WHITE PAPER

Factorized Power Architecture and VI Chips

Flexible, High Performance Power System Solutions

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Introduction

As electronic systems continue to trend toward lower voltages with higher currents and as the speed of contemporary loads – such as state-of-the-art processors and memory – continues to increase, the power systems designer is challenged to provide small, cost effective and efficient solutions that offer the requisite performance. Traditional power architectures cannot, in the long run, provide the required performance. Vicor's new Factorized Power Architecture™ (FPA), and its new families of integrated power components, called VI Chips, provides a revolutionary new and optimal power conversion solution that addresses the challenge in every respect.

The Architectural Problems of Power Conversion

With each new generation of processor, memory, DSP and ASIC, the trend is toward lower voltages, higher currents, higher speeds and more on-board voltages. System designers are challenged to contend with a proliferation of lower voltages; provide ever-faster transient response; improve overall power system efficiency; and do it all using less board area.

Historically, a variety of power systems architectures have been adopted as solutions. Principal among them have been Centralized Power Architecture (CPA), Distributed Power Architecture (DPA) and Intermediate Bus Architecture (IBA).

CPA, one of the oldest power systems architectures, generates all system voltages at a central location and distributes them to load locations via distribution buses. This can be effective if the voltages are high and the currents low or if the distances between the power supply and the loads are small. However, for low voltages and widely distributed loads, the problem of distribution losses becomes unmanageable as distribution power loss increases, due to the rising current (as power loss = I^2R). The bus cross-section would have to increase as the square of the reduction in the voltage in order to maintain constant distribution efficiency – an impractical solution in today's complex, low-voltage systems.

The introduction in the early 1980s of modular, high-density power converters, enabled the migration to DPA and overcame some of the problems of CPA. The "bricks" of DPA deliver all of the functions of a classic DC-DC converter – isolation, voltage transformation and regulation – at the point of load. As on-board voltages proliferated, however, DPA solutions required increasing numbers of bricks, thereby exacting a penalty in terms of board space and cost. Furthermore, typical DPA brick topologies are inadequate for the transient response requirements of today's fast loads.

Factorized Power Architecture (FPA): Solving the Contemporary Power Conversion Problem

FPA uses Vicor's power architecture research, and ASIC-based product development strategy. The enabling components are integrated power components called 'VI Chips' which set new standards in terms of density, efficiency, responsiveness and system cost and offer the power architect entirely new ways to solve power problems. The name 'VI Chips' comes from their ability to multiply currents and divide voltages while preserving the VI power product (the "•") essentially constant.

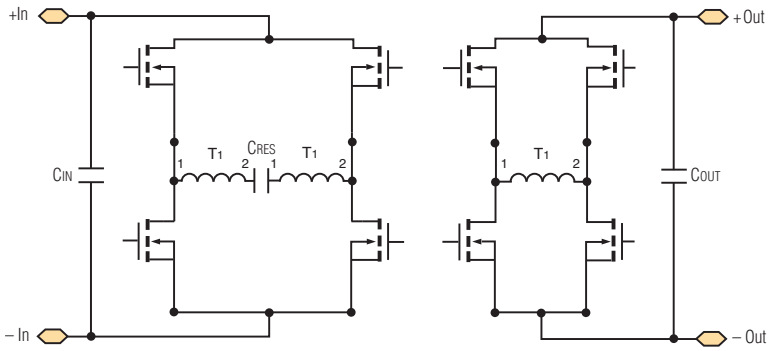
Voltage Transformation Module (VTM): Sine Amplitude Converter

The VTM® (Fig. 1) — the building blocks of FPA — is a wide voltage range input, high efficiency voltage transformation unit using a proprietary Zero Current Switching-Zero Voltage Switching (ZCS-ZVS) Sine Amplitude Converter™ (SAC™).

Figure 1
Photo of Voltage Transfomation Module

A simplified schematic of a Sine Amplitude Converter is shown in Fig. 2. The power train is a low-charge (Q), high-frequency controlled oscillator, with high spectral purity and common-mode symmetry, resulting in essentially noise-free operation. The control architecture locks the operating frequency to the power train resonant frequency, optimizing efficiency and minimizing output impedance by effectively canceling reactive components. R_{OUT} can be as low as 0.8 milliohm from a single VTM. If that is not low enough, or if more power is required, VTMs can be paralleled with accurate current sharing. Quiet and powerful, the SAC-based VTM can be considered as a linear voltage / current converter with a flat output impedance up to about 1 MHz.

Figure 2
Simplified schematic of the Sine Amplitude Converter



The secondary current in a SAC VTM® is basically a pure sinusoid. Selected SAC VTM operating waveforms (Fig. 3) show the purity, low output impedance and fast response of a typical VTM. Note also that the time scale in Fig. 4a is only 200 nanoseconds per division and that the waveform in Fig. 4a is with no external output capacitance across the load. The very low, non-inductive output impedance of the VTM allows an almost instantaneous response to the 100% step change in load current of Fig. 4b. Because there is no internal regulation circuitry in a VTM, and none of the attendant loop delays or stability issues, no internal control action is required to respond to the change in load. The internal ASIC controller simply continues its function of controlling and synchronizing the operation of the switches to maintain operation at resonance.

Figure 3
Selected SAC VTM waveforms

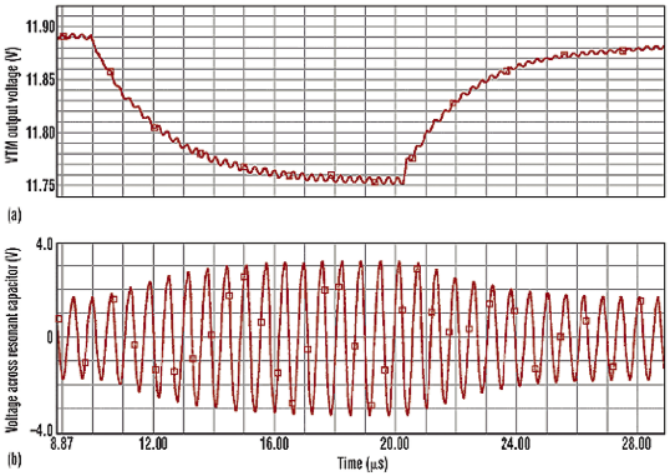
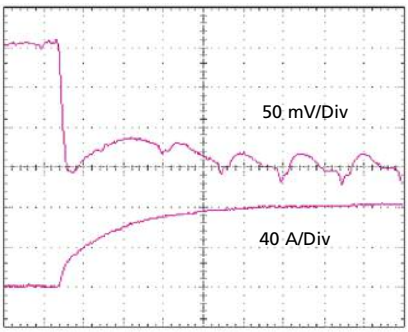
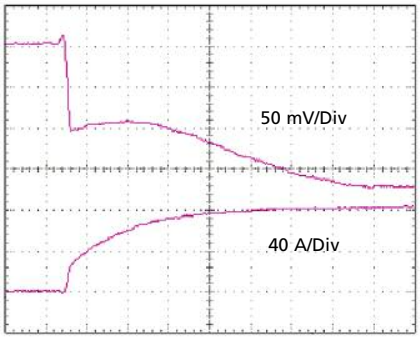


Figure 4a
VTM dynamic response



0 – 80 A Load step with NO output capacitance

Figure 4b



0 – 80 A Load step with 100 µF output capacitance

The VTM – transformation and isolation

The VTM offers speed, density and efficiency levels designed to meet the demands of DSP, FPGA, ASIC, processor cores and microprocessor applications at the point of load while providing isolation from input to output. Its response time is less than 1 µs, and it delivers up to 100 A with very high efficiency.

The VTM® can be considered a fixed-ratio DC-DC transformer with the following capabilities:

- input range compatible with 48 V and 24 V PRMs;
- power up to 400 W or 100 A;
- power density up to 1,095 W/in^3;
- efficiency up to 97%;
- isolation to 2,250 Vdc in 1.1 in^2 package;
- low power dissipation at point-of-load;
- low output impedance enabling fast transient response.

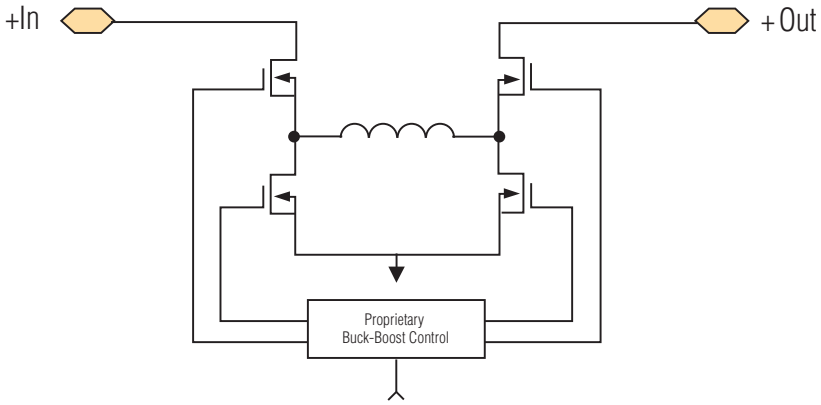
For DC-DC power conversion, the VTM is designed to operate with the PRM (see next section), which provides soft start, regulation, and the initial Vcc pulse at start up. This pulse is received through the VTM control (VC) pin. Standalone VTM operation is possible if a Vcc is available see Application Note AN:007 "Using VTMs as 26-55 V Input Bus Converter..

Pre-Regulator Module (PRM): An efficient buck-boost

The PRM® shown in Fig. 5 uses a patented ZVS Buck-Boost Regulator control architecture (see Fig. 6) to give high efficiency step-up / step-down voltage regulation. Efficiency is maximized when the output voltage is close to the input voltage. The PRM operates at a typical fixed operating frequency of 1 MHz (1.5 MHz max.). Like VTMs, PRMs may be paralleled to achieve increased output power. A unique feature of the PRM control architecture is that the switching sequence does not change in either buck or boost mode – only the relative duration of phases within an operating cycle need be controlled.

Figure 5
Photo of Pre-Regulator Module

Figure 6
Simplified PRM schematic



The PRM® provides a regulated output voltage – a 'factorized bus' – from an unregulated input source. The combination of the PRM and VTM® creates an isolated, regulated DC-DC converter. PRMs can also be used stand alone as non-isolated voltage regulators. The PRM has the following attributes:

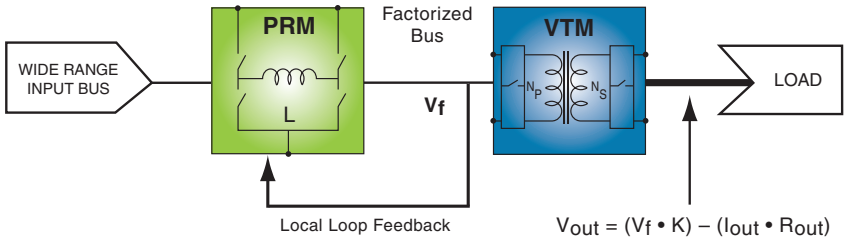
- input ranges of 18-36 V and 36-75 V
- power up to 320 W
- power density up to 1100 W/in^3
- efficiency up to 97%
- 1.5 MHz switching frequency
- up to 125°C operation

PRM+VTM architectures and applications

The PRM control system and supporting ASICs enable the VTM output voltage to be controlled using a choice of methods.

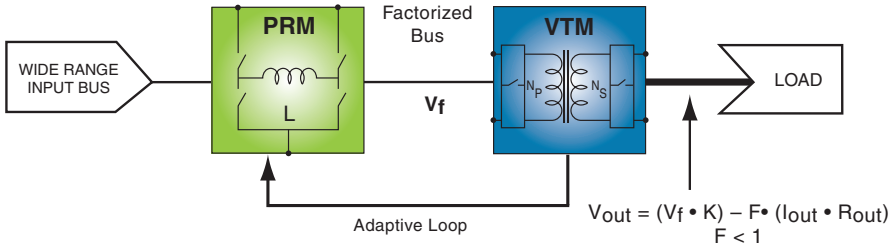
Local loop control is the simplest control scheme. Under local loop control, illustrated in Fig. 7, the PRM senses its own output voltage and regulates the Factorized Bus Voltage to a constant value. Load voltage will exhibit a "droop" proportional to the VTM output resistance.

Figure 7
FPA with local loop control



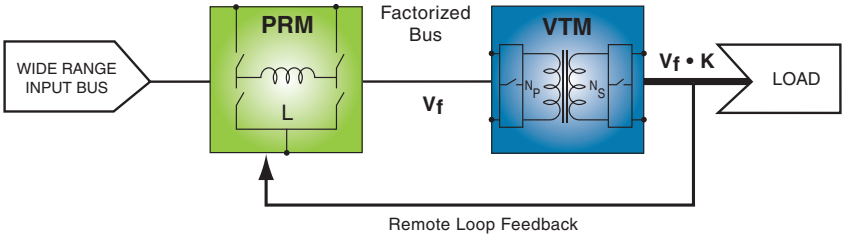
Under adaptive loop control, illustrated in Fig. 8, the VTM sends a signal back to the PRM to enable the PRM to adjust the Factorized Bus Voltage to compensate for the VTM output resistance. Adaptive loop control provides improved regulation over the simple local loop control – within +/- 1% – yet requires only a simple, non-isolated, feedback connection between the VTM and PRM.

Figure 8
FPA with adaptive loop control



Under remote loop control, illustrated in Fig. 9, the voltage at the load is sensed and fed back to the PRM. This feedback protocol provides the most accurate load regulation – within +/- 0.2% – but may require isolation in the feedback path.

Figure 9
FPA with remote loop control



With the addition of a (PI1004) Picor point-of-load IC, remote loop control can incorporate a digital control option compatible with the latest processor VID specifications.

Bus Converter Module (BCM): Intermediate Bus Conversion

The BCM® (Fig. 10), also a Sine Amplitude Converter, provides an isolated intermediate bus voltage to power non-isolated POL converters from a narrow-input-range DC source to maximize power conversion. The BCM functions as a fixed-ratio DC-DC transformer, with the following characteristics:

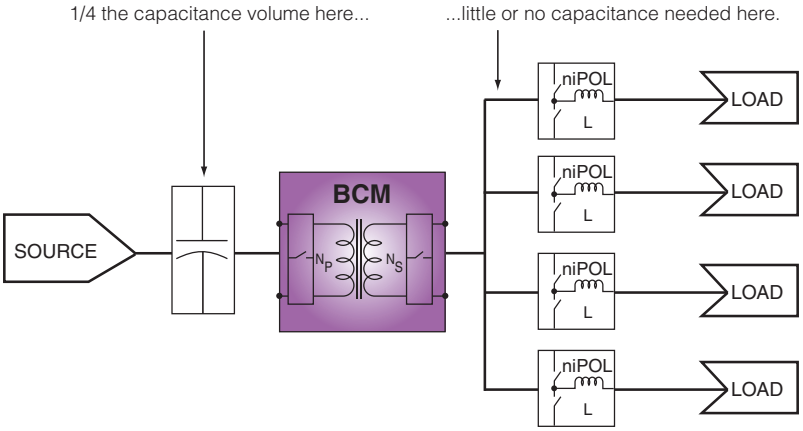
- 48 V and high voltage input ranges;
- power up to 300 W or 100 A;
- power density up to 1,036 W/in^3;
- efficiency up to 97%;
- lightweight at 0.4 ounces (12 grams);
- isolation to 4,242 Vdc in a 1.1 in^2 package.

Figure 10
Photo of Bus Converter Module

The BCM may be used to power non-isolated POL converters or as an independent DC source. Due to its fast response time and low noise, the need for limited life aluminum electrolytic or tantalum capacitors load is reduced – or eliminated – resulting in savings of board area, materials and total system cost. BCMs inherently support current-sharing, which allows parallel operation without additional control circuitry or interconnects.

High-power density BCMs that minimize total system capacitance when used as a bus converter enable dense IBA systems (see Fig. 11). For more information on using BCMs for IBA, see Application Note AN:001 "Configuring BCMs for Low Power NiPOLs.

Figure 11
Bus conversion using BCMs



BCMs are also available with high voltage (352 V, 384 V) input capabilities for high density DC-DC conversion, typically following a PFC stage in offline AC-DC conversion down to 48 V or 12 V.

Using FPA: Why Factorize?

Small size—more power in less space

VI Chips are the smallest power components available today — about the size of a 1/16 brick — and very power dense. They can be used as building blocks to replace existing circuits (quarter bricks and silver box power supplies). Factorized Power means more space at the point(s) of load: one-half the power dissipation and the regulation function can be remotely located.

Flexibility — more options for designing a power system

One of the key objectives of factorized power and VI Chips is to increase power system flexibility. In DPA, DC-DC converters bundle the three classic converter functions (isolation, transformation and regulation) into bricks that are no longer adequate in terms of performance or cost-effectiveness. In IBA, non-isolated POL converters forego isolation and high-ratio voltage transformation to improve cost-effectiveness. But they depend upon a nearby bus converter to supply power at a low input voltage and expose over-voltage sensitive loads to deadly faults and ground loops.

Families of VI Chip® BCMs, VTMs and PRMs, optimized for different nominal input and output voltages, and packaged for power capabilities, provide power systems designers with a stable of power conversion components that can be used to economically solve a virtually limitless variety of power conversion problems. Complex systems can use combinations of VI Chips in a variety of control modes to rapidly configure high-density, low-profile solutions that minimize the need for external components, are cost-effective and highly efficient, and provide state-of-the-art performance.

VI Chips provide isolation and regulation where they are needed. You can put the VTM® at the point of load and the PRM® alongside—or remotely, in the backplane or on a daughtercard.

FPA systems with a multiplicity of input and output voltages may actually have fewer unique components compared to a brick-based equivalent. With the VTM® you use the same device no matter what the input voltage; with the PRM® you use the same device no matter what the output voltage. There's a continuum of output voltages available.

You can design new systems with PRMs and VTMs or retrofit existing architectures. Figs. 12, 13 and 14 illustrate a few of the design options.

Figure 12
High-current, low-voltage supply

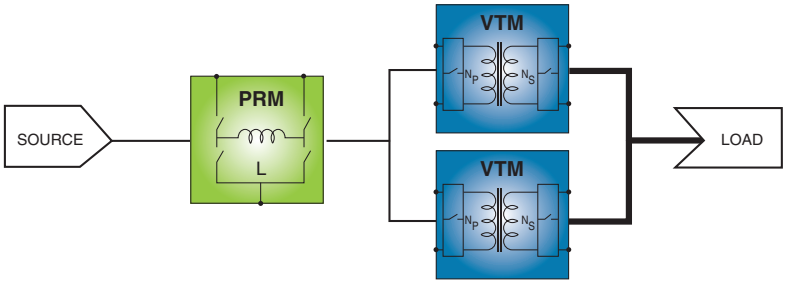


Figure 13
High-voltage outputs

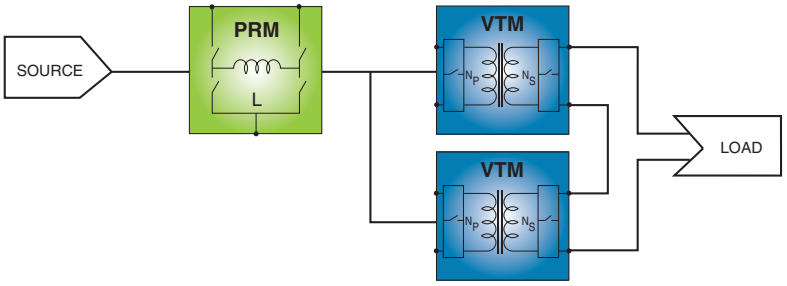
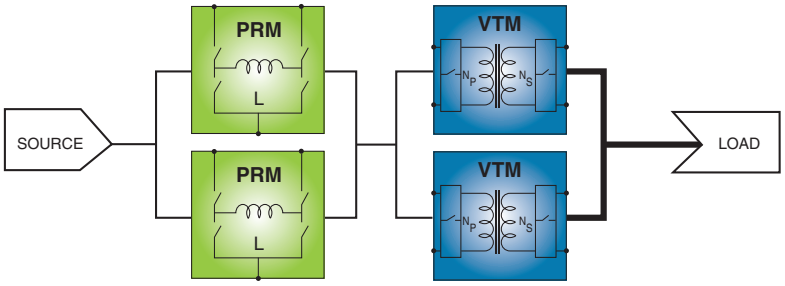


Figure 14
High-power arrays



Efficiency—more power for the load, less heat left behind

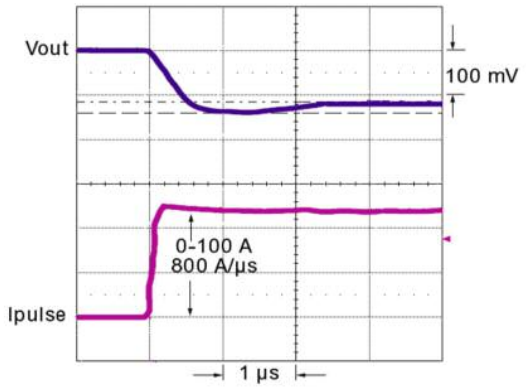
Both the PRM and VTM can achieve higher than 97% efficiency. Overall efficiency for a power system – including the combination of a PRM and a VTM – operating from an unregulated DC source and supplying a low-voltage DC output typically ranges from 90% to 95%. In many cases, it is possible to achieve overall efficiency exceeding 95% even at full load. With higher efficiency comes lower total heat dissipation, another important consideration in power systems design.

VI Chips offer flexible thermal management: a low thermal impedance package and the design of the VI Chip package simplifies heat sink design.

Fast Transient Response—providing more power for fast changing loads

Many of today's loads require not only higher current but faster transient response. VTMs respond to load changes, regardless of magnitude, in less than one microsecond with an effective switching frequency of 3.5 MHz. This is 20 times faster than the fastest competitive brick. (see Fig. 15).

Figure 15
Fast transient response



The VTM's high bandwidth obsoletes the need for massive point-of-load bypass capacitance. Even without any external output capacitors, the output of a VTM® exhibits a limited voltage perturbation in response to a sudden power surge. A minimal amount of external bypass capacitance, in the form of low ESR/ESL ceramic capacitors, suffices to eliminate any transient voltage overshoot.

From Bricks and niPOLs to VI Chips

IBA has proven effective as an interim method of containing power system cost while addressing the trend toward a proliferation of lower load voltages. IBA relies on non-isolated point-of-load regulators (niPOLs), reducing the POL function to regulation and transformation. The niPOLs operate from an intermediate bus voltage provided by upstream isolated converters. However, traditional IBA has inherent limitations that require tradeoffs between distribution and conversion loss and that limit responsiveness to rapid load changes.

Conclusion

FPA and VI Chips offer a power conversion architecture and enabling power building blocks that overcome these limitations while providing higher performance in every critical system specification. Factorized power, in fact, maximizes the competitiveness of a power system by providing the highest degree of system flexibility, power density, conversion efficiency, transient responsiveness, noise performance, and field reliability.

For more information about FPA, VI Chips and associated products, please visit the - Vicor web site at: vicorpower.com.