UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/286,542	11/14/2017	9819263	TWT04774/US	1984

60589 7590 10/25/2017

JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jian-Hong ZENG, Taoyuan City, TAIWAN;
DELTA ELECTRONICS, INC., Taoyuan City, TAIWAN;
Shou-Yu HONG, Taoyuan City, TAIWAN;
Xiao-Ni XIN, Taoyuan City, TAIWAN;
Pei-Qing HU, Taoyuan City, TAIWAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60589 7590 09/22/2017
JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/286,542	10/05/2016	Jian-Hong ZENG	TWT04774/US	1984

TITLE OF INVENTION: POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/22/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
PIZZUTO, CHARLES M	2847	361-749000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 CKC & PARTNERS CO., LTD.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: DELTA ELECTRONICS, INC.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): TAOYUAN CITY, TAIWAN

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 504669 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /James Lynn O'Sullivan/ Date 2017-10-17
Typed or printed name James Lynn O'Sullivan Registration No. 65618

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Electronic Patent Application Fee Transmittal

Application Number:	15286542
Filing Date:	05-Oct-2016
Title of Invention:	POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jian-Hong ZENG
Filer:	James Lynn O'Sullivan/Anny TENG
Attorney Docket Number:	TWT04774/US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**960**

Electronic Acknowledgement Receipt	
EFS ID:	30672847
Application Number:	15286542
International Application Number:	
Confirmation Number:	1984
Title of Invention:	POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jian-Hong ZENG
Customer Number:	60589
Filer:	James Lynn O'Sullivan/Anny TENG
Filer Authorized By:	James Lynn O'Sullivan
Attorney Docket Number:	TWT04774/US
Receipt Date:	16-OCT-2017
Filing Date:	05-OCT-2016
Time Stamp:	23:21:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$960
RAM confirmation Number	101717INTEFSW00010164504669
Deposit Account	504669
Authorized User	Candy CHEN
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	TWT04774US-FeeTransmittal-20171017.pdf	239723 bdfa738c95f95168c94954f1fee8525afc01a81b	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30675 a34727600b6aefc346f6d192d6ac959c75cbda14	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	270398		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60589 7590 09/22/2017

JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

EXAMINER
PIZZUTO, CHARLES M

ART UNIT	PAPER NUMBER
2847	

DATE MAILED: 09/22/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/286,542	10/05/2016	Jian-Hong ZENG	TWT04774/US	1984

TITLE OF INVENTION: POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/22/2017

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60589 7590 09/22/2017
JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/286,542	10/05/2016	Jian-Hong ZENG	TWT04774/US	1984

TITLE OF INVENTION: POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	12/22/2017

EXAMINER	ART UNIT	CLASS-SUBCLASS
PIZZUTO, CHARLES M	2847	361-749000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
❑ Issue Fee
❑ Publication Fee (No small entity discount permitted)
❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
❑ A check is enclosed.
❑ Payment by credit card. Form PTO-2038 is attached.
❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
❑ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/286,542	10/05/2016	Jian-Hong ZENG	TWT04774/US	1984

60589 7590 09/22/2017

JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

EXAMINER	
PIZZUTO, CHARLES M	
ART UNIT	PAPER NUMBER
2847	

DATE MAILED: 09/22/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/286,542	Applicant(s) ZENG ET AL.	
	Examiner Charles Pizzuto	Art Unit 2847	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Application filed on 10/05/2016*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-24*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☒ All b) ☐ Some *c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/Charles Pizzuto/
Examiner, Art Unit 2847

DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Allowable Subject Matter

Claims 1-24 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art taken either singularity or in combination fails to anticipate or fairly suggest the limitations of the independent claim, in such a manner that a rejection under 35 U.S.C. 102 or 103 would be improper.

The prior art fails to teach a combination of all the claimed features as presented in independent claim 1 with the allowable features being:

> a power converter, comprising: a carrier, comprising: an upper surface; and a lower surface; a first electronic component disposed at the lower surface of the carrier; a second electronic component disposed at the upper surface of the carrier; and a first connection part, comprising: a first terminal electrically coupled to the upper surface or the lower surface of the carrier; and a second terminal attached to a surface of the first electronic component apart from the carrier,

wherein the second terminal of the first connection part is a bonding pad; wherein the carrier is disposed at 1/3 to 2/3 of a height of the power converter

Therefore **claim 1 is allowed**.

Claims 2-11 are allowed as being dependent on an allowable independent claim 1.

The prior art fails to teach a combination of all the claimed features as presented in independent claim 12 with the allowable features being:

method for manufacturing a power converter, comprising: … connecting the first electronic component at a lower surface of a carrier; and bonding a second electronic component at an upper surface of the carrier to form the power converter, wherein the carrier is disposed at 1/3 to 2/3 of a height of the power converter

Therefore **claim 12 is allowed.**

Claims 13-24 are allowed as being dependent on an allowable independent claim 12.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Pizzuto whose telephone number is (571)270-7887. The examiner can normally be reached on M,Tu,Th,F 9-5 (EST).

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Thompson can be reached on 571-272-2342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Charles Pizzuto/

Examiner, Art Unit 2847

/TIMOTHY THOMPSON/

Supervisory Patent Examiner, Art Unit 2847

Notice of References Cited	Application/Control No. 15/286,542	Applicant(s)/Patent Under Reexamination ZENG ET AL.	
	Examiner Charles Pizzuto	Art Unit 2847	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2009/0175014 A1	07-2009	Zeng; JIAN-HONG	H05K1/141	361/782
*	B	US-2014/0085848 A1	03-2014	Zeng; Jian-Hong	H05K1/141	361/768
*	C	US-9,030,027 B2	05-2015	Zeng; Jian-Hong	H05K1/141	257/777
*	D	US-2016/0366780 A1	12-2016	Liang; Le	H02M3/04	1/1
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15286542	ZENG ET AL.
	Examiner	Art Unit
	CHARLES PIZZUTO	2847

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	08/25/2017								
1	1	=								
2	2	=								
3	3	=								
4	4	=								
5	5	=								
6	6	=								
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22	22	=								
23	23	=								
24	24	=								

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15286542	ZENG ET AL.
	Examiner	**Art Unit**
	CHARLES PIZZUTO	2847

CPC						
Symbol					**Type**	**Version**
H02M		3	/	156	F	2013-01-01
H01F		27	/	24	I	2013-01-01
H01F		27	/	28	I	2013-01-01
H05K		1	/	028	I	2013-01-01
H05K		1	/	111	I	2013-01-01
H05K		1	/	181	I	2013-01-01
H05K		3	/	22	I	2013-01-01
H05K		3	/	305	I	2013-01-01
H05K		3	/	4038	I	2013-01-01
H05K		2201	/	1003	A	2013-01-01
H05K		2203	/	02	A	2013-01-01
H05K		2203	/	0228	A	2013-01-01
H05K		1	/	145	A	2013-01-01
H05K		1	/	147	A	2013-01-01
H05K		1	/	18	I	2013-01-01
H05K		2201	/	10946	A	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

/CHARLES PIZZUTO/ Examiner.Art Unit 2847	08/25/2017	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	24	
/TIMOTHY THOMPSON/ Supervisory Patent Examiner.Art Unit 2847	09/17/2017	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1, 12	1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15286542	ZENG ET AL.
	Examiner	Art Unit
	CHARLES PIZZUTO	2847

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION		
CLASS	SUBCLASS	CLAIMED		NON-CLAIMED
361	749	H 0 2 M 3 / 156 (2006.01.01)		
CROSS REFERENCE(S)		H 0 5 K 1 / 02 (2006.01.01)		
		H 0 5 K 1 / 18 (2006.01.01)		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)	H 0 5 K 3 / 22 (2006.01.01)		
		H 0 1 F 27 / 24 (2006.01.01)		
		H 0 5 K 3 / 30 (2006.01.01)		
		H 0 5 K 1 / 11 (2006.01.01)		
		H 0 1 F 27 / 28 (2006.01.01)		
		H 0 5 K 3 / 40 (2006.01.01)		

/CHARLES PIZZUTO/ Examiner.Art Unit 2847 (Assistant Examiner)	08/25/2017 (Date)	**Total Claims Allowed:** 24
/TIMOTHY THOMPSON/ Supervisory Patent Examiner.Art Unit 2847 (Primary Examiner)	09/17/2017 (Date)	O.G. Print Claim(s) 1, 12 O.G. Print Figure 1

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15286542	ZENG ET AL.
	Examiner	**Art Unit**
	CHARLES PIZZUTO	2847

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17												
2	2	18	18												
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16	16														

/CHARLES PIZZUTO/ Examiner.Art Unit 2847 (Assistant Examiner)	08/25/2017 (Date)	**Total Claims Allowed:** 24	
/TIMOTHY THOMPSON/ Supervisory Patent Examiner.Art Unit 2847 (Primary Examiner)	09/17/2017 (Date)	O.G. Print Claim(s) 1, 12	O.G. Print Figure 1

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15286542	ZENG ET AL.
	Examiner	Art Unit
	CHARLES PIZZUTO	2847

CPC- SEARCHED		
Symbol	Date	Examiner
H01F27/24	8/28/2017	cp
H01F27/28	8/28/2017	cp
H02M3/156	8/28/2017	cp
H05K1/111	8/28/2017	cp
H05K1/18	8/28/2017	cp
H05K1/181	8/28/2017	cp
H05K3/22	8/28/2017	cp
H05K3/4038	8/28/2017	cp
H05K1/028	8/28/2017	cp

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
361	749	8/28/2017	cp

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
IDS items searched	8/28/2017	cp
Double Patenting searched	8/28/2017	cp
Inventors' names searched	8/28/2017	cp
Assignee searched	8/28/2017	cp
Reference Manager items searched	8/28/2017	cp
Prior Art supplied by applicant searched	8/28/2017	cp
Keywords searched	8/28/2017	cp

/CHARLES PIZZUTO/ Examiner.Art Unit 2847	

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
NPL - InnovationQ NPL searched	8/28/2017	cp
Classifications with text modification searched	8/28/2017	cp

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
361	749	8/28/2017	cp
H01F	27/24	8/28/2017	cp
H01F	27/28	8/28/2017	cp
H02M	3/156	8/28/2017	cp
H05K	1/028	8/28/2017	cp
H05K	1/111	8/28/2017	cp
H05K	1/18	8/28/2017	cp
H05K	1/181	8/28/2017	cp
H05K	3/22	8/28/2017	cp
H05K	3/4038	8/28/2017	cp

/CHARLES PIZZUTO/ Examiner.Art Unit 2847	

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BIB DATA SHEET

CONFIRMATION NO. 1984

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/286,542	10/05/2016	361	2847	TWT04774/US

APPLICANTS
DELTA ELECTRONICS, INC., Taoyuan City, TAIWAN;

INVENTORS
Jian-Hong ZENG, Taoyuan City, TAIWAN;
Shou-Yu HONG, Taoyuan City, TAIWAN;
Xiao-Ni XIN, Taoyuan City, TAIWAN;
Pei-Qing HU, Taoyuan City, TAIWAN;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************
CHINA 201510648280.1 10/09/2015

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
10/18/2016

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /CHARLES M PIZZUTO/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		TAIWAN	20	24	2

ADDRESS

JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

TITLE

POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME

FILING FEE RECEIVED		
1920	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	
Filing Date	2016-10-05
First Named Inventor	Jian-Hong ZENG
Art Unit	
Examiner Name	
Attorney Docket Number	TWT04774/US

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/C.P./	1	203057001	CN	U	2013-07-10	TOSHIBA LIGHTING & TECHNOLOGY		
/C.P./	2	201330190	TW	A	2013-07-16	INTERSIL INC		
/C.P./	3	242820	TW	B	2005-11-01	SILICONWARE PREC IND CO LTD		

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	2016-10-05
	First Named Inventor	Jian-Hong ZENG
	Art Unit	
	Examiner Name	
	Attorney Docket Number	TWT04774/US

/C.P./	4	471357	TW	B	2015-02-01	DSM IP ASSETS BV		
/C.P./	5	412655	TW	B	2013-10-21	TAKIGEN MFG CO		

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
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EXAMINER SIGNATURE

Examiner Signature	/CHARLES PIZZUTO/	Date Considered	08/25/2017

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	2016-10-05
	First Named Inventor	Jian-Hong ZENG
	Art Unit	
	Examiner Name	
	Attorney Docket Number	TWT04774/US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/James Lynn O'Sullivan/	Date (YYYY-MM-DD)	2016-10-05
Name/Print	James Lynn O'Sullivan	Registration Number	65618

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/286,542	10/05/2016	Jian-Hong ZENG	TWT04774/US

CONFIRMATION NO. 1984

60589
JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

PUBLICATION NOTICE

OC000000090605939

Title:POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME

Publication No.US-2017-0104410-A1
Publication Date:04/13/2017

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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证　明

本证明之附件是向本局提交的下列专利申请文件副本。

申　　请　　号：201510648280.1

申　请　类　型：发明专利

发明 创造 名称：电源变换器及其制造方法

申　　请　　日：2015 年 10 月 09 日

申　　请　　人：台达电子工业股份有限公司

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权 利 要 求 书 155162CN01

1.一电源变换器，包含：

一载具，包含上表面和下表面；

一第一电子元器件，配置于所述载具的下表面；

一第二电子元器件，配置于所述载具的上表面；以及

一第一连接部，包含：

一第一端，电性耦接于所述载具的上表面或下表面；以及

一第二端，为一焊垫结构，贴合于所述第一电子元器件的远离所述载具的表面；

其中所述载具配置于电源变换器高度的 1/3 至 2/3 处，所述第一连接部以所述第一电子元器件作为机械支撑而制成。

2.如权利要求 1 所述的电源变换器，还包含多个第一电子元器件与多个第二电子元器件，所述多个第一电子元器件中的最高者与所述下表面的垂直高度为一第一高度，所述多个第二电子元器件中的最高者与所述上表面的垂直高度为一第二高度，所述第一高度、所述第二高度与所述载具的厚度的和为所述电源变换器高度。

3.如权利要求 1 所述的电源变换器，其中所述第一电子元器件的高度等于所述第二电子元器件的高度。

4. 如权利要求 2 所述的电源变换器，其中所述第二高度不大于两倍的所述第一高度，或所述第一高度不大于两倍的所述第二高度。

5. 如权利要求 1 所述的电源变换器，其中所述第一连接部与所述载具的连接采用 SMT 方式或直插方式。

6. 如权利要求 1 所述的电源变换器，其中所述第一电子元器件、所述第二电子元器件及所述载具共同形成一电感元件，所述第一电子元器件与所述第二电子元器件分别为所述电感元件的铁芯的一部分。

7. 如权利要求 6 所述的电源变换器，还包含：一第三电子元器件和一第四电子元器件，分别配置于所述载具的下表面和上表面，其中所述第三电子元器件、所述第四电子元器件及所述载具共同形成一变压器，所述第三电子元器件与所述第四电子元器件分别为所述变压器铁芯的一部分。

8. 如权利要求 1 所述的电源变换器，其中所述第一电子元器件、所述第二电子元器件及所述载具共同形成一变压器，所述第一电子元器件与所述第二电子元器件分别为所述变压器铁芯的一部分。

9. 如权利要求 1 所述的电源变换器，其中所述电源变换器还包含一直插接脚，安装于所述第一连接部的第二端，用以将焊垫连接方式转换为直插连接方式。

10. 如权利要求 9 所述的电源变换器，还包含多个第一连接部，每个第一连接部的第二端一一对应所述直插接脚，透过一支架来固定所述直插接脚。

11. 如权利要求 10 所述的电源变换器，还包含一粘结层，用以粘合所述第一电子元器件与所述支架。

12. 如权利要求 10 所述的电源变换器，其中，所述第一连接部采用引线框架制作而成。

13. 如权利要求 1 所述的电源变换器，还包含：

一芯片，配置于所述第一电子元器件的远离所述载具的表面，所述芯片表面设有一个或多个接脚。

14. 如权利要求 1 所述的电源变换器，还包含：

一软性印刷电路板，配置于所述第一连接部的外侧，所述软性印刷电路板的一端连接所述载具，另一端连接所述第一连接部的第二端。

15. 如权利要求 1 所述的电源变换器，还包含内嵌于所述载具中的至少一电子元件。

16. 如权利要求 1 所述的电源变换器，其中，所述载具为一印刷电路板。

17. 一种电源变换器的制造方法，其特征在于，该制造方法包含以下步骤：

粘着一第一电子元器件于一引线框架上，其中所述引线框架包含一固持部及一连接部；

切除所述引线框架的所述固持部；

以所述第一电子元器件作为机械支撑而弯曲所述连接部，使所述连接部固定于所述第一电子元器件；

连接所述第一电子元器件于一载具的下表面；

粘着一第二电子元器件于所述载具的上表面，以形成一电源变换器，其中所述载具配置于所述电源变换器高度的 1/3 至 2/3 处。

18. 如权利要求 17 所述的制造方法，其中所述连接部透过粘着剂以直接与所述第一电子元器件进行粘着。

19. 如权利要求 17 所述的制造方法，还包含：

将所述连接部穿透所述载具，并连接至所述第二电子元器件。

20. 如权利要求 19 所述的制造方法，其中将所述连接部穿透所述载具的步骤包含：

在所述载具上开一孔洞，以使所述连接部透过所述孔洞而穿透所述载具；

在所述载具的所述孔洞上放置一锡块；以及

以波峰焊或回流焊的方式使所述锡块填满所述孔洞。

21. 如权利要求 17 所述的制造方法，其中所述第一电子元器件、所述第二电子元器件及所述载具共同形成一电感元件，所述第一电子元器件与所述第二电子元器件分别为所述电感元件的铁芯的一部分。

22. 如权利要求 17 所述的制造方法，其中所述第一电子元器件、所述第二电子元器件及所述载具共同形成一变压器，所述第一电子元器件与所述第二电子元器件分别为所述变压器的铁芯的一部分。

23. 如权利要求 17 所述的制造方法，所述连接部包含一第一端和一第二端，所述制造方法还包含：

粘着一直插接脚于所述连接部的第二端。

24. 如权利要求 17 所述的制造方法，其中所述第一电子元器件包含一第一表面及一第二表面，所述制造方法还包含：

粘着所述第一电子元器件的第一表面于所述载具的下表面；

透过胶水配置一芯片于所述第一电子元器件的第二表面；以及

设置一个或多个接脚于所述芯片的表面。

25. 如权利要求 17 所述的制造方法，所述连接部包含一第一端和一第二端，所述制造方法还包含：

配置一软性印刷电路板以连接所述载具与所述连接部的第二端。

26. 如权利要求 17 所述的制造方法，还包含：

对所述电源变换器进行一模造制程；以及

对所述电源变换器上的模造材料进行打磨制程，直到所述电源变换器的部分结构外露为止。

27. 如权利要求 17 所述的制造方法，其中，所述第一电子元器件为一磁性元件，所述制造方法还包含：

涂布胶水于所述磁性元件和所述载具的连接位置；

提供一电磁吸盘于所述磁性元件的远离所述载具的表面；

通过所述电磁吸盘产生的粘力吸合所述磁性元件和所述连接部；以及

加温固化所涂布的胶水，以定位所述磁性元件与所述载具。

28. 如权利要求 27 所述的制造方法，还包含：

对所述电源变换器进行一模造制程；以及

对所述电源变换器上的模造材料进行打磨制程，以裸露所述第二电子元器件和/或所述第一电子元器件。

29. 如权利要求 27 所述的制造方法，还包含：

对所述电源变换器进行一模造制程；以及

对所述电源变换器上的模造材料进行打磨制程，以裸露所述连接部的外侧。

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说　　明　　书　　155162CN01

电源变换器及其制造方法

技术领域

本发明涉及电源转换技术领域，特别涉及一种电源变换器及其制造方法。

背景技术

随着智能生活科技的进展，数据处理的需求也日益增加。平均每年全球在数据处理上的能耗，达到数千亿甚至数万亿度，此外，一个大型数据中心的占地面积往往高达数万平方米。因此，高效率和高功率密度成为产业永续发展的关键指标。

数据中心的运行关键是服务器，其主机板通常由 CPU、Chipsets、存储器等等数据处理芯片和它们的供电电源及必要周边元件组成。芯片的供电需求为电压低、电流大的电源，因此，为减少输出引线的损耗和阻抗影响，需要直接为芯片供电的电源，而这些电源被称为负载点(Point of the Load, POL)。

根据系统架构的不同，POL 的输入有 12V、48V 甚至 400V 不等。由于 POL 电压低、电流大的特性，其脚位(Pin)的体积和阻抗，对 POL 电源的功率密度和效率会有非常直接的影响。因此，如何设计脚位是此类电源变换器的关键之一。若以适用范围广为考量来设计脚位，则电源变换器的体积较大、成本较高，且电能损耗较大。若以电源变换器的体积小、成本低及损耗低为考量来设计脚位，则其适用范围较窄。

由此可见，上述现有的方式，显然仍存在不便与缺陷，而有待改进。为了解决上述问题，相关领域莫不费尽心思来谋求解决之道，但长久以来仍未发展出适当的解决方案。

发明内容

本发明内容的目的之一是提供一种电源变换器及其制造方法，藉以改善先前技术的问题。

为达上述目的，根据本发明的一个方面，提供了一种电源变换器。此电源变换器包含载具、第一电子元器件、第二电子元器件及第一连接部。上述载具包含上表面及下表面，第一连接部包含第一端及第二端。多个第一电子元器件配置于载具的下表面，多个第二电子元器件配置于载具的上表面。第一连接部的第一端电性耦接于载具的上表面或下表面。第一连接部的第二端为一焊垫结构贴合于第一电子元器件的远离载具表面，上述载具配置于电源变换器高度的 1/3 至 2/3 处。第一连接部是以多个第一电子元器件作为机械支撑而制成。

为达上述目的，根据本发明的另一个方面，提供了一种电源变换器的制造方法包含以下步骤：粘着第一电子元器件于引线框架上，其中引线框架包含固持部及连接部；切除引线框架的固持部；以第一电子元器件作为机械支撑而弯曲连接部，使连接部固定于第一电子元器件；粘着第一电子元器件于载具的下表面；粘着第二电子元器件于载具的上表面，以形成电源变换器，其中载具配置于电源变换器高度的 1/3 至 2/3 处。

因此，根据本发明实施例的技术内容，通过提供一种电源变换器及其制造方法，藉以改善电源变换器的脚位设计无法兼顾适用范围广及体积小、成本低及损耗低的问题。

在参阅下文实施方式后，本领域的技术人员当可轻易了解本发明的基本精神及其他发明目的，以及本发明所采用的技术手段与实施态样。

附图说明

为让本发明的上述和其他目的、特征、优点与实施例能更明显易懂，所附图式的说明如下：

图 1 是根据本发明一实施例绘示一种电源变换器的示意图。

图 2 是根据本发明另一实施例绘示一种电源变换器的示意图。

图 3 是根据本发明再一实施例绘示一种电源变换器的示意图。

图 4 是根据本发明又一实施例绘示一种电源变换器的示意图。

图 5 是根据本发明另一实施例绘示一种电源变换器的示意图。

图 6 是根据本发明再一实施例绘示一种电源变换器的示意图。

图 7 是根据本发明又一实施例绘示一种电源变换器的示意图。

图 8 是根据本发明另一实施例绘示一种电源变换器的示意图。

图 9 是根据本发明再一实施例绘示一种电源变换器的示意图。

图 10 是根据本发明又一实施例绘示一种电源变换器的示意图。

图 11 是根据本发明另一实施例绘示一种电源变换器的示意图。

图 12 是根据本发明再一实施例绘示一种电源变换器的示意图。

图 13 是根据本发明又一实施例绘示一种电源变换器的示意图。

图 14 是根据本发明另一实施例绘示一种电源变换器于制程中的部分结构示意图。

图 15 是根据本发明再一实施例绘示一种电源变换器于制程中的部分结构示意图。

图 16 是根据本发明又一实施例绘示一种电源变换器于制程中的部分结构示意图。

图 17 是根据本发明另一实施例绘示一种电源变换器于制程中的部分结构示意图。

图 18 是根据本发明再一实施例绘示一种电源变换器于制程中的部分结构示意图。

图 19 是根据本发明又一实施例绘示一种电源变换器于制程中的部分结构示意图。

图 20 是根据本发明另一实施例绘示一种电源变换器于制程中的部分结构示意图。

图 21 是根据本发明再一实施例绘示一种电源变换器于制程中的部分结构示意图。

图 22 是根据本发明又一实施例绘示一种电源变换器的示意图。

图 23 是绘示根据本发明另一实施方式的一种电源变换器的制造方法的流程图。

图 24 是绘示根据本发明另一实施方式的一种电源变换器的制程示意图。

具体实施方式

为了使本发明内容的叙述更加详尽与完备，下文针对了本发明的实

施态样与具体实施例提出了说明性的描述；但这并非实施或运用本发明具体实施例的唯一形式。实施方式中涵盖了多个具体实施例的特征以及用以建构与操作这些具体实施例的方法步骤与其顺序。然而，亦可利用其他具体实施例来达成相同或均等的功能与步骤顺序。

除非本说明书另有定义，此处所用的科学与技术词汇的含义与本发明所述技术领域的普通技术人员所理解与惯用的意义相同。

图 1 是根据本发明一实施例绘示一种电源变换器的示意图。如图所示，电源变换器 100 包含载具 PCB、第一电子元器件 C1、第二电子元器件 C2、第一连接部 P1、第二连接部 P2。本领域的技术人员应当理解，在图 1 所示的实施例中，电源变换器 100 包括第一连接部 P1 和第二连接部 P2，然而本发明并不只局限于此，在其他的实施例中，电源变换器 100 可仅仅包括第一连接部 P1，该第一连接部 P1 的第二端 Pad1 为一焊垫结构（pad），贴合于第一电子元器件 C1 的远离该载具的表面。实质上，从图 1 亦可知晓，第二连接部 P2 与第一连接部 P1 的端子结构基本相同或相似。进一步而言，载具 PCB 包含上表面 S1 及下表面 S2，第一连接部 P1 包含第一端 Pin1 及第二端 Pad1，第二连接部 P2 包含第一端 Pin2 及第二端 Pad2。在实现本发明时，载具 PCB 可为印刷电路板，而第一连接部 P1 及第二连接部 P2 可为接脚（Pin），然本发明并不以此为限，其仅用以例示性地说明本发明的实现方式之一。

在结构上，第一电子元器件 C1 配置于载具 PCB 的下表面 S2，而第二电子元器件 C2 配置于载具 PCB 的上表面 S1。第一连接部 P1 的第一端 Pin1 连接于载具 PCB 的下表面 S2，此时，第一连接部 P1 与载具 PCB 采用表面粘着方式（Surface Mount Technology，SMT）进行连接。或者，在另一实施例中，第一连接部 P1 的第一端 Pin1 连接于载具 PCB 的上表面 S1，此时，第一连接部 P1 与载具 PCB 采用直插方式进行连接。第一连接部 P1 的第二端 Pad1 是一焊垫结构，贴合于第一电子元器件 C1 的远离载具 PCB 的表面。由图中得以看出，载具 PCB 可配置于电源变换器高度的 1/3 至 2/3 处。此外，第一连接部 P1 是以第一电子元器件 C1 作为机械支撑而制成。

再者，第一连接部 P1 的第二端 Pad1 可用以与外部装置（图中未示）

进行连接。因此，外部装置可透过第一连接部 P1 的第二端 Pad1 及第一端 Pin1 而与载具 PCB 进行电性连接。类似地，第二连接部 P2 的第一端 Pin2 连接于载具 PCB 的下表面 S2，或者在另一实施例中，第二连接部 P2 的第一端 Pin2 连接于载具 PCB 的上表面 S1。第二连接部 P2 的第二端 Pad2 是一焊垫结构，贴合于第一电子元器件 C1 的远离载具 PCB 的表面，此外，第二连接部 P2 的第二端 Pad2 可用以与外部装置（图中未示）进行连接。因此，外部装置可透过第二连接部 P2 的第二端 Pad2 及第一端 Pin2 而与载具 PCB 进行电性连接。此外，第二连接部 P2 是以第一电子元器件 C1 作为机械支撑而制成。

在另一实施例中，载具 PCB 的下表面 S2 上可配置多个第一电子元器件（如电子元器件 C1、C4），这些第一电子元器件中的最高者（如电子元器件 C1）与下表面 S2 的垂直高度为第一高度 H1。载具 PCB 的上表面 S1 上可配置多个第二电子元器件（如电子元器件 C2、C3），这些第二电子元器件中的最高者（如电子元器件 C2）与上表面 S1 的垂直高度为第二高度 H2。上述第一高度 H1、第二高度 H2 与载具 PCB 的厚度 H3 之和为电源变换器高度，载具 PCB 配置于电源变换器高度的 1/3 至 2/3 处。

在一实施例中，由于连接部 P1、P2 是直接以第一电子元器件 C1 作为机械支撑而制成，因此，可使得连接部 P1、P2 与第一电子元器件 C1 之间的间隙近乎于零。再者，由于以第一电子元器件 C1 为机械支撑来制作连接部 P1、P2，因此，连接部 P1、P2 本身的尺寸，可视电气需求而定，无需额外考量本身的机械强度和装配需要。因此，本发明实施例的电源变换器的连接部 P1、P2 的本体体积小，安装所需的空间随之变小，因而可大幅提升电源变换器的空间利用率，以达成较高的功率密度。另外，由于连接部 P1、P2 的尺寸仅以电性连接为考虑，因此，可以达成更小的损耗。此外，由于连接部 P1、P2 的体积小，因而可进一步降地制造成本。

在另一实施例中，连接部 P1、P2 可透过粘着剂以直接与第一电子元器件 C1 进行粘着。于再一实施中，第一电子元器件 C1 与第二电子元器件 C2 以载具 PCB 为中心线而上下对称，如此，可以充分利用载具 PCB 资源，并有利于整个电源变换器的应力均匀分布，因此，无需额外的应

力解决方案，以避免采用额外的应力解决方案时，将导致电源变换器的体积增加的问题。在又一实施例中，上述的对称的定义可为，第二高度 H2 不大于两倍的第一高度 H1，或第一高度 H1 不大于两倍的第二高度 H2。在一实施例中，第一电子元器件 C1 的高度等于第二电子元器件 C2 的高度。

在另一实施例中，连接部 P1、P2 可采用引线框架（lead frame），并以第一电子元器件 C1 作为机械支撑而制成。在再一实施例中，连接部 P1、连接部 P2 与载具 PCB 的连接采用表面粘着方式。

图 2 是根据本发明另一实施例绘示一种电源变换器的示意图。相较于图 1 所示的电源变换器 100，图 2 的电源变换器 200 的连接部 P1、P2 与载具 PCB 的连接采用直插方式。举例而言，连接部 P1、P2 连接于第一电子元器件 C1 且连接部 P1、P2 穿透载具 PCB 以连接于第二电子元器件 C2。若连接部 P1、P2 与载具 PCB 由图 1 所示的表面粘着方式改为图 2 所示的直插方式，则可使连接部 P1、P2 与载具 PCB 之间的连接更加稳固，以减少载具 PCB 到连接部 P1、P2 的传递损耗，此连接方式可适用于低压大电流状况。此外，如图 2 所示，连接部 P2 可位于载具 PCB 的最外侧，亦即电源变换器 200 的最外侧，如此一来，可进一步降低载具 PCB 的面积，以提升功率密度。

在另一实施例中，由于连接部 P1、P2 与第一电子元器件 C1 之间不一定需要电性连接，因此，第一电子元器件 C1 可为完整的电子元件，诸如为金属氧化物半导体场效应晶体管或集成电路。此外，第一电子元器件 C1 亦可为完整的电子元件组合，诸如功率模组。再者，第一电子元器件 C1 亦可包含磁性元件铁芯的一部份。于再一实施中，第一电子元器件 C1、第二电子元器件 C2 及载具 PCB 共同形成一电感元件，第一电子元器件 C1 与第二电子元器件 C2 分别为电感元件的铁芯的一部分，此时，电源变换器 200 为升压电路（Boost circuit）或降压电路（Buck circuit）。

在又一实施例中，第一电子元器件 C1、第二电子元器件 C2 及载具 PCB 共同形成变压器，第一电子元器件 C1 与第二电子元器件 C2 分别为变压器铁芯的一部分。例如，电源变换器 200 可为隔离型直流对直流变换器（isolated DC/DC converter）。

图 3 是根据本发明再一实施例绘示一种电源变换器的示意图。相较于图 1 所示的电源变换器 100，图 3 的电源变换器 300 还包含第三电子元器件 C1’及第四电子元器件 C2’，分别配置于载具 PCB 的下表面 S2 和上表面 S1，其中第三电子元器件 C1’、第四电子元器件 C2’及载具 PCB 共同形成一变压器，第三电子元器件 C1’与第四电子元器件 C2’分别为变压器铁芯的一部分。

图 4 是根据本发明又一实施例绘示一种电源变换器的示意图。相较于图 3 所示的电源变换器 300，图 4 的电源变换器 400 包含多个第一连接部 P1 及多个第二连接部 P2，第一连接部 P1 的每一者包含第一端 Pin1 以及第二端 Pad1，而第二连接部 P2 的每一者包含第一端 Pin2 以及第二端 Pad2。于结构上，第一连接部 P1 的第一端 Pin1 分别连接于第一电子元器件 C1 及第三电子元器件 C1’，并连接于载具 PCB。第一连接部 P1 的第二端 Pad1 用以与外部装置（图中未示）进行连接。第二连接部 P2 的第一端 Pin2 分别连接于第一电子元器件 C1 及第三电子元器件 C1’，并连接于载具 PCB。第二连接部 P2 的第二端 Pad2 用以与外部装置（图中未示）进行连接。由图中得以看出，本发明实施例的电源变换器的结构对称，因此，制作电源变换器的第一连接部 P1 及第二连接部 P2 较为简单。此外，如图 3 与图 4 所示的电源变换器 300、400，本发明实施例可选择性根据实际需求而将第一连接部 P1 及第二连接部 P2 制作于单一元件（如元件 C1）上，或制作于多个元件（如元件 C1、C1’）上。

在另一实施例中，第三电子元器件 C1’与第四电子元器件 C2’透过载具 PCB 以形成变压器铁芯。于再一实施中，第三电子元器件 C1’与第四电子元器件 C2’透过载具 PCB 以形成电感铁芯。

在又一实施例中，若第一电子元器件 C1 与第二电子元器件 C2 形成变压器铁芯，且第三电子元器件 C1’与第四电子元器件 C2’形成电感铁芯，则电源变换器 400 包含隔离型直流对直流变换器及降压型电源变换器，以形成一两级架构。此架构较适合输入输出比例大的状况，诸如 48V 及 400V。

图 5 是根据本发明另一实施例绘示一种电源变换器的示意图。相较于图 2 所示的电源变换器 200，图 5 的电源变换器 500 还包含至少一直插

接脚(如：Pin1'或 Pin2')，安装于第一连接部 P1 的第二端 Pad1，用以将焊垫连接方式转换为直插连接方式。

图 6 是根据本发明再一实施例绘示一种电源变换器的示意图。相较于图 5 所示的电源变换器 500，图 6 的电源变换器 600 的连接部 P1、P2 的第二端 Pad1、Pad2 一一对应直插接脚 Pin1'、Pin2'，并透过支架 610 来固定这些直插接脚 Pin1'、Pin2'。这是因为同时配置多个直插接脚 Pin1'、Pin2'时，其间的相互定位较为困难，因此，支架 610 可用以预先固定直插接脚 Pin1'、Pin2'，随后再将多个直插接脚 Pin1'、Pin2'同时配置于连接部 P1、P2 上。如此，可简化制作难度并有效控制精确度。

图 7 是根据本发明又一实施例绘示一种电源变换器的示意图。相较于图 6 所示的电源变换器 600，图 7 的电源变换器 700 还包含粘结层 710，此粘结层 710 可用以黏合第一电子元器件 C1 与支架 610，以防止直插接脚 Pin1'、Pin2'于使用时脱落。在一实施例中，连接部 P1 或连接部 P2 可采用引线框架（lead frame）制作而成。

图 8 是根据本发明另一实施例绘示一种电源变换器的示意图。如图所示，由于电源变换器 800 的结构对称，举例而言，其第一电子元器件 C1 与第二电子元器件 C2 以载具 PCB 为中心线而上下对称，因此，电源变换器 800 适合进行模造(Molding)制程，以使电源变换器 800 的结构更加牢固与可靠，并具备更佳的散热能力。

图 9 是根据本发明再一实施例绘示一种电源变换器的示意图。相较于图 8，于图 9 中对电源变换器 900 上的模造材料 910 进行打磨制程，直到电源变换器 900 的部分结构外露为止，例如进行打磨制程直到第二电子元器件 C2 露出为止，以便进一步减小体积，并提升散热能力。

图 10 是根据本发明又一实施例绘示一种电源变换器的示意图。如图所示，第一电子元器件 C1 包含第一表面 S3 及第二表面 S4，上述第一电子元器件 C1 的第一表面 S3 配置于载具 PCB 的下表面 S2。此外，电源变换器还包含芯片 IC，此芯片 IC 配置于第一电子元器件 C1 的第二表面 S4(亦即配置于第一电子元器件 C1 的远离载具 PCB 的表面)。再者，芯片 IC 包含一个或多个接脚(如：接脚 Pin3)，如此，芯片 IC 的信号可通过第一连接部 P1 及第二连接部 P2 来进行传递，或透过一个或多个接脚(如：

接脚 Pin3)来进行传递。

图 11 是根据本发明另一实施例绘示一种电源变换器的示意图。如图所示，电源变换器 1100 还包含软性印刷电路板 FPCB，此软性印刷电路板 FPCB 配置于第一连接部 P1 的外侧，软性印刷电路板 FPCB 的一端 Pad3 连接载具 PCB，另一端 Pad4 连接第一连接部 P1 的第二端 Pad1。由于可通过软性印刷电路板 FPCB，将信号由载具 PCB 传送至第一连接部 P1 的第二端 Pad1，因而可解决信号脚位数量较多的问题。此外，软性印刷电路板 FPCB 的另一端 Pad4 可用以与外部装置(图中未示)进行连接，因此软性印刷电路板 FPCB 可作为连接载具 PCB 与外部装置的连接器。于再一实施中，软性印刷电路板 FPCB 可透过异方性导电胶（Anisotropic Conductive Film, ACF）粘着于载具 PCB。由于异方性导电胶 ACF 为各向异性导电，若采用异方性导电胶 ACF 来连接软性印刷电路板 FPCB 与载具 PCB，则可实现高精确度的多信号连接。

图 12 是根据本发明再一实施例绘示一种电源变换器的示意图。相较于图 2 所示的电源变换器 200，图 12 的电源变换器 1200 还包含至少一电子元器件 C5 及/或 C6，内嵌于载具 PCB 中，如此，可进一步提升空间利用率。

图 13 是根据本发明又一实施例绘示一种电源变换器的示意图。如图 13 所示，第一电子元器件 C1 的第一连接部 P1 的第一端 Pin1 与载具 PCB 的连接为直插式，形成直插式的步骤如后：于载具 PCB 上开一孔洞，以使第一连接部 P1 的第一端 Pin1 透过孔洞而穿透载具 PCB；以及于载具 PCB 的孔洞上放置锡块 1310，以解决锡量不足的问题。锡量不足的原因往往是由于载具 PCB 上的其它元件通常为表面粘着装置（surface mount device, SMD）板，焊锡的放置为钢板印刷，因为这些元器件各板之间的距离可能很小，为了保证焊接品质，锡量不宜过多，亦即将钢板做得比较薄，通常在 0.1～0.2 毫米之间。若第一电子元器件 C1 的第一连接部 P1 的第一端 Pin1 与载具 PCB 之间为直插式连接，为了方便安装，需要将载具 PCB 上与第一连接部 P1 的第一端 Pin 相对应的孔洞开得较大。举例而言，孔洞的直径要比第一连接部 P1 的第一端 Pin1 的直径大 0.2 毫米。如此，钢板印刷的锡量就不足以填充第一连接部 P1 的第一端 Pin1 与孔洞

之间的空隙 1320，从而使得接触电阻过大。故在孔洞上方放置相应体积的锡块 1310，以弥补锡量的不足。需说明的是，图 13 显示的是制作过程，最终锡块 1310 已填充进上述空隙 1320，实际的电源变换器 1300 上不会有上述锡块 1310 的存在。

请参阅图 4，由于电源变换器 400 可包含多个第一连接部 P1 的第一端 Pin1 及第二端 Pad1 与多个第二连接部 P2 的第一端 Pin2 及第二端 Pad2，在制作图 4 的电源变换器 400 时，需确保上述第一连接部 P1 的第一端 Pin1 及第二端 Pad1 与第二连接部 P2 的第一端 Pin2 及第二端 Pad2 的平整度。为确保上述平整度，本发明提供一套制作流程，以图 14 至图 22 加以说明。

图 14 至图 22 是根据本发明一实施例绘示一种电源变换器于制程中的部分结构示意图。如图 14 所示，先行准备电源变换器的第一电子元器件 C1、第一连接部 P1 及第二连接部 P2，并将其结合为一组合结构。如图 15 所示，先行将载具 PCB 的下表面 S2 处，有与其电气连接的元器件，以表面粘着技术安装/焊接于下表面 S2 上。如图 16 所示，于上述组合结构与载具 PCB 之间涂上胶水，以将上述组合结构相应地插入载具 PCB，并通过与上述组合结构的下表面有粘力的平板 B1 以将上述组合结构与载具 PCB 连接，并可确保上述组合结构的平整度。由于上述组合结构的第一电子元器件 C1 可为磁性元件，因此，上述平板 B1 可为电磁吸盘，以与第一电子元器件 C1 之间产生吸力，而利于组装。随后，加温固化胶水，以将上述组合结构与载具 PCB 定型，而能确保整体结构的平整度。组装完成后，可视状况移除上述平板 B1。如图 17 所示，于载具 PCB 表面刷锡膏 1710，并放置各元件，随后进行焊接。如图 18 所示，将第二电子元器件 C2 黏接于载具 PCB 的上表面。

至图 18 的步骤，电源变换器已完成，如不需进行模造制程，则将拼板分离即可得到各个电源变换器。若需要继续进行模造制程，则继续进行图 19 至图 22 的流程。

如图 19 所示，以拼板周边为支点，进行模造制程。由于本发明实施例的电源变换器的结构对称，因此，模腔的分配十分有规律，模具成本因而较低且模流容易控制，制造良率高以进一步降低成本。如图 20 所示，

完成模造制程后，可通过磨砂等制程将下表面的胶水去除，以确保下表面的可焊性。此外，亦可于除胶后，进行镀锡或镀金等制程以提升下表面的可焊性。如图 21 所示，可通过打磨制程将上方的模造材料磨除，以露出第二电子元器件 C2，如此一来，即可大幅降低因模造制程为电源变换器带来的额外体积。此外，经打磨制程的第二电子元器件 C2 的裸露表面十分平整，有利于安装散热器于其上，且散热效果较佳。如图 22 所示，通过切割制程，将电源变换器分离，而得到模造的电源变换器。此外，透过调整切割位置，可将电源变换器的第二连接部 P2 的外侧裸露，将整体模造的电源变换器的体积降低。

图 23 是绘示根据本发明另一实施方式的一种电源变换器的制造方法的流程图。如图所示，本发明的电源变换器的制造方法 2300 包含以下步骤：

步骤 2310：粘着第一电子元器件于引线框架上，其中引线框架包含固持部及连接部；

步骤 2320：切除引线框架的固持部；

步骤 2330：以第一电子元器件作为机械支撑而弯曲连接部，使连接部固定于第一电子元器件；

步骤 2340：粘着第一电子元器件于载具的下表面；

步骤 2350：粘着第二电子元器件于载具的上表面，以形成电源变换器，其中载具配置于电源变换器高度的 1/3 至 2/3 处。

为使本发明实施例的电源变换器的制造方法易于理解，请一并参阅图 23 及图 24，图 24 是绘示根据本发明另一实施方式的一种电源变换器的制程示意图。于步骤 2310 中，请参阅图 24 的流程 2430，粘着第一电子元器件 C1 于引线框架 2480 上，其中引线框架 2480 包含固持部 2460 及连接部 2470。于步骤 2320 中，请参阅图 24 的流程 2440，切除引线框架 2480 的固持部 2460，只留下引线框架 2480 的连接部 2470。于步骤 2330 中，请参阅图 24 的流程 2450，以第一电子元器件 C1 作为机械支撑而弯曲连接部 2470，使连接部 2470 固定于第一电子元器件 C1，图 24 的流程 2450 的上下两图分别用以显示第一电子元器件 C1 的上下表面。

为使本发明实施例的电源变换器的制造方法易于理解，请一并参阅

图 23、图 16 及图 18，于步骤 2340 中，请参阅图 16 及其相关说明，粘着第一电子元器 C1 件于载具 PCB 的下表面。于步骤 2350 中，请参阅图 18 及其相关说明，粘着第二电子元器件 C2 于载具 PCB 的上表面，以形成电源变换器，其中载具 PCB 配置于电源变换器高度的 1/3 至 2/3 处。

在一实施例中，请参阅图 1，由本发明的制造方法 2300 所制成的电源变换器 100 的连接部 P1、P2，是直接以第一电子元器件 C1 作为机械支撑而制成，因此，可使得连接部 P1、P2 与第一电子元器件 C1 之间的间隙近乎于零。在另一实施例中，连接部 P1、P2 可透过粘着剂以直接与第一电子元器件 C1 进行粘着。

于再一实施中，第一电子元器件 C1 与第二电子元器件 C2 以载具 PCB 为中心线而上下对称，如此，可以充分利用载具 PCB 资源，并有利于整个电源变换器的应力均匀分布，因此，无需额外的应力解决方案，以避免采用额外的应力解决方案时，将导致电源变换器的体积增加的问题。在又一实施例中，上述的对称的定义可为，第二高度 H2 不大于两倍的第一高度 H1，或第一高度 H1 不大于两倍的第二高度 H2。于一实施例中，第一电子元器件 C1 的高度等于第二电子元器件 C2 的高度。

在另一实施例中，相较于图 1 所示的电源变换器 100，由制造方法 2300 所制成的图 2 的电源变换器 200 的连接部 P1、P2 与载具 PCB 的连接采用直插方式。举例而言，连接部 P1、P2 连接于第一电子元器件 C1 且连接部 P1、P2 穿透载具 PCB 以连接于第二电子元器件 C2。若连接部 P1、P2 与载具 PCB 由图 1 所示的表面粘着方式改为图 2 所示的直插方式，则可使连接部 P1、P2 与载具 PCB 之间的连接更加稳固，以减少载具 PCB 到连接部 P1、P2 的传递损耗，此一连接方式可适用于低压大电流状况。

在又一实施例中，由于连接部 P1、P2 与第一电子元器件 C1 之间不一定需要电气连接，因此，第一电子元器件 C1 可为完整的电子元件，诸如为金属氧化物半导体场效应晶体管或积体电路，此外，第一电子元器件 C1 亦可为完整的电子元件组合，诸如功率模组，再者，第一电子元器件 C1 亦可包含磁性元件铁芯的一部份。于再一实施中，第一电子元器件 C1、第二电子元器件 C2 及载具 PCB 共同形成一电感元件，第一电子元器件 C1 与第二电子元器件 C2 分别为电感元件的铁芯的一部分，此时，

电源变换器 200 为升压电路（Boost circuit）或降压电路（Buck circuit）。

在另一实施例中，第一电子元器件 C1、第二电子元器件 C2 及载具 PCB 共同形成变压器，第一电子元器件 C1 与第二电子元器件 C2 分别为变压器铁芯的一部分

于再一实施例中，相较于图 1 所示的电源变换器 100，由制造方法 2300 所制成的图 3 的电源变换器 300 还包含第三电子元器件 C1'及第四电子元器件 C2'，分别配置于载具 PCB 的下表面 S2 和上表面 S1，其中第三电子元器件 C1'、第四电子元器件 C2'及载具 PCB 共同形成一变压器，第三电子元器件 C1'与第四电子元器件 C2'分别为变压器铁芯的一部分。

于再一实施例中，相较于图 3 所示的电源变换器 300，由制造方法 2300 所制成的图 4 的电源变换器 400 包含多个第一连接部 P1 及多个第二连接部 P2，第一连接部 P1 的每一者包含第一端 Pin1 以及第二端 Pad1，而第二连接部 P2 的每一者包含第一端 Pin2 以及第二端 Pad2。于结构上，第一连接部 P1 的第一端 Pin1 分别连接于第一电子元器件 C1 及第三电子元器件 C1'，并连接于载具 PCB。第一连接部 P1 的第二端 Pad1 用以与外部装置（图中未示）进行连接。第二连接部 P2 的第一端 Pin2 分别连接于第一电子元器件 C1 及第三电子元器件 C1'，并连接于载具 PCB。第二连接部 P2 的第二端 Pad2 用以与外部装置（图中未示）进行连接。由图中得以看出，本发明实施例的电源变换器的结构对称，因此，制作电源变换器的第一连接部 P1 及第二连接部 P2 较为简单。此外，如图 3 与图 4 所示的电源变换器 300、400，本发明实施例可选择性根据实际需求而将第一连接部 P1 及第二连接部 P2 制作于单一元件（如元件 C1）上，或制作于多个元件（如元件 C1、C1'）上。

在另一实施例中，第三电子元器件 C1'与第四电子元器件 C2'透过载具 PCB 以形成变压器铁芯。于再一实施中，第三电子元器件 C1'与第四电子元器件 C2'透过载具 PCB 以形成电感铁芯。

在又一实施例中，若第一电子元器件 C1 与第二电子元器件 C2 形成变压器铁芯，且第三电子元器件 C1'与第四电子元器件 C2'形成电感铁芯，则电源变换器 400 包含隔离型直流对直流变换器及降压型电源变换器，以形成一两级架构。此架构较适合输入输出比例大的状况，诸如 48V 及

400V。

于再一实施例中，请参阅图 5，本发明的电源变换器的制造方法 2300 还包含：粘着直插接脚 Pin1’、Pin2’于连接部 P1、P2，此直插接脚 Pin1’、Pin2’用以与外部装置（图中未示）进行连接。

在另一实施例中，请参阅图 6，本发明的电源变换器的制造方法 2300 还包含：以一支架 610 来固定直插接脚 Pin1’、Pin2’。增加上述步骤是因为同时配置多个直插接脚 Pin1’、Pin2’时，其间的相互定位较为困难，因此，支架 610 可用以预先固定直插接脚 Pin1’、Pin2’，随后再将多个直插接脚 Pin1’、Pin2’同时配置于连接部 P1、P2。如此，可简化制作难度并有效控制精确度。在另一实施例中，请参阅图 7，本发明的电源变换器的制造方法 2300 还包含：以粘结层 710 黏合第一电子元器件 C1 与支架 610。如此一来，可防止直插接脚 Pin1’、Pin2’于使用时脱落。

于再一实施例中，请参阅图 8，本发明的电源变换器的制造方法 2300 还包含：对电源变换器 800 进行一模造(Molding)制程。由于电源变换器 800 的结构对称，因此，电源变换器 800 适合进行模造(Molding)制程，以使电源变换器 800 的结构更加牢固与可靠，并具备更佳的散热能力。请参阅图 9，本发明的电源变换器的制造方法 2300 还包含：对电源变换器 900 上的模造材料 910 进行打磨制程，直到电源变换器 900 的部分结构外露为止。举例而言，对电源变换器 900 上的模造材料 910 进行打磨制程以裸露第二电子元器件 C2 和/或第一电子元器件 C1，或者，对电源变换器 900 上的模造材料 910 进行打磨制程以裸露连接部 P2 的外侧，以便进一步减小体积，并提升散热能力。

于再一实施例中，请参阅图 10，步骤 2340 所述的粘着第一电子元器件 C1 于载具 PCB 的下表面的步骤包含：粘着第一电子元器件 C1 的第一表面 S3 于载具 PCB 的下表面 S2。此外，本发明的电源变换器的制造方法 2300 还包含：透过胶水配置芯片 IC 于第一电子元器件 C1 的第二表面 S4(亦即配置于第一电子元器件 C1 的远离载具 PCB 的表面)；以及设置一个或多个接脚(如：接脚 Pin3)于芯片 IC 的表面，如此，芯片 IC 的信号可通过第一连接部 P1 及第二连接部 P2 来进行传递，或透过接脚(如：接脚 Pin3)来进行传递。

在又一实施例中，请参阅图 11，连接部 P1 包含第一端 Pin1 和第二端 Pad1，本发明的电源变换器的制造方法 2300 还包含：配置软性印刷电路板 FPCB 以连接载具 PCB 与连接部 P1 的第二端 Pad1。由于可通过软性印刷电路板 FPCB，将信号由载具 PCB 传送至连接部 P1 的第二端 Pad1，因而可解决信号脚位数量较多的问题。此外，软性印刷电路板 FPCB 可作为连接载具 PCB 与外部装置的连接器。再者，上述透过软性印刷电路板 FPCB 以连接载具 PCB 与连接部 P1 的步骤包含：透过异方性导电胶 ACF 以将软性印刷电路板 FPCB 粘着于载具 PCB。由于异方性导电胶 ACF 为各向异性导电，若采用异方性导电胶 ACF 来连接软性印刷电路板 FPCB 与载具 PCB，则可实现高精确度的多信号连接。

在另一实施例中，请参阅图 12，本发明的电源变换器的制造方法 2300 还包含：内嵌电子元件 C5 及/或 C6 于载具中 PCB。如此，可进一步提升空间利用率。

在又一实施例中，于制造方法 2300 所制成的电源变换器 1300 中，第一电子元器件 C1 的第一连接部 P1 的第一端 Pin1 与载具 PCB 的连接为直插式，形成直插式的步骤如后：于载具 PCB 上开一孔洞，以使第一连接部 P1 的第一端 Pin1 透过孔洞而穿透载具 PCB；于载具 PCB 的孔洞上放置锡块 1310；以及以波峰焊（wave soldering）或回流焊（reflow soldering）的方式使锡块 1310 填满孔洞，以解决锡量不足的问题。需说明的是，图 13 显示的是制作过程，最终锡块 1310 已填充进空隙 1320，实际的电源变换器 1300 上不会有上述锡块 1310 的存在。

于再一实施例中，请参阅图 16，第一电子元器件 C1 为磁性元件，本发明的电源变换器的制造方法 2300 还包含：涂布胶水于磁性元件 C1 和载具 PCB 的连接位置；提供一电磁吸盘 B1 于磁性元件 C1 的远离载具 PCB 的表面；通过电磁吸盘 B1 产生的粘力吸合磁性元件 C1 和连接部 P1；以及加温固化所涂布的胶水，以定位磁性元件 C1 与载具 PCB。

所属技术领域中具有通常知识者当可明白，电源变换器的制造方法 2300 中的各步骤依其执行的功能予以命名，仅是为了让本案的技术更加明显易懂，并非用以限定这些步骤。将各步骤予以整合成同一步骤或分拆成多个步骤，或者将任一步骤更换到另一步骤中执行，皆仍属于本发

明内容的实施方式。

由上述可知，本发明实施例通过提供一种电源变换器及其制造方法，藉以改善电源变换器的脚位设计无法兼顾适用范围广及体积小、成本低及损耗低的问题。

此外，本发明实施例的电源变换器，特别适合用于高功率密度、高效率场合，诸如功率密度大于 300W/inch3 及效率高于 90%的场合。本发明实施例的电源变换器的工作频率可高于 500KHz，而输入电压范围可介于 1V~400V 之间。然本发明的电源变换器的实现方式并不以上述实施例为限，其仅用以例示性地说明本发明的实现方式之一。

再者，相较于现有技术，本发明实施例通过提供一种电源变换器及其制造方法，尤其是对于连接部 P1、P2 的制作方式，具有更佳的电性能、热性能与更高的功率密度。另外，其可充分使用空间，且生产方便，非常利于提高电源变换器的功率密度或者效率。此外，本发明实施例所示的具体结构、生产工艺、流程等，亦十分可行有效。因此，本发明实施例十分适合用以提升电源变换器的整体性能和性价比，特别是 POL 的整体性能和性价比。

虽然上文实施方式中揭露了本发明的具体实施例，然其并非用以限定本发明，本发明的本领域的技术人员，在不悖离本发明的原理与精神的情形下，当可对其进行各种更动与修饰，因此本发明的保护范围当以随附的权利要求书所界定者为准。

100

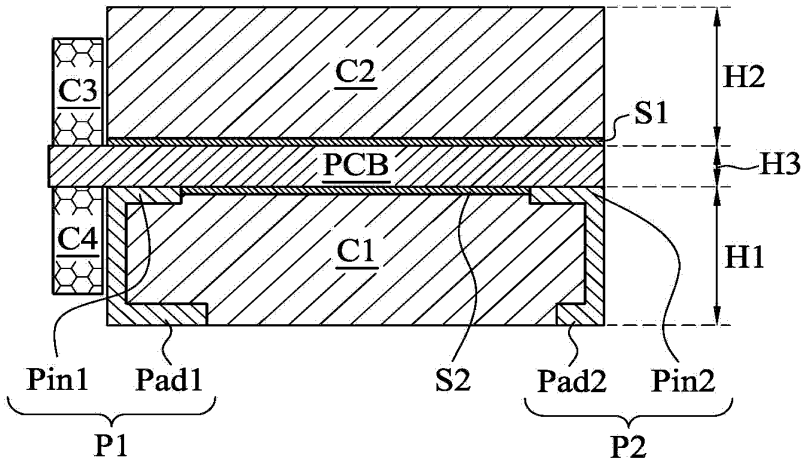

C2
C3
S1
H2
PCB
H3
C4
C1
H1
Pin1
Pad1
S2
Pad2
Pin2
P1
P2

图1

200

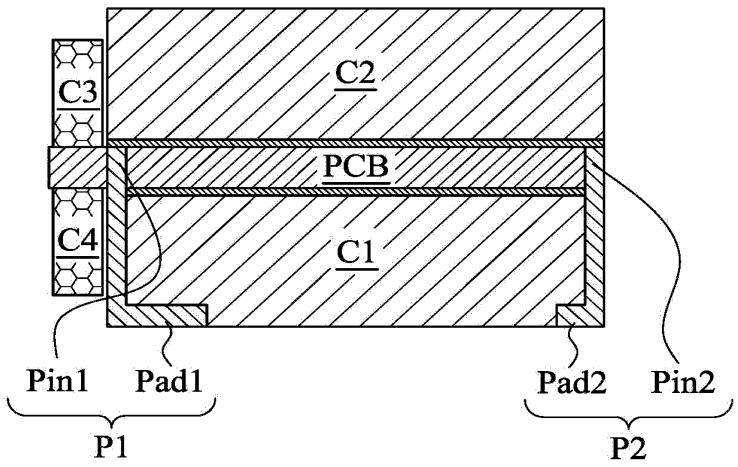

C2
C3
PCB
C4
C1
Pin1
Pad1
Pad2
Pin2
P1
P2

图2

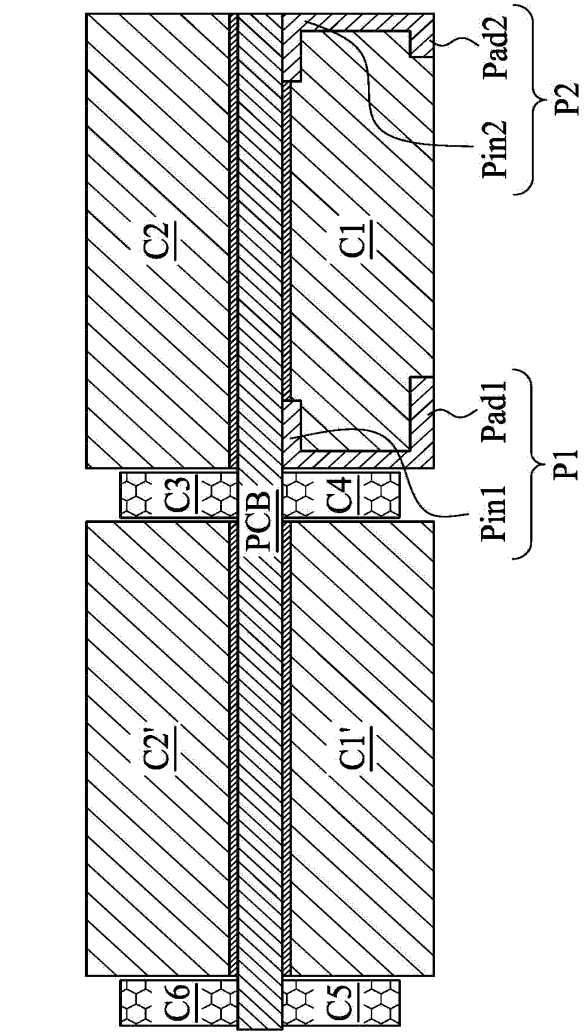


图3

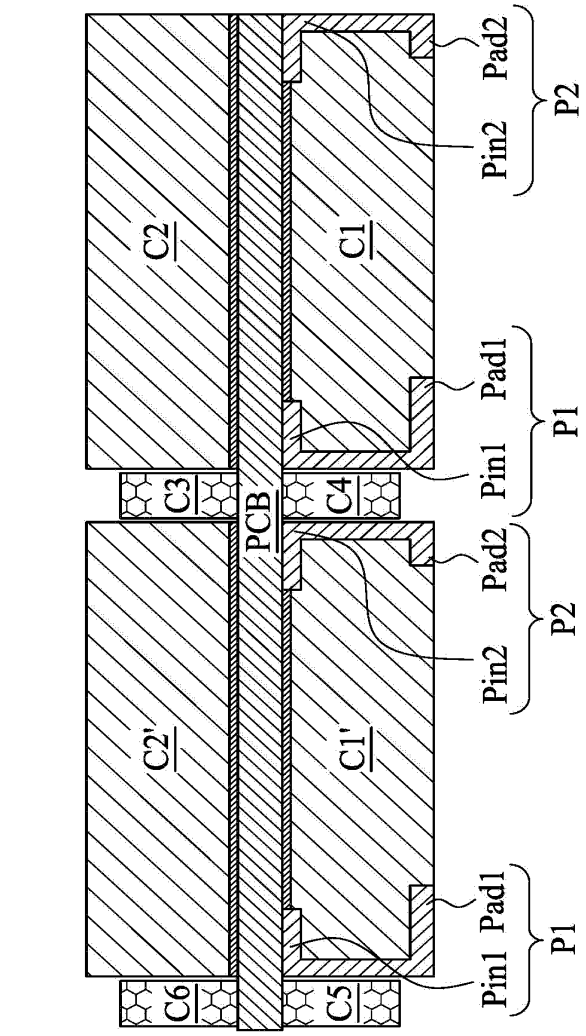

400
C6
C5
C2'
C1'
PCB
C3
C4
C2
C1
Pin1
Pad1
P1
Pin2
Pad2
P2
Pin1
Pad1
P1
Pin2
Pad2
P2

图4

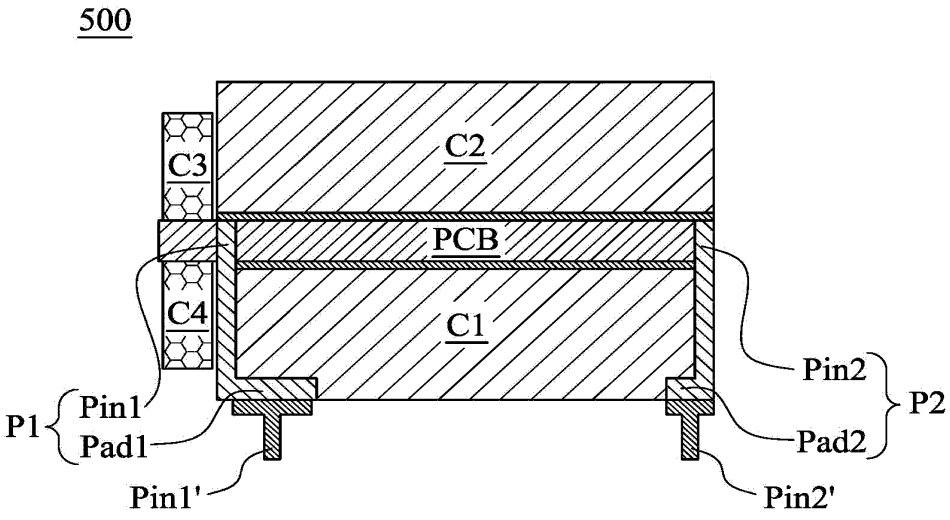

500
C3
C2
PCB
C4
C1
Pin2
P2
P1
Pin1
Pad1
Pad2
Pin1'
Pin2'

图5

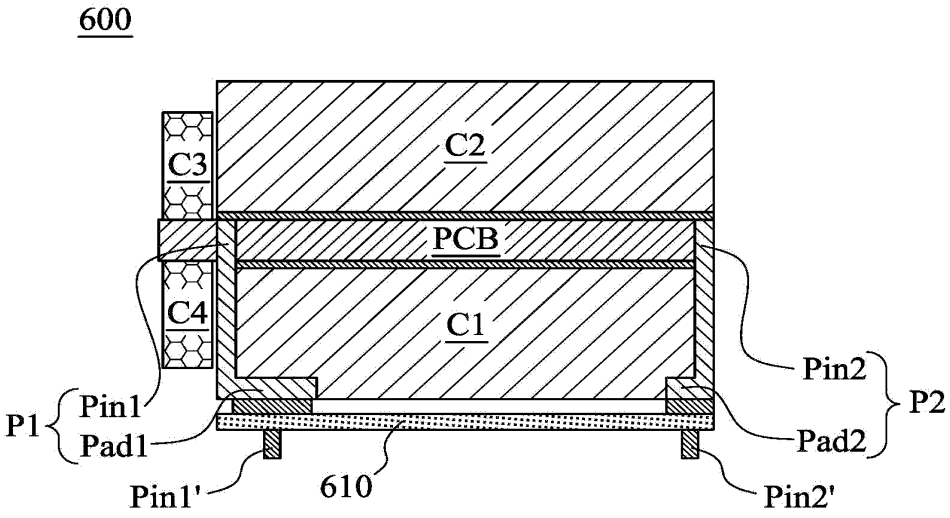

600
C3
C2
PCB
C4
C1
Pin2
P2
P1
Pin1
Pad1
Pad2
610
Pin1'
Pin2'

图6

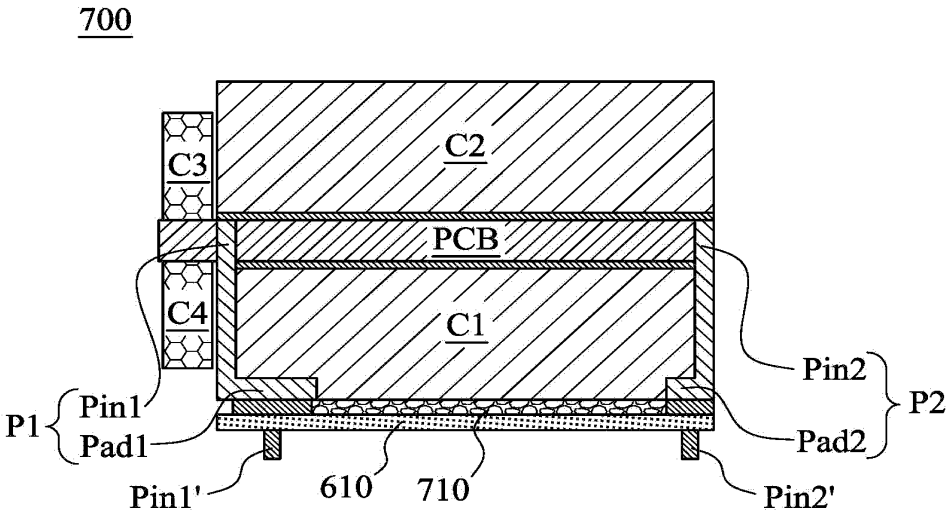


图7

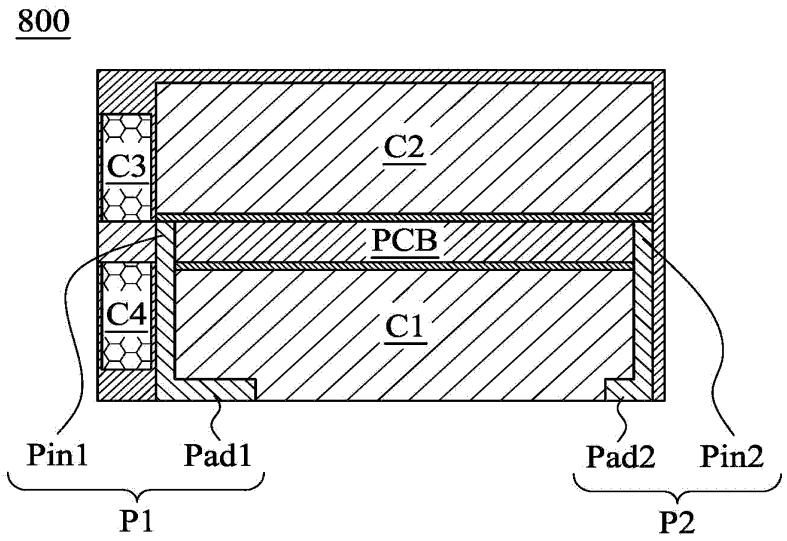

800
C3
C2
PCB
C4
C1
Pin1
Pad1
Pad2
Pin2
P1
P2

图8

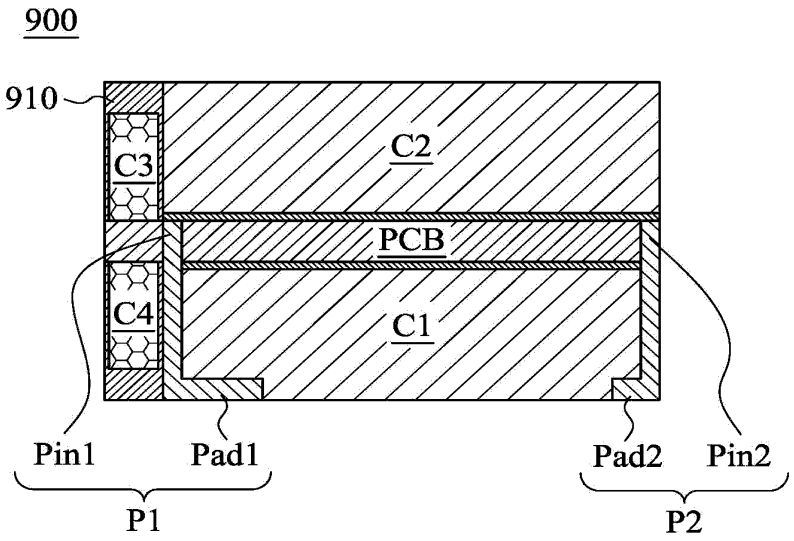

900
910
C3
C2
PCB
C4
C1
Pin1
Pad1
Pad2
Pin2
P1
P2

图9

2015106482801

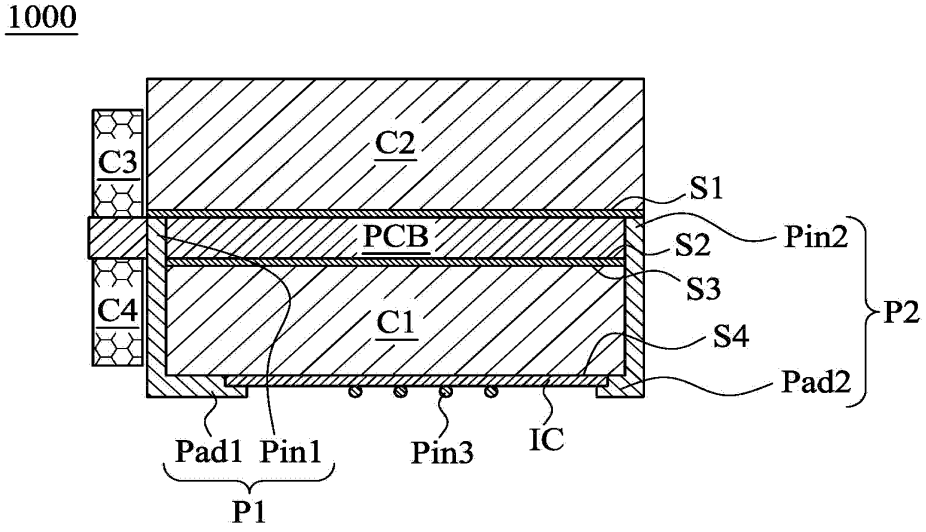


图10

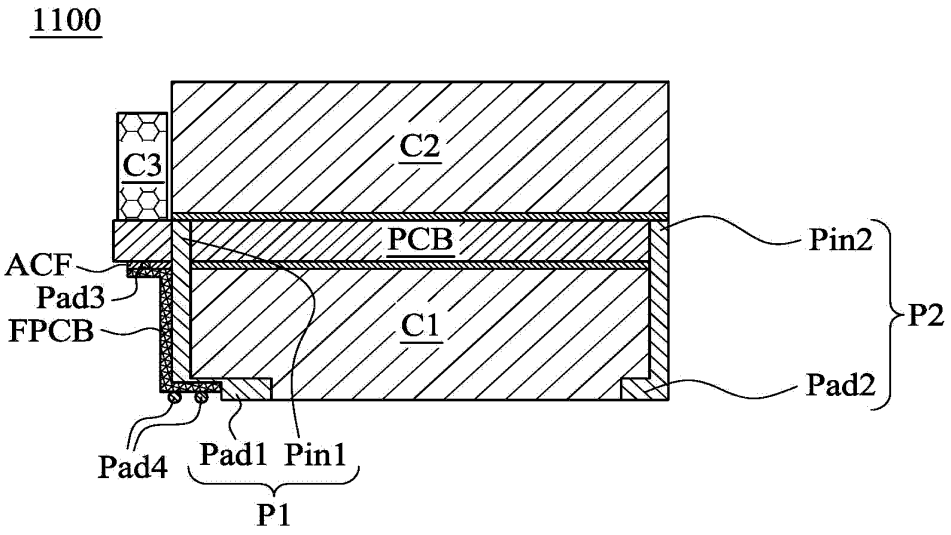


图11

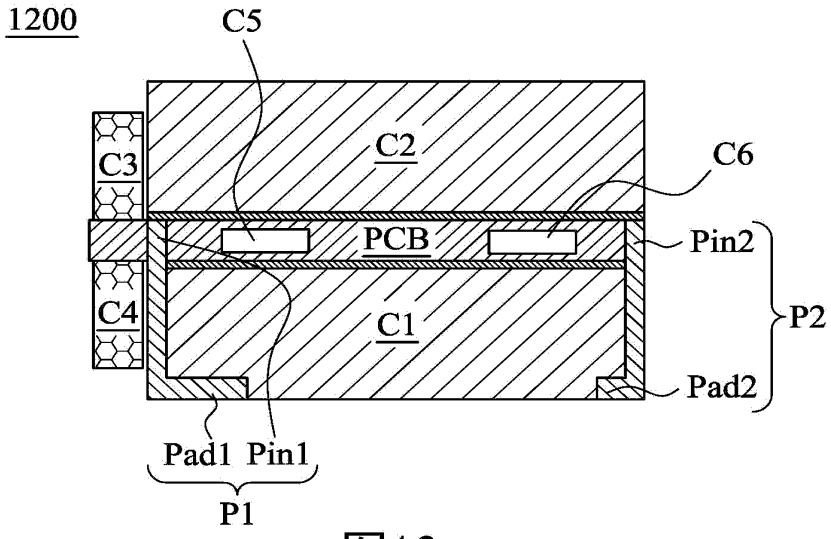

1200
C5
C2
C6
C3
PCB
Pin2
C4
C1
P2
Pad2
Pad1
Pin1
P1

图12

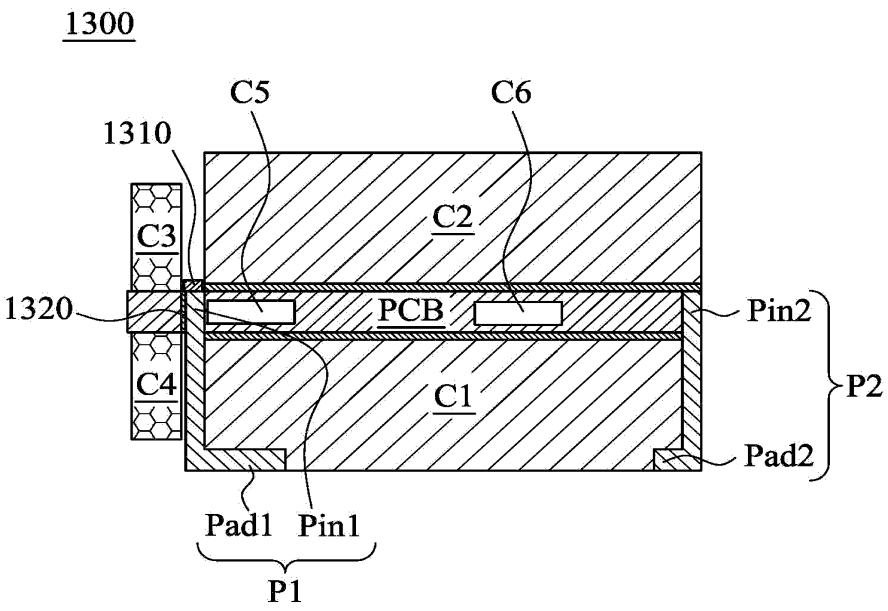

1300
C5
C6
1310
C2
C3
1320
PCB
Pin2
C4
C1
P2
Pad2
Pad1
Pin1
P1

图13

2015106482801

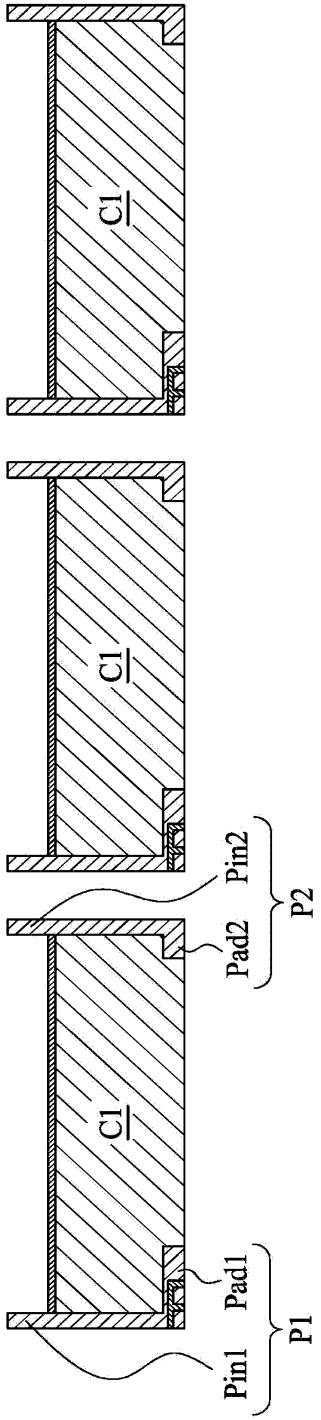


图14

2015106482801

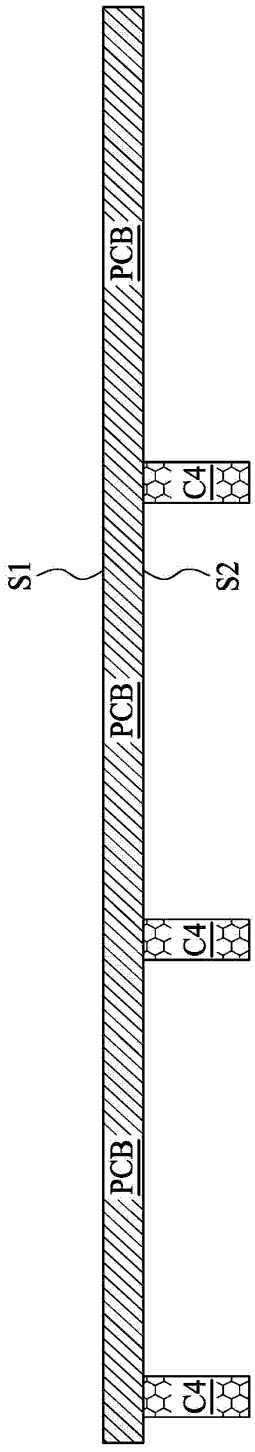


图15

2015106482801

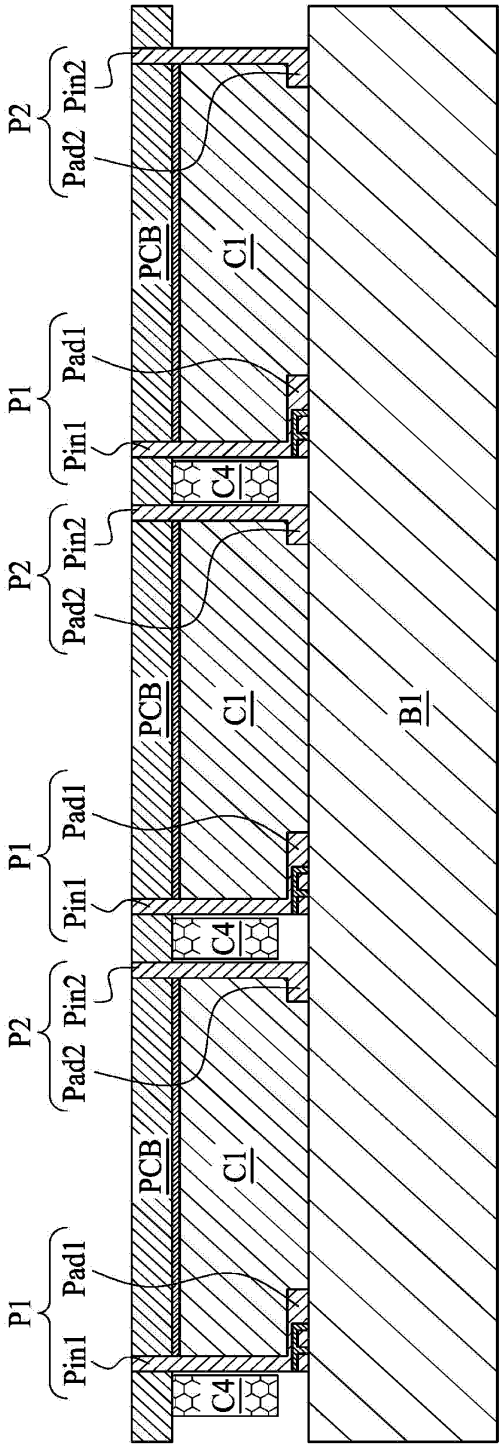


图16

2015106482801

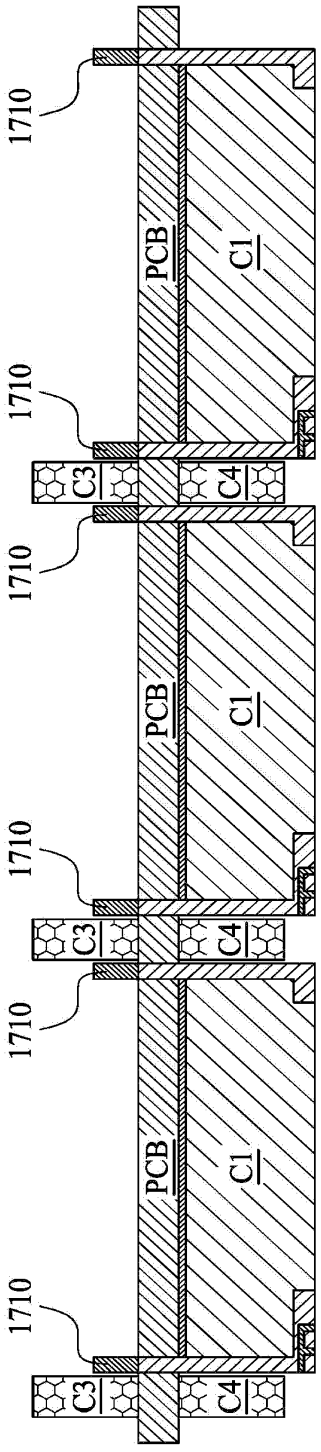


图17

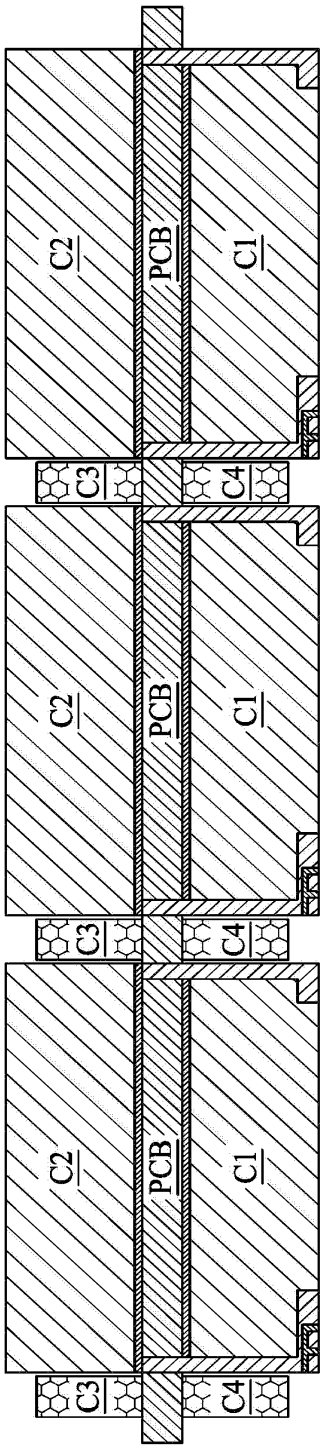


图18

2015106482801

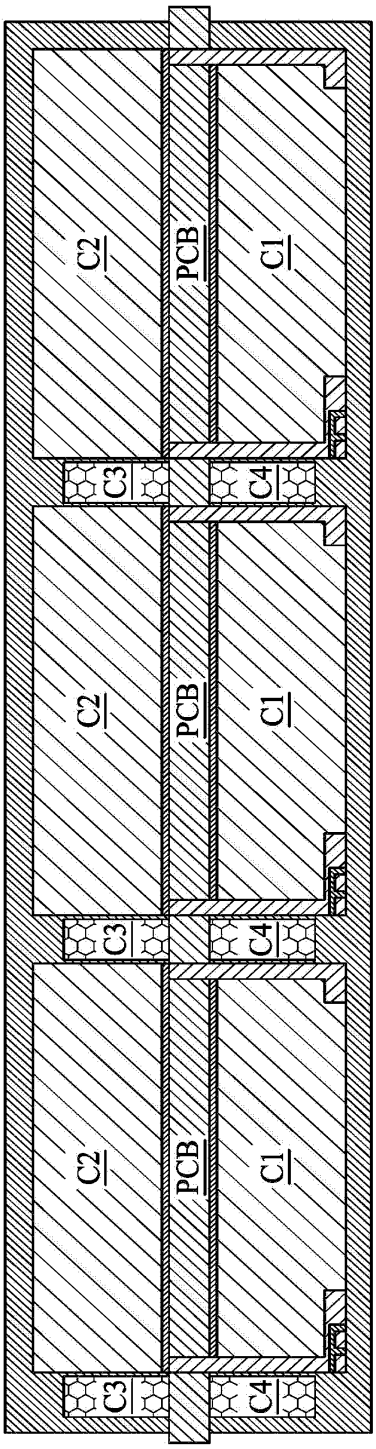


图19

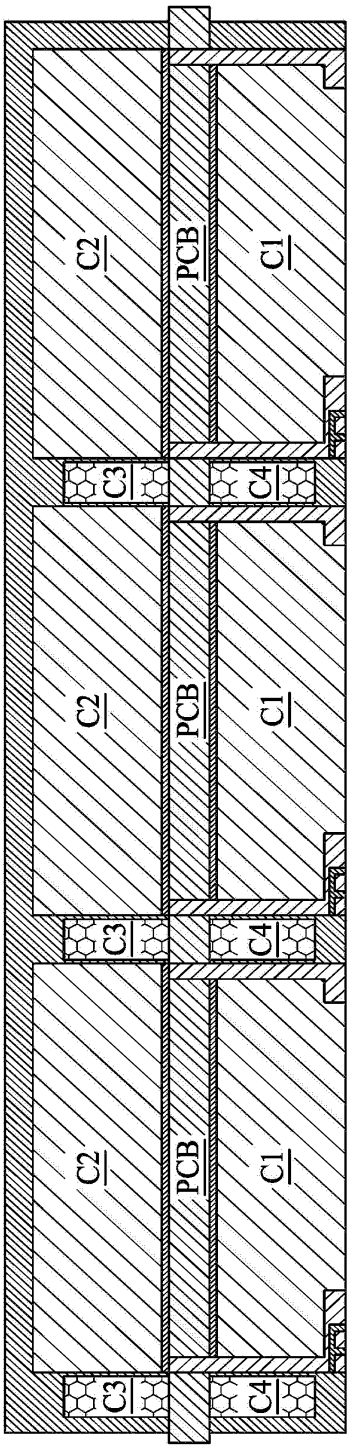


图20

2015106482801

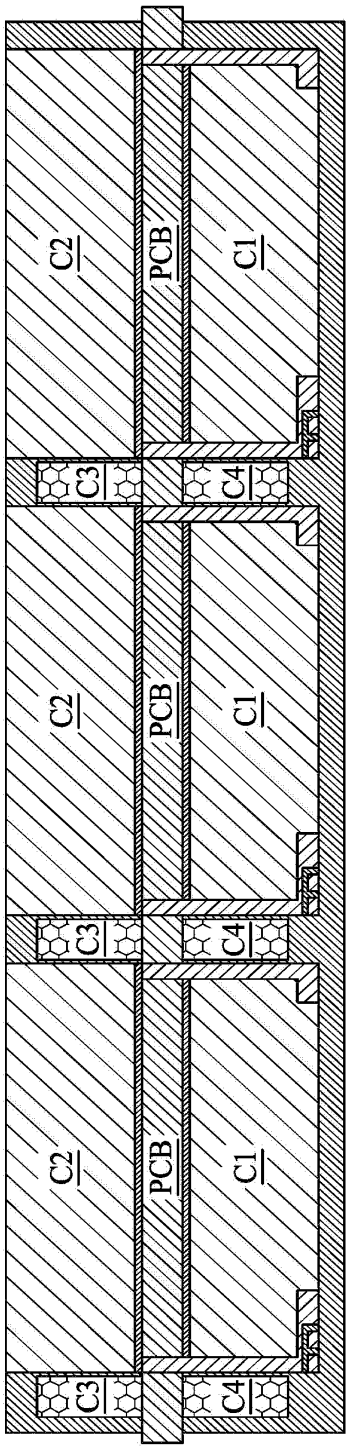


图21

2015106482801

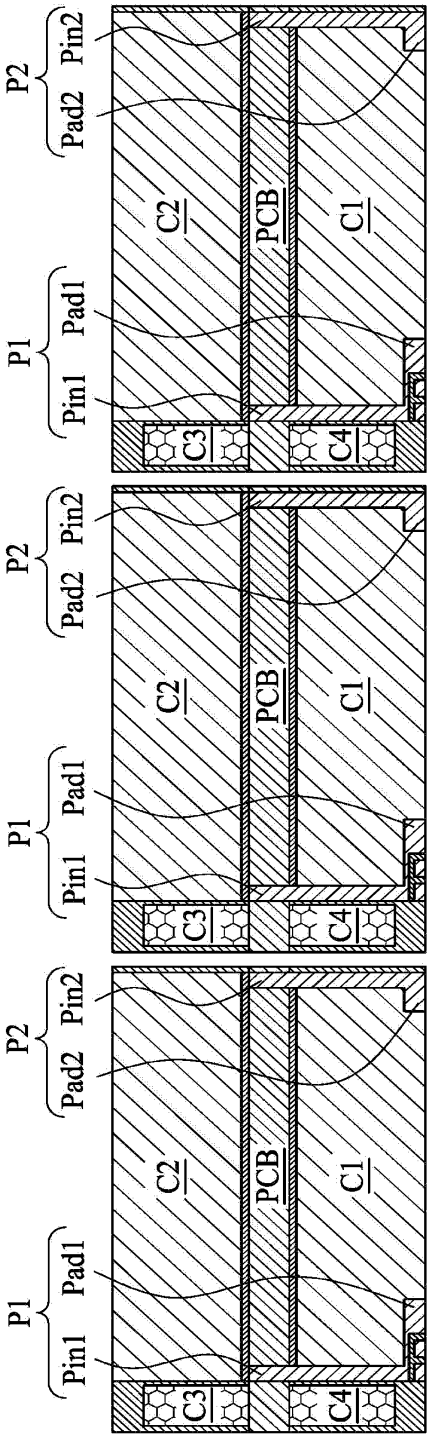


图22

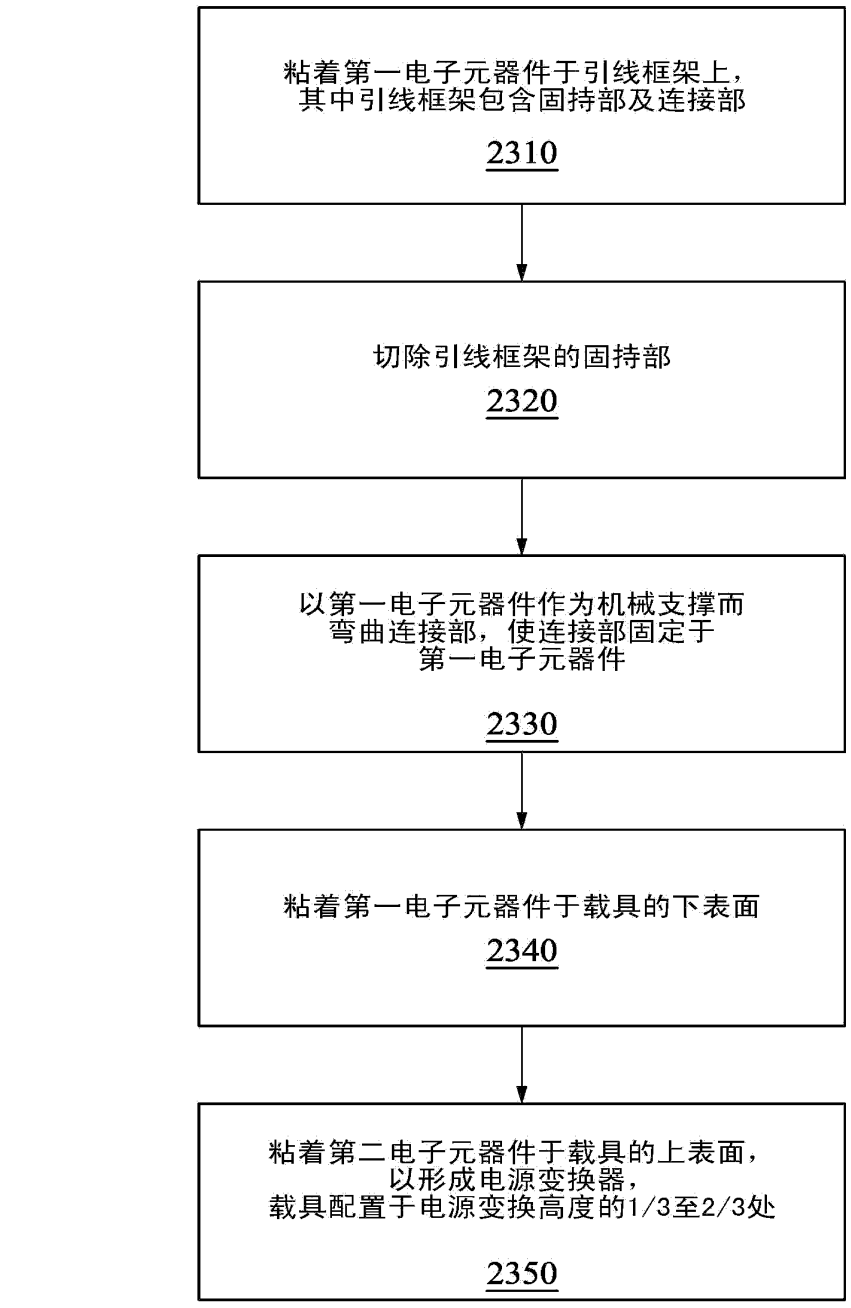

2300
粘着第一电子元器件于引线框架上，
其中引线框架包含固持部及连接部
2310
切除引线框架的固持部
2320
以第一电子元器件作为机械支撑而
弯曲连接部，使连接部固定于
第一电子元器件
2330
粘着第一电子元器件于载具的下表面
2340
粘着第二电子元器件于载具的上表面，
以形成电源变换器，
载具配置于电源变换高度的1/3至2/3处
2350

图23

2015106482801

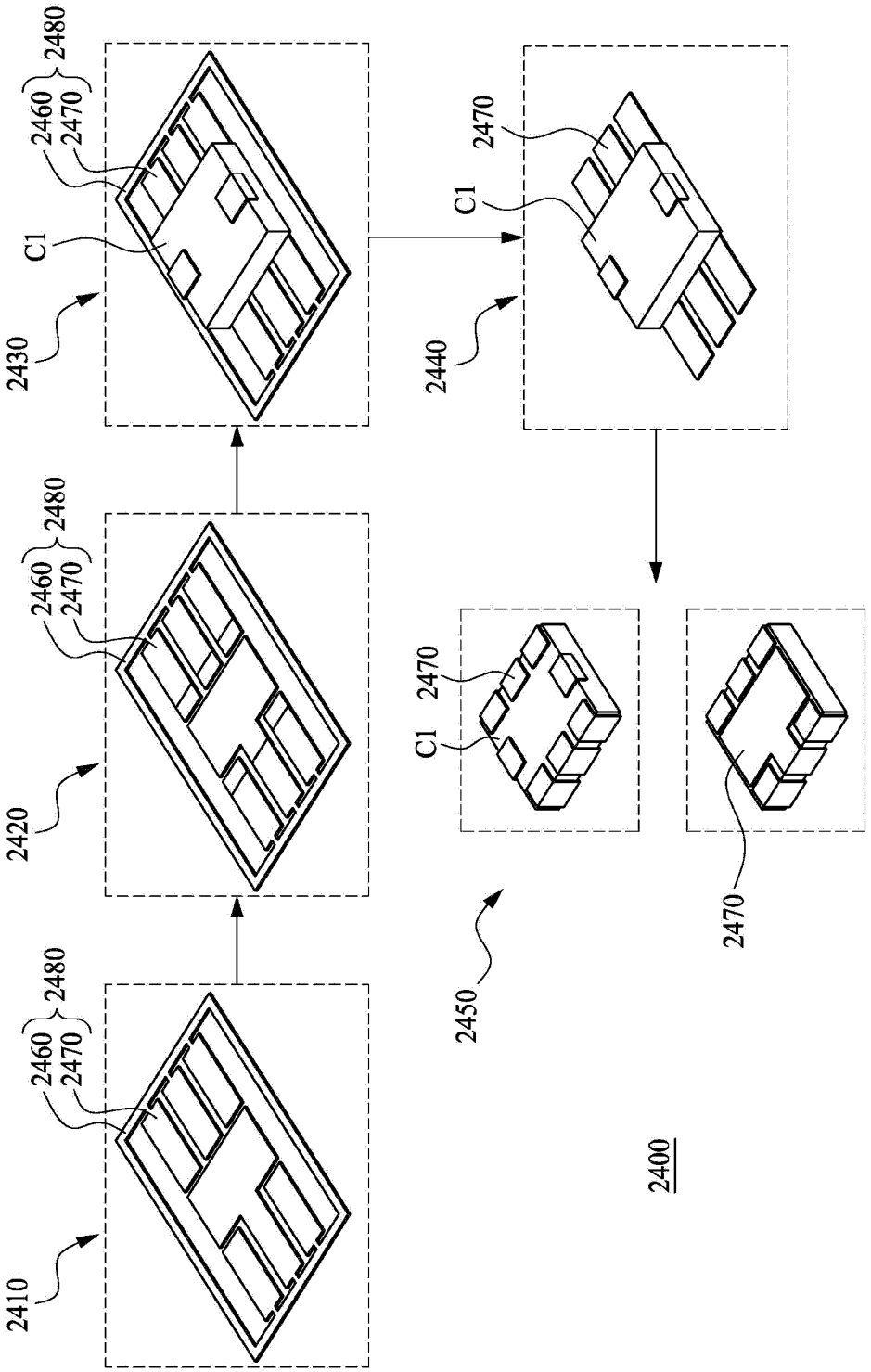


图24

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/286,542	10/05/2016	2838	1920	TWT04774/US	24	2

CONFIRMATION NO. 1984

FILING RECEIPT

60589
JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

OC000000088358853

Date Mailed: 10/20/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jian-Hong ZENG, Taoyuan City, TAIWAN;
Shou-Yu HONG, Taoyuan City, TAIWAN;
Xiao-Ni XIN, Taoyuan City, TAIWAN;
Pei-Qing HU, Taoyuan City, TAIWAN;

Applicant(s)

DELTA ELECTRONICS, INC., Taoyuan City, TAIWAN;

Power of Attorney: The patent practitioners associated with Customer Number 60589

Domestic Applications for which benefit is claimed - None.
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
CHINA 201510648280.1 10/09/2015

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 10/18/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/286,542**

Projected Publication Date: 04/13/2017

Non-Publication Request: No

Early Publication Request: No

Title

POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME

Preliminary Class

363

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/286,542

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	24 minus 20 =	* 4			OR	x 80 =	320
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1920

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☒ Practitioners associated with Customer Number: 60589

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☒ The address associated with Customer Number: 60589

OR

☐	Firm or Individual Name		
	Address		
	City	State	Zip
	Country		
	Telephone	Email	

Assignee Name and Address: Delta Electronics, Inc.
31-1 Xingbang Road, Guishan Industrial Zone ,Taoyuan City 33370, Taiwan R. O. C.

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/AIA/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	C. H. T.	Date	Sept. 2, 2015
Name	TING CHAOPING	Telephone	886-2-8797-2088
Title	General Counsel		

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NP-16519-US/20140443-US

PTO/AIA/01 (06-12)
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [■] The attached application, or
- [ ] United States application or PCT international application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

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LEGAL NAME OF INVENTOR

Inventor: Jian-Hong ZENG Date (Optional): 2016/8/29

Signature: Jian-Hong ZENG

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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- [ ] United States application or PCT international application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: Shou-Yu HONG Date (Optional): 2016. 9. 27

Signature: Shou-Yu HONG

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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This declaration is directed to:

- ☒ The attached application, or
- ☐ United States application or PCT international application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: Xiao-Ni XIN Date (Optional): 2016.9.27

Signature: Xiao-Ni XIN

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/01 (06-12)
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ■ The attached application, or
- ☐ United States application or PCT international application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Pei-Qing HU Date (Optional): 2016.8.27

Signature: Pei-Qing HU

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	TWT04774/US
	Application Number	
Title of Invention	POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jian-Hong		ZENG	

Residence Information (Select One) US Residency ● Non US Residency Active US Military Service

City	Country of Residence [i]
Taoyuan City	TW

Mailing Address of Inventor:

Address 1	31-1 Xingbang Road, Guishan Industrial Zone
Address 2	
City	Taoyuan City
State/Province	
Postal Code	33370
Country [i]	TW

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shou-Yu		HONG	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Country of Residence [i]
Taoyuan City	TW

Mailing Address of Inventor:

Address 1	31-1 Xingbang Road, Guishan Industrial Zone
Address 2	
City	Taoyuan City
State/Province	
Postal Code	33370
Country [i]	TW

Inventor 3 Remove

Legal Name

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	TWT04774/US
	Application Number	
Title of Invention	POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Xiao-Ni		XIN	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Taoyuan City	Country of Residence [i]	TW

Mailing Address of Inventor:

Address 1	31-1 Xingbang Road, Guishan Industrial Zone
Address 2	
City	Taoyuan City
State/Province	
Postal Code	33370
Country [i]	TW

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Pei-Qing		HU	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Taoyuan City	Country of Residence [i]	TW

Mailing Address of Inventor:

Address 1	31-1 Xingbang Road, Guishan Industrial Zone
Address 2	
City	Taoyuan City
State/Province	
Postal Code	33370
Country [i]	TW

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	60589		
Email Address	info@ckc-ip.com	Add Email	Remove Email

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	TWT04774/US
	Application Number	
Title of Invention	POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME	

Application Information:

Title of the Invention	POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME		
Attorney Docket Number	TWT04774/US	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)		**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	60589		

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	TWT04774/US
	Application Number	
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Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201510648280.1	CN	2015-10-09	

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	TWT04774/US
	Application Number	
Title of Invention	POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	TWT04774/US
	Application Number	
Title of Invention	POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	DELTA ELECTRONICS, INC.		
Mailing Address Information For Applicant:			
Address 1	31-1 Xingbang Road, Guishan Industrial Zone		
Address 2			
City	Taoyuan City	**State/Province**	
Country	TW	Postal Code	33370
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	TWT04774/US
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Title of Invention	POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/James Lynn O'Sullivan/			Date (YYYY-MM-DD)	2016-10-05
First Name	James	Last Name	O'Sullivan	Registration Number	65618

Additional Signature may be generated within this form by selecting the Add button. Add

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	TWT04774/US
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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME

RELATED APPLICATIONS

[0001] This application claims priority to Chinese Patent Application No. 201510648280.1, filed on October 9, 2015, which is herein incorporated by reference.

BACKGROUND

Field of Disclosure

[0002] The present disclosure relates to a power converting technology, and more particularly, to a power converter and a method for manufacturing the same.

Description of Related Art

[0003] With the development of smart life technology, demands for data processing have been increased. The averaged energy consumption for data processing throughout the world achieves hundreds of billions of kilowatt-hours or even trillions of kilowatt-hours per year. Furthermore, a large data center is often has an occupied area up to ten thousands of square meters. Therefore, high efficiency and high power density are key factors for sustainable development of industry.

[0004] The key to the function of the data center is a server, where the motherboard usually consists of data processing chips such as CPU, chipsets and memory and their power supply source and essential peripheral components. The power supply needs for chips are power sources with low voltage and high current. Therefore, power sources for directly providing

power to chips are needed for reducing the effects of loss and resistance of output wires, and these power sources are called points of the load (POL).

[0005] According to various system architectures, the inputs of the POL include 12V, 48V or even 400V. Because of low voltage and high current of the POL, the volume and resistance of the pins thereof may have very direct effect on the power density and the efficiency of the POL power source. Therefore, how to design the pins is one of the keys for such kind of power converter. If wide application range is considered for designing the pins, the size of the power converter is larger, the cost is higher, and the power consumption is greater. If small size, low cost and low consumption of the power converter are considered for designing the pins, the application range becomes narrower.

[0006] In view of the foregoing, there exist problems and disadvantages in the existing products that await further improvement. However, those skilled in the art sought vainly for a solution.

SUMMARY

[0007] The following summary presents a simplified summary of the disclosure in order to provide a basic understanding to the reader. This summary is not an extensive overview of the disclosure and it does not identify key/critical elements of the present disclosure or delineate the scope of the present disclosure.

[0008] The present disclosure provides a power converter, which addresses the problem existed in the prior art.

[0009] Another technical aspect of the present disclosure is a power converter. The power converter includes a carrier, a first electronic component, a second electronic component and a first connection part. The carrier includes an upper surface and a lower surface, and the first connection part includes a first terminal and a second terminal. The first electronic component is disposed at the lower surface of the carrier, and the second electronic component is disposed at the upper surface of the carrier. The first terminal of the first connection part is electrically connected to the upper surface or the lower surface of the carrier. The second terminal of the first connection part is a bonding pad attached to a surface of the first electronic component apart from the carrier. The carrier is disposed at 1/3 to 2/3 of a height of the power converter. The first connection part is fabricated by mechanical support of the first electronic component.

[0010] Another technical aspect of the present disclosure is a method for manufacture a power converter, including the following steps: bonding a first electronic component on a lead frame which includes a retaining part and a connection part; cutting off the retaining part of the lead frame; curving the connection part by mechanical support of the first electronic component to fix the connection part at the first electronic component; connecting the first electronic component at a lower surface of a carrier; and bonding a second electronic component at an upper surface of the carrier to form the power converter, where the carrier is disposed at 1/3 to 2/3 of a height of the power converter.

[0011] Therefore, in view of the foregoing, embodiments of the present disclosure provide a power converter and a method for manufacturing the same to improve the problems associated with the difficulty in simultaneously considering wide application range, small size, low cost and low consumption.

[0012] These and other features, aspects, and advantages of the present disclosure, as well as the technical means and embodiments employed by the present disclosure, will become better understood with reference to the following description in connection with the accompanying drawings and appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The present disclosure can be more quite understood by reading the following detailed description of the embodiment, with reference made to the accompanying drawings as follows:

[0014] FIG. 1 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure.

[0015] FIG. 2 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure.

[0016] FIG. 3 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure.

[0017] FIG. 4 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure.

[0018] FIG. 5 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure.

[0019] FIG. 6 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure.

[0020] FIG. 7 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure.

[0021] FIG. 8 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure.

[0022] FIG. 9 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure.

[0023] FIG. 10 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure.

[0024] FIG. 11 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure.

[0025] FIG. 12 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure.

[0026] FIG. 13 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure.

[0027] FIG. 14 illustrates a partial schematic diagram of a power converter during a process in accordance with embodiments of the present disclosure.

[0028] FIG. 15 illustrates a partial schematic diagram of a power converter during a process in accordance with embodiments of the present disclosure.

[0029] FIG. 16 illustrates a partial schematic diagram of a power converter during a process in accordance with embodiments of the present disclosure.

[0030] FIG. 17 illustrates a schematic diagram of a portion of a power converter during a process in accordance with embodiments of the present disclosure.

[0031] FIG. 18 illustrates a schematic diagram of a portion of a power converter during a process in accordance with embodiments of the present disclosure.

[0032] FIG. 19 illustrates a schematic diagram of a portion of a power converter during a process in accordance with embodiments of the present disclosure.

[0033] FIG. 20 illustrates a schematic diagram of a portion of a power converter during a process in accordance with embodiments of the present disclosure.

[0034] FIG. 21 illustrates a schematic diagram of a portion of a power converter during a process in accordance with embodiments of the present disclosure.

[0035] FIG. 22 illustrates a schematic diagram of a portion of a power converter in accordance with embodiments of the present disclosure.

[0036] FIG. 23 illustrates a flowchart of a method of fabricating a power converter in accordance with embodiments of the present disclosure.

[0037] FIG. 24 illustrates a schematic diagram of a process of a power converter in accordance with embodiments of the present disclosure.

[0038] In accordance with common practice, the various described features/elements are not drawn to scale but instead are drawn to best illustrate specific features/elements relevant to the present disclosure. Also, like reference numerals and designations in the various drawings are used to indicate like elements/parts.

DETAILED DESCRIPTION

[0039] The detailed description provided below in connection with the appended drawings is intended as a description of the present examples and is not intended to represent the only forms in which the present example may be constructed or utilized. The description sets forth the functions of the example and the sequence of steps for constructing and operating the example. However, the same or equivalent functions and sequences may be accomplished by different examples.

[0040] Unless otherwise defined herein, scientific and technical terminologies employed in the present disclosure shall have the meanings that are commonly understood and used by one of ordinary skill in the art.

[0041] FIG. 1 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure. As shown in FIG. 1, the power converter 100 includes a carrier PCB, a first electronic component C1, a second electronic component C2, a first connection part P1 and a second connection part P2. Those skilled in the art will appreciate that, in the embodiment shown in FIG. 1, the power converter 100 includes the first connection part P1 and the second connection part P2. However, the present disclosure is not limited thereto. In another embodiment, the power converter 100 may only include the first connection part P1, and the second terminal Pad1 of the first connection part P1 is a bonding pad attached to a surface of the first electronic component C1 apart from the carrier PCB. Substantially, as can be known from FIG. 1, the terminal structure of the second connection part P2 and

the first connection part P1 is substantially the same or similar. Furthermore, the carrier PCB includes a top surface S1 and a bottom surface S2, the first connection part P1 includes a first terminal Pin1 and a second terminal Pad1, and the second connection part P2 includes a first terminal Pin2 and a second terminal Pad2. For implementing the present disclosure, the carrier PCB may be a printed circuit board, and the first connection part P1 and the second connection part P2 may be pins. However, the present disclosure is not limited thereto, which is only used for illustratively describe one of the ways for implementing the present disclosure.

[0042] With respect to structure, the first electronic component C1 is disposed at the bottom surface S2 of the carrier PCB, and the second electronic component C2 is disposed at the top surface S1 of the carrier PCB. The first terminal Pin1 of the first connection part P1 is connected to the bottom surface S2 of the carrier PCB, and at this time, the first connection part P1 and the carrier PCB are connected by using surface mount technology (SMT). Alternatively, in another embodiment, the first terminal Pin1 of the first connection part P1 is connected to the top surface S1 of the carrier PCB, and at this time, the first connection part P1 and the carrier PCB are connected by using insertion connection, for example, the carrier PCB has a through hole, the first terminal Pin1 inserts the carrier PCB from the bottom surface S2 to the top surface S1. The second terminal Pad1 of first connection part P1 is a bonding pad attached to the surface of the first electronic component C1 apart from the carrier PCB. As can be seen from the figure, the carrier PCB can be disposed at 1/3 to 2/3 of the height of the power converter. In addition, the first connection part P1 is fabricated by mechanical support of the first electronic component C1.

[0043] Moreover, the second terminal Pad1 of the first connection part P1 may be connected to an external device (not shown). Therefore, the external device may be electrically connected to the carrier PCB through the second terminal Pad1 and the first terminal Pin1 of the first connection part P1. Similarly, the first terminal Pin2 of the second connection part P2 is connected to the bottom surface S2 of the carrier PCB. Alternatively, in another embodiment, the first terminal Pin2 of the second connection part P2 is connected to the top surface S1 of the carrier PCB. The second terminal Pad2 of the second connection part P2 is a bonding pad attached to a surface of the first electronic component C1 apart from the carrier PCB. In addition, the second terminal Pad2 of the second connection part P2 can be used to connect with an external device (not shown). Therefore, the external device can be electrically connected with the carrier PCB through the second terminal Pad2 and the first terminal Pin2 of the second connection part P2. In addition, the second connection part P2 is fabricated by mechanical support of the first electronic component C1.

[0044] In another embodiment, a plurality of first electronic components (e.g. electronic components C1 and C4) may be attached on the bottom surface S2 of the carrier PCB, and a first height H1 is defined as the vertical height between a highest one of the first electronic components (e.g. the electronic component C1) and the bottom surface S2 of the carrier PCB. A plurality of second electronic components (e.g. electronic components C2, C3) may be attached on the top surface S1 of the carrier PCB, and a second height H2 is defined as the vertical height between a highest one of the second electronic components (e.g. the electronic component C2) and the top surface S1 of the

carrier PCB. The height of the power converter 100 is calculated by adding the first height H1, the second height H2 and the thickness H3 of the carrier PCB, and the carrier PCB is disposed at 1/3 to 2/3 of the height of the power converter. However, the power converter structure of the present disclosure is not limited to that shown in FIG. 1, which is only used for illustratively describe one of the ways for implementing the present disclosure.

[0045] In one embodiment, the connection parts P1 and P2 are fabricated by mechanical support of the first electronic component C1, and thus the gap between the connection parts P1 and P2 and the first electronic component C1 is close to zero. Moreover, the connection parts P1 and P2 are fabricated by mechanical support of the first electronic component C1, and thus the connection parts P1 and P2 themselves can be determined according to electrical requirements without additionally considering their mechanical strengths and mounting requirements. Therefore, according to embodiments of the disclosure, the connection parts P1 and P2 of the power converter have small body size, and the space needed for mounting is reduced accordingly, thereby substantially improving the space utilization ratio of the power converter to achieve higher power density. Furthermore, only electrical connection is considered for the size of the connection parts P1 and P2, and thus less consumption can be achieved. In addition, the size of the connection parts P1 and P2 is small, and thus the manufacture cost can be further reduced.

[0046] In another embodiment, the connection parts P1 and P2 may be directly bonded with the first electronic component C1 through an adhesive. In a further embodiment, the first electronic component C1 and the second

electronic component C2 are symmetric with respect to the carrier PCB. As such, the resource of the carrier PCB can be quite utilized, and the uniform strain distribution of throughout the converter can be benefited. Therefore, no additional strain solution is needed, for avoiding the problem of increasing of the power converter volume resulted from using an additional strain solution. In a further embodiment, the definition of the symmetry mentioned above may be that, the second height H2 is not greater than twice the first height H1, or the first height H1 is not greater than twice the second height H2. In one embodiment, the height of the first electronic component C1 equals to the height of the second electronic component C2.

[0047] In another embodiment, the connection parts P1 and P2 may use a lead frame and are fabricated by mechanical support of the first electronic component C1. In a further embodiment, the connection part P1, the connection part P2 and the carrier PCB are connected by using surface mount technology (SMT).

[0048] FIG. 2 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure. In comparison with the power converter 100 shown in FIG. 1, the connection parts P1, P2 and the carrier PCB of the power converter 200 of FIG. 2 are connected by using insertion connection. For example, the connection parts P1 and P2 are connected to the first electronic component C1, and the connection parts P1 and P2 penetrate through the carrier PCB for being connected to the second electronic component C2. If the surface mount technology for the connection parts P1, P2 and the carrier PCB shown in FIG. 1 is replaced by the insertion

connection shown in FIG. 2, the connection between the connection parts P1, P2 and the carrier PCB can be more stable, so as to reduce the transmission loss from the carrier PCB to the connection parts P1 and P2, and such connection may be adapted to the conditions with low voltage and high current. In addition, as shown in FIG. 2, the connection part P2 may be at the outermost side of the carrier PCB, i.e., the outermost side of the power converter 200. As such, the area of the carrier PCB can be further reduced, so as to improve the power density.

[0049] In another embodiment, an electrical connection is not necessarily required between the connection parts P1, P2 and the first electronic component C1, and thus the first electronic component C1 may be an entire electronic component, such as a metal oxide semiconductor field effect transistor (MOSFET) or an integrated circuit. In addition, the first electronic component C1 may also be an entire combination of electronic components, such as a power module. Moreover, the first electronic component C1 may also include a part of a core of the magnetic element. In a further embodiment, the first electronic component C1, the second electronic component C2 and the carrier PCB are used to form an inductor element, and the first electronic component C1 and the second electronic component C2 are respectively parts of a core of the inductor element. At this time, the power converter 200 is a boost circuit or a buck circuit.

[0050] In a further embodiment, the first electronic component C1, the second electronic component C2 and the carrier PCB are used to form a transformer, and the first electronic component C1 and the second electronic component C2

are respectively parts of a core of the transformer. For example, the power converter 200 may be an isolated DC/DC converter.

[0051] FIG. 3 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure. In comparison with the power converter 100 shown in FIG. 1, the power converter 300 of FIG. 3 further includes a third electronic component C1' and a fourth electronic component C2' respectively disposed at the bottom surface S2 and the top surface S1 of the carrier PCB, where the third electronic component C1', the fourth electronic component C2' and the carrier PCB are used to form a transformer, and the third electronic component C1' and the fourth electronic component C2' are respective parts of a core of the transformer.

[0052] FIG. 4 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure. In comparison with the power converter 300 shown in FIG. 3, the power converter 400 in FIG. 4 includes a plurality of first connection parts P1 and a plurality of second connection parts P2, where each of the first connection parts P1 includes a first terminal Pin1 and a second terminal Pad1, and each of the second connection part P2 includes a first terminal Pin2 and a second terminal Pad2. With respect to structure, the first terminals Pin1 of the first connection parts P1 are respectively connected to the first electronic component C1 and the third electronic component C1', and are connected to the carrier PCB. The second terminal Pad1 of the first connection part P1 is used to connect with an external device (not shown). The first terminals Pin2 of the second connection parts P2 are respectively connected to the first electronic component C1 and the third

electronic component C1', and are connected to the carrier PCB. The second terminal Pad2 of the second connection part P2 is used to connect with an external device (not shown). As can be seen from the drawing, the power converter structure of the present disclosure is symmetric, and thus manufacturing of the first connection part P1 and the second connection part P2 of the power converter is simpler. In addition, as the power converters 300 and 400 shown in FIG. 3 and FIG. 4, in the present disclosure, the first connection part P1 and the second connection part P2 can be selectively fabricated on a single component (e.g. the first electronic component C1) or on several components (e.g. the first electronic component C1 and the third electronic component C1') according to practical needs.

[0053] In another embodiment, the third electronic component C1' and the fourth electronic component C2' form a core of the transformer through the carrier PCB. In a further embodiment, the third electronic component C1' and the fourth electronic component C2' form an inductor core through the carrier PCB.

[0054] In a further embodiment, if the first electronic component C1 and the second electronic component C2 form a core of the transformer and the third electronic component C1' and the fourth electronic component C2' form an inductor core, the power converter 400 includes an isolated DC/DC transformer and a buck power converter, thereby forming a two-stage architecture. Such architecture is suitable to a high input/output condition, such as 48V and 400V.

[0055] FIG. 5 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure. In comparison with

the power converter 200 shown in FIG. 2, the power converter 500 of FIG. 5 further includes at least one insertion pin (e.g. Pin1' or Pin2') installed at the second terminal Pad1 of the first connection part P1 for converting bonding pad connection into insertion connection.

[0056] FIG. 6 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure. In comparison with the power converter 500 shown in FIG. 5, in the power converter 600 of FIG. 6, the second terminals Pad1 and Pad2 of the connection parts P1 and P2 respectively correspond to the insertion pins Pin1' and Pin2', and the insertion pins Pin1' and Pin2' are fixed through the bracket 610. This is because the mutual location between the insertion pins Pin1' and Pin2' disposed simultaneously is more difficult. Therefore, the bracket 610 may be used to prefix the insertion pins Pin1' and Pin2', and then the insertion pins Pin1' and Pin2' are disposed on the connection parts P1 and P2 simultaneously. As such, the manufacturing difficulty can be simplified, and the accuracy may be effectively controlled.

[0057] FIG. 7 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure. In comparison with the power converter 600 shown in FIG. 6, the power converter 700 of FIG. 7 further includes a bonding layer 710, and the bonding layer 710 may be used to bond the first electronic component C1 and the bracket 610, so as to prevent the insertion pins Pin1' and Pin2' from detaching when in use. In one embodiment, the connection part P1 or the connection part P2 may be fabricated by using a lead frame.

[0058] FIG. 8 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure. As shown in FIG. 8, the power converter 800 is a symmetric structure, e.g., the first electronic component C1 and the second electronic component C2 are symmetric with respect to the carrier PCB, and thus the power converter 800 is suitable for a molding process, making the structure of power converter 800 more rigid and reliable and has better heat dissipation ability.

[0059] FIG. 9 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure. In comparison with FIG. 8, in FIG. 9, a grinding process is performed on a molding material 910 on the power converter 900, until a part of the power converter 900 is externally exposed. For example, the grinding process is performed until the second electronic component C2 is exposed, for further reducing the size and improving the heat dissipation ability of the power converter 900.

[0060] FIG. 10 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure. As shown in FIG. 10, the first electronic component C1 includes a first surface S3 and a second surface S4, and the first surface S3 of the first electronic component C1 is disposed at the bottom surface S2 of the carrier PCB. In addition, the power converter further includes a chip IC disposed at the second surface S4 of the first electronic component C1 (i.e. disposed at the surface of the first electronic component C1 apart from the carrier PCB). Moreover, the chip IC includes one or more pins (e.g. the pin Pin3), and as such, signals of the chip IC may be

transmitted through the first connection part P1 and the second connection part P2 or through one or more pins (e.g. the pin Pin3).

[0061] FIG. 11 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure. As shown in FIG. 11, the power converter 1100 further includes a flexible printed circuit board FPCB disposed at an external side of the first connection part P1. A terminal Pad3 of the flexible printed circuit board FPCB is connected to the carrier PCB, and the other terminal Pad4 may be mechanically connected to the second terminal Pad1 of the first connection part P1, for example, the second terminal Pad1 is used to provide mechanical support for the terminal Pad4 of the flexible printed circuit board FPCB. In addition, the terminal Pad4 may be also electrically connected to the second terminal Pad1 so as to transmit signal therebetween. Because signal can be transmitted from the carrier PCB to the second terminal Pad1 of the first connection part P1 by the flexible printed circuit board FPCB, the problem of more signal pins can be solved. In addition, the other terminal Pad4 of the flexible printed circuit board FPCB can be connected to an external device (not shown), and thus the flexible printed circuit board FPCB can be used as a connector for connecting the carrier PCB and an external device. In a further embodiment, the flexible printed circuit board FPCB may be mounted at the carrier PCB through an anisotropic conductive film ACF. Because the anisotropic conductive film ACF is anisotropic conductive, if the anisotropic conductive film ACF is used to connect the flexible printed circuit board FPCB and the carrier PCB, multi-signal connection with high accuracy can be realized.

[0062] FIG. 12 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure. In comparison with the power converter 200 shown in FIG. 2, the power converter 1200 of FIG. 12 further includes at least an electronic component C5 and/or C6 embedded in the carrier PCB, and thus the space utilization ratio can be further improved.

[0063] FIG. 13 illustrates a schematic diagram of a power converter in accordance with embodiments of the present disclosure. As shown in FIG. 13, the first terminal Pin1 of first connection part P1 of the first electronic component C1 and the carrier PCB is connected by insertion connection, and the step of forming the insertion structure is as the following: forming a hole in the carrier PCB to make the first terminal Pin1 of the first connection part P1 penetrate through the carrier PCB; and disposing a solder block 1310 on the hole of the carrier PCB, so as to solve the problem of tin insufficiency. The reason of tin insufficiency is that, the other components on the carrier PCB are usually surface mount devices (SMD), and the soldering tin is disposed for stencil printing. Because the distance between the components could be very short, an excessive amount of soldering tin had not better to be used for ensuring solder quality; that is, the plate is made thinner and is usually between 0.1-0.2 mm. If the first terminal Pin1 and the carrier PCB is insertion connection, the hole on the carrier PCB corresponding to the first terminal Pin of the first connection part P1 needs to be bored wider for convenient installation. For example, the diameter of the hole is 2 mm greater than the diameter of the first terminal Pin1 of the first connection part P1. As such, the soldering tin for stencil printing is not sufficient to fill a gap 1320 between the first terminal Pin1 of the first connection part P1 and the hole, resulting in an excessive contact

resistance. Therefore, the solder block 1310 with a corresponding volume is disposed on the hole, to compensate for tin insufficiency. It should be noted that, FIG. 13 shown a manufacturing process, the solder block 1310 has been filled into the gap 1320 in the end, and practically the solder block 1310 does not exist on the power converter 1300.

[0064] Please refer to FIG. 4, the power converter 400 may include a plurality of first terminals Pin1 and second terminals Pad1 of the first connection part P1 and a plurality of first terminals Pin2 and second terminals Pad2 of the second connection part P2, and thus the flatness of the first terminal Pin1 and the second terminal Pad1 of the first connection part P1 and the first terminal Pin2 and the second terminal Pad2 of the second connection part P2 needs to be ensured when manufacturing the power converter 400 of FIG. 4. For ensuring the flatness, the present disclosure provides a set of manufacturing processes described accompanying with FIGs. 14-22.

[0065] FIGs. 14-22 illustrate schematic diagrams of a portion of a power converter during a process in accordance with embodiments of the present disclosure. As shown in FIG. 14, the first electronic component C1, the first connection part P1 and the second connection part P2 of the power converter are prepared in advance and are combined into a combination structure. As shown in FIG. 15, the components electrically connected to the bottom surface S2 of the carrier PCB are installed/soldered onto the bottom surface S2 of the carrier PCB through SMT in advance. As shown in FIG. 16, glue is coated between the combination structure and the carrier PCB for corresponding inserting the combination structure into the carrier PCB and connecting the

combination structure and the carrier PCB by a panel B1 of the lower surface of the combination structure with viscosity, and the flatness of the combination structure can be ensured. The first electronic component C1 of the combination structure may be a magnetic element, and thus the panel B1 may be a magnetic sucker, for generating suction between the panel B1 and the first electronic component C1 to benefit packaging. Afterwards, the glue is heated and solidified to fix the combination structure and the carrier PCB, thereby ensuring the flatness of the overall structure. After the packaging, the panel B1 may be removed depending on conditions. As shown in FIG. 17, solder paste 1710 is brushed at the surface of the carrier PCB, each component is placed, and then a soldering process is performed. As shown in FIG. 18, the second electronic component C2 is attached to the upper surface of the carrier PCB.

[0066] The power converter is completed at the step of FIG. 18, and if the molding process does not need to be performed, each power converter is obtaining by separating the pieces. If the molding process needs to be performed continuously, the processes of FIGs. 19-22 are performed continuously.

[0067] As shown in FIG. 19, the molding process is performed with the periphery of the pieces being a pivot. The power converter of embodiments of the present disclosure is a symmetric structure, and thus the arrangement of mold cavities is quite regular, such that the mold cost is low and the molding flow is easy to be controlled, and the manufacturing yield is high, for further reducing the cost. As shown in FIG. 20, after the molding process, the glue of

the lower surface may be removed by a process such as grinding, for ensuring the solderability of the lower surface. In addition, a tin plating process or a gold plating process may be performing after removing the glue, for improving the solderability of the lower surface. As shown in FIG. 21, the second electronic component C2 may be exposed by performing a grinding process to grind off the above molding material. As such, the extra volume from the molding process to the power converter can be greatly reduced. In addition, the exposed of the second electronic component C2 through a grinding process is quite flat, which is beneficial for installing a heat dissipator thereon, and the heat dissipation effect is better. As shown in FIG. 22, the power converter is separated to obtain a molded power converter by a cutting process. In addition, the cutting position can be adjusted to expose an external side of the second connection part P2 of the power converter, thereby reducing the volume of the power converter of overall molding.

[0068] FIG. 23 illustrates a flowchart of a method of fabricating a power converter in accordance with embodiments of the present disclosure. As shown in FIG. 23, the method 2300 for manufacturing a power converter of the present disclosure includes the following steps:

[0069] Step 2310: bonding a first electronic component on a lead frame, where the lead frame comprises a retaining part and a connection part;

[0070] Step 2320: cutting off the retaining part of the lead frame;

[0071] Step 2330: curving the connection part by mechanical support of the first electronic component to fix the connection part at the first electronic component;

[0072] Step 2340: connecting the first electronic component at a lower surface of the carrier; and

[0073] Step 2350: bonding a second electronic component at an upper surface of the carrier to form the power converter, where the carrier is disposed at 1/3 to 2/3 of the height of the power converter.

[0074] For facilitating understanding of the method for manufacturing the power converter of embodiments of the present disclosure, please also refer to FIG. 23 and FIG. 24, FIG. 24 illustrates a schematic diagram of a process of a power converter in accordance with embodiments of the present disclosure. In step 2310, please refer to the process 2430 of FIG. 24, the first electronic component C1 is mounted on a lead frame 2480, where the lead frame 2480 includes a retaining part 2460 and a connection part 2470. In step 2320, please refer to the process 2440 of FIG. 24, the retaining part 2460 of the lead frame 2480 is cut off, and only the connection part 2470 of the lead frame 2480 is left. In step 2330, please refer to the process 2450 of FIG. 24, the connection part 2470 is curved by mechanical support of the first electronic component C1, for the connection part 2470 to be fixed at the first electronic component C1. The upper and lower figures of process 2450 of FIG. 24 are respectively used to show the upper and lower surfaces of the first electronic component C1.

[0075] For facilitating understanding of the method for manufacturing the power converter of embodiments of the present disclosure, please also refer to FIG. 23, FIG. 16 and FIG. 18, in step 2340, please refer to FIG. 16 and related description, the first electronic component C1 is mounted at the lower surface of

the carrier PCB. In step 2350, please refer to FIG. 18 and related description, the second electronic component C2 is mounted at an upper surface of the carrier PCB to form power converter, where the carrier PCB is disposed at 1/3 to 2/3 of the height of the power converter.

[0076] In one embodiment, please refer to FIG. 1, in the power converter 100 fabricated by the method 2300 of the present disclosure, the connection parts P1 and P2 are fabricated by mechanical support of the first electronic component C1, and thus the gap between the connection parts P1, P2 and the first electronic component C1 is close to zero. In another embodiment, the connection parts P1 and P2 may be directly bonded with the first electronic component C1 through an adhesive.

[0077] In a further embodiment, the first electronic component C1 and the second electronic component C2 are symmetric with respect to the carrier PCB. As such, the resource of the carrier PCB can be quite utilized, and the uniform strain distribution of throughout the converter can be benefited. Therefore, no additional strain solution is needed, for avoiding the problem of increasing of the power converter volume resulted from using an additional strain solution.

[0078] In a further embodiment, in comparison with the power converter 100 shown in FIG. 1, in the power converter 200 of FIG. 2 fabricated by the method 2300, the connection parts P1, P2 and the carrier PCB are connected by using insertion connection. For example, the connection parts P1 and P2 are connected to the first electronic component C1, and the connection parts P1 and P2 penetrate through the carrier PCB for being connected to the second electronic component C2. If the surface mount technology(SMT) for the

connection parts P1, P2 and the carrier PCB shown in FIG. 1 is replaced by the insertion connection manner shown in FIG. 2, the connection between the connection parts P1, P2 and the carrier PCB can be more stable, so as to reduce the transmission loss from the carrier PCB to the connection parts P1 and P2, and such connection may be adapted to the conditions with low voltage and high current.

[0079] In a further embodiment, an electrical connection is not necessarily required between the connection parts P1, P2 and the first electronic component C1, and thus the first electronic component C1 may be an entire electronic component, such as a MOSFET or an integrated circuit. In addition, the first electronic component C1 may also be an entire combination of electronic components, such as a power module. Moreover, the first electronic component C1 may also include a part of a core of the magnetic element. In a further embodiment, the first electronic component C1, the second electronic component C2 and the carrier PCB are used to form an inductor element, and the first electronic component C1 and the second electronic component C2 are respectively parts of a core of an inductor element, and at this time, the power converter 200 is a boost circuit or a buck circuit.

[0080] In a further embodiment, the first electronic component C1, the second electronic component C2 and the carrier PCB are used to form a transformer, the first electronic component C1 and the second electronic component C2 are respectively parts of a core of the transformer.

[0081] In a further embodiment, in comparison with the power converter 100 shown in FIG. 1, the power converter 300 of FIG. 3 fabricated by the method

2300 further includes a third electronic component C1' and a fourth electronic component C2' respectively disposed at the bottom surface S2 and the top surface S1 of the carrier PCB, wherein the third electronic component C1', the fourth electronic component C2' and the carrier PCB are used to form a transformer, and the third electronic component C1' and the fourth electronic component C2' are respectively parts of a core of the transformer.

[0082] In a further embodiment, in comparison with the power converter 300 shown in FIG. 3, the power converter 400 of FIG. 4 fabricated by the method 2300 includes a plurality of first connection parts P1 and a plurality of second connection parts P2, where each of the first connection parts P1 includes a first terminal Pin1 and a second terminal Pad1, and each of the second connection parts P2 includes a first terminal Pin2 and a second terminal Pad2. With respect to structure, the first terminals Pin1 of the first connection parts P1 are respectively connected to the first electronic component C1 the third electronic component C1', and are connected to the carrier PCB. The second terminal Pad1 of the first connection part P1 is used to connect with an external device (not shown). The first terminals Pin2 of the second connection parts P2 are respectively connected to the first electronic component C1 and the third electronic component C1', and are connected to the carrier PCB. The second terminal Pad2 of the second connection part P2 is used to connect with an external device (not shown). As can be seen from the drawing, the power converter structure of the present disclosure is symmetric, and thus manufacturing of the first connection part P1 and the second connection part P2 of the power converter is simpler. In addition, as the power converters 300 and 400 shown in FIG. 3 and FIG. 4, in the present disclosure, the first

connection part P1 and the second connection part P2 can be selectively fabricated on a single component (e.g. the first electronic component C1) or on several components (e.g. the first electronic component C1 and the third electronic component C1') according to practical needs.

[0083] In a further embodiment, the third electronic component C1' and the fourth electronic component C2' form a core of the transformer through the carrier PCB. In a further embodiment, the third electronic component C1' and the fourth electronic component C2' form an inductor core through the carrier PCB.

[0084] In a further embodiment, if the first electronic component C1 and the second electronic component C2 form a core of the transformer, and the third electronic component C1' and the fourth electronic component C2' form an inductor core, the power converter 400 includes an isolated DC/DC transformer and a buck power converter, thereby forming a two-stage architecture. Such architecture is suitable to a high input/output condition, such as 48V and 400V.

[0085] In a further embodiment, please refer to FIG. 5, the method 2300 for manufacturing a power converter of the present disclosure further includes: bonding insertion pins Pin1' and Pin2' at the connection parts P1 and P2. The insertion pins Pin1' and Pin2' are used to connect with an external device (not shown).

[0086] In a further embodiment, please refer to FIG. 6, the method 2300 for manufacturing a power converter of the present disclosure further includes: using a bracket 610 to fix the insertion pins Pin1' and Pin2'. The above step is added because the mutual location between the insertion pins Pin1' and Pin2'

disposed simultaneously is more difficult. Therefore, the bracket 610 may be used to prefix the insertion pins Pin1' and Pin2', and then the insertion pins Pin1' and Pin2' are disposed on the connection parts P1 and P2 simultaneously. As such, the manufacturing difficulty can be simplified, and the accuracy may be effectively controlled. In another embodiment, please refer to FIG. 7, the method 2300 for manufacturing a power converter of the present disclosure further includes: using a bonding layer 710 to bond the first electronic component C1 and the bracket 610. As such, the insertion pins Pin1' and Pin2' can be prevented from detaching when in use.

[0087] In a further embodiment, please refer to FIG. 8, the method 2300 for manufacturing a power converter of the present disclosure further includes: performing a molding process to the power converter 800. The power converter 800 is a symmetric structure, and thus the power converter 800 is suitable for a molding process, making the structure of power converter 800 more rigid and reliable and has better heat dissipation ability. Please refer to FIG. 9, the method 2300 for manufacturing a power converter of the present disclosure further includes: performing a grinding process on a molding material 910 on the power converter 900, until a part of the power converter 900 is externally exposed. For example, the grinding process is performed on the molding material 910 on the power converter 900 to expose the second electronic component C2 and/or the first electronic component C1. Alternatively, the grinding process is performed on the molding material 910 on the power converter 900 to expose an outer side of the connection part P2, for further reducing the size and improving the heat dissipation ability of the power converter 900.

[0088] In a further embodiment, please refer to FIG. 10, the step of bonding the first electronic component C1 at the lower surface of the carrier PCB described in step 2340 includes: bonding the first surface S3 of the first electronic component C1 at the bottom surface S2 of the carrier PCB. In addition, the method 2300 for manufacturing a power converter of the present disclosure further includes: disposing a chip IC at the first electronic component C1 of the second surface S4 with glue (i.e. disposing at a surface of the first electronic component C1 apart from the carrier PCB); and disposing one or more pins (e.g. the pin Pin3) at a surface of the chip IC. As such, signals of the chip IC may be transmitted through the first connection part P1 and the second connection part P2 or through one or more pins (e.g. the pin Pin3).

[0089] In a further embodiment, please refer to FIG. 11, the connection part P1 includes a first terminal Pin1 and a second terminal Pad1, the method 2300 for manufacturing a power converter of the present disclosure further includes: disposing a flexible printed circuit board FPCB to connect the carrier PCB and the second terminal Pad1 of the connection part P1. Because signal can be transmitted from the carrier PCB to second terminal Pad1 of the first connection part P1 by the flexible printed circuit board FPCB, the problem of more signal pins can be solved. In addition, the flexible printed circuit board FPCB can be used as a connector for connecting the carrier PCB and an external device. Moreover, the aforementioned step of connecting the carrier PCB and the connection part P1 through the flexible printed circuit board FPCB includes: mounting the flexible printed circuit board FPCB at the carrier PCB through an anisotropic conductive film ACF. Because the anisotropic conductive film ACF is anisotropic conductive, if the anisotropic conductive film ACF is used to

connect the flexible printed circuit board FPCB and the carrier PCB, multi-signal connection with high accuracy can be realized.

[0090] In a further embodiment, please refer to FIG. 12, the method 2300 for manufacturing a power converter of the present disclosure further includes: embedding the electronic component C5 and/or C6 in the carrier PCB. As such, the space utilization ratio can be further improved.

[0091] In a further embodiment, in the method 2300 for manufacturing the power converter 1300, the first terminal Pin1 of first connection part P1 of the first electronic component C1 and the carrier PCB is connected by using insertion connection. The step of forming the insertion structure is as the following: boring a hole in the carrier PCB for the first terminal Pin1 of the first connection part P1 to penetrate the carrier PCB through the hole; disposing a solder block 1310 on the hole of the carrier PCB; and using wave soldering or reflow soldering to fill the hole with the solder block 1310 to compensate for tin insufficiency. It should be noted that, FIG. 13 shown a manufacturing process, the solder block 1310 has been filled into the gap 1320 in the end, and actually the solder block 1310 does not exist on the power converter 1300.

[0092] In a further embodiment, please refer to FIG. 16, the first electronic component C1 is a magnetic element, and the method 2300 for manufacturing the power converter further includes: coating glue at a connecting position between the magnetic element C1 and the carrier PCB; providing a magnetic sucker B1 at a surface of the magnetic element C1 apart from the carrier PCB; sucking the magnetic element C1 and the connection part P1 by adhesive

power generated by the magnetic sucker B1; heating and solidifying the coated glue to locate the magnetic element C1 and the carrier PCB.

[0093] Those skilled in the art will appreciate that each of the steps of the method 2300 for manufacturing the power converter named after the function thereof is merely used to describe the technology in the embodiment of the present disclosure in detail, but the present disclosure is not limited in this regard. Therefore, combining the steps of said method into one step, dividing the steps into several steps, or rearranging the order of the steps is within the scope of the embodiment in the present disclosure.

[0094] In view of the above embodiments of the present disclosure, it is apparent that the application of the present invention has the advantages as follows. In view of the foregoing, embodiments of the present disclosure provide a power converter and a method for manufacturing the same to improve the problems associated with the difficulty in simultaneously considering wide application range, small size, low cost and low consumption.

[0095] In addition, the power converter of the present disclosure is suitable for high power density and high efficiency condition, such as the condition in which the power density higher than 300 W/inch^3 and the efficiency higher than 90%. The operating frequency of the power converter of the present disclosure can be higher than 500 KHz, and the input voltage range can be between 1V-400 V. However, the method for realizing the power converter of the present disclosure is not limited to the abovementioned embodiments, which are only used for illustratively describe one of the ways for implementing the present disclosure.

[0096] Moreover, in comparison with the known art, the power converter and the method for manufacturing the same of embodiments of the present disclosure, especially the method for manufacturing the connection parts P1 and P2, have better electrical performance and thermal performance and higher power density. Furthermore, the space can be quite used and the manufacture is convenient, which are beneficial to improve the power density or the efficiency of the power converter. In addition, the concrete structure, manufacturing technique and processes shown in embodiments of the present disclosure are also quite feasible and effective. Therefore, embodiments of the present disclosure are quite suitable for improving the overall performance and the capability to price ratio of the power converter, especially the overall performance and the capability to price ratio of the POL.

[0097] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the disclosure without apart from the scope or spirit of the present disclosure. In view of the foregoing, it is intended that the present disclosure cover modifications and variations of this disclosure provided they fall within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A power converter, comprising:

a carrier, comprising:

an upper surface; and

a lower surface;

a first electronic component disposed at the lower surface of the carrier;

a second electronic component disposed at the upper surface of the carrier; and

a first connection part, comprising:

a first terminal electrically coupled to the upper surface or the lower surface of the carrier; and

a second terminal attached to a surface of the first electronic component apart from the carrier, wherein the second terminal of the first connection part is a bonding pad;

wherein the carrier is disposed at 1/3 to 2/3 of a height of the power converter, and wherein the first connection part is fabricated by mechanical support of the first electronic component.

2. The power converter of claim 1, further comprising a plurality of first electronic components and a plurality of second electronic components, wherein a first height is defined as a vertical height between the highest one of the first electronic components and the lower surface of the carrier, a second height is defined as a vertical height between the highest one of the second electronic components and the upper surface of the carrier, and the height of

the power converter is calculated by adding the first height, the second height and thickness of the carrier.

3. The power converter of claim 1, wherein a height of the first electronic component is equal to a height of the second electronic component.

4. The power converter of claim 1, wherein the first electronic component, the second electronic component and the carrier are used to form an inductive element, and the first electronic component and the second electronic component are respectively parts of a core of the inductive element.

5. The power converter of claim 4, further comprising:

a third electronic component and a fourth electronic component respectively disposed at the lower surface and the upper surface of the carrier;

wherein the third electronic component, the fourth electronic component and the carrier are used to form a transformer, and the third electronic component and the fourth electronic component are respectively parts of the core of the transformer.

6. The power converter of claim 1, wherein the first electronic component, the second electronic component and the carrier are used to form a transformer, and the first electronic component and the second electronic component are respectively parts of a core of the transformer.

7. The power converter of claim 1, wherein the power converter further comprises insertion pins installed at the second terminal of the first connection part for converting SMT connection to insertion connection.

8. The power converter of claim 7, further comprising a plurality of first connection parts, wherein the second terminal of the first connection parts respectively corresponds to the insertion pins, and the insertion pins are fixed through a bracket.

9. The power converter of claim 1, further comprising:

a chip disposed at the surface of the first electronic component apart from the carrier, wherein the surface of the chip has one or more pins.

10. The power converter of claim 1, further comprising:

a flexible printed circuit board disposed at the outer side of the first connection part, wherein one terminal of the flexible printed circuit board is connected to the carrier, the other terminal of the flexible printed circuit board is connected to the second terminal of the first connection part.

11. The power converter of claim 1, further comprising at least an electronic element embedded in the carrier.

12. A method for manufacturing a power converter, comprising:

bonding a first electronic component on a lead frame, wherein the lead frame comprises a retaining part and a connection part;

cutting off the retaining part of the lead frame;

curving the connection part by mechanical support of the first electronic component to fix the connection part at the first electronic component;

connecting the first electronic component at a lower surface of a carrier; and

bonding a second electronic component at an upper surface of the carrier to form the power converter, wherein the carrier is disposed at 1/3 to 2/3 of a height of the power converter.

13. The method of claim 12, wherein the connection part is directly bonded with the first electronic component through an adhesive.

14. The method of claim 12, further comprising:

penetrating the connection part through the carrier, and connecting the connection part to the second electronic component .

15. The method of claim 14, wherein the step of penetrating the connection part through the carrier comprises:

forming a hole in the carrier to make the connection part penetrate through the carrier;

disposing a solder block on the hole of the carrier; and

filling the hole with the solder block by wave soldering or reflow soldering.

16. The method of claim 12, wherein the first electronic component, the second electronic component and the carrier are used to form an inductive element, and the first electronic component and the second electronic component are respectively parts of a core of the inductive element.

17. The method of claim 12, wherein the first electronic component, the second electronic component and the carrier are used to form a transformer, and the first electronic component and the second electronic component are respectively parts of a core of the transformer.

18. The method of claim 12, further comprising:

bonding an insertion pin at a terminal of the connection part.

19. The method of claim 12, further comprising:

bonding a first surface of the first electronic component at the lower surface of the carrier;

disposing a chip at a second surface of the first electronic component with glue; and

disposing one or more pins at a surface of the chip.

20. The method of claim 12, further comprising:

disposing a flexible printed circuit board to connect the carrier and a second terminal of the connection part.

21. The method of claim 12, further comprising:

performing a molding process on the power converter; and

performing a grinding process on a molding material on the power converter, until a part of the power converter is externally exposed.

22. The method of claim 12, wherein the first electronic component is a magnetic element, the method further comprising:

coating glue at a connecting position between the magnetic element and the carrier;

providing a magnetic sucker at a surface of the magnetic element apart from the carrier;

sucking the magnetic element and the connection part by adhesive power generated by the magnetic sucker; and

heating and solidifying the coated glue to locate the magnetic element and the carrier.

23. The method of claim 22, further comprising:

performing a molding process on the power converter; and

performing a grinding process on a molding material of the power converter to expose the second electronic component and/or the first electronic component .

24. The method of claim 22, further comprising:

performing a molding process on the power converter; and

performing a grinding process on a molding material on the power converter to expose an outer side of the connection part.

ABSTRACT OF THE DISCLOSURE

A power converter includes a carrier, a first electronic component, a second electronic component, and a connection part. The first electronic component is disposed on the bottom surface of the carrier. The second electronic component is disposed on the top surface of the carrier. A first terminal of the connection part is coupled to the top surface or the bottom surface of the carrier. A second terminal of the connection part is a bonding pad and attached to the first electronic component's surface apart from the carrier. The carrier is disposed at 1/3 to 2/3 of a height of the power-converter. The connection part is fabricated by mechanical support of the first electronic component.

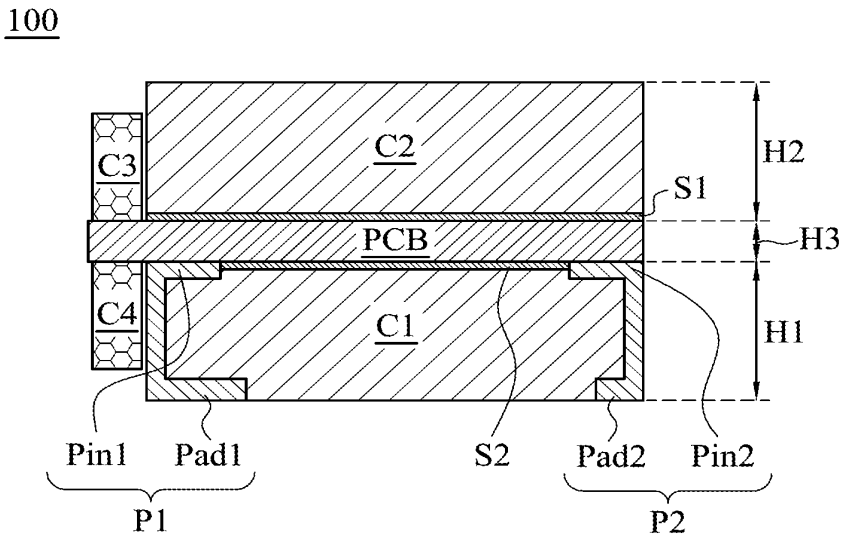

100
C2
C3
S1
H2
PCB
H3
C4
C1
H1
Pin1
Pad1
S2
Pad2
Pin2
P1
P2

Fig. 1

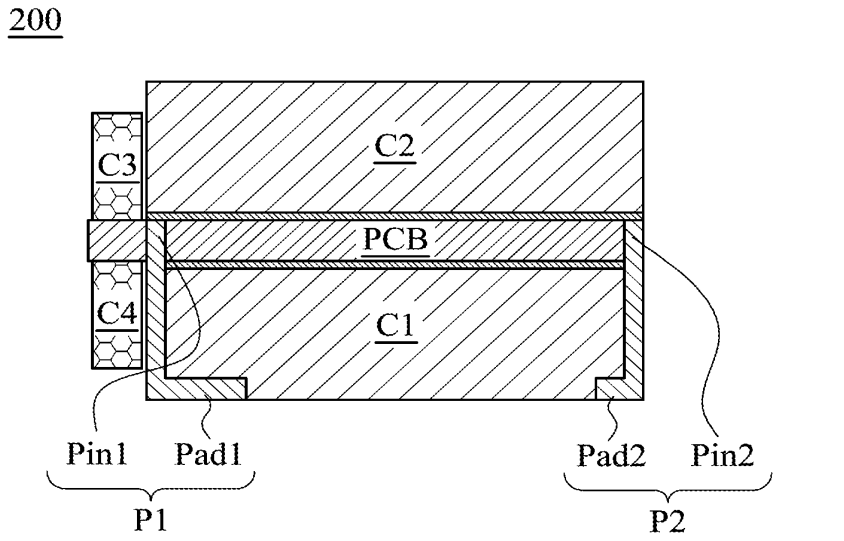

200
C2
C3
PCB
C4
C1
Pin1
Pad1
Pad2
Pin2
P1
P2

Fig. 2

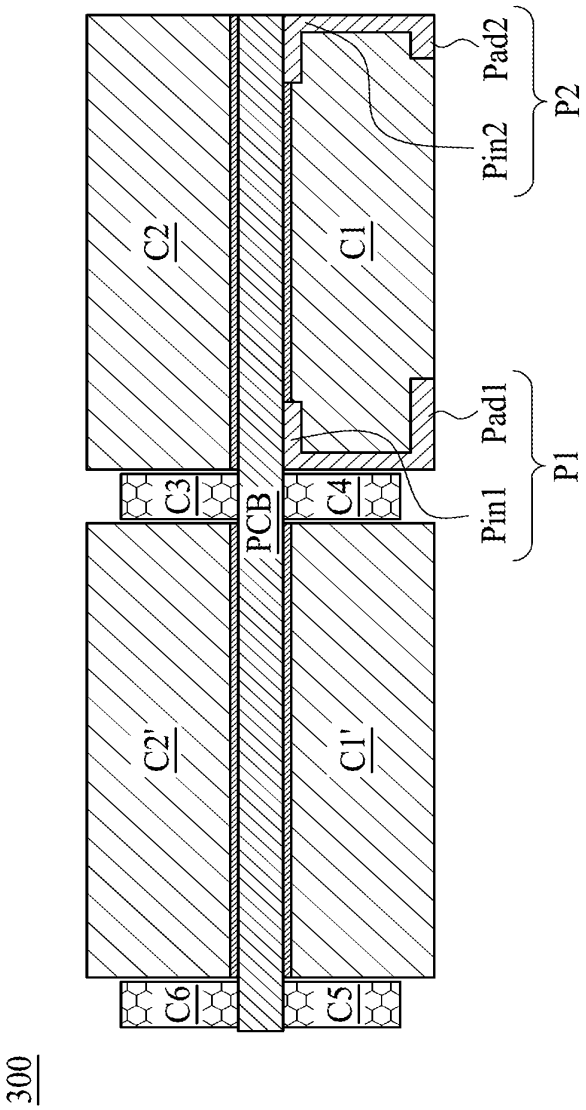


Fig. 3

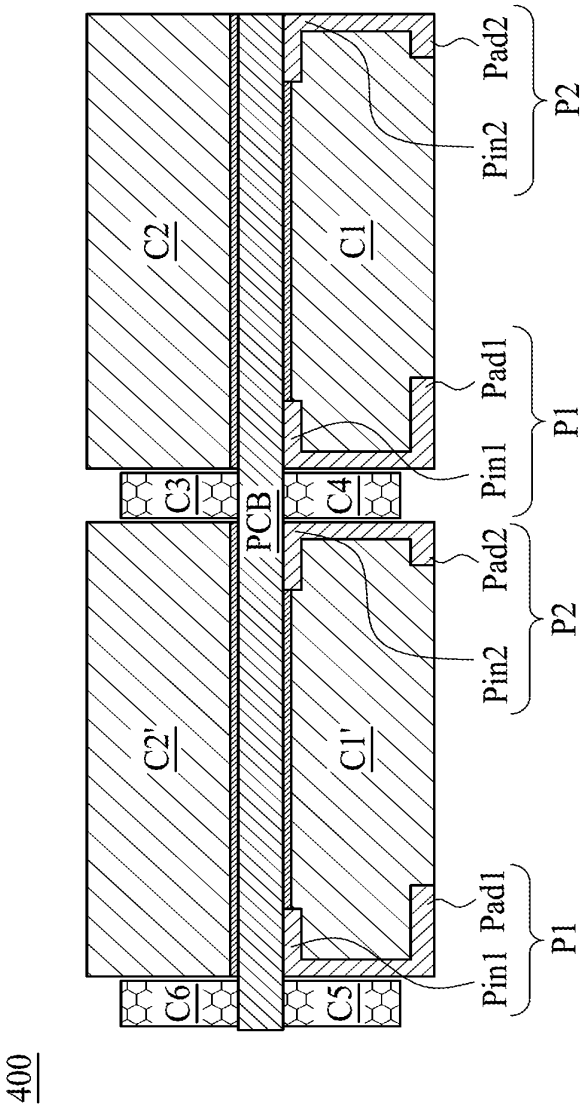

400
C2
C1
C3
C4
PCB
C2'
C1'
C6
C5
Pad2
Pin2
P2
Pad1
Pin1
P1
Pad2
Pin2
P2
Pad1
Pin1
P1

Fig. 4

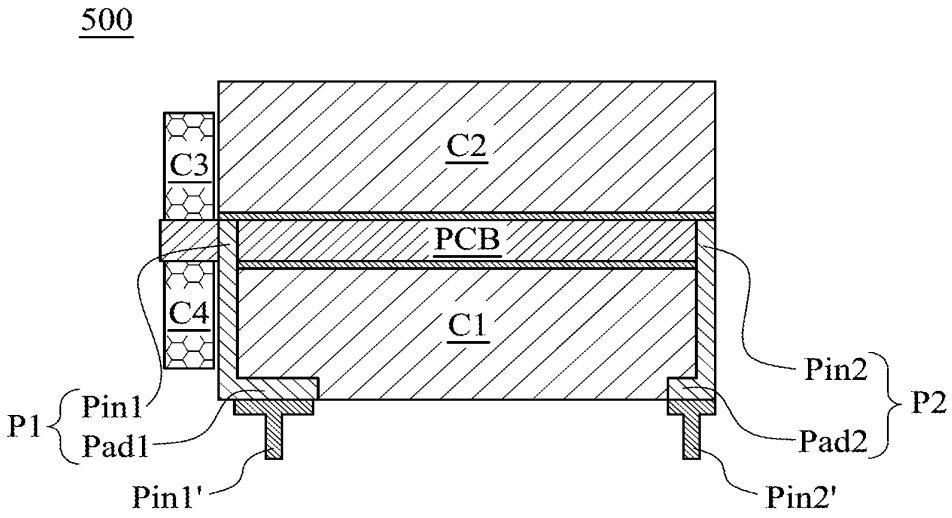

500
C2
C3
PCB
C4
C1
Pin2
P2
P1
Pin1
Pad1
Pad2
Pin1'
Pin2'

Fig. 5

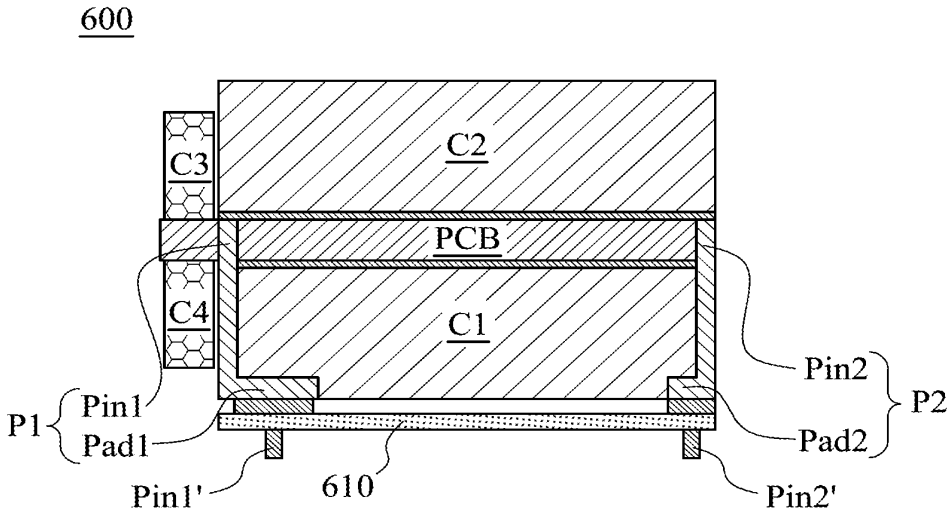

600
C2
C3
PCB
C4
C1
Pin2
P2
P1
Pin1
Pad1
Pad2
Pin1'
610
Pin2'

Fig. 6

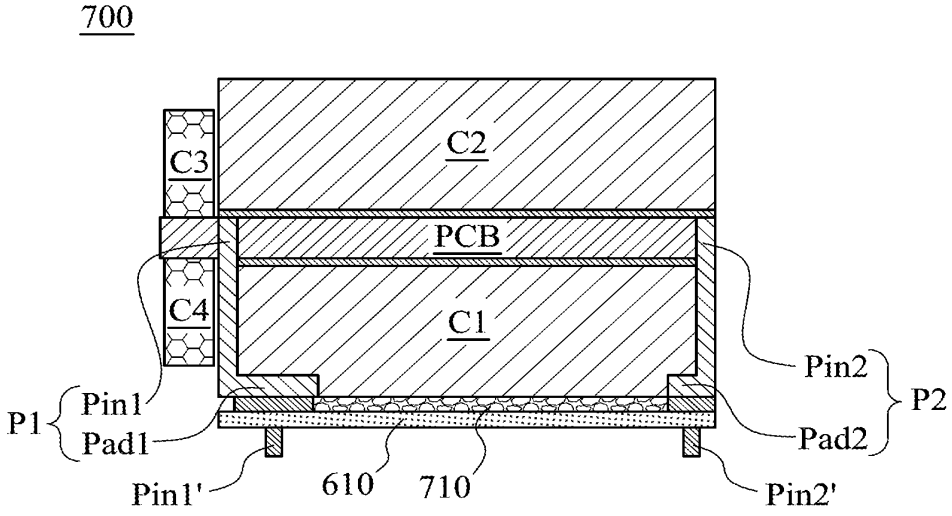


Fig. 7

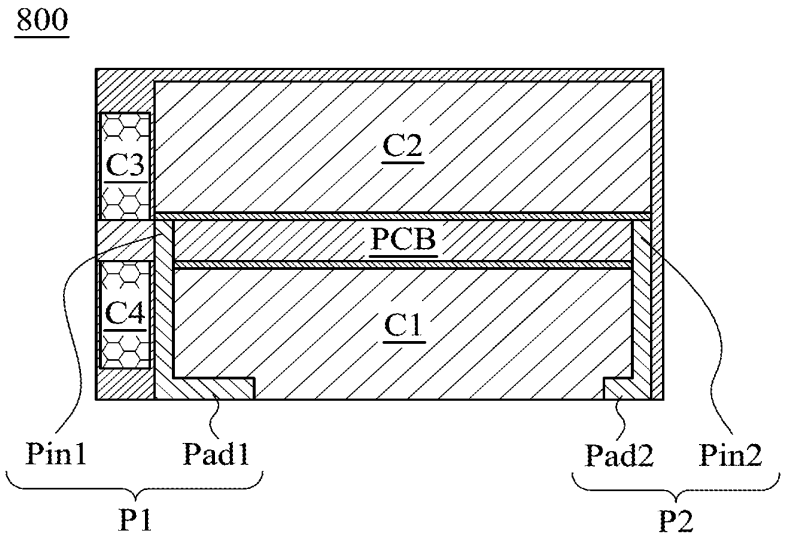

800
C3
C2
PCB
C4
C1
Pin1
Pad1
Pad2
Pin2
P1
P2

Fig. 8

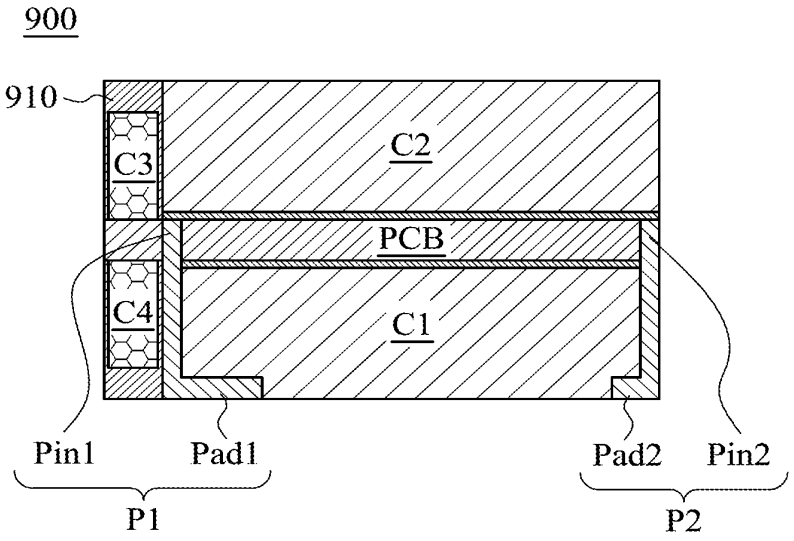

900
910
C3
C2
PCB
C4
C1
Pin1
Pad1
Pad2
Pin2
P1
P2

Fig. 9

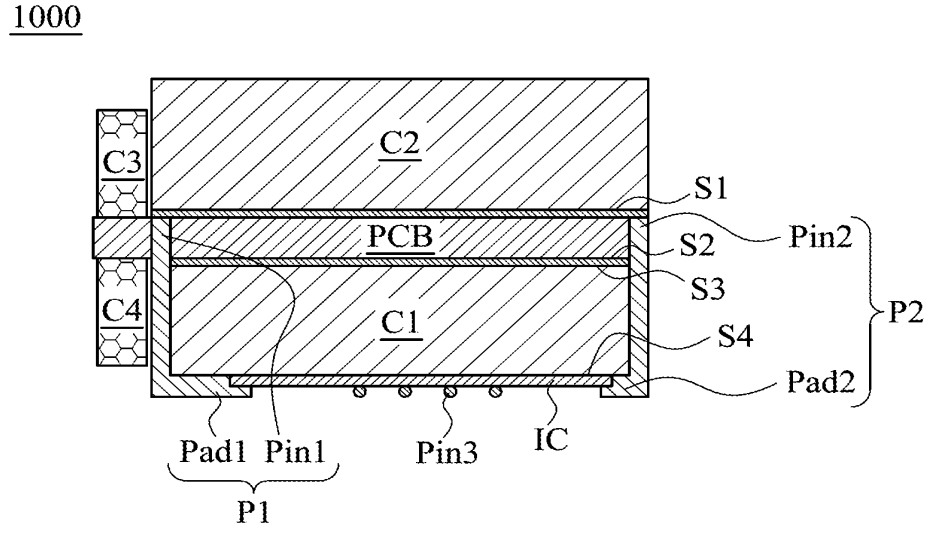


Fig. 10

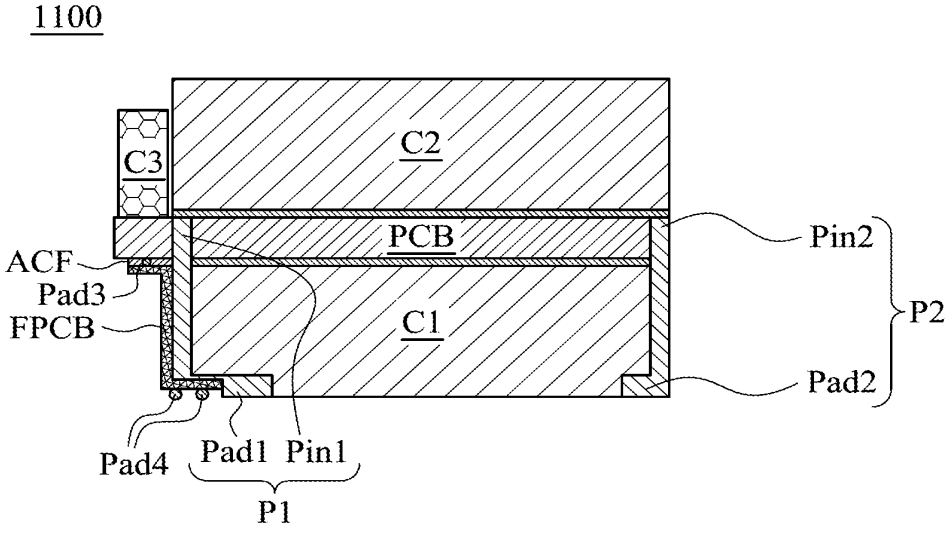


Fig. 11

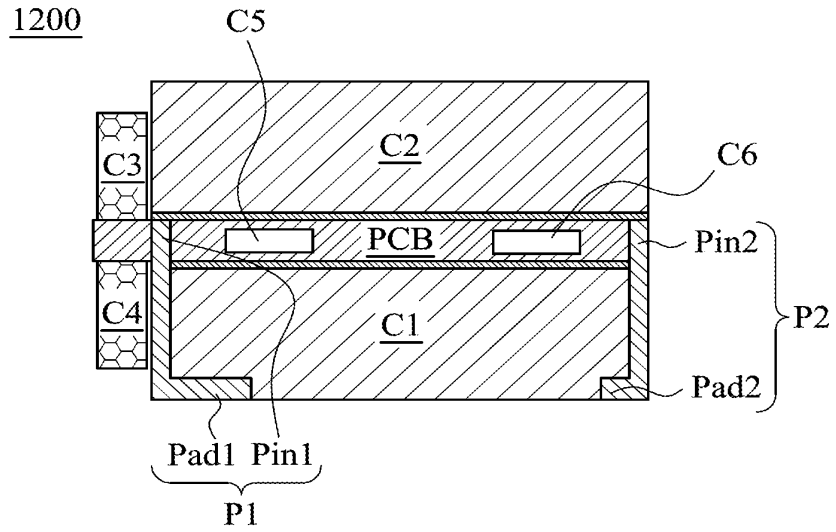

1200
C5
C2
C6
C3
PCB
Pin2
C4
C1
P2
Pad2
Pad1
Pin1
P1

Fig. 12

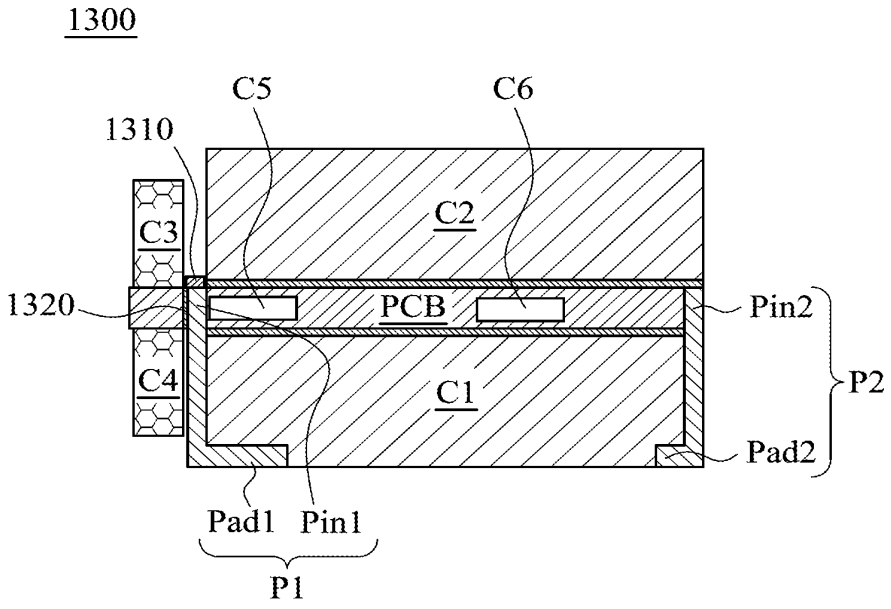

1300
C5
C6
1310
C2
C3
1320
PCB
Pin2
C4
C1
P2
Pad2
Pad1
Pin1
P1

Fig. 13

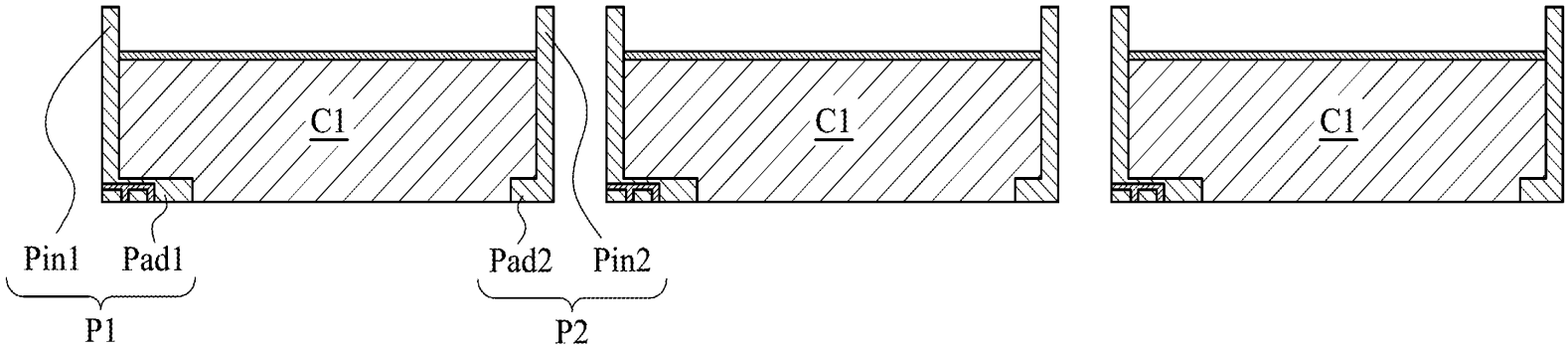


Fig. 14

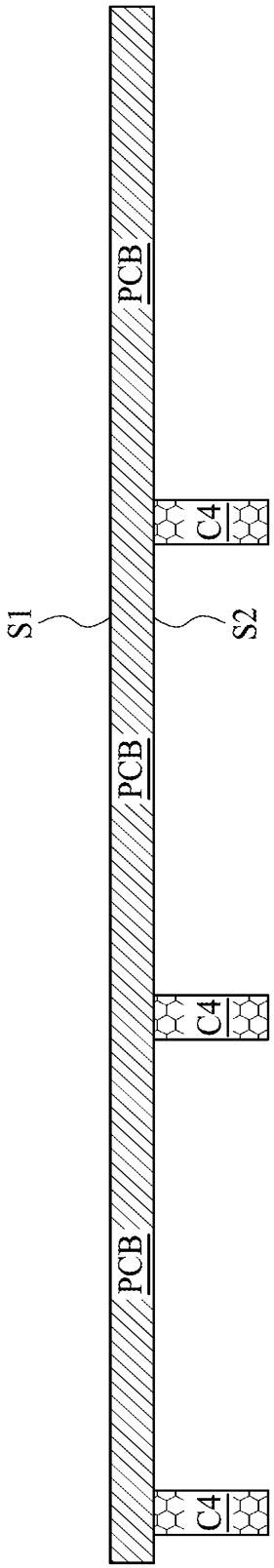


Fig. 15

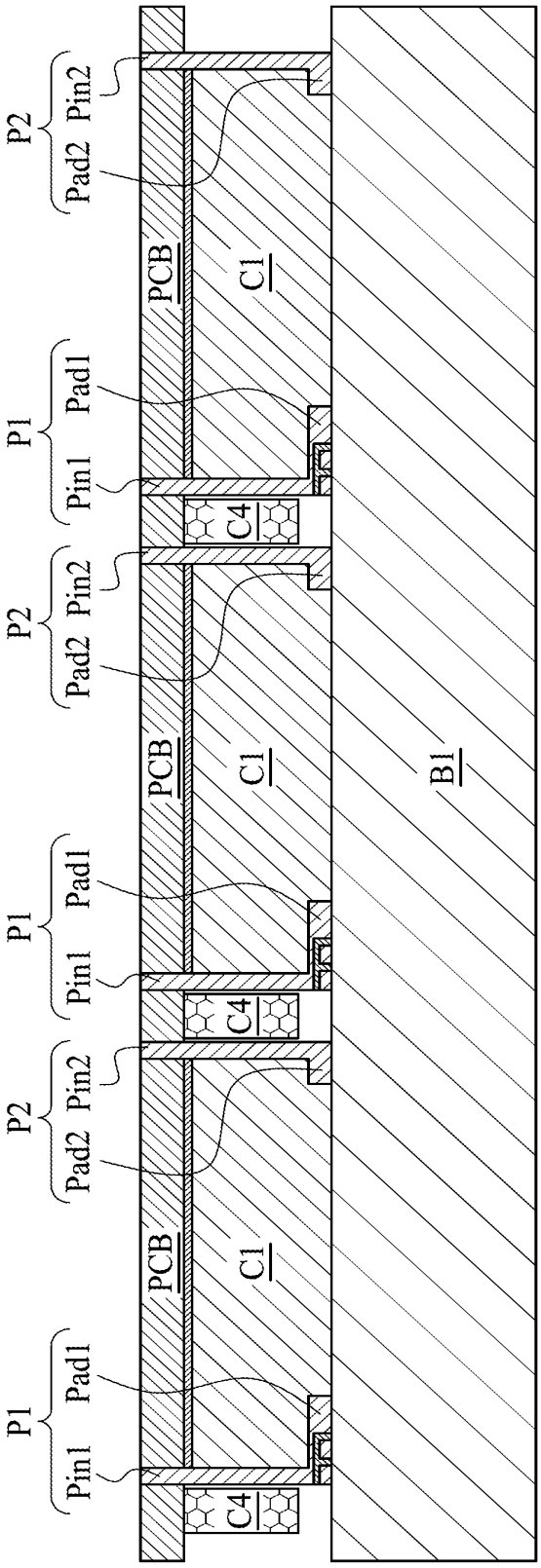


Fig. 16

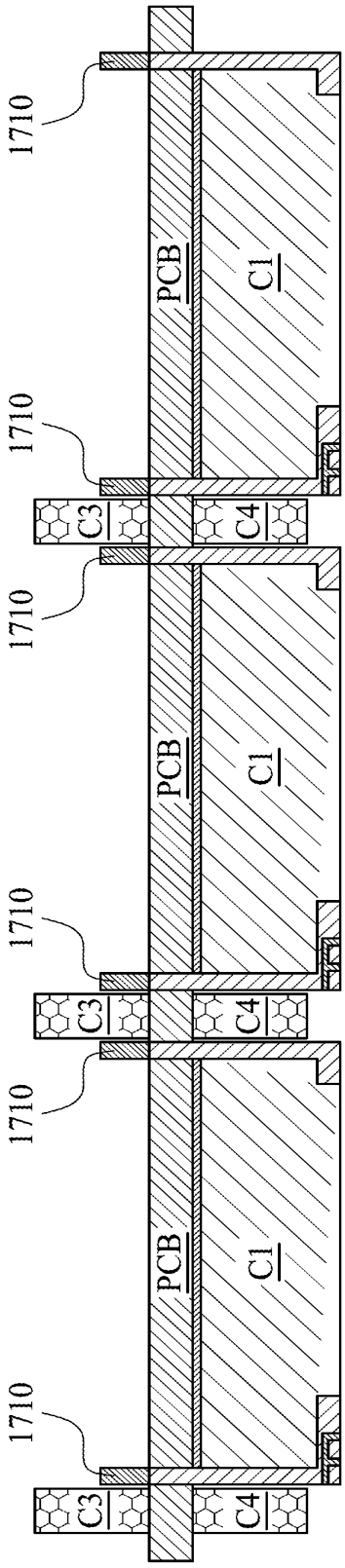

1710
PCB
C1
1710
C3
C4
1710
PCB
C1
1710
C3
C4
1710
PCB
C1
1710
C3
C4

Fig. 17

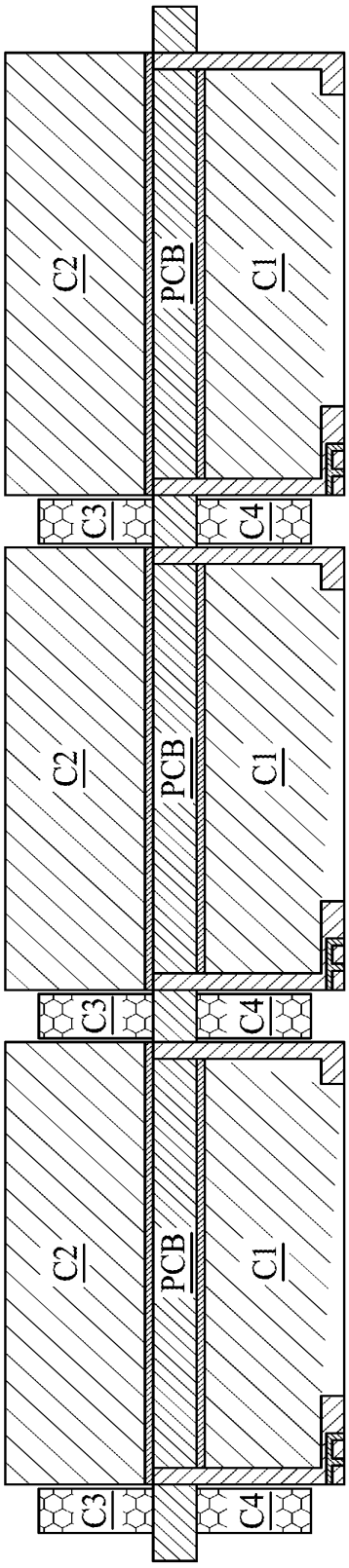


Fig. 18

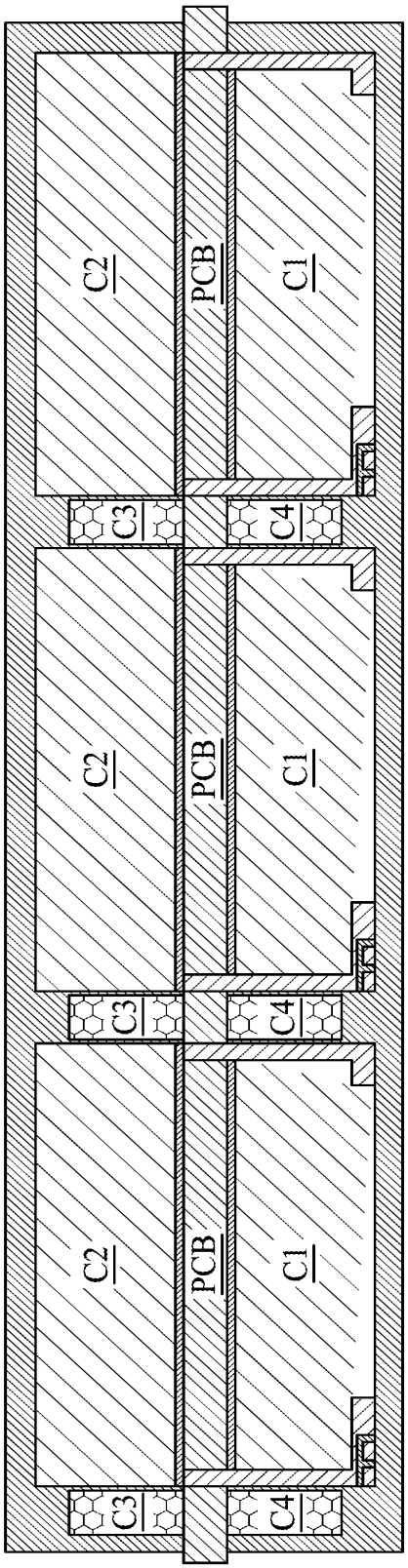


Fig. 19

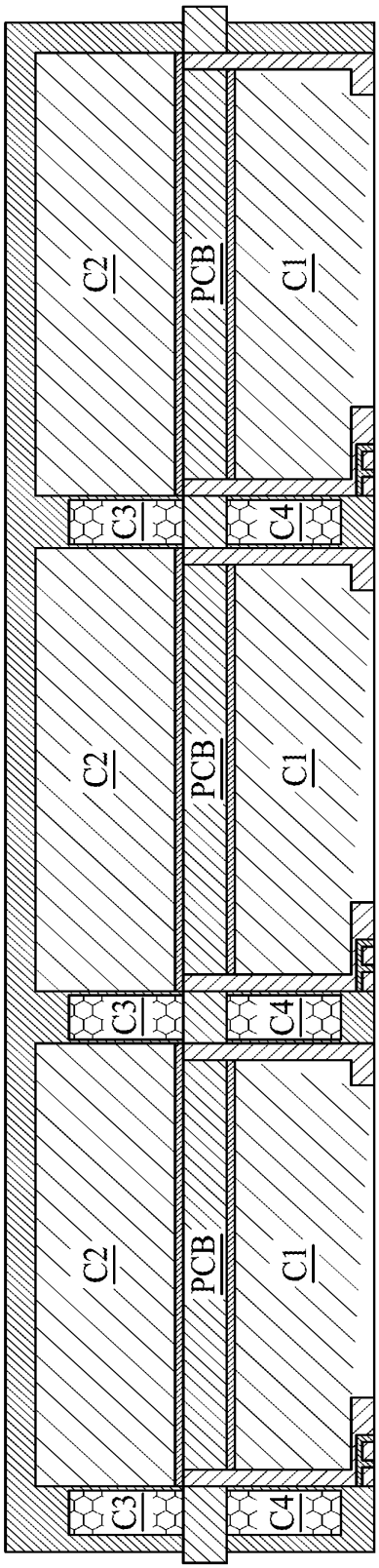


Fig. 20

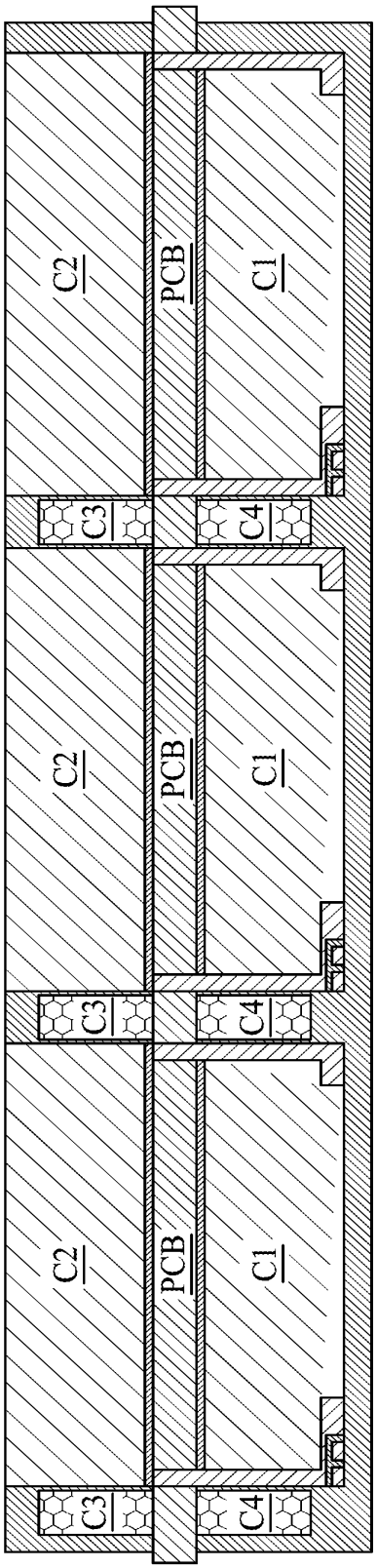


Fig. 21

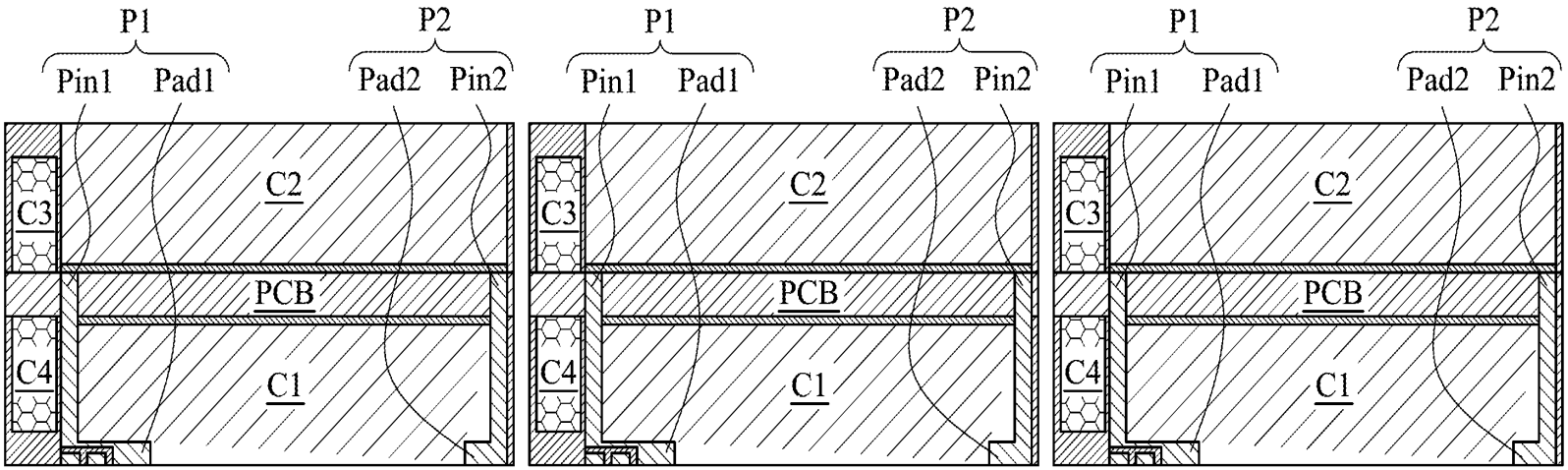


Fig. 22

2300

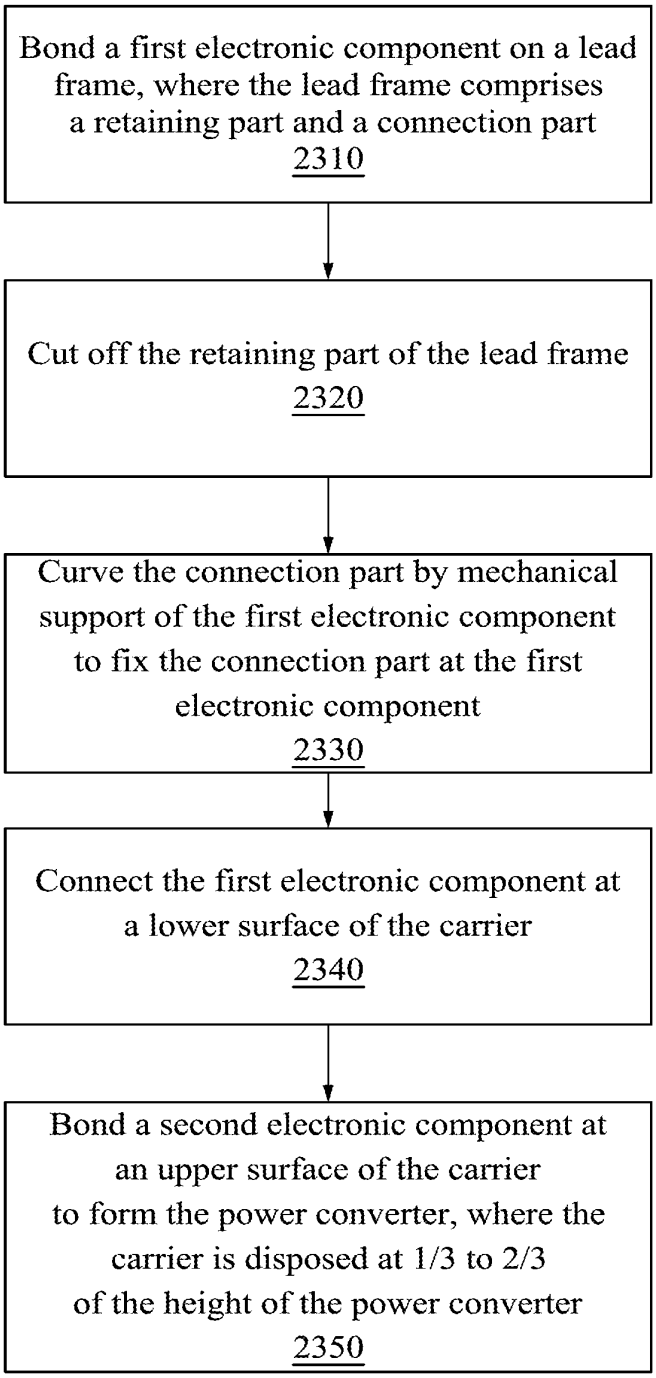

Bond a first electronic component on a lead frame, where the lead frame comprises a retaining part and a connection part
2310
Cut off the retaining part of the lead frame
2320
Curve the connection part by mechanical support of the first electronic component to fix the connection part at the first electronic component
2330
Connect the first electronic component at a lower surface of the carrier
2340
Bond a second electronic component at an upper surface of the carrier to form the power converter, where the carrier is disposed at 1/3 to 2/3 of the height of the power converter
2350

Fig. 23

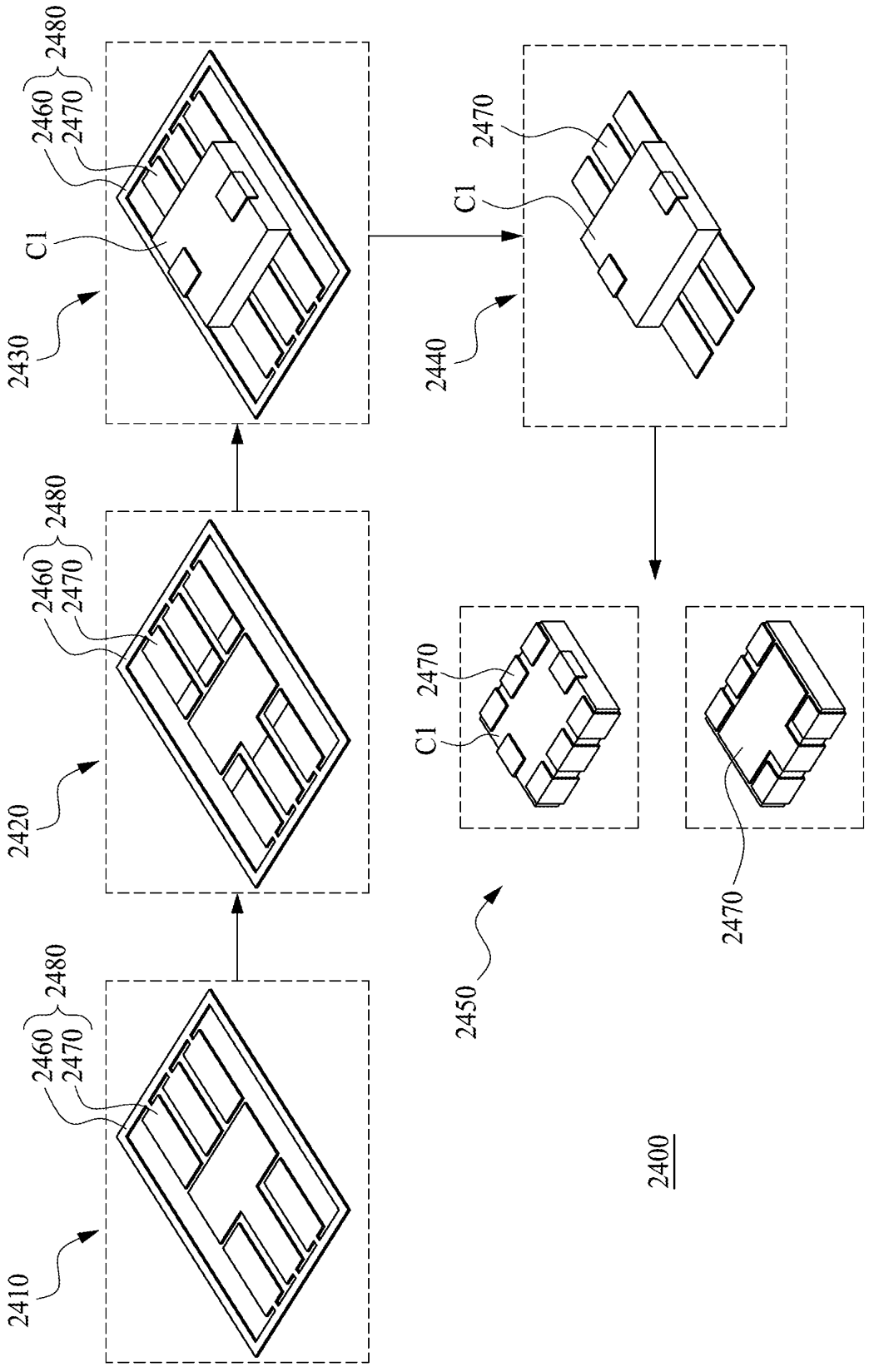


Fig. 24

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Jian-Hong ZENG	Confirmation No. : N/A
Serial No.N/A	Group Art Unit : N/A
Filed : 2016-10-05	Examiner : N/A
	Docket No. TWT04774/US

For : POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME

INFORMATION DISCLOSURE STATEMENT

U.S. PATENT AND TRADEMARK OFFICE
Commissioner for Patents
P.O.BOX 1450
ALEXANDRIA, VA 22313-1450,
U.S.A.

Dear Sir,

This information disclosure statement is filed in accordance with 37 C.F.R.§ §§1.56, 1.97, and 1.98, and specifically :

☒ under 37 CFR 1.97(b), or

(with Three months of filing national application ; or date of entry of international application ; or before mailing date of first office action on the merits ; or before the mailing of a first office action after the filing of a request for continued examination under §1.114 ; whichever occur last)

☐ under 37 CFR 1.97(c) together with either a :

- ☐ Statement Under 37 C.F.R.1.97(e), or
- ☐ a fee under 37 CFR 1.17(p), or

(After the CFR 1.97(b) time period, but before the final office action or notice of allowance, whichever occurs first)

☐ under 37 CFR1.97(d) together with a :

☐ Statement Under 37 C.F.R.1.97(e), and

☐ a petition fee set forth in 37 CFR 1.17(p).

(Filed after final office action or notice of allowance, whichever occurs first, but before payment of the issue fee)

☒ At any time during the pendency of this application, please charge any fees required to Deposit Account pursuant to 37 CFR 1.25. The Commissioner is hereby requested to credit any overpayment to Deposit Account No. 504669.

☒ Applicant(s) submit herewith Form PTO SB/08A-08B-08a – Information Disclosure Statement by Applicant together with copies (where required) of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may or may not be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56. As required by 37 C.F.R. §1.98(a), a legible copy of each document is provided.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Forms SB/08A-08B-08a, as presently understood by the individual(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed in the form PTO SB/08A-08B-08a and is enclosed herewith.

The following rights are reserved by the Applicant(s)：the right to establish the patentability of the claimed invention over any of the listed document should they be applied as reference, and/or the right to prove that some of these documents may not be prior art, and/or the right to prove that some of these documents may not be enabling for the teachings they purport to offer.

This statement should not be construed as a representation that an exhaustive search has been made, or that information more material to the examination of the present application does not exist. Any statements or identifications regarding the relevance of any portion(s) of cited references should not be construed as a representation that the most relevant portion(s) have been identified, and the absence of such statements or identifications should not be construed as representations that there are no relevant portion(s). The Examiner is specifically requested not to rely

solely on the materials submitted herewith. The Examiner is requested to conduct an independent and thorough review of the documents, and to form independent opinion as to their significance.

It is requested that the information disclosed herein be made of record in this application and that the Examiner initial and return a copy of the enclosed PTO SB/08A-08B-08a to indicate the documents have been considered.

Respectfully submitted,

/James Lynn O'Sullivan /

_____

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	2016-10-05
	First Named Inventor	Jian-Hong ZENG
	Art Unit	
	Examiner Name	
	Attorney Docket Number	TWT04774/US

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	1	203057001	CN	U	2013-07-10	TOSHIBA LIGHTING & TECHNOLOGY		
	2	201330190	TW	A	2013-07-16	INTERSIL INC		
	3	242820	TW	B	2005-11-01	SILICONWARE PREC IND CO LTD		

EFS Web 2.1.17

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	2016-10-05
	First Named Inventor	Jian-Hong ZENG
	Art Unit	
	Examiner Name	
	Attorney Docket Number	TWT04774/US

	4	471357	TW	B	2015-02-01	DSM IP ASSETS BV			
	5	412655	TW	B	2013-10-21	TAKIGEN MFG CO			

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	
	Filing Date	2016-10-05
	First Named Inventor	Jian-Hong ZENG
	Art Unit	
	Examiner Name	
	Attorney Docket Number	TWT04774/US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/James Lynn O'Sullivan/	Date (YYYY-MM-DD)	2016-10-05
Name/Print	James Lynn O'Sullivan	Registration Number	65618

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Espacenet

Bibliographic data: CN203057001 (U) — 2013-07-10

Switch power supply apparatus and lighting device

Inventor(s): NORIYUKI KITAMURA; YUJI TAKAHASHI; HITOSHI KAWANO; MASATOSHI KUMAGAI; YOSUKE SAITO ± (NORIYUKI KITAMURA, ; YUJI TAKAHASHI, ; HITOSHI KAWANO, ; MASATOSHI KUMAGAI, ; YOSUKE SAITO)

Applicant(s): TOSHIBA LIGHTING & TECHNOLOGY ± (TOSHIBA LIGHTING & TECHNOLOGY CORP)

Classification: - international: ***H02M7/162; H05B37/02***
- cooperative: **H05B33/0803**

Application number: CN20122453049U 20120906

Priority number(s): JP20110249832 20111115

Also published as: EP2595452 (A1) US2013119860 (A1) US9006974 (B2) JP2013106469 (A) JP5831153 (B2)

Abstract of CN203057001 (U)

The utility model provides a switch power supply apparatus and a lighting device, which can improve heat dissipation performance and realize miniaturization. The power supply apparatus comprises a switch element, an inductor, a drive circuit, an installation substrate and an installation substrate. The switch element is connected between a power supply and a lighting load. The inductor and the switch element are in series connection. The drive circuit controls the switch element and converts the voltage supplied by the power supply. The installation substrate is equipped with the drive circuit. The insulation substrate is in hot link with the switch element; the thermal conductivity of the insulation substrate is higher than the thermal conductivity of the installation substrate.

(19)中华人民共和国国家知识产权局

(12)实用新型专利

(10)授权公告号 CN 203057001 U
(45)授权公告日 2013.07.10

(21)申请号 201220453049.9

(22)申请日 2012.09.06

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2011-249832 2011.11.15 JP

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(74)专利代理机构 北京同立钧成知识产权代理有限公司 11205
代理人 臧建明 张洋

(51)Int.Cl.
H02M 7/162(2006.01)
H05B 37/02(2006.01)

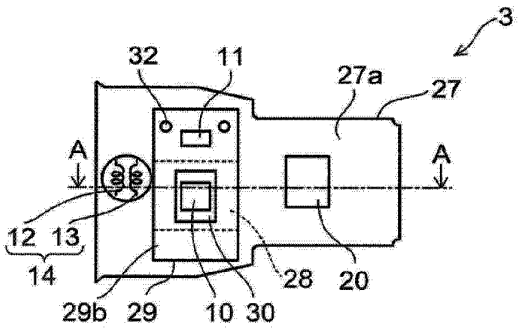
权利要求书2页 说明书11页 附图5页

(54)实用新型名称

开关电源装置及照明装置

(57)摘要

本实用新型提供一种开关电源装置及照明装置，可改善散热特性且可实现小型化。本实用新型的开关电源装置，包括：开关元件、电感器、驱动电路、安装基板、以及绝缘基板。所述开关元件连接在电源与照明负载之间。所述电感器与所述开关元件串联连接。所述驱动电路控制所述开关元件并对从所述电源供给的电压进行转换。所述安装基板安装有所述驱动电路。所述绝缘基板热连接于所述开关元件，且所述绝缘基板的导热性比所述安装基板的导热性高。



CN 203057001 U

1. 一种开关电源装置，其特征在于包括：

开关元件，其连接在电源与照明负载之间；

电感器，其与所述开关元件串联连接；

驱动电路，其控制所述开关元件并对从所述电源供给的电压进行转换；

安装基板，其安装有所述驱动电路；以及

绝缘基板，其热连接于所述开关元件，且所述绝缘基板的导热性比所述安装基板的导热性高。

2. 根据权利要求 1 所述的开关电源装置，其特征在于：

还包括平滑电容器，其设置在所述安装基板的与设置有所述电感器的第 1 主面侧相反侧的第 2 主面上。

3. 根据权利要求 1 所述的开关电源装置，其特征在于：

还包括交流 - 直流转换电路，其具有设置在所述安装基板的与设置有所述电感器的第 1 主面侧相反侧的第 2 主面上的平滑电容器，且将从所述电源供给的交流电压转换成直流电压。

4. 根据权利要求 2 所述的开关电源装置，其特征在于：

所述绝缘基板设置在所述第 1 主面侧。

5. 根据权利要求 1 所述的开关电源装置，其特征在于：

所述开关元件安装在所述绝缘基板上。

6. 根据权利要求 1 所述的开关电源装置，其特征在于：

所述开关元件安装在所述安装基板上，且经由设置在所述安装基板上的开口部而与所述绝缘基板热连接。

7. 根据权利要求 1 所述的开关电源装置，其特征在于：

所述开关元件安装在所述安装基板上，且经由导电体而与所述绝缘基板热连接。

8. 根据权利要求 1 所述的开关电源装置，其特征在于：

所述电感器为设置在所述绝缘基板上的螺旋电感器。

9. 根据权利要求 8 所述的开关电源装置，其特征在于：

还包括反馈绕组，其设置在所述绝缘基板上，且与所述电感器磁耦合。

10. 根据权利要求 9 所述的开关电源装置，其特征在于：

所述电感器与所述反馈绕组在所述绝缘基板上设置在同一平面上。

11. 一种照明装置，其特征在于包括：

开关电源装置；

照明负载，其作为所述开关电源装置的负载电路而连接；以及

框体，其收容所述开关电源装置；且

所述开关电源装置包括：

开关元件，其连接在电源与所述照明负载之间；

电感器，其与所述开关元件串联连接；

驱动电路，其控制所述开关元件并对从所述电源供给的电压进行转换；

安装基板，其安装有所述驱动电路；以及

绝缘基板，其热连接于所述开关元件，且所述绝缘基板的导热性比所述安装基板的导

热性高。

12. 根据权利要求 11 所述的照明装置，其特征在于：

所述绝缘基板与所述框体热连接。

13. 根据权利要求 11 所述的照明装置，其特征在于：

还包括平滑电容器，其设置在所述安装基板的与设置有所述电感器的第 1 主面侧相反侧的第 2 主面上。

14. 根据权利要求 11 所述的照明装置，其特征在于：

还包括交流 - 直流转换电路，其具有设置在所述安装基板的与设置有所述电感器的第 1 主面侧相反侧的第 2 主面上的平滑电容器，且将从所述电源供给的交流电压转换成直流电压。

15. 根据权利要求 13 所述的照明装置，其特征在于：

所述绝缘基板设置在所述第 1 主面侧。

16. 根据权利要求 11 所述的照明装置，其特征在于：

所述开关元件安装在所述绝缘基板上。

17. 根据权利要求 11 所述的照明装置，其特征在于：

所述开关元件安装在所述安装基板上，且经由设置在所述安装基板上的开口部而与所述绝缘基板热连接。

18. 根据权利要求 11 所述的照明装置，其特征在于：

所述开关元件安装在所述安装基板上，且经由导电体而与所述绝缘基板热连接。

19. 根据权利要求 11 所述的照明装置，其特征在于：

所述电感器为形成在所述绝缘基板上的螺旋电感器。

20. 根据权利要求 19 所述的照明装置，其特征在于：

还包括反馈绕组，其设置在所述绝缘基板上，且与所述电感器磁耦合。

开关电源装置及照明装置

技术领域

[0001] 本实用新型的实施形态涉及一种开关电源装置及照明装置。

背景技术

[0002] 利用开关元件的开关电源作为适合于省电力·小型化的电源而用于各种广泛的用途。作为其一例，也可以用作照明的电源。

[0003] 近年来，在照明装置中，照明光源正在从白炽灯泡或荧光灯更换为节能·长寿命的光源，例如发光二极管(Light-emitting diode：LED)。另外，例如有机发光二极管(Organic light-emitting diode：OLED)等新的照明光源也已得到开发。

[0004] 现有技术文献

[0005] 专利文献

[0006] 专利文献 1 日本专利特开 2011-119237 号公报

[0007] 但是，若开关电源高频化且小型化，则开关元件等的发热密度增大。

实用新型内容

[0008] 要解决的课题

[0009] 本实用新型的实施形态的目的在于提供一种开关电源装置及照明装置，可改善散热特性且可实现小型化。

[0010] 实施形态的开关电源装置包括：开关元件、电感器、驱动电路、安装基板、以及绝缘基板。所述开关元件连接在电源与照明负载之间。所述电感器与所述开关元件串联连接。所述驱动电路控制所述开关元件并对从所述电源供给的电压进行转换。所述安装基板安装有所述驱动电路。所述绝缘基板热连接于所述开关元件，且所述绝缘基板的导热性比所述安装基板的导热性高。

[0011] 所述的开关电源装置，还包括平滑电容器，其设置在所述安装基板的与设置有所述电感器的第 1 主面侧相反侧的第 2 主面上。

[0012] 所述的开关电源装置，还包括交流－直流转换电路，其具有设置在所述安装基板的与设置有所述电感器的第 1 主面侧相反侧的第 2 主面上的平滑电容器，且将从所述电源供给的交流电压转换成直流电压。

[0013] 所述的开关电源装置，其中，所述绝缘基板设置在所述第 1 主面侧。

[0014] 所述的开关电源装置，其中，所述开关元件安装在所述绝缘基板上。

[0015] 所述的开关电源装置，其中，所述开关元件安装在所述安装基板上，且经由设置在所述安装基板上的开口部而与所述绝缘基板热连接。

[0016] 所述的开关电源装置，其中，所述开关元件安装在所述安装基板上，且经由导电体而与所述绝缘基板热连接。

[0017] 所述的开关电源装置，其中，所述电感器为设置在所述绝缘基板上的螺旋电感器。

[0018] 所述的开关电源装置，还包括反馈绕组，其设置在所述绝缘基板上，且与所述电感

器磁耦合。

[0019] 所述的开关电源装置，其中，所述电感器与所述反馈绕组在所述绝缘基板上设置在同一平面上。

[0020] 实施形态的照明装置包括：开关电源装置、照明负载以及框体。照明负载，其作为所述开关电源装置的负载电路而连接。框体，其收容所述开关电源装置。所述开关电源装置包括：开关元件、电感器、驱动电路、安装基板以及绝缘基板。开关元件，其连接在电源与所述照明负载之间。电感器，其与所述开关元件串联连接。驱动电路，其控制所述开关元件并对从所述电源供给的电压进行转换。安装基板，其安装有所述驱动电路。绝缘基板，其热连接于所述开关元件，且所述绝缘基板的导热性比所述安装基板的导热性高。

[0021] 所述的照明装置，其中，所述绝缘基板与所述框体热连接。

[0022] 所述的照明装置，还包括平滑电容器，其设置在所述安装基板的与设置有所述电感器的第 1 主面侧相反侧的第 2 主面上。

[0023] 所述的照明装置，还包括交流 - 直流转换电路，其具有设置在所述安装基板的与设置有所述电感器的第 1 主面侧相反侧的第 2 主面上的平滑电容器，且将从所述电源供给的交流电压转换成直流电压。

[0024] 所述的照明装置，其中，所述绝缘基板设置在所述第 1 主面侧。

[0025] 所述的照明装置，其中，所述开关元件安装在所述绝缘基板上。

[0026] 所述的照明装置，其中，所述开关元件安装在所述安装基板上，且经由设置在所述安装基板上的开口部而与所述绝缘基板热连接。

[0027] 所述的照明装置，其中，所述开关元件安装在所述安装基板上，且经由导电体而与所述绝缘基板热连接。

[0028] 所述的照明装置，其中，所述电感器为形成在所述绝缘基板上的螺旋电感器。

[0029] 所述的照明装置，还包括反馈绕组，其设置在所述绝缘基板上，且与所述电感器磁耦合。

[0030] 实用新型的效果

[0031] 根据本实用新型的实施形态，提供一种改善散热特性且可实现小型化的开关电源装置及照明装置。

附图说明

[0032] 图 1（a）~ 图 1（c）是对第 1 实施形态的开关电源装置进行例示的示意图，其中图 1（a）为俯视图，图 1（b）为图 1（a）及图 1（c）的 A-A 线剖面图，图 1（c）为仰视图。

[0033] 图 2（a）、图 2（b）是第 1 实施形态的开关电源装置的开关元件附近的放大图，其中图 2（a）为平面图，图 2（b）为图 2（a）的 B-B 线剖面图。

[0034] 图 3 是对包含第 1 实施形态的开关电源装置的照明装置进行例示的电路图。

[0035] 图 4 是对第 2 实施形态的开关电源装置进行例示的剖面图。

[0036] 图 5（a）、图 5（b）是对第 3 实施形态的开关电源装置进行例示的示意图，其中图 5（a）为平面图，图 5（b）为图 5（a）的 C-C 线剖面图。

[0037] 图 6 是对第 4 实施形态的开关电源装置进行例示的剖面图。

[0038] 图 7（a）~ 图 7（c）是对包含开关电源装置的照明装置进行例示的部分剖面图，其

中图 7（a）为正面图，图 7（b）为图 7（a）的 D-D 线剖面图，图 7（c）为图 7（a）的 E-E 线剖面图。

[0039] 图 8（a）、图 8（b）是对照明装置进行例示的另一部分剖面图，其中图 8（a）为正面图，图 8（b）为图 8（a）的 F-F 线剖面图。

[0040] 图 9 是对照明装置进行例示的另一部分剖面图。

[0041] 附图标记：

[0042] 1、1a、1b：照明装置

[0043] 2：照明负载

[0044] 3、3a、3b、3c、3d：开关电源装置

[0045] 4：照明光源

[0046] 5：交流电源

[0047] 6：交流 - 直流（AC-DC）转换电路

[0048] 7：开关元件

[0049] 8：恒定电流元件

[0050] 9：整流元件

[0051] 10：半导体元件

[0052] 11：驱动电路

[0053] 12：电感器

[0054] 13：反馈绕组

[0055] 14：变压器

[0056] 15：耦合电容器

[0057] 16、17：分压电阻

[0058] 18：输出电容器

[0059] 19：输入电容器

[0060] 20：整流电路

[0061] 21：扼流圈

[0062] 22：平滑电容器

[0063] 23、24：输入端子

[0064] 25：高电位输出端子

[0065] 26：低电位输出端子

[0066] 27、27d：安装基板

[0067] 27a：第 1 主面

[0068] 27b：第 2 主面

[0069] 28、28d：绝缘基板

[0070] 29：安装基板（子基板）

[0071] 29a：第 1 主面

[0072] 29b：第 2 主面

[0073] 30、37：开口部

[0074] 31：粘结层

[0075] 32 :导通孔

[0076] 33 :配线层

[0077] 34 :接合线

[0078] 35 :焊垫

[0079] 36 :保护层

[0080] 38 :热导电体

[0081] 101、101a :基座

[0082] 102、102a :框体

[0083] 103、103a :透光遮罩

[0084] 104 :照明基板

[0085] 105 :绝缘体

[0086] 106 :灯头部

[0087] 107 :导电体

具体实施方式

[0088] 以下，参照图式对实施形态进行详细说明。再者，图式是示意性或概念性的图，各部分的形状与宽度的关系、部分间的大小的比率等未必与实际者相同。另外，即便当表示相同部分时，也存在彼此的尺寸或比率因图式而不同地表示的情况。另外，在本申请案的说明书与各图中，对与在已出现过的图中进行了叙述的要素相同的要素附上相同的符号，且适当地省略详细的说明。

[0089] 首先，对第 1 实施形态进行说明。

[0090] 图 1 (a)～图 1 (c)是对第 1 实施形态的开关电源装置进行例示的平面图及剖面图，其中图 1 (a)为俯视图，图 1 (b)为图 1 (a)及图 1 (c)的 A-A 线剖面图，图 1 (c)为仰视图。

[0091] 如图 1 (a)及图 1 (b)所示，在开关电源装置 3 中，在安装基板(主基板)27 的第 2 主面 27b 侧安装有输入电容器 19、扼流圈 21、平滑电容器 22 等相对大型的个头高的元件。第 2 主面 27b 为零件面。

[0092] 另外，如图 1 (b)及图 1 (c)所示，在开关电源装置 3 中，在安装基板 27 的第 1 主面 27a 侧安装有绝缘基板 28、安装了将开关元件集成化而成的半导体元件 10 及驱动电路 11 的安装基板(子基板)29、变压器 14、以及整流电路 20。安装基板 27 例如为酚醛纸基板，且例如为玻璃环氧基板。第 1 主面 27a 为焊料面，且安装有相对小型的个头低的元件。

[0093] 绝缘基板 28 为包含例如氧化铝(Al_2O_3)、例如氮化铝(AlN)的陶瓷基板。绝缘基板 28 的导热性比安装基板 27、安装基板 29 高，且与开关元件热连接。绝缘基板 28 安装在安装基板 29 的第 1 主面 29a 侧。

[0094] 安装基板 29 例如为酚醛纸基板，且例如为玻璃环氧基板。

[0095] 在安装基板 29 上设置有开口部 30，在开口部 30 中绝缘基板 28 露出。半导体元件 10 安装在开口部 30 中的绝缘基板 28 上。驱动电路 11 安装在与安装基板 29 的第 1 主面 29a 相反侧的安装基板 29 的第 2 主面 29b 侧。

[0096] 绝缘基板 28 与安装基板 29 经由粘结层 31 而安装在安装基板 27 的第 1 主面 27a

侧。粘结层 31 例如为热硬化树脂。另外，安装基板 29 经由导通孔 32 而与安装基板 27 电性连接。

[0097] 再者，如参照图 3 的电路图进行说明般，输入电容器 19、整流电路 20、扼流圈 21、平滑电容器 22 构成对输入至一对输入端子 23、24 中的交流电压进行整流而使其平滑化的 AC-DC 转换电路。另外，半导体元件 10、驱动电路 11、变压器 14 等构成使平滑电容器 22 的电压下降的 DC-DC 转换器。

[0098] 图 2（a）、图 2（b）是第 1 实施形态的开关电源装置的开关元件附近的放大图，其中图 2（a）为平面图，图 2（b）为图 2（a）的 B-B 线剖面图。

[0099] 在图 2（a）、图 2（b）中，将开关电源装置 3 的绝缘基板 28 与安装基板 29 中，包含开关元件的半导体元件 10 附近放大表示。

[0100] 半导体元件 10 是将开关元件 7、恒定电流元件 8、整流元件 9 集成化而成的元件。半导体元件 10 裸芯片安装在安装基板 29 上。即，设置在半导体元件 10 上的焊垫 35 与设置在安装基板 29 上的配线层 33 通过接合线 34 而电性连接。集成化为半导体元件 10 的开关元件 7 与绝缘基板 28 热连接。

[0101] 保护层 36 例如为树脂层，其保护半导体元件 10、接合线 34、焊垫 35。再者，在图 1（b）、图 1（c）、及图 2（a）中，省略保护层 36。

[0102] 再者，开关元件 7、恒定电流元件 8、整流元件 9 也可以分别裸芯片安装在安装基板 29 上。即，也可以通过接合线将开关元件 7、恒定电流元件 8、整流元件 9 的各裸芯片上的电极与安装基板 29 上的配线层 33 电性连接。另外，也可以不使用接合线，而进行倒装芯片安装。进而，可以将开关元件 7、恒定电流元件 8、整流元件 9 分别封入至封装体（package）中，也可以对各元件进行表面安装。在以下将说明的其他实施形态中也同样如此。

[0103] 开关元件 7 及恒定电流元件 8 例如为高电子迁移率晶体管（HighElectron Mobility Transistor：HEMT），且例如为 GaN 系 HEMT。

[0104] 包含半导体元件 10、驱动电路 11、变压器 14 等的 DC-DC 转换器可实现例如 10MHz 左右的高频化，因此可使变压器 14 小型化。其结果，变压器 14 可安装在供相对小型的元件安装的第 1 主面 27a 侧。另外，平滑电容器 22 等相对大型的元件安装在与第 1 主面 27a 相反侧的第 2 主面 27b 侧。

[0105] 另外，在本实施形态中，设置有热连接于开关元件 7，且导热性比安装基板 27、安装基板 29 高的绝缘基板 28。其结果，开关元件 7 的散热性得到改善，且可实现小型化。

[0106] 再者，在本实施形态中，例示了在安装基板 27 上安装有包含输入电容器 19、整流电路 20、扼流圈 21、平滑电容器 22 的 AC-DC 转换电路的构成。但是，也可以将半导体元件 10、驱动电路 11、变压器 14 安装在安装基板 27 上，而构成 DC-DC 转换器。在此情况下，由于绝缘基板 28 热连接于开关元件 7，且导热性比安装基板 27 高，因此散热性也得到改善，也可以实现小型化。另外，当不安装平滑电容器 22 时，也可以将变压器 14 安装在安装基板 27 的第 2 主面 27b 侧。在以下将说明的其他实施形态中也同样如此。

[0107] 图 3 是对包含第 1 实施形态的开关电源装置的照明装置进行例示的电路图。

[0108] 照明装置 1 包括照明负载 2 与开关电源装置 3。照明负载 2 具有例如 LED 等照明光源 4，且由开关电源装置 3 供给电力而点灯。

[0109] 开关电源装置 3 包括：将从交流电源 5 供给的交流电压转换成直流电压的 AC-DC

转换电路6、开关元件7、恒定电流元件8、整流元件9、以及控制开关元件7并设定恒定电流元件8的恒定电流值的驱动电路11。再者，从开关电源装置3中去除AC-DC转换电路6后的部分构成DC-DC转换器。

[0110] AC-DC转换电路6包括：输入电容器19、整流电路20、扼流圈21、平滑电容器22。输入电容器19连接于一对输入端子23、24。整流电路20包含二极管电桥，且经由一对输入端子23、24而从交流电源5输入交流电压。利用包含扼流圈21与平滑电容器22的低通滤波器来使从整流电路20输出的直流电压(脉动电压)平滑化。再者，交流电源5例如为商用电源。

[0111] 开关元件7的漏极连接于平滑电容器22的一端(正极侧)，开关元件7的源极连接于恒定电流元件8的漏极。开关元件7的栅极经由驱动电路11的耦合电容器15而连接于反馈绕组13的一端。

[0112] 恒定电流元件8的源极连接于电感器12的一端及反馈绕组13的另一端，恒定电流元件8的栅极连接于驱动电路11的分压电阻16、分压电阻17的连接点。另外，经由偏压电阻而对分压电阻16、分压电阻17供给平滑电容器22的电压。其结果，对恒定电流元件8的栅极供给相对于恒定电流元件8的源极为负极性的电位。再者，分压电阻16为可变电阻，可使分压电阻16的电阻值变化来调整恒定电流元件8的恒定电流值。

[0113] 整流元件9将从平滑电容器22的另一端朝恒定电流元件8的方向作为正向，而连接在恒定电流元件8的源极与平滑电容器22的另一端(负极侧)之间。

[0114] 电感器12的另一端连接于高电位输出端子25，平滑电容器22的另一端连接于低电位输出端子26。另外，输出电容器18连接在高电位输出端子25与低电位输出端子26之间。

[0115] 再者，当从电感器12的一端朝另一端的方向，即从恒定电流元件8的源极或整流元件9的阴极朝高电位输出端子25的方向增加的电流流动时，电感器12与反馈绕组13以对开关元件7的栅极供给相对于源极为负极性的电压的极性进行磁耦合。另外，电感器12与反馈绕组13构成变压器14。

[0116] 另外，开关元件7及恒定电流元件8例如为GaN系HEMT，且为常通(normally on)形的元件。开关元件7、恒定电流元件8及整流元件9作为半导体元件10而集成化。另外，在开关元件7及恒定电流元件8各自的栅极上连接有保护二极管。连接于开关元件7及恒定电流元件8各自的栅极、且供给栅极电位的耦合电容器15，分压电阻16、分压电阻17，保护二极管构成驱动电路11。

[0117] 照明负载2在高电位输出端子25与低电位输出端子26之间，与输出电容器18并联连接。

[0118] 其次，对开关电源装置3的动作进行说明。

[0119] 若从交流电源5供给电源电压，则在平滑电容器22的两端生成直流电压。

[0120] 当在平滑电容器22的两端生成直流电压时，开关元件7及恒定电流元件8由于是常通形的元件，因此均接通。而且，电流以开关元件7、恒定电流元件8、电感器12、输出电容器18的路径流动，并对输出电容器18进行充电。输出电容器18的两端的电压，即高电位输出端子25与低电位输出端子26之间的电压作为开关电源装置3的输出电压而供给至照明负载2的照明光源4中。

[0121] 若输出电压达到规定电压，则输出电流流入至照明光源 4 中，照明光源 4 进行点灯。此时，电流以开关元件 7、恒定电流元件 8、电感器 12、输出电容器 18 及照明光源 4 的路径流动。例如，当照明光源 4 为 LED 时，该规定电压为 LED 的正向电压，且对应于照明光源 4 而决定。

[0122] 在电感器 12 中流动的电流随时间而增加，在反馈绕组 13 中感应到将耦合电容器 15 侧作为高电位的极性的电动势。因此，经由耦合电容器 15 而对开关元件 7 的栅极供给相对于源极为正的电位，开关元件 7 维持接通的状态。

[0123] 若在恒定电流元件 8 中流动的电流超过恒定电流值，则恒定电流元件 8 的漏极 •源极间电压急剧上升。因此，开关元件 7 的栅极 • 源极间电压变得低于阈值电压，开关元件 7 断开。再者，恒定电流值为恒定电流元件 8 的饱和电流值，其由从分压电阻 16、分压电阻 17 输入至恒定电流元件 8 的栅极中的电位规定。再者，如上所述，恒定电流元件 8 的栅极电位相对于源极为负电位，因此可将饱和电流值限制为适当值。

[0124] 电感器 12 使电流以整流元件 9、输出电容器 18 及照明负载 2、电感器 12 的路径持续流动。此时，电感器 12 放出能量，因此电感器 12 的电流减少。因此，在反馈绕组 13 中感应到将耦合电容器 15 侧作为低电位的极性的电动势。经由耦合电容器 15 而对开关元件 7 的栅极供给相对于源极为负的电位，开关元件 7 维持断开的状态。

[0125] 若电感器 12 中所蓄积的能量变成零，则在电感器 12 中流动的电流变成零。在反馈绕组 13 中感应到的电动势的方向再次反向，而感应到如将耦合电容器 15 侧作为高电位般的电动势。由此，对开关元件 7 的栅极供给比源极高的电位，开关元件 7 接通。由此，恢复成所述输出电压达到规定电压的状态。

[0126] 以后，重复所述动作。由此，针对开关元件 7 的接通及断开的切换自动地重复，而对照明光源 4 供给使如下的直流电压下降而成的输出电压，所述直流电压是使从交流电源 5 供给的电源电压平滑化而成的电压。另外，通过恒定电流元件 8 而将供给至照明光源 4 中的电流限制为恒定电流值。因此，可使照明光源 4 稳定地点灯。另外，如上所述，该恒定电流值可通过使分压电阻 16 的电阻值变化来调整。

[0127] 在本实施形态中，由于开关元件 7 及恒定电流元件 8 为 GaN 系 HEMT，因此可使开关频率高频化，例如可使开关频率变成 10MHz 左右。其结果，可使由电感器 12、反馈绕组 13 构成的变压器 14 小型化。

[0128] 另外，将开关元件 7 及恒定电流元件 8 热连接在导热性比安装驱动电路 11 等电路元件的安装基板 27、安装基板 29 高的绝缘基板 28 上，由此散热性得到改善。其结果，可避免发热密度增加的问题，并实现小型化及收容在密闭空间内。

[0129] 再者，在本实施形态中，例示了如下的构成：具备 AC-DC 转换电路 6，将从交流电源 5 供给的电源电压转换成直流电压，并通过 DC-DC 转换器使直流电压下降后输出。但是，也可以设为省略 AC-DC 转换电路 6，并通过 DC-DC 转换器使从直流电源供给的直流电压下降后输出的构成。

[0130] 其次，对第 2 实施形态进行说明。

[0131] 图 4 是对第 2 实施形态的开关电源装置进行例示的剖面图。

[0132] 如图 4 所示，第 2 实施形态与第 1 实施形态的不同点在于：安装基板 27 的构成、及省略绝缘基板（子基板）29。即，在安装基板 27 上设置有开口部 37。绝缘基板 28 安装在安

装基板 27 的第 1 主面 27a 上，且在开口部 37 中露出。半导体元件 10 安装在开口部 37 中的绝缘基板 28 上。另外，驱动电路 11 安装在安装基板 27 的第 2 主面 27b 上。除此以外，本实施形态与第 1 实施形态相同，开关电源装置 3a 的电路构成也与开关电源装置 3 相同。

[0133] 在本实施形态中，由于不使用安装基板 29，因此构造简单化而可降低成本，并且可使安装高度变低。

[0134] 另外，在本实施形态中，也设置有热连接于开关元件 7，且导热性比安装基板 27 高的绝缘基板 28。其结果，开关元件 7 的散热性得到改善，可实现小型化。

[0135] 另外，在本实施形态中，也使用 GaN 系 HEMT 作为开关元件 7，因此可通过高频化而实现电感器 12、反馈绕组 13 的小型化。其结果，可将包含电感器 12 与反馈绕组 13 的变压器 14 安装在安装基板 27 的第 1 主面 27a 侧，即焊料面侧，而可进一步小型化。

[0136] 其次，对第 3 实施形态进行说明。

[0137] 图 5（a）、图 5（b）是对第 3 实施形态的开关电源装置进行例示的示意图，其中图 5（a）为平面图，图 5（b）为图 5（a）的 C-C 线剖面图。

[0138] 如图 5（a）、图 5（b）所示，第 3 实施形态与第 2 实施形态相比，半导体元件 10 及变压器 14 的构成不同。即，半导体元件 10 被封入至封装体中，且表面安装在绝缘基板 28 上。另外，构成变压器 14 的电感器 12 与反馈绕组 13 为螺旋电感器，且形成在绝缘基板 28 上。

[0139] 在本实施形态中，也使用 GaN 系 HEMT 作为开关元件 7，因此可通过高频化而将电感器 12、反馈绕组 13 以螺旋电感器安装在绝缘基板 28 上。其结果，开关元件 7 的散热性得到改善，并且变压器 14 的散热性也得到改善，且可进一步小型化。另外，由于开关元件 7 与变压器 14 之间不包含连接器等，因此可使寄生电感及寄生电容变小，进一步有利于高频化。

[0140] 本实施形态中的所述以外的构成及效果与第 2 实施形态相同，开关电源装置 3b 的电路构成也与开关电源装置 3 相同。

[0141] 再者，也可以设置包围变压器 14 的强磁性体层，而进行磁屏蔽。另外，电感器 12、反馈绕组 13 也可以叠加为 2 层来形成。另外，构成变压器 14 的电感器 12 与反馈绕组 13 在绝缘基板 28 上，可形成在同一平面上，另外，也可以上下积层来形成。

[0142] 图 6 是对第 4 实施形态的开关电源装置进行例示的剖面图。

[0143] 如图 6 所示，第 4 实施形态与第 2 实施形态的不同点在于：半导体元件 10 经由热导电体 38 而热连接于绝缘基板 28。即，热导电体 38 贯穿安装基板 27 而设置，并热连接于半导体元件 10 及绝缘基板 28。热导电体 38 例如为包含铜（Cu）及铝（Al）的至少任一种的金属。

[0144] 在本实施形态中，由于不在安装基板 27 上设置开口部 37，因此可进一步小型化。

[0145] 本实施形态中的所述以外的构成及效果与第 2 实施形态相同，开关电源装置 3c 的电路构成也与开关电源装置 3 相同。

[0146] 图 7（a）～图 7（c）是对包含开关电源装置的照明装置进行例示的部分剖面图，其中（a）为正面图，图 7（b）为图 7（a）的 D-D 线剖面图，图 7（c）为图 7（a）的 E-E 线剖面图。

[0147] 如图 7（a）～图 7（c）所示，照明装置 1 包括：基座 101、框体 102、透光遮罩 103、照明基板 104、开关电源装置 3。基座 101 与框体 102 及透光遮罩 103 形成为灯泡形状。

[0148] 开关电源装置 3 与图 1（a）～图 1（c）、图 2（a）～图 2（b）、图 3 中所例示的开关电源装置 3 相同，在安装基板 27 的第 1 主面 27a 侧设置有绝缘基板 28。将开关元件 7 集成化而成的半导体元件 10 热连接于绝缘基板 28。包含电感器 12 及反馈绕组 13 的变压器 14 等相对小型的个头低的元件设置在安装基板 27 的第 1 主面 27a 侧。另外，在与安装基板 27 的第 1 主面 27a 相反侧的第 2 主面 27b 侧设置有输入电容器 19、扼流圈 21、平滑电容器 22 等相对大型的个头高的元件。再者，在图 7（a）～图 7（c）中，为了容易看图，省略安装基板（子基板）29 等的图示而进行了简化。

[0149] 开关电源装置 3 中，安装基板 27 的第 2 主面 27b 平行于框体 102 的虚拟的中心轴、且从中心轴朝外侧仅偏移距离 W 而设置。另外，在框体 102 的内部埋入导热性高的绝缘体 105，将开关电源装置 3 固定，并且使绝缘基板 28 热连接于框体 102。再者，绝缘体 105 例如为硅酮。

[0150] 基座 101 收纳开关电源装置 3 的一部分，并且使开关电源装置 3 的一对输入端子 23、24 连接于交流电源。

[0151] 框体 102 例如由包含铝（Al）的金属形成，其收纳开关电源装置 3 与设置在开关电源装置 3 上的照明基板 104。

[0152] 透光遮罩 103 使从设置在照明基板 104 上的照明光源 4 放射的光扩散并透过，并且保护照明基板 104。

[0153] 在本实施形态中，开关元件 7 热连接于导热性比安装基板 27 高的绝缘基板 28，进而经由绝缘体 105 而热连接于框体 102，因此散热性得到改善。其结果，可实现照明装置 1 的小型化。

[0154] 另外，在本实施形态中，由于开关电源装置 3 得以小型化，因此可缩短框体 102 的长度而使透光遮罩大型化。其结果，可使光分配更宽广，而可增大从透光遮罩 103 的中心部朝基座 101 侧的方向的光输出。

[0155] 进而，在本实施形态中，安装基板 27 的第 2 主面 27b 从框体 102 的中心轴起仅偏移距离 W，因此安装平滑电容器 22 等相对大型的个头高的元件变得容易，可进一步小型化。

[0156] 图 8（a）、图 8（b）是对照明装置进行例示的另一部分剖面图，其中图 8（a）为正面图，图 8（b）为图 8（a）的 F-F 线剖面图。

[0157] 如图 8（a）、图 8（b）所示，照明装置 1a 与照明装置 1 相比，开关电源装置 3 的构成不同。即，照明装置 1a 将照明装置 1 中的开关电源装置 3 替换成开关电源装置 3d。

[0158] 开关电源装置 3d 与开关电源装置 3 相比，安装基板 27 及绝缘基板 28 的形状不同。即，在开关电源装置 3d 中，安装基板 27d 的平面形状形成为长方形，绝缘基板 28d 的平面形状以与框体 102 接触的方式形成。其结果，开关元件 7 的朝框体 102 的散热性得到改善。另外，当通过绝缘基板 28d 来分割框体 102 的内部，并仅朝安装基板的第 1 主面 27a 侧填充绝缘体 105 时，可减少填充量。再者，也可以朝由绝缘基板 28d 所分割的框体 102 的内部的第 1 主面 27a 侧与第 2 主面 27b 侧均填充绝缘体 105。

[0159] 图 9 是对照明装置进行例示的另一部分剖面图。

[0160] 如图 9 所示，照明装置 1b 包括：基座 101a、框体 102a、透光遮罩 103a、照明光源 4、开关电源装置 3a。基座 101a 与框体 102a 及透光遮罩 103a 形成为圆筒形状。

[0161] 开关电源装置 3a 与图 4 中所例示的开关电源装置 3a 相同，在圆环状的安装基板

27 的第 1 主面 27a 侧设置有绝缘基板 28。将开关元件 7 集成化而成的半导体元件 10 热连接于绝缘基板 28。包含电感器 12 及反馈绕组 13 的变压器 14 等相对小型的个头低的元件设置在安装基板 27 的第 1 主面 27a 侧。另外，在安装基板 27 的与第 1 主面 27a 相反侧的第 2 主面 27b 侧设置有输入电容器 19、扼流圈 21、平滑电容器 22 等相对大型的个头高的元件。再者，在图 9 中，为了容易看图，省略第 2 主面 27b 侧的平滑电容器 22 以外的元件的图示而进行了简化。

[0162] 开关电源装置 3a 中，安装基板 27 的第 2 主面 27b 垂直于框体 102a 的虚拟的中心轴而设置。另外，也可以在框体 102a 的内部埋入导热性高的绝缘体 105。绝缘基板 28 也可以与框体 102a 接触来进行热连接。另外，绝缘基板 28 也可以经由绝缘体 105 而热连接于框体 102a。再者，绝缘体 105 例如为硅酮。

[0163] 基座 101a 包括：灯头部 106，其为例如包含铝（Al）的金属且形成为圆板形状；以及导电体 107。灯头部 106 设置在框体 102a 的上部，且与设置在照明装置本体（未图示）的散热体热连接。导电体 107 在框体 102a 的上部设置有多个，其使开关电源装置 3a 的一对输入端子 23、24 经由照明装置本体而连接于交流电源。

[0164] 框体 102a 由例如包含铝（Al）的金属形成，周边部收纳开关电源装置 3a，中央部收纳照明光源 4。照明光源 4 与灯头部 106 热连接。照明光源 4 作为开关电源装置 3a 的照明负载 2，由开关电源装置 3a 供给电力而点灯。

[0165] 透光遮罩 103a 形成为圆板形状，其覆盖照明光源 4 而设置在框体 102a 的下部，即与框体 102a 的基座 101a 相反侧。透光遮罩 103a 使从照明光源 4 放射的光透过，并且保护照明光源 4。

[0166] 在本实施形态中，开关元件 7 也热连接于导热性比安装基板 27 高的绝缘基板 28，进而热连接于照明光源 4 与框体 102a，因此散热性得到改善。其结果，可增大照明装置 1b 的光输出功率并实现小型化。

[0167] 以上，一面参照具体例一面对实施形态进行了说明，但并不限定于这些实施形态，可进行各种变形。

[0168] 例如，开关电源装置中的 DC-DC 转换器的构成并不限定于图 3 所示的构成。只要可对直流电压进行降压即可，也可以是其他构成。

[0169] 另外，开关元件 7 及恒定电流元件 8 并不限定于 GaN 系 HEMT。例如，也可以是如下的半导体元件，即在半导体基板上使用如碳化硅（SiC）或氮化镓（GaN）或金刚石般的具有宽带隙（wideband gap）的半导体（宽带隙半导体）而形成的半导体元件。此处，所谓宽带隙半导体，是指带隙比带隙约为 1.4eV 的砷化镓（GaAs）更大的半导体。例如包括带隙为 1.5eV 以上的半导体、磷化镓（GaP，带隙约为 2.3eV）、氮化镓（GaN，带隙约为 3.4eV）、金刚石（C，带隙约为 5.27eV）、氮化铝（AlN，带隙约为 5.9eV）、以及碳化硅（SiC）等。此种宽带隙半导体元件在使耐压相等的情况下，可比硅半导体元件小，因此寄生电容小，可进行高速动作，所以可提高开关频率，并可实现电感器等绕组零件或电容器等的小型化。

[0170] 另外，照明光源 4 并不限于 LED，也可以是 OLED 等，也可以将多个照明光源 4 串联或并联地连接于照明负载 2。

[0171] 虽已对本实用新型的若干实施形态及实例进行了说明，但这些实施形态或实例是作为例子而提示的实施形态或实例，并无对实用新型的范围进行限定的意图。所述新颖的

实施形态或实例能够以其他的各种形态来实施，在不脱离实用新型的宗旨的范围内，可进行各种省略、替换、变更。这些实施形态、实例、变形及其均等的范围皆包含在本实用新型的范围中。

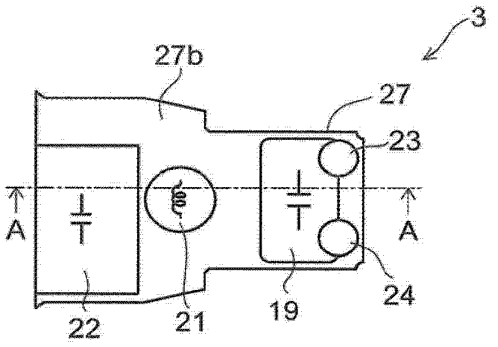


图 1(a)

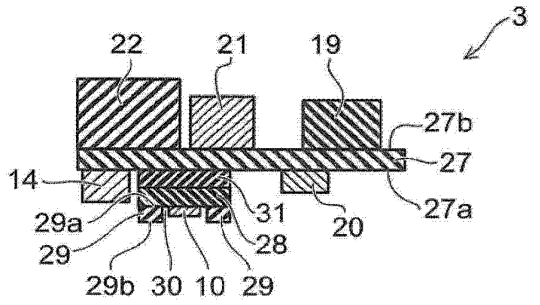


图 1(b)

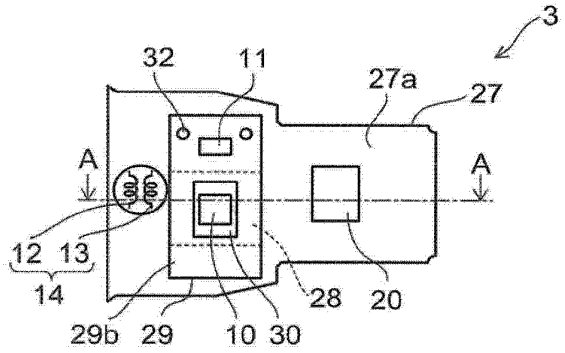


图 1(c)

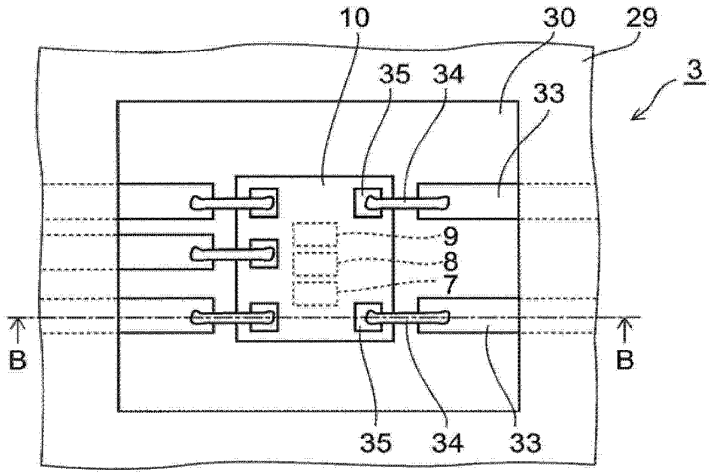


图 2(a)

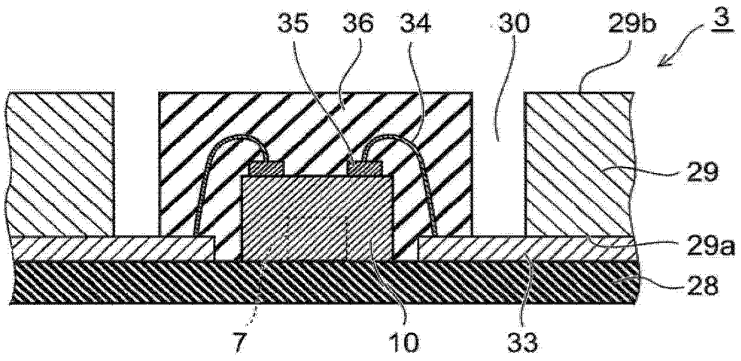

35
36
34
30
29b
3
29
29a
28
7
10
33

图 2(b)

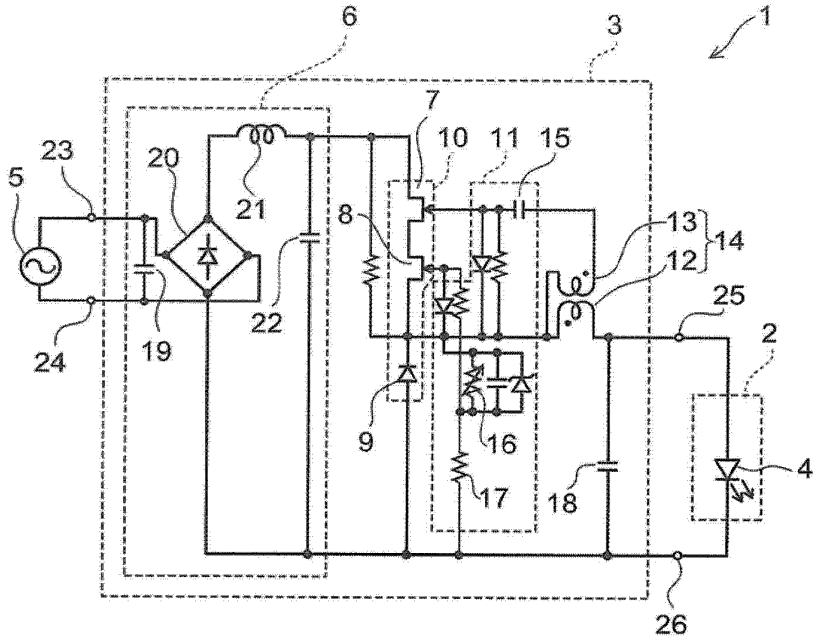

6
3
1
7
10
11
15
23
20
5
21
8
13
14
12
25
2
22
24
19
9
16
4
17
18
26

图 3

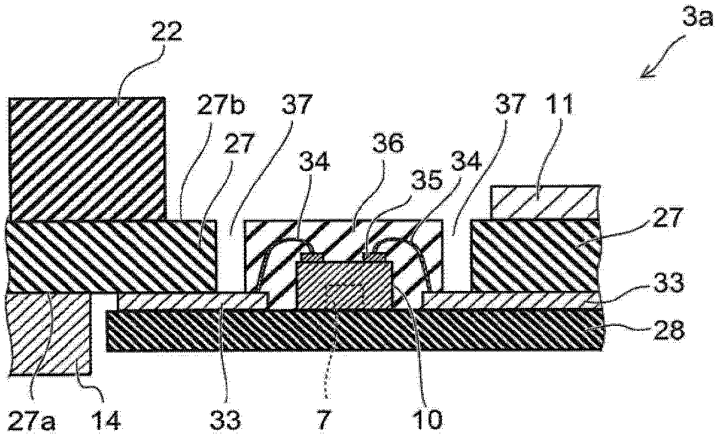

3a
22
27b
37
27
34
36
35
34
37
11
27
33
28
27a
14
33
7
10

图 4

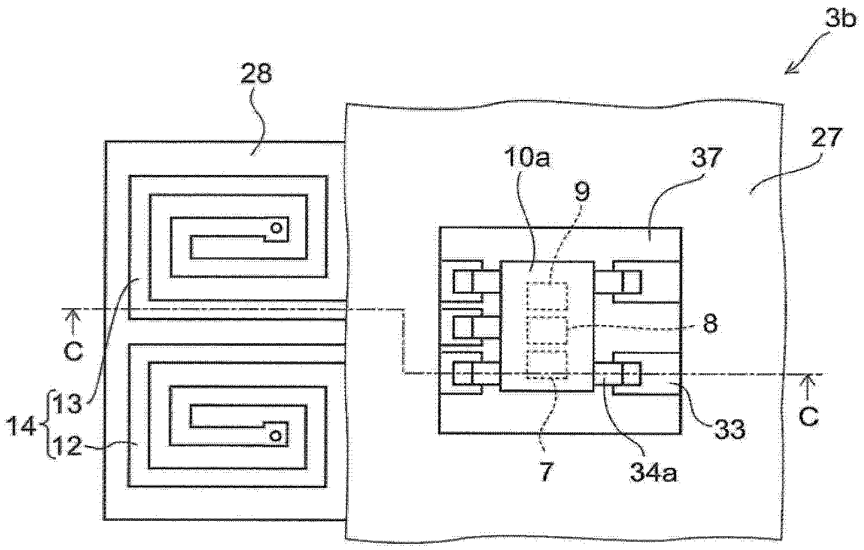

3b
28
27
10a
9
37
8
C
13
14
12
33
C
7
34a

图 5(a)

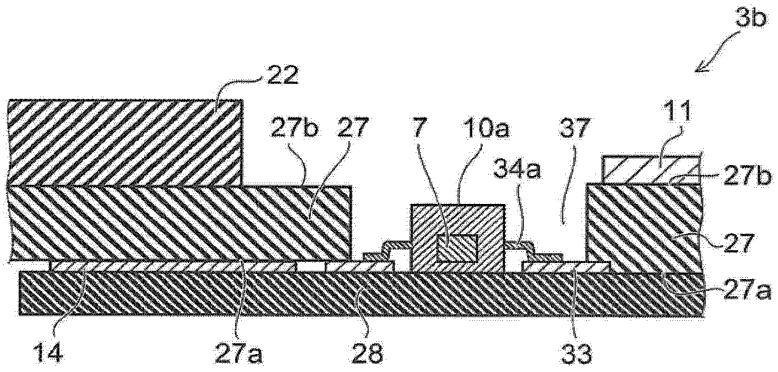


图 5(b)

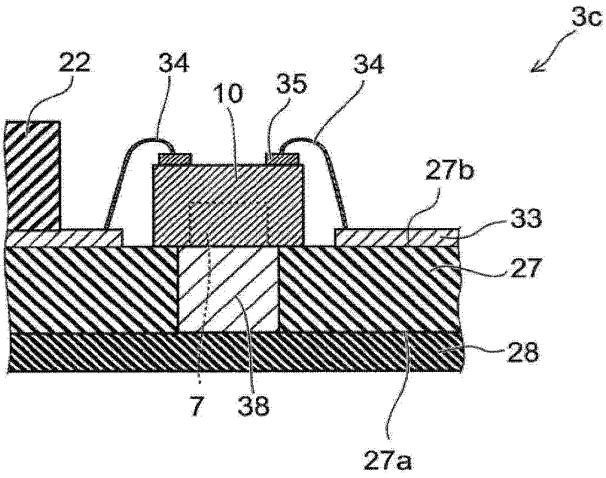


图 6

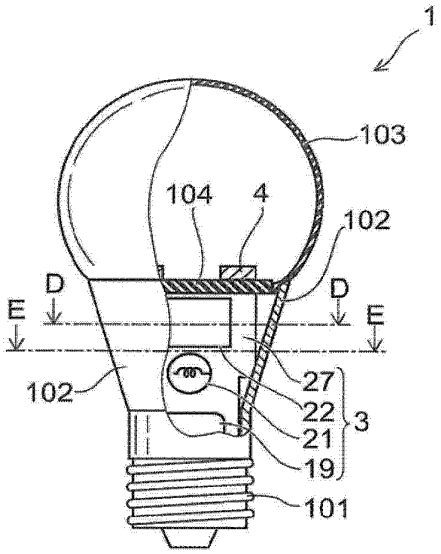


图 7(a)

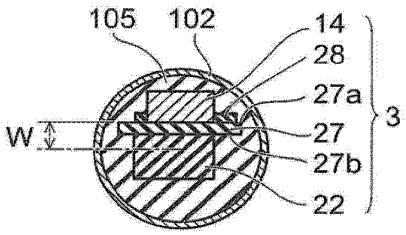


图 7(b)

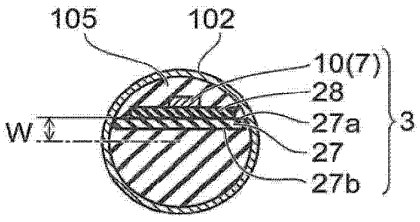


图 7(c)

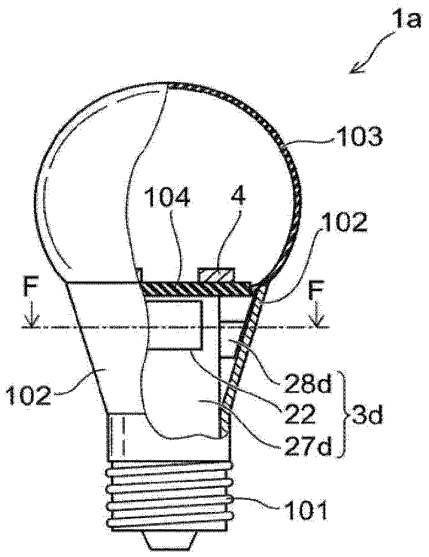

1a
103
104
4
102
F
F
102
28d
22
27d
3d
101

图 8(a)

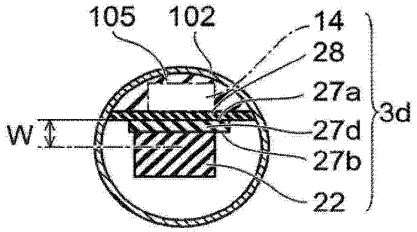

105
102
14
28
27a
27d
3d
W
27b
22

图 8(b)

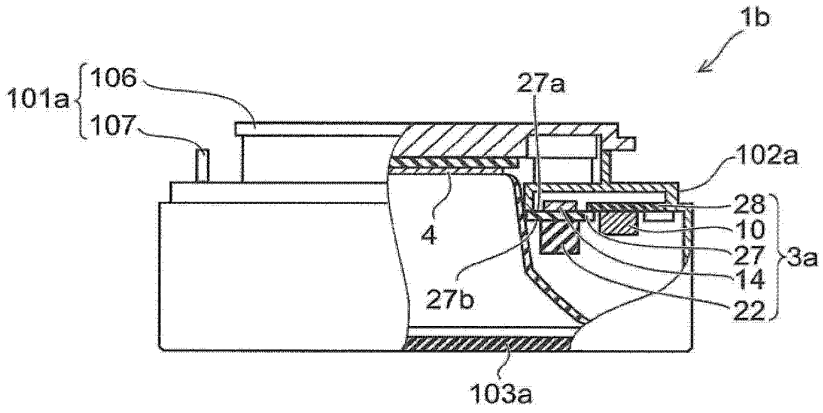

1b
101a
106
107
27a
102a
28
10
27
14
22
3a
4
27b
103a

图 9

Espacenet

Bibliographic data: TW201330190 (A) — 2013-07-16

Systems and methods for lead frame locking design features

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Applicant(s): INTERSIL INC [US] ± (INTERSIL AMERICAS INC)

Classification: - international: ***H01L23/28; H01L23/495***
- cooperative: **H01L21/4828**; **H01L23/3114**; **H01L23/495**; **H01L23/49503**; **H01L23/49541**; **H01L23/49548**; H01L2224/32245; H01L23/3107

Application number: TW20120138204 20121017

Priority number(s): US201161549523P 20111020 ; US201213446489 20120413

Also published as: US2013099366 (A1) US8497165 (B2) US2015357265 (A1) US2013285226 (A1) US9165863 (B2)

Abstract of TW201330190 (A)

Systems and methods for lead frame locking design features are provided. In one embodiment, a method comprises: fabricating a lead frame for a chip package, the lead frame having a paddle comprising a step-out bottom locking feature profile across at least a first segment of an edge of the paddle that provides an interface with a mold compound; etching the paddle to have at least a second segment of the edge having either an extended-step-out bottom locking feature profile or an overhanging top locking feature profile; and alternating first and second segments along the edge of the paddle.

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2012/04/13 美國 13/446,489
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美國
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申請實體審查：無 申請專利範圍項數：29 項 圖式數：9 共 52 頁

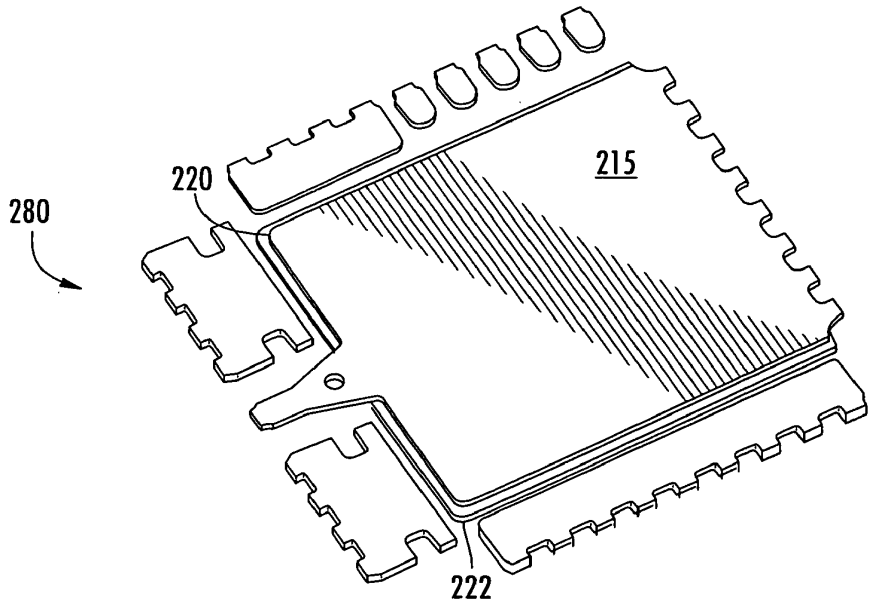
(54)名稱

引線框架鎖定設計部分之系統和方法

SYSTEMS AND METHODS FOR LEAD FRAME LOCKING DESIGN FEATURES

(57)摘要

提供了用於引線框架鎖定設計部分的系統和方法。在一個實施方案中，方法包括：製作晶片封裝的引線框架，該引線框架具有襯墊，該襯墊包括一突出底部鎖定部輪廓，其橫越該襯墊邊緣的至少第一區段，該襯墊邊緣提供與塑封料的接合部；蝕刻該襯墊為具有該邊緣的至少第二區段，該第二區段具有延長突出底部鎖定部輪廓或懸垂頂部鎖定部輪廓；和沿著該襯墊的該邊緣交替之第一區段和第二區段。



215：襯墊
220：線型突出底部鎖定部
280：襯墊俯視圖

201330190

發明專利說明書

（本說明書格式、順序，請勿任意更動，※記號部分請勿填寫）

※申請案號：101138204

※申請日：101.10.17　　※IPC分類：H01L 23/28 (2006.01)
H01L 23/495 (2006.01)

一、發明名稱：（中文/英文）

引線框架鎖定設計部分之系統和方法

SYSTEMS AND METHODS FOR LEAD FRAME LOCKING DESIGN FEATURES

二、中文發明摘要：

提供了用於引線框架鎖定設計部分的系統和方法。在一個實施方案中，方法包括：製作晶片封裝的引線框架，該引線框架具有襯墊，該襯墊包括一突出底部鎖定部輪廓，其橫越該襯墊邊緣的至少第一區段，該襯墊邊緣提供與塑封料的接合部；蝕刻該襯墊爲具有該邊緣的至少第二區段，該第二區段具有延長突出底部鎖定部輪廓或懸垂頂部鎖定部輪廓；和沿著該襯墊的該邊緣交替之第一區段和第二區段。

三、英文發明摘要：

Systems and methods for lead frame locking design features are provided. In one embodiment, a method comprises: fabricating a lead frame for a chip package, the lead frame having a paddle comprising a step-out bottom locking feature profile across at least a first segment of an edge of the paddle

that provides an interface with a mold compound; etching the paddle to have at least a second segment of the edge having either an extended-step-out bottom locking feature profile or an overhanging top locking feature profile; and alternating first and second segments along the edge of the paddle.

四、指定代表圖：

(一)本案指定代表圖為：圖　。

(二)本代表圖之元件符號簡單說明:

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

無

六、發明說明：

相關申請的交叉參考

本申請要求2011年10月20日申請的名爲“SYSTEMS AND METHODS FOR LEAD FRAME LOCKING DESIGN FEATURES”的美國臨時申請 61/549,523 的權益和優先權，該申請以引用的方式並入本文。

技術領域

本發明涉及防止晶片封裝分層和斷裂的系統和方法。

發明背景

安裝好的晶片封裝遭受可能導致晶片封裝分層或斷裂的應力。例如，晶片封裝遭受由來自周圍環境和/或元件熱迴圈、高電負載、高溫熱環境、晶片封裝安裝期間所施加的衝擊負載或類似因素的熱應力導致的應力。應力可能導致剪力和撓曲應力的積累，其易於在晶片封裝錨固至在晶片封裝內包封一個或多個晶粒和引線框架的塑封料處形成。剪應力和撓曲應力的積累會導致晶片封裝分層或斷裂。

發明概要

提供引線框架鎖定設計部的系統和方法。在一個實施方案中，方法包括：製作晶片封裝的引線框架，該引線框架具有包括跨提供與塑封料的介面的襯墊的邊緣的至少第一區段的突出底部鎖定部輪廓的襯墊；蝕刻襯墊爲具有邊緣的至少第二區段，該第二區段具有延長突出底部鎖定部輪廓或懸垂頂部鎖定部輪廓；和沿著襯墊的邊緣交替第一區段和第二區段。

具體實施方式

在下文詳細描述中，參考附圖，該附圖形成其部分且在其中是經由可實踐本發明的特定說明性實施方案來示出。充分詳細地描述這些實施方案使得本領域技術人員能夠實踐本發明，且應瞭解可使用其他實施方案以及可進行邏輯、機械和電變更而不脫離本發明的範圍。所以，下文詳細描述不得以限制意義來理解。

本發明的實施方案提供解決由於剪應力和撓曲應力的積累而導致的晶片封裝（諸如積體電路、半導體或其他矽裝置）的分層和斷裂，該剪應力和撓曲應力易於在晶片封裝的引線框架錨固至在晶片封裝內包封一個或多個晶粒和引線框架的塑封料處形成。這是通過引入將塑封料聯鎖至襯墊的新穎機械襯墊表面破裂鎖定部來實現的。這些應力可能由例如來自周圍環境和/或元件熱迴圈、高電負載、高溫熱環境、晶片封裝安裝期間所施加的衝擊負載的熱應力導致。諸如這些應力以及其他原因的影響可基於本公開該的實施方案所說明的技術來緩解。

如本文中所使用的術語，引線框架對裝置（例如，諸如晶粒）提供機械支撐且包括附著晶粒的襯墊和提供外部電連接的引線。例如，晶粒可通過打線接合或其他連接方法連接至引線。封裝介面剪應力可能引起引線框架和塑封料分層。在存在分層的情況下，封裝所引起的撓曲應力可能在引線框架熱墊邊緣上增大超過 4 倍。因此，通過防止分層，本發明的實施方案旨在減小應力和消除封裝斷裂。

解決分層對於使用因其更高的電性能和熱性能而在許多電力產品中廣泛使用且具有高楊氏模量性質的晶粒附著粘合材料（例如，諸如焊料）的產品尤爲關鍵。通過解決分層情況，可控制拉伸應力使其不增大超過包封材料撓曲強度，因此防止封裝斷裂。

本發明的實施方案可實施於任何基於引線框架的晶片封裝（諸如但不限於電源方形扁平無引線（PQFN）、方形扁平無引線（QFN）、小尺寸積體電路（SOIC）、薄型縮小尺寸封裝（TSSOP）、方形小尺寸封裝（QSOP）、縮小尺寸封裝（SSOP）等），以解決介面分層和濕度敏感等級（MSL）問題並且消除封裝包封斷裂。此外，本文提出的設計部件可用于增進其他 MSL 改進技術以進一步優化性能。

圖 1A 至圖 1C 是介紹本發明的一個或多個實施方案所使用的鎖定部（示爲 110、120 和 130）的不同外形的圖。每個圖是以圖示襯墊 105 的邊緣的橫截面剖面圖繪製，其中表面 107 是頂表面（例如，其中可如下圖所示般安裝晶粒）且表面 106 是底表面。這些外形在實施在晶片封裝內時各用於減小襯墊的邊緣處的剪應力以防止分層開始。即，使用這些表面破裂鎖定部改進了襯墊與塑封料相接的介面處的機械聯鎖，因此減小晶片封裝中分層及斷裂形成的機率。

圖 1A 中大致示爲 110 的第一鎖定部輪廓圖示了包括本文中所稱的懸垂頂部鎖定部輪廓的襯墊 105 的邊緣。懸垂頂部鎖定部輪廓 110 的特徵爲沿著襯墊 105 的底表面 106

的邊緣並且進入其中的部分蝕刻 112，其導致懸垂部分蝕刻 112 的從頂表面 107 開始的懸垂 114。在一個實施方案中，懸垂頂部鎖定部輪廓 110 是通過從底表面 106 蝕刻至襯墊 105 中達 0.100±0.030 mm 的深度“d”以形成具有 0.050±0.006 mm 的寬度“w”的懸垂 114 來形成。

圖 1B 中大致示爲 120 的第二鎖定部輪廓圖示了包括本文中所稱的突出底部鎖定部輪廓的襯墊 105 的邊緣。突出底部鎖定部輪廓 120 的特徵爲沿著襯墊 105 的頂表面 107 並且進入其中的部分蝕刻 122（示爲寬度 w_1），其導致從底表面 106 開始的突出 124。在一個實施方案中，突出底部鎖定部輪廓 120 是通過從頂表面 107 蝕刻至襯墊 105 中達 0.127±0.050 mm 的深度“d”以形成具有 0.050±0.006 mm 的寬度 w_1 的突出 124 來形成。

圖 1C 中大致示爲 130 的第三鎖定部輪廓圖示了包括本文中所稱的延長邊緣突出底部鎖定部輪廓的襯墊 105 的邊緣。延長邊緣突出底部鎖定輪廓 130 是旨在結合突出底部鎖定部輪廓 120 使用的突出底部鎖定部輪廓 120 的形式。延長邊緣突出底部鎖定輪廓 130 的特徵爲沿著頂表面 107 並且進入其中的部分蝕刻 132，其具有大於部分蝕刻 122 寬度 w_1 的寬度（示爲寬度 w_2）。這導致從襯墊 105 的底表面 106 開始且具有大於突出 124 的寬度的突出 134。在一個實施方案中，突出底部鎖定部輪廓 120 是通過從頂表面 107 蝕刻至襯墊 105 中達 0.127±0.050 mm 的深度“d”以形成具有 0.150±0.006 mm 的寬度 w_1 的突出 134 來形成。

可將晶片封裝的襯墊製成包括由鎖定部輪廓 110、120 和 130 的不同組合形成的鎖定部。當如下文不同實施方案該般配置時，這些襯墊鎖定部 110、120 和 130 沿著襯墊 105 的邊緣實施表面破裂圖案以通過改進聯鎖和應力再分佈而防止封裝斷裂發生和蔓延。

在一些實施方案中，引線框架可通過衝壓或蝕刻而由平板金屬製成。蝕刻形成鎖定部輪廓 110、120 和 130 涉及根據所要的引線框架圖案選擇性地用光阻劑覆蓋板金屬。板金屬隨後暴露於化學蝕刻劑，該化學蝕刻劑去除未被光阻劑覆蓋的區域。在蝕刻過程後，經蝕刻的框架被切割成條。衝壓是採用模具和衝擊裝置通過一系列衝壓/衝擊步驟逐漸實現所要鎖定部輪廓 110、120 和 130 的機械過程。對於一些實施方案，在衝壓或蝕刻後，隨後用清潔、鍍銀、貼膠和下移設置步驟完成引線框架。鍍銀可在接合指狀物和晶粒墊上完成以改進打線接合和晶粒附著質量。貼膠可包括在引線上方放置引線鎖定膠帶以防止引線變形，同時下移設置可包括根據標準行業規定相對于接合指狀物下推襯墊。雖然本公開主要結合“蝕刻”的懸垂和突出部討論襯墊鎖定部 110、120 和 130，但是本領域的一般技術人員在閱讀本公開時能理解本申請中所討論的任何懸垂和突出部可通過衝壓而非蝕刻形成。

圖 2A 至圖 2D 是圖示本發明的一個實施方案的晶片封裝 200 的圖。大致如圖 2B 中的橫截面圖 210 所示，至少一個晶粒 212 通過晶粒附著材料 213（例如，其可爲焊料或樹

脂粘合劑）固定至襯墊 215。圖 2A 在 230 圖示了從襯墊 215 的頂表面蝕刻而來的邊緣 216 和 217 的部分蝕刻。襯墊 215 的邊緣 216 和 217 各包括示爲 220 和 222 的線型突出底部鎖定部。即，襯墊 215 的整個邊緣 216 已從頂部（如圖 205 中頂部部分蝕刻 230 所示）部分蝕刻爲具有如突出底部鎖定部輪廓 120 所示的輪廓。類似地，襯墊 215 的整個邊緣 217 已從頂部（如圖 205 中頂部部分蝕刻 230 所示）部分蝕刻爲具有如突出底部鎖定部輪廓 110 所示的輪廓。

還圖示了底部部分蝕刻 240，其中從襯墊 215 的底表面執行部分蝕刻。例如，在一個實施方案中，一個或多個第二元件 250 從底部部分蝕刻以提供具有懸垂頂部鎖定部（諸如圖 2B 中 255 所示）的元件。鎖定部 220 與 255 之間的體積 260 填充塑封料 262，該塑封料填充部分蝕刻區域 230 和 240，因此將襯墊 215 和晶粒 212 錨固至晶片封裝 200 內的塑封料 262。圖 2C 在 280 處提供圖示線型突出底部鎖定部 220 和 222 的襯墊 215 的俯視圖。圖 2D 在 285 處提供圖示突出底部鎖定部 255 的襯墊 215 的仰視圖。這些部件以邊緣 216 和 217 形成連續線的意義描述爲“線型”。

圖 3A 至圖 3D 圖示了通過組合不同的輪廓區段以形成不連續邊緣而不是線型邊緣而形成的鎖定部。圖 3A 圖示了根據本發明的一個實施方案的晶片封裝 300 的俯視圖。圖 3B 和圖 3C 圖示了晶片封裝 300 的對應橫截面圖 310 和 311。在本實施方案中，至少一個晶粒 312 通過晶粒附著材料 313（例如，其可爲焊料或樹脂粘合劑）固定至襯墊 315。

襯墊 315 的邊緣 316 和 317 各包括 320 和 322 所示且本文中所稱的不連續突出底部鎖定部。

圖 3A 圖示了從襯墊 315 的頂表面蝕刻而來的邊緣 316 和 317 的部分蝕刻。區段 331 包括具有突出底部鎖定部輪廓 120 的邊緣 316 和 317 的長度。區段 332 包括具有延長突出底部鎖定部輪廓 130 的邊緣 316 和 317 的長度。在一個實施方案中，還圖示了底部部分蝕刻 340，其中從襯墊 315 的底表面執行部分蝕刻。例如，在一個實施方案中，一個或多個第二元件 350 從底部部分蝕刻以提供具有懸垂頂部鎖定部（諸如圖 3B 和 3C 中 355 所示）的元件。鎖定部 320/322 與 355 之間的體積 360 填充塑封料 362，該塑封料 362 填充鎖定部 320/322 和 340 的部分蝕刻區段，因此將襯墊 315 和晶粒 312 錨固至晶片封裝 300 內的塑封料 362。

如圖 3A 所示，襯墊 315 的邊緣 316 已從頂部部分蝕刻（示爲頂部部分蝕刻 330）爲具有組合突出底部鎖定部輪廓 120（圖 3B 所示）和延長突出底部鎖定部輪廓 130（圖 3C 所示）的交替區段的輪廓。類似地，襯墊 315 的邊緣 317 已從頂部部分蝕刻（示爲頂部部分蝕刻 330）爲具有組合突出底部鎖定部輪廓 120（圖 3B 所示）和延長突出底部鎖定部輪廓 130（圖 3C 所示）的交替表面破裂區段的輪廓。

通過組合具有這些不同輪廓的交替表面破裂區段 331 和 332，結果是襯墊 315 與塑封料 362 之間的襯墊 315 的頂部上有不連續介面。換句話說，所得介面不是連續的線而是在不同區段間具有不連續。圖 3D 提供襯墊（諸如襯墊

215）的線型邊緣與襯墊（諸如襯墊 315）的不連續邊緣的簡化對比。與圖 2A 和圖 2B 的線型鎖定部相比，在不連續介面中導致塑封料分層和破裂所需的表面張力因該張力沿著襯墊 315 的邊緣行進更大距離而增大。此外，不連續圖案要求塑封料-襯墊介面上的應力改變方向以進一步蔓延，其進一步阻礙這種蔓延。不連續狀設計部充當分層止擋。若存在發生的局部化分層，那麼不連續鎖定部將控制該分層，防止其自由蔓延。爲此原因，不連續狀鎖定部還用於使斷裂發生。通常，不連續狀鎖定部在塑封料與引線框架之間在這些元件引線界接的臨界應力集中區域的介面處促進引線機械聯鎖。因此，包括沿著晶粒附著襯墊 315 的邊緣的表面破裂交替圖案的鎖定部通過針對塑封料改進襯墊聯鎖和應力再分佈而防止封裝分層和斷裂發生和蔓延。

圖 4A 至圖 4G 圖示了具有通過組合不同的輪廓區段以形成不連續邊緣而不是線型邊緣而形成的鎖定部的其他實施方案。圖 4A 圖示了晶片封裝 400 的俯視圖。圖 4B 和圖 4C 提供晶片封裝 400 的橫截面圖 410 和 411。在本實施方案中，至少一個晶粒 412 通過晶粒附著材料 413（例如，其可爲焊料或樹脂粘合劑）固定至襯墊 415。邊緣 416 被製成包括 420 所示且本文中所稱的不連續懸垂頂部鎖定部。即，襯墊 415 的邊緣 416 已從頂部部分蝕刻（示爲頂部部分蝕刻 430）及從底部部分蝕刻（示爲底部部分蝕刻 432）爲具有通過組合突出底部鎖定部輪廓 120（圖 4B 中 410 所示）與懸垂頂部鎖定部輪廓 110（圖 4C 中 411 所示）的交替表

面破裂區段而形成的輪廓。區段 433 包括具有懸垂頂部鎖定部輪廓 110 的邊緣 416 的長度而區段 431 包括具有突出底部鎖定部輪廓 130 的邊緣 416 的長度。

圖 4A 中還圖示了底部部分蝕刻 440，其中從襯墊 415 的底表面執行部分蝕刻。例如，在一個實施方案中，一個或多個第二元件 450 從底部部分蝕刻以提供具有懸垂頂部鎖定部 455（如圖 4B 和圖 4C 所示）的元件。鎖定部 420 與 455 之間的體積 460 填充塑封料 462，該塑封料填充部分蝕刻區域 430、432 和 440，因此將襯墊 415 和晶粒 412 錨固至晶片封裝 400 內的塑封料 462。

如圖 4D 和圖 4E 所示，通過組合交替表面破裂區段 431 和 433，結果是襯墊 415 與塑封料 462 之間的襯墊 415 頂部上有不連續介面，其並入懸垂頂部鎖定部輪廓 110 和突出底部鎖定部輪廓 120 兩者。圖 4D 在 488 處提供襯墊 415 的俯視圖。圖 4D 在 485 處提供襯墊 415 的仰視圖。圖 4F 提供示出襯墊 415 的區段 431 的突出底部輪廓與區段 433 的懸垂頂部輪廓之間的空間關係的另一圖。

通過組合交替的表面破裂區段 431 和 433，結果是襯墊 415 與塑封料 462 之間的襯墊 415 頂部上有不連續介面。與圖 2A 和圖 2B 的線型鎖定相比，導致分層所需的表面張力因通過沿著襯墊 415 的邊緣的改進的連鎖部而實現的減小的剪應力而增大。與圖 3A 至圖 3C 的線型鎖定相比，導致分層以及塑封料破裂所需的表面張力也進一步增大。通過不連續懸垂頂部鎖定部 420 提供的不連續圖案需要塑封料-

襯墊介面上的應力改變方向以進一步蔓延，其進一步阻止此蔓延。即，不連續狀設計部充當分層止擋。即存在發生的局部化分層，不連續鎖定部將控制該分層，防止其自由蔓延。爲此原因，不連續狀鎖定部還用於阻止斷裂生長。通常，不連續狀鎖定部在塑封料與引線框架之間在界接這些元件的的臨界應力集中區域的介面處促進引線機械聯鎖。因此，包括沿著晶粒附著襯墊 415 的邊緣的表面破裂交替圖案的鎖定部通過針對襯墊聯鎖和應力再分佈改進塑封料而防止封裝分層和斷裂發生和蔓延。圖 4G 爲說明示例性尺寸的目的而圖示具有 620 所示的不連續懸垂頂部鎖定部的襯墊 615。

圖 5 是圖示具有襯墊 515 的晶片封裝 500 的替代實施方案的圖，其提供作爲上文參考圖 4A 至圖 4C 該的不連續懸垂頂部鎖定部的替代不連續懸垂頂部鎖定部 520。在一個實施方案中，晶粒 512 被安裝至襯墊 515。如圖 5 所示，不連續懸垂頂部鎖定部 520 包括包括懸垂頂部鎖定部輪廓 120 的區段 431 和包括突出底部鎖定部輪廓 130 的區段 433。襯墊 515' 的鎖定部 520 還包括位於每個交替區段 431 與 433 之間的間隔 533。在一個實施方案中，間隔 533 是不提供鎖定部的襯墊 515 的邊緣的部分。圖 5 圖示了具有 .076 mm 的尺寸的間隔 533。包括間隔 533 對於沒有足夠精度的處理設備以在懸垂頂部鎖定部輪廓 110 與直接鄰近的突出底部鎖定部輪廓 120 之間交替的製造設施而言是有利的。

本領域一般技術人員應瞭解本公開中提供的任何尺寸

僅爲舉例的目的並且可任選地使用。但是，其不得視作對其他實施方案的限制。此外，如本說明書中已經使用的術語“部分蝕刻”指的是未從襯墊的一個表面穿透至相對表面的任何深度的蝕刻。例如，對於本公開中該的任何實施方案，從襯墊頂部開始的部分蝕刻的示例性深度爲 0.127 mm±0.050 mm 的數量級，而從襯墊底部開始的部分蝕刻的示例性深度爲 0.100 mm±0.030 mm 的數量級。此外，例如，使用交替不連續區段的鎖定部可具有沿著襯墊邊緣 0.150±0.006 mm 量級的長度。但是，預期有其他尺寸的鎖定部並且該鎖定部可基於諸如總晶片封裝的尺寸比例、所使用的塑封料的材料特性和運行時的熱考量的因素確定。

諸如上文參考襯墊 415 和 515 說明，使用交替鎖定部區段的優點在於其解決涉及所有三個尺寸發生的應力，例如，如圖 6A（如 610 大致所示）、圖 6B（如 620 大致所示）和圖 6C（如 630 大致所示）所示，輪廓 611 的交替區段在每個 XY、XZ 和 YZ 平面中提供不連續以防止任何這些平面中的分層和斷裂發生。

圖 7 圖示了如參考任何上述公開實施方案的一個或多個鎖定部輪廓 110、120 及 130 的本發明的一個實施方案的方法。方法從 710 製作晶片封裝的引線框架開始，引線框架具有襯墊，該襯墊包括跨該襯墊中提供與塑封料的界接的邊緣的至少第一區段的突出底部鎖定部輪廓。方法繼續至 720，將襯墊製成包括具有延長突出底部鎖定部輪廓的邊緣的至少第二區段，其中第二區段的突出具有大於第一區

段的突出的寬度。通過沿著襯墊邊緣交替的第一表面破裂區段及第二表面破裂區段（730所示），提供諸如參考圖3A該的鎖定部。

圖8圖示了本發明的一個實施方案的另一方法。方法從810製作晶片封裝的引線框架開始，引線框架具有襯墊，該襯墊包括跨在該襯墊中提供與塑封料的界接的邊緣的至少第一區段的突出底部鎖定部輪廓。方法繼續至820，其中將襯墊製成具有邊緣的至少一個第二區段，該第二區段具有懸垂頂部鎖定部輪廓。通過沿著襯墊邊緣交替第一表面破裂區段和第二表面破裂區段（830所示），提供諸如參考圖4A該的鎖定部。在一個實施方案中，方法繼續至840，其中在每個第一區段與第二表面破裂區段之間提供第三區段，該第三區段提供無鎖定部的間隔。以此方式，提供諸如參考圖5A該的鎖定部。

圖7或圖8的任一方法中引線的製作可包括蝕刻或衝壓引線框架來製作第一區段的突出底部鎖定部和第二區段的延長突出底部鎖定部輪廓。方法可任選地繼續至將襯墊包封在塑封料中，其將第一區段和第二區段固定至塑封料。在一些實施方案中，襯墊還可包括安裝至襯墊的至少一個晶粒。因此，方法還可包括將襯墊和至少一個晶粒包封在塑封料中，其將第一區段和第二區段固定至塑封料。在一些實施方案中，引線框架可包括具有懸垂頂部鎖定部輪廓的襯墊的一個或多個第二元件。這些第二元件還可由塑封料包封並且通過懸垂頂部鎖定部輪廓固定至塑封料。

圖 9 圖示了包括控制器 910 的本發明的一個實施方案的系統 900，該控制器 910 包括諸如參考任何上述實施方案該的晶片封裝的晶片封裝 915。例如，在一個實施方案中，晶片封裝 915 使用線型突出底部鎖定部。在另一實施方案，晶片封裝 915 使用包括交替的突出底部鎖定部輪廓和延長邊緣突出底部鎖定部輪廓的不連續突出底部鎖定部。在另一實施方案中，晶片封裝 915 使用包括交替的突出底部鎖定部輪廓和懸垂頂部鎖定部輪廓的不連續懸垂頂部鎖定部。在一個這樣的實施方案中，在突出底部鎖定部輪廓與懸垂頂部鎖定部輪廓的交替區段之間提供間隔區段。在其他實施方案中，使用具有線型突出底部鎖定部、不連續突出底部鎖定部和不連續懸垂頂部鎖定部的組合的晶片封裝 915。

在一個實施方案中，控制器 910 是電力控制器。控制器 910 從電源 905 提供電力並且在一個實施方案中提供輸出至至少一個元件，諸如調節元件 920。在一個實施方案中，控制器 910 任選地接收來自調節元件 920 的反饋回路信號，該反饋回路信例如可由晶片封裝 915 用於控制控制器輸出。在一個實施方案中，系統 900 提供輸出至負載元件 930，該輸出至少部分由晶片封裝 915 控制。在一些實施方案中，晶片封裝 915 可包括高功率或高速運算放大器（Op Amp）。

<u>示例性實施方案</u>

實施例 1 包括晶片封裝，其包括：引線框架；至少一

個晶粒，其安裝至引線框架；其中引線框架的至少第一部分具有包括突出底部鎖定部輪廓的鎖定部；和塑封料，其包封引線框架和至少一個晶粒；其中引線框架通過鎖定部固定至塑封料。

實施例 2 包括實施例 1 的晶片封裝，其中鎖定部是線型突出底部鎖定部。

實施例 3 包括實施例 1 或實施例 2 任一者的晶片封裝，其中鎖定部還包括引線框架的第二部分，該第二部分包括延長邊緣突出底部鎖定部輪廓。

實施例 4 包括實施例 3 的晶片封裝，其中鎖定部是不連續突出底部鎖定部。

實施例 5 包括任何實施例 1 至實施例 4 的晶片封裝，其中鎖定部還包括引線框架的第二部分，該第二部分包括懸垂頂部鎖定部輪廓。

實施例 6 包括實施例 5 的晶片封裝，其中鎖定部是不連續懸垂頂部鎖定部。

實施例 7 包括實施例 5 的晶片封裝，其中鎖定部還包括第三部分，該第三部分包括懸垂頂部鎖定部輪廓與突出底部鎖定部輪廓之間的間隔區段。

實施例 8 包括任何實施例 5 至實施例 7 的晶片封裝，其還包括具有懸垂頂部鎖定部輪廓的一個或多個第二元件，其中一個或多個第二元件通過懸垂頂部鎖定部輪廓固定至塑封料。

實施例 9 包括一種方法，其包括：蝕刻晶片封裝的襯

墊爲具有跨該襯墊中與塑封料界接的邊緣的至少第一區段的突出底部鎖定部輪廓；蝕刻襯墊爲具有邊緣的至少第二區段，該第二區段具有延長突出底部鎖定部輪廓，其中第二區段的突出具有大於第一區段的突出的寬度；和沿著襯墊的邊緣交替第一區段和第二區段。

實施例 10 包括實施例 9 的方法，其還包括：將至少一個晶粒固定至襯墊。

實施例 11 包括任何實施例 9 至 10 的方法，其還包括：將襯墊和至少一個晶粒包封在塑封料中，其將第一區段和第二區段固定至塑封料。

實施例 12 包括實施例 11 的方法，其還包括：部分蝕刻襯墊的一個或多個第二元件爲具有懸垂頂部鎖定部輪廓，其中一個或多個第二元件通過懸垂頂部鎖定部輪廓固定至塑封料。

實施例 13 包括一種方法，其包括：蝕刻晶片封裝的襯墊爲具有跨該襯墊中與塑封料界接的邊緣的至少第一區段的突出底部鎖定部輪廓；蝕刻襯墊爲具有邊緣的至少一個第二區段，該第二區段具有懸垂頂部鎖定部輪廓；沿著襯墊的邊緣交替第一區段和第二區段。

實施例 14 包括實施例 13 的方法，其還包括：蝕刻襯墊以在每個第一區段與第二區段之間提供第三區段，該第三區段提供無鎖定部的間隔。

實施例 15 包括任何實施例 13 至 14 的方法，其還包括：將至少一個晶粒固定至襯墊。

實施例 16 包括實施例 15 的方法，其還包括：將襯墊和至少一個晶粒包封在塑封料中，其將第一區段和第二區段固定至塑封料。

實施例 17 包括實施例 16 的方法，其還包括：部分蝕刻襯墊的一個或多個第二元件爲具有懸垂頂部鎖定部輪廓，其中一個或多個第二元件通過懸垂頂部鎖定部輪廓固定至塑封料。

實施例 18 包括一種系統，其包括：電源；控制器，其具有包括安裝至引線框架的至少一個晶粒的晶片封裝，其中引線框架的至少第一部分具有至少包括突出底部鎖定部輪廓的鎖定部；和元件，其接收控制器的輸出。

實施例 19 包括實施例 18 的系統，其中鎖定部還包括引線框架的第二部分，該第二部分包括延長邊緣突出底部鎖定部輪廓。

實施例 20 包括任何實施例 18 至 19 的系統，其中鎖定部還包括引線框架的第二部分，該第二部分包括懸垂頂部鎖定部輪廓。

實施例 21 包括實施例 20 的系統，其中鎖定部是不連續懸垂頂部鎖定部。

實施例 22 包括任何實施例 20 至 21 的系統，其中鎖定部還包括第三部分，該第三部分包括懸垂頂部鎖定部輪廓與突出底部鎖定部輪廓之間的間隔區段。

系統 23 包括任何實施例 20 至 22 的系統，其中控制器接收來自元件的反饋信號，該反饋信號由晶片封裝用於控

制控制器的輸出。

實施例24包括任何實施例18至23的系統，晶片封裝還包括：塑封料，其包封引線框架和至少一個晶粒；其中引線框架通過鎖定部固定至塑封料。

實施例25包括實施例24的系統，晶片封裝還包括具有懸垂頂部鎖定部輪廓的一個或多個第二元件，其中一個或多個第二元件通過懸垂頂部鎖定部輪廓固定至塑封料。

本說明書中使用的相對位置的術語是基於平行於晶片或基板的常規平面或工作表面的平面來界定，而不考慮晶片或基板的定向。如本說明書中使用的術語“水平”或“側向”定義爲平行於晶片或基板的常規平面或工作表面，而不考慮晶片或基板的定向。術語“垂直”指的是垂直于水平的方向。諸如“上”、“側”（如“側壁”中）、“較高”、“較低”、“上方”、“頂部”、“底部”和“下方”的術語相對於位於晶片、基板或引線框架頂表面上的常規平面或工作表面定義，而不考慮晶片或基板的定向。尺寸是爲說明的目的而提供且不應被視爲限制性。

雖然本文中已說明和描述特定實施方案，但是本領域一般技術人員應瞭解被計算來實現相同目標的任何配置可替代所示的特定實施方案。上述每個實施方案的元件可彼此組合以提供其他實施方案。本申請旨在覆蓋本發明的任何修改或變動。所以，本發明明顯旨在僅受權利要求和其等效物限制。

附圖簡述

在結合優選實施方案的描述和附圖考慮時可以更容易理解本發明的實施方案以及更易於明白其其他優點和用途，其中：

圖 1A 至圖 1C 是圖示本發明的一個或多個實施方案中所使用的表面破裂鎖定部的不同外形的剖面圖；

圖 2A 至圖 2D 是圖示本發明的一個或多個實施方案的表面破裂鎖定部的圖；

圖 3A 至圖 3D 是圖示本發明的一個或多個實施方案的表面破裂鎖定部的圖；

圖 4A 至圖 4G 是圖示本發明的一個或多個實施方案的表面破裂鎖定部的圖；

圖 5 是圖示圖 4A 至圖 4D 所展示的實施方案的變動的圖；

圖 6A 至圖 6C 是圖示具有多個尺寸的表面破裂鎖定部的一個實施方案的實施例的圖；

圖 7 和圖 8 圖示了本發明的一個或多個實施方案的方法；和

圖 9 圖示了本發明的一個實施方案的系統。

根據慣例，不同的該部件未按比例繪製而是被繪製來強調與本發明相關的部件。在附圖和正文各處，參考符號表示相同元件。

圖中主要元件的參考符號列表

七、申請專利範圍：

1.一種晶片封裝，其包括：

引線框架，其具有襯墊；

其中該引線框架的至少第一部分具有包括突出底部鎖定部輪廓的鎖定部；和

塑封料，其包封該引線框架和該至少一個晶粒；

其中該引線框架藉由該鎖定部固定至該塑封料。

2.如申請專利範圍第1項之晶片封裝，其進一步包括安裝至該襯墊的至少一個晶粒。

3.如申請專利範圍第1項之晶片封裝，其中該鎖定部進一步包括該引線框架的第二部分，該第二部分包括延長邊緣突出底部鎖定部輪廓。

4.如申請專利範圍第3項之晶片封裝，其中該鎖定部包括不連續突出底部鎖定部。

5.如申請專利範圍第1項之晶片封裝，其中該鎖定部進一步包括該引線框架的第二部分，該第二部分包括懸垂頂部鎖定部輪廓。

6.如申請專利範圍第5項之晶片封裝，其中該鎖定部是不連續懸垂頂部鎖定部。

7.如申請專利範圍第5項之晶片封裝，其中該鎖定部另外包括第三部分，該第三部分包括在該懸垂頂部鎖定部輪廓與該突出底部鎖定部輪廓之間的間隔區段。

8.如申請專利範圍第5項之晶片封裝，其還包括具有懸垂頂部鎖定部輪廓的一個或多個第二元件，其中該一個或

多個第二元件係藉由該懸垂頂部鎖定部輪廓固定至該塑封料。

9.一種方法，其包括：

製作用於晶片封裝的引線框架，該引線框架具有襯墊，該襯墊包括突出底部鎖定部輪廓，其橫越該襯墊邊緣的至少第一區段，該襯墊邊緣提供與塑封料的接合部的；

將該襯墊製成包括該邊緣的至少第二區段，該第二區段具有延長突出底部鎖定部輪廓，其中該第二區段的突出具有大於該第一區段的突出的寬度；和

沿著該襯墊的該邊緣交替的第一區段和第二區段。

10.如申請專利範圍第9項的方法，其還包括：

將至少一個晶粒固定至該襯墊。

11.如申請專利範圍第10項該的方法，其還包括：

將該襯墊和該至少一個晶粒包封在塑封料中，其將該第一區段和該第二區段固定至該塑封料。

12.如申請專利範圍第11項的方法，其還包括：

將該襯墊的一個或多個第二元件製成具有懸垂頂部鎖定部輪廓，其中該一個或多個第二元件係藉由該懸垂頂部鎖定部輪廓固定至該塑封料。

13.如申請專利範圍第9項的方法，其還包括蝕刻該引線框架以製作該第一區段的該突出底部鎖定部和該第二區段的該延長突出底部鎖定部輪廓。

14.如申請專利範圍第9項的方法，其還包括衝壓該引線框架以製作該第一區段的該突出底部鎖定部和該第二區

段的該延長突出底部鎖定部輪廓。

15.一種方法，其包括：

製作用於晶片封裝的引線框架，該引線框架具有襯墊，該襯墊包括突出底部鎖定部輪廓，其橫越該襯墊邊緣的至少第一區段，該襯墊邊緣提供與塑封料的接合部；

將該襯墊製成具有該邊緣的至少一個第二區段，該第二區段具有懸垂頂部鎖定部輪廓；和

沿著該襯墊的該邊緣交替的第一區段和第二區段。

16.如申請專利範圍第 13 項的方法，其還包括：

將該襯墊製成在每個第一區段與第二區段之間提供第三區段，該第三區段提供間隔。

17.如申請專利範圍第 13 項的方法，其還包括：

將至少一個晶粒固定至該襯墊。

18.如申請專利範圍第 17 項的方法，其還包括：

將該襯墊和該至少一個晶粒包封在塑封料中，其將該第一區段和該第二區段固定至該塑封料。

19.如申請專利範圍第 18 項的方法，其還包括：

將該襯墊的一個或多個第二元件製成具有懸垂頂部鎖定部輪廓，其中該一個或多個第二元件係藉由該懸垂頂部鎖定部輪廓固定至該塑封料。

20.如申請專利範圍第 15 項的方法，其還包括蝕刻該引線框架以製作該第一區段的該突出底部鎖定部和該第二區段的該延長突出底部鎖定部輪廓。

21.如申請專利範圍第 15 項的方法，其還包括衝壓該引

線框架以製作該第一區段的該突出底部鎖定部和該第二區段的該延長突出底部鎖定部輪廓。

22.一種系統，其包括：

電源；

控制器，其具有包括安裝至引線框架的至少一個晶粒的晶片封裝，其中該引線框架的至少第一部分具有包括至少一個突出底部鎖定部輪廓的鎖定部；和

構件，其接收該控制器的輸出。

23.如申請專利範圍第22項的系統，其中該鎖定部進一步包括該引線框架的第二部分，該第二部分包括延長邊緣突出底部鎖定部輪廓。

24.如申請專利範圍第22項的系統，其中該鎖定部進一步包括該引線框架的第二部分，該第二部分包括懸垂頂部鎖定部輪廓。

25.如申請專利範圍第24項的系統，其中該鎖定部是不連續懸垂頂部鎖定部。

26.如申請專利範圍第24項的系統，其中該鎖定部另外包括第三部分，該第三部分包括介於該懸垂頂部鎖定部輪廓與該突出底部鎖定部輪廓之間的間隔區段。

27.如申請專利範圍第22項的系統，其中控制器接收來自該構件的反饋信號，該晶片封裝利用該構件以控制該控制器的輸出。

28.如申請專利範圍第 22 項的系統，該晶片封裝還包括：

塑封料，其包封該引線框架和該至少一個晶粒；

其中該引線框架係藉由該鎖定部固定至該塑封料。

29.如申請專利範圍第28項的系統，該晶片封裝另外包括具有懸垂頂部鎖定部輪廓的一個或多個第二元件，其中該一個或多個第二元件係藉由該懸垂頂部鎖定部輪廓固定至該塑封料。

八、圖式：

(如次頁)

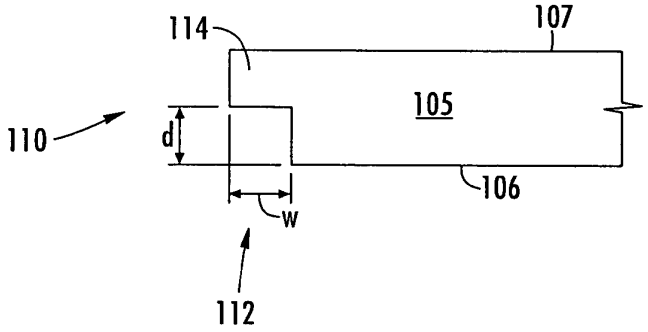


圖1A

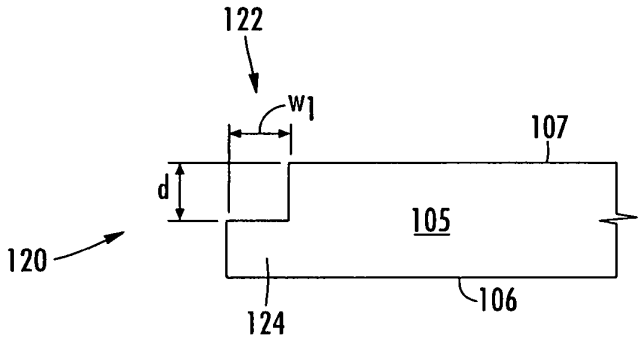


圖1B

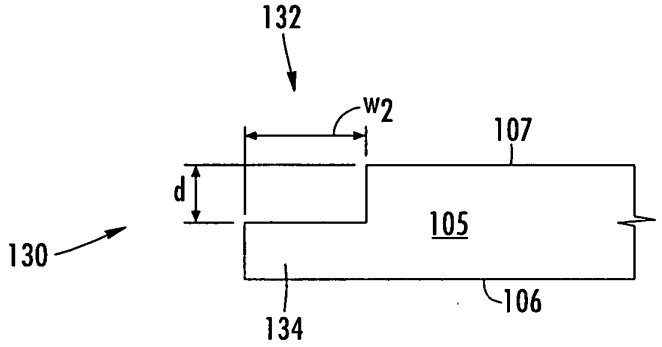


圖1C

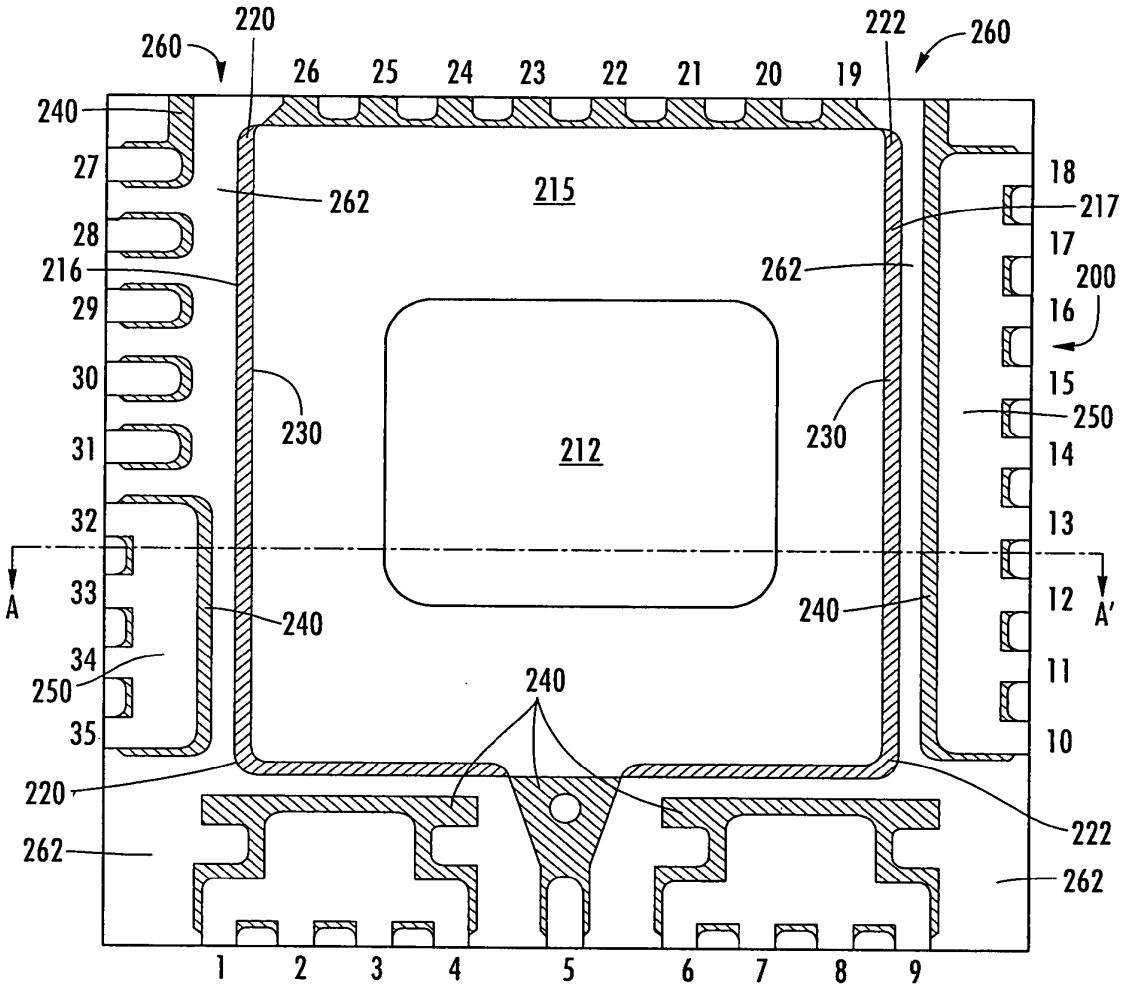

220
222
260
260
26
25
24
23
22
21
20
19
240
27
262
215
18
217
28
17
216
262
200
29
16
30
230
230
15
250
31
212
14
32
13
A
A'
33
240
240
12
34
250
240
11
35
10
220
222
262
262
1
2
3
4
5
6
7
8
9

圖2A

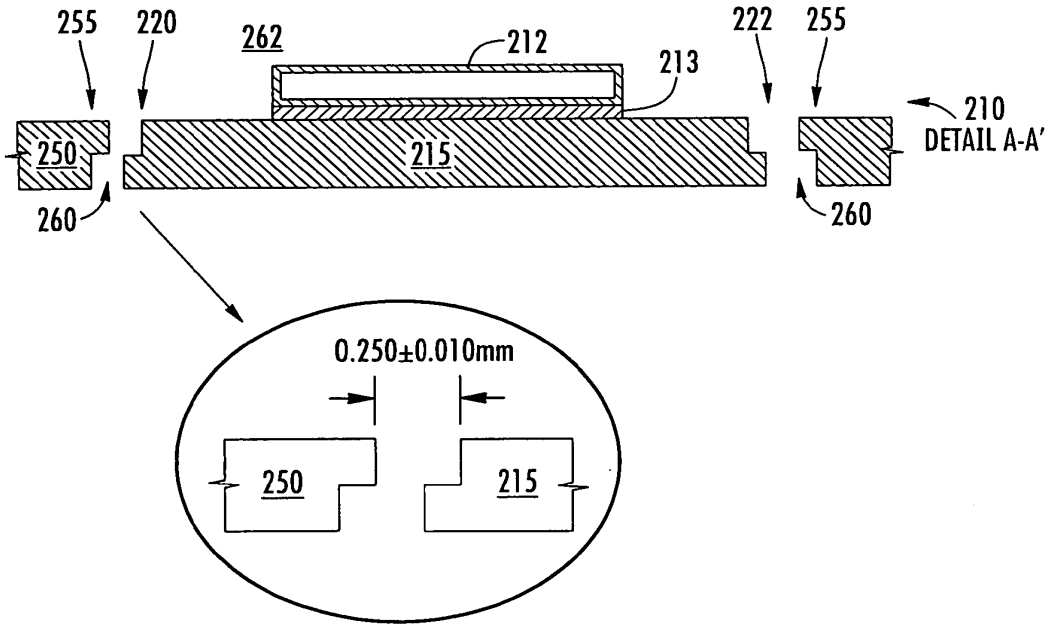

255
220
262
212
213
222
255
210
DETAIL A-A'
250
215
260
260
0.250±0.010mm
250
215

圖2B

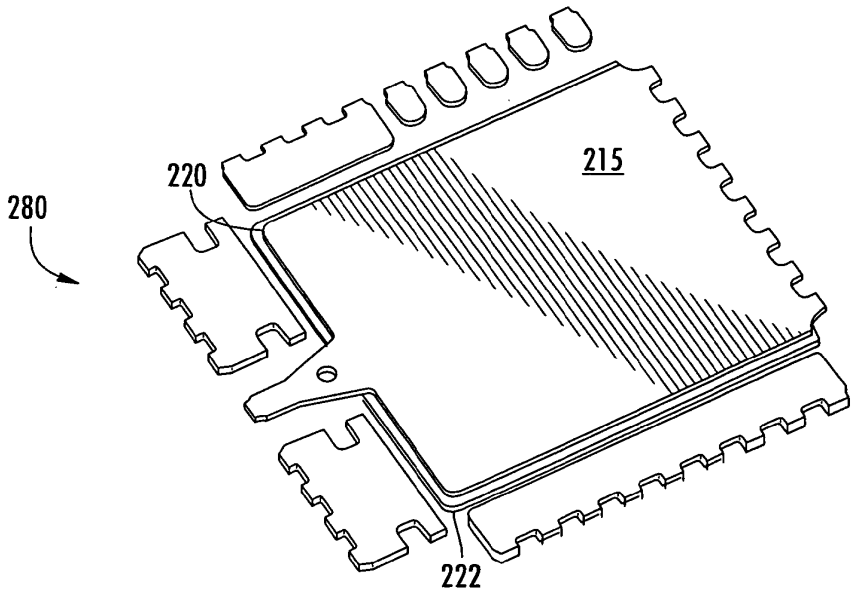


圖2C

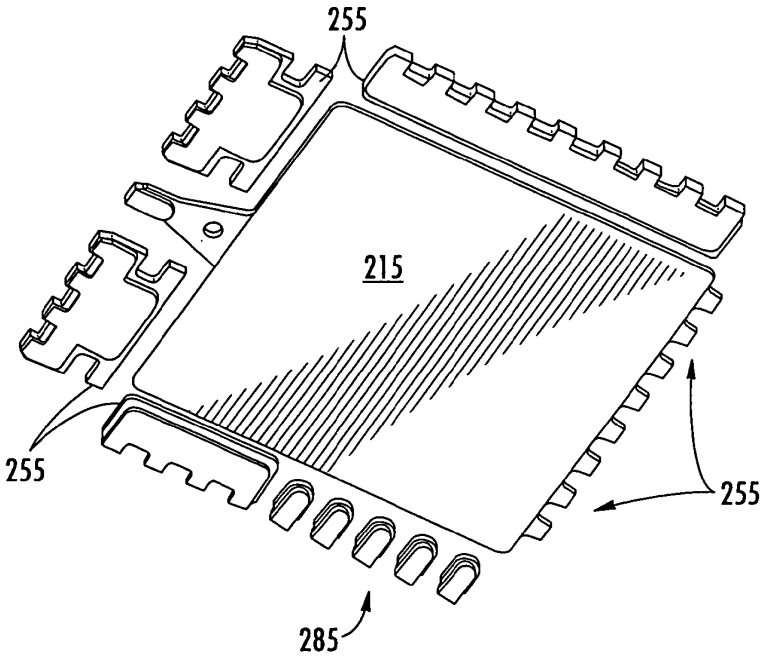


圖 2D

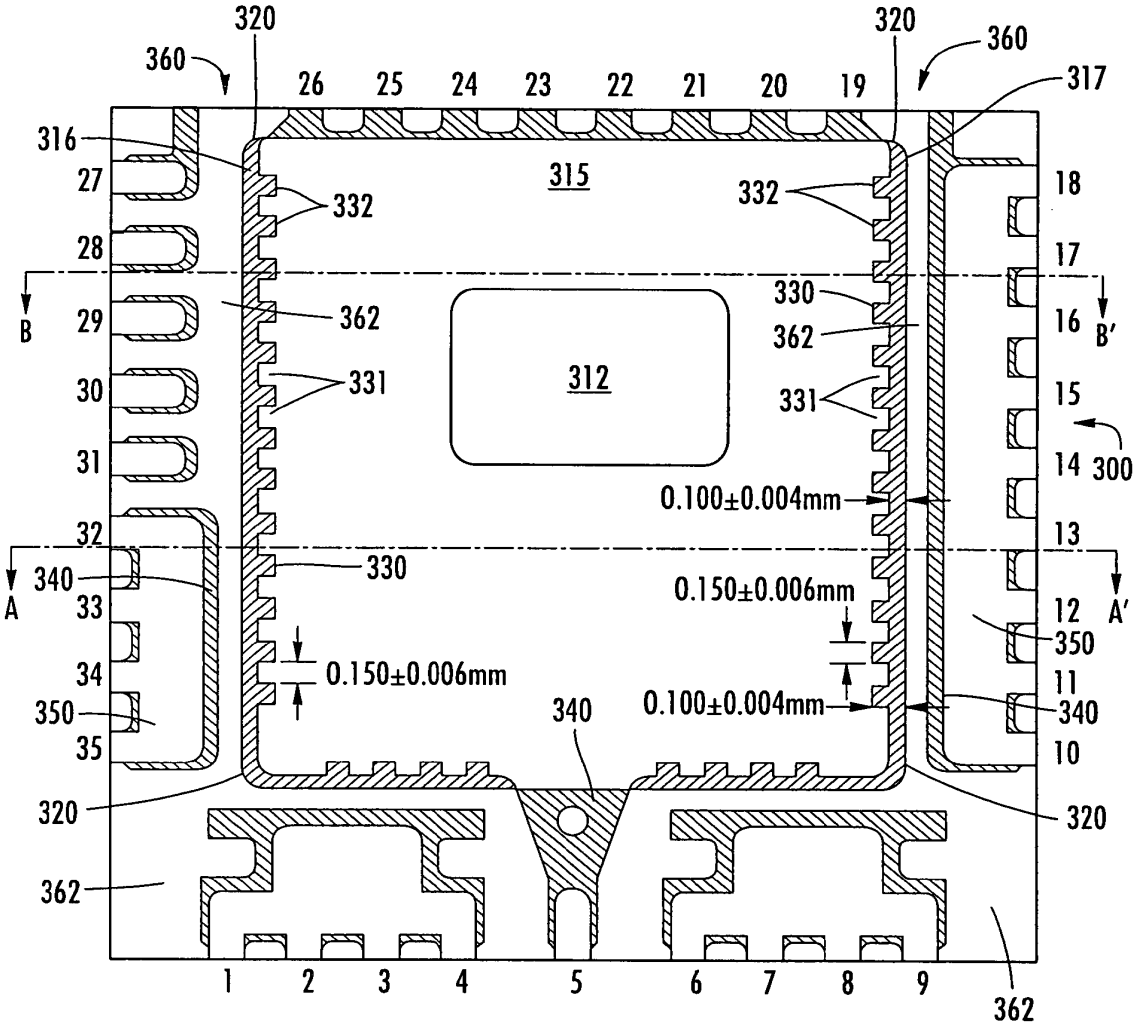

320
360
26
25
24
23
22
21
20
19
320
360
317
316
27
315
332
332
18
28
17
B
29
362
330
362
16
B'
312
331
331
30
15
31
14
300
0.100±0.004mm
32
13
A
340
330
0.150±0.006mm
33
12
A'
350
34
0.150±0.006mm
0.100±0.004mm
11
350
340
340
35
10
320
320
362
1
2
3
4
5
6
7
8
9
362

圖3A

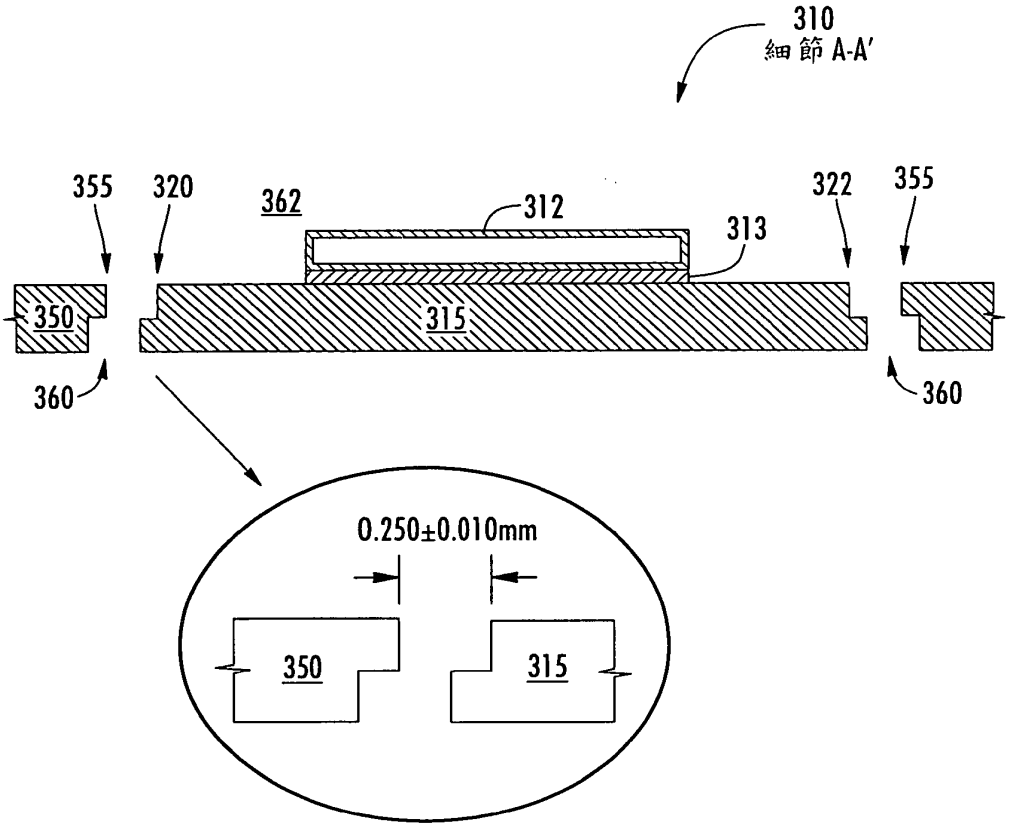

310
細節 A-A'
355
320
362
312
313
322
355
350
315
360
360
0.250±0.010mm
350
315

圖 3B

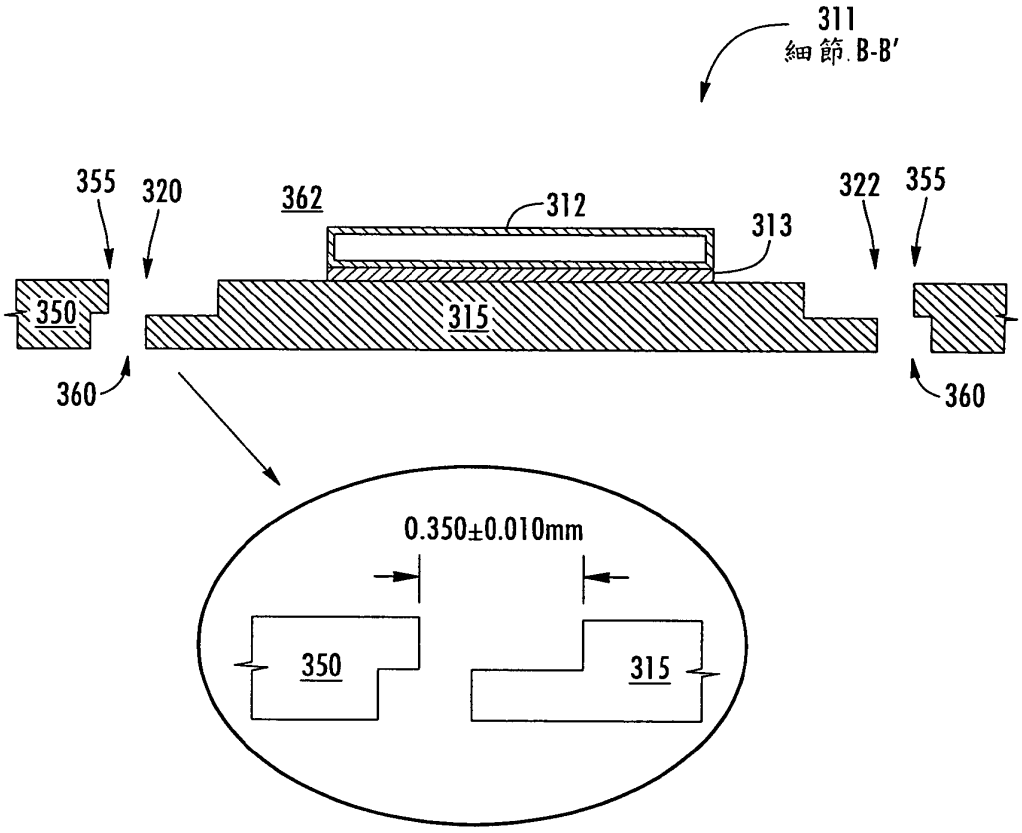

311
細節 B-B'
355
320
362
312
313
322
355
350
315
360
360
0.350±0.010mm
350
315

圖3C

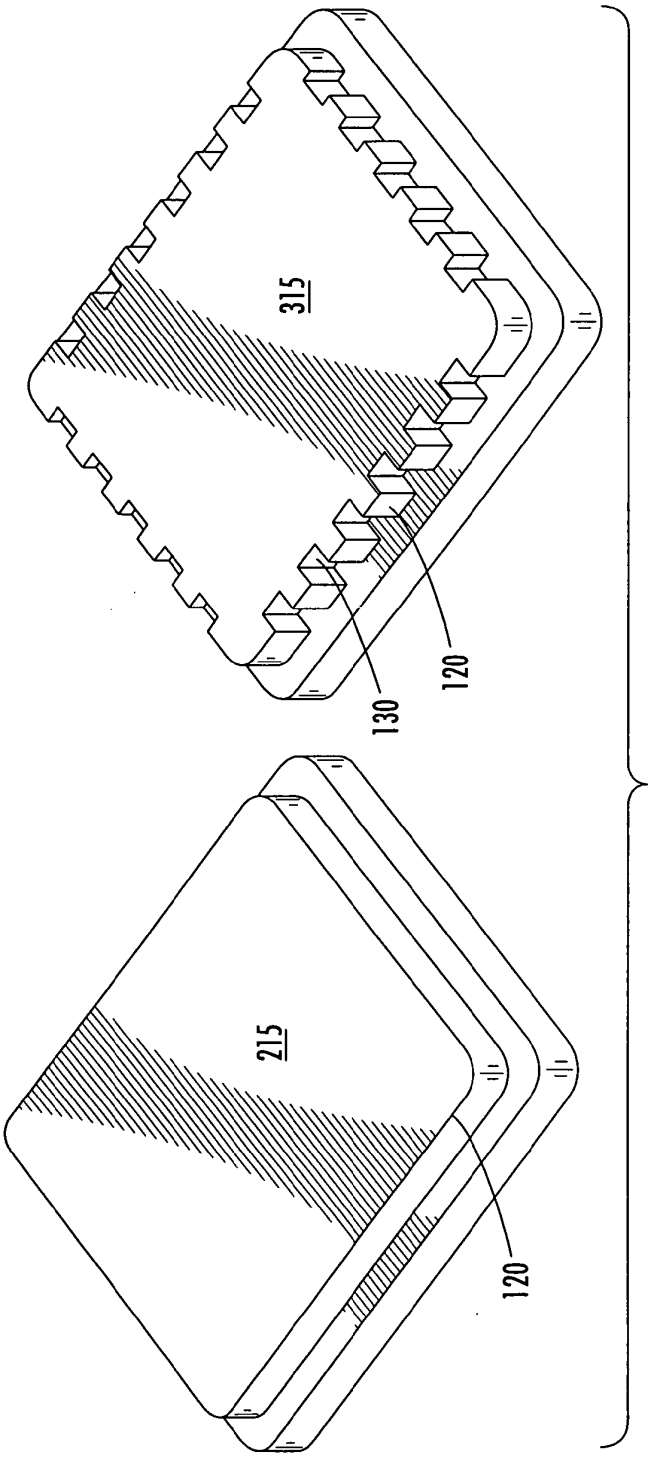


圖3D

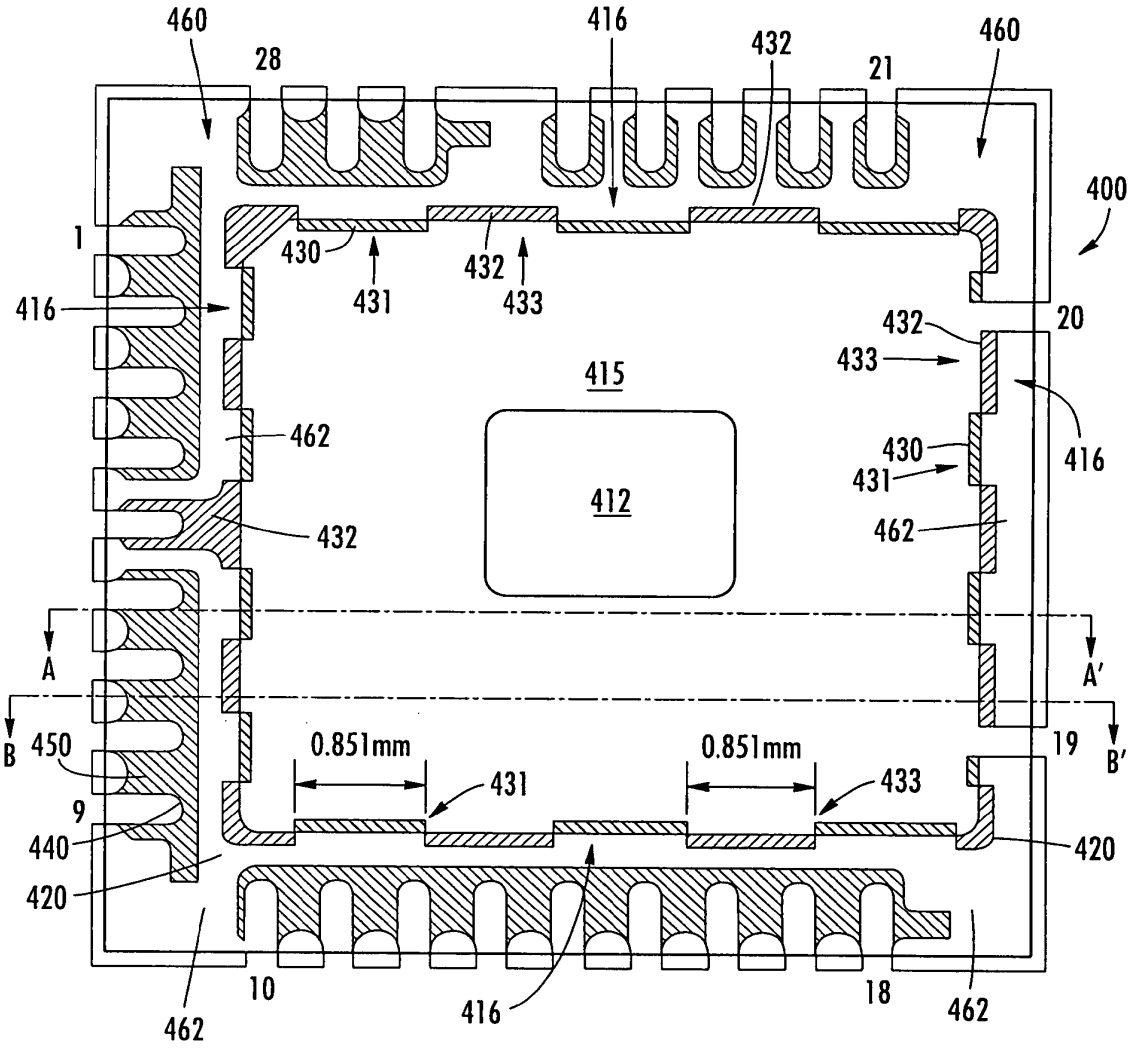

460
28
416
432
21
460
400
1
430
431
432
433
416
20
432
433
415
462
412
430
431
416
462
432
A
A'
B
450
0.851mm
0.851mm
19
B'
431
433
9
440
420
420
10
416
18
462
462

圖4A

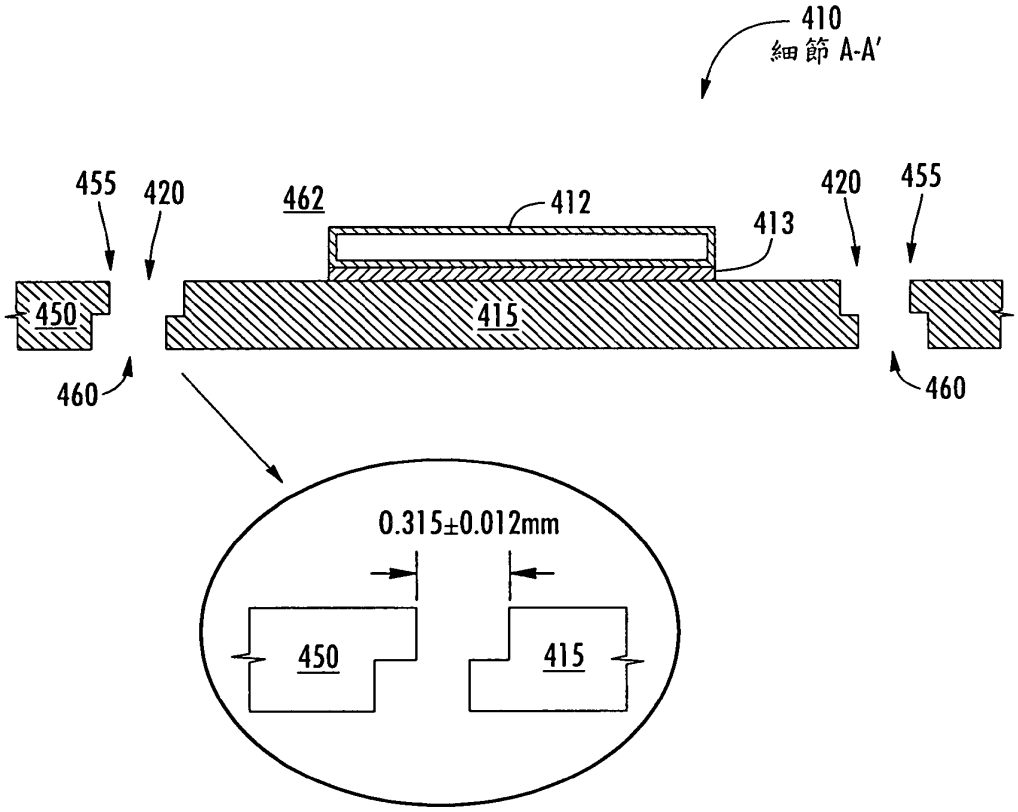

410
細節 A-A'
455
420
462
412
413
420
455
450
415
460
460
0.315±0.012mm
450
415

圖4B

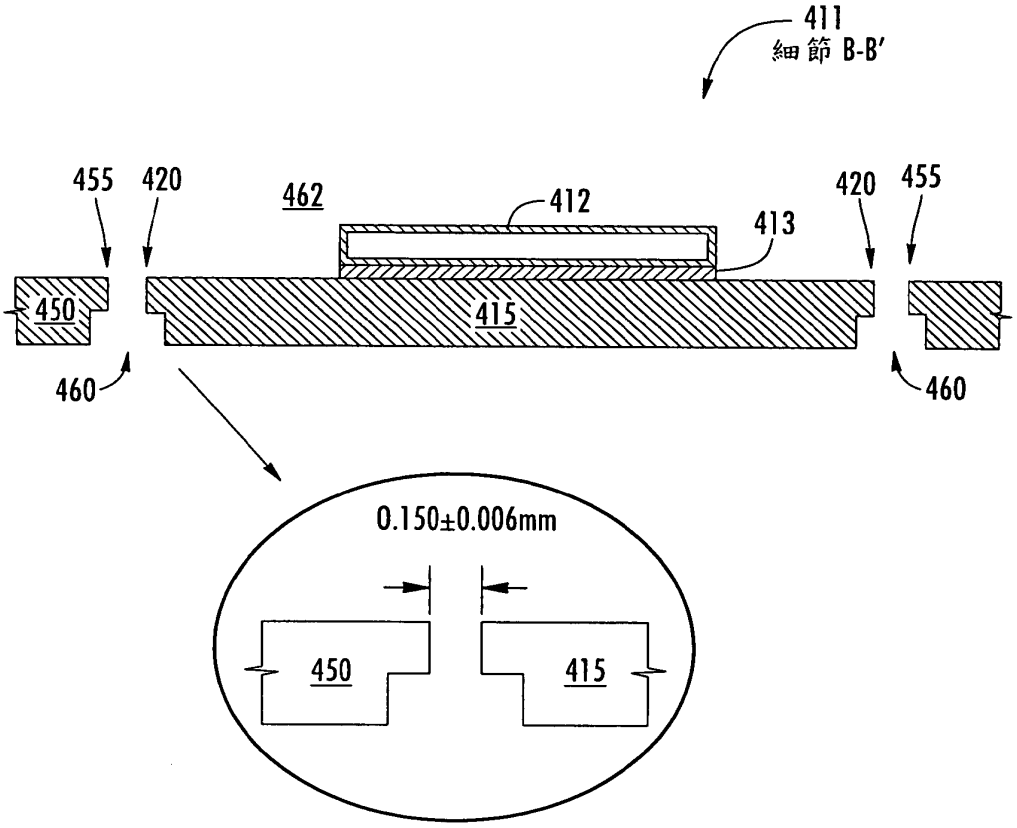

411
細節 B-B'
455
420
462
412
413
420
455
450
415
460
460
0.150±0.006mm
450
415

圖4C

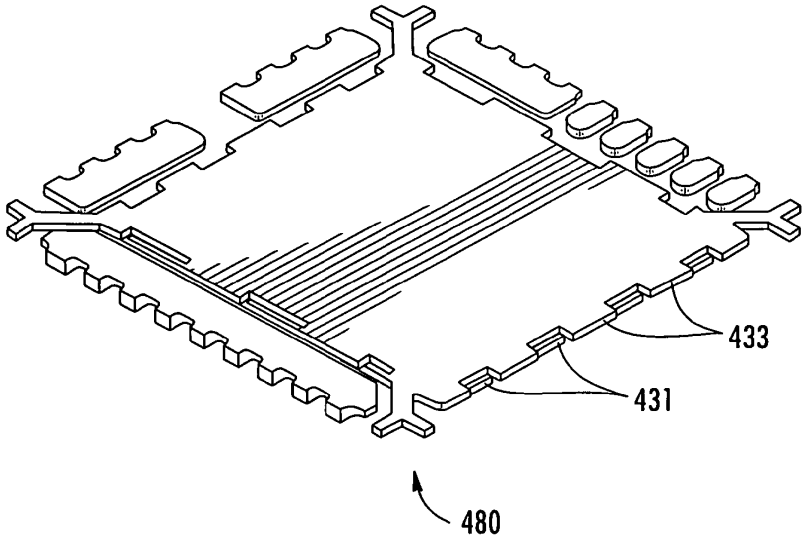


圖4D

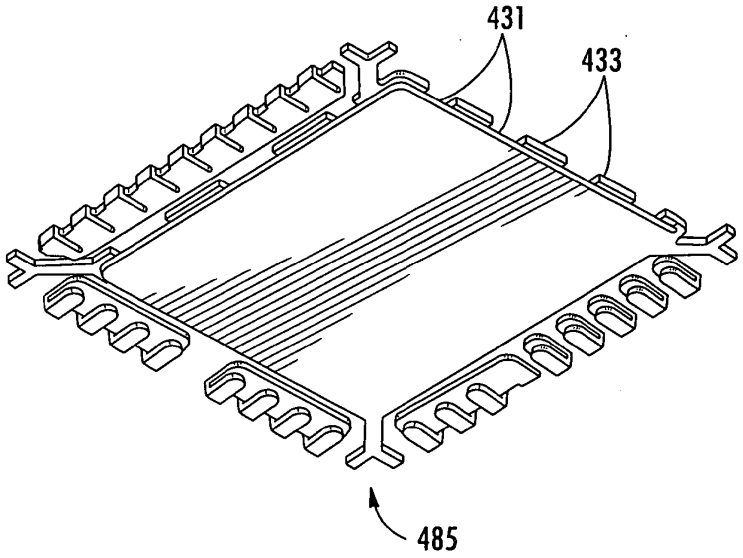


圖4E

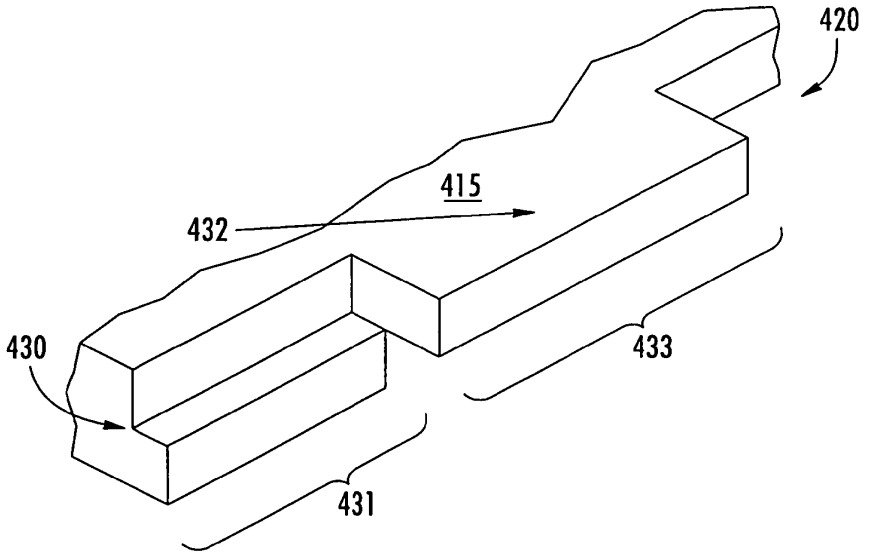


圖4F

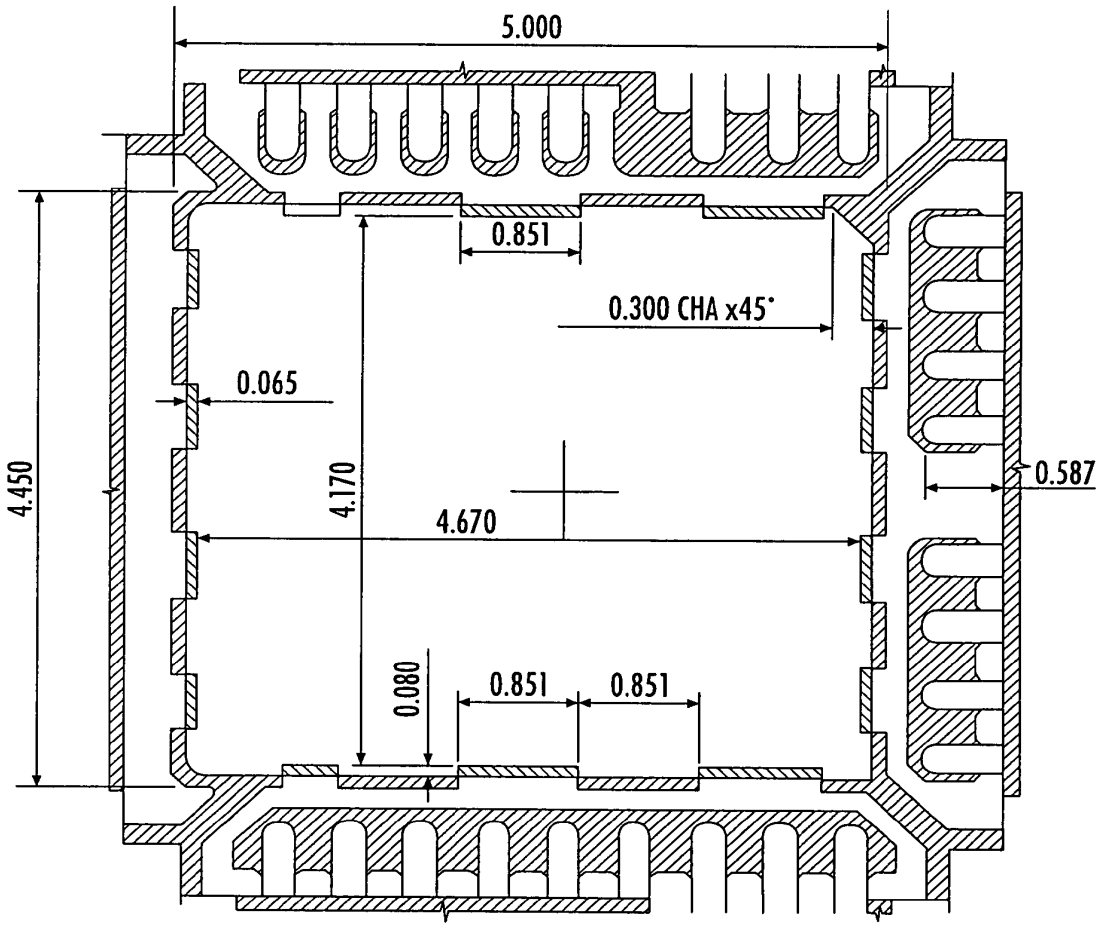

5.000
0.851
0.300 CHA x45°
0.065
4.450
4.170
4.670
0.587
0.080
0.851
0.851

圖4G

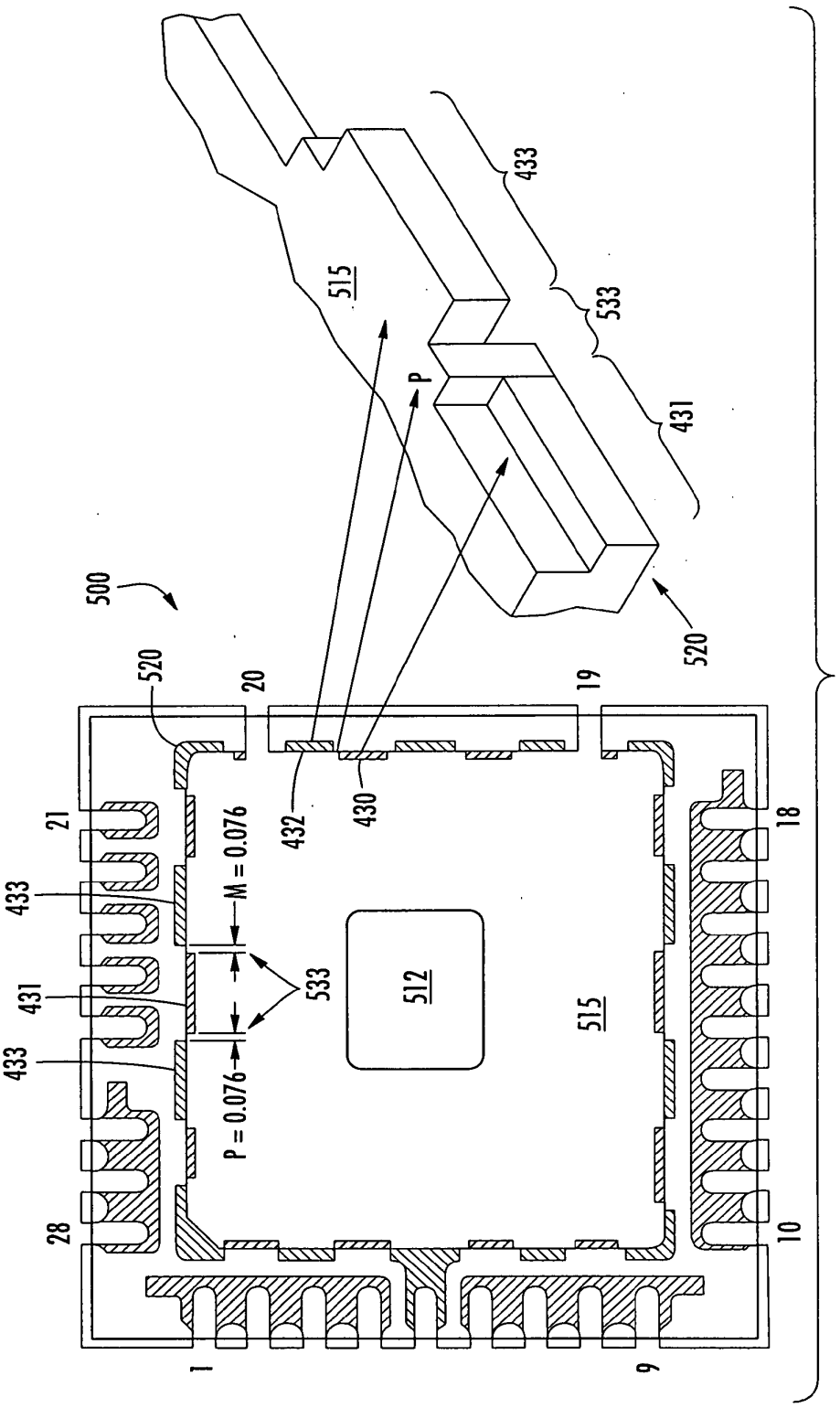

500
520
20
19
515
433
533
431
P
520
432
430
21
18
433
M = 0.076
431
533
512
515
433
P = 0.076
28
10
1
9

圖5

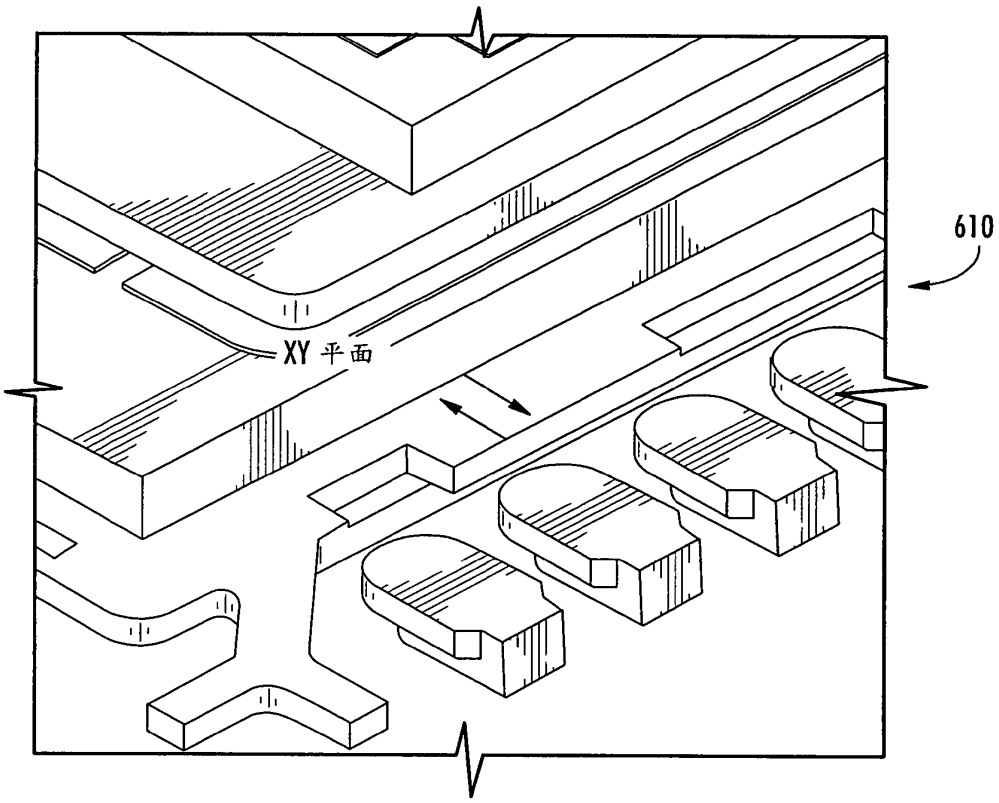


圖6A

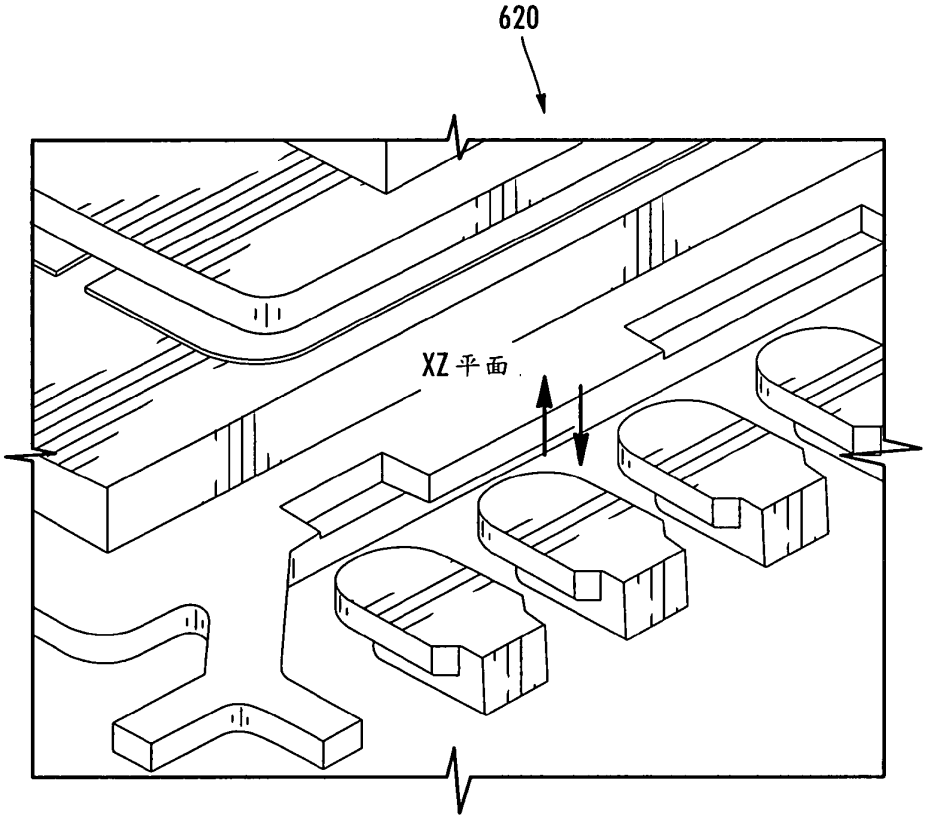


圖6B

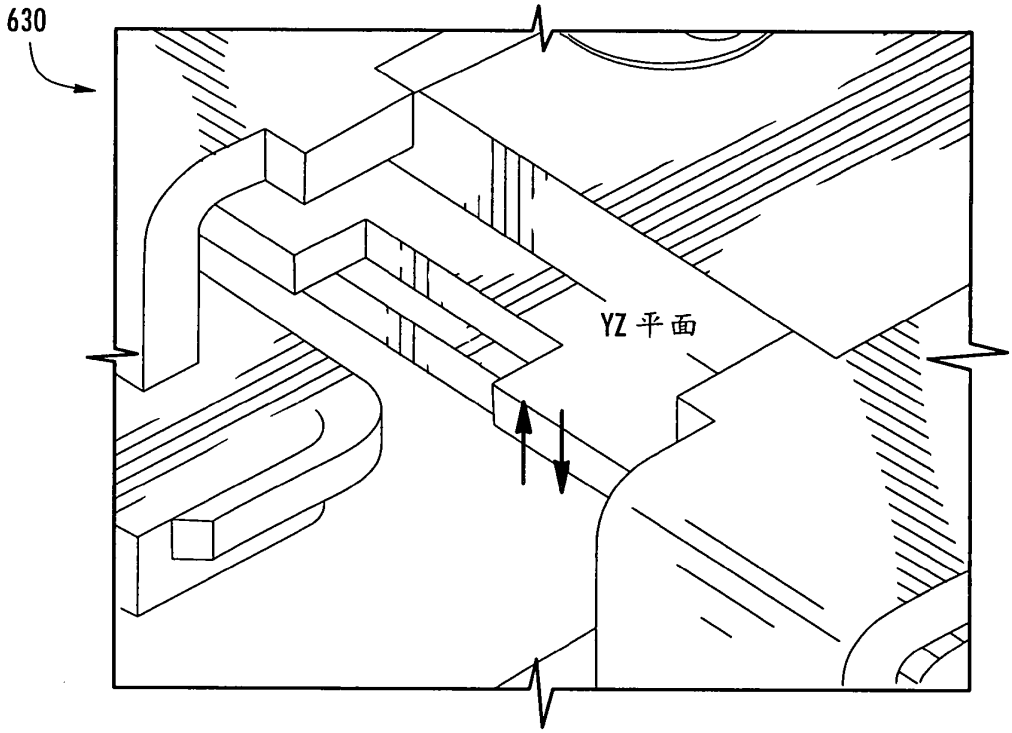


圖6C

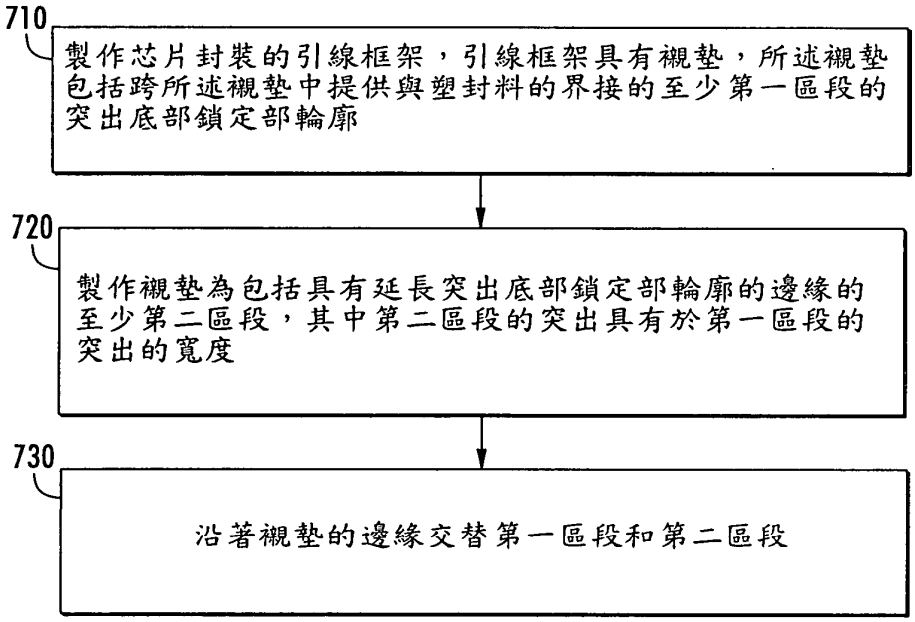

710
製作芯片封裝的引線框架，引線框架具有襯墊，所述襯墊包括跨所述襯墊中提供與塑封料的界接的至少第一區段的突出底部鎖定部輪廓
720
製作襯墊為包括具有延長突出底部鎖定部輪廓的邊緣的至少第二區段，其中第二區段的突出具有於第一區段的突出的寬度
730
沿著襯墊的邊緣交替第一區段和第二區段

圖7

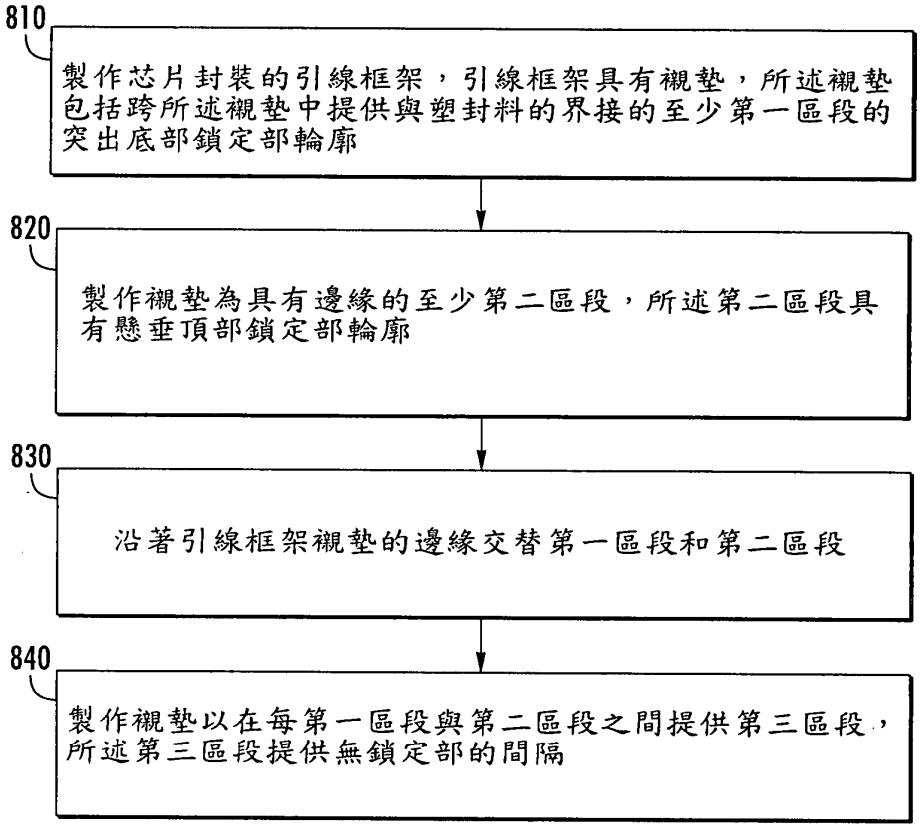

810
製作芯片封裝的引線框架，引線框架具有襯墊，所述襯墊包括跨所述襯墊中提供與塑封料的界接的至少第一區段的突出底部鎖定部輪廓
820
製作襯墊為具有邊緣的至少第二區段，所述第二區段具有懸垂頂部鎖定部輪廓
830
沿著引線框架襯墊的邊緣交替第一區段和第二區段
840
製作襯墊以在每第一區段與第二區段之間提供第三區段，所述第三區段提供無鎖定部的間隔

圖8

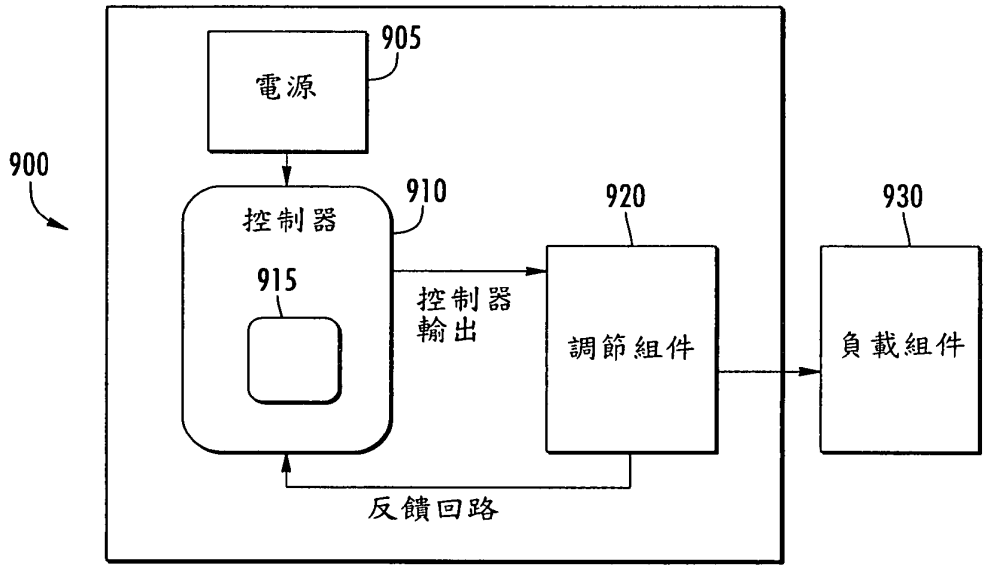


圖9

I011320

102 年 1 月 17 日修正替換頁

四、指定代表圖：

(一)本案指定代表圖為：圖 2C 。

(二)本代表圖之元件符號簡單說明:

215 襯墊

220 線型突出底部鎖定部

280 襯墊俯視圖

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

無

六、發明說明：

相關申請的交叉參考

本申請要求 2011 年 10 月 20 日申請的名爲“SYSTEMS AND METHODS FOR LEAD FRAME LOCKING DESIGN FEATURES”的美國臨時申請 61/549,523 的權益和優先權，該申請以引用的方式並入本文。

技術領域

本發明涉及防止晶片封裝分層和斷裂的系統和方法。

發明背景

安裝好的晶片封裝遭受可能導致晶片封裝分層或斷裂的應力。例如，晶片封裝遭受由來自周圍環境和/或元件熱迴圈、高電負載、高溫熱環境、晶片封裝安裝期間所施加的衝擊負載或類似因素的熱應力導致的應力。應力可能導致剪力和撓曲應力的積累，其易於在晶片封裝錨固至在晶片封裝內包封一個或多個晶粒和引線框架的塑封料處形成。剪應力和撓曲應力的積累會導致晶片封裝分層或斷裂。

發明概要

提供引線框架鎖定設計部的系統和方法。在一個實施方案中，方法包括：製作晶片封裝的引線框架，該引線框架具有包括跨提供與塑封料的介面的襯墊的邊緣的至少第一區段的突出底部鎖定部輪廓的襯墊；蝕刻襯墊爲具有邊緣的至少第二區段，該第二區段具有延長突出底部鎖定部輪廓或懸垂頂部鎖定部輪廓；和沿著襯墊的邊緣交替第一區段和第二區段。

在結合優選實施方案的描述和附圖考慮時可以更容易理解本發明的實施方案以及更易於明白其其他優點和用途，其中：

圖 1A 至圖 1C 是圖示本發明的一個或多個實施方案中所使用的表面破裂鎖定部的不同外形的剖面圖；

圖 2A 至圖 2D 是圖示本發明的一個或多個實施方案的表面破裂鎖定部的圖；

圖 3A 至圖 3D 是圖示本發明的一個或多個實施方案的表面破裂鎖定部的圖；

圖 4A 至圖 4G 是圖示本發明的一個或多個實施方案的表面破裂鎖定部的圖；

圖 5 是圖示圖 4A 至圖 4D 所展示的實施方案的變動的圖；

圖 6A 至圖 6C 是圖示具有多個尺寸的表面破裂鎖定部的一個實施方案的實施例的圖；

圖 7 和圖 8 圖示了本發明的一個或多個實施方案的方法；和

圖 9 圖示了本發明的一個實施方案的系統。

根據慣例，不同的該部件未按比例繪製而是被繪製來強調與本發明相關的部件。在附圖和正文各處，參考符號表示相同元件。

圖中主要元件的參考符號列表

105　襯墊

106　表面

107 表面

110 懸垂頂部鎖定部輪廓

112 部分蝕刻

114 懸垂

120 突出底部鎖定部輪廓

122 部分蝕刻

124 突出

130 延長邊緣突出底部鎖定輪廓

132 部分蝕刻

134 突出

200 晶片封裝

210 橫截面圖

212 晶粒

213 晶粒附著材料

215 襯墊

216 邊緣

217 邊緣

220 線型突出底部鎖定部

222 線型突出底部鎖定部

230 頂部部分蝕刻

240 底部部分蝕刻

250 第二元件

255 懸垂頂部鎖定部

260 體積

262 塑封料

280 襯墊俯視圖

285 襯墊仰視圖

300 晶片封裝

310 橫截面圖

311 橫截面圖

312 晶粒

313 晶粒附著材料

315 襯墊

316 邊緣

317 邊緣

320 不連續突出底部鎖定部

322 不連續突出底部鎖定部

331 交替表面破裂區段

332 交替表面破裂區段

340 底部部分蝕刻

350 第二元件

355 懸垂頂部鎖定部

360 體積

362 塑封料

400 晶片封裝

410 橫截面圖

411 橫截面圖

412 晶粒

413 晶粒附著材料

415 襯墊

416 邊緣

420 不連續懸垂頂部鎖定部

430 頂部部分蝕刻

431 交替表面破裂區段

432 底部部分蝕刻

433 交替表面破裂區段

440 底部部分蝕刻

450 第二元件

455 懸垂頂部鎖定部

460 體積

462 塑封料

480 襯墊俯視圖

485 襯墊仰視圖

500 晶片封裝

512 晶粒

515 襯墊

520 不連續懸垂頂部鎖定部

533 間隔

610 交替區段

611 輪廓

615 襯墊

620 交替區段

630 交替區段

710 製作晶片封裝的引線框架

720 將襯墊製作成包括具有延長突出底部鎖定部輪廓的邊緣的至少第二區段

730 鎖定部

810 製作晶片封裝的引線框架

820 將襯墊製作成具有邊緣的至少第二區段，該第二區段具有懸垂頂部鎖定部

830 鎖定部

840 在每個第一區段與第二表面破裂區段之間提供第三區段，該第三區段提供無鎖定部的間隔

900 系統

905 電源

910 控制器

915 晶片封裝

920 調節元件

930 負載元件

七、申請專利範圍：

1.一種晶片封裝，其包括：

引線框架，其具有襯墊；

其中該引線框架的至少第一部分具有包括突出底部鎖定部輪廓的鎖定部；和

塑封料，其包封該引線框架和該至少一個晶粒；

其中該引線框架藉由該鎖定部固定至該塑封料。

2.如申請專利範圍第 1 項之晶片封裝，其進一步包括安裝至該襯墊的至少一個晶粒。

3.如申請專利範圍第 1 項之晶片封裝，其中該鎖定部進一步包括該引線框架的第二部分，該第二部分包括延長邊緣突出底部鎖定部輪廓。

4.如申請專利範圍第 3 項之晶片封裝，其中該鎖定部包括不連續突出底部鎖定部。

5.如申請專利範圍第 1 項之晶片封裝，其中該鎖定部進一步包括該引線框架的第二部分，該第二部分包括懸垂頂部鎖定部輪廓。

6.如申請專利範圍第 5 項之晶片封裝，其中該鎖定部是不連續懸垂頂部鎖定部。

7.如申請專利範圍第 5 項之晶片封裝，其中該鎖定部另外包括第三部分，該第三部分包括在該懸垂頂部鎖定部輪廓與該突出底部鎖定部輪廓之間的間隔區段。

8.如申請專利範圍第 5 項之晶片封裝，其還包括具有懸垂頂部鎖定部輪廓的一個或多個第二元件，其中該一個或

多個第二元件係藉由該懸垂頂部鎖定部輪廓固定至該塑封料。

9.一種方法，其包括：

製作用於晶片封裝的引線框架，該引線框架具有襯墊，該襯墊包括突出底部鎖定部輪廓，其橫越該襯墊邊緣的至少第一區段，該襯墊邊緣提供與塑封料的接合部的；

將該襯墊製成包括該邊緣的至少第二區段，該第二區段具有延長突出底部鎖定部輪廓，其中該第二區段的突出具有大於該第一區段的突出的寬度；和

沿著該襯墊的該邊緣交替的第一區段和第二區段。

10.如申請專利範圍第 9 項的方法，其還包括：

將至少一個晶粒固定至該襯墊。

11.如申請專利範圍第 10 項該的方法，其還包括：

將該襯墊和該至少一個晶粒包封在塑封料中，其將該第一區段和該第二區段固定至該塑封料。

12.如申請專利範圍第 11 項的方法，其還包括：

將該襯墊的一個或多個第二元件製成具有懸垂頂部鎖定部輪廓，其中該一個或多個第二元件係藉由該懸垂頂部鎖定部輪廓固定至該塑封料。

13.如申請專利範圍第 9 項的方法，其還包括蝕刻該引線框架以製作該第一區段的該突出底部鎖定部和該第二區段的該延長突出底部鎖定部輪廓。

14.如申請專利範圍第 9 項的方法，其還包括衝壓該引線框架以製作該第一區段的該突出底部鎖定部和該第二區

段的該延長突出底部鎖定部輪廓。

15.一種方法，其包括：

製作用於晶片封裝的引線框架，該引線框架具有襯墊，該襯墊包括突出底部鎖定部輪廓，其橫越該襯墊邊緣的至少第一區段，該襯墊邊緣提供與塑封料的接合部；

將該襯墊製成具有該邊緣的至少一個第二區段，該第二區段具有懸垂頂部鎖定部輪廓；和

沿著該襯墊的該邊緣交替的第一區段和第二區段。

16.如申請專利範圍第 13 項的方法，其還包括：

將該襯墊製成在每個第一區段與第二區段之間提供第三區段，該第三區段提供間隔。

17.如申請專利範圍第 13 項的方法，其還包括：

將至少一個晶粒固定至該襯墊。

18.如申請專利範圍第 17 項的方法，其還包括：

將該襯墊和該至少一個晶粒包封在塑封料中，其將該第一區段和該第二區段固定至該塑封料。

19.如申請專利範圍第 18 項的方法，其還包括：

將該襯墊的一個或多個第二元件製成具有懸垂頂部鎖定部輪廓，其中該一個或多個第二元件係藉由該懸垂頂部鎖定部輪廓固定至該塑封料。

20.如申請專利範圍第 15 項的方法，其還包括蝕刻該引線框架以製作該第一區段的該突出底部鎖定部和該第二區段的該延長突出底部鎖定部輪廓。

21.如申請專利範圍第 15 項的方法，其還包括衝壓該引

線框架以製作該第一區段的該突出底部鎖定部和該第二區段的該延長突出底部鎖定部輪廓。

22.一種系統，其包括：

電源；

控制器，其具有包括安裝至引線框架的至少一個晶粒的晶片封裝，其中該引線框架的至少第一部分具有包括至少一個突出底部鎖定部輪廓的鎖定部；和

構件，其接收該控制器的輸出。

23.如申請專利範圍第22項的系統，其中該鎖定部進一步包括該引線框架的第二部分，該第二部分包括延長邊緣突出底部鎖定部輪廓。

24.如申請專利範圍第22項的系統，其中該鎖定部進一步包括該引線框架的第二部分，該第二部分包括懸垂頂部鎖定部輪廓。

25.如申請專利範圍第24項的系統，其中該鎖定部是不連續懸垂頂部鎖定部。

26.如申請專利範圍第24項的系統，其中該鎖定部另外包括第三部分，該第三部分包括介於該懸垂頂部鎖定部輪廓與該突出底部鎖定部輪廓之間的間隔區段。

27.如申請專利範圍第22項的系統，其中控制器接收來自該構件的反饋信號，該晶片封裝利用該構件以控制該控制器的輸出。

28.如申請專利範圍第 22 項的系統，該晶片封裝還包括：

塑封料，其包封該引線框架和該至少一個晶粒；

其中該引線框架係藉由該鎖定部固定至該塑封料。

29.如申請專利範圍第28項的系統，該晶片封裝另外包括具有懸垂頂部鎖定部輪廓的一個或多個第二元件，其中該一個或多個第二元件係藉由該懸垂頂部鎖定部輪廓固定至該塑封料。

八、圖式：

(如次頁)

Espacenet

Bibliographic data: TWI242820 (B) — 2005-11-01

Sensor semiconductor device and method for fabricating the same

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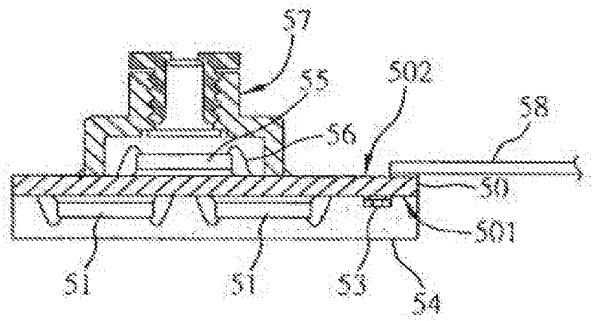
Classification: - international: ***H01L21/56; H01L25/16; H01L27/146;*** (IPC1-7): H01L21/56
- cooperative: **H01L24/97**; **H01L25/167**; **H01L27/14618**; **H01L27/14683**; H01L2224/32225; H01L2224/48247; H01L2224/73265; H01L27/14625; H01L2924/181 more

Application number: TW20050109707 20050329

Priority number(s): TW20050109707 20050329

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Abstract of TWI242820 (B)



A sensor semiconductor device and a method for fabricating the same are proposed, wherein a chip carrier module plate composed of a plurality of chip carrier units having a first surface and corresponding second surface are provided, for setting and electrically connecting at least a chip on the first surface of the chip carrier unit. A molding compound is formed on the first surface of the chip carrier units for covering entirely the chip and the first surface of the chip carrier units. A sensor chip and a flexible print circuit are mounted and electrically connected on the second surface of the chip carrier unit, and an optical lid is mounted on the second surface of the chip carrier unit corresponding to the sensor chip, so as to fabricate a optical module structure with a step-reduced, low-cost, and

I242820

公告本

發明專利說明書

（本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫）

※ 申請案號：94109707

※ 申請日期：94.3.29　　※IPC 分類：H01L 21/56

一、發明名稱：（中文/英文）

感測式半導體裝置及其製法

SENSOR SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

二、申請人：（共 1 人）

姓名或名稱：（中文/英文）

矽品精密工業股份有限公司

SILICONWARE PRECISION INDUSTRIES CO., LTD.

□ 指定　　為應受送達人

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國　籍：（中文/英文）1.至5. 中華民國/R.O.C.

四、聲明事項：

☐ 主張專利法第二十二條第二項☐第一款或☐第二款規定之事實，其事實發生日期為：　年　月　日。

☐ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號　順序註記】

☐ 有主張專利法第二十七條第一項國際優先權：

☐ 無主張專利法第二十七條第一項國際優先權：

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日、申請案號　順序註記】

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料　【格式請依：寄存機構、日期、號碼　順序註記】

國外生物材料　【格式請依：寄存國家、機構、日期、號碼　順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

五、中文發明摘要：

一種感測式半導體裝置及其製法，主要係提供一陣列式晶片承載件模組片，該晶片承載件模組片係由多數呈陣列方式排列之晶片承載件所構成者，同時，各該晶片承載件具有第一表面及相對第二表面，以供接置至少一晶片於各該晶片承載件第一表面上，並使該晶片電性連接至該晶片承載件，接著形成用以全面包覆各該晶片承載件第一表面及該晶片之封裝膠體，再進行切單作業以形成個別整合半導體晶片之封裝單元，之後於該晶片承載件第二表面接置感測式晶片、對應之透光蓋體與軟式印刷電路板(FPC)，並使該感測式晶片及軟式印刷電路板與該晶片承載件間形成電性連接關係，藉以提供步驟簡化、低成本與高產能之模組化結構。

六、英文發明摘要：

A sensor semiconductor device and a method for fabricating the same are proposed, wherein a chip carrier module plate composed of a plurality of chip carrier units having a first surface and corresponding second surface are provided, for setting and electrically connecting at least a chip on the first surface of the chip carrier unit. A molding compound is formed on the first surface of the chip carrier units for covering entirely the chip and the first surface of the chip carrier units. A sensor chip and a flexible print circuit are mounted and electrically connected on the second surface of the chip carrier unit, and an optical lid is mounted on the second surface of the chip carrier unit corresponding to the sensor chip, so as to fabricate a optical module structure with a step-reduced, low-cost, and high-produced method.

七、指定代表圖：

(一)本案指定代表圖為：第（ 5E ）圖。

(二)本代表圖之元件代表符號簡單說明：

50	基板單元
501	第一表面
502	第二表面
51	半導體晶片
53	被動元件
54	封裝膠體
55	感測式晶片
56	銲線
57	透光蓋體
58	軟式印刷電路板

八、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

本案無化學式。

九、發明說明：

【發明所屬之技術領域】

本發明係有關一種感測式半導體裝置及其製法，尤指一種整合感測式晶片之半導體封裝結構及其製作方法。

【先前技術】

傳統之影像感測式封裝件(Image sensor package)係如第 1 圖所示之美國第 6,696,752 號所揭示者，其主要係將感測式晶片(Sensor chip)10 接置一預先模壓之具凹部之導線架 11 上，並透過銲線 12 加以電性連接該感測式晶片 10 及導線架 11 後，於該感測式晶片 10 上方封蓋住一玻璃 13，以供影像光線能為該感測式晶片 10 所截取。如此，該完成構裝之影像感測式封裝件即可供系統廠進行整合至如印刷電路板(PCB)等外部裝置上，以供如數位相機(DSC)、數位攝影機(DV)、光學滑鼠、行動電話、指紋辨識器等各式電子產品之應用。

另電子產品之縮小化，已為長久以來的發展趨勢，並且以往單一功能型態的電子產品已無法再滿足消費者的需求，如行動電話結合數位相機之多功能(Multiple function)電子產品等，使得隨身型的電子產品不再僅有單一使用功能。因此，為迎合現今電子產品係朝多功能、高電性及高速運作之方向發展，同時為提供電子產品之輕薄短小化，半導體業者莫不積極研發能整合有複數個晶片之半導體裝置之多晶片模組(Multi Chip Module, MCM)，以符合電子產品之需求。

請參閱第 2 圖所示，係美國專利第 6,661,089 號所揭示之整合型感測式模組化(Sensor module)結構，其係在原先設置有感測式晶片 20 之感測式封裝件內，整合並電性連結有例如數位訊號處理器 DSP(digital signal processor)等感測式晶片之控制單元 24，以求縮小電子產品中感測式模組化結構使用尺寸。

復請參閱第 3 及第 4 圖所示，係美國專利第 6,686,588 號及第 6,384,397 號所揭示之另一種整合型感測式模組化(Sensor module)結構。於該美國專利第 6,686,588 號所揭露之模組化結構中(如第 3 圖所示)，除在基板 31 上表面接置有感測式晶片 30 外，並在基板下表面額外利用表面黏著技術(SMT)以及個別封裝製程，而接置其餘如控制單元等電子元件 34。另該美國專利第 6,384,397 號所揭露之模組化結構(如第 4 圖所示)，主要除係在感測式封裝件 4 上表面設置有光學透鏡 45 外，另可透過銲錫凸塊(solder bump)46 而接置有一軟式電路板(flex circuit)47，以透過該軟式電路板 47 而將電子訊號連接至電子產品上。如此，即可在感測式封裝件中進行其餘電子元件之整合，藉以提供電子產品多功能電性需求。

惟前述之各種感測式模組化(Sensor module)結構中，仍需為容納許多封裝件而佔用模組化結構許多空間，而不利輕薄短小之發展趨勢；再者為完成該些模組化結構，需額外進行多種不同種類之半導體封裝件之製作，同時亦需多次利用表面黏著技術(SMT)以將該些不同類型之半導體

封裝件加以接置於該模組化結構，如此不僅提高製程複雜度，同時亦增加製程成本，且由於該些模組化結構中因需在感測式封裝件中整合多種不同功能之半導體封裝件，而無法有效利用批次方式大量生產製造，故受到種種限制而不利於產業上之應用。

因此，如何提供一種具低成本、簡單製程、具可縮小模組化結構尺寸與高整合度，亦可供批次方式量產之感測式半導體裝置及其製法，實為目前業界亟欲解決的課題。

【發明內容】

鑒於以上所述習知技術之缺點，本發明之主要目的在於提供一種具低成本且具高整合度之感測式半導體裝置及其製法。

本發明之再一目的在於提供一種具簡單製程之感測式半導體裝置及其製法。

本發明之另一目的在於提供一種可縮小構裝尺寸之感測式半導體裝置及其製法。

本發明之又一目的在於提供一種可供批次方式量產之感測式半導體裝置及其製法。

為達上揭及其它目的，本發明之感測式半導體裝置之製法，係包括：提供一陣列式晶片承載件模組片，該晶片承載件模組片係由多數呈陣列方式排列之晶片承載件所構成者，同時，各該晶片承載件具有第一表面及相對之第二表面；接置至少一半導體晶片於該晶片承載件第一表面上，並使該半導體晶片電性連接至該晶片承載件；形成用

以全面包覆各該晶片承載件第一表面及該半導體晶片之封裝膠體；進行切單作業以形成個別整合半導體晶片之封裝單元；以及於該晶片承載件第二表面接置感測式晶片、對應之透光蓋體與軟式印刷電路板(Flexible Print Circuit, FPC)，並使該感測式晶片及軟式印刷電路板與該晶片承載件間形成電性連接關係。其中，該晶片承載件係為基板結構(例如為 LGA(LAND GRID ARRAY)基板)，該晶片承載件第一表面上之半導體晶片係可以覆晶、打線或堆疊等方式加以接置其上，該晶片承載件第二表面上之感測式晶片係可為打線式感測式晶片或為晶片尺寸封裝(Chip Size Package, CSP)型感測式晶片。

另外，本發明之感測式半導體裝置除可採用批次方式大量製造生產外，若實際製程許可，亦可以單顆方式進行。

本發明亦揭露一種感測式半導體裝置，係包括：一具第一表面及相對第二表面之晶片承載件；至少一半導體晶片，係接置並電性連接至該晶片承載件第一表面上；一封裝膠體，係全面完整包覆該半導體晶片及該晶片承載件第一表面；至少一感測式晶片，係接置並電性連接至該晶片承載件第二表面上；以及至少一軟式印刷電路板(FPC)係接置並電性連接至該晶片承載件第二表面上。

另外，可選擇性於該晶片承載件之第一及第二表面上接置被動元件，以提升該感測式半導體裝置之電性功能；再者，於該感測式半導體裝置中亦可包括有一接置於該封裝膠體上之散熱結構，藉以提供該感測式半導體裝置之散

熱效能。

因此，本發明之感測式半導體裝置及其製法主要係將非為感測式晶片之其餘功能性半導體晶片，先行採用批次方式快速、量化地完成封裝，而後再於構成該封裝件之晶片承載件外露部分接置有感測式晶片及軟式印刷電路板(FPC)，以構成高整合度之模組化之感測式半導體裝置，如此，即可採用低成本及簡單製程方法，達成縮小模組化結構尺寸，此外，本發明亦可供批次方式量產結合有感測式晶片與其餘功能性半導體晶片之模組化結構，藉以避免習知之感測式模組化結構中需為額外進行多種不同種類之半導體封裝件之製作，以及需多次利用表面黏著技術(SMT)以將該些不同類型之半導體晶片或封裝件加以接置於該模組化結構中所導致增加製程複雜度及製程成本等問題。

【實施方式】

以下係藉由特定的具體實施例說明本發明之實施方式，熟習此技藝之人士可由本說明書所揭示之內容輕易地瞭解本發明之其他優點與功效。本發明亦可藉由其他不同的具體實施例加以施行或應用，本說明書中的各項細節亦可基於不同觀點與應用，在不悖離本發明之精神下進行各種修飾與變更。

[第一實施例]

請參閱第5A至5E圖，係為本發明之感測式半導體裝置製法第一實施例之剖面示意圖。

如第5A圖所示，首先，係提供一陣列式基板模組片

50A，該基板模組片 50A 包含有複數個基板單元 50 以陣列方式排列所構成者。該基板單元 50 具有一第一表面 501 及相對之第二表面 502，以於該基板模組片 50A 中各基板單元 50 第一表面 501 上接置有半導體晶片 51，並使該半導體晶片 51 得以藉由複數銲線 52 而電性連接至該基板單元 50 第一表面 501，另可視實際電性設計需求而在該基板單元 50 第一表面 501 上接置有被動元件 53。其中基板單元 50 型態係可例如為 LGA (LAND GRID ARRAY)基板，該半導體晶片 51 係可例如為微控制器(MCU)、記憶體單元等功能性半導體晶片。另該基板模組片 50A 除以陣列方式排列外，亦可以直條方式排列，且如製程條件許可亦可採用單顆基板單元方式進行。

如第 5B 圖所示，將該接置有半導體晶片 50 及被動元件 53 之基板模組片 50A 置入封裝模具之模穴(未圖示)中進行模壓作業，以在該基板模組片 50A 上形成一用以全面完整包覆該半導體晶片 51、銲線 52、被動元件 53 及基板單元第一表面 501 之封裝膠體 54。

如第 5C 圖所示，進行切單製程，藉以形成複數整合半導體晶片 51 之封裝單元 500，同時使該基板單元 50 的側面係外露出所形成之封裝膠體 54，並與該封裝膠體 54 之側面切齊。

如第 5D 圖所示，於外露出封裝膠體 54 之該基板單元 50 第二表面 502 上接置感測式晶片(sensor chip)55，並透過銲線 56 以使該感測式晶片 55 電性連接至該基板單元

50。

如第 5E 圖所示，於該基板單元 50 第二表面 502 上對應該感測式晶片 55 位置接置一透光蓋體 57，以供影像光線能為該感測式晶片 55 所截取，藉以形成整合有感測式晶片 55 與功能性半導體晶片 51 之模組化結構，並對應於該基板單元 50 第二表面 502 之電性接點上利用導電材料接置並電性連接有軟式印刷電路板(FPC)58，以供該模組化結構加以透過該軟式印刷電路板 58 而電性連接至外部裝置。

透過前述製程，本發明亦揭露一種感測式半導體裝置(即如第 5E 圖所示)，係包括：一具第一表面 501 及相對第二表面 502 之例如基板單元 50 之晶片承載件；至少一半導體晶片 51，係接置並電性連接至該基板單元 50 第一表面 501 上；一封裝膠體 54，係全面完整包覆於該半導體晶片 51 及該基板單元 50 第一表面 501；至少一感測式晶片 55 與對應透光蓋體 57，係接置於該基板單元 50 第二表面 502 上，且該感測式晶片 55 係與該基板單元 50 相互電性連接；以及至少一軟式印刷電路板(FPC)58 係接置並電性連接至該基板單元 50 第二表面 502 上。

因此，本發明之感測式半導體裝置及其製法主要係將非為感測式晶片之其餘功能性半導體晶片，先行採用批次方式快速、量化地完成封裝，而後再於構成該封裝件之晶片承載件外露部分接置有感測式晶片及軟式印刷電路板(FPC)，以構成高整合度之模組化之感測式半導體裝置，如此，即可採用低成本及簡單製程方法，達成縮小模組化結

構尺寸，此外，本發明亦可供批次方式量產結合有感測式晶片與其餘功能性半導體晶片之模組化結構，藉以避免習知之感測式模組化結構中需為額外進行多種不同種類之半導體封裝件之製作，以及需多次利用表面黏著技術(SMT)以將該些不同類型之半導體晶片或封裝件加以接置於該模組化結構中所導致增加製程複雜度及製程成本等問題。

[第二實施例]

請參閱第6圖所示，係為本發明之感測式半導體裝置第二實施例之剖面示意圖。

本實施例中該感測式半導體裝置係由相似於前述第一實施例之方法而製成者，其不同處在於本實施例中，係可在該基板單元60第二表面602上接置被動元件63，藉以提供該感測式半導體裝置更佳之電性功能。

[第三實施例]

請參閱第7圖所示，係為本發明之感測式半導體裝置第三實施例之剖面示意圖。

本實施例中該感測式半導體裝置係由相似於前述第一實施例之方法而製成者，其不同處在於本實施例中，接置於該基板單元70第二表面702上之感測式晶片75亦可採用晶片尺寸封裝(CSP)技術而加以電性連接至該基板單元70第二表面702，後續再於該基板單元70第二表面702上對應該感測式晶片75位置接置透光性蓋體77，以供影像光線能為該感測式晶片75所截取。

[第四實施例]

請參閱第 8A 及 8B 圖所示，係為本發明之感測式半導體裝置第四實施例之剖面示意圖。

本實施例中該感測式半導體裝置係由相似於前述第一實施例之方法而製成者，其不同處在於本實施例中，接置於該基板單元 80 第一表面 801 上之半導體晶片 81，係可選擇性以覆晶方式電性連接至該基板單元 80 第一表面 801(如第 8A 圖所示)；另外，接置於該基板單元 80 第一表面 801 上之半導體晶片 81 亦可進行堆疊(如第 8B 圖所示)，藉以提升該感測式半導體裝置之電性功能。

[第五實施例]

請參閱第 9A 及 9B 圖所示，係為本發明之感測式半導體裝置第五實施例之剖面示意圖。

本實施例中該感測式半導體裝置係由相似於前述第一實施例之方法而製成者，其不同處在於本實施例中，復可於該感測式半導體裝置上對應該基板單元 90 第一表面 901 之一側之封裝膠體 94 上接置有散熱片 991 或表面呈凹凸狀之散熱結構，藉以提供該感測式半導體裝置較佳之散熱效能。

上述實施例僅例示性說明本發明之原理及其功效，而非用於限制本發明。尤其應特別注意者，係該半導體晶片、感測式晶片與基板之電性連接方式之採用及被動元件、散熱結構之設置等，係可加以選擇變化設計，任何熟習此項技藝之人士均可在不違背本發明之精神及範疇下，對上述實施例進行修飾與改變。因此，本發明之權利保護範圍，

應如後述之申請專利範圍所列。

【圖式簡單說明】

第 1 圖係為美國專利第 6,696,752 號案所揭露之影像感測式封裝件剖面示意圖；

第 2 圖係為美國專利第 6,661,089 號案所揭露之整合型感測式模組化結構剖面示意圖；

第 3 圖係為美國專利第 6,686,588 號案所揭露之整合型感測式模組化結構剖面示意圖；

第 4 圖係為美國專利第 6,384,397 號案所揭露之整合型感測式模組化結構剖面示意圖；

第 5A 至 5E 圖係為本發明之感測式半導體裝置製法第一實施例之剖面示意圖；

第 6 圖係為本發明之感測式半導體裝置第二實施例之剖面示意圖；

第 7 圖係為本發明之感測式半導體裝置第三實施例之剖面示意圖；

第 8A 及 8B 圖係為本發明之感測式半導體裝置第四實施例之剖面示意圖；以及

第 9A 及 9B 圖係為本發明之感測式半導體裝置第五實施例之剖面示意圖。

【主要元件符號說明】

10,20,30	感測式晶片
11	導線架
12	銲線

13	玻璃
24	控制單元
31	基板
34	電子元件
4	感測式封裝件
45	光學透鏡
46	銲錫凸塊
47	軟式電路板
50A	基板模組片
50,60,70,80,90	基板單元
501,801,901	第一表面
502,602,702	第二表面
500	封裝單元
51,81	半導體晶片
52	銲線
53,63	被動元件
54,94	封裝膠體
55,75	感測式晶片
56	銲線
57,77	透光蓋體
58	軟式印刷電路板
901	散熱片
902	散熱結構

十、申請專利範圍：

1. 一種感測式半導體裝置之製法，係包括：

提供一陣列式晶片承載件模組片，該晶片承載件模組片係由多數呈陣列方式排列之晶片承載件所構成者，同時，各該晶片承載件具有一第一表面及一第二表面，以供接置至少一半導體晶片於該晶片承載件之第一表面上，並使該半導體晶片電性連接至該晶片承載件；

形成用以全面包覆各該晶片承載件第一表面及該晶片之封裝膠體；

進行切單作業以形成個別整合半導體晶片之封裝單元；以及

於該晶片承載件第二表面接置感測式晶片、對應之透光蓋體及軟式印刷電路板(FPC)，並使該感測式晶片及該軟式印刷電路板與該晶片承載件形成電性連接關係。

2. 如申請專利範圍第1項之感測式半導體裝置製法，其中，該晶片承載件係為基板，且其型態係採用矩陣式排列及條狀排列之其中一者。

3. 如申請專利範圍第1項之感測式半導體裝置製法，其中，該半導體晶片係以銲線及覆晶方式之其中一者而電性連接至該晶片承載件。

4. 如申請專利範圍第1項之感測式半導體裝置製法，其中，該晶片承載件第一及第二表面上係可選擇性設置被動元件。

5. 如申請專利範圍第1項之感測式半導體裝置製法，其中，該晶片承載件係為LGA (LAND GRID ARRAY)基板。

6. 如申請專利範圍第1項之感測式半導體裝置製法，其中，該半導體晶片係為微控制器(MCU)、記憶體單元所構成之功能性半導體晶片。

7. 如申請專利範圍第1項之感測式半導體裝置製法，其中，該感測式晶片係為打線式感測式晶片及晶片尺寸封裝(Chip Size Package, CSP)型感測式晶片之其中一者。

8. 如申請專利範圍第1項之感測式半導體裝置製法，其中，該軟式印刷電路板(FPC)係利用導電材料以接置於晶片承載件第二表面之電性接點。

9. 如申請專利範圍第1項之感測式半導體裝置製法，其中，該接置於晶片承載件第一表面上之半導體晶片係可採複數堆疊方式。

10. 如申請專利範圍第1項之感測式半導體裝置製法，其中，該晶片承載件第一表面側之封裝膠體上接置有散熱片及表面呈凹凸狀之散熱結構之其中一者。

11. 一種感測式半導體裝置，係包括：

一具第一表面及相對第二表面之晶片承載件；

至少一半導體晶片，係接置並電性連接至該晶片承載件第一表面上；

一封裝膠體，係全面完整包覆該半導體晶片及該晶片承載件第一表面；

至少一感測式晶片與對應透光蓋體，係接置於該晶片承載件第二表面上，且該感測式晶片係與該晶片承載件相互電性連接；以及

至少一軟式印刷電路板(FPC)係接置並電性連接至該晶片承載件第二表面上。

12. 如申請專利範圍第 11 項之感測式半導體裝置，其中，該晶片承載件係為基板。

13. 如申請專利範圍第 11 項之感測式半導體裝置，其中，該晶片承載件側面係外露出所形成之封裝膠體，並與該封裝膠體之側面切齊。

14. 如申請專利範圍第 11 項之感測式半導體裝置，其中，該半導體晶片係以銲線及覆晶方式之其中一者而電性連接至該晶片承載件。

15. 如申請專利範圍第 11 項之感測式半導體裝置，其中，該晶片承載件第一及第二表面上係可選擇性設置被動元件。

16. 如申請專利範圍第 11 項之感測式半導體裝置，其中，該晶片承載件係為 LGA (LAND GRID ARRAY)基板。

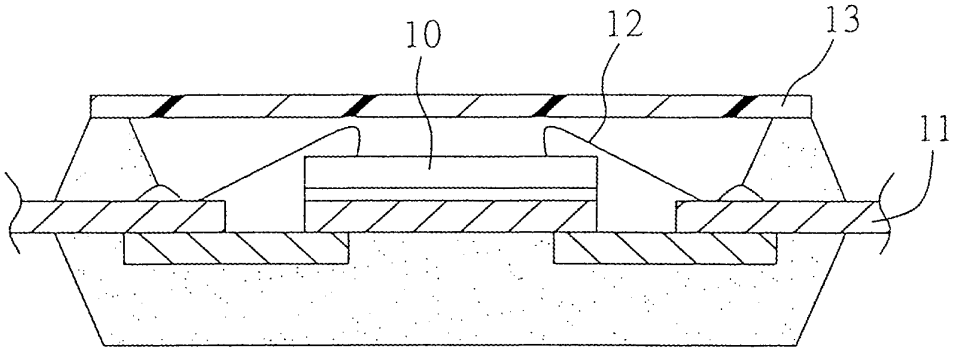
17. 如申請專利範圍第 11 項之感測式半導體裝置，其中，該半導體晶片係為微控制器(MCU)、記憶體單元所構成之功能性半導體晶片。

18. 如申請專利範圍第 11 項之感測式半導體裝置，其中，該感測式晶片係為打線式感測式晶片及晶片尺寸封裝(Chip Size Package, CSP)型感測式晶片之其中一者。

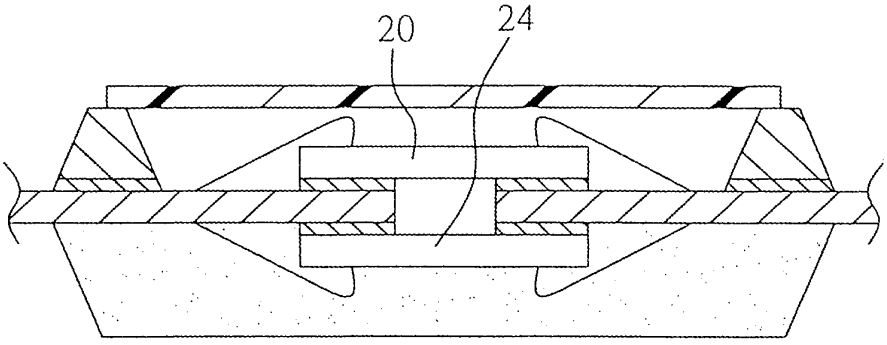
19. 如申請專利範圍第 11 項之感測式半導體裝置，其中，該軟式印刷電路板(FPC)係利用導電材料以接置於晶片承載件第二表面之電性接點。

20. 如申請專利範圍第 11 項之感測式半導體裝置，其中，該接置於晶片承載件第一表面上之半導體晶片係可採複數堆疊方式。

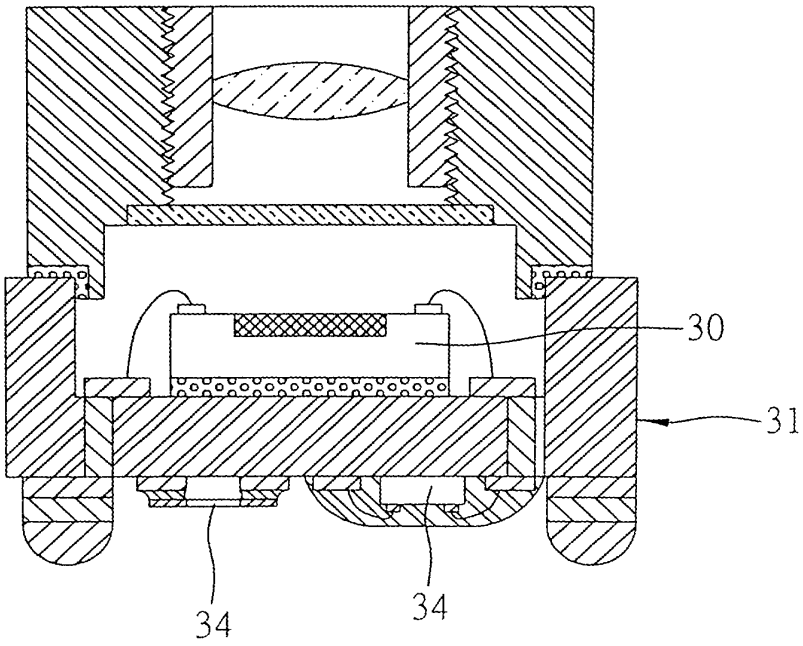
21. 如申請專利範圍第 11 項之感測式半導體裝置，其中，該晶片承載件第一表面側之封裝膠體上接置有散熱片及表面呈凹凸狀之散熱結構之其中一者。



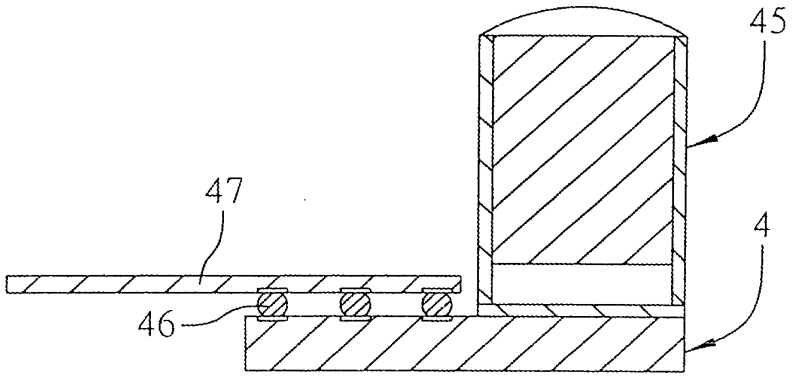
第 1 圖



第 2 圖

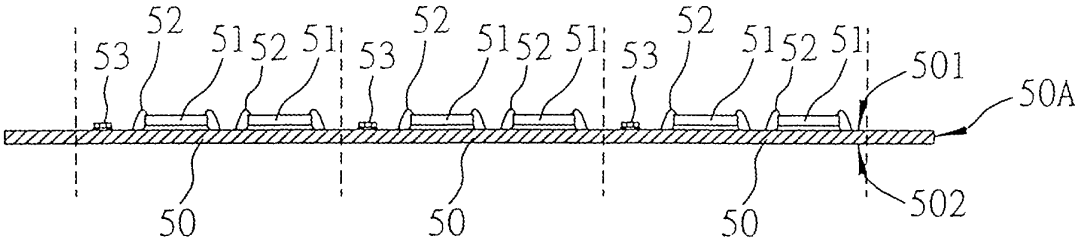


第 3 圖

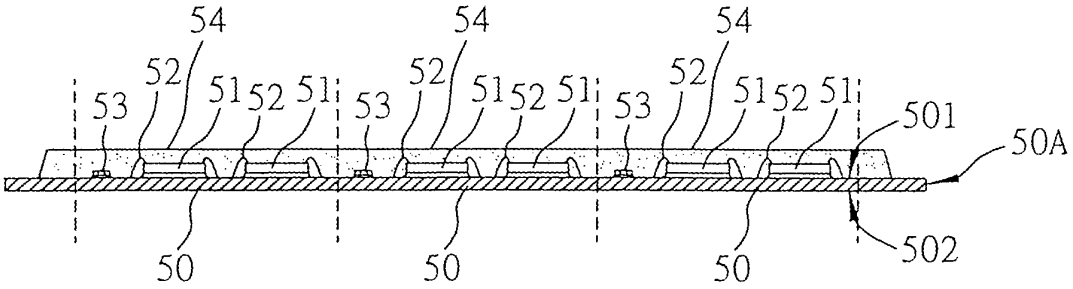


第 4 圖

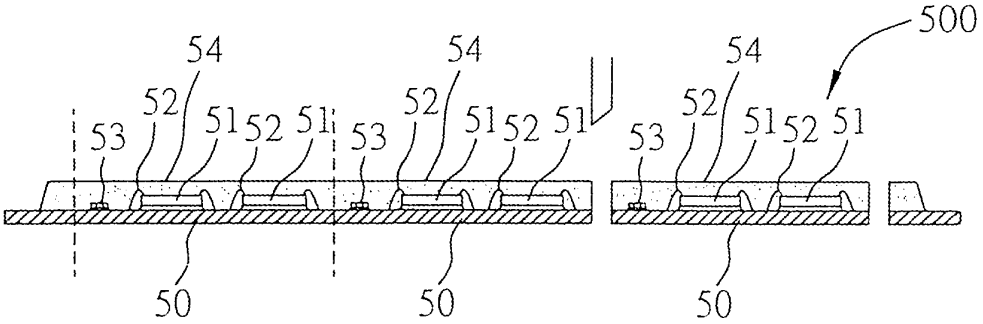
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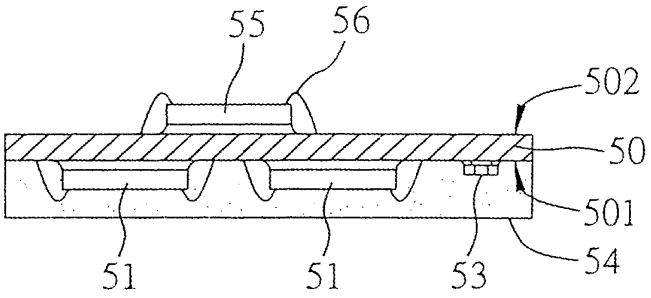
第 5A 圖



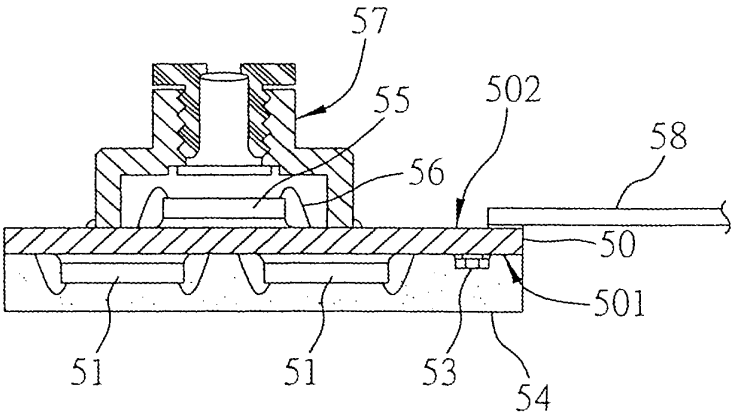
第 5B 圖



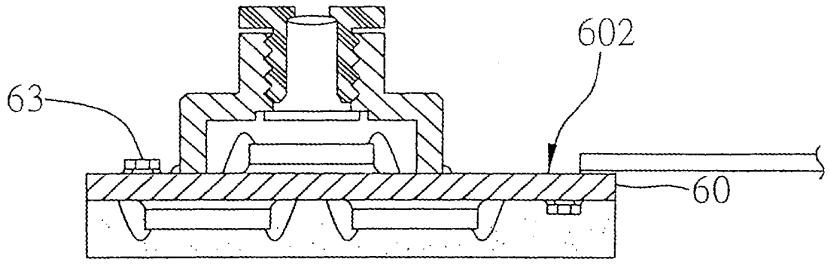
第 5C 圖



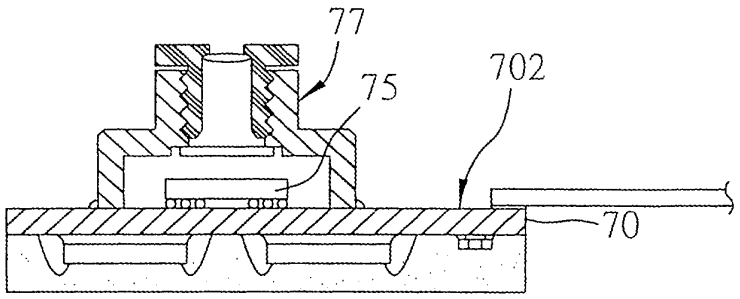
第 5D 圖



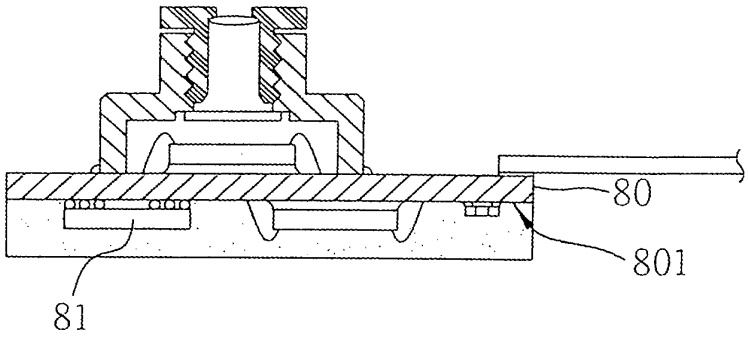
第 5E 圖



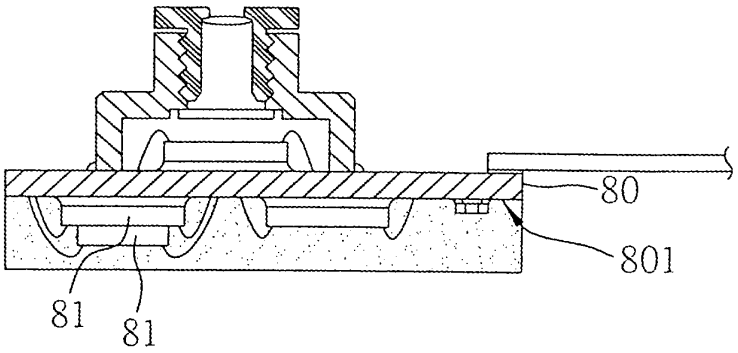
第 6 圖



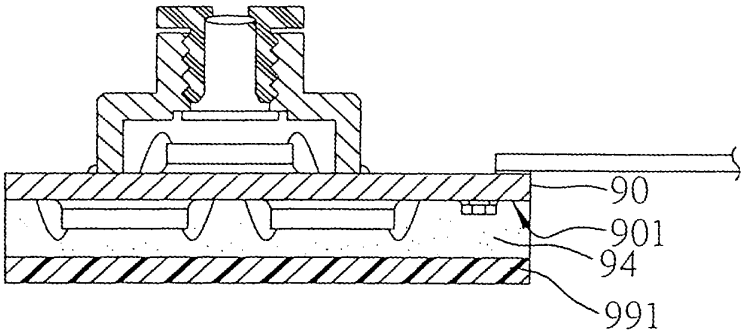
第 7 圖



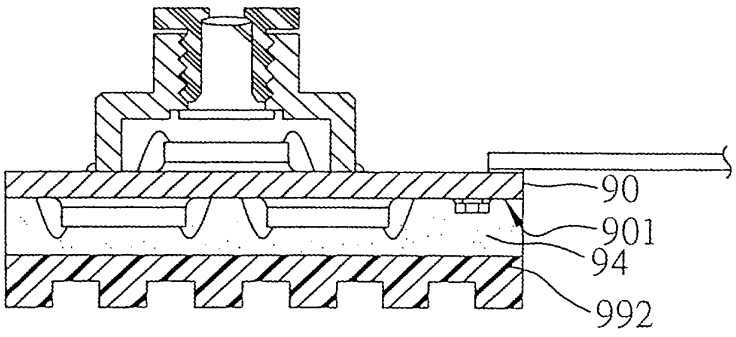
第 8A 圖



第 8B 圖



第 9A 圖



第 9B 圖

Espacenet

Bibliographic data: TWI471357 (B) — 2015-02-01

E/E connector and polymer composition used therein

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Applicant(s): DSM IP ASSETS BV [NL] ± (DSM IP ASSETS B. V)

Classification: **- international:** ***C08G69/26; H01R13/46***
- cooperative: **C08G69/265**; **C08K3/0033**; **C08K3/0058**; **C08L77/06**; **H01R13/527**; C08K3/38; C08K7/14; C08L25/18 more

Application number: TW20080127765 20080722

Priority number(s): EP20070014395 20070723

Also published as: TW200911880 (A) WO2009012936 (A1) US2010279550 (A1) US9080029 (B2) KR20100051666 (A) more

Abstract of TW200911880 (A)

This invention relates to a flame retardant polyamide composition comprising a semi-aromatic polyamide, a flame retardant system and a reinforcing agent, wherein the semi-aromatic polyamide comprises units derived from dicarboxylic acids comprising terephthalic acid and aliphatic dicarboxylic acids, and aliphatic diamines. In the semi-aromatic polyamide the aliphatic diamines consist of 10-70 mole % of a short chain aliphatic diamine with 2-5 C atoms and 30-90 mole % of a long chain aliphatic diamine with at least 6 C atoms; the dicarboxylic acids consist of 5-65 mole % aliphatic dicarboxylic acid and optionally aromatic dicarboxylic acid other than terephthalic acid and 35-95 mole % terephthalic acid; and the combined molar amount of terephthalic acid and the long chain aliphatic diamine is at least 60 mole %, relative to the total molar amount of the dicarboxylic acids and diamines. The invention also relates to a housing for an electrical / electronic (E/E) connector and use therein of the flame retardant polyamide composition, to a surface mounting process wherein the E/E connector is used and to a surface mounted device comprising the E/E connector.

I471357

公告本 第097127765號專利申請案 說明書替換頁 日期：102年11月29日

發明專利說明書

102年11月29日修正替換頁

（本說明書格式、順序及粗體字，請勿任意更動，※記號部分請勿填寫）

※申請案號：97127765

※申請日期：97.7.22 ※IPC分類：C08G 69/26
H01R 13/46

一、發明名稱：（中文/英文）

電氣/電子連接器及用於其中的聚合物組成物

E/E CONNECTOR AND POLYMER COMPOSITION USED THEREIN

二、申請人：（共 1 人）

姓名或名稱：（中文/英文）

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荷蘭 / THE NETHERLANDS

三、發明人：（共 5 人）

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   VAN PELT, WILFRED WILHELMUS GERARDUS JOHANNES
3. 徐康哲 / HSU, KANG TSE
4. 杜弗爾 彼得 R. / DUFOUR, PETER REMCO
5. 入部宏美 / IRIBE, HIROMI

國　籍：（中文/英文）

1.2.4. 荷蘭 / THE NETHERLANDS

3. 台灣 / TAIWAN

5. 日本 / JAPAN

四、聲明事項：

☐ 主張專利法第二十二條第二項☐第一款或☐第二款規定之事實，其事實發生日期為：。

☑ 申請前已向下列國家（地區）申請專利：

【格式請依：受理國家（地區）、申請日、申請案號　順序註記】

☑ 有主張專利法第二十七條第一項國際優先權：

1. EPO、　2007/07/23、　07014395.3

☐ 無主張專利法第二十七條第一項國際優先權：

☐ 主張專利法第二十九條第一項國內優先權：

【格式請依：申請日、申請案號　順序註記】

☐ 主張專利法第三十條生物材料：

☐ 須寄存生物材料者：

國內生物材料 【格式請依：寄存機構、日期、號碼　順序註記】

國外生物材料 【格式請依：寄存國家、機構、日期、號碼　順序註記】

☐ 不須寄存生物材料者：

所屬技術領域中具有通常知識者易於獲得時，不須寄存。

五、中文發明摘要：

本發明係有關於一種阻燃性聚醯胺組成物，包含半芳香族聚醯胺、阻燃系統，及強化劑，其中，半芳香族聚醯胺包含自包含對苯二甲酸及脂族二羧酸之二羧酸及脂族二胺衍生之單元。於半芳香族聚醯胺，脂族 二胺係由10-70莫耳%之具有2-5個C碳子之短鏈脂族二胺及30-90莫耳%之具有至少6個C原子之長鏈脂族二胺所組成；二羧酸係由5-65莫耳%之脂族二羧酸及選擇性之非對苯二甲酸之芳香族二羧酸及35-95莫耳%之對苯二甲酸所組成；且對苯二甲酸及長鏈脂族二胺之混合莫耳量相對於二羧酸及二胺之總莫耳量係至少60莫耳%。本發明亦係有關於一種用於電氣/電子(E/E)連接器之外殼，及阻燃性聚醯胺組成物於其它之使用，其間使用此E/E連接器之表面安裝方法，及包含此E/E連接器之表面安裝裝置。

六、英文發明摘要：

This invention relates to a flame retardant polyamide composition comprising a semi-aromatic polyamide, a flame retardant system and a reinforcing agent, wherein the semi-aromatic polyamide comprises units derived from dicarboxylic acids comprising terephthalic acid and aliphatic dicarboxylic acids, and aliphatic diamines. In the semi-aromatic polyamide the aliphatic diamines consist of 10-70 mole% of a short chain aliphatic diamine with 2-5 C atoms and 30-90 mole % of a long chain aliphatic diamine with at least 6 C atoms; the dicarboxylic acids consist of 5-65 mole% aliphatic dicarboxylic acid and optionally aromatic dicarboxylic acid other than terephthalic acid and 35-95 mole % terephthalic acid; and the combined molar amount of terephthalic acid and the long chain aliphatic diamine is at least 60 mole %, relative to the total molar amount of the dicarboxylic acids and diamines. The invention also relates to a housing for an electrical / electronic (E/E) connector and use therein of the flame retardant polyamide composition, to a surface mounting process wherein the E/E connector is used and to a surface mounted device comprising the E/E connector.

七、指定代表圖：

(一)本案指定代表圖為：第（　　）圖。(無)

(二)本代表圖之元件符號簡單說明：

八、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

(無)

九、發明說明：

【發明所屬之技術領域】

本發明係有關於電氣/電子(E/E)連接器及其它之非阻燃性及阻燃性之聚醯胺組成物之使用。本發明亦係有關於其間使用此E/E連接器之表面安裝方法，及包含此E/E連接器之表面安裝裝置。本發明進一步係有關於包含半芳香族聚醯胺、阻燃系統，及強化劑之阻燃性聚醯胺組成物，其中，半芳香族聚醯胺包含自包含對苯二甲酸及脂族二羧酸之二羧酸及脂族二胺衍生之單元，其可用於連接器。

【先前技術】

電氣連接器係一種用以使電路結合在一起之導電裝置。例如，安裝於印刷電路板(PCB)上之端子台能使個別之電線與電路板連接。此連接可為暫時，如用於攜帶式設備，或可能需要用於組裝及移除之工具，或可能係二電線或裝置間之永久性之電氣結合。典型上，此一電氣連接器包含導電元件，或以由電絕緣材料(諸如，塑膠材料)製造之外殼包封之二或更多之導電元件。塑膠材料可為包含不同組份之聚合物組成物，且外殼可藉由射出成型方法製造。用於電氣及電子應用之射出成型零件之聚合物組成物需遵從許多要求，一般包含作為基本要求之阻燃性。對於許多此等應用，阻燃劑之存在對於通過UL-94 V-0 易燃性分級係重要的，以便獲得作為電氣及電子組件之UL資格。其次，亦有其間阻燃性要求較不嚴格且阻燃劑並不一定需要(例如，其間UL-HB分級係足夠者)之連接器應用。由於連接器

之小型化，機械性質亦變得更重要，例如，有關於PCB上之剝離強度、觸點上之高預載，及重環境測試，其需要高的抗濕熱衝擊性。再者，經常地，射出成型零件係相常複雜，且其於最終使用條件下之尺寸安定性變成係性能之重要特質。此於其間零件之截面相當薄及其間相同零件可能相對較長之電氣/電子(E/E)連接器應用係特別真。對於電子連接器，組件整體性及插針位置之保持需要於焊接處理期間所遭遇之高溫下之優異尺寸安定性。於許多情況，當電子連接器使用表面安裝技術(SMT)與電路板焊接時，此等處理遭遇之高的表面溫度造成塑膠連接器起泡。由於鉛之禁止，焊接溫度因波峰焊接及回流焊接而增加。起泡係於焊接處理條件下之孔隙、捕獲水份，或氣體膨脹而顯現。因為高溫無鉛焊接方法之趨勢，使用傳統聚醯胺組成物與現今之連接器處理程序結合對於避免起泡係不足夠。控制且因而避免E/E連接器外殼起泡之關鍵參數係控制模製零件之水份吸收。起泡係於外殼之樹脂以水蒸氣超飽和時發生。許多用於PCB之組件係於世界上之太平洋沿岸區域為之。連接器可能被曝置之高的溫度及水份含量會造成此等連接器以水飽和。

浮泡開始之溫度係依數個因素而定，包含零件內之水份百分率、連接器加熱速度，及回流處理之峰值溫度、結晶性，及模製條件(例如，模製溫度、熔融溫度)、貯存條件(例如，溫度、% RH、時間)，及零件設計特性(即，厚度、長度)。模製零件通常貯存於潮濕條件下，以降低焊接處理

期間起泡之傾向。

峰值溫度愈高，起泡發生前允許之水份含量愈低。無鉛之焊料需要較高之峰值溫度，因此，起泡之發生頻率愈大。

聚醯胺樹脂組成物因其水份吸收特性(此不利地影響尺寸安定性及其於焊接條件下對起泡之抗性)而於歷史上發現於電子/電氣應用具有限之利用。

用於連接器之聚醯胺之例子係，例如，聚醯胺-46及半芳香族共聚醯胺。以對苯二甲酸(TA)及六甲撐基二胺(HMD)為主，選擇性包含作為脂族二羧酸之己二酸，之半芳香族共聚醯胺一般係描述於專利文獻。自TA及脂族二胺製成之高溫，半結晶性，半芳香族耐綸共聚物，與自TA、脂族二羧酸，及脂族二胺製成之共聚物係自US-6,140,459得知。US-6,140,459之共聚物係以TA、具有9-12個碳原子之脂族二羧酸，及作為脂族二胺之HMD為主。

如於US-6,140,459中所述，專利文獻中所述或於商業上存在之許多以TA及HMD為主之共聚物於表面安裝應用賦予極邊際之性能。此係6T/DT [50/50莫耳比例](六甲撐基對苯二甲醯胺(6T)及2-甲基五甲撐基對苯二甲醯胺(DT)之共聚物)之情況(Mok, Pagilagan之美國專利第5,378,800號案；Lahary, Coquard之美國專利第5,322,923號案)，其係因其高的玻璃轉移溫度(Tg)及高的後模製收縮率。以3種酸(對苯二甲酸(TA)、間苯二甲酸(IA)及己二酸(AA))及HMD為主之六甲撐基對苯二甲醯胺/六甲撐基間苯二甲醯胺/六甲撐

基己二醯胺(6T/6I/66)[65/25/10莫耳比例]之三元共聚物(Poppe, Lisle等人之美國專利第Re. 34,447號案)當安裝於冷模上具有高的模製及後模製之收縮率。相似者係對於六甲撐基對苯二甲醯胺/六甲撐基間苯二甲醯胺/六甲撐基癸二醯胺(6T/6I/610)之三元共聚物[70/20/10莫耳比例](Amimoto等人之美國專利第5,424,104號案)之情況，其係因為其高的Tg。此亦係於六甲撐基對苯二甲醯胺/己內醯胺(6T/6)[70/30]之共聚物(Kopietz, Betz, Blinne, Koch 之EP 413258)之情況，其係因以TA、AA及HMD為主，以55/45莫耳比例(美國專利第5,424,104號案)或65/35莫耳比例(美國專利第Re. 34,447號案)之六甲撐基對苯二甲醯胺/六甲撐基己二醯胺(6T/66)之共聚物之其高的Tg，展現可接受之後模製收縮率，但於熔融加工處理性(即，熱安定性及流動性)、吸水性，及抗起泡性係不及。

如於US-6,140,459中進一步陳述，除如上之半芳香族聚醯胺外，對於許多之E/E連接器應用，聚醯胺46、PPS及LCP已被使用。但是，聚醯胺46係對水份敏感，因此，起泡會於回流焊接處理條件下觀察到。PPS因其脆性而易造成腐蝕問題及零件破壞。LCP可提供比其它材料更佳之性能，但其熔接線強度低且價格高。

US-6,140,459提供之解答係一種阻燃性聚合物組成物，其包含阻燃系統、選擇性之無機填料，及自對苯二甲酸(TA)、具有9-12個碳原子之脂族二羧酸，及六甲撐基二胺(HMD)製成之半結晶，半芳香族耐綸共聚物，其中，此

聚合物具有少於或等於90℃之玻璃轉移溫度(Tg)及至少295℃之熔點(Tm)。此等產物被請求提供於用於電子連接器所需之SMT(表面安裝技術)IR熔回流焊接條件下之低的後模製收縮率、良好之熔融安定性及加工處理性、低吸水性，及優異之抗起泡性。

基於安裝中涉及之更高峰值溫度，以去除可能火災危險之安全方面而言之增加的重要性，及造成具有更為尺寸精準之更小零件之小型化之各種趨勢，需要更為，且甚至更佳之於SMT條件下顯示良好之熔融安定性及加工處理性、尺寸安定性、良好之機械性質，及優異之抗起泡性之阻燃性材料。此等材料需顯示擴大之抗起泡性及擴大之焊接能力，此等材料需顯示之其它性質係提供長流動路徑、薄零件、低孔隙之高流動性，同時維持良好之機械性質(諸如，高硬挺性及韌性)。再者，尺寸安定性於脫模後，焊接前後，及於熱/濕條件之環境曝置後係需要。

【發明內容】

因此，目的係提供一用於電氣連接器之塑料外殼，及一包含此塑料外殼之連接器 ，及另外之可用於連接器之阻燃性聚合物材料，其以抗起泡性而言具有較佳性質。同時，此材料需具有良好之熔融安定性及加工處性理之平衡、機械性質及尺寸安定性，較佳地，整體平衡亦被改良。

此目的已以依據本發明之連接器及其中之由包含強化劑及包含自包含對苯二甲酸之二羧酸及包含脂族二胺之二胺衍生之單元之半芳香族聚醯胺共聚物之強化聚合物組成

物製造之塑料外殼達成，其中，

a.二羧酸(A)係由5-65莫耳%之脂族二羧酸及選擇性之非對苯二甲酸之芳香族二羧酸(A1)及35-95莫耳%之對苯二甲酸(A2)之混合物所組成；及

b.脂族二胺(B)係由10-70莫耳%之具有2-5個C原子之短鏈脂族二胺(B1)及30-90莫耳%之具有至少6個C原子之長鏈脂族二胺之混合物所組成；

c.對苯二甲酸(A2)及長鏈脂族二胺(B2)之混合莫耳量相較於二羧酸及二胺之總莫耳量係至少60莫耳 %。

【實施方式】

為了緊湊及閱讀性，半芳香族聚醯胺共聚物於此亦表示為半芳香族聚醯胺X，或甚至更短地為聚醯胺X。

此目的已以一強化阻燃性聚合物組成物所達成，其係以阻燃添加劑及強化劑配製，且包含半芳香族聚醯胺，其中，半芳香族聚醯胺係與此間於上對於連接器所述者相同。

為了本發明，包含外殼或其包封材料之電氣或電子連接器係意指用以使此連接可為暫時性，如用於攜帶式裝置，或可能需要用於組裝及移除之工具，或可為二電線或裝置間之永外性電氣接合。

於本發明之一較佳實施例，連接器之塑料外殼係由此間於上所述之阻燃性聚合物組成物所製成。

由該強化聚合物組成物所製成之依據本發明之塑料連接器外殼於用於電子連接器之表面安裝技術(SMT)使用之回流焊接條件下展現優異之抗起泡性，與良好之加工處理

性，及機械性能、收縮行為與尺寸安定性之極良好之平衡。

本發明之E/E連接器已被發現具有優於其它聚醯胺組成物(包含PA46、PA6T/66及PA9T組成物)之改良之抗起泡性。此係不可預期，特別是，本發明之E/E 連接器之水份吸收或吸取係大量地高於被認為"良好之抗起泡性"之傳統聚醯胺E/E連接器(諸如，PA 9T)。

除無鉛焊接方法之趨勢外，具有使E/E連接器進一步小型化之趨勢。此趨勢導致未彎曲且於高溫能具有良好機械性質(諸如，硬挺性)之薄壁設計之需求。與適用於E/E連接器之傳統聚醯胺組成物相比，本發明之E/E連接器能提供改良之抗彎曲性及於高溫時之改良硬挺性之組合。等向性之行為、於與聚合物流動平行及垂直方向之相關之相似的線性熱膨脹系數，及於高溫之改良硬挺性之組合係驚人的，因為於機械性質(諸如，硬挺性)之改良典型上係與各向異性之材料有關，其中，促進之性質係自此材料增加方向衍生。

依據本發明之塑料連接器外殼中之強化聚合物組成物亦顯示比相對應之以PA-6T/66為主之阻燃性組成物更佳之流動及較高之硬挺性。此新穎組成物亦顯示高模量及極良好之尺寸安定性，其不僅於低於Tg時，而且於高於Tg時。此以本發明組成物中之高溫半結晶性聚醯胺具有相對較低結晶性且，再者，淨聚醯胺本身於高於Tg時具有相對較低模量之事實而言係特別驚人。依據本發明之組成物所包含之半結晶性聚醯胺亦具有相對較高之Tg，其數個實施例具有高於90°C之Tg，即，高於US-6,140,459般之90°C上限，而

仍具有極良好之尺寸安定性。某些聚合物具有與6T/DT者(此聚合物於US-6,140,459中提及係不適用於電氣連接器)一樣高之Tg，甚至於150°C模製溫度模製，係因為其高的玻璃轉移溫度(Tg)及高的後模製收縮。 與PA6T/66及PA46相比之改良之抗起泡性及良好之尺寸安定性結果亦於半結晶性半芳香族聚醯胺包含與，例如，作為長鏈二胺之己二胺混合之作為短鏈二胺之1,4-二胺基丁烷，及作為羧酸之 對苯二甲酸及己二酸(因此表示PA6T/66/46共聚物)時獲得。同時，本發明組成物之其它良好性質被維持。此結果以聚醯胺46係高度水份敏感性，其模製物件易為尺寸不安定且起泡係於回流焊接處理條件下經常觀察到(如US-6,140,459中所報導)之事實係特別驚人。

依據本發明第二實施例之強化阻燃性聚醯胺組成物不僅展現上述之強化聚合物組成物之性質，而且亦顯示高的介電破壞強度，甚至比數種其它聚醯胺組成物更佳。

需注意，若可應用，此等改良係以以半芳香族聚醯胺X，個別是依據所述習知技藝之共聚醯胺(諸如，聚醯胺6T/66) 為主之聚醯胺組成物之比較為基準，其中，聚醯胺X及該共聚醯胺被配製成具有相似熔融溫度。

塑料連接器外殼及依據本發明之強化阻燃性聚醯胺組成物所包含之半芳香族聚醯胺X包含自脂族之二胺及二羧酸衍生之單元。自二羧酸衍生之單元可表示為A-A單元，且自二胺衍生之單元可表示為B-B單元。與其一致地，聚醯胺可表示為AABB聚合物，其係相對應於，例如，Nylon Plastic

handbook, Ed. M.I. Kohan, Hanser Publishers, Munich, ISBN 1-56990-189-9 (1995)，第5頁中之分類。

短鏈脂族二胺(B1)係C2-C5脂族二胺，或其混合物。換言之，其具有2-5個碳(C)原子。短鏈脂族二胺可為，例如，1,2-乙二胺、1,3-丙二胺、1,4-丁二胺，及1,5-戊二胺，及其等之混合物。較佳地，短鏈脂族二胺係選自1,4-丁二胺、1,5-戊二胺，及其等之混合物所組成之族群，更佳係1,4-丁二胺。

長鏈脂族二胺(B2)係具有至少6個碳(C)原子之脂族二胺。長鏈脂族二胺可為線性、分支，及/或脂環狀。長鏈脂族二胺可為，例如，2-甲基-1,5-戊二胺(亦稱為2-甲基五甲撐基二胺)、1,5-己二胺、1,6-己二胺、1,4-環己二胺、1,8-辛二胺、2-甲基-1,8-辛二胺、1,9-壬二胺、三甲基六甲撐基二胺、1,10-癸二胺、1,11-十一烷二胺、1,12-十二烷二胺、間-二甲苯二胺，及對-二甲苯二胺，及其等之混合物。較佳地，長鏈脂族二胺具有6-12個碳原子，且適合地係C8-或C10二胺。於一較佳實施例，長鏈二胺係由50-100莫耳%，更佳係75- 100莫耳%之具有6至9個碳原子之二胺所組成。此造成具有更佳之高溫性質之材料。更佳地，長鏈脂族二胺係選自1,6-己二胺、2-甲基-1,8-辛二胺、1,9-壬二胺，及其等之混合物所組成之族群，更佳係1,6-己二胺。此較佳選擇且特別是更佳選擇1,6-己二胺之優點係依據本發明之共聚醯胺之高溫性質係更佳。

脂族二羧酸可為直鏈、分支鏈，及/或脂環狀，且其間之碳原子數並被特別限制。但是，脂族二羧酸較佳係包含

具有4至25個碳原子之直鏈或分支鏈之脂族二羧酸，或其等之混合物，更佳係6-18個且更佳係6-12個碳原子。適合之脂族二羧酸係，例如，己二酸(C6)、1,4-環己烷二羧酸(C8)、辛二酸(C8)、癸二酸(C10)、十二烷二酸(C12)，或其等之混合物。較佳地，脂族二羧酸係C6-C10脂族二羧酸，包含己二酸、癸二酸，或其等之混合物，且更佳地，脂族二羧酸係C6-C8脂族二羧酸。最佳地，脂族二羧酸係己二酸。

除對苯二甲酸外，芳香族二羧酸可包含其它之芳香族二羧酸，例如，間苯二甲酸及/或萘二羧酸。

除對苯二甲酸外，此半-芳香族聚醯胺可適合地包含脂族 二羧酸，及選擇性地，非對苯二甲酸之 芳香族二羧酸，與其等之任何混合物。較佳地，相較於脂族二羧酸及非對苯二甲酸之芳香族二羧酸(A1)之總莫耳量，非對苯二甲酸之芳香族二羧酸之量係少於50莫耳%，更佳係少於25莫耳%。

於依據本發明之組成物中之半芳香族聚醯胺，短鏈脂族二胺(B1)構成10-70莫耳%，且長鏈脂族二胺(B2)構成脂族二胺單元(B)之剩餘之30-90莫耳%。

較佳地，相較於短鏈及長鏈之二胺之莫耳量，短鏈脂族二胺之莫耳量最多係60莫耳%，更佳係50莫耳%，40莫耳%，或甚至35莫耳%。具有此一較低莫耳量之短鏈二胺之共聚醯胺之優點係對於具特定Tm之共聚醯胺，起泡行為改善。

亦較佳地，相對於短鏈脂族二胺及長鏈脂族二胺之總

莫耳量，半芳香族聚醯胺內之短鏈脂族二胺之莫耳量係至少15莫耳%，更佳地，係至少20莫耳%。短鏈脂族二胺之莫耳量愈高，聚醯胺之熱安定性愈好。

脂族二羧酸及非對苯二甲酸之芳香族二羧酸(A1)構成5-65莫耳%，且對苯二甲酸(A2)構成二羧酸單元(A)之剩餘35-95莫耳%。

較佳地，二羧酸由至少40莫耳%，更佳係至少45莫耳%，或甚至至少50莫耳%之對苯二甲酸組成。增加量之對苯二甲酸之優點係高溫性質被進一步改良。亦較佳地，脂族二羧酸及選擇性非對苯二甲酸之芳香族二羧酸(A1)之量係二羧酸之至少10莫耳%，更佳係至少15莫耳%。此較高量具有組成物具有較佳加工處理性之優點。

於一高度較佳實施例，相較於二羧酸之莫耳量，二羧酸(A)係由50-85莫耳%之對苯二甲酸(A2)及50-15莫耳%之脂族二羧酸及選擇性之非對苯二甲酸之芳香族二羧酸(A1)所組成，其間之非對苯二甲酸之芳香族二羧酸若存在，其相較於脂族二羧酸及非對苯二甲酸之芳香族二羧酸(A1)之總莫耳量，係少於25莫耳%，且相較於脂族二胺之總莫耳量，脂族二胺(B)係由40-80莫耳%之長鏈二胺(B2)及60-20莫耳%之短鏈二胺(B1)所組成。此較佳之組成物賦予起泡性質、介電破壞強度、加工行為，及機械性質之較佳整體平衡。

若相較於脂族二胺之總莫耳量，長鏈脂族二胺之最小量係30莫耳%，且相較於二羧酸之莫 耳量，對苯二甲酸之

數小量係35莫耳%，則相較於二羧酸及二胺之總莫耳量，對苯二甲酸及長鏈脂族二胺之混合莫耳量係至少60莫耳%。其結果係當長鏈脂族二胺之相對量係最小30莫耳%，對苯二甲酸之相對量係至少90莫耳%。有利地，當對苯二甲酸之相對量係最小35莫耳%，長鏈脂族二胺之相對量係至少85莫耳%。

於另一高度較佳實施例，相較於二羧酸及二胺之總莫耳量，對苯二甲酸(A2)及長鏈脂族二胺(B2)之莫耳量總和係至少65莫耳%，更佳係至少70莫耳%，且更佳係至少75莫耳%。具有對苯二甲酸(A2)及長鏈脂族二胺(B2)之莫耳量總和較高之聚醯胺之優點 係此聚醯胺結合較高之介電破壞值與較佳之熱安定性及良好之熔融加工處理性。適合地，相較於二羧酸及二胺之總莫耳量，該總和係於70-85莫耳%之範圍內，或甚至75-80莫耳%。

除自二羧酸(AA)及二胺(BB)衍生之A-A-B-B單元外，依據本發明之聚醯胺可包含自其它組份(諸如，脂族胺基羧酸(AB單元)及相對應之環狀內醯胺)衍生之單元，與 小量之分支劑及/或鏈中止劑。

較佳地，相較於聚醯胺之總質量，依據本發明之聚醯胺包含至多10質量%，更佳係至多8質量%，且更佳係至多5質量%，之自非二羧酸及二胺之組份衍生之單元。最佳地，依據本發明之聚醯胺不包含此等其它組份，且僅由自二羧酸及二胺衍生之A-A-B-B單元組成。優點係邏輯上較簡單之處理及較佳之結晶性質。

較佳地，具芳香族聚醯胺具有多於100°C，更佳係至少110°C，或甚至至少120°C之玻璃轉移溫度(Tg)。較佳地，Tg至多係140°C，更佳係至多130°C。亦較佳地，半芳香族聚醯胺具有至少295°C，較佳係至少300°C，更佳係至少310°C之熔融溫度(Tm)。較佳地，Tm係至多340°C，更佳係至多330°C。較高之Tm造成較佳之抗起泡性。Tg及Tm於此等限制內之另一優點係於抗起泡性、尺寸安定性，及加工行為之較佳平衡。

此間之Tg及Tm之測量係藉由DSC使用下列方法為之。熔點(溫度)一辭於此被瞭解係依據ASTM D3417-97/D3418-97藉由DSC且以10℃/分鐘之加熱速率測量之溫度，其係落於熔融範圍且顯示最高熔融速率。玻璃轉移點一辭於此被瞭解係依據ASTM E 1356-91藉由DSC且以10°C/分鐘之加熱速率測量且以母加熱曲線之第一衍生線(關於時間)之波峰處，相當於母加熱曲線之彎曲點，之溫度而決定之溫度。

該半芳香族聚醯胺可具有於廣範圍變化之黏度。驚人地，已觀察到該半芳香族聚醯胺可具有低達1.6或甚至更低之相對黏度，而仍維持抗起泡性及良好之機械性質，甚至對於包含強化劑及阻燃劑之強化阻燃性組成物。一般，聚醯胺且特別是具有此低分子量之半芳香族聚醯胺係極脆，此性質係於填料及阻燃劑被包含時提高。與包含依據引述之習知技藝之半芳香族聚醯胺之相對應組成物相比較，依據本發明之強化阻燃性組成物顯示改良之硬挺性。

較佳地，相對黏度係至少1.7，更佳係1.8，或甚至1.9。機械強度之保持對於此等模製零件係確實重要，其於低相對黏度時仍係事實。亦較佳地，相對黏度係少於4.0，更佳係少於3.5，且更佳係少於3.0。此較低相對黏度具有於模製期間之流動係較佳且具較薄元素之模製零件可被製得之優點。需注意相對黏度之值係與於依據ISO 307，第4版，之方法於96%硫酸中測量之相對黏度有關。

該半芳香族聚醯胺亦可由具高的相對黏度之半芳香族聚醯胺及具低的相對黏度者之摻合物所組成。適合地，此摻合物包含一具有至少1.8，更佳係至少1.9之相對黏度之組份，及一具少於1.7，更佳係少於1.6之相對黏度之組份。具有至少1.9之相對黏度之第一組份可具有至少10,000之分子量，而具有少於1.6之相對黏度之第二組份可具有少於7,500，較佳係少於5,000之分子量。第一及第二組份可以於大範圍，且較佳係於19:1 – 1:1，更佳係於9:1 – 3:1之範圍改變之重量比例存在。具相對較低黏度之第二組份存在之優點係聚醯胺組成物之模製行為被進一步改良，而能模製具有更薄之壁區段之零件。

可製造本發明連接器外殼之強化聚合物組成物可包含於廣範圍變化之量之半芳香族聚醯胺X。適合地，半芳香族聚醯胺之量係於25-95重量%之範圍，更佳地，相較於強化聚合物組成物之總重量，此組成物包含35-90重量%，或甚至45-85重量%。於依據本發明之阻燃性聚醯胺組成物，半芳香族聚醯胺亦可以於廣範圍改變之量存在。由於亦欲被

包含之阻燃劑，相對含量一般會更低。適合地，其內之半芳香族聚醯胺X之量係於25-80重量%之範圍，更佳地，此組成物包含25-60重量%，或甚至30-50重量%之半芳香族聚醯胺。

除半結晶性半芳香族聚醯胺及強化劑外，依據本發明之連接器外殼及組成物可包含一或更多之其它組份，及選擇性之阻燃系統。阻燃系統可包含聚合物阻燃劑。其它組份可包含非高溫半結晶性半芳香族聚醯胺及選擇性之聚合物阻燃劑之聚合物或聚合物組份。此等其它聚合物可包含，例如，橡膠及熱塑性聚合物。橡膠適合地包含衝擊改質劑。熱塑性聚合物可為其它聚醯胺。較佳地，聚醯胺係具有比高溫半結晶性半芳香族聚醯胺之熔融溫度更低之熔融溫度之半結晶性聚醯胺。

相較於組成物總重量，此其它聚合物較佳係以少於25重量%之量存在，更佳地，若存在，係1-20重量%，更佳係2-15重量%，且最佳係5-10重量%之量。

較低含量之其它聚合物，特別是無諸如聚醯胺-46及聚醯胺-6T/66之聚合物之優點係，例如，於曝置於較高溫度及高濕度之環境條件後，介電強度被較佳地維持。

阻燃系統可包含鹵化阻燃劑及/或無鹵素之阻燃劑，且除該阻燃劑或其組合物外，選擇性地亦包含阻燃增效劑。鹵化阻燃劑可為溴化聚合物，例如，溴化聚苯乙烯、聚溴苯乙烯共聚物、溴化環氧樹脂，及/或溴化聚苯撐氧。適合地，鹵化阻燃劑係具有高的溴含量(例如，61-70重量%)之

範圍之溴化聚苯乙烯。較高溴含量容許較低增充量之阻燃劑，及較低之流動性質。無鹵素之阻燃劑可適合地為含氮之阻燃劑、含磷之阻燃劑，及/或含氮及磷之阻燃劑。適合之無鹵素之阻燃劑係，例如，磷酸鹽，特別是聚磷酸鹽，諸如，密胺聚磷酸鹽及次膦酸鹽，特別是有機次膦酸鹽之金屬鹽，諸如，鈣及鋁之二乙基次膦酸鹽。適合增效劑之例子係銻化合物，如，三氧化銻、五氧化銻，及銻酸鈉及其它金屬氧化物，及硼酸鋅及其它金屬硼酸鹽。較佳地，增效劑係硼酸鋅，因為此提供改良之抗起泡性。

適合地，相較於組成物之總重量，阻燃系統係以1- 40重量%，較佳係5-35重量%之總量存在。較佳地，相較於組成物之總重量，阻燃劑係以5-30重量%，更佳係10-25重量%之量存在，且增效劑較佳係以0-15重量%，更佳係1-10重量%，且更佳係5-10重量%之量存在。

強化劑可包含不同之纖維材料，包含玻璃纖維及碳纖維，其中，玻璃纖維係較佳。適合地，相較於組成物總重量，強化劑係以5-50重量%，較佳係15-45重量%，更佳係25-40重量%之量存在。如前所述，強化劑對於高於Tg時之組成物模量具有強烈增加功效，此增加係大於數種其它聚醯胺。此能限制強化劑之量，但仍能達極良好之機械性質。於低程度之強化劑，強化劑之限制亦能限制阻燃劑之量以達特定之阻燃性程度。此等別是於無鹵素之阻燃劑之情況。整體功效係良好阻燃性質係以可與其它半芳香族聚醯胺相比擬但低於，例如，聚醯胺4,6所需者之量獲得，即使

本發明組成物中之半結晶性聚醯胺包含以短鏈脂族二胺及脂族羧酸為主之AABB單元，諸如，聚醯胺 4,6。進一步之優點係此等組成物之流動性質遠比以，例如，聚醯胺6T/66為主之具相似機械性質之相對應組成物更佳。

可由本發明組成物包含之其它添加劑包含用於射出成型化合物之無機填料及輔助添加劑。無機填料係，例如，玻璃薄片馭礦物填料，諸如，黏土、高嶺土、矽灰石，及滑石，及其它礦物，及其等之任何混合物。無機填料之量可於大範圍改變，但適合地，相較於組成物總重量，係於0－25重量%之範圍。

輔助添加劑被瞭解係熟習製造聚醯胺模製組成物技藝者所知之一般包含於該聚醯胺組成物內之添加劑。適合之輔助添加劑係，例如，安定劑(諸如，UV安定劑、熱安定劑，及抗氧化劑)、著色劑、加工處理助劑(例如，脫模劑及潤滑劑)、流動改良添加劑(諸如，聚醯胺寡聚物)，及用以改良耐衝擊性之試劑。輔助添加劑之量可於大範圍改變，但適合地，相較於組成物總重量，係於0－10重量%，較佳係0.1－5重量%之範圍。

於本發明之一較佳實施例，連接器外殼係由一種由如下所組成之聚合物組成物製成：

- 25-85重量%之半芳香族聚醯胺X，
- 5-50重量%之強化劑，及
- 以所示量之至少一選自下列族群之組份：
- 至多50重量%之阻燃系統，

- 至多25重量%之非半芳香族聚醯胺及聚合物阻燃劑之聚合物，
- 至多25重量%之無機填料，及/或
- 至多10重量%之其它添加劑，

其中，重量百分率(重量%)係相較於組成物之總重量。

於本發明之另一較佳實施例，聚合物組成物係由如下所組成之阻燃性組成物：

- 25-80重量%之半芳香族聚醯胺，
- 5-50重量%之強化劑，及
- 1-40重量%之阻燃系統，及
- 0-25重量%之非半芳香族聚醯胺及聚合物阻燃劑之聚合物，
- 0 - 25重量%之無機填料，及/或
- 0 - 5重量%之輔助添加劑，

其中，重量百分率(重量%)係相較於組成物之總重量。

此間之其它聚合物、無機填料，及輔助添加劑係選擇性之組份，意指此等之無或僅一者，或僅二者或全部三者之混合物可存在。適合地，至少一或多種之輔助添加劑存在。

更佳地，組成物係由下述所組成：

- 30-60重量%之半芳香族聚醯胺，
- 15-45重量%之強化劑，及
- 5-35重量%之阻燃系統，
- 0.1 - 5重量%之輔助添加劑，及

- 0 - 25重量%之非半芳香族聚醯胺及聚合物阻燃劑之聚合物，及
- 0- 25重量%之無機填料。

依據本發明之共聚醯胺可以本身已知之用於製備聚醯胺及其共聚物之各種方式製備。適合方法之例子係描述於，例如，Polyamide, Kunststoff Handbuch 3/4, Hanser Verlag (München), 1998, ISBN 3-446-16486-3。包含共聚醯胺、阻燃系統，及強化劑，及一或多種添加劑之阻燃性組成物亦可藉由熟習此項技藝者所知之化合技術製造，例如，於雙螺桿擠塑機內。

此間所述之用於依據本發明之連接器之聚合物組成物可被模製成用於表面安裝之電氣/電子裝置之塑料零件，此等零件於更嚴苛之焊接處理條件下提供較佳之抗起泡性。

模製可藉由熟習塑料射出成型之技藝者所知之射出成型技術完成。包含半芳香族聚醯胺X之組成物之良好模製性有利於此等方法。對於模製性之測量，Barflow方法或螺形流方法可被應用，其中，聚合物組成物係於特定之熔融溫度及注出壓力(例如，80 Mpa，90 Mpa及/或100 Mpa)射出成型於具特定寬度及厚度之模穴內，且射出成型樣本之長度被測定。此等測試方法間之差異係於第一情況中，樣本係線性，而於第二情況，其具有似螺旋之形狀。依據本發明之阻燃性組成物之良好模製性已於螺形流測試中證實。對於製造依據本發明之連接器外殼，包含半芳香族聚醯胺X之聚合物組成物於些微高於半芳香族聚醯胺X之熔融溫度

之溫度時具有於廣範圍變化之螺形流動長度。由於該組成物之高溫安定性，射出成型裝置之設定溫度及熔融物之形成溫度可被足夠地大量提升以進一步降低螺形流動長度，且不會使聚醯胺明顯降解。但是，較佳地，聚合物組成物具有至少100 mm，更佳係至少120 mm，且更佳係至少133 mm之螺形流長度(其係於高於半芳香族聚醯胺X之熔融溫度10℃之溫度，於具有280 x 15 x 1 mm之尺寸之螺形模穴測定)。

本發明亦係有關於用於電氣連接器之塑料外殼。於一較佳實施例，塑料外殼包含如上所述之阻燃性聚醯胺組成物。本發明亦係有關於用於使電氣或電子應用內之電路結合在一起之電氣連接器，包含一導電元件及一包埋該導電元件之至少部份之塑料外殼，且其中，塑料外殼包含依據如上申請專利範圍中任一者之阻燃性聚醯胺組成物。

電氣連接器可為，例如，I/O連接器、卡座連接器，諸如，PCB連接器，FPC(平印刷電路)連接器，或FFC(平可撓性電纜)連接器，高速連接器、端子台型式、MID(模組式積體裝置)連接器、插頭插座式連接器、測試座，或其等之組合物。例如，印刷電路板(PCB)安裝之端子台被焊接於此板，但其能以拉開型式利用，使此端子台之電接連線之半部份自焊接至PCB之部份拔掉。

依據本發明之用於電氣連接器之外殼及相對應之電氣連接器提供促進之性質，其可有利地用於各種連接器應用。對於I/O連接器，優點係降低之起泡、於低填充量之阻

燃劑時增加之硬挺性，及/或纖維強化。

I/O連接器可為，例如，用於電池連接器裝置、移動式設備(諸如，行動電話)，或辦公室設備之連接器。此等應用一般涉及包含焊接步驟之SMT(表面安裝技術)之安裝方法。依據本發明之外殼於焊接處理期間顯示極佳之尺寸安定性。於此應用，由於連接器(較小之間距及主機板尺寸)(PCB上之剝離強度，觸點上之高預載，重環境測試(高濕度熱震)尺寸減小，機械性質變得更重。以且燃劑為主及以非阻燃性組成物為主之依據本發明之I/O連接器於此等方面實施良好。

I/O連接器亦可為用於汽車之連接器，即，用於電氣及電子汽車系統(例如，ECU集束連接裝置、密封式連接器、ABS模組)之連接器。依據本發明之外殼提供低吸水性及尺寸安定性、低翹曲性，及良好機械性質(亦於高溫時)、良好之抗化學性，且可被雷射焊接，所有用於汽車連接器應用所需之所有性質。

對於卡座連接器，小型化造成組合及使用期間更高之機械力，且需較佳之流動物料，同時更強且顯示較少翹曲性。依據本發明之外殼顯示比以聚醯胺-6,6為主之相對應組成物更佳之流動性，甚至比聚醯胺-46更少之翹曲性，同時仍顯示極佳之機械性質。於此等應用，高預載被應用於觸點(由於降低之高度)，造成外殼上之高機械載荷。此於回流焊接期間係重要。LCP長期被用於此等應用，但於降低厚度變重要。依據本發明之連接器於高溫(SMT溫度)保持硬挺

性。

卡座連接器適合地係PCB連接器、FPC(平印刷電路)連接器，或FFC(平可撓性電纜)連接器。特別地，對於FPC及FFC連接器，良好流動性、高硬挺性、低吸水性，及良好尺寸安定性係重要參數，此等性質於依據本發明之塑料外殼係良好平衡。

依據本發明之塑料外殼亦顯示極安定之介電分佈，且於室溫與高於此之廣泛溫度範圍，甚至於具高溫度之條件時，之極低介電反應及低介電常數，且於此方面係比依據習知技藝之相對應之半芳香族聚醯胺(諸如，聚醯胺6T/66)更佳地實施。此對於高速連接器係一重要優點。高速連接器係，例如，高速底板連接器(第3層連接器)或hdmi / UDI / 顯示器接口連接器(用於高清淅度TV)。

依據本發明之外殼及相對應之連接器之進 一步優點係藉由用以製造外殼之聚醯胺組成物所展現之高CTI(比較痕跡指數)，及相似之高介電強度，即使當組成物包含阻燃系統時。其CTI值係遠高於由，例如，聚醯胺66/6T製成之相對應產物。高CTI值使連接器高度適於高電壓應用，特別是用於端子台，及用於鐵路應用(高電壓)之連接器，且亦能進一步降低持續之小型化所需之連接器尺寸。典型上，CTI值高於400 V，符合依據UL 746-A之第1類。當以作為強化劑之一般玻璃纖維及一般阻燃劑(包含以密胺及/或磷酸鹽衍生物為主之無鹵素之阻燃劑(例如，密胺聚磷酸鹽，及次膦酸鹽之金屬鹽)，及以含鹵素之聚合物為主之含鹵素之阻

燃系統(諸如，聚溴苯乙烯)，及阻燃增效劑(諸如，硼酸鋅)，及降低CTI之遺漏或有限之添加劑)配製時，600V及更高之CTI值可被達成，因而符合依據UL 746-A之第0類。以CTI而言係中性或對於CTI具有正面作用，且避免或限制對於CTI具負面作用之添加劑之量之添加劑之選擇可由熟習製造射出成型產物之技藝者，符合一般之CTI要求且特別是UL法規，以一般知識及例行實驗為基準而選擇。高CTI值結合良好機械性質及低翹曲性可有利地產業上之高電壓端子台。較佳地，此間使用之依據本發明之外殼及阻燃材料之CTI具有至少500 V，更佳係至少600 V之CTI。

本發明進一步係有關於使用於此之如上所述之該電氣連接器用於包含回流焊接步驟之SMT方法，及包含藉由包含焊接步驟之SMT方法安裝之電氣連接器之電氣或電子裝置。除回流焊接步驟外，此方法包含涉及加熱步驟之相以安裝步驟。於加熱步驟，由於包含半芳香族聚醯胺X之聚合物組成物之抗起泡性，峰值溫度可相當高。此溫度可高達250°C及更高，且適合地係260 °C - 300°C，較佳係270°C - 280°C之範圍。藉由極短之熱載荷，即，極短期間之曝置於峰值溫度，峰值溫度可甚至高於300°C。

有數種現今可利用之焊接方法。其包含蒸氣相焊接、波焊、浸焊、IR回流焊接，及傳統之熱空氣回流焊接。本申請案請求之半芳香族聚醯胺之阻燃性組成物提供由如下表中所示之起泡結果所預期之較優之抗焊接性。上述焊接方法提供電子電路板上之表面安裝裝置之高生產力之方

法。此等方法(皆涉及加熱步驟)中之安裝步驟一般可分類為涉及熱焊接步驟之方法。

本發明以下列實施例及比較例作例示說明。

實驗

用於製備E/E連接器之聚醯胺組成物係先製備實施例1至5(E-1至E-5)及比較例(CE)A、B、C及F之聚醯胺聚合物。比較例D及E係商業上之阻燃劑，配製用於諸如開關裝置之電氣裝置之玻璃纖維強化之聚醯胺組成物。

聚合物之製備

E-1聚合物：PA-6T/4T/46 (莫耳比例67.5/21.3/11.2)

179.8克之四甲撐基二胺、347.25克之六甲撐基二胺、537克之水、0.36克之次磷酸鈉單水合物、72.36克之己二酸，及653.38克之對苯二甲酸之混合物於2.5公升之高壓釜內攪拌，並且加熱及藉由蒸餾移除水。需注意，相較於經計算之聚醯胺組成物之組成，約2-4重量%之些微過量之四甲撐基二胺已被使用，以補償於製備聚醯胺期間損失之四甲撐基二胺。約27分鐘後，91重量%之鹽水溶液被獲得。於此方法，溫度從169°C增至223°C。聚合反應係於210°C至226°C之增加溫度實行21分鐘，期間，壓力升至1.3 MPa，其後，高壓釜之內容物被蒸餾，且固體產物於氮氣下進一步冷卻。因而獲得之預聚物其後於乾燥室於125°C時於真空下且於0.02 Mpa之氮氣流加熱乾燥數小時。經乾燥之預聚物於金屬管式反應器(d= 85mm)內，於200°C且於氮氣流(2400克/小時)下數小時加熱，然後，於氮/水蒸氣之氣流(3/1

重量比例，2400克/小時)下，於225°C持續2小時，且於260°C持續4小時，而以固相後縮合。然後，聚合物冷卻至室溫。

E-2聚合物：製備PA-6T/4T/46(莫耳比例74.5/10/15.5)

以如E-1聚合物般相同之方式，127.09克之四甲撐基二胺、350.05克之六甲撐基二胺、487克之水、0.66克之次磷酸鈉單水合物、91.59克之己二酸，及567.48克之對苯二甲酸之混合物於2.5公升之高壓釜內攪拌，並且加熱，以於22分鐘後獲得91重量%之鹽水溶液。於此方法，溫度從176°C增至212°C。聚合反應係於220°C至226°C之增加溫度實行22分鐘，期間，壓力升至1.4 MPa。因而獲得之預聚物其後於乾燥室於125°C及180℃時於真空下且於0.02 Mpa之氮氣流加熱乾燥數小時。預聚物於金屬管式反應器(d= 85mm)內，於190°C及230℃且於氮氣流(2400克/小時)下數小時加熱，然後，於氮/水蒸氣之氣流(3/1重量比例，2400克/小時)下，於251°C持續96小時，而以固相後縮合。然後，聚合物冷卻至室溫。

E-3聚合物：製備PA-6T/56 (莫耳比例85/15)，其係相等於PA-6T/5T/66 (莫耳比例70/15/15)

55.3克之五甲撐基二胺(98重量%)、529.7克之含水之六甲撐基二胺(59.6重量%)、360.4克之水、0.5克之次磷酸鈉單水合物、67.2克之己二酸，及433.04克之對苯二甲酸之混合物於2.5公升之高壓釜內攪拌，並且加熱，且蒸餾移除水。35分鐘後，獲得90重量%之鹽水溶液，同時使溫度從170℃上升至212℃。然後，關閉高壓釜。聚合反應係於212°C

至250°C之增加溫度實行25分鐘。混合物於250℃攪拌15分鐘，期間，壓力升至2.9 MPa，其後，高壓釜之內容物被閃蒸，且固體產物於氮氣下進一步冷卻。預聚物於金屬管式反應器(d= 85mm)內，於200℃且於氮氣流(2400克/小時)下數小時加熱，然後，於氮/水蒸氣之氣流(3/1重量比例，2400克/小時)下，於230°C持續2小時，且於260℃持續24小時，而以固相後縮合。然後，聚合物冷卻至室溫。

E-4聚合物：製備PA-6T/5T/56(莫耳比例75.5/15/9.5)

78.4克之五甲撐基二胺(98重量%)、473.3克之含水之六甲撐基二胺(59.6重量%)、382.56克之水、0.5克之次磷酸鈉單水合物、42.6克之己二酸，及461.5克之對苯二甲酸之混合物於2.5公升之高壓釜內攪拌，並且加熱，且蒸餾移除水。35分鐘後，獲得90重量%之鹽水溶液，同時使溫度從170℃上升至212℃。然後，關閉高壓釜。聚合反應係於212°C至250°C之增加溫度實行25分鐘。混合物於250℃攪拌15分鐘，期間，壓力升至2.8 MPa，其後，高壓釜之內容物被閃蒸，且固體產物於氮氣下進一步冷卻。預聚物其後被乾燥，且以與E-1聚合物相同方式以固相後縮合。然後，聚合物冷卻至室溫。

E-5聚合物：製備PA-6T/66/56(莫耳比例76.5/12/11.5)

36.9克之五甲撐基二胺(98重量%)、553.0克之含水之六甲撐基二胺(59.6重量%)、351.2克之水、0.5克之次磷酸鈉單水合物、105.8克之己二酸，及391.4克之對苯二甲酸之混合物於2.5公升之高壓釜內攪拌，並且加熱，且蒸餾移除

水。35分鐘後，獲得90重量%之鹽水溶液，同時使溫度從170℃上升至212℃。然後，關閉高壓釜。聚合反應係於212°C至250°C之增加溫度實行25分鐘。混合物於250℃攪拌15分鐘，期間，壓力升至2.8 MPa，其後，高壓釜之內容物被閃蒸，且固體產物於氮氣下進一步冷卻。預聚物其後被乾燥，且以與E-1聚合物相同方式以固相後縮合。然後，聚合物冷卻至室溫。

CE-A聚合物: PA6T/66 (莫耳比例60 / 40)

以如聚合物1般相同之方式，520克之六甲撐基二胺、537克之水、0.36克之次磷酸鈉單水合物、330克之己二酸，及420克之對苯二甲酸之混合物於2.5公升之高壓釜內攪拌，並且加熱，以於27分鐘後獲得91重量%之鹽水溶液。於此方法，溫度從169°C增至223°C。聚合反應係於210°C至226°C之增加溫度實行21分鐘，期間，壓力升至1.3 MPa。預聚物其後被乾燥，且以與E-1聚合物相同方式以固相後縮合。然後，聚合物冷卻至室溫。

CE-B,C 聚合物: PA 46

以如聚合物1般相同之方式，430.4克之四甲撐基二胺、500克之水、0.33克之次磷酸鈉單水合物，及686.8克之己二酸之混合物於2.5公升之高壓釜內攪拌，並且加熱，以於25分鐘後獲得90重量%之鹽水溶液。於此方法，溫度從110°C增至162°C。聚合反應係於162°C至204°C之增加溫度實行，期間，壓力升至1.3 MPa。預聚物其後被乾燥，且以與E-1聚合物相同方式以固相後縮合。然後，聚合物冷卻至

室溫。

比較例CE-F: 製備PA-6T/5T(莫耳比例56/44)

201.4克之五甲撐基二胺、300.8克之六甲撐基二胺、521.1克之水、0.65克之次磷酸鈉單水合物，及722.18克之對苯二甲酸之混合物於2.5公升之高壓釜內攪拌，並且加熱，且蒸餾移除水。27分鐘後，獲得90重量%之鹽水溶液，同時使溫度從170℃上升至211℃。然後，關閉高壓釜。聚合反應係於211°C至250°C之增加溫度實行15分鐘。混合物於250℃攪拌15分鐘，期間，壓力升至2.9 MPa，其後，高壓釜之內容物被閃蒸，且固體產物於氮氣下進一步冷卻。預聚物其後被乾燥，且以與E-3聚合物相同方式以固相後縮合。然後，聚合物冷卻至室溫。

化合物之製備

E-1至E-5、CE-A至C，及CE-F亦包合 下列組份：

・用於聚醯胺之標準玻璃纖維等級；

・阻燃劑：溴化聚苯乙烯(可得自Albermarle 之Saytex® HP3010)；

・阻燃增效劑：硼酸鋅(可得自Luzenac之Firebrake® 500)；及

・包含脫模劑及安定包裝物之輔助添加劑，

比較實驗D及E係以商業產品為基礎：CE-D係Zytel HTNFR52G30BL，DuPont之PA6T/66產品，且CE-E係Genestar GN2332 BK，Kururay 之PA9T產品。傳統分析技術被用以評估用於此等商業產品之溴化聚苯乙烯、增效

劑，及輔助添加劑之比例。Genestar 之PA9T產品之分析顯示聚醯胺組份係由PA8T及PA9T以約20:80莫耳比例組成。

E-1至E-5、CE-A至C及CE-F化合物係於設定為325°C平溫度之Werner & Pfleiderer KSK 4042D擠塑機製備。所有組份被添加至擠塑機之供料口，例外者係玻璃纖維係經由側供料口個別添加至熔融物內。聚合物熔融物係於擠塑機之端部被除氣而成為股材，冷卻，及切成粒狀物。化合及商業上之組成物係顯示於第1表。

射出成型：

上述材料於用於射出成型前藉由施加下列條件而預先乾燥：共聚醯胺於0.02 Mpa之真空下加熱至80°C，於此溫度及壓力維持24小時，同時使氮氣流通過。經預先乾燥之材料於具22 mm螺桿直徑及Campus UL 0.8 mm 2殼體射出成型模具之Arburg 5射出成型機射出成型。機筒溫度設定為345°C，且模具溫度設定為140°C。因而獲得之Campus UL桿材被用於進一步之測試。

第1表：化合物組成

	E-1	E-2	E-3	E-4	E-5	CE-A	CE-B	CE-C	CE-D	CE-E	CE-F
聚合物%	42	37	42	42	42	42	37	42	41	41	42
玻璃纖維	30	40	30	30	30	30	40	30	30	33	30
溴化聚苯乙烯	20	16	20	20	20	20	16	20	24	20	20
增效劑	7	6	7	7	7	7	6	7	4	5	7
輔助添加劑	1	1	1	1	1	1	1	1	1	1	1

測試方法

相對黏度(RV)係於1質量%之甲酸溶液內測定。

螺形流動係於具280 x 15 x 1 mm尺寸之螺旋模穴，於高於半芳香族聚醯胺X之熔融氫度10℃之溫度，於80 Mpa有效注射壓力測定。

藉由DSC之熱 特性分析

熔點(T_m)及玻璃轉移溫度(T_g)係藉由差式掃瞄量熱術(DSC)(2第二操作，10°C/分鐘)依據ASTM D3417-97 E793-85/794-85測定。

E-模量係於23°C及5 mm/分鐘之抗張測試，依據ISO 527而測定。

衝擊測試(凹口-Charpy)係於23°C依據ISO 179/1A測定。

水/濕氣之吸收(吸取)測試：

預先乾燥之樣品(0.8 mm UL桿材)於濕化櫃或具有蒸餾水之容器內，於預定之溫度及濕度程度調節，重量之增加隨時間監測至達到飽和程度為止。於飽和程度之重量增加係以預乾燥樣品之起始重量之百分率計算。

於回流焊接條件下之起泡性能

對於在回流焊接條件下之起泡性能，大數量之預先乾燥樣品於濕化櫃內，於預設之溫度及濕度程度，以與用於上述吸水性測試相同之方式調節。於不同之時間間隔，個別之樣品(10個為一批)自櫃取出，於周圍條件短暫冷卻至室溫，置於回流爐內，且接受應用於回流焊接方法之溫度條件。應用之溫度分佈如下。首先，樣品以平均1.5°C/秒之加熱坡度於80秒後預熱至140°C之溫度，其後，樣品更徐緩地加熱於起始210秒後達160°C之溫度。然後，樣品以約6°C/

秒之起始加熱坡度加熱於220秒後達220°C之溫度，且以2°C /秒之更徐緩之加熱速率於起始290秒後達260°C之溫度而加熱至260°C。其後，樣品於20秒內冷卻至140°C。然後，10個樣品自爐取出，冷卻至室溫，且檢測浮泡之存在。對於在濕化櫃內之每一條節期，顯示浮泡發生之樣品之百分率被分級。具浮泡之樣品之百分率被記錄。

線性熱膨脹系數係依據ISO 11359-1/-2測定。

樣品之介電常數(DAM)係依據IEC 60250以3 Ghz頻率於23°C測定。

樣品之介電強度(DAM)係依據IEC 60243-1測定。

比較痕跡指數係依據IEC 60112測定。

熱變形溫度係依據ISO 75-1/-2以施加1.8 Mpa之載荷量而測定。

所有化合物符合用於0.8 mm測試桿材之UL-94-V0。

結果

實驗結果係呈現於第2表。

如第2表所示，本發明之組成物藉由提供具有改良之於高溫之抗起泡性、尺寸安定性，及機械性質且至少維持傳統組成物之所需的加工處理、電，及阻燃性質之聚醯胺 組成物,，而克服與焊接具傳統聚醯胺組成物之E/E連接器有關之問題。

本發明之組成物已被發現對適於E/E連接器之聚醯胺組成物提供改良之起泡性能。於本發明範圍下之組成物被發現符合JEDEC 2/2a之起泡測試(IPC/JEDEC J-STD-020C

2004年7月)之要求。相反地，任一比較例能符合此產業標準。

若使樣品於85°C及85%相對濕度調節168小時後，於迴流焊接條件後未觀察到起泡，則JEDEC之第2級被達成。

若使樣品於30°C及60%相對濕度調節696小時後，於迴流焊接條件後未觀察到起泡，則JEDEC之第2a級被達成。

比較例中，包含以聚醯胺 9T為主之組成物CE-E記錄最佳之起泡性能，即使仍比本發明範圍內之組成物高得多。此發現基於CE-E之較低吸水性而被預期。事實上，比較例內之起泡結果顯示起泡性能及水份吸取程度間之相關係。

改良之起泡性能經由生產吸收較少水份之更具疏水性之聚醯胺而達成之教示亦出現於US 6,140,459及WO2006/135841，其揭示於包含自包含對苯二甲酸之二羧酸單體及具有10至20個碳原子之脂族二胺衍生之重複單元之聚醯胺組成物(例如，PA10T)之改良之起泡性能。因此，驚人地係與傳統之聚醯胺相比，於本發明範圍下之實施例具有更優之起泡性能，即使其相對較高之吸水性。

為了比較目的，需注意於引述技藝US 6,140,459，起泡係40°C, 95% RH調節96小時且施加最高達250℃之峰值溫度後而測試。於此等測試，PA 6T/66於240°C時已失敗，且PA 6T/D6甚至未通過210°C。

與比較例相反，本發明之組成物展現等向性之行為，如藉由於聚合物流之垂直及平行方向間之線性熱膨脹系數

(CLTE)之較低變化而例示。此低變化性造成較不易翹曲之組件。此性質由於降低組份壁厚度之趨勢而漸增重要性。相似之改良亦於關於模收縮性能觀察到。

相同地，於高溫之硬挺性(藉由載荷下變形之溫度(T_{def})測量)係使薄壁組件能機械性抵抗於焊接處理期間遭遇之高溫環境之增加重要性之因素。本發明之組成物展現改良之於高溫時之硬挺性，與以PA 66/6T及PA 9T為主之組成物之T_m及T_{def}間之約20℃差異相比，組件能抵抗其熔點之11°C內之載荷。

第 2 表 E/E 連接器之聚醯胺組成物之性能特性

	E-1	E-2	E-3	E-4	E-5	CE-A	CE-B	CE-C	CE-D	CE-E	CE-F
CLTE 平行/垂直($x10^{-5}K^{-1}$)	3.0/3.7	3.0/3.1				2.2/5.8	2.5/5.0	2.5/5.4	2.1/6.0	3.0/4.0	
CLTE 垂直-平行($x10^{-5}K^{-1}$)	0.7	0.1				3.6	2.5	2.9	3.9	1.0	
12 小時 85°C/85%之起泡%	0	0							100	100	
48 小時 50°C/95%之起泡%	0	0				100			100	20	
96 小時 85°C/60%之起泡%	0	0	0	20	30		100	100	80	40	100
168 小時 85°C/60%之起泡%	0	20					100	100	100	100	
696 小時 30°C/60%之起泡%	0	0					100	100	80	80	
H_2O 吸取 50°C.95%(重量%)	2.9	2.5				2.3	3.6	4.8	2.8	1.1	
H_2O 吸取(於 H_2O 中)23°C(重量%)	3.8	3.3	4.0	4.8	5.3	3.2	4.5	5.5	3.3	1.0	5.5
熔融溫度 T_m(°C)	318	320	320	311	313	313	295	295	305	305	312
玻璃轉移溫度 T_g(°C)	134	135	126	120	110	100	75	75	90	125	142
變形溫度 T_{def}(°C)	307	309	307	295	297	291	290	290	285	285	282
$T_m - T_{def}$(°C)	11	11	13	16	16	22	5	5	20	20	30
介電強度-DAM(kV/mm)	33	33				36	30	30	37	30	
-70°C/62%RH (kV/mm)	33	33					20	20			
-23°C/100%RH (kV/mm)	25	24					4	4			
介電常數 23°C(3 GHz)	3.4					3.7		4.2	3.8	3.3	
CTI (V)	520	480				520	320	220	520	400	
RV 丸粒/UL 桿材	1.95/1.87	1.95/1.91	2.0/-			2.33/2.41			1.97/1.95		3.2/-
E-mod(GPa)	13.5	16.5				13.0	12	15	12	13	

Charpy 凹口(KJ/m²)											
螺形流動:80MPa(mm)	153	135				127	110	130	153	177	
	14	17				13	12	11	10	14	

【圖式簡單說明】

(無)

【主要元件符號說明】

(無)



十、申請專利範圍：

1. 一種阻燃性聚醯胺組成物，包含含有自脂族二胺及二羧酸衍生之單元之半芳香族聚醯胺(X)、強化劑，及阻燃系統，其中，

a)該二羧酸(A)係由5-65莫耳%之脂族二羧酸及選擇性之非對苯二甲酸之芳香族二羧酸(A1)及35-95莫耳%之對苯二甲酸(A2)之混合物所組成；及

b)該脂族二胺(B)係由10-70莫耳%之具有2-5個C原子之短鏈脂族二胺(B1)及30-90莫耳%之具有至少6個C原子之長鏈脂族二胺(B2)之混合物所組成；

c)該對苯二甲酸(A2)及該長鏈脂族二胺(B2)之混合莫耳量相較於該二羧酸(A)及該脂族二胺(B)之總莫耳量係至少60莫耳 %。

2. 如申請專利範圍第1項之阻燃性聚醯胺組成物，其中，該半芳香族聚醯胺具有多於100°C之Tg，及/或至少295°C之Tm。

3. 如申請專利範圍第1項之阻燃性聚醯胺組成物，具有至少500V之比較痕跡指數(CTI)。

4. 如申請專利範圍第1項之阻燃性聚醯胺組成物，其中，該組成物係由下述組成：

- 25-80重量%之該半芳香族聚醯胺；
- 5-50重量%之該強化劑；
- 1-40重量%之該阻燃系統；及
- 0-25重量%之非該半芳香族聚醯胺之聚合物，

- 0 - 25重量%之無機填料，及/或
- 0 - 5重量%之輔助添加劑，

其中，重量百分率(重量%)係相較於該組成物之總重量。

5. 一種用於電氣連接器之塑料外殼，包含強化聚合物組成物，其包含強化劑及如申請專利範圍第1項之半芳香族聚醯胺X。

6. 如申請專利範圍第5項之塑料外殼，其中，該強化聚合物組成物係如申請專利範圍第1-4項中任一項之阻燃性聚醯胺組成物。

7. 一種用於使電氣或電子應用內之電路連接在一起之電氣連接器，包含一導電元件，及一包埋該導電元件之至少部份之塑料外殼，其係如申請專利範圍第5-6項中任一項之塑料外殼。

8. 如申請專利範圍第7項之電氣連接器，其中，該電氣連接器係I/O連接器、卡座(PCB)連接器、FPC(可撓性印刷電路)連接器、FFC(可撓性箔材電路)連接器、高速連接器、端子台、MID(模組式積體裝置)連接器，或插頭插座式連接器，或其等之組合物。

9. 一種如申請專利範圍第7或8項之電氣連接器之用途，其係用於包含熱焊接步驟之SMT方法。

10. 一種電氣或電子之裝置，包含藉由包含熱焊接步驟之SMT方法安裝之如申請專利範圍第8項之電氣連接器。

Espacenet

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Magnet chatch

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Abstract of TW201105851 (A)

The present invention provides a magnet chatch of which the distance between fixing holes of a pair of bases is adjustable according to pitch size of receptable hole. The magnet chatch comprises a case body for receiving magnet, a pair of bases for fixing the case body to the object to be mounted, the case body and the pair of bases being constructed separately, an adjusting arm for making the bases get into and out of a base-storing chamber from the opening for inserting the base provided in the case body, and a base body with a hole for fixing to the object to be mounted. The inner end of the adjusting arm is provided with a guide slot, and a guide projection to be inserted into the guide slot is provided onto the back cover of the base-storing chamber.; Each sidewall of the base-storing chamber has a pair of engaging tongues which elastically deform in the thickness direction of the sidewall. The base is fixed and maintained to the case body and the distance between the fixing holes of the pair of bases is adjusted by elastically engaging the racks of each engaging tongue with the racks to be engaged on the side surface of the adjusting arm.

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(56)參考文獻：

TW 514001 TW M266449

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審查人員：江國雄

申請專利範圍項數：1 項 圖式數：36 共 0 頁

(54)名稱

電磁吸盤

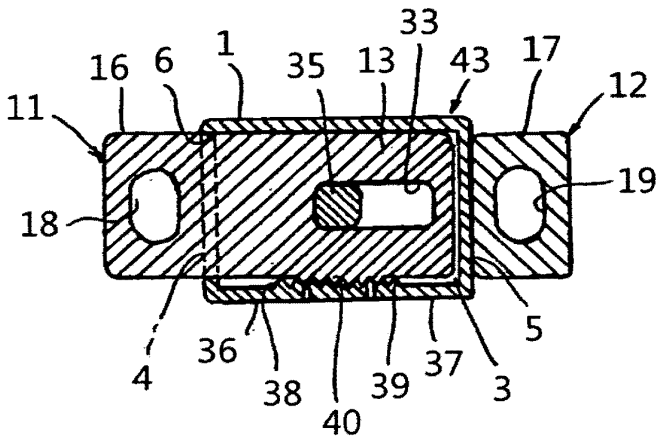
MAGNET CHATCH

(57)摘要

本發明係提供一種電磁吸盤，係與穿通孔之間距尺寸對應，而可廣範圍增減調整一對底座之固設孔間之距離。

本發明之電磁吸盤，係將收容有磁鐵之箱本體、與用以固設前述箱本體於裝設對象物之一對底座分別構成，且以從前述箱本體之底座插入用開口進出於底座收納室之調整用臂與具有用於固設於裝設對象物之固設孔之底座本體來構成前述各底座；在前述各調整用臂之內側端部設置導槽，在前述底座收納室之背蓋板設置用以插入於前述兩導槽之引導突起，在前述底座收納室之其他側壁設置朝該側壁厚度方向彈性變形之一對卡止舌片，藉由使前述各卡止舌片之卡止用齒列彈性卡合於前述各調整用臂之側面部之被卡止用齒列，使前述底座固定保持於前述箱本體，以增減調整前述一對底座之固設孔間之距離。

The present invention provides a magnet chatch of which the distance between fixing holes of a pair of bases is adjustable according to pitch size of receptable hole. The magnet chatch comprises a case body for receiving magnet, a pair of bases for fixing the case body to the object to be mounted, the case body and the pair of bases being constructed separately, an adjusting arm for making the bases get into and out of a base-storing chamber from the opening for inserting the base provided in the case body, and a base body with a hole for fixing to the object to be mounted. The inner end of the adjusting arm is provided with a guide slot, and a guide projection to be inserted into the guide slot is provided onto the back cover of the base-storing chamber. Each sidewall of the base-storing chamber has a pair of engaging tongues which elastically deform in the thickness direction of the sidewall. The base is fixed and maintained to the case body and the distance between the fixing holes of the pair of bases is adjusted by elastically engaging the racks of each engaging tongue with the racks to be engaged on the side surface of the adjusting arm.



第 6 圖

1・・・電磁吸盤之箱本體

3・・・底座收納室

4、5・・・底座收納室之側壁

6・・・底座插入用開口

11、12・・・底座

13・・・調整用臂

16、17・・・底座本體

18・・・用於固設於裝設對象物之固設孔

33・・・調整用臂之導槽

35・・・引導突起

36、37・・・卡止舌片

38、39・・・卡止用齒列

40・・・被卡止用齒列

43・・・電磁吸盤

公告本

發明專利說明書

（本說明書格式、順序，請勿任意更動，※記號部分請勿填寫）

※申請案號：98129503

※申請日：98.9.2　※IPC分類：E05C 19/16 (2006.01)

一、發明名稱：（中文/英文）

電磁吸盤

MAGNET CHATCH

二、中文發明摘要：

本發明係提供一種電磁吸盤，係與穿通孔之間距尺寸對應，而可廣範圍增減調整一對底座之固設孔間之距離。

本發明之電磁吸盤，係將收容有磁鐵之箱本體、與用以固設前述箱本體於裝設對象物之一對底座分別構成，且以從前述箱本體之底座插入用開口進出於底座收納室之調整用臂與具有用於固設於裝設對象物之固設孔之底座本體來構成前述各底座；在前述各調整用臂之內側端部設置導槽，在前述底座收納室之背蓋板設置用以插入於前述兩導槽之引導突起，在前述底座收納室之其他側壁設置朝該側壁厚度方向彈性變形之一對卡止舌片，藉由使前述各卡止舌片之卡止用齒列彈性卡合於前述各調整用臂之側面部之被卡止用齒列，使前述底座固定保持於前述箱本體，以增減調整前述一對底座之固設孔間之距離。

三、英文發明摘要：

The present invention provides a magnet chatch of which the distance between fixing holes of a pair of bases is adjustable according to pitch size of receptable hole. The magnet chatch comprises a case body for receiving magnet, a pair of bases for fixing the case body to the object to be mounted, the case body and the pair of bases being constructed separately, an adjusting arm for making the bases get into and out of a base-storing chamber from the opening for inserting the base provided in the case body, and a base body with a hole for fixing to the object to be mounted. The inner end of the adjusting arm is provided with a guide slot, and a guide projection to be inserted into the guide slot is provided onto the back cover of the base-storing chamber. Each sidewall of the base-storing chamber has a pair of engaging tongues which elastically deform in the thickness direction of the sidewall. The base is fixed and maintained to the case body and the distance between the fixing holes of the pair of bases is adjusted by elastically engaging the racks of each engaging tongue with the racks to be engaged on the side surface of the adjusting arm.

四、指定代表圖：

(一)本案指定代表圖為：第（ 6 ）圖。

(二)本代表圖之元件符號簡單說明：

1	電磁吸盤之箱本體
3	底座收納室
4、5	底座收納室之側壁
6	底座插入用開口
11、12	底座
13	調整用臂
16、17	底座本體
18	用於固設於裝設對象物之固設孔
33	調整用臂之導槽
35	引導突起
36、37	卡止舌片
38、39	卡止用齒列
40	被卡止用齒列
43	電磁吸盤

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

無。

六、發明說明：

【發明所屬之技術領域】

本發明係關於一種在機器之製造現場及使用現場等，藉由磁性吸附而將二個對象物予以連結保持所使用之電磁吸盤。

【先前技術】

習知所使用之電磁吸盤，係在收容有磁鐵之箱本體之左右側面部一體形成底座部，且在該等底座部設有用於裝設對象物的固設孔（參照專利文獻 1）。

在專利文獻 1 之電磁吸盤中，由於左右之底座部無法相對於箱本體移動，因此前述固設孔間之距離係固定不變，當裝設對象物側之穿通孔的間距尺寸與前述固設孔間的距離不一致時，即無法適用在該裝設對象物上。

依裝設對象物側之穿通孔之間距尺寸不同，製作變更前述固設孔間之距離的電磁吸盤，變成少量少樣生產，而使得製作成本高漲。此外，生產前述固設孔間之距離不同之多種類電磁吸盤時，其庫存管理亦變得複雜。

[先前技術文獻]

[專利文獻 1]日本特開 2008-19646 號公報

【發明內容】

[發明所欲解決之課題]

本發明之目的係提供一種電磁吸盤，其可與裝設對象物所設之穿通孔之間距尺寸對應，而廣範圍增減調整一對底座之固設孔間之距離。

[解決問題之方案]

本發明之電磁吸盤，係將收容有磁鐵之箱本體、與用以固設前述箱本體於裝設對象物之一對底座分別構成，且以從前述箱本體之底座插入用開口進出於底座收納室之調整用臂與具有用於固設於裝設對象物之固設孔之底座本體來構成前述各底座；在前述各調整用臂之內側端部設置導槽（guide slot），在前述底座收納室之背蓋板設置用以插入於前述兩導槽之引導突起，在前述底座收納室之其他側壁設置朝該側壁厚度方向彈性變形之一對卡止舌片，藉由使前述各卡止舌片之卡止用齒列彈性卡合於前述各調整用臂之側面部之被卡止用齒列，使前述底座固定保持於前述箱本體，以增減調整前述一對底座之固設孔間之距離。

[發明之功效]

如此，在本發明之電磁吸盤中，係使前述一對底座朝彼此接近或離開之方向滑動，藉此即可在前述調整用臂之導槽之長度與前述背蓋板之引導突起之長度之差分之2倍範圍內，改變前述一對底座相對於前述箱本體之配置位置，再者，藉由使前述底座收納室之其他側壁所設置之一對卡止舌片之卡止用齒列，彈性卡合於前述各調整用臂之側面部之被卡止用齒列，即可使前述一對底座在該變更位置中固定保持於前述箱本體。亦即，依據本發明，可與裝設對象物所設之穿通孔之間距尺寸對應，簡單且確實地增減調整前述一對底座之固設孔間之距離，而可廣泛使用在固設具之穿通孔之間距尺寸不同之各種裝設對象物。

由於可以1種電磁吸盤對應穿通孔間距尺寸不同之多種裝設對象物，因此可進行大量生產節省生產成本，亦可簡化庫存管理。

【實施方式】

在圖示之實施例中，係在以磁通易穿透之合成樹脂形成之箱本體1，相鄰接地設有磁鐵收容室2與底座收納室3，在底座收納室3之左右一對側壁4、5，設有底座插入用開口6、7。將磁鐵8收容於磁鐵收容室2之後，將內蓋板10輕壓入於磁鐵收容室2與底座收納室3間之段差部9，且藉由焊接機（welder）將內蓋板10熔接密封於箱本體1。藉此，此電磁吸盤亦可適用於半導體製造設備之無塵室（clean room）。

左右一對底座11、12係將從底座插入用開口6、7進出於底座收納室3之調整用臂13、14與具有用以固設於裝設對象物15之固設孔18、19之底座本體16、17一體形成者。底座插入用開口6、7係為在矩形之一方之長邊以交錯（offset）狀形成凹部20、21者，而在調整用臂13、14之橫剖面之外周輪廓，係形成有嵌合於凹部20、21之凸部22、23。此外，在左側之底座11之調整用臂13之上面，係與凸部22鄰接形成凹陷部24，且於右側之底座12之調整用臂14之下面，與凸部23鄰接地形成隆起部25，且隆起部25與凹陷部24嵌合。以此等嵌合之綜合作用而言，左右一對底座11、12係緊密組合，在朝左右方向相對滑動之任何位置都不會搖擺。

在底座收納室 3 之背面開口，於背蓋板 26 之前後側面係設有剖面為直角三角形之止回突起 27、28，而與此對應地在底座收納室 3 之前後一對側壁 29、30 之內面，係設有剖面直角三角形之止回凹部 31、32。將背蓋板 26 施加壓力而嵌入於底座收納室 3 之背面開口時，止回突起 27、28 係卡合於止回凹部 31、32，背蓋板 26 係藉此而牢固地固定於箱本體 1。此等直角三角形之止回突起與止回凹部，亦可設於前後左右 4 邊。

在左右一對底座 11、12 之調整用臂 13、14 之內側端部，係設有在該底座之滑動方向較長之導槽 33、34。當將調整用臂 13、14 壓入至底座收納室 3 達最深時，各導槽 33、34 之根部部分係處於重疊之位置關係。在背蓋板 26 之內面之大致中央部，係設有插入於兩導槽 33、34 之引導突起 35。引導突起 35 之前端面，係與右側底座 12 之調整用臂 14 一同抵接於內蓋板 10。背蓋板 26 之主體部內面，係與左側之底座 11 之調整用臂 13 抵接。

在與設有底座插入用開口 6、7 之側壁 4、5 正交之底座收納室 3 之前面側壁 42，係設有左右一對卡止舌片 36、37。卡止舌片 36、37 係呈矩形之 3 邊從側壁 42 之母材切斷之形狀者，且以未切之 1 邊部作為支點朝該側壁 42 之厚度方向彈性變形者。在各卡止舌片 36、37 之前端部內面側，各設有 2 個卡止用齒列 38、39。在各調整用臂 13、14 之側面部，各設有 6 個被卡止用齒列 40、41。此等卡止用齒列 38、39 藉由與被卡止用齒列 40、41 彈性卡合，底座

11、12係牢固地保持於箱本體1。

藉由底座11、12採取接近箱本體1之位置或從箱本體1離開之位置，使底座本體16、17固設於裝設對象物15之固設孔18、19間之距離得變更。

被電磁吸盤43磁性吸附之承座件44，係在將磁性板46收容在由磁通易於穿透之合成樹脂所形成之箱體45之後，將背板47以焊接機熔接而加以密封者。電磁吸盤43係藉由從底座本體16、17之固設孔18、19插入於裝設對象物15之穿通孔48、49之合成樹脂製螺栓-螺帽50、51，緊固固設於裝設對象物15。承座件44係藉由從箱體45之固設孔52、53插入於另一裝設對象物54之穿通孔55、56之合成樹脂製螺栓-螺帽 57、58，而緊固固設於其他裝設對象物54。

【圖式簡單說明】

第1圖係為本發明一實施例之電磁吸盤之前視圖，左右一對底座係處於插入箱本體達最深的狀態。

第2圖係為第1圖之電磁吸盤之平面圖。

第3圖係為第1圖之電磁吸盤之仰視圖。

第4圖係為第1圖之電磁吸盤之左側面圖。

第5圖係為第1圖之電磁吸盤之右側面圖。

第6圖係為第1圖之A-A線剖面圖。

第7圖係為第1圖之B-B線剖面圖。

第8圖係為第2圖之C-C線剖面圖。

第9圖係為第1圖之D-D線剖面圖。

第 10 圖係為與第 1 圖之電磁吸盤組合所使用之承座件之前視圖。

第 11 圖係為第 10 圖之承座件之平面圖。

第 12 圖係為第 10 圖之 E-E 線剖面圖。

第 13 圖係為第 1 圖之電磁吸盤與第 10 圖之承座件之使用狀態前視圖，顯示解除磁性吸附之狀態。

第 14 圖係為使用在第 1 圖之電磁吸盤之箱本體之前視圖。

第 15 圖係為第 14 圖之箱本體之平面圖。

第 16 圖係為第 14 圖之箱本體之左側面圖。

第 17 圖係為第 14 圖之箱本體之右側面圖。

第 18 圖係為第 14 圖之 F-F 線剖面圖。

第 19 圖係為第 16 圖之 G-G 線剖面圖。

第 20 圖係為第 14 圖之 H-H 線剖面圖。

第 21 圖係為第 20 圖之圓形鏈線部分之放大圖。

第 22 圖係為使用在第 1 圖之電磁吸盤之左側底座之前視圖。

第 23 圖係為第 22 圖之底座之背面圖。

第 24 圖係為第 22 圖之底座之平面圖。

第 25 圖係為第 22 圖之底座之仰視圖。

第 26 圖係為第 22 圖之底座之右側面圖。

第 27 圖係為第 22 圖之 I-I 線剖面圖。

第 28 圖係為使用在第 1 圖之電磁吸盤之右側底座之前視圖。

第 29 圖係為第 28 圖之底座之平面圖。

第 30 圖係為第 28 圖之底座之底面圖。

第 31 圖係為第 28 圖之底座之左側面圖。

第 32 圖係為第 28 圖之 J-J 線剖面圖。

第 33 圖係為使用在第 1 圖之電磁吸盤之背蓋板之前視圖。

第 34 圖係為第 33 圖之背蓋板之平面圖。

第 35 圖係為第 33 圖之背蓋板之右側面圖。

第 36 圖係為第 34 圖之 K-K 線剖面圖。

【主要元件符號說明】

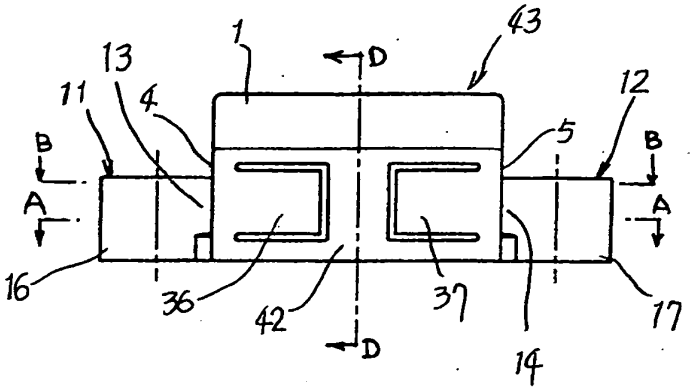
1	電磁吸盤之箱本體
2	磁鐵收容室
3	底座收納室
4、5	底座收納室之側壁
6、7	底座插入用開口
8	磁鐵
9	段差部
10	內蓋板
11、12	底座
13、14	調整用臂
15	電磁吸盤之裝設對象物
16、17	底座本體
18、19	用於固設於裝設對象物之固設孔
20、21	底座插入用開口之凹部

22、23	調整用臂之凸部
24	調整用臂之凹陷部
25	調整用臂之隆起部
26	背蓋板
27、28	背蓋板之止回突起
29、30	底座收納室之側壁
31、32	底座收納室之止回凹部
33、34	調整用臂之導槽
35	引導突起
36、37	卡止舌片
38、39	卡止用齒列
40、41	被卡止用齒列
42	底座收納室之前面側壁
43	電磁吸盤
44	承座件
45	承座件之箱體
46	磁性板
47	承座件之背板
48、49	裝設對象物之穿通孔
50、51、57、58	螺栓-螺帽
52、53	箱體之固設孔
54	其他裝設對象物
55、56	其他裝設對象物之穿通孔

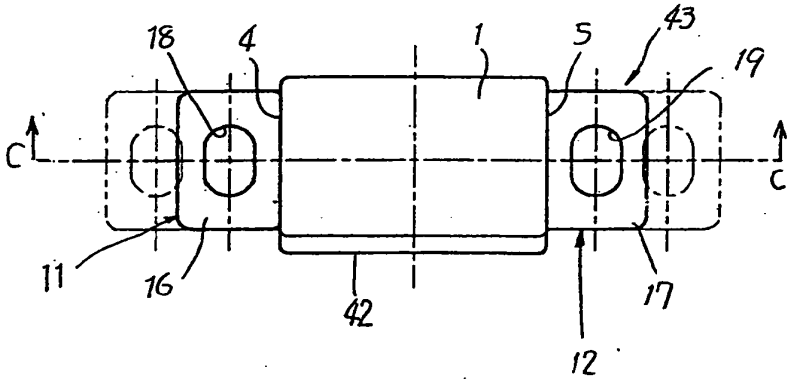
七、申請專利範圍：

1. 一種電磁吸盤，係將收容有磁鐵之箱本體、與用以固設前述箱本體於裝設對象物之一對底座分別構成，且以從前述箱本體之底座插入用開口進出於底座收納室之調整用臂與具有用於固設於裝設對象物之固設孔之底座本體來構成前述各底座本體；在前述各調整用臂之內側端部設置導槽（guide slot），在前述底座收納室之背蓋板設置用以插入於前述兩導槽之引導突起，在前述底座收納室之其他側壁設置朝該側壁厚度方向彈性變形之一對卡止舌片，藉由使前述各卡止舌片之卡止用齒列彈性卡合於前述各調整用臂之側面部之被卡止用齒列，使前述底座固定保持於前述箱本體，以增減調整前述一對底座之固設孔間之距離。

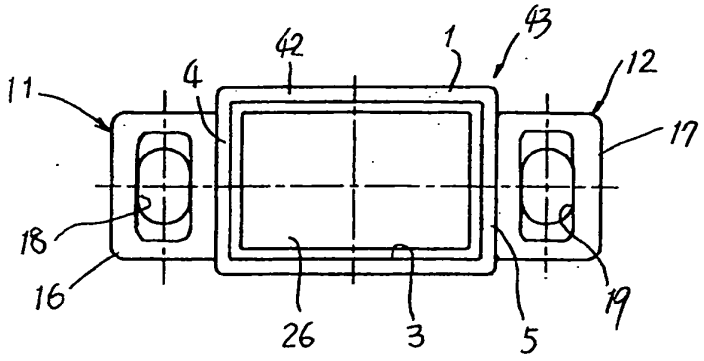
八、圖式：


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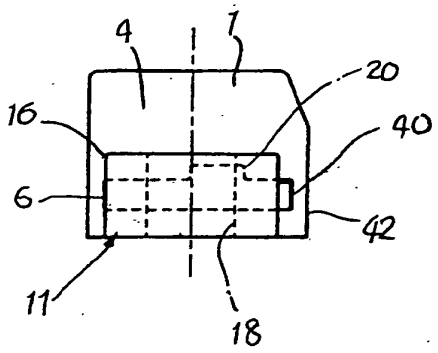
第 1 圖


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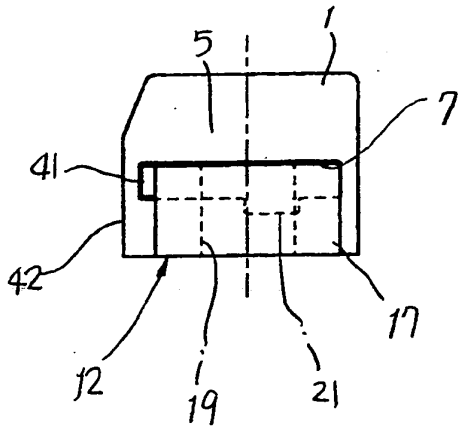
第 2 圖



第 3 圖

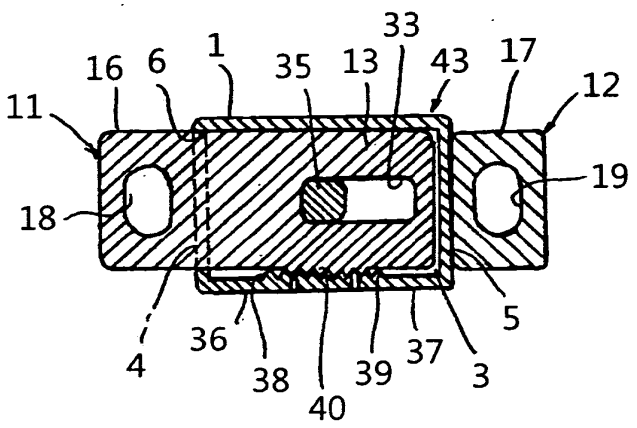


第 4 圖



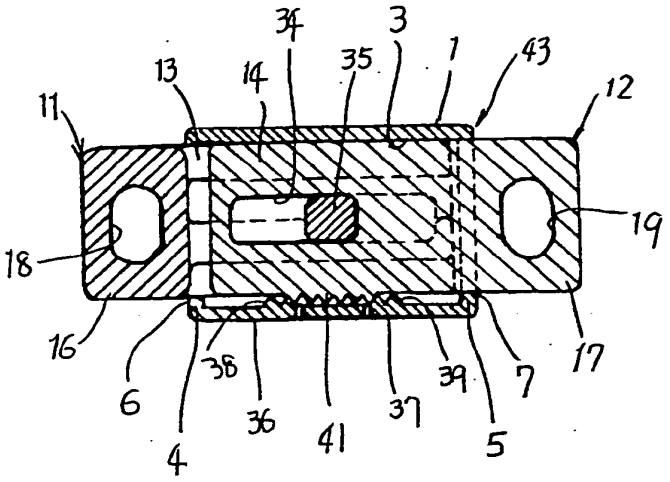
第 5 圖

第 098129503 號專利申請案
102 年 6 月 28 日修正替換頁

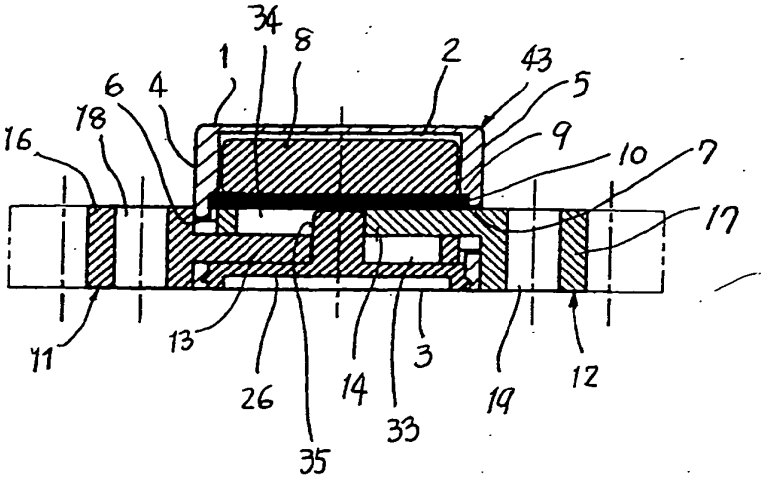


第 6 圖

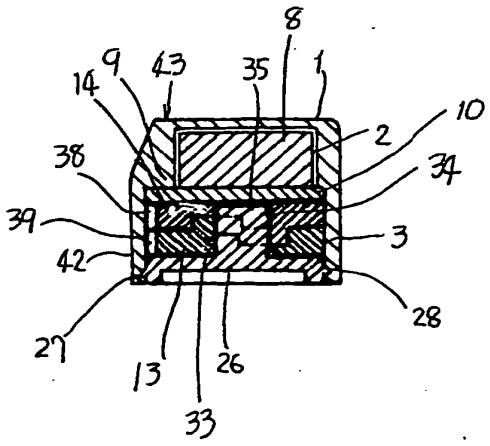
102 6 28
年 月 日修(更)正替換頁



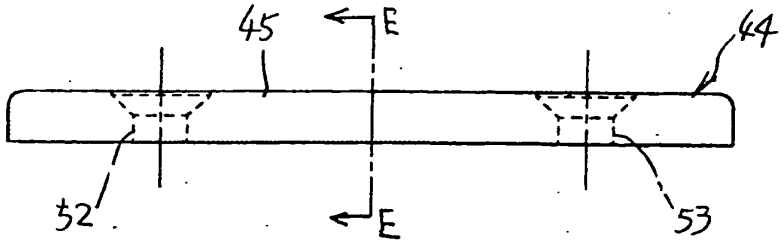
第 7 圖


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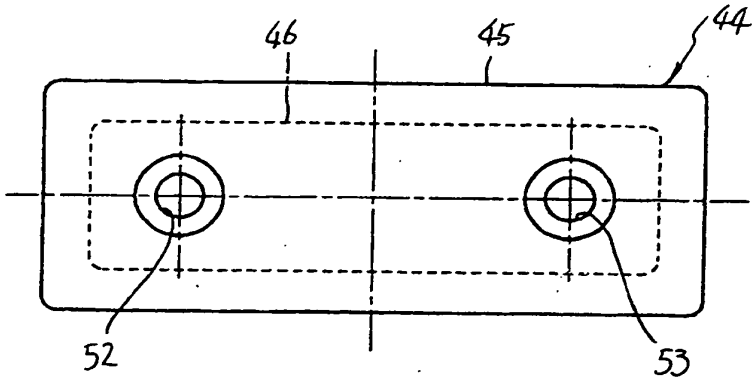
第 8 圖


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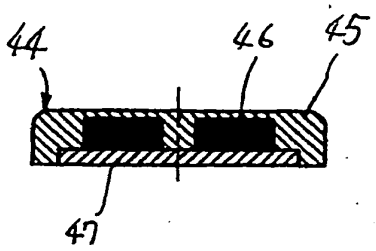
第 9 圖



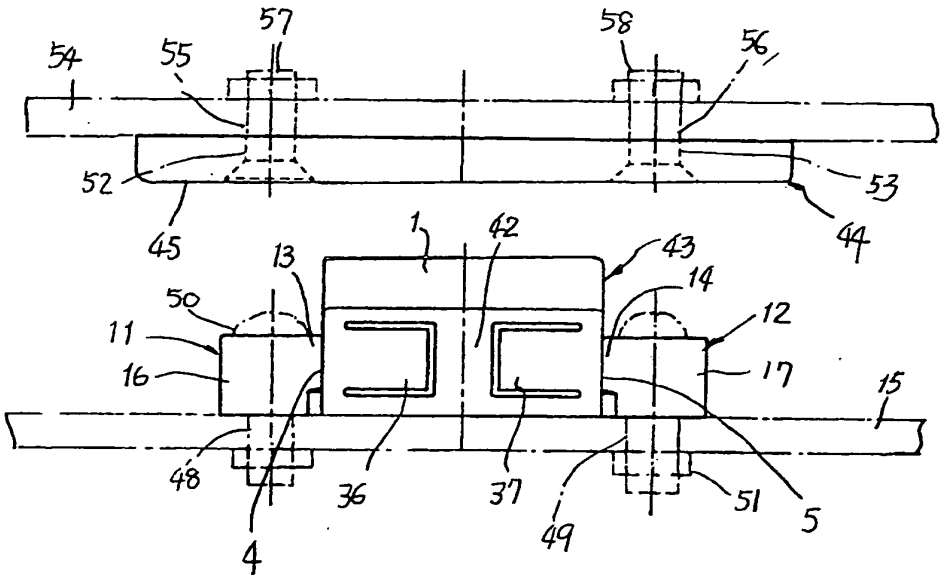
第 10 圖



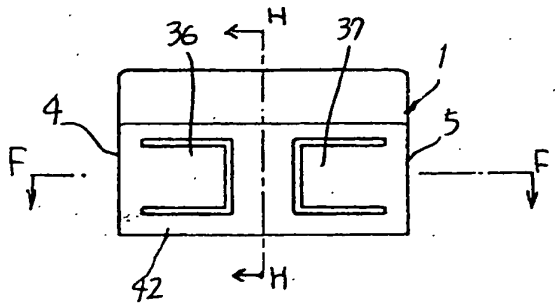
第 11 圖



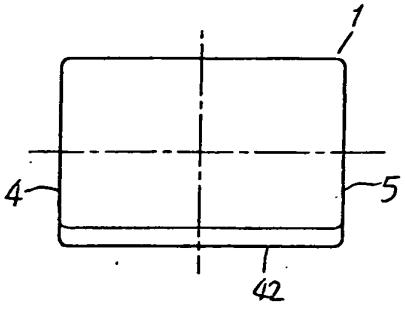
第 12 圖


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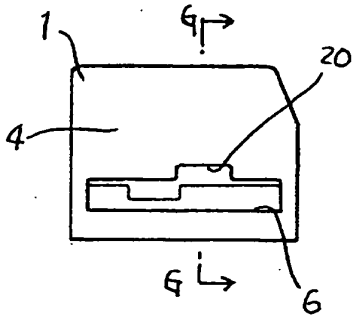
第 13 圖


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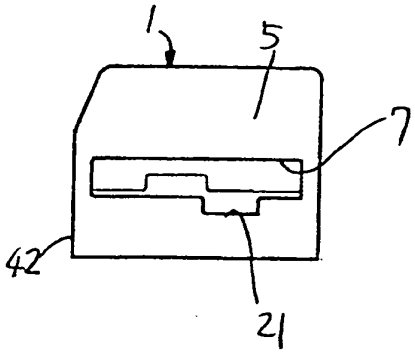
第 14 圖



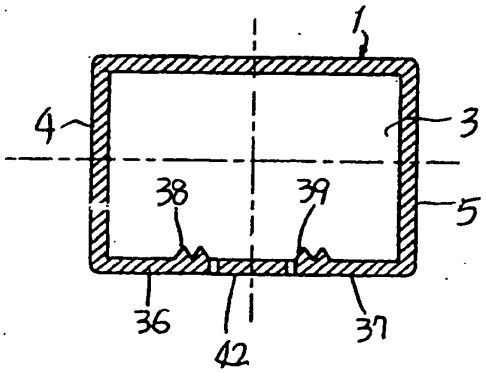
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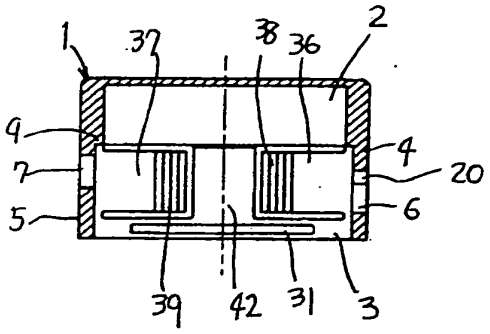
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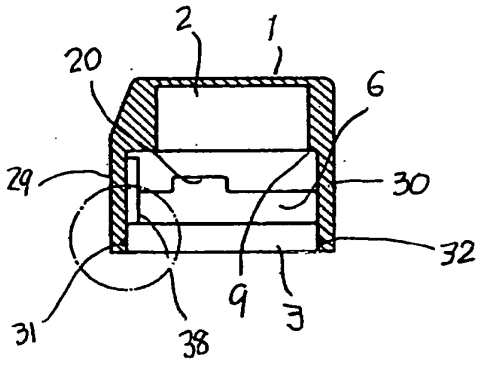
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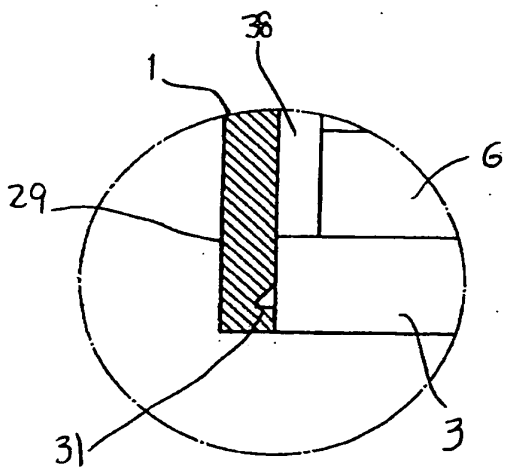
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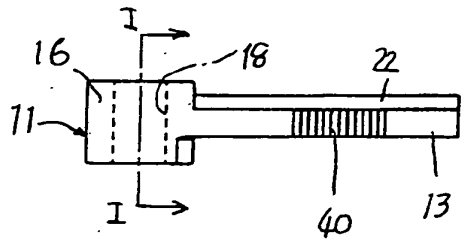
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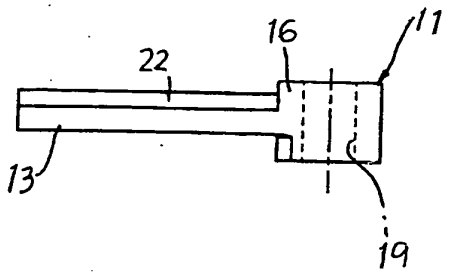
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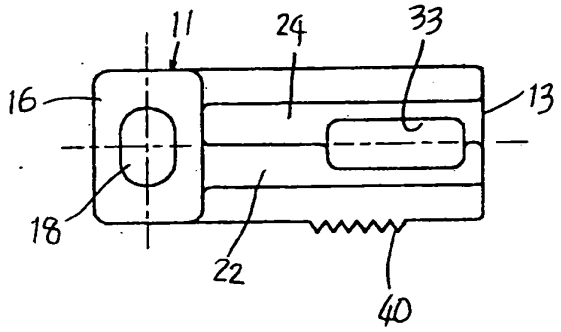
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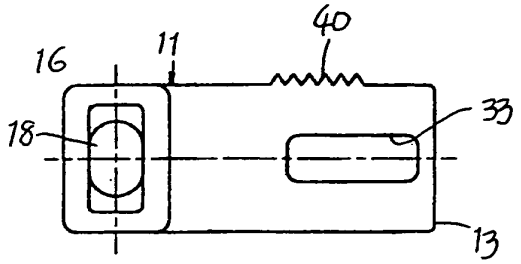
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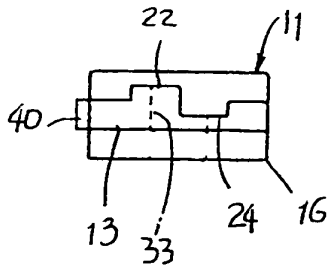
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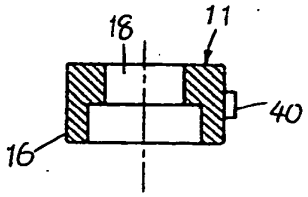
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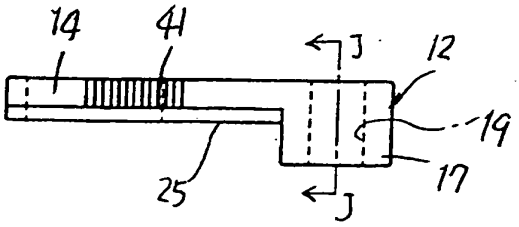
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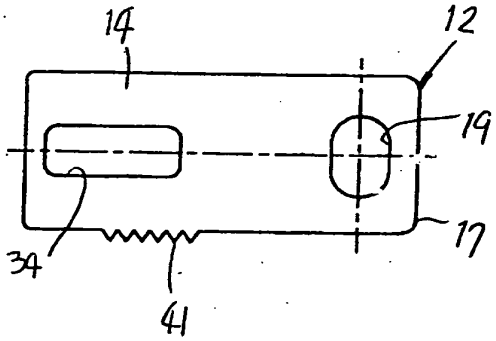
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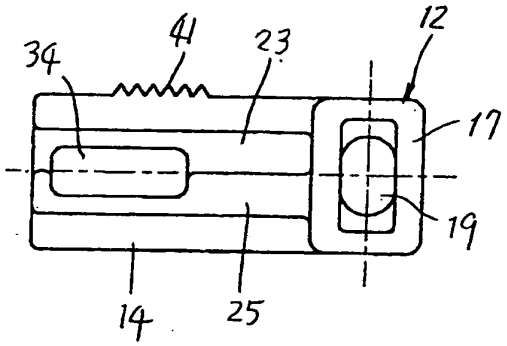
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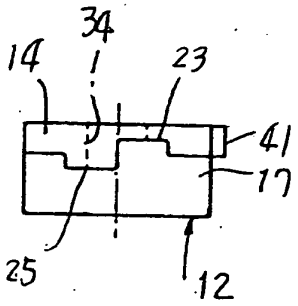
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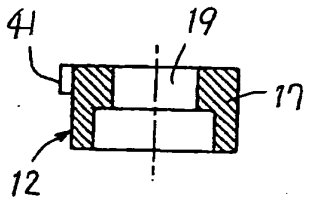
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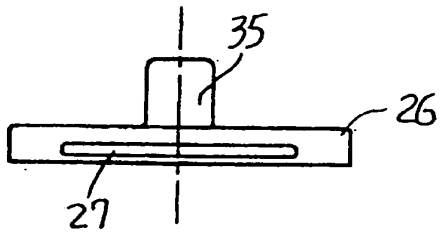
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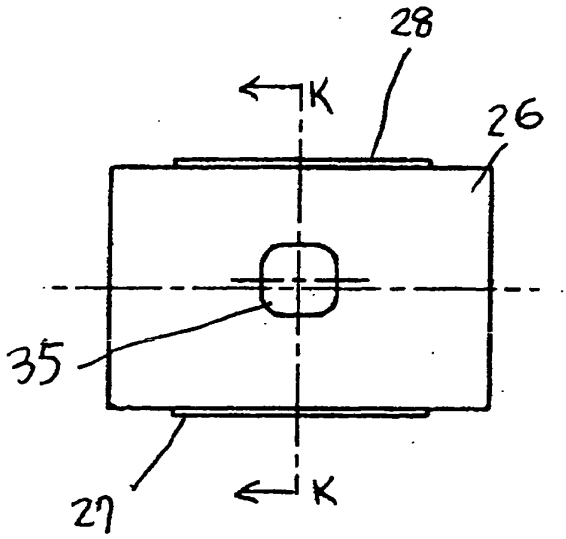
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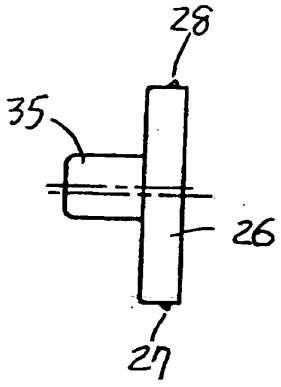
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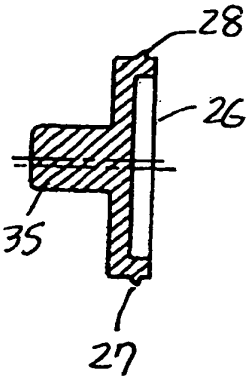
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第 34 圖



第 35 圖



第 36 圖

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jian-Hong ZENG
Filer:	James Lynn O'Sullivan/Anny TENG
Attorney Docket Number:	TWT04774/US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
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UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	4	80	320
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	1920

Electronic Acknowledgement Receipt	
EFS ID:	27123323
Application Number:	15286542
International Application Number:	
Confirmation Number:	1984
Title of Invention:	POWER CONVERTER AND METHOD FOR MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jian-Hong ZENG
Customer Number:	60589
Filer:	James Lynn O'Sullivan
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Payment information:

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Payment Type	DA
Payment was successfully received in RAM	$1920
RAM confirmation Number	100616INTEFSW00006784504669
Deposit Account	504669
Authorized User	James O'Sullivan
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Warnings:					
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2	Oath or Declaration filed	TWT04774US-Declaration.pdf	7931693 ced8ccab794888e3c55802a7512d5e26e95d8320	no	5
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3	Application Data Sheet	TWT04774US-ADS.pdf	1823181 86fd626e9cc9bef5d52dec6432d74a5109af04d5	no	9
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4		TWT04774US-spec.pdf	5601901 dc48d095701895081effcb4ecd67ec32560902fd	yes	38

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	31
Claims	32	37
Abstract	38	38

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5	Drawings-only black and white line drawings	TWT04774US-figs.pdf	1937423 f14b17caa8cb993e4a368000b85117d8439faf3e	no	20

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6	Transmittal Letter	TWT04774US-IDSLetter.pdf	429006 54e07108e7e399254f061fa9ca38789c59b8eee9	no	3
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7	Information Disclosure Statement (IDS) Form (SB08)	TWT04774US-IDSForm.pdf	1035121 a7b2e70c60ca26bff33e4484149e748526494015	no	4
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.