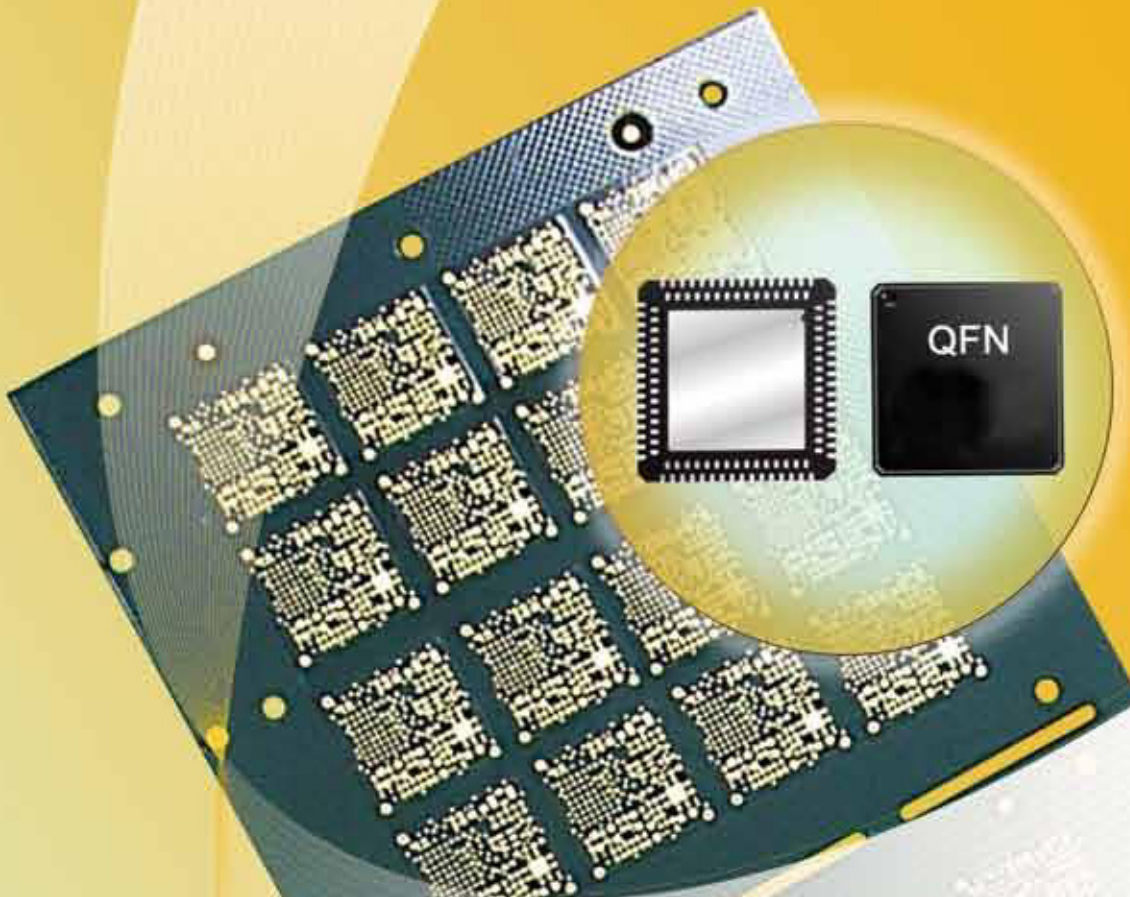


# IPC-7093

## Design and Assembly Process Implementation for Bottom Termination Components

March 2011



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# **Design and Assembly Process Implementation for Bottom Termination SMT Components**

Developed by the IPC Bottom Termination Components (BTC) Task Group (5-21h) of the Assembly & Joining Processes Committee (5-20) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

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## Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the IPC Bottom Termination Components (BTC) Task Group (5-21h) of the Assembly & Joining Processes Committee (5-20) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of IPC extend their gratitude.

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| Zhen Feng, Flextronics                                     | Murad Kurwa, Flextronics International                                                                      | Bill Werner, Trimble Navigation                                         |
| Joe Fjelstad, Verdant Electronics                          | Paul Lotosky, Cookson Electronics                                                                           | Robert Wettermann, BEST Inc.                                            |
| Mark Fulcher, Continental Automotive Systems               | Todd MacFadden, Bose Corporation                                                                            | Dewey Whittaker, Honeywell Inc. Air Transport Systems                   |
| Lionel Fullwood, WKK Distribution Ltd.                     | Brian Madsen, Continental Automotive Systems                                                                | Ian Williams, Intel Corporation                                         |
| Ava Fung, Trimble Navigation                               | Kelly Miller, SigmaPoint Technologies Inc.                                                                  | Bob Willis, The SMART Group                                             |
| Thomas Gardeski, Gemini Sciences                           | David Nelson, Adtran Inc.                                                                                   | Linda Woody, Lockheed Martin Missile & Fire Control                     |
| David Geiger, Flextronics International                    | Jack Olson, Caterpillar Inc.                                                                                | Dongji Xie, Flextronics International                                   |
|                                                            | Richard Otte, PROMEX Industries, Inc.                                                                       |                                                                         |

**A special note of thanks goes to the following individuals for their dedication to bringing this project to fruition. We would like to highlight those individuals who made major contributions to the development of this standard.**

|                                                |                                                    |                                                     |
|------------------------------------------------|----------------------------------------------------|-----------------------------------------------------|
| Dudi Amir, Intel Corporation                   | Bruce Hughes, U.S. Army Aviation & Missile Command | Jeff Shubrooks, Raytheon Company                    |
| Richard Arnold, Continental Automotive Systems | David Nelson, Adtran                               | Vern Solberg, Solberg Technical Consulting          |
| Raiyomand Aspandiar, Intel Corporation         | Dick Otte, Promex                                  | Kris Troxel, Hewlett Packard                        |
| Scott Butters, Intel Corporation               | Ray Prasad, Ray Prasad Consultancy Group           | Bill Werner, Trimble Navigation                     |
| Beverley Christian, Research In Motion Limited | Stan Rak, Continental Automotive Systems           | Robert Wettermann, BEST Inc.                        |
| Werner Engelmaier, Engelmaier Associates       | Robert Rowland, RadiSys                            | Bob Willis, The SMART Group                         |
| David Hillman, Rockwell Collins                |                                                    | Linda Woody, Lockheed Martin Missile & Fire Control |

#### **Illustrations courtesy of the following:**

Amkor Technologies: Figures 3-5, 3-6, 3-7, 4-28, 4-29, 4-35, 6-8, 6-16, 6-17, 6-21, 6-22, 6-23, 8-1, 8-2, 8-3, 8-5, Table 4-7

Analog Devices: Figures 4-40, 4-42, 6-4, 6-8, 6-11, 6-14, 7-24, 7-27, 7-28, Table 4-9

BEST Inc.: Figures 7-28, 7-33, 7-34, 7-35

Continental Automotive Systems: Figures 7-19, 7-20, 7-21, 7-22

Fairchild Semiconductor: Figure 4-36

Intersil: Figure 4-37

Intel Corporation: Figures 9-3, 9-4, 9-10, 9-11, 9-12, 9-19, 9-20, 9-21, 9-27, 9-28

JEDEC: Figures 4-6, 4-7, 4-8, 4-12, 4-13, 4-17, 4-18, 4-20, 4-21, 4-38, 4-39, 4-43

Martin GmbH: Figure 7-32

Mini Micro Stencil: Figure 7-29

National Semiconductor: Figures 4-41, 6-3, 6-9, 7-1, 7-2, 7-3, 7-10, 7-11, 7-15

QPL Group: Figure 6-2

Raytheon Co.: Figure 7-14, 7-18

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# Design and Assembly Process Implementation for Bottom Termination Components

## 1 SCOPE

This document describes the design and assembly challenges for implementing Bottom Termination surface mount Components (BTCs) whose external connections consist of metallized terminations that are an integral part of the component body. Throughout this document the word “BTC” can mean all types and forms of bottom only termination components intended for surface-mounting. This includes such industry descriptive nomenclature as QFN, DFN, SON, LGA, MLP, and MLF, which utilize surface to surface interconnections. The focus of the information contained herein is on critical design, assembly, inspection, repair, and reliability issues associated with BTCs.

**1.1 Purpose** The target audiences for this document are managers, design and process engineers, and operators and technicians who deal with the electronic design, assembly, inspection, and repair processes. The intent is to provide useful and practical information to those companies who are using or considering tin/lead, lead-free, adhesives or other forms of interconnection processes for assembly of BTC type components.

**1.2 Intent** This document, although not a complete recipe, identifies many of the characteristics that influence the successful implementation of robust and reliable assembly processes and provides guidance information to component suppliers regarding the issues being faced in the assembly process. The exchange of information between the component supplier, product designer, and assembly personnel about those parameters that influence good assembly practices are more critical with BTC implementation than with many other surface mount parts.

## 2 APPLICABLE DOCUMENTS

### 2.1 IPC<sup>1</sup>

**IPC-T-50** Terms and Definitions for Interconnecting and Packaging Electronic Circuits

**IPC-CH-65** Guidelines for Cleaning of Printed Boards and Assemblies

**IPC-D-279** Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

**IPC-A-610** Acceptability of Electronic Assemblies

**IPC-SM-785** Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

**IPC-1756** Manufacturing Process Data Management

**IPC-2226** Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

**IPC-4101** Specification for Base Materials for Rigid and Multilayer Printed Boards

**IPC-4761** Design Guide for Protection of Printed Board Via Structures

**IPC-6012** Qualification and Performance Specification for Rigid Printed Boards

**IPC-7351** Generic Requirements for Surface Mount Design and Land Pattern Standard

**IPC-7525** Stencil Design Guidelines

**IPC-7526** Stencil and Misprinted Board Cleaning Handbook

**IPC-9201** Surface Insulation Resistance Handbook

**IPC-9701** Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

**J-STD-001** Requirements for Soldered Electrical and Electronic Assemblies

**J-STD-002** Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

**J-STD-005** Requirements for Soldering Pastes

**J-STD-020** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

**J-STD-033** Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

<sup>1</sup> . [www.ipc.org](http://www.ipc.org)

## 2.2 JEDEC<sup>2</sup>

**JEDEC Publication 95** JEDEC Design Standard, Design Requirements for Outlines of Solid State and Related Products Design Guide: 4.8, Plastic Quad and Dual Inline Square and Rectangular No Lead Packages (With Optional Thermal Enhancements) (QFN/SON) Date: September 2006, Issue: C

**JEDEC Publication 95** JEDEC Design Standard, Design Requirements for Outlines of Solid State and Related Products Design Guide: 4.19, Quad No-Lead Staggered and Inline Multi-Row Packages (With Optional Thermal Enhancements) (QFN) Date: May 2007, Issue: D

**JEDEC Publication 95** JEDEC Design Standard, Design Requirements for Outlines of Solid State and Related Products Design Guide: 4.20, Small Scale Plastic Quad and Dual InLine Square and Rectangular No-Lead Packages (With Optional Thermal Enhancements) (QFN/SON) Date: September 2009, Issue: D.01

**JEDEC Publication 95** JEDEC Design Standard, Design Requirements For Outlines of Solid State and Related Products Design Guide: 4.23, Punch-Singulated Fine Pitch Square Very Thin and Very-Very Thin Profile, Leadframe-Based Quad No-Lead Staggered Dual-Row Packages (with Optional Thermal Enhancements) Date: November 2005

## 3 SELECTION CRITERIA AND MANAGING BTC IMPLEMENTATION

This section provides a high level overview of the entire document. It is the executive summary of the usage and implementation of BTC parts in the electronic assembly. For technical details on BTC design, assembly and reliability issues, refer to the sections related to those topics.

**3.1 Terms and Definitions** Terms and definitions used herein are in accordance with IPC-T-50 except as otherwise specified. Any definition denoted with an asterisk (\*) is a reprint of the term defined in IPC-T-50.

**3.1.1 Bottom Termination Components (BTC)** Surface mountable electronic components whose external connections consist of metallized terminations that are an integral part of the component body. The terminology BTC includes such industry descriptive nomenclature as QFN, DFN, SON, LGA, MLP, and MLF, which utilize surface to surface interconnections.

**3.1.2 Component Mounting Site** The location on a printed board or mounting structure that consists of a land pattern and conductor fan-out to additional circuit features such as lands for testing or vias that are associated with the mounting of a single component.

**3.1.3 Conductive Pattern\*** The configuration or design of the conductive material on a base material. (This includes traces, lands, vias, planes, and passive components when these are an integral part of the printed board manufacturing process.)

**3.1.4 Land Pattern\*** A combination of lands that is used for the mounting, interconnection and testing of a particular component.

**3.1.5 Mixed Component-Mounting Technology\*** A component mounting technology that uses both through-hole and surface-mounting technologies on the same packaging and interconnecting structure.

**3.1.6 Printed Board Assembly** The generic term for an assembly that uses a printed board for component mounting and interconnecting purposes.

**3.1.7 Surface Mounting Technology (SMT)\*** The electrical connection of components to the surface of a conductive pattern that does not utilize component holes.

**3.2 BTC Executive Summary** The term BTC represents industry descriptive package names such as DFN (Dual Flat No-lead), QFN (Quad Flat No-Lead package), LGA (Land Grid Array), SON (Small Outline No-Lead – leads on two sides), PQFN (Plastic Quad Flat No-Lead), MLFP (Micro Leadframe Plastic Package), and MLP (Micro Leadframe Package) etc. They are in some ways similar to BGAs which also have hidden terminations, but they are also very different. They do not have spheres but rather metallized terminations or pads underneath the package.

When implementing BTCs into an electronic assembly, one must keep in mind that these parts are not the only components that must be mounted on the interconnection product board. The board will have other packages such as BGAs, fine pitch and even some through-hole components, and those components may have their own unique design and assembly implementation requirements.

There are two key issues in BTCs: providing the appropriate amount of solder paste and ensuring solder joint reliability. This entire document is essentially dealing with these two issues in various design and assembly sections. Other variables such as surface finish, stencil selection, thermal profile are also discussed and may not be different because of BTCs. Since there is no protruding lead on the package, reliability of the solder joint is essentially controlled by solder joint area and height. Lower paste volume can reduce floating and voids but increases the risk of solder opens so a balance is required to ensure overall solder joint reliability.

2 . [www.jedec.org](http://www.jedec.org)

Most, but not all, BTC packages have an exposed Die Attach Pad (DAP) feature on the package bottom to provide a thermal interface with the mating circuit board surface. When it comes to inspection, they pose even more challenge than Ball Grid Arrays (BGAs) which allow inspection by endoscopes. One may not be able to see side solder fillets and even when they are seen on BTCs with cut metal leadframes, they may look non-wetted or dewetted. If plating is on the side metal, dewetted and non-wetted side fillets on BTCs may indicate solder bonding problems. Examples of BTC components covered in this section are shown in Figures 3-1 to 3-4.

- a) General types: Discrete components (diodes, transistors, inductors etc.) – some DFNs as shown in Figure 3-1.
- b) Quad Flat No Lead (QFN): Component part with I/O (input/output) on four sides as shown in Figure 3-2.
- c) Small Outline No Lead (SON): Component part with I/O on two sides (includes some DFNs) as shown in Figure 3-3.
- d) Land Grid Array (LGA): Component part with I/O in rows and columns [structured or random] as shown in Figure 3-4.

The basic driver for BTCs is the cost. It is a package with the lowest per pin cost, as low as half a cent per pin. To put this in a proper perspective, if a package costs less than one cent per pin, it is considered a very low cost package. So BTCs become an ideal package especially in high volume applications such as cell phones or other mobile products.

Although many select BTC packaging for its favorable cost factor, the package family has become widely used for semiconductors requiring electrical performance and improved thermal management. Assembly processing, however, will require a careful attention to process control from solder material selection, deposition, package placement and solder reflow profile. In regard to the mounting structure, the PCB must exhibit minimal warp and the land patterns for BTC attachment must provide a uniform surface finish.

Because there are no protruding leads, BTCs have proved to exhibit minimal parasitic losses due to their very low electrical resistance and capacitance, and heat transfer from the package to the PCBs is excellent due to their large thermal pad in direct contact with PCB.

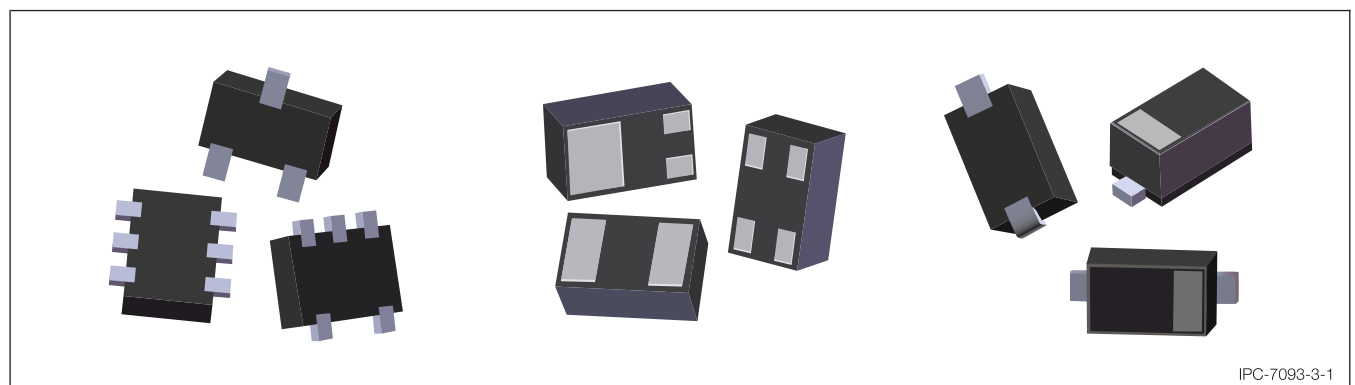
In order to ensure a robust package-to-PCB interface, solder paste deposition must be tightly controlled. Excessive or unevenly deposited solder paste volume may cause the package to float, resulting in poor land pattern alignment, random solder bridging, voiding and opens.

Too little solder volume may compromise product reliability. Even minimal warping in the package or PCB can result in solder joint opens. Because the terminal features may not protrude beyond the package body, visual inspection and uncompromised verification of the solder interface will be difficult.

### 3.3 Description of Different Component Structures

Surface mount components with bottom only terminations are becoming more and more prevalent and there are many types of bottom only termination components that go by various names. Unlike the more traditional leadframe packaged semiconductors with protruding leads, the BTC devices are furnished with flat pads or terminations on the bottom of the package. Those terminations are provided on only two sides or on all four sides of the package in single or multiple rows. The Bottom Termination Component task group has decided to use a common name for all these package types since they require a common approach of design and assembly. That common name is BTC or Bottom Termination surface mount Component to represent all of these packages in this document.

The BTC packages are leadless, near Chip Scale Package (CSP) size with low profile (1.0 mm and less), excellent thermal dissipation and good electrical performance. Typical BTCs have solderable terminations that are flush with the bottom of the device. These devices can also have smaller solderable termination areas located along the perimeter sides or flanks of the package near the bottom of the device.



IPC-7093-3-1

**Figure 3-1 Discrete General Types of Bottom-Only Terminations**

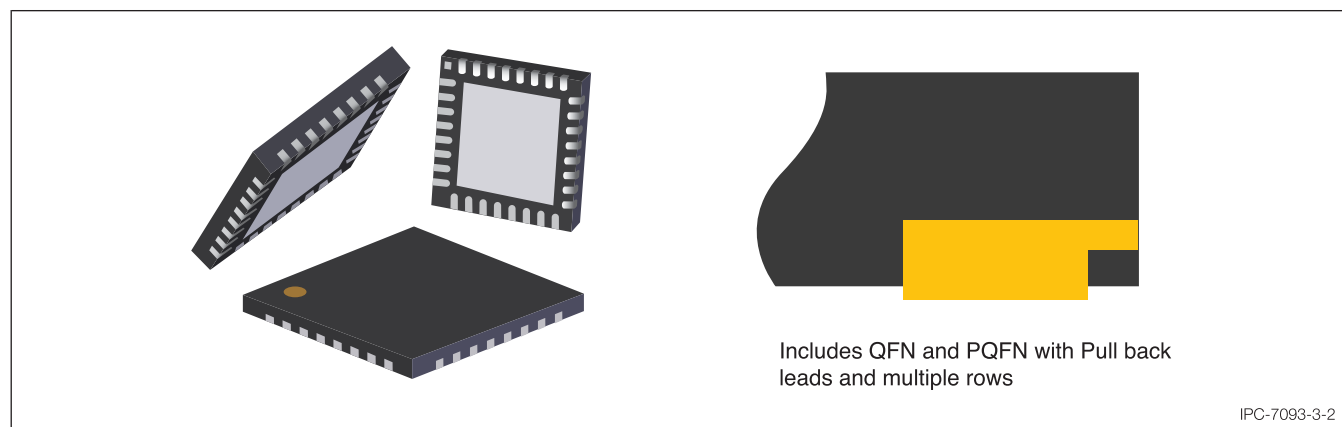


**Figure 3-2 Quad Flat No Lead Type Bottom-Only Terminations**

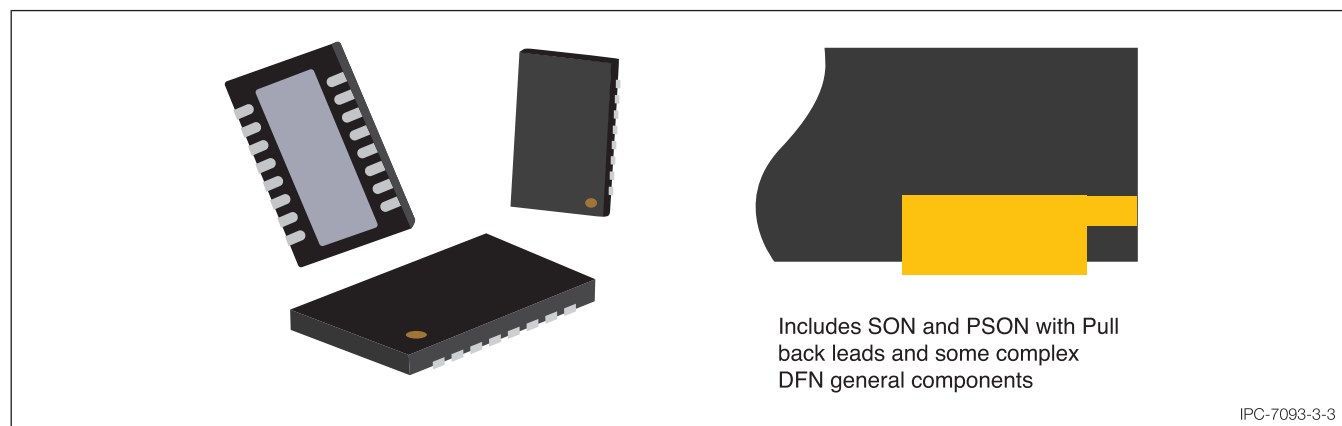


**Figure 3-3 Small Outline No Lead Type Bottom-Only Terminations**

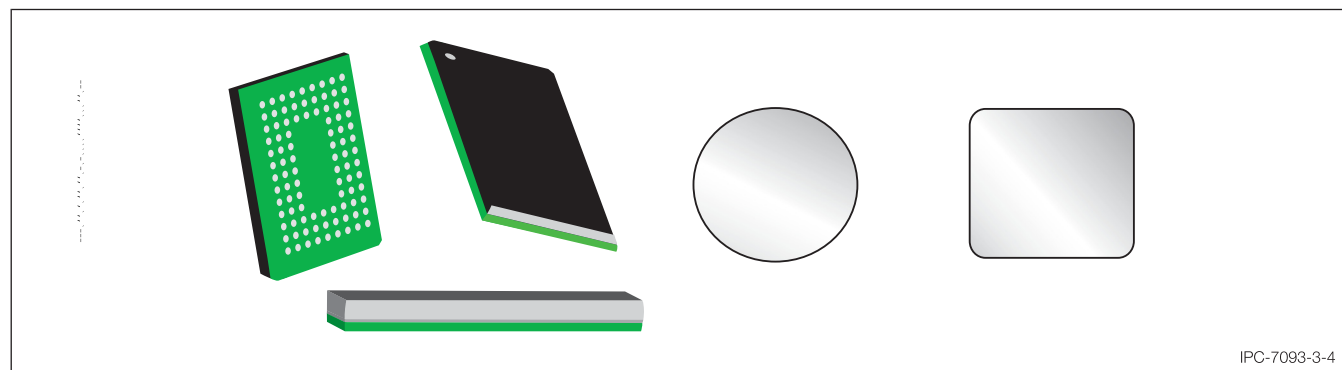


**Figure 3-4 Land Grid Array Type Bottom-Only Terminations**

One of the primary benefits provided by the BTC package is a very low profile. This is a key requirement for newer generations of portable, wireless and handheld electronic products where both weight and package thickness must be minimized. This trend reduces the semiconductor package outlines and profile for portable handheld devices.

The contact pitch for BTC packages is generally 1.0 mm or less and the packages tend to be smaller in size. The body outline dimensions can be as small as 2.0 mm x 2.0 mm or as large as 12.0 mm x 12.0 mm. Due to finer contact pitch variations this package is able to accommodate a die element that is nearly the same size as the package

Traditional gull-wing leaded packages have very good long solder joint reliability life compared to leadless components of the same size, since they have very flexible leads. The BTC packages, on the other hand, are not compliant and may exhibit a relatively shorter solder joint life when subjected to operation in harsh environments. This is because they do not have leads that can take up stresses and strains introduced by differing coefficients of thermal expansion between the package and the substrate.

Many of the BTC packages are furnished with a copper leadframe substrate and offer a thermal enhancement by exposing the die attach pad on the bottom of the package

surface. The die-attach pad provides an efficient heat path when soldered directly to the board. This enhancement also enables stable ground interface by use of down bonds or by electrical connection through a conductive die attach material. But such thermal pads have the potential for large voids and may even lead to the package floating if solder paste volume is not tightly controlled.

The BTC package comes in two formats: punch singulated and saw singulated. While punch singulated packages are individually punched from molded strip during final assembly, saw singulated packages are assembled in array format and separated into individual components during the final sawing operation. See Figure 3–5. Both singulation methods can leave the terminal edges without a wettable surface finish.

The saw singulated package is further divided into two options: Full Lead package, and Lead Pullback package. While the full lead package has the whole thickness of the lead exposed on the package sides, the lead pullback package has a bottom half etch leadframe, resulting in only

the top half of the lead thickness exposed to the sides of the package. Figure 3–6 shows the differences in these package configurations.

One of the biggest benefits of the BTC packages is their thickness. In mobile applications such as the cell phone, palm top and laptop, weight and thickness of the device becomes even more important. BTC packages allow much thinner devices than possible when using other types of surface mount components. Figure 3–7 shows relative package thickness of various component packages. The MLF package is much thinner than traditional SMT packages.

While the lack of traditional leads or balls allows lower package thickness and better electrical and thermal performance, the low standoff height makes it difficult to remove any trapped flux residues that remain in and around the solder joints. And if the flux is active, the corrosion potential is increased. Also, it is necessary that the package and PCB be very flat to achieve good interconnection; otherwise, the potential for opens in solder joints is increased. And since

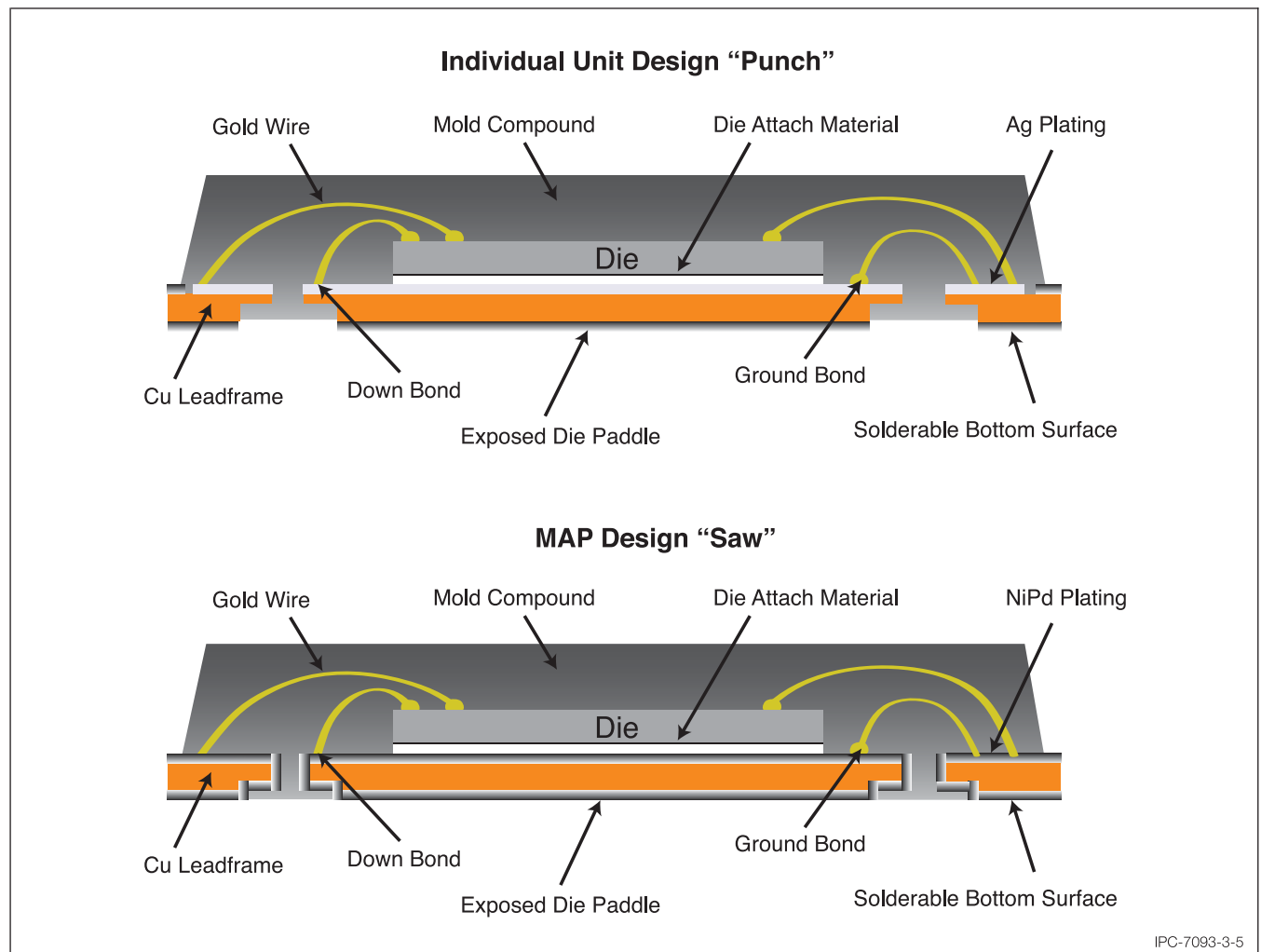


**Figure 3-5 Typical QFN Cross-Section**

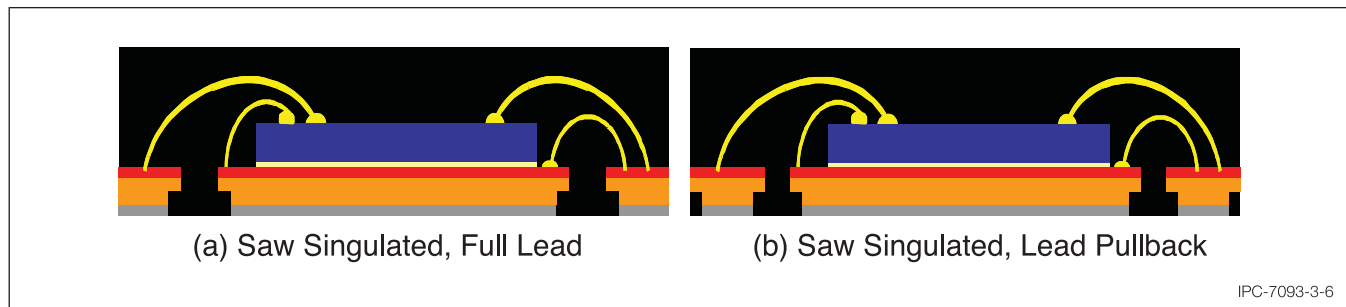


Figure 3-6 Saw Singulated (a, b) BTC Package

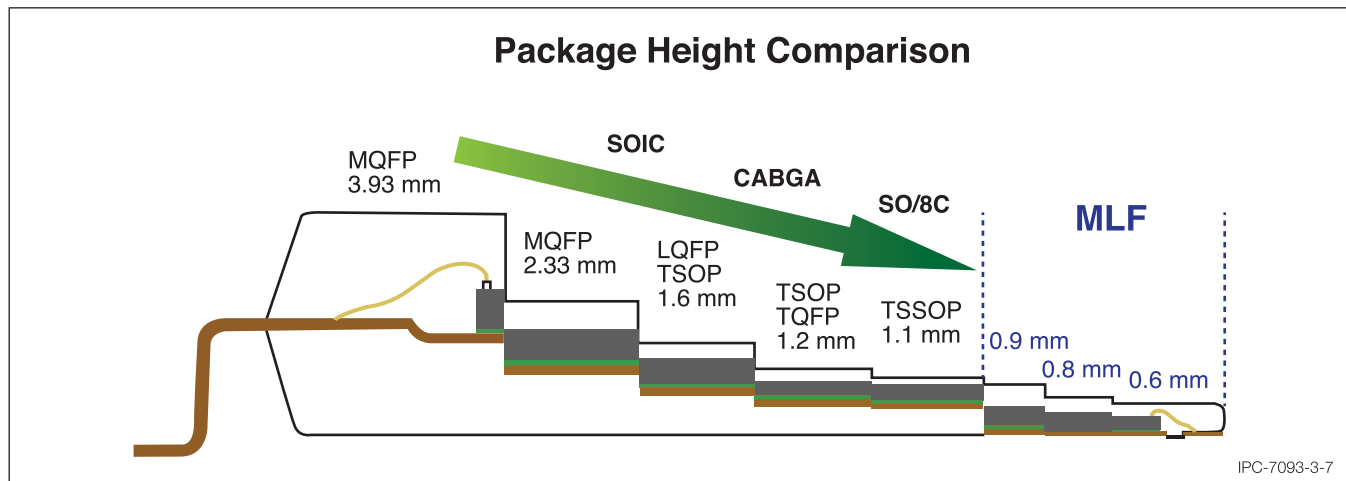


Figure 3-7 MLF Package Thickness When Compared to Other Types of Packages

the standoff height is very low, solder joint reliability may be a concern in harsher environments.

**3.4 Total Cost of Ownership** Low package cost is a key driver for widespread use of BTCs. However, the low package cost may not immediately translate into overall low assembly cost since this package presents many challenges in assembly, inspection, and rework.

In practical reality, the total cost of the final assembly is often greatly impacted by decisions made early in the design process. Too often accounting systems track “cost in the door” but fail to track “cost out the door”. Purchasing is measured and rewarded by identifying and procuring at the lowest price, without understanding and fully appreciating the impact on the manufacturing process and long term reliability of the product and the implied cost of failures. Thus it is incumbent on management to prudently consider and decide on the amount of effort to devote to “up front” engineering, including component selection or package design, solder joint design, board design, and design verification. Management must also understand and appreciate the true piece part cost which is comprised of several elements including the cost of components, incoming inspection, assembly, test, and final inspection. The decisions made will directly impact product reliability. Table 3–1 below lists the key components of Total Cost of Ownership.

### 3.5 Design and Assembly Process Considerations for QFN Type BTC Packages

Land pattern design and stencil designs are the key tools to prevent potentials for opens and shorts in the same package. Since some BTCs require wide lands for power/ground pins and narrow lands for signals, it may be necessary to increase the stencil aperture for signal pins to prevent opens but at the same time make the stencil apertures much smaller than the power and ground pads to prevent squeeze balls and shorts.

Figure 3–8 shows guidelines for land pattern design. The lands are larger than the lead footprint. The land pattern should extend beyond the package footprint especially underneath the package. The stencil aperture may have to be the same size as the land pattern. When the spacing becomes very close, solder mask is used in order to retain the solder in the land pattern area as shown in Figure 3–8.

Stencil aperture design is not only critical to preventing opens and shorts in BTC package, it is also important to prevent floating of BTC packages, a very common phenomenon.

The reality is that BTC packages will be used with all other types of surface mount components, including BGAs, PQFPs, etc. So the selection of solder powder size will have to be done based on the lowest pitch component on the board. That particular package may or may not be a BTC

Table 3-1 Total Cost of Ownership of Bottom Terminated Components (BTC)

| Cost Contributor            | Impact                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Incoming inspection         | The incoming component inspection level is a function of the confidence the buyer has in the supplier considered in view of the cost of the different potential defects which might be encountered and how they might be resolved. Rework is an expensive process but product returns can ruin a business.                                                                                                                                                                                                                                                                                                                                                             |
| Component or package design | To meet cost and reliability targets, a reasonable rule of thumb is to select or design the lowest cost package that meets the lead count requirement and power dissipation with the largest pitch tolerable within design constraints. Consideration of the potential change to product specifications to improve product cost and reliability may be desirable under certain circumstances.                                                                                                                                                                                                                                                                          |
| Solder joint quality        | The solder joint is the most critical factor in product reliability today. Solder volume and solder placement is critical to yield and reliability of BTC assembly. The die attach pad (DAP) has been identified as an item that may be of high importance as some data show that reliability is reduced when it is not soldered in place.                                                                                                                                                                                                                                                                                                                             |
| Board design                | The board materials choice, layout and land pattern design are all vital and directly impacts board cost, assembly yield and reliability.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| Assembly method             | The assembly process has several steps including solder paste deposition, component placement, reflow and cleaning. The method chosen can represent a relatively minor % of overall cost when done with a well controlled process but costly otherwise. In some cases with BTCs, supplementary process equipment may be needed. While this will add some cost, overall cost will be reduced by improving yield.                                                                                                                                                                                                                                                        |
| Test & inspection           | While it is impossible to inspect quality into a product, test and inspection are commonly used to assure process control. Thus some level of visual, X-ray and electrical test is used to verify the quality of assemblies. Assembling BTC devices with solderable flanks has been shown to promote improved post-reflow inspection capability. Current BTC device processing steps do not guarantee solderable flanks. Requiring device suppliers to produce BTCs with solderable flanks may require adding additional processing. Post-reflow inspection that allows bad or marginal solder joint escapes leads to lower end user confidence and higher total cost. |
| Reliability                 | Rigorous design control reduces cost by ensuring reliability. Demonstrating the reliability of a design can be an expensive process and represent a major up front cost. A failure, however, especially a field failure, has arguably even greater cost impact.                                                                                                                                                                                                                                                                                                                                                                                                        |

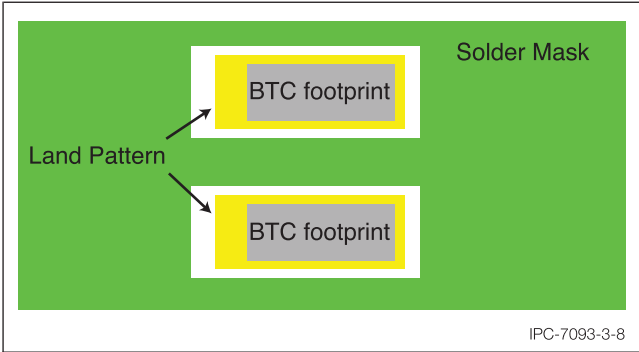


Figure 3-8 Solder Mask Clearance Guideline for BTCs

package. Also the thickness of the paste for BTC is critical since too little paste will create insufficient or, most likely, open solder joints. But excessive paste may cause floating of BTC. To prevent package float during the solder process, paste deposit thickness (especially on the center located thermal pad) should not be on the excessive side. Figure 3–9 shows a stencil design approach to achieve 50 to 60% of the thermal pad area.

It is recommended that the stencil design provide 50 to 60% solder paste coverage on the thermal pad area and 100% solder paste coverage on the I/O lands. Figure 3–10 shows a stencil design for both a ground plane with reduced paste coverage and outer I/O pad with stencil apertures with 100% paste coverage.

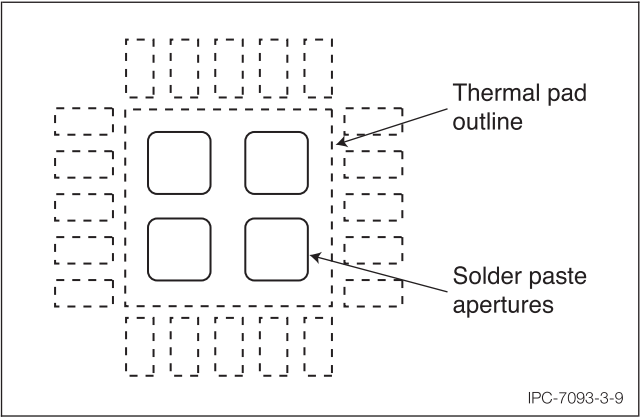


Figure 3-9 Example of Segmented Stencil Pattern Design on Thermal Land

The land pattern design should allow extension of the land beyond the package footprint outside of the package to facilitate AOI or visual inspection. It is important to keep in mind that a toe fillet is not required since it is not possible to achieve a toe fillet on a consistent basis since the packages are sawed and have an exposed unplated surface. A land pattern extension should provide visual evidence of reflowed solder at the toe of the BTCs even though the edge of the metallization is not wetted.

It is difficult to inspect BTC solder joints from the top of the package. So it may be necessary to tilt the PCB to inspect

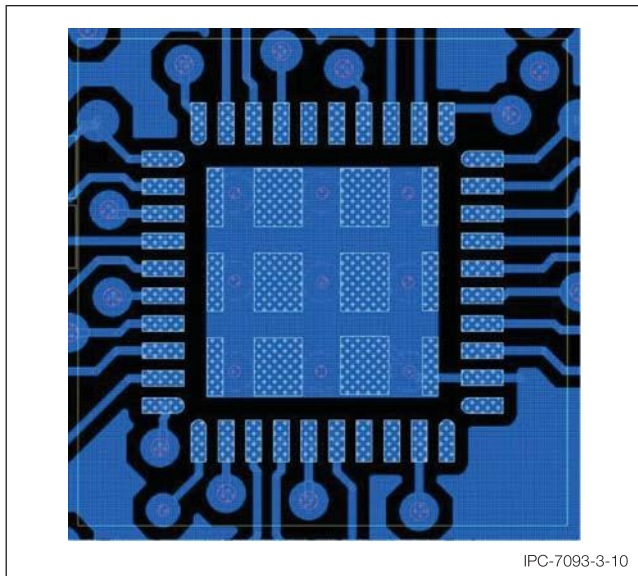


**Figure 3-10 Recommended Stencil Design to Provide 50–60% Paste Coverage to Ground Lands (but 100% on I/O lands)**

BTC solder joints to see solder underneath the package even though no toe or end fillet is expected. See 7.4 for more detail for post assembly inspection techniques of BTC devices.

X-ray inspection is one way to detect solder shorts underneath the BTC package. The X-ray image is also a good way to view solder voids in the solder joints. The acceptance limit of percentage of voiding in BTCs should be less than acceptable limits of 25% voids allowed in BGAs since there are no balls in BTCs and hence the potential for void is much less than in BGAs. However the void limits in the BTC thermal solder joints will have to be much higher because of much higher solder paste volume used on thermal pads. It is recommended that producers/manufacturers determine the voids allowable in volume and distribution for respective application requirements.

The micro-sectioning and die penetration techniques are other methods of inspecting solder joints. These methods are not meant for production inspection, but should be used for process development.

BTC components removed during PCB rework should not be reused for final assemblies. A package that has been attached to a PCB and then removed has seen two solder reflows and if the PCB is double sided, the package has seen three solder reflows. Thus the package is at or near the end of the tested and qualified range of known survivability. These removed BTC components should be properly disposed of so they will not be mixed in with fresh equivalent BTC components. See 7.7 for more detail for rework and repair of BTC devices.

The rework station for BTCs should be similar to many other type rework systems and have available the tools to

remove and replace faulty components. Tools such as hot air and laser systems are used for rework of assemblies by removing the component in question, redressing the lands and adding the appropriate solder paste or perform and positioning the component before applying heat.

**3.6 Future Needs and Expectations** BTC packages are becoming more and more popular because of their lower cost. But the lower package cost has not necessarily translated into lower cost overall when you take into account the total cost of the package, assembly, inspection, repair and potentially increased field failures. The root cause often attributed to this increased failure is the lack of protruding leads which, on the positive side, is the foundation of increased thermal and electrical benefits of the BTC package family.

As the industry has been constantly focused on cost reduction, the package suppliers have carved out a niche to reduce package cost. There remains a lot to be done about reducing PCB and manufacturing cost.

## 4 COMPONENT CONSIDERATIONS

This section provides the details of various BTC from the point of view of the component manufacturer. The common fabrication methods using both leadframes and substrates are described as well as common defects from each of these processes. The section also describes the manufacturing process flow for producing the different packages as well as the geometries, materials and many standard variations.

Although a number of small outline semiconductor package innovations have been available (e.g., BGA and FBGA), an effective method to significantly reduce the package area and cost was not available until the introduction of the SON and QFN package technology. The most significant feature of all of these small outline leadframe package families is their power dissipation capability and minimal electrical parasitics. The improved thermal dissipation performance comes from the exposed leadframe that is used to help pull heat out of the die to a mating thermal pad on the circuit board. Electrical parasitics are inherently low due to the small size and short wire bonds.

**4.1 General Description of Different BTC Packages** A large variety of bottom termination component packages are in the market. A few of the options are:

- 1) package configuration
- 2) pitch (1.0–0.4 mm)
- 3) termination geometry
- 4) land pattern geometry
- 5) package thickness
- 6) thermal pad geometry
- 7) plating

Figure 4–1 shows some of the BTC parts as shipped by the manufacturer to the board assembly plant.

These parts are available in a variety of configuration. Table 4–1 shows the configurations of QFN and SON (DFN) that are available from one packaging foundry. Other foundries are likely to have many of these as well as some that do not appear here. The JEDEC Standards list many other size, lead and thickness combinations that result from a general approach. Most of those listed, however, are not in common use.

**Table 4-1 QFN and DFN Configurations**

| Typical QFN/SON (DFN)<br>Plastic Packages that are Commercially Available<br>All dimensions in millimeters |         |       |            |                   |
|------------------------------------------------------------------------------------------------------------|---------|-------|------------|-------------------|
| Size                                                                                                       | QFN     | DFN   | Lead Pitch | Nominal Thickness |
| 2x2                                                                                                        |         | 6, 8  | 0.50       | 0.9               |
| 3x3                                                                                                        | 8       |       | 0.65       | 0.9               |
| 3x3                                                                                                        | 12, 16, | 8, 10 | 0.50       | 0.9               |
| 3x3                                                                                                        | 20      |       | 0.40       | 0.9               |
| 4x3                                                                                                        |         | 12    | 0.50       | 0.9               |
| 4x4                                                                                                        | 16      |       | 0.65       | 0.9               |
| 4x4                                                                                                        | 20,24   |       | 0.5        | 0.9               |
| 5x5                                                                                                        | 20      |       | 0.65       | 0.9               |
| 5x5                                                                                                        | 28, 32  |       | 0.50       | 0.9               |
| 6x6                                                                                                        | 40      |       | 0.50       | 0.9               |
| 7x7                                                                                                        | 48      |       | 0.50       | 0.9               |
| 7x7                                                                                                        | 56      |       | 0.40       | 0.9               |
| 8x8                                                                                                        | 52, 56  |       | 0.50       | 0.9               |
| 9x9                                                                                                        | 64      |       | 0.50       | 0.9               |
| 12x12                                                                                                      | 100     |       | 0.40       | 0.9               |

Land Grid Arrays are built in comparable sizes to those in the JEDEC standards and those in the table above. LGAs are typically larger than 5 mm x 5 mm and are almost always

built on a multilayer substrate. Many of the laminate based LGA components include multiple die elements and a number of passive devices. These configurations may consist of several different, but complementary, functions that together create a product that can be classified as a system-in-package (SiP). See Figure 4–2.

## 4.2 Detailed Description and Standards for BTCs

### 4.2.1 Single Row Molded Lead-Frame Based Packaging

The Die Attach Pad (DAP), when exposed outside the mold compound, also serves as a heat spreader. The die element is first bonded to the DAP surface followed by wire-bond termination from the die bond pads to the contact features at its perimeter (see Figure 4–3). The package is completed when the plastic casing is molded around the die and wire-bond area leaving only the bottom area of terminals and heat spreader exposed for solder attachment.

To control the effects of the large surface area of the die attach pad feature during the reflow soldering process, it will be necessary to tailor the solder stencil pattern or alter the mating thermal plane on the PC board.

### 4.2.2 Multiple Row Molded Lead-Frame Based Packaging

Plastic quad configured multiple row no-Lead packages (QFN) are plastic semiconductor packages with metallized terminals. Terminal contacts are located along the edges of the bottom surface of the package body arranged in 1, 2 or 3 rows. Typical of the single row QFN, the multiple row QFN package is a lead-frame based product. Before wire-bond, the die is bonded to the DAP surface followed by wire-bond termination from the die bond pads to the contact features at its perimeter (see Figure 4–4).

The package is completed when the plastic casing is molded around the die and wire-bond area leaving only the bottom area of terminals and heat spreader exposed for solder attachment. The die attach ‘paddle’, when exposed, also serves as a heat spreader.



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**Figure 4-1 Various Forms of BTC Parts**

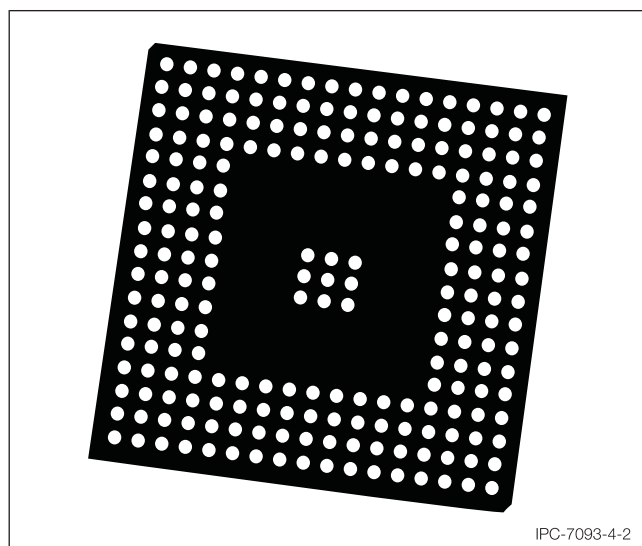


Figure 4-2 Singulated LGA Showing Bottom of Part

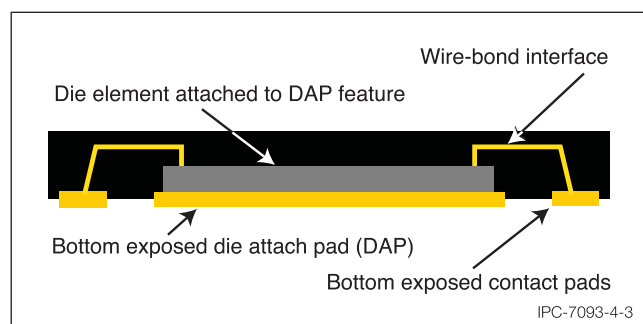


Figure 4-3 Basic Single Row Lead-Frame Based SON-QFN Package Assembly Model

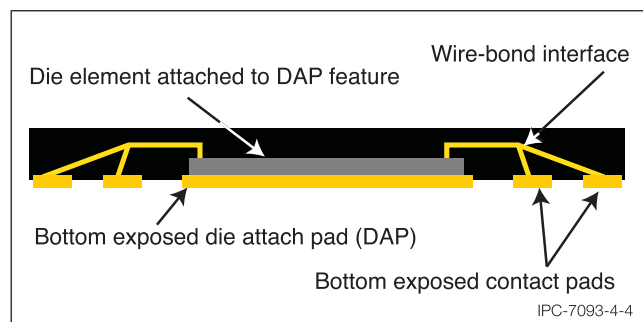


Figure 4-4 Basic Multiple Row QFN Package Assembly Model

**4.2.3 JEDEC Publication 95 Design Guide 4.8** The following excerpts are for Plastic Quad and Dual Inline, Square and Rectangular, No-Lead Packages (With Optional Thermal Enhancements). They include JEDEC definitions for SON and QFN packaging.

**4.2.3.1 SON (DFN)** Plastic Dual Inline Flat No-Lead Package is a semiconductor package with metallized terminals located on the bottom of the package. The SON has terminals on only two opposite sides of the bottom surface. By design, these terminals are flush with the bottom surface

of the plastic package body outline. The industry also uses the term DFN (dual flat no-lead) to describe SONs.

**4.2.3.2 QFN** Plastic Quad Flat No-Lead Packages have terminals on all four edges of the bottom surface of the package. The QFN can have either a square or rectangular body outline as well as either symmetric or asymmetric terminal patterns.

The single row small outline no-lead (SON) and quad flatpack no-lead (QFN) package technology has become a viable low cost methodology furnishing a package outline only slightly greater than the die. JEDEC defines the QFN/SON as a plastic semiconductor package with metallized terminals located on the bottom of the package body along its periphery as detailed in Figure 4-5.

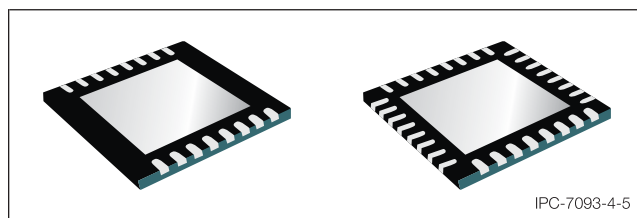


Figure 4-5 Terminal Configuration for Single Row SON and QFN Packaging

As noted in earlier sections, because the terminal features are flush with the bottom surface of the plastic body and do not protrude beyond the body outline, these packages are categorized as “bottom termination components” or “no-lead”. In addition, the supplier has the option of supplying an exposed heat spreader element on the bottom surface to assist in transferring thermal rise generated by the die element into the host circuit structure using solder or thermally conductive compounds.

The JEDEC design guide defines the symbology, algorithms, and recommended dimensions and tolerances for a family of QFN and SON Packages. The guidelines are based on hard metric dimensions and adhere to the geometric dimensioning and tolerancing principles defined in ASME Y14.5M.

In regard to the contact numbering method for the SON package positions terminal #1 (viewed from the top surface) at the lower left corner. Dimension ‘D’ should then be measured in the horizontal direction. Similarly, measure dimension ‘E’ in the vertical direction for both package types. For QFN, the position of terminal #1 is perpendicular to the body edge in the upper left corner as compared in Figure 4-6.

Terminal #1 identifier and terminal numbering convention will conform to JEDEC Pub.95, Sec 4.3, SPP-002. Terminal #1 identifier will be located within the zone indicated on the outline drawing. Topside terminal #1 indicator may be a

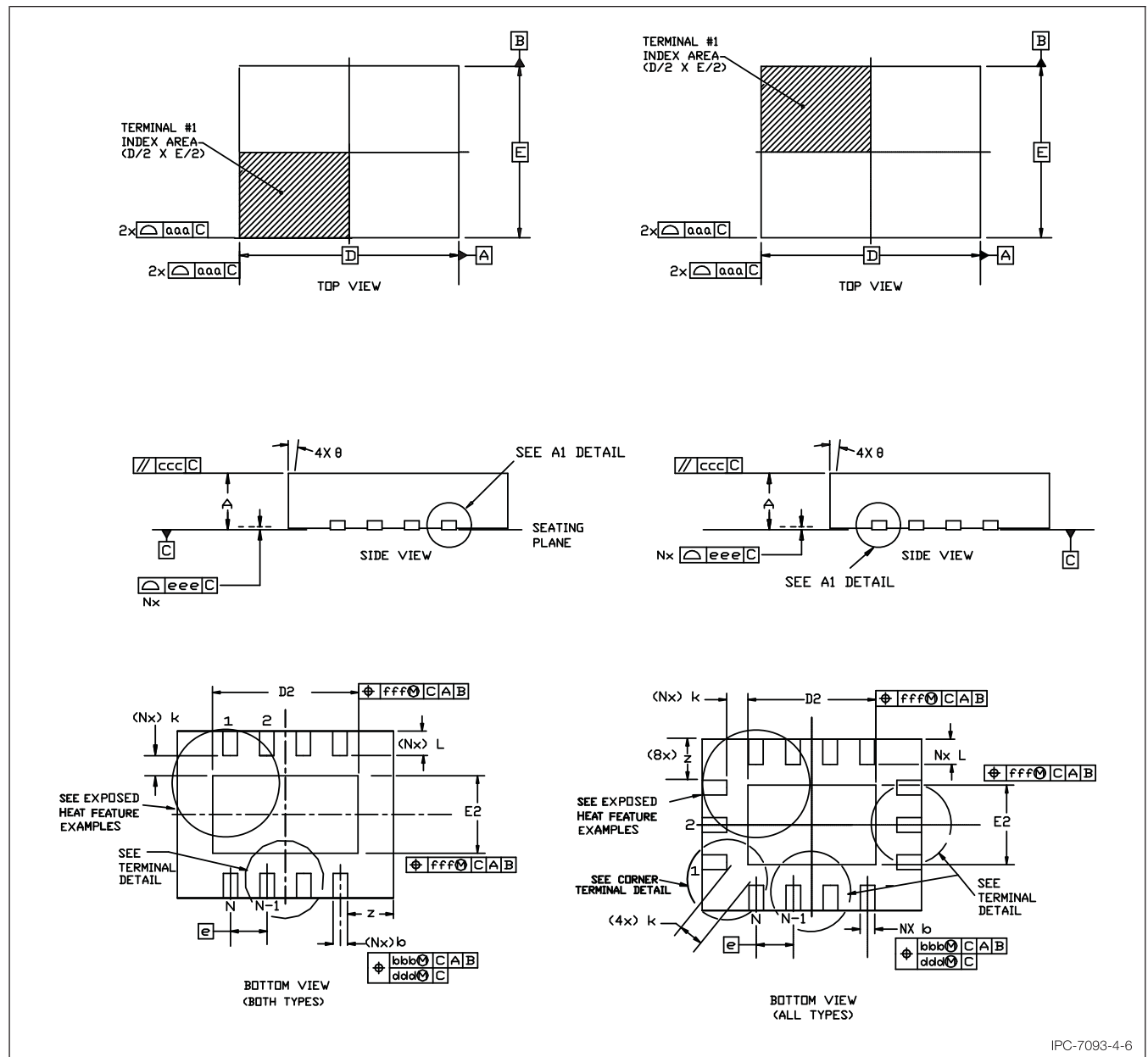


**Figure 4-6 JEDEC Defined Package Outlines for Single Row SON and QFN Packaging**

molded or marked feature. Optional indicator marking or features may also be furnished on the bottom surface as well.

Basic dimension for D and E dimensions suggested in the JEDEC design guide to be in increments of 0.50 mm ranging from 1.00 mm through 12.00 mm. Outlines with 'D' and 'E' increments less than 0.50 mm should be Registered as 'standalone' outlines. These outlines should use as many of the algorithms and dimensions (stated in this guide) as possible to ensure predictability in manufacturing.

The JEDEC members acknowledge that differing manufacturing processes by supplier companies will require some flexibility in the package configuration. Although the primary controlling dimensions will remain common, the terminal geometry may vary from one supplier to another.

An example of two terminal design variations is detailed in Figure 4-7.

There are three terminal variations:

1. Pullback – The terminals are located completely under the package body outline.
2. No Pullback – The terminals extend all the way to the edge of the package outline.
3. Extended – Terminals extend beyond the body outline (flange type molded version) but the overall measurements do not exceed the 'D' and 'E' dimensions defined in the guideline.

The terminal contacts may be furnished in 'odd' or 'even' numbers as illustrated in Figure 4-8. Inner edge of corner terminals may be chamfered or rounded in order to achieve

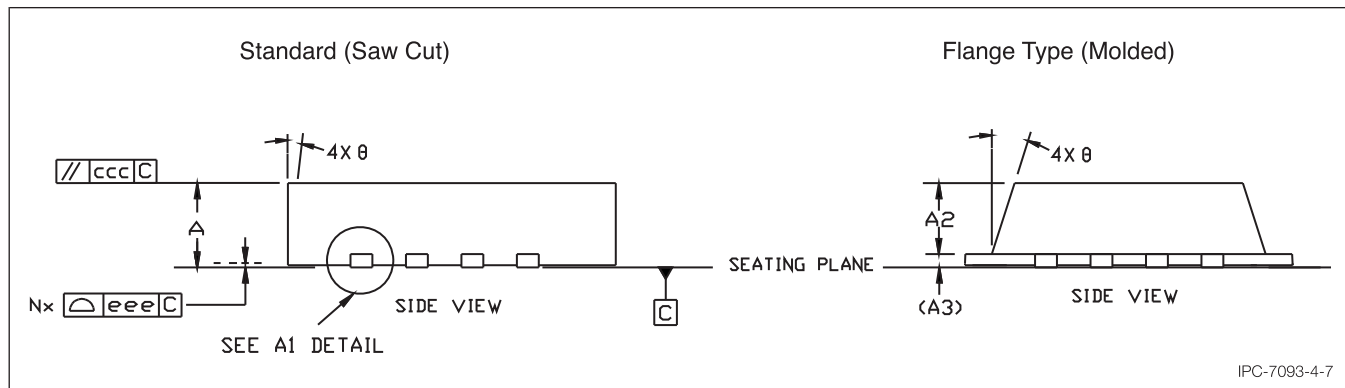


Figure 4-7 Terminal Design Variations for Single Row SON and QFN Packaging

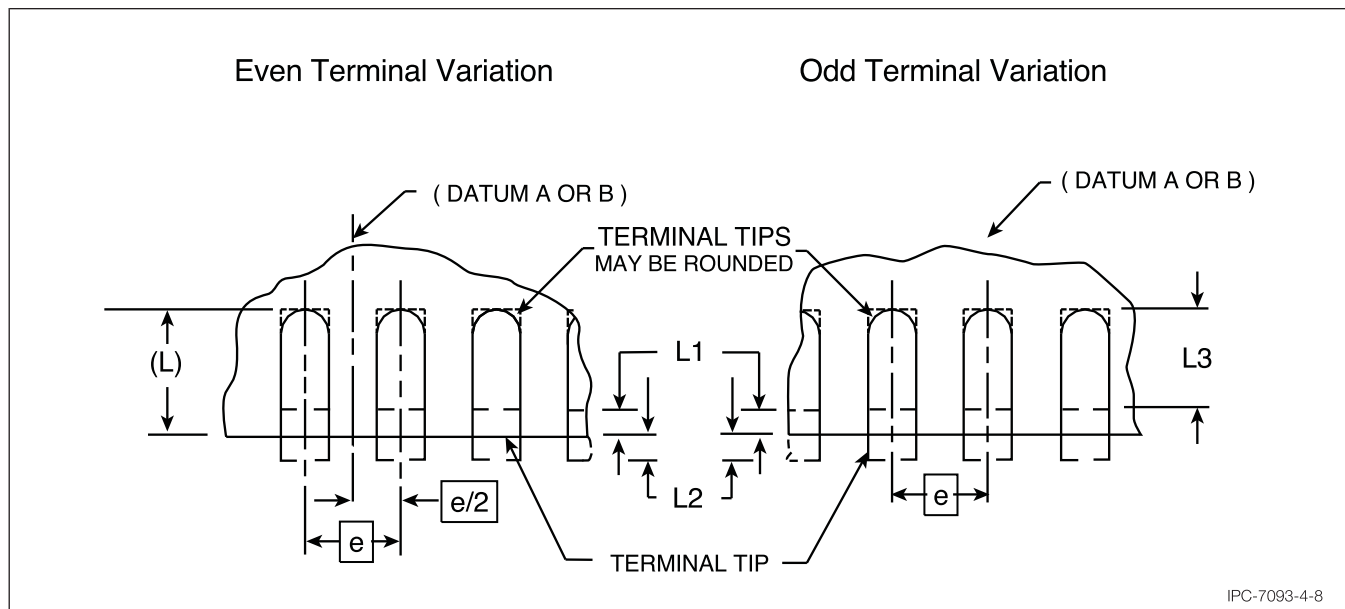


Figure 4-8 Odd and Even Terminal Contact Layout

minimum gap 'k'. This feature should not affect the terminal width 'b' which is measured from the edge of the package body.

Suppliers will generally furnish components with a balanced depopulation to reduce unequal surface tension forces that may occur during reflow solder assembly processing. Non-symmetric package configurations should be separate mechanical outline variations including depopulation graphics. See Figure 4-9. Corner population of terminal features is also an option on the QFN package and both SON and QFN, as noted, may be furnished with an exposed portion of the die attach pad on the bottom surface as shown in Figure 4-10. The bottom exposed die attach pad may be a solid or segmented, arranged in a matrix format, and may have optional corner radii on each segment.

#### 4.2.3.3 SON/QFN Terminal Spacing and Dimensions

The 'b' dimension represents the width of the metallized terminals (including lead finish) exposed at the bottom surface of the package. The terminal width (b) will vary as the pitch dimension narrows as shown in Table 4-2.

The length (L) of the terminal as measured from the edge of the plastic body. The JEDEC 4.8 guideline document allows two optional length dimensions defined as 'short foot' and 'long foot'. The terminal is classified as 'short foot' when 'L' nominal is 0.35–0.45 mm. If the package terminal dimension 'L' nominal is 0.50–0.60 mm, it is classified as a 'long foot' variation.

In regard to contact pitch, although six variations are included in the guideline standard, a majority of products actually reaching the market have been supplied with either 0.65 mm or 0.50 mm pitch. The 0.40 mm pitch devices are also being offered for limited applications, however, second level assembly processing requires very strict control.

**4.2.4 JEDEC Publication 95 Design Guide 4.23** The JEDEC Design Guide applies to Punch-Singulated, Fine Pitch, Square, Very Thin and Ultra Thin Profile, Lead-frame Based, Quad No-Lead Staggered Dual-Row Packages (with optional Thermal Enhancements). The examples shown in Figure 4-11 represent dual and triple row QFN with and without optional exposed die attach pad features.

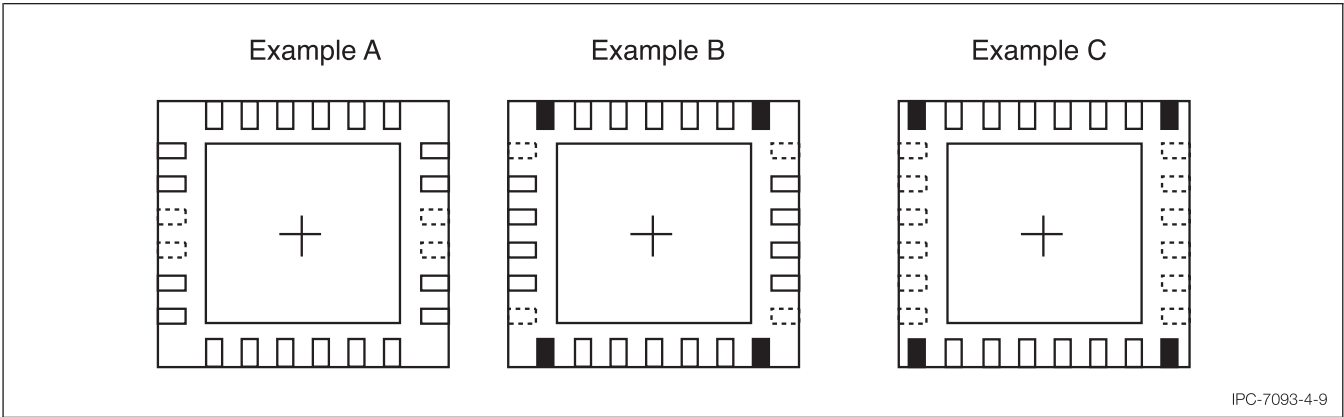


Figure 4-9 Depopulation Schemes for Single Row QFN Packaging

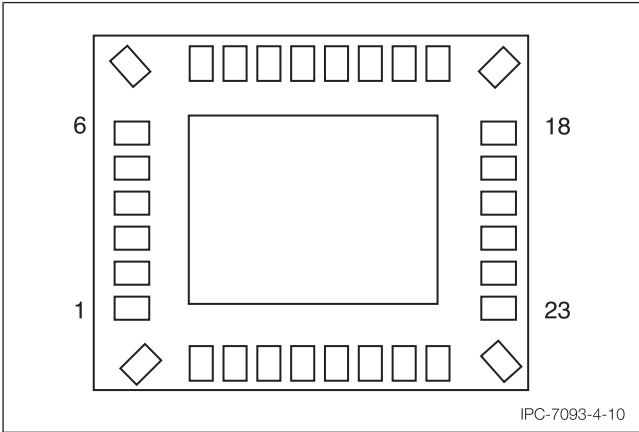


Figure 4-10 Corner Terminals and Exposed Heat Spreader

The QFN is described as a plastic semiconductor package with metallized terminals located along the peripheral edges of the bottom surface of the package. As noted, the package terminals are flush with the bottom surface of the plastic package body, so the packages are considered to be “BTC” or “no-lead”. This package has 2 rows of terminals on all four peripheral edges of the bottom surface of the package (see Figure 4-12).

The dual row QFN package may have either symmetric or asymmetric terminal patterns. Terminal A1 identifier must be located within the zone indicated on the outline drawing. Topside terminal A1 indicator may be a molded or marked feature and an optional indicator on bottom surface may be furnished as a molded, marked, or metallized feature.



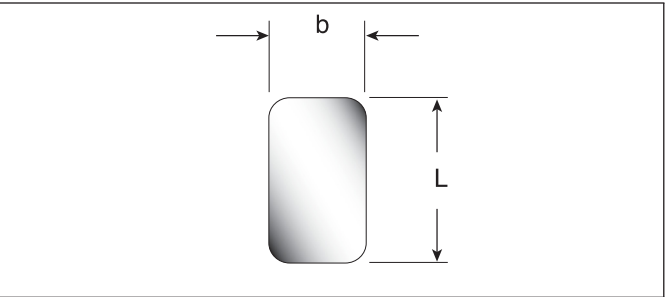
Figure 4-11 Fine-Pitch Two Row QFN (No lead) Packaging

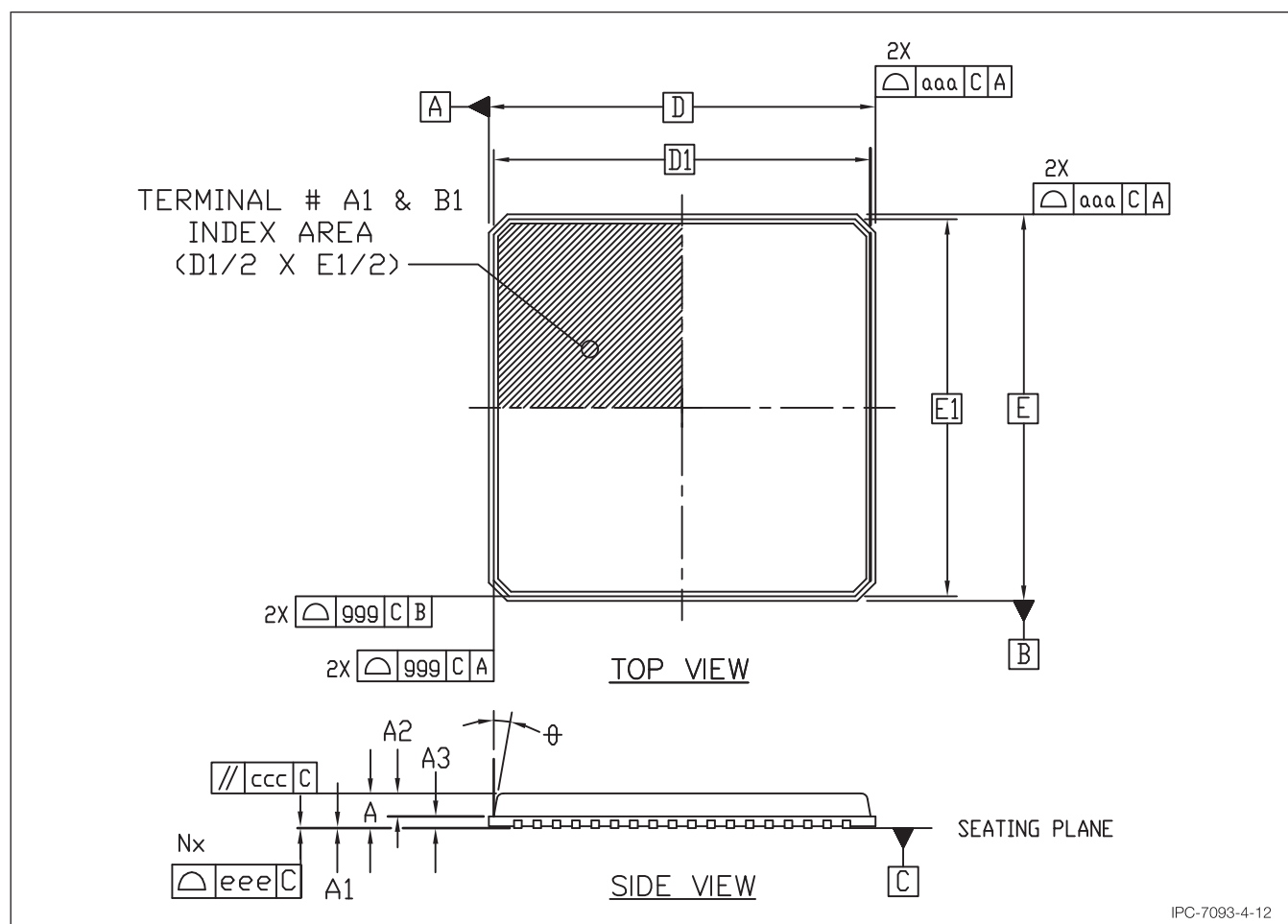
In regard to the description of the package as ‘very thin’ and ‘very-very thin’, the overall component height is measured from the seating plane (surface of the host substrate). The very thin (V) version will have a maximum dimension of 1.0 mm while the package defined as very-very thin (W) configuration has a 0.8 mm height limitation. The uniform square body dimensions are established in 1.0 mm increments from 5.0 mm through 12.0 mm and, depending on contact pitch (0.50 mm or 0.65 mm), an established maximum terminal count possible in the two row configuration (see Table 4-3).

Outlines with “D” and “E” increments less than 1.00 mm will likely be registered as “stand-alone” outlines. These outlines should use as many of the algorithms and dimensions (stated in this guide) as possible to ensure predictability in manufacturing.

Table 4-2 Terminal width variations for SON and QFN

| Contact Pitch | Terminal Width (b) |      |      |
|---------------|--------------------|------|------|
| 1.27          | 0.30               | 0.40 | 0.50 |
| 1.00          | 0.30               | 0.40 | 0.45 |
| 0.80          | 0.25               | 0.30 | 0.35 |
| 0.65          | 0.25               | 0.30 | 0.35 |
| 0.50          | 0.18               | 0.25 | 0.30 |
| 0.40          | 0.15               | 0.20 | 0.25 |





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Figure 4-12 QFN Dual Row Package (top and side views)

Table 4-3 Body Outline and Maximum Terminal Count

| Body Outline                                                       | Terminal Count by Pitch |         |
|--------------------------------------------------------------------|-------------------------|---------|
|                                                                    | 0.65 mm                 | 0.50 mm |
| 5.00 x 5.00                                                        | 36                      | 52      |
| 6.00 x 6.00                                                        | 44                      | 68      |
| 7.00 x 7.00                                                        | 60                      | 84      |
| 8.00 x 8.00                                                        | 76                      | 100     |
| 9.00 x 9.00                                                        | 84                      | 116     |
| 10.00 x 10.00                                                      | 100                     | 132     |
| 11.00 x 11.00                                                      | 108                     | 148     |
| 12.00 x 12.00                                                      | 124                     | 164     |
| Maximum terminal counts are calculated using established formulas. |                         |         |

Depopulation of terminal features is allowed, but only under the following conditions:

1. Depopulation scheme must be consistent in each quadrant of the package.
2. Non-symmetric variations should be broken out as separate mechanical outline variations, including depopulation graphics.

In regard to terminal layout variations, terminals are defined as even row spacing or odd row spacing as illustrated in Figure 4-13.

The JEDEC design guide document explains that the tolerance that controls the position of the entire terminal pattern (bbb) with respect to Datum's A and B cannot exceed 0.10 mm. The center of the tolerance zone for each terminal is defined by the basic dimension "eT" as related to Datum's A and B.

The bilateral profile tolerance (aaa) that controls the position of the plastic body sides cannot exceed 0.10 mm. The centers of the profile zones are defined by the basic dimensions D and E. Centerline-to-centerline spacing between two adjacent rows of terminals (eR) is 0.65 mm for the 0.50 mm pitch terminals and for the 0.65 mm pitch variation the spacing is specified at 0.75 mm. The nominal length (L) specified for the metallized terminals (including lead finish) exposed at the bottom surface of the package is 0.40 mm with a min./max. tolerance of 0.10 mm as illustrated in Figure 4-14. The minimum separation between the inner terminal tip and the heat spreader feature and or between the terminals at the package corners is 0.20 mm.

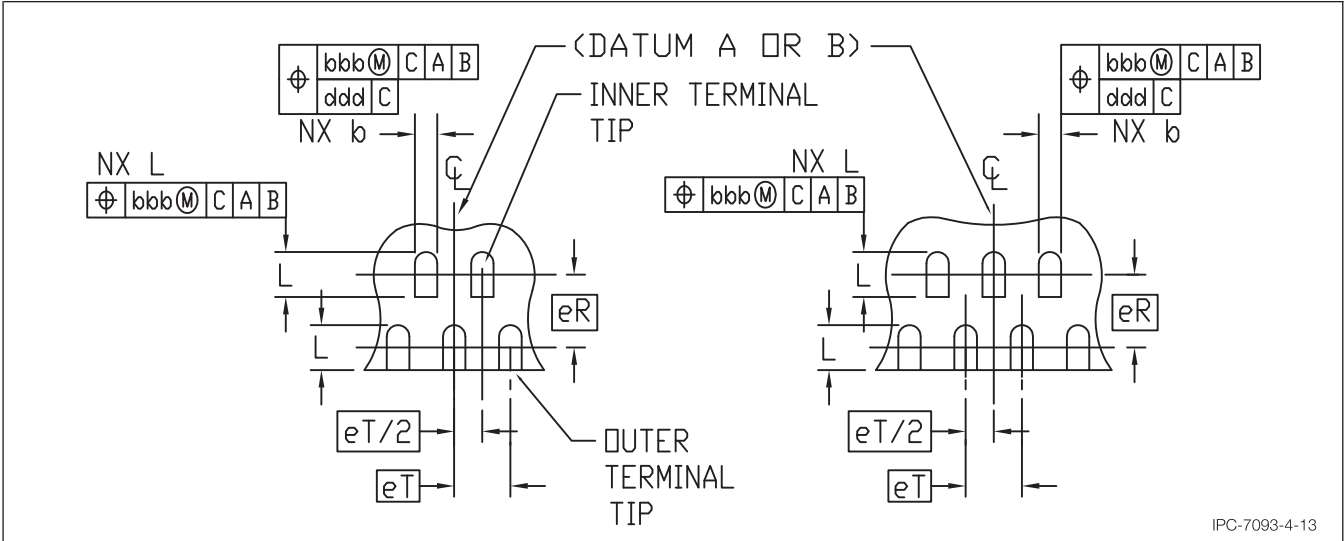


Figure 4-13 Outer and Inner Terminal Layout Variations

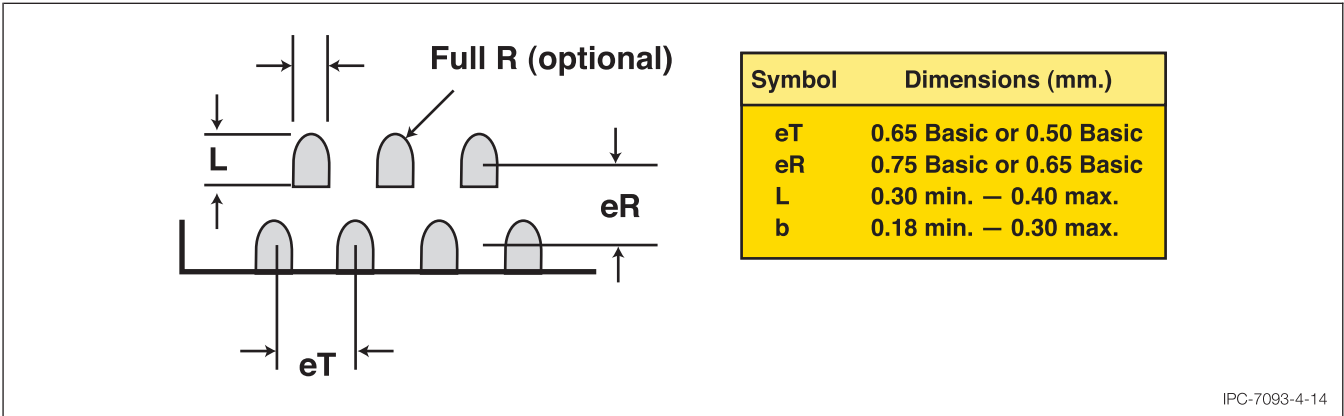


Figure 4-14 Two Row Terminal Layout

The tolerance that controls the position of the optional exposed metal heat spreader feature is positioned so that the center of the tolerance zone will be the datums defined by the centerlines of the package body. Because the die element is mounted to the inside surface of the heat spreader, thermal transfer of any heat generated by the die can be effectively transferred onto the surface of the host circuit structure. Although the dimple detail on the top surface of the mold compound clearly identifies the orientation of the device, the addition of a small chamfer or notch feature on the exposed die attach pad (illustrated in Figure 4-15) further assists in confirming the location of the A1 and B1 terminal.

**4.2.5 JEDEC Publication 95 Design Guide 4.19** JEDEC defines this package family as a 'Plastic Quad No-Lead (QFN)' having staggered or inline multi-row terminals. Typical of the preceding package configurations, this QFN family is classified as a plastic semiconductor package with metallized terminals located along the edges of the bottom surface of the package body. This design guide furnishes the primary outline features of the family of packaging that may

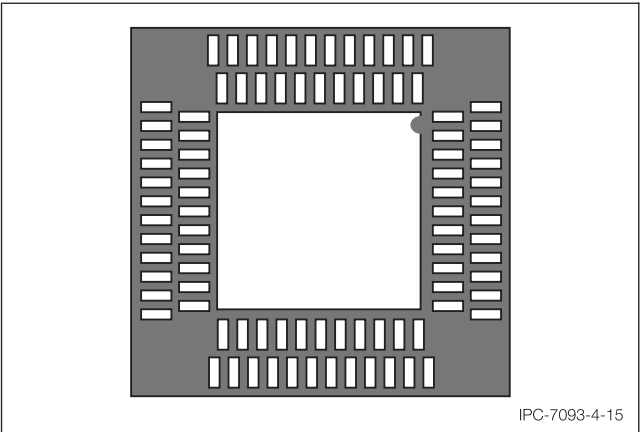


Figure 4-15 The Notch Feature on the Exposed Die Attach Pad Confirms Package Orientation with Reference to the A1 and B1 Terminals

be laminate based or plastic molded leadframe-based. The primary difference of this variation from the two previous guidelines is that this guideline details the requirements for square or rectangular contact terminal features arranged in 2 or 3 rows typical of those shown in Figure 4-16.

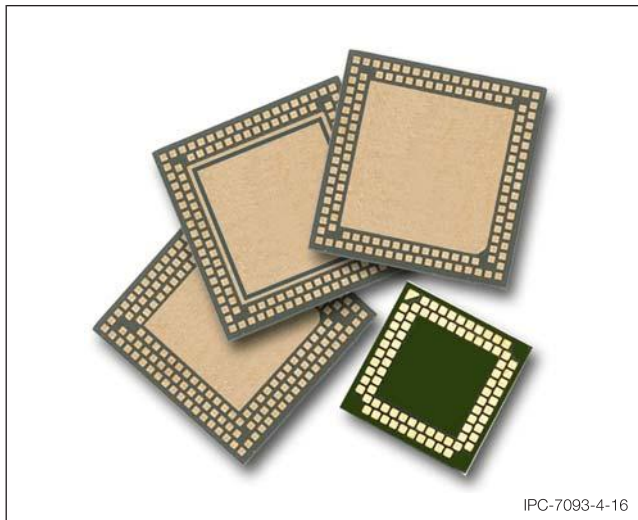


**Figure 4-16 Two and Three Row QFN Package Examples**

By design the package terminals are flush with the bottom surface of the plastic package body, so the packages are considered to be “BTC” or “no-lead” and, as noted, the package has 2 rows or 3 rows of terminals on all four edges of the bottom surface of the package.

The package can have a square or a rectangular body as well as symmetric or asymmetric terminal patterns as detailed in Figure 4-17 and Figure 4-18.

Three contact pitch ( $e$ ) variations are specified; 0.65 mm, 0.50 mm and 0.40 mm. The dimensions defined for the terminals are adjusted to allow clearance at various pitch conditions and the supplier has the option of selecting uniform or non-uniform ‘ $b$ ’ and ‘ $L$ ’ dimensions to provide a square or rectangular geometry. (See Figure 4-19).

The tolerance that controls the position of the terminals to each other ( $e$ ) is nominally defined at 0.05 mm. The

tolerance that controls the position of the entire terminal pattern with respect to Datum’s A and B is 0.10 mm for the 0.65 mm and 0.50 mm pitch package and is reduced to 0.07 mm for the 0.40 mm pitch package variation. The center of the tolerance zone for each terminal is defined by the basic dimension ‘ $e$ ’ as related to Datum’s A and B.

The overall package outline dimensions are defined as ‘ $D$ ’ for package width and ‘ $E$ ’ for package length. The current document specifies that the ‘ $D$  and ‘ $E$ ’ dimensions be in increments of 0.50 mm ranging from 4 mm to 19 mm. Outlines with ‘ $D$ ’ and ‘ $E$ ’ increments less than 0.50 mm should be registered as “stand-alone” outlines. These outlines should use as many of the algorithms and dimensions (stated in this guide) as possible to ensure predictability in manufacturing. The overall package height is not specifically defined but the guideline recommends a profile no higher than 1.0 mm where the overall component height is measured from the seating plane (surface of the host substrate). The unilateral tolerance located above the seating plane wherein the bottom surface of all terminals must be located is 0.08 mm. This tolerance is commonly known as the “coplanarity” of the package terminals. The tolerance which controls the top surface of the package is nominally 0.10 mm. The basic QFN package outline shown in Figure 4-20 defines the basic outline features referenced above for ‘ $D$ ’ (package width) and ‘ $E$ ’ (package length) and ‘ $A$ ’, overall package height.

Terminal A1 identifier must be located within the zone indicated on the outline drawing. Topside terminal A1 indicator may be a molded or marked feature. Optional indicator on bottom surface may be a molded, marked, or metallized feature. See Figure 4-21 for examples of pin 1 indicator.

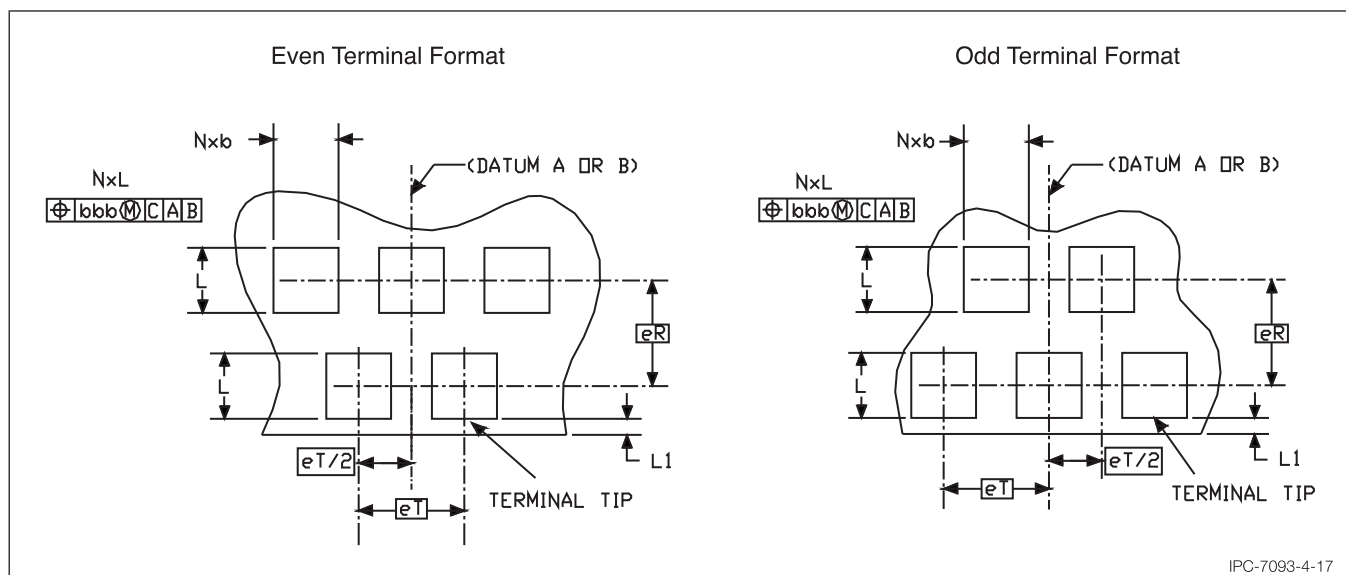


**Figure 4-17 Basic Two Row Terminal Layout Variations**

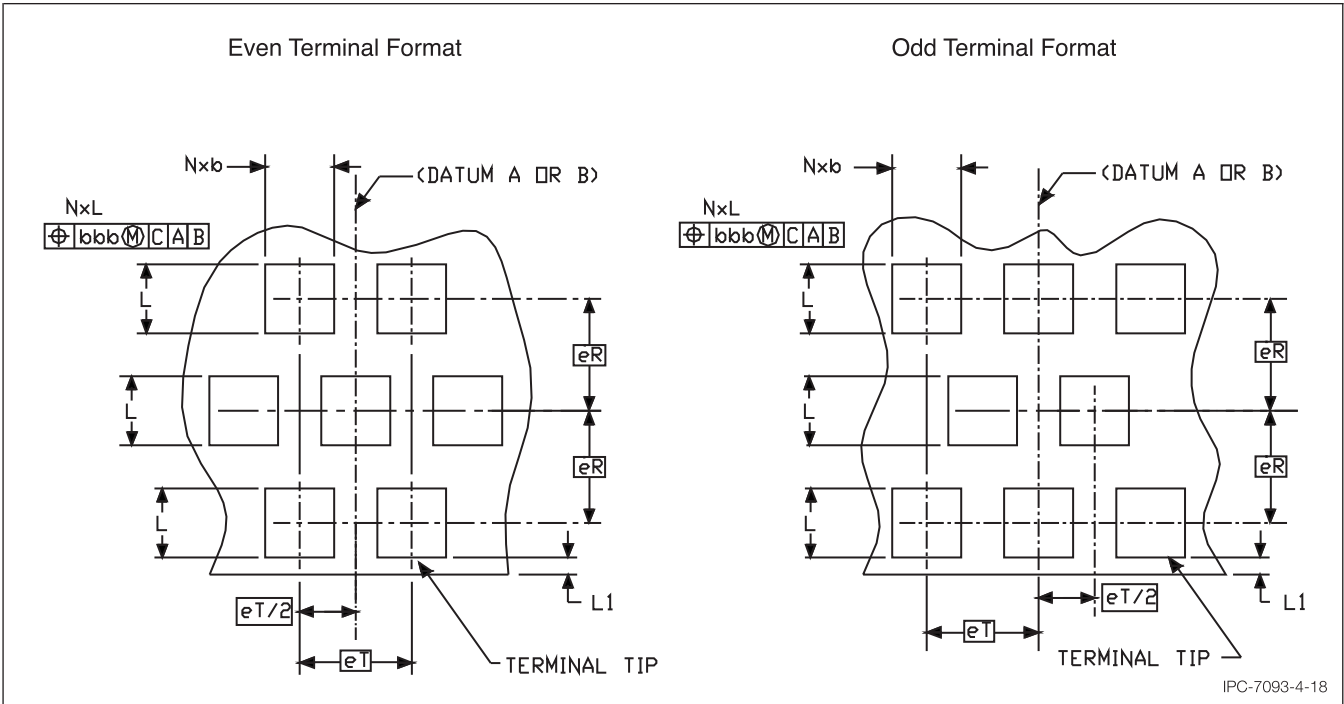
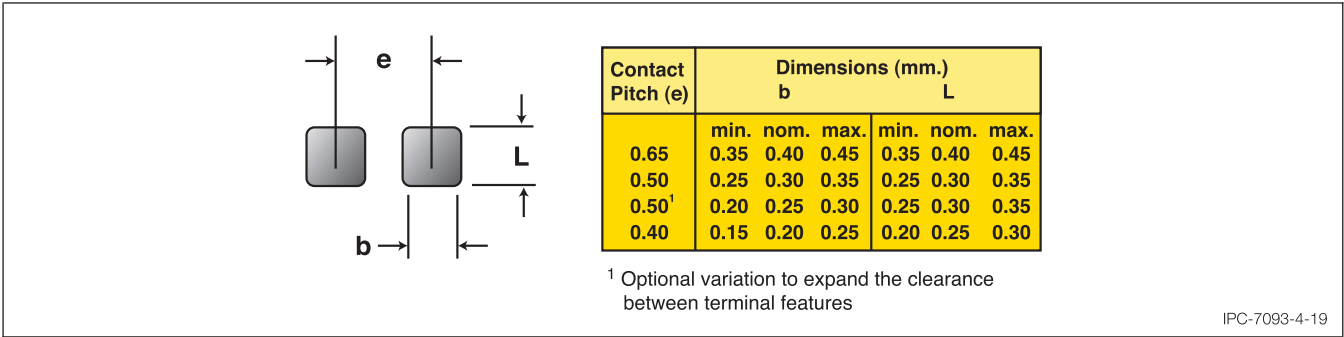


Figure 4-18 Basic Three Row Terminal Layout Variations



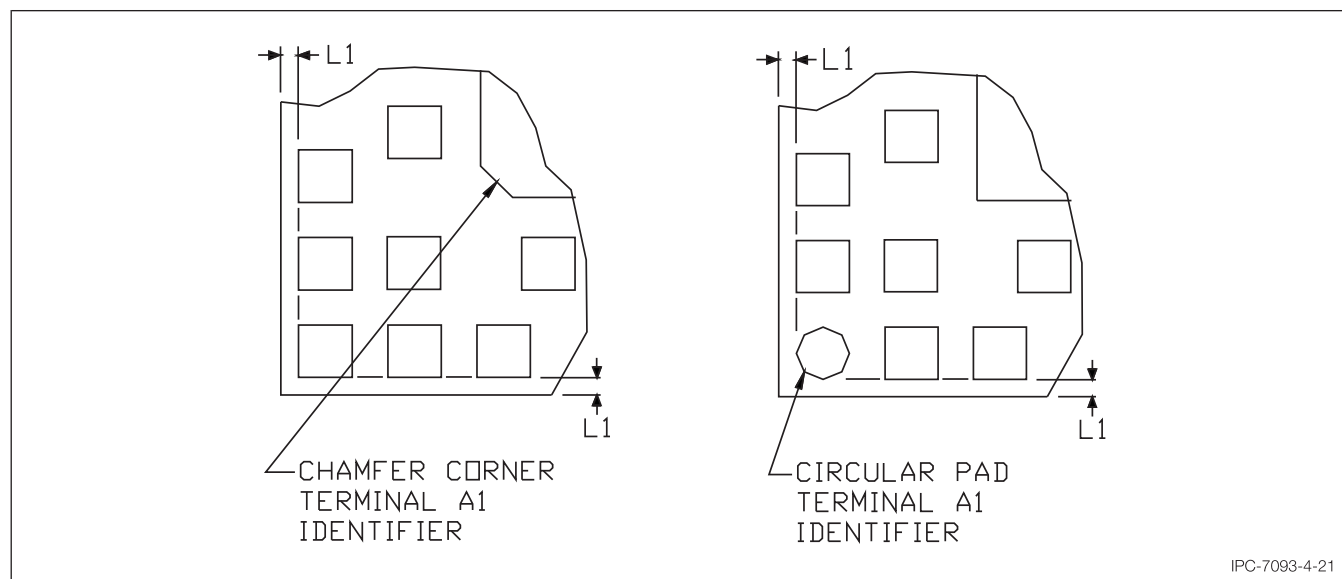


**Figure 4-21 Pin 1 Location Option**

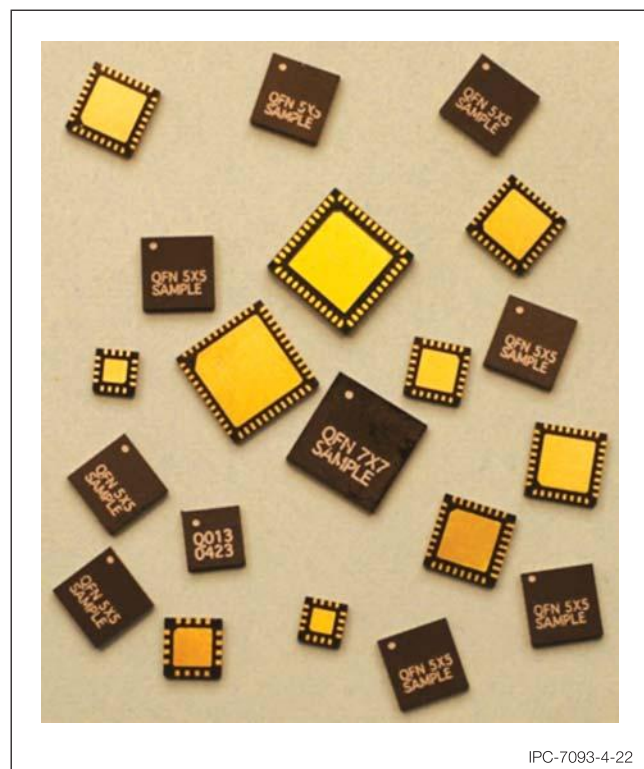


**Figure 4-22 BTC Multiple Package Configurations**

The leadframe panel shown in Figure 4-23 and Figure 4-24 measures 75 mm x 300 mm and includes four sections each having 42, 7.0 mm x 7.0 mm QFN sites. The bottom, or terminal side of the leadframe panel will be covered with a protective film that prevents mold compound from encroaching onto the terminals surface during the overmold process.

Leadframes are usually made from rolled sheet copper etched from both sides with slightly different patterns. The difference in etch pattern gives the undercut evident in the

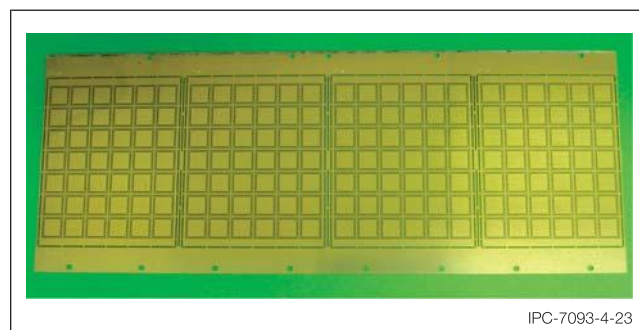


**Figure 4-23 Typical Die Attach Side Leadframe with Ni-PdAu Finish for QFNs**

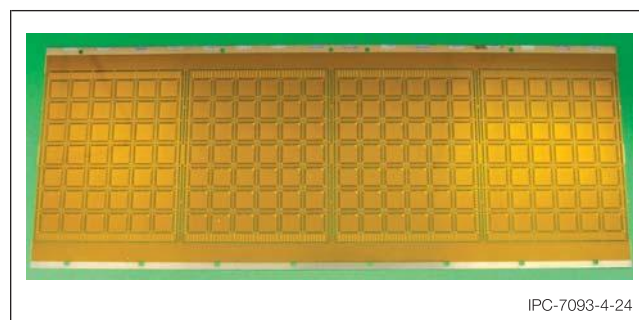


**Figure 4-24 Typical Solder Pad Side of QFN Panel for with Tape over the Leadframe**

drawings and sketches in section 4. The major purpose of the undercuts is to provide mechanical interlocking of the mold compound and leads to increase the mechanical strength.

In preparation for package assembly and to accommodate the eventual mounting of the BTC package, the leadframes are electroplated with alloys compatible with both wire-bond processing and reflow solder soldering (a NiPdAu alloy composition is most common).

Another option is to spot plate the wire-bond sites with a silver alloy leaving the remaining area of the copper based leadframe without plating until after the overmold process. The remaining exposed contact and thermal pad features on the panel are plated with a tin-alloy finish for solder attachment.

The BTC package assembly process may vary somewhat from one supplier to another, but, the basic sequence of assembly for the product described above will follow the flow of the diagram detailed in Figure 4-25.

An overmolded version of the leadframe in Figure 4-23 is shown in Figure 4-26. The example is a four section overmolded array right after it was removed from the mold. The dark colored areas are the molding compound that form the 4 arrays, each of which measures approximately 45 mm x 55 mm. The dark areas around the periphery and between the molded arrays are mold compound that fill slots in the leadframe.

Following the overmold process the individual devices will be marked and singulated from the panel format. The most common method for singulation of BTC devices is a precision saw. An alternate method uses a punch press operation. For this method the mold design will be pre-segmented at each device site to provide access for the die-punch. Due to the high cost of tooling and additional

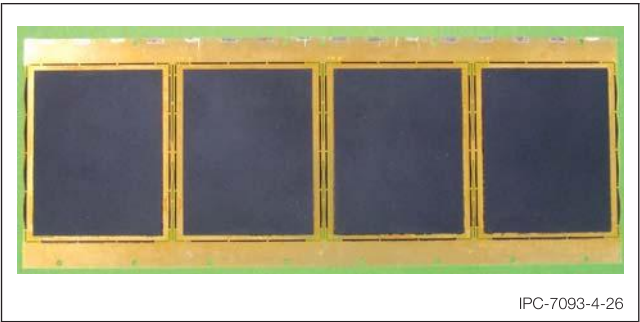


Figure 4-26 Overmolded Leadframe Configuration

equipment required for punch singulation, the technique is typically reserved for very high volume production.

The process flow for Punch Singulated QFNs is illustrated in Figure 4-27.

The mold design for the punch singulation method is more complex and expensive than those used for saw singulation. Punch singulation requires a mold with a cavity for each part so that the web of the leadframe remains exposed between individual parts. This web is punched out in a single stroke with a die that matches the part.

Both saw singulation and punch singulation leave bare copper edges on the leads where they are cut from the leadframe. These bare edges can serve as a surface for a

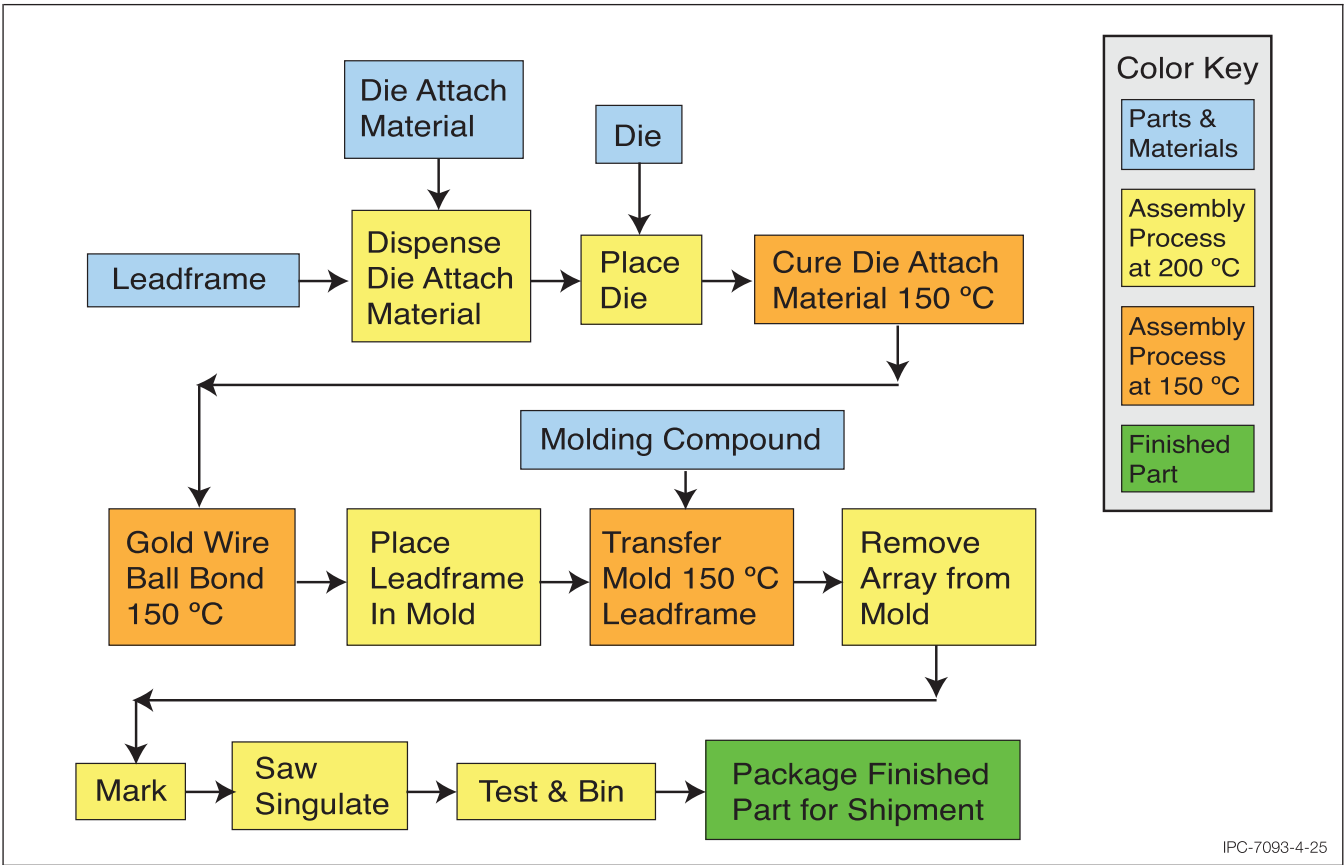


Figure 4-25 QFN Fabrication with Saw Singulation

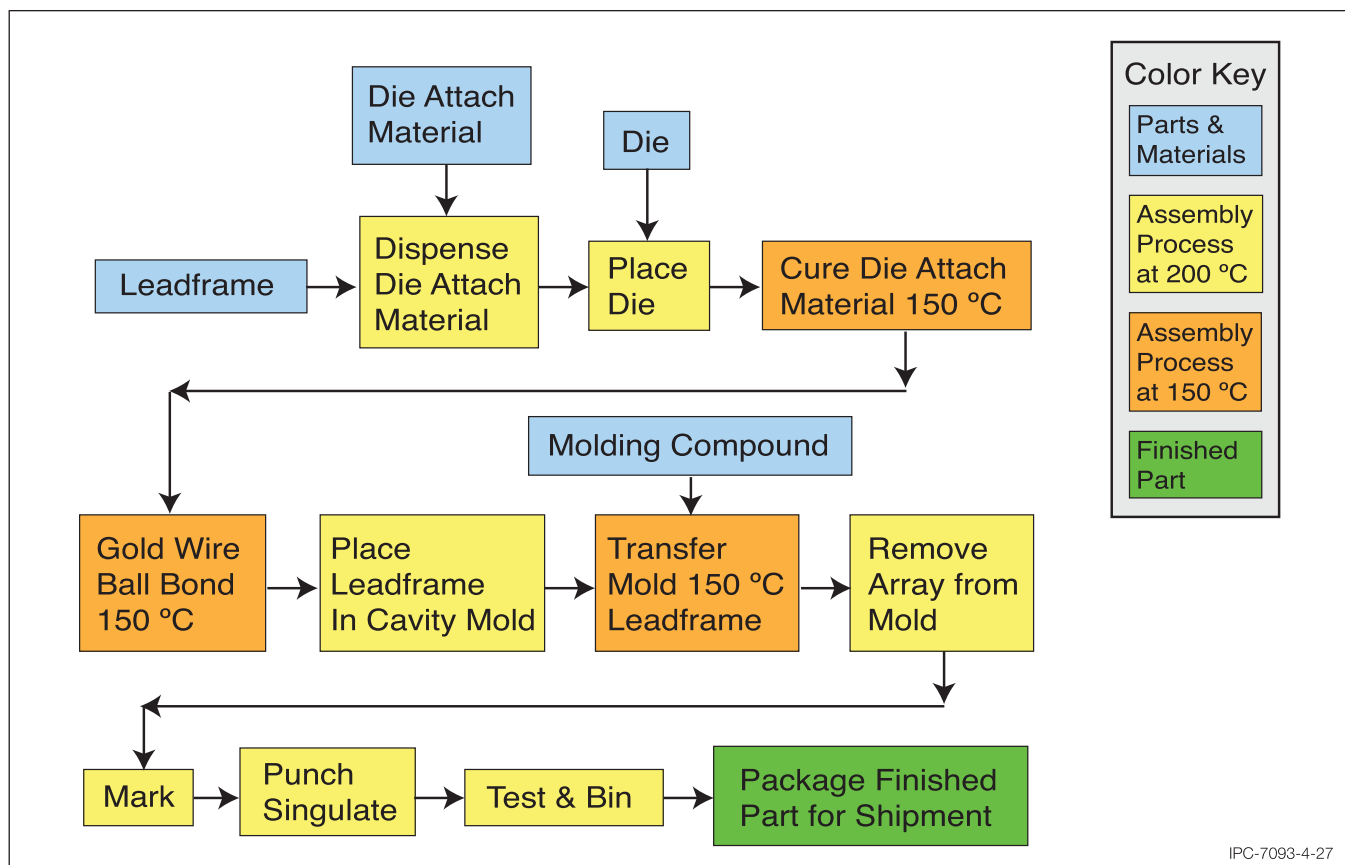


**Figure 4–27 QFN Fabrication with Punch Singulation**

solder fillet if the solder system will wet the bare copper. Some users may also require BTC suppliers to take additional measures, after singulation, to preserve flank solderability. These measures are intended to allow users to rely on toe fillets formed along the BTC flanks as an aid to reliable assembly inspection.

The illustrations in Figure 4–28 show the detailed differences that result using punch singulation and saw singulation.

While punch singulated packages are individually punched from molded strip during final assembly, the saw singulated package are assembled in array format and separated into individual components during the final sawing operation.

The image on the left of Figure 4–28 is punch singulated from an array of individually molded sites. The mold cavity walls have some draft shown in the sketch to facilitate removing the molded parts from the cavities.

A second characteristic of punch singulated devices evident in the image on the left of Figure 4–28 is the small leadframe extension beyond the edge of the molding compound to provide space to prevent the die from cutting the mold compound.

The sketch on the right of Figure 4–28 shows the saw singulated cross section that lacks both draft and the extended lead.

Figure 4–28 also shows the 3 common wire bond options:

- bonds between the die and the finger leads
- bonds between the die and the die attach pad (so called “down bonds”)
- bonds from the die pad to the finger leads

These wire bond options are used to make the required electrical connections.

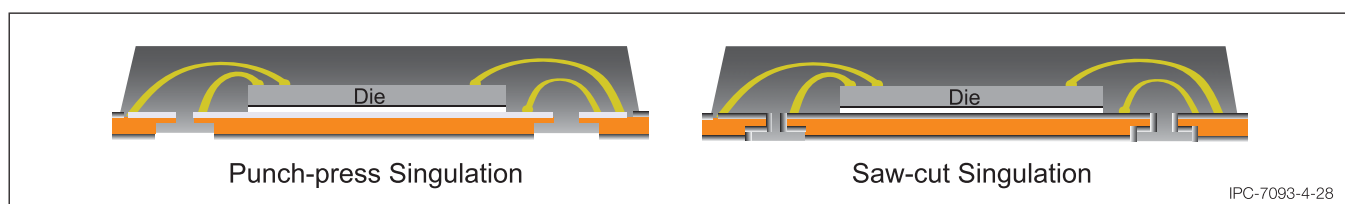


**Figure 4–28 Comparing Punch-Press and Saw-Cut Singulation and Illustrating Wire Bond Options**

Saw singulated packages are further divided into two options as illustrated in Figure 4–29: the no-pullback (full) lead package, and the pullback lead package. While the full lead package has the whole thickness of the lead exposed on the package sides, the lead pullback package has a bottom half etch leadframe, resulting in only the top half of the lead thickness exposed to the sides of the package.

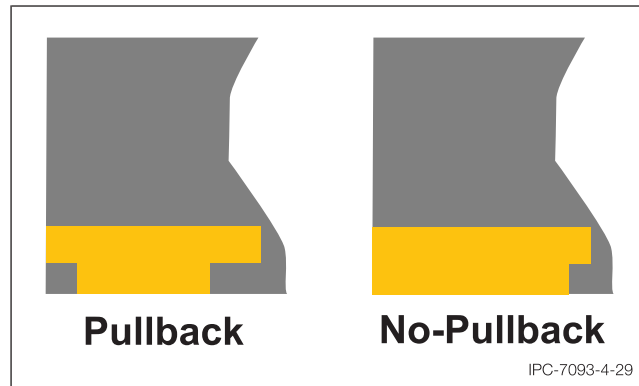


**Figure 4–29 Example of Half Etch Pullback Contact and Full Etch No-Pullback Perimeter Contact Configurations**

The pullback approach is only viable when the package is built into an etched leadframe. The pullback approach provides better capture of the lead and thus makes the package stronger. One disadvantage is that some test sockets may not be designed to make contact in this area.

A more important disadvantage of the pullback configuration is that the solder joint is not visible making inspection more difficult. The mold compound blocking access to the ‘pullback’ terminal makes it impossible to form a solder fillet on the outer edge of the device. While the unplated surface of these edges that result from both the punching and sawing processes makes solder wetting difficult, the pull back configuration virtually guarantees that a fillet cannot form with any soldering process.

**4.3.2 Types of Defects** Common defects that result from the fabrication methods described are:

- delamination of the mold compound from the leadframe that sometimes results in wire bonds pulling loose from the leadframe
- mold compound flash on the leads or die pad that interferes with soldering, die attach or wire bonding
- voids resulting from incomplete mold compound fill
- bond wire sweep in the molding process resulting in shorted wires or, less frequently, broken wires
- smear of copper during the sawing process along the side

of the package, sometimes severe enough to result in shorting, especially during SMT solder reflow

- burrs from the sawing or punching process interfering with the planarity of the part or the geometry of the solder joint
- inadequate tolerance control of the part dimensions, especially the width and length, resulting in a poor fit to test sockets
- incorrect marking of pin 1

Table 4–4 shows some examples of common leadframe package defects. The table provides three levels of defects and highlights the possible causes.

The plating characteristics are an important part of the leadframe BTC construction. Attachment both within the component package as well as the external terminations must be carefully addressed for the most robust joint structure. Table 4–5 provides some examples of the potential defects.

**4.3.3 Marking Alternatives** Common methods of marking BTC packages are:

- Pad printing with a high contrast ink, usually white
- Laser marking to give finer features that often has low contrast
- Laser marking using an ink that provides good contrast as well as fine features

**4.3.4 Materials Used** Leadframes are most commonly made of copper. A variety of molding compounds are used. Which is used depends not only on the part and components within the QFN-SON, but the mold design and molding machine. These molding compounds are formulated to have excellent flow characteristics to ensure fill while minimizing wire sweep.

A variety of lead finishes are used. The most common are NiPdAu, and Tin. SnBi is also sometimes used as a plating finish as is plated solder using other alloys. Table 4–5 shows some of the plating variations while Figure 4–30 shows the thickness relationships of some of the plating combinations.

**4.3.5 Solderability Testing** The solderability testing of BTC components should be conducted in accordance with the IPC-J-STD-002 specification. A number of individual test methods are applicable to the BTC components. Test Method S (for tin/lead solder processes) and S1 (for lead-free solder processes) are the most applicable for BTC surface mount components.

**4.4 Custom QFN and SON (DFN)** One of the attractive features of the leadframe based QFN family of BTC packages is the relative low cost and minimal time required to design and fabricate a custom version. All of the

Table 4-4 Leadframe Package Defects and Failure Modes

| Common Leadframe-Based Package Defects and Failure Modes                                                                          |                                                    |                                   |                                                                                                 |
|-----------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------|-----------------------------------|-------------------------------------------------------------------------------------------------|
| Defect/Failure Mode                                                                                                               | Potential Failure                                  | Detection Method                  | Cause                                                                                           |
| <b>Level 1, within package</b>                                                                                                    |                                                    |                                   |                                                                                                 |
| Excess water content due to inadequate storage or drying                                                                          | Pop corning, delamination during solder reflow.    | Hard to detect.                   | Water uptake from environment when parts are not stored or dried properly                       |
| Detrimental package compound voids                                                                                                | Corrosion, delamination                            | Ultrasonic                        | Poor molding control or poor handling                                                           |
| Cracked package                                                                                                                   | Mechanical and/or electrical failure               | Visual examination, die penetrant | Excess mechanical bending of package, mold compound knit line                                   |
| Lead to compound failure potentially resulting in lead fall out                                                                   | Lead falling off or breaking wire bond             | Visual examination                | Molding, sawing or punching process defect                                                      |
| Paddle to die delamination                                                                                                        | Overheating, wire break, die cracking              | Ultrasonic, decapsulation         | Poor wetting, incorrect cure                                                                    |
| Broken wires                                                                                                                      | Electrical open                                    | X-ray                             | Wire bonding process control error, mold compound sweep                                         |
| Lifted stitch/broken heel to leadframe                                                                                            | Electrical open                                    | X-ray, electrical test            | Wire bond process control error, surface contamination, inadequate plating                      |
| Lifted wire bond balls from die                                                                                                   | Electrical open                                    | X-ray, electrical test            | Wire bond process control error, surface contamination, die metallization error                 |
| Shorted wire                                                                                                                      | Electrical short                                   | X-ray, electrical test            | Mold wire sweep, or wire bond process control                                                   |
| <b>Level 2, outside of package</b>                                                                                                |                                                    |                                   |                                                                                                 |
| Non-wetting lead surfaces                                                                                                         | Open connection                                    | Visual, X-ray                     | Oxidized surfaces, plating contamination or incorrect thickness                                 |
| Out of dimensional spec                                                                                                           | Poor contact in test socket                        | Measurement                       | Molding (thickness) or singulation                                                              |
| Lead smear of copper                                                                                                              | Shorting of leads                                  | Visual                            | Sawing conditions                                                                               |
| Inadequate flatness                                                                                                               | Open joints                                        | Visual                            | Molding or singulation method                                                                   |
| Burrs                                                                                                                             | Electrical shorts                                  | Visual                            | Singulation process                                                                             |
| Dimples on pads cause by test socket contact                                                                                      | Void in solder joint and potential open connection | Visual                            | Aggressive probing breaks through plating resulting in non-wetting spot and void in final joint |
| Marking defects                                                                                                                   | Wrong part or unknown part                         | Visual                            | Poor marking, handling damage                                                                   |
| <b>Level 3 package to board</b>                                                                                                   |                                                    |                                   |                                                                                                 |
| Voiding in joints                                                                                                                 | Long term electrical open                          | X-ray                             | Solder paste or reflow process                                                                  |
| Non-wetting of pads                                                                                                               | Electrical open                                    | X-ray, electrical test            | Part contamination or solder process                                                            |
| Bridging under package                                                                                                            | Electrical short                                   | X-ray, electrical test            | Part or board contamination, solder process                                                     |
| Liftoff of package from PCB due to floating on the solder                                                                         | Electrical open, less shock resistance             | Visual                            | Too much solder paste                                                                           |
| Sinking of package into solder due to its weight causing detrimental solder displacement resulting in bridges and/or poor joints. | Electrical short                                   | X-ray                             | Part too heavy for reflow conditions, paste or solder rheology at temperature                   |

Table 4-5 Plating Systems Used on Metal Leadframes

| Plating types                                                            | Characteristic Descriptions     |                                                       |
|--------------------------------------------------------------------------|---------------------------------|-------------------------------------------------------|
| Tin plate 10 $\mu\text{m}$ min.                                          |                                 | Most common                                           |
| NiPdAu 0.508 $\mu\text{m}$ , 0.013 $\mu\text{m}$ and 0.005 $\mu\text{m}$ | Often called the Samsung finish | 0.4 mm pitch are all NiPdAu. Larger are other systems |
| Tin finish with Ag on bond sites                                         |                                 | Post mold tin plate of bare copper                    |
| NiPdAu 1.02 $\mu\text{m}$ , 0.08 $\mu\text{m}$ and 0.010 $\mu\text{m}$   | Often called the Shinko finish  | 0.4 mm pitch are all NiPdAu. Larger are other systems |

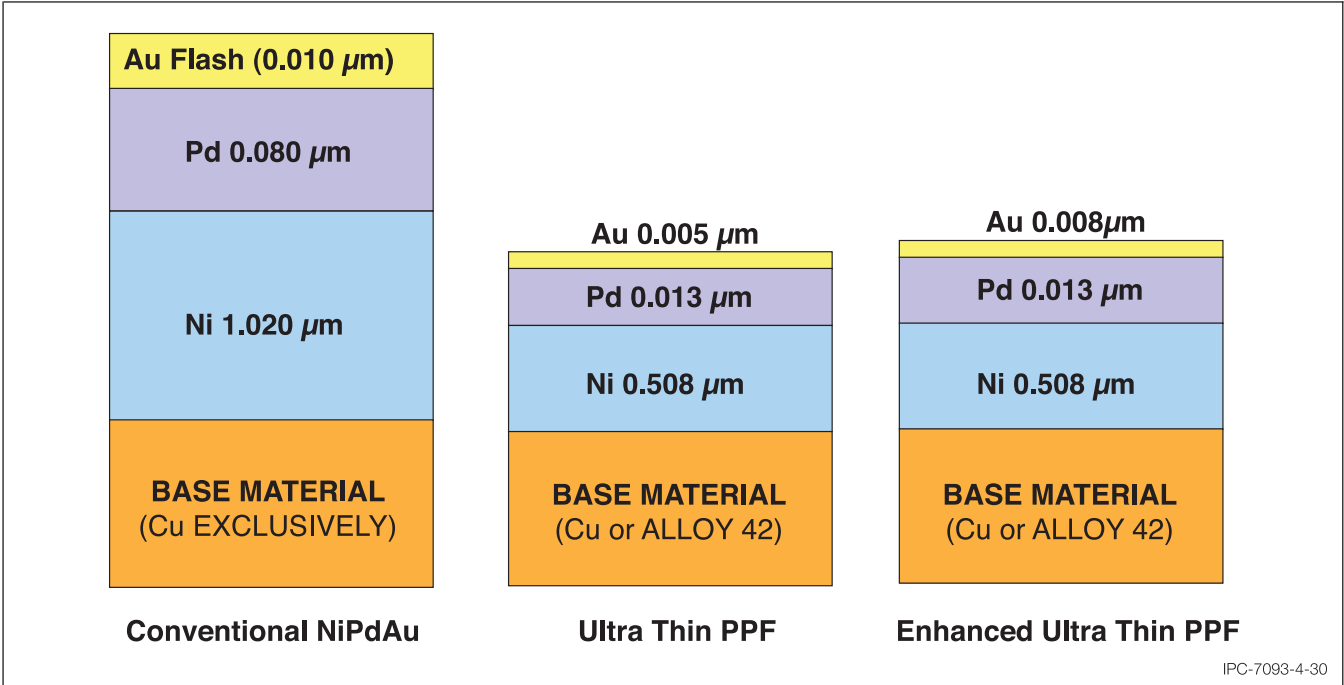


Figure 4-30 Plating Layer Construction Comparison

processes, materials, etc., are described above for QFNs. The major method of customizing is modifying the leadframe. Figure 4-31 shows several modifications built into one leadframe.

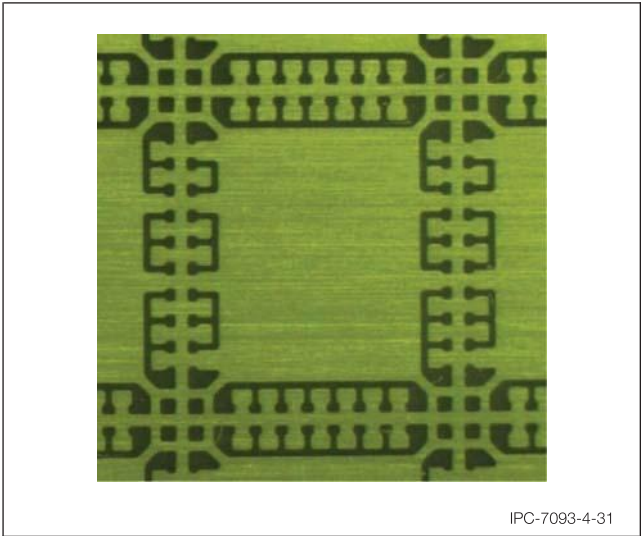


Figure 4-31 Detailed View of a Custom Site for a QFN

This leadframe is not square but measures 5 mm x 7 mm with 7 leads on one side and 9 on the other. In addition, leads on two sides are tied directly to the die paddle.

Another alternative is to split the thermal die pad. That option allows some thermal isolation of individual die.

4.5 Detailed Description of LGA, QFN and SON (DFN) Substrate-Based Packages

**4.5.1 Manufacturing Methods for Substrate-Based Packages** Substrate-based packages are similar to leadframe-based packages in many ways. Many devices that can be packaged using the leadframe approach could also be packaged using a substrate. For reasons having to do with cost and reliability, substrates are used as an alternative to leadframes in only small volume.

Substrates are sometimes used for individual die but more commonly to interconnect and package multiple active and passive components. Many of these assemblies are SiPs (system in a package) per the ITRS definition implying at least 2 different active components. Others that do not comply with the strict SiP definition are simply high density

electronic assemblies. The density is increased by using direct die attach, stacking die, flip chip assembly, 0201 and 01005 SMT parts.

The substrates used for BTC devices are essentially multi-layer circuit boards, often built with BT dielectric and frequently implemented utilizing HDI technology. Figures 4-32 and 4-33 show both sides of a typical substrate for a BTC part.

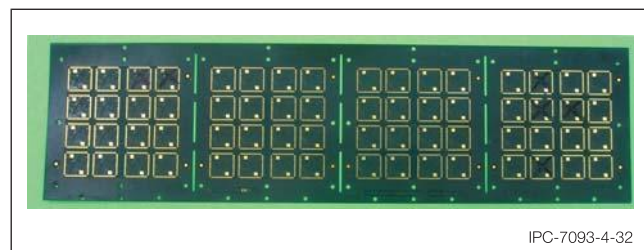


**Figure 4-32 Bottom View of Land Grid Array Printed Board**

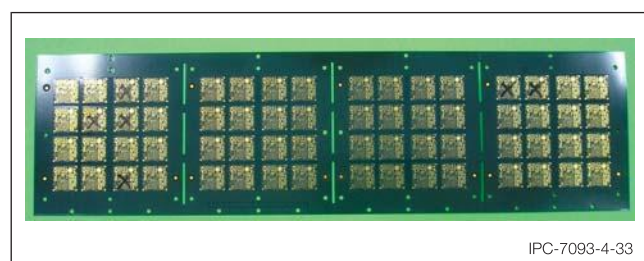


**Figure 4-33 Top View of Land Grid Array Printed Board**

The substrate measures ~75 mm x 300 mm. This bottom surface of the substrate is eventually soldered to the circuit board. Those sites with an “X” were found to be defective during board test and will not be populated. This particular substrate does not have a large pad in the center as many QFNs do because the final package does not dissipate a lot of heat so a good thermal connection to the circuit board on which the BTC device is attached is not required.

Figure 4-33 shows the top surface of the substrate where parts are placed. 0402 down to 01005 size SMT parts are commonly used. Die interconnect is either wire bond or flip chip, often with multiple die. 25 parts in a 7 mm x 7 mm size is common. Many of these assemblies are Systems in a Package (SiP).

A typical process flow to assemble a BTC using a substrate like that above is shown in Figure 4-34.

**4.5.2 Types of Defects** Some common defects that result from the BTC on substrate fabrication methods described are:

- delamination of the mold compound from the substrate that results in pulling parts off of the substrate
- mold compound flash on the leads that interferes with soldering

- voids resulting from complex internal geometry that is hard to fill or from mold compound that does not flow for some reason
- wire sweep in the molding process resulting in shorted wires or, less frequently, broken wires
- sawing induced defects such as delamination of the mold compound from the substrate
- warpage from the molding process or inherent in the substrate that interferes with the planarity of the part or the geometry of the solder joint
- movement or sweeping off of SMT parts due to excessive temperature rise during the molding process
- excess water uptake by the part during storage resulting in delamination during solder reflow

Table 4-6 shows some examples of common substrate based package defects. The table provides three levels of defect potential and highlights the possible causes.

**4.5.3 Marking Alternatives** Common methods of marking these packages are the same as those used with QFNs and SONs (DFN):

1. Pad printing with a high contrast ink, usually white
2. Laser marking to give finer features but often furnish a low contrast image
3. Laser marking onto a printed ink background provides good contrast as well as fine features

**4.5.4 Materials Used** Substrates are commonly built using standard circuit board fabrication methods. Many of the substrates incorporate HDI technology to increase density. Four-layer boards are common.

The most common dielectrics are BT and FR-4.

A variety of board finishes are used depending on choice of the designers working with both the substrate fabricator and the assembly house. Since most BTC substrate based packages incorporate some wire bonded die, gold finish on at least the component surface of the substrate is common. A typical system is NiPd with an Au flash that is wire bondable, solderable and avoids the risk of solder embrittlement.

A variety of molding compounds are used. The choice depends not only on the part and components within the QFN-SON, but the mold design and molding machine. These molding compounds are formulated to have excellent flow characteristics to ensure fill while minimizing wire sweep. They are also formulated to have a TCE that is close to copper and to comply with environmental requirements.

**4.6 Description of Commercial Variations** Many detailed variations of the QFN and SON (DFN) type of BTC have been developed. These are now marketed under a

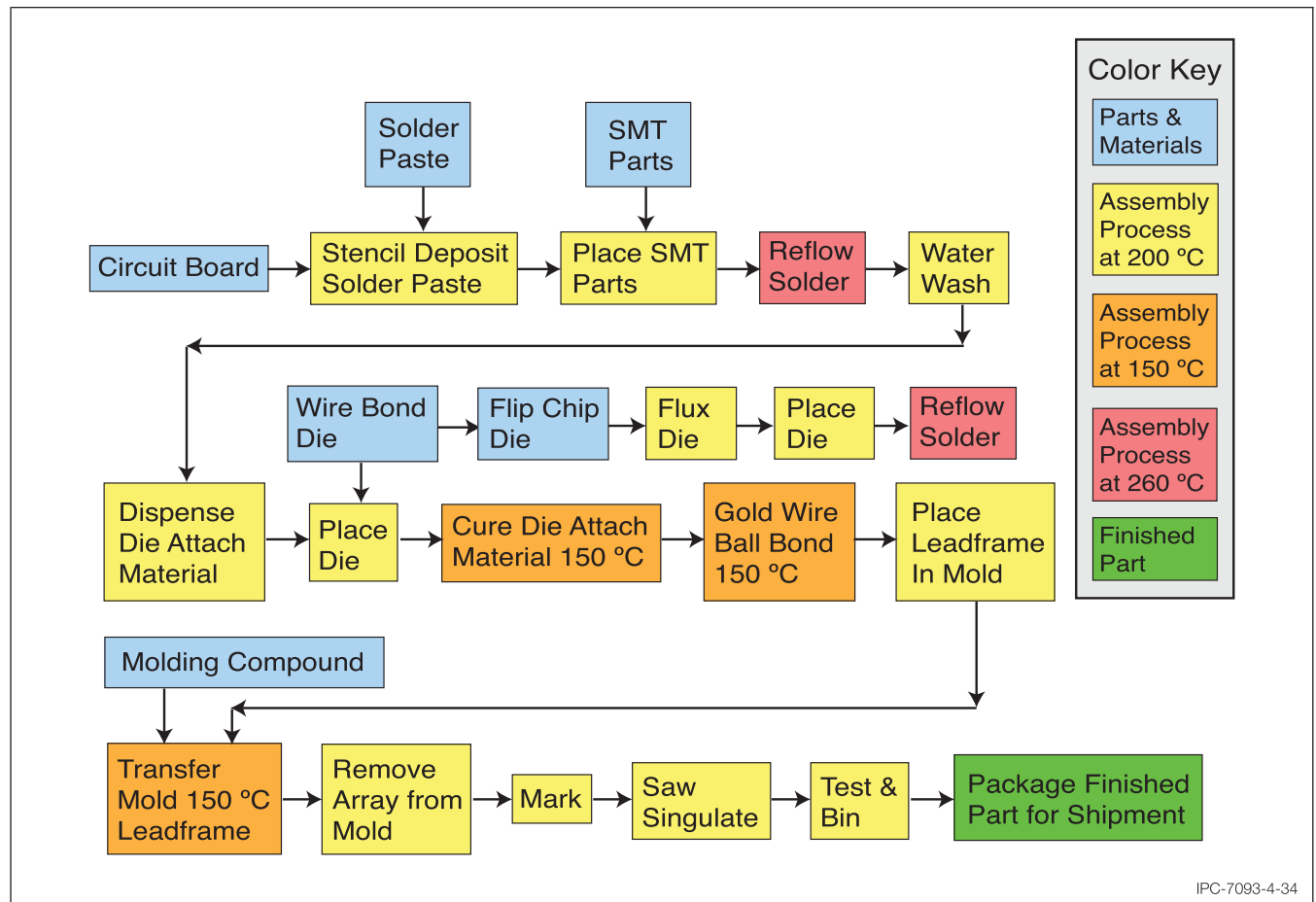


**Figure 4–34 BTC Fabrication on a Substrate with Saw Singulation**

broad number of trademarks and acronyms by various companies, a few of which are described below.

#### 4.6.1 Detailed Description of MLF®, MLP, and MLFP™ Components

**4.6.1.1 Part Descriptions** The microleadframe (MLF®), micro leadframe package (MLP) and micro leadframe plastic package (MLFP™) are all near CSP size plastic encapsulated quad contact configured no-lead (QFN) packages with a copper lead-frame substrate. This package family uses perimeter lands on the bottom of the package to provide electrical contact to the PCB. Typical of all QFN packaging, these variations offer a thermal enhancement by having the die attach paddle exposed on the bottom of the package surface to provide an efficient heat path when soldered directly to the PCB as exhibited in Figure 4–35.

Fairchild and Carsem's MLP (Micro Leadframe Package) are near chip-size plastic encased packages that are JEDEC MO-220 and MO-229 compliant QFN and SON (DFN) plastic packages. The high-density lead-frame package design is furnished with RoHS compliant lead-free plating and meets the most stringent moisture sensitivity level (MSL)1. To provide even greater utilization of package space and

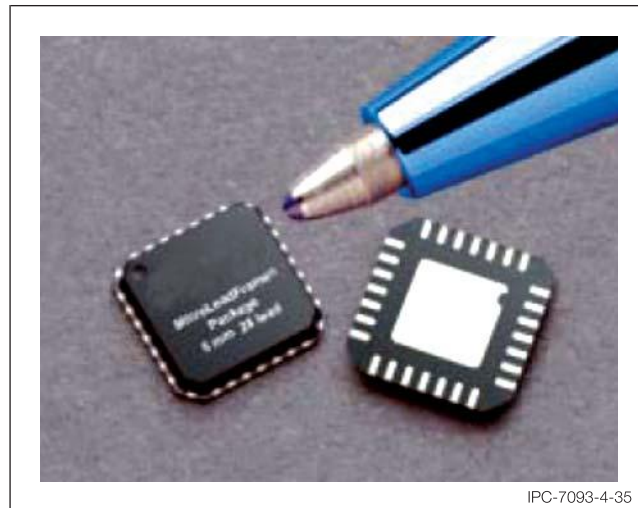
enhanced performance, MLPs have the bottom exposed thermal feature visible in Figure 4–36.

Carsem's MLP (Micro Leadframe Package) is a family of JEDEC compliant QFN plastic packages. This near CSP package is available in three versions. The Quad (MLPQ™) has 4 sides of I/Os with a body size range of 3 x 3 mm with 8 I/Os to 9 x 9 mm with 64 I/Os and body thickness options of 0.9 mm, 0.75 mm, plus the Ultra-Thin that is only 0.5 mm thick. The Micro (MLPM™) has 2 sides of I/Os with a body size range of 2 x 2 mm with 3 I/Os to 3 x 3 mm with 10 I/Os and a thickness of 0.9 mm. The Dual (MLPD™) versions are designed to provide a footprint compatible replacement for SOIC, SSOP, TSSOP and MSOP packages. Typical of most QFN and SON devices, MLPs have an exposed die attach pad for improved thermal performance. However, the company also offers a non-exposed pad option they refer to as COL™ (Chip On Lead), FCOL™ and other special applications.

The Micro Leadframe Plastic Package (MLFP) from Intersil is also a JEDEC standard package outline (EIA/JEDEC Publication 95, MO-220). Figure 4–37 illustrates a section view of a 16-Lead MLFP package. The die pad and perimeter I/O pads are fabricated from a planar copper

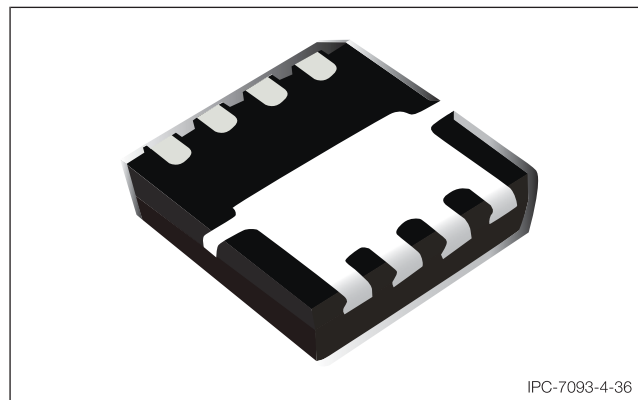
**Table 4-6 Substrate Based Package Defects and Failure Modes**

| <b>Substrate Based Package Defects and Failure Modes</b>                                                                          |                                                               |                                             |                                                                                                 |
|-----------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------|---------------------------------------------|-------------------------------------------------------------------------------------------------|
| <b>Defect/Failure Mode</b>                                                                                                        | <b>Potential Failure</b>                                      | <b>Detection method</b>                     | <b>Cause</b>                                                                                    |
| <b>Level 1, within package</b>                                                                                                    |                                                               |                                             |                                                                                                 |
| Excess water content due to inadequate storage or drying                                                                          | Pop corning, delamination during solder reflow                | Hard to detect                              | Water uptake from environment when parts are not stored or dried properly                       |
| Detrimental package compound voids                                                                                                | Corrosion, delamination                                       | Ultrasonic                                  | Poor molding control                                                                            |
| Cracked package                                                                                                                   | Mechanical and/or electrical failure                          | Ultrasonic                                  | Poor molding control or poor handling                                                           |
| Substrate to compound failure                                                                                                     | Broken connection, corrosion from water ingress               | Visual examination, die penetrant           | Molding or sawing process defect                                                                |
| Part to substrate delamination                                                                                                    | Open circuit, die overheating, bond wire break, part cracking | Ultrasonic, decapsulation, cross sectioning | Inadequate mold compound flow, poor wetting of parts and substrate, surface contamination       |
| Broken wire bonds                                                                                                                 | Electrical open                                               | X-ray                                       | Wire bonding process control error, mold compound sweep                                         |
| Lifted wire bond stitch/broken heel to substrate                                                                                  | Electrical open                                               | X-ray, electrical test                      | Wire bond process control error, surface contamination, inadequate plating                      |
| Lifted wire bond ball from die                                                                                                    | Electrical open                                               | X-ray, electrical test                      | Wire bond process control error, surface contamination, die metallization error                 |
| Shorted wire                                                                                                                      | Electrical short                                              | X-ray, electrical test                      | Mold wire sweep, or wire bond process control                                                   |
| <b>Level 2, outside of package</b>                                                                                                |                                                               |                                             |                                                                                                 |
| Non-wetting lead surfaces                                                                                                         | Open connection                                               | Visual, X-ray                               | Oxidized surfaces, plating contamination or thickness                                           |
| Out of dimensional spec                                                                                                           | Poor contact in test socket                                   | Measurement                                 | Molding (thickness) or singulation                                                              |
| Lead smear of copper                                                                                                              | Shorting of leads                                             | Visual                                      | Sawing conditions                                                                               |
| Inadequate flatness                                                                                                               | Open joints                                                   | Visual                                      | Substrate defect, Molding or singulation method                                                 |
| Burrs                                                                                                                             | Electrical shorts                                             | Visual                                      | Singulation process                                                                             |
| Dimples on pads cause by test socket contact                                                                                      | Void in solder joint and potential open connection            | Visual                                      | Aggressive probing breaks through plating resulting in non-wetting spot and void in final joint |
| Marking defects                                                                                                                   | Wrong part or unknown part                                    | Visual                                      | Poor marking, handling damage                                                                   |
| <b>Level 3, package to board</b>                                                                                                  |                                                               |                                             |                                                                                                 |
| Voiding in joints                                                                                                                 | Long term electrical open                                     | X-ray                                       | Solder paste or reflow process                                                                  |
| Non-wetting of pads                                                                                                               | Electrical open                                               | X-ray, electrical test                      | Part contamination or solder process                                                            |
| Bridging under package                                                                                                            | Electrical short                                              | X-ray, electrical test                      | Part or board contamination, solder process                                                     |
| Liftoff of package from PCB due to floating on the solder                                                                         | Electrical open, less shock resistance                        | Visual, cross-section                       | Too much solder paste                                                                           |
| Sinking of package into solder due to its weight causing detrimental solder displacement resulting in bridges and/or poor joints. | Electrical short                                              | X-ray, cross section                        | Part too heavy for reflow conditions, paste or solder rheology at temperature                   |



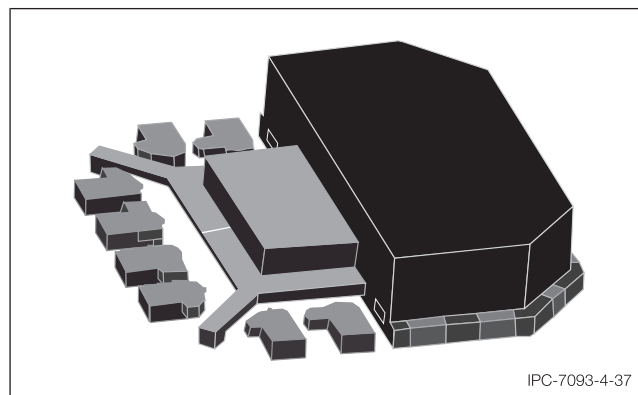
IPC-7093-4-35

**Figure 4-35 Amkor's 28 I/O MicroLeadFrame® Package**



IPC-7093-4-36

**Figure 4-36 Fairchild's MLP is a Thermally Enhanced SON Developed for Power Switch Technology**



IPC-7093-4-37

**Figure 4-37 Intersil's Quad No-lead Micro Leadframe Plastic Package (MLFP)**

lead-frame substrate. This family is described as plastic encapsulated device with the bottom of the die attach pad and contacts.

The die pad and perimeter I/O pads are fabricated from a planar copper lead-frame substrate. This is encapsulated in plastic with the bottom of the die attach pad (DAP) and I/O pads exposed to create a very small package outline. In

addition to furnishing a small outline the package has minimal mass and can be processed using the existing package assembly infrastructure

**4.6.1.2 Tolerances** Dimensions and tolerances conform to ANSI Y14.5M, all dimensions are in millimeters and angles are in degrees. Figure 4-38 represents the basic QFN package outline

The QFN family detailed in JEDEC registered outline MO-220 ranges in size from 2.0 mm x 2.0 mm to 12.0 mm x 12.0 mm graduating in 1.0 mm increments. For each outline there are two lead spacing formats, odd and even. The image shown in Figure 4-39 represents the even row variation.

There are five contact pitch variations allowed for the QFN; 1.0 mm, 0.8 mm, 0.65 mm, 0.50 mm and 0.40 mm. The length (L) and width of the contact can vary significantly between suppliers. Although square outlines are most common, rectangular outlines are allowed. The examples shown in Table 4-7 are represent a number of square and rectangular QFN package outlines currently available from a prominent package assembly service provider.

**4.6.1.3 Material Specification** QFN packages are available in several alloy finishes: post plated SnPb, Matte Sn, SnBi, pre-plated NiPd with flash of Au. Surface mount studies on parts plated with NiPd and Matte Sn show no significant difference compared to SnPb finish parts. The following are typical of the basic materials used for QFN package assembly:

- Die thickness: 250  $\mu\text{m} \pm 50 \mu\text{m}$  (thinner for special applications)
- Plating: Sn/Pb, Matte Sn, SnBi, NiPd (flash Au)
- Marking: Laser
- Lead-frame: Copper Alloy, Dual gauge
- Die attach: Conductive Epoxy
- Bond Wire: 25  $\mu\text{m}$  low loop
- Mold compound: Pb-free/Green capable

**4.6.2 Detailed Description of LLC™ and LFCSP™ Components** The LLC from Analog Devices and LFCSP from National Semiconductor are near chip scale plastic encapsulated wire bond QFN packages with a copper leadframe substrate in a BTC package format.

**4.6.2.1 Part Description** The LLP and LFCSP package is available in two thicknesses variations. The 0.8 mm is the most prevalent thickness but the package is selectively available in a lower 0.6 mm profile thickness as well. Perimeter input/output pads are located on the outside edges of the package. Electrical contact to the printed circuit board (PCB) is made by soldering the perimeter pads and exposed

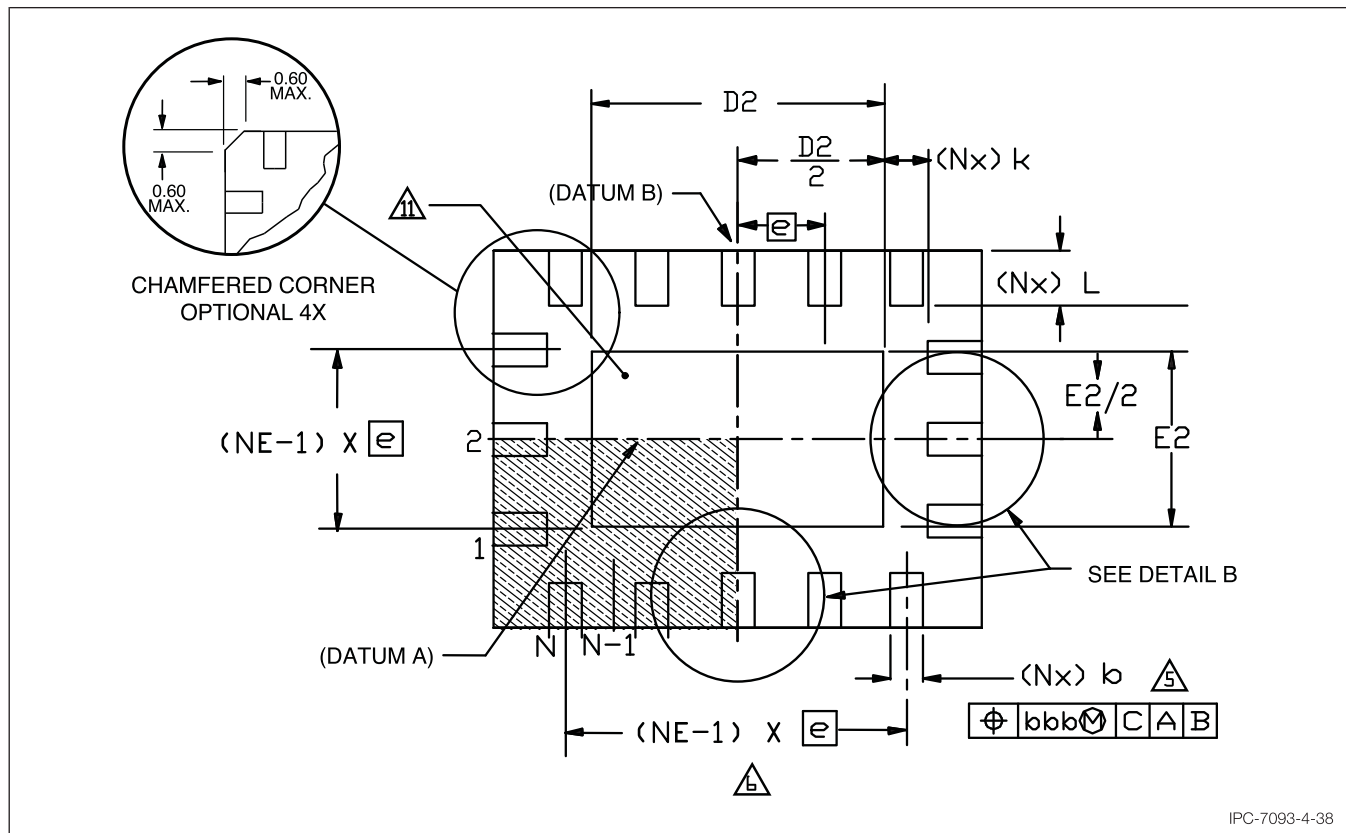


Figure 4-38 JEDEC MO-220 Package Outline

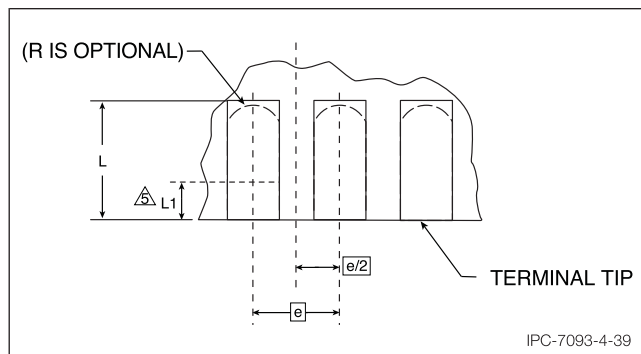


Figure 4-39 QFN Contact Design

paddle on the bottom surface of the package to the PCB. Heat is efficiently conducted from the package by soldering the exposed thermal paddle to the PCB as illustrated in Figure 4-40.

Stable electrical ground connections are provided through down bonds and through conductive die attach material. Wire bonding is provided using gold wires. Perimeter and thermal pad finish is plated as 100% Sn (Sn/Pb is available as well). Packages are punched or sawed from a molded strip during final assembly. Half-etching of the leadframe provides mold compound locking features for the perimeter pads and die thermal paddle. This package is currently characterized as moisture sensitivity level (MSL) 3 (see IPC/JEDEC J-STD-020 for MSL levels).

#### Terminal contacts:

- The contact pads (or solder pad) are located peripherally in single row format depending on the specific number of pins and body size.
- For certain specific applications the packages are incorporated with common power and/or ground pins
- All contacts are plated with matte tin solder for ease of surface mount processing.

The bottom termination QFN package family (see JEDEC MO-220) furnishes enhanced chip speed, reduced thermal impedance, and, because of its small outline, minimizes the printed circuit board area required for mounting. The small size and very low profile make this package, shown in Figure 4-41, ideal for high density PCBs used in small-scale electronic applications such as cellular phones, pagers, and handheld PDAs.

In addition to their small package outline and low profile the LLP and LFCSP have a low thermal resistance and reduced electrical parasitic.

**4.6.2.2 Package Tolerances** This JEDEC design guideline standard for this package family applies to packages with optional thermal enhancements as well as various height profiles and pitches. This package has terminals on all four edges of the bottom surface of the package. The LLC and LFCSP can have either a square or a rectangular

Table 4-7 Typical Package Outline and I/O for QFN

| Body Size (mm)     | QFN lead counts<br>0.8, 0.65, 0.5, 0.4 mm pitch | DFN/SON lead counts<br>1.27, 0.95, 0.5 mm pitch | Dual Row lead counts<br>0.5 mm pitch |
|--------------------|-------------------------------------------------|-------------------------------------------------|--------------------------------------|
| < 2 x 2 (saw only) | -                                               | 4 / 6 / 8                                       | -                                    |
| 2 x 3              | -                                               | 6 / 8                                           | -                                    |
| 3 x 3              | 4 / 8 / 10 / 12 / 16                            | 8 / 10                                          | -                                    |
| 4 x 4              | 12 / 16 / 20 / 24 / 28                          | -                                               | -                                    |
| 5 x 5              | 16 / 20 / 28 / 32 / 36                          | -                                               | 44 / 52                              |
| 6 x 5              | 36                                              | 8                                               | -                                    |
| 6 x 6              | 20 / 28 / 36 / 40 / 48                          | -                                               | 60/68                                |
| 7 x 7              | 28 / 32 / 44 / 48 / 56                          | -                                               | 76 / 84                              |
| 8 x 8              | 32 / 40 / 52 / 56 / 68                          | -                                               | 92 / 100                             |
| 9 x 9              | 36 / 44 / 60 / 64 / 76                          | -                                               | 108 / 116                            |
| 10 x 10            | 44 / 52 / 68 / 72 / 88                          | -                                               | 124 / 132                            |
| 11 x 11            | -                                               | -                                               | 140 / 148                            |
| 12 x 12            | 48 / 60 / 84 / 88 / 100                         | -                                               | 156 / 164                            |

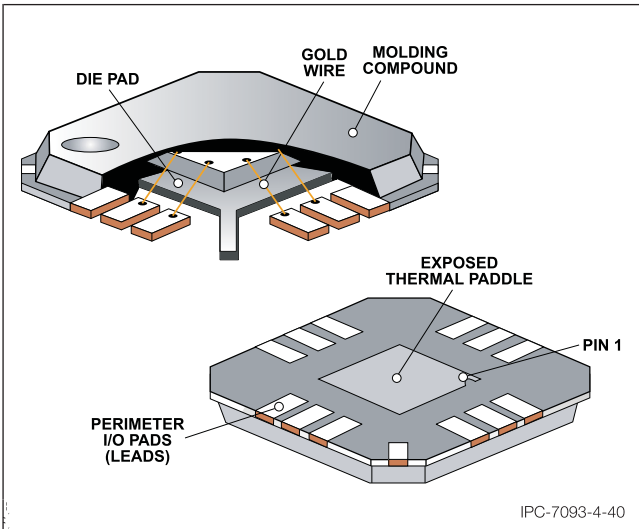


Figure 4-40 Analog Devices LFCSP™ (Leadframe Chip-Scale Package)

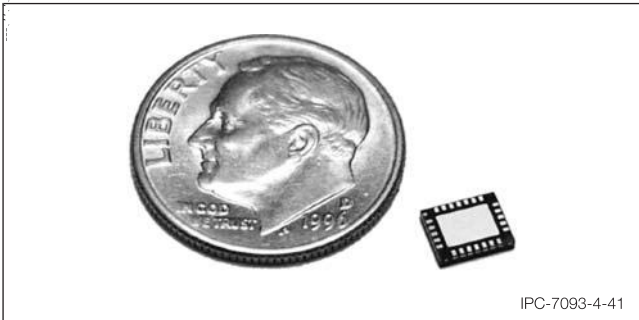


Figure 4-41 National Semiconductor LLP™ (Leadless Package)

body outline as well as either symmetric or asymmetric terminal patterns. Versions of the package may also have terminals placed in the corners at 45 degrees to neighboring leads. The basic dimensions for the package outline are shown in increments of 0.50 mm ranging from 1.00 mm

through 12.00 mm. The outline detail shown in Figure 4-42 illustrates the primary dimensions used when developing the land pattern and thermal paddle geometries.

The width of the metallized terminals (including lead finish) exposed at the bottom surface of the package is detailed in Table 4-8.

For component tolerances and profile tolerances usually given in the package outline drawings are converted into maximum material condition (MMC) and least material condition (LMC) based tolerances.

**4.6.2.3 Material Specifications** In compliance with RoHS and WEEE, companies modified molding compounds and, in some cases, die attach materials. In addition, there was strong support from users for converting mold compounds to more robust versions so that packages are compatible with higher temperatures required for reflow soldering lead-free alloys. The data supplied in Table 4-9 is typical of the device packaging materials listed in a ‘materials declaration’ form for the LLC and LFCSP.

The change to RoHS compliant elements provided base material sets that demonstrate capability to meet elevated reflow conditions of 255°C (+5/-0°C) for lead-free reflow. Additionally, most companies are offering lead-free lead finish on all plastic encased LFCSP packages from Sn85Pb15 to 100% Sn (tin plating) to eliminate Pb from these package types.

Other material elements:

- |                            |              |
|----------------------------|--------------|
| Internal leadframe plating | Ag (silver)  |
| External leadframe plating | Sn (tin)     |
| Bond wires                 | Au (gold)    |
| Die element                | Si (silicon) |

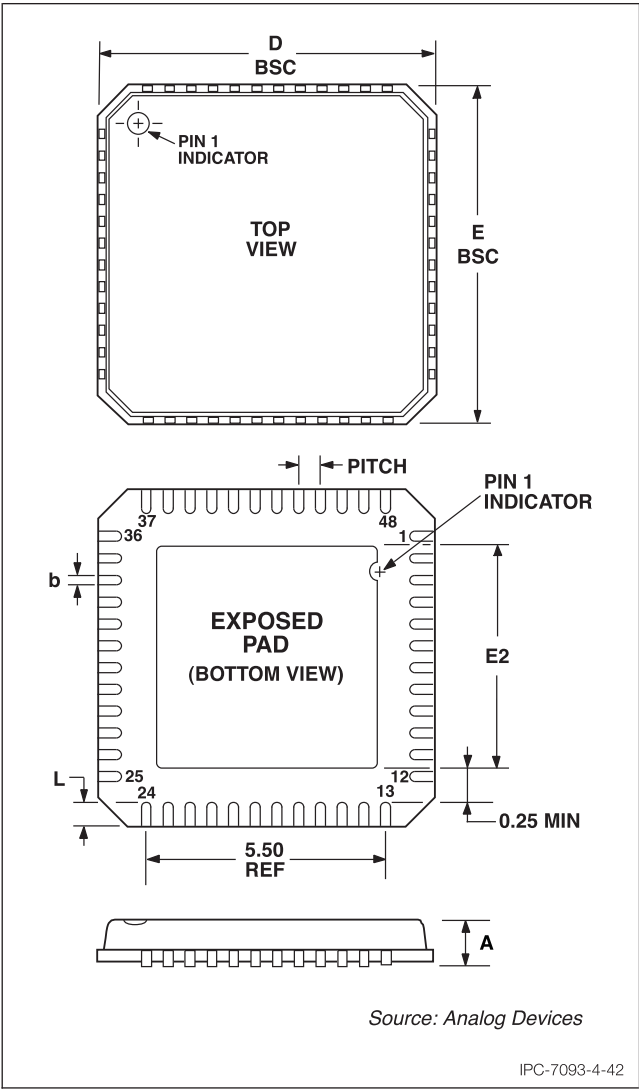


Figure 4-42 Typical LLC and LFCSP Outline Detail

Table 4-8 Contact Pitch and Width Variations

| Contact Pitch | Terminal Dimensions |         |         |
|---------------|---------------------|---------|---------|
|               | Minimum             | Nominal | Maximum |
| 0.65          | 0.25                | 0.30    | 0.35    |
| 0.50          | 0.18                | 0.25    | 0.30    |
| 0.40          | 0.15                | 0.20    | 0.25    |

Although no change may be made to a component’s part number, products converted to lead-free will be identified on the outer packaging label, and if space permits, a Pb-free symbol will be marked on converted devices.

**4.7 Packaging and Handling** BTC parts are shipped in a variety of standard configurations designed for automated assembly system efficiency. QFN products and BTC devices built on substrates are shipped in tubes, stackable JEDEC

Table 4-9 Basic Material Elements for the LLC and LFCSP Devices

| Category            | Materials               | Content |
|---------------------|-------------------------|---------|
| Mold compounds      | SiO2 Fillers            | 86.9%   |
|                     | Epoxy and Phenol Resins | 12.8%   |
|                     | Carbon Black            | 0.3%    |
| Die attach material | Ag (silver)             | 73.4%   |
|                     | Epoxy Resin             | 18.35%  |
|                     | Metal Oxide             | 2.75%   |
|                     | Curing Agents           | 2.75%   |
|                     | Gamma Butyrolacetone    | 2.75%   |
| Leadframe           | Cu (copper)             | 97.5%   |
|                     | Fe (Iron)               | 2.35%   |
|                     | Zn (zinc)               | 0.12%   |
|                     | P (phosphorus)          | 0.03%   |

tray carriers (Figure 4-43), or in tape and reel. SON (DFN) devices are commonly shipped in tubes or tape and reel.

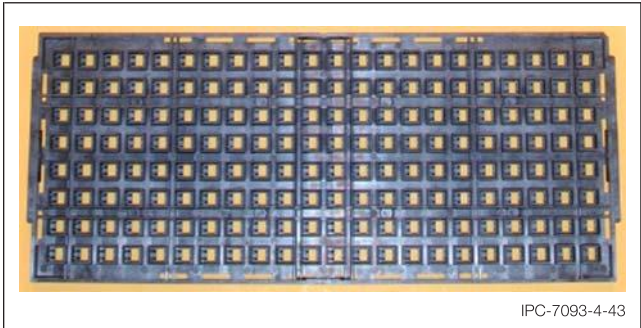


Figure 4-43 JEDEC Tray Carrier Format

The overall dimensions of the JEDEC shipping and handling tray carrier are 135.9 mm x 322.6 mm with components arranged in a column and row format. The matrix of the pocket pattern is fixed to a standard formula based on the outline of the semiconductor package. Although the components mounted in the carrier are shipped with a ‘dry pack’ wrapping, the plastic material used to mold the carrier must withstand thermal exposure typical of that required for ‘bake-out’ of components that are exposed to ambient conditions and prone to moisture retention. For more detailed information on the carrier tray specification see JEDEC Publication 95 Design Guide 4.10.

All of these package delivery systems use ESD safe materials.

The environmental conditions these devices are designed to tolerate are:

- Moisture sensitivity JEDEC Level 1\* characterization 85°C/85%, 168 hours
- HAST 130°C/85% RH, 96 hours
- Temp cycle -65/+150°C, 1000 cycles
- Temp/Humidity 85°C/85% RH, 1000 hours
- High temp storage 150°C, 1000 hours

## 5 MOUNTING STRUCTURES

This section provides information on the various materials and concepts used to produce a mounting structure onto which the BTC may be placed and properly attached. Also included in addition to the physical requirements will be electrical, thermal and construction detail intended to provide a clear correlation with the BTC design and assembly process. Some new techniques for providing interconnection concepts will be explored as well as a method for embedding the BTC into the mounting structure.

**5.1 Types of Mounting Structures** PCBs and other similar types of interconnection platforms serve as the mounting structures for BTCs and other components. There are a variety of alternative mounting structures available which serve BTC needs as interconnection substrates for electronic assemblies. These structures employ a wide range of materials, both organic and inorganic and have a wide range of physical properties. Materials choice is normally made based on cost/performance needs of the finished product.

**5.1.1 Organic Resin Systems** Organic substrates are the most commonly used in the construction of electronic interconnection structures. There is a well-established worldwide manufacturing base for this type of product. As a result of the large manufacturing base, this type of interconnection structure has the lowest cost among the competing technologies. Organic materials have intrinsic beneficial electrical properties. Most notable is a relatively low dielectric constant on average which can be made much lower by the proper choice of resin and reinforcement. Organic substrates are commonly reinforced using an appropriate material such as woven glass cloth; however, flexible circuit materials are not commonly reinforced.

**5.1.2 Inorganic Structures** Inorganic substrates are alternatives to the organic substrates; they are usually refractory materials comprised of sintered metal oxides. While they are typically brittle, they have some significant benefits not easily obtained with organic substrates.

Chief among the advantages are excellent thermal properties. Like organic structures, there are a number of possible choices available: ceramic, silicon, and enameled metals. The dielectric properties of these materials tend to be higher than organic based materials and, because they are brittle, they are generally more prone to breakage. Because of the more limited vendor base for inorganic substrates, these structures are normally more expensive.

**5.1.3 Layering (Multilayer, Sequential or Build-Up and HDI)** While single and two metal layer circuits are still common, multilayer interconnection structures are commonly required to support the interconnection of BTCs in today's high performance electronics. There are several

approaches to creating multilayer circuit product. The traditional multilayer is created by printing and etching thin layers of copper clad substrates and laminating them into a monolithic structure which can be drilled and plated so as to make connection between the layers where required.

More recently, however, alternative structures have been developed to address the higher density and routing difficulties associated with BTCs. These newer structures employ a variety of different approaches to create suitable multilayer structures. The new structures are referred to as High Density Interconnect (HDI) printed boards and include build-up multilayers, sequential multilayers and co-laminated multilayers.

A key feature of these structures is their use of very small vias. The term microvias has been applied to describe these miniscule interconnections. A typical microvia is less than 150  $\mu\text{m}$  in diameter and has a capture land (where the via starts) and a smaller target land (where the via ends). Figure 5-1 shows one of the most popular HDI structures, although methods of stacking the micro vias have also been developed as shown in IPC-2226.

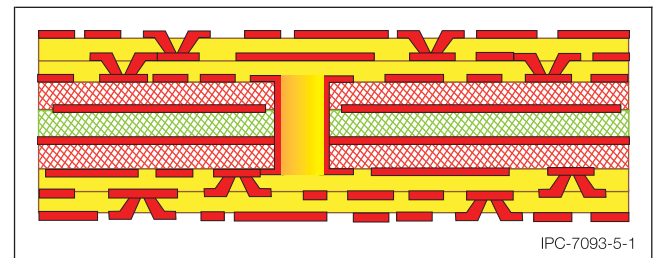


**Figure 5-1 Typical Build-Up HDI Platform, 2[4]2 Layer Configuration**

**5.2 Properties of Mounting Structures** Mounting structures for BTCs are identical to those that satisfy the needs of many different component package configurations. These configurations drive the complexity of the mounting structure and determines the resin, reinforcement and, for many applications, the metallic configuration of the surface to which the components are attached.

PTH vias connect the PCB thermal pad to any electrically appropriate internal PCB plane(s). For double-sided PCBs, the un-tented PTH vias has the potential for solder, during wave soldering of mixed assembly, to reach the PCB top side and cause secondary reflow, leading to potential opens and shorts. So PTH vias should be plated shut, plugged with epoxy or tented with solder mask to avoid low package stand-off height due to solder wicking into the PTH vias during the reflow process. However, plating of vias shut may increase PCB cost.

To achieve the highest possible thermal performance, it is good to use a maximum number of PTH vias, but it is important to keep in mind that they do impact the soldering surface of the PCB thermal pad. A recommended via pattern

is 0.3 mm PTH via drill diameter on 1 mm centers but much smaller vias are also being used. Improved thermal performance can be obtained with a greater density of vias and larger vias on the same pattern that provides good solderability.

**5.2.1 Resin Systems** There are a number of different resin systems suitable for use in organic laminate construction. There is a long and well understood history and years of faithful service for the traditional resins systems. However, to support the move to meet legislated lead-free requirements by the EU, many new resins are being developed to meet the higher temperature assembly reflow requirements. Test methods have been developed, i.e.,  $T_d$  (Temperature of decomposition) and T260, T288, T300 (Time to Delaminate), to quantify material properties for conformance to the new EU requirements. Some of the new resin systems are classified to new material slash sheets such as IPC-4101 /99, /101, /121, /124, /126 and /129.

**5.2.1.1 Epoxy** There are a number of different resin systems that can be used to create a printed wiring substrate. Epoxy is among the organic resins with the longest history and it is one of the most commonly used resin systems for PCBs. It offers a good blend of physical, electrical and processing properties at reasonable cost. The general properties are provided in Table 5–1. Higher temperature capability epoxy resin systems have been developed for lead-free applications and are available at a cost premium.

**5.2.1.2 Polyimide** Polyimide offers the highest operating temperature among resin systems in use today. It has been a favorite for military applications where the potential for board rework and repair in the field with uncontrolled soldering tools is anticipated. Because of its high glass transition temperature, polyimide provides a safety margin and potential to reduce damage to the board when uncontrolled soldering irons are used to remove or replace a component. The general properties are provided in Table 5–1.

**5.2.1.3 Bismaleimide Triazine** Bismaleimide triazine or BT resin is the most popular choice for the construction of some semiconductor packages including BTCs, because of its combined advantages of high temperature capability at reasonable cost. The general properties are provided in Table 5–1.

**5.2.2 Reinforcements** Reinforcements provide the dimensional stability and the bulk of the mechanical properties of the organic substrate laminate. Following are some of the more commonly used reinforcements.

**5.2.2.1 Glass Cloth** Glass cloths are the most commonly used reinforcement for printed board substrates. They are

widely available and are processed with relative ease. The cloths are available in a number of different thicknesses and weaves. The chemical make-up of the glass can vary and can affect the electrical properties. Presently, E type glass is the most commonly used glass cloth for printed circuit substrates.

**5.2.2.2 Glass Felt** Glass felt or non-woven glass mat has been commonly used as a reinforcement material for fluoroplastic resins and is commonly used in low loss, RF or microwave applications. It has seen some application in formable laminates as well but the technology is not widespread.

**5.2.2.3 Aramid Cloth** Aramid cloth has been used to reinforce certain laminates. It is unusual in that it has a negative CTE in the X and Y direction, which helps to offset the in-plane CTE of the resin. Because of the counteracting expansion and contraction, laminate materials of this combination can match approximately the CTE of ceramic. However, a drawback of the material is that the aramid has Z axis CTE much higher than glass and, in thermal excursions, can fracture nearby resin, leaving micro-cracks along the surface of the fibers.

**5.2.2.4 Aramid Paper** The supply of non-woven aramid paper has diminished due to a lack of manufacturing sources. Aramid papers have been effectively used in a number of multilayer applications. They have most of the benefits of the aramid cloth with more process latitude. They are often used for thin core layers at or near the surfaces of the multilayer printed boards to better control CTE. Because the aramid is organic, it has the added advantage of being more easily processed by laser ablation and can also be processed using plasma etching for making holes. The organic nature of the material also helps to keep the dielectric constant low.

**5.2.3 Reliability Concerns with High Temperature Lead-Free Soldering** The higher temperatures required for soldering lead-free solders creates reliability concerns for the survivability of the PCB resins as well as the integrity of the PCB interconnect structures, such as plated-through holes and vias.

The properties that are most important in this respect are the thermal expansion, the glass transition temperature and the decomposition temperature. The thermal expansion from 50–260°C,  $TE(50-260^\circ C)$  is a composite of the thermal expansions below and above the glass transition temperature. The glass transition temperature ( $T_g$ ) is the temperature at which an amorphous polymer, or the amorphous regions in a partially-crystalline polymer, changes from being in a hard and relatively-brittle condition to being in a viscous or rubbery condition. These different molecular

**Table 5-1 Environmental Properties of Common Dielectric Materials**

| Environmental Property                                                            | Material                   |                               |                              |                                    |           |                  |
|-----------------------------------------------------------------------------------|----------------------------|-------------------------------|------------------------------|------------------------------------|-----------|------------------|
|                                                                                   | FR-4<br>(Epoxy<br>E-glass) | Multi-<br>Functional<br>Epoxy | High<br>Performance<br>Epoxy | Bismaleimide<br>Triazine/<br>Epoxy | Polyimide | Cyanate<br>Ester |
| Coefficient of Thermal Expansion, xy-plane, CTE(xy) (ppm/°C)                      | 16 - 19                    | 14 - 18                       | 14 - 18                      | ~15                                | 8 - 18    | ~15              |
| Coefficient of Thermal Expansion, z-axis below $T_g^1$ , CTE(z,< $T_g$ ) (ppm/°C) | 50 - 85                    | 44 - 80                       | ~44                          | ~70                                | 35 - 70   | ~81              |
| Coefficient of Thermal Expansion z-axis above $T_g^1$ , CTE(z,> $T_g$ ) (ppm/°C)  | 240 - 390                  | 240 - 390                     | 240 - 390                    | TBD                                | TBD       | TBD              |
| Thermal Expansion z-axis, TE(50–260°C) (%)                                        | 3.0 - 4.5                  | 2.5 - 4.0                     | 2.0 - 3.5                    | TBD                                | TBD       | TBD              |
| Glass Transition Temperature <sup>2</sup> , $T_g$ (°C)                            | 110 - 140                  | 130 - 160                     | 165 - 190                    | 175 - 200                          | 220 - 280 | 180 - 260        |
| Decomposition Temperature <sup>3</sup> , $T_d$ (5%) (°C)                          | 310 - 330                  | 320 - 350                     | 330 - 400                    | ~334                               | ~376      | ~376             |
| Soldering Temperature Impact Index <sup>4</sup> , STII                            | 170 - 205                  | 200 - 220                     | 215 - 260                    | TBD                                | TBD       | TBD              |
| Flexural Modulus (GPa)                                                            |                            |                               |                              |                                    |           |                  |
| Fill <sup>5</sup>                                                                 | 18.6                       | 18.6                          | 19.3                         | 20.7                               | 26.9      | 20.7             |
| Warp <sup>6</sup>                                                                 | 12.0                       | 20.7                          | 22.0                         | 24.1                               | 28.9      | 22.0             |
| Tensile Strength (MPa)                                                            |                            |                               |                              |                                    |           |                  |
| Fill <sup>5</sup>                                                                 | 413                        | 413                           | 413                          | 393                                | 482       | 345              |
| Warp <sup>6</sup>                                                                 | 482                        | 448                           | 524                          | 427                                | 551       | 413              |
| Water Absorption (wt%)                                                            | 0.5                        | 0.1                           | 0.3                          | 1.3                                | 1.3       | 0.8              |

**Notes:**

1. CTE (z,< $T_g$ ) is also known as Alpha 1, and CTE(z,> $T_g$ ) as Alpha 2. Contact supplier for specific values of the other materials.
2. The glass transition temperature can be measured by three different methods (TMA, DSC, DMA). Of these the values obtained by TMA are the most pertinent for the purpose of assessing reliability issues. A very rough relationship between the results of these three methods is  $T_g$  (TMA) =  $T_g$  (DSC) -10°C ≈  $T_g$  (DMA) -20°C. Contact supplier for specific values of other materials.
3. The decomposition temperature can be measured to two different values of weight loss,  $T_d$  (2%) and  $T_d$  (5%).  $T_d$  (5%) is more commonly used, but  $T_d$  (2%) is becoming popular because of its greater usefulness. Contact supplier for specific values of other materials.
4. Soldering Temperature Impact Index, STII, which is defined as  $STII = T_g/2 + T_d/2 - (TE\% (50 \text{ to } 260^\circ\text{C}) \times 10)$ .
5. Fill – yarns that are woven in a crosswise direction of the fabric.
6. Warp (cloth) – yarns that are woven in a lengthwise direction of the fabric.

structures result in very different physical properties. See Figure 5–2. The decomposition temperature ( $T_d$ ) measures the temperature at which the resin decomposes irreversibly, and thereby loses weight; typically the temperature to a weight loss of 2% or 5% is measured.

The impact of these three properties is captured with the Soldering Temperature Impact Index, STII, which is defined as  $STII = T_g/2 + T_d/2 - (TE\% (50\text{--}260^\circ\text{C}) \times 10)$ . This equation relates to the material  $T_g$  and  $T_d$  plus the thermal expansion characteristics. See Table 5–1.

Where:

$T_g$  is the laminate glass transition temperature

$T_d$  is the temperature that the material decomposes

TE is the thermal expansion from 50 to 260°C in percent

**5.2.4 Thermal Expansion** Thermal expansion is usually characterized in terms of changes to the x-y plane, which is

controlled primarily by the reinforcement of the material. The x-y expansion will have the greatest effect on surface mounted components and their reliability. Thermal expansion also occurs in the z-axis at a rate significantly larger than in the x-y plane, particularly at temperatures above the  $T_g$ . The z-axis expansion will have its greatest effect on plated-through hole and via reliability.

Table 5–1 shows the conditions for various reinforced resin types. All thermal expansion is measured in parts/million/change in temperature (°C).

**5.2.5 Moisture Absorption** Most organic materials are hygroscopic to some degree and soak up moisture at different rates; some do so relatively rapidly. This moisture absorption changes the electrical properties of the material such as loss tangent and as well the processing characteristics of the material as outgassing can result in blisters. It can also impact physical dimensions and the laminate's weight.

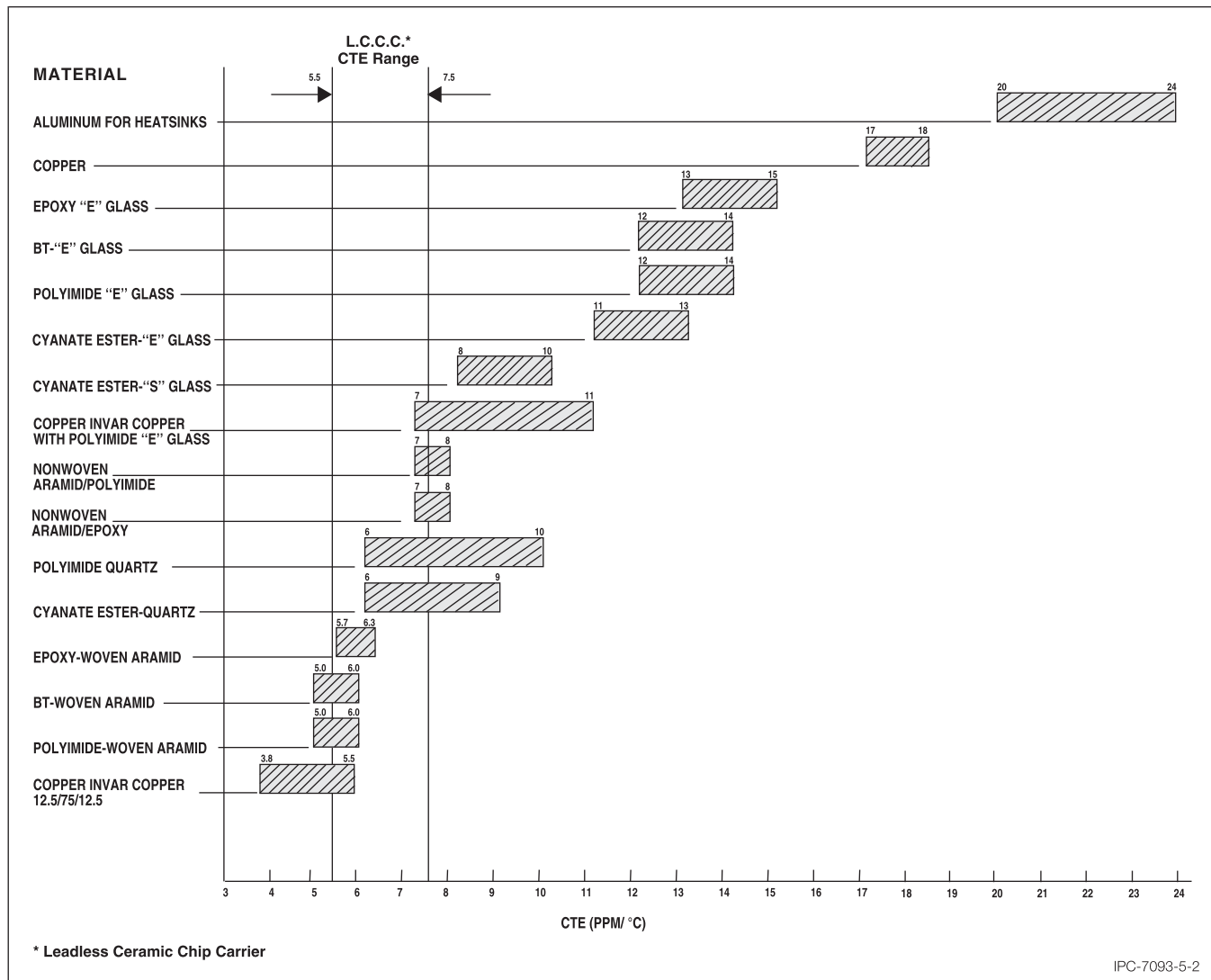


**Figure 5-2 Material Thermal Expansion Comparison**

Thus a simple way to determine that the material has absorbed moisture is to note the increase in weight under defined moisture exposure conditions. Table 5-1 shows the water absorption rate by weight for the various materials highlighted in this section.

**5.2.6 Flatness (Bow and Twist)** The planarity of 1.5, 2.25 and 3.0 millimeter thick boards varies, especially with respect to being able to assemble BTC type parts. Flatness is measured in relationship to the length and width of the laminate or the completed printed board. The term bow is applied to the longest dimension of the part; whereas, twist requirements are applied to the length across the diagonal distance. These requirements are usually set as a percentage allowance of the distance in question. Thus, the allowable bow of a printed board might be specified as 0.50% of the length of the longest dimension.

The key to flatness in regards to the mount of BTCs, however, needs to be evaluated based on localized flatness measurement with such techniques as shadow moire imag-

ing. This technology allows local flatness measurement at room temperature, and also at the elevated temperatures (e.g., 260°C) for implementing lead-free soldering. Traditional techniques of measuring overall board flatness do not reflect the problems in attaching high terminal count BTCs to certain local areas of a board.

**5.3 Surface Finishes** Printed board surface finishes serve several functions, these include: solderability provision and protection, reliable contact surface for contacts/switches, wire bondable surface, and solder joint interface. Although BTCs are the focus of this document, the other components and assembly operations of the printed board must be taken into consideration when choosing the most appropriate surface finish. There is no single surface finish that will be best for all applications.

While no surface finish is ideal for all applications, the search continues for improved surface finish solutions. Because of the component mix many have been satisfied with some of the immersion surface finishes, immersion

silver in particular, however since the emphasis on mounting BTCs is to make sure that there is sufficient solder volume some companies still require some form of solder as the preferred finish. The concern is mainly the uniformity of the final board finish as well as the flatness of the plating or coating on the land to which the BTC will be attached.

Some of the application features are provided in Table 5–2.

**5.3.1 Hot Air Solder Leveling (HASL)** The surface finish of long standing is hot air solder leveling (HASL). In this process, the finished printed board is dipped either vertically or horizontally into a molten solder bath and the excess solder is blown away and leveled with hot air, giving the process its name. The HASL process is the first soldering stress that the printed board experiences. Some material combinations may be prone to delamination during the multiple excess temperature exposures.

The HASL finish provides a virtual guarantee of solderability in that the process creates one half of the soldered joint by fully wetting the copper substrate. The quality of the product regarding solderability can be confirmed easily through a simple dip test, conditioned by an aging process or by simple visual inspection. Any evidence of non-wetting or dewetting is immediately apparent as the board exits the process.

The HASL solder surface finish provides a long solderable shelf life. Solderability is lost only when the intermetallic has grown through the surface. Thus, a properly applied coating can last more than a year if stored correctly. In addition, the coating’s solderability properties will survive several cycles of adhesive cure or paste reflow.

**5.3.1.1 Tin Lead HASL** Although the tin lead surface finish was the main solution for many printed boards, one concern with the HASL process is the coating thickness uniformity. Often in the process, the solder thickness varies

widely from 0.75 µm to 35 µm. It is generally held that the lower thickness is not acceptable because the very thin layer of solder is completely transformed into copper-tin intermetallic, which has very poor solderability. However, studies on the solderability evaluation of printed boards with HASL and other protective coatings indicate that soldering performance as indicated by visual examination showed no correlation to the solder thickness or solder coverage on the lands observed in cross-sections. As a result, acceptance criteria for the solderability of printed circuit boards should be based on functional testing of sample boards.

The wide variation seen in solder thickness in HASL affects the coplanarity of solder termination on the printed board and hence the components. Moreover, the uneven surface makes more difficult the paste-printing task, because it makes it more difficult to achieve good sealing of the stencil while printing. Lack of a good seal or “gasketing” will result in leakage of solder paste beneath the stencil. The result is that the manufacturer must either increase the frequency of cleaning (thus lowering throughput) or risk increased potential for bridging (thus lowering yield).

**5.3.1.2 Lead-Free HASL** The lead-free hot air solder leveling process has proven to provide both quality and reliability of the surface finish in providing long shelf life solderability. The most likely candidates for lead-free HASL are Sn-Cu eutectic (227°C melting point), or Sn-Ag-Cu eutectic (217°C melting point). Other SAC alloys such as 105, 305 or others may also be candidates. The Sn-Ag-Cu alloy appears to offer an advantage due to its lower melting point, but there are also advantages of the tin-copper system since the raw materials are readily available, and represent the lowest cost. The Sn-Cu solder pool is easy to manage and recycle since there are only two constituents. The solder bath is not too aggressive, has low copper pick up characteristics, and is relatively tolerant of common impurities.

Table 5-2 Key Attributes for Various Board Surface Finishes

|                                       | HASL<br>SnPb/SnCu <sup>1</sup>   | OSP                                    | Electroless<br>Ni/Immersion<br>AU | Electrolytic<br>Ni/Electroplated<br>AU | Immersion<br>Silver <sup>2</sup> | Immersion Tin             |
|---------------------------------------|----------------------------------|----------------------------------------|-----------------------------------|----------------------------------------|----------------------------------|---------------------------|
| Shelf Life<br>proper<br>Handling      | 1 Year                           | 6 Months                               | > 1 Year                          | > 1 Year                               | 6 Months                         | 6 Months                  |
| Handling                              | Normal                           | Avoid physical<br>contact              | Normal                            | Normal                                 | Avoid physical<br>contact        | Avoid physical<br>contact |
| SMT land Sur-<br>face topology        | Domed/Not flat                   | Flat                                   | Flat                              | Flat                                   | Flat                             | Flat                      |
| Multiple<br>assembly<br>reflow cycles | Good, need<br>robust<br>laminate | Fair, better<br>with thick<br>coatings | Good                              | Good                                   | Fair/Good                        | Fair/Good                 |

Notes:

- 1. Tin copper alloy is the preferred alloy for lead-free HASL
- 2. May require an organic preservative in order to remain untarnished.

The melting point is low enough for most current equipment and components and, with some of the newer laminate properties, is compatible with the printed board fabrication sequence and processing. In order to fine tune the process, solder alloy bath suppliers have added a proprietary stabilizing constituent—HASL, which is identified as Sn-0.7Cu. A typical alloy developed for lead-free soldering is SnCuNi with a melting temperature of 227°C and a processing temperature for soldering of 250°C to 260°C [482°F to 500°F]. Copper dissolution can be a problem if the bath exceeds 0.85% copper which will likely increase the incidence of bridges, icicles, and other defects. The Sn-0.7Cu+Ni is 227–265°C (38°C variation) vs. Sn63Pb37 183–250°C (67°C variation).

The finish has good solderability which is retained through thermal excursions and storage. The finish is smooth and bright and less domed than the tin/lead it is replacing. The solder bath composition can be held stable by the use of a low copper top-up alloy, and dross losses are low. Most important is that the alloy is not aggressive towards solder bath materials.

In situations where large boards (>250 x 250 mm) are used with large BTCs (>25 x 25 mm), it may be a good idea to increase the printed board thickness to at least 2 mm to minimize board bending and flexing. This will reduce or eliminate interfacial failures due to mechanical stress that is caused by bending and flexing of the printed board. However, with the conversion to lead free, thicker boards will require a greater time at temperature exposure making reliability a greater concern. The increase in the use of thin PCBs (<0.5 mm in thickness) in many handheld products may preclude the use of HASL because of warping of the PCBs during processing.

**5.3.2 Organic Surface Protection (Organic Solderability Preservative) Coatings** With wide spread use of bottom termination components (BTC) and more fine pitch devices such as the land grid array, the need for increased control of PCB flatness is more critical. As an alternative to HASL, which can cause warping, an alternative surface finish is organic solderability preservative (OSP). An OSP is an anti-tarnish coating of an organic compound (such as a benzimidazole-based compound) which is applied over exposed copper surfaces to prevent oxidation. An OSP is commonly a water-based organic compound that selectively bonds with copper to provide an organometallic layer that protects the copper, preserving its solderability.

Various chemistries of OSPs are available. Some common ones are benzotriazol, imidazol and benzimidazol. These coatings keep the copper surface solderable by preventing oxidation or tarnish. The coating is commonly applied either by dipping the board in an OSP bath or by spray. As long as the process is controlled to achieve uniform OSP coating,

either method will work. The coating thickness can range from very thin (0.01 µm) to relatively thick 0.2 to 0.5 µm. The thicker coatings are preferred over the thinner coatings, especially if there is need for multiple reflow cycles and/or a long wait (e.g., days) between soldering of each side. It should be noted that all OSPs are not alike since there are specially developed OSPs to withstand the higher reflow profiles associated with lead free.

The OSP surface has many advantages. Most important of all, it avoids the key problem of the tin/lead HASL by keeping the board surface flat. It is also lead-free and will meet with EU legislative requirements. An OSP may also improve gasketing, thereby reducing solder paste printing related defects and thus provides better overall yield.

Because the OSP coating is transparent, the coated terminations maintain their copper appearance, further enabling the detection of any solder paste misprint conditions. Alcohol or other solvents, if used for washing off the misprinted paste, will also wash off coatings, and therefore will increase the risk of oxidation of the copper which impacts solderability. However, such boards can be recoated if necessary. Washing and wiping the board is not recommended, but should instead be processed in accordance with IPC-7526 which recommends stencil and misprinted board application data. Process engineers should work with chemical cleaning suppliers to establish the correct cleaning process that will remove the wet paste and minimize removal of the OSP surface.

There are some potential process incompatibilities with OSPs. For example, if paste or flux does not cover all land surfaces during soldering, there may be some dewetted appearance after reflow soldering. It is thus important for flux to get into the PTH during wave soldering to achieve topside fillet. Similarly, in the SMT process, the paste must cover the entire land surface to avoid dewetted appearance at the land edges. Another example may be potential incompatibility between no-clean fluxes and certain solvents. There is also the potential of solderability concerns when the assembly is subjected to multiple thermal cycles during reflow, wave, and hand soldering.

**5.3.3 Noble Metal Platings/Coatings** With the EU's legislation to remove lead from electronic solder, noble metals, for example gold and palladium, are seeing increased use as PCB surface finishes. Two other noble metal surface finishes have gained popularity, and are electroless nickel/electroless palladium/immersion gold (ENEPIG) and direct immersion gold (DIG). These are also sometimes called universal surface finishes since they can be soldered to, wire bonded to, and are also suitable as contactable surface finishes. ENEPIG, in particular, can alleviate solder

joint brittleness problems occasionally seen with ENIG when used with SAC lead-free BTC termination finishes.

**5.3.3.1 Electroless Nickel/Immersion Gold (ENIG)** Electroless nickel/immersion gold (ENIG) provides very good shelf life, a flat soldering surface for SMT processing, and a good surface for electrical probe contact required for in-circuit-test (ICT). The ENIG finish provides solderable surfaces which can survive through multiple reflow operations and they are less prone to handling related problems. The presence of nickel plating strengthens the through-hole barrels during multiple reflow cycles and rework of through-hole components. Noble metal plating finishes typically cost more than OSP finishes, and are either comparable or more expensive than HASL, depending on the complexity of the PCB. If it is desired to mix multiple board finishes on a single board, for example Ni/Au in some areas and OSP in others, this can be difficult and expensive to achieve in manufacturing.

The reducing agents used in the electroless nickel process contain either phosphorous or boron. In the reduction of the nickel in the electroless nickel deposition, either phosphorous or boron is incorporated into the nickel deposit. The level of these co-deposited elements should be controlled within the specified process limit. Variation of phosphorous or boron level, outside the specified process limits, may have adverse effects on the solderability of the finish and possibly the reliability of the solder joints.

**5.3.3.2 Electrolytic Nickel/Electroplated Gold** Another version of a nickel/gold combination is the electrolytic nickel/electroplated gold surface finish. This plating is similar, however it results in a different grain structure from electroless nickel/immersion gold, and does not exhibit the 'black pad' joint cracking phenomenon.

Electrolytic nickel/electroplated gold is applied after pattern plating and most often before solder mask, and therefore carries some risk of surface contamination. Solder mask applied over electrolytic nickel/electroplated gold exhibits lower solder mask adhesion than other surface finishes. This can create problems during assembly of BTCs, and especially during rework. If the solder mask dams covering the conductors between BTC lands and vias peel off, solder will flow from the lands into the vias and cause insufficient or open solder joints.

Another concern is that it can be difficult to control the gold thickness across the board. The gold may be too thin (for example in areas with dense circuitry) or the gold may be too thick (for example in isolated circuits). This latter situation may lead to gold embrittlement due to excessive gold (>3%) in the solder joints.

**5.3.3.3 Electroless Nickel / Electroless Palladium / Immersion Gold (ENEPIG)** In order to address some of the problems with the electroless nickel/immersion gold

(ENIG) process, another combination of electroless and immersion plating processes have been developed. The switch to lead-free solder has raised many issues on the manufacture, processing, and reliability of lead-free electronic products. Some of the evaluations included a Ni-7%P/Pd/Au (ENEPIG) (5 µm/0.06 µm/0.03 µm) process.

**5.3.3.4 Direct Immersion Gold (DIG)** Direct immersion gold (DIG), is another surface finish that is able to deposit a fine and uniform gold layer directly on the copper surfaces. By examining the deposition reaction of the flash gold plating bath, it can be confirmed that copper does not co-deposit with gold and also that the main driving force for deposition is an auto-catalytic reaction. The copper surface roughness affects solder spread-ability, and the solder joint characteristics are excellent when the film thickness is within the range of 30 to 80 nm. In addition, good wire bonding characteristics can also be derived from deposits plated by a neutral pH, auto-catalytic type heavy electroless gold plating bath, atop the flash gold.

Lead-free solder results are usually inferior (spread less) as compared to tin/lead eutectic solder with a DIG finish. It is necessary to understand this characteristic when lead-free solder is utilized, in that the IMC layer changes at 150°C with time and shows:

- a) A small difference between Sn/Ag/Cu solder and tin/lead solder IMC layer thickness at 0 hours
- b) After 100 hours of exposure the IMC thickness is usually equal
- c) The IMC layer of Cu<sub>3</sub>Sn thickness continues to grow as the heating time increases
- d) As with tin/lead solder, Cu<sub>3</sub>Sn is clearly apparent when Sn/Ag/Cu solder is used

**5.3.3.5 Immersion Silver** Immersion Silver is a metallic solderability preservative. It can be permanent, becoming an integral part of the assembled board, or sacrificial, preventing copper oxidation and preserving solderability through the assembly process. Immersion silver is also a good surface for contact probe testing.

The industry continues to search for alternative surface finishes that can overcome the disadvantages associated with the HASL, OSP, and ENIG finishes. Some of the most promising alternative surface finishes are immersion silver and immersion tin.

**5.3.3.6 Immersion Tin** Immersion tin has a relatively long history but its use has been limited due to earlier concerns about intermetallic formation and reduced solderability. These concerns seem to be getting addressed in more recent processes. Immersion tin is a metallic solderability preservative that is sacrificial, preventing copper oxidation and preserving solderability through the assembly process.

Due to the higher contact resistance of tin it is not as good as immersion silver for contact probe testing. One of the concerns about the amount of tin in the solder joint of lead-free solder is the growth of tin whiskers as the unit experiences changes in various stresses.

Both immersion silver and immersion tin are deposited on the board surface using the immersion method of metal deposition.

**5.3.3.7 Solid Solder Deposition** Solid Solder Deposit (SSD) has been in existence since 1986. It is a method for pre-loading the surface mount lands with all of the solder needed to complete the component attachment, in a solid form. The SSD process uses an adhesive flux coating to hold the components in place during the final reflow cycle. The adhesive flux once dried has a much higher holding power than solder paste and it does not matter if it is smeared as it is non conductive and non corrosive. This means that placing components with lead styles that are blind or underneath the component body can be done with more predictability and achieve better yields.

The basic steps for the SSD application are shown in Figure 5–3.

The manufacturing considerations for an SSD product are:

- Solid Solder Deposit Application Process Sequence (see Figure 5–4)
- Printing paste onto pads and reflowing it without disturbing it is an easier method for applying solder paste. All defects associated with Z-axis pressure from component placement is eliminated.
- Reflowing solder paste on to surface mount lands also highlights solderability issues associated with the surface finish. De-wetting is easily identified without the components in the way.
- Reflowing solder without components allows proper out-gassing of the flux. Consequently the formation of voids is decreased or eliminated.
- Cleaning flux residue from bare boards is easier and more efficient without the components in the way.
- The adhesive flux supplied with SSD is tackier than solder paste and will last up to 6 months if stored properly. The design of a SSD printed circuit board is no different than a standard printed circuit board.

The design considerations for an SSD product are:

- Completely surround every surface mount feature with solder mask. This means dams in between all pads to help shape the SSD during flattening.
- Isolate all holes including via holes so that paste does not drain during reflow.
- Identify lands with via holes in them and the SSD

process can be modified to accommodate a solder filled via hole in a surface mount land.

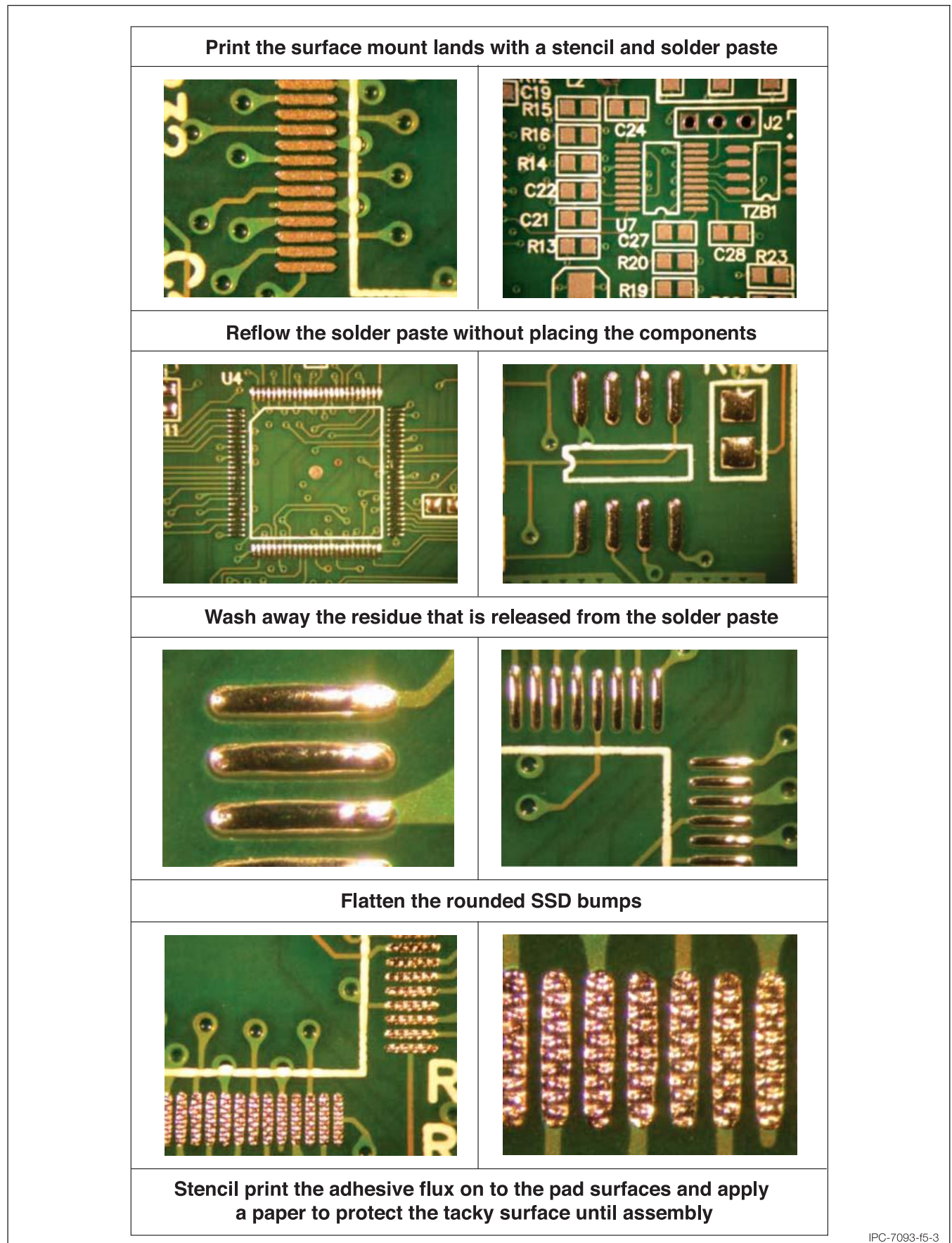
- Step small boards into arrays for handling. Depending on the design, some boards can be separated from the array and fluxed as single images before shipping.

**5.4 Solder Mask** Solder mask is a polymer coating which serves to protect copper surfaces which are not to be soldered. Unlike the laminate, which is a composite, solder mask is commonly a homogeneous material. As the name suggests, solder mask is used to mask off the outer surfaces of the board where solder is not required. Having solder mask over the copper also helps to prevent bridging between conductors. Because of process changes for lead-free soldering, evaluating solder mask performance takes on a whole new meaning.

In the past not all boards required a solder mask because the conductors and lands were spaced quite far apart. The solder bridges between adjacent conductors during wave soldering were not likely. But with the advent of fine lines and spaces, the use of a solder mask has become almost mandatory for boards that are going to be wave soldered. On a full SMT board where no wave soldering is required, tenting or plugging of via holes is done to assist drawing a vacuum on some ICT testers. Also, the application of solder mask to block or plug a via allows closer spacing between a via and the adjacent conductors.

**5.4.1 Wet and Dry Film Solder Masks** Permanent solder masks are available in dry film and wet film. Dry film masks can have an aqueous or a solvent base. In both cases, the mask starts out as a polymer film, which is applied to the board by vacuum lamination. Wet film solder masks, as the name implies, are liquid or paste-like. They include photoimageable and wet screenable solder masks. The latter are differentiated by the method of cure. Some wet screenable solder masks can be cured by UV light and some can be cured thermally in convection or IR ovens. UV masks do not provide as good adhesion as thermal masks but require only seconds to cure as opposed to 30–60 minutes for thermal cure.

Each of the liquid solder masks has advantages and disadvantages. They are inexpensive and highly durable. Being liquid, they flow between conductors and prevent the formation of air pockets. There is no trim waste, and the thickness of the mask can be controlled for each design. Since the wet film solder masks are screened on (a mechanical process), they are difficult to register and have a tendency to skip over conductors, especially on fine line boards. They also tend to bleed onto the lands and surface mount lands during cure. Wet screenable masks are difficult to use on boards with fine lines and spaces (<200 µm), and they are also vulnerable to voids, bubbles and pin holes. The



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Figure 5–3 SSD Application Basic Fabrication Steps

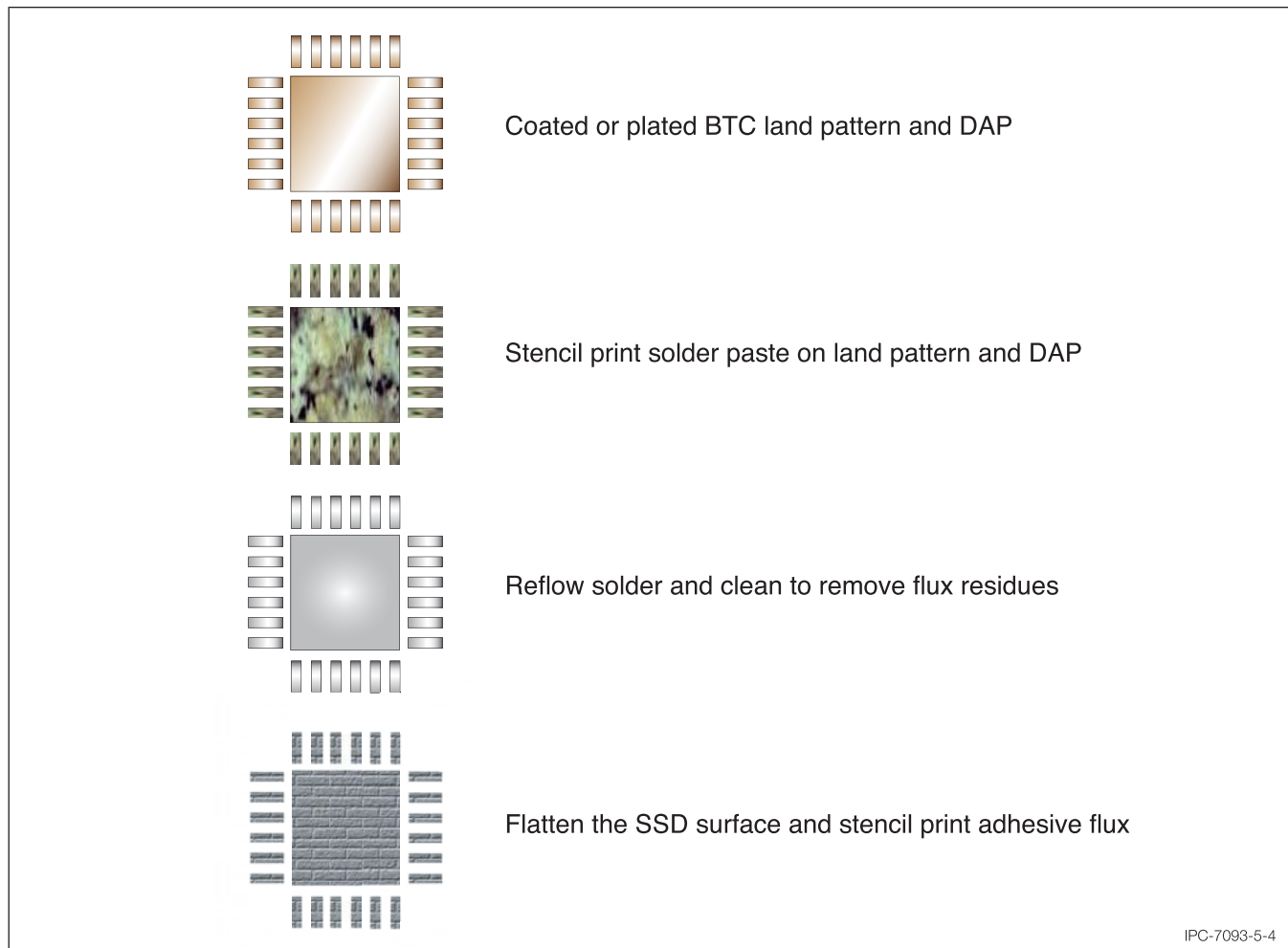


**Figure 5-4 SSD Process Steps**

use of screenable mask has been on decline as photoimageable solder masks have gained in popularity.

The wet film solder mask cannot successfully tent via holes. The degree of fill needs some control in order to develop a plug that prevents chemistry from going through the via. Partially filled vias trap process chemicals and are difficult to clean.

Dry film solder masks have some advantages over their wet screen counterparts. The former provide very accurate registration, which is critical in preventing solder bridging or bleeding on fine line boards, as well as sharper resolution. Tenting of via holes is also superior with dry film solder masks because they are never in a liquid state and do not drip into the via during vacuum lamination. However some problems may arise when trying to laminate a semisolid dry film over an uneven board surface with conductors and lands. Any bow and twisting of the board will compound the problem, possibly causing air pockets underneath the dry film near conductors.

Dry film masks are more costly than the wet film variety, and the supplier base is limited. Moreover, the application process for dry film solder masks is sometimes difficult to

control. Not many film thicknesses are commercially available, and this can limit flexibility and increase cost. Typically, most dry film solder masks are 75  $\mu\text{m}$  to 100  $\mu\text{m}$  thick.

The thicker masks can cause problems in reflow soldering as well. For example, a dry film mask applied between the lands of BTCs can cause standoff problems during reflow soldering because of the rocking effect of the mask. For this reason, dry film solder mask should not be used between the lands of BTCs or in assemblies that have components glued to the bottom side for wave soldering.

**5.4.2 Photoimageable Solder Masks** Photoimageable solder masks combine the advantages of dry film and wet solder masks. Dry film is also a photoimageable mask. Focusing on wet film photoimageable masks provide accurate registration; they are easy to apply, encapsulate the circuit lines totally, have excellent durability, and are less expensive than dry film.

Photoimageable masks can be either screened on or applied by a process called curtain-coating, in which the board is passed at high speed through a curtain or waterfall of solder mask.

The photoimageable mask may contain solvent along with photopolymer liquid. If the solvent is added in the mask, the liquid mask is screened on, solvent is dried off in an oven, and then the mask is exposed to UV light by off-contact or on-contact methods. (If no solvents are used, the liquid is 100% reactive to UV light.) The off-contact method requires a collimated light system to minimize diffraction and scatter in liquid. This makes the system more expensive. The on-contact approach needs no collimated UV light source, and the system is relatively cheaper. Photoimageable solder masks can tent only very small via holes. Most photoimageable wet film masks will not reliably tent 0.35 mm via holes because it is difficult to cure polymer in via holes. If tenting is required, dry film is needed because only dry film can tent via holes effectively.

**5.4.3 Registration** Registration between individual boards within a multi board panel becomes critical for any surface mount application. This is especially true when the board is made in a panel array format to assist the assembly process and throughput characteristics. Board manufacturers inherently build printed boards in a manufacturing panel format; assemblers also want to take advantage of the multiple board array format when they complete their assembly.

The positioning and orientation of individual boards on any panel is usually at the discretion of the board manufacturer. The manufacturer optimizes the use of the material in the panel and the tolerance conditions that can be achieved with the material used to build a particular board. It is a well known fact that organic materials are prone to movement (e.g., growth and/or shrinkage); thus, the board manufacturer, based on their knowledge of materials and their predicted dimensional change movement, will commonly adjust the phototool to compensate for material stretch or shrinkage depending on the circuit, the board size and the particular properties of the selected material.

It is important to understand that assembly companies frequently build their stencils based on a process of “step

and repeat” where elements of an individual board are repeated to match the arrangement of the boards on the subpanel. It is vital that the exact layout used by the board manufacturer is understood to accurately provide the relationships of the land pattern for a BTC on one board with all other land patterns of sister boards in the same panel. Inconsistent arrangement of the assembly array can result in misprints when stenciling solder paste onto the panel for surface mount assembly.

#### 5.4.4 Via Protection

**5.4.4.1 Encroached vias** The encroached via concept is one that permits solder mask being on the land without filling the via plated-through hole. Encroachment vias take the primary solder mask opening and adjust it so that it is slightly larger than the via hole size.

This concept will permit any outgassing or cleaning of the via plated-through hole, provide more surface coverage and increase adhesion between the solder mask and copper of the annular ring. It will also provide a larger web between the land and the via, and thus should minimize solder mask removal during BTC removal for rework. See Figure 5-5.

**5.4.4.2 Via Filling** Via filling, capping, flooding, tenting and plugging (conductive or nonconductive) are some of the process names applied to techniques used to cover or fill via holes with different materials. Materials currently being used to protect vias include standard liquid photoimageable and non-imageable solder masks, dry film solder masks, specially formulated hole plugging inks, conductive inks, liquid dielectric materials and even materials not used in other PCB constructions.

The processes for protection of via structures serve different purposes. Via filling is normally performed on boards that use both reflow soldering and wave soldering. Via filling is also recommended under certain specified conditions, such as for boards where exposed vias under BTCs are exposed to a wave solder. The concern is based on the fact that, when

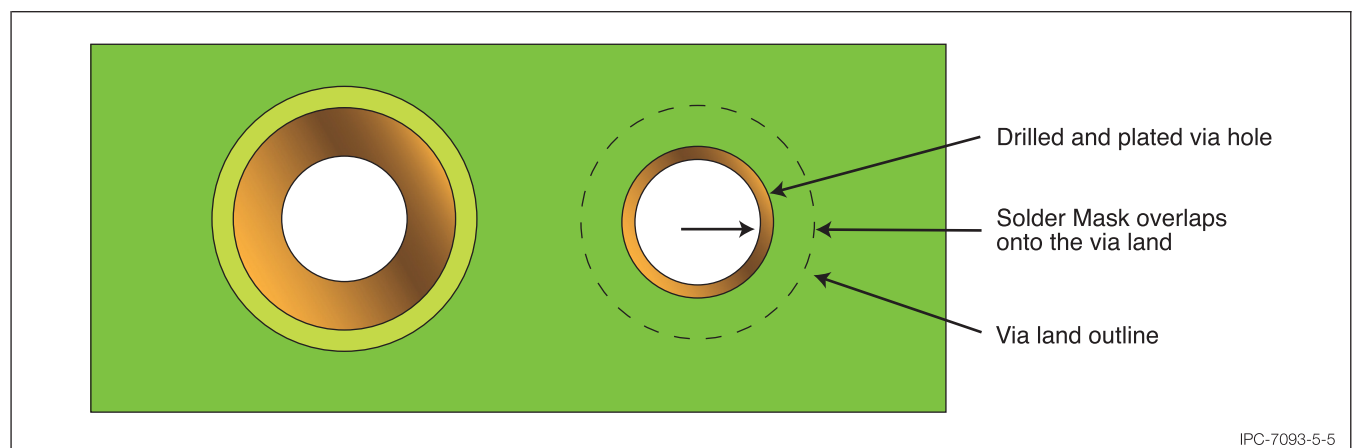


**Figure 5-5 Comparing Solder Mask off Via Land with a Solder Mask Encroached Via Land**

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a board with BTCs on the first side is processed through wave soldering, a large amount of heat can transfer from the vias. This can be very significant because some BTCs can have very high via densities beneath them.

There are three basic characteristics of via protection addressed in IPC-4761. The first is a bumped via, where the hole being plugged or filled with material protrudes above the surface of the hole interface producing a convex shape. The second characteristic is one that has a dimple in the construction where the hole plugging or fill material recedes below the hole interface producing a concave shape. The last of the conditions is identified as a planarized via where the excess hole plugging or fill material protruding above the hole interface has been removed by a process to produce a coplanar surface. See Figure 5–6.

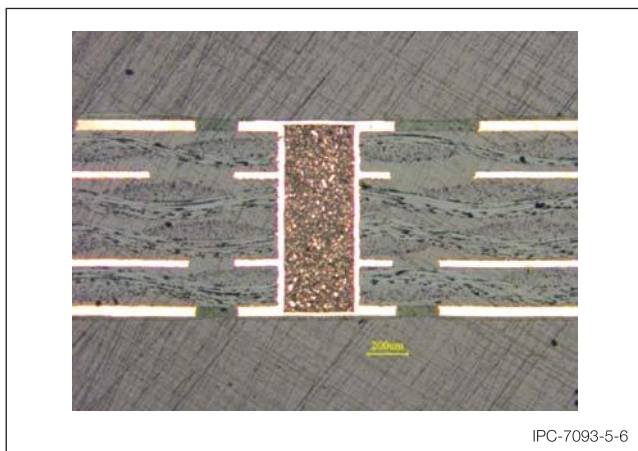


**Figure 5-6 Planarized and Capped Via Protection Example**

The following definitions apply to the various via filling operations. There are four basic concepts which include:

- *Tented Via* – A via covered with dry film solder mask; the via has no fill. When tenting from both sides there may be issues with air entrapment and expansion during mass soldering. When tenting on one side there may be issues with chemical entrapment during the assembly process, especially when using aggressive flux.
- *Flooded Via* – A via that is flooded with LPI solder mask; the via is partially filled or the walls are coated with solder mask. This process could possibly be improved by using a vacuum assist table.
- *Plugged Via* – An additional operation which is done

prior to solder mask application; the via is filled with a conductive or nonconductive material.

- *Filled Via* – A via with material applied into the via targeting a full penetration and encapsulation of the hole.
- *Capped Via* – A secondary operation providing a metallized coating covering the via. The metallization is on both sides.

Via plugging is frequently used in conjunction with BTCs to prevent solder flow to the BTC solder joints when wave soldering is used. Table 5–3 shows the relationship between via filling and the surface finish conditions.

As a general rule, via flooding and capping processing should be performed after a surface finish has been applied. For OSP and ImAg (immersion silver) finishes, via capping must be done after the surface finish is applied because the harsh chemicals that are used to clean the copper surface can become trapped around the via cap. These trapped chemicals can damage the via wall resulting in open vias. Applying the via caps after the surface finish has been applied can degrade some surface finishes (e.g., OSP, ImAg, ImSn) due to the thermal exposure that is necessary to cure the via cap material.

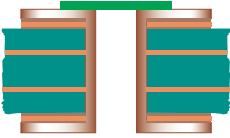
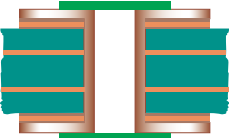
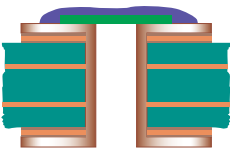
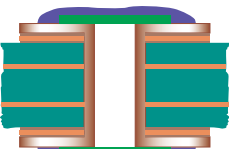
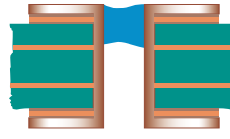
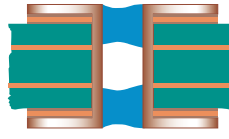
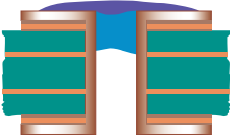
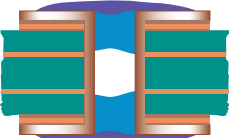
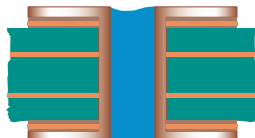
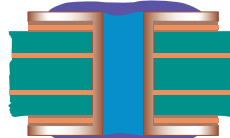
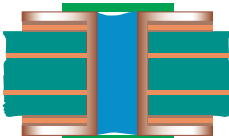
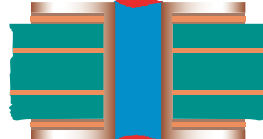
There are presently seven different methods of via plugging/capping identified in IPC-4761. These are shown in Figure 5–7. It is important to realize that the choice of tented, plugged and filled vias for via protection can have direct impacts on the subsequent assembly processes.

Besides identifying the seven via protection methods, there are also pros and cons indicated in IPC-4761. The preference of the plugging method among the options presented will depend on the capabilities of both the fabricators and the assemblers. To avoid complication during assembly, it is imperative that all involved in the manufacturing process understand the trade-offs among the options.

For printed boards with HASL finish, the solder coating will effectively prevent most surface degradation due to chemical exposure. HASL finishes also increase overall wall thickness of the via barrel. It should be noted that for vias that are solder coated before plugging, the solder coating will melt during second side reflow. As a result, the plugging material can become loose. In some cases, when there is excessive solder coating thickness or solder

**Table 5-3 Via filling/encroachment to surface finish process evaluation**

| Surface Finish | Tenting | Flooding        | Capping | Plugging | Encroaching |
|----------------|---------|-----------------|---------|----------|-------------|
| HASL           | Okay    | Okay            | Okay    | Okay     | Okay        |
| OSP            | Okay    | Not Recommended | Okay    | Okay     | Okay        |
| ENIG           | Okay    | Okay            | Okay    | Okay     | Okay        |
| ImAg           | Okay    | Not Recommended | Okay    | Okay     | Okay        |
| ImSn           | Okay    | Not Recommended | Okay    | Okay     | Okay        |

|                                                                                                                        |                                                                                                                        |                                                                                                                                                                                                                                    |
|------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  <p><b>Type I Single Sided</b></p>    |  <p><b>Type I Double Sided</b></p>    | <p><b>Via, Tented</b><br/><b>(Type 1 Via)</b><br/>A via with a mask material (typically dry film) applied bridging over the via wherein no additional materials are in the hole. It may be applied to one side or both.</p>        |
|  <p><b>Type II Single Sided</b></p>   |  <p><b>Type II Double Sided</b></p>   | <p><b>Via, Tented and Covered</b><br/><b>(Type II Via)</b><br/>A Type I via with a secondary covering of mask material applied over the tented via.</p>                                                                            |
|  <p><b>Type III Single Sided</b></p>  |  <p><b>Type III Double Sided</b></p>  | <p><b>Via, Plugged</b><br/><b>(Type III Via)</b><br/>A via with material applied allowing partial penetration into the via. It may be applied from either one side or both sides.</p>                                              |
|  <p><b>Type IV Single Sided</b></p>  |  <p><b>Type IV Double Sided</b></p>  | <p><b>Via, Plugged and Covered</b><br/><b>(Type IV Via)</b><br/>A Type III via with a secondary covering of material applied over the via. The secondary covering may be applied from either one side or both sides.</p>           |
|  <p><b>Type V</b></p>               |                                                                                                                        | <p><b>Via, Filled</b><br/><b>(Type V Via)</b><br/>A via with material applied into the via targeting a full penetration and encapsulation of the hole.</p>                                                                         |
|  <p><b>Type VI Single Sided</b></p> |  <p><b>Type VI Double Sided</b></p> | <p><b>Via, Filled and Covered</b><br/><b>(Type VI Via)</b><br/>A Type V via with a secondary covering of material (liquid or dry film solder mask) applied over the via. It may be applied from either one side or both sides.</p> |
|  <p><b>Type VII</b></p>             |                                                                                                                        | <p><b>Via, Filled and Capped</b><br/><b>(Type VII Via)</b><br/>A Type V via with a secondary metallized coating covering the via. The metallization is on both sides.</p>                                                          |

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Figure 5-7 Via Protection Methods

entrapped within via during fabrication, solder can potentially outgas and spatter or drain to the remaining openings.

**5.5 Thermal Spreader Structure Incorporation (e.g., Metal Core Boards)** When structural, thermal, or electrical requirements dictate, a conductive constraining core or metal core can be added to the organic substrate to make the new structure. It is recommended that the board circuit layer configuration be made symmetrical about the center of the core. It is possible to create structures that are asymmetrical (i.e., having a different number of layers to either side of the core); however, plated-through holes going through the entire stack may be less reliable due to the differences in expansion on either side of the metal or constraining core. See Figure 5–8.

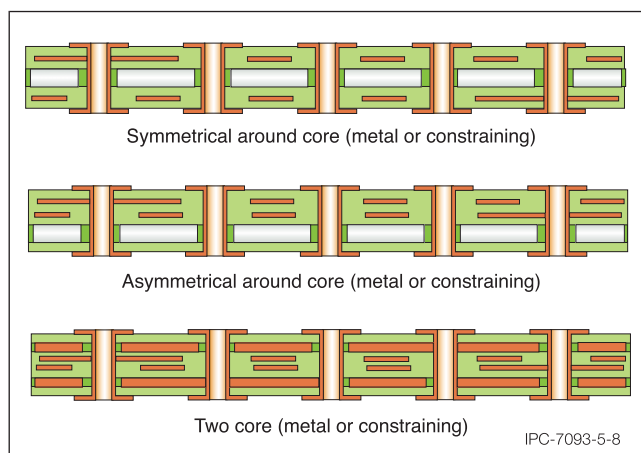


**Figure 5-8 Metal Core Board Construction Examples**

The advantage of the asymmetrical design is that it can separate electrical properties and functions from mechanical features, and/or areas requiring heat dissipation. Among the drawbacks are the significant differences in the coefficient of thermal expansion of the board and the core material. The circuit board may distort during assembly soldering/reflow operations, or while the system is in use if exposed to excessive operating temperature variations.

Some compensation can be achieved by having additional copper planes added to the back of the interconnection product. The extra copper plane may increase the expansion coefficient slightly and make soldering more difficult due to the need to put more energy into the board to assure proper solder joint formation; however, a positive effect is that it enhances thermal conductivity.

**5.5.1 Lamination Sequences** The more desirable constructions are those where circuit layers are symmetrical about the core chosen to serve at the center of the board. By so doing, individual multilayer circuits can be produced separately, each with their own laminating sequence. For example, a four layer board might be manufactured having vias through the entire four layers and this can be duplicated for use on either side of the core.

To achieve mechanical constraint within a chosen and useful range, the total thickness of the core in the multilayer should be approximately 25% of the board's total thickness. Constraining core board is more often used because the core layers may be imaged, etched, and connected to the plated-through hole. The thicker center core must be pre-drilled before lamination to accommodate drilled and plated holes needed to join the two outer sections of the PCB. Better thermal cycle survival has been shown in some studies for structure having two constraining cores in the board rather than one.

Another configuration is to have a special constraining core board made by bonding a multilayer board to each side of a thick metal core after each of the boards has been completed. The composite board is then sequentially drilled, plated, and etched to form plated-through hole connections between the two boards. Coupons should be provided to test the integrity of the composite structure.

**5.5.2 Heat Transfer Pathway** Metal core boards add significantly to the thermal mass of the assembly. This may force the preheating soldering process to be operated at abnormally high limits. These designs should be thoroughly evaluated under production conditions prior to release. Laminate ruptures and discoloration and grainier textured solder are typical effects that have been observed. The heat transfer path between components and the planes are usually accomplished through either direct contact with the plane or through thermal vias positioned under the component and connected to the thermal core or plane in its position.

**5.5.3 Thermal Pad Attachment** In order to obtain peak performance of some BTC high pin count packages the printed board must be properly designed and the package mounted with special consideration. For enhanced thermal, electrical, and board-level performance, the exposed pad on the package should be soldered to the board using a corresponding thermal pad on the printed board. For proper heat conduction through the board, thermal vias should be incorporated in the printed board design in the thermal pad region. Clearance between the inner row's terminations and the thermal pad are required for vias to route the inner row signals. The amount of clearance required depends on the application.

The printed board land pattern design should take into account the dimensional tolerance of package, the printed board, and board assembly. Some of the factors that can significantly affect the mounting of the BTC package on the board and the quality of the solder joints are:

- The amount of solder paste coverage in the thermal pad region
- The stencil design for peripheral and thermal pad region
- The type of via used to interconnect the BTC

- The printed board thickness
- The plated finish on the terminations of the package
- The surface finish on the board
- The type of solder paste
- The reflow profile

Ideally, the size of the thermal pad should match the exposed die paddle size of the BTC. Due to needed clearance for vias, the thermal pad size may need to be reduced to less than the package paddle size. From a board mounting perspective, there are no major issues if the board thermal pad is smaller than the package paddle size, however from a thermal efficiency perspective, there is minimal efficiency loss as long as the thermal pad on the board is close to the same size as the die inside the package.

The thermal pad design on the printed board should have 75% paste coverage and may use a hatch pattern to reduce the amount of total solder paste. The number of openings should be chosen in order to maintain a web thickness between openings of approximately 0.20 mm. This will allow space for flux volatiles to escape, thus minimizing voids.

**5.5.4 Thermal Vias** In order to effectively transfer heat from the top metal layer of the PCB to the inner or bottom layers, thermal vias should be incorporated into the thermal pad design. The number of thermal vias will depend on the application, power dissipation, and electrical requirements. Although more thermal vias improve the package's thermal performance, there is a point of diminishing returns where additional thermal vias may not significantly improve the performance. Usually BTC suppliers recommend incorporating an array of thermal vias at 1.0 mm to 1.2 mm pitch with via diameters of 0.3 mm to 0.4 mm. The number of thermal vias should be determined for each application operating environment and condition.

Thermal vias may take several configurations. They could be left open, they could be filled with thermally conductive materials, they could be plated shut or capped with plating as in the description of a type VII via fill defined shown in Figure 5–9. Any thermal via should be connected to a plane within the multilayer board in order to transfer the heat to a cooler material surface. The concept for BTC removal or replacement needs to address the soldered connection of the thermal pad and the amount of mass that must be heated in order to disconnect the BTC from the mounting surface.

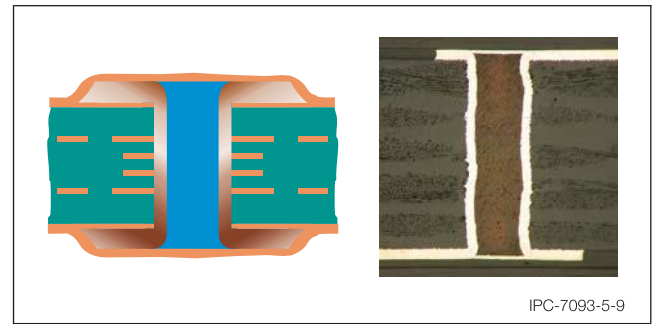


**Figure 5-9 Examples of Type VII Filled and Capped Vias**

**5.6 Solderless Interconnections Systems** Due to the regulations eliminating the use of some materials in the fabrication of the electronic assembly interconnecting structures, several alternative and unique assembly methods designed to eliminate solder completely from the assembly process are generating interest. One approach for discussion is a process identified as Solderless Interconnection process, e.g., plating process. In this process, tested and burned-in packaged components are encapsulated and the electrical connections are made to component leads using an electroplating process during the circuit patterning, thus bypassing the soldering process.

The BTC packages are devices which conform to a common fundamental grid pitch in order to facilitate design and testing. The other components that are part of the electronic assembly should also be available in a bottom only termination mode. The prospective of benefits of such processing include: lower material use, reduced energy requirements, fewer manufacturing steps, simpler designs with fewer wiring layers, higher performance, improved thermal management, better EMI and ESD protection, obviation of concerns about metal finish solderability, solder joint quality or tin whiskers.

The burned-in or tested components are bonded to a temporary or permanent organic base material, after which the components and base material are over molded with an insulating material. The assembly is inverted and the component leads or terminations are accessed by ablation of the organic base material. Vias are then plated along the circuit layers as shown in Figure 5–10.

Structures fabricated without having to be exposed to high temperatures can open doors to new potentials in terms of interconnection and thermal management. The structures themselves could be assembled in a modular form into 3D

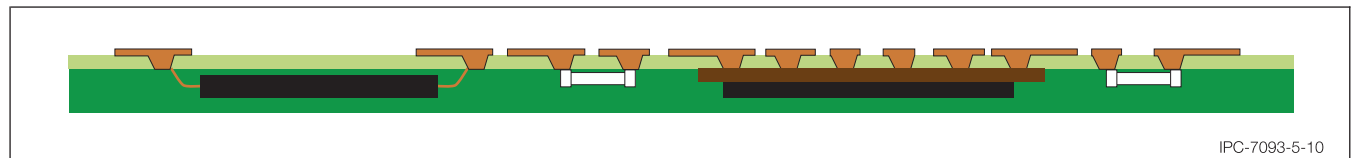


**Figure 5–10 Example of Circuit Development of Solderless Connection Technology**

structures that are interconnected on all sides. There are several of these concepts being developed which make the interconnecting substrate part of the assembly process and thus the lines of responsibility for testing become somewhat blurred. Only time will tell as to which application provides the most benefit to the user and the status of the infrastructure that can provide this form of interconnection methodology.

## 6 PRINTED CIRCUIT ASSEMBLY DESIGN CONSIDERATIONS

This section provides information on the design principles for incorporating bottom termination components (BTC) into electronic products including modules and product board design concepts. The principles define placement and interconnection rules and the mounting characteristics that must be considered during the design process. Methods of mounting structure requirements are detailed to the extent that they coincide with the assembly process considerations. Emphasis is also placed on the thermal management of the final assembly and the contribution that the mounting structure provides to the assembly.

**6.1 BTC Part Description** BTC parts are a near chip scale plastic encapsulated wire bond package with a copper leadframe or organic laminate substrate in a BTC package format. The QFN and LGA are representative of the package technology. The QFN variation offers a number of significant benefits over standard plastic lead-frame packages:

- Reduction in board mounting space as die size is closer to the package size.
- Superior electrical characteristics are obtained due to minimal lead lengths, reducing the electrical path distance between die and PCB.
- Lower thermal resistance because the bottom exposed die attach paddle can be soldered directly to a corresponding thermal feature on the PCB surface.
- The QFN leadframe type package assembly process utilizes existing proven SO-IC leadframe package infrastructure.
- Standard SMT assembly equipment can be used and high assembly yields can be realized from the self-aligning characteristic of the low mass package.

Coplanarity is not an area of concern for this component family because all contacts are flush with the bottom of the package. In regard to moisture sensitivity level (MSL), the molding compounds used for encapsulation are a resin-based material, so moisture absorption will vary depending on the size of the specific package, the size of the die attach pad (DAP) and the number of wire-bonds.

**6.1.1 BTC Package Variations** The BTC packages are available in various lead formats and thicknesses. In general

terms, the family of BTC components includes: peripherally leaded dual (two) and quad (four) sided devices, peripheral multi-row (in-line and staggered leads) and full and partial area array devices. The leads on the bottoms of the packages can be rectangular or round depending on the type with lead-frame devices (e.g., QFN) typically represented by the former and substrate devices (e.g., LGA) represented by the latter. (see Figure 6–1) Because BTC packages do not have solder balls terminations, the electrical connection between the package and the assembly board must be made using only the solder deposited on to the circuit board. Getting sufficient solder on the lands and making viable and reliable solder joints is one of the significant challenges for this type or product. Thus, special attention is needed in designing the land pattern.

The component land pattern for the PCB is commonly predicated either on guidelines developed by the component manufacturer, within a company or by following established industry standards such as IPC-7351. While BTCs such as the SON and QFN have been available for some time, they have not been broadly used and thus the learning experience with them is still limited and industry guidelines may not have been refined. The development of an optimum geometry may require some experimental trials. Moreover, because certain structures of the exposed die attach paddle and the package lands on the bottom side of the package, certain constraints must be considered.

The SON and QFN versions are of high interest to industry. The 0.8 mm is perhaps the most prevalent thickness but the package is selectively available in a lower profile thickness as well such as 0.6 mm. Perimeter input/output pads are located on the outside edges of the package. Electrical contact to the printed circuit board (PCB) is made by soldering the perimeter pads and exposed paddle on the bottom surface of the package to the PCB. Heat is efficiently conducted from the package by soldering the exposed thermal paddle to the PCB as illustrated in Figure 6–2.

Stable electrical ground connections are provided through down bonds and through conductive die attach material. Wire bonding is provided using gold wires. Perimeter and thermal pad finish is plated as 100% Sn (Sn/Pb is available as well). As noted in Sections 3 and 4 SON and QFN packages are punched or sawed from a molded strip during final assembly. Half-etching of the leadframe provides mold compound locking features for the perimeter pads and die thermal paddle. This package is currently characterized as moisture sensitivity (MSL) level 3 (see J-STD-020 for MSL levels).

Terminal contacts:

- The contact pads (or solder pad) are located peripherally in single row format depending on the specific number of pins and body size.

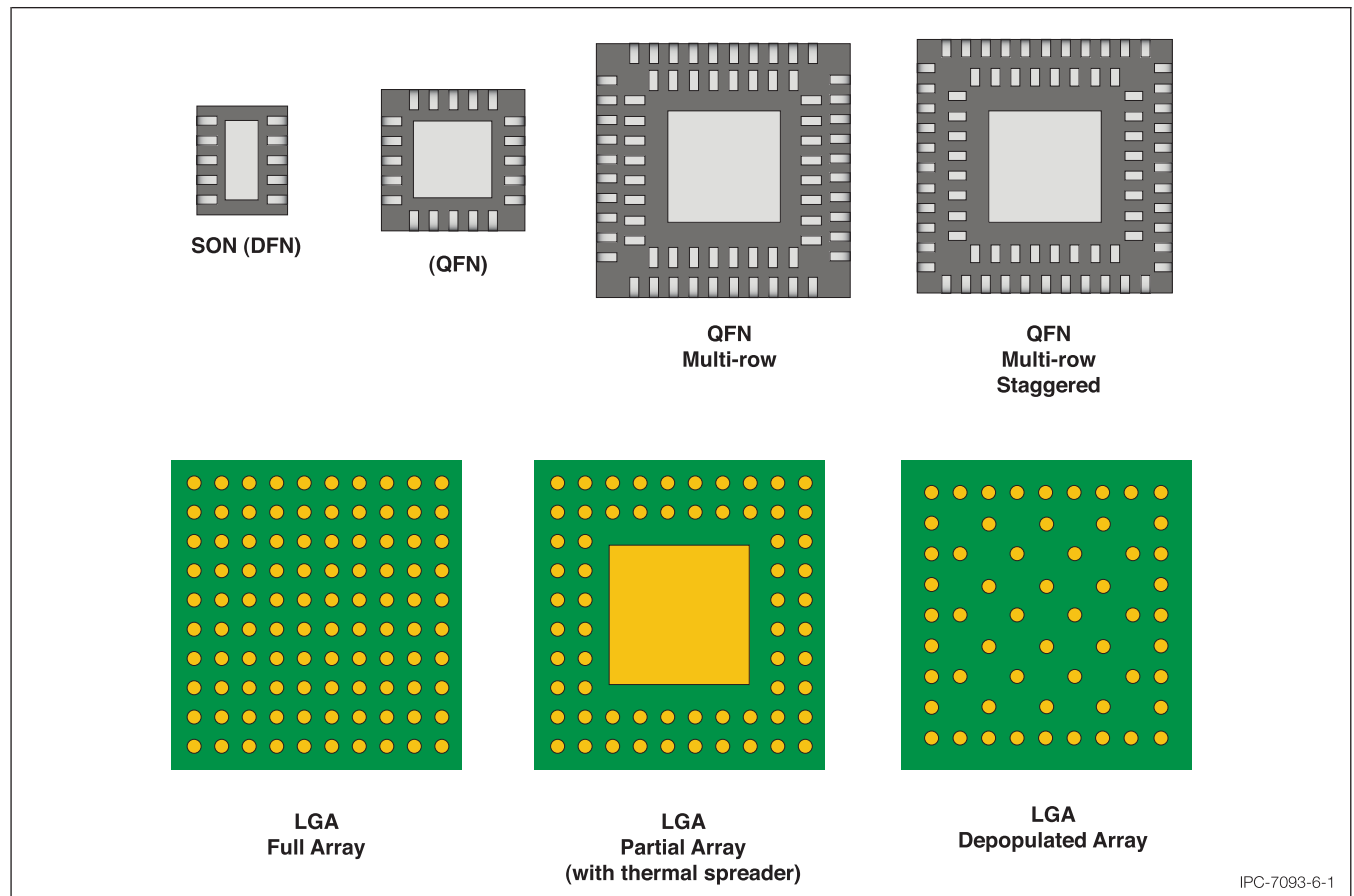


Figure 6-1 Family of Bottom Termination Components (BTC)

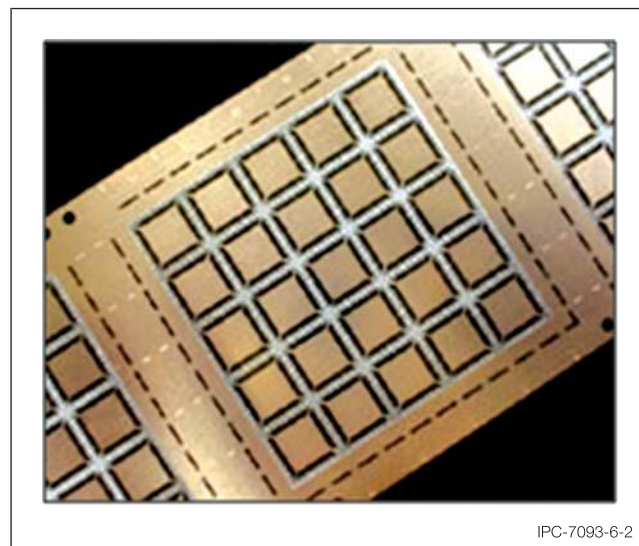


Figure 6-2 QFN Bottom Termination Component Lead-Frame Array

- For certain specific applications the packages are incorporated with common power and/or ground pins.
- All contacts are plated with matte tin solder for ease of surface mount processing.

The bottom termination QFN package family (see JEDEC MO-220) furnishes enhanced chip speed, reduced thermal

impedance, and, because of its small outline, minimizes the printed circuit board area required for mounting. The small size and very low profile make this package ideal for high density PCBs used in small-scale electronic applications such as cellular phones, pagers, and handheld PDAs.

In addition to their small package outline and low profile, the BTC devices have a low thermal resistance and reduced electrical parasitic.

**6.1.1.1 Board Material** As detailed in Section 5 standard epoxy glass substrates (FR-4) are compatible with BTC assembly. Use of a substrate with lower coefficient of thermal expansion (CTE) can improve reliability. A printed board can also be affected by factors such as number of metal layers, laminate material selected, balanced construction, trace density, operating environment, site population density, and mounting of components on the reverse side of the printed board. For specific board material specifications refer to IPC-4101.

**6.1.1.2 Surface Finish** The surface finish on the printed board is also very important to proper design of the assembly. There are a variety of finishes available (see Section 5), and many times a compromise is required in order to meet the conditions of all the components that are

part of the assembly. The methodology for the analysis includes the finish on the component package and the compatibility with the alloy that has been chosen to solder all of the parts into place.

**6.1.2 Termination Formats** The SON and QFN device packages are available in both Pullback and No-Pullback contact configurations and soldering the exposed die attach pad (DAP) to the PCB optimizes thermal performance. (See Section 4.)

In the Pullback configuration the standard solder pads are offset from the edge of the package by 0.1 mm. In the No-Pullback configuration the standard solder pads extend and terminate at the edge of the package as compared in Figure 6–3.

The advantage of the No-Pullback design is that the end-exposed contact feature offers a more visible solder fillet after board mounting.

**6.1.3 Mounting Conditions** In order for components to perform at peak level, special considerations must be addressed to properly design the circuit board and to mount the package. For example, for enhanced thermal, electrical, and board level performance, the exposed die attach pad (DAP) on the package needs to be soldered to the board using a corresponding thermal pad on the board. Recent data indicate that this may be important for board reliability as well. In addition, to assure proper heat conduction through the board for higher power devices, thermal vias may be needed in the PCB in the thermal pad region. The PCB assembly design should account for the dimensional and manufacturing tolerances of all elements of the design including the package, PCB, and assembly.

There are a number of factors which may impact mounting BTC packages on the board and the quality of solder joints. These factors include: amount of solder paste coverage in thermal pad region, stencil design for peripheral and thermal pad region, type of vias, board thickness, lead finish on the package, surface finish on the board, type of solder paste, and reflow profile. It should be emphasized that these

guidelines are offered to help the user in developing the proper printed board design and surface mount practices and requirements but that characterization of the processes used for assembly.

**6.1.3.1 PCB Design Guidelines** The PCB land pattern dimensions required for a design are shown in Figure 6–4. In the figure, the dimensions ZD max and GD min (and ZE max and GE min) are the outside to outside and inside to inside land dimensions, respectively. The dimension X and Y indicate the width and the length of the land, respectively. Two additional clearances  $C_{LL}$  and  $C_{PL}$  are also defined to avoid solder bridging.

While  $C_{LL}$  defines the minimum distance between land to land for the corner joints on adjacent sides,  $C_{PL}$  defines the minimum distance between the inner tip of the peripheral lands and the outer edge of the thermal pad. In developing the land pattern for the SON with contact only on two sides, the designer can apply the same basic rules. See Figure 6–5.

In order to design a proper land pattern, tolerance analysis is required on package and printed board dimensions. The 6 I/O package outline example illustrated in Figure 6–5 is typical of the configuration selected for power amplifiers, signal translators and load switching functions.

With contacts only on two sides of the package, the land pattern and DAP layout is less complex than the quad contact variations. The example shown in Figure 6–6 is the land pattern of the 6 I/O devices illustrated in the Figure 6–5.

For component tolerances, the profile tolerances usually given in the package outline drawing are converted into Maximum Material Condition (MMC) and Least Material Condition (LMC) based tolerances. The minimum and maximum values can thus be obtained for various QFN type packages. In order to determine the land pattern dimensions, three sets of tolerances are involved; one set for the overall component tolerances, and the other two sets for the leads on each end. Since it is unrealistic to assume that all three tolerances will be at their worse case, a more realistic RMS (root-mean-square) system is used here as described in IPC-7351. See Figure 6–7.

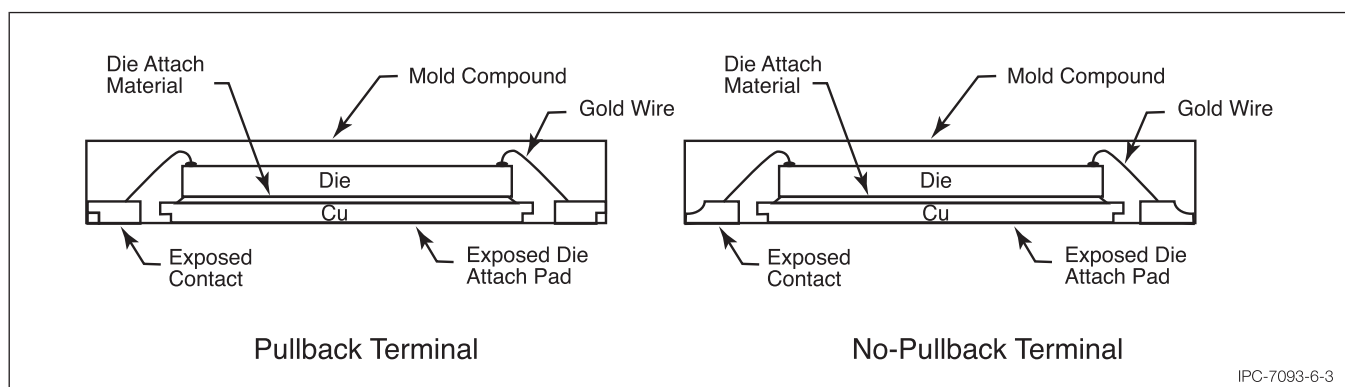


**Figure 6-3 Comparing Pullback and No-Pullback Configurations**

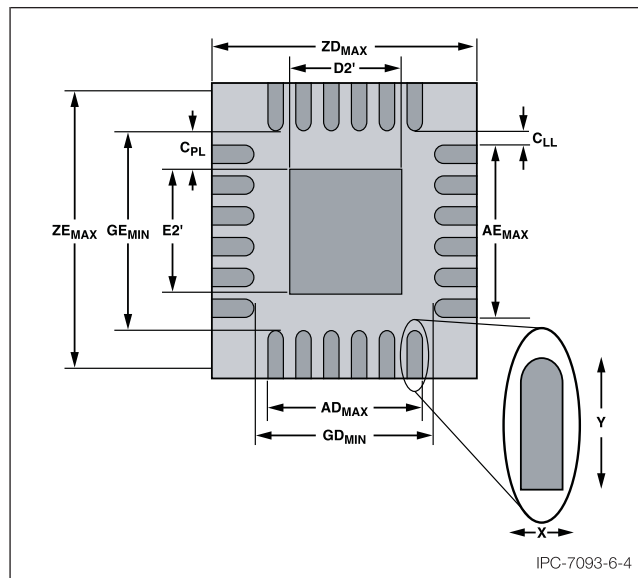


Figure 6-4 Land Pattern and DAP Land Layout Guide

The dimension between internal component pads, shown in Figure 6-7 is not normally shown in package outline drawings. Since this dimension is required to determine the land pattern length, it is calculated as follows:

$$\text{Space between pads } [S]_{\min} = A_{\min} - 2T_{1\max}$$

$$\text{Space between pads } [S]_{\max} = A_{\min} + [S]_{\text{tol}} (\text{rms})$$

Where,

$$[S]_{\text{tol}} (\text{rms}) = \sqrt{(A_{\max} - A_{\min})^2 + 2(T_{1\max} - T_{1\min})^2}$$

The board tolerance defines the difference between the MMC and LMC of each land pattern dimension and is assumed as 0.05 mm in this example. The placement tolerance is also assumed as 0.05 mm Diameter of True Position (DTP), given that most placement machines have placement accuracy between 20 and 70 microns. The minimum values for solder joint fillets, defined in Figure 6-8, used to calculate the land pattern dimensions are:

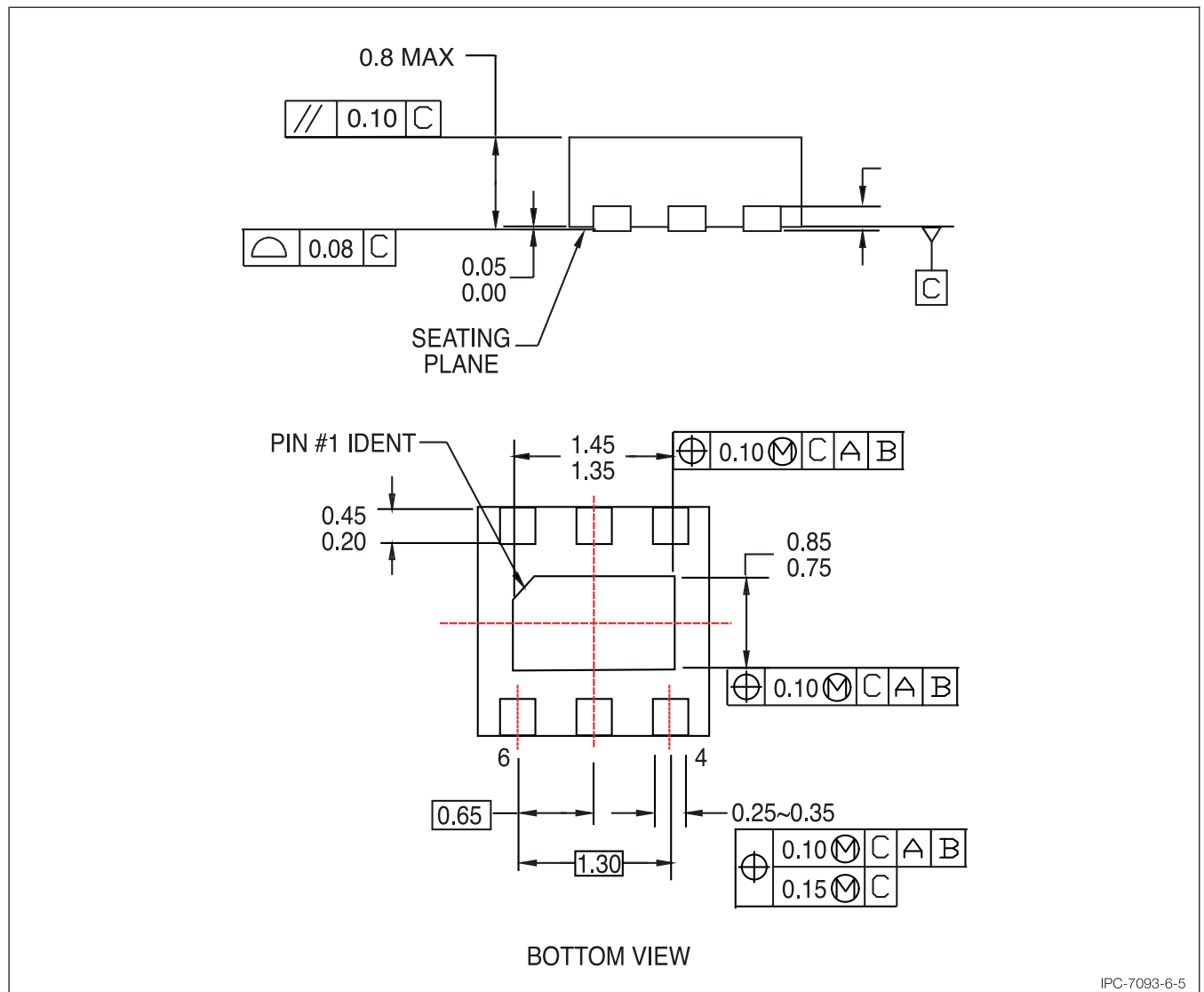


Figure 6-5 Basic Outline Drawing for the 6 I/O SON

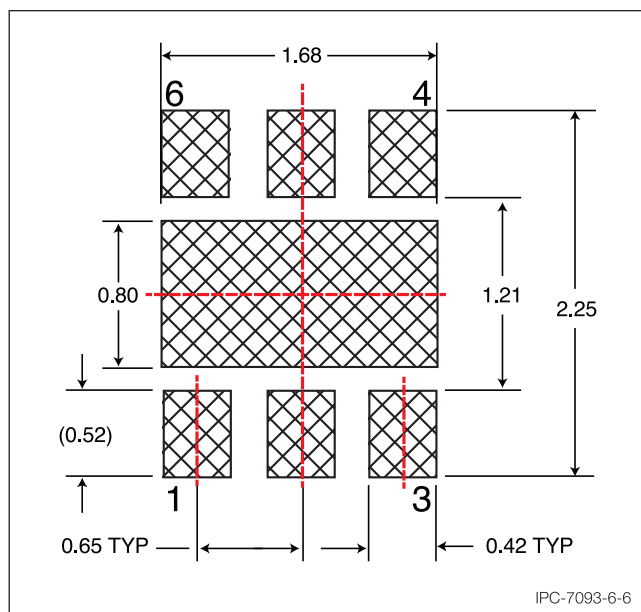


**Figure 6-6 Recommended Land Pattern for JEDEC 6 I/O SON Package**

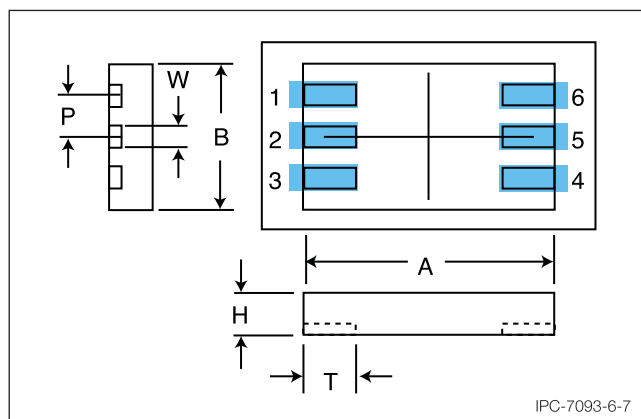


**Figure 6-7 QFN Component and Land Pattern Composite**

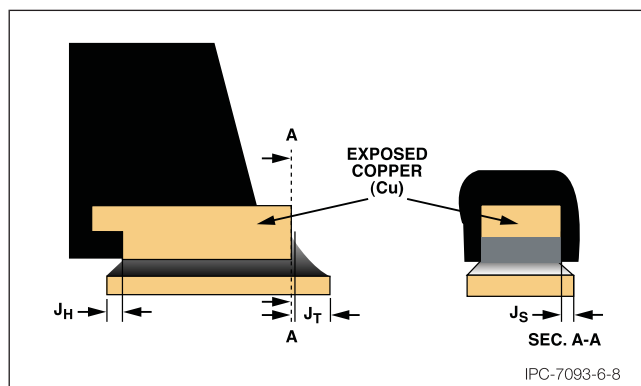


**Figure 6-8 Definition of Toe, Heel and Side Fillets**

Minimum Toe Fillet =  $J_T \min = 0.1 \text{ mm}$

Minimum Heel Fillet =  $J_H \min = 0.05 \text{ mm}$

Minimum Side Fillet =  $J_S \min = 0.0 \text{ mm}$

The values are selected recognizing that both sides and one end of the leads are embedded in the mold compound and

solder fillets cannot be formed on these sides. The fourth side, however, has either all or half of the thickness of the lead exposed on the side of the package, depending on the full lead or lead pull back options. Since the pad pattern dimension is most likely to be larger than the nominal lead dimension, solder joints may assume some angular shape or fillets as shown in Figure 6–8 for full lead option.

It should be noted that the formation of toe fillets is not guaranteed unless specific measures are taken (usually by the BTC supplier) to ensure solder wetting to the sides of the leads during typical reflow assembly. It is generally observed, however, that the toe fillets are formed depending on the type of solder paste used and length of exposure of package to environment. The toe fillet, if formed, will improve the solder joint reliability and allocation must be made for its formation. Although the toe fillet is not expected to form for the lead pullback option, the same land pattern as the one for full lead option can be used for this design. Table 6–1 shows the target conditions for three variations of land patterns.

**6.1.3.2 Land Pattern Design Calculations** With the assumptions and tolerances previously described, the land pattern dimensions are determined by using the following relations:

$$Z_{\max} = A_{\min} + 2J_T + T_T$$

$$X_{\max} = W_{\min} + 2J_S + T_S$$

$$G_{\min} = S_{\max} - 2J_H - T_H$$

Where:

$T_T$ ,  $T_H$ , and  $T_S$  are the RMS values of toe, heel and side tolerance accounting for component, board, and placement tolerances.

The calculations for these values are defined in more detail in IPC-7351 document. The above calculation for  $G_{\min}$  does not account for the leads on all four sides of the package. In order to include this and to avoid any solder bridging between the two perpendicular leads on each corner, a minimum clearance,  $C_{LL}$ , is needed. This clearance is assumed as 0.1 mm and the final value of  $G_{\min}$  is determined by using the following constraint:

$$G_{\min} \geq A_{\max} + 2 C_{LL}$$

Where:

$A_{\max} = (\text{Lead Pitch}) \times (\# \text{ of leads on one side} - 1) + \text{Pad Width}$

Finally, the pad length is determined as:

$$Y = (Z_{\max} - G_{\min})/2$$

Using the above methodology, the perimeter land pattern dimensions for various QFN packages with full-lead option are listed in Table 6–2. It should be noted that the calculated  $X_{\max}$  dimension (pad width) from the above equations is

**Table 6-1 Quad Flat No Lead Tolerance Goals for Solder Joint Formation**

| Lead Part        | Minimum (Least)<br>Density Level C                                       | Median (Nominal)<br>Density Level B | Maximum (Most)<br>Density Level A |
|------------------|--------------------------------------------------------------------------|-------------------------------------|-----------------------------------|
| Toe ( $J_T$ )    | 0.20                                                                     | 0.30                                | 0.40                              |
| Heel ( $J_H$ )   | 0.00                                                                     | 0.00                                | 0.00                              |
| Side ( $J_S$ )   | -0.04                                                                    | -0.04                               | -0.04                             |
| Round-off factor | Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15 |                                     |                                   |
| Courtyard excess | 0.1                                                                      | 0.25                                | 0.5                               |

**Note:** The rationale for the relatively large negative heel stems from the tolerances for the lead lengths as also being relatively large. To maintain a minimum clearance of 0.20 mm to the thermal tab it becomes necessary to trim the heel by -0.2 mm. Without a thermal tab the heel can usually be increased to as much as 0.50 mm.

reduced for 0.4 and 0.5 mm pitch devices to avoid any solder bridging issues. The pads may also be rounded on the inner edge. Also, because of rectangular dimension of the package in most cases, the suffix D and E from dimension notations in Figure 6-4 (e.g., ZD and ZE) are dropped in the table and it is implied that  $Z_{\max} = ZD_{\max} = ZE_{\max}$ .

The  $X_{\max}$  dimension reduced for the 0.4 and 0.5 mm pitch devices to avoid solder bridging. Refer to 'Exposed Pad Variations' in the Package Outline Drawing for specific D2 and E2 dimensions. D2' should be equal to Component D2 or D2'TH max above, whichever is minimum. Analysis of the land pattern geometry requires the consideration of a) component tolerances, b) the PCB tolerances, and c) the accuracy of the equipment used for placing the component. In addition, minimum values of toe, heel, and side fillets must be considered for the formation of reliable solder joints.

**6.1.3.3 PCB Land Pattern Development** The PCB land pattern for the QFN may be furnished by the component manufacturer, guidelines developed by the board assembler, or by following an industry standard such as IPC-7351. Because of exposed thermal paddle and the package perimeter pads on the bottom side of the package, constraints should be added to the IPC methodology.

The tolerance analysis requires the consideration of:

- Component tolerances
- PCB tolerances
- Accuracy of the equipment used for placing the component

The PCB land pattern for the BTC defined in Figure 6-9.

The thermal land is a metal (normally copper) region centrally located under the package and on top of the PCB. It has a rectangular or square shape and should match the dimensions of the exposed DAP on the bottom of the package (1:1 ratio). The legend for the mechanical dimensions referenced in Figure 6-9 is furnished in Table 6-3.

**6.1.3.4 Land Pattern Design Adjustment** To ensure a robust design and to minimize any possibility of solder bridging during board assembly, a minimum metal-to-metal clearance of 0.2 mm is required. Therefore, a final adjustment to the land pattern is made by overlaying the package outline with the maximum metal dimensions and adjusting the land pattern to maintain 0.2 mm minimum metal-to-metal clearance. Land pattern dimensions are determined initially using the following:

$$Z_{\max} = A_{\min} + 2J_T + T_T$$

**Note:**  $A_{\min}$  is the package external outline minimum value. See Figure 6-10.

**6.1.3.5 Thermal Pad Design** As noted, BTC devices are designed with an exposed thermal pad to conduct heat away from the package and into the PCB. By incorporating thermal vias into the PCB thermal pad, heat is dissipated more effectively into the inner metal layers of the PCB. Depending upon the package pad size, the PCB thermal pad size is modified to avoid solder bridging between the thermal pad and the perimeter pads. This is done by defining a minimum clearance between the outer edges of the thermal pad and the inner edges of the perimeter pads. This minimum clearance is fixed at 0.2 mm.

The number of thermal vias incorporated into the design will depend on the power dissipation and electrical requirements of the specific application. There is a point of diminishing returns where additional thermal vias may not significantly improve the performance of the package. This is shown in Figure 6-11 where the effect of number of vias is plotted for 7 mm x 7 mm, 48-lead packages.

A via diameter of 0.3 mm is used for this simulation. As the via pitch decreases, more vias can be incorporated for the same thermal pad size; however, the incremental performance improvement reduces. Thermal vias are necessary because they conduct heat from the exposed pad of the package to the ground plane. The number of vias is application specific and is dependent upon electrical requirements and power dissipation. The thermal performance

Table 6-2 Package and Land Pattern (Pullback and No-Pullback) Dimensions

| Package |             |                |               |            |            | Package Dimensions with Tolerance |            |            |            |            |            | Board Land Pattern Dimensions |      |      |       |       |              |
|---------|-------------|----------------|---------------|------------|------------|-----------------------------------|------------|------------|------------|------------|------------|-------------------------------|------|------|-------|-------|--------------|
| Size    | I/O         | Leads/<br>Side | Lead<br>Pitch | D<br>(min) | D<br>(max) | E<br>(min)                        | E<br>(max) | b<br>(min) | b<br>(max) | L<br>(min) | L<br>(max) | Xmax                          | Yref | Amax | Gmin  | Zmax  | D2'th<br>max |
| 6x5     | 8<br>(dual) | 4              | 1.27          | 5.90       | 6.10       | 4.90                              | 5.10       | 0.35       | 0.47       | 0.5        | 0.7        | 0.50                          | 0.96 | NA   | 4.39  | 6.31  | 4.09         |
| 3x3     | 12          | 3              | 0.8           | 2.90       | 3.10       | 2.90                              | 3.10       | 0.28       | 0.40       | 0.5        | 0.7        | 0.42                          | 0.57 | 2.02 | 2.17  | 3.31  | 1.87         |
| 4x4     | 12          | 3              | 0.8           | 3.90       | 4.10       | 3.90                              | 4.10       | 0.28       | 0.40       | 0.5        | 0.7        | 0.42                          | 0.96 | 2.02 | 2.39  | 4.31  | 2.09         |
| 5x5     | 16          | 4              | 0.8           | 4.90       | 5.10       | 4.90                              | 5.10       | 0.28       | 0.40       | 0.5        | 0.7        | 0.42                          | 0.96 | 2.82 | 3.39  | 5.31  | 3.09         |
| 6x6     | 20          | 5              | 0.8           | 5.90       | 6.10       | 5.90                              | 6.10       | 0.28       | 0.40       | 0.5        | 0.7        | 0.42                          | 0.96 | 3.62 | 4.39  | 6.31  | 4.09         |
| 7x7     | 28          | 7              | 0.8           | 6.90       | 7.10       | 6.90                              | 7.10       | 0.28       | 0.40       | 0.5        | 0.7        | 0.42                          | 0.96 | 5.22 | 5.39  | 7.31  | 5.09         |
| 8x8     | 32          | 8              | 0.8           | 7.90       | 8.10       | 7.90                              | 8.10       | 0.28       | 0.40       | 0.5        | 0.7        | 0.42                          | 0.96 | 6.02 | 6.39  | 8.31  | 6.09         |
| 9x9     | 36          | 9              | 0.8           | 8.90       | 9.10       | 8.90                              | 9.10       | 0.28       | 0.40       | 0.5        | 0.7        | 0.42                          | 0.96 | 6.82 | 7.39  | 9.31  | 7.09         |
| 10x10   | 44          | 11             | 0.8           | 9.90       | 10.10      | 9.90                              | 10.10      | 0.28       | 0.40       | 0.5        | 0.7        | 0.42                          | 0.87 | 8.42 | 8.57  | 10.31 | 8.27         |
| 2x3     | 8<br>(dual) | 4              | 0.65          | 1.90       | 2.10       | 2.90                              | 3.10       | 0.23       | 0.35       | 0.3        | 0.5        | 0.37                          | 0.76 | NA   | 0.79  | 2.31  | 0.49         |
| 3x3     | 8<br>(dual) | 4              | 0.65          | 2.90       | 3.10       | 2.90                              | 3.10       | 0.23       | 0.35       | 0.5        | 0.7        | 0.37                          | 0.96 | NA   | 1.39  | 3.31  | 1.09         |
| 4x4     | 16          | 4              | 0.65          | 3.90       | 4.10       | 3.90                              | 4.10       | 0.23       | 0.35       | 0.5        | 0.7        | 0.37                          | 0.92 | 2.32 | 2.47  | 4.31  | 2.17         |
| 5x5     | 20          | 5              | 0.65          | 4.90       | 5.10       | 4.90                              | 5.10       | 0.23       | 0.35       | 0.5        | 0.7        | 0.37                          | 0.96 | 2.97 | 3.39  | 5.31  | 3.09         |
| 6x6     | 28          | 7              | 0.65          | 5.90       | 6.10       | 5.90                              | 6.10       | 0.23       | 0.35       | 0.5        | 0.7        | 0.37                          | 0.95 | 4.27 | 4.42  | 6.31  | 4/12         |
| 7x7     | 32          | 8              | 0.65          | 6.90       | 7.10       | 6.90                              | 7.10       | 0.23       | 0.35       | 0.5        | 0.7        | 0.37                          | 0.96 | 4.92 | 5.39  | 7.31  | 5.09         |
| 8x8     | 40          | 10             | 0.65          | 7.90       | 8.10       | 7.90                              | 8.10       | 0.23       | 0.35       | 0.5        | 0.7        | 0.37                          | 0.96 | 6.22 | 6.39  | 8.31  | 6.09         |
| 9x9     | 44          | 11             | 0.65          | 8.90       | 9.10       | 8.90                              | 9.10       | 0.23       | 0.35       | 0.5        | 0.7        | 0.37                          | 0.96 | 6.87 | 7.39  | 9.31  | 7.09         |
| 10x10   | 52          | 13             | 0.65          | 9.90       | 10.10      | 9.90                              | 10.10      | 0.23       | 0.35       | 0.5        | 0.7        | 0.37                          | 0.96 | 8.17 | 8.39  | 10.31 | 8.09         |
| 3x3     | 8           | 2              | 0.50          | 2.90       | 3.10       | 2.90                              | 3.10       | 0.18       | 0.30       | 0.5        | 0.7        | 0.28                          | 0.96 | 0.78 | 1.39  | 3.31  | 1.09         |
| 3x3     | 12          | 3              | 0.50          | 2.90       | 3.10       | 2.90                              | 3.10       | 0.18       | 0.30       | 0.5        | 0.7        | 0.28                          | 0.94 | 1.28 | 1.43  | 3.31  | 1.13         |
| 3x3     | 16          | 4              | 0.50          | 2.90       | 3.10       | 2.90                              | 3.10       | 0.18       | 0.30       | 0.3        | 0.5        | 0.28                          | 0.69 | 1.78 | 1.93  | 3.31  | 1.63         |
| 4x4     | 20          | 5              | 0.50          | 3.90       | 4.10       | 3.90                              | 4.10       | 0.18       | 0.30       | 0.5        | 0.7        | 0.28                          | 0.94 | 2.28 | 2.43  | 4.31  | 2.13         |
| 4x4     | 24          | 6              | 0.50          | 3.90       | 4.10       | 3.90                              | 4.10       | 0.18       | 0.30       | 0.3        | 0.5        | 0.28                          | 0.69 | 2.78 | 2.93  | 4.31  | 2.63         |
| 5x5     | 28          | 7              | 0.50          | 4.90       | 5.10       | 4.90                              | 5.10       | 0.18       | 0.30       | 0.5        | 0.7        | 0.28                          | 0.94 | 3.28 | 3.43  | 5.31  | 3.13         |
| 5x5     | 32          | 8              | 0.50          | 4.90       | 5.10       | 4.90                              | 5.10       | 0.18       | 0.30       | 0.3        | 0.5        | 0.28                          | 0.69 | 3.78 | 3.93  | 5.31  | 3.63         |
| 6x6     | 36          | 9              | 0.50          | 5.90       | 6.10       | 5.90                              | 6.10       | 0.18       | 0.30       | 0.5        | 0.7        | 0.28                          | 0.94 | 4.28 | 4.43  | 6.31  | 4.13         |
| 6x6     | 40          | 10             | 0.50          | 5.90       | 6.10       | 5.90                              | 6.10       | 0.18       | 0.30       | 0.3        | 0.5        | 0.28                          | 0.69 | 4.78 | 4.93  | 6.31  | 4.63         |
| 7x7     | 44          | 11             | 0.50          | 6.90       | 7.10       | 6.90                              | 7.10       | 0.18       | 0.30       | 0.5        | 0.7        | 0.28                          | 0.94 | 5.28 | 5.43  | 7.31  | 5.13         |
| 7x7     | 48          | 12             | 0.50          | 6.90       | 7.10       | 6.90                              | 7.10       | 0.18       | 0.30       | 0.3        | 0.5        | 0.28                          | 0.69 | 5.78 | 5.93  | 7.31  | 5.63         |
| 8x8     | 52          | 13             | 0.50          | 7.90       | 8.10       | 7.90                              | 8.10       | 0.18       | 0.30       | 0.5        | 0.7        | 0.28                          | 0.94 | 6.28 | 6.43  | 8.31  | 6.13         |
| 8x8     | 56          | 14             | 0.50          | 7.90       | 8.10       | 7.90                              | 8.10       | 0.18       | 0.30       | 0.3        | 0.5        | 0.28                          | 0.69 | 6.78 | 6.93  | 8.31  | 6.63         |
| 9x9     | 60          | 15             | 0.50          | 8.90       | 9.10       | 8.90                              | 9.10       | 0.18       | 0.30       | 0.5        | 0.7        | 0.28                          | 0.94 | 7.28 | 7.43  | 9.31  | 7.13         |
| 9x9     | 64          | 16             | 0.50          | 8.90       | 9.10       | 8.90                              | 9.10       | 0.18       | 0.30       | 0.3        | 0.5        | 0.28                          | 0.69 | 7.78 | 7.93  | 9.31  | 7.63         |
| 10x10   | 68          | 17             | 0.50          | 9.90       | 10.10      | 9.90                              | 10.10      | 0.18       | 0.30       | 0.5        | 0.7        | 0.28                          | 0.94 | 8.28 | 8.43  | 10.31 | 8.13         |
| 10x10   | 72          | 18             | 0.50          | 9.90       | 10.10      | 9.90                              | 10.10      | 0.18       | 0.30       | 0.3        | 0.5        | 0.28                          | 0.69 | 8.78 | 8.93  | 10.31 | 8.63         |
| 8x8     | 68          | 17             | 0.4           | 7.90       | 8.10       | 7.90                              | 8.10       | 0.15       | 0.25       | 0.3        | 0.5        | 0.25                          | 0.76 | 6.65 | 6.80  | 8.31  | 6.50         |
| 10x10   | 84          | 21             | 0.4           | 9.90       | 10.10      | 9.90                              | 10.10      | 0.15       | 0.25       | 0.3        | 0.5        | 0.25                          | 0.76 | 8.25 | 8.79  | 10.31 | 8.49         |
| 12x12   | 100         | 25             | 0.4           | 11.90      | 12.10      | 11.90                             | 12.10      | 0.15       | 0.25       | 0.5        | 0.7        | 0.25                          | 0.96 | 9.85 | 10.39 | 12.31 | 10.09        |

of a package may be improved by increasing the number of vias. Figure 6–12 shows the effect for a 36 I/O BTC with a 9 x 9 mm body and 7 x 7 mm pad.

The via diameter should be 0.2 mm to 0.33 mm with 1 oz. copper via barrel plating. It is important to plug the via to avoid any solder wicking inside the via during the soldering process. The thermal vias can be tented with solder mask on the top surface of the PCB. The solder mask diameter

should be at least 75  $\mu$  larger than the via hole diameter. The solder mask thickness should be the same across the entire PCB.

Two via diameters illustrated are 0.2 mm and 0.33 mm. Different patterns are also shown to depict possible layouts for specific numbers of vias. Two die sizes are shown in this example, 2.1 mm x 2.1 mm and 6.4 mm x 6.4 mm. For a given number of vias, placing the vias toward the periphery

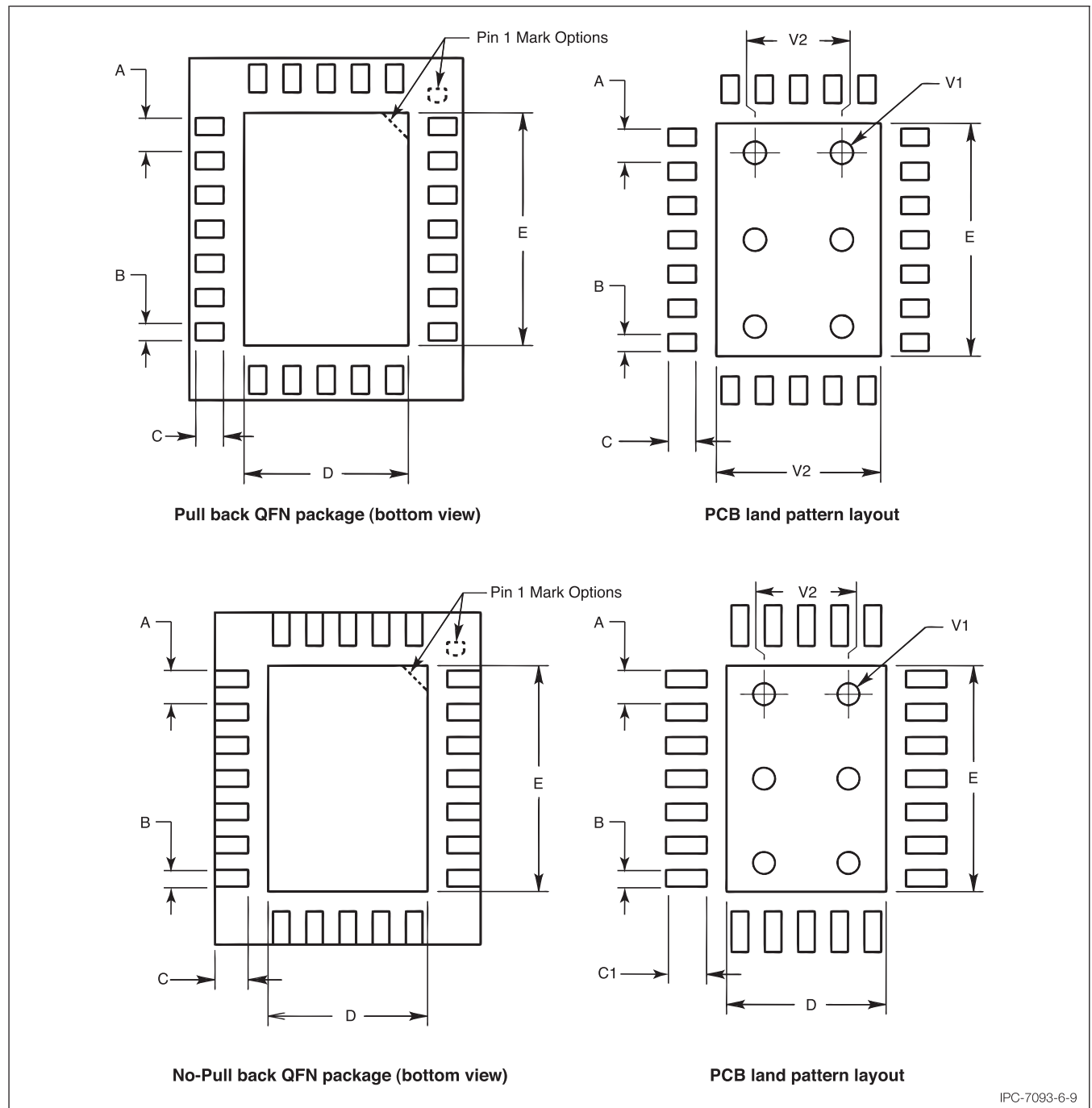


**Figure 6-9 Comparing Pull Back to no-Pull Back Package Outline and Land Pattern Thermal Land Layout**

of the pad provides up to 5% improvement over centrally placed vias. There is diminishing improvement, however, as the number of vias increases.

**6.1.3.6 Solder Mask Design** Two types of land patterns are used for surface mount packages: 'Non-Solder Mask Defined' lands (NSMD) and 'Solder Mask Defined' lands (SMD). NSMD has an opening that is slightly larger than the land geometry, while the SMD land surface is defined by a solder mask opening that is smaller than the metal land geometry. Figure 6-13 illustrates the two different types of solder mask to land pattern geometry.

Because the copper etching process has tighter control than the solder masking process, NSMD is preferred over SMD. The solder mask opening on NSMD pads is larger than the copper land to allow the solder to adhere to the sides of the copper land, improving reliability of the solder joints.

The recommended solder mask opening should be 120  $\mu\text{m}$  to 150  $\mu\text{m}$  larger than the copper land size to allow for solder mask registration tolerances, typically between 50  $\mu\text{m}$  to 65  $\mu\text{m}$ . The solder mask web must be a minimum of 75  $\mu\text{m}$  in width to adhere to the PCB surface. This constraint allows each land to be individually masked for

Table 6-3 Legend for Basic Mechanical Attributes

| Dimensions A, B, C, D, and E of PCB are 1:1 ratio with package pad dimensions. For specific detailed package dimensions, refer to respective marketing outlines. |    |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| Terminal Pitch                                                                                                                                                   | A  |
| Terminal Width                                                                                                                                                   | B  |
| Terminal Length                                                                                                                                                  | C  |
| Exposed DAP Width                                                                                                                                                | D  |
| Exposed DAP Length                                                                                                                                               | E  |
| Thermal Via Diameter. Recommended 0.2 – 0.33 mm                                                                                                                  | V1 |
| Thermal Via Pitch. Recommended 1.27 mm                                                                                                                           | V2 |

Source: National Semiconductor

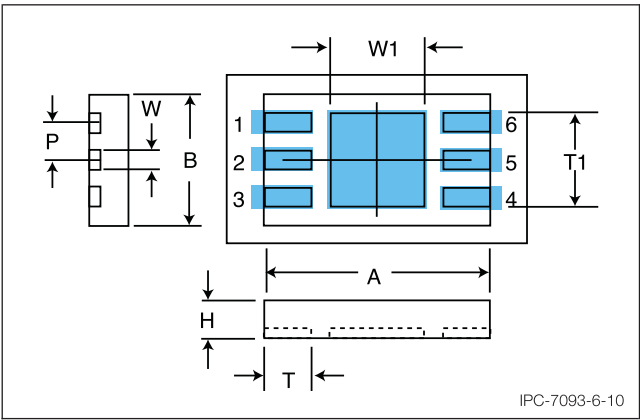


Figure 6-10 SON 0.5 mm Pitch, 6 Pin with Thermal Tab

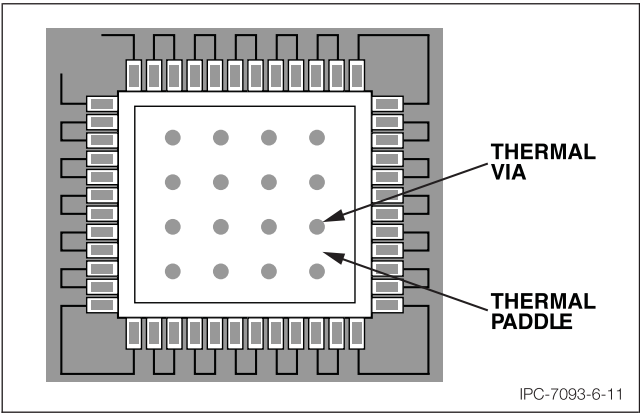


Figure 6-11 DAP to PCB Interface Example

lead pitches of 0.5 mm and higher. However, for 0.4 mm pitch parts with PCB land width of 0.25 mm, not enough space is available for solder mask web in between the lands. It is recommended to use a trench type solder mask opening where a big opening is designed around all lands on each side of the package with no solder mask in between the lands, as shown in Figure 6-14.

It is better to round the inner edge of the solder mask, especially for corner leads, to allow for enough solder mask web in the corner area. For the cases where thermal land

dimension is close to the theoretical maximum, it is recommended that the thermal pad area should be solder mask defined in order to avoid any solder bridging between the thermal pad and the perimeter pads. The mask opening should be 100 microns smaller than the thermal pad size on all four sides. This will guarantee 25  $\mu$ m solder mask overlap even for the worse case mis-registration.

**6.1.4 Package Tolerances** The JEDEC design guideline standard for QFN package family detailed in Section 4 applies to packages with optional thermal enhancements as well as various height profiles and pitches. This package has terminals on all four edges of the bottom surface of the package. A BTC may have either square or rectangular body outline as well as either symmetric or asymmetric terminal patterns. Versions of the package may also have terminals placed in the corners at 45° to neighboring leads. The basic dimensions for the package outline are in increments of 0.50 mm ranging from 1.00 mm through 12.00 mm. See Figure 6-15.

The outline detail shown in Figure 6-15 illustrates the primary package outline dimensions used when developing the land pattern and thermal pad geometries. The width of the metallized terminals (including lead finish) exposed at the bottom surface of the package are detailed in Table 6-4.

The component tolerances and profile tolerances usually given in the package outline drawings are converted into maximum material condition (MMC) and least material condition (LMC) based tolerances.

**6.1.4.1 Circuit Routing, Thermal Pad and Via Design**

For best performance, all circuit traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the BTC device to minimize parasitic trace inductance. Using wide conductors for V-IN, V-OUT and GND will help minimize parasitic electrical effects along with enhancing the thermal transfer between the case and the ambient environment.

Additional good practices are:

- Dedicate an internal power plane to spread the heat and optimize thermal dissipation.
- Make the heat sink plane within the circuit board as large as possible to minimize board and die temperature.
- Use conductive copper plated vias to make the electrical and thermal tie to the heat sink plane.

As stated, the SON and QFN package is designed to provide a superior thermal performance. This is partly achieved by incorporating an exposed die paddle on the bottom surface of the package. However, in order to take full advantage of this feature, the PCB must have features to effectively conduct heat away from the package. This can be achieved by incorporating thermal pad and thermal vias on the PCB.

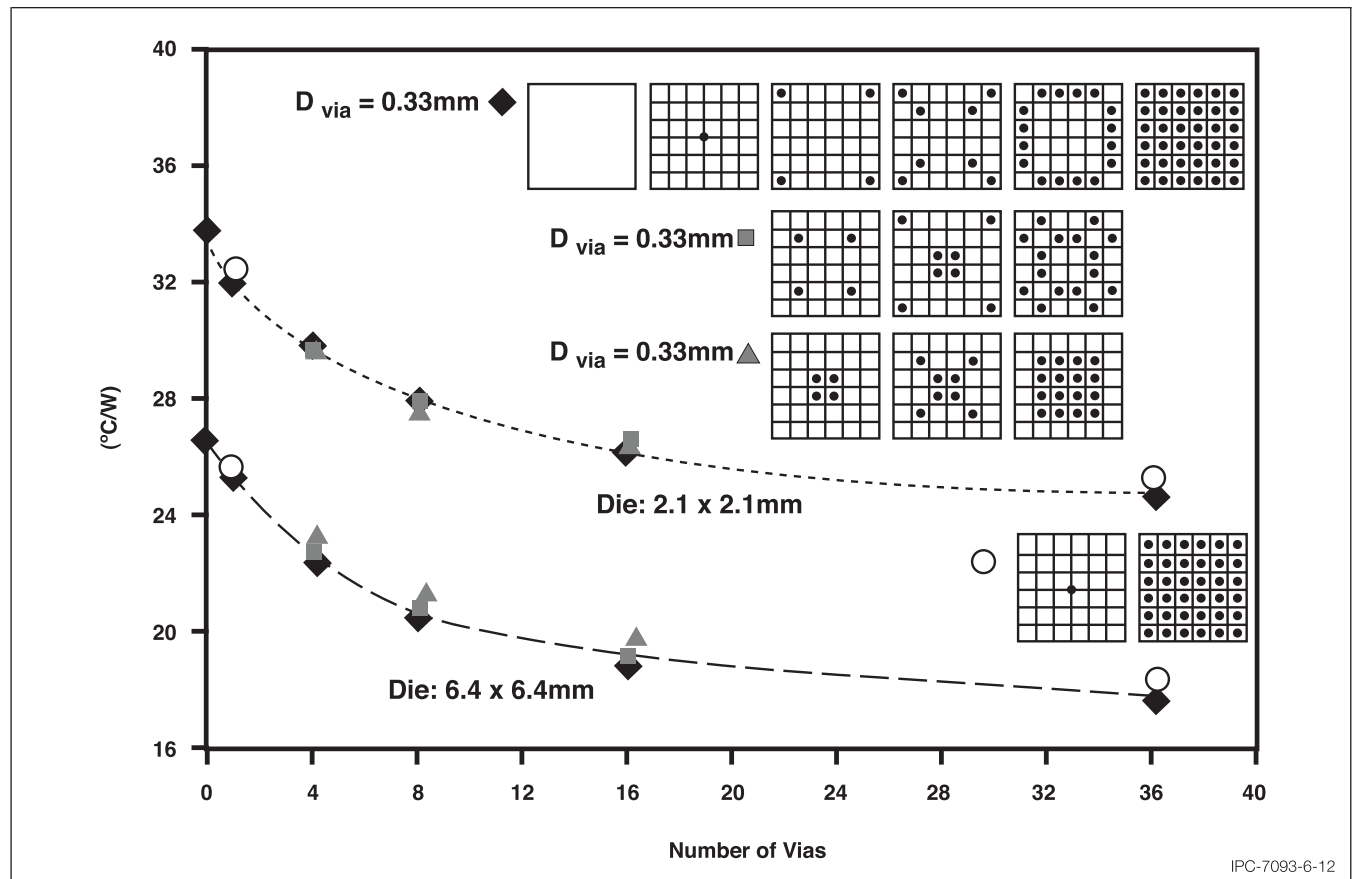


Figure 6-12 The Affect of  $\theta_{JA}$  vs. Number, Distribution and Diameter of Thermal Vias and Die Sizes for a 36 I/O QFN with a 9 x 9 mm Body and 7x7 mm Thermal Land

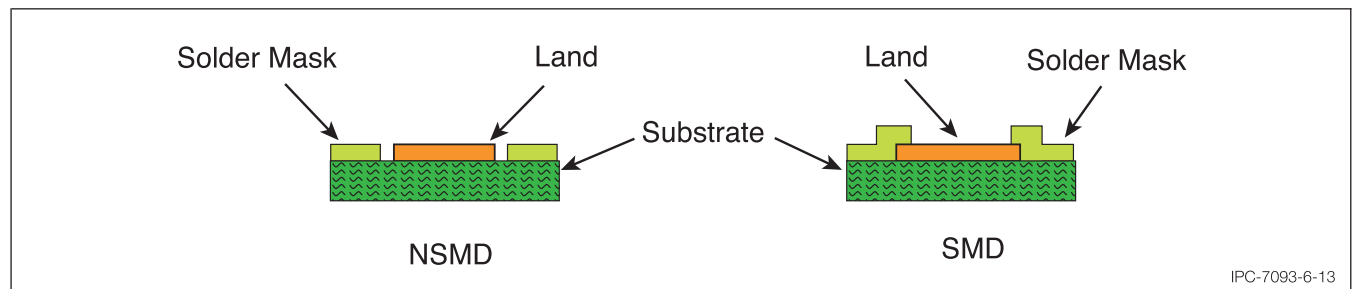


Figure 6-13 Comparing Optional Solder Mask Variations

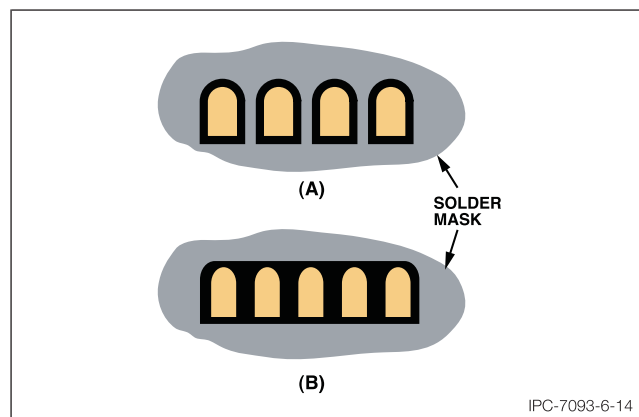


Figure 6-14 Solder Mask for (A) Perimeter Lands for 0.5 mm and Higher Pitch Parts, and (B) for 0.4 mm Pitch Parts

While a thermal pad provides a solderable surface on the top surface of the PCB (to solder the package die pad on the board), thermal vias are needed to achieve a suitable thermal path to inner and/or bottom layers of the PCB to remove the heat.

Generally, the size of the thermal pad on the PCB should match the exposed die paddle feature provided on the device. However, depending upon the die paddle size, this size needs to be modified in some cases to avoid solder bridging between thermal pad and the perimeter pads. This is done by defining a clearance between the outer edges of the thermal pad and the inner edges of perimeter pads. It should be noted that the D2'TH dimension gives the theoretical maximum value. Since the size of the exposed die paddle on the component may actually be much smaller

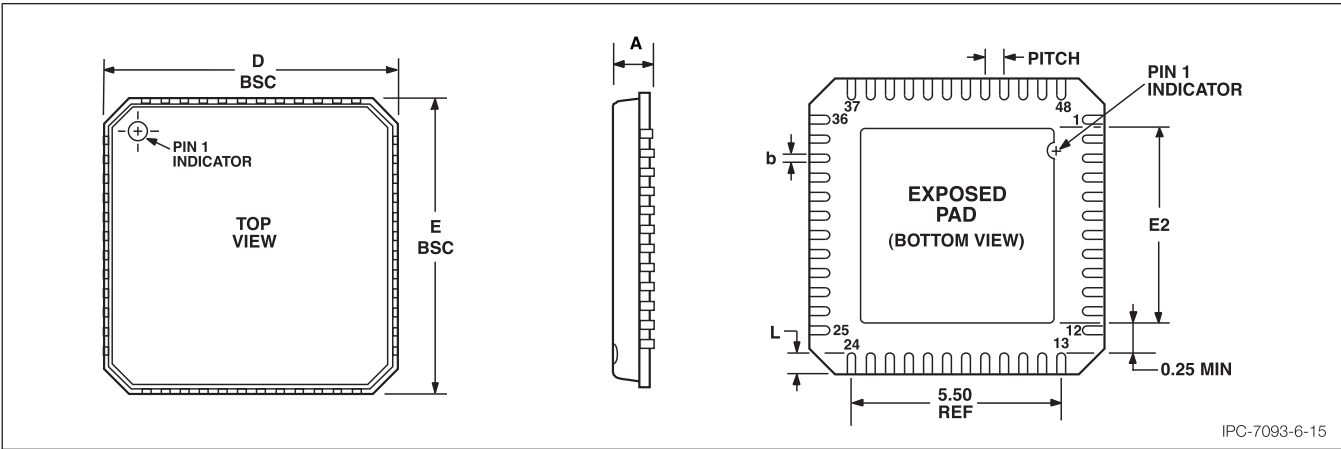


Figure 6-15 Representative BTC Outline Detail

Table 6-4 Contact Pitch and Width Variations

| Contact Pitch | Terminal Dimension |         |         |
|---------------|--------------------|---------|---------|
|               | Minimal            | Nominal | Maximum |
| 0.65          | 0.25               | 0.30    | 0.35    |
| 0.50          | 0.18               | 0.25    | 0.30    |
| 0.40          | 0.15               | 0.20    | 0.25    |

than this value, the actual D2' dimension should be modified by Component  $D2 \leq D2' \leq D2'_{TH \max}$  Note: QFN with down-bond ring design does not require the ring to be soldered to the board. The thermal pad design on the board should be based on the exposed paddle area, excluding the ring area.

In order to effectively transfer heat from the top metal layer of the PCB to the inner or bottom layers, thermal vias need to be incorporated into the thermal pad design. The number of thermal vias will depend on the application and power dissipation and electrical requirements. Although more thermal vias improve the package thermal performance, there is a point of diminishing returns as additional thermal vias may not significantly improve the performance. This is

shown in Figure 6-16 where the effect of number of vias plotted for 7 mm x 7 mm, 48 contact package. A via diameter of 0.3 mm was used for this simulation. As the via pitch decreases more vias can be incorporated for the same thermal pad size but the incremental performance improvement diminishes.

With this constraint, the maximum size of the thermal pad is calculated by the following relationship and is listed under the graph in figure 6-16 for various package sizes. Based on this and similar thermal simulations, it is recommended that an array of thermal vias should be incorporated at 1.0 mm to 1.2 mm pitch with via diameter of 0.3 mm to 0.33 mm. Representative of these arrays are shown in Figure 6-17 for 7x7 mm, 48 lead and 10x10 mm, 68 lead packages.

**6.1.4.2 Standard Grids** Standard grids offer the potential for significant improvement in routing and BTC components are key. The industry is presently compelled to deal with legacy component lead pitches because of the long established precedent. The now registered and accepted range of options include: 0.100" (2.54 mm) which was the original single de facto standard for IC components. It has

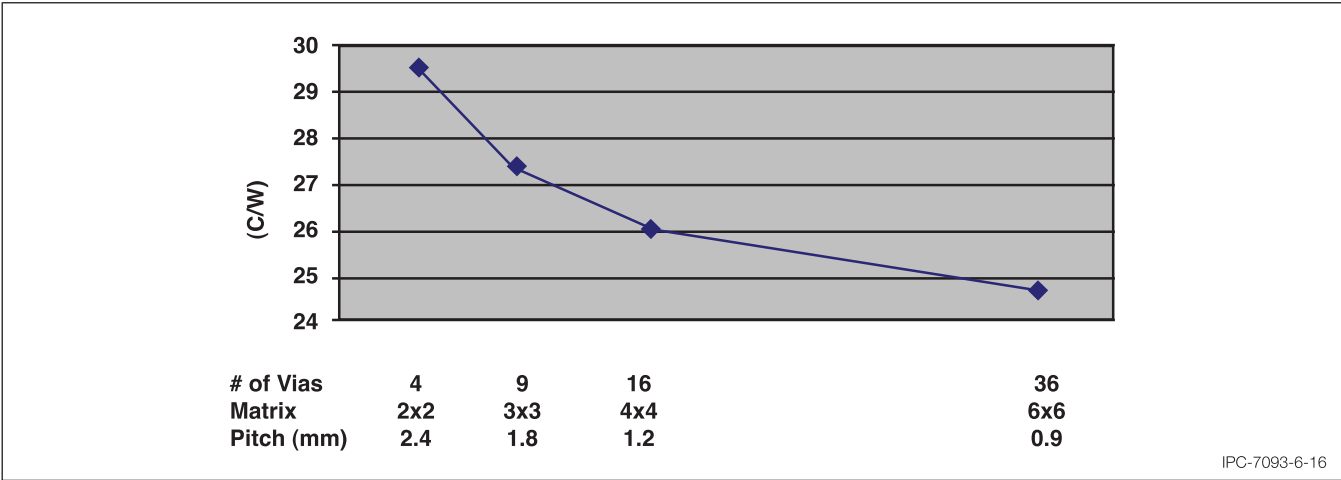


Figure 6-16 Effect of Number of Thermal Via on Package Thermal Performance

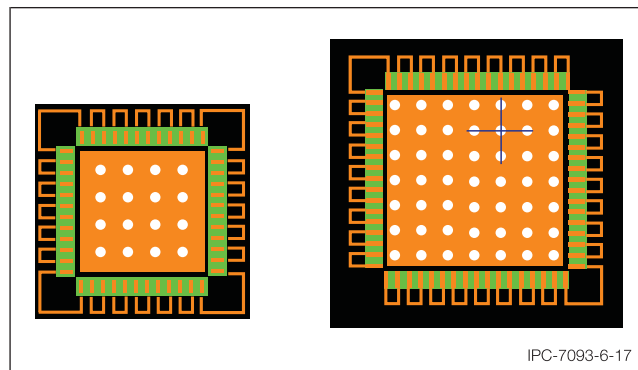


**Figure 6-17 PCB Thermal Pad and Via Array for 7x7 mm, 48 lead and 10x10 mm, 68 Lead Packages**

the advantage of allowing the designer to lay out his entire design using that value as a fundamental pitch. The first full metric pitch of 1.0 mm was established, from this point on the “80% Rule” has been in effect. The component pitches for IC packages that followed in service of the new convention were 0.8 mm, 0.65 mm, 0.5 mm, 0.4 mm and 0.3 mm.

The key thing to remember is that the “80% Rule” has been applied regardless of the component lead configuration, be it two sided, four sided or area array. The effect is illustrated in Figure 6-18. As can be seen in the graphic on the left, following the de facto 80% rule leads to greatly increase routing complexity as only 2 of the 5 grid pitches derived from the concept have ability to conform to a common grid based on the smallest defined lead pitch for component I/O (in this case 0.5 mm which is the accepted lower limit for effective soldering). This might seem a trivial concern but it has far reaching impact in design.

If components of varying grid pitch are used in the assembly as seen on the left side of the figure, the routing of interconnections will be more complex and more sophisticated routing tools are required and, more importantly more layers as well. In contrast, on the right side can be seen the same number of components with placement based on the use of a common grid pitch and wherein it can be seen that every component lead falls on grid. “Manhattan routing” is the term frequently used for electronic circuits using the principals of base grid, street and avenue routing. This has a number of compelling benefits.

For example, there is potential for much improved routability as the streets and avenues used for routing channels are perfectly defined making the routing much easier and faster. No less important is all of the circuit board real estate which can be potentially returned to use for components. Clearly, the mixture of peripheral and area array leads of various lead pitches results in much more complex circuit routing challenges. This necessitates the distancing of components and addition of many more circuit layers than would normally be required to accommodate the redistribution

wiring. Adding additional layers to make all of the required connections may actually reduce circuit performance. See Figure 6-18.

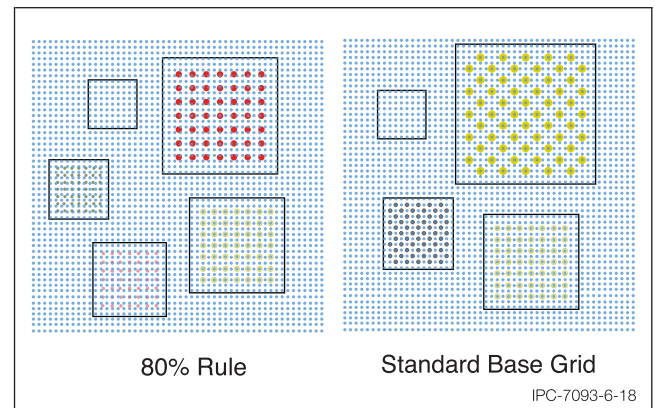


**Figure 6-18 Comparison of the 80% Rule with Standard Grid Systems for Routing Improvement**

BTC area array components based on the “80% Rule”, increase routing complexity requiring more sophisticated routing tools. Note that only 2 of the 5 grid pitches derived from the concept have the ability to conform to a common grid based on the smallest defined lead pitch for component I/O (in this case 0.5 mm). In contrast, on the right side of Figure 6-18 can be seen a number of components based on the use of a common grid pitch where it can be seen that every component lead falls on grid allowing for high efficiency “Manhattan routing” of circuits.

**6.1.5 Attachment Techniques** Because of the small metal pad termination surface area and the sole reliance on printed solder paste on the PCB surface, care must be taken to form reliable solder joints for BTC packages. This is further complicated by the large thermal pad underneath the package and its proximity to the inner edges of the leads. Although the pad pattern design suggested above might help in eliminating some of the surface mounting problems, special considerations are needed in stencil design and paste printing for both perimeter and thermal pads. Since surface mount processes vary from company to company, careful process development is recommended.

**6.1.5.1 Stencil Design for Perimeter Pads** Though it is not commonly their responsibility, the designer of the PCB should understand stencil design requirements. In general, the optimum and reliable solder joints on the perimeter pads should have about 50  $\mu\text{m}$  to 75  $\mu\text{m}$  standoff height and desirably, a fillet on the outside terminal ends if possible. A solder joint with good standoff height but no fillet, or minimal fillet at the terminal end, should still provide a reliable interface for most applications. The first step in achieving good standoff is the solder paste stencil design for perimeter pads. The stencil aperture opening should be so

designed that maximum paste release is achieved. This is typically accomplished by considering the following two ratios:

1. Area Ratio = Area of Aperture Opening/Aperture Wall Area; and
2. Aspect Ratio = Aperture Width/ Stencil Thickness

For rectangular aperture openings, as required for this package, these ratios are given as Area Ratio =  $LW/2T(L+W)$ , and Aspect Ratio =  $W/T$ , Where L and W are the aperture length and width, and T is stencil thickness. For optimum paste release the area and aspect ratios should be greater than 0.66 and 1.5 respectively. It is recommended that the stencil aperture should be 1:1 to PCB land sizes as both area and aspect ratio targets are easily achieved by this aperture. The opening can be reduced for the lead pullback option because of reduction of solderable area on the package. The stencil should be laser cut and electro polished. The polishing helps in smoothing the stencil walls which results in better paste release. It is also recommended that the stencil aperture tolerances should be tightly controlled, especially for 0.4 mm and 0.5 mm pitch devices, as these tolerances can effectively reduce the aperture size. More detailed information for stencil development is available in IPC-7525.

**6.1.5.2 Stencil Design for Thermal Pad** In order to effectively remove the heat from the package and to enhance electrical performance the die pad needs to be soldered to the PCB thermal pad. For larger thermal pad geometry it is recommended that the stencil be designed to

provide smaller multiple openings. This will typically result in 50 to 80% solder paste coverage.

**6.1.5.3 Via Types and Solder Voiding** Voids within solder joints can have an adverse effect on high speed and RF applications as well as on thermal performance. As the typical BTC package incorporates a large center pad, controlling solder voiding within this region can be difficult. Voids within this center plane can increase the current path of the circuit. The maximum size for a void should be less than the via pitch within the plane. This recommendation would assure that any one via would not be rendered ineffectual based on any one void increasing the current path beyond the distance to the next available via.

The presence of small voids in the thermal pad region is not likely to result in degradation of thermal and electrical performance. The specific thermal simulation shown in Figure 6–19 indicates that combining smaller multiple voids up to 50% of the thermal pad area, does not result in a loss in thermal performance. It should also be noted that the voids in thermal pad region do not impact the reliability of perimeter solder joints.

Large voids in thermal pad area should be avoided. In order to control these voids, via filling may be required. Filling the via holes, located in the DAP area, will prevent solder from wicking inside the via during the reflow solder process. There are different methods employed within the industry for this purpose: “via tenting” (from top or bottom side) using dry film solder mask, “via plugging” with liquid

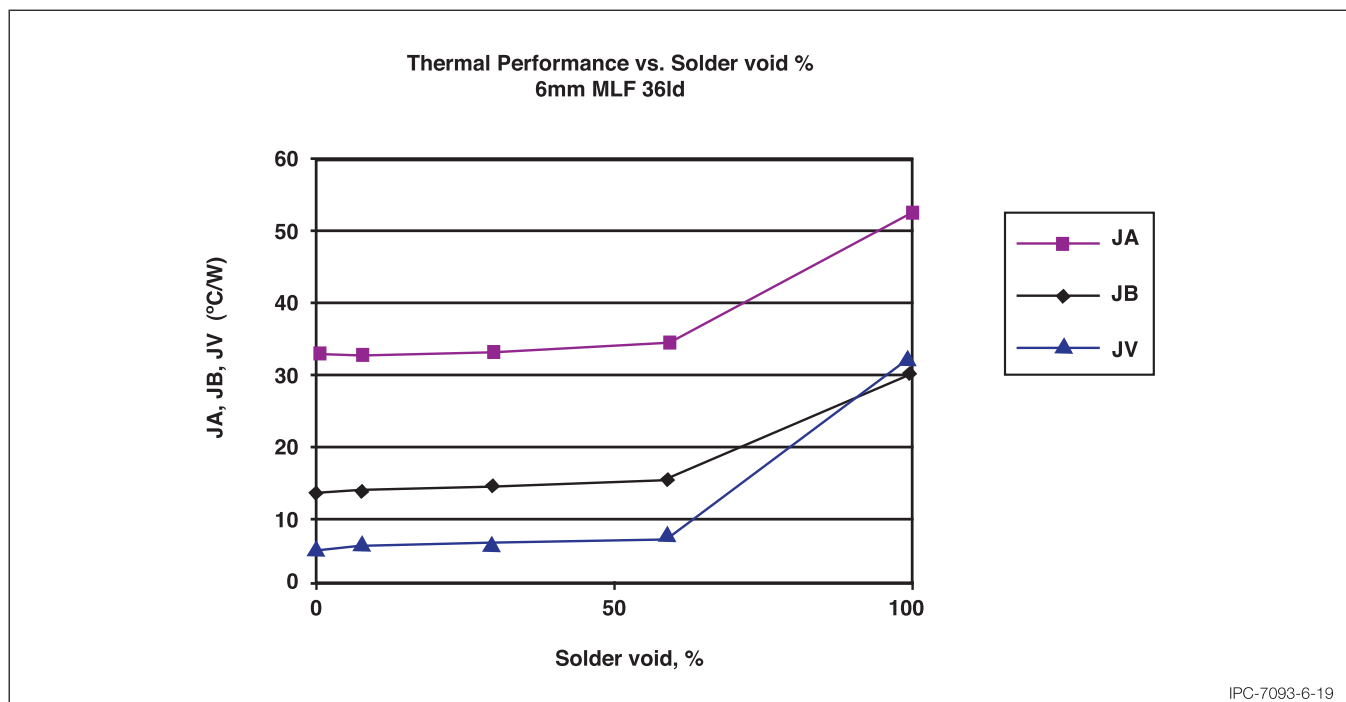


**Figure 6–19 Effect of Voids on Thermal Performance**

photo-imageable (LPI) solder mask from the bottom side, “via encroaching,” or “via capping.” Via filling is discussed more in 5.4.4.2.

All of these options have pros and cons when mounting QFN package on the board. While via tenting from top side may result in smaller voids, the presence of solder mask on the top side of the board may hinder proper paste printing. On the other hand, both via tenting from bottom or via plugging from bottom may result in larger voids due to out-gassing, covering more than two vias. Finally, encroached vias allow the solder to wick inside the vias and reduce the size of the voids. However, it also results in lower standoff of the package, which is controlled by the solder underneath the exposed pad. Figure 6–20 shows representative X-ray pictures of QFN packages mounted on boards with different via treatments. In case of via tenting, the solder mask diameter should be 100  $\mu\text{m}$  larger than via diameter.

Encroached via, depending on the board thickness and amount of solder printed underneath the exposed pad, can result in solder protruding from the other side of the board. It should be noted that the vias are not completely filled with solder, suggesting that solder wets down the via walls until the ends are plugged. This protrusion is a function of PCB thickness, amount of paste coverage in the thermal pad region, and the surface finish of the PCB. Manufacturers note that this protrusion can be avoided by using lower volume of solder paste and reflow peak temperature of less than 215°C in the case of SnPb soldering.

Via filling and capping is a good option to prevent the issues with tenting, flooding, and encroach vias though it does require a secondary process. It is important to ensure that the capping process produces minimal depressions in the

pad ( $<0.002$  in). By accepting larger depressions, air/gas entrapment within the depression may create voids that bridge between vias.

**6.1.5.4 Solder Joint Standoff Height and Fillet Formation** The design should facilitate the creation of a suitable solder joint standoff. Solder joint standoff is a direct function of amount of paste coverage on the thermal pad and the type of vias used for BTCs with an exposed pad at the bottom. It is worthwhile for the designer to know, that board mounting studies have shown that the package standoff increases by increasing the paste coverage and by using plugged vias in the thermal pad region.

The standoff height varies by the amount of solder that wets or flows into the PTH via. The encroached via provides an easy path for solder to flow into the PTH and decreases package standoff height while the plugged via impedes the flow of solder into the via due to the plugged via’s closed barrel end. In addition, the number of vias and their finished hole size will also influence the standoff height for encroached via design. The standoff height is also affected by the type and reactivity of solder paste used during assembly, PCB thickness and surface finish, and reflow profile. To achieve the preferred 50  $\mu\text{m}$  thick solder joints it is recommended that the solder paste coverage be at least 50% for plugged vias and 75% for encroached via types.

The peripheral solder joint fillets formation is also driven by multiple factors. Due to the singulation process during package assembly, a majority of the commercial non-pullback BTC devices are furnished with uncoated copper on the exposed terminal ends. The resulting bare copper on these surfaces will oxidize and may compromise solder wetting during typical reflow assembly process, especially if the packages are not stored in a controlled environment. Additional measures would need to be taken by suppliers to

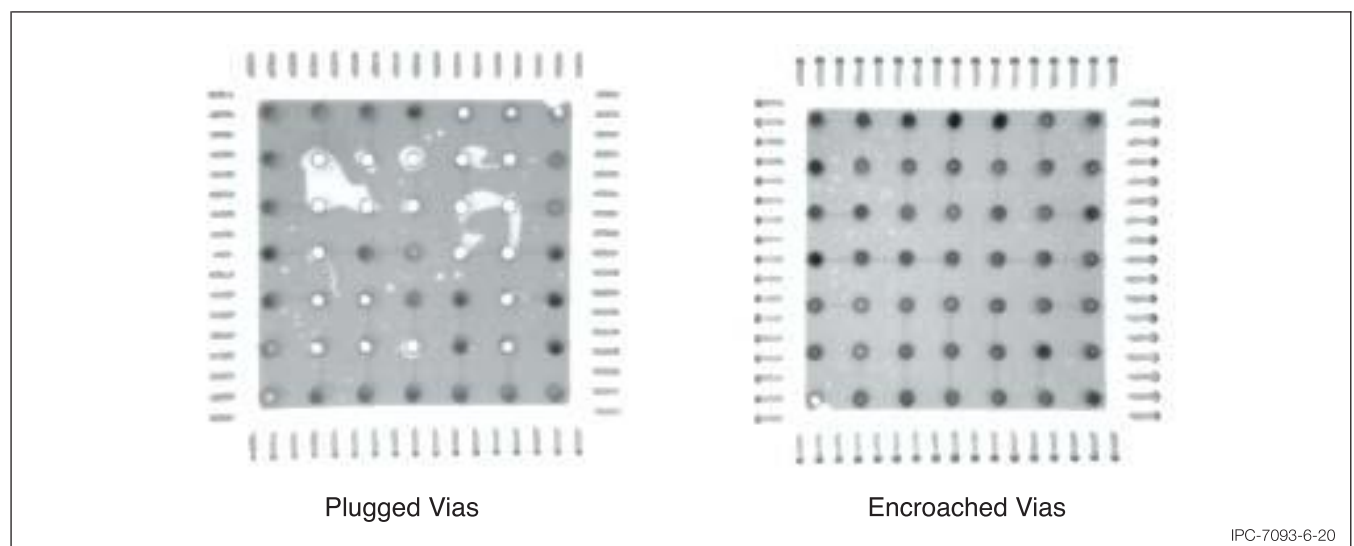
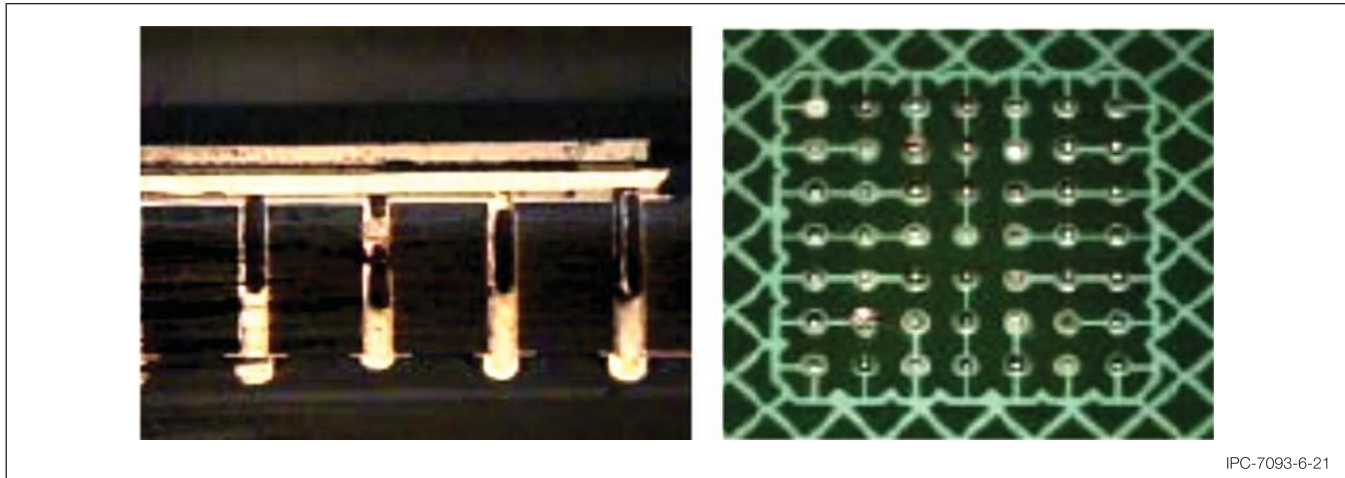


**Figure 6–20 X-Ray Example Showing Voids in the Thermal Pad**

IPC-7093-6-20



IPC-7093-6-21

**Figure 6-21 Solder Protrusion from the Bottom Side of PCB for Encroached Vias**

coat or plate exposed copper terminal ends to ensure solder wetting. It is, however, possible that a solder fillet will be formed depending on the solder paste (flux) used and the level of oxidation.

The fillet formation is also a function of PCB land size, printed solder volume, and the package standoff height. The land size concepts for toe and heel fillets, along with 1:1 aperture, will provide sufficient solder for fillet formation if the package standoff is not excessive. Since there is only limited solder available, higher standoff—controlled by paste coverage on the thermal pad—may not leave enough solder for fillet formation. Conversely, if the standoff is too low, large convex shape fillets may form.

When solder wetting to the exposed terminal ends of the BTC leads does occur, solder fillets will form along the BTC perimeter, especially when these parts are mounted on the PCB with a protruding land pattern and 1:1 stencil aperture for peripheral located land patterns. Since center land coverage and via type were shown to have the greatest impact on standoff height, the volume of solder necessary to create optimum fillet varies.

If protrusion of the solder through thermal vias cannot be avoided, the components may have to be assembled on the top side (or final pass) assembly, as the protruded solder will impede acceptable solder paste printing on the other side of the PCB. See Figure 6-21.

## 7 ASSEMBLY OF BTCs ON PRINTED BOARDS

The assembly processes for attaching BTCs requires careful process development and control. Process defect rates can be significantly reduced; however good process control is a necessity.

**7.1 PCB Surface Finish Requirements** A uniform PCB plating thickness is key for high assembly yield. There is no perfect surface finish. All finishes have some issues. Even

lead-free HASL is being reconsidered by some despite board warpage and uneven solder surface. When using immersion tin, some concern should be considered due to solderability and health concerns.

For an (ENIG) electroless nickel immersion gold finish, the gold thickness should range from 0.05  $\mu\text{m}$  to 0.20  $\mu\text{m}$  to avoid solder joint gold embrittlement. ENIG is a good choice but has black pad concerns; however, the concern is generally for PCBs when using BGAs. Black pad is less of a concern with BTCs.

Using a PCB with Organic Solderability Preservative coating (OSP) finish is also recommended as an alternative to Ni-Au. A high temperature OSP must be utilized if performing a lead-free soldering process. OSPs may not survive multiple reflow processes such as for double sided assemblies. OSP is a good choice (lower cost) but multiple reflow or hole-fill in wave are some of the key concerns in OSP. High temp OSPs are available to address these concerns but they do add to the cost.

Immersion silver is acceptable as a flat surface but other issues such as champagne voiding and caving from inadequate plating processes are concerns and must be addressed. Also, immersion silver shelf life is limited and this plating type will tarnish if not protected and may not be suitable for assemblies requiring multiple reflows. Immersion Silver addresses most of the issues in OSP but planar microvoids, creeping corrosion and tarnishing in salty and sulfur environments are a concern.

For a PCB with Hot Air Solder Leveling (HASL) finish, the surface flatness should be understood and monitored to ensure uniform solder connections across the BTC.

Since all surface finishes of some concerns, it may be wise to consider two finishes: OSP for single sided; ENIG and immersion silver for double sided and mixed (SMT and Through Hole) boards. Use of nitrogen in reflow and wave

will allow additional flexibility in using OSP but one can get away without nitrogen with ENIG even when using no clean flux. Use of aggressive flux allows additional flexibility. When using aggressive flux, OSP can be used even without nitrogen. So it is important to keep in mind that use of nitrogen, type of flux, reliability concerns and cost sensitivity play a critical role selection of surface finish. See Section 5.

For more information on surface finishes, see IPC-2221 and IPC-6012.

**7.2 PCB Design** Proper land pattern design is critical for maintaining high yields and good reliability of BTC solder joints. Figure 7-1 shows examples of good BTC land patterns; Figure 7-2 shows examples of poor land patterns for BTC type parts.

The solder pad on the device should be aligned with the lands on the board such that a complete solder connection is made between the device pad and the board land. Also, it is recommended for pull-back packages that the board land extend beyond the outer edge of the device package to allow visual access for inspection of solder joint flow.

**7.2.1 Consideration for Soldering Process** Because of the small terminal pad surface area and the sole reliance on printed solder paste on the PCB surface, care must be taken to form reliable solder joints for BTC packages. This is further complicated by the large thermal pad underneath some BTC packages and its proximity to the inner edges of the leads. Although the land pattern design might help in eliminating some of the surface mounting problems, special considerations are needed in stencil design and paste print-

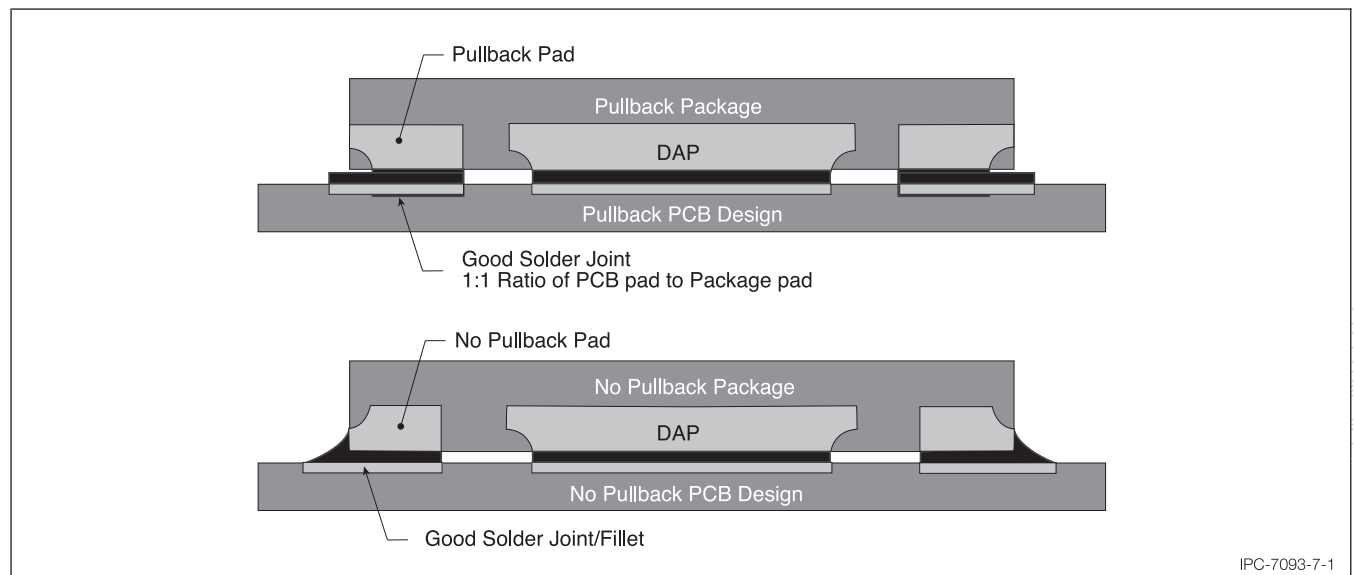


**Figure 7-1 Example of Good Land Patterns for Bottom Termination Components**

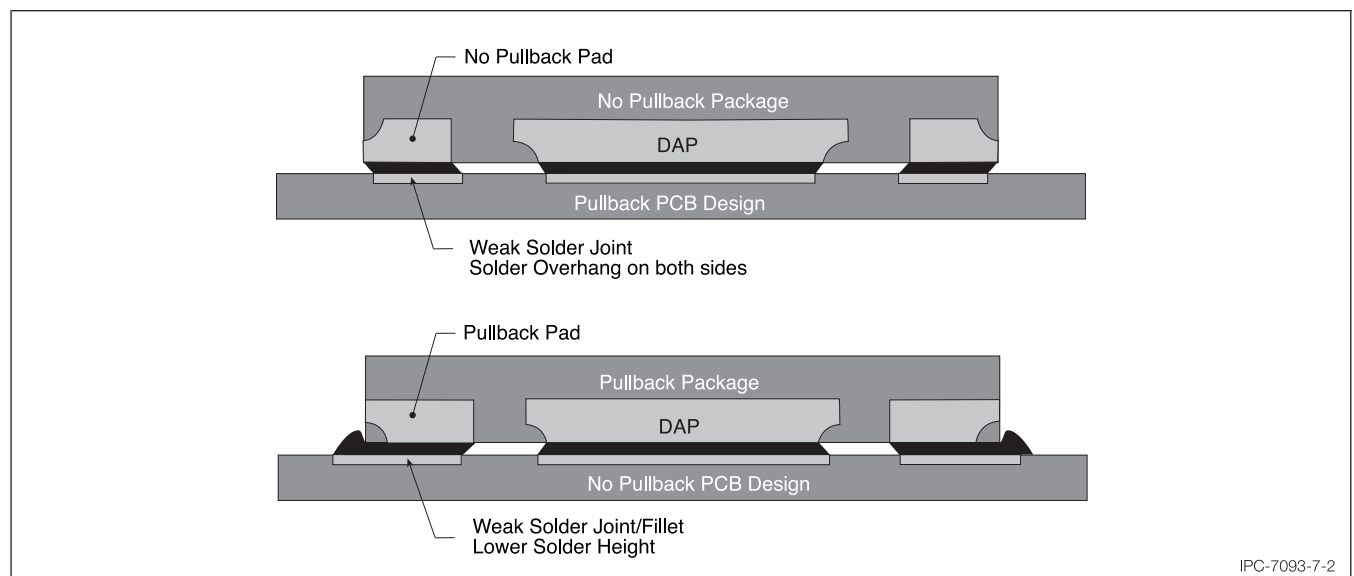


**Figure 7-2 Example of Poor Land Patterns for Bottom Termination Components**

ing for both perimeter and thermal pads. Since surface mount processes vary from company to company, careful process development is recommended.

**7.2.2 Component Preconditioning Bake** BTCs shipped in moisture barrier bags require special handling to insure proper surface mount conditions are met. The moisture barrier bag will be labeled with the proper instructions concerning the correct handling of the BTCs. BTCs exposed to room temperature and humidity conditions beyond the cumulative time specified on the label must be baked prior to surface mount reflow. The BTC size, thickness and MSL determine the bake times and conditions. Industry standard bodies such as JEDEC publish tables with bake times and temperatures. J-STD-033 should be followed to prevent damaging the BTC devices.

**7.2.3 Component Preparation for Assembly** Component solder dipping is not recommended for BTC terminal surface preparation. Dip soldering will not maintain coplanarity and makes the BTC unproducible during assembly. Inconsistent solder on the thermal plane can raise the BTC and cause the signal terminations to not make contact during reflow creating solder opens. Non uniform solder volume on the signal terminations can also create a non contact condition resulting in solder opens in random locations. See Figure 7-3.

Land pattern and thermal pad geometry on the PCB must be sized and aligned to ensure uncompromised electrical and mechanical interface with the BTC device. The example shown in Figure 7-4 illustrates the potential for compromising the solder interface between surfaces.

**7.2.4 Solder Paste and its Application** The quality of the paste print is a critical factor in producing high yield

reliable assemblies that use BTC technology. The surface mount assembly process uses solder paste to connect the BTC terminations to the lands on the board. Solder paste can be applied to the lands using several methods including screen or stencil printing and dispensing or jetting.

Solder paste consists of a homogeneous mixture of metal powder particles and flux. The metal content (typically 90% by weight) in the solder paste determines the amount of solid alloy in the solder joint. Metal powder particles are generally spherical in shape. A uniform powder shape aids the printing or dispensing process and it decreases the surface area, which minimizes oxidation.

Flux, solvent and jelling agent makes up the remainder of the solder paste volume. The activators in the flux remove oxides from the solder particles, the land patterns, and the BTC termination surfaces to promote good solderability during the reflow process. The solvents have an important role in controlling the tackiness of the paste and affecting the rheological properties. The formation of voids in the BTC solder joint may be related to the solvents in the solder paste. Solvents with low boiling points and/or improper reflow parameters can increase the incidence of voids in BTC solder joints.

For successful fine pitch BTC printing, the solder paste must pass through very small apertures in the stencil. The solder paste needs to remain printable and tacky for an extended period of time, and it must maintain print definition prior to and during reflow. Solder paste viscosity, particle size and stencil life are critical parameters for solder paste application.

Solder paste dispensing is not as widely used as printing due to a reduction in throughput speed; however, selective dispensing allows for more flexible paste volume deposition

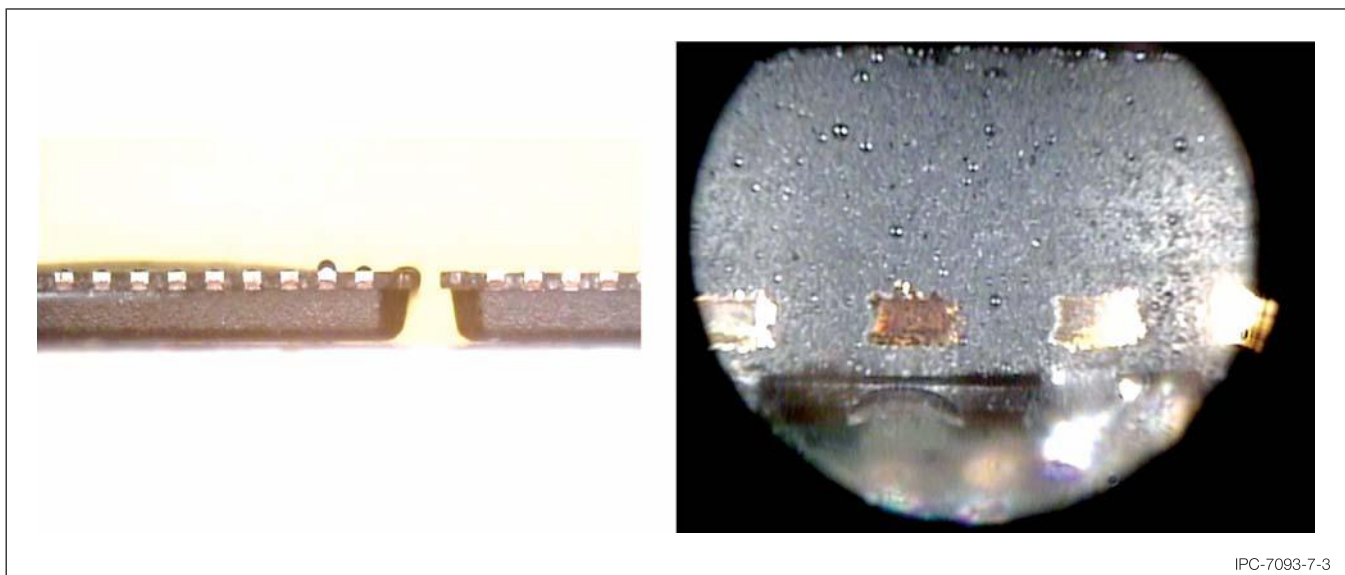


**Figure 7-3 Comparison of Solder Dipped and a Non Solder-Dipped BTC and Resultant No Solder Condition**

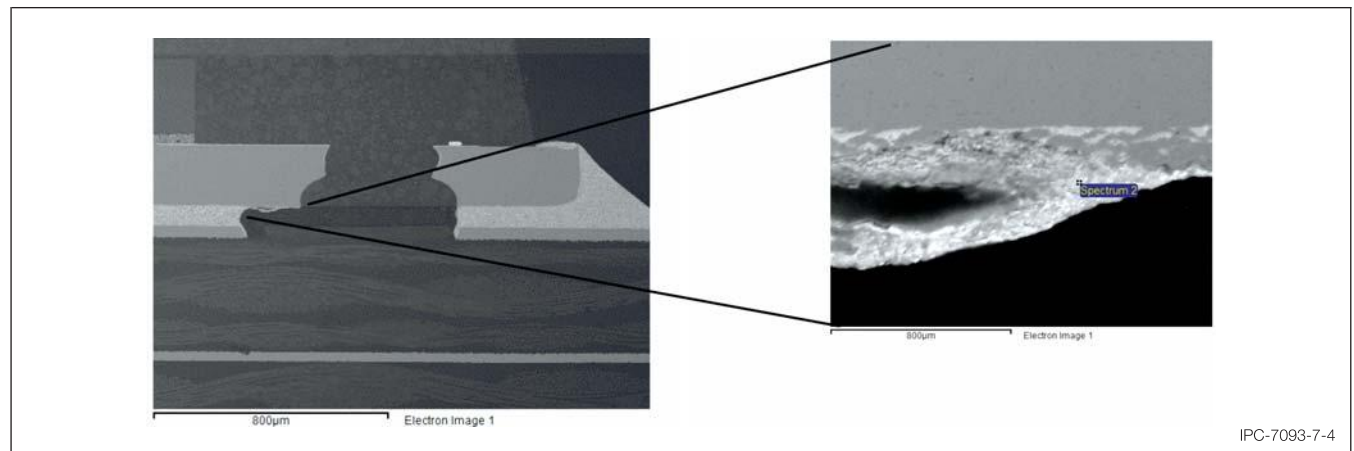


**Figure 7-4 Undersized PCB Pads Resulting in Potential Areas Where Pure Tin Finish Has Not Mixed with SnPb Solder Paste**

and placement for tighter process control. A technology referred to as solder paste “jetting” has greatly increased solder deposition speed while still allowing for the flexibility of volume and placement accuracy. The jetting technology, however, requires specific solder paste formulations which may have limited wide industry acceptance. Future refinements in the equipment and dispensing methods could make this technology more viable and desirable as a way of maintaining tighter process control.

**7.2.4.1 Particle Size and Paste Selection** A Type 3 or 4, low residue, no-clean solder paste (Sn63/Pb37 or 96.5Sn/3.0Ag/0.5Cu) is commonly used in mounting BTC packages; however, water soluble flux materials are also widely used. Solder paste composition is often a compromise given the variety of components which must be placed on a PCB, and special SMT specific solder pastes are being marketed by solder paste vendors that minimize voiding in the solder joint.

The solder particle size is classified by J-STD-005 (see Table 7-1).

**Table 7-1 Particle Size Comparisons**

| Solder paste type | Mesh      | Maximum particle size [µm] |
|-------------------|-----------|----------------------------|
| Type 2            | -200/+325 | 80                         |
| Type 3            | -325/+500 | 50                         |
| Type 4            | -400/+500 | 40                         |
| Type 5            | -500      | 30                         |

**7.2.4.2 Stencil Thickness and Aperture Design** The formation of reliable solder joints is a necessity. The large numbers of terminal contacts on some BTC type parts can present a challenge in producing a uniform solder print thickness. To this end, careful consideration must be applied to the stencil design. The stencil thickness, as well as the etched pattern geometry, determines the precise volume of solder paste deposited onto the device land pattern. Stencil alignment accuracy and consistent solder volume transfer is

critical for uniform reflow-solder processing. Stencils are usually made of stainless steel or electroformed nickel. Apertures should be trapezoidal to ensure uniform release of the solder paste to reduce smearing. The solder joint thickness for the attachment of BTCs should typically be 50 µm to 75 µm after reflow.

Aperture modifications:

- Specify  $\leq 0.6$  mm radius to inside corners of all apertures
- Reduce all 0.8 mm pitch and finer aperture widths to 50% of pitch
- Segment BTC thermal pad apertures to reduce printed solder volume by 50% or less, or as specified by the manufacturer’s recommendation

**Note:** Segmented solder paste deposits may not be required on some components. Apertures with a dimension greater than 5.0 mm [0.200 in] are broken into multiple apertures.

Stencil thickness:

It is recommended to use a 125 µm [0.005 in] stencil thickness for  $\leq 0.5$  mm [0.020 in] pitch or smaller and a 150 µm [0.006 in] stencil thickness for larger pitches. The stencil may require stepped areas to allow for both small pitches and larger pitches on the same board. Typical BTC arrays and passive components as small as 0402 and 0201 may also require a 125 µm thick stencil.

The stencil thicknesses should all be considered as recommendations for a Laser Cut stencil. A checkerboard pattern should be used on large thermal pads. Thickness of the stencil (C) is usually in the 100 µm to 150 µm [0.004 in to 0.006 in] range. The actual thickness of a stencil is dependent on other surface mount devices on the PCB. A squeegee durometer of 95 or harder or a metal squeegee should be used to distribute the paste. The blade angle, pressure, and speed must be fine-tuned to ensure even paste transfer. An inspection of the stenciled board is recommended before placing parts; as proper stencil application is

the most important factor with regards to reflow yields later in the process. See Figure 7-5.

In order to effectively remove the heat from the package and to enhance electrical performance the die paddle needs to be soldered to the PCB thermal pad. If the solder paste coverage is too large, it is recommended that smaller multiple openings in stencil be used instead of one big opening for printing solder paste on the thermal pad region. This will typically result in 50 to 80% solder paste coverage. Some examples of different stencil configurations are shown in Figure 7-6 describing ways to achieve an appropriate level of coverage.

**7.2.4.3 Importance of Paste Volume** It is very important to design a stencil aperture that will provide good paste release. In order to ensure good paste release, an aspect ratio of 1.5 minimum is recommended for laser cut foils. Aspect ratio is the ratio between stencil aperture width and stencil thickness. The aspect ratio relates to the manufacture of stencils and the solder paste stencil aperture and/or thickness and may need to be modified to maintain acceptable aspect ratio.

Using thicker stencils may increase the probability of balling and bridging, while compensating for the increased thickness with a reduction in aperture size diminishes the release efficiency, leading to less predictable printed volume. Using thinner stencils necessitates the use of a 1:1 aperture to feature ratio which increases the chances of even minor misalignment causing balling, while any reduction in the aperture to feature ratio or less than perfect release threatens insufficient volume, starved or open joints, and may lead to poor mechanical strength.

Regardless of the stencil features, proper care must be given to the printing process at the assembler's facility and are best handled by qualified technical staff. The preparation,

paste rheology, handling time, standoff distance, blade hardness and speed, and re-flow process details are critical in conjunction with careful stencil design to ensure maximum yield and minimum failure rates. It is important to find out what printing techniques are used at any assembly facility where the BTC will be installed. Each of these sites should be able to provide recommendations for stencil design limitations.

Another commonly used ratio and preferred technique is area ratio. An area ratio of greater than 0.66 is recommended for laser cut foils. The formula to calculate area ratio is the area of the stencil aperture divided by the area of the stencil aperture walls. Area of aperture divided by area of aperture walls equals  $L*W/2*(L+W)*T > 0.66$ .

The stencil aperture opening should be designed such that maximum paste release is achieved. This is typically accomplished by considering the following 2 ratios and Figure 7-7.

$$\text{Area Ratio} = LW / 2T (L + W)$$

$$\text{Aspect Ratio} = W/T$$

Where L and W are the aperture length and T is the stencil thickness

$$\text{Aspect Ratio} = \frac{\text{Aperture Width (W)}}{\text{Stencil Thickness (T)}} > 1.5$$

$$\text{Area Ratio} = \frac{\text{Area of Aperture (L} \times \text{W)}}{\text{Area of Aperture Walls (2} \times \text{(L} + \text{W)} \times \text{T)}} > 0.66$$

**Note:** If the apertures are different than described above, then recalculate the area ratio. But for simplicity, the previous equation may be used and will result in a slightly conservative number.

Use of electroform stencils can yield success with area ratios of <0.6. IPC-7525 Stencil Design Guidelines contains more information on other stencil design rules.

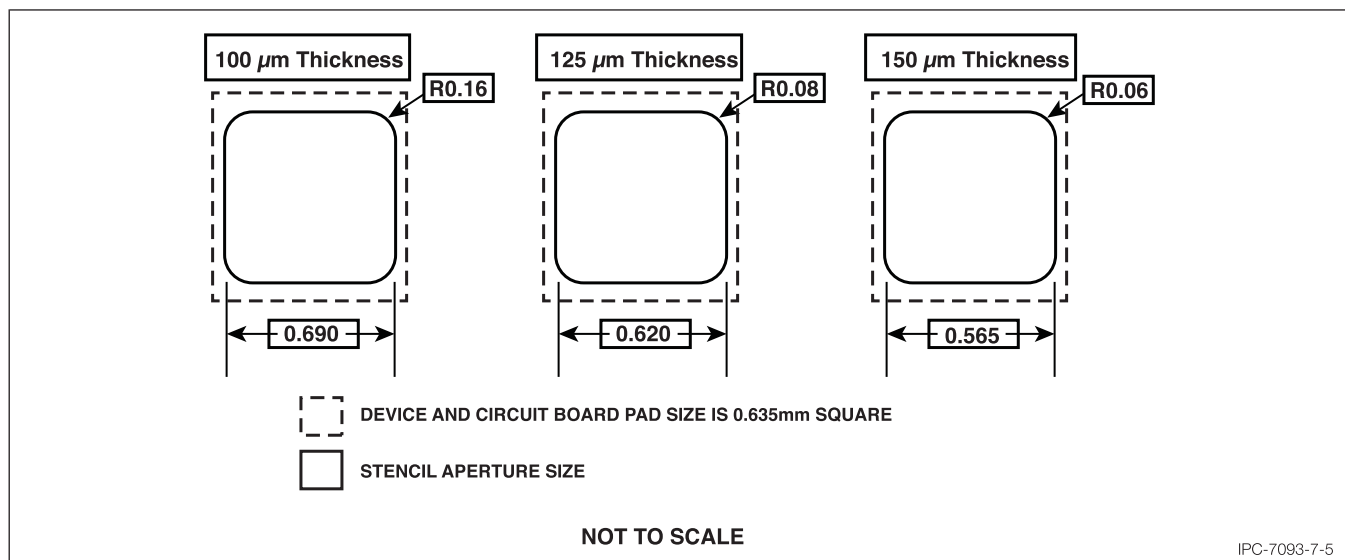


Figure 7-5 Recommended Aperture Dimensions for Commonly Used Stencil Thicknesses

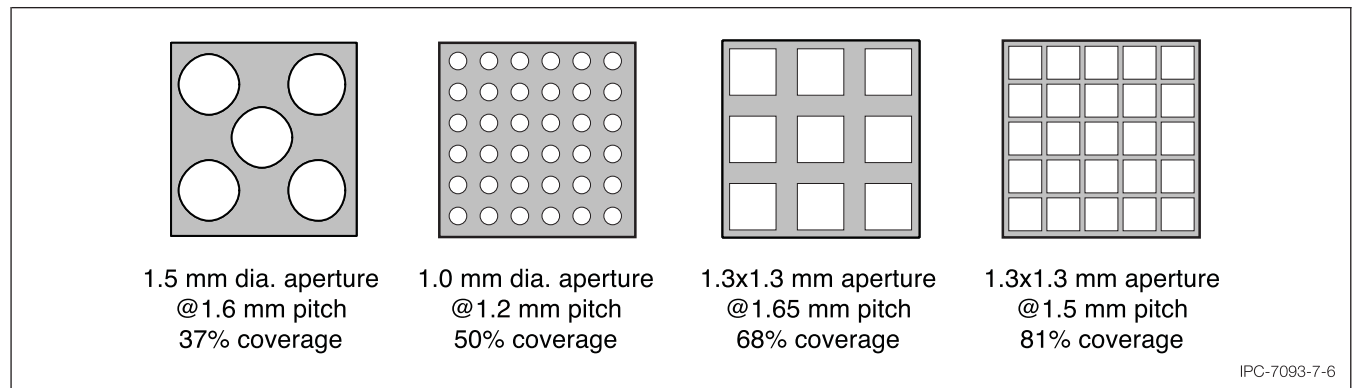


**Figure 7-6 Thermal Pad Stencil Designs for 7x7 mm and 10x10 mm BTC Devices**

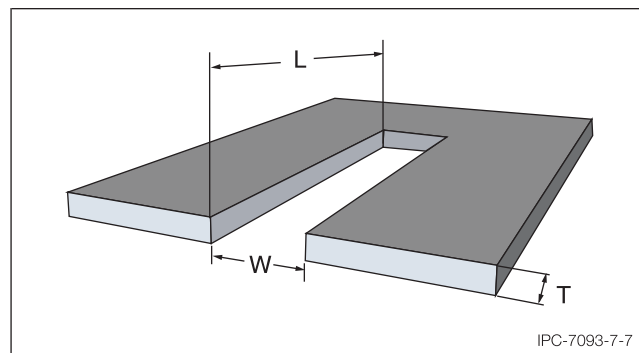


**Figure 7-7 Solder Stencil Aperture Wall Area**

In addition to the variable constraints in stencil thickness and aperture design to balance volume and proper release, gold embrittlement is an issue with some BTC components that have a gold finish (more so when also combined with an ENIG finish PCB). In order to get enough volume to mitigate embrittlement, there may be situations where thicker stencils or overprinting may be considered. However, these methods for applying solder can lead to issues with solder paste release and bridging.

**7.2.5 Component Placement Impact** The pick and place accuracy governs the package placement and rotational

alignment. This is equipment and process dependent. Slightly misaligned parts (less than 25 percent off the land center) will automatically self-align during reflow (see Figure 7–8). Grossly misaligned packages (greater than 50 percent off land and pad centers) should be removed prior to reflow as they may develop electrical shorts, as a result of solder bridges during reflow solder processing.

**7.2.5.1 Vision Systems for Placement Accuracy** Placement accuracy is a very critical part of the BTC process. It is strongly recommended to not move a BTC after machine placement to correct placement problems as this may cause solder bridging in adjacent solder joints, since the connections cannot be seen visually. The placement machine's accuracy is largely dependent on the vision system and the ability of the nozzle to hold the component. Matching the vision system to the application is also important. The vision system determines the X, Y and theta offset of each component prior to placement. In addition to determining the component offset, the vision system can also inspect the component for dimensional integrity. Charge-Coupled Device (CCD) camera-based systems employ two lighting methods, referred to as binary and gray scale. Both methods can be sensitive to contrast and lighting changes.

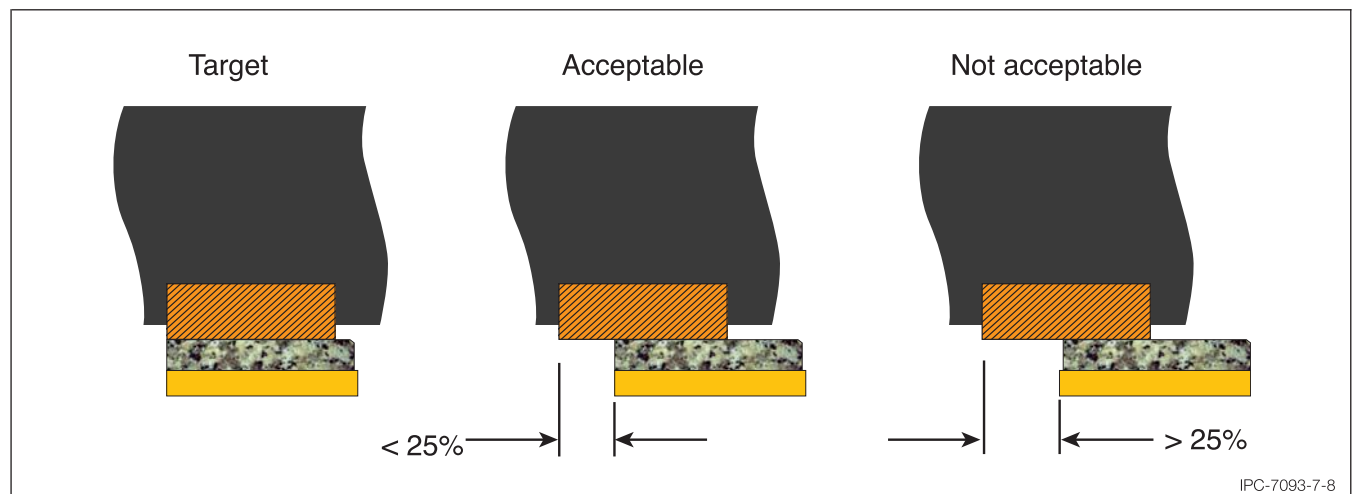


**Figure 7-8 Assessing Maximum Pre-Reflow Off-Land Acceptance**

There are two popular methods for package alignment using machine vision: package silhouette, where the vision system locates the package outline; and terminal recognition, where the vision system locates the terminals or leads of the package.

Some vision systems can directly locate on the pad metalization pattern. Both methods are acceptable for BTC placement. The terminal recognition type alignment tends to be more accurate, but is also slower since more complex vision processing is required of the pick and place machine. The package silhouette method allows the pick and place system to run faster, but is generally less accurate. Both methods are acceptable, and have been successfully demonstrated by major pick and place equipment vendors and contract PCB assembly houses.

Depending upon the type of pick and place system, a change in package carrier format may be required. Local fiducials may also be helpful in helping the vision systems recognize the exact location of the land pattern for the BTC, similar to what is used for fine-pitch peripheral leaded parts.

Gray scale systems use front lighting, which illuminates the component from below. Surface features are reflected into the CCD camera for processing. Binary systems use back lighting, which illuminates the component from above. The outline of the component is projected into the CCD camera for processing. Binary imaging, which is the older of the two methods, locates a feature using the contrast between black and white images. Gray scale systems can usually interpret 256 levels of contrast. Both systems use an algorithm to determine the center of the component. Binary imaging requires less computing capability than gray scale imaging.

Gray scale imaging places BTC components based on land location while binary imaging places BTC components based on the component outline. In some cases the tolerance between the BTC outline and the location of the printed board lands is significant. Gray scale imaging is more

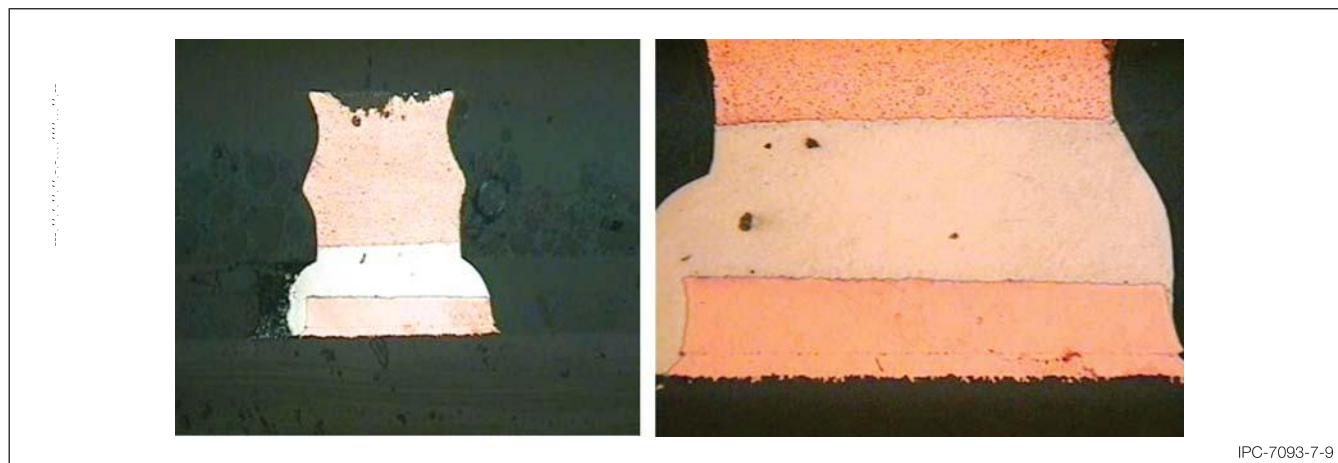
desirable for placing BTC components because it eliminates placement error due to variations in the component outline.

Placement machine nozzle designs vary from supplier to supplier. It is important that the correct nozzle is chosen which will have sufficient surface area to hold the part without any shifting during the placement process. The nozzle must gasket against the part, not allowing vacuum leakage. Tactile sensing, which helps control the Z axis (vertical) stroke of the spindle, is desirable because it prevents a component from being crushed between the vacuum nozzle and the substrate.

Also, without leads or balls to act as a hard stop or standoff, extra care must be taken to limit the Z axis pressure of the part into the solder paste, which can result in solder shorts.

**7.2.6 Reflow Soldering and Profiling** As with all SMT components, it is important that profiles be monitored on all new board designs. In addition, if there are multiple package types on the board, the thermal profile should be measured at multiple locations. Component temperatures may vary because of surrounding components, location of the device on the board, and package densities. To maximize the self-alignment effect of a BTC (see Figure 7–9), it is recommended that the maximum reflow temperature specified for the solder paste not be exceeded. A good guide is to subject the PCB to a temperature ramp not exceeding 4°C per second. The reflow profile guidelines are based on the temperature at the actual solder pad to PCB land pad solder joint location.

The actual temperature at the solder joint is often different than the temperature settings in the reflow system due to the location of the system thermocouple placement. The reflow system needs to be profiled using thermocouples at various locations on the PC board. Thermocouples should be placed on one of the largest as well as the smallest components on the PCB. It is suggested that the peak temperature differential between the smallest and largest package be 10°C or



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**Figure 7-9 Metal Defined Land Solder Joint**

less for average size PC boards. See J-STD-020 for reflow recommendations. BTCs are typically moisture sensitive and fall into level classifications defined by JEDEC. Specific levels are stated on moisture sensitive labels shipped with BTC devices. Commercial BTC devices may be compatible with SnPb and/or lead-free solder processing and the supplier is responsible for defining the maximum reflow profile limit (e.g., 215–245°C peak body temperature). See IPC-1756.

#### 7.2.6.1 Example of Thermal Profile Development

Solder paste is applied and a sample BTC is mounted on a specific board intended to be assembled using a lead-free solder paste. The board was a four layer multilayer board, 1.5 mm thick, 75 mm by 95 mm in size, and was to be sent through a reflow oven using a lead-free assembly. Thermocouples were placed on the BTC lands and on the bottom of the FR-4 board to monitor the temperatures at these locations. A third thermocouple to monitor the oven environment temperature was also attached on top of the FR-4 board. The temperature profile was monitored in seven different oven zones, approximately 30 seconds apart. The data gathered and the temperature profile used to mount the sample BTC to this board is shown in Table 7–2, Table 7–3 and Figure 7–10. To achieve this profile, the oven environment was set to 260°C maximum with a maximum zone slope of 2.0°C/sec.

From Table 7–2, it is important to note that the sample BTC only achieves a maximum temperature of 240°C even though the oven temperature is set to 260°C. This is consistent with the reflow requirements of 250°C maximum for the BTC body temperature. Analyses of the solder joint obtained from this profile indicated excellent joint formation. Table 7–3 shows the profile variation between a tin/lead profile and those used for lead-free SAC alloys.

Figure 7–11 and Table 7–4 show the details for several SAC alloys used in developing a specific profile for two versions of SAC.

#### 7.2.6.2 Unique Profile for Each Printed Board Assembly

There is some misunderstanding by some people that one convection oven profile will work for all boards and hence there is no need for developing a unique profile for each board. This is simply not true because each board has a different thermal mass and one may have different loading patterns (distance between boards as they are loaded in the oven). Even the same double-sided board, depending upon component placement and distribution of copper planes on each side, may require a different profile for each side. A specific profile for each printed board assembly may be needed since a different thermal mass could be associated with each board. This is recommended so that a proper profile is assured.

**Table 7-2 Typical Reflow Profile for Eutectic (63Sn/37Pb) Solder Paste**

| Profile Elements            | Straight Line Profile              | Low Soak Profile               |
|-----------------------------|------------------------------------|--------------------------------|
| Ramp rate                   | 0.8 – 1.2°C/sec (RT to Peak temp)  | 1.5 – 2.0°C/sec (RT to 145°C)  |
| Dwell @ 145 to 160°C        | N/A                                | 30 – 120 seconds               |
| 2nd Ramp rate               | N/A                                | 1.5 – 2.0°C/sec (to Peak temp) |
| Time above liquidus (183°C) | 45 – 75 seconds                    |                                |
| Peak temperature range      | 210 – 225°C typical (240°C max)    |                                |
| Ramp-down rate to RT        | 1 – 3°C/sec typical, (4°C/sec max) |                                |

**Note:** For details, please refer to solder paste manufacturer's recommendation

**Table 7-3 Profile Comparison Between SnPb and SAC Alloys**

| Profile Topic                          | SnPb Alloy       | Lead-free Alloy (SAC) |
|----------------------------------------|------------------|-----------------------|
| Alloy Solidus temperature              | 183°C            | 217–220°C             |
| Alloy soldering temp range             | 210–220°C        | 235–245°C             |
| Minimum peak reflow temperature **     | 205°C            | 230°C                 |
| Component ramp up rate                 | 1–4°C/sec *      | 1–4°C/sec *           |
| Component ramp down rate               | 2–4°C/sec *      | 2–4°C/sec *           |
| Soak or preheat activation temperature | 100–180°C *      | 140–220°C *           |
| Soak or preheat activation time        | 60–120 seconds * | 60–150 seconds *      |
| Dwell time above liquidus              | 60–90 seconds    | 60–90 seconds         |
| Dwell time at peak temp.               | 20 seconds max   | 20 seconds max        |

\* Verify with the supplier

\*\* Coolest Temperature on the board

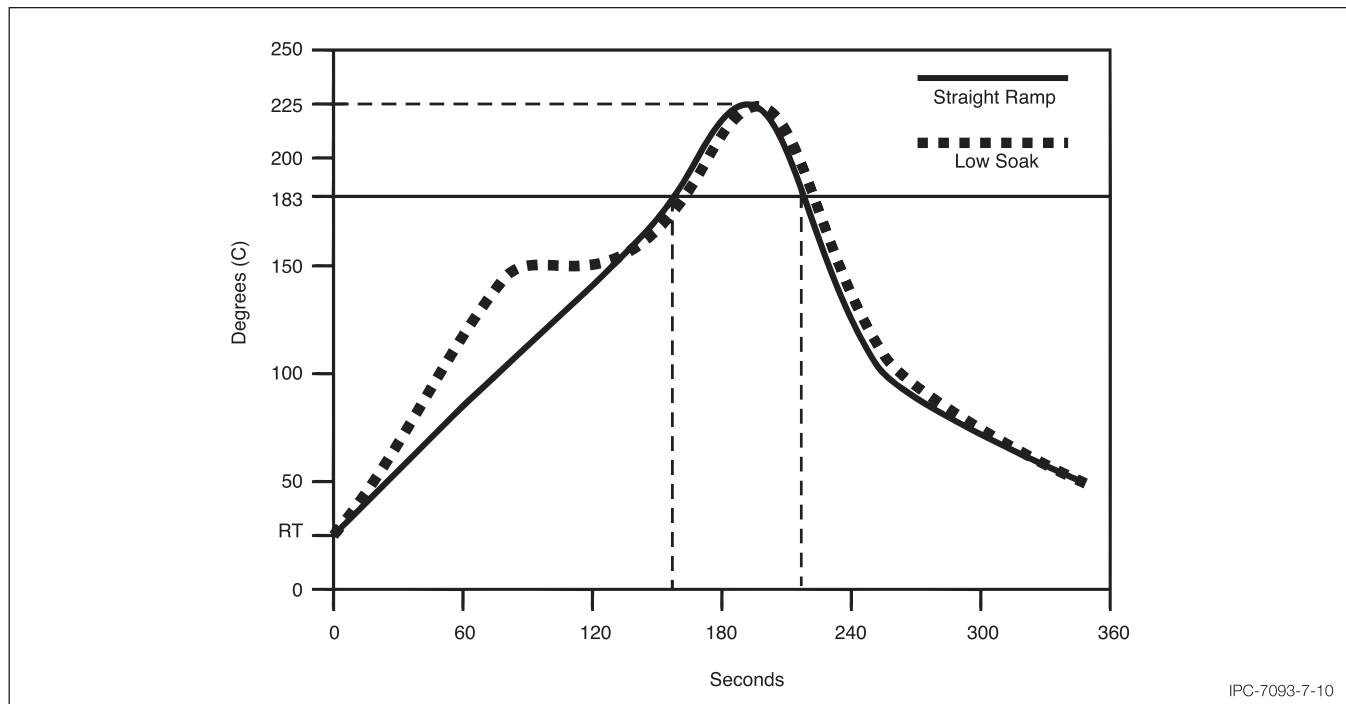


Figure 7-10 Profile for Tin/Lead Solder Reflow

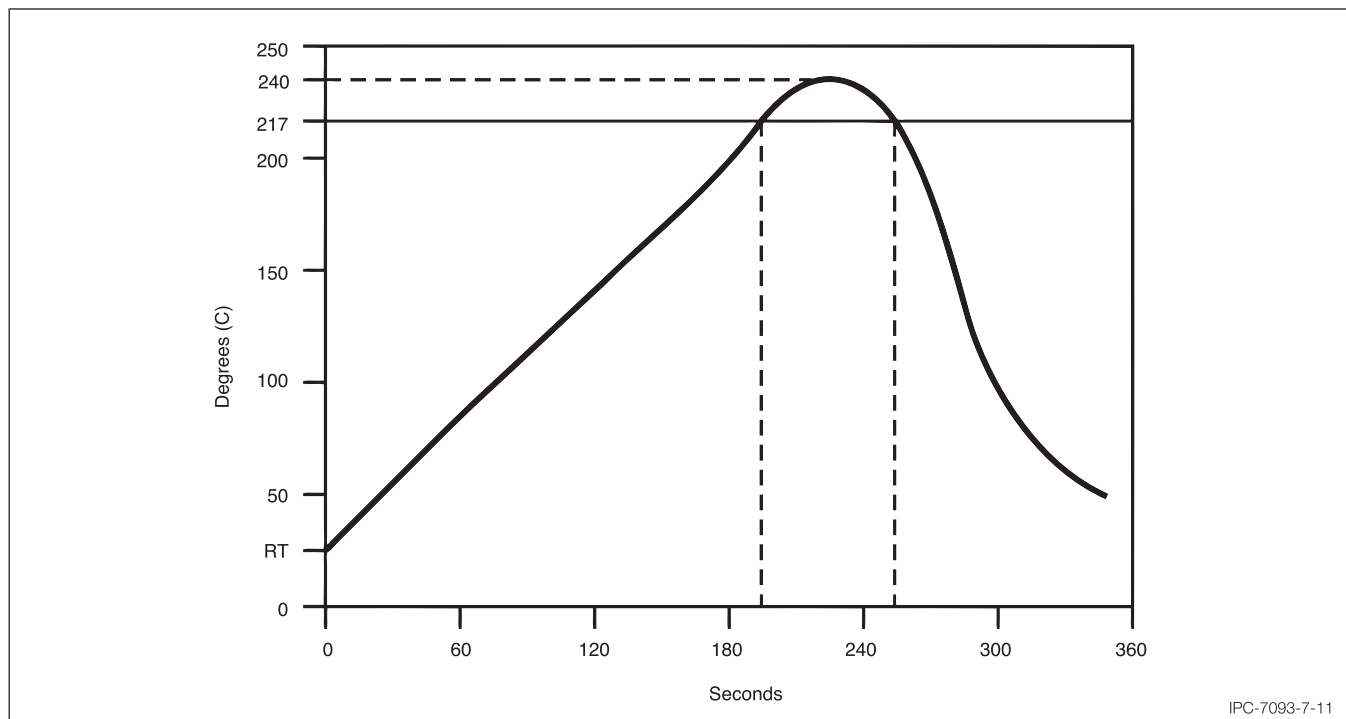


Figure 7-11 Profile for SAC Alloy Solder Reflow

There is also a misconception that if you need to change a profile, simply change the belt speed. Having to change only the belt speed is certainly easy, but it may not be the right approach. Changing the belt speed changes the temperature of the board in every zone. Consideration must be made for the thermal profile to ensure the large thermal masses achieve accurate reflow while not causing an excessive temperature condition on the small thermal masses.

**7.2.7 Reflow Process Impact on Material** Flux has two key attributes. First it must remove contamination and, second, it must protect the solderable surfaces after contamination removal. A common mistake is to use a time/temperature profile that consumes the flux before the solder melts. Ideally, the flux would be consumed just as the solder begins to melt. Activation time should range from 90 to 120 seconds. Flux usually becomes active at around

**Table 7-4 Typical Reflow Profile for Lead-Free  
(SAC305 or SAC405) Solder Paste**

| Profile Elements            | Convection or IR                   |
|-----------------------------|------------------------------------|
| Ramp rate (RT to Peak temp) | 0.8 – 1.2 °C/s                     |
| Time above liquidus (217°C) | 35 – 80 seconds                    |
| Peak temperature range      | 235 – 240 °C typical (260°C max)   |
| Ramp-down rate to RT        | 1 – 2 °C/sec typical (6°C/sec max) |

**Note:** For details, please refer to solder paste manufacturer's recommendation

130°C for tin lead solder pastes. Typically, solder paste activation for lead-free solder will be higher, in the 150°C range; however, it is recommended to work with your solder paste supplier for recommendation on that specific solder paste.

Component termination finish will affect solderability. There are a number of component terminal finishes being used today, including tin/lead, gold, tin and palladium. It is important to select a flux and solder alloy that works well with the finish being used on the BTCs.

Components can be damaged by the incorrect application of heat. All components have a heat exposure limit. Most tin/lead compatible surface mount components should tolerate a peak temperature of 220°C for up to 60 seconds. Lead-free BTCs will be rated to a higher temperature which is approximately 240–260°C. Thermal shock, caused by the rapid application of heat, can crack certain components. However, since the peak temperature of reflow ovens varies, the intent is to heat the solder in a controlled established profile to a solder joint temperature of 210–220°C for tin-lead products and for 235–245°C for lead-free products.

Warpage is another consideration as BTCs packages become larger. Flatness is important to proper seating of the package and solder joint reliability. The higher temperature reflow profile required for lead-free soldering may cause excessive PCB warpage and should be evaluated.

**7.2.8 Vapor Phase** Vapor phase reflow can be operated as a single fluid system or a two fluid system, utilizing a primary and a secondary fluid. The process was developed using the two-fluid approach in batch equipment; but modern in-line systems are normally operated with only one fluid. Whichever system is used, the maximum temperature reached by assemblies in vapor phase (VP) reflow depends on the choice of the primary fluid. Primary fluids are available in a number of temperature ranges, with 218–222°C being common with tin lead products and 235–245°C for lead-free products. While all the primary fluids can be classed as perfluorocarbons, the basic structure (amine, cyclic or ether) will determine the key properties of in-use stability solder paste chemicals solubility and overall process economics. The choice of a fluid is normally based on the melting point of the solder alloy to be reflowed.

For the range cited, the lower temperatures are suitable for the typical tin/lead or tin/lead-silver alloys used for standard attachment processes. The upper end of the range will permit reflow of high lead alloys, which are used to attach pins to PGA packages. Users faced with reflow of a specialty alloy have been successful in mixing two primary fluids to tailor a vapor phase system for a specific stable boiling point. Higher temperatures will permit shorter times, which may be advantageous with some solder pastes.

The primary vapor phase should be inert and not introduce contaminants that must be removed later. Solder paste chemicals that dissolve in the fluid are carried in the high boiling vapor then deposited on the surface of the boards. Such residues tend to be difficult to remove. Minimizing solder paste residue in the primary fluid will maximize the lifetime of the fluid, prevent boiling point elevation due to dissolved paste ingredients, and simplify cleaning.

The secondary vapor blanket was originally CFC-113, a lower boiling fluorinated material, which formed a low cost sacrificial 'lid' over the more costly primary fluid. The constant exposure to the high boiling primary fluid at the interface of the two fluids could cause the secondary fluid to undergo thermal decomposition at the interface, generating HCl (hydrochloric) and HF (hydrofluoric) acid vapors. These corrosive vapors often attacked the soldering equipment over time. While in theory the vapors could be absorbed in flux residues and cause problems for high reliability products, this was rare in comparison to the attack on the equipment.

With the phase out of CFC-113, a low boiling perfluorocarbon was introduced to replace it. This second generation secondary blanket fluid was more stable than CFC-113 for prolonged exposure to the high boiling vapor phase fluids. As surface mount technology grew, most users converted to the higher throughput in-line machines, which used the single fluid approach. Defluxing after vapor phase reflow should be done with either a bipolar solvent formulation or include an aqueous cleaning formulation that can ensure removal of all the solder paste residues, with the choice of cleaning process based on the composition of the solder paste. Secondary factors influencing the decision would be compatibility, and the component to PWB surface spacing. In addition, most companies gave serious thought to con-

sidering the potential chemical loss from using this type of equipment since many perfluoro compounds are very long-lived global warming compounds.

**7.2.9 Cleaning vs. No-Clean** Residue from the surface mount process can create resistive connections between pads on BTC packages. If a low residue, no-clean solder paste is used, PCB cleaning is not required and has little effect on a BTC. With the elimination of materials containing CFCs, most companies have moved to a no-clean or aqueous flux-based system.

“No clean” fluxes and solders simply mean that there are no harmful residues left on the board that could cause corrosion or damage to the components if left on the board. Residues have sometimes been shown to be a collection point for outside contamination on the board surface. Because there are so many different types of no-clean solder pastes available, application specific evaluations should be performed to identify if any remaining residue still needs to be removed from the boards in final production.

The cleaning process itself must be analyzed to ensure that no residual cleaning material is left behind under the parts. Because of the low profiles and the geometry of the BTC, cleaning solution may penetrate under the part but may not always completely rinse out. Depending on the chemistry used, this could introduce long-term reliability concerns. Refer to IPC-CH-65 and IPC-9201 for guidance in cleaning assemblies.

**7.2.10 Package Standoff** The package standoff is one of the prime parameters determining the reliability of the BTC solder joints. Package standoff for a BTC is defined as the distance between the land on the bottom of the package substrate and the land on the top of the board surface. This distance varies depending on the volume of solder paste. When BTCs are soldered onto the board, the flux and solvent within the printed paste material separates from the alloy. The post-reflow standoff height will be approximately 50% of the original solder paste thickness. The standoff height on all BTCs should be verified during the set up of your process. It is recommended to establish the process to reproduce the standoff height for specific components.

The standoff height is also affected by the type and percent of powder in the solder paste, PCB surface finish, and reflow profile. Standoff heights are inversely proportional to the land diameters, i.e., as land diameters increase, stand off heights decrease. For non-solder mask defined (NSMD) lands, a solder mask relief around the land may reduce the standoff height, because the solder will wet out along the conductors as well as along the edges of the land. This is shown in Figure 7–12.

Additionally, the figure shows lead-free, SAC-305 solder paste did not readily flow down ground land thermal

dissipation vias. The X-ray pictures confirm that only minimal solder actually flowed down the ground land vias; some voiding is seen but does not hurt thermal dissipation or reliability.

Factors that determine the post-reflow BTC package standoff from the board include the BTC package weight, the volume solder paste, the land size and land configuration (solder mask defined or non-solder mask defined). However, for packages with a large I/O count, the package weight may have less effect on the standoff height.

For QFN components the solder joint standoff is a direct function of amount of paste coverage on the thermal pad and the type of vias used for BTCs with exposed pad at the bottom. Board mounting studies have shown that the package standoff increases by increasing the paste coverage and by using plugged vias in the thermal pad region. The standoff height varies by the amount of solder that wets or flows into the PTH via. An open via provides an easy path for solder to flow into the PTH and decreases package standoff height while the plugged via impedes the flow of solder into the via due to the plugged via's closed barrel end. In addition, the number of vias and their finished hole size will also influence the standoff height for open via design.

The standoff height is also affected by the type and reactivity of solder paste used during assembly, PCB thickness and surface finish, and reflow profile. To achieve 50 micron thick solder joints, which help in improving the board reliability, it is recommended that the solder paste coverage be at least 50% for plugged vias and 75% for encroached via.

The fillet formation is also a function of PCB land size, printed solder volume, and the package standoff height. The land size recommended for most BTCs, along with 1:1 stencil aperture, will provide sufficient solder for fillet formation if the package standoff is not excessive. Since there is only limited solder available, higher standoff—controlled by paste coverage on the thermal pad—may not leave enough solder for fillet formation. Conversely, if the standoff is too low, large convex shape fillets may form. This is shown in Figure 7–13.

The figure also shows that although the contact ends are not plated solder fillets were still formed when these parts are mounted on the PCB with a protruding land pattern and 1:1 aperture for peripheral leads. Since center pad coverage and via type were shown to have the greatest impact on standoff height the volume of solder necessary to create optimum fillet varies. Package standoff height and PCB pads size will establish the required volume.

If solder protrusion cannot be avoided, the components may have to be assembled on the top side (or final pass) assembly, as the protruded solder will impede acceptable solder paste printing on the other side of the PCB.



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**Figure 7-12 SAC Alloy Flow Characteristics**



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**Figure 7-13 Post Assembly Contact and DAP Solder Joint Profile**

**7.3 Post-SMT Processes** There are several processes that must be considered after the reflow operation. Some of these are shown in the following sections and require various degrees of careful handling in order to maintain the integrity of the assembly.

**7.3.1 Conformal Coatings** Special consideration should be taken when using conformal coatings with BTC type packages. Allowing coating material to wick underneath the package may cause early solder joint failures due to the “Z” axis expansion of the coating material during thermal excursions.

**7.3.2 Use of Underfills and Adhesives** Underfill and adhesive (edge and/or corner bonding) may extend the solder joint life during vibration and shock. The use of solder mask in the PCB design may make the standoff distance between the PCB and BTC too small for most

underfill materials to spread effectively under the part. Test vehicle evaluation is recommended to determine if these materials are appropriate or required for the application and mission life of the electronics assembly.

**7.3.3 Depaneling of Boards and Modules** During a mechanical depaneling process stress may be placed on solder joints in the area being punched or routed. Suppliers of mechanical routing equipment should recommend specifications for keep out areas. Laser routing is an attractive for singulation as it is noncontact; however, laser systems are more costly.

**7.4 Inspection Techniques** Inspection of a BTC on a PCB is typically accomplished by using transmission type X-ray equipment. In most cases, 100 percent inspection is not performed. Typically X-ray inspection is used to establish process parameters, and then to monitor the production equipment and process. There are many different types of X-ray inspection equipment available and functionality varies. X-ray inspection system features range from manual to automated X-ray inspection (AXI).

Different systems also provide single or multiple dimensional inspection capabilities. Depending on size and weight, a BTC will self-align to the land pad using surface tension during the solder reflow process. As a result, it is unlikely that a BTC will be marginally misaligned. If misalignment does occur it is likely to be by an entire pad. This effect makes it possible to do a gross visual alignment check after reflow. Visual checks can be aided by the use of PCB fiducial marks which also aid manual placement of units during any rework.

**7.4.1 X-Ray Usage** X-ray inspection is generally used when there is a high proportion of hidden solder joints that are not visually accessible, and when there are a significant number of un-testable solder joints. Examples of un-testable solder joints are redundant connections, and back-to-back BTCs where the fanout vias are inaccessible and space does not allow for additional test points. X-ray methods can complement the test process chosen, and can provide faster feedback to the manufacturing line; however, solder bonding is not necessarily observable through X-ray and other testing might be necessary to prove metallurgical bonding.

Depending on the capability of the X-ray system being used, X-ray can detect solder related defects such as bridging, open solder joints, insufficient solder, and excessive solder volume but, in general, X-ray is not considered to be a reliable inspection technique to confirm good solder joints, especially those marginal solder joints that may lead to intermittent contact. Other defect types such as missing solder, misregistration, and package popcorning can also be identified. In addition to defect detection, X-ray can be used to provide trend analysis for solder volume and solder joint shape.

**7.4.1.1 X-Ray Image Acquisition** Real Time X-ray inspection systems utilize an X-ray source and a detector system which converts the invisible X-ray image into a video display signal. These systems provide immediate imaging results of samples. The images produced from these systems should not be distorted or include false artifacts induced by the X-ray system itself. Figure 7-14, 7-15 and 7-16 illustrates a comparable level of image quality that should be expected from a manual X-ray inspection system. Real time systems are available in a broad range of sizes from small desktop systems to large console floor models. They are also available with a broad range of X-ray tube voltages and tube currents or powers.

There is not a specific X-ray tube voltage or current/power needed to inspect BTCs. The settings required will, in part, depend on the sensitivity of the particular X-ray system employed, the structure and characteristics of the BTC

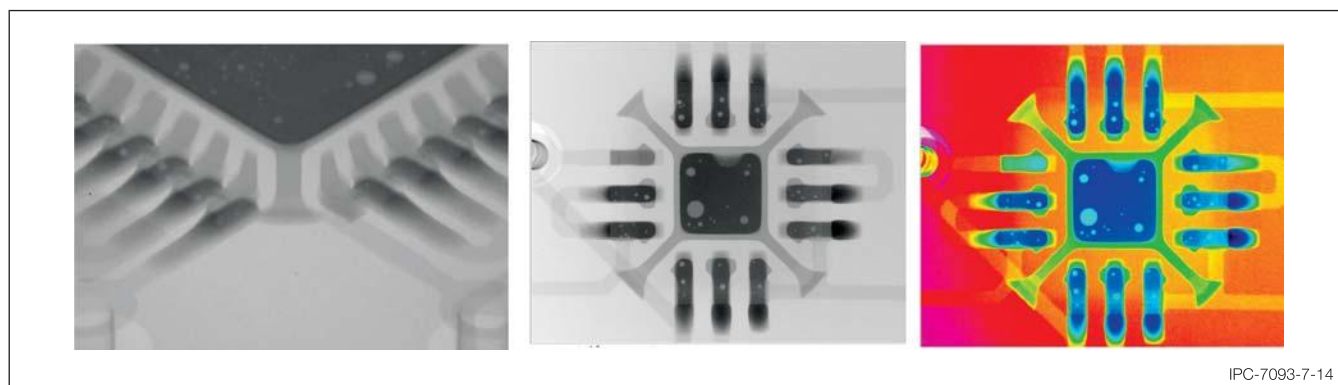
under inspection, and the thickness and features of the board upon which it sits. BTC's with copper heat sinks, for example, will typically require higher tube voltage and tube current/power settings. On the other hand, BTC's with aluminum heat sinks will typically require less since aluminum has a lower atomic number than copper and is therefore more transparent to X-rays.

**7.4.2 Scanning Acoustic Microscopy** Scanning acoustic microscopy (SAM), also called scanning acoustic tomography (SAT), is a nondestructive failure analysis tool. It uses sound waves to scan the internal layers of an assembly. This technique can also locate delamination or voids inside a BTC package as well as locating similar anomalies in underfill after the BTC has been attached to the substrate.

The SAM illustration in Figure 7-17 shows locating a flip-chip assembly with the sample being inspected being immersed in liquid during the SAM analysis. Voids or areas of delamination that are open to liquid ingress, however, cannot be detected with this method.

The resolution of delamination or void detection depends on the acoustic frequency used for analysis. Resolution increases with increasing frequency, however there is less penetration at the higher frequencies. A 230 MHz transducer can bring detection resolution down to around a 25 mm gap. A single point observation is called a SAM, a line scan is called a b-SAM, and an area scan is called a c-SAM.

**7.4.3 BTC Standoff Measurement** BTC standoff measurements are important for process control and should be checked during process development and subsequent process validation. Feeler gauges provide a nondestructive method of determining the approximate finished standoff of the BTC after reflow. Feeler gauges can be used at each corner after reflow and the combined results can be used to determine an average standoff measurement. This method is not as accurate as cross-sectioning, but it is much less expensive and nondestructive provided that the operator does not attempt to force a feeler gauge under the device. Doing so could result in breaking solder joints.



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**Figure 7-14 X-Ray Images Using Various Techniques to Detect Missing Solder**

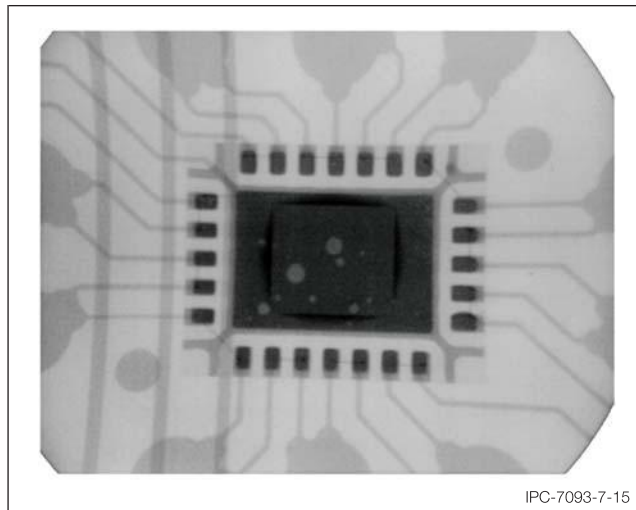


**Figure 7-15 Typical X-Ray After Process**

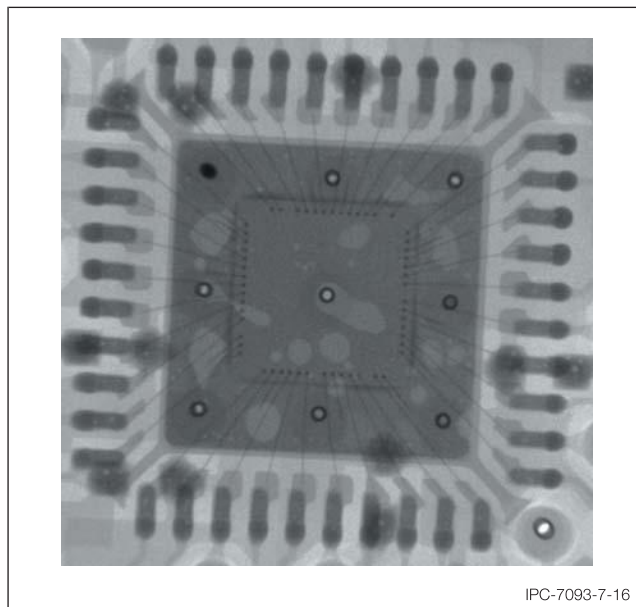


**Figure 7-16 Wire-bond X-Ray to Leadframe Illustration**

The feeler gauge measurement method does require adequate space around the BTC for unrestricted access. The standoff height of a BTC can give some indication that the solder joint reflowed completely and uniformly. Since each package has its own stand-off characteristics, users should develop a part assembly profile in order to make the use of feeler gauges applicable.

**7.4.4 Optical Inspection** Endoscopy is an optical inspection method that permits visual inspection of tiny objects in a small, confined area. This technology has been adapted and applied to BTC solder joint inspection. Adding localized fiducial locations also can help in identifying accurate position for placing BTC devices.

BTC solder joints can be inspected and analyzed for a variety of critical factors such as:

- Overall Solder Joint Quality – evidence of proper wetting
- Solder Joint Shape – evidence of proper reflow
- Solder Joint Surface Texture – smooth vs. irregular
- Overall Solder Joint Appearance – flux residue, etc.
- Solder Joint Defects – solder shorts, opens, cold solder

Endoscope inspection technology is best suited for inspecting only the exterior row BTC solder joints. A limitation of this technology is the inability to view interior rows with the same level of quality and clarity. It is sometimes possible to focus on interior solder joints but not at the same level of detail as the exterior rows.

**7.4.5 Destructive Analysis Methods** If the nondestructive measures used to identify a malfunction do not succeed in eliciting the cause of failure, then destructive analysis techniques may be used. Such techniques will render the analyzed assembly unusable. Once the cause of the failure has been identified the information can be used to implement corrective actions to eliminate the problem.

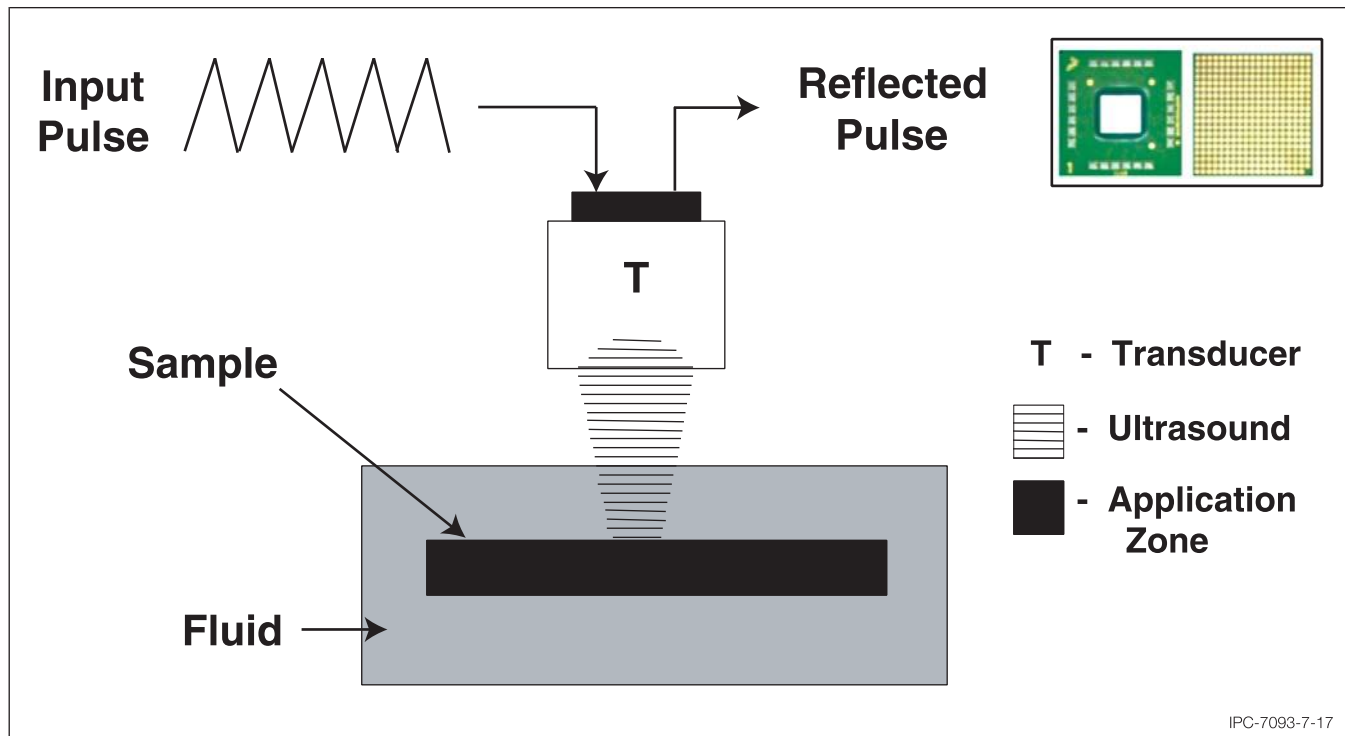
**7.4.5.1 Cross-Sectioning** If nondestructive methods fail to identify the cause of an anomaly, it may be necessary to use destructive methods to isolate the problem area. One method traditionally employed for failure analysis is cross-sectioning, enabling an operator to analyze a specific section of the component, substrate and solder joint.

If more than one area is suspect then it needs to be determined whether those areas can be accessed sequentially on the same component. If not, then the areas will need to be prioritized according to the possibility of finding the problem or more than one component will need to be analyzed.

Next, if the problem area is a part of a larger assembly, it may need to be isolated into a small more manageable portion by cutting it out of the larger assembly. Care must be taken to ensure that the area of analysis is not tampered with or destroyed during the cutting and polishing process.

For proper sectioning, the sample should be molded in resin to alleviate chipping or destruction of the sample during cross-sectioning. If fine polishing of the area of interest is going to be required, then the sample should be sectioned a reasonable distance away from the interface of interest leaving sufficient distance for fine polishing of the interface.

In some cases, the entire component may need to be ground through and looked at for the integrity of various interfaces. A common failure analyzed through cross-sectioning is an open occurring in an assembly. Such opens may occur at the solder interface. See Appendix A for detailed instructions for performing cross-sectioning.



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**Figure 7-17 Scanning Acoustic Microscopy**

**7.4.5.2 Dye Penetrant** Dye penetrant methods can be used during process set-up and in failure analysis to detect solder joint cracking and wetting problems, and package delamination. In this process, the sample is immersed in a low viscosity liquid dye which penetrates most cracks, delaminated areas, or open voids. The sample component can then be peeled away and examined for the presence of dye in the solder joints or at material interfaces.

If a fluorescent dye is used, the sample is inspected under UV light. The dye enhances the visibility of flaws that might otherwise be difficult to detect. The presence of dye on a solder land indicates poor wetting to the land, and can be used to estimate the portion of the land that was not wetted; however, very thin cracks may be so small that liquids cannot completely enter because the surface tension of the liquid will not allow it. See Appendix B for detailed instructions for performing dye penetrant testing.

**7.5 Testing and Product Verification** Testing methodology will vary depending on complexity of the assembly and product application. During the initial stages of prototype and preproduction development a great deal of data is necessary in order to fine-tune the process for a particular assembly. A good design will provide feedback from some of the test sequences that can be used to institute process improvement procedures.

**7.5.1 Electrical Testing** Electrical testing may require the adoption of boundary scan to verify solder joint integrity if net access for mechanical probing is restricted or not

practical. Similar to testing BGAs, BTCs can be tested with a probe if a conductor and via is added as a test point. Electrical testing is used to evaluate the functionality of the electronic assembly. There are two commonly used electrical test approaches: in-circuit test (ICT) and functional test (FT).

ICT utilizes a dedicated bed-of-nails fixture to probe the completed assembly. This test method is used to detect faults caused by the manufacturing process and also to isolate the majority of nonfunctional components. The faults found by ICT include solder bridging, solder opens, component mis-orientation, wrong component, component not functional and conductor short.

Another approach is to place a low cost in-circuit tester near the end of the assembly line and use it as a manufacturing defect analyzer (MDA). Boards are tested immediately after the components are placed and soldered. Problems are quickly relayed back to manufacturing so corrective action can take place while the product is being assembled.

ICT can be supplemented by a complete functional test at the end of assembly. This test for product functionality can, depending on type of product and the acceptability requirements, be as simple as a 'go/no-go' test or as complex as a complete exercising of all circuit functionality. FT is used to detect device faults on the assembly at speed. With the higher temperatures on lead-free solder pastes, there may be an increase in oxidized test lands or test vias. Typically, with tin/lead alloys you may print and reflow solder pastes to provide a soldered test point for the ICT probes. Lead-free

solder pastes do not spread as well and may cause issues with ICT. It is recommended to run a quick experiment during the development stage of the process to understand the impact of lead-free solder pastes on this process.

**7.5.2 Test Coverage** Given the current complexity in electronic assemblies, the level of ‘coverage’ of test has become an industry issue. The more complex a board or assembly, the more difficult it is to fully test. Indeed, it may be difficult to test even a reasonable portion of the assembly in a reasonable, i.e., cost effective, period of time.

While test of an assembly may be aided by incorporating test into the silicon devices, this strategy is not applicable to bare boards. Thus the challenge of test is to provide test coverage at a high level of confidence within a reasonable period of time.

An effective process monitoring system consists of overlapping tools that create a large bandwidth of coverage. Multiple tools and methods are required since there is not one single tool or method that provides the desired coverage. Optical inspection, X-ray, SAM, ICT and FT are examples of overlapping coverage. These verification methods should be used to monitor products and process; they should not be used solely to screen and separate good and bad product.

**7.5.3 Burn-In Testing** Burn-in is an operational and environmental test of the complete assembly at the upper limits of the application. This test typically finds more component related problems than solder joint defects. The use of burn-in testing is still in use for component evaluation. Burn-in on electronic assembly is decreasing in favor of some form of accelerated test exposure to screen out marginal results.

**7.5.4 Product Screening Tests** Environmental stress screening (ESS) is used to screen ongoing production for poor product quality and latent defects. The purpose of ESS is to accelerate the latent defects to actual failures, thus eliminating these latent defects from causing failures in the field. Care must be taken that the ESS procedures are not sufficiently severe to damage good product and produce new latent defects. Solder fatigue life on BTCs **shall** be evaluated on the thermal cycling of these ESS tests, other tests, and the operating life thermal environments.

**7.6 Assembly Process Control Criteria for Plastic BTCs** BTC solder joints have a tendency to voiding from the release of volatiles in the solder paste during the solder reflow process. The degree of voids permitted in the BTC assembly attachment process and the impact on reliability is of interest to members of the electronics industry. The detailed requirements for end product acceptance **shall** be in

accordance with J-STD-001; workmanship requirements **shall** follow the requirements of IPC-A-610.

This section establishes the practicable process development and maintenance criteria as well as attempting to address the issues related to an acceptable assembly process.

**7.6.1 Voids in BTC Solder Joints** Voiding should be minimized by solder process development and recurring process controls. The thermal pad joint of BTCs can have substantial voiding mainly due to the relatively large area of the joint. Most vendors recommend a minimum of 50% coverage of the solderable area of the thermal pad; however, thermal calculations should determine the actual required minimum coverage area to allow for proper heat transfer (see Figure 7-18). Solderable surface area does not include open, filled or solder mask encroached vias unless they are overplated or filled with solderable material.

If the various process parameters such as reflow profile and paste printing guidelines discussed in this document are followed, voids can be greatly minimized. As has been stated, a good stencil design tries to achieve 50 to 60% paste coverage of the thermal pad. Proper stencil aperture design with respect to any vias located in the thermal pad can also minimize voids. Based on agreement between user and supplier, Table 7-5 can be used as a process guideline for void occurrence in different applications. The resulting thermal pad contact percentage is based on the goal of the stencil design intending to have 50% coverage of the thermal pad. Table 7-5 shows the maximum potential voiding expected for the indicated stencil design and via conditions.

The results shown in Table 7-5 are consistent with those shown in Figure 7-18 through Figure 7-21. The examples and X-ray images indicate that the most desirable pattern is

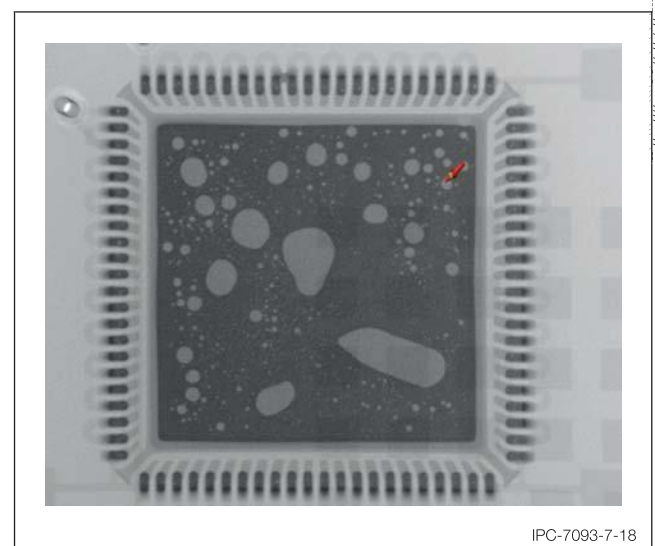


**Figure 7-18 Typical Thermal Plane Voiding**

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**Table 7-5 Guidelines for Void Criteria in Thermal/Ground Planes of BTCs**

| Design Application                   | No Vias in Plane      | Open Vias in Plane     | Capped Via in Plane    |
|--------------------------------------|-----------------------|------------------------|------------------------|
| Stencil Design Solid                 | 50% Potential Voiding | 70 % Potential Voiding | 35 % Potential Voiding |
| Stencil Design Segmented             | 35% Potential Voiding | 45% Potential Voiding  | 25% Potential Voiding  |
| Stencil Design Dot Pattern           | 15% Potential Voiding | 35% Potential Voiding  | 15% Potential Voiding  |
| Assembly Contact Solid Stencil       | 25% of Pad Level A    | 15% of Pad Level A     | 32.5% of Pad Level A   |
| Assembly Contact Segmented Stencil   | 32.5% of Pad Level B  | 22.5% of Pad Level A   | 37.5% of Pad Level B   |
| Assembly Contact Dot Pattern Stencil | 42.5% of Pad Level C  | 32.5% of Pad Level B   | 43.5% of Pad Level C   |

**Note:** Levels A, B, and C reflect the design producibility. Level A = General; Level B = Moderate; Level C = High

one that avoids solder paste over via location and using the dot pattern appears to provide greater attachment potential through less voiding.

It is also important to understand the relationship between paste applied on large thermal pads and any thermal vias in those pads. Figure 7–19 shows solder paste printed over plugged thermal vias using segments on the left and dots on the right. The corresponding X-ray images in Figure 7–20 showed far less voiding for solder paste dots compared to solder paste segments.

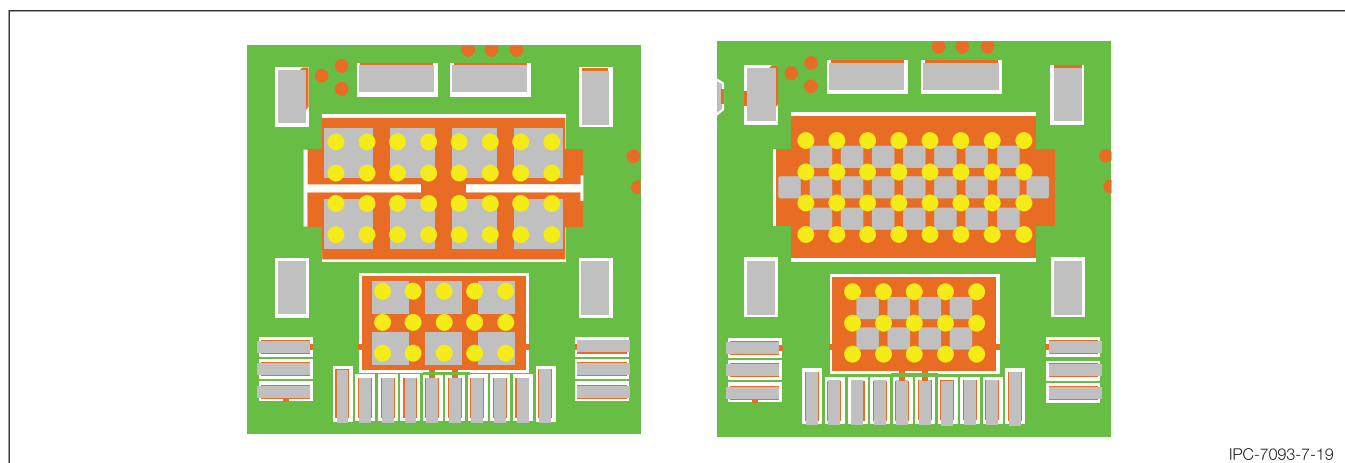
Figure 7–19 shows relatively large solder voids when using the solder paste segment approach compared to using solder paste dots. Another set of examples are provided in Figure 7–21 and Figure 7–22.

The appearance of a void after reflow assembly is an indicator that the reflow process has taken place. However, a change in void size or frequency of voids may be an indication that the manufacturing parameters need to be adjusted. Two reported causes of voids are trapped flux that has not had enough time to be released from the solder paste, and contaminants on improperly cleaned circuit boards. Voids appear in an X-ray image as a lighter area inside the solder joint.

Some X-ray systems can distort the size of voids due to parallax issues. It is possible to accurately measure the true volume of a void but the procedure can be involved and requires a known reference for radiometric calibration of the X-ray film or detector. In most cases the effort is better spent on identifying and eliminating the cause of the voids. BTC solder joints are prone to more voiding than other solder joints due to the nature of the thermal pad joint itself. BTC solder joints are formed mainly between two parallel surfaces and depending on the ability of volatiles or other trapped gasses to escape can result in voiding.

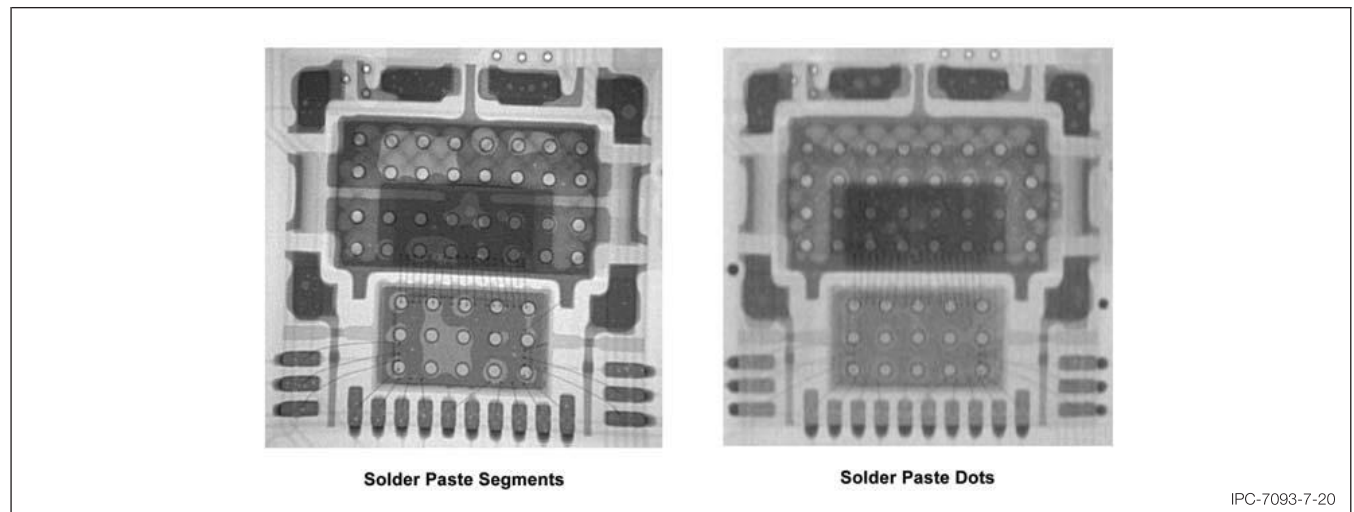
All of these options have pros and cons when mounting BTC packages on the board. While via tenting from top side may result in smaller voids, the presence of solder mask on the top side of the board may hinder proper paste printing. On the other hand, both via tenting from bottom or via plugging from bottom may result in larger voids due to out-gassing. Finally, open vias allow the solder to wick inside the vias and reduce the size of the voids. However, it also results in lower standoff of the package, which is controlled by the solder underneath the exposed pad.

**7.6.2 Solder Bridging** Solder bridging is unacceptable. Electrical testing, optical inspection (endoscope) or X-ray



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**Figure 7-19 Solder Paste Segments vs. Solder Paste Dots Printed over Plugged Thermal Vias**



**Figures 7-20 X-Ray Images Showing Solder Segment and Solder Dot Voiding Results**

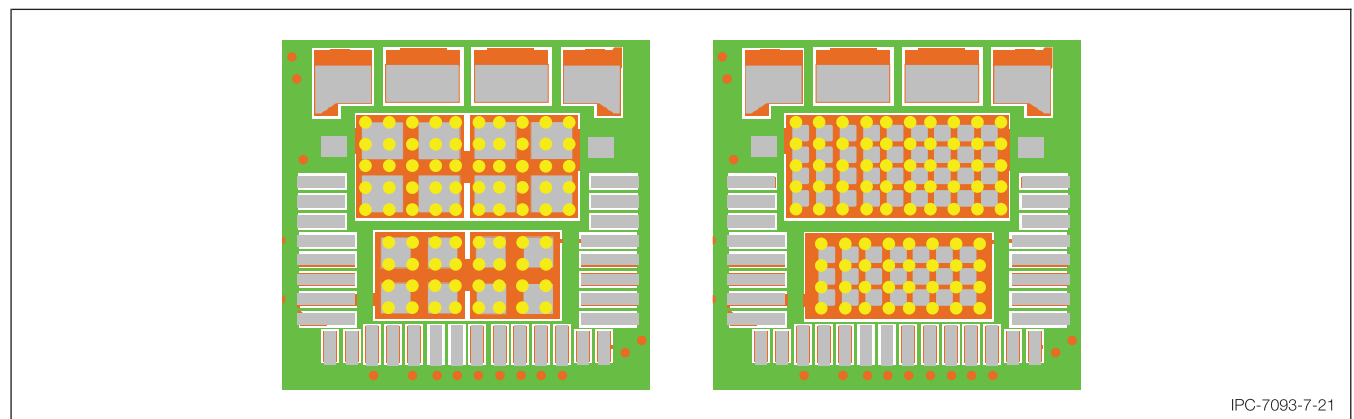


**Figure 7-21 Solder Paste Printing Strategy: Segments (left) vs. Solder Dots (right)**

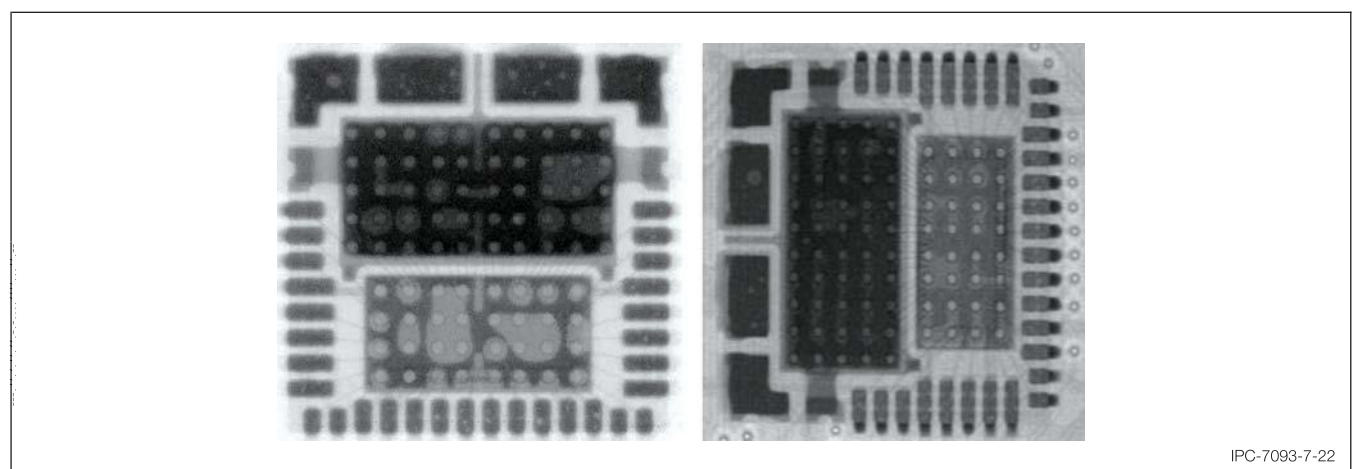


**Figure 7-22 Solder Segments vs. Solder Dots – Void Potential**

inspection is necessary to detect solder bridging. Poor solder paste printing, inaccurate placement, manual ‘tweaking’ after placement and solder splattering during reflow are typical causes of solder bridging.

**7.6.3 Opens** Solder opens are also unacceptable. A combination of electrical testing, optical inspection (endoscope)

or X-ray inspection is usually necessary to detect solder opens. Poor solder paste printing, inaccurate placement and manual ‘tweaking’ after placement, are typical assembly related causes of solder opens. Coplanarity and substrate solderability problems can also cause opens. Excessive mechanical stress can also cause solder joints to crack and create opens.

**7.6.4 Cold Solder** The reflow profile should reach temperatures high enough to ensure that the solder melts completely and proper wetting of the land surface occurs. A cold solder joint can reduce mechanical integrity and can cause the component to fail electrically or function intermittently. Optical inspection after cross-sectioning is the best way to inspect for cold solder joints.

**7.6.5 Defect Correlation/Process Improvement** The manufacturing process produces solder joints that are either acceptable or unacceptable. This can be determined through inspection using methods and tools discussed previously. In many cases a visual inspection of a BTC is the first clue to any problems. An operator can look at the edge of the BTC on all four sides.

To directly observe the solder connections under a BTC, X-ray or optical inspection (endoscope) is necessary. These methods can be used to inspect for obvious defects such as bridges and missing solder joints.

Quantitative measurement of the solder bond X-ray image can be performed using image analysis software. Such software is useful but not necessarily required for the inspection of BTCs. The advantage of the software is in its ability to identify and display subtle variations in the size and shape of the solder bond image which is not easily observed by an operator. These subtle variations are a signature of the process used to manufacture the part and can be used to monitor the process and to correct for deficiencies. A number of signatures can be correlated with known process deficiencies.

**7.6.6 Effect of Insufficient and/or Uneven Heating** A common process problem is insufficient or uneven heating of the BTC. This problem occurs more often during rework but can also be seen in production when working with multilayer boards with many ground or power planes. The problem can also happen on double-sided boards when a shielded component is on the backside near the location of the BTC. The problem occurs when a thermal conductor removes the heat from the BTC preventing thorough wetting of the solder. The X-ray image of this problem is characterized by a variation in the size of the solder joint at different locations under the package.

Insufficient heating is generally characterized in an X-ray image by small partially reflowed solder joints in the center or to one side of the package. Insufficient heating may also be characterized by a jaggedness around the perimeter of these solder joints; indicating that the solder partially reflowed but not long enough to completely wet to the land. Misalignment of the BTC with respect to the land is also an indicator of inadequate heating. The X-ray image of misalignment is characterized by elongated solder joints which may or may not have a consistent orientation.

**7.6.7 BTC Component Solderability Testing** Solderability evaluations using standard 'Dip and Look' techniques can result in false negative test results for some BTC devices. BTC packages which have non-symmetrical pad patterns and/or configurations can result in unintended flux interactions and a lack of molten solder contact. See Figure 7-23 and 7-24. It is recommended that Test S, Surface Mount Process Simulation Test as defined in J-STD-002, be used for the testing of BTC packages.

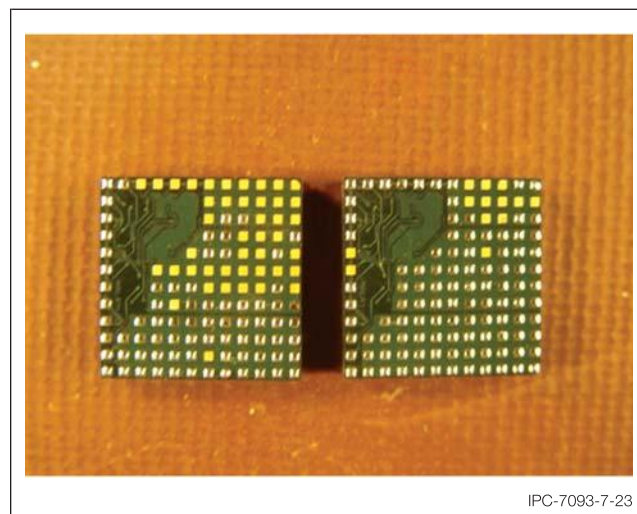


Figure 7-23 Dip and Look Test

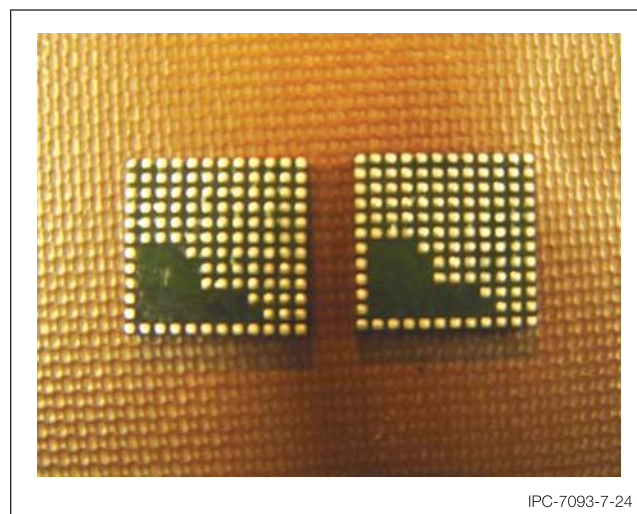


Figure 7-24 Process Simulation Test

**7.6.8 Solder Ball Defects** Solder balls, which form for a variety of reasons during reflow, are a reliability concern, especially when fine pitch devices are involved.

## 7.7 Repair Processes

**7.7.1 Rework/Repair Philosophy** In general, the rework station for BTCs are typical of systems currently used for rework of BGAs. The system should have a split light system, an XY table for alignment and a hot air reflow system with top and bottom heater for component removal.

If the BTC is being removed from tightly packed boards such as cell phones, a laser rework system may have an advantage since they will not heat the neighboring components as would be the case when using hot air systems.

The standard industry practice for rework consists of various steps including:

- Printed board assembly – bake 125°C for 24 hours
- Printed board assembly – preheated to 125°C
- Reflow of component solder
- Removal of component <via machine vacuum, manual plunger or tweezers>
- Cleaning and prep of PCB lands
  - Screening or dispensing of solder paste onto PCB
  - “Bumping” of solder paste onto device
- Placement and reflow of new component
- Inspection of solder joints

To remove the faulty component from the board, heat from hot air or lasers should be applied from the top and bottom heaters. An air nozzle with the correct size should be used to conduct the heat to the BTC component such that the vacuum pick up tool can properly remove the component. The laser does not require different size nozzles for removal.

Once the BTC component is removed, the site is cleaned and dressed to prepare for the new component placement. A de-soldering station can be used for solder dressing.

A mini-stencil with the same stencil thickness, aperture opening and pattern as the normal stencil is placed on the component site. A mini-metal squeegee blade deposits solder paste in the specific area.

The printed pad should be inspected to ensure even and sufficient solder paste before component placement. Unlike in repair of BGAs, the correct amount of paste is critical for successful rework of BTC.

In situations where neighboring parts are in close proximity with the BTC components and the mini-stencil method is not an option, apply solder paste carefully on each land using a syringe. The volume of solder paste will be difficult to control unless an automated dispenser is used as in the case with higher end dispensing systems available in laser rework systems.

A vacuum nozzle is used to pick the new package up. The split light system displays images of both the BTC leads and the footprint on the PCB. The two superimposed images are aligned manually (or automatically in higher end systems) by adjusting the XY table. Once the PCB and the package are aligned, the package is placed down on the PCB. The replaced component is then soldered to the PCB.

## 7.7.2 Removal of BTC

**7.7.2.1 PC Board Bake** It is recommended to bake the PCB for approximately 24 hours at 125°C prior to rework in order to drive off residual moisture that could cause other component failures during the rework reflow process. Proper handling of the PCB during the bake cycle should also be taken into account.

**7.7.2.2 PC Board Preheat** Once the PCB has finished the baking process, the PCB under rework is then placed in the rework holder and preheated to a temperature of 125°C. Localized heating of the area under rework is recommended (use 4°C/second maximum ramp rate).

Specialized vacuum collets come in contact with the rework component. These collets incorporate a hot gas shroud that heats up the part to a temperature required for reflowing the solder interconnects. Once the solder reflows, the vacuum lifts the unit from the PCB. The nozzle size and hot gas flow should be optimized to keep the heat flow localized to the component being removed, while uniformly heating the component.

**7.7.3 BTC Assembly Defect Repair** In the event of defects occurring after component attachment, the board assembly will require rework to remove and replace the device. Since most of the soldered joint is inaccessible, correction of the defect will generally require the complete removal and remounting or replacement of the component. Usual applications for BTC devices involve mounting on small, thin, densely populated PCBs. These factors, coupled with the small size of the components themselves, can lead to challenges in reworking defects. Because of product dependent complexities, the following is only a guideline and a starting point for the development of a successful rework process for these packages.

The rework process includes the following steps:

1. Board preparation
2. Component removal
3. PCB land clean up
4. Application of solder paste
5. Component alignment and placement
6. Component attachment
7. Inspection of rework

**7.7.3.1 Component Removal** In order to facilitate the removal of the component from the PCB, the solder joints attaching component to the board should be reflowed. Ideally the reflow profile used for removing the component should be the same as that used for component attachment. Figure 7–25 shows a typical component removal setup.

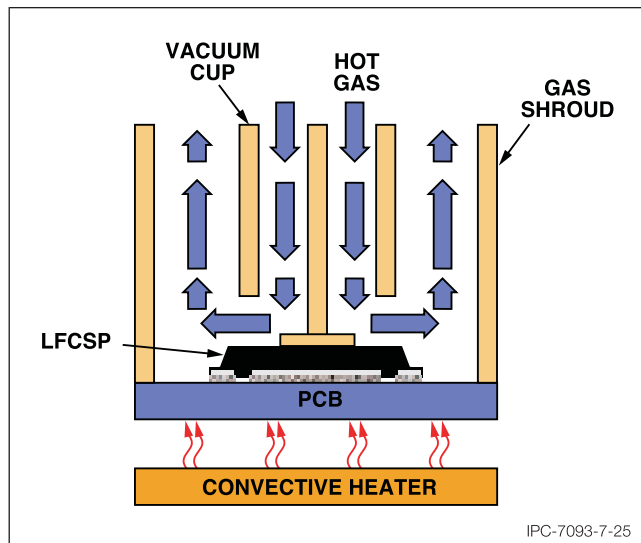


**Figure 7-25 Solder is Heated to Liquidus State and the BTC is Withdrawn Before Solder Re-Solidification**

The time the solder alloy is above liquidus can be reduced as long as the reflow is complete. During reflow, localized heating of the PCB from the bottom side using a heating source is recommended. There are several heating methods for bottom side heating including, but not limited to, hot air and IR. Reflow of the solder joint is achieved by directing heat to the topside of the component; this can be accomplished using a heat gun or IR radiation. During the reflow of the solder joints, a vacuum cup operating within the confines of the gas shroud attaches to the top side of the component. Once the reflow of the solder joints has taken place, either a vacuum-assisted suction cup or some mechanical lifting technique such as tweezers can be employed to lift the component off of the PCB. Use ESD-safe components which are properly grounded, when using manual lifting devices. Given the small size of the components, the vacuum pressure should be kept below 0.5 kg/cm<sup>2</sup>. This will prevent the component being lifted out before all the joints have been reflowed and avoid pad lift.

**Note:** Because of the potential for internal damage during repeated thermal exposure, removed components should not be reused.

#### 7.7.3.2 Laser Enabled Rework for BTC Assemblies

Laser technology has gone through a tremendous change, from traditional YAG and CO<sub>2</sub> lasers to semiconductor technology of diode lasers. Many applications exist where laser soldering will be more cost-effective than traditional methods discussed above. Laser soldering has proved to be cost-effective selective soldering of components when contact or convection reflow is not technically feasible.

Unlike hot air/gas rework systems, laser soldering does not need special fixtures that add to variable cost. Focused laser soldering parameters are controlled in four stages; preheat temperature, laser power (8 to 30 W), wave length (800 to

900 nanometers), and time in milliseconds (generally less than a second for a typical solder joint), with or without the use of built-in preheat. In addition to using traditional preheaters, the laser can be programmed for post-heat operations (just a few milliseconds) to achieve desired solder joint quality.

Because laser soldering time is measured in milliseconds (as opposed to seconds), the intermetallic thickness is less than 1 µm.

**7.7.3.3 PCB Land Preparation for Reattachment** Once the component has been removed, the site should be adequately prepared to receive the replacement device.

Cleaning the site is done in two steps:

1. *Desoldering* – Desoldering is achieved through the use of a ‘desoldering braid’ in conjunction with a blade-type soldering iron typical of that shown in Figure 7-26. The width of the blade should match the maximum width of the component footprint, and the blade temperature should be low enough to avoid any damage to the circuit board.
2. *Cleaning* – The site should be wiped clean using a lint free cloth and solvent. The solvent is usually specific to the type of solder paste used in the original assembly.

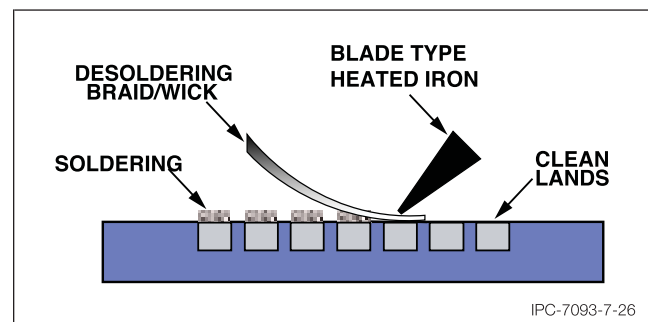


**Figure 7-26 Desoldering of the BTC Mounting Site**

#### 7.7.3.4 Application of Solder Paste

When reworking BTC components there are two main approaches to attaching the device onto the already-populated PCB. One involves the selective solder application on to the PCB while the other involves the selective application of the solder onto the replacement part. The application of the solder paste is accomplished by one of several methods including solder paste printing, solder paste dispensing or hand soldering.

Pad geometries of the BTC component present a challenge in producing an even solder line thickness on reflow. A number of critical features of the print stencil should be

considered. Stencil alignment accuracy and consistent solder volume transfer is critical for uniform reflow solder processing. The stencil thickness, as well as the etched pattern geometry, determines the precise volume of solder paste deposited. Stencils are usually made of brass or stainless steel, with stainless steel being more durable.

As a guide it is recommended to use a 125 micron [0.005 in] stencil thickness for the BTC components.

Laser formed stencil apertures are normally trapezoidal, as shown in Figure 7-27 where dimension A is greater than dimension B. This form factor helps to ensure a uniform release of the solder paste and minimizes solder paste smearing.

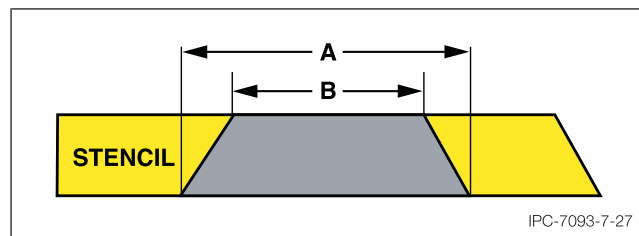


**Figure 7-27 Typical Laser Ablated Stencil Aperture Geometry**

Due to the smaller land geometries and dense component population of the PCBs, accurate and uniform screen-printing of solder paste onto an already populated board is very difficult. It is recommended that the solder paste be applied directly onto the base of the component before placement.

Land geometries along with the existence of a large area ground pad of the BTC presents a challenge for making sure that the stencil is designed properly for solder paste application in order to produce an even solder thickness upon reflow. A number of print stencil features are critical (see 7.2.4):

- For optimum paste release the area and aspect ratios should be greater than 0.66 and 1.5 respectively.
- For 'stay-in-place' stencils on the PCB the aspect ratio is not important as it is not released from the PCB.
- It is recommended that the stencil aperture should be 1:1 to PCB land sizes as both the area and aspect ratio targets can be achieved using this guideline.
- For the larger exposed solder pads (such as the center ground) found on some BTC designs the stencil opening in this area needs to be divided into an array of smaller openings. Dividing the larger exposed pads into the smaller screen openings reduces the risk of solder voiding and allows the solder joints for the smaller terminal lands to be at the same height as the larger ones. It is recommended that "window pane" stencil opening patterns are used for the large exposed thermal pad as shown in Figure 7-28.

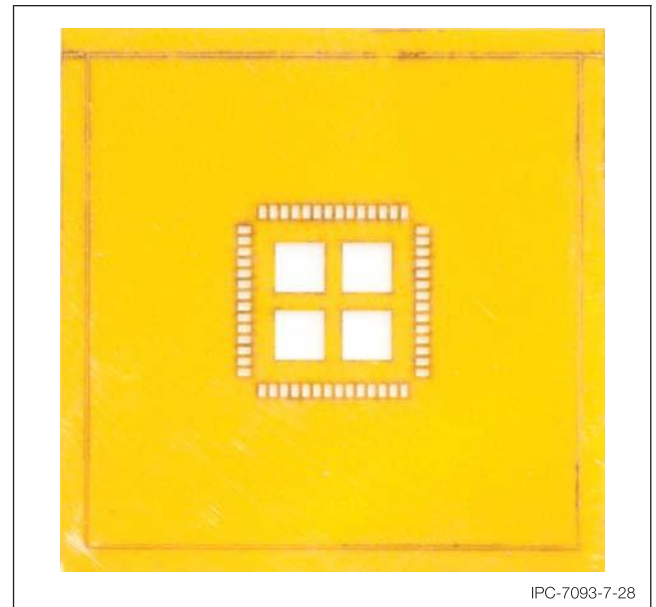


**Figure 7-28 Example of Window Pane Pattern on Stencil**

- The stencil aperture sizes need to be closely controlled in the case of peel and release type of stencils as the geometries are critical
- The recommended stencil thickness should be between 75  $\mu\text{m}$  and 125  $\mu\text{m}$  [0.003 in and 0.005 in]
- Stencils can be made from a variety of materials but are typically made from brass, stainless steel or polyimide. See Figure 7-29.

The process is shown in Figures 7-30 and 7-31 where:

- The component is placed and secured onto a stencil fixture
- Solder paste is then applied using a metal squeegee blade

**Note:** The minimal standoff height of BTC package may not leave enough gap for efficient post reflow solder cleaning,

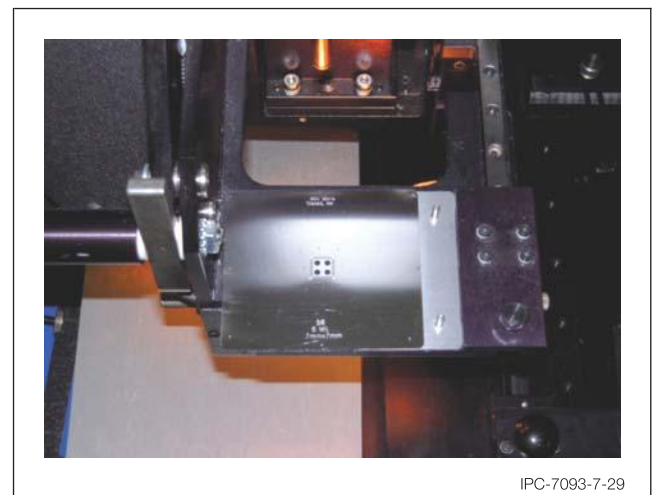
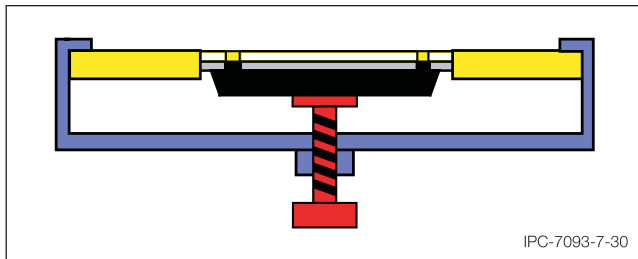
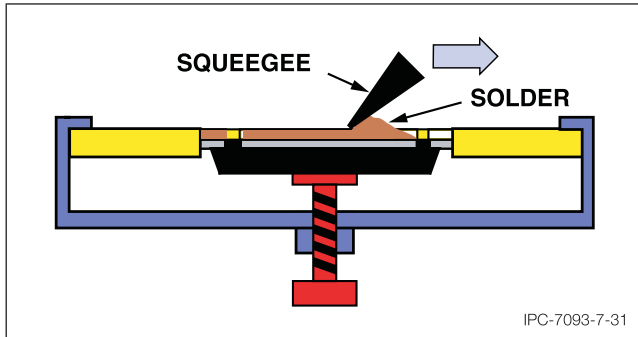


**Figure 7-29 Typical Metal Stencil for Printing onto Component**



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**Figure 7-30 BTC Device is Clamped into Stencil Fixture**



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**Figure 7-31 Solder Paste is Transferred Through Stencil Apertures onto the Undersurface Features of the BTC**

therefore, the manufacturer recommends that the operator use a Type 3, 4, or 5 no clean solder paste (see J-STD-005).

*Application via dispensing:* Solder paste dispensing can be used for dispensing solder paste in a very controlled fashion onto the PCB. Typically a programmable X-Y-Z axis controller such as a robot moves into the correct position where a precise volume of paste is dispensed. Very accurate placement and controllable volumes of paste are the result of this technique.

*Application via hand soldering:* Hands soldering of leadless packages can be achieved in some cases for the peripheral pads. Access to these pads depends on the existing of a

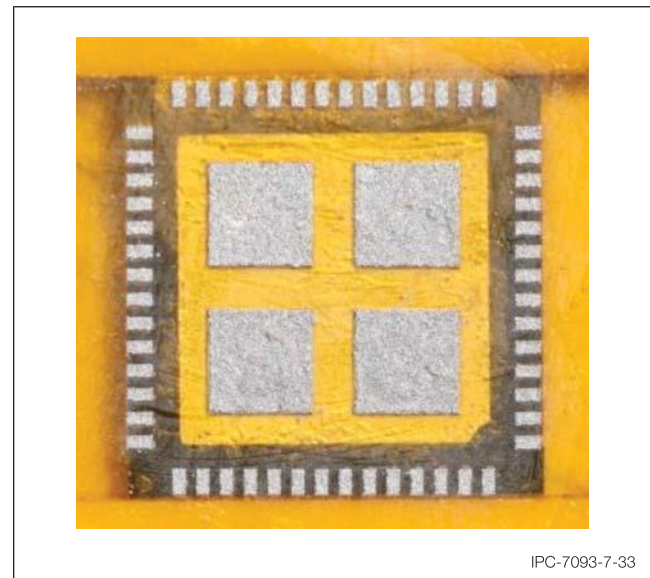


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**Figure 7-32 Typical Dispensing System**

solder surface on the side of the package, access to an exposed pad underneath the device and space on the board. However, hand soldering cannot access unexposed bottom side terminations. In addition the geometries involved require a very high degree of hand soldering precision and excellent tooling else damage to the component and nearby components is likely. For these reasons, hand soldering is not a recommended practice for solder paste application on BTCs.

*Application onto the part-solder “bumping”:* Due to the smaller geometries, dense component population of the PCBs, accurate and uniform screen printing of solder paste using a print and release stencil design is difficult and requires a high degree of operator dexterity and skill. In these cases it is recommended that the solder paste be applied directly on top the base of the component before placement. Either metal stencils, paste dispensing or polyimide “peel and release” stencils can be used. Once the device is “bumped” the component can be precision placed and reflowed similar to other area array devices. See Figure 7-33



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**Figure 7-33 Solder Bumping Method Using a Stencil**

**7.7.3.5 Component Alignment and Placement** The accuracy of component placement of the package is equipment and process method dependent. It is challenging to place the parts in many cases as the package sizes of BTC devices tend to have a small footprint. While BTC do have the ability to self align to an extent due to their small mass, this is counterbalanced by the greater surface tension of lead free solders. Slightly misaligned parts should self-align during reflow as a result of surface tension within the liquid solder. Grossly misaligned parts are likely to result in shorting and bridging.

There are a variety of methods one can use to place the parts including the use of a split beam optical system as part of the rework system or a stay in place alignment stencil.

A split-beam system is used to place either a “bumped” component—a component which has solder applied to its bottom side (see Figure 7-35)—or to place a component in to solder paste which has been printed/dispensed onto the PCB (see Figure 7-34). This type of split-beam optical system is used to align the component to the solder pad array on the PCB as the BTC leads are located on the underside of the package. This imaging system will provide an image of the leads that are superimposed and by adjustment overlaid onto the corresponding footprint of the PCB and therefore align the component with the pad array. This alignment is done at magnification. The placement machine must have the capability of allowing for fine adjustments in X, Y and the rotational axis. Once aligned and placed, the reflow profile used should be optimized to mimic the original assembly profile.

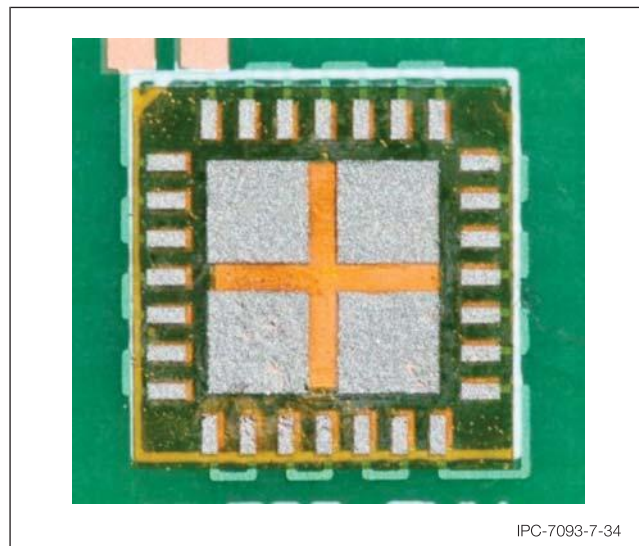


**Figure 7-34 Alignment Stencil on PCB**

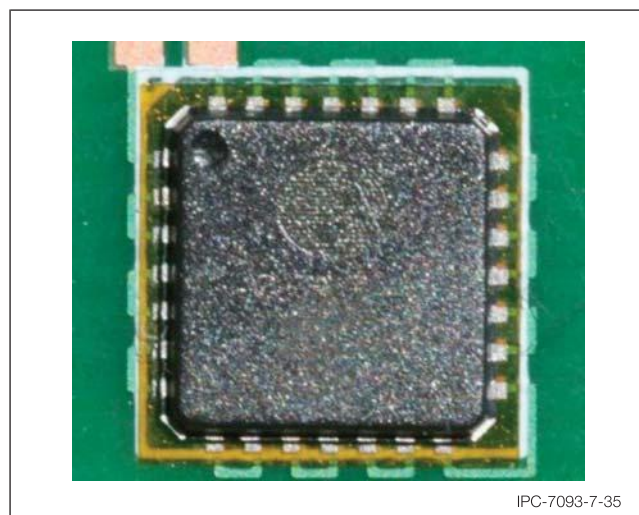


**Figure 7-35 “Bumped” Part Placed and Reflowed**

A second method which can be used for rework involves the use of a stay-in-place stencil which acts as the alignment guide of the part onto the PCB. In this method the stencil is

aligned to land patterns of the device being placed, placed and adhered to the PCB. After solder paste is rolled in to the apertures and the stencil wiped of any remnant solder paste, a bumped part is then align and placed in to those apertures by hand. The part is then reflowed as previously described.

## 8 RELIABILITY

This section provides insight into the method of stress testing in order to validate that a part, board or assembly will work for a specific period of time within an acceptable failure limit. Information is concentrated on the solder joint and the metallurgical bond between the attachment surfaces.

**8.1 Accelerated Reliability Testing** The validation and qualification tests should follow the guidelines given in IPC-SM-785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments and/or IPC-9701, Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments. For some products, the accelerated temperature cycling (ATC) needs to be combined with mechanical shock and/or vibration testing.

Accelerated reliability testing is carried out on design prototypes, typically to failure or until a predetermined reliability goal is achieved. The appropriate reliability goal can be determined with an appropriate acceleration model (see IPC-D-279). Once failure occurs, the resulting failure modes are analyzed as to the underlying failure mechanism(s). If it fails expectations then corrective action is necessary. Either the assembly process needs to be improved or the product needs to be redesigned. In either case retesting may be necessary after the corrective action has been implemented.

Recognizing that a matrix was needed to determine the exact requirements and the testing necessary for performance under various conditions the IPC Product Reliability Committee developed the following table “Product Categories and Use Environments.” Table 8-1 attempts to relate seven product categories by typical application to the thermal, mechanical, atmospheric, and electrical performance requirements that they must meet during typical manufacturing processes, storage, and during operation.

**8.2 Damage Mechanisms and Failure of Solder Attachments** The reliability of an electronic assembly depends on the reliability of the sum of the individual elements of the mechanical thermal and electrical interfaces (or attachments) between these elements. One interface type, the surface mount solder attachment, is unique since the solder joint not only provides the electrical interconnection, but is also the sole mechanical attachment of the electronic components to the printed board. It often provides the critical heat transfer function as well. A solder joint in isolation is neither reliable nor unreliable; it becomes so only in the context of application.

Table 8-1 Accelerated Testing for End Use Environments

| Worst-case use environment                       |                     |                     |                         |                      |                          |                          |                                | Accelerated testing |                     |                                                 |                    |
|--------------------------------------------------|---------------------|---------------------|-------------------------|----------------------|--------------------------|--------------------------|--------------------------------|---------------------|---------------------|-------------------------------------------------|--------------------|
| Use category                                     | T <sub>min</sub> °C | T <sub>max</sub> °C | ΔT <sup>(1)</sup> °C    | t <sub>b</sub> hrs   | Cycles/year              | Typical years of service | Approx. accept. failure risk % | T <sub>min</sub> °C | T <sub>max</sub> °C | ΔT <sup>(2)</sup> °C                            | t <sub>b</sub> min |
| 1) Consumer                                      | 0                   | +60                 | 35                      | 12                   | 365                      | 1–3                      | 1                              | +25                 | +100                | 75                                              | 15                 |
| 2) Computers                                     | +15                 | +60                 | 20                      | 2                    | 1 460                    | 5                        | 0.1                            | +25                 | +100                | 75                                              | 15                 |
| 3) Telecom                                       | -40                 | +85                 | 35                      | 12                   | 365                      | 7–20                     | 0.01                           | 0                   | +100                | 100                                             | 15                 |
| 4) Commercial aircraft                           | -55                 | +95                 | 20                      | 12                   | 365                      | 20                       | 0,001                          | 0                   | +100                | 100                                             | 15                 |
| 5) Industrial & automotive Passenger Compartment | -55                 | +95                 | 20<br>&40<br>&60<br>&80 | 12<br>12<br>12<br>12 | 185<br>100<br>60<br>20   | 10                       | 0.1                            | 0                   | +100                | 100                                             | 15                 |
|                                                  |                     |                     |                         |                      |                          |                          |                                |                     |                     | & COLD <sup>(3)</sup>                           |                    |
| 6) Military Ground & ship                        | -55                 | +95                 | 40<br>&60               | 12<br>12             | 100<br>265               | 10                       | 0.1                            | 0                   | +100                | 100                                             | 15                 |
|                                                  |                     |                     |                         |                      |                          |                          |                                |                     |                     | & COLD <sup>(3)</sup>                           |                    |
| 7) Space<br>Leo<br>Geo                           | -55                 | +95                 | 3<br>to 100             | 1<br>12              | 8 760<br>365             | 5–30                     | 0.001                          | 0                   | +100                | 100                                             | 15                 |
|                                                  |                     |                     |                         |                      |                          |                          |                                |                     |                     | & COLD <sup>(3)</sup>                           |                    |
| 8) Military avionics<br>a<br>b<br>c              | -55                 | +95                 | 40<br>60<br>80<br>&20   | 2<br>2<br>2<br>1     | 365<br>365<br>365<br>365 | 10                       | 0.01                           | 0                   | +100                | 100                                             | 15                 |
|                                                  |                     |                     |                         |                      |                          |                          |                                |                     |                     | & COLD <sup>(3)</sup>                           |                    |
| 9) Automotive under hood                         | -55                 | +125                | 60<br>&100<br>&140      | 1<br>1<br>2          | 1 000<br>300<br>40       | 5                        | 0.1                            | 0                   | +100                | 100                                             | 15                 |
|                                                  |                     |                     |                         |                      |                          |                          |                                |                     |                     | & COLD <sup>(3)</sup> & LARGE ΔT <sup>(4)</sup> |                    |

& = in addition

- (1) ΔT represents the maximum temperature swing but does not include power dissipation effects; for power dissipation calculate ΔT; power dissipation can make pure temperature cycling accelerated testing significantly inaccurate. It should be noted that the cyclic temperature range, ΔT is not the difference between the possible minimum, T<sub>min</sub> and maximum, T<sub>max</sub>, operational temperature extremes; ΔT is typically significantly less.
- (2) All accelerated test cycles **shall** have temperature ramps, 20°C/minute and dwell times at temperature extremes **shall** be 15 minutes measured on the test boards. This will give ~24 test cycles/day.
- (3) The failure/damage mechanism for solder changes at lower temperature; for assemblies seeing significant cold environment operations, additional "COLD" cycling, from perhaps -40 to 0°C, with dwell times long enough for temperature equilibration and for a number of cycles equal to the "COLD" °C operational cycles in actual use is recommended.
- (4) The failure/damage mechanism for solder is different for large cyclic temperature swings traversing the stress-to-strain -20 to +20°C transition region; for assemblies seeing such cycles in operation, additional appropriate "LARGE ΔT" testing with cycles similar in nature and number to actual use is recommended.

The characteristics of these three elements—component, substrate, and solder joint—together with the use conditions, the design life, and the acceptable failure probability determine the reliability of the surface mount solder attachment. The general characteristics of most lead free solders as compared to tin/lead solders, include (1) significantly greater strength, (2) significantly slower creep rates, (3) greater difficulties of proper spread, and (4) significantly higher soldering temperatures.

The consequence of the greater strength and the slower creep rates are higher stresses on the whole solder attach-

ment structure during either temperature changes causes thermal expansion mismatches or PCB/component warping or bending. These higher stresses combine with less strong solder to base material connections due to inadequate wetting or interfacial structural weaknesses to cause brittle interfacial failure.

**8.2.1 Differences in Accelerated Testing of SAC vs. Tin/Lead** SAC solder joints may develop additional failure modes and damage mechanisms during accelerated test, such as temperature cycling, as compared to tin/lead solders. The reasons for this are founded in the facts that SAC

solders are stiffer and have much lower creep rates; both of these conditions generate higher stresses.

**8.2.2 Mixed Alloy Soldering** Since the only solder in the board to package interconnect comes from the solder paste there is no risk of mixed alloy soldering that exists in BGAs. However, since any assembly may have both BGAs and BTCs the possibility of mixed alloy exists, thus alloy selection should consider, mounting land finish, BTC terminal finish and BGA ball solder alloy compatibility.

**8.2.3 Mold Compound Material** Mold component selection has an impact on the package reliability. Selection of mold material should be based on meeting package reliability requirements like moisture sensitivity level and meeting the board level reliability. Board level reliability directly depends on the CTE of the mold compound. Mold compound with lower CTE preformed worse in reliability testing than ones with higher CTE close to the board material. The mold compound modulus also impacts the stiffness of the package. Higher modulus will result in stiffer package and lower fatigue life.

**8.2.4 Die Size** Die size has significant impact on board level reliability. As the die to package ratio decreases the board level reliability increases. With smaller die the board level reliability is better because the die edge, which has a low CTE, is farther away from the peripheral solder joints.

**8.2.5 Full vs. Half Etched Leadframe** Package pads can come with two options: a full pad and a half etched pad. The package pad is the same and both cannot be soldered on the side to create a fillet there is no impact on reliability. Since the package is going through singulation process after plating the exposed side leads are not plated. The copper on the side lead is oxidized and is not solderable during reflow. In some cases when a side lead fillet is created data indicates improvement in reliability.

**8.2.6 Gold/Silver/Palladium Embrittlement** As the joint standoff is very small in BTCs compared to BGAs, noble metal embrittlement could be a reliability issue.

Gold, palladium, as well as silver-embrittlement, work in combination. “Au/Ag-embrittlement” is the weakening of the solder structure by too many weak interfaces with the crystalline AuSn-IMC platelets and the solder. Larger number of such IMC platelets result in higher density of such interfaces and an increased SJ weakness. There is an interfacial loading that comes from a CTE-difference between these IMCs and the surrounding solder volume. There is little practical difference in the effect of either AuSn-IMCs, AgSn-IMCs or any combination of them.

The widely-used 3 to 4% by wt. of noble metal in the solder joint is basically a rule-of-thumb. It applies to the total solder volume and assumes that the IMCs are uniformly

distributed throughout the solder volume. This, however, is rarely the case and problems with ‘embrittlement’ have occurred with less than 3% by wt. of Au.

It is important to put the issues into the correct perspective. Au- and Ag-embrittlement occurs with the thick and somewhat uncontrolled deposits that can result from electroplating of Au and Ag; they do not occur with immersion plating of either Au for ENIG or imAg as a surface treatment.

**8.2.7 Stand-Off Height** Increasing stand-off height is one way to enhance the solder joint reliability of bottom termination components. The design of the center pad (thermal pad), its coverage and the number and size of vias on it has been shown to have the largest impact on standoff height. Increased standoff can be achieved by using a thicker stencil. There are limits to this option due to aperture area and aspect ratio requirements for paste release and floating risk of the center pad. Also, since multiple types of components are mounted on the same board, using a thicker stencil for one or two components is not desirable.

One alternative is to increase the thickness of the plating on the thermal pad on the underside of the package. This has been used by Amkor in the Bump MLF concept as shown in Figure 8–1. A plating thickness of 100 microns increased the stand-off height of the package solder joints by 100 microns. This resulted in a 2X increase in the board reliability of the package as shown in Figure 8–2.

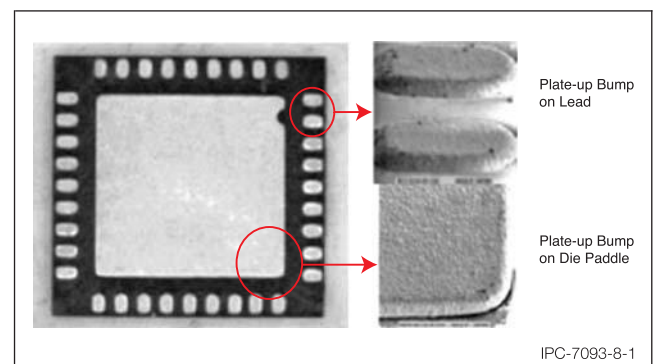


**Figure 8-1 Plate-Up Bumped Option**

**8.3 PCB Design Considerations** Several design characteristics impact the solder joint reliability.

**8.3.1 Land Size** Another influence on reliability is the geometry of the solder joint that is derived from the land metallization on the board. Since BTCs are leadless devices, the solder joint shape relates to the land. A larger land under a BTC package provides better reliability as shown on the Weibull plot in Figure 8–3. Comparing a 7 mm package with 28 terminations and with land sizes of 0.28 mm x 0.6 mm and a 48 terminal package with land size of 0.23 mm x 0.4 mm QFNs, results in a 2X improvement in fatigue life. The larger land results in a larger solder joint and longer path for a complete crack to formation.

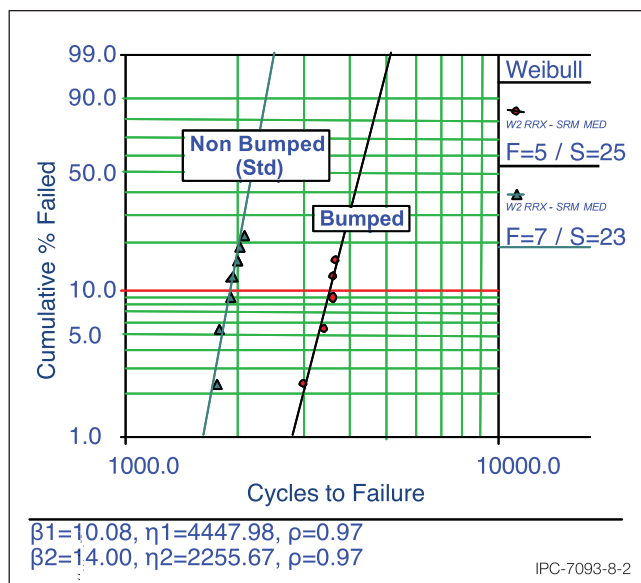


**Figure 8-2 Cracks in QFN Solder Joints after Temperature Shock**

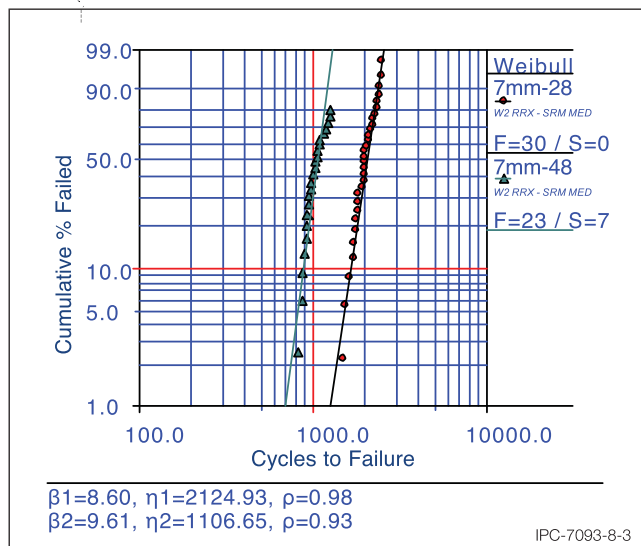


**Figure 8-3 Land Size Impact on Fatigue Life of 7 mm BTC Package**

**8.3.2 Fillet Formation** While BTC suppliers typically do not require fillets to be formed on the toe of their packages, it is generally agreed that these fillets can improve reliability. Solder fillets are formed along the flank or perimeter toe edges of BTCs. Toe fillet formation should not be expected since some BTC suppliers do not protect exposed copper from oxidation after device singulation.

The surface mount process parameter can also influence fillet formation. Some of the variables are PCB land size, solder paste volume, solder paste flux activity, reflow atmosphere and standoff height. When a fillet forms, it increases the joint length which provides a longer path for the crack to form.

**8.3.2.1 Methods for Inspecting BTCs** An approach demonstrated as effective for Inspecting BTCs for unsoldered connections and cold solder joints requires:

1. Solder Paste Inspection (SPI) to determine whether sufficient solder paste is present.
2. Automated Optical Inspection (AOI) to inspect fillets formed on device sides or flanks.

Automated X-ray inspection (AXI) can also cover the inspection for sufficient solder. In that case, an SPI system is not necessary, but AOI is still required. It is important to note that AXI alone does not have the required detection rate to protect against BTC assembly defects like unsoldered connections and cold solder joints.

**8.3.2.2 Inspectable Side Fillets Require BTCs with Wettable Flanks** In the method discussed above, the AOI system is used to establish whether proper BTC assembly was achieved by allowing for the evaluation of solder fillets visible along the sides (flanks) of the device. To achieve externally visible solder fillets after reflow assembly requires wettable flanks at the BTC component edges.

Perimeter side edges of BTC (e.g. QFN components according to JEDEC MO220), typically have exposed copper on the cut or punch separation surfaces or flanks. These exposed copper areas are wettable as long as the copper is not significantly oxidized. After even a few days of storage, however, copper surfaces may oxidize to the point that sufficient solder wetting is no longer possible with typical No-Clean fluxes. For this reason, exposed copper areas of QFN leads that have no special treatment to ensure solderability are not expected to be wettable. See QFN example in Figure 8-4.

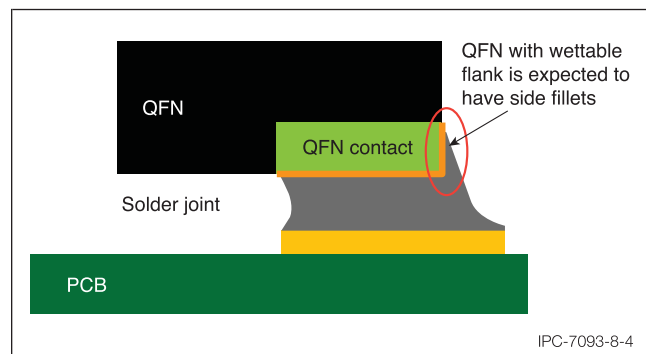


**Figure 8-4 QFN with Wettable Flanks**

**8.3.2.3 Specification for BTC Flank Wettability** JEDEC MO220 defines the basic characteristics of QFN components which generally now should also apply to all BTCs. In addition, the following are also required for specification purposes related to BTC Flank Wettability:

- Each IO lead must have a visible flank at the side of the component (no pullback I/O leads).

- Each flank must be wettable.
- Mold compound is not allowed on any part of the flank of the IO leads.
- Double or Multi rows with similarly blinded IO leads are not inspectable using the method described here.

Flanks **shall** also meet the same solderability requirement as the rest of the device.

**8.3.3 Board Thickness** Thinner printed boards result in better board level reliability. The board material FR4 (~17 ppm/°C) has a larger CTE than the package mold compound (~10 ppm/°C). Thinner PCBs reduce cyclic strains due to the global CTE mismatch between the PCB and the package by flexing and increase solder joint fatigue life. Tests conducted on 10 mm -68 lead and 5 mm -32 lead packages using 0.8 mm and 1.6 mm thick boards show at least 30% improvement in fatigue life for the thinner board. See Figure 8-5.

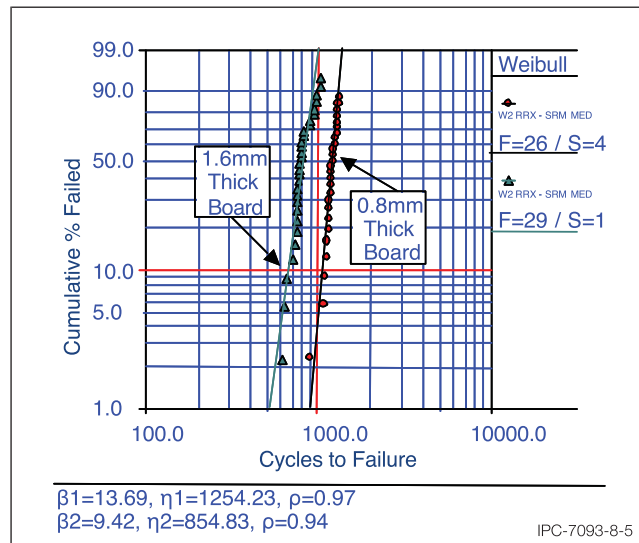


**Figure 8-5 Weibull Plot Showing Thinner Board Results in Higher Fatigue Life**

**8.4 Voids in Thermal Pad** Voids in thermal pads could cause reliability concern. There is no rule of what is the acceptable level of voiding. It is specific to the component and the use condition of the device. As long as the thermal pad is providing sufficient coverage for cooling requirements during maximum operation condition, then it is acceptable. The requirements should derive from thermal modeling.

**8.5 Design for Reliability (DfR) Process** The fatigue behavior of surface mount solder joints has been investigated experimentally in numerous studies. The results of the studies that were carried out in a manner to assure the same damage mechanism as the mechanism operative in typical electronic products have yielded a mathematical solder fatigue model. This model has been expanded and aug-

mented to its current form, presented in IPC-D-279, as additional test results became available.

The model is for uncoated solder attachments. The complexity and vast differences in conformal coatings make it impossible to develop a generic model that considers all the variables. Products with conformal coatings should be evaluated using test vehicles having the same coating and test vehicles without the coating in order to assess the impact of the coating on reliability.

Appropriate DfR-measures to improve reliability can take one of two forms, which are best employed in combination for improved reliability margins. These measures are:

1. CTE-tailoring to reduce the global expansion mismatch;
  2. Increasing attachment compliancy to accommodate the global expansion mismatch;
  3. Eliminate the effect of the global expansion mismatch by mechanically coupling the component and the substrate with an appropriate underfill;
- Further, a DfR procedure aiming at high-reliability should also include:
4. Choosing base materials that have not too large a local CTE-mismatch with solder; or
  5. In case item 4 cannot be done, reduce the continuous wetted length to reduce interfacial stresses.

CTE-tailoring involves choosing the materials or material combinations of the PCB and/or the components to achieve an optimum DCTE. An optimum DCTE for active components dissipating power is ~1–3 ppm/°C (depending on the power dissipated) with the PCB having the larger CTE, and 0 ppm/°C for passive components. Of course, since an assembly has a multitude of components, full CTE-optimization cannot be achieved for all components—it needs to be for the components with the largest threat to reliability. For military applications with the requirement of hermetic—and thus ceramic—components, CTE-tailoring has meant the CTE-constraining of the PCBs with such materials as Kevlar™ and graphite fibers, or copper-Invar-copper and copper-molybdenum-copper planes. Such solutions are too expensive for most commercial applications for which glass-epoxy or glass-polyimide are the materials of choice for the PCBs. Thus, CTE-tailoring has to take the form of avoiding larger size components that are either ceramic (CGAs, MCMs), have plastic with Alloy 42 lead-frames (TSOPs, SOTs), or are plastic with rigid bonded silicon die (PBGAs).

Increasing attachment compliancy for BTC solder attachments means increasing the solder joint height (see Section 8.2.7) or switching to a compliant leaded attachment technology. For compliant leaded attachments increasing lead compliancy can mean changing component suppliers to

those having lead geometries promoting higher lead compliance or switching to fine-pitch technology.

The DfR-process needs to emphasize a physics-of-failure perspective without neglecting the statistical distribution of failures. The process might involve the following steps:

1. Identify Reliability Requirements: expected design life and acceptable cumulative failure probability at the end of this design life.
2. Identify Loading Conditions: use environments (e.g., IPC-SM-785) and thermal gradients due to power dissipation, which may vary and produce large numbers of mini-cycles (Energy Star).
3. Identify/Select Assembly Architecture: part and substrate selections, material properties (e.g., CTE), and attachment geometry.
4. Assess Reliability: determine reliability potential of the designed assembly and compare to the reliability requirements using the approach shown here (see IPC-9701), or some other suitable technique; this process may be iterative.
5. Balance Performance, Cost and Reliability Requirements.

**8.5.1 Wear-Out Mechanisms** The primary failure mechanism that affects the reliability of any solder joint connection is damage accumulation by thermo-mechanical processes such as creep and fatigue. Failures are also caused by electro-migration and thermal-migration of metal which result in opens. Both the thermal-mechanical and electrical failures can be increased by chemical reactions or species which can cause corrosion or enhance migration of metallic ions (shorts). A solder bump wear-out failure in the field has never been observed. This indicates both the robustness of the solder bump and conservativeness of the reliability models that will be subsequently explained.

**8.5.2 Creep-Fatigue Interaction** Solder joints can see large strains during temperature cycling. The strains are generated by the difference in the thermal expansion between the die and the substrate. The cyclic nature of the temperature variation causes the strains experienced by the solder joints to be cyclic and, therefore, the damage in the solder to be a function of the number of thermal cycles. By this definition, solder joints experience thermal creep-fatigue. At uniform strain distributions, fatigue causes damage by the initiation and propagation of micro-cracks. Fracturing of solder joints is increased with high rates of change of strain.

In general, components see thermal cycling which can range from 0.4 T<sub>m</sub> to 0.8 T<sub>m</sub>, where T<sub>m</sub> is the absolute melting temperature of solder. As a rule of thumb, creep is an operative deformation mechanism whenever the tempera-

ture is above half the absolute melting temperature of the material. For example, the melting temperature of 63/37 Sn/Pb solder is 456° Kelvin (183.6°C), half the absolute melting temperature is 228K or -45°C. Hence, creep deformation can occur in solder at a given load even at temperatures as low as -45°C.

The relation between stress experienced by the solder joint and the activation energy is expressed by the general creep equation:

$$\epsilon = A\delta^n \left( \frac{-Q}{kT} \right)$$

Where:

$\epsilon$  = strain rate

A = constant

$\delta$  = stress

n = stress exponent

Q = activation energy

k = Boltzmann constant

T = temperature in degrees kelvin

Creep strain is the result of thermally activated dislocation motion and/or movement of vacancies and atoms when the material is subjected to a given load. Stress relaxation over time observed in solder joints is a direct result of creep processes. Hence the damage accumulated in solder joints during temperature cycling is a result of creep and fatigue processes. Deformation due to creep has been observed in packages which have been subjected to both cyclic loading as well as static loading conditions.

Static loading conditions can arise, for example, from the weight of a heat sink on a package. Depending on how the board is placed, that is, sideways, right side up, or inverted, the solder joints can experience shear, compressive or tensile loads. The constant load in one direction can cause failure by creep processes.

**8.5.2.1 Electro-Migration** In alloy systems, the mobility of each atomic species under an applied electric field is different based on the effective valence and mass of the species. Electro-migration has been observed on chips as well as in solder joints. In a joint, migration of voids to chip or board interface has been observed. Small voids can coalesce causing a mechanical reliability concern or current crowding can occur if the effective conductive cross section is reduced. In both cases observing design rules with regard to current density and dimension can solve the problem.

**8.5.2.2 Corrosion** Solder joint corrosion is usually caused by moisture and ionic contaminants. This can be prevented by proper packaging design and process control. Due to the close proximity of flip chip solder joints, the cleanliness of the solder joints is essential. Residues from

corrosive processing chemicals must be minimized. Depending on use conditions, the flip chip solder joints should be either hermetically sealed, or encapsulated with a material that prevents a continuous moisture path.

**8.5.2.3 Thermo-Migration** Thermo-migration is caused by excessive thermal gradients across solder bumps incorporated on the terminations of BTC packages, especially at higher IC junction temperatures. In the thermo-migration process, atoms diffuse in the direction of, or in opposition to, the thermal gradient. Atoms in the solder bump can diffuse, leading to voiding at the interface of the solder and the UBM (Under Bump Metallurgy). The bump will eventually become electrically open. For a given bump geometry, thermo-migration is a function of thermal gradient, ambient temperature, and alloy composition.

**8.5.3 Solder Thickness Mechanical Reliability** There are numerous factors that can affect the mechanical reliability of BTC attachments. Some of these are:

- Strain
- Temperature Hold Times
- Chip Underfill
- Solder Alloy Composition

**8.5.3.1 Strain** The effect of strain is significant. Its impact on solder bump fatigue is dependent upon several factors. These are determined by the design, application and manufacture of the device. Table 8-2 shows the CTE difference between the chip silicon, alumina, leadframe, printed board; all which can be part of a typical BTC package. Strain is directly proportional to DNP, the distance from the furthest, functional solder bump to the neutral point on the chip.

**Table 8-2 Coefficients of Thermal Expansion for Typical Materials**

| Material         | CTE (ppm/°C) |
|------------------|--------------|
| Silicon          | 2.8          |
| GaAs             | 6.0–7.0      |
| Solder (Sn3Pb97) | 28–29        |
| Chip underfill   | 18–35        |
| Alumina          | 6.0–7.0      |
| FR-4             | 16–19        |
| Copper leadframe | 17–18        |

Strain is inversely proportional to joint height. Table 8-3 furnishes typical heights for varying solder bump diameters.

The resources required to perform these test are often limited. Consequently, methods have evolved that use existing solder bump footprints with known fatigue histories

**Table 8-3 Typical Heights (Joined)**

| Solder Bump Condition | Diameter (μm) | Height (μm) | Range (μm) |
|-----------------------|---------------|-------------|------------|
| Option A              | 150           | 82          | 64–100     |
| Option B              | 125           | 77          | 64–95      |
| Option C              | 100           | 70          | 64–85      |
| Option D              | 150           | >82         | 64–100     |

to predict performance of a solder bump footprint with similar characteristics and packaging but varying DNP.

**8.5.3.2 Effect of Thermal Expansion Mismatch** The neutral point or geometric center of solder bumps remains stationary relative to the substrate during thermal excursions. Determination of the neutral point is critical for calculating DNP. Figure 8-6 illustrates the result of near-interface failure due to thermal excursion of dissimilar materials.



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**Figure 8-6 The Crack Formation is the Result of the CTE Mismatch**

The geometrical shape of the solder joint can greatly affect the local strain. The top and bottom land diameters combined with the volume of solder will determine the height of the joint, a prime influence on reliability. Stress “riser” factors can influence crack initiation and propagation. Ideally a tall, slender solder column will distribute the strain in the solder joint and extend fatigue lifetime. A short, squat solder joint may reduce product life.

**8.5.3.3 Temperature Cycling Frequency** Testing of the life of components under actual use conditions would take as long as the design life of the component. For this reason, packages are tested by accelerating the thermal cycles, i.e., by increasing the temperature range and decreasing the hold times at each end of the cycle. Increasing the temperature range subjects the joints to greater strain, the extent of which is determined by the thermal expansion mismatch

between the different materials. Hence, increasing the temperature range should increase the damage stored in the joints if enough time is allowed for the elastic stresses generated in the solder joints to relax out by converting the elastic strains into plastic deformations by creep. If enough time is not allowed during the hold times, which is typically the case with accelerated tests, then the damage stored is not equal to what it would be if the solder joints were allowed to creep completely. However, it needs to be noted that increasing the temperature range of the test much beyond the temperatures in the field will cause a confounding of multiple damage mechanisms.

The design of the temperature cycle ideally should be such that the stresses generated because of the thermal expansion mismatch have enough time to relax out. However, this is impossible for accelerated testing. Increasing the frequency of cycling can change the failure mechanism and/or suppress the damage stored per cycle in the solder joints. For example, changing the temperature rapidly during thermal shock testing can cause high strain rates as well as high strains due to component warpage to be imposed on the solder, which changes the failure mechanism.

With near-eutectic solders it is necessary to have hold times ranging from 5–10 minutes to achieve a significant, but still incomplete, creep in the joints. The stress relaxation in high lead (90%Pb-10%Sn) solders is slower than that observed in eutectic solders and therefore the hold times at the temperature extremes need to be greater. Thermal cycles represent the number of thermal excursions a flip chip or chip scale product will be exposed to during its lifetime. These excursions consist of power on-off cycles and environmental temperature fluctuations. Temperature cycling tests the inelastic properties of the solder, namely stress-relaxation as a function of temperature and time.

**8.6 Wear-Out Mechanisms Review** Bottom termination interconnects have many potential failures, but there are primarily five degradation or wear-out mechanisms which affect metal interconnects. These are:

- Creep
- Fatigue
- Corrosion
- Electro-migration
- Solid state diffusion

These mechanisms can all lead to degradation and eventual failure of BTC interconnects. They are very dependent on materials used, processing defects, reduced geometries, assembly stresses, and environmental conditions. Creep is caused by stresses or displacements applied to the interconnect in one direction. Properly selected materials can minimize this mechanism for most environments. Corrosion could become a concern in some applications. The BTC

assemblies are used in a number of non-hermetic applications. Reliable operation without corrosion effects will depend on process control in terms of well sealed sites, cleaning of the attach sites, and controlling environmental exposure to avoid contaminants from the application environment. In general, this wear-out mechanism is best controlled through design and process control.

Electro-migration mechanisms are affected by current density. If the designer keeps current density within the constraints of the materials being used, and there is strict process control on defects, electro-migration should not be a problem for most applications.

**8.6.1 Reliability Factors** Creep-fatigue is the primary mechanism for wear-out of BTC assemblies. Creep-fatigue is accumulated damages caused by cyclic thermal stressing by the environment or application and the creeping of the solder under these loads. This cycling behavior causes plastic deformation within the BTC interconnects, which initiates a crack that will eventually grow to open or substantially degrade the interconnect. Most system applications will have temperature changes which will eventually fatigue the interconnects.

It is important that the user of BTC package technologies have a fundamental understanding of the intrinsic material properties and on the design/process driven dimensions for their application. The application environment factors involved in fatigue are temperature, temperature cycle range, and hold times of the temperature cycling. The BTC assembly will affect the reliability in terms of presence of under-fill, the symmetry of interconnect pattern, misalignments and variations of bump geometries and device size.

Under thermal cycling, the failures will first occur at locations farthest from the thermal expansion center point. It is possible to develop detailed models, as most are based on some form of the Coffin-Manson equation for low-cycle fatigue modified to account for the effects of creep. A model for each BTC approach could be established if the geometry, material and application conditions are known. There are various published data on bottom only termination type component reliability. It is extremely important that a user establish this level of knowledge to apply these technologies reliably.

**8.6.2 Benefits of Reinforcement** BTC underfill can substantially enhance fatigue life. When the underfill is applied correctly, it reduces the solder joint strain level by constraining the expansion of the BTC interconnect to be used in a wider range of environments and larger device sizes can be accommodated. Underfill material must be carefully selected, so that it adheres to the assembly surface, but does not adversely stress the BTC interconnect joints. The material must have properties which allow easy application

to avoid process defects, and it also must not contain or trap contaminants which could initiate corrosion related problems.

If an underfill fails, it will most likely lose adhesion to the device and/or substrate. This would lead to failure due to fatigue, creep, or it could also increase chances of corrosion and other failure mechanisms.

**8.6.3 Event Related Failures** The assembled BTC assembly can experience unexpected thermal and/or mechanical transients, which are isolated events related to maintenance or just abnormal system operating conditions. These events could, if they are severe enough, cause catastrophic failure, or they can initiate failure sites which will then fail at a later date. These types of failures are best accommodated by selecting the most robust technology that can be used. There are some additional failure mechanisms which need to be considered when using flip chip technology.

Most BTC finishes are 63/37 tin/lead alloy, tin, gold or SAC, thus some BTC interconnects use alloy combinations that include lead content to improve ductility. This can lead to trace amounts of radioactive elements which emit alpha particles which can cause soft errors in semiconductor devices. It is important to factor the lead and underfill, much lower level particle emissions for proximity to sensitive device features to minimize this effect. Most semiconductor devices have ESD protection placed near the pads and most available devices are not configured for flip chip interconnection. Rerouting layers will be applied to the surface of the device to convert these devices to a BTC array configuration. This will result in some metal runs in close proximity to device structures that are not protected.

**8.7 Design for Reliability Issues and Concerns** The reliability of electronic assemblies requires a definitive design effort that has to be carried out concurrently with the other design functions during the developmental phase of the product. There exists a misconception in the industry, that quality manufacturing is all that is required to assure the reliability of an electronic assembly.

Consistent high quality manufacturing and all that this implies in terms of Design for Manufacturability (DfM), Design for Assembly (DfA), Design for Testability (DfT), etc., is a necessary prerequisite to assure the reliability of the product. Only a Design for Reliability (DfR) can assure that the design, manufactured to good quality, will be reliable in its intended application. Thus, adherence to quality standards is necessary but not sufficient. For example, solder joint quality is generally measured against criteria in both IPC-A-610 'Acceptability of Electronic Assemblies', for overall workmanship and ANSI/J-STD-001 'Requirements for Soldered Electrical and Electronic Assemblies.' However, meeting these criteria does not assure reliable solder connections, only quality solder connections.

To clarify the difference between the two requires an explanation and a definition of reliability. Reliability is defined in IPC-SM-785 'Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments' by:

*Reliability is the ability of a product to function under given conditions and for a specified period of time without exceeding acceptable failure levels.*

In the short term, reliability is threatened by infant mortality failures due to insufficient product quality; these infant mortalities caused by defects can be eliminated prior to shipping by the use of appropriate screening procedures.

Long-term failures are the result of premature wear-out damage caused by inadequate designs of the assembly. It is for this reason that IPC-D-279 'Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies' has been developed.

**8.7.1 Damage Mechanisms and Failure of Solder Attachments** The reliability of electronic assemblies depends on the reliability of their individual elements and the reliability of the mechanical, thermal, and electrical interfaces (or attachments) between these elements. One of these interface types, surface mount solder attachment, is unique since the solder joints not only provide the electrical interconnections, but are also the sole mechanical attachment of the electronic components to the printed board and often serve critical heat transfer functions as well.

A solder joint in isolation is neither reliable nor unreliable; it becomes so only in the context of the electronic components that are connected via the solder joints to the printed board. The characteristics of these three elements – component, substrate, and solder joint together with the use conditions, the design life, and the acceptable failure probability for the electronic assembly determine the reliability of the surface mount solder attachment.

**8.7.2 Solder Joints and Attachment Types** Solder joints are anything but a homogeneous structure. A solder joint consists of a number of quite different materials, many of which are only superficially characterized. A solder joint consists of:

- the base metal at the printed board
- one or more intermetallic compounds (IMC)
- a layer from which the solder constituent forming the PCB-side IMC(s) has been depleted
- the solder grain structure, consisting of at least two phases containing different proportions of the solder constituents as well as any deliberate or inadvertent contaminations
- a layer from which the solder constituent forming the component-side IMC(s) has been depleted

- one or more IMC layers of a solder constituent with the component base metal
- the base metal at the component

**8.7.3 Solder Interface Grain Structure Effects** The grain structure of solder is inherently unstable. The grains will grow in size over time as the grain structure reduces the internal energy of a fine-grained structure. This grain growth process is enhanced by elevated temperatures as well as strain energy input during cyclic loading. The grain growth process is thus an indication of the accumulating fatigue damage. At the grain boundaries contaminants like lead oxides are concentrated; as the grains grow these contaminants are further concentrated at the grain boundaries, weakening these boundaries. After the consumption of ~25% of the fatigue life micro-voids can be found at the grain boundary intersections; these micro-voids grow into micro-cracks after ~40% of the fatigue life; these micro-cracks grow and coalesce into macro-cracks leading to total fracture as is schematically shown in Figure 8-7.

The different surface mount solder attachment compositions can have significantly different failure modes. Solder joints with essentially uniform load distributions, e.g., QFNs, flip chip, BGA, CGA, show similar behavior. Solder joints with non-uniform load distributions, i.e., those on bottom termination only components, leadless chip carriers, CSPs and all leaded solder joints, show localized damage concentrations with the damage in the form of macro-cracking. The solder joints frequently connect materials of highly disparate properties, causing global thermal expansion mismatches and are made of a material, solder, that itself often has properties significantly different than the bonding structure materials, causing local thermal expansion mismatches. The severity of these thermal expansion mismatches, and thus the severity of the reliability threat, depends on the design parameters of the assembly and the operational use environment.

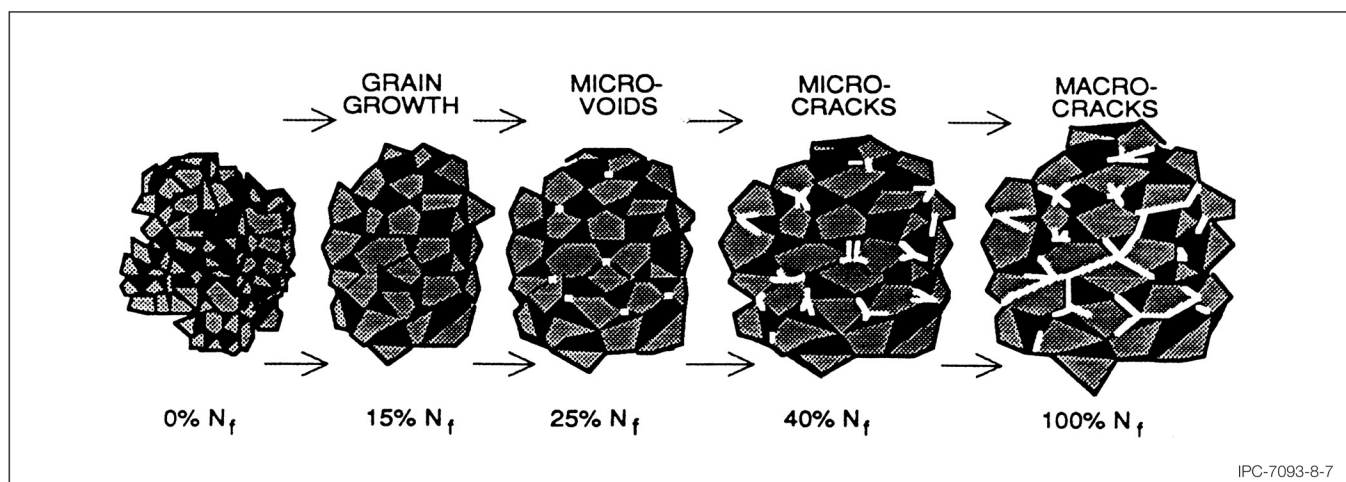
**8.7.4 Global Expansion Mismatch** The global expansion mismatches result from differential thermal expansions of an electronic component or connector and the printed board to which it is attached via the surface mount solder joints. These thermal expansion differences result from differences in the CTEs and thermal gradients as the result of thermal energy being dissipated within active components. This global expansion mismatch will cyclically stress, and thus fatigue, the solder joints. The cyclically cumulative fatigue damage will ultimately cause the failure of one of the solder joints, typically a corner joint, of the component causing functional electrical failure that is initially intermittent. See Figure 8-8.



IPC-7093-8-8

**Figure 8-8 Solder Crack Due to Cte Mismatch after 1000 Cycles**

**8.7.5 Local Expansion Mismatch** The local expansion mismatch results from differential thermal expansions of the solder and the base material of the electronic component or PCB to which it is soldered. These thermal expansion differences result from differences in the CTE of the solder and those of the base materials together with thermal excursions.



IPC-7093-8-7

**Figure 8-7 Depiction of the Effects of Accumulating Fatigue Damage in the Solder Joint Structure**

Local CTE-mismatches typically range from  $\Delta\text{CTE} \sim 7$  ppm/ $^{\circ}\text{C}$  with copper to  $\sim 18$  ppm/ $^{\circ}\text{C}$  with ceramic and  $\sim 20$  ppm/ $^{\circ}\text{C}$  with Alloy 42 and Kovar<sup>TM</sup>. Local thermal expansion mismatches typically are smaller than the global expansion mismatches since the acting distance, the maximum wetted area dimension, is much smaller, in the order of hundreds of microns.

**8.7.6 Internal Expansion Mismatch** An internal CTE-mismatch of  $\sim 6$  ppm/ $^{\circ}\text{C}$  results from the different CTEs of the Sn-rich and Pb-rich phases of the solder. Internal thermal expansion mismatches typically are the smallest since the acting distance, the size of the grain structure, is much smaller than either the wetted length or the component dimension in the order of less than 25  $\mu\text{m}$ .

**8.8 Solder Attachment Failure** The failure of the solder attachment of a component to the substrate to which it is surface mounted is commonly defined as the first complete fracture of any of the solder joints of which the component solder attachment consists. Given that the loading of the solder joints is typically in shear, rather than in tension, the mechanical failure of a solder joint is not necessarily the same as the electrical failure. Electrically, the mechanical failure of a solder joint results, at least initially, in the occasional occurrence of a short-duration ( $< 1 \mu\text{s}$ ) high-impedance event during either mechanical or thermal disturbance. From a practical point of view, the solder joint failure is defined as the first observation of such an event.

For some applications this failure definition might be inadequate. For high-speed signals with sharp rise times, signal deterioration prior to the complete mechanical failure of a solder joint might require a more stringent failure definition. Similarly, for applications which subject the electronic assemblies to significant mechanical vibration and/or shock loading, a failure definition that considers the mechanical weakening of the solder joints as the result of the accumulating fatigue damage might be necessary.

**8.9 Validation and Qualification Tests** Performance test methods and qualification requirements are specified in IPC-9701; IPC-9701A includes guidelines for lead free

solder joint reliability testing. However, in the current absence of generally useful reliability acceleration models, there currently are no qualification requirements for lead free solder joint.

The validation and qualification tests should follow the guidelines given in IPC-SM-785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments. However, for large components with significant heat dissipation, for components of asymmetric construction, and for small global CTE mismatches, temperature cycling tests are inadequate to provide the required information; full functional cycling including external temperature and internal power cycling is necessary.

## 8.10 Screening Procedures

**8.10.1 Solder Joint Defects** The solder joint defects of greatest reliability concern are those involving inadequate wetting for whatever reason. Properly wetted solder joints have adequate strength even for severe mechanical loading conditions as well as no diminished thermal cyclic fatigue reliability. However, solder joints not properly wetted, can prematurely fail both as the result of mechanical and thermal cyclic loading. Voids in the solder joints are generally regarded as not constituting a reliability threat. However, there are some exceptions. Large voids reducing the solder joint cross-section enough to reduce a required thermal heat transfer function, such as those for the thermal pads on MLF and QFN devices, can cause premature device failure.

**8.10.2 Screening Recommendations** Effective screening procedures need to be capable of causing the failure of latent solder joint defects, i.e., weak inadequately wetted solder joints, without causing significant damage to high quality solder joints. The best recommendation is random vibration (6–10 grams for 10–20 minutes), preferably at low temperature, e.g.,  $40^{\circ}\text{C}$ . This loading does not damage good solder joints, but overstresses weakly bonded ones. Thermal shock can also be successfully used, however some damage to good solder joints can be expected, particularly for larger components.

## 9 DEFECT AND FAILURE ANALYSIS CASE STUDIES

This section provides information on BTC package attachment defects.

The illustrations are provided to assist the user as a process effects condition. The illustrations may be used as a troubleshooting guide and controlled experiment characteristics in order to determine potential solutions for eliminating any problems.

### 9.1 Solder Attachment Failures

#### 9.1.1 Solder Attachment Failure Conditions



IPC-7093-9-1

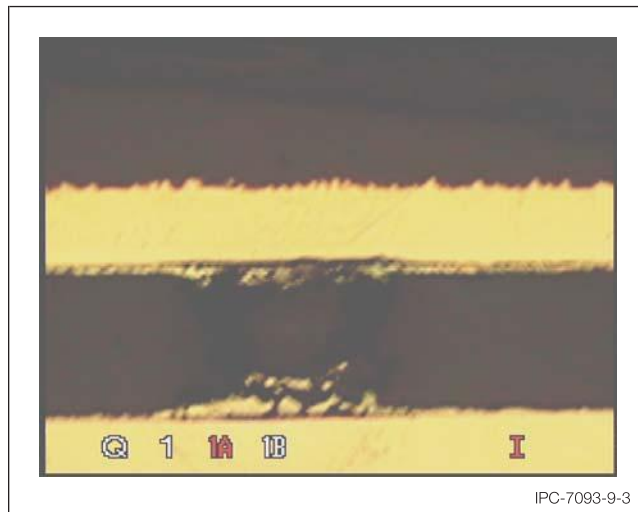
**Figure 9-1** Optical image of acceptable QFN edge terminations. Solder fillets should exist if the design incorporates pads that extend beyond the package width.



IPC-7093-9-2

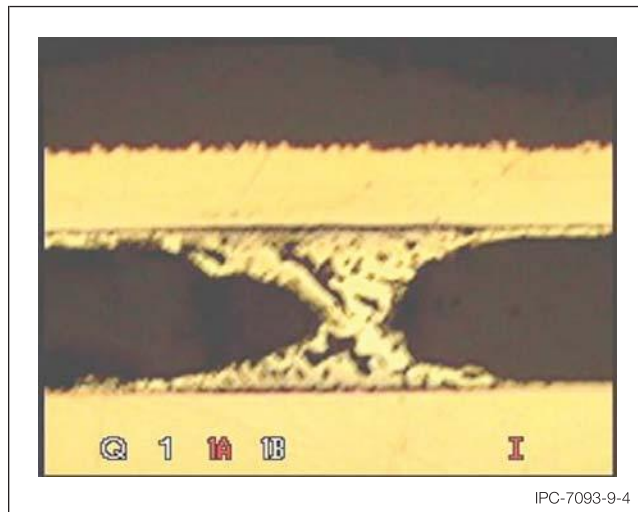
**Figure 9-2** Optical image of acceptable QFN edge terminations. Solder fillets should be visible to a minimum of 75% of the width of the termination.

#### 9.1.2 Insufficient Solder Failures



IPC-7093-9-3

**Figure 9-3** Cross section of BTC open joint due to insufficient solder paste volume during printing.



IPC-7093-9-4

**Figure 9-4** Cross section of BTC reliability failure after 1000 cycles due to insufficient solder paste volume during printing.

### 9.1.3 Land, Nonsolderable

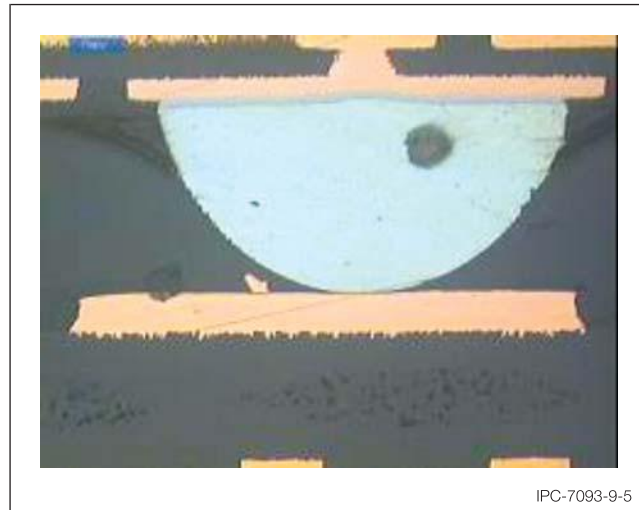


Figure 9-5 Nonsolderable land on LGA package.

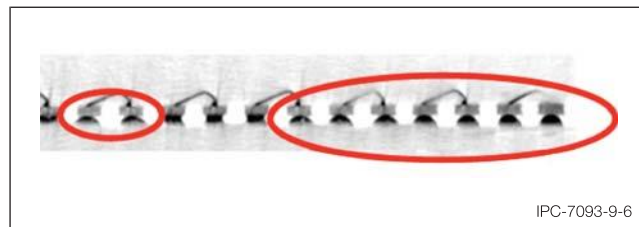


Figure 9-6 3-D X-ray shows non-wet joints on a QFN.

### 9.1.4 Termination, Nonsolderable

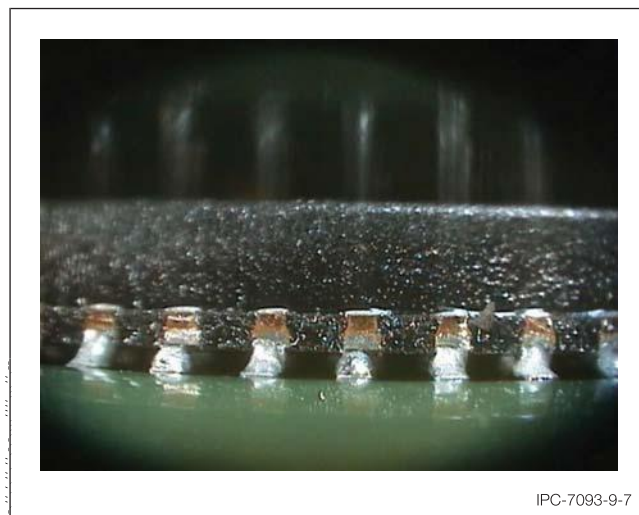


Figure 9-7 Optical image of unacceptable QFN edge terminations. The solder rise is limited and an open joint can be seen. The package is also 'floating' above the surface of the pads.

## 9.2 Package Failures

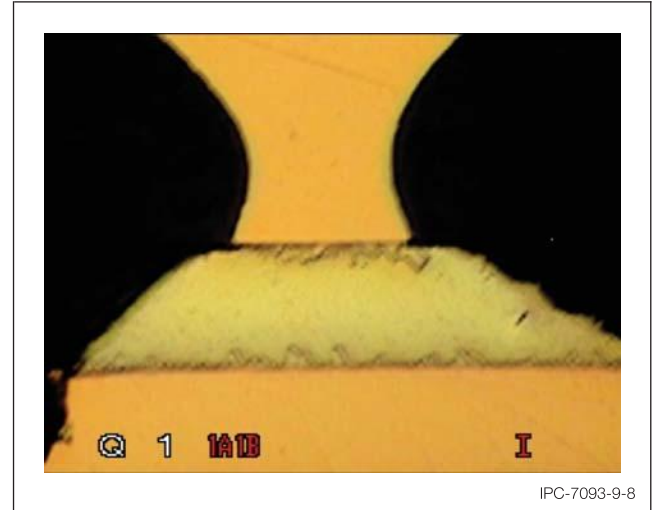


Figure 9-8 Cross section image of QFN with an open joint caused by nonwetting of the solder to the bottom land of the QFN.

### 9.2.1 Package Warpage

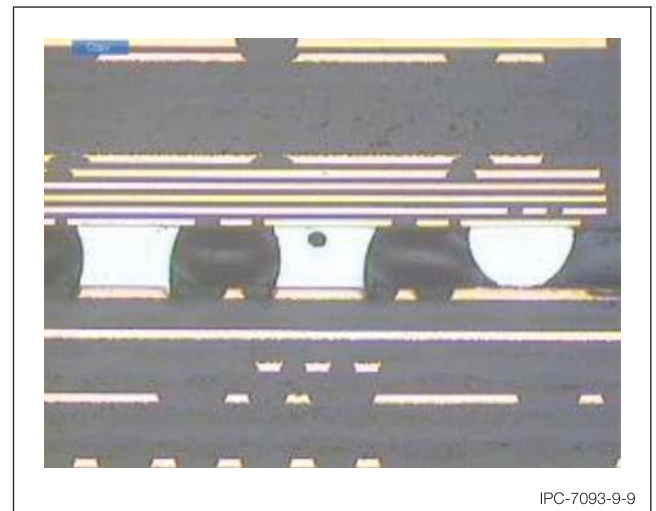


Figure 9-9 Cross section of LGA with a corner joint failure. The paste wicked to the package.

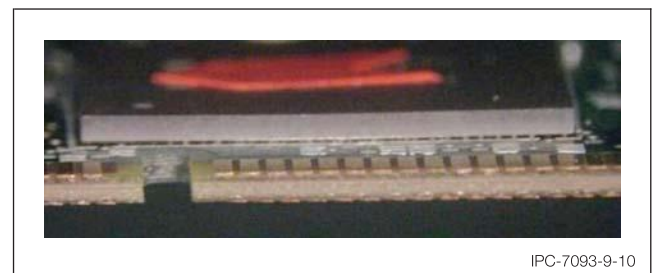


Figure 9-10 Concave warpage on 15x15 mm BTC.

### 9.3 Dewetting Failures

#### 9.3.1 Dewetting on QFN

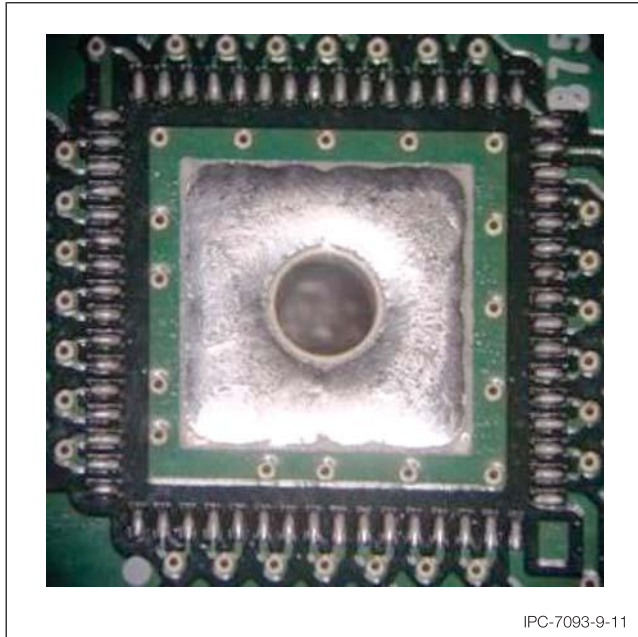


**Figure 9-11** Good wetting on QFN thermal pad after printing and reflow.

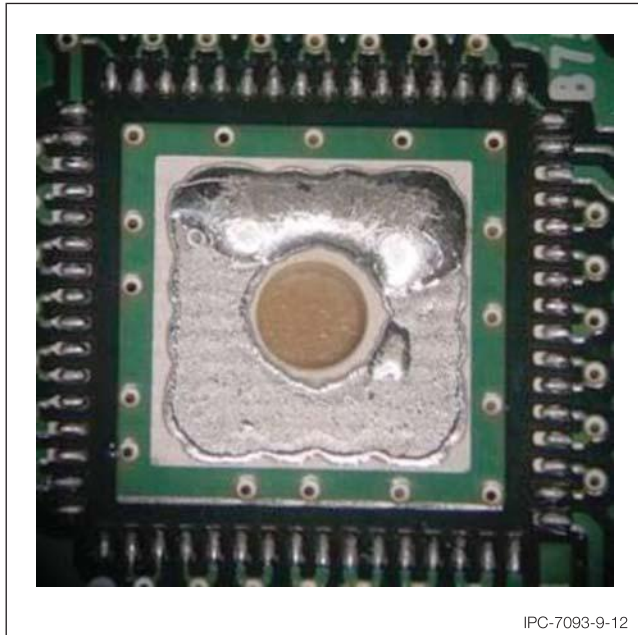


**Figure 9-12** Dewetting on QFN thermal pad after printing and reflow.

### 9.4 Cracked Solder Joint Failure

#### 9.4.1 Cracks in Solder Joints

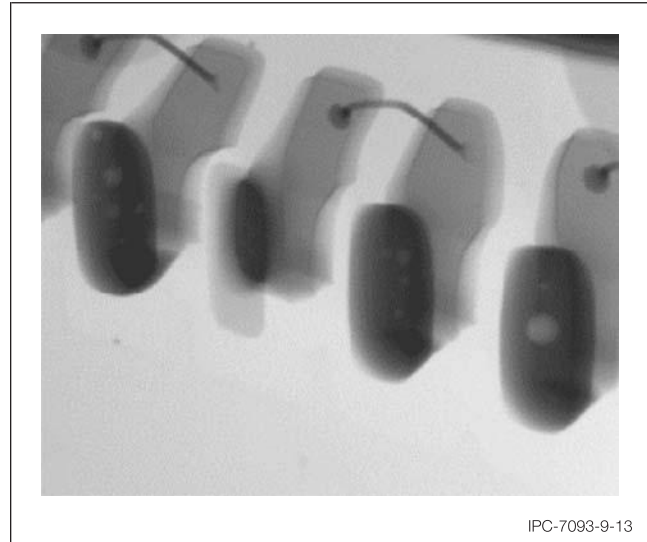


**Figure 9-13** Defect Condition of QFN edge joints showing insufficient solder in a joint.

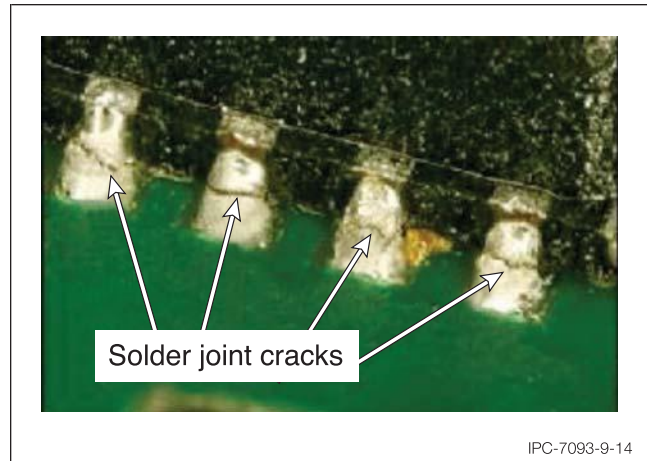


**Figure 9-14** Cracks in QFN solder joints after temperature shock.

## 9.5 Component Failures

### 9.5.1 Tilted Component



Figure 9-15 Tilted BTC causing high joint height open on the left.

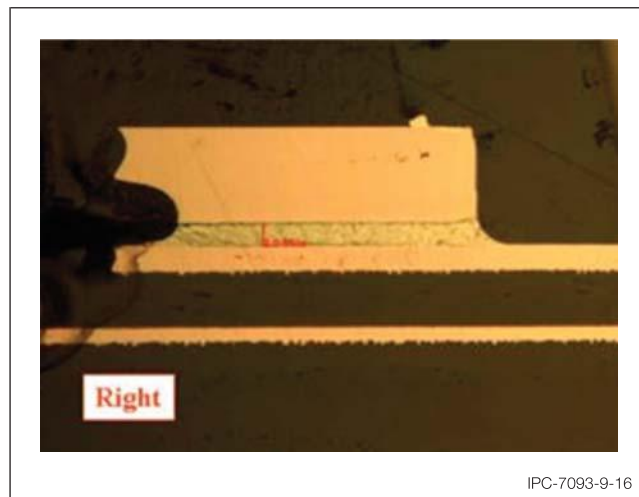


Figure 9-16 Tilted BTC causing good height on the right.

### 9.5.2 Lead Configuration Conditions



Figure 9-17 Full lead option on BTS component.



Figure 9-18 Half etched option on BTS component.

### 9.5.3 Joint Configuration Condition



**Figure 9–19** Small fillet due to nonwetting of the side copper.



**Figure 9–20** Side fillet on bottom termination component good wetting to copper lead.

### 9.5.4 Solder Joint Volume

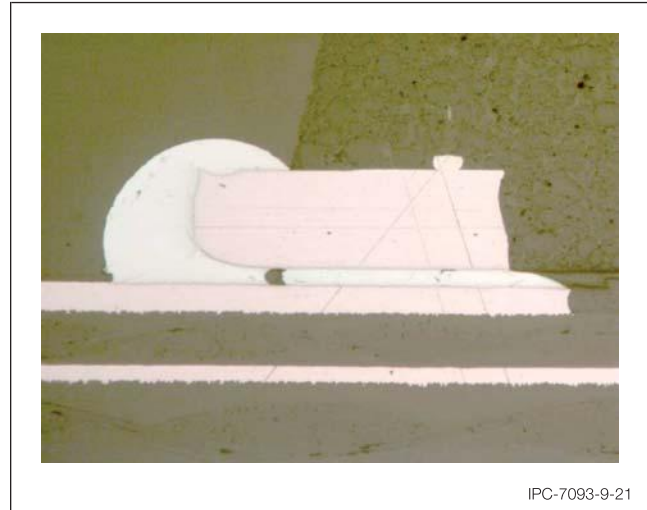


**Figure 9–21** Large fillet due to increase of solder volume.



**Figure 9–22** No Side fillet on bottom termination component.

## 9.6 Voids

### 9.6.1 Voids in Solder Joint Through Xray

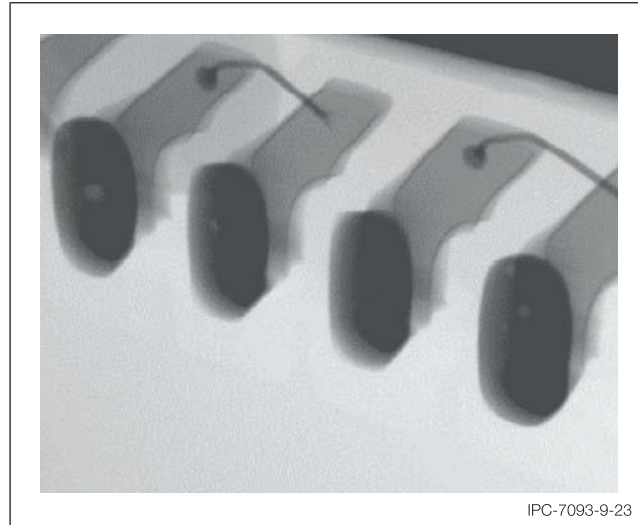


**Figure 9-23 Target Condition of QFN edge joints where showing a moderate level of voiding within joints is acceptable. All joints have reflowed.**

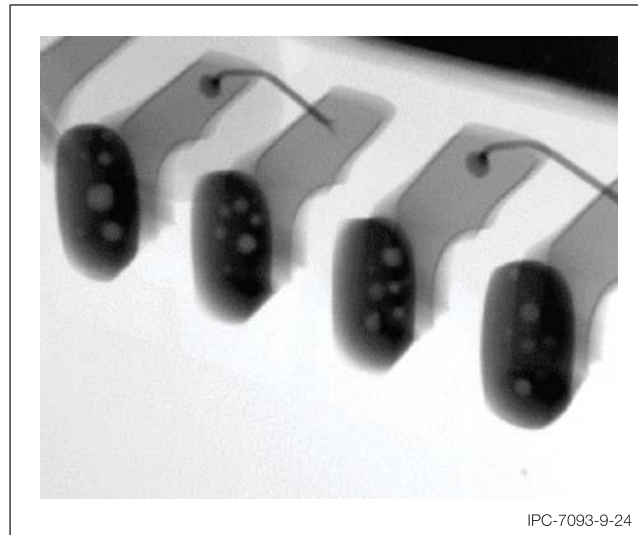


**Figure 9-24 Acceptable Condition of QFN edge joints showing an increased level of voiding within the joints but well within any action level.**

### 9.6.2 Voids in Solder Joints Microsection and X-Ray

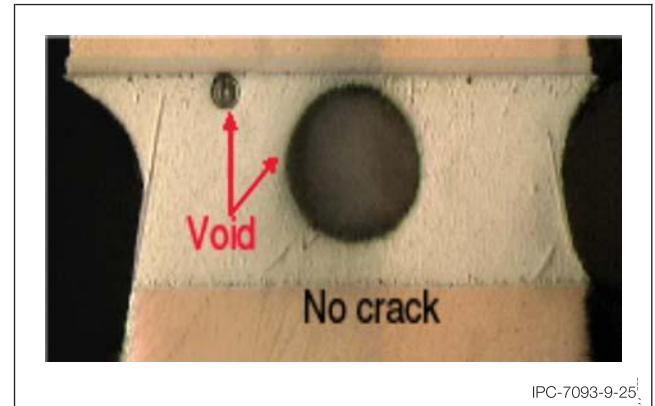


**Figure 9-25 BTC component with a large edge joint. The joint did not have any cracking after shock test.**

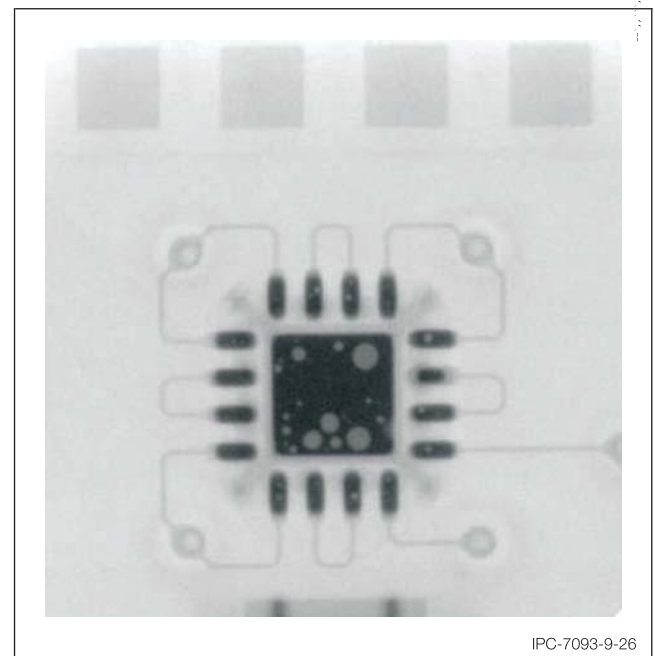


**Figure 9-26 16-pin QFN with voids in the joint and the thermal pad but well within action level.**

### 9.6.3 Voids in Thermal Pad

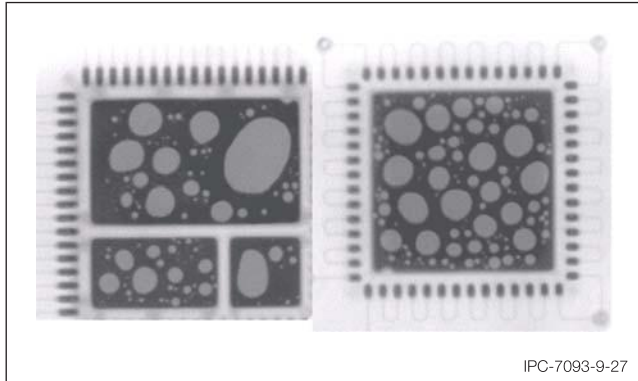


**Figure 9–27** QFN component with increase level of voiding to above 30%. Could be a reliability concern.

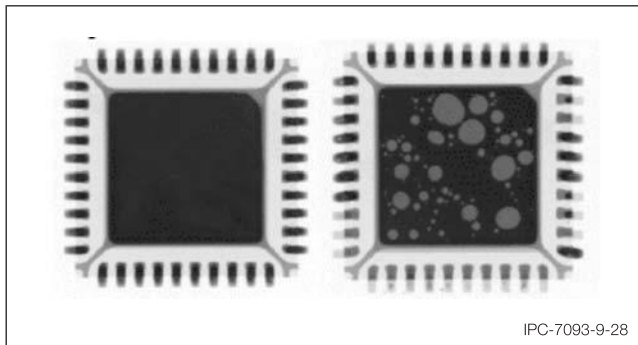


**Figure 9–28** Acceptable Condition of QFN edge joints showing an increased level of voiding within the joints but well within any action level.

**10 GLOSSARY AND ACRONYMS**

|        |                                                         |
|--------|---------------------------------------------------------|
| AABUS  | As Agreed Upon Between User And Supplier.               |
| ASIC   | Applications Specific IC                                |
| ASM    | Array Surface Mount                                     |
| ASMP   | Application Specific Module Packaging                   |
| BGA    | Ball Grid Array                                         |
| BOC    | Board-On-Chip                                           |
| BT     | Bismaleimide-Triazine                                   |
| BTC    | Bottom Termination Components                           |
| CBGA   | Ceramic Ball Grid Array                                 |
| CGA    | Column Grid Array                                       |
| COB    | Chip-On-Board                                           |
| CPU    | Central Processing Unit                                 |
| CSP    | Chip Scale Packages                                     |
| CTE    | Coefficient Of Thermal Expansion                        |
| CTF    | Critical To Function                                    |
| DAP    | Die Attach Pad                                          |
| DBDPE  | Decabromodiphenyl Ether                                 |
| Df     | Dissipation Factor                                      |
| DFN    | Dual Flat No-lead                                       |
| DfR    | Design For Reliability                                  |
| DIG    | Direct Immersion Gold                                   |
| Dk     | Dielectric Constant                                     |
| ENEPIG | Electroless Nickel/Electroless Palladium/Immersion Gold |
| ENIG   | Electroless Nickel Immersion Gold                       |
| FAT    | Flux Activation Time                                    |
| FBGA   | Fine Pitch Ball Grid Array                              |
| FC     | Flip Chip                                               |
| FPT    | Fine Pitch Technology                                   |
| HASL   | Hot Air Solder Level                                    |
| HAST   | Highly Accelerated Stress Testing                       |
| HDB    | High Density Printed Boards                             |
| I/O    | Input/Output                                            |
| IMC    | Intermetallic Compound                                  |
| IR     | Infrared                                                |
| LCP    | Liquid Crystal Polymer                                  |
| LFBGA  | Low-Profile Fine-Pitch Ball Grid Array                  |
| LGA    | Land Grid Array                                         |
| LMC    | Least Material Condition                                |
| MCM    | Multichip Module                                        |
| MCM-L  | Multichip Module-Laminate                               |
| MCP    | Multichip Package                                       |
| MD     | Metal Defined                                           |
| MDS    | Multi Device Subassembly                                |
| MLC    | Multilayer Ceramic                                      |
| MMB    | Moisture Membrane Bag                                   |
| MMC    | Maximum Material Condition                              |
| MSL    | Moisture Sensitivity Level                              |
| NSMD   | Non Solder Mask Defined                                 |
| OEM    | Original Equipment Manufacturer                         |
| OSP    | Organic Solderability Preservative                      |
| PBB    | Polybrominated Biphenyl                                 |

|                |                                              |
|----------------|----------------------------------------------|
| PBBO           | Polybrominated Biphenyl Oxide                |
| PBDE           | Polybrominated Diphenyl Ether                |
| PBGA           | Plastic Ball Grid Array                      |
| PCA            | Printed Circuit Assembly                     |
| PCB            | Printed Circuit Board                        |
| PCM            | Phase Change Materials                       |
| PLCC           | Plastic Leaded Chip Carrier                  |
| PSA            | Pressure Sensitive Adhesives                 |
| PTH            | Plated Through-Hole                          |
| QFN            | Quad Flat No-Lead                            |
| QFP            | Quad Flat Pack                               |
| RDS            | Rectangular Die Size                         |
| RF             | Radio Frequency                              |
| RFID           | Radio Frequency Identification               |
| RMS            | root mean, square                            |
| RoHS           | Restriction of Hazardous Substances          |
| SDRAM          | Synchronous Dynamic random access memory     |
| SMD            | Solder Mask Defined                          |
| SMOBC          | Solder Mask Over Bare Copper                 |
| SMT            | Surface Mounting Technology                  |
| SO-DIMM        | Small Outline Dual In-Line Memory Module     |
| SOIC           | small outline integrated circuit             |
| SON            | Small Outline No-lead                        |
| SPC            | Statistical Process Control                  |
| SRAM           | Static random access memory                  |
| SSO            | Simultaneously Switching Output              |
| TAB            | Tape-Automated Bonding                       |
| TBBPA          | Tetrabromobisphenol A                        |
| T <sub>d</sub> | Decomposition Temperature                    |
| TFBGA          | Thin Profile Fine Pitch Ball Grid Array      |
| T <sub>g</sub> | Transition Temperature                       |
| TIM            | Thermal Interface Materials                  |
| UFPT           | Ultra Fine Pitch Technology                  |
| UtRAM          | Uni-transistor Random Access Memory          |
| UUT            | Unit Under Test                              |
| UV             | Ultraviolet                                  |
| VFBGA          | Very Thin-Profile Fine-Pitch Ball Grid Array |

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## APPENDIX A

# Metallographic Preparation

### INTRODUCTION

Preparing tin-lead solder joints for metallographic evaluation requires extra care. The samples are composed of high hardness (Copper-Tin) intermetallic compound particles dispersed in a very soft (Lead, Lead-Tin) matrix. This heterogeneous mass is coated on a hard basis material of copper or iron alloy. The lead-tin matrix can recrystallize at temperatures achieved during the curing of some epoxy mounting materials or hardening of some thermoplastic mounting materials. Polyester or acrylic mounting materials with as LOW a temperature rise during cure or setup as possible are recommended. Great care is required in revealing the undeformed, undamaged structure under the superficial layer.

General comments on metallographic sample preparation, mounting, and polishing can be found in IPC-TM-650, 2.1.10 and 2.1.1.2, in IPC-MS-810, “Guidelines for High Volume Microsection,” and in Leco Corporation’s “Metallography Principles and Procedures” which also contains reprints of ASTM E407–70 and ASTM E340–68. In addition, pages 5–12 in the ITRI publication 580 are instructive in dealing with tin-lead solder joint destructive physical analysis (DPA).

**A1 Cutting** The initial step for metallographic preparation is the isolation of the component or solder joint for mounting. This entails the use of a jeweler’s saw, router, abrasive saw, or similar cutting device to remove the specimen. Several factors should be considered during this initial step:

1. **Cut Location:** Care must be taken to remove the specimen without cutting too close to the solder joint of interest. The cut should, however, be close enough that excessive grinding is not required. If in doubt, leave a little extra material. Usually 2.5 mm of material around the area of interest is sufficient.
2. **Fixturing:** Care must be taken to ensure that damage is not done to the specimen while holding it for cutting.
3. **Cutting Speed:** A smooth, consistent feed rate and pressure should be maintained to avoid damaging the specimen. Vibration of the specimen during cutting must be avoided.
4. **Cutting Fluids:** Oil, water, or other types of coolant should be used with abrasive blades, especially diamond blades. The cutting fluid serves two main purposes:
  - a) Removal of the cutting debris, allowing for efficient material removal.
  - b) Removal of heat generated during cutting. When a situation requires dry cutting, extreme care must be taken to avoid generating heat which may affect the specimen, particularly solder joints or polymeric materials. A coolant should be chosen which can be cleaned off of the specimen easily and completely, so that the encapsulating epoxy can bond to the sample surface.

5. **Ceramic Precautions:** Due to their hardness, aluminum oxide ceramic specimens require the use of diamond bonded cutting equipment during both cutting and grinding. Also, beryllium and beryllium oxide materials produce toxic dust and must never be cut dry.

**A2 Mounting** The specimen should be encapsulated in some rigid medium for grinding and polishing, so as to achieve a flat, uniform surface and to protect the solder joint. Caution must be used to ensure that the mounting procedure does not change the solder joint microstructure. Overplating with copper or nickel can help to protect highly deformable materials. Two mounting methods are:

1. **Quick Mounting:** This method utilizes a thermoplastic material such as polymethylmethacrylate, and typically is not entirely transparent. Filling of small cavities and adhesion to the sample may be inferior to the results of slow mounting. However, one mount can usually be prepared in approximately 5–15 minutes. The heat generated by quick mount systems varies widely from product to product.
2. **Slow Mounting:** This method typically utilizes epoxides as the mounting media. Vacuum impregnation techniques can be used to remove air bubbles and improve flow of the encapsulant into confined spaces. Some encapsulants must be cured at temperatures ranging from 60 to 90°C, while others are room temperature curing, but can generate even higher temperatures by exothermic reactions. Experimentation with empty molds will reveal whether this is a problem. Curing in a water bath helps to remove excess heat. Mounting time can vary from 1 to 8 hours depending upon the product and the curing conditions.

**A3 Preparation for Mounting** When mounting a specimen, it is important that it be oriented properly. Proper orientation depends upon your grinding and polishing equipment and technique. Practice will determine what works, and what does not. Here are two basic mounting methods:

1. **Vertical Mounting:** The sample is held vertical relative to the bottom of the mold either by gluing it to the mold

floor or by using special clips. The encapsulant can then be poured into the mold until it is full.

2. **Half-Mounts:** The sample is placed horizontally into a mold which is half full of previously cured encapsulant. The mold is then filled with encapsulant and allowed to cure. The sample is then ground from the side, and may not fit into some automatic machines. If this is a problem, then vertical mounting should be used. Note: The grinding and polishing sections of this procedure were written from the point of view of manually grinding and polishing the sample. Most of the concepts are applicable, however, to automatic processing. Attempts have been made to reconcile the differences between the two procedures.

**A4 Grinding** The third step of sample preparation involves removing material from the specimen to expose the areas of interest. Grinding is an abrasive process to slowly remove deformed surface material and reveal underlying, nondeformed regions. Grinding is typically done using silicon carbide papers, progressing from 120 to 1000 grit depending on the amount of material removal required. Several factors should be considered during this step:

1. **Pressure:** Sample hardness dictates, to some extent, the amount of pressure required. Pressure should be kept light to avoid excess deformation of the specimen surface.
2. **Time:** The grinding time for each piece of grinding paper should be kept short. Excessive grinding time can cause faceting as the grinding paper wears down and the particles get dull. Faceting is usually corrected by switching to a new, sharp piece of grinding paper.
3. **Cutting Fluid:** As with the cutting operation, fluid is used to remove debris and prevent the specimen from overheating. Water is the most common cutting fluid.
4. **Ceramic Materials:** Due to the hardness of ceramics, components, packages and substrates made of ceramics such as aluminum oxide (alumina) or beryllium oxide (beryllia) require the use of diamond bonded cutting wheels and grinding disks. Mechanical processes such as grinding and polishing of beryllia pieces create a dust defined as a hazardous material; this dust must be suppressed by sufficient coolant and cutting fluid. OSHA and EPA handling requirements will supersede any technical handling or use requirements. The beryllia dust mixed with the fluid is defined as a hazardous material; this aspect must be considered during disposal.
5. **Viewing Window:** Often during precision grinding it is helpful to look clearly at the sample from above. This can be accomplished by grinding and polishing a flat area on the surface of the epoxy perpendicular to the sectioning plane. Some automatic equipment does not allow mounting of these irregularly shaped samples, however.

6. The hard intermetallic compounds such as Cu<sub>6</sub>Sn<sub>5</sub>, Cu<sub>3</sub>Sn, Ni<sub>3</sub>Sn<sub>2</sub>, Ni<sub>3</sub>Sn<sub>7</sub>, AuSn, AuSn<sub>2</sub>, AuSn<sub>4</sub>, FeSn, FeSn<sub>2</sub>, and Ag<sub>3</sub>Sn can cause grooves and channels in the soft lead or lead-tin matrix when the particles break free and roll downstream. Manually or automatically moving or rotating the sample counter to the wheel rotation will minimize grooves and channels.

**A5 Polishing** The next stage of metallographic preparation following the grinding step is polishing the sectioning plane. Polishing is a less severe continuation of the specimen surface abrasion. Polishing media can include diamond, aluminum oxide, silicon oxide, or chromium oxide. Polishing media particle size progresses from about 9 µm to as fine as 0.05 µm to produce a uniform, scratch free surface. This is usually divided into coarse (9 to 1 µm) and fine (1 to 0.05 µm) polishing. Again several factors should be considered during this step:

1. **Cleanliness:** WASH THE SAMPLE FREQUENTLY. It is extremely important that the sample and anything that comes near it (including hands and work benches) be as clean as possible at all times during polishing. The sample should be washed and rinsed with warm soapy water before beginning to polish the sample and after each step. Brief ultrasonic cleaning is the most effective way to clean out small cavities such as cracks or voids.
2. **Polishing Cloth Selection:** The primary difference between grinding and polishing is that while grinding grit is fixed in place, polishing uses freely flowing particles in a slurry. This slurry is held on a cloth which determines the extent of the surface relief and the polish quality. Lower nap cloths will produce a flatter surface than high nap cloths, but may not remove all scratches as effectively. Special low nap fine polishing cloths can produce a very flat, nearly scratch-free surface.
3. **Polish Extenders:** Extenders play an analogous role in polishing to that of the cutting fluid in grinding, removing debris and minimizing heat generation. An extender also ensures proper dispersion of the polishing media. Care must be taken to use the proper amount of extender. Too much extender will allow the sample to float, causing excessive relief. Too little extender may allow the encapsulant to soften and absorb polishing media, especially diamond particles. The extender used is a function of the polishing medium, and is usually either deionized water or a special polishing oil.
4. **Pressure:** Polishing pressure should be very light. Excessive pressure causes excessive surface relief.
5. **Direction:** Coarse polishing can be done either of two ways. Trial and error will indicate which is best for you, and results may vary for different types of samples. Omni-directional polishing involves rotating the sample around the polishing wheel either counter to, or with the wheel rotation. In this way the polishing is performed in

all directions. Uni-directional polishing is where the sample is held stationary, and the polishing scratches are all aligned in one direction. This is particularly useful on layered structures. Fine polishing is almost always performed omni-directionally. Most automatic machines function only in the omni-directional mode.

**A6 Etching** Etching is the final step in metallographic sample preparation. The specimen should be examined before the etching step is performed for defects, inclusions, porosity, cracks, intergranular corrosion, intermetallic compound development, and other anomalies. Etching removes a thin layer of abraded surface deformation, revealing the microstructural details of the specimen. Etching requires the use of an acid or a base to chemically attack the sample surface. Many enchants are available for etching a variety of materials. The disposal of the wastes generated may be a problem due to the presence of heavy metals such as the chromates and of toxics such as beryllia dust. See ASTM E407–70 for safety cautions. The chemicals used should be USP or NF or better. See ITRI publication 580 for etchants specific to tin and its alloys and for photomicrographs of the resulting sample surfaces.

1. *Lead-Tin Phases:* Nital (1–5 ml HNO3 100 ml ethanol (95%) or methanol (95%) Immerse 5–40 seconds in 5% HNO3 solution. To remove stain, immerse 25 seconds in 10% HCl-Methanol solution.

2. A variety of etches for Copper-Tin IMC is shown in Table A-1:

**Table A1-1 Etchants used to highlight Intermetallic compounds**

| Various Etchants       |               |                 |                   |
|------------------------|---------------|-----------------|-------------------|
| 95 ml H2O              | 7 grams FeCl3 | 100 ml H2O      | 100 ml NH4OH, 35% |
| 10 ml 10% Chromic Acid | 75 ml HCl     | 100 ml H2O2, 3% | 100 ml H2O2, 3%   |
| 2 ml HCl               | 200 ml H2O    |                 |                   |
| 5 ml H2SO4             |               |                 |                   |

3. *Solder:* Solder can be chemically etched using a dilute (5% maximum) hydrochloric acid solution, but acceptable results can usually be obtained by extensive final polishing using extremely light pressure. Solder is extremely reactive to most etches, and care must be taken not to destroy its structure.

4. *Copper:*

- 50 ml Ammonium Hydroxide
- 50 ml Water
- 3 to 5 gm Ammonium Persulfate

5. *Stainless Steel or Kovar:*

- 10 gm Copper Sulfate
- 50 ml Hydrochloric Acid
- 50 ml Water

## APPENDIX B

# Dye Penetrant

Dye penetrant analysis of BTC packages on printed wiring assemblies can be used to confirm assembly process parameters and solder joint quality/integrity. The following procedure utilizes a fluorescent dye that enhances defect flaws when inspected under UV light.

**Step 1: BTC Package Cleaning** Prepare the selected BTC package of interest by cleaning with an Acetone solvent rinse. Fully submerge the BTC package in Acetone and subject the package/solution to 60 second duration in an ultrasonic cleaner. Remove the BTC package from the Acetone solvent solution, use clean compressed air to blow any residual solution from the component, and bake at 100°C for 20 minutes to ensure that the package is free from residual liquid solvent. This cleaning process is intended to ensure that the BTC package is free from flux residue and other materials that may impede the penetration of the dye.

**Step 2: Apply the Dye** Submerge the BTC package in dye penetrant. If full submersion of the BTC package is not possible or removal of the BTC package from the printed wiring assembly not possible, lay the printed wiring assembly flat and apply the penetrant to the edge of the BTC package to allow the dye to wick beneath the package body. Ensure that sufficient dye has been added such that the entire underside of the BTC package has been covered

**Step 3: Vacuum** After the BTC package has been submerged, apply an external vacuum to draw out air that may be entrapped under the package body. A 60 second duration under vacuum is acceptable; however, longer durations can be used. Caution should be exercised during the application of the vacuum as the dye penetrant will likely boil and splatter. Adjustment of the vacuum intensity can be conducted to minimize the dye solution boiling. The boiling action of the dye will impact the efficiency of the dye to wick and penetrate small cracks in the BTC package. Note: different dye formulations have specific vacuum reaction characteristics.

**Step 4: Dry the Dye** Wipe the BTC package with a laboratory wipe to remove excess dye. Bake the BTC package at 100°C for a minimum of 30 minutes. Bake the BTC package at 50 °C to 100 °C for a minimum of 10–30 minutes. The bake time/temperature duration may require adjustment for your specific dye formulation, the BTC packages being tested and/or assemblies with large thermal masses.

**Step 5: Freeze the BTC Package** It is recommended that the BTC Package be submerged in liquid Nitrogen freezing the package allowing for easier pry removal. Caution should be exercised as liquid nitrogen will burn skin if direct contact is achieved. A use proper safety precaution (gloves, eye protection etc.) is required. The duration of the BTC package being submerged in the Liquid N2 is dependant on the package thermal mass. The liquid N2 will “boil” as the room temperature BTC package is submerged. As the package reaches equilibrium with the liquid nitrogen the boiling action will cease.

**Step 6: Remove the BTC Package and Pry** Remove the BTC package from the liquid nitrogen bath and pry. The BTC package should pry off easily provided the pry tools are adequate for the package size. Caution should be exercised during the pry step to insure that a vertical/tensile force and not a horizontal/shear force is applied to the BTC package. A shearing force will affect the quality of the solder joint fracture surface.

**Step 7: Inspection of Fractured Solder Joints** Inspect the resulting surfaces and document results. It is important to inspect both fracture surfaces (PCB and BTC) for presence of the dye.

Figure B1–1 illustrates a BTC component and PCB land after undergoing the Dye and Pry procedure

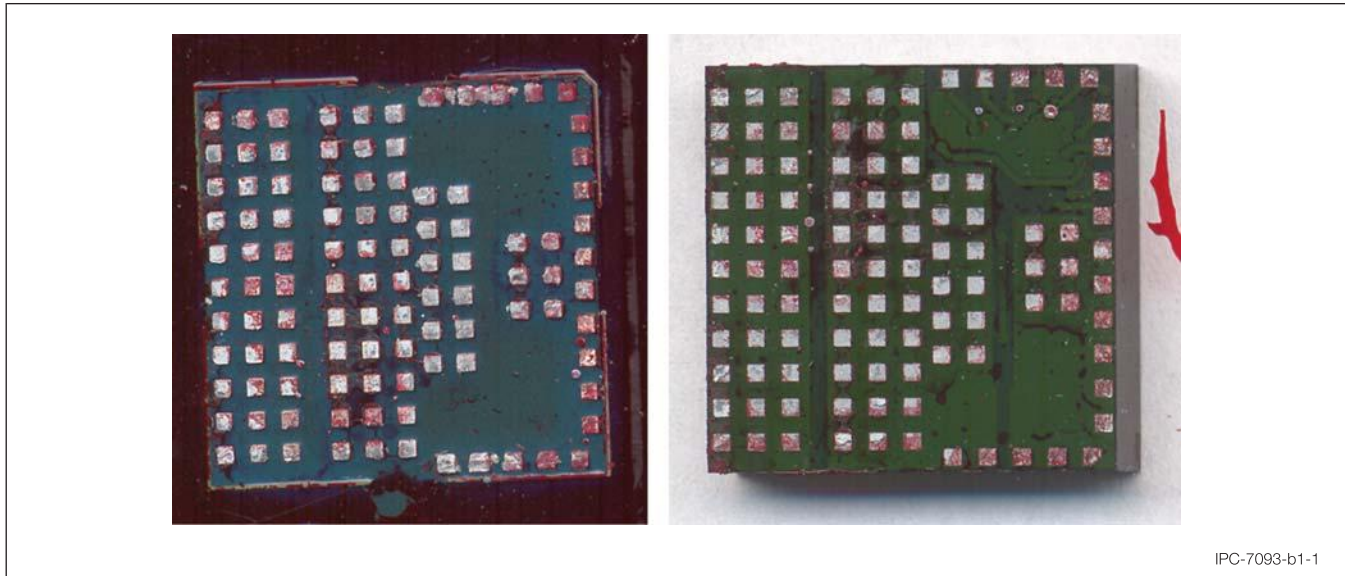


**Figure B1-1** BTC Component (left) and PCB (right) after Part Removal

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1. I recommend changes to the following:

\_\_\_ Requirement, paragraph number \_\_\_\_\_  
\_\_\_ Test Method number \_\_\_\_\_, paragraph number \_\_\_\_\_

The referenced paragraph number has proven to be:

\_\_\_ Unclear \_\_\_ Too Rigid \_\_\_ In Error  
\_\_\_ Other \_\_\_\_\_

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2. Recommendations for correction:

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3. Other suggestions for document improvement:

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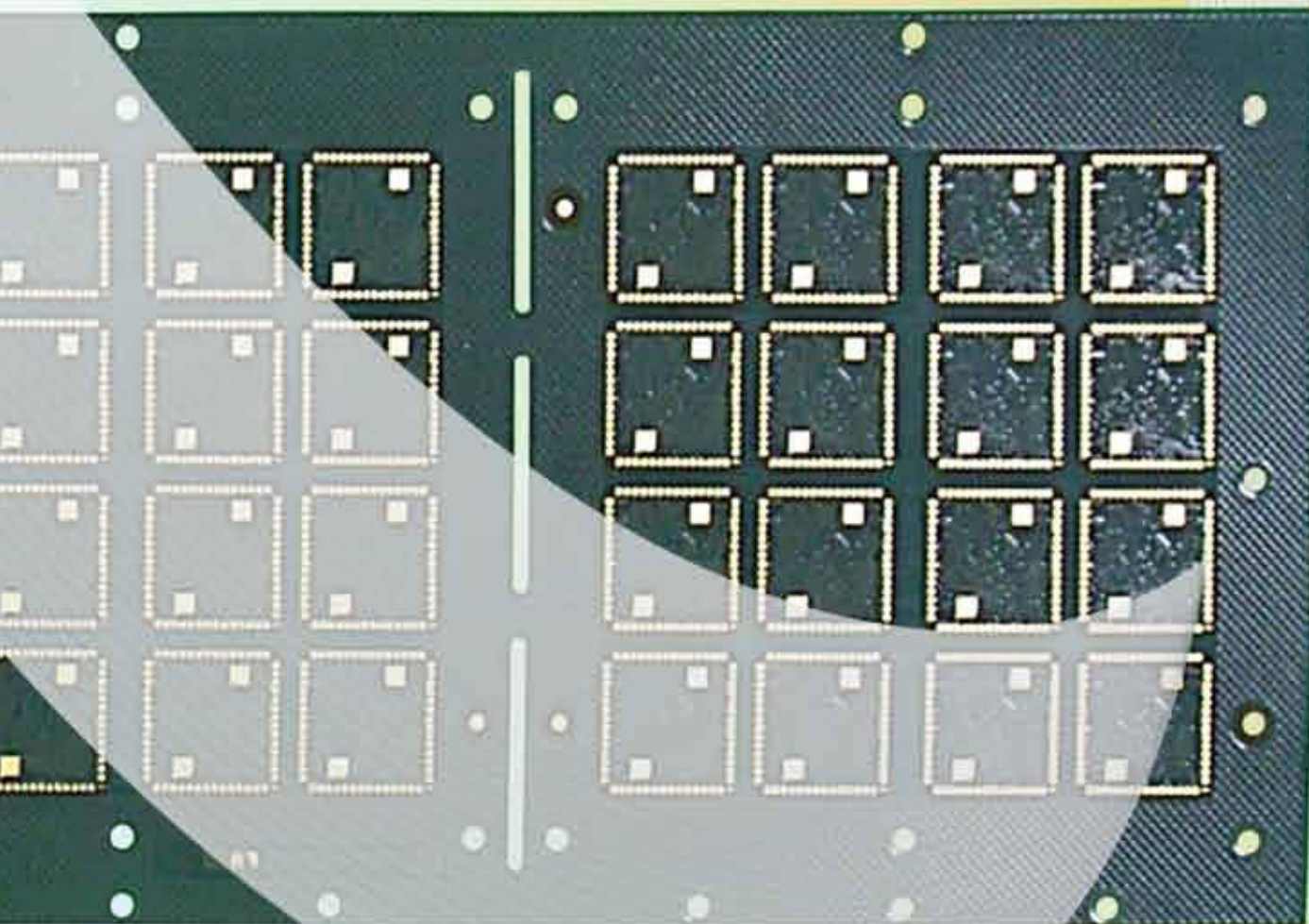
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ISBN # 1-580986-90-0

IPR2024-00705 EX. 2003