VTM™ Current Multiplier

VTM2308S60Z1513T00

Sine Amplitude Converter (SAC™)

Features & Benefits

- 2250V_{DC} Galvanically Isolated Output Voltage
- 48 – 12V_{DC} 12.5A Current Multiplier
  - Operating from Standard 48V or 24V PRM™ Regulators
  - Up to 60 Volts DC Input
  - K of 1/4 Provides up to 12.5A DC Output Current
  - Up to 16x Reduction in Output Capacitance Requirements
- High Efficiency (>95%) Reduces System Power Consumption
- High Density (215A/in^3)
- Vicor VTM2308 SM-ChiP™ Package Enables Low-Impedance Interconnect to System Board
- Provides Enable / Disable Control, Internal Temperature Monitoring
- ZVS / ZCS Resonant Sine Amplitude Converter Topology
- Can Be Used in Parallel for High-Current Applications

Typical Applications

- CPU, GPU & ASIC Core Rails
- Computing and Telecom Systems
- Automated Test Equipment
- Communications Systems

Product Ratings	
V_{IN} = 0 – 60V	I_{OUT} = 12.5A (Nominal)
V_{OUT} = 0 – 15V (No Load)	K = 1/4

Product Description

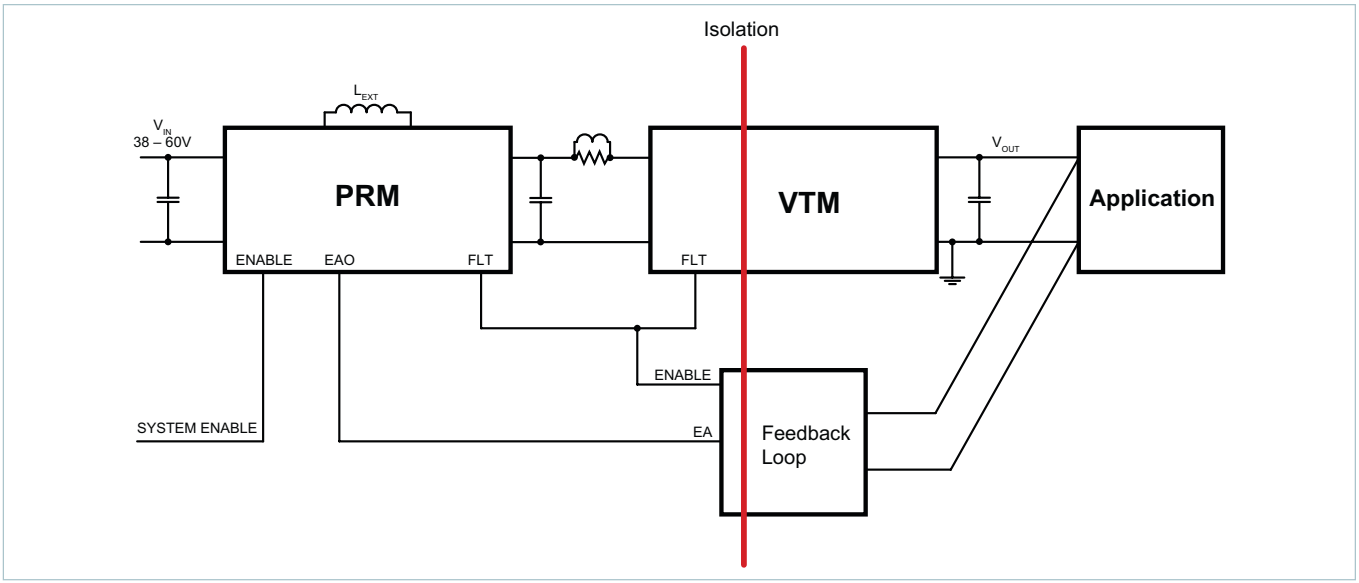
The Vicor VTM2308 SM-ChiP current multiplier is an isolated, high-efficiency Sine Amplitude Converter (SAC) designed to deliver low-voltage output. The Sine Amplitude Converter offers a low AC impedance beyond the bandwidth of most downstream regulators; therefore capacitance normally at the load can be located at the input to the Sine Amplitude Converter. Capacitance at the input of the VTM is reflected to the output by a factor of $(1/K)^2$, resulting in savings of board area, materials and total system cost.

Vicor SM-ChiP packages are compatible with standard pick-and-place assembly processes. The co-molded ChiP package provides enhanced thermal management due to a large thermal interface area and superior thermal conductivity. The high conversion efficiency of the VTM increases overall system efficiency and lowers operating costs compared to conventional approaches.

When powered by a PRM, the VTM enables the utilization of Factorized Power Architecture™, which provides efficiency and size benefits by lowering conversion and distribution losses and promoting high-density point-of-load conversion.

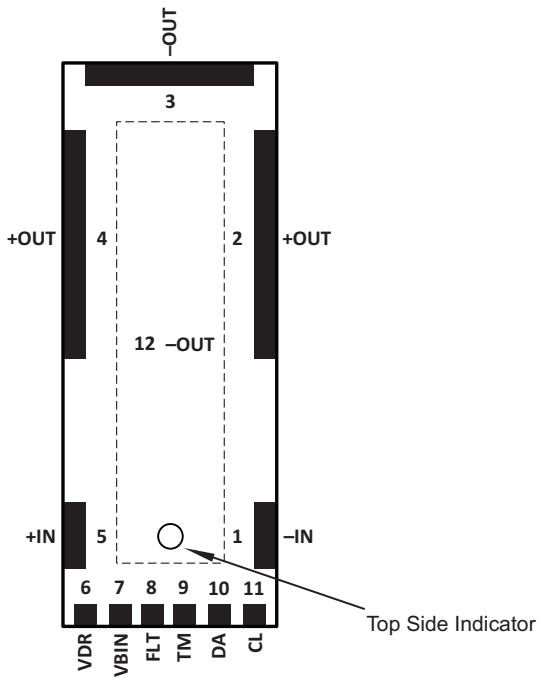
VICOR 1017
VICOR v. DELTA ELECTRONICS
IPR2024-00705

Typical Application



Typical application: Isolated DC-DC PoL converter using Factorized Power Architecture™

Pin Configuration



Pin Descriptions

Signal Name	Pin Number	Type	Description
–IN	1	INPUT POWER RETURN	Negative input power terminal
+OUT	2, 4	OUTPUT POWER	Positive output power terminal
–OUT	3, 12 [a]	OUTPUT POWER RETURN	Negative output power terminal
+IN	5	INPUT POWER	Positive input power terminal
VDR	6	INPUT	Low-voltage bias input, Powertrain controller supply
VBIN	7	NO CONNECT	Factory use only
FLT	8	INPUT / OUTPUT	DISABLE pin; PRM™ SM-ChiP fault management pin
TM	9	OUTPUT	Temperature monitor / Fault Flag
DA	10	No Connect	Factory use only
CL	11	No Connect	Factory use only

[a] Represents product top and bottom conductive, mechanical plating. Reference product outline for additional details.

Part Ordering Information

Part Number	Temperature Grade	Option	Tray Size
VTM2308S60Z1513**T**0**0**	**T** = –40 to 125°C	**0** = None	88 parts per tray

All products shipped in JEDEC standard high-profile (0.400″ thick) trays (JEDEC Publication 95, Design Guide 4.10).

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
VDR to –IN		–0.3	5.5	V_{DC}
FLT to –IN		–0.3	5.5	V_{DC}
TM to –IN		–0.3	5.5	V_{DC}
+IN to –IN		–1.0	75	V_{DC}
+IN / –IN to +OUT / –OUT (Hipot)			2250	V_{DC}
+OUT to –OUT		–1.0	25	V_{DC}

Electrical Specifications

Specifications apply over all line and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade). All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted. Electrical performance data includes VDR bias losses where appropriate.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain						
Input Voltage Range	V_{IN}	VDR applied	**0**[b]		**60**	V_{DC}
V_{IN} Slew Rate	dV_{IN}/dt				**1**	V / µs
No-Load Power Dissipation	P_{NL}	V_{IN} = 48V			**3.1**	W
		V_{IN} = 0 – 60V			**5.2**	
		V_{IN} = 48V		1.6	2.0	
		V_{IN} = 0 – 60V			3.7	
DC Input Current	I_{IN_DC}	Steady state			3.4	A
Transfer Ratio	K	K = V_{OUT} / V_{IN}		**1/4**		V / V
Output Voltage	V_{OUT}	$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{OUT}$, I_{OUT} = 0A	**0**		**15**	V
Output Current (Average)	I_{OUT_AVG}	Steady state			**12.5**	A
Output Current (Peak)	I_{OUT_PK}	t_{PEAK} ≤ 10ms, I_{OUT_AVG} < 12.5A, duty cycle = 25%			**16.7**	A
Output Power (Average)	P_{OUT_AVG}	I_{OUT_AVG} ≤ 12.5A			**187**	W
Efficiency (Ambient)	η_{AMB}	V_{IN} = 48V, I_{OUT} = 12.5A	95	95.6		%
		V_{IN} = 26 – 60V, I_{OUT} = 12.5A	91.4			
		V_{IN} = 48V, I_{OUT} = 6.25A	95.8	96.3		

[b] VTM operation tested at 26V_{IN} minimum. VTM operation guaranteed by design 0 – 26V_{IN}.

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade). All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted. Electrical performance data includes VDR bias losses where appropriate.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain (Cont.)						
Efficiency (Hot)	η_{HOT}	T_{INT} = 100°C, V_{IN} = 48V, I_{OUT} = 12.5A	93.5	94.9		%
Efficiency (Over Load Range)	$\eta_{30\%}$	3.75A < I_{OUT} < 12.5A, V_{IN} = 48V	**92.9**			%
Output Resistance (Cold)	R_{OUT_COLD}	T_{INT} = –40°C, I_{OUT} = 12.5A	17.2	22.8	28.5	mΩ
Output Resistance (Ambient)	R_{OUT_AMB}	T_{INT} = 25°C, I_{OUT} = 12.5A	23.8	30.0	36.1	mΩ
Output Resistance (Hot)	R_{OUT_HOT}	T_{INT} = 100°C, I_{OUT} = 12.5A	25.9	36.7	47.5	mΩ
Switching Frequency	F_{SW}		**1.79**	1.86	**2.00**	MHz
Output Ripple Frequency	F_{SW_RP}		**3.55**	3.72	**4.00**	MHz
Output Voltage Ripple	V_{OUT_PP}	C_{OUT} = 0µF, I_{OUT} = 12.5A, V_{IN} = 48V, 20MHz BW		150	**300**	mV_{P-P}
Output Inductance (Parasitic)	L_{OUT_PAR}	Frequency up to 30MHz, simulated leads model		270		pH
Output Capacitance (Internal)	C_{OUT_INT}	Effective value at $12V_{OUT}$		7		µF
Protection						
Overvoltage Lockout	V_{IN_OVLO+}	VTM latches after fault	61.6	64.8	68	V
Overvoltage Lockout Response Time	t_{OVLO}	Internal digital control		0.5		µs
Output Overcurrent Trip	I_{OCP}	VTM latches after fault	**20**	23	**30**	A
Short Circuit Protection Trip Current	I_{SCP}	VTM latches after fault	20			A
Output Overcurrent Blanking Time	t_{OCP}	Internal digital blanking timer		12		ms
Short Circuit Protection Response Time	t_{SCP}	Duration from detection to cessation of switching, cycle-by-cycle short-circuit detection		0.1		µs
Overtemperature Shut-Down Set Point	T_{OT}		125	135	145	°C
Overtemperature Shut-Down Hysteresis	T_{OT_HYS}			25		°C
Reverse Inrush Current Protection		Reverse inrush protection is enabled for this product				

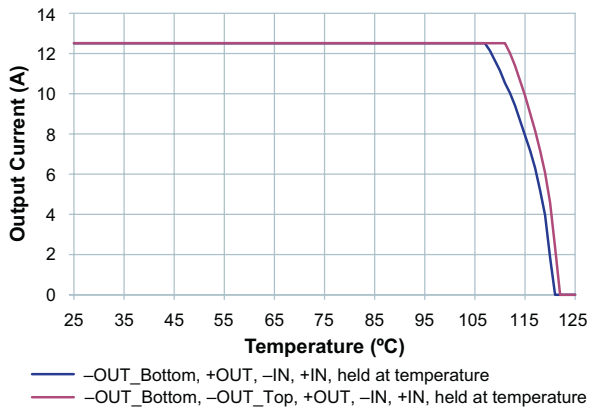


***Figure 1** — Specified thermal operating area, high line, full load*

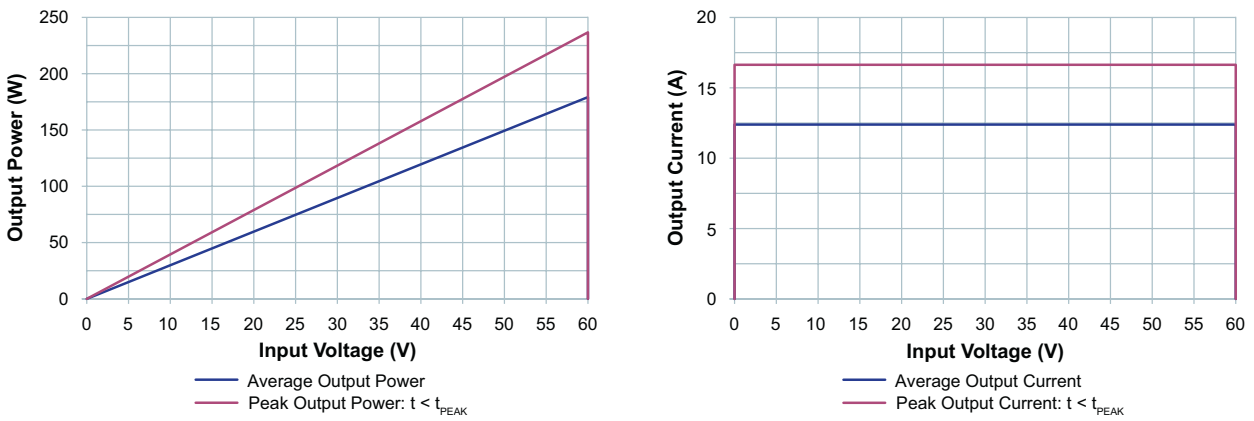


***Figure 2** — Specified electrical operating area, R_{OUT} max hot*

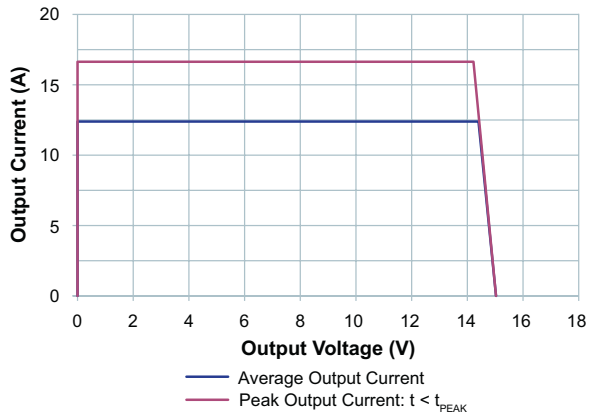


***Figure 3** — Specified electrical operating area*

Signal Characteristics

Specifications apply over all line and load conditions unless otherwise noted; **boldface** specifications apply over the temperature range of –40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade). All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted. Electrical performance data includes VDR bias losses where appropriate.

VTM Driver Supply: VDR

- Used to wake up internal control circuitry.
- VDR voltage must be continuously applied and must be within specified limit for proper operation.

Signal Type	State	Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Analog Input	Steady	VDR Voltage (External)	V_{VDR_EXT}		**4.85**		**5.35**	V
		VDR Current Draw	I_{VDR}	VDR = 5.1V, V_{IN} = 48V, T_{INT} = 100°C		99	**116**	mA
				Fault mode. VDR > 4.85V		23		
	Start Up	VDR Inrush Current	I_{INR_VDR}	VDR = 5.35V, dVDR / dt = 1V/µs			**2**	A
	Transitional	VDR to TM Turn-On Delay	t_{ON}	V_{IN} = 0V, FLT floating, VDR applied, C_{FLT} = 0µF	23	28	**34**	ms
		VDR to FLT Delay	t_{VDR_FLT}	VDR = 4.85V to FLT high, V_{IN} = 0V, dVDR / dt = 1V/µs		0.2	**0.3**	ms
		VDR Capacitance (Internal)	C_{VDR_INT}	VDR = 0V		2.2		µF

Fault Management: FLT

- The FLT pin disables the VTM module. When held below 1V, the VTM module will be disabled.
- FLT pin outputs 4.7V minimum during normal operation. FLT pin is equal to 0V minimum during fault mode given VDR > 4.85V and floating FLT pin.
- Module will shut down when pulled low with an impedance less than 25kΩ.
- A 100pF maximum filtering capacitor can be used on this pin.

Signal Type	State	Attribute	Symbol	Conditions / notes	Min	Typ	Max	Unit
Analog Output	Steady	FLT Voltage	V_{FLT}			5		V
		FLT Source Current	I_{FLT_OP}				**10**	µA
	Start Up	FLT Source Current	I_{FLT_EN}				**10**	µA
Digital Input/ Output	Enable	FLT Voltage	V_{FLT_EN}			3	**4**	V
	Disable	FLT Voltage (Disable)	V_{FLT_DIS}		**1**	**2**		V
		FLT Resistance (External)	R_{FLT_EXT}	Connected to –IN. Min value to guarantee start up (open circuit OK), FLT > 4V	**1600**			kΩ
		FLT Sink Capability	I_{FLT_SINK}	Fault State	**1**			mA

Temperature Monitor: TM

- The TM pin monitors the internal temperature of the VTM controller IC within an accuracy of ±5°C.
- Can be used as a "Power Good" flag to verify VTM module operation.
- The TM pin has a room temperature setpoint of 3V and approximate gain of 10mV/K.
- Output drives Temperature Shut-down comparator.

Signal Type	State	Attribute	Symbol	Conditions / notes	Min	Typ	Max	Unit
Analog Output	Steady	TM Voltage	V_{TM}	T_{INT} controller = 27°C, I_{TM} < 100µA	2.85	3	3.15	V
		TM Source Current	I_{TM}				**100**	µA
		TM Gain	A_{TM}			10		mV/K
		TM Voltage Ripple	V_{TM_PP}	C_{TM} = 0F, V_{IN} = 48V, I_{OUT} = 12.5A		150	**350**	mV
Digital Output (Fault Flag)	Steady	TM Disable Voltage	V_{TM_DIS}	PGOOD deasserted		0.2		V
		TM Enable Source Current	I_{TM_FLT}	V_{TM} > 1V	20			mA
		TM Fault Sink Current	I_{TM_FAULT}	V_{TM} ≤ 0.1V, Fault state	1			mA
	Transitional	TM Capacitance (External)	C_{TM_EXT}				**100**	pF
		TM Fault Response Time	t_{FR_TM}	From fault detection to TM driven low		0.02		µs

Application Characteristics

The following values are typical of an application environment. Electrical performance data includes VDR bias losses where appropriate. See associated figures for general trend data.

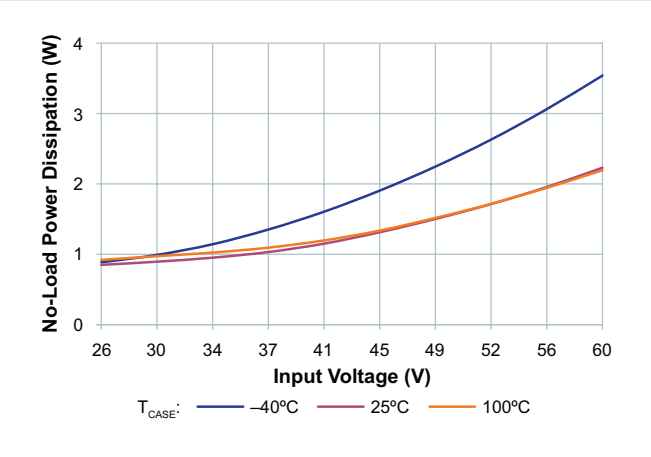


***Figure 4** — No-load power dissipation vs. input voltage*

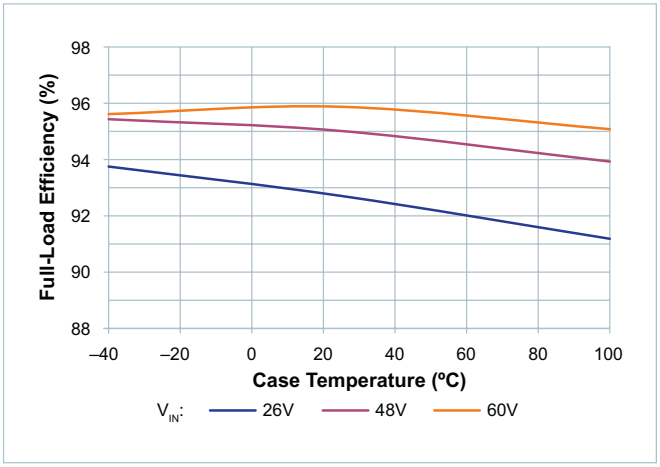


***Figure 5** — Full-load efficiency vs. case temperature*

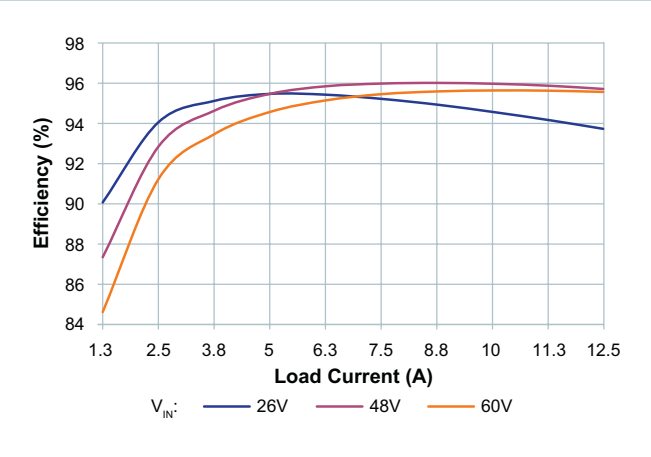


***Figure 6** — Efficiency at –40°C case temperature*

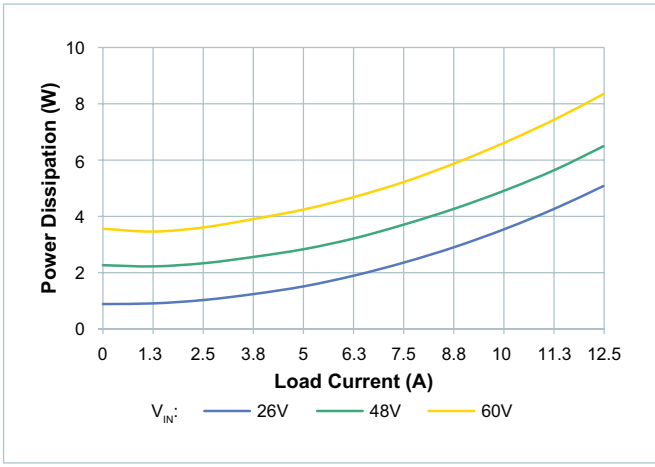


***Figure 7** — Power dissipation at –40°C case temperature*

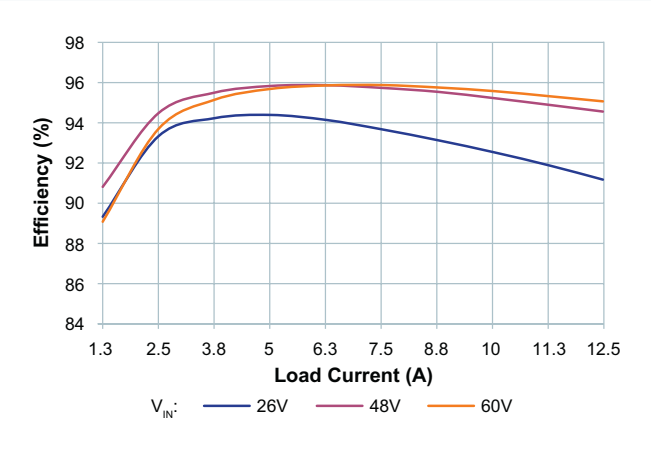


***Figure 8** — Efficiency at 25°C case temperature*

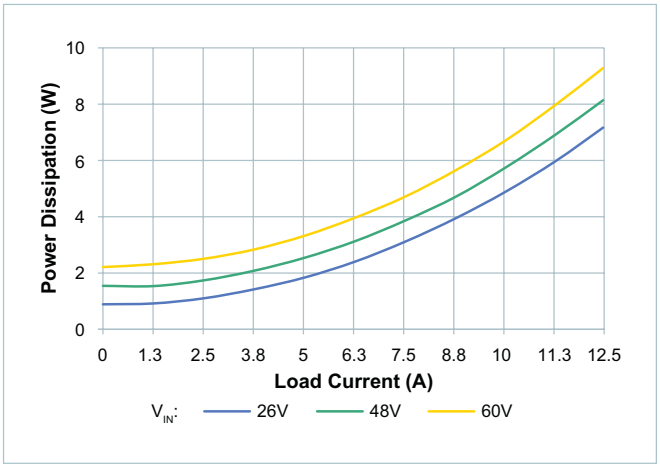


***Figure 9** — Power dissipation at 25°C case temperature*

Application Characteristics (Cont.)

The following values are typical of an application environment. Electrical performance data includes VDR bias losses where appropriate.
See associated figures for general trend data.

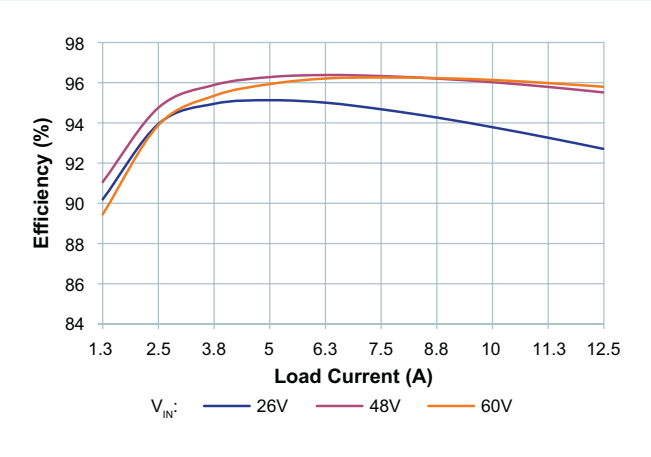


Figure 10 *— Efficiency at 100°C case temperature*

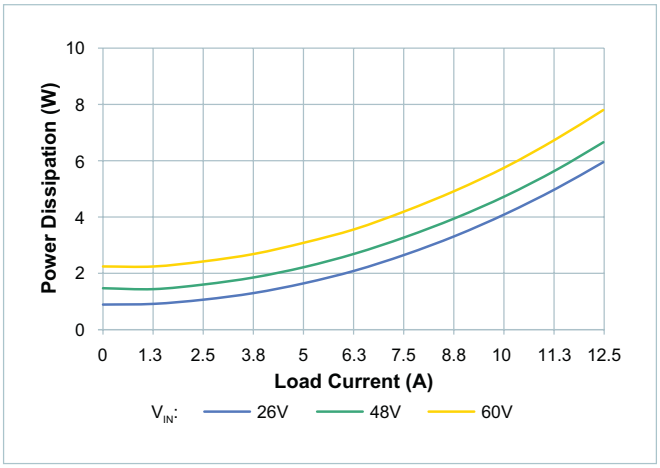


Figure 11 *— Power dissipation at 100°C case temperature*

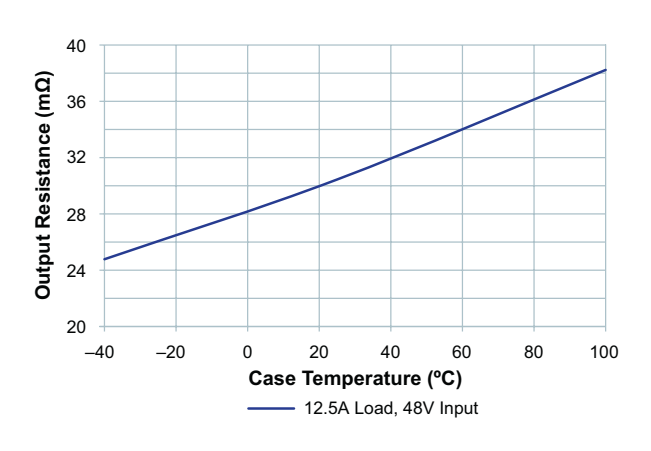


Figure 12 *— Output resistance (R_{OUT}) vs. case temperature at nominal input voltage*

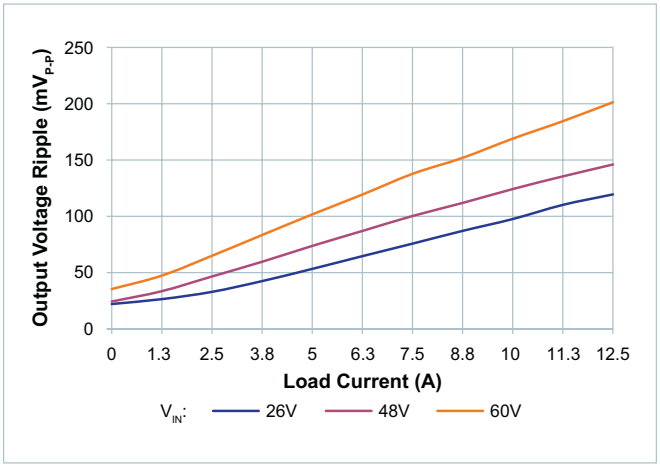


Figure 13 *— Output voltage ripple (V_{RIPPLE}) vs. load (I_{OUT}); no external C_{OUT}.*

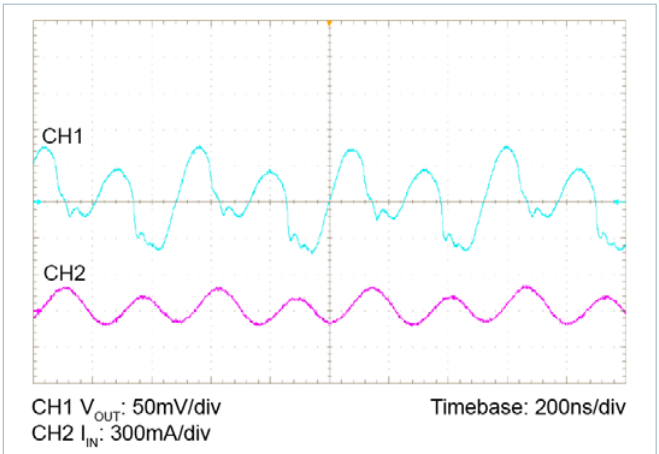


Figure 14 *— Full-load ripple, 100µF C_{IN}; no external C_{OUT}.*

General Characteristics

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Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L		22.7 [0.894]	22.83 [0.899]	22.96 [0.904]	mm [in]
Width	W		8.39 [0.33]	8.52 [0.335]	8.65 [0.34]	mm [in]
Height	H		4.775 [0.188]	4.9 [0.193]	5.025 [0.198]	mm [in]
Volume	Vol	No heat sink		0.953 [0.058]		cm^3 [in^3]
Weight	W			3.670 [0.1295]		g [oz]
Exterior Package Plating		Nickel	3		6	µm
		Gold	0.08		0.2	
Thermal						
Operating Temperature	T_{INT}	T-Grade	–40		125	°C
Thermal Capacity				2.5		Ws / °C
Assembly						
Peak Compressive Force Applied to Case (Z-Axis)					5	lbs
					16.6	lbs / in^2
Storage Temperature	T_{ST}	T-Grade	–55		125	°C
ESD Withstand	ESD_{HBM}	Human Body Model, (JEDEC JS-001-2012 Table 2B) Class 1C	2000			V_{DC}
	ESD_{CDM}	Charge Device Model, (JESD22-C101E) Class III	500			
Soldering						
Peak Temperature During Reflow		MSL 4			245	°C
Safety						
Isolation Voltage (Hipot)	V_{HIPOT}		2250			V
Isolation Capacitance	C_{IN_OUT}	Unpowered unit measured at 1MHz		370		pF
Isolation Resistance	R_{IN_OUT}	Measured at 500V_{DC}	10			MΩ
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		10		MHrs
		Telcordia Issue 2 - Method I Case III; Ground Benign, Controlled		23.1		MHrs
Agency Approvals / Standards		cURus, UL 60950-1				
		cTÜVus, EN 60950-1				
		UKCA, electrical equipment (safety) regulations				
		CE marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

Using the Control Signals VDR, EN, FLT, TM

VDR: The VTM VDR Supply

This pin is an input pin which powers the internal bias circuit within the specified voltage range.

Some additional notes on using the VDR pin:

- The VDR voltage must be applied indefinitely allowing for continuous operation for entire input voltage range of VTM.
- The fault response of the VTM module is latching. Recycle of input voltage in presence of VDR is required in order to restart the unit, provided the FLT and EN pins are floating.

FLT: Fault Management

This pin can be used to accomplish the following functions:

- *VTM output disable:* FLT pin can be actively pulled down in order to disable the module. The pull down resistance shall be lower than 25kΩ. The FLT voltage should be lower than the minimum disable threshold as specified in signal characteristics in order to keep the VTM off.
- *VTM start up:* VTM will start up after FLT signal crosses its maximum undervoltage threshold point. In order to guarantee VTM start up, resistance applied from FLT pin to ground must exceed the minimum external resistance as specified in signal characteristics.
- *VTM start up after FLT pulled low:* Disabling the VTM by pulling the FLT pin of the VTM low is latching. Recycling the input voltage in presence of VDR is required in order to restart the VTM, provided the EN pin is floating.
- *VTMs array fault shut down:* In an array, the FLT pin of VTMs should be tied together. In the case of a fault on one of the VTMs, the FLT pin of VTM under fault can pull the common FLT signal low and shut the VTM array off.
- *VTMs array start up:* In an array, FLT signal can be used as a Power Good/Ready signal to apply the input voltage to the VTM. The FLT signal should be above maximum enable threshold voltage to ensure all VTMs in the array are ready.

TM: Temperature Monitor

This pin provides a voltage proportional to the absolute temperature of the converter control IC.

It can be used to accomplish the following functions:

- *Monitor the control IC temperature:* The temperature in Kelvin is equal to the voltage on the TM pin scaled by 100 (i.e., 3.0V = 300K = 27°C). If a heat sink is applied, TM can be used to thermally protect the system.
- *Fault detection flag:* The TM voltage source is internally turned off as soon as a fault is detected. For system monitoring purposes (microcontroller interface) faults are detected on falling edges of TM signal.
- *VTMs array start up:* In an array, TM signal can be used as a Power Good/Ready signal to apply the input voltage to the VTM. The TM signal of all VTMs should be high to ensure all VTMs in the array are ready.

VTM Start Up

The VTM module is designed to operate with an upstream PRM™. Start-up and fault-retry control is primarily managed by the regulator. Soft start is achieved by the PRM output voltage ramp up typically proportional to the internal or external slew rate of the feedback loop reference voltage. (Figure 15)

The VTM input voltage slew rate is the only means to control the inrush current through the VTM into a large VTM output capacitive load.

To start the VTM apply bias voltage to VDR pin. VDR voltage must be applied first to wake up the internal controller. Input voltage, output voltage and overtemperature are all checked prior to powertrain operation. Once faults are checked and only if all faults are cleared the controller initiates the powertrain within a time period specified by t_{ON} (see VDR Signal Characteristics).

- A VTM input greater than 1.25V prior to applying a bias voltage is not recommended. Permanent module damage may occur or the module may fail to start.
- A VTM output voltage prior or during a start-up check triggers a reverse inrush protection mode that is cleared a few powertrain cycles after VTM input voltage exceeds the equivalent pre-applied output voltage with respect to the VTM K factor.

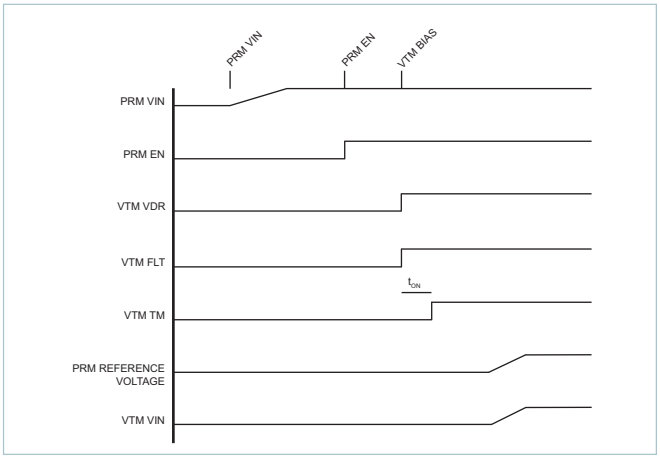


***Figure 15** — VTM start up*

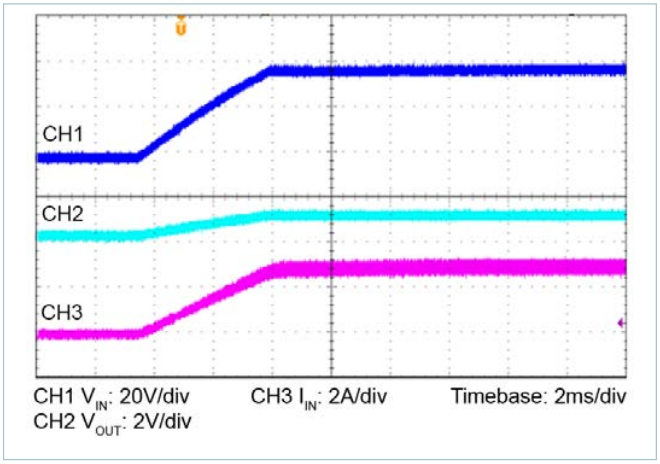


***Figure 16** — Typical VTM start up*

VTM Fault Response

A fault event such as: input or output overvoltage, overtemperature, or FLT pin externally driven low to disable the module triggers a VTM latching shut-down condition. A low VTM V_{IN} state less than 1.25V or a VDR (5V) recycle is required to clear the fault latch when reapplying VDR. If V_{IN} is ≥1.25V, the module will latch. The powertrain will resume or restart switching only if the fault trigger is not persistent. Typically the TM pin through a 10kΩ is used to hold the PRM EN low until the VTM faults clear. Once the VTM fault is cleared, the system is allowed to reset by first allowing the PRM EN followed by a reference soft start and VTM V_{IN} ramp up. It is also possible to connect PRM FLT to VTM FLT to manage interoperability.

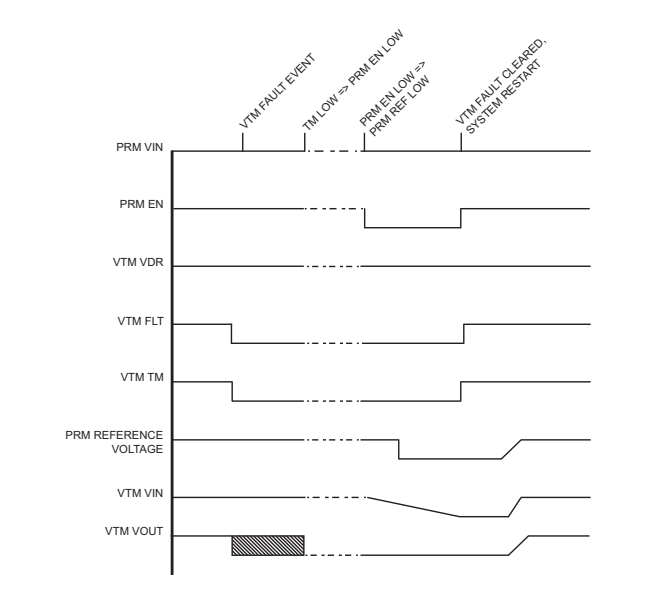


Figure 17 — *VTM fault response*

Protection

The VTM relies heavily on the upstream PRM and/or system controller for protection from many abnormal events. The designer should insure that the complete system provides the VTM with adequate short circuit and output overcurrent protection. Using a validated reference design is a way to be assured that the VTM is appropriately protected at a system level. For assistance in selecting and implementing a complete reference design, please consult with Vicor Applications Engineering.

Sine Amplitude Converter Point-of-Load Conversion

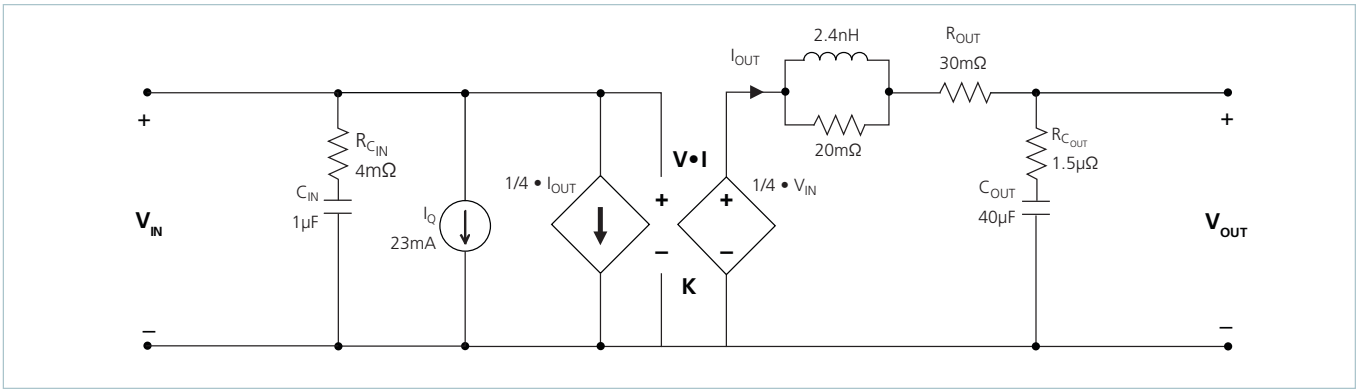


Figure 18 — *Sine Amplitude Converter AC model*

The Sine Amplitude Converter (SAC™) uses a high frequency resonant tank to move energy from input to output. (The resonant tank is formed by Cr and leakage inductance Lr in the power transformer windings as shown in the VTM Module Block Diagram). The resonant LC tank, operated at high frequency, is amplitude modulated as a function of input voltage and output current. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving power density.

The SAC can be simplified into the following model:

At no load:

$$V_{OUT} = V_{IN} \bullet K \qquad (1)$$

K represents the "turns ratio" of the SAC.
Rearranging Equation 1:

$$K = \frac{V_{OUT}}{V_{IN}} \qquad (2)$$

In the presence of load, V_{OUT} can be approximated as:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{OUT} \qquad (3)$$

and I_{OUT} can be approximated as:

$$I_{OUT} = \frac{I_{IN} - I_Q}{K} \qquad (4)$$

R_{OUT} represents the impedance of the SAC, and is a function of the R_{DSON} of the input and output MOSFETs and the winding resistance of the power transformer. I_Q represents the quiescent current of the SAC control and gate drive circuitry.

The use of DC voltage transformation provides additional interesting attributes. Consider an idealized SAC with K = 1/40, R_{OUT} = 0Ω and I_Q = 0A. Equation 3 now becomes Equation 1 and is essentially load independent. In this example, resistor R is now placed in series with V_{IN} as shown in Figure 19.

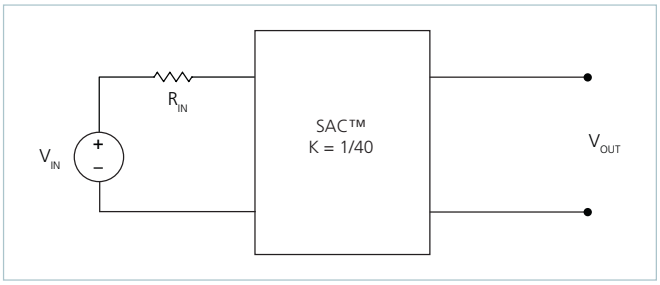


Figure 19 — *Sine Amplitude Converter with series input resistor*

The relationship between V_{IN} and V_{OUT} becomes:

$$V_{OUT} = (V_{IN} - I_{IN} \bullet R_{IN}) \bullet K \qquad (5)$$

Substituting the simplified version of Equation 4 (I_Q is assumed = 0A) into Equation 5 yields:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{IN} \bullet K^2 \qquad (6)$$

This is similar in form to Equation 3, where R_{OUT} is used to represent the characteristic impedance of the SAC™. However, in this case a real R on the input side of the SAC is effectively scaled by K^2 with respect to the output.

Assuming that R = 1Ω, the effective R as seen from the secondary side is 0.62mΩ, with K = 1/40 as shown in Figure 19.

A similar exercise should be performed with the addition of a capacitor or shunt impedance at the input to the SAC. A switch in series with V_{IN} is added to the circuit. This is depicted in Figure 20.

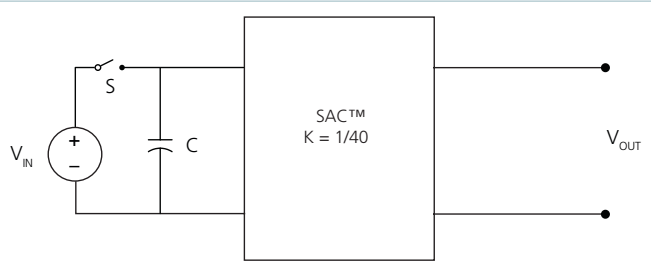


Figure 20 *— Sine Amplitude Converter with input capacitor*

A change in V_{IN} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\,\frac{dV_{IN}}{dt} \qquad (7)$$

Assume that with the capacitor charged to V_{IN}, the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{OUT} \bullet K \qquad (8)$$

Substituting Equation 1 and 8 into Equation 7 reveals:

$$I_{OUT} = \frac{C}{K^2} \bullet \frac{dV_{OUT}}{dt} \qquad (9)$$

The equation in terms of the output has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity, results in an effectively larger capacitance on the output when expressed in terms of the input. With a K = 1/40 as shown in Figure 23, C = 1µF would appear as C = 1600µF when viewed from the output.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, the benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low, i.e., well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low-loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the VTM module are:

- No load power dissipation (P_{NL}): defined as the power used to power up the module with an enabled powertrain at no load. It includes the components due to input voltage and VDR voltage.
- Resistive loss (R_{OUT}): refers to the power loss across the VTM module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{NL} + P_{R_{OUT}} \qquad (10)$$

Therefore,

$$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{R_{OUT}} \qquad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{R_{OUT}}}{P_{IN}} \qquad (12)$$

$$= \frac{V_{IN} \bullet I_{IN} - P_{NL} - (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}$$

$$= 1 - \left(\frac{P_{NL} + (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}\right)$$

Open Loop Transient Performance of a Sine Amplitude Converter

The VTM package provides very low parasitic inductance on both the input and output connections. This combined with the use of a high frequency Sine Amplitude Converter topology results in a very low input to output impedance characteristic for the VTM. This low impedance is approximately between 1.2 and 1.5 times R_{OUT} from DC to approximately 1MHz. This yields significant benefits in transient performance by effectively presenting upstream capacitive energy storage at the output of the VTM will very little intervening impedance. This can be illustrated in the following way. Figure 21 shows a test circuit that applies a 130A load step to a VTM with a K = 1/40. An array of MOSFETs ($Q1_{ARRAY}$) is gated by a function generator to provide a current pulse with a <5µs rise time. The actual output current is measured using R_{SENSE}.

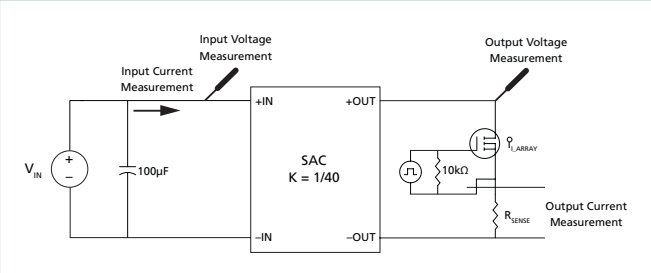


Figure 21 — *Sine Amplitude Converter with input capacitor*

The response of the VTM to a 0 – 100% load step can be seen in Figure 22 and the VTM response to a 100 – 0% load step can be seen in Figure 23. There are several important characteristics to note concerning the VTM transient response.

1. The VTM shows a "current multiplier" characteristic where the input and output current are proportional. The input current to the VTM reaches the steady state value within a few switching cycles (~400ns).

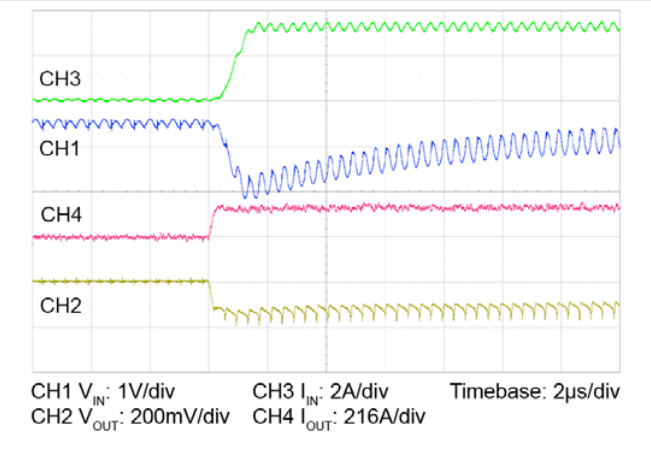


Figure 22 — *VTM (K = 1/40) response to 0 – 100% (0 – 130A) load step*

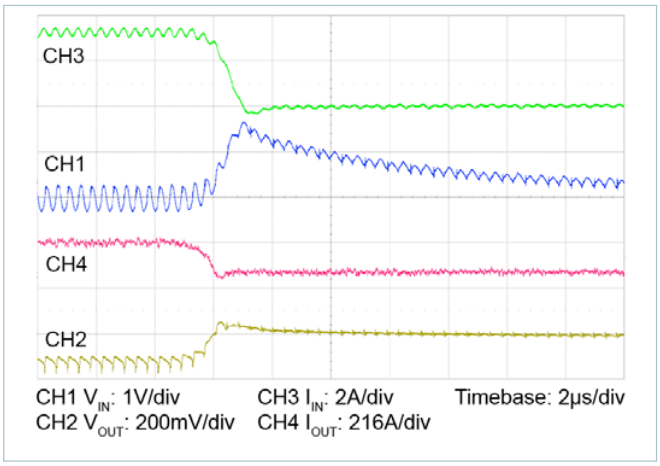


Figure 23 — *VTM (K = 1/40) response to a 100 – 0% (130 – 0A) load step*

2. The input power supply response is reflected directly to the output of the VTM. The input supply settles within 12µs of the load step and the voltage settling waveform can be clearly seen on the output, scaled by the K factor.

3. The output voltage of the VTM drops in proportion to the output load current. This V_{OUT} drop can be expressed as:

$$\Delta V_{OUT} = \delta \bullet R_{OUT} \bullet \Delta I_{OUT} \qquad (13)$$

In this equation R_{OUT} is the output resistance as specified in the datasheet and δ is a scaling factor to compensate for higher order terms in the $V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{OUT}$ equation. δ is typically between 1.2 and 1.5 and varies based on the model of VTM and the size of the load step.

As a result of these key characteristics in the VTM response, capacitance with ESR >> R_{OUT} and ESL >> L_{OUT_PAR} located at the output of the VTM will not contribute significantly to the transient response of a system. The VTM effectively unburdens the system from needing bypass capacitance for frequency response below 1MHz, leaving only the >1MHz component to require filtering at the point of load.

Input and Output Filter Design

A major advantage of a SAC™ system versus a conventional PWM converter is that the former does not require large functional filters. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of input voltage and output current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving high power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- *Guarantee low source impedance:*

  To take full advantage of the VTM current multiplier dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5MHz. Input capacitance may be added to improve transient performance or compensate for high source impedance.

- *Further reduce input and/or output voltage ripple without sacrificing dynamic response:*

  Given the wide bandwidth of the VTM module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the VTM module multiplied by its K factor.

- *Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and cause failures:*

  The module input/output voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even when disabled, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it.

  Common mode sensitive applications may require an external bypass capacitor from –IN to –OUT. The common mode voltage can be approximated to be $V_{IN} \bullet K \bullet (2)^{-1/2}$. Generally a series stacked ceramic capacitor with a typical value of 5400pF is found to effectively reduce this noise.

Capacitive Filtering Considerations for a Sine Amplitude Converter

It is important to consider the impact of adding input and output capacitance to a Sine Amplitude Converter on the system as a whole. Both the capacitance value and the effective impedance of the capacitor must be considered.

A Sine Amplitude Converter has a DC R_{OUT} value which has already been discussed. The AC R_{OUT} of the SAC contains several terms:

- Resonant tank impedance
- Input lead inductance and internal capacitance
- Output lead inductance and internal capacitance

The values of these terms are shown in the behavioral mode. It is important to note on which side of the transformer these impedances appear and how they reflect across the transformer given the K factor.

The overall AC impedance varies from model to model. For most models it is dominated by DC R_{OUT} value from DC to beyond 500kHz. The behavioral model should be used to approximate the AC impedance of the specific model.

Any capacitors placed at the output of the VTM reflect back to the input of the VTM module by the square of the K factor (Equation 9) with the impedance of the VTM module appearing in series. It is very important to keep this in mind when using a PRM™ regulator to power the VTM module. Most PRM modules have a limit on the maximum amount of capacitance that can be applied to the output. This capacitance includes both the PRM output capacitance and the VTM module output capacitance reflected back to the input. In PRM remote sense applications, it is important to consider the reflected value of VTM module output capacitance when designing and compensating the PRM control loop.

Capacitance placed at the input of the VTM module appear to the load reflected by the K factor with the impedance of the VTM module in series. In step-down ratios, the effective capacitance is increased by the K factor. The effective ESR of the capacitor is decreased by the square of the K factor, but the impedance of the module appears in series. Still, in most step-down VTM modules an electrolytic capacitor placed at the input of the module will have a lower effective impedance compared to an electrolytic capacitor placed at the output. This is important to consider when placing capacitors at the output of the module. Even though the capacitor may be placed at the output, the majority of the AC current will be sourced from the lower impedance, which in most cases will be the module. This should be studied carefully in any system design using a module. In most cases, it should be clear that electrolytic output capacitors are not necessary to design a stable, well-bypassed system.

Current Sharing

The SAC™ topology bases its performance on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal current multiplier with some resistive drop and positive temperature coefficient.

This type of characteristic is close to the impedance characteristic of a DC power distribution system, both in behavior (AC dynamic) and absolute value (DC dynamic).

When connected in an array with the same K factor, the VTM module will inherently share the load current (typically 5%) with parallel units according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide the PCB layout as symmetric as possible.
- Apply same input / output filters (if present) to each unit.

For further details see:
AN:016 Using BCM® Bus Converters in High Power Arrays.

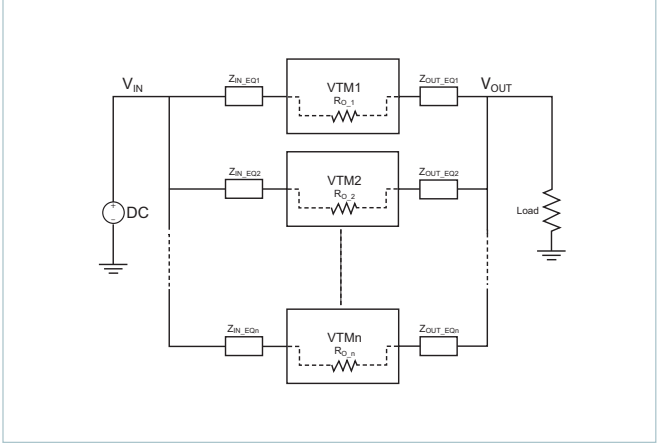


***Figure 24** — VTM current multiplier array*

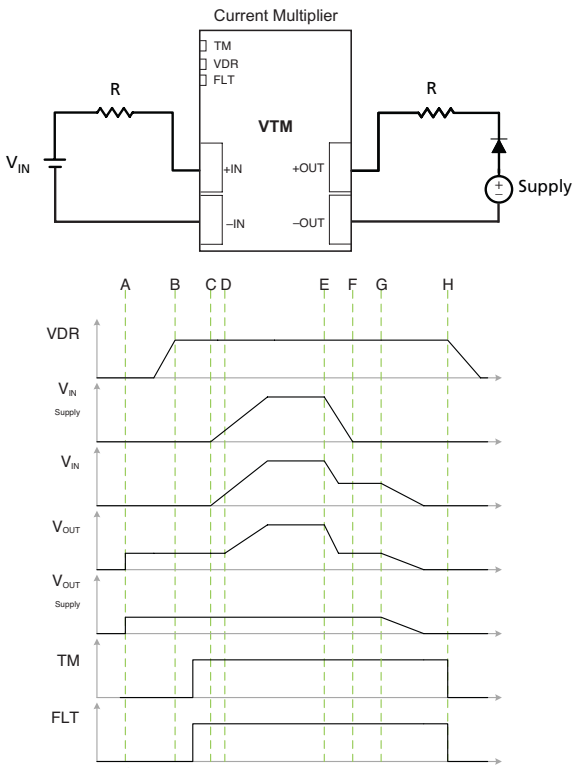
Fuse Selection

The VTM is not internally fused, see safety approvals for required fusing.

Reverse Inrush Current Protection

The VTM provides reverse inrush protection which prevents reverse current flow until the input voltage is high enough to first establish current flow in the forward direction. In the event that there is a DC voltage present on the output before the VTM module is powered up, this feature protects sensitive loads from excessive dV/dt during power up as shown in Figure 25.

If a voltage is present at the output of the VTM module which satisfies the condition $V_{OUT} > V_{IN} \bullet K$ after a successful power up the energy will be transferred from secondary to primary. The input to output ratio of the VTM module will be maintained. The VTM module will continue to operate in reverse as long as the input and output voltages are within the specified range. The VTM has not been qualified for continuous reverse operation.



A: V_{OUT} supply > 0V
B: VDR to –IN > 4.85V controller wakes up, FLT pulled high, reverse inrush protection blocks V_{OUT} supplying V_{IN}
C: V_{IN} supply ramps up
D: $V_{IN} > V_{OUT}/K$, powertrain starts in normal mode
E: V_{IN} supply ramps down
F: $V_{IN} > V_{OUT}/K$, powertrain transfers reverse energy
G: V_{OUT} ramps down, V_{IN} follows
H: VDR turns off

***Figure 25** — Reverse inrush protection*

Thermal Design

Figure 26 shows a thermal impedance model that can estimate the maximum temperature of the highest temperature component for a given operating condition (T_{INT}). T_{INT} must be within the specified operating temperature grade of the product. Use of non-conductive TIM (Thermal Interface Material) is required to prevent shorting conductive surfaces on case. Thermal model (a) and (b) below represent similar cooling conditions shown in Figure 1.

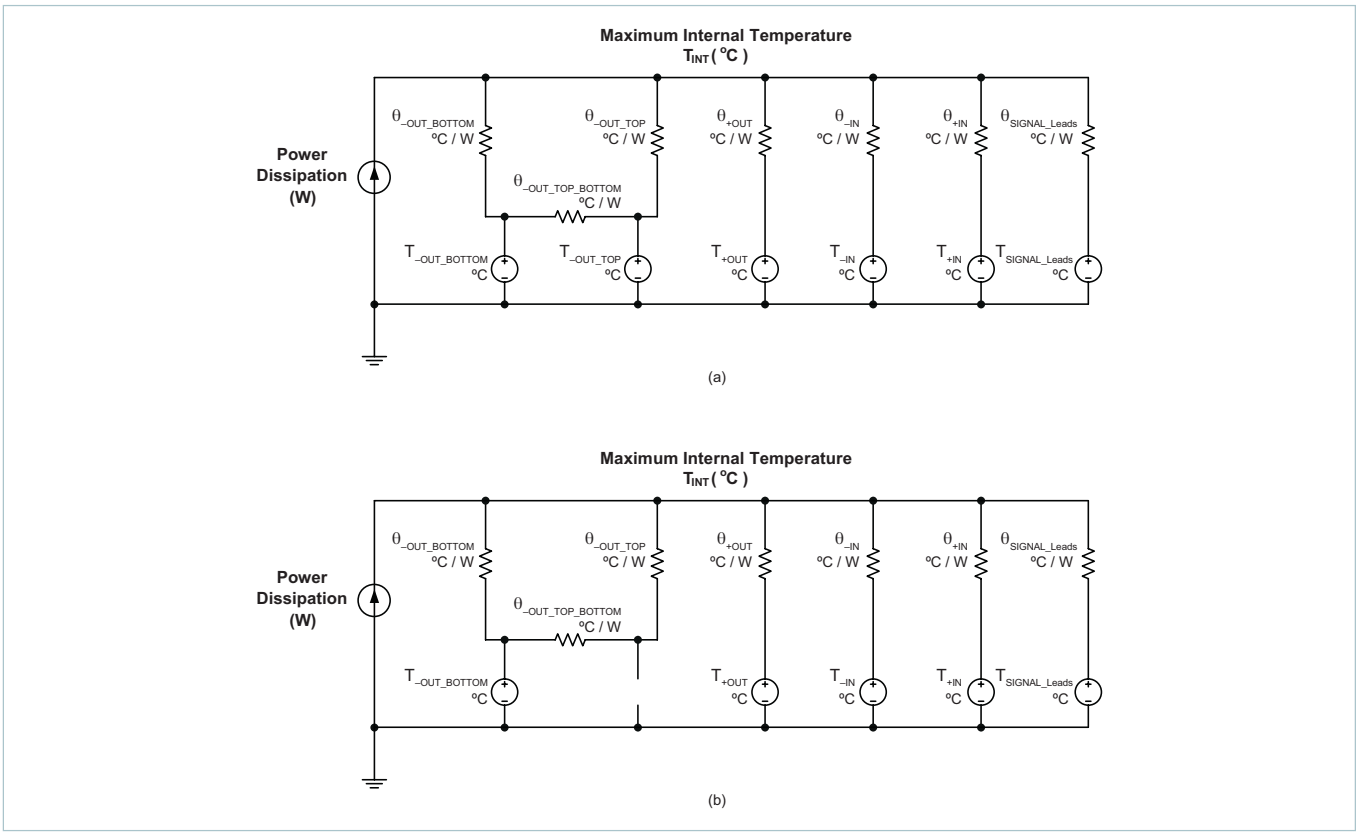


Figure 26 — *Thermal circuit model*

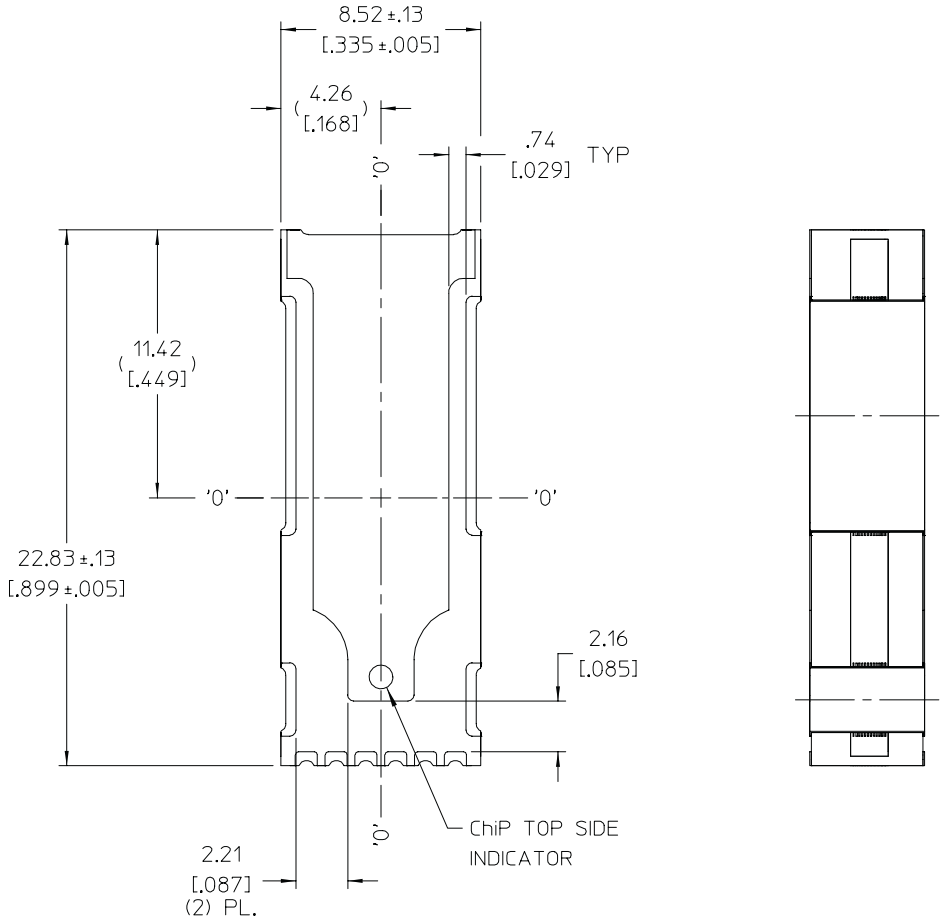
Where the symbol in Figure 27 is defined as the following:

θ_{-OUT_BOTTOM}	is defined as the thermal resistance from the maximum internal temperature to the –OUT thermal pads and –OUT pads shown on the recommended land pattern.
θ_{-OUT_TOP}	is defined as the thermal resistance from the maximum internal temperature to the –OUT copper on top of the VTM.
$\theta_{-OUT_TOP_BOTTOM}$	is defined as the thermal resistance from the –OUT_TOP to the –OUT_BOTTOM.
θ_{+OUT}	is defined as the thermal resistance from the maximum internal temperature to the +OUT pads shown on the recommended land pattern.
θ_{-IN}	is defined as the thermal resistance from the maximum internal temperature to the –IN pads shown on the recommended land pattern.
θ_{+IN}	is defined as the thermal resistance from the maximum internal temperature to the +IN pads shown on the recommended land pattern.
θ_{SIGNAL_Leads}	is defined as the thermal resistance from the maximum internal temperature to the SIGNAL_Leads pads shown on the recommended land pattern.

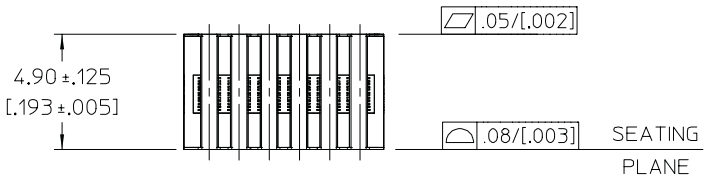
Thermal Impedance						
θ_{-OUT_BOT} (°C / W)	θ_{-OUT_TOP} (°C / W)	$\theta_{-OUT_TOP_BOTTOM}$ (°C / W)	θ_{+OUT} (°C / W)	θ_{-IN} (°C / W)	θ_{+IN} (°C / W)	θ_{SIGNAL_Leads} (°C / W)
3.8	5.6	15	12	39	44	85

Table 1 — *Thermal impedance*

Product Outline Drawing – Top View

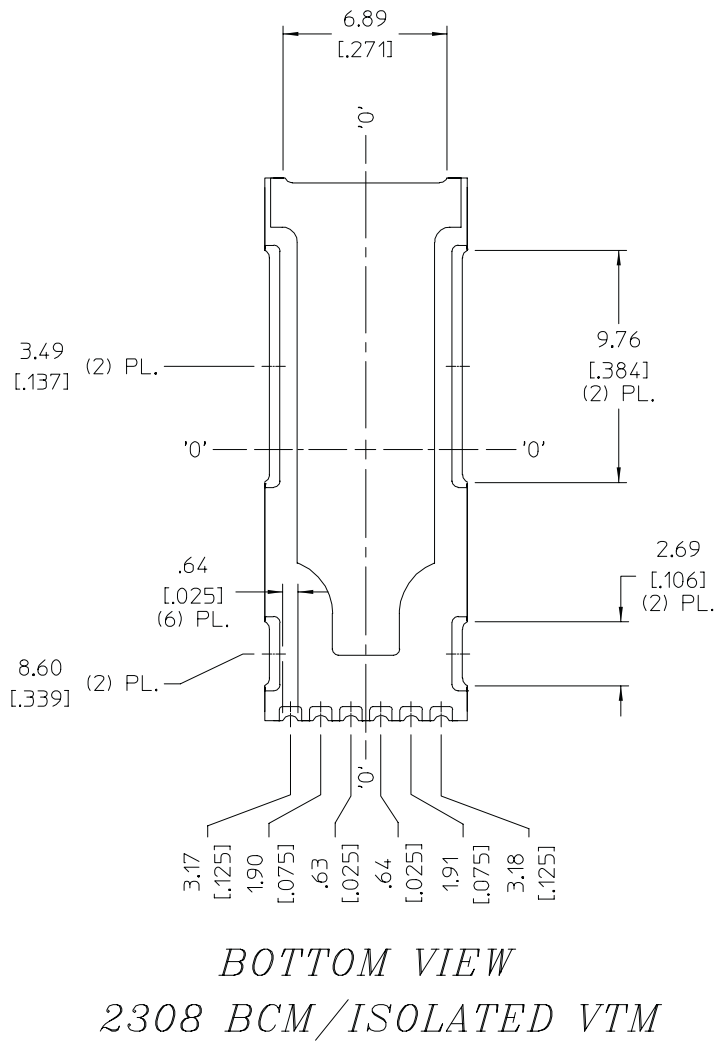


TOP VIEW (COMPONENT SIDE)
2308 BCM/ISOLATED VTM

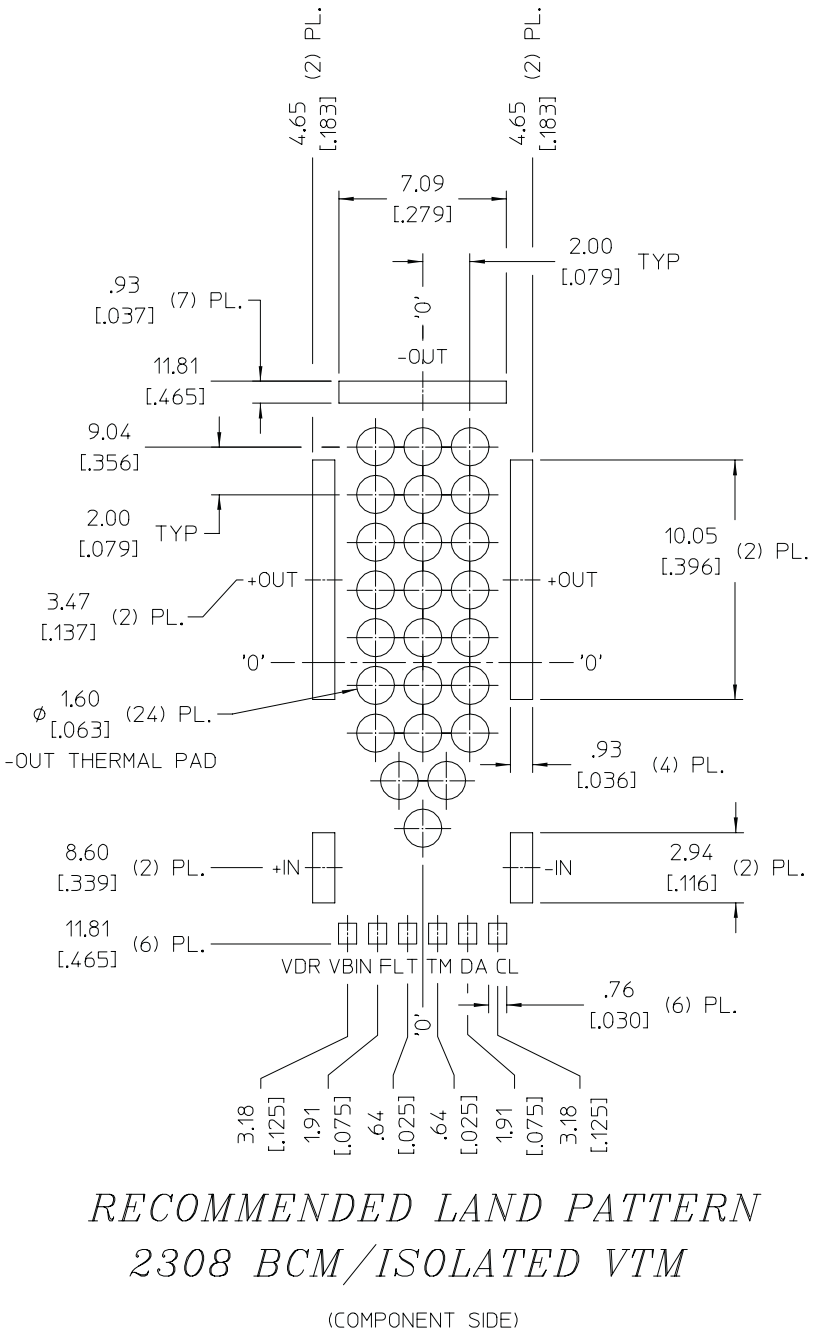


UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE MM [INCH]

Product Outline Drawing – Bottom View



Recommended Land Pattern



–OUT Thermal Pad: Must be copper-defined pads if part is water washed post assembly. Otherwise, if no-clean solder flux is used during assembly, thermal pads may be solder-mask-defined openings.

Revision History

Revision	Date	Description	Page Number(s)
1.0	02/27/19	Initial release	n/a
1.1	05/03/19	Updated absolute max rating (+OUT to –OUT)	4
1.2	02/05/20	Updated isolation resistance specification	11
1.3	06/15/20	Internal bias function removed; VBIN pin is made a "No Connect" pin	2, 3, 4, 7, 11
1.4	02/07/22	Revised agency approvals	1, 10
1.5	12/01/22	Clarified overtemperature fault	5
1.6	10/13/23	Revised minimum ambient efficiency at 12.5A Revised overcurrent trip typical and max Revised VDR current draw max	4 5 7

Note: page removed in Rev 1.3

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Vicor Corporation
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715
www.vicorpower.com

email
Customer Service: custserv@vicorpower.com
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