

RFICs for Reduced Size, Cost and Power Consumption in Handheld Wireless Transceivers

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Abstract

The high volume potential of existing and proposed wireless Personal Communications Systems in the 800-2500 MHz frequency range presents tremendous challenges and opportunities to designers and suppliers of RFICs. Amplifiers, oscillators, frequency converters and synthesizers are now required to operate from lower supply voltages, consume less current and reduce their physical size while meeting aggressive targets for performance, quality, cost and uniformity. This paper describes Silicon Bipolar and GaAs RFIC process technologies which are particularly well suited to this market. Furthermore, the roles of existing and future RFICs, hybrid modules and discrete devices for a typical RF system architecture in a half-duplex digital radio are discussed. Some key technical constraints that impact the performance of RFIC components at supply voltages of 3V or less are also illustrated in detail.

Introduction

Wireless communication systems for voice and data are expected to experience exponential growth throughout this decade. Example systems in the 800-2500 MHz frequency range currently include AMPS, NADC, JDC, GSM, DCS-1800, CT2, DECT and PHP. One common denominator for mass consumer success in all of these systems is the availability of cost effective portable terminals. Consumers demand hand-portable terminals that are inexpensive, easy to operate, small, lightweight, and reliable. They also require good voice quality, personal privacy and operation for long periods of time without battery recharging or replacement. Terminal manufacturers will inevitably differentiate their products by focusing on some or all of these attributes. For a given system with its attendant constraints for type certification, optimization of hand-portable terminal performance is highly dependent on the available components.

Part of the current trend towards smaller and lighter terminals includes reducing the number of battery cells. For most CMOS baseband processing components, power dissipation is proportional to the square of the supply voltage. Thus although total energy storage in the terminal decreases linearly with the reduction in the number of cell, the discharge time with respect to the baseband CMOS ICs can actually increase at lower supply voltages. Unfortunately, the same trend does not apply to most of the RF semiconductor functions. In fact, the current trend to lower voltages in wireless terminals creates major challenges for RF semiconductor suppliers. This paper will discuss several technical problems in the design of RFICs at supply voltages of 3V or less.

Considerable debate has existed in recent years over the roles of competing RF semiconductor technologies for applications in the 800-2500 MHz frequency range. For example, within Hewlett-

Packard, RFIC designers can select from three different high frequency silicon bipolar processes, a high speed BiCMOS process, and several GaAs processes including an ultra-low noise GaAs PHEMT IC process, an Heterojunction Bipolar IC process as well as several conventional depletion mode GaAs IC processes that are optimized for different applications. Hewlett-Packard also manufactures a wide variety of RF diodes, transistors and hybrid modules in high volume which can be lower in cost and/or have superior performance than current RFIC equivalents. Realistically, no single IC technology can provide an optimum solution for the RF semiconductor portion of a radio in the 800-2500 MHz range at this time. Today, the optimum solution requires a mix of discrete, hybrid and IC technologies in both Silicon and GaAs. This paper describes specific Silicon Bipolar and GaAs MESFET IC processes that are well suited for wireless communications and suggests an RF system partitioning to best exploit these complementary technologies.

RFIC Process Technology

A cross-section of Hewlett-Packard's ISOSATtm Silicon Bipolar process is given in Figure 1. Key npn device metrics include an f_t of 15-20 GHz and an f_{max} of over 25 GHz for this process which has been in volume production for several years. The npn devices are drawn with .6 μ m emitters on a 1.6 μ m emitter-base pitch and polysilicon thin-film resistors are available at 125 Ω /sq and 1500 Ω /sq. Although these overall performance parameters are comparable with several other high speed bipolar processes in the industry, ISOSAT has several distinguishing features that offer distinct advantages for high-volume wireless communications applications in the 800-2500 MHz frequency range.

First consider the basic npn device structure. Nominal h_{FE} of 150 minimizes base shot noise for premium low-noise amplifier

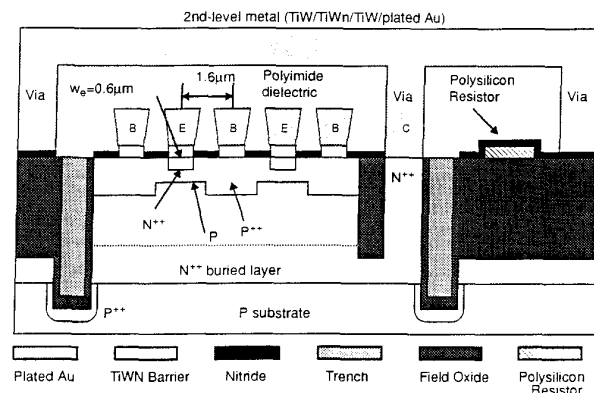


Figure 1 - Cross-section of the ISOSAT silicon bipolar IC process.

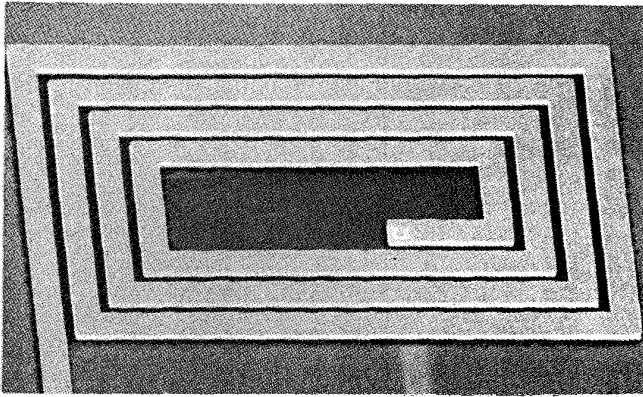


Figure 2 - SEM photograph of an ISOSAT inductor.

(LNA) performance while also easing the design of low-current temperature-compensated bias circuits. The $8\text{ }\mu\text{m}$ deep trench isolation with channel stop implant allows for a relatively low-doped substrate which reduces the parasitic collector-substrate capacitance. Most modern VLSI polysilicon emitter bipolar processes use aluminum metal as in CMOS. However, ISOSAT devices are completely interdigitated with gold metal and titanium-tungsten-nitride barriers to provide low emitter resistance, high current density (for transmit power) and superior reliability.

Passive elements in the ISOSAT process are key to its application in battery-operated wireless systems. The process uses a thick $2\text{ }\mu\text{m}$ field oxide which greatly reduces the parasitic capacitance of interconnects, bondpads and thin-film resistors compared to most polysilicon emitter processes which have only $0.7\text{ }\mu\text{m}$ of field oxide. Metal-insulator-semiconductor (MIS) capacitors with $.5\text{ fF}/\mu\text{m}^2$ are produced with typical Q values of 25 in the 800-2500 MHz range and a high 5:1 ratio of desired capacitance to parasitic substrate capacitance. The combination of thick plated gold metal layers and field oxide also facilitates the use of inductors and transformers (or baluns) with Q values comparable to those of GaAs in the 800-2500 MHz range. For example, Figure 2 is an SEM photograph of a 5 nH ISOSAT inductor with a self-resonant frequency above 5 GHz and a Q of about 10 at 2 GHz. Practical inductors can be realized in ISOSAT up to about 20 nH and capacitors are practical up to about 20 pF.

Finally ISOSAT also has several additional devices such as low-leakage lateral pnps (for bias circuits) and Schottky diodes with 100 GHz f_c for level shifters and mixers. The next-generation ISOSAT process will have $.4\text{ }\mu\text{m}$ emitters on a $.8\text{ }\mu\text{m}$ emitter-base pitch which results in devices with a 30 GHz f_t and 60 GHz f_{max} with no loss in the performance of the passive elements.

Cost considerations are crucial in the design of RFIC's for the wireless market. For a given application, cost comparisons between Silicon and GaAs implementations are inevitably controversial. The cost of processing a wafer using the processes previously described is not significantly different for either technology except that the starting material in GaAs remains 20-50 times more expensive. When small die are used or the number of die per wafer is high, this cost differential becomes negligible at the die level. Thus, the major cost differences in high volumes (where factory utilization is high) arise from wafer size and/or yield with both factors currently favoring Silicon. For a small die associated with low levels of integration, the comparable cost of test and assembly

in both technologies serves to further lower the relative overall cost difference. Therefore, the current situation favors using GaAs for performance critical front-end functions such as the LNA, and the last stage(s) of the power amplifier (PA) since the performance premium can often justify a slightly higher price. Furthermore, certain functions such as high performance RF switches are more easily realized using a FET structure.

As previously mentioned, in theory, price parity between GaAs and Silicon Bipolar Integrated Circuits can be achieved given comparable yields. Unfortunately, it is difficult to obtain such high yields in GaAs with a simple low cost process. Although a great deal can be gained by solid design techniques, the basic process must be capable of high yields. A cross section of a low cost GaAs IC process optimized for RFIC applications in the 800-2500 GHz frequency range is shown in Figure 3. It is a simple depletion mode process with 8 mask steps. Vapor-Phase Epitaxy (VPE) material is used to provide excellent uniformity. The process has been optimized for low voltage operation and features a nominal gate length of $.6\text{ }\mu\text{m}$, utilizing G Line stepper technology with a device Ft of 26 GHz. Gold metalization is used for low resistance interconnect and improved reliability. Resistors are fabricated using thin film NiCr as well as bulk GaAs. (Several optional features such as thin film NiCr resistors and backside vias are only used when needed to minimize cost.) Metal-Nitride-Metal capacitors are available and Silicon Nitride Passivation is used. Tradeoffs between breakdown voltage, and device performance have resulted in a process which represents a good compromise between low noise, power efficiency, gain and isolation (for switches). Although an optimized process could produce superior devices for a specific circuit (i.e. LNA) in most cases, the penalty paid in the performance of other devices (for example a switch or a power amplifier) is too severe. Therefore, the RFIC process is really intended for multifunction devices providing good performance for a number of possible circuits.

A major technology limitation for high volume wireless applications is low-cost semiconductor packaging. The parasitic lead inductance of most industry standard surface-mount plastic packages (typically 1-4 nH) can significantly degrade the performance of both Silicon and GaAs devices in the 800-2500 MHz range. In addition, package lead-lead isolation can often limit the gain and/or complexity of multi-function RFICs, and the high thermal resistance of these packages must be taken into account in the design.

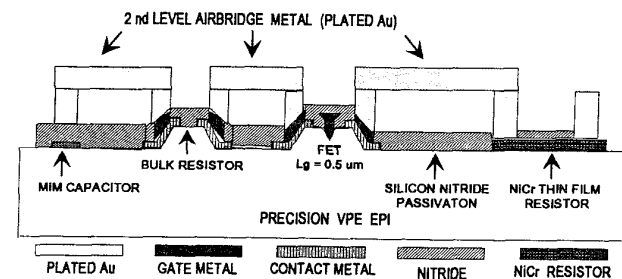


Figure 3 - Cross-section of Low Cost GaAs RFIC process.

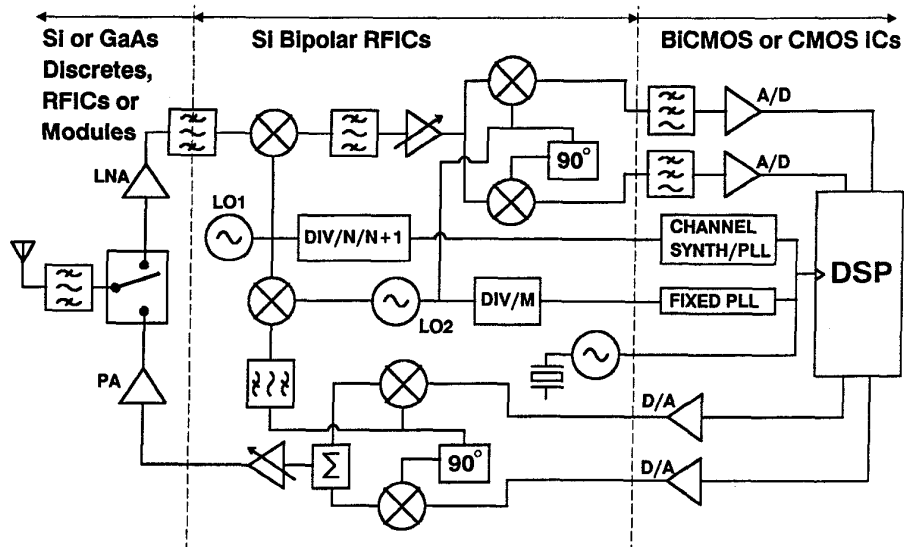


Figure 4 - RF architecture of generic half-duplex transceiver.

Example System Architecture

Figure 4 illustrates a possible RF system architecture for a half-duplex radio. This architecture does not represent any particular personal communications system nor does it necessarily represent an "optimum" RF system approach. Figure 4 simply shows the types of RF functions that RFIC suppliers must build and their general relationships within a system.

The receiver architecture of Figure 4 consists of a conventional first downconversion followed by an image-reject second downconversion. Alternatively, double-downconversion might also be used. The demodulation scheme would reflect the type of modulation utilized and the system requirements. Image-reject first downconverters or "zero-IF" direct downconversion receivers are also feasible from an RF component viewpoint. However, these alternatives have other system limitations such as LO isolation, DC offsets, channel mismatch or insufficient dynamic range or excessive power consumption.

The transmitter architecture of Figure 4 uses direct conversion from modulating baseband quadrature inputs I and Q to the RF carrier. The transmit LO for the modulator is generated from the desired mixer product of the two LOs which are needed in the receiver architecture. Alternatively, IF quadrature modulation at the second LO frequency followed by an upconversion to the final RF carrier could be used to generate the transmit signal. Valid arguments can be made for either approach from both the system and components points of view. Efficient and repeatable gain control at the transmit RF as shown in Figure 4 is also a significant challenge for RFICs especially in linear systems. In general, for systems with transmit levels of 100 mW or more (peak power), the DC power consumption of the PA can dominate the overall transmit-mode power consumption, which places a critical requirement on the PA efficiency.

Figure 4 also attempts to delineate the possible boundaries between optimum process technology choices. Baseband processing and low frequency functions are usually handled by CMOS or BiCMOS IC technologies. In the RF section a multitude

of technology choices are possible. Closest to the antenna, the front-end functions such as the LNA, duplex switch and PA are usually implemented today with high-performance, narrowband-tuned discrete transistors of either silicon or GaAs. Often the PA is implemented using discrete transistors that are packaged, biased and tuned on a small hybrid circuit (multi-chip module). However, the bulk of the RF semiconductor functions in Figure 4 consists of frequency converters, oscillators, prescalers for synthesizers and various other amplifiers or buffers. Today the implementation of these functions with silicon bipolar technologies can be accomplished by designs that range in complexity from discrete transistors to multi-function LSI RF subsystem ICs. In fact, packaging is possibly the greatest barrier to integrating the entire RF section of a half-duplex radio on a single silicon bipolar IC. Using present day technology, the resultant die size would be on the order of 10 mm² excluding bondpads. Silicon bipolar technology has distinct performance advantages over GaAs for many of these functions due to its superior threshold uniformity, higher transconductance and lower 1/f noise. Furthermore, the excellent device models and the manufacturing maturity of silicon bipolar devices can provide significant time-to-market advantages over GaAs for multi-function designs. BiCMOS IC technology is extremely effective in the implementation of synthesizers. However, high performance BiCMOS still has inherent cost disadvantages and the processes currently available do not offer the narrowband RF performance possible with a microwave bipolar process such as ISOSAT.

Although Figure 4 has focused on RF functions, a modern battery-powered, half-duplex digital radio has significant control circuitry as an integral part of its RF section. The control functions include power-up, status reporting of different functions, transmit or receive timing (especially complex for TDMA radios), channel selection, output power level, receive signal leveling in addition to many other tasks. The necessary control logic must thus be integrated with the RF functions for large multi-function RFICs.

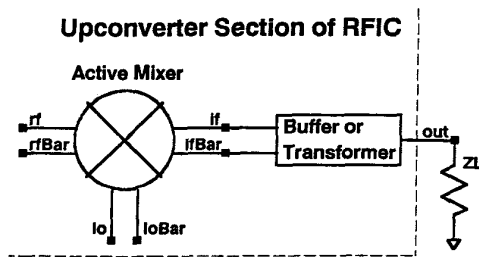


Figure 5 - Active mixer application on an RFIC

Example Circuit Topologies

As evident from Figure 4, the primary RF functions that RFICs must address to reduce the size, cost and power consumption of handheld transceivers are amplifiers, frequency converters, phase shifters, prescalers and oscillators. Multi-function Silicon Bipolar RFICs are a promising approach to transceiver size reductions although package technology and filter requirements continue to constrain system size. Total manufacturing cost (though not necessarily total semiconductor cost) can also be reduced by multifunction integration if simple manufacturable processes and standard plastic packages are used. Reducing the overall RF section power consumption for a given system is largely dependent on the transceiver architecture, the semiconductor technology performance and the RFIC circuit topologies. This section focuses on key challenges facing silicon bipolar and GaAs MESFET designers to achieve efficient narrowband performance at supply voltages of approximately 3V.

For Silicon Bipolar RFICs, reduction of supply voltages complicates the implementation of all RF functions. Frequency converters or mixers are usually impacted most by the supply voltage reduction although biasing of efficient low-noise and power amplifiers is also greatly complicated. Prescalers for synthesizers are composed of D-type latches and combinational logic gates which can be similar to the mixers in topology but much simpler to implement due to lower voltage swings and consistent DC coupling requirements. Figure 5 shows a mixer driven by LO and RF inputs with an IF output delivered to an off-chip load. A conventional Gilbert-cell active mixer topology¹ is shown in Figure 6. This same basic topology can be used for both downconverters and upconverters although the exact device size, bias conditions and output buffer or transformer are usually very different between the two applications. Downconverters tend to be somewhat simpler because the two dominant tones LO-RF and LO+RF are greatly separated in frequency. The key design issue for a downconverter is usually optimizing the noise and input linearity for a given supply current. In an upconverter, the two dominant tones are both near the LO frequency and often the low frequency or baseband RF input voltage swings are relatively large. When the desired output tone of the upconverter or modulator is at the final transmit frequency, obtaining maximum output power for minimum supply current is usually the most important design goal.

Typical DC bias voltages for an upconverting active mixer at $V_{CC}=3V$ and $T=25^{\circ}C$ are shown in Figure 6. The DC bias current for the active mixer section shown in Figure 6 can vary greatly

depending on the application but typical values of I_{bias} in Figure 6 are .5-5 mA. The design of bias circuits to provide "constant" output power and/or linearity over supply voltage (2.7-3.3V) and temperature (-40 to $+85^{\circ}C$) is a major challenge. At 3V bandgap regulator circuits can still be used effectively. Figure 7 illustrates some of the many IF output buffer or transformer options compatible with the upconverting mixer of Figure 6. Typical DC bias voltages for $V_{CC}=3V$ and $T=25^{\circ}C$ are also shown. In the cases where the $ifBar$ output of the active mixer is not used, $ifBar$ would normally be connected directly to VCC. All inductors and capacitors shown in Figure 7 represent real (not parasitic) elements. Package lead and bond parasitics, though extremely important, are not explicitly shown in Figure 7 but they can sometimes be exploited to benefit.

Option 1 in Figure 7 is typical of an output stage that has been used for wideband 5V active mixers¹. In this case the emitter-follower provides power gain and sets a broadband output match. By partitioning much of the total current into the emitter-follower, less current is "wasted" by ignoring the differential $ifBar$ output of the active mixer. However, this approach is still inherently very inefficient. For example, at 3V supply the voltage drop on the load resistor is about 500 mV where $V_{drop}=I_{bias} \cdot R_L$. At 1 dB gain compression (or about -20 dBc 3rd order intermodulation), about one-half of I_{bias} can typically be steered in the input RF differential pair. Thus the output swing is on the order of $\pm .5V_{drop}$. The emitter-follower is therefore extremely inefficient in this example since 83% of its power dissipation ($V_{CC}-V_{drop}$) $\cdot I_{bias}$ does not contribute to the output drive at all or is thus "wasted".

Alternatively, in Option 2a of Figure 7 a wideband-matched, single-ended output is taken directly from the active mixer cell. For a 50 Ω output impedance and 2:1 output VSWR the load resistor R_L would be approximately 100 Ω . Thus for $V_{drop}=500mV$, $I_{bias}=5mA$. As with Option 1 this simple wideband approach is very inefficient since again about 83% of the power dissipation from a 3V supply does not contribute to the output power. In fact, Option 2a as described is even worse than Option 1 since another 50% of the available output power (the $ifBar$ output) is also ignored. In both cases it is obvious that a single-ended wideband-matched output is inconsistent with the goal of minimizing power consumption for wireless transceivers.

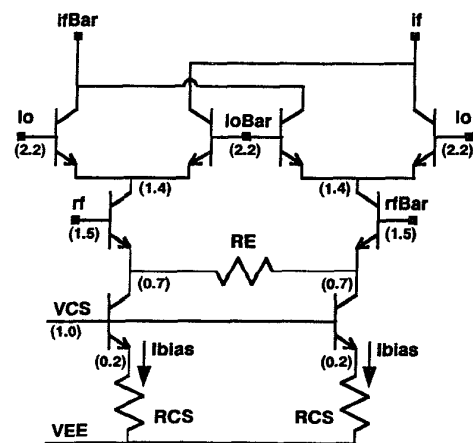


Figure 6 - Gilbert-cell active mixer topology.

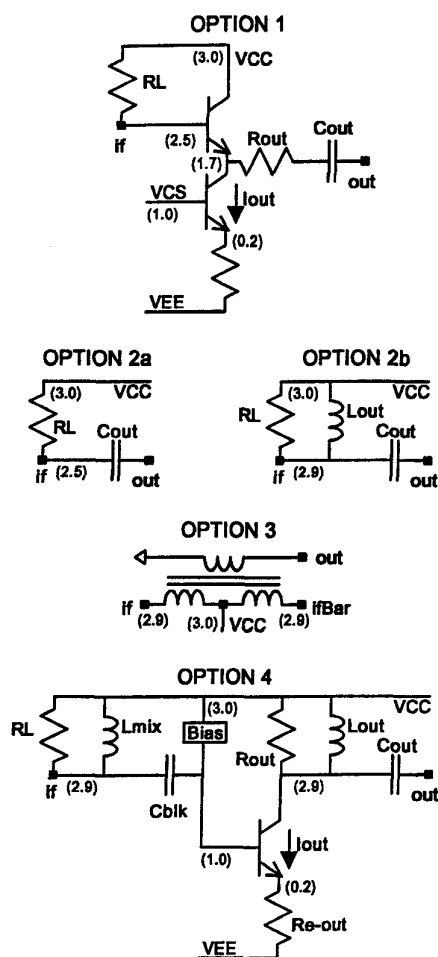


Figure 7 - Output stage options for upconverting mixer.

Several approaches can be taken to improve the efficiency while keeping the same basic active mixer topology. Option 2b uses a "narrowband" L-C impedance transformation on the IF output. Practical L and C values realized on-chip with the ISOSAT silicon bipolar process yield about 10-20% bandwidth on the output match which is more than adequate for most wireless applications. With Option 2b the load impedance for the *if* output can be raised typically to 200-400 Ω in-band while maintaining a good 50 Ω output match. Thus less current is required to swing all available voltage. In addition, the inductor bias places the *if* output DC voltage at VCC and thus increases considerably the available voltage swing. Although 50% of the mixer power (from *ifBar*) is still ignored in Option 2b, the net improvement in output power can easily be 6 dB with respect to Option 2a.

Another approach to improve efficiency by combining both differential outputs *if* and *ifBar* in a center-tapped transformer (or balun) is shown as Option 3 in Figure 7. Theoretically, this approach is superior to Option 2b since both differential outputs are used and same voltage swings are possible. In addition, the common-mode rejection may also have benefits in many applications. An alternative approach is to provide differential open collector outputs with the customer supplying a 4:1 ratio output balun external to the IC package. In addition to

complicating the transceiver board and increasing cost, an external balun has serious performance problems for 800-2500 MHz applications. Since the output impedance to the board is high (for example, 200 Ω with a 4:1 balun into 50 Ω) for either *if* or *ifBar*, stray capacitance on the output lines acts as a low-pass filter. For a typical bipolar or BiCMOS process (though not ISOSAT), bond pad and lead capacitances can total about 800 fF. Thus even if board and balun parasitics are ignored, this low-pass filter limits the IF bandwidth independent of transistor limitations with an $f_{3db}=1$ GHz. In the ISOSAT silicon bipolar IC technology, a 2:1 output balun can be realized directly on the RFIC to provide a single-ended narrowband-matched 50 Ω output. Combined with lower bond pad capacitance, this low impedance output corresponds to an $f_{3db}=8$ GHz for ISOSAT although transistor parasitics will usually limit the IF bandwidth to lower frequencies. Baluns fabricated in ISOSAT have shown approximately 1.5 dB loss at 2 GHz with nearly octave-band output flatness. The 1.5 dB loss can be used as part of the output match as well. In summary, baluns can increase the efficiency of upconverters if realized on the RFIC. However, most of the power consumption in the active mixer (about 70% in Figure 6) still does not contribute to the output drive and this situation is worse as supply voltages decrease.

A final approach to increase overall power efficiency is shown by Option 4 in Figure 7. As with Option 1, the active mixer currents *Ibias* would be kept small and most of the total current would be used for *Iout*. However unlike Option 1, the output stage of Option 4 is a common-emitter amplifier with a narrowband-tuned output for high efficiency and good output match. In the amplifier, the output voltage can swing about ± 2 V around VCC=3V which leaves far less "wasted" voltage drop than any other Option in Figure 7. For best overall efficiency, the low current output of the active mixer is also narrowband transformed from a high impedance load to the relatively low input impedance of the common-emitter amplifier. At 2 GHz typical values for the transformer elements of Figure 7 are 6-8 nH and 0.6-1.0 pF. The parasitic lead and bond wire inductance of approximately 3 nH can be used effectively for part of the Option 4 inductances with the remainder realized by low-loss ISOSAT inductors with excellent uniformity on-chip. Low-parasitic capacitors can also be fabricated repeatably on an ISOSAT die. For many conventional silicon bipolar or BiCMOS processes which lack premium passive elements, open collectors combined with discrete external inductors and capacitors could be used to implement Option 4 of Figure 7. However as with external baluns described in Option 3, high impedance outputs combined with normal stray capacitances severely limit the utility of such an approach for 800-2500 MHz applications.

A valid criticism of Option 4 can be made for the common upconversion application where one of the two nominally equal tones LO-RF or LO+RF is removed by filtering before the power amplifier. By going to the off-chip filter directly from the IF output, the first-stage amplifier as shown in Option 4 of Figure 7 would handle only one tone instead of two (a 6 dB advantage in terms of peak power). However, some of this advantage would be lost due to the extra 50 Ω input and output matches required and the extra gain following the filter complicates overall isolation. In the case of a direct conversion modulator (such as used for BPSK or $\pi/4$ QPSK), this criticism is not valid at all since both tones of the mixer will pass through the entire amplifier chain.

Although 3V supply already causes RFIC designers considerable

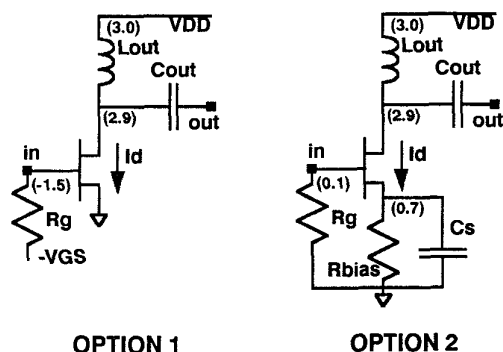


Figure 8 - Bias Options for GaAs MESFET amplifier stage.

difficulties, 2V or even 1V transceiver ICs may be demanded eventually. At a nominal $V_{CC}=2V$, the Gilbert-cell topology of Figure 6 cannot use current sources derived from a bandgap regulator and must have the $I_{o,loBar}$ DC biases within 300 mV of V_{CC} . In this situation narrowband loads and output stages implemented by on-chip passive elements will be almost mandatory. The high performance Schottky diodes available in ISOSAT will also be needed as low-voltage level shifters in a variety of applications including high-speed digital logic. At $V_{CC}=1V$, the Gilbert-cell active mixer topology is not practical for most silicon bipolar RFICs. Both balanced and unbalanced mixer topologies based on Schottky diodes are possible for 1V RFIC operation.

GaAs amplifier circuits are also impacted considerably by the reduction of supply voltage especially if only a single supply is available. Two options for biasing a single depletion-mode MESFET as a power amplifier (PA) stage are shown in Figure 8. In Option 1 a negative voltage must be provided to the gate. Ideally the V_{gs} supply is generated by sensing the drain current I_d and using feedback to set V_{gs} . Alternatively V_{gs} is often set by a resistor split to a fixed negative supply with allowance to adjust on a unit basis the I_d - V_{gs} curve of each individual device. In the Option 1 bias scheme the output drain voltage can swing about $\pm 2V$ around V_{DD} which is analogous to the collector voltage swing on a common-emitter bipolar amplifier such as Option 4 of Figure 7. Although the Silicon Bipolar and GaAs MESFET amplifiers thus have similar collector or drain "efficiencies", in practice the GaAs amplifier has higher power-added efficiency due to inherently higher gain per stage for commercially-available technologies. The additional gain may also allow a three-stage silicon bipolar PA to become a two-stage GaAs PA. This further improves the overall efficiency, reduces size and may actually have no impact on cost since fewer of the expensive GaAs devices are required.

However, if negative voltages are not available within the portable transceiver, then a GaAs PA stage can be biased by raising the source voltage positive as shown for example by Option 2 in Figure 8. This approach is easier for a customer to use and self-biases according to the relationship $I_d(V_{gs}) = -V_{gs}/R_{bias}$. Typically the MESFET available in the RFIC process is biased at V_{gs} near $-0.6V$ as indicated in Figure 8. For devices with an I_d - V_{ds} "knee voltage" of about 1V, the resultant output swing is now restricted to about $\pm 1.5V$ around V_{DD} . The lower voltage swing

thus decreases the output efficiency considerably although the still higher gain keeps the power-added efficiency similar to a silicon bipolar stage. Thus, at true single supply operation of 3V (no negative gate bias) or less, GaAs has little advantage over silicon bipolar for power amplification especially in applications below 1 GHz.

Other transceiver functions ideal for monolithic GaAs integration such as an antenna switch or a low noise amplifier are more straightforward to implement from a single +3V supply. The single-pole, double-throw switch of Figure 4 can be integrated by floating the source voltage to V_{DD} . The RFIC process has a pinch-off V_{gs} of about 2V. A low-noise amplifier could be biased from a single 3V supply similar to Option 2 of Figure 8 with excellent performance. An alternative approach would use an area-ratioed MESFET as an I_{dss} current source for the amplifier device.

Example RFICs

A wide variety of RFICs in several technologies are now available from several vendors. A brief summary of recently fabricated RFIC products or prototypes at Hewlett-Packard is given in Table 1. This is a partial list of the many combinations and permutations of RF functions (and associated specifications) being investigated using monolithic Silicon and GaAs RFICs.

The first RFIC in Table 1 is a combination low noise amplifier (LNA) and downconverting mixer. The LNA and mixer are both narrowband-tuned for maximum linearity from minimum current. The use of on-chip ISOSAT inductors allows the mixer noise figure to be much lower for given current and linearity than possible with conventional Bipolar or BiCMOS processes. A 900 MHz version of the same IC has 3 dB higher gain in the LNA with 1.5 dB lower noise figure. This 3V RFIC is intended to be used in an industry-standard plastic SO-16 package. The second RFIC in Table 1 is a direct conversion vector modulator² designed primarily for 900 MHz digital cellular applications such as GSM, NADC and JDC. The modulator uses essentially the output stage topology of Option 4/Figure 7 although this design is optimized for supply voltages above 4V. By utilizing the narrowband reactive tuning elements within the SO-16 package, this modulator provides excellent single-ended output power efficiency while maintaining a good 50 Ω output match. The third entry in Table 1 is a 200 mW driver amplifier designed specifically for GSM, although this device is appropriate for a variety of applications from 150-1000 MHz. This amplifier also makes extensive use of reactive interstage matching elements within the IC package to increase efficiency. The SO-8 package (which uses an industry-standard footprint) was modified to achieve the necessary power dissipation. These first three RFICs are good examples of the present level of monolithic integration currently being deployed in portable wireless transceivers.

The fourth ISOSAT RFIC of Table 1 is an example of the level of integration expected for the next generation wireless applications. This single receiver IC in a small low-cost 32-lead plastic package (32PQFP) contains two downconversion stages, a negative-resistance cell for a VCO, a variety of prescalers, a digital phase-frequency detector (DPFD) and a TTL clock driver. The RFIC was designed primarily for Global Positioning System (GPS) where spread-spectrum satellite signals are received at 1575 MHz. At 3V and only 40 mA, the double downconverter provides 70 dB of gain from 1575 MHz to 15 MHz (through a 135 MHz first IF) while synthesizing a 1440 MHz LO from a 20 MHz reference³.

Paging receivers at 930 MHz are probably the only mass market

in the 800-2500 MHz range that currently use a 1V power supply in the RF section. At present most pagers use discrete bipolar transistors to implement the the receiver. The fifth ISOSAT RFIC of Table 1 is a prototype two-stage ISOSAT low-noise amplifier that consumes only 2 mA from a 1V supply. The IC was assembled in a SOT143 4-lead transistor package and delivered approximately 18 dB gain with 2.2 dB noise figure at 930 MHz. This prototype represents a step towards building multi-function RFICs or use with extremely low single power supply voltages.

The final RFIC of Table 1 is a GaAs multifunction IC that consists of the combination of an LNA, a single-pole double-throw switch and an power amplifier. Although the power amplifier requires a negative gate voltage, (as discussed previously to achieve the efficiency reported in Table 1.), the LNA and switch are biased from a single 3V supply. This RFIC is intended to be a cost-effective approach to reducing the size and component count of existing discrete front-end solutions while maintaining excellent RF performance.

Conclusions

The emerging wireless communication component market offers tremendous opportunities for the use of both Silicon Bipolar and GaAs MESFET IC technologies. To successfully address these markets, the choice of the appropriate IC technology for a given circuit function is essential. The IC technology options and several tradeoffs in IC design have been discussed. In addition, key design considerations were reviewed and several different approaches for implementing various circuit functions in a 3 Volt system were also discussed in detail.

In summary, as the available power supply voltage is reduced and system performance requirements remain aggressive, the use of the appropriate process technology and design techniques will become crucial, resulting in significant opportunities for both GaAs and Silicon Bipolar IC technologies. These technologies will coexist for the immediate future and this situation will result in a major opportunity for the development of new packages technology or possibly low cost/high performance RF multichip modules.

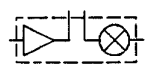
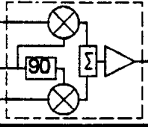
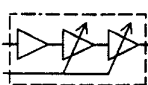
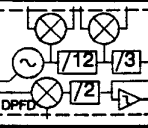
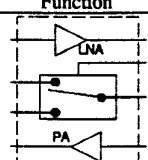
Function	LNA/Mixer
	VCC=3 V, ICC=11 mA, RF=1900 MHz LNA: Gain=10 dB, NF=4 dB, IP3=+4 dBm Mixer: Gain=6 dB, NF=11 dB, IP3= +3 dBm Technology: ISOSAT Package: SO-16
Function	Vector Modulator
	VCC=5 V, ICC=36 mA, LO=900 MHz Output to 50Ω: P1dB=+9 dBm, VSWR=1.5:1 Ave Map Error=3%, Typ SSB Suppr=35 dBc Technology: ISOSAT Package: SO-16
Function	Driver Amplifier
	VCC=5 V, ICC=160 mA, RF=900 MHz Output to 50Ω: P1dB=+23 dBm Gain = 32 dB, Gain Control Range = 50 dB Technology: ISOSAT Package: SO-8
Function	GPS Receiver
	VCC=3 V, ICC=40 mA, RF=1575 MHz Overall: Gain = 70 dB, NF = 12 dB DPFD Output=2 V/rad, TTL edge=8 ns Technology: ISOSAT Package: 32PQFP
Function	Pager LNA
	VCC=1 V, ICC=2 mA, RF=930 MHz Output to 50Ω: Gain = 18 dB, NF = 2.2 dB Technology: ISOSAT Package: SOT-143
Function	LNA/Switch/PA
	VDD=3 V, RF=1900 MHz LNA: Gain=12 dB, NF=1.7 dB, IDD=5 mA Switch: Loss=1 dB, Iso.=20 dB, IP3=50 dBm PA: Gain=13 dB, P1dB=26 dBm, PAE=45% Technology: GaAs Package: μPak-16

Table 1 - Example RFICs

References

- 1 J. Wholey et al., "Silicon bipolar double-balanced active mixer MMICs for RF/microwave applications up to 6 GHz," in IEEE MTT-S Int. Microwave Symp. Dig., June 1989.
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- 3 K.J. Negus, et al., "3.3V GPS receiver MMIC implemented on a mixed-signal, silicon bipolar array," in IEEE MTT-S Int. Microwave Symp. Dig., June 1992.