

SP 23.8: Silicon Bipolar VCO Family for 1.1 to 2.2GHz with Fully-Integrated Tank and Tuning Circuits

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In recent years several RFIC manufacturers have developed highly-integrated chips but the voltage-controlled oscillator (VCO) has thus far proven impossible to fully integrate in a standard silicon RFIC process. Traditionally VCOs are implemented in 3 different ways. First and foremost is the hybrid module that has the advantage of ease of use at the price of bulky size (especially height) and relatively high cost. For fairly sophisticated handset manufacturers, a second approach has been to build the VCO discretely on the RF transceiver board which saves cost but requires significant board space, engineering investment and time. A third recent compromise integrates the negative resistance portion of the VCO on an RFIC with the complete tank circuit including resonator and varactor implemented discretely on the board. This work introduces fully-integrated VCOs implemented in the mature ISOSAT silicon bipolar RFIC process. The ISOSAT silicon bipolar process has transistors with $15\text{GHz } f_T$ and $30\text{GHz } f_{\text{max}}$ along with MIS capacitors of $Q > 50$ and spiral inductors with Q up to 10 for the values and frequency range of interest. Recently, a voltage-variable capacitor (or "varactor") is characterized within the process. This device has up to 3:1 capacitance range from 0 to 3V reverse bias and also has Q of 30-50 in the 1.1-2.2GHz frequency range desired for these VCOs.

A conceptual schematic of the monolithic VCO is given in Figure 1 and can be described in terms of 5 functional cells or subcircuits. The core negative resistance cell (or "-R cell") is shown in Figure 2. Also shown in Figure 2 is the output buffer differential pair that helps isolate the VCO output load from the tank. A third major subcircuit is the bandgap reference generator (BGR). The VCO circuit also has a fully-integrated differential tank circuit on-chip consisting of spiral inductors, MIS capacitors, and integrated varactors. The inductors also supply bias current to the -R cell and have typical Q values of 8-10 as shown for example in Figure 3 for a 4nH inductor used by the 1.55GHz example VCO. Finally, Figure 1 indicates a balun transformer used to bias the output buffer and allow for a 50Ω matched single-ended output.

The key performance parameter that drives design is phase noise. For the VCO as described the phase noise can be conceptually separated into two components. First, wideband thermal and shot noise is produced by various noise sources in the feedback loop of the -R cell. And second, noise from the BGR is mixed around the carrier during oscillation.

For wideband noise in the oscillator feedback loop, Reference 1 gives the phase noise per Hz in the -6dB per octave region as:

$$N/S_{\Delta f} = \frac{|ELG|}{8(Q_L \cos \theta)^2} (f_o / \Delta f)^2 (V_n^2 / V_{\text{rms}}^2) \quad (1)$$

where ELG is the excess loop gain defined as the ratio of -R cell impedance where oscillation is just sustained to the actual -R cell impedance, Q_L is the open loop resonator Q with all active circuit parasitics included, θ is the phase delay between voltage and current in the -R cell, f_o the carrier frequency of oscillation, Δf the offset frequency from the carrier, V_n^2 the tank referred noise power density per Hz and V_{rms}^2 the tank signal power density. Note that earlier expressions such as Reference 2 effectively assumed $ELG=1$ (which is unrealistic for a robust product) and $\theta=0$ (which implies infinitely fast transistors). From Equation 1

some key design imperatives are obvious. First, the tank elements and -R cell devices must be carefully modeled and optimized to maximize Q_L . Furthermore, the choice of tank elements and -R cell bias currents must also be such that the voltage swing is fully used to maximize V_{rms}^2 without causing hard saturation. The device sizes, tank load impedance and bias currents in the -R cell are critical to minimize the phase delay that effectively "de-Q's" the oscillator per Equation 1.

First a linear ac simulation of one of the example VCOs is performed with the loop opened but a dummy load added to keep the correct active circuit parasitics on the resonator. This gives $f_o=1550\text{MHz}$, $Q_L=8$ and $V_n^2=5.3e-17\text{V}^2/\text{Hz}$. Then a transient simulation and FFT analysis of the same circuit with loop closed for oscillation produced again $f_o=1550\text{MHz}$, $\theta=24^\circ$ (43ps delay), $ELG=1.75$ and $V_{\text{rms}}^2=744\text{V}^2$. Then $N/S=7.05e-11\text{Hz}^{-1}$ (or -101.5dBc/Hz) by Eqn (1) for $\Delta f=100\text{kHz}$. Note that the design choice of $ELG=1.75$ sacrifices 2.4dB of phase noise to ensure that $ELG > 1$ always (i.e. device always oscillates) over the full range of process parameter variations, power supply (2.7-5.5 V) and temperature (-40 to +85°C). Next BGR noise effect on the VCO is calculated. BGR noise power density of $8.3e-18\text{V}_{\text{rms}}^2/\text{Hz}$ from ac analysis is multiplied by the power transfer function from the VCS terminal of the -R cell in Figure 2 to the VCO output. This transfer function is determined by FFT analysis of the VCO output while modulating the VCS terminal with a $10\mu\text{V}$ 4MHz sinusoidal test source. When referred to 100kHz offset, this results in a N/S contribution of $5.25e-12\text{Hz}^{-1}$ (or -112.8dBc/Hz). Adding these two noise powers together gives: $(N/S)_{\Delta f=100\text{kHz}} = 7.05e-11 + 5.25e-12 = 7.58e-11\text{Hz}^{-1} = -101.2\text{dBc/Hz}$ that compares quite closely with the measured results for $f_o=1550\text{MHz}$, as shown in Figure 4.

Phase noise plots at 2.7V and 25°C for two different example VCOs are given in Figures 4 and 5. Both VCOs are capable of meeting the GSM900 or DCS1800 transmit spectral mask requirements and the 1550 MHz version also exceeds the -131dBc/Hz at 4MHz offset required for DECT by about 3dB. A summary of performance parameters for three example VCOs is given in Table 1. The pushing and pulling figures are comparable to those of hybrid VCOs. The distribution of the 16mA of current in the 1550MHz VCO is approximately 8mA in the -R cell, 4 mA in the output buffer and 4mA in the BGR. The relatively high BGR current was needed to make its noise contribution small as indicated by the detailed analysis.

Over -40 to +85°C and 2.7 to 5.5V, these VCOs typically have $\pm 1\text{dB}$ variation in output power and $\pm 1.5\text{dB}$ variation in phase noise. A photo of the .8x1.2mm² die is given as Figure 6. The upper 40% of the die is the differential tank circuit. The resonant output balun is visible at the bottom. All measured results are in the MSOP10 surface mount plastic package on an FR-4 test board.

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Cobblestone Wireless LLC, Exhibit 2018

Page 2018 - 1

IPR2024-00707, Hewlett Packard Enterprise Co. v. Cobblestone, LLC

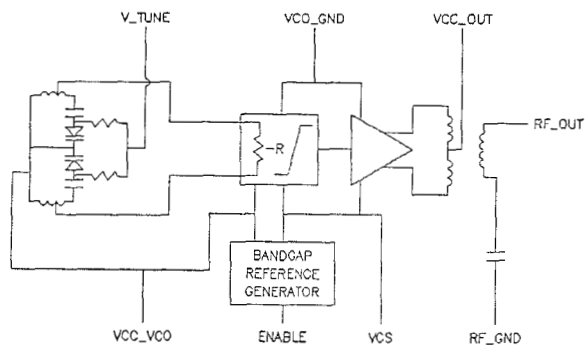


Figure 1: Conceptual schematic of VCO.

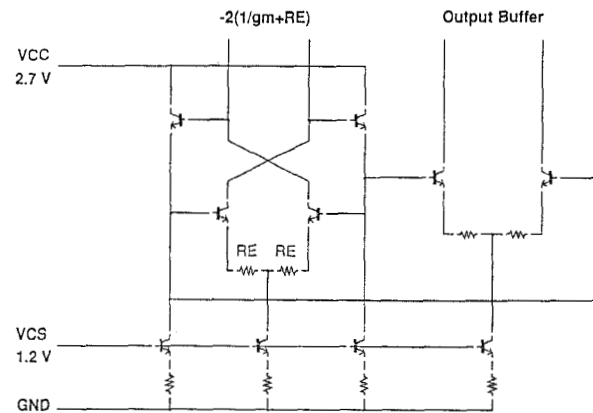


Figure 2: -R cell and output buffer.

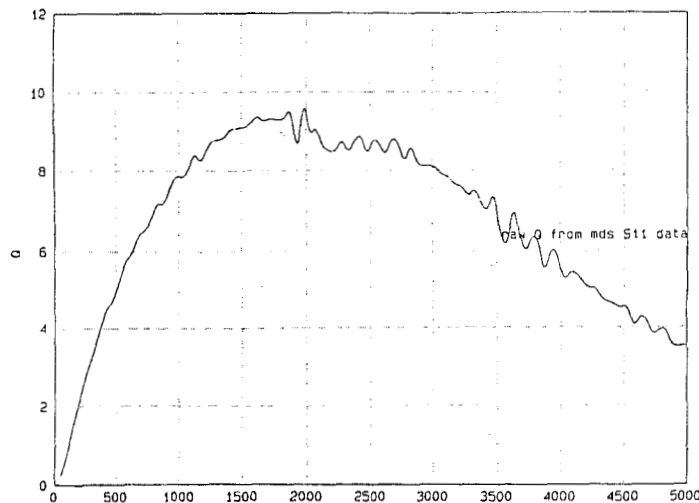


Figure 3: Measured Q of 4nH inductor.

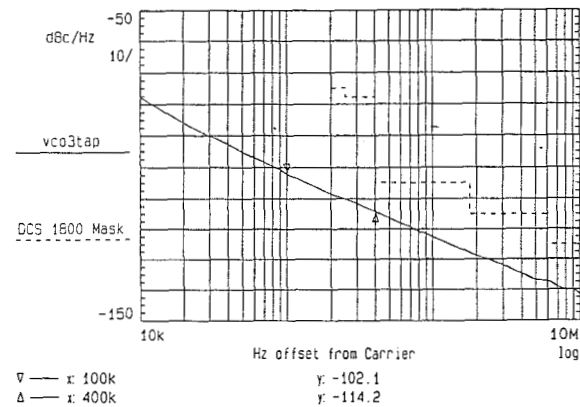


Figure 4: Measured N/S of 1550MHz VCO.

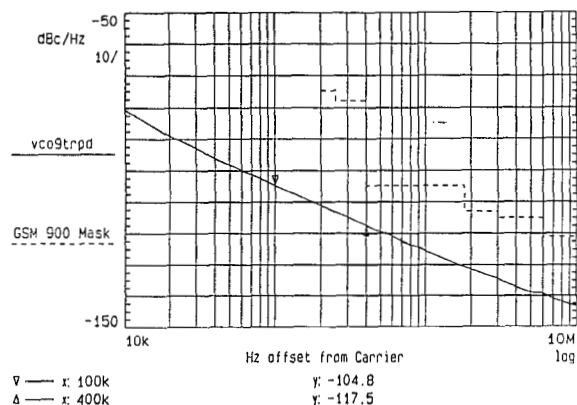


Figure 5: Measured N/S of 1100MHz VCO.

Figure 6: See page 492.

Nominal freq. f_0 (MHz)	1100	1550	2200
Tuning range (MHz)	150	200	250
Supply current (mA)	15	16	16
(N/S) $\Delta f=100$ kHz (dBc/Hz)	-105	-102	-99
Pushing figure (MHz/V)	1	1	2
Pulling figure (MHz) **	1	2	3
Output power (dBm)	-3	-3	-3

** Measured into a load of 12dB return loss, all phases

Table 1: Measured parameters of example VCOs.

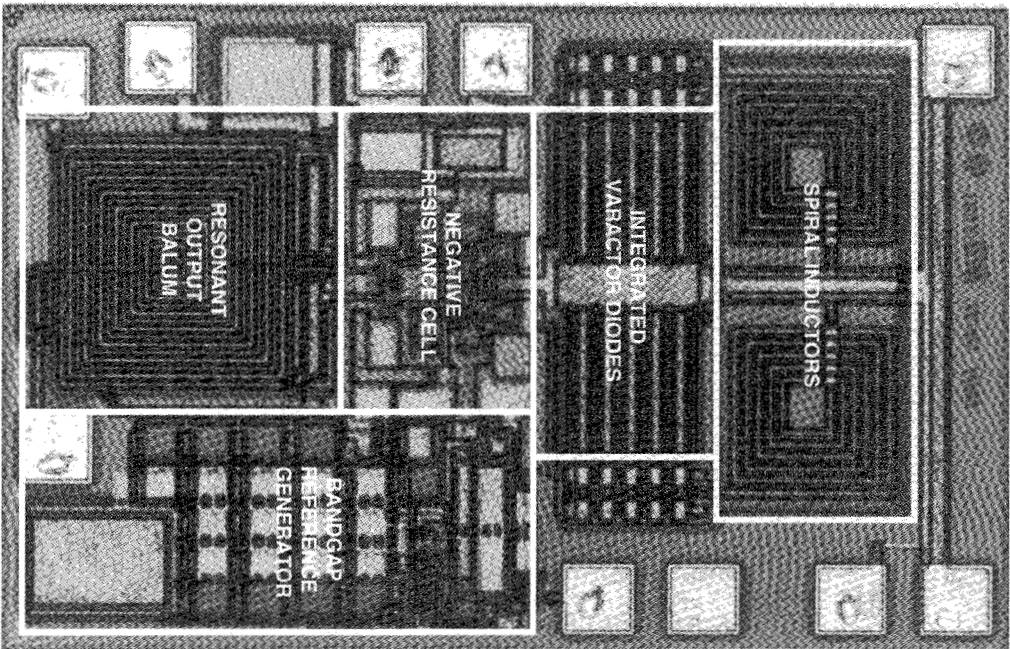


Figure 6: Micrograph of 0.8x1.2mm² VCO.

SP 24.1: A 20MB/s Data Rate 2.5V Flash Memory with Current-Controlled Field Erasing for 1M Cycle Endurance
(Continued from page 397)

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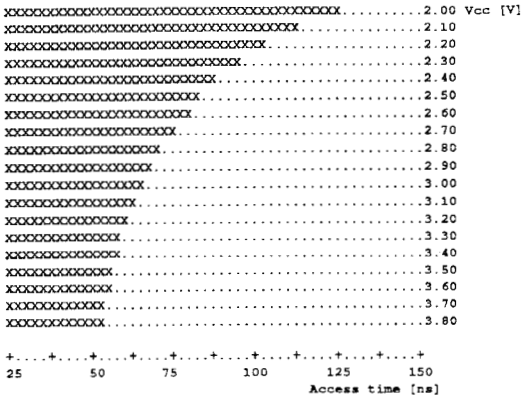


Figure 5: Access schmo plot: T=25°C, SRAM interface.

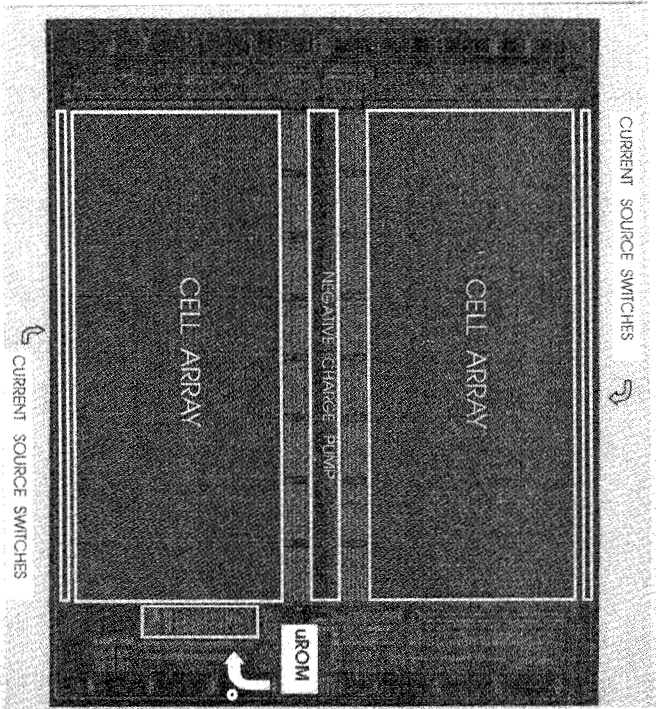


Figure 7: Chip micrograph.

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Page 2018 - 3

IPR2024-00707, Hewlett Packard Enterprise Co. v. Cobblestone, LLC