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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/840,063	05/22/2018	9977476	TWT04064/US	8903

60589 7590 05/02/2018

JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 78 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jian-Hong ZENG, Taoyuan City, TAIWAN;
DELTA ELECTRONICS, INC., Taoyuan City, TAIWAN;
Chao YAN, Taoyuan City, TAIWAN;
Pei-Qing HU, Taoyuan City, TAIWAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14840063
Filing Date	2015-08-31
First Named Inventor	Jian-Hong ZENG
Art Unit	2115
Examiner Name	LEE, THOMAS C
Attorney Docket Number	TWT04064/US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
Change(s) applied to document, /D.W./ 2/13/2018	1	20080101025	A1	2008-05-01	~~HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P~~	Harris et al.
	2	20120173892	A1	2012-07-05	TONG SONG-LIN et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2399684	GB	A	2004-09-22	SHUTTLE INC		
	2	M253836	TW	U	2004-12-21	VAC CORP		

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60589 7590 02/12/2018
JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/840,063	08/31/2015	Jian-Hong ZENG	TWT04064/US	8903

TITLE OF INVENTION: POWER SUPPLY APPARATUS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	05/14/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
YANCHUS III, PAUL B	2127	713-300000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 CKC & PARTNERS CO., LTD.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: DELTA ELECTRONICS, INC.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): TAOYUAN CITY, TAIWAN

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 504669 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /James Lynn O'Sullivan/ Date 2018-04-20
Typed or printed name James Lynn O'Sullivan Registration No. 65618

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Electronic Patent Application Fee Transmittal

Application Number:	14840063
Filing Date:	31-Aug-2015
Title of Invention:	POWER SUPPLY APPARATUS
First Named Inventor/Applicant Name:	Jian-Hong ZENG
Filer:	James Lynn O'Sullivan/Anny TENG
Attorney Docket Number:	TWT04064/US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt

EFS ID:	32392969
Application Number:	14840063
International Application Number:	
Confirmation Number:	8903
Title of Invention:	POWER SUPPLY APPARATUS
First Named Inventor/Applicant Name:	Jian-Hong ZENG
Customer Number:	60589
Filer:	James Lynn O'Sullivan/Anny TENG
Filer Authorized By:	James Lynn O'Sullivan
Attorney Docket Number:	TWT04064/US
Receipt Date:	20-APR-2018
Filing Date:	31-AUG-2015
Time Stamp:	04:19:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1000
RAM confirmation Number	042018INTEFSW00007887504669
Deposit Account	504669
Authorized User	null null

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	TWT04064US-FeeTransmittal-20180420.pdf	238193 2a01e9b3963b55c813cd0642302821a4d99fada5	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	29959 6f492c30cad77affd9849bd8826f08d87175204c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	268152		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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United States Patent and Trademark Office
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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

60589 7590 02/12/2018

JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

EXAMINER
YANCHUS III, PAUL B

ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 02/12/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/840,063	08/31/2015	Jian-Hong ZENG	TWT04064/US	8903

TITLE OF INVENTION: POWER SUPPLY APPARATUS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	05/14/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

60589 7590 02/12/2018
JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/840,063	08/31/2015	Jian-Hong ZENG	TWT04064/US	8903

TITLE OF INVENTION: POWER SUPPLY APPARATUS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	05/14/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
YANCHUS III, PAUL B	2127	713-300000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

IPR2024-00715 EX. 2005

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/840,063	08/31/2015	Jian-Hong ZENG	TWT04064/US	8903

60589 7590 02/12/2018

JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

EXAMINER	
YANCHUS III, PAUL B	
ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 02/12/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/840,063	Applicant(s) ZENG ET AL.	
	Examiner PAUL YANCHUS III	Art Unit 2115	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendments filed on 10/26/17*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-11 and 13-19*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☒ All b) ☐ Some *c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/26/17
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/PAUL YANCHUS III/
Primary Examiner, Art Unit 2115
February 5, 2018

DETAILED ACTION

This office action is in response to amendments filed on 10/26/17.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Allowable Subject Matter

Claims 1-11 and 13-19 are allowed.

Election/Restrictions

Newly submitted claims 20-40 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Claims 20-40 are directed to a power supply apparatus embodiment that includes a bearing plate and insulation material, while claims 1-11 and 13-19 are directed to a different power supply apparatus embodiment that includes power circuitry such as power switches or power converters.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 20-40 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

This application is in condition for allowance except for the presence of claims 20-40 directed to a power supply apparatus embodiment that includes a bearing plate and insulation material, which have been constructively non-elected without traverse. Accordingly, claims 20-40 have been cancelled.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL YANCHUS III whose telephone number is (571)272-3678. The examiner can normally be reached on Mon-Fri 9AM-5PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ali can be reached on (571) 272-4105. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/PAUL YANCHUS III/
Primary Examiner, Art Unit 2115
February 5, 2018

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14840063
Filing Date	2015-08-31
First Named Inventor	Jian-Hong ZENG
Art Unit	2115
Examiner Name	YANCHUS III, PAUL B
Attorney Docket Number	TWT04064/US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	1332512	CN	A	2002-01-23	ZHONGXING COMM CO LTD SHENZHEN		
	2	103596365	CN	A	2014-02-19	SHANGHAI INST SPACE POWER SOURCES		
	3	103872036	CN	A	2014-06-18	SAMSUNG ELECTRO MECH		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /Z.Y./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14840063
	Filing Date	2015-08-31
	First Named Inventor	Jian-Hong ZENG
	Art Unit	2115
	Examiner Name	YANCHUS III, PAUL B
	Attorney Docket Number	TWT04064/US

	4	103824853	CN	A	2014-05-28	SILERGY SEMICONDUCTOR TECHNOLOGY HANGZHOU CO LTD		

If you wish to add additional Foreign Patent Document citation information please click the Add button [Add]

NON-PATENT LITERATURE DOCUMENTS [Remove]

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		

If you wish to add additional non-patent literature document citation information please click the Add button [Add]

EXAMINER SIGNATURE

Examiner Signature	/PAUL B YANCHUS III/	Date Considered	02/05/2018

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /P.B.Y./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S60	2	("20080101025" | "20120173892").PN.	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S61	3	("2008/0101025").URPN.	USPAT	OR	OFF	2018/02/05 10:13
S62	13	("20030198033" | "20040218367" | "4628407" | "4916575" | "5734555" | "5801924" | "6151215" | "6816378" | "6819562" | "6979784" | "7005586" | "7072185" | "7289328").PN.	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S63	8	("6979784").URPN.	USPAT	OR	OFF	2018/02/05 10:13
S64	20	("20020172022" | "20030002268" | "20030057548" | "4616655" | "5136471" | "5313096" | "5315069" | "5574630" | "5894411" | "6239485" | "6304450" | "6326647" | "6356448" | "6452113" | "6452804" | "6490160" | "6501103" | "6556455" | "6558169" | "6642730").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/02/05 10:13
S65	31	("6400566" | "6483704" | "6621701" | "5587882" | "6058013" | "4462462" | "5966291" | "5995370" | "4965710" | "6414867" | "6504722" | "5548090" | "5986887" | "6285550" | "5801924" | "6212076" | "6239366" | "5214563" | "5828125" | "5930115" | "5729433" | "5804872" | "6219236" | "6064573" | "6166937" | "5734555" | "5901040" | "6191945" | "6462410" | "6490161" | "5862038").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/02/05 10:13
S66	220	(power with stack$4) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S67	32	(stack$4 with (regulator$1 or converter$1)) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S68	0	(vertical$2 with power with stage$1) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S69	29	(vertical$2 with (regulator$1 or converter$1)) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S70	227	(power with vertical$2) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S71	19	S66 and S70	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13

S72	12	("20040179339" | "3904934" | "20010000053" | "20050024963" | "6661690" | "20060220224" | "20040173894" | "5266912" | "6540525" | "6664617" | "20040225853" | "6864569").PN.	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S73	2	("6864569").URPN.	USPAT	OR	OFF	2018/02/05 10:13
S74	12	("5707242" | "5805596" | "5847985" | "5963464" | "6049467" | "6101089" | "6109929" | "6431879" | "6476476" | "6477593" | "6552914" | "6731514").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/02/05 10:13
S75	5262	(vertical$2 or stack$2) same (power adj1 densit$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/02/05 10:13
S76	2111	(vertical$2 or stack$2) with (power adj1 densit$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/02/05 10:13
S77	111	(vertical$2 or stack$2) with (power adj1 pressur$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/02/05 10:13
S78	353	shar$4 near3 (magnetic adj1 core)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/02/05 10:13
S79	14	S78 same (vertical$2 or stack$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/02/05 10:13
S80	131	S78 and (vertical$2 or stack$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/02/05 10:13
S81	2	S78 and ((regulator$1 or converter$1) near4 (vertical$2 or stack$4))	US-PGPUB; USPAT; USOCR	OR	OFF	2018/02/05 10:13
S82	56	S78 same (regulator$1 or converter$1)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/02/05 10:13
S83	11	S78 same (stage$1)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/02/05 10:13
S84	18	("4437235" | "5191404" | "5323060" | "5726612" | "5910885" | "6051886" | "6313998" | "6333562" | "6472758" | "6531784").PN. OR ("6801440").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/02/05 10:13
S85	9	S70 same mold$4	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S86	46	S70 and mold$4	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S87	1288	(vertical$2 or stack$2) with (power near6	US-	OR	OFF	2018/02/05

		stage$1)	PGPUB; USPAT; USOCR			10:13
S88	3	(stack$4 with power with stage$1) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S89	204	(stack$4 with (power adj3 stage$1))	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S90	135	(stack$4 near6 (power adj3 stage$1))	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S91	1	"7526634".pn.	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S92	3100	(stack$4) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S93	969	S92 and g06f$.cpc.	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S94	8945	(stack$4 with (regulator$1 or converter$1))	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S95	32	S94 same motherboard$1	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S96	105	(vertical$2 near6 (power adj3 stage$1))	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S100	3347	(stack$4 near4 (regulator$1 or converter$1))	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13
S111	1357	((stack$4 or vertical$1) with (regulator$1 or converter$1)) and molding$1	US-PGPUB; USPAT	OR	OFF	2018/02/05 10:13

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	488291	g06f$.cpc.	USPAT	OR	OFF	2018/02/05 10:27
L2	2	1 and (side adj1 facet).clm.	USPAT	OR	OFF	2018/02/05 10:27

2/ 5/ 2018 10:28:28 AM
C:\ Users\ pyanchus\ Documents\ EAST\ Workspaces\ 14840063.wsp

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14840063	ZENG ET AL.
	Examiner	**Art Unit**
	PAUL YANCHUS III	2115

CPC						
Symbol					**Type**	**Version**
G06F		1	/	26	F	2013-01-01
G06F		1	/	20	I	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	18	
/PAUL YANCHUS III/ Primary Examiner.Art Unit 2115	2/5/18	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

U.S. Patent and Trademark Office

Part of Paper No. 20180205

IPR2024-00715 EX. 2005

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14840063	ZENG ET AL.
	Examiner	**Art Unit**
	PAUL YANCHUS III	2115

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
		G	0	6	F	1 / 26 (2006.01.01)						
CROSS REFERENCE(S)												
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)											

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	18	
/PAUL YANCHUS III/ Primary Examiner.Art Unit 2115	2/5/18	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

U.S. Patent and Trademark Office

Part of Paper No. 20180205

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14840063	ZENG ET AL.
	Examiner	**Art Unit**
	PAUL YANCHUS III	2115

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	16	17		33										
2	2	17	18		34										
3	3	18	19		35										
4	4		20		36										
5	5		21		37										
6	6		22		38										
7	7		23		39										
8	8		24		40										
9	9		25												
10	10		26												
11	11		27												
	12		28												
12	13		29												
13	14		30												
14	15		31												
15	16		32												

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 18	
/PAUL YANCHUS III/ Primary Examiner.Art Unit 2115 (Primary Examiner)	2/5/18 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 4

U.S. Patent and Trademark Office

Part of Paper No. 20180205

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14840063	ZENG ET AL.
	Examiner	Art Unit
	PAUL YANCHUS III	2116

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (see attached)	1/9/17	PBY
Inventor Name Search in PALM	1/9/17	PBY
NPL (Google)	1/9/17	PBY
Updated EAST Search	7/22/17	PBY
Updated EAST Search	2/5/18	PBY

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
G06F	All	2/5/18	PBY

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BIB DATA SHEET

CONFIRMATION NO. 8903

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
14/840,063	08/31/2015	713	2115	TWT04064/US

APPLICANTS

DELTA ELECTRONICS, INC., Taoyuan City, TAIWAN;

INVENTORS

Jian-Hong ZENG, Taoyuan City, TAIWAN;
Chao YAN, Taoyuan City, TAIWAN;
Pei-Qing HU, Taoyuan City, TAIWAN;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

CHINA 201410442972.6 09/02/2014

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

09/14/2015

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /PAUL B YANCHUS III/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		TAIWAN	11	18 ~~19~~	3

ADDRESS

JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

TITLE

POWER SUPPLY APPARATUS

FILING FEE RECEIVED		
3960	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/840,063	Filing Date 08/31/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	10/26/2017	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 39	Minus	** 20	= 19	X $80 =	1520
	Independent (37 CFR 1.16(h))	* 5	Minus	***3	= 2	X $420 =	840
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**2360**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
TAMARA DARKO

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant :	ZENG ET AL.	Attorney Docket No. :	TWT04064/US
Serial No. :	14/840,063	Group Art Unit:	2115
Filed :	2015/08/31	Examiner:	YANCHUS III, PAUL B
Title:	POWER SUPPLY APPARATUS		

AMENDMENT AND RESPONSE TO OFFICE ACTION

Honorable Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

In response to the Official Action mailed July 27, 2017, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Amendments to the Drawings begin on page 12 of this paper.

Remarks and Responses begin on page 13 of this paper.

Respectfully submitted,

/James Lynn O'Sullivan/

Date：October 27, 2017

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IPR2024-00715 EX. 2005

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Agent for Applicant(s)

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Previously Presented) A power supply apparatus, comprising:

a power unit electrically connected with a motherboard, comprising a first base plate, at least a power switch chip allocated at the first base plate and a plurality of pads;

a control unit stacked with the power unit, comprising a second base plate and at least a control chip for controlling the power switch chip turn on/ off in the power unit and a plurality of pads; and

a plurality of pins for electrically connecting the power unit to the control unit and mother board and allocated at periphery of the power unit and control unit;

wherein the plurality of pads of the power unit and control unit are allocated on side facet of the first base plate and second base plate respectively, both plurality of pads of the power unit and control unit are electrically connected with the plurality of pins so that the power unit and the control unit are electrically connected with each other, the power supply apparatus provides a power source for a load in the neighborhood thereof on the motherboard.

2. (Previously Presented) The power supply apparatus of claim 1,

wherein the first base plate and the second base plate are in a substantially same size.

3. (Original) The power supply apparatus of claim 1, wherein the second base plate integrates a power switch chip to improve area utilization thereof.

4. (Original) The power supply apparatus of claim 1, further comprising molding material, wherein the molding material encapsulates the power unit and control unit respectively, the plurality of pads of the power unit and control unit emerges from molding material respectively.

5. (Original) The power supply apparatus of claim 4, wherein the molding material of the control unit has a plurality of recesses reserved for connection with the pins thereof.

6. (Original) The power supply apparatus of claim 4, wherein the molding material encapsulates two sides of the power unit.

7. (Original) The power supply apparatus of claim 6, wherein the power unit further comprises bottom pads emerged from one side of power unit that is encapsulated by the molding material for adjacent electrical connection thereof.

8. (Original) The power supply apparatus of claim 1, further comprising another power unit stacked with the power unit and the control unit, wherein

the another power unit is parallel connected with the power unit and controlled by the control unit.

9. (Original) The power supply apparatus of claim 8, wherein each of the power unit and the another power unit has a magnetic device, the magnetic devices of the power unit and the another power unit share the same magnetic core.

10. (Previously Presented) The power supply apparatus of claim 1, wherein the plurality of pins cover outer surface of the power unit and the control unit respectively.

11. (Original) The power supply apparatus of claim 1, wherein the power unit is the one close to the motherboard, the control unit is the other one stacked on the power unit.

12. (Canceled)

13. (Original) The power supply apparatus of claim 1, further comprising:

a heat sink, attached with the power unit to improve heat dissipation.

14. (Previously Presented) A power supply apparatus, comprising:

a first stage power converter receiving a power source from a mother board and configured with a plurality of pads located on side facet thereof;

a second stage power converter configured with a plurality of pads

located on side facet thereof and stacked with the first stage power converter to receive an output of the first stage power converter to provide a power to a load in adjacent area thereof on the motherboard; and

a plurality of pins connected with the pads of the first or/and second stage power converter and the motherboard to realize the electrical connection therebetween.

15. (Original) The power supply apparatus of claim 14, wherein the output voltage of the second stage power converter is lower than the output voltage of the first stage power converter.

16. (Previously Presented) The power supply apparatus of claim 14, wherein the first stage converter and the second stage converter are configured in a substantially same size.

17. (Previously Presented) A power supply apparatus, comprising:

a first unit electrically connected with a motherboard, comprising a first base plate, and at least a power switch chip allocated at the first base plate;

a second unit stacked with the first unit;

a plurality of pins for electrically connecting the first unit to the second unit and mother board and allocated at periphery of the first unit ; and

a plurality of pads distributed along a lateral side of the first unit and a lateral side of the second unit, and electrically coupled with the plurality of pins, wherein the plurality of pins include surface-mount pins, and are distributed along the outer surface of the first unit and the second unit, so that the first unit and the second unit could electrically connected with each other, the

power supply apparatus provides a power source for a load in the neighborhood thereof on the motherboard.

18. (Previously Presented) The power supply apparatus of claim 17, wherein the second unit has a surface facing the first unit and a plurality of connection pads disposed on the surface.

19. (Currently Amended) The power supply apparatus of claim 18, wherein the pins extend along ~~extends along~~ the out surface of the first unit to connect the connection pad of the second unit with the first unit.

20. (New) A power supply apparatus, comprising:

a bearing plate;

insulation material formed on two opposite surfaces of the bearing plate; and

a plurality of pins electrically connected to the bearing plate and allocated along lateral sides of the insulation material.

21. (New) The power supply apparatus of claim 20, further comprising:

a plurality of first pads disposed on lateral sides of the bearing plate.

22. (New) The power supply apparatus of claim 21, wherein the plurality of pins are electrically connected to the plurality of first pads, and the plurality of first pads are electrically connected to the bearing plate.

23. (New) The power supply apparatus of claim 22, wherein two

terminals of each of the pins have two SMD pads, wherein the two SMD pads of each of the pins are extending to an upper surface and a lower surface of the insulation material, respectively.

24. (New) The power supply apparatus of claim 23, wherein edges of the upper surface and the lower surface of the insulation material have recesses, and the two SMD pads of each of the pins extend to the recesses at the upper surface and the lower surface of the insulation material.

25. (New) The power supply apparatus of claim 21, further comprising:

at least one second pad, wherein the second pad is located at an upper surface or a lower surface of the insulation material and the second pad is electrically connected to the bearing plate.

26. (New) The power supply apparatus of claim 20, wherein the two opposite surfaces of the bearing plate are covered with the insulation material, and at least one lateral side of the bearing plate is exposed from the insulation material.

27. (New) The power supply apparatus of claim 26, further comprising:

at least one second pad, wherein the second pad is located at an upper surface or a lower surface of the insulation material and the second pad is electrically connected to the bearing plate.

28. (New) The power supply apparatus of claim 20, wherein the bearing plate is embedded in the insulation material to form a cuboid body,

edges of an upper surface and a lower surface of the cuboid body have recesses, and two terminals of each of the pins have SMD pads extending to the recesses at the upper surface and the lower surface of the cuboid body.

29. (New) The power supply apparatus of claim 28, further comprising:

a plurality of first pads disposed on lateral sides of the cuboid body, wherein the plurality of pins are electrically connected to the plurality of first pads, and the plurality of first pads are electrically connected to the bearing plate.

30. (New) The power supply apparatus of claim 28, further comprising:

at least one second pad, wherein the second pad is located at the upper surface or the lower surface of the cuboid body and the second pad is electrically connected to the bearing plate.

31. (New) The power supply apparatus of claim 20, wherein the power supply apparatus is a power unit or a control unit.

32. (New) The power supply apparatus of claim 20, wherein the power supply apparatus is a non-regulated isolated transforming module, wherein a regulated module is stacked on the non-regulated isolated transforming module and electrically connected with at least one of the plurality of pins.

33. (New) The power supply apparatus of claim 20, wherein two terminals of each of the pins have two SMD pads, wherein the two SMD pads of each of the pins are extending to an upper surface and a lower surface of

the insulation material, respectively.

34. (New) A power supply apparatus, comprising:

a bearing plate;

insulation material formed on two opposite surfaces of the bearing plate; and

at least one pin electrically connected to the bearing plate and contacting at least part of the insulation material.

35. (New) The power supply apparatus of claim 34, further comprising:

at least one first pad disposed on a lateral side of the bearing plate, wherein the pin is electrically connected to the first pad, and the first pad is electrically connected to the bearing plate.

36. (New) The power supply apparatus of claim 34, wherein the pin covers at least part of a lower surface, at least part of an upper surface of the insulation material and at least part of two lateral sides of the bearing plate.

37. (New) The power supply apparatus of claim 36, wherein at least one lateral side of the bearing plate is exposed from the insulation material.

38. (New) The power supply apparatus of claim 36, wherein two terminals of the pin have SMD pads located at the upper surface of the insulation material.

39. (New) The power supply apparatus of claim 34, wherein the

bearing plate is embedded in the insulation material to form a cuboid body, and the pin covers at least part of a lower surface, at least part of an upper surface and at least part of two lateral sides of the cuboid body.

40. (New) The power supply apparatus of claim 39, wherein two terminals of the pin have SMD pads located at the upper surface of the cuboid body.

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Amendments to the Drawings

Attached hereto is a replacement sheet of drawings that comply with the provisions of 37 C.F.R. § 1.84. This sheet, in Fig. 25, previously omitted element "pad 3440' " has been added. Support for the amendment to drawings is found in as-filed specification.

It is respectfully requested that the corrected drawings be approved and made a part of the record of the above-identified application.

Remarks and Responses

The Examiner is thanked for the thorough examination of the present application. The Office Action, however, tentatively rejected claims 1-11 and 13-19. In response, new claims have been amended to more clearly define over the cited art. These new claims are supported by Figures 4, 18, 25, 26 and 27, and the related portions of as-filed specification, such as paragraphs [0061], [0078], [0100] and [0101]. Accordingly, the amendments do not introduce any new matter.

Claim Rejection - 35 U.S.C. § 102 and 103

Applicant respectfully requests reconsideration of the rejections for at least the reasons that follow.

> *A claim is anticipated only if **each and every** element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as **complete detail** as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).*
>
> *"All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).*

First, the Examiner's attention is drawn to Fig. 1 of *Matsumoto* (US 20050189566 A1), which is reproduced below. Fig. 1 of *Matsumoto* only shows that the conductor land patterns 4 are provided on the **top surface** of

the circuit boards 2. It is clear that *Matsumoto* fails to disclose that the conductor land patterns 4 are allocated on **side facet** of the circuit boards 2.

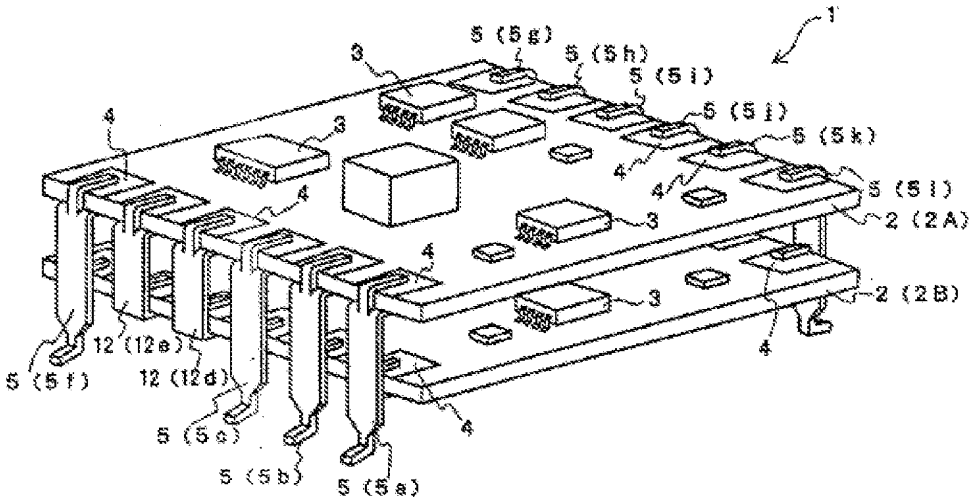


Fig. 1 of *Matsumoto*

Accordingly, *Matsumoto* fails to describe each and every element (e.g., the plurality of pads of the power unit and control unit are allocated on **side facet** of the first base plate and second base plate respectively) as set forth in the claim 1.

Similarly, *Matsumoto* also fails to describe each and every element (e.g., a first stage power converter configured with a plurality of pads located on **side facet** thereof, and a second stage power converter configured with a plurality of pads located on **side facet** thereof) as set forth in the claim 14.

Similarly, *Matsumoto* still also fails to describe each and every element (e.g., a plurality of pads distributed along a **lateral side** of the first unit and a lateral side of the second unit) as set forth in the claim 17.

In view of the foregoing remarks, it is respectfully submitted that the prior art utilized by the Office Action fails to disclose all claim limitations

recited in independent claims 1, 14 and 17. Accordingly, reconsideration and withdrawal of this portion of the 35 U.S.C. § 103 rejections are respectfully requested. Insofar as all remaining claims depend from claims 1, 14 and 17, the rejections of the remaining claims should be withdrawn for at least the same reasons. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Conclusions

For all of the aforementioned reasons, applicants submit that the specification and claims are now in proper form, and that the claims define patentably over the prior art of record. Therefore applicants respectfully request allowance for this case at the Examiner's earliest convenience.

The Commissioner is hereby authorized to charge Deposit Account 50-4669 for any deficiencies or credit for any over payments.

Respectfully submitted,

/James Lynn O'Sullivan/

_____

Date：October 27, 2017

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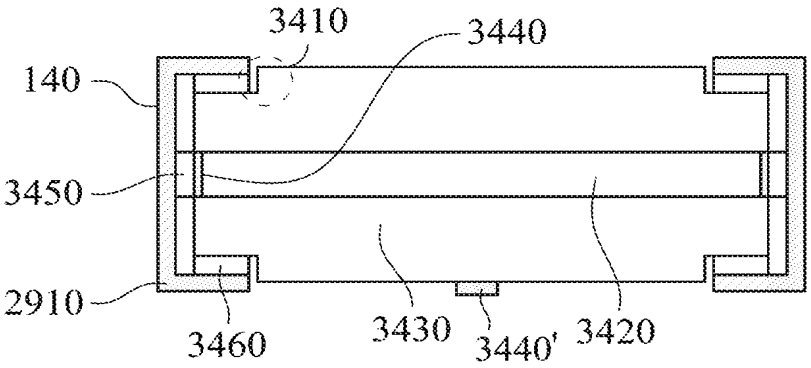


Fig. 25

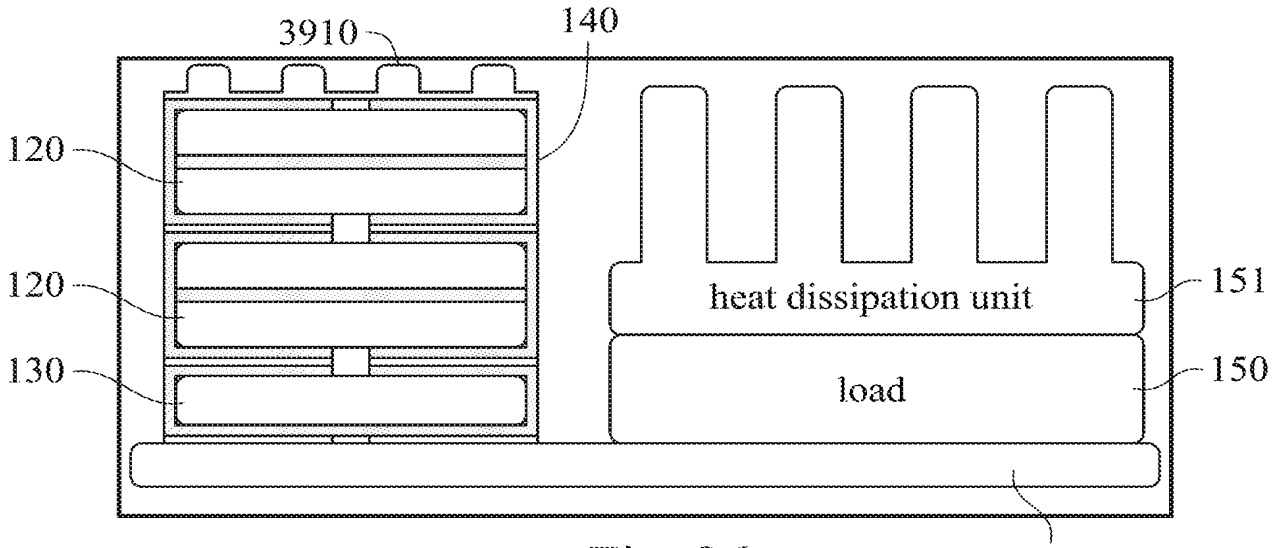


Fig. 26

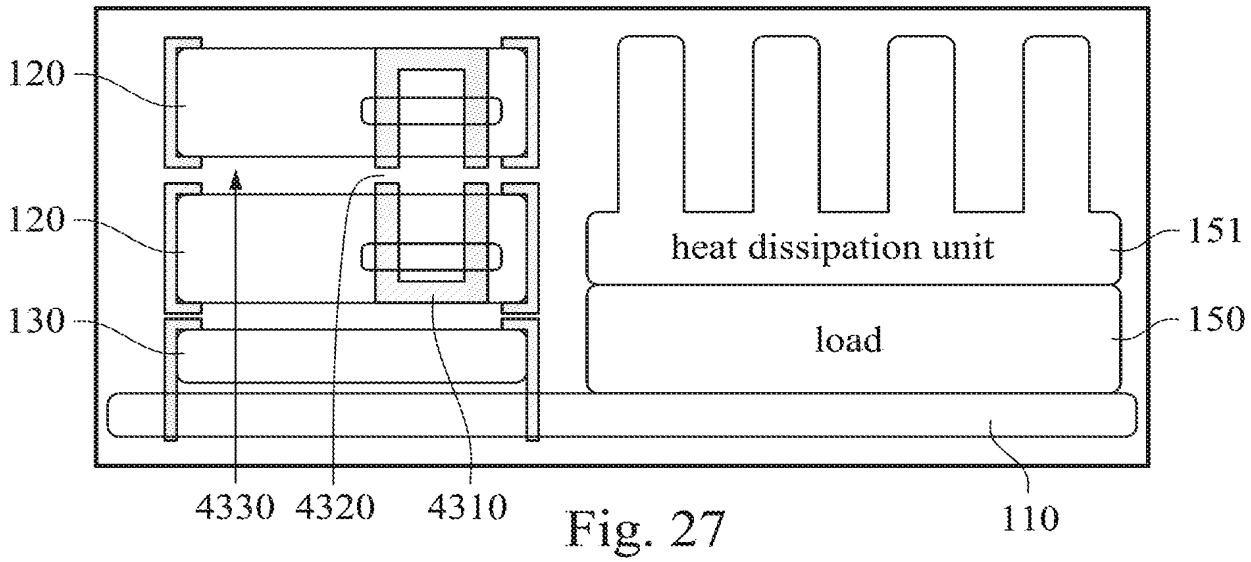


Fig. 27

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of：Jian-Hong ZENG	Confirmation No.：8903
Serial No.14/840,063	Group Art Unit：2115
Filed：August 31, 2015	Examiner：YANCHUS III, PAUL B
	Docket No. TWT04064/US

For：POWER SUPPLY APPARATUS

INFORMATION DISCLOSURE STATEMENT

U.S. PATENT AND TRADEMARK OFFICE
Commissioner for Patents
P.O.BOX 1450
ALEXANDRIA, VA 22313-1450,
U.S.A.

Dear Sir,

This information disclosure statement is filed in accordance with 37 C.F.R.§ §§1.56, 1.97, and 1.98, and specifically：

☐ under 37 CFR 1.97(b), or
(with Three months of filing national application；or date of entry of international application；or before mailing date of first office action on the merits；or before the mailing of a first office action after the filing of a request for continued examination under §1.114；whichever occur last)

☒ under 37 CFR 1.97(c) together with either a：
☒ Statement Under 37 C.F.R.1.97(e), or
☐ a fee under 37 CFR 1.17(p), or
(After the CFR 1.97(b) time period, but before the final office action or notice of allowance, whichever occurs first)

☐ under 37 CFR1.97(d) together with a：

IPR2024-00715 EX. 2005

☐ Statement Under 37 C.F.R.1.97(e), and

☐ a petition fee set forth in 37 CFR 1.17(p).

(Filed after final office action or notice of allowance, whichever occurs first, but before payment of the issue fee)

☒ At any time during the pendency of this application, please charge any fees required to Deposit Account pursuant to 37 CFR 1.25. The Commissioner is hereby requested to credit any overpayment to Deposit Account No. 504669.

☒ Applicant(s) submit herewith Form PTO SB/08A-08B-08a – Information Disclosure Statement by Applicant together with copies (where required) of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may or may not be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56. As required by 37 C.F.R. §1.98(a), a legible copy of each document is provided.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Forms SB/08A-08B-08a, as presently understood by the individual(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed in the form PTO SB/08A-08B-08a and is enclosed herewith.

The following rights are reserved by the Applicant(s)：the right to establish the patentability of the claimed invention over any of the listed document should they be applied as reference, and/or the right to prove that some of these documents may not be prior art, and/or the right to prove that some of these documents may not be enabling for the teachings they purport to offer.

This statement should not be construed as a representation that an exhaustive search has been made, or that information more material to the examination of the present application does not exist. Any statements or identifications regarding the relevance of any portion(s) of cited references should not be construed as a representation that the most relevant portion(s) have been identified, and the absence of such statements or identifications should not be construed as representations that there are no relevant portion(s). The Examiner is specifically requested not to rely

solely on the materials submitted herewith. The Examiner is requested to conduct an independent and thorough review of the documents, and to form independent opinion as to their significance.

It is requested that the information disclosed herein be made of record in this application and that the Examiner initial and return a copy of the enclosed PTO SB/08A-08B-08a to indicate the documents have been considered.

Respectfully submitted,

/James Lynn O'Sullivan /

_____

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(Not for submission under 37 CFR 1.99)

Application Number	14840063
Filing Date	2015-08-31
First Named Inventor	Jian-Hong ZENG
Art Unit	2115
Examiner Name	YANCHUS III, PAUL B
Attorney Docket Number	TWT04064/US

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	1	1332512	CN	A	2002-01-23	ZHONGXING COMM CO LTD SHENZHEN		
	2	103596365	CN	A	2014-02-19	SHANGHAI INST SPACE POWER SOURCES		
	3	103872036	CN	A	2014-06-18	SAMSUNG ELECTRO MECH		

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14840063
	Filing Date	2015-08-31
	First Named Inventor	Jian-Hong ZENG
	Art Unit	2115
	Examiner Name	YANCHUS III, PAUL B
	Attorney Docket Number	TWT04064/US

	4	103824853	CN	A	2014-05-28	SILERGY SEMICONDUCTOR TECHNOLOGY HANGZHOU CO LTD		

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14840063
	Filing Date	2015-08-31
	First Named Inventor	Jian-Hong ZENG
	Art Unit	2115
	Examiner Name	YANCHUS III, PAUL B
	Attorney Docket Number	TWT04064/US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/James Lynn O'Sullivan/	Date (YYYY-MM-DD)	2017-10-27
Name/Print	James Lynn O'Sullivan	Registration Number	65618

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Bibliographic data: CN1332512 (A) — 2002-01-23

Improved modular power source structure

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Applicant(s): ZHONGXING COMM CO LTD SHENZHEN [CN] ± (ZHONGXING COMMUNICATION CO., LTD., SHENZHEN CITY, ; ZHONGXING COMMUNICATION CO., LTD., SHENZHEN)

Classification: - international: ***H01L23/36; H02M1/00; H05K7/20;*** (IPC1-7): H01L23/36; H02M1/00; H05K7/20

- cooperative:

Application number: CN2000125619 20000929

Priority number(s): CN2000125619 20000929

Also published as: CN1118922 (C)

Abstract of CN1332512 (A)

The improved structure of modular power source includes: heat conducting metal underplate with one layer of slightly smaller heat conducting insulating material; magnetic device and power tube with bottom adhered to the heat conducting insulating material and upwards bending pins welded to the printed circuit board; the printed circuit board with bottom layer for setting power circuit and top layer for setting control device; and pins welded to the printed circuit board. The present invention has simple structure, low cost, simple manufacture process and no common-mode noise.

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权利要求书2页 说明书4页 附图页数2页

[54]发明名称 一种模块电源的改进结构

[57]摘要

本发明公开了一种模块电源的改进结构，其结构为：在模块的底层是导热金属基板208，其上贴一层面积稍小的导热绝缘材料207；磁性器件205、功率管206的底面粘贴在导热绝缘材料207上；磁性器件205的引脚向上引出，功率管206的引脚向上折弯，一起焊接在印制线路板204上；印制线路板204的底层主要放置功率线路，顶层主要放置控制器件202；插针一201和插针二203焊接在印制线路板204上。从而解决了传统电源结构复杂、成本过高、工艺繁杂而且容易产生共模噪声的问题。

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权利要求书

1、一种模块电源的改进结构，包括插针一（201）、插针二（203）、控制元器件（202）、印制线路板（204）、磁性元件（205）、功率管（206），其特征在于它还包括导热金属基板（208）和导热绝缘材料（207）；

所述导热金属基板（208）位于模块的底层；

所述导热绝缘材料（207）位于所述导热金属基板（208）上面，其面积比导热金属基板稍小；

所述磁性器件（205）和所述功率管（206）的底面粘贴在所述导热绝缘材料（207）上；

所述磁性器件（205）的引脚向上引出，所述功率管（206）的引脚向上折弯，一起焊接在所述印制线路板（204）上；

所述控制器件（202）位于所述印制线路板（204）上层面上；

所述插针一（201）和所述插针二（203）焊接在所述印制线路板（204）上。

2、如权利要求 1 所述模块电源的改进结构，其特征在于所述导热绝缘材料（207）是双面导热绝缘胶带。

3、如权利要求 1 所述模块电源的改进结构，其特征在于所述导热金属基板（208）是铝板。

4、如权利要求 1 所述模块电源的改进结构，其特征在于所述导热金属基板（208）是铜板。

5、如权利要求 1 所述模块电源的改进结构，其特征在于所述磁性器件（205）包括电感和变压器。

6、如权利要求 1 所述模块电源的改进结构，其特征在于功率线路放置在所述印制线路板（204）的下层面上。

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00.10.13

7、如权利要求 1 所述模块电源的改进结构，其特征在于所述印制线路板（204）是多层印制线路板。

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说 明 书

一种模块电源的改进结构

本发明涉及电源领域，尤其涉及开关电源中的模块电源。

模块电源作为开关电源的一个分支，目前在通讯、航天、汽车等领域内得到了越来越广泛的应用。其中高功率密度模块电源为目前主要的发展趋势之一，其体积和散热是必须考虑的问题，如果没有一个良好的散热系统，不仅影响模块电源的工作，而且会造成某些器件因过热而损坏。在传统的工艺中，通常采用铝基板工艺方案来改善散热效果。该方案将不需要散热的控制电路放在上层的印制板上，发热的功率管和磁性器件放在下层铝基板上，两层板通过两个插针实现电器和物理连接。这样可以利用铝基板良好的散热性能将功率管和磁性器件产生的热量散发出去，降低功率管和磁性器件的温度，使模块的功率密度可以提高到 120W/inch^3。但该方案存在的缺点也是很明显的；首先就是铝基板的加工需要多层保护，印制板加工费用较高，可以达到普通单层印制板的 30 倍以上，多层印制板的加工费更是昂贵；其次是铝基板的回流工艺复杂，焊接至少需要八个温区的热板炉，这在一般的回流设备上实现起来比较困难；另外，铝基板上非弹性焊盘贴装的器件尺寸不能超过 1812，否则热疲劳容易造成器件的失效。虽然可以把这些器件焊接到陶瓷基片上，再通过导热粘接剂粘接到铝基板上，但这样操作工艺变得更为复杂；采用这一工艺方案，还有其他的一些缺点，如在铝基板上焊插针时需要专用的卡具来支撑以及铝基板上功率器件器件与铝板之间的分布电容大，输出端容易产生共模噪声等。

本发明的目的是克服上述铝基板工艺的缺点，提供一种结构简单、成本低廉、工艺简单而且能够有效避免共模噪声的模块电源的改进结构。

为实现上述目的，本发明构造了一种模块电源的改进结构，该结构主要由以下几部分组成：插针一 201 和插针二 203、控制元器件 202、印制线路板 204、

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磁性器件 205、功率管 206、导热绝缘材料 207 和导热金属基板 208，其中导热金属基板 208 可以采用铝板、铜板或其他具有良好的导热性能的金属材料。具体结构如下：在模块的底层是导热金属基板 208，上面贴一层面积比导热金属基板稍小的导热绝缘材料 207，磁性器件 205、功率管 206 的底面粘贴在导热绝缘材料 207 上，磁性器件 205 的引脚向上引出，功率管 206 的引脚向上折弯，一起焊接在印制线路板 204 上，印制线路板 204 的底层主要放置功率线路，印制线路板 204 的顶层主要放置控制器件 202，插针一 201 和插针二 203 焊接在印制线路板 204 上。

由于本发明采用导热金属基板替代传统工艺方案中的铝基板，不仅极大地降低了成本，而且也避免了铝基板复杂的焊接工艺；另外，主功率线路放在上层印制板的底层，减少了共模干扰；对于两个插针，由于全部放在上层印制线路板上，焊接时也不需要专门的卡具；铝板上没有非弹性焊盘贴装的大尺寸器件，不会由于热疲劳而造成器件失效，从而真正地实现了降低模块的成本，简化模块的加工工艺，提高模块的性能价格比的目的。

下面结合附图和实施例对本发明作进一步的详细描述：

图 1 是传统工艺方案的结构框图；

图 2 是本发明的结构框图；

图 3 是作为本发明第一个实施例的结构框图；

图 4 是作为本发明第二个实施例的结构框图。

图 1 中传统的铝基板工艺方案是将不需要散热的控制电路 102 放在上层的印制板 104 上，发热的功率管 105 和磁性器件 106 放在下层铝基板上，两层板通过插针一 101 和插针二 103 实现电器和物理连接。这样做不仅成本过高，而且制造工艺也比较复杂，不能有效地避免共模噪声。

在图 2 中，本方案采用导热金属基板 208 代替铝基板工艺方案中的铝基板 107，利用导热绝缘材料 207 将功率管 206 和磁性器件 205 粘接在导热金属基板

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208 上，功率管 206 的引脚向上折弯，磁性器件 205 引脚向上引出，一起焊接到上层印制线路板 204 上，这样主功率线路放在上层印制板 204 的底层，插针一 201 和插针二 203 全部放在上层印制线路板 204 上。

图 3 所示实施例主要由以下几个部分组成：插针一 301、插针二 303、控制元器件 302、四层印制线路板 304、变压器 305、功率管 306、电感 307、双面导热绝缘胶带 308 和铝板 309。具体结构如下：在模块的底层是铝板 309，上面贴上一层面积比铝板稍小的双面导热绝缘胶带 308，变压器 305、电感 307、功率管 306 的底面粘贴在双面导热绝缘胶带 308 上，电感 307、变压器 305 的引脚向上引出，功率管 306 的引脚向上折弯，一起焊接在四层印制线路板 304 上，印制线路板 304 的底层主要放置功率线路，印制线路板 304 的顶层主要放置控制器件 302，插针一 301 和插针二 303 焊接在印制线路板 304 上。从电路原理上讲，电感 307、变压器 305 和功率管 306 这些功率器件是主要的发热源，功率线路只要设计得合理，功率线路的发热是可以忽略不计的。也就是说在热设计时只要将电感 307、变压器 305 和功率管 306 的热量散发出去即可。由于双面导热绝缘胶带 308 具有良好的导热特性，所以这种结构能有效地将功率器件的热量通过铝板 309 散发出去。这样就会降低功率管 306、变压器 305 和电感 307 的温度，达到散热之目的。由于直接用铝板 309 代替铝基板 107，这样大大减少了用于散热的材料成本；由于只要将功率器件通过双面导热绝缘胶带 308 粘贴在铝板 309 上，这样避免了铝基板复杂的加工工艺，简化了模块的加工工艺，减少了加工成本；又由于铝板上除了功率器件外没有其他器件，所以也不存在铝基板上大尺寸器件热疲劳容易造成器件的失效的缺点；同时插针一 301 和插针二 303 都放在印制线路板 304 上，在焊接时不需要专门的卡具；由于功率线路放在印制线路板 304 的底层，铝板 309 只是起到散热作用，功率管 306 与铝板 309 之间的分布电容对输出共模噪声的影响会大大减小。

图 4 所示实施例 2 与实施例 1 不同之处在于以铜板代替铝板，铜板同样具有良好的导热性能和成本便宜的特点。本实施例主要由以下几个部分组成：插针一 401、插针二 403、控制元器件 402、四层印制线路板 404、变压器 405、

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功率管 406、电感 407、双面导热绝缘胶带 408 和铜板 409。具体结构如下：在模块的底层是铜板 409，上面贴上一层面积比铜板稍小的双面导热绝缘胶带 408，变压器 405、电感 407、功率管 406 的底面粘贴在双面导热绝缘胶带 408 上，电感 407、变压器 405 的引脚向上引出，功率管 406 的引脚向上折弯，一起焊接在四层印制线路板 404 上，印制线路板 404 的底层主要放置功率线路，印制线路板 404 的顶层主要放置控制器件 402，插针一 401 和插针二 403 焊接在印制线路板 404 上。由于双面导热绝缘胶带 408 具有良好的导热特性，所以这种结构能有效地将功率器件的热量通过铜板 409 散发出去。这样就会降低功率管 406、变压器 405 和电感 407 的温度，达到散热之目的。

本发明采用导热金属基板替代铝基板，降低了模块的成本，简化了模块的加工工艺，提高了模块的性能价格比，是一种很经济实用的方案。

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说 明 书 附 图

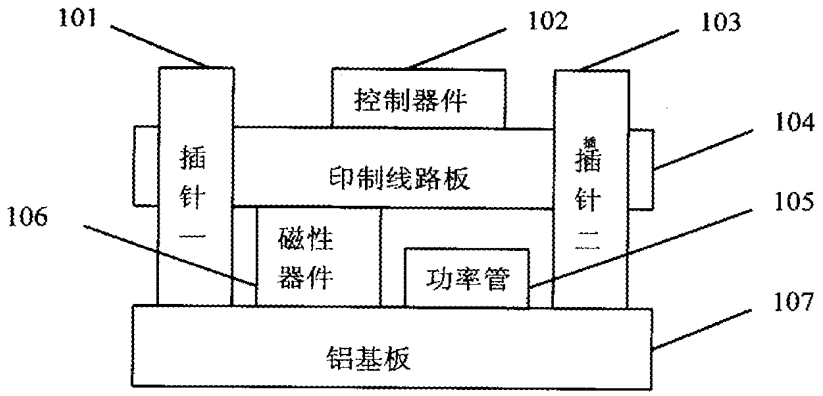

101
102
103
控制器件
插针一
印制线路板
插针二
104
106
磁性器件
功率管
105
107
铝基板

图 1

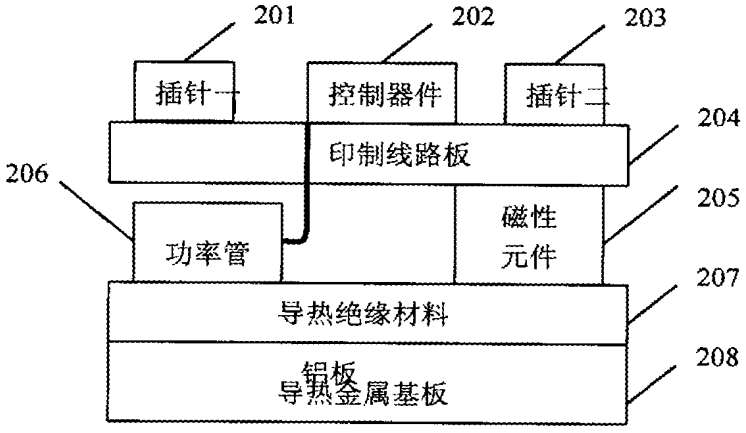

201
202
203
插针一
控制器件
插针二
204
印制线路板
206
功率管
磁性元件
205
207
导热绝缘材料
铝板
208
导热金属基板

图 2

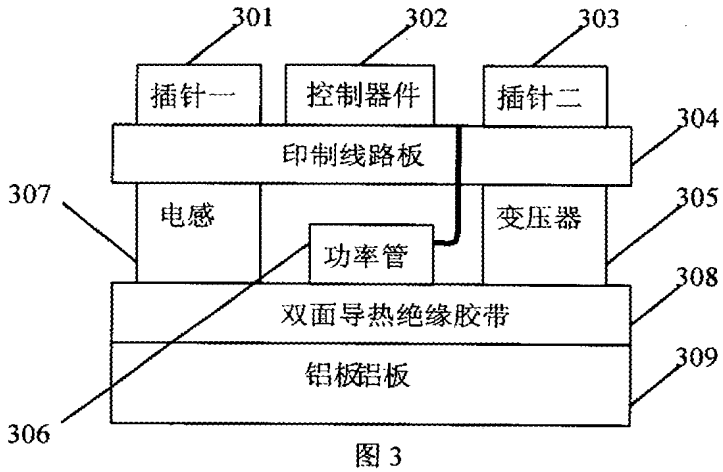


图 3

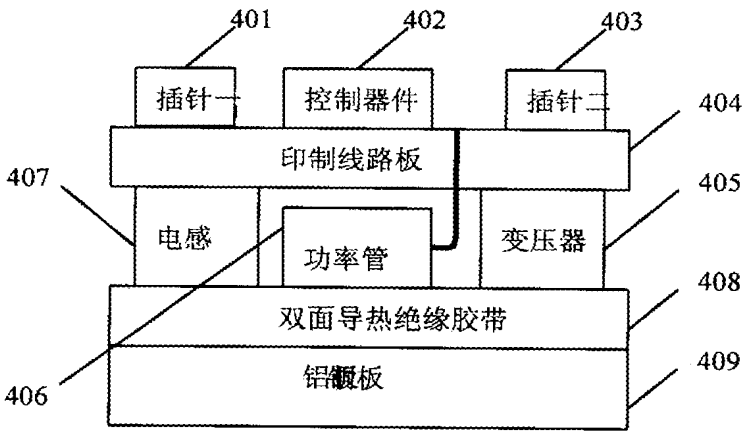


图 4

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Bibliographic data: CN103596365 (A) — 2014-02-19

Installation structure of power tubes and printed circuit board

Inventor(s): DAI YONGLIANG; LIU YUAN; SHI YUAN; ZHANG TINGTING; ZHOU JIAN; LIU YONG ± (DAI YONGLIANG, ; LIU YUAN, ; SHI YUAN, ; ZHANG TINGTING, ; ZHOU JIAN, ; LIU YONG)

Applicant(s): SHANGHAI INST SPACE POWER SOURCES ± (SHANGHAI INSTITUTE OF SPACE POWER-SOURCES)

Classification: **- international:** ***H05K1/18***
- cooperative:

Application number: CN20131614483 20131128 Global Dossier

Priority number(s): CN20131614483 20131128

Also published as: CN103596365 (B)

Abstract of CN103596365 (A)

The invention discloses an installation structure of power tubes and a printed circuit board. The installation structure comprises a power controller main structure, the printed circuit board and two rows of the power tubes, wherein the middle of the power controller main structure is provided with an installation groove; the printed circuit board is inserted into the installation groove; the two rows of the power tubes are installed on the power controller main structure and are located on the two sides of the printed circuit board, and pins of the power tubes are welded to the printed circuit board. The printed circuit board and the power tubes are fixedly connected with the power controller main structure through fasteners. The outer walls of the fasteners are provided with insulating sleeves in a sleeved mode. The installation structure effectively reduces space occupied by the power tubes in installation, reduces the size and the weight of a whole power controller structural part, and is beneficial for optimization design of high power density of a spacecraft power supply.

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(51)Int.Cl.
H05K 1/18(2006.01)

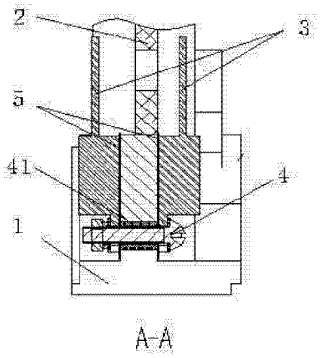
权利要求书1页 说明书2页 附图2页

(54)发明名称

一种功率管与印制电路板的安装结构

(57)摘要

本发明公开了一种功率管与印制电路板的安装结构，包含：电源控制器主结构，其中部位置处开设有安装槽；印制电路板，其插入在所述的安装槽内；两排功率管，其分别安装在电源控制器主结构上，且位于印制电路板两侧，功率管的引脚焊接与印制电路板上。印制电路板及功率管通过紧固件与电源控制器主结构固定连接。紧固件外壁上套设有绝缘套管。该结构有效地减小了功率管安装所占用的空间，降低了整个电源控制器结构件的体积和重量，有利于航天器电源高功率密度的优化设计。



A-A

CN 103596365 A

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1. 一种功率管与印制电路板的安装结构，其特征在于，包含：

电源控制器主结构（1），其中部位置处开设有安装槽（11）；

印制电路板（2），其插入在所述的安装槽（11）内；

两排功率管（3），其分别安装在电源控制器主结构上，且位于印制电路板（2）两侧，所述功率管（3）的引脚焊接与印制电路板（2）上。

2. 如权利要求 1 所述的功率管与印制电路板的安装结构，其特征在于，所述的印制电路板（2）及功率管（3）通过紧固件（4）与电源控制器主结构（1）固定连接。

3. 如权利要求 2 所述的功率管与印制电路板的安装结构，其特征在于，所述紧固件外壁上套设有绝缘套管（41）。

4. 如权利要求 1 或 2 所述的功率管与印制电路板的安装结构，其特征在于，所述的印制电路板（2）与安装槽（11）内壁之间设有绝缘导热垫片（5）。

5. 如权利要求 4 所述的功率管与印制电路板的安装结构，其特征在于，所述的绝缘导热垫片（5）采用非金属材料环氧玻璃布层压板。

6. 如权利要求 1 所述的功率管与印制电路板的安装结构，其特征在于，所述的电源控制器主结构（1）采用镁合金材料。

一种功率管与印制电路板的安装结构

技术领域

[0001] 本发明涉及航天电源控制领域，特别涉及一种功率管与印制电路板的安装结构。

背景技术

[0002] 提高功率密度是现今航天器电源系统的发展趋势，特别是在月球探测器的电源控制器设计中。相较于以往的航天器，现代探测器（如月球探测器）对电源控制器的体积、重量、热耗、力学性能等方面都提出了更高的要求。因此，在月球探测器电源控制器的设计过程中要充分考虑结构与电气性能的关系。其中，功率管不仅体积大，重量重，还要充分考虑其抗力学设计和发热的问题，这必然给电源控制器的整体布局和重量控制带来一定的影响。

[0003] 当前，在航天器电源控制器的功率管安装设计中，通常采用功率管壳体直接安装在电源控制器结构件上，功率管引脚垂直于印制板通过大的焊盘直插印制板的安装设计形式，但是，功率管壳体和其引脚本身长度占据电源控制器结构件大部分空间，致使模块空间极度浪费，此外功率管引脚贯穿印制板，势必降低印制板机械强度。这种功率管直插式安装于电源控制器的安装方式，根本不符合航天器电源小型化、轻量化的发展趋势，更无法满足航天器电源高性能、高可靠性、高功率密度市场需求。因此，从电源控制器功率管的可靠性、重量以及安装布局等优化设计的方面考虑，拟发明一种应用于月球探测器电源控制器的功率管与印制电路板及结构件的安装设计。

发明内容

[0004] 本发明的目的是提供一种功率管与印制电路板的安装结构，该结构有效地减小了功率管安装所占用的空间，降低了整个电源控制器结构件的体积和重量，有利于航天器电源高功率密度的优化设计。

[0005] 为了实现以上目的，本发明是通过以下技术方案实现的：

一种功率管与印制电路板的安装结构，其特点是，包含：

电源控制器主结构，其中部位置处开设有安装槽；

印制电路板，其插入在所述的安装槽内；

两排功率管，其分别安装在电源控制器主结构上，且位于印制电路板两侧，所述功率管的引脚焊接与印制电路板上。

[0006] 所述的印制电路板及功率管通过紧固件与电源控制器主结构固定连接。

[0007] 所述紧固件外壁上套设有绝缘套管。

[0008] 所述的印制电路板与安装槽内壁之间设有绝缘导热垫片。

[0009] 所述的绝缘导热垫片采用非金属材料环氧玻璃布层压板。

[0010] 所述的电源控制器主结构采用镁合金材料。

[0011] 本发明与现有技术相比，具有以下优点：

1、该设计不仅能够将功率管可靠地安装到电源控制器结构件上，而且将功率管引脚用

表贴焊盘方式对贴焊接到印制板上，较直插式安装方法，不但增加散热面积，而且增强印制板的机械强度。

[0012] 2、传统功率管安装方式是直插式平行结构件、垂直印制板，在本设计中改变成表贴式变成垂直结构件、平行印制板，考量功率管本身尺寸，表贴式安装设计较直插式结构件厚度立减为原来的一半左右，又由于采用对贴安装，结构件得利用率提高原来的一倍。

[0013] 3、省去了功率管与印制电路板之间的内部电缆，极大地避免了传统功率管安装方式下的空间浪费，可大幅降低电源控制器的重量，对月球探测器整体的轻量化设计具有重要意义。

[0014] 4、目前，应用于月球探测器电源控制器的功率继电器与印制电路板及结构件的一体化设计已应用于月球探测器电源控制器产品上，已完成了抗力学环境、热环境、EMC 及空间环境试验。试验结果证明该设计具有很好的力学和温度适应性，满足月球探测器各项环境要求。

附图说明

[0015] 图 1 为本发明一种功率管与印制电路板的安装结构的主视图；

图 2 为本发明一种功率管与印制电路板的安装结构 A-A 向剖视图；

图 3 为本发明一种功率管与印制电路板的安装结构的俯视图。

具体实施方式

[0016] 以下结合附图，通过详细说明一个较佳的具体实施例，对本发明做进一步阐述。

[0017] 如图 1、图 2 及图 3 所示，一种功率管与印制电路板的安装结构，包含：电源控制器主结构 1，其中部位置处开设有安装槽 11；印制电路板 2，其插入在所述的安装槽 11 内；两排功率管 3，其分别安装在电源控制器主结构 1 上，且位于印制电路板 2 两侧，所述功率管 3 的引脚焊接与印制电路板 2 上，完成功率管 3 和印制电路板 2 的电气连接。

[0018] 印制电路板 2 及功率管 3 通过紧固件 4 与电源控制器主结构 1 固定连接，该紧固件 4 为螺钉。所述紧固件外壁上套设有绝缘套管 41。所述的印制电路板 2 与安装槽 11 内壁之间设有绝缘导热垫片 5。绝缘导热垫片 5 采用非金属材料环氧玻璃布层压板。

[0019] 电源控制器主结构 1 采用镁合金材料。

[0020] 本发明应用时，先将印制电路板 2 插入至电源控制器主结构 1 上，紧固件 4 套上绝缘套管 41，并紧固件 4 装入电源控制器主结构 1 的定位孔，完成印制板电路板 2 与电源控制器主结构 1 之间的预装配；功率管 3 放置于电源控制器主结构 1 上，完成功率管 3 与印制电路板 2 及电源控制器主结构 1 之间的预装配；拧紧紧固件 4，进行固定；最后将功率管 3 的引脚焊接于印制电路板 2，完成功率管 3 和印制电路板 2 的电气连接。

[0021] 综上所述，本发明一种功率管与印制电路板的安装结构，该结构有效地减小了功率管安装所占用的空间，降低了整个电源控制器结构件的体积和重量，有利于航天器电源高功率密度的优化设计。

[0022] 尽管本发明的内容已经通过上述优选实施例作了详细介绍，但应当认识到上述的描述不应被认为是对本发明的限制。在本领域技术人员阅读了上述内容后，对于本发明的多种修改和替代都将是显而易见的。因此，本发明的保护范围应由所附的权利要求来限定。

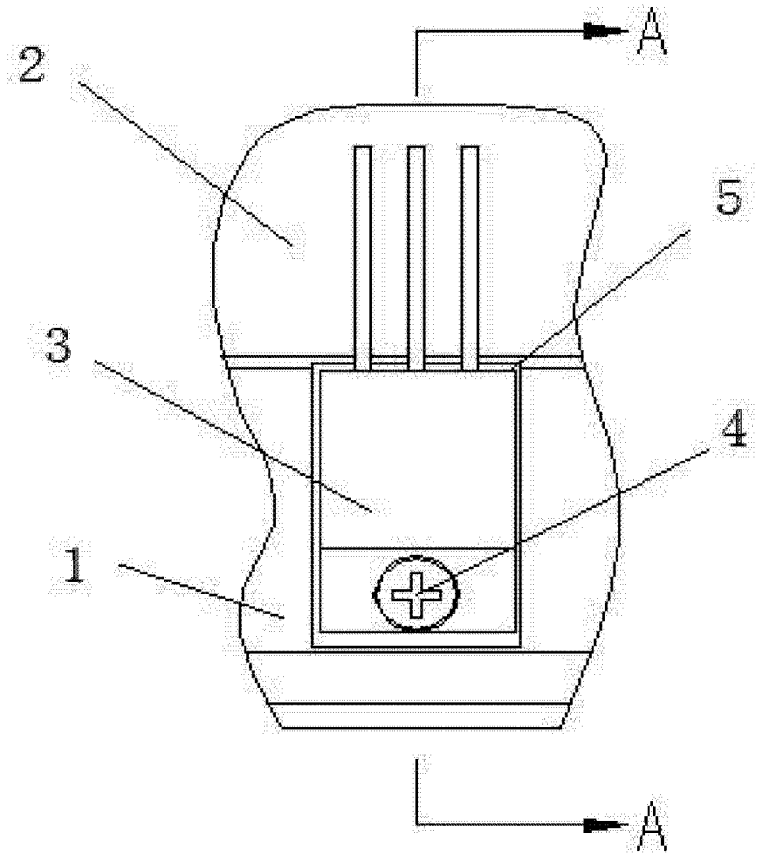


图 1

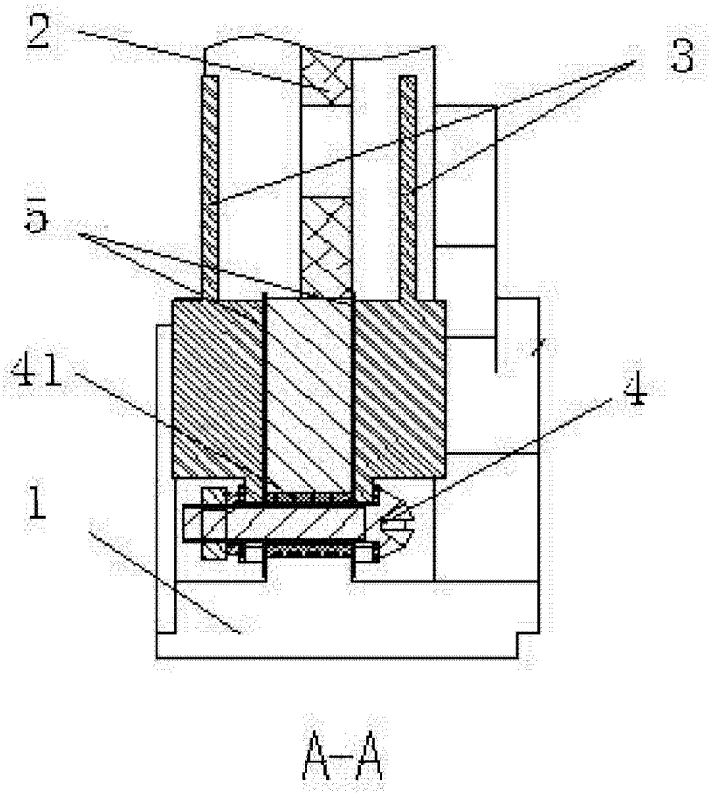


图 2

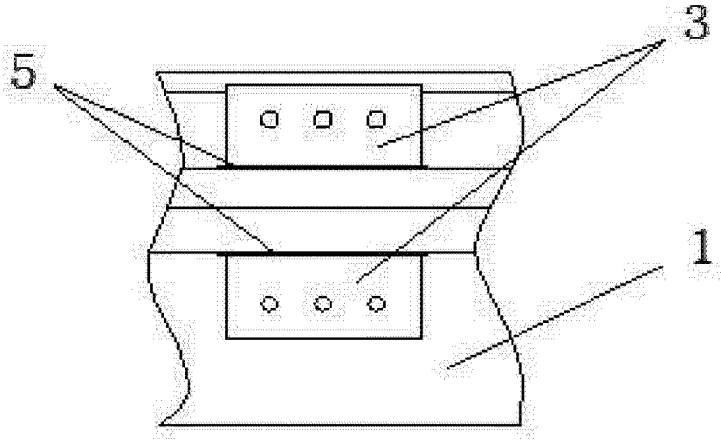


图 3

Espacenet

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SEMICONDUCTOR MODULE AND METHOD OF MANUFACTURING THE SAME

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Classification: - international: ***H01L21/50; H01L21/60; H01L23/367; H01L23/48; H01L25/16***
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Abstract of CN103872036 (A)

There is provided a semiconductor module capable of being easily manufactured. The semiconductor module includes: a control part including at least one control device; and a power part including at least one power device, wherein any one of the control part and the power part includes contact pins having elasticity, and the control part and the power part are electrically connected to each other by the contact pins.

(19)中华人民共和国国家知识产权局

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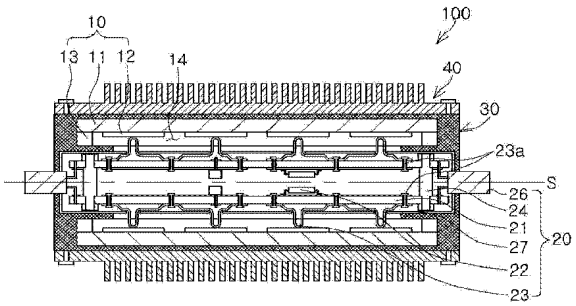
权利要求书2页 说明书8页 附图4页

(54)发明名称

半导体模块及其制造方法

(57)摘要

本发明提供了一种能够被容易地制造的半导体模块和一种制造该半导体模块的方法。所述半导体模块包括：控制部，包括至少一个控制器件；功率部，包括至少一个功率器件，其中，控制部和功率部中的任何一个包括具有弹性的接触引脚，控制部和功率部通过接触引脚彼此电连接。



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1. 一种半导体模块，所述半导体模块包括：

控制部，包括至少一个控制器件；以及

功率部，包括至少一个功率器件，

其中，控制部和功率部中的任何一个包括具有弹性的接触引脚，控制部和功率部通过接触引脚彼此电连接。

2. 如权利要求 1 所述的半导体模块，其中，控制部包括至少一个控制模块基板，控制器件安装在控制模块基板的一个表面上，接触引脚安装在控制模块基板的另一个表面上。

3. 如权利要求 2 所述的半导体模块，其中，控制部还包括壳体，壳体将控制模块基板和控制器件容纳在壳体中，接触引脚在贯穿壳体的同时向外突出。

4. 如权利要求 2 所述的半导体模块，其中，控制部包括两个控制模块基板，所述两个控制模块基板彼此结合，使得控制模块基板的控制器件安装在其上的表面彼此面对。

5. 如权利要求 4 所述的半导体模块，其中，控制部还包括介于两个控制模块基板之间的至少一个分隔件，以维持两个控制模块基板之间的间隔。

6. 如权利要求 2 所述的半导体模块，其中，控制部还包括设置在控制模块基板的一侧上并且电连接到外部的连接部。

7. 如权利要求 2 所述的半导体模块，其中，功率部包括：

至少一个功率模块基板，功率器件安装在所述至少一个功率模块基板的一个表面上；

框架，沿功率模块基板的边缘设置在功率模块的一个表面上以形成功率部的厚度。

8. 如权利要求 7 所述的半导体模块，其中，功率部还包括形成在功率模块基板的一个表面上或者功率器件的外表面上并且接触接触引脚的至少一个接触焊盘。

9. 如权利要求 2 所述的半导体模块，所述半导体模块还包括：

箱体，将控制部和控制部容纳在箱体中；

至少一个热辐射部，紧固到箱体的外表面。

10. 如权利要求 9 所述的半导体模块，其中，箱体包括：

第一容纳部，功率部以滑动方式插入到第一容纳部中的同时结合到第一容纳部；

第二容纳部，将控制部容纳在第二容纳部中。

11. 如权利要求 10 所述的半导体模块，其中，第一容纳部和第二容纳部之间形成有开放部，功率部结合到第一容纳部使得功率器件通过开放部面对控制部。

12. 一种半导体模块，所述半导体模块包括：

控制部，包括在控制部的两侧上突出的多个接触引脚；

两个功率部，分别设置在控制部的两侧上，

其中，功率部在接触接触引脚的同时电连接到控制部。

13. 一种制造半导体模块的方法，所述方法包括：

准备控制部，控制部包括在控制部的两侧上突出的多个接触引脚；

在控制部的两侧上分别设置功率部；以及

在将功率部和控制部彼此紧密地附着的同时将功率部和控制部彼此固定地结合，使得功率部接触接触引脚。

14. 如权利要求 13 所述的方法，其中，准备控制部的步骤包括：准备两个控制模块基板，控制器件安装在所述控制模块基板的一个表面上，接触引脚安装在所述控制模块基板

的另一个表面上；将所述两个控制模块基板彼此结合，使得控制模块基板的安装有接触引脚的表面指向外部。

15. 如权利要求 13 所述的方法，其中，设置功率部的步骤包括以滑动方式分别将功率部插入到上箱体中和下箱体中。

16. 如权利要求 15 所述的方法，其中，功率部和控制部的固定地结合步骤包括使上箱体和下箱体彼此结合并固定，从而控制部被容纳在通过上箱体和下箱体形成的空间中。

17. 如权利要求 16 所述的方法，所述方法还包括将至少一个热辐射部紧固到上箱体和下箱体的外表面。

半导体模块及其制造方法

[0001] 本申请要求于 2012 年 12 月 12 日提交到韩国知识产权局的第 10-2012-0144256 号韩国专利申请的权益，该韩国专利申请的公开通过引用被包含于此。

技术领域

[0002] 本公开涉及一种半导体模块以及一种制造该半导体模块的方法，更具体地说，涉及一种能够被容易地制造的功率半导体模块以及一种制造该功率半导体模块的方法。

背景技术

[0003] 近来，对便携式电子产品的需求快速增长。为了满足该需求，减小安装在这种便携式电子产品中的电子组件的尺寸和重量是必要的。

[0004] 因此，除了减小电子组件自身尺寸的方法之外，在设计半导体模块时，在有限空间中尽可能多地安装器件和导线的方法也很重要。

[0005] 同时，在驱动功率半导体器件时，会产生大量的热。由于这种热对电子产品的寿命和操作有影响，因此辐射半导体模块的热是重要的。

[0006] 为此，根据相关技术中的功率半导体模块具有功率器件和控制器件两者安装在电路板的一个表面上而热辐射板安装在电路板的另一表面上的结构。

[0007] 然而，如上所述的根据相关技术的功率半导体模块会具有下述问题。

[0008] 首先，由于功率半导体模块的小型化，安装在相同空间中的半导体器件的数量增加，从而在功率半导体模块中可以产生大量的热。然而，热辐射板仅设置在功率半导体模块的下表面上，使得热不能被有效地辐射。

[0009] 另外，根据相关技术的功率半导体模块的缺点在于：由于器件设置在电路板的单个表面上，因此功率半导体模块的尺寸会增加。

[0010] 此外，设置在根据相关技术的功率半导体模块中的器件或者器件和外部连接端子通常通过引线键合方式彼此连接。因此，由于引线键合导致制造工艺所需的时间增加。另外，由于在制造功率半导体模块过程中施加到键合引线的物理压力导致键合引线会变形和被损坏，并且由于在驱动半导体模块时产生的热导致在键合引线和器件彼此结合的位置处会产生分层，从而在长时间使用功率半导体模块时可靠性会降低。

[0011] 因此，需要一种具有优异的热辐射特性、能够容易地被制造并且使可靠性得到保证的功率半导体模块。

[0012] [相关技术文件]

[0013] （专利文件 1）第 2007-0065207 号韩国专利特开公布

发明内容

[0014] 本公开的一方面可以提供一种具有优异的热辐射特性的功率半导体模块和一种制造该功率半导体模块的方法。

[0015] 本公开的另一方面可以提供一种不使用键合引线的功率半导体模块和一种制造

该功率半导体模块的方法。

[0016] 本公开的另一方面可以提供一种能够容易地被制造的功率半导体模块和一种制造该功率半导体模块的方法。

[0017] 根据本公开的一方面，一种半导体模块可以包括：控制部，包括至少一个控制器件；功率部，包括至少一个功率器件，其中，控制部和功率部中的任何一个包括具有弹性的接触引脚，控制部和功率部通过接触引脚彼此电连接。

[0018] 控制部可以包括至少一个控制模块基板，控制器件安装在控制模块基板的一个表面上，接触引脚可以安装在控制模块基板的另一个表面上。

[0019] 控制部还可以包括壳体，壳体将控制模块基板和控制器件容纳在壳体中，接触引脚可以在贯穿壳体的同时向外突出。

[0020] 控制部可以包括两个控制模块基板，其中，所述两个控制模块基板彼此结合，使得控制模块基板的控制器件安装在其上的表面彼此面对。

[0021] 控制部还可以包括介于两个控制模块基板之间的至少一个分隔件，以维持两个控制模块基板之间的间隔。

[0022] 控制部还可以包括设置在控制模块基板的一侧上并且电连接到外部的连接部。

[0023] 功率部可以包括：至少一个功率模块基板，功率器件安装在所述至少一个功率模块基板的一个表面上；框架，沿功率模块基板的边缘设置在功率模块的一个表面上以形成功率部的厚度。

[0024] 功率部还可以包括形成在功率模块基板的一个表面上或者功率器件的外表面上并且接触接触引脚的至少一个接触焊盘。

[0025] 所述半导体模块还可以包括：箱体，将控制部和控制部容纳在箱体中；至少一个热辐射部，紧固到箱体的外表面。

[0026] 箱体可以包括：第一容纳部，功率部以滑动方式插入到第一容纳部中的同时结合到第一容纳部；第二容纳部，将控制部容纳在第二容纳部中。

[0027] 第一容纳部和第二容纳部之间可以形成有开放部，功率部可以结合到第一容纳部使得功率器件通过开放部面对控制部。

[0028] 根据本公开的另一方面，一种半导体模块可以包括：控制部，包括在控制部的两侧上突出的多个接触引脚；两个功率部，分别设置在控制部的两侧上，其中，功率部在接触接触引脚的同时电连接到控制部。

[0029] 根据本公开的另一方面，一种制造半导体模块的方法可以包括：准备控制部，控制部包括在控制部的两侧上突出的多个接触引脚；在控制部的两侧上分别设置功率部；在将功率部和控制部彼此紧密地附着的同时将功率部和控制部彼此固定地结合，使得功率部接触接触引脚。

[0030] 准备控制部的步骤可以包括：准备两个控制模块基板，控制器件安装在所述控制模块基板的一个表面上，接触引脚安装在所述控制模块基板的另一个表面上；将所述两个控制模块基板彼此结合，使得控制模块基板的安装有接触引脚的表面指向外部。

[0031] 设置功率部的步骤可以包括以滑动方式分别将功率部插入到上箱体中和下箱体中。

[0032] 功率部和控制部的固定地结合步骤可以包括使上箱体和下箱体彼此结合并固定，

从而控制部被容纳在通过上箱体和下箱体形成的空间中。

[0033] 所述方法还可以包括将至少一个热辐射部紧固到上箱体和下箱体的外表面。

附图说明

[0034] 通过下面结合附图进行的详细描述，本公开的上述和其他方面、特点及其他优点将会被更加清楚地理解，在附图中：

[0035] 图 1 是示意性地示出了根据本公开示例性实施例的半导体模块的透视图；

[0036] 图 2 是沿图 1 中的 A-A’线截取的半导体模块的剖视图；

[0037] 图 3 是图 2 中示出的半导体模块的分解透视图；

[0038] 图 4 是沿图 3 中的 B-B’线截取的功率部的平面图；

[0039] 图 5 和图 6 是沿图 3 中的 C-C’线截取的控制部的平面图；

[0040] 图 7 是沿图 3 中的 D-D’线截取的控制部的平面图。

具体实施方式

[0041] 现在，将参照附图详细描述本公开的示例性实施例。

[0042] 图 1 是示意性地示出了根据本公开示例性实施例的半导体模块的透视图；图 2 是沿图 1 中的 A-A’线截取的半导体模块的剖视图；图 3 是图 2 中示出的半导体模块的分解透视图。

[0043] 另外，图 4 是沿图 3 中的 B-B’线截取的功率部的平面图；图 5 和图 6 是沿图 3 中的 C-C’线截取的控制部的平面图；图 7 是沿图 3 中的 D-D’线截取的控制部的平面图。这里，图 6 和图 7 示出了在没有壳体的情况下的控制部。

[0044] 参照图 1 到图 7，根据本公开示例性实施例的半导体模块 100 可以包括功率部 10、控制部 20、箱体 30 和热辐射部 40。

[0045] 同时，根据本公开示例性实施例的半导体模块 100 可以具有基于中心水平线（图 2 中的 S）竖直对称的结构。因此，在下面的描述中，相同的组件可以设置在基于中心水平线彼此对称的位置中。因此，将省略重复组件的描述。

[0046] 功率部 10 可以包括功率模块基板 11、至少一个功率器件 12 和框架 13。

[0047] 功率模块基板 11 可以是印刷电路板（PCB）、陶瓷基板、预成型基板、直接敷铜（DBC）基板或者绝缘金属基板（IMS）。

[0048] 另外，虽然未示出，但是具有各种形式的布线图案、安装电极等可以形成在功率模块基板 11 的一个表面上。

[0049] 功率模块基板 11 可以具有安装在其一个表面上的至少一个功率器件 12。功率器件 12 可以是用于控制功率的功率转换器件或功率电路器件，诸如伺服驱动器、逆变器、功率调节器、转换器等。

[0050] 例如，功率器件 12 可以包括功率金属氧化物半导体场效应晶体管（MOSFET）、双极结型晶体管（BJT）、绝缘栅双极型晶体管（IGBT）、二极管或它们的组合。即，在本公开示例性实施例中，功率器件 12 可以包括上述器件中的全部或部分。

[0051] 具体地说，根据本公开示例性实施例的功率器件 12 可以被构造成几对。每个功率器件 12 包括绝缘栅双极型晶体管（IGBT）和二极管。然而，这仅仅是示例，并且本公开不必

须限制于此。

[0052] 功率器件 12 可以通过粘合构件(未示出)附着到功率模块基板 11 的一个表面,将在下面描述。这里,粘合构件可以是导电的或不导电的。例如,粘合构件可以是导电焊料、导电膏或胶带。另外,可以使用焊料、金属环氧树脂、金属膏、环氧基树脂、具有优异耐热性的粘性胶带等作为粘合构件。

[0053] 同时,至少一个接触焊盘 11a 可以形成在功率模块基板 11 的一个表面上或者功率器件 12 的外表面上,从而被电连接到控制部 20,将在下面描述。因此,接触焊盘 11a 可以设置在与控制部 20 的接触引脚 23 的末端相对应的位置中。

[0054] 在本公开的示例性实施例中,以示例的方式描述了所有的接触焊盘 11a 设置在功率器件 12 的外表面上的情况。然而,本公开不限于此。即,如果需要,接触焊盘 11a 可以选择性地设置在功率模块基板 11 上或者功率器件 12 上。

[0055] 框架 13 可以结合到功率模块基板 11 的一个表面,被形成为具有边缘形状,并且沿着功率模块基板 11 的边缘设置。框架 13 可以被设置为用来保证功率部 10 的厚度。即,框架 13 可以被设置为用来保证当功率部 10 结合到箱体 30 时将要安装功率部 10 的功率器件 12 的空间 14。

[0056] 框架 13 可以由各种材料(诸如金属材料、树脂材料等)形成,只要框架 13 的形状不容易改变即可。

[0057] 控制部 20 可以包括控制模块基板 21、控制器件 22、接触引脚 23 和壳体 27。

[0058] 与功率模块基板 11 相似,其上安装有控制器件 22 和接触引脚 23 的控制模块基板 21 可以是印刷电路板(PCB)、陶瓷基板、预成型基板、直接敷铜(DBC)基板或者绝缘金属基板(IMS)。

[0059] 控制器件 22 可以安装在控制模块基板 21 的一个表面上,即,控制模块基板 21 的内表面上。控制器件 22 可以电连接到接触引脚 23 (将在下面描述)并且可以通过接触引脚 23 电连接到功率器件 12。因此,控制器件 22 可以控制功率器件 12 的操作。

[0060] 例如,控制器件 22 可以是微处理器。另外,控制器件 22 可以是诸如电阻器、逆变器或电容器的无源器件或者诸如晶体管的有源器件。

[0061] 同时,可以针对一个功率器件 12 设置一个控制器件 22 或者多个控制器件 22。即,控制器件 22 的种类和数量可以根据功率器件 12 的种类和数量适当地选取。

[0062] 另外,与上述功率器件 12 类似地,控制器件 22 可以通过诸如导电焊料的粘合构件(未示出)安装在控制模块基板 21 上。

[0063] 接触引脚 23 可以安装在控制模块基板 21 的另一表面上,即控制模块基板 21 的外表面上。接触引脚 23 可以以下述形式被设置 :接触引脚 23 从控制模块基板 21 向外突出并且接触引脚 23 具有接触功率模块基板 11 的接触焊盘 11a 的末端。

[0064] 具体地说,根据本公开示例性实施例的接触引脚 23 可以形成为具有片簧的形状,并且沿接触引脚 23 突出的方向具有弹性。因此,在接触引脚 23 接触接触焊盘 11a 的情况下,接触引脚 23 可以弹性地接触接触焊盘 11a。

[0065] 接触引脚 23 可以通过分开的固定引脚 23a 固定地紧固到控制模块基板 21。固定引脚 23a 可以被设置为即使在接触引脚 23 被按压的情况下仍维持接触引脚 23 和控制模块基板 21 之间的结合力。因此,当确保接触引脚 23 和控制模块基板 21 之间的结合力时,可

以省略固定引脚 23a。

[0066] 另外，在根据本公开示例性实施例的控制部 20 中，两个控制模块基板 21 可以以两个控制模块基板 21 彼此面对的形式而彼此结合。这里，控制模块基板 21 可以彼此结合，使得控制模块基板 21 的其上安装有控制器件 22 的表面彼此面对。因此，当控制模块基板 21 彼此结合时，控制模块基板 21 的两个外表面可以具有接触引脚 23 在其上突出的形状。

[0067] 这里，两个控制模块基板 21 可以具有介于其间的分隔件 24。分隔件 24 可以用来使两个控制模块基板 21 彼此分隔开预定的间隔。因此，即使在控制模块基板 21 彼此结合的情况下，仍可以防止设置在彼此面对的表面上的控制器件 22 之间的接触。

[0068] 为了将半导体模块 100 电连接到外部，可以设置连接部 26。为此，连接部 26 可以紧固到至少一个控制模块基板 21，从而被电连接到控制模块基板 21。

[0069] 在本公开的示例性实施例中，以示例的方式描述了在控制部 20 的两端中的每端处形成一个连接部 26 的情况，即，总共形成两个连接部 26 的情况。这里，两个控制模块基板 21 都可以被构造为电连接到一个连接部 26。因此，在这种情况下，即使仅使用两个连接部 26 中的任意一个连接部 26，它仍可以电连接到两个控制模块基板 21。

[0070] 然而，本公开不必须限制于上述构造，而是可以各种地实施。例如，一个控制模块基板 21 还可以被构造为仅电连接到连接部 26 中的任何一个。

[0071] 另外，仅设置一个连接部 26 而不是设置两个连接部 26 并且两个控制模块基板 21 通过一个连接部 26 彼此电连接的构造也是可以的。

[0072] 壳体 27 可以形成控制部 20 的外壳，并保护控制部 20 不受外部影响。因此，上述两个控制模块基板 21 可以结合到并被容纳在形成壳体 27 的内部空间中。

[0073] 另外，壳体 27 可以具有形成在其中的至少一个贯穿孔 28。贯穿孔 28 可以被用作上述接触引脚 23 通过其向外突出的通道。因此，贯穿孔 28 可以形成为尺寸比接触引脚 23 的尺寸大的开口。

[0074] 参照附图，在本公开的示例性实施例中描述了三个接触引脚 23 设置为穿过一个贯穿孔 28 的情况。然而，本公开不限于上述构造，而是可以各种地实施。即，可以在一个贯穿孔 28 中仅设置一个接触引脚 23，或者一个贯穿孔 28 可以被形成为较大的尺寸使得三个或更多个接触引脚 23 可以被设置为贯穿一个贯穿孔 28。

[0075] 箱体 30 可以形成整个半导体模块 100 的外壳并保护功率部 10 和控制部 20 不受外部环境的影响。为此，箱体 30 可以包括上箱体 30a 和下箱体 30b。

[0076] 上箱体 30a 和下箱体 30b 可以具有相同的形状并且是彼此对称的，上箱体 30a 和下箱体 30b 可以以上箱体 30a 和下箱体 30b 彼此面对的方式彼此结合。另外，随着上箱体 30a 和下箱体 30b 彼此结合，可以在箱体 30 内形成容纳空间，功率部 10 和控制部 20 可以被容纳在该容纳空间内。

[0077] 箱体 30 可以在将功率部 10 和控制部 20 容纳在其中的同时将功率部 10 和控制部 20 彼此固定地结合。为此，箱体 30 可以包括容纳功率部 10 的第一容纳部 31 和容纳控制部 20 的第二容纳部 32。

[0078] 第一容纳部 31 可以使功率部 10 固定地结合到第一容纳部 31。根据本公开示例性实施例的功率部 10 可以以滑动方式插入到第一容纳部 31 中的同时结合到箱体 30。因此，第一容纳部 31 可以形成为具有与功率部 10 的外壳相对应的尺寸的空间，使得功率部 10 可

以滑动地结合到第一容纳部 31。

[0079] 另外，第一容纳部 31 可以包括分别形成在上箱体 30a 和下箱体 30b 中并且具有局部开放的一个表面的开放部 33。开放部 33 可以用作功率器件 12 和控制部 20 的接触引脚 23 彼此电连接的通道。因此，功率部 10 可以结合到第一容纳部 31，从而功率器件 12 朝向开放部 33，控制部 20 的接触引脚 23 可以通过开放部 33 电连接到功率模块基板 11。

[0080] 第二容纳部 32 可以被限定为在上箱体 30a 和下箱体 30b 彼此结合的状态下在中心形成的容纳空间。第二容纳部 32 可以将控制部 20 容纳在第二容纳部 32 中。因此，第二容纳部 32 可以形成为与控制部 20 的形状或尺寸相对应的形状。

[0081] 在如上所述的箱体 30 中，上箱体 30a 和下箱体 30b 可以通过诸如螺钉等单独的固定构件 35 彼此结合。然而，本公开不限于上述构造。即，如果需要，可以使用诸如组装结合方式、使用粘合构件的方式等各种方式。

[0082] 另外，箱体 30 可以由绝缘材料形成。具体地说，可以使用诸如具有高导热率的硅凝胶、导热环氧树脂、聚酰亚胺等材料作为箱体 30 的材料。然而，本公开不限于此。

[0083] 在如上所述的箱体 30 中，上箱体 30a 和下箱体 30b 可以通过单独的固定构件 35 彼此结合。然而，本公开不限于上述构造。即，上箱体 30a 和下箱体 30b 还可以通过介于上箱体 30a 和下箱体 30b 之间的粘合构件彼此附着以及彼此一体地形成。这里，可以使用粘合剂、胶带等作为粘合构件。

[0084] 热辐射部 40 可以紧固到箱体 30 的至少一个外表面，以使从功率部 10 产生的热辐射到外部。

[0085] 为了有效地将热辐射到外部，热辐射部 40 可以由金属材料形成。例如，可以使用能够以相对低的成本容易地使用并具有优异导热率的铝(Al)或铝合金作为热辐射部 40 的材料。然而，本公开不限于此。即，可以使用具有优异导热率的各种材料(诸如石墨等)来作为热辐射部 40 的材料，即使它们不是金属。

[0086] 另外，热辐射部 40 可以包括形成在其外表面上的多个突起 42 或者狭缝，以增加外部面积。

[0087] 热辐射部 40 可以通过单独的固定构件 45 固定地紧固到箱体 30。然而，本公开不限于上述构造。即，热辐射部 40 还可以通过介于热辐射部 40 和箱体 30 之间的粘合构件而附着到箱体 30。在这种情况下，可以使用各种材料作为粘合构件的材料，只要它们可以具有高的导热率并且能够将热辐射部 40 和箱体 30 彼此结合并固定地安装即可。

[0088] 接下来，将描述根据本公开示例性实施例的制造半导体模块的方法。

[0089] 参照图 3，在根据本公开示例性实施例的制造半导体模块的方法中，首先准备控制部 20。这里，如上所述，可以通过将两个控制模块基板 21 彼此结合而形成控制部 20。即，可以通过下述步骤来形成控制部 20：通过使两个控制模块基板 21 通过分隔件 24 彼此结合使得其上安装有控制器件 22 的两个控制模块基板 21 的表面彼此面对，并且利用壳体 27 来覆盖两个控制模块基板 21 的外部，以将两个控制模块基板 21 彼此固定。

[0090] 同时，可以与上述过程分开地执行将功率部 10 结合到箱体 30 的过程。功率部 10 可以在以滑动方式插入到箱体 30 的第一容纳部 31 中的同时结合到箱体 30。这里，功率部 10 可以结合到箱体 30，使得功率部 10 的其上安装有功率器件 12 的表面暴露到壳体 27 的开放表面。

[0091] 由于将功率部 10 结合到箱体 30 的过程可以与上述准备功率部 20 的过程分开执行，因此可以在准备控制部 20 的过程之前或之后执行将功率部 10 结合到箱体 30 的过程。选择性地，可以与准备控制部 20 的过程同时地执行将功率部 10 结合到箱体 30 的过程。在与准备控制部 20 的过程同时地执行将功率部 10 结合到箱体 30 的过程的情况下，可以减少制造时间。

[0092] 接下来，结合有功率部 10 的箱体 30 和控制部 20 可以彼此结合。控制部 20 可以在被容纳在由箱体 30 形成的第二容纳部 32 中的同时结合到箱体 30。在这个过程中，控制部 20 的接触引脚 23 可以通过箱体 30 的开放部 33 接触功率部 10 的接触焊盘 11a。因此，控制部 20 和功率部 10 可以彼此电连接。

[0093] 同时，在这个过程中，接触引脚 23 可以在被功率部 10 朝着控制模块基板 21 按压的同时接触功率部 10。因此，由于接触引脚 23 弹性地接触功率部 10 的接触焊盘 11a，因此可以保证电接触和物理接触的可靠性。

[0094] 随后，热辐射部 40 可以结合到箱体 30 的外部。因此，可以完成根据本公开示例性实施例的半导体模块 100。

[0095] 如上所述，在根据本公开示例性实施例的半导体模块中，可以以控制部和功率部彼此对称的形式成对地设置控制部和功率部。另外，用于与外部连接的连接部可以设置在半导体模块的侧部。此外，控制部和功率部可以在通过具有弹性的接触引脚而不是键合引线彼此弹性接触的同时彼此电连接。

[0096] 因此，由于可以省略根据相关技术中已经用来在器件之间电连接或器件和外部端子之间连接的键合引线，因此可以有效地设置多个功率器件和控制器件。因此，与相关技术相比，半导体模块可以具有减小的尺寸，从而半导体模块可以容易地在需要小型化和高度集成的各种电子设备中使用。

[0097] 另外，由于与使用键合引线的相关技术相比可以保证结合可靠性并且可以解决键合引线在制造半导体模块的过程中变形的问题，因此可以显著减少在制造半导体模块的过程中产生的缺陷。

[0098] 另外，在根据本公开示例性实施例的半导体模块中，可以使用热辐射部分别设置在箱体的两个表面上的双侧散热结构，并且安装功率器件的功率部与热辐射部可以设置为彼此显著地相邻。因此，可以显著减小热的传导路径，并且热可以通过半导体模块的两表面辐射。因此，由于可以获得与相关技术的热辐射特性相比显著提高的热辐射特性，因此可以保证半导体模块的长期可靠性。

[0099] 此外，在根据本公开示例性实施例的制造半导体模块的方法中，由于使用具有弹性的接触引脚，因此接触部和功率部可以仅通过将控制部和功率部彼此机械地结合的过程而彼此电连接。因此，由于省略了根据相关技术中已经使用的键合引线等的过程，因此制造半导体模块的过程会非常容易，并且制造半导体模块所需的时间会显著减少。

[0100] 上面描述的根据本公开示例性实施例的半导体模块不限于上述示例性实施例，而是可以各种实施。例如，虽然已经以示例的方式描述了半导体模块大体上具有矩形平行六面体的形状的情况，但是本公开不限于此。即，如果需要，半导体模块可以具有诸如圆柱体的形状、多棱柱(poly prismatic)的形状等的各种形状。

[0101] 另外，虽然在上述示例性实施例中已经通过示例的方式描述了功率半导体模块，

但是本公开不限于此，而是可以不同地实施为封装有至少一个功率器件的电子组件。

[0102] 尽管已经在上面描述并且示出了示例性实施例，但是本领域的技术人员将清楚的是，在不脱离由权利要求限定的本公开的精神和范围的情况下，可进行修改和变型。

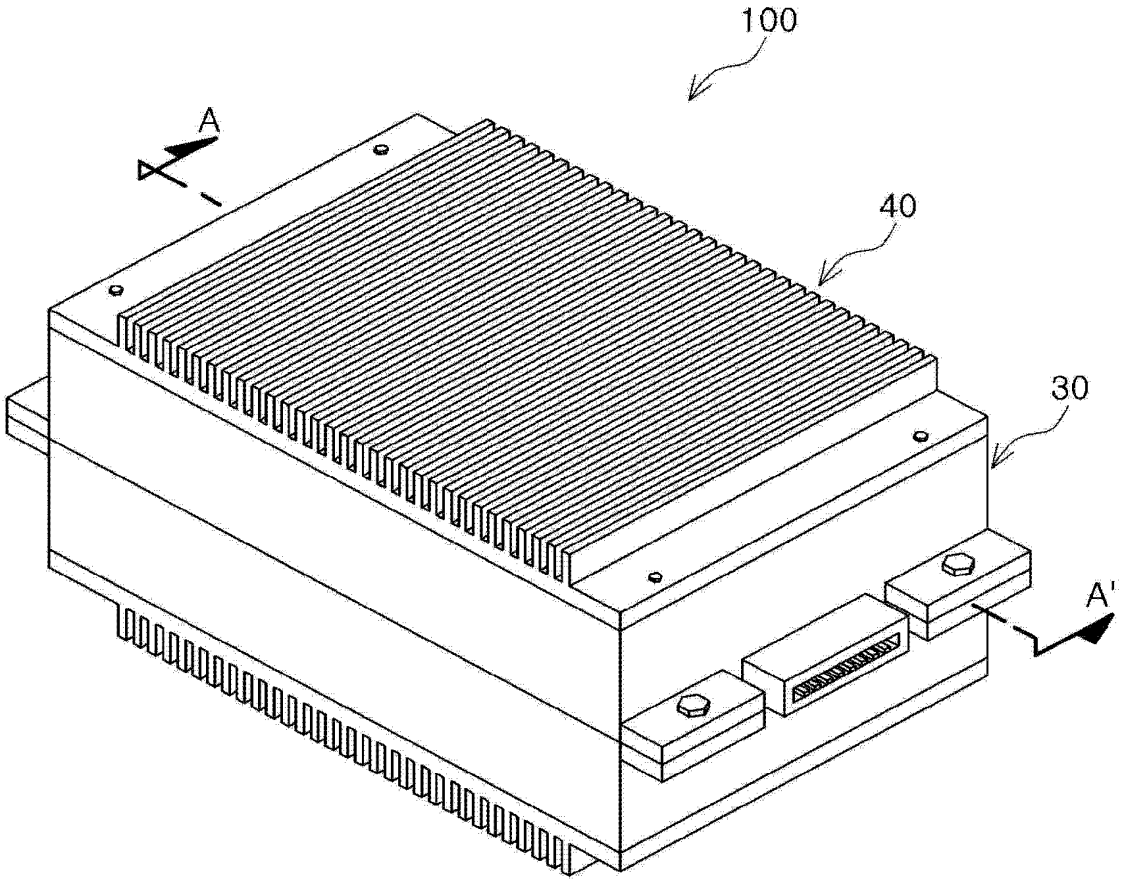


图 1

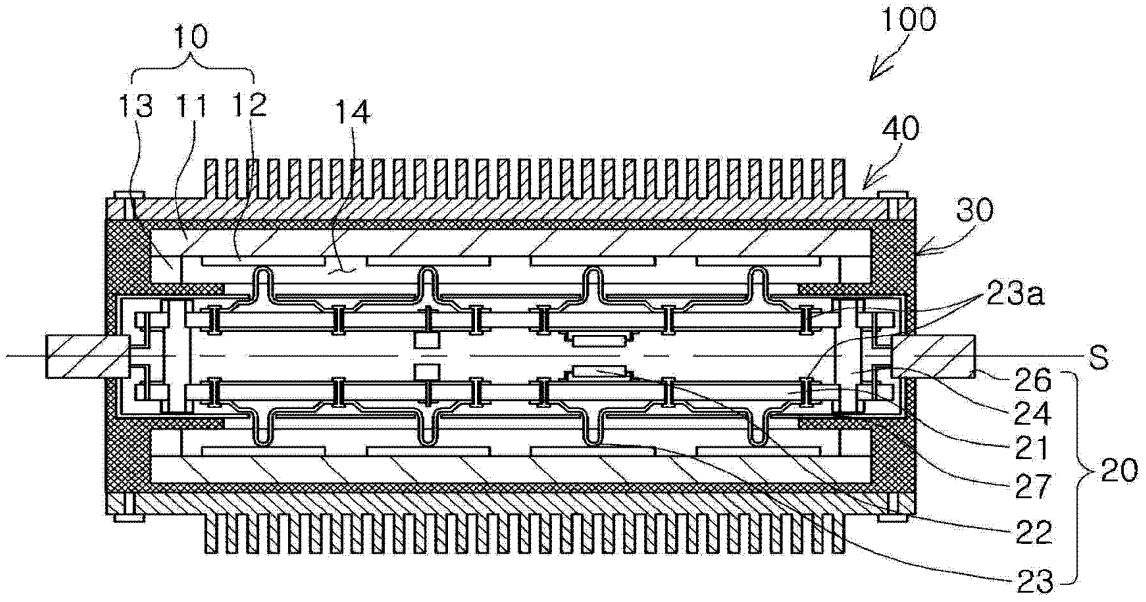


图 2

12

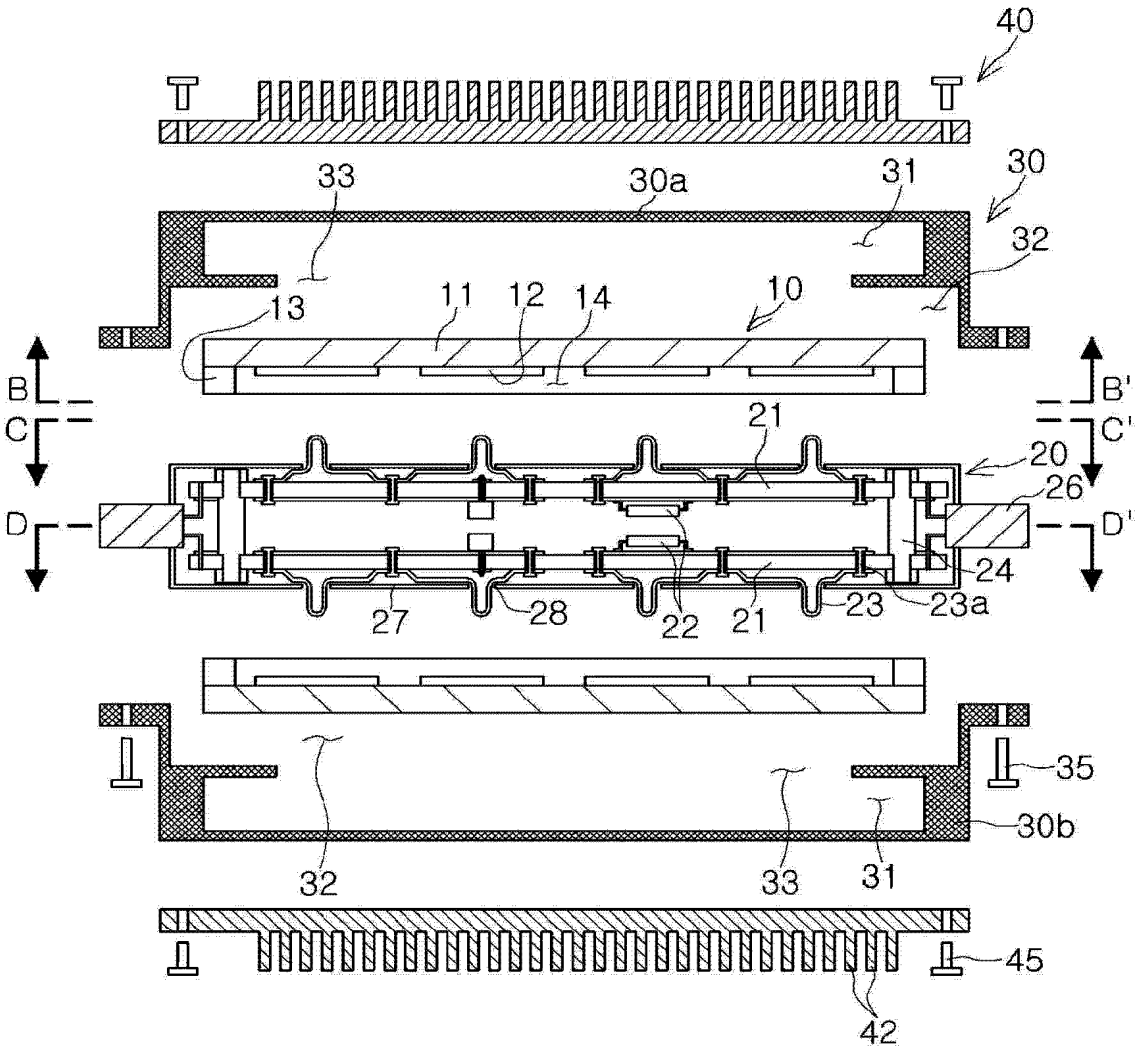

40
33
30a
31
30
32
13
11
12
14
10
B
C
B'
C'
21
20
26
D
D'
24
27
28
22
21
23
23a
35
30b
32
33
31
45
42

图 3

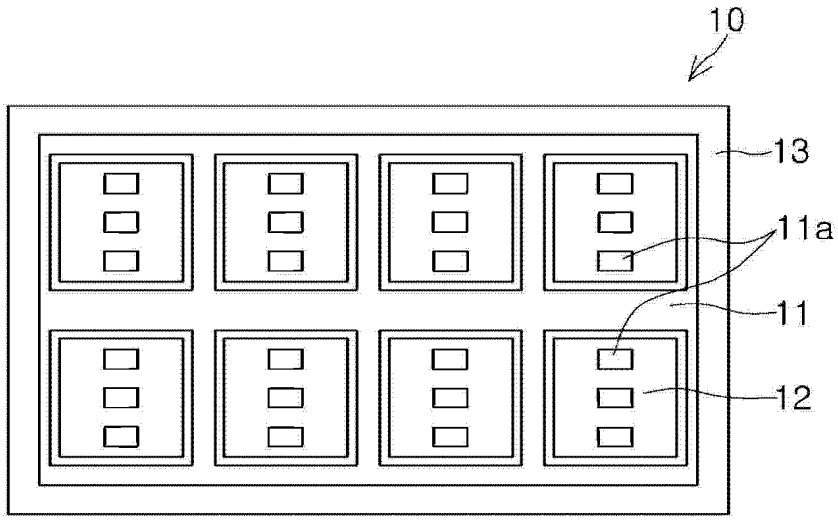


图 4

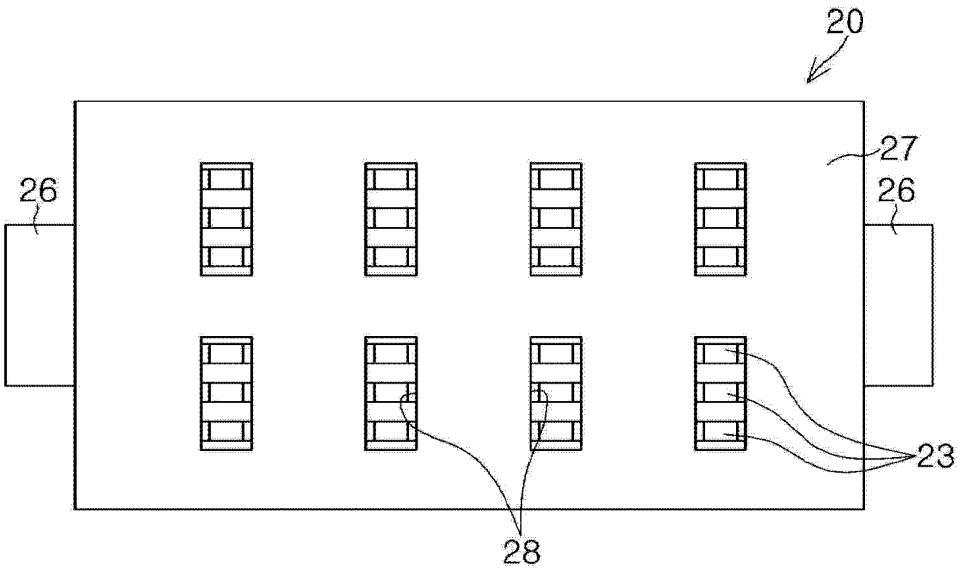


图 5

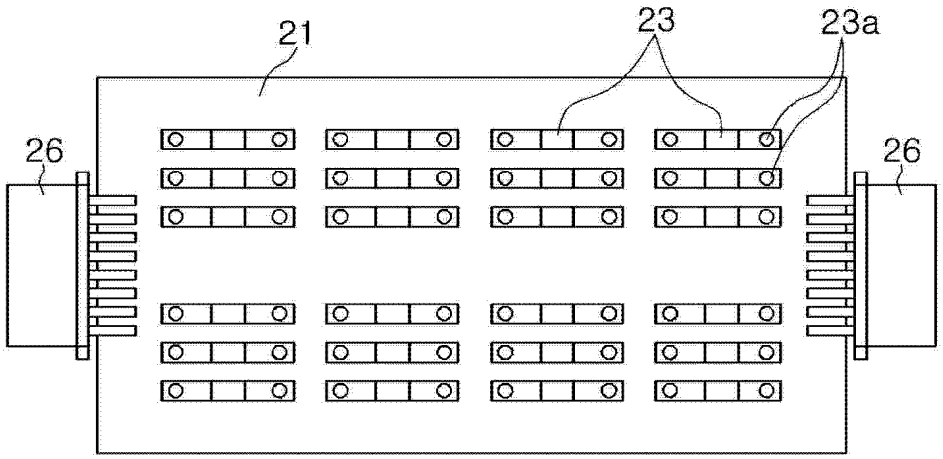


图 6

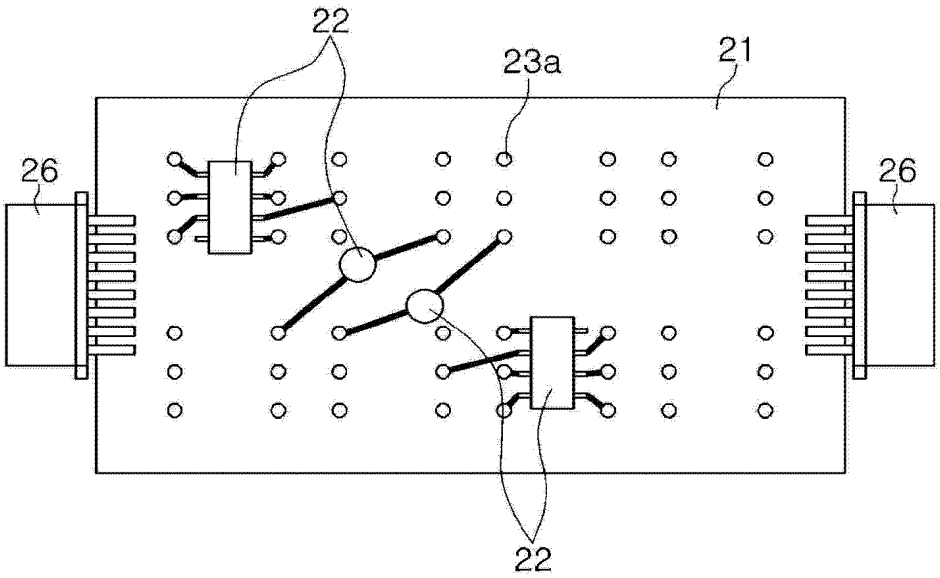


图 7

Espacenet

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Integrated circuit module applied to switch type regulator

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Abstract of CN103824853 (A)

The invention discloses an integrated circuit module applied to a switch type regulator. The integrated circuit module applied to the switch type regulator comprises a lead frame, a first power device chip, control chips and an intermediate electric conduction component. The lead frame is provided with multiple pins and a substrate. A first electrode and a control electrode are arranged on the front face of the first power device chip, and a second electrode is arranged on the back face of the first power device chip. The control chips are stacked above the first power device chip and are provided with internal control driving circuits and multiple welding pads electrically connected with the internal control driving circuits. The intermediate electric conduction component is provided with a surface for mutual connection of welding flux. The control electrode of the first power device chip is electrically connected to the intermediate electric conduction component through an electric conductive lug, and the intermediate electric conduction component is connected to one of the corresponding welding pads of the control chips through a bonding wire. The integrated circuit module applied to the switch type regulator promotes the electrical connection of the control chips and the first power device chip below the control chips, and the reliability of the integrated circuit module is improved.

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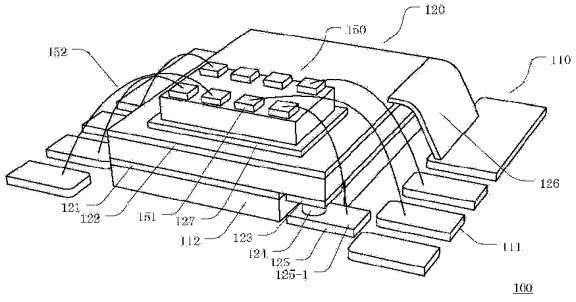
权利要求书2页 说明书7页 附图3页

(54)发明名称

应用于开关型调节器的集成电路组件

(57)摘要

公开了一种应用于开关型调节器的集成电路组件，包括：引线框，其具有多个引脚和基底；第一功率器件芯片，其正面具有第一电极和控制电极，其背面具有第二电极；控制芯片，控制芯片堆叠在第一功率器件芯片上方，并且具有内部控制驱动电路以及与内部控制驱动电路电连接的多个焊垫；以及中间导电部件，其具有用于焊料互连的表面，其中，第一功率器件芯片的控制电极通过导电凸块电连接到中间导电部件，中间导电部件通过键合线连接到控制芯片的多个焊垫中的相应一个焊垫。该集成电路组件有利于控制芯片与其下方的第一功率器件芯片的电连接，并且提高了集成电路组件的可靠性。



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IPR2024-00715 EX. 2005

1. 一种应用于开关型调节器的集成电路组件，包括：

引线框，其具有多个引脚和基底；

第一功率器件芯片，其正面具有第一电极和控制电极，其背面具有第二电极；

控制芯片，所述控制芯片堆叠在所述第一功率器件芯片上方，并且具有内部控制驱动电路以及与内部控制驱动电路电连接的多个焊垫；以及

中间导电部件，其具有用于焊料互连的表面，

其中，所述第一功率器件芯片的第一电极附着在所述基底上且与所述基底形成电连接，所述第一功率器件芯片的第二电极电连接至所述引线框的所述多个引脚中的至少一个引脚，所述第一功率器件芯片的控制电极通过导电凸块电连接到所述中间导电部件，所述中间导电部件通过键合线连接到所述控制芯片的所述多个焊垫中的相应一个焊垫。

2. 根据权利要求 1 所述的集成电路组件，还包括：

第一金属带，将第一功率器件芯片的第二电极电连接至所述引线框的所述多个引脚中的至少一个引脚。

3. 根据权利要求 1 所述的集成电路组件，还包括：

第二功率器件芯片，其正面具有第一电极和控制电极，其背面具有第二电极，

其中，所述第二功率器件芯片堆叠在所述第一功率器件芯片上方，

所述第二功率器件芯片的第一电极电连接至所述引线框的所述多个引脚中的至少一个引脚，所述第二功率器件芯片的第二电极电连接至所述第一功率器件芯片的第一电极，所述第二功率器件芯片的控制电极通过键合线连接到所述控制芯片的所述多个焊垫中的相应一个焊垫。

4. 根据权利要求 3 所述的集成电路组件，还包括：

导电层，其设置在第一功率器件芯片的第二电极上；以及

第一金属带，将导电层电连接至所述引线框的所述多个引脚中的至少一个引脚。

5. 根据权利要求 4 所述的集成电路组件，还包括：

绝缘层，其设置在控制芯片和导电层之间。

6. 根据权利要求 4 所述的集成电路组件，还包括：

第二金属带，将第二功率器件芯片的第一电极电连接至所述引线框的所述多个引脚中的至少一个引脚。

7. 根据权利要求 3 所述的集成电路组件，还包括：

第一绝缘层，其设置在第一功率器件芯片的第二电极上；

导电层，其设置在所述第一绝缘层和第二功率器件芯片的第二电极之间；以及

第一金属带，将导电层电连接至所述引线框的所述多个引脚中的至少一个引脚。

8. 根据权利要求 7 所述的集成电路组件，还包括：

第二金属带，将第二功率器件芯片的第一电极电连接至所述引线框的所述多个引脚中的至少一个引脚。

9. 根据权利要求 8 所述的集成电路组件，其中第一金属带和第二金属带通过公共的引脚电连接。

10. 根据权利要求 8 所述的集成电路组件，还包括：

第三金属带，将第二功率器件芯片的第二电极电连接至所述引线框的所述多个引脚中

的至少一个引脚。

11. 根据权利要求 7 所述的集成电路组件，还包括：

第二绝缘层，其设置在控制芯片和导电层之间。

12. 根据前述权利要求 1-11 中任一项所述的集成电路组件，其中所述第一电极是场效应晶体管的源极和漏极中的一个，所述第二电极是场效应晶体管的源极和漏极中的另一个，所述控制电极是场效应晶体管的栅极。

13. 根据前述权利要求 1-11 中任一项所述的集成电路组件，其中所述第一电极是双极性晶体管的发射极和集电极中的一个，所述第二电极是双极性晶体管的发射极和集电极中的另一个，所述控制电极是双极性晶体管的基极。

14. 根据前述权利要求 1 所述的集成电路组件，还包括封装料，所述封装料覆盖控制芯片和第一功率器件芯片，并且覆盖引线框的至少一部分，使得引线框的引脚的端部或底部暴露用于外部电连接。

15. 根据前述权利要求 3 所述的集成电路组件，还包括封装料，所述封装料覆盖控制芯片、第一功率器件芯片和第二功率器件芯片，并且覆盖引线框的至少一部分，使得引线框的引脚的端部或底部暴露用于外部电连接。

应用于开关型调节器的集成电路组件

技术领域

[0001] 本发明涉及半导体封装组件，更具体地涉及应用于开关型调节器的集成电路组件。

背景技术

[0002] 开关型调节器，例如直流－直流变换器，用来给各种各样的电系统提供稳定的电压源。低电源设备中(如手提电脑、手机等)电池管理尤其需要高效率的直流－直流变换器。开关型调节器把输入直流电压转换成高频率电压，然后将高频输出电压进行滤波进而转换成直流输出电压。

[0003] 随着电子元件的小型化、轻量化以及多功能化的需求的增加，希望在应用于开关型调节器的集成电路芯片中集成更多的元件。除了控制芯片之外，集成电路芯片还可以包含传统的分立元件，例如功率器件，以尽可能地减少分立元件的使用。在开关型调节器工作时，功率器件承载大电流，而控制芯片承载小电流。结果，在集成电路芯片内部，功率器件可能对控制芯片产生干扰。

[0004] 为了解决上述的干扰问题，可以将开关型调节器的控制芯片以及功率器件分别形成在不同的半导体芯片中，然后将控制芯片以及功率器件的至少一个封装在在一个封装料中，形成集成电路组件。在集成电路组件中，控制芯片堆叠在功率器件上方，因此控制芯片与位于其下方的功率器件之间的电连接非常困难。有时甚至需要改变功率器件内部的结构。例如，功率器件包括位于芯片一侧表面的源电极和栅电极，以及位于芯片相对的另一侧表面的漏电极。为了在功率器件上堆叠控制芯片，在功率器件中可能需要形成附加的导电通道，使得栅电极设置在与漏电极相同一侧的表面上。这将导致功率器件的结构复杂化，进一步导致封装组件的成本增加。此外，在采用键合线连接控制芯片和功率器件时，焊接和回流可能对功率器件造成损坏。这将导致封装组件的可靠性变差。

[0005] 因此，在应用于开关型调节器的集成电路组件中，期望进一步改进控制芯片和功率器件的布局和连接方式。

发明内容

[0006] 有鉴于此，本发明的目的在于提供一种应用于开关型调节器的集成电路组件，以解决现有技术中控制芯片与功率器件之间的连接对其性能造成不利影响的问题。

[0007] 根据本发明，提供一种应用于开关型调节器的集成电路组件，包括：引线框，其具有多个引脚和基底；第一功率器件芯片，其正面具有第一电极和控制电极，其背面具有第二电极；控制芯片，所述控制芯片堆叠在所述第一功率器件芯片上方，并且具有内部控制驱动电路以及与内部控制驱动电路电连接的多个焊垫；以及中间导电部件，其具有用于焊料互连的表面，其中，所述第一功率器件芯片的第一电极附着在所述基底上且与所述基底形成电连接，所述第一功率器件芯片的第二电极电连接至所述引线框的所述多个引脚中的至少一个引脚，所述第一功率器件芯片的控制电极通过导电凸块电连接到所述中间导电部件，

所述中间导电部件通过键合线连接到所述控制芯片的所述多个焊垫中的相应一个焊垫。

[0008] 优选地，所述集成电路组件还包括：第一金属带，将第一功率器件芯片的第二电极电连接至所述引线框的所述多个引脚中的至少一个引脚。

[0009] 优选地，所述集成电路组件还包括：第二功率器件芯片，其正面具有第一电极和控制电极，其背面具有第二电极，其中，所述第二功率器件芯片堆叠在所述第一功率器件芯片上方，所述第二功率器件芯片的第一电极电连接至所述引线框的所述多个引脚中的至少一个引脚，所述第二功率器件芯片的第二电极电连接至所述第一功率器件芯片的第一电极，所述第二功率器件芯片的控制电极通过键合线连接到所述控制芯片的所述多个焊垫中的相应一个焊垫。

[0010] 优选地，所述集成电路组件还包括：导电层，其设置在第一功率器件芯片的第二电极上；以及第一金属带，将导电层电连接至所述引线框的所述多个引脚中的至少一个引脚。进一步优选地，所述集成电路组件还包括：绝缘层，其设置在控制芯片和导电层之间。进一步优选地，所述集成电路组件还包括：第二金属带，将第二功率器件芯片的第一电极电连接至所述引线框的所述多个引脚中的至少一个引脚。

[0011] 优选地，所述集成电路组件还包括：第一绝缘层，其设置在第一功率器件芯片的第二电极上；导电层，其设置在所述第一绝缘层和第二功率器件芯片的第二电极之间；以及第一金属带，将第一功率器件芯片的第二电极电连接至所述引线框的所述多个引脚中的至少一个引脚。进一步优选地，所述集成电路组件还包括：第二金属带，将第二功率器件芯片的第一电极电连接至所述引线框的所述多个引脚中的至少一个引脚。进一步优选地，在所述集成电路组件中，第一金属带和第二金属带通过公共的引脚电连接。进一步优选地，所述集成电路组件还包括：第三金属带，将第二功率器件芯片的第二电极电连接至所述引线框的所述多个引脚中的至少一个引脚。进一步优选地，所述集成电路组件还包括：第二绝缘层，其设置在控制芯片和导电层之间。

[0012] 优选地，在所述集成电路组件中，所述第一电极是场效应晶体管的源极和漏极中的一个，所述第二电极是场效应晶体管的源极和漏极中的另一个，所述控制电极是场效应晶体管的栅极。

[0013] 优选地，在所述集成电路组件中，所述第一电极是双极性晶体管的发射极和集电极中的一个，所述第二电极是双极性晶体管的发射极和集电极中的另一个，所述控制电极是双极性晶体管的基极。

[0014] 优选地，所述集成电路组件还包括封装料，所述封装料覆盖控制芯片和第一功率器件芯片，并且覆盖引线框的至少一部分，使得引线框的引脚的端部或底部暴露用于外部电连接。

[0015] 优选地，所述集成电路组件还包括封装料，还包括封装料，所述封装料覆盖控制芯片、第一功率器件芯片和第二功率器件芯片，并且覆盖引线框的至少一部分，使得引线框的引脚的端部或底部暴露用于外部电连接。

[0016] 在本发明的集成电路组件中，针对控制芯片与下部层面的的电连接，使用了中间连接部件。功率器件芯片的控制电极可以面朝下设置，从而不需要在功率器件芯片内部设置附加的导电通道。这提供了集成电路组件的设计灵活性，并且降低了集成电路组件的制造成本。并且，在集成电路组件的封装过程中，键合线未直接连接至下部层面的功率器件芯

片的控制电极。这不仅便于实现电连接，而且可以减轻在功率器件芯片的控制电极上焊接键合线而导致功率器件芯片损坏的风险。

附图说明

[0017] 通过以下参照附图对本发明实施例的描述，本发明的上述以及其他目的、特征和优点将更为清楚，在附图中：

[0018] 图 1a 和 1b 分别示出根据本发明的第一实施例的应用于开关型调节器的集成电路组件的透视图和俯视图；

[0019] 图 2a 和 2b 分别示出根据本发明的第二实施例的应用于开关型调节器的集成电路组件的透视图和俯视图；以及

[0020] 图 3a 和 3b 示出根据本发明的第三实施例的应用于开关型调节器的集成电路组件的透视图和俯视图。

具体实施方式

[0021] 以下将参照附图更详细地描述本发明的各种实施例。在各个附图中，相同的元件采用相同或类似的附图标记来表示。

[0022] 为了清楚起见，附图中的各个部分没有按比例绘制。为了简明起见，可以在一幅图中描述经过数个步骤后获得的组件结构。此外，还可能省略某些公知的细节，例如，在所有的附图中未示出焊料和封装料，在一些附图中未示出用于支撑引线框的支撑材料和 / 或外部框架。

[0023] 应当理解，在描述组件结构时，当将一层、一个区域称为位于另一层、另一个区域“上面”或“上方”时，可以指直接位于另一层、另一个区域上面，或者在其与另一层、另一个区域之间还包含其它的层或区域。并且，如果将器件翻转，该一层、一个区域将位于另一层、另一个区域“下面”或“下方”。如果为了描述直接位于另一层、另一个区域上面的情形，本文将采用“直接在……上面”或“在……上面并与之邻接”的表述方式。

[0024] 在下文中描述了本发明的许多特定的细节，例如集成电路组件的结构、材料、尺寸、处理工艺和技术，以便更清楚地理解本公开。但正如本领域的技术人员能够理解的那样，可以不按照这些特定的细节来实现本公开。

[0025] 图 1a 和 1b 分别示出根据本发明的第一实施例的应用于开关型调节器的集成电路组件 100 的透视图和俯视图。在集成电路组件 100 中，功率器件芯片 120 安装在引线框 110 上，然后在功率器件芯片 120 上堆叠控制芯片 150。引线框 110 包括用于外部电连接的引脚 111 以及主要用于提供机械支撑的基底 112。应当注意，该集成电路组件 100 可以包括更多的晶体管和 / 或集成电路。

[0026] 功率器件芯片 120 包括位于其一侧表面上的第一电极 121 和控制电极 123，以及位于相对的另一侧表面上的第二电极 122。控制电极 123 与第一电极 121 之间彼此电隔离，并且与导电凸块 124（例如铜柱或焊球）接触。功率器件芯片 120 的第一电极 121 固定在引线框 110 的基底 112 上，然后经由基底 112 接地或连接至集成电路组件 100 的外部。功率器件芯片 120 的第二电极 122 经由金属带 126（例如铝带或铜夹）连接至引线框 110 的至少一个引脚 111。

[0027] 功率器件芯片 120 例如是选自双极性晶体管和场效应晶体管的一种。在双极性晶体管的情形下，功率器件芯片 120 的第一电极是发射极和集电极中的一个，第二电极是发射极和集电极中的另一个，控制电极是基极。在场效应晶体管的情形下，功率器件芯片 120 的第一电极是源极和漏极中的一个，第二电极是源极和漏中的另一个，控制电极是栅极。

[0028] 控制芯片 150 位于功率器件芯片 120 的上方，并且二者之间设置绝缘层 127，以实现电隔离。控制芯片 150 包括内部控制驱动电路，以及与内部控制驱动电路电连接的多个焊垫 151。所述多个焊垫 151 经由键合线 152 连接至相应的引脚 111。

[0029] 集成电路组件 100 还包括中间连接部件 125。中间连接部件 125 具有用于焊料互连的表面 125-1。中间连接部件 125 可以是引线框 110 的一部分，也可以是与引线框 110 不同的独立部分。在中间连接部件 125 的表面 125-1 上，中间连接部件 125 与功率器件芯片 120 的导电凸块 124 形成焊料互连。然后，中间连接部件 125 经由键合线 152 连接到控制芯片 150 的焊垫 151，使得功率器件芯片 120 的控制电极 123 与控制芯片 150 的驱动电极电连接。

[0030] 尽管未在图中示出，集成电路组件 100 还可以包括封装料。例如，该封装料覆盖控制芯片 150、功率器件芯片 120，并且覆盖引线框 110 的至少一部分，使得引线框 110 的引脚 111 的端部或底部暴露用于外部电连接。

[0031] 在优选的实施例中，由于中间连接部件 125 不需要与外围电路连接，因此可以将中间连接部件 125 完全包封在封装料内，从而可以避免将控制电极 123 引出封装料外部而产生的干扰。

[0032] 在优选的实施例中，在中间连接部件 125 的表面形成凹陷部。可以通过刻蚀方式制作凹陷部。将功率器件芯片 120 的导电凸块 124 设置于中间连接部件 125 的凹陷部中，从而有利于导电凸块 124 的对准和机械固定。

[0033] 在上述实施例中，描述了功率器件芯片 120 的第一电极 121、第二电极 122 和控制电极 123 分别与集成电路组件的各个导电部件的表面接触，因此可以避免将任何键合线直接连接至下部层面的功率器件芯片 120。然而，在替代的实施例中，可以将键合线直接连接到第一电极 121 和第二电极 122 中的至少一个上，仍然使用中间连接部件 125，以避免将键合线直接连接至功率器件芯片 120 的控制电极。在本发明的各个实施例中，中间连接部件 125 作为功率器件芯片 120 的控制电极 123 与控制芯片 150 的驱动电极之间的导电路径的一部分。

[0034] 在上述根据第一实施例的集成电路组件 100 中，由于使用了中间连接部件 125，功率器件芯片 120 的控制电极 123 可以面朝下设置，从而不需要在功率器件芯片 120 内部设置附加的导电通道。这提供了集成电路组件的设计灵活性，并且降低了集成电路组件的制造成本。并且，在集成电路组件 100 的封装过程中，键合线 152 连接至中间连接部件 125，而未直接连接至下部层面的功率器件芯片 120 的控制电极 123。这不仅便于下部层面的功率器件芯片 120 的电连接，而且可以避免在功率器件芯片 120 的控制电极 123 上焊接键合线 152 而导致功率器件芯片 120 损坏的风险。

[0035] 图 2a 和 2b 分别示出根据本发明的第二实施例的应用于开关型调节器的集成电路组件 200 的透视图和俯视图。在集成电路组件 200 中，功率器件芯片 220 安装在引线框 210 上，然后在功率器件芯片 220 上堆叠功率器件芯片 230 和控制芯片 250。引线框 210 包括用

于外部电连接的引脚 211 以及主要用于提供机械支撑的基底 212。应当注意，该集成电路组件 200 可以包括更多的晶体管和 / 或集成电路。

[0036] 第二实施例与第一实施例的不同之后在于在集成电路组件 200 中包含两个功率器件芯片 220、230，并且控制芯片 250 和功率器件芯片 230 位于同一个层面上。

[0037] 功率器件芯片 220 包括位于其一侧表面上的第一电极 221 和控制电极 223，以及位于相对的另一侧表面上的第二电极 222。控制电极 223 与第一电极 221 之间彼此电隔离，并且与导电凸块 224（例如铜柱或焊球）接触。功率器件芯片 220 的第一电极 221 固定在引线框 210 的基底 212 上，然后经由基底 212 接地或连接至集成电路组件 200 的外部。在功率器件芯片 220 的第二电极 222 上设置导电层 228（例如厚铜层）。

[0038] 功率器件芯片 230 位于功率器件芯片 220 上方。功率器件芯片 230 包括位于其一侧表面上的第一电极 231 和控制电极 233，以及位于相对的另一侧表面上的第二电极 232。功率器件芯片 230 的第一电极 231 经由金属带 234（例如铝带或铜夹）连接至引线框 210 的至少一个引脚 211。功率器件芯片 230 的第二电极 232 接触导电层 228，从而与功率器件芯片 220 的第二电极 222 电连接。导电层 228 经由金属带 226（例如铝带或铜夹）连接至引线框 210 的至少一个引脚 211。

[0039] 控制芯片 250 位于功率器件芯片 220 上方。例如，控制芯片 250 位于导电层 228 上方。优选地，在控制芯片 250 和导电层 228 之间设置绝缘层 229，以实现电隔离，从而避免功率器件芯片 220 中的大电流对控制芯片 250 的干扰。控制芯片 250 包括内部控制驱动电路，以及与内部控制驱动电路电连接的多个焊垫 251。所述多个焊垫 251 经由键合线 252 连接至相应的引脚 211，以及连接到同一层面的功率器件芯片 230 的控制电极 233。

[0040] 集成电路组件 200 还包括中间连接部件 225。中间连接部件 225 具有用于焊料互连的表面 225-1。中间连接部件 225 可以是引线框 210 的一部分，也可以是与引线框 210 不同的独立部分。在中间连接部件 225 的表面 225-1 上，中间连接部件 225 与功率器件芯片 220 的导电凸块 224 形成焊料互连。然后，中间连接部件 225 经由键合线 252 连接到控制芯片 250 的焊垫 251，使得功率器件芯片 220 的控制电极 223 与控制芯片 250 的驱动电极电连接。

[0041] 尽管未在图中示出，集成电路组件 200 还可以包括封装料。例如，该封装料覆盖控制芯片 250、功率器件芯片 220 和 230，并且覆盖引线框 210 的至少一部分，使得引线框 210 的引脚 211 的端部或底部暴露用于外部电连接。

[0042] 根据第二实施例的集成电路组件 200 的其他部分与根据第一实施例的集成电路组件 100 的相应部分相同。

[0043] 在上述根据第二实施例的集成电路组件 200 中，控制芯片 250 与同一层面的功率器件芯片 230 之间连接容易，因此采用键合线 252 直接连接。对于下部层面的功率器件芯片 220 的控制电极 223，使用了中间连接部件 225。如上所述，该中间连接部件 225 提供了设计灵活性、降低成本、以及提高集成电路组件的可靠性。

[0044] 图 3a 和 3b 示出根据本发明的第三实施例的应用于开关型调节器的集成电路组件 300 的透视图和俯视图。在集成电路组件 300 中，功率器件芯片 320 安装在引线框 310 上，然后在功率器件芯片 320 上堆叠功率器件芯片 330 和控制芯片 350。引线框 310 包括用于外部电连接的引脚 311 以及主要用于提供机械支撑的基底 312。应当注意，该集成电路组件

300 可以包括更多的晶体管和 / 或集成电路。

[0045] 第三实施例与第二实施例的不同之后在于功率器件芯片 320 的第二电极 322 与功率器件芯片 330 的第一电极 331 电连接，并且与功率器件芯片 330 的第二电极 332 电隔离。

[0046] 功率器件芯片 320 包括位于其一侧表面上的第一电极 321 和控制电极 323，以及位于相对的另一侧表面上的第二电极 322。功率器件芯片 320 的第二电极 322 经由金属带 334（例如铝带或铜夹）连接至引线框 310 的至少一个引脚 311。控制电极 323 与第一电极 321 之间彼此电隔离，并且与导电凸块 324（例如铜柱或焊球）接触。功率器件芯片 320 的第一电极 321 固定在引线框 310 的基底 312 上，然后经由基底 312 接地或连接至集成电路组件 300 的外部。在功率器件芯片 320 的第二电极 322 之间设置彼此独立的第一绝缘层 328 和第二绝缘层 336，以实现电隔离。在第二绝缘层 336 上设置导电层 337。第一绝缘层 328 是优选的，用于避免功率器件芯片 320 中的大电流对控制芯片 350 的干扰。在替代的实施例中，第二绝缘层 336 和第一绝缘层 328 一体形成。在第二绝缘层 336 上设置导电层 337。

[0047] 功率器件芯片 330 包括位于其一侧表面上的第一电极 331 和控制电极 333，以及位于相对的另一侧表面上的第二电极 332。功率器件芯片 330 的第一电极 331 经由金属带 335（例如铝带或铜夹）连接至引线框 310 的至少一个引脚 311。在封装料部，金属带 334 和金属带 335 可以连接至相同的引脚 311，使得第一功率器件芯片 320 的第二电极 322 与第二功率器件芯片 330 的第一电极 331 彼此电连接。功率器件芯片 330 的第二电极 332 接触导电层 337。导电层 337 经由金属带 326（例如铝带或铜夹）连接至引线框 310 的至少一个引脚 311。

[0048] 控制芯片 350 位于功率器件芯片 320 上方。例如，在第一绝缘层 328 上设置控制芯片 350，使得第一绝缘层 328 将控制芯片 350 与功率器件芯片 320 的第二电极 322 隔开。控制芯片 350 包括内部控制驱动电路，以及与内部控制驱动电路电连接的多个焊垫 351。所述多个焊垫 351 经由键合线 352 连接至相应的引脚 311，以及连接到同一层面的功率器件芯片 330 的控制电极 333。

[0049] 集成电路组件 300 还包括中间连接部件 325。中间连接部件 325 具有用于焊料互连的表面 325-1。中间连接部件 325 可以是引线框 310 的一部分，也可以是与引线框 310 不同的独立部分。在中间连接部件 325 的表面 325-1 上，中间连接部件 325 与功率器件芯片 320 的导电凸块 324 形成焊料互连。然后，中间连接部件 325 经由键合线 352 连接到控制芯片 350 的焊垫 351，使得功率器件芯片 320 的控制电极 323 与控制芯片 350 的驱动电极电连接。

[0050] 尽管未在图中示出，集成电路组件 300 还可以包括封装料。例如，该封装料覆盖控制芯片 350、功率器件芯片 320 和 330，并且覆盖引线框 310 的至少一部分，使得引线框 310 的引脚 311 的端部或底部暴露用于外部电连接。

[0051] 根据第三实施例的集成电路组件 300 的其他部分与根据第二实施例的集成电路组件 200 的相应部分相同。

[0052] 在上述根据第三实施例的集成电路组件 300 中，控制芯片 350 与同一层面的功率器件芯片 330 之间连接容易，因此采用键合线 352 直接连接。对于下部层面的功率器件芯片 320 的控制电极 323，使用了中间连接部件 325。如上所述，该中间连接部件 325 提供了设计灵活性、降低成本、以及提高集成电路组件的可靠性。

[0053] 应当说明的是，在本文中，诸如第一和第二等之类的关系术语仅仅用来将一个实体或者操作与另一个实体或操作区分开来，而不一定要求或者暗示这些实体或操作之间存在任何这种实际的关系或者顺序。而且，术语“包括”、“包含”或者其任何其他变体意在涵盖非排他性的包含，从而使得包括一系列要素的过程、方法、物品或者设备不仅包括那些要素，而且还包括没有明确列出的其他要素，或者是还包括为这种过程、方法、物品或者设备所固有的要素。在没有更多限制的情况下，由语句“包括一个……”限定的要素，并不排除在包括所述要素的过程、方法、物品或者设备中还存在另外的相同要素。

[0054] 依照本发明的实施例如上文所述，这些实施例并没有详尽叙述所有的细节，也不限制该发明仅为所述的具体实施例。显然，根据以上描述，可作很多的修改和变化。本说明书选取并具体描述这些实施例，是为了更好地解释本发明的原理和实际应用，从而使所属技术领域技术人员能很好地利用本发明以及在本发明基础上的修改使用。本发明仅受权利要求书及其全部范围和等效物的限制。

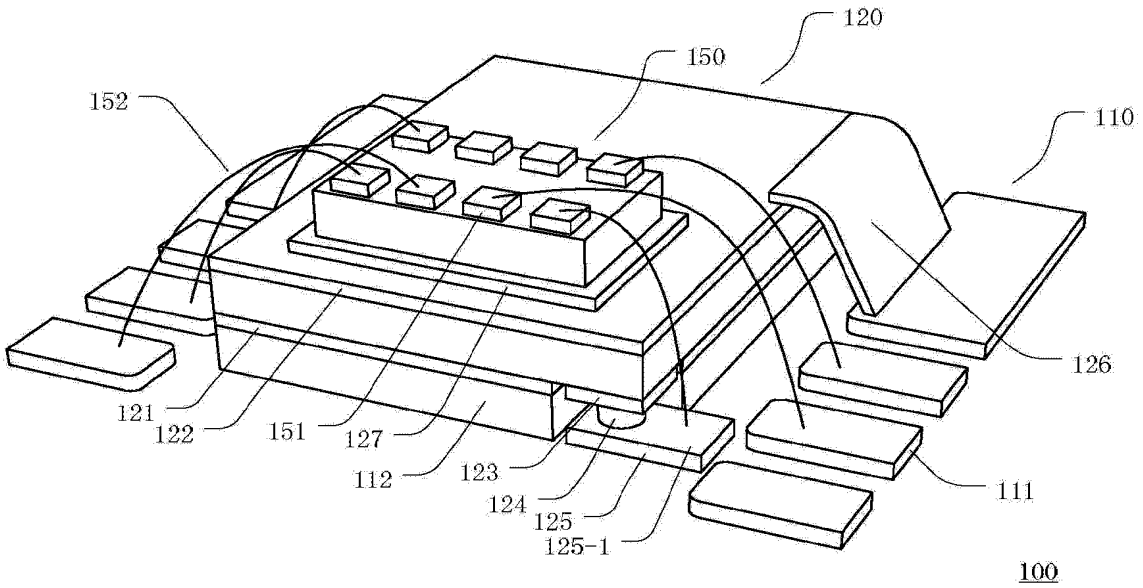

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图 1a

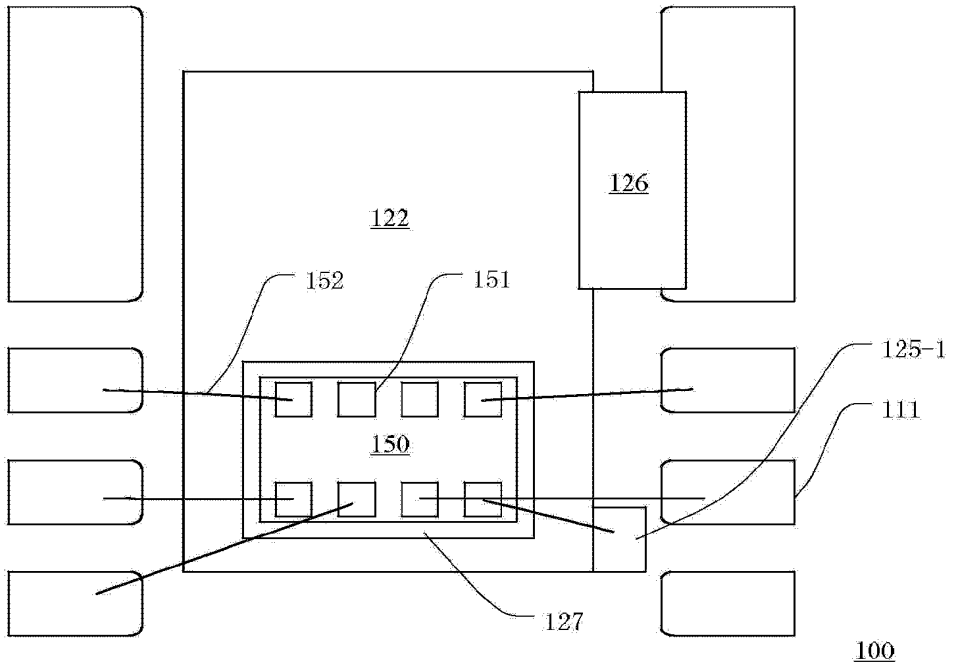

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图 1b

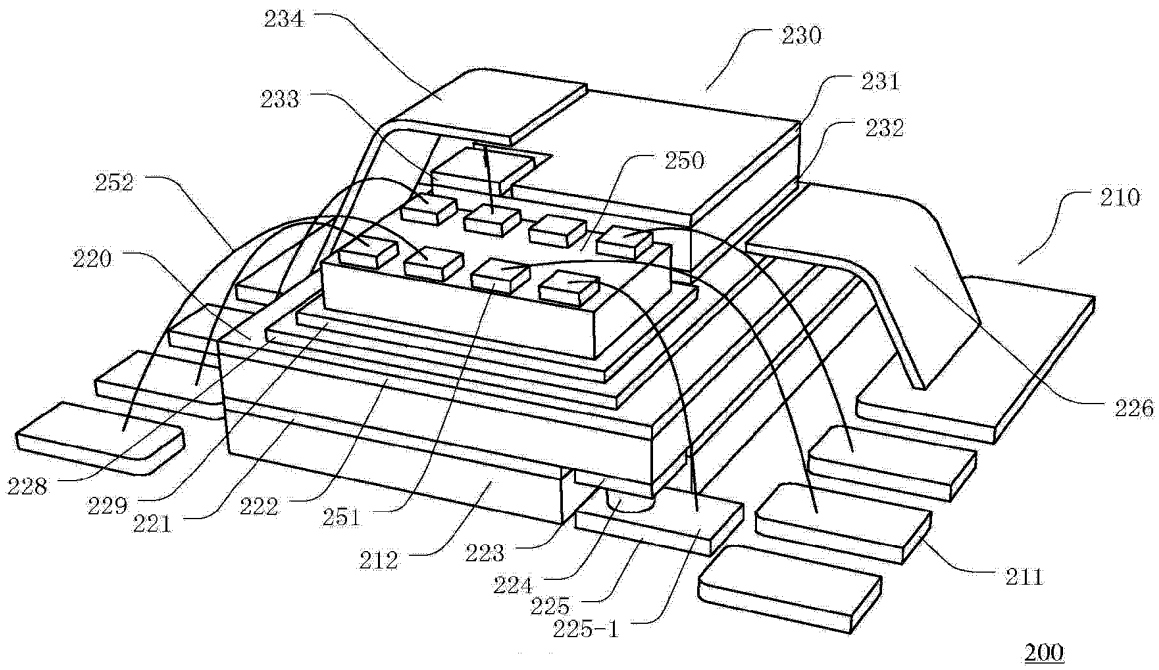

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图 2a

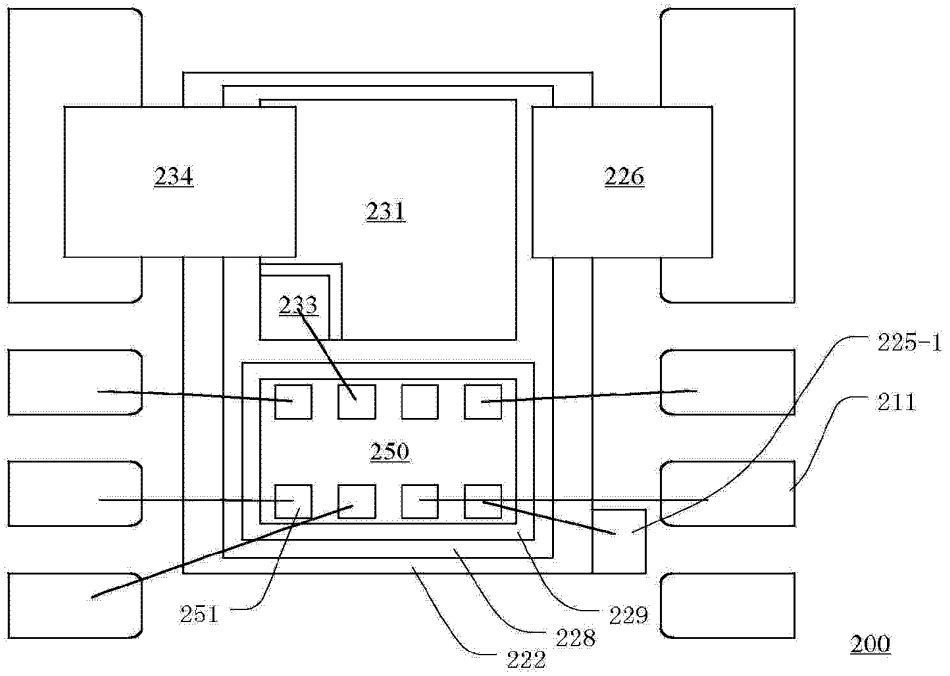

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图 2b

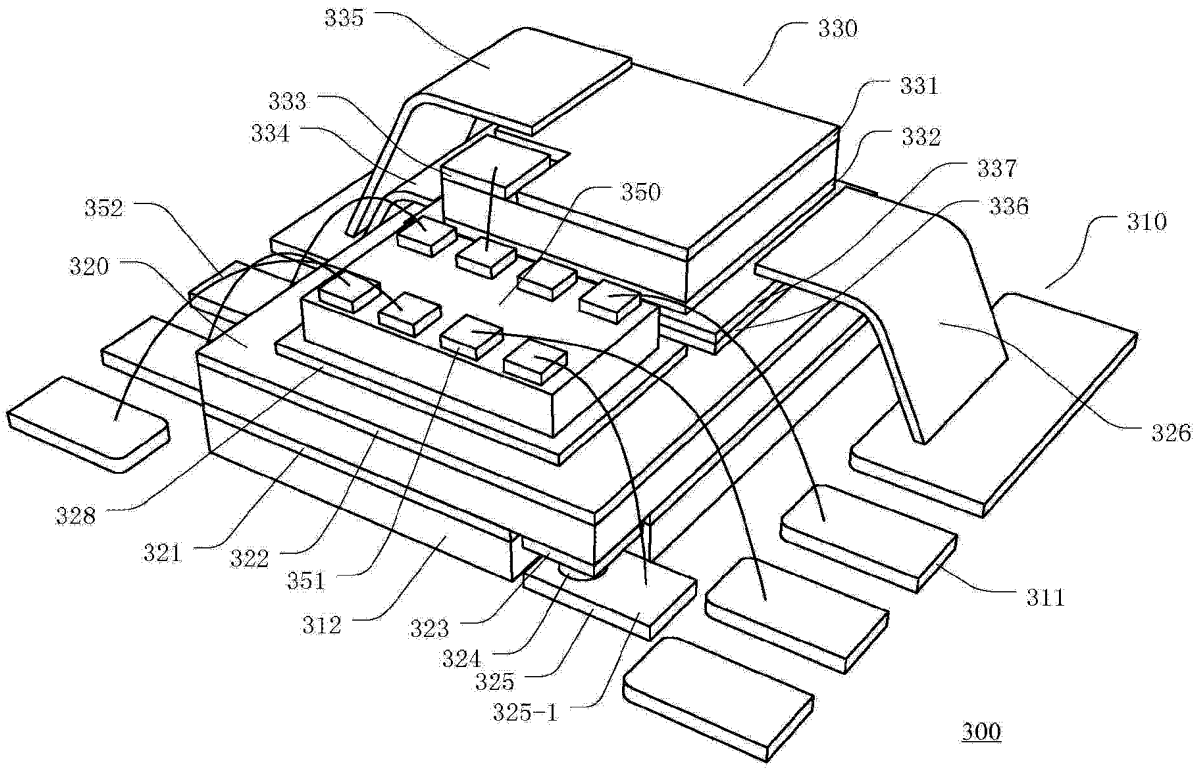

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图 3a

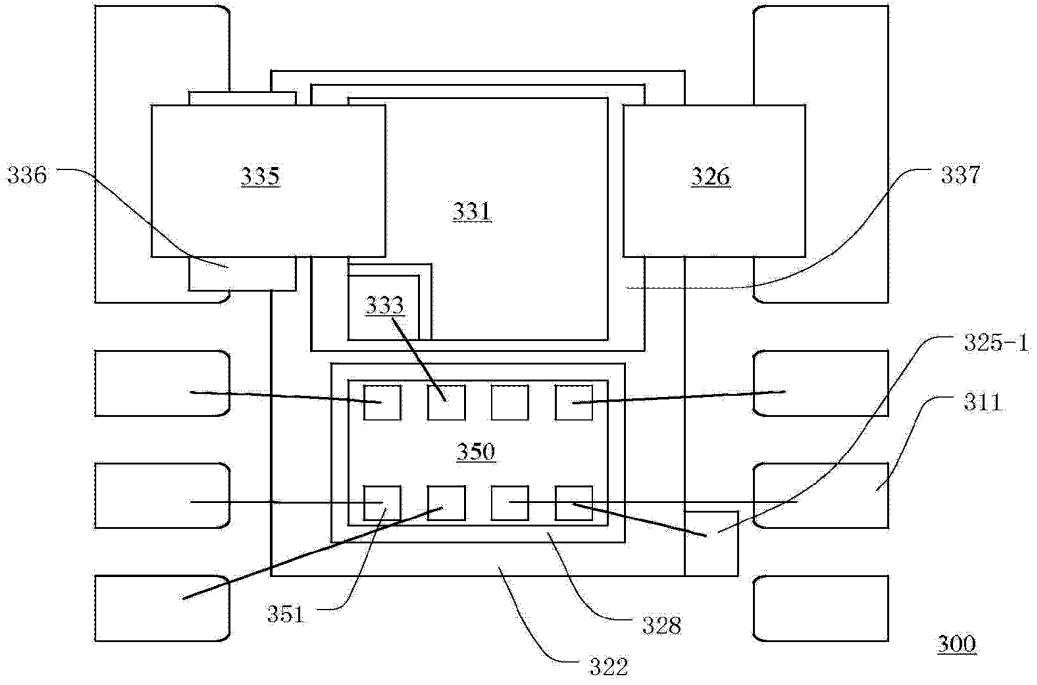

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图 3b

Electronic Patent Application Fee Transmittal

Application Number:	14840063
Filing Date:	31-Aug-2015
Title of Invention:	POWER SUPPLY APPARATUS
First Named Inventor/Applicant Name:	Jian-Hong ZENG
Filer:	James Lynn O'Sullivan/Anny TENG
Attorney Docket Number:	TWT04064/US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	19	80	1520
INDEPENDENT CLAIMS IN EXCESS OF 3	1201	2	420	840
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

IPR2024-00715 EX. 2005

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2360**

Electronic Acknowledgement Receipt

EFS ID:	30777371
Application Number:	14840063
International Application Number:	
Confirmation Number:	8903
Title of Invention:	POWER SUPPLY APPARATUS
First Named Inventor/Applicant Name:	Jian-Hong ZENG
Customer Number:	60589
Filer:	James Lynn O'Sullivan
Filer Authorized By:	
Attorney Docket Number:	TWT04064/US
Receipt Date:	26-OCT-2017
Filing Date:	31-AUG-2015
Time Stamp:	23:36:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$2360
RAM confirmation Number	102717INTEFSW00010604504669
Deposit Account	504669
Authorized User	James O'Sullivan

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	TWT04064US-rNonFinal-20171027.pdf	217686 13176a0cc4e1d449e1209fc9e87b762158c347af	no	16
Warnings:					
Information:					
2	Drawings-only black and white line drawings	TWT04064US-rFig-20171027.pdf	157397 a19060baf526edaa35d8c05550bfc05b0cceb532	no	1
Warnings:					
Information:					
3	Transmittal Letter	TWT04064US-IDSLetter-20171027.pdf	97922 3861c955da743c90db542232e324e5e60b1f9a5d	no	3
Warnings:					
Information:					
4	Information Disclosure Statement (IDS) Form (SB08)	TWT04064US-IDSForm-20171027.pdf	1035413 3bbe4574b903bee8668d9891b795411466af9e16	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
5	Foreign Reference	CN1332512A.pdf	2752871 09b412244bd6516602871dd273b23d2b780bedb9	no	10
Warnings:					
Information:					

6	Foreign Reference	CN103596365A.pdf	907439 e7846a767b1c9f53a60b36beb62c24d9b834c6c7	no	7
Warnings:					
Information:					
7	Foreign Reference	CN103872036A.pdf	2520527 2de3d52f0f2340ec3e77b80cbe496f8f3b17a0ab	no	16
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8	Foreign Reference	CN103824853A.pdf	2423455 b4d34cd91cdebe7eb8c506c7c208284cd32179f3	no	14
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9	Fee Worksheet (SB06)	fee-info.pdf	32109 78d97b5f7e4cf1bb94243b8175f3ac77d3d6cbf5	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	10144819	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/840,063	08/31/2015	Jian-Hong ZENG	TWT04064/US	8903

60589 7590 07/27/2017

JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

EXAMINER
YANCHUS III, PAUL B

ART UNIT	PAPER NUMBER
2115	

NOTIFICATION DATE	DELIVERY MODE
07/27/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

info@ckc-ip.com
ckchen@ckc-ip.com
josullivan@ckc-ip.com

Office Action Summary	Application No. 14/840,063	Applicant(s) ZENG ET AL.	
	Examiner PAUL YANCHUS III	Art Unit 2115	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/14/17*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-11 and 13-19* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-11 and 13-19* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

IPR2024-00715 EX. 2005

DETAILED ACTION

This non-final office action is in response to communications filed on 4/14/17.

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Rejections - 35 USC § 102

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

Claims 1-3, 8, 10, 11 and 17-19 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Matsumoto et al., US Patent Application Publication no. 2005/0189566 [Matsumoto].

Regarding claim 1, Matsumoto discloses a power supply apparatus, comprising:

a power unit electrically connected with a motherboard, comprising a first base plate, at least a power switch chip allocated at the first base plate and a plurality of pads [switching power supply circuit 2B (or P_B), Figures 1 and 2 and paragraphs 0037, 0039, 0040 and 0045-0047];

a control unit stacked with the power unit, comprising a second base plate and at least a control chip for controlling the power switch chip turn on/ off in the power unit and a plurality of pads [switching power supply circuit 2A (or P_A) includes a control circuit section for controlling semiconductor switches 30a and 30b, Figures 1 and 2 and paragraphs 0037, 0039, 0040 and 0045-0047]; and

a plurality of pins for electrically connecting the power unit to the control unit and mother board and allocated at periphery of the power unit and control unit [Figure 1 and paragraphs 0037-0040];

wherein the plurality of pads of the power unit and control unit are allocated on side facet of the first base plate and second base plate respectively, both plurality of pads of the power unit and control unit are electrically connected with the plurality of pins so that the power unit and the control unit are electrically connected with each other, the power supply apparatus provides a power source for a load in the neighborhood thereof on the motherboard [Figure 1 and paragraphs 0037-0040 and 0040-0047].

Regarding claim 2, Matsumoto further discloses that the first base plate and the second base plate are in a substantially same size [Figure 1].

Regarding claim 3, Matsumoto further discloses that the second base plate integrates a power switch chip to improve area utilization thereof [paragraph 0045].

Regarding claim 8, Matsumoto further discloses another power unit stacked with the power unit and the control unit, wherein the another power unit is parallel connected and controlled by the control unit [paragraph 0076].

Regarding claim 10, Matsumoto further discloses that the plurality of pins cover outer surface of the power unit and the control unit respectively [Figure 1 and paragraphs 0037-0040].

Regarding claim 11, Matsumoto further discloses that the power unit is the one close to the motherboard, the control unit is the other one stacked on the power unit [Figures 1 and 2 and paragraphs 0037, 0039, 0040 and 0045-0047].

Regarding claim 17, Matsumoto discloses a power supply apparatus, comprising:

a first unit electrically connected with a motherboard, comprising a first base plate, and at least a power switch chip allocated at the first base plate [switching power supply circuit 2B (or P_B), Figures 1 and 2 and paragraphs 0037, 0039, 0040 and 0045-0047];

a second unit stacked with the first unit [switching power supply circuit 2A (or P_A), Figures 1 and 2 and paragraphs 0037, 0039, 0040 and 0045-0047];

a plurality of pins for electrically connecting the first unit to the second unit and mother board and allocated at periphery of the first unit [Figure 1 and paragraphs 0037-0040]; and

a plurality of pads distributed along a lateral side of the first unit and a lateral side of the second unit, and electrically coupled with the plurality of pins, wherein the plurality of pins include surface-mount pins, and are distributed along the outer surface of the first unit and the second unit [Figure 1 and paragraphs 0037-0040].

Regarding claim 18, Matsumoto further discloses that the second unit has a surface facing the first unit and a plurality of connection pads disposed on the surface [Figure 1 and paragraphs 0037-0040].

Regarding claim 19, Matsumoto further discloses that the pins extends along the out surface of the first unit to connect the connection pad of the second unit with the first unit [Figure 1 and paragraphs 0037-0040].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4-7, 9 and 13 are rejected under 35 U.S.C. 103 as being unpatentable over Matsumoto et al., US Patent Application Publication no. 2005/0189566 [Matsumoto].

Regarding claims 4-7, Matsumoto does not disclose using molding materials for encapsulating the power unit and control unit. Examiner takes official notice that molding materials were conventionally used in stacked circuit applications before the effective filing date of the claimed invention. Accordingly, it would have been obvious to one of ordinary skill in the art use conventional molding materials to encapsulate the power and control units in Matsumoto.

Regarding claim 9, Matsumoto discloses that each of the power unit and the another power unit has a magnetic device [paragraphs 0044 and 0057]. Matsumoto

does not disclose that the magnetic devices of the power unit and the another power unit share the same magnetic core. Examiner takes official notice multiple coupled power units conventionally shared magnetic cores before the effective filing date of the claimed invention. Accordingly, it would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to have the magnetic devices in Matsumoto share the same magnetic core in order reduce the number of components required to implement the power system.

Regarding claim 13, Matsumoto does not disclose a heat sink attached to the power unit to improve hear dissipation. Examiner takes official notice that heat sinks were conventionally included in power units to improve heat dissipation before the effective filing date of the claimed invention. Accordingly, it would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to attach a conventional heat sink to the power unit in Matsumoto in order to improve heat dissipation.

Claims 14-16 are rejected under 35 U.S.C. 103 as being unpatentable over Matsumoto et al., US Patent Application Publication no. 2005/0189566 [Matsumoto], in view of Kondou et al., US Patent Application Publication no. 2014/0306674 [Kondou].

Matsumoto, as described above, discloses a plurality of power circuits stacked vertically and connected via pins to each other and to a motherboard in order to provide converted power. Matsumoto does not disclose that the power circuits are arranged in cascaded stages such that one of the power circuits provides power to the input of the

other power circuit. Like Matsumoto, Kondou discloses a power conversion circuit arrangement in which power circuits may be stacked vertically. Specifically, Kondou discloses that the power control circuits may be power conversion stages stacked vertically and cascaded such that a second power conversion stage receives input power from a first power conversion stage [paragraph 0058]. Since it was known in the art before the effective filing date of the claimed invention to arrange power conversion circuits in a cascaded and vertically stacked configuration, it would have been obvious to one of ordinary skill in the art to apply the Matsumoto teachings to cascaded and vertically stacked power conversion circuits.

Response to Arguments

Applicant's arguments, with respect to the previous rejections of claims 1-11 and 13-19 have been fully considered and are persuasive. Therefore, the rejections have been withdrawn. However, upon further consideration, new grounds of rejection are made in view of Matsumoto and the combination of Matsumoto and Kondou.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL YANCHUS III whose telephone number is (571)272-3678. The examiner can normally be reached on Mon-Fri 10AM-6PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/PAUL YANCHUS III/
Primary Examiner, Art Unit 2115
July 22, 2017

Notice of References Cited	Application/Control No. 14/840,063	Applicant(s)/Patent Under Reexamination ZENG ET AL.	
	Examiner PAUL YANCHUS III	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2014/0306674 A1	10-2014	KONDOU; Masafumi	H02M3/158	323/271
*	B	US-2005/0189566 A1	09-2005	Matsumoto, Tadahiko	H02M3/33538	257/200
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	104	(vertical$2 near6 (power adj3 stage$1))	US-PGPUB; USPAT	OR	OFF	2017/07/22 12:24
L2	8	(vertical$2 near4 (regulator$1 or converter$1)) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2017/07/22 12:25
L3	4	("6879493" | "20050017345" | "6809268" | "20050051889").PN.	US-PGPUB; USPAT	OR	OFF	2017/07/22 12:30
L4	10	(stack$4 near4 (regulator$1 or converter$1)) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2017/07/22 12:39
L5	3168	(stack$4 near4 (regulator$1 or converter$1))	US-PGPUB; USPAT	OR	OFF	2017/07/22 12:39
L6	93	((stack$4 near4 stage$1) with (regulator$1 or converter$1))	US-PGPUB; USPAT	OR	OFF	2017/07/22 12:40
L7	83	((vertical$2 near4 stage$1) with (regulator$1 or converter$1))	US-PGPUB; USPAT	OR	OFF	2017/07/22 12:40
L8	13	(stack$4 near4 (power adj1 supply)) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2017/07/22 12:51
L9	9	("2005/0189566").URPN.	USPAT	OR	OFF	2017/07/22 12:54
L10	12	("4571663" | "5079835" | "5446620" | "5754408" | "5847985" | "6005778" | "6487078" | "6545868" | "6621155" | "6801440").PN. OR ("7403397").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/07/22 12:54
L11	262	(vertical$2 with cascad$4) with (converter$1 or stage$1 or regulator$1)	US-PGPUB; USPAT	OR	OFF	2017/07/22 13:51
L12	312	(stack$5 with cascad$4) with (converter$1 or stage$1 or regulator$1)	US-PGPUB; USPAT	OR	OFF	2017/07/22 13:51
L13	1	11 and motherboard$1	US-PGPUB; USPAT	OR	OFF	2017/07/22 14:00
L14	1	12 and motherboard$1	US-PGPUB; USPAT	OR	OFF	2017/07/22 14:00
L15	3	1 and molding$1	US-PGPUB; USPAT	OR	OFF	2017/07/22 15:06
L16	1297	((stack$4 or vertical$1) with (regulator$1 or converter$1)) and molding$1	US-PGPUB;	OR	OFF	2017/07/22 15:07

			USPAT			
L17	59	((stack$4 or vertical$1) with (regulator$1 or converter$1)) and (molding adj1 material$1)	US-PGPUB; USPAT	OR	OFF	2017/07/22 15:07
L18	1	"20050189566".pn. and transformer$1	US-PGPUB; USPAT	OR	OFF	2017/07/22 15:18
L19	1	"20050189566".pn. and (heat or thermal)	US-PGPUB; USPAT	OR	OFF	2017/07/22 15:25
S34	2972	(stack$4) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2017/07/21 16:50
S35	920	S34 and g06f$.cpc.	US-PGPUB; USPAT	OR	OFF	2017/07/21 16:50
S36	8503	(stack$4 with (regulator$1 or converter$1))	US-PGPUB; USPAT	OR	OFF	2017/07/21 16:50
S38	32	S36 same motherboard$1	US-PGPUB; USPAT	OR	OFF	2017/07/21 16:51

EAST Search History (Interference)

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14840063	ZENG ET AL.
	Examiner	Art Unit
	PAUL YANCHUS III	2116

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/09/2017	07/22/2017							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							
	11	✓	✓							
	12	✓	-							
	13	✓	✓							
	14	✓	✓							
	15	✓	✓							
	16	✓	✓							
	17	✓	✓							
	18	✓	✓							
	19	✓	✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14840063	ZENG ET AL.
	Examiner	Art Unit
	PAUL YANCHUS III	2116

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (see attached)	1/9/17	PBY
Inventor Name Search in PALM	1/9/17	PBY
NPL (Google)	1/9/17	PBY
Updated EAST Search	7/22/17	PBY

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant :	ZENG ET AL.	Attorney Docket No. :	TWT04064/US
Serial No. :	14/840,063	Group Art Unit:	2115
Filed :	2015/08/31	Examiner:	YANCHUS III, PAUL B
Title:	POWER SUPPLY APPARATUS		

AMENDMENT AND RESPONSE TO OFFICE ACTION

Honorable Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

In response to the Official Action mailed Jan. 17, 2017, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks and Responses begin on page 8 of this paper.

Respectfully submitted,

/James Lynn O'Sullivan/

.....

Date : April 14, 2017

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Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently amended) A power supply apparatus, comprising:

a power unit electrically connected with a motherboard, comprising a first base plate, at least a power switch chip allocated at the first base plate and a plurality of pads;

a control unit stacked with the power unit, comprising a second base plate and at least a control chip for controlling the power switch chip turn on/ off in the power unit and a plurality of pads; and

a plurality of pins for electrically connecting the power unit to the control unit and mother board and allocated at periphery of the power unit and control unit;

wherein the plurality of pads of the power unit and control unit are allocated on side facet of the first base plate and second base plate respectively, both plurality of pads of the power unit and control unit are electrically connected with the plurality of pins so that the power unit and the control unit ~~could~~ are electrically connected with each other, the power supply apparatus provides a power source for a load in the neighborhood thereof on the motherboard.

2. (Currently amended) The power supply apparatus of claim 1,

wherein the first base plate and the second base plate are in a substantially same sizeapproximate sizes.

3. (Original) The power supply apparatus of claim 1, wherein the second base plate integrates a power switch chip to improve area utilization thereof.

4. (Original) The power supply apparatus of claim 1, further comprising molding material, wherein the molding material encapsulates the power unit and control unit respectively, the plurality of pads of the power unit and control unit emerges from molding material respectively.

5. (Original) The power supply apparatus of claim 4, wherein the molding material of the control unit has a plurality of recesses reserved for connection with the pins thereof.

6. (Original) The power supply apparatus of claim 4, wherein the molding material encapsulates two sides of the power unit.

7. (Original) The power supply apparatus of claim 6, wherein the power unit further comprises bottom pads emerged from one side of power unit that is encapsulated by the molding material for adjacent electrical connection thereof.

8. (Original) The power supply apparatus of claim 1, further comprising another power unit stacked with the power unit and the control unit, wherein

the another power unit is parallel connected with the power unit and controlled by the control unit.

9. (Original) The power supply apparatus of claim 8, wherein each of the power unit and the another power unit has a magnetic device, the magnetic devices of the power unit and the another power unit share the same magnetic core.

10. (Currently amended) The power supply apparatus of claim 1, wherein the plurality of pins cover outer surface of the power unit and the control unit respectively ~~as much as possible to expand the surface area thereof.~~

11. (Original) The power supply apparatus of claim 1, wherein the power unit is the one close to the motherboard, the control unit is the other one stacked on the power unit.

12. (Canceled)

13. (Original) The power supply apparatus of claim 1, further comprising:

a heat sink, attached with the power unit to improve heat dissipation.

14. (Currently amended) A power supply apparatus, comprising:

a first stage power converter ~~received~~ receiving a power source from a mother board and configured with a plurality of pads located on side facet

thereof;

a second stage power converter configured with a plurality of pads located on side facet thereof and stacked with the first stage power converter to receive an output of the first stage power converter to provide a power to a load in adjacent area thereof on the motherboard; and

a plurality of pins connected with the pads of the first or/and second stage power converter and the motherboard to realize the electrical connection therebetween.

15. (Original) The power supply apparatus of claim 14, wherein the output voltage of the second stage power converter is lower than the output voltage of the first stage power converter.

16. (Currently amended) The power supply apparatus of claim 14, wherein the first stage converter and the second stage converter are configured in a substantially same sizeapproximate sizes.

17. (Currently amended) A power supply apparatus, comprising:

a first unit electrically connected with a motherboard, comprising a first base plate, and at least a power switch chip allocated at the first base plate and a plurality of pads;

a second unit stacked with the first unit, having a plurality of connection pads for electrical connection; and

a plurality of pins for electrically connecting the first unit to the second unit and mother board and allocated at periphery of the first unit ; and

a plurality of pads distributed along a lateral side of the first unit and a

lateral side of the second unit, and electrically coupled with the plurality of pins, wherein the plurality of pins include surface-mount pins, and are distributed along the outer surface of the first unit and the second unit.

~~wherein the plurality of pads of the first unit are allocated on side facet of the first base plate, both plurality of pads of the first unit and plurality of connection pads of the second unit are electrically connected with the plurality of pins~~ so that the first unit and the second unit could electrically connected with each other, the power supply apparatus provides a power source for a load in the neighborhood thereof on the motherboard.

18. (Currently amended) The power supply apparatus of claim 17, wherein ~~the connection pads of~~ the second unit has a surface facing the first unit and a plurality of connection pads disposed on the surface, ~~allocates on the surface that stacked on the first unit.~~

19. (Original) The power supply apparatus of claim 18, wherein the pins extends along the out surface of the first unit to connect the connection pad of the second unit with the first unit.

Remarks and Responses

The Examiner is thanked for the thorough examination of the present application. The Office Action, however, tentatively rejected claims 1-19. In response, claims have been amended to more clearly define over the cited art.

Support for the amendment to claims is found in as-filed specification. Accordingly, the amendments do not introduce any new matter.

Claim Objection

Claims 1 and 14 have been corrected as suggested by the Examiner. Therefore, the objection of these claims should be withdrawn.

Claim Rejection - 35 U.S.C. § 112

Regarding the rejection of claims 2, 10, 16 and 18, these claims have been amended in a clear manner. Therefore, the rejection of these claims should be withdrawn.

Moreover, since claim 12 has been cancelled, the rejection of claim 12 should be withdrawn.

Claim Rejection - 35 U.S.C. § 102 and 103

Applicant respectfully requests reconsideration of the rejections for at least the reasons that follow.

> *A claim is anticipated only if **each and every** element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention*

*must be shown in as **complete detail** as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).*

"All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

First, *Harris* (US 2008/0101025 A1) only discloses that the power system **130** can include numerous embodiments for providing power to electronic components (such as heat-generating components **110**) but fails to disclose an **actual control unit** stacked with the power system **130**. Therefore, *Harris* fails to describe each and every element (e.g., a control unit stacked with the power unit) as set forth in the claim 1. According to this the stack structure as defined in claim 1, the height of the power supply can be more properly utilized so as to realize a smaller floor space at a given volume while retaining sufficient volume to ensure a higher efficiency; accordingly, it accomplishes both the high power pressure and high efficiency. (*See* par [0031] of the present application).

In addition, *Harris* not only fails to teach or suggest that the heat-generating component **110** has a control chip for controlling the power switch chip turn on/ off in the power system **130**, but also fails to teach or suggest that the power system **130** has a control chip for controlling the power switch chip turn on/ off in the heat-generating component **110**. Accordingly, it is clear that *Harris* fails to teach or suggest "a control unit ... comprising ... at least a control chip for controlling the power switch chip turn on/ off in the

power unit" as set forth in claim 1. Therefore, *Harris* does not disclose every element as set forth in claim 1. For at least this additional reason, the rejection of claim 1 should be withdrawn.

Moreover, *Inoue* (US-2002/0131258A1) only discloses that the module substrates **3a** and **3b** are connected in series, and the sum (Va+Vb) of an output voltage Va of the lower module substrate **3a** and an output voltage Vb of the upper module substrate **3b** is supplied to the load. However, *Inoue* fails to teach or suggest that the lower module substrate **3a** receives an output of the upper module substrate **3b** and/or the upper module substrate **3b** receives an output of the lower module substrate **3a**. Accordingly, it is clear that *Inoue* fails to teach or suggest "a second stage power converter ... to receive an output of the first stage power converter" as set forth in claim 14. Therefore, *Inoue* does not disclose every element as set forth in claim 14. For at least this reason, the rejection of claim 14 should be withdrawn.

Moreover, in Fig. 1B of *Inoue*, connecting pads **12** are fastened on a top surface of the motherboard **2** rather than lateral sides of the module substrate **3a** and **3b**. According to *Inoue*'s teaching, the module substrate **3a** and/or **3b** cannot act as the motherboard. In fact, connecting pads **12a** are used for connecting the motherboard **2** and the module substrate **3a** through connecting member **4a**, and connecting pads **12b** are used for connecting the motherboard **2** and the module substrate **3b** through connecting member **4b**.

However, in the present application, pads are used for connecting one unit (e.g., first/second unit) to another unit (e.g., second/first unit) rather than motherboard, and a first unit electrically connected with a motherboard is defined in claim 17 without needing *Inoue*'s pads **12** of motherboard **2**.

Accordingly, it is clear that *Inoue* fails to teach or suggest "a plurality of pads distributed along a lateral side of the first unit and a lateral side of the second unit" as set forth in claim 17. In order to achieve a better dissipation effect and to further reduce the overall size of the module, in claim 17, the pads are disposed at the lateral side of the bearing plate in each unit (*See* par [0100] of the present application). Therefore, *Inoue* does not disclose every element as set forth in claim 17. For at least this reason, the rejection of claim 17 should be withdrawn.

Based on 37 CFR 1.104, when a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified. However, the Office Action only roughly cites some paragraphs of the prior art, but fails to clearly explain which element of the prior art can be equaled to each and every element as set forth in the claims 1, 14 and 17.

In view of the foregoing remarks, it is respectfully submitted that the prior art utilized by the Office Action fails to disclose all claim limitations recited in independent claims 1, 14 and 17. Accordingly, reconsideration and withdrawal of this portion of the 35 U.S.C. § 103 rejections are respectfully requested. Insofar as all remaining claims depend from claims 1, 14 and 17, the rejections of the remaining claims should be withdrawn for at least the same reasons. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Conclusions

For all of the aforementioned reasons, applicants submit that the specification and claims are now in proper form, and that the claims define patentably over the prior art of record. Therefore applicants respectfully request allowance for this case at the Examiner's earliest convenience.

The Commissioner is hereby authorized to charge Deposit Account 50-4669 for any deficiencies or credit for any over payments.

Respectfully submitted,

/James Lynn O'Sullivan/

Date：April 14, 2017

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Electronic Acknowledgement Receipt

EFS ID:	28926575
Application Number:	14840063
International Application Number:	
Confirmation Number:	8903
Title of Invention:	POWER SUPPLY APPARATUS
First Named Inventor/Applicant Name:	Jian-Hong ZENG
Customer Number:	60589
Filer:	James Lynn O'Sullivan
Filer Authorized By:	
Attorney Docket Number:	TWT04064/US
Receipt Date:	14-APR-2017
Filing Date:	31-AUG-2015
Time Stamp:	04:56:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	TWT04064US-rNonFinal-20170414.pdf	2294347 d1b1dee1b10005e8350819ba6f4dc3af93b9eee2	no	12

Warnings:

IPR2024-00715 EX. 2005

Information:	
Total Files Size (in bytes):	2294347

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/840,063	Filing Date 08/31/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **04/14/2017**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
BRENDA HARRISON

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/840,063	08/31/2015	Jian-Hong ZENG	TWT04064/US	8903

60589 7590 01/17/2017

JAMES O""SULLIVAN
Room 1901, 19/F, Lee Garden One, 33 Hysan Avenue,
Causeway Bay
Hong Kong,
HONG KONG

EXAMINER
YANCHUS III, PAUL B

ART UNIT	PAPER NUMBER
2115	

NOTIFICATION DATE	DELIVERY MODE
01/17/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

info@ckc-ip.com
ckchen@ckc-ip.com
josullivan@ckc-ip.com

Office Action Summary	Application No. 14/840,063	Applicant(s) ZENG ET AL.	
	Examiner PAUL YANCHUS III	Art Unit 2116	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/18/16*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-19* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-19* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *8/31/15* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☒ All b)☐ Some** c)☐ None of the:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *7/18/16*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Objections

Claims 1 and 14 are objected to because of the following informalities:

Regarding claim 1, it appears that “could" in line 15 should instead be “are”.

Regarding claim 14, it appears that "received" in line 2 should instead be "receiving".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of 35 U.S.C. 112(b):

> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112(d):

> (d) REFERENCE IN DEPENDENT FORMS.—Subject to subsection (e), a claim in dependent form shall contain a reference to a claim previously set forth and then specify a further limitation of the subject matter claimed. A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.

Claim 10 is rejected under 35 U.S.C. 112(b), as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention. The language "as much

as possible" is indefinite because it is unclear what amount of coverage it is referring to. For examination purposes, the limitation will be disregarded.

Claims 2 and 16 are rejected under 35 U.S.C. 112(b) as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention. It is unclear what the language "in approximate sizes" means. For examination purposes, the limitation will be interpreted as the same size.

Claim 12 is rejected under 35 U.S.C. 112(d) as being of improper dependent form for failing to further limit the subject matter of the claim upon which it depends, or for failing to include all the limitations of the claim upon which it depends. Claim 12 conflicts with parent claim 1 in that claim requires the power unit and the control unit to be stacked while claim 12 requires that the power unit and control unit be on opposite sides of a motherboard. Since the claims conflict with each other, claim 12 fails to include all limitations of claim 1. Applicant may cancel the claim(s), amend the claim(s) to place the claim(s) in proper dependent form, rewrite the claim(s) in independent form, or present a sufficient showing that the dependent claim(s) complies with the statutory requirements.

Claim 18 is rejected under 35 U.S.C. 112(b) as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention. It is unclear what the language "wherein the connection pads of the second unit allocates on the surface that stacked on the first unit" means. For examination purposes, the limitation will be

interpreted such that the connection pads of the second unit are on the surface that is stacked on the first unit.

Claim Rejections - 35 USC § 102

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

Claims 1- 3, 8, 10, 11 and 13 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Harris et al., US Patent Application Publication no. 2008/0101025 [Harris][1].

Regarding claims 1 and 10, Harris discloses a power supply apparatus, comprising:

a power unit electrically connected with a motherboard, comprising a first base plate, at least a power switch chip allocated at the first base plate and a plurality of pads [Figure 1 and paragraphs 0024, 0026, 0028-0030 and 0039];

[1] Harris was cited in the 7/18/16 IDS.

a control unit stacked with the power unit, comprising a second base plate and at least a control chip for controlling the power switch chip turn on/ off in the power unit and a plurality of pads [Figure 1 and paragraphs 0024, 0026, 0028-0030 and 0039]; and

a plurality of pins for electrically connecting the power unit to the control unit and mother board and allocated at periphery of the power unit and control unit [connectors 140 in Figure 1 and paragraph 0028];

wherein the plurality of pads of the power unit and control unit are allocated on side facet of the first base plate and second base plate respectively, both plurality of pads of the power unit and control unit are electrically connected with the plurality of pins so that the power unit and the control unit could electrically connected with each other [Figure 1 and paragraph 0028], the power supply apparatus provides a power source for a load in the neighborhood thereof on the motherboard [paragraph 0024].

Regarding claim 2, Harris further discloses that the first base plate and the second base plate are in approximate sizes [Figure 1A].

Regarding claim 3, Harris further discloses that the second base plate integrates a power switch chip to improve area utilization thereof [paragraphs 0024 and 0026].

Regarding claim 8, Harris further discloses another power unit stacked with the power unit and the control unit, wherein the another power unit is parallel connected with the power unit and controlled by the control unit [paragraph 0045].

Regarding claim 11, Harris further discloses that the power unit is the one close to the motherboard, the control unit is the other one stacked on the power unit [paragraphs 0024 and 0045].

Regarding claim 13, Harris further discloses heat sink, attached with the power unit to improve heat dissipation [paragraph 0027].

Claims 14-19 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Inoue et al., US Patent Application Publication no. 2002/0131258 [Inoue].

Regarding claim 14, Inoue discloses a power supply apparatus, comprising:

a first stage power converter receiving a power source from a mother board and configured with a plurality of pads located on side facet thereof [Figure 1A and paragraphs 0038, 0039 and 0055];

a second stage power converter configured with a plurality of pads located on side facet thereof and stacked with the first stage power converter to receive an output of the first stage power converter to provide a power to a load in adjacent area thereof on the motherboard [Figure 1A and paragraphs 0038, 0039 and 0055]; and

a plurality of pins connected with the pads of the first or/and second stage power converter and the motherboard to realize the electrical connection therebetween [Figure 1A and paragraph 0040].

Regarding claim 15, Inoue further discloses that the output voltage of the second stage power converter is lower than the output voltage of the first stage power converter [paragraph0077].

Regarding claim 16, Inoue further discloses that the first stage converter and the second stage converter are configured in approximate sizes [paragraph 0080].

Regarding claim 17, Inoue discloses a power supply apparatus, comprising:

a first unit electrically connected with a motherboard, comprising a first base plate, at least a power switch chip allocated at the first base plate and a plurality of pads [Figure 1A and paragraphs 0038, 0039 and 0055];

a second unit stacked with the first unit, having a plurality of connection pads for electrical connection [Figure 1A and paragraphs 0038, 0039 and 0055]; and

a plurality of pins for electrically connecting the first unit to the second unit and mother board and allocated at periphery of the first unit [Figure 1A and paragraphs 0038, 0039, 0040 and 0055];

wherein the plurality of pads of the first unit are allocated on side facet of the first base plate, both plurality of pads of the first unit and plurality of connection pads of the second unit are electrically connected with the plurality of pins so that the first unit and the second unit could electrically connected with each other, the power supply apparatus provides a power source for a load in the neighborhood thereof on the motherboard [Figure 1A and paragraphs 0038, 0039, 0040 and 0055].

Regarding claim 18, Inoue further discloses that that the connection pads of the second unit are on the surface that is stacked on the first unit [Figure 1A].

Regarding claim 19, Inoue further discloses that the pins extends along the out surface of the first unit to connect the connection pad of the second unit with the first unit [Figure 1A and paragraphs 0038, 0039, 0040 and 0055].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4-7 and 9 are rejected under 35 U.S.C. 103 as being unpatentable over Harris et al., US Patent Application Publication no. 2008/0101025 [Harris].

Regarding claims 4-7, Harris does not disclose using molding materials for encapsulating the power unit and control unit. Examiner takes official notice that molding materials were conventionally used in stacked circuit applications before the effective filing date of the claimed invention. Accordingly, it would have been obvious to one of ordinary skill in the art use conventional molding materials to encapsulate the power and control units in Harris.

Regarding claim 9, Harris does not disclose that each of the power unit and the another power unit has a magnetic device, the magnetic devices of the power unit and the another power unit share the same magnetic core. Examiner takes official notice that power units conventionally included magnetic devices and multiple coupled power units conventionally shared magnetic cores before the effective filing date of the claimed invention. Accordingly, it would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to include conventional magnetic devices on the power units in Harris and to share the same magnetic core in order reduce the number of components required to implement the power system.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Elbanhawy et al., US Patent Application Publication no. 2010/0093132 discloses a stacked power module including an indictor and power transistor circuitry which is coupled to a motherboard.

Harris et al., US Patent no. 7,068,525 discloses a stacked power module system with redundant power modules.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAUL YANCHUS III whose telephone number is (571)272-3678. The examiner can normally be reached on Mon-Fri 10AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/PAUL YANCHUS III/
Primary Examiner, Art Unit 2116
January 9, 2017

Notice of References Cited	Application/Control No. 14/840,063	Applicant(s)/Patent Under Reexamination ZENG ET AL.	
	Examiner PAUL YANCHUS III	Art Unit 2116	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2010/0093132 A1	04-2010	Elbanhawy; Alan	H01L25/16	438/108
*	B	US-2002/0131258 A1	09-2002	Inoue, Keiji	H05K1/141	361/803
*	C	US-7,068,515 B2	06-2006	Harris; Shaun L.	H05K7/1092	165/80.3
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14840063	ZENG ET AL.
	Examiner	Art Unit
	PAUL YANCHUS III	2116

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	01/09/2017								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
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	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14840063
Filing Date	2015-08-31
First Named Inventor	Jian-Hong ZENG
Art Unit	2115
Examiner Name	LEE, THOMAS C
Attorney Docket Number	TWT04064/US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20080101025	A1	2008-05-01	HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P	
	2	20120173892	A1	2012-07-05	TONG SONG-LIN et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2399684	GB	A	2004-09-22	SHUTTLE INC		
	2	M253836	TW	U	2004-12-21	VAC CORP		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /B.Y./

IPR2024-00715 EX. 2005

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14840063
Filing Date	2015-08-31
First Named Inventor	Jian-Hong ZENG
Art Unit	2115
Examiner Name	LEE, THOMAS C
Attorney Docket Number	TWT04064/US

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NON-PATENT LITERATURE DOCUMENTS [Remove]

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		

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EXAMINER SIGNATURE

Examiner Signature	/PAUL B YANCHUS III/	Date Considered	01/09/2017

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /P.B.Y./

IPR2024-00715 EX. 2005

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	("20080101025" | "20120173892").PN.	US-PGPUB; USPAT	OR	OFF	2017/01/05 11:24
S2	2	("2008/0101025").URPN.	USPAT	OR	OFF	2017/01/05 12:34
S3	13	("20030198033" | "20040218367" | "4628407" | "4916575" | "5734555" | "5801924" | "6151215" | "6816378" | "6819562" | "6979784" | "7005586" | "7072185" | "7289328").PN.	US-PGPUB; USPAT	OR	OFF	2017/01/05 12:35
S4	8	("6979784").URPN.	USPAT	OR	OFF	2017/01/05 13:15
S5	20	("20020172022" | "20030002268" | "20030057548" | "4616655" | "5136471" | "5313096" | "5315069" | "5574630" | "5894411" | "6239485" | "6304450" | "6326647" | "6356448" | "6452113" | "6452804" | "6490160" | "6501103" | "6556455" | "6558169" | "6642730").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/01/05 13:15
S6	31	("6400566" | "6483704" | "6621701" | "5587882" | "6058013" | "4462462" | "5966291" | "5995370" | "4965710" | "6414867" | "6504722" | "5548090" | "5986887" | "6285550" | "5801924" | "6212076" | "6239366" | "5214563" | "5828125" | "5930115" | "5729433" | "5804872" | "6219236" | "6064573" | "6166937" | "5734555" | "5901040" | "6191945" | "6462410" | "6490161" | "5862038").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/01/05 13:16
S7	211	(power with stack$4) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2017/01/05 15:47
S8	31	(stack$4 with (regulator$1 or converter$1)) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2017/01/05 15:48
S10	0	(vertical$2 with power with stage$1) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2017/01/05 15:48
S11	28	(vertical$2 with (regulator$1 or converter$1)) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2017/01/05 15:48
S12	212	(power with vertical$2) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2017/01/05 15:48
S13	18	S7 and S12	US-PGPUB; USPAT	OR	OFF	2017/01/05 15:49

S14	12	("20040179339" | "3904934" | "20010000053" | "20050024963" | "6661690" | "20060220224" | "20040173894" | "5266912" | "6540525" | "6664617" | "20040225853" | "6864569").PN.	US-PGPUB; USPAT	OR	OFF	2017/01/05 15:52
S15	2	("6864569").URPN.	USPAT	OR	OFF	2017/01/05 15:56
S16	12	("5707242" | "5805596" | "5847985" | "5963464" | "6049467" | "6101089" | "6109929" | "6431879" | "6476476" | "6477593" | "6552914" | "6731514").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/01/05 15:56
S17	4851	(vertical$2 or stack$2) same (power adj1 densit$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2017/01/05 15:56
S18	1949	(vertical$2 or stack$2) with (power adj1 densit$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2017/01/05 15:57
S19	108	(vertical$2 or stack$2) with (power adj1 pressur$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2017/01/05 15:57
S20	316	shar$4 near3 (magnetic adj1 core)	US-PGPUB; USPAT; USOCR	OR	OFF	2017/01/05 16:18
S21	14	S20 same (vertical$2 or stack$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2017/01/05 16:18
S22	115	S20 and (vertical$2 or stack$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2017/01/05 16:19
S23	2	S20 and ((regulator$1 or converter$1) near4 (vertical$2 or stack$4))	US-PGPUB; USPAT; USOCR	OR	OFF	2017/01/05 16:20
S24	49	S20 same (regulator$1 or converter$1)	US-PGPUB; USPAT; USOCR	OR	OFF	2017/01/05 16:20
S25	11	S20 same (stage$1)	US-PGPUB; USPAT; USOCR	OR	OFF	2017/01/05 16:21
S26	18	("4437235" | "5191404" | "5323060" | "5726612" | "5910885" | "6051886" | "6313998" | "6333562" | "6472758" | "6531784").PN. OR ("6801440").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/01/05 16:26
S27	9	S12 same mold$4	US-PGPUB; USPAT	OR	OFF	2017/01/05 16:41
S28	45	S12 and mold$4	US-PGPUB; USPAT	OR	OFF	2017/01/05 16:41
S29	1167	(vertical$2 or stack$2) with (power near6	US-	OR	OFF	2017/01/09

		stage$1)	PGPUB; USPAT; USOCR			12:16
S30	3	(stack$4 with power with stage$1) same motherboard$1	US-PGPUB; USPAT	OR	OFF	2017/01/09 12:17
S31	166	(stack$4 with (power adj3 stage$1))	US-PGPUB; USPAT	OR	OFF	2017/01/09 12:19
S32	104	(stack$4 near6 (power adj3 stage$1))	US-PGPUB; USPAT	OR	OFF	2017/01/09 12:20

EAST Search History (Interference)

<This search history is empty>

1/9/2017 2:05:44 PM
C:\Users\pyanchus\Documents\EAST\Workspaces\14840063.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	14840063	ZENG ET AL.
	Examiner	Art Unit
	PAUL YANCHUS III	2116

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (see attached)	1/9/17	PBY
Inventor Name Search in PALM	1/9/17	PBY
NPL (Google)	1/9/17	PBY

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

PTO/SB/08a (03-15)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	14840063
Filing Date	2015-08-31
First Named Inventor	Jian-Hong ZENG
Art Unit	2115
Examiner Name	LEE, THOMAS C
Attorney Docket Number	TWT04064/US

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20080101025	A1	2008-05-01	HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P	
	2	20120173892	A1	2012-07-05	TONG SONG-LIN et al.	

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	1	2399684	GB	A	2004-09-22	SHUTTLE INC		
	2	M253836	TW	U	2004-12-21	VAC CORP		

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14840063
	Filing Date	2015-08-31
	First Named Inventor	Jian-Hong ZENG
	Art Unit	2115
	Examiner Name	LEE, THOMAS C
	Attorney Docket Number	TWT04064/US

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	14840063
	Filing Date	2015-08-31
	First Named Inventor	Jian-Hong ZENG
	Art Unit	2115
	Examiner Name	LEE, THOMAS C
	Attorney Docket Number	TWT04064/US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/James Lynn O'Sullivan/	Date (YYYY-MM-DD)	2016-07-19
Name/Print	James Lynn O'Sullivan	Registration Number	65618

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(12) UK Patent Application (19) GB (11) 2 399 684 (13) A

(43) Date of A Publication 22.09.2004

(21) Application No: 0306126.4

(22) Date of Filing: 18.03.2003

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United Kingdom

(51) INT CL[7]:
H05K 1/18

(52) UK CL (Edition W):
H1R RAC

(56) Documents Cited:
GB 2126013 A **US 4942550 A**

(58) Field of Search:
UK CL (Edition V) **H1R**
INT CL[7] **G06F, H05K**
Other: **ONLINE:WPI,PAJ,EPODOC**

(54) Abstract Title: **Layout for integrated motherboard**

(57) The layout for an integrated motherboard comprises placing a CPU 13 at the approximate centre of the motherboard 1, an input/output module 11 above the CPU, at least one PCI slot 12 on the left of the CPU, a power module 14 on the right of the CPU, a south bridge/north bridge chipset 15 below the CPU and a memory module 16 below the south bridge/north bridge chipset. The size of the motherboard is ideally 25.4 centimetres by 18.5 centimetres. Alternatively, the layout of the components can be reversed around the central vertical axis of the motherboard.

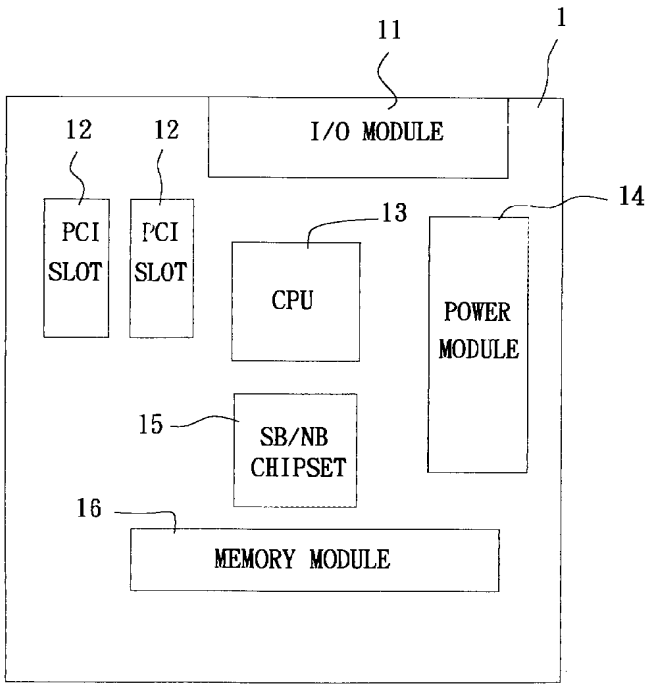


FIG. 1

GB 2 399 684 A

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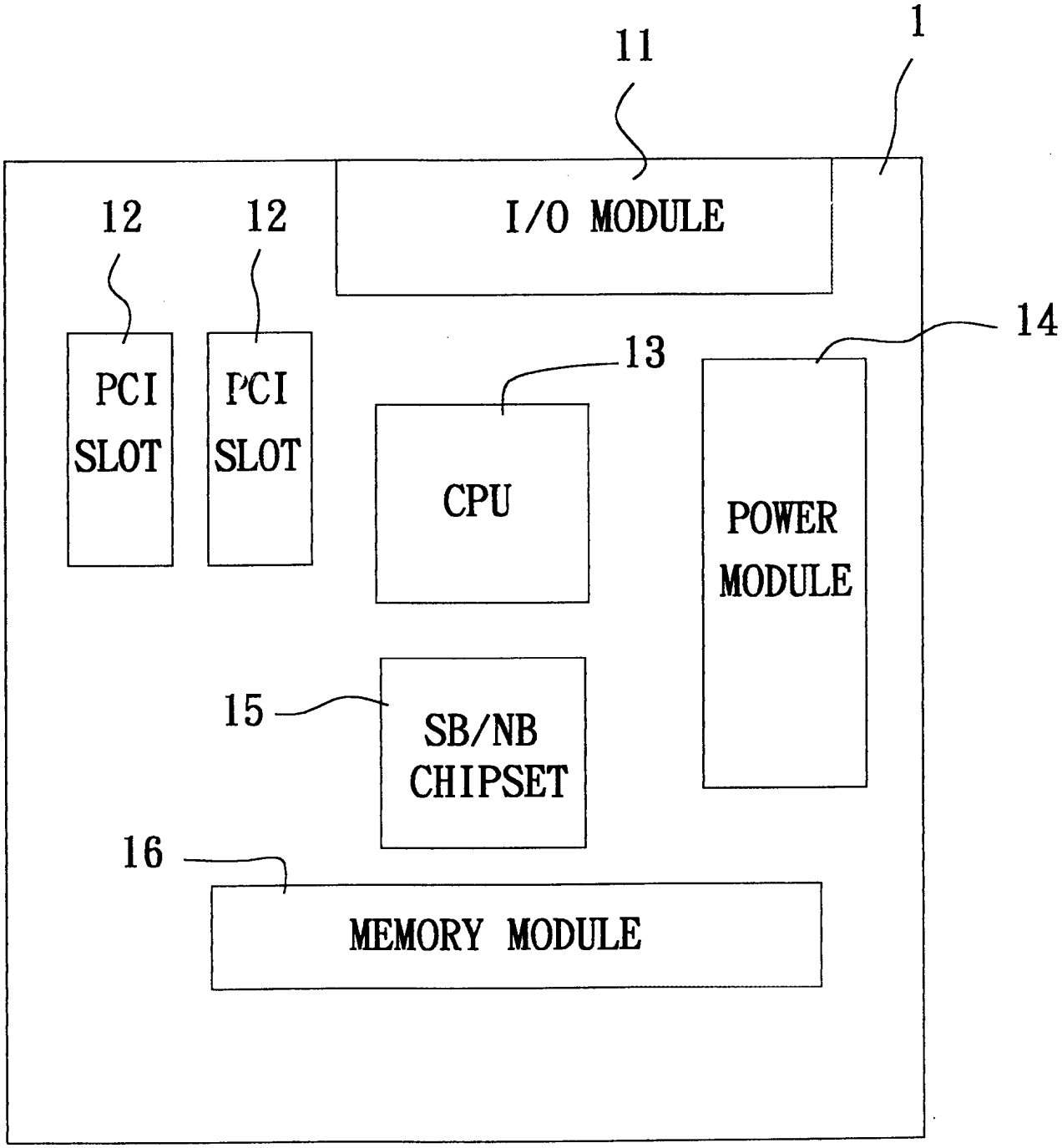


FIG. 1

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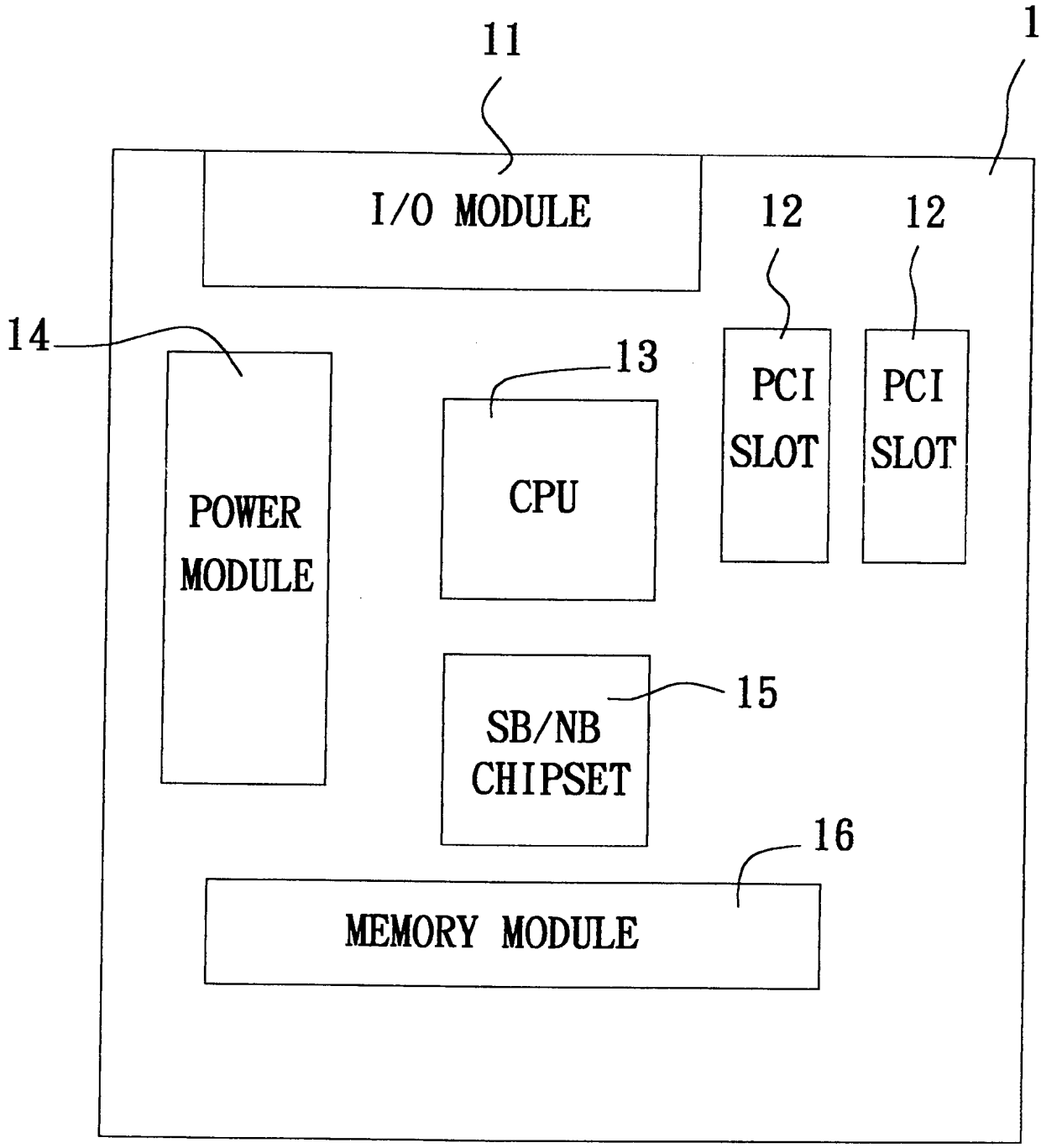


FIG. 2

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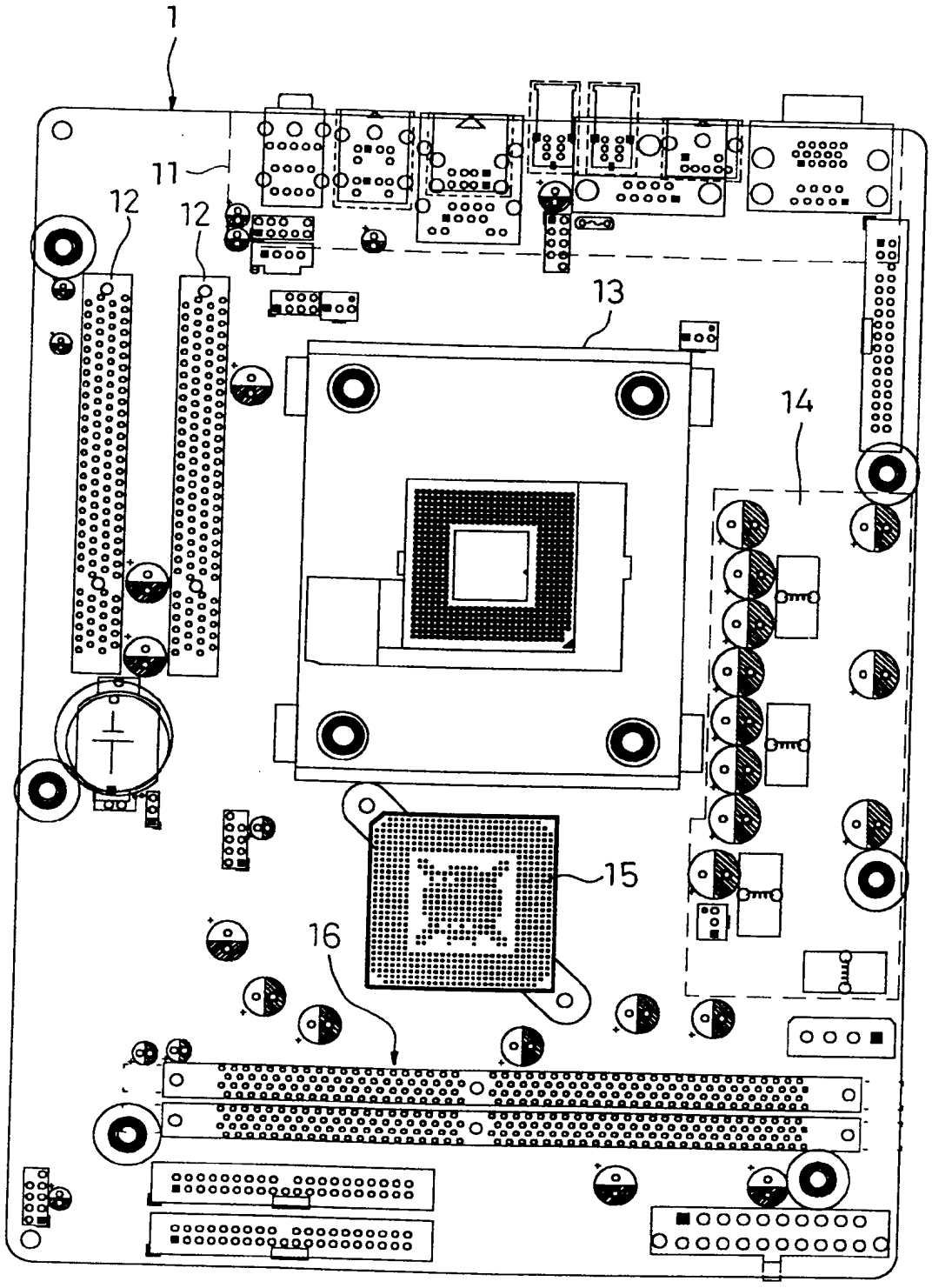


FIG. 3

PLACEMENT STRUCTURE OF AN INTEGRATED MOTHERBOARD

FIELD OF THE INVENTION

The present invention relates generally to a placement structure of an integrated motherboard. More particularly, the present invention relates to an integrated motherboard, wherein, a CPU is placed at the approximate center of the motherboard, and other peripheral components are placed around the CPU, so as to achieve an objective to optimum placement of the integrated motherboard.

BACKGROUND OF THE INVENTION

Recently, the process technology of Integrated Circuit (IC) has progressed rapidly. The function of the IC is more powerful but the size of the IC is smaller, thus makes increasing the peripheral components, such as LAN chip, MODEM chip, Graphic chip and surrounding audio chip being integrated into the motherboard. However, it is difficult that the motherboard designer could place the peripheral components and their respective connectors into the motherboard and could not increase the size of the motherboard. INTEL Corp. has designed a rule for designing P4 CPU and chipset on a motherboard, only if the motherboard designer following the designing rule, he (or she) could design a P4 motherboard correctly. However, the size of the integrated motherboard designed following the INTEL's rule couldn't meet the requirement of the market.

Therefore, it needs an integrated motherboard that the peripheral components and their respective connectors could place into the motherboard and would not increase the size of the motherboard.

SUMMARY OF THE INVENTION

To solve the above problems, it is an object of the present invention to provide

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a placement structure of an integrated motherboard, which integrates the peripheral components and their respective connectors into the motherboard and could not increase the size of the motherboard.

To accomplish the above object of the present invention, there is provided placement structure of an integrated motherboard, wherein a CPU is placed at the approximate center of the motherboard, a input/output module is placed above the CPU, at least one PCI slot is placed left the CPU, a power module is placed right the CPU, a south bridge/north bridge chipset is placed below the CPU, and a memory module is placed below the south bridge/north bridge chipset, so as to achieve an objective to optimum placement of the integrated motherboard.

The present invention also provides a placement structure of an integrated motherboard, wherein a CPU is placed at the approximate center of the motherboard, at least one PCI slot is placed right the CPU, a input/output module is placed above the CPU, a power module is placed left the CPU, a south bridge/north bridge chipset is placed below the CPU, and a memory module is placed below the south bridge/north bridge chipset, so as to achieve an objective to optimum placement of the integrated motherboard.

The novel features of the invention are set forth with particularity in the appended claims. The invention will be best understood from the following description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a block diagram of a placement structure of an integrated motherboard in accordance with one embodiment of the present invention.

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Fig. 2 shows a block diagram of a placement structure of an integrated motherboard in accordance with another embodiment of the present invention.

Fig. 3 shows a diagram of the main components of an integrated motherboard in accordance with one embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Fig. 1 shows a block diagram of a placement structure of an integrated motherboard in accordance with one embodiment of the present invention. As shown in Fig. 1, the placement structure of the integrated motherboard **1**, is characterized in: a CPU **13** is placed at the approximate center of the motherboard **1**, a input/output module **11** is placed above the CPU **13**; at least one PCI slot **12** is placed left the CPU **13**, a power module **14** is placed right the CPU **13**, a south bridge/north bridge chipset **15** is placed below the CPU **13**, and a memory module **16** is placed below the south bridge/north bridge chipset **15**, so as to achieve an objective to optimum placement of the integrated motherboard **1**. Wherein, the size of the motherboard **1** is 25.4 cm X 18.5 cm.

Wherein, the input/output module **11** further comprises such as a COM1, COM2, VGA, AV and S terminal, LAN, USB, or PS/2 connector or combination of them.

Referring to Fig. 2 shows a block diagram of a placement structure of an integrated motherboard in accordance with another embodiment of the present invention. As shown in Fig. 2, the placement structure of the integrated motherboard **1** of the present invention is characterized in: the CPU **13** is placed at the approximate center of the motherboard **1**, the input/output module **11** is placed above the CPU **13**; the power module **14** is placed left the CPU **13**; at least one PCI slot **12** is placed right the CPU **13**, the south bridge/north bridge chipset **15** is placed below the CPU **13**, and the memory module **16** is placed below the south bridge/north

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bridge chipset **15**, so as to achieve an objective to optimum placement of the integrated motherboard **1**. Wherein, the size of the motherboard **1** is also 25.4 cm X 18.5 cm.

Wherein, the input/output module **11** also further comprises such as a COM1, COM2, VGA, AV and S terminal, LAN, USB, or PS/2 connector or combination of them.

Referring to Fig. 3 shows a diagram of the main components of an integrated motherboard in accordance with one embodiment of the present invention. As shown in Fig. 3, the integrated motherboard **1** of the present invention comprises: the CPU **13** is placed at the approximate center of the motherboard **1**, the input/output module **11** is placed above the CPU **13**; at least one PCI slot **12** is placed left the CPU **13**, the power module **14** is placed right the CPU **13**, the south bridge/north bridge chipset **15** is placed below the CPU **13**, and the memory module **16** is placed below the south bridge/north bridge chipset **15**, so as to achieve an objective to optimum placement of the integrated motherboard **1**. Beside, the size of the motherboard **1** is 25.4 cm X 18.5 cm.

While the invention has been described with reference to a preferred embodiment thereof, it is to be understood that modifications or variations may be easily made without departing from the spirit of this invention, which is defined by the appended claims.

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WHAT IS CLAIMED IS:

1. A placement structure of an integrated motherboard, wherein a CPU is placed at the approximate center of the motherboard, a input/output module is placed above said CPU, at least one PCI slot is placed left said CPU, a power module is placed right said CPU, a south bridge/ north bridge chipset is placed below said CPU, and a memory module is placed below said south bridge/north bridge chipset, so as to achieve an objective to optimum placement of said integrated motherboard.

2. A placement structure of an integrated motherboard as claimed in claim 1, wherein the size of said motherboard is 25.4 cm X 18.5 cm.

3. A placement structure of an integrated motherboard, wherein a CPU is placed at the approximate center of said motherboard, at least one PCI slot is placed right said CPU, a input/output module is placed above said CPU, a power module is placed left said CPU, a south bridge/north bridge chipset is placed below said CPU, and a memory module is placed below said south bridge/north bridge chipset, so as to achieve an objective to optimum placement of said integrated motherboard.

4. A placement structure of an integrated motherboard as claimed in claim 3, wherein the size of said motherboard is 25.4 cm X 18.5 cm.

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Application No: GB 0306126.4 **Examiner:** Charles Jarman
Claims searched: 1-4 **Date of search:** 24 April 2003

Patents Act 1977 : Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance	
A	-	GB 2126013 A	(BOWTHORPE HOLDINGS PLC) See whole document.
A	-	US 4942550	(BURR-BROWN LTD) See whole documents.

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC[V]:

H1R

Worldwide search of patent documents classified in the following areas of the IPC[7]:

H05K, G06F

The following online and other databases have been used in the preparation of this search report:

WPI, PAJ, EPODOC

Espacenet

Bibliographic data: TWM253836 (U) — 2004-12-21

Motherboard for notebook computer

Inventor(s):	HUA JUNG-JENG [TW] ± (HUA, JUNG-JENG)
Applicant(s):	VAC CORP [TW] ± (VAC CORPORATION)
Classification:	**- international:** ***G06F15/02;*** (IPC1-7): G06F15/02 **- cooperative:**
Application number:	TW20040203391U 20040308
Priority number(s):	TW20040203391U 20040308

Abstract not available for TWM253836 (U)

English abstract of TW M253836 U

One kind of motherboard-based notebook computer provided within the framework of notebook computers, which accounted for half of the frame of the motherboard, and the other half of the frame is provided with a battery, a CD-ROM drive, and a thermal module located at the top of the frame edge in the middle. The system board includes a plate having a top surface and a bottom surface. A central processing system provided on the top surface of the plate; a memory system provided on the top surface of the peripheral portion of and adjacent to the central processor; a plurality of external line slots arranged side by side on the top surface of the plate on the edge ; a plurality of connector lines to be placed in the back of the plate; and South Bridges chip is provided on the rear panel of the body; whereby the external slot exposed to different notebooks of different sides.

公告本

申請日期：93 03 08	IPC分類
申請案號：93203391	G06F 15/02

（以上各欄由本局填註）

新型專利說明書 M253836

一、新型名稱	中 文	筆記型電腦之主機板
	英 文	
二、創作人（共1人）	姓 名（中文）	1. 花仲正
	姓 名（英文）	1.
	國 籍（中英文）	1. 中華民國 TW
	住居所（中 文）	1. 台北市信義區信義路4段456號20樓
	住居所（英 文）	1.
三、申請人（共1人）	名稱或姓 名（中文）	1. 精鍊科技股份有限公司
	名稱或姓 名（英文）	1.
	國 籍（中英文）	1. 中華民國 TW
	住居所（營業所）（中 文）	1. 台北市信義區信義路4段456號20樓 （本地址與前向貴局申請者相同）
	住居所（營業所）（英 文）	1.
	代表人（中文）	1. 蔡其建
	代表人（英文）	1.

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一、本案已向

國家(地區)申請專利	申請日期	案號	主張專利法第一百零五條準用第二十四條第一項優先權
無			

二、□主張專利法第一百零五條準用第二十五條之一第一項優先權:

申請案號:

無

日期:

三、主張本案係符合專利法第九十八條第一項□第一款但書或□第二款但書規定之期間

日期:

四、中文創作摘要　（創作名稱：筆記型電腦之主機板）

一種筆記型電腦之主機板係設置於筆記型電腦之框架內，該主機板佔該框架之半邊，該框架之另一半邊設有一電池、一光碟機、及一散熱模組設於框架之頂緣中間。該主機板包括有一板體係具有一頂面及一底面。一中央處理器係設於該板體之頂面；一記憶體係設於該週邊部之頂面且鄰該中央處理器；複數個外接插槽係併排地設置於該板體頂面的上緣；複數個連接器係設於該板體之背面；及南、北橋晶片係設於板體之背面；藉此該外接插槽可外露於不同筆記型電腦之不同側邊。

五、英文創作摘要　（創作名稱：）

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六、指定代表圖

（一）、本案代表圖為：第二圖

（二）、本案代表圖之元件代表符號簡單說明：

主機板	5	板體	50
隨機存取記憶體	510	中央處理器	511
唯讀記憶體	512	電源插座	513
北橋晶片	515	南橋晶片	517
外接插槽	53	連接器	54、55

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四、創作說明（1）

【新型所屬之技術領域】

本創作係有關一種筆記型電腦之主機板，特別指一種組裝於筆記型電腦中之主機板，具有一種佈局設計，而可以旋轉至不同方位以置於不同筆記型電腦上。

【先前技術】

有句名言說「科技來自人的需求」，因此新一代筆記型電腦不僅要在行動運算技術的效能上再次提升，也要在使用上以更彈性運用的擴充性來滿足消費者對迅馳奔騰的期待與需求，進一步提供消費者更高品味的移動生活。

其中筆記型電腦給予消費者的購買要因，除了內在配備的性能外，還有外表外觀之吸引力，因此廠商為著抓住消費者，莫不花盡心力一面著力於配備的升級，另一面且持續設計新穎的外觀，以滿足消費者這兩方面的需求。然而，廠商要同時滿足上述兩種要求並非小事，在外觀設計的同時，又要更新內部的零件，往往是牽一髮而動全身，影響筆記型電腦整體的設計。往往為了推出一款配備不同、外觀新穎的筆記型電腦，幾乎是常常需要全新設計整塊主機板。

筆記型電腦的廠商在組裝不同規格以滿足各種消費者需求時，最大的限制就是主機板無法共用在不同之筆記型電腦上，由於受限於整體零件的設計擺設，常常在外表上無法作太大變動的設計，並不具有太大變化，如此一來，即使內在配備雖然已經升級，外在卻仍缺少新穎的設計，

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四、創作說明 (2)

無法滿足消費者喜歡新奇而與眾不同之購買特性。

是以，由上可知，上述習知的筆記型電腦在內部整體設計上，對於產品的更新設計顯然具有不便與缺失存在，而可待加以改善者。

緣是，本創作人有感上述缺失之可改善，乃特潛心研究並配合學理之運用，終於提出一種設計合理且有效改善上述缺失之本創作。

【新型內容】

本創作之主要目的係提供一種筆記型電腦之主機板，其中該主機板係具有一種佈局設計，而可供旋轉至不同的方位而設置於不同筆記型電腦之框架內，藉著交錯配置不同之等級主機板與不同筆記型電腦之框架，以設計數種不同規格筆記型電腦。

為達上述之目的，本創作之一種筆記型電腦之主機板，係設置於筆記型電腦之框架內，該主機板佔該框架之一半面積，該框架之另一半面積設有一電池、一光碟機及一散熱模組，該主機板包括有一板體，該板體設有一缺口且具有一頂面及一底面；該板體的頂面具有隨機存取記憶體係大體位於該板體中間、中央處理器係設於該板體邊緣、唯讀記憶體、電源插座係鄰近該中央處理器、硬碟可拆換地設置於該板體、複數個外接插槽設於該板體的上緣且朝向該框架之側邊、及複數個連接器；該板體的背面包括有北橋晶片係鄰近該缺口、南橋晶片設置於該硬碟的背

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四、創作說明（3）

面、及複數個連接器大體分佈於該板體中間；藉此該外接插槽係可外露於不同筆記型電腦之不同側邊。

茲配合圖式將本創作之較佳實施例詳細說明如下，但是此等說明僅係用來說明本創作，而非對本創作的權利範圍作任何的限制。

【實施方式】

請參閱第一圖，為本創作之筆記型電腦之仰視立體分解圖。該筆記型電腦１具有一顯示面板２及一主機３。該主機３係包括有上、下殼體３１、３２及一金屬材質的框架３４係設於該上、下殼體３１、３２之間。該顯示面板２係樞接於該框架３４的一側。

該框架３４乃用以容納筆記型電腦之各種電子零件，至少包括一主機板５、一散熱模組３５以逸散該主機板５所產生之熱量、一光碟機３６以存取資料，例如ＶＣＤ或ＤＶＤ，及一電池３７以提供筆記型電腦電力。該框架３４乃略呈一長方矩形。該主機板５佔該框架３４之一半面積，該框架３４之另一半面積供該電池３７、該光碟機３６及該散熱模組３５擺設。

本創作乃重新考量設計該主機板５的輪廓及其擺設，以使該主機板５可旋轉至不同方位而設置於不同筆記型電腦之框架內，藉此該筆記型電腦可具有各種不同之外觀，而有利於設計。該主機板５包括有一板體５０係具有一頂面５０２以及一底面５０４、複數個電子零件係設置於該

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四、創作說明（4）

板體５０上、及電路係形成於該板體５０上。該板體５０乃略呈長方形，並且形成一矩形之缺口５０８，該缺口５０８有利於節省該主機板５所佔的空間。

請參閱第二圖，係為本創作之主機板的仰視圖。該主機板５之設計乃以桌上型電腦觀念為出發點，將各種必要的電子零件儘量以可替換之方式組裝設置於該板體５０上。該主機板５之頂面５０２包括有隨機存取記憶體（RAM, random-access memory）５１０、中央處理器５１１、唯讀記憶體(ROM, read-only memory)５１２、電源插座５１３可連接AC變壓器之插頭、硬碟５１４、複數個外接插槽５３、及複數個連接器５５。

該中央處理器５１１乃設於主機板５之邊緣而方便該散熱模組３５之配置。該隨機存取記憶體５１０乃大體位於該主機板５的中間，該硬碟５１４乃鄰近該主機板５之下緣並且以可拆換的方式插設於該主機板５上。該複數個外接插槽５３係併排地設置於該主機板５之上緣，以供與外界之週邊設備電性連接。本實施例中該外接插槽５３包括有一個VGA埠５３１、一個1394接頭５３２、一個RJ-45數據機接頭５３３、一個RJ-11乙太網路接頭５３４、二個ＵＳＢ埠５３５、５３６、一個麥克風接頭５３７、及一個耳機接頭５３８。該複數個連接器５５包括有一風扇連接器５５１、電池連接器５５２、光碟機連接器５５３、及無線模組插座５５４乃設於該主機板５之邊緣。

該主機板５之該板體５０的頂面５０２進一步可以包

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四、創作說明（5）

括有一無線模組５１６、一數據機模組（Modem）５１８。該無線模組５１６乃以鎖固方式設置鄰近於該板體５０之邊緣，以利於無線通訊之收發。

請參閱第三圖，係本創作中該主機板背面之俯視圖。該主機板5的背面５０４包括有北橋晶片５１５、南橋晶片(South Bridge)５１７、及複數個連接器５４。該北橋晶片５１５乃鄰近該缺口５０８，其主要角度的工作是聯繫ＲＡＭ記憶體５１０、中央處理器５１１、還有顯示卡等高速周邊，而大體位於該中央處理器５１１及該ＲＡＭ５１０的背面。其中該南橋晶片５１７，其主要角色乃作為控制連接硬碟５１４、光碟等儲存設備的連接界面及界面卡插槽等低速周邊，而設置於該硬碟５１４的背面。該複數個連接器５４係大體分佈於該主機板５之中間部位以供各種電子零件電性連接，本較佳實施例中乃包括有鍵盤連接器５４１、指示燈連接器５４２、麥克風連接器５４３、揚聲器(speaker)連接器５４４、LVDS（Low Voltage Differential Signal，低電壓差動信號）接頭５４５、以及控制基板連接器５４６、變壓整流器(inverter)５４７、觸控板連接器５４８、及讀卡機連接器５４９。藉著上述之該複數個連接器５４之配置，由於大體設置於主機板５之背面５０４中間部位，且外露於該框架３４之中間開口（如第一圖所示），藉此電子零件的排線與主機板５非常容易檢視並拆離，有利於維修。

請參閱第三Ａ圖，係本創作中該主機板之側視圖。該

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四、創作說明（6）

主機板５之該複數外接插槽５３乃外露於其較長的側邊，當該主機板５旋轉設置時，該外接插槽５３也旋轉至不同的方向。該主機板５乃非常輕巧，由圖可看出該主機板５之寬度略等於該外接插槽５３的寬度，加上該中央處理器５１１的寬度總和。本實施例中該主機板５之長側邊為230mm，其短側邊為155mm。該缺口５０８則為60mm X 40mm。

請參閱第四圖，為本創作之主機板組裝於一種框架的組合仰視圖（拆下該下殼體３２）。整體觀之本創作之該主機板５與該筆記型電腦１的該框架３４的比例上，該主機板５約佔該框架３４之一半邊，該框架３４之另一半邊設有該電池３７、該光碟機３６、及該散熱模組３５設於框架３４之頂緣。該主機板５長側邊仍略短於該框架３４短側邊，該主機板５短側邊約為該框架３４長側邊一半，因而該主機板５可於該框架３４轉至另一方向擺設。

請參閱第五圖，為本創作之主機板組裝於另一種框架的組合仰視圖（拆下該下殼體３２）。由於上述之比例及本創作之主機板５的佈局設計，該主機板５乃可以同一種的佈局設計而旋轉至另一方位，以放置於不同之框架３４a上。其中該主機板５之外接插槽５３在本實施例之框架３４a乃位於筆記型電腦的側邊，即圖中的右側，可產生明顯外觀之差別。因此本創作之同一種的主機板５能適用於不同之筆記型電腦，能有效降低主機板之庫存壓力，也有利於廠商減少重新研發時的人力和成本，只要著力於外

四、創作說明（7）

觀的研發。

本創作之主機板乃極有利於創作不同外觀及配備之筆記型電腦，試想，只要就本創作之主機板而稍作更改不同之中央處理器及其他配備，如不同廠牌中央處理器，即具有至少三種不同等級之主機板；再加上，本創作提供之橫向、直向的兩種框架，即配搭六種不同配備及外觀之筆記型電腦。更何況，本創作之主機板5可配合第三種框架，使該外接插槽53可轉至筆記型電腦右側，三種框架配上三種不同等級之主機板，乃可產生九種不同配備及外觀之筆記型電腦。

〔創作優點及特點〕

因此藉本創作所能產生之特點及功能經整理如后：

該主機板5係可以旋轉至另一方位以置於不同之框架上，如此該主機板5之外接插槽53乃可置於不同筆記型電腦之不同側邊上，造就最明顯的外觀上之差異，極其有利於通路商之研發，擁有明顯的差異性及變化性，不用重新設計主機板，也能降低庫存的壓力及風險。

該主機板5係可旋轉至不同方位而設置於不同筆記型電腦之框架內，因此藉著不同之等級主機板與不同筆記型電腦之框架的交錯配置，即可容易地具有數種不同規格之筆記型電腦供消費者選擇。

筆記型電腦之廠商可一口氣推出多款新型筆記型電腦並配備多規格支援升級能力，良好之擴充功能，對於消費者充滿具大的吸引力。

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四、創作說明（8）

綜上所述，本創作實已符合新型專利之要件，依法提出申請。惟以上所揭露者，僅為本創作較佳實施例而已，自不能以此限定本創作之權利範圍，因此依本創作申請範圍所做之均等變化或修飾，仍屬本創作所涵蓋之範圍。尚請審查委員撥冗細審，並盼早日准予專利以勵創作，實感德便。



圖式簡單說明

第一圖：係本創作之筆記型電腦之仰視立體分解圖。

第二圖：係為本創作之主機板的仰視圖。

第三圖：係為本創作之主機板的俯視圖。

第三A圖：係為本創作之主機板的側視圖。

第四圖：係為本創作之主機板組裝於一種框架的組合仰視圖。

第五圖：係為本創作之主機板組裝於另一種框架的組合仰視圖。

【圖式中之參照號數】

〔本創作〕

筆記型電腦 1			
顯示面板 2			
主機 3			
上殼體	31	下殼體	32
框架	34、34a	散熱模組	35
光碟機	36	電池	37
主機板 5			
板體	50	頂面	502
底面	504	缺口	508
隨機存取記憶體	510	中央處理器	511
唯讀記憶體	512	電源插座	513
硬碟	514	無線模組	516
北橋晶片	515	南橋晶片	517

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圖式簡單說明

數據機模組　518

外接插槽　53

VGA埠　531　　1394接頭　532

RJ-45數據機接頭533

RJ-11乙太網路接頭534

USB埠　535、536

麥克風接頭　537　　耳機接頭　538

連接器　54

鍵盤連接器　541　　指示燈連接器542

麥克風連接器543　　揚聲器連接器544

LVDS接頭　545　　控制基板連接器546

變壓整流器　547　　觸控板連接器548

讀卡機連接器549

連接器　55

風扇連接器　551　　電池連接器　552

光碟機連接器553　　無線模組插座554

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五、申請專利範圍

1、一種筆記型電腦之主機板，係設置於筆記型電腦之框架內，該主機板佔該框架之一半面積，該框架之另一半面積設有一電池、一光碟機及一散熱模組，該主機板包括有：

一板體，該板體設有一缺口且具有一頂面及一底面；

該板體的頂面具有隨機存取記憶體係大體位於該板體中間、中央處理器係設於該板體邊緣、唯讀記憶體、電源插座係鄰近該中央處理器、硬碟可拆換地設置於該板體、複數個外接插槽設於該板體的上緣且朝向該框架之側邊、及複數個連接器；

該板體的背面包括有北橋晶片係鄰近該缺口、南橋晶片設置於該硬碟的背面、及複數個連接器大體分佈於該板體中間；藉此

該外接插槽係可外露於不同筆記型電腦之不同側邊。

2、如申請專利範圍第1項所述之筆記型電腦之主機板，其中該外接插槽包括有一個VGA埠、一個1394接頭、一個RJ-45數據機接頭、一個RJ-11乙太網路接頭、二個USB埠、一個麥克風接頭、及一個耳機接頭。

3、如申請專利範圍第2項所述之筆記型電腦之主機板，其中該主機板之寬度略等於該外接插槽的寬度，加上該中央處理器的寬度總和。

4、如申請專利範圍第1項所述之筆記型電腦之主機板，其中該板體頂面的連接器包括有一風扇連接器、電池連接器、光碟機連接器、及無線模組插座乃設於該主機板

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五、申請專利範圍

之邊緣。

5、如申請專利範圍第1項所述之筆記型電腦之主機板，其中該板體之頂面進一步可以包括有一無線模組乃設置鄰近於該板體之邊緣。

6、如申請專利範圍第5項所述之筆記型電腦之主機板，其中該板體之頂面進一步可以包括有一數據機模組乃鄰近該無線模組。

7、如申請專利範圍第1項所述之筆記型電腦之主機板，其中該板體背面的連接器包括有包括有鍵盤連接器、指示燈連接器、麥克風連接器、揚聲器連接器、LVDS接頭、以及面板電源連接器、變壓整流器、觸控板連接器、及讀卡機連接器。

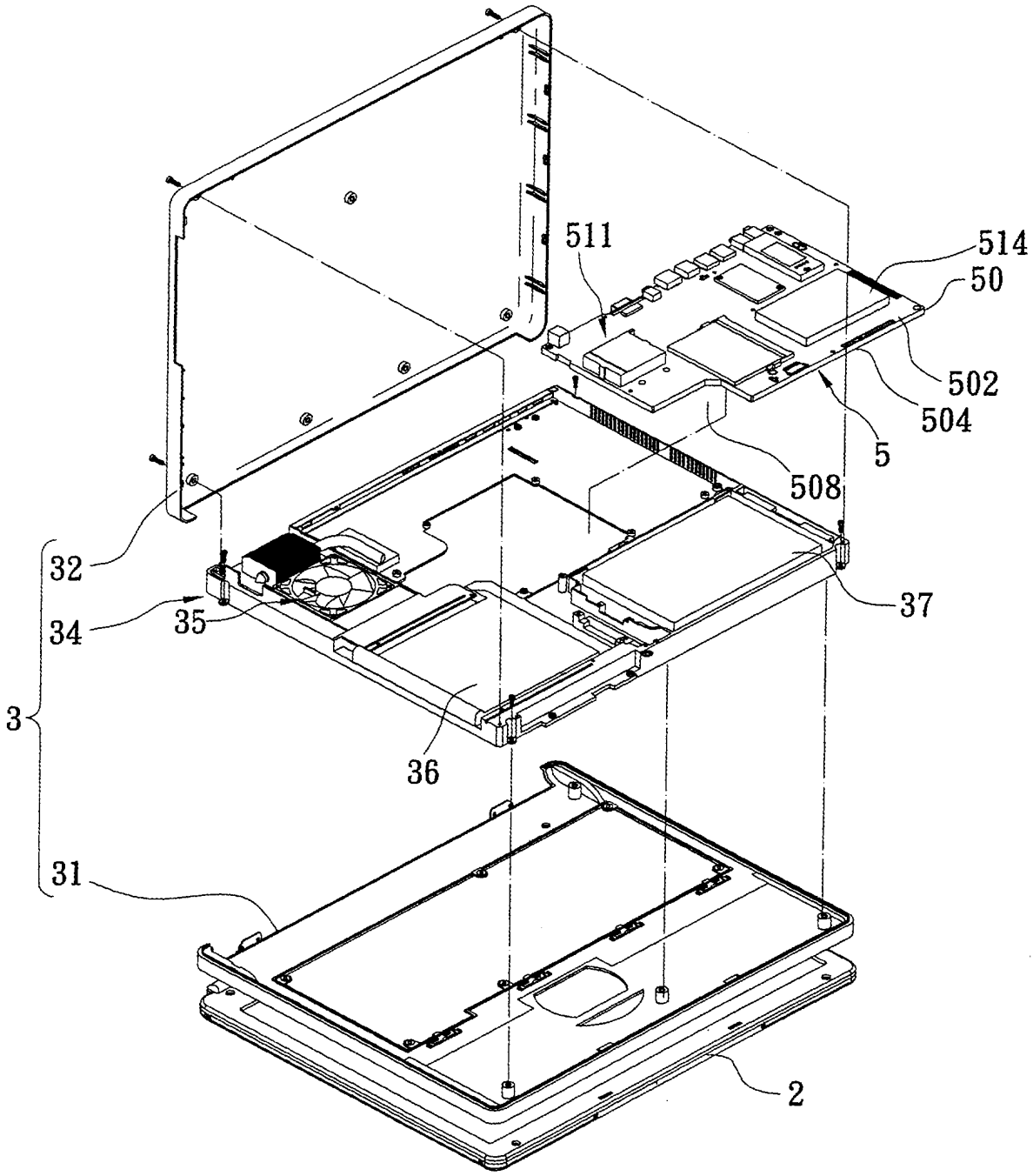
8、如申請專利範圍第1項所述之筆記型電腦之主機板，其中該主機板長側邊略短於該筆記型電腦之短側邊。

9、如申請專利範圍第1項所述之筆記型電腦之主機板，其中該主機板之短側邊約為該框架之長側邊之一半。

10、如申請專利範圍第1項所述之筆記型電腦之主機板，其中該主機板長側邊為230mm，短側邊為155mm。

11、如申請專利範圍第1項所述之筆記型電腦之主機板，其中該缺口則為60mm X 40mm。

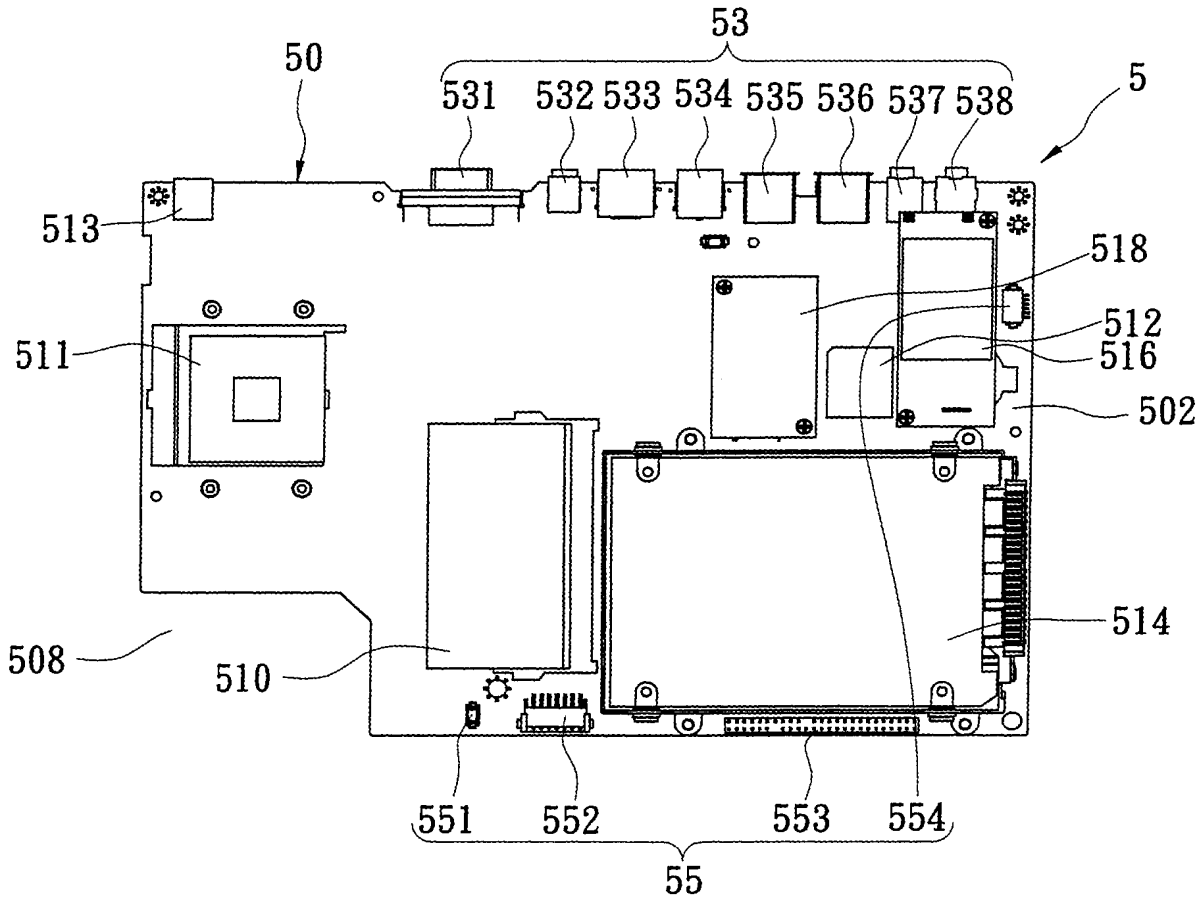
圖式



第一圖

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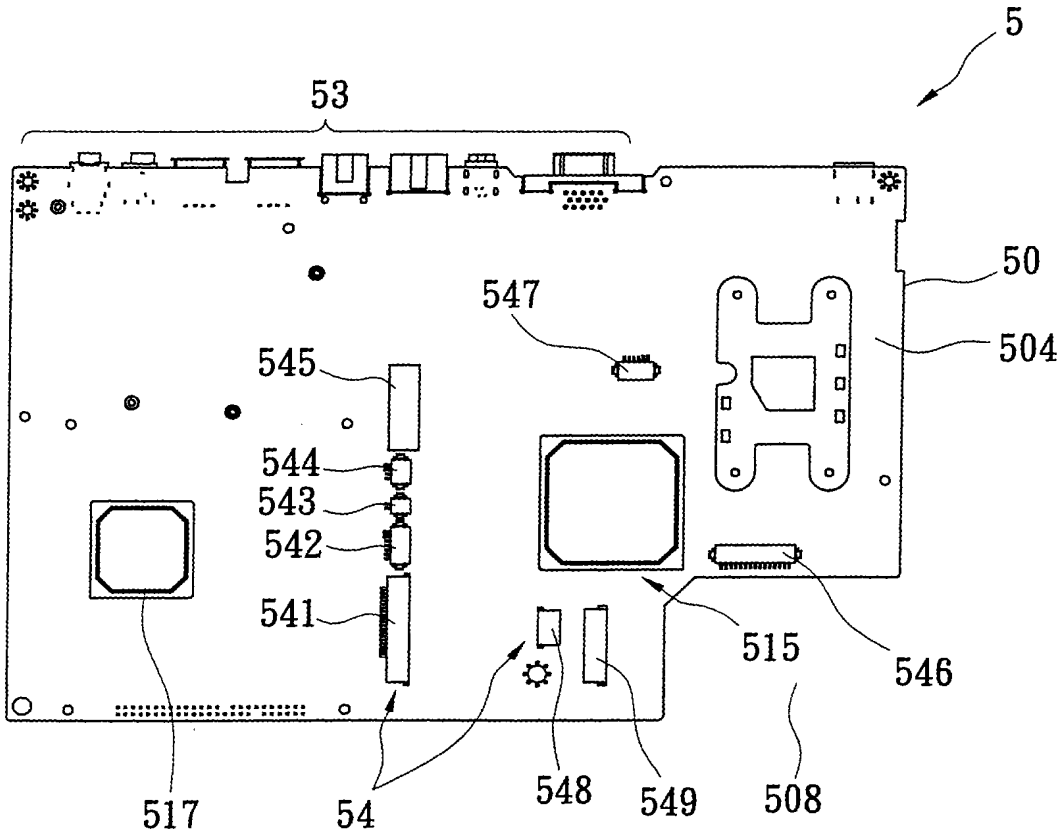
圖式



第二圖

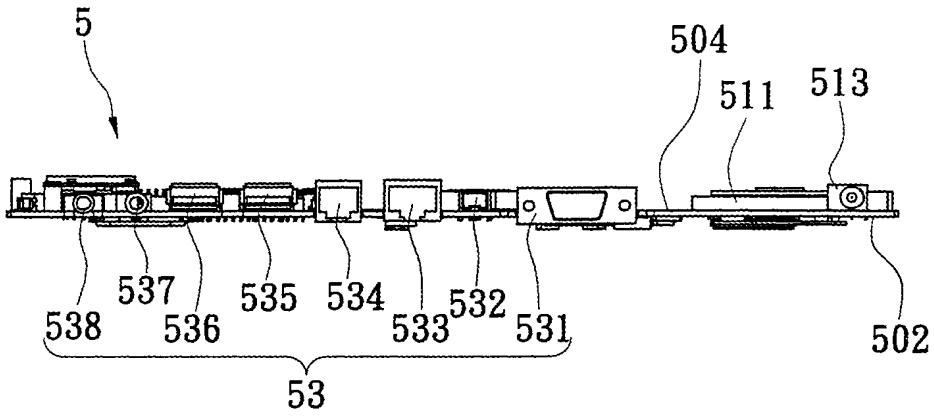
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圖式



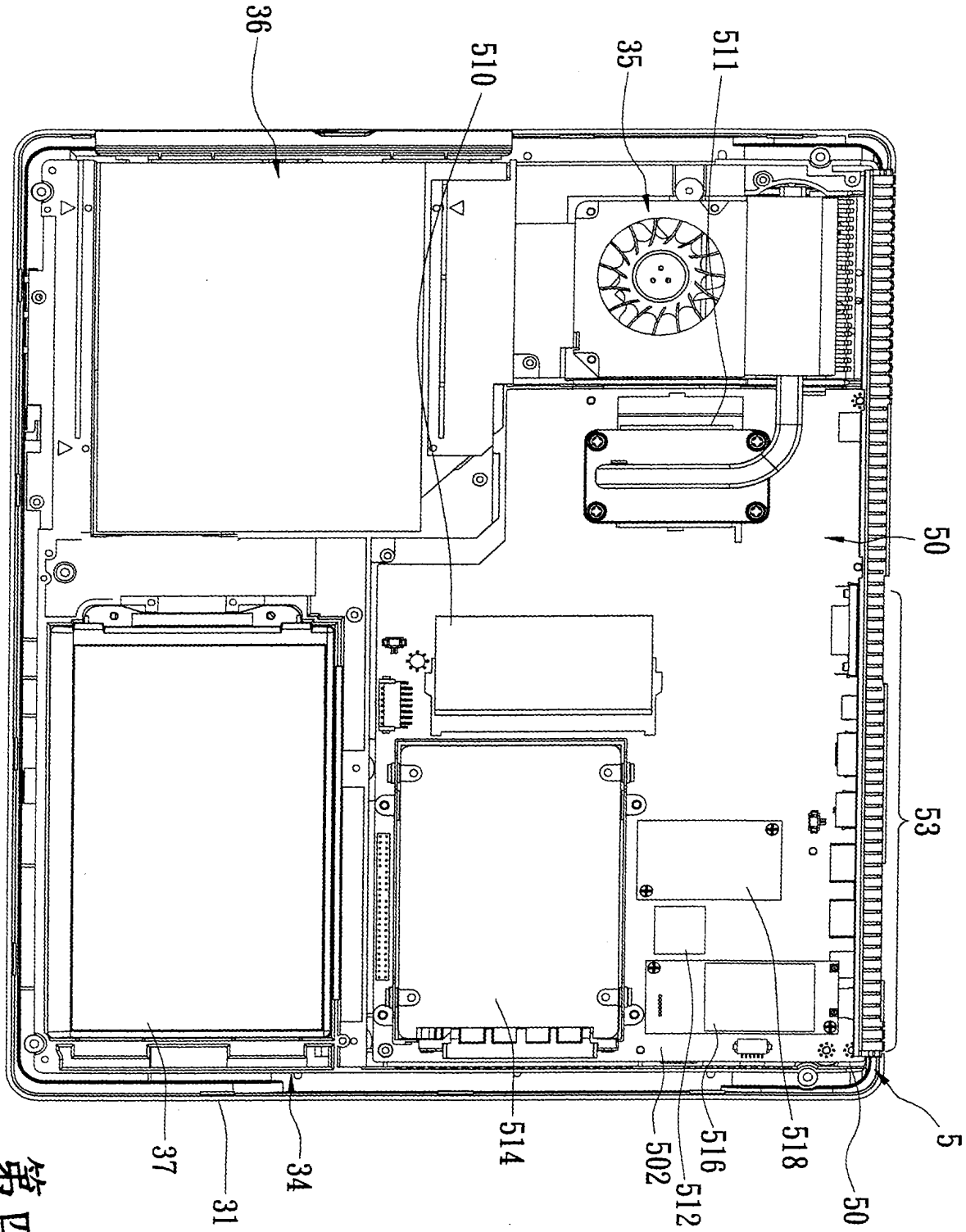
第三圖

圖式



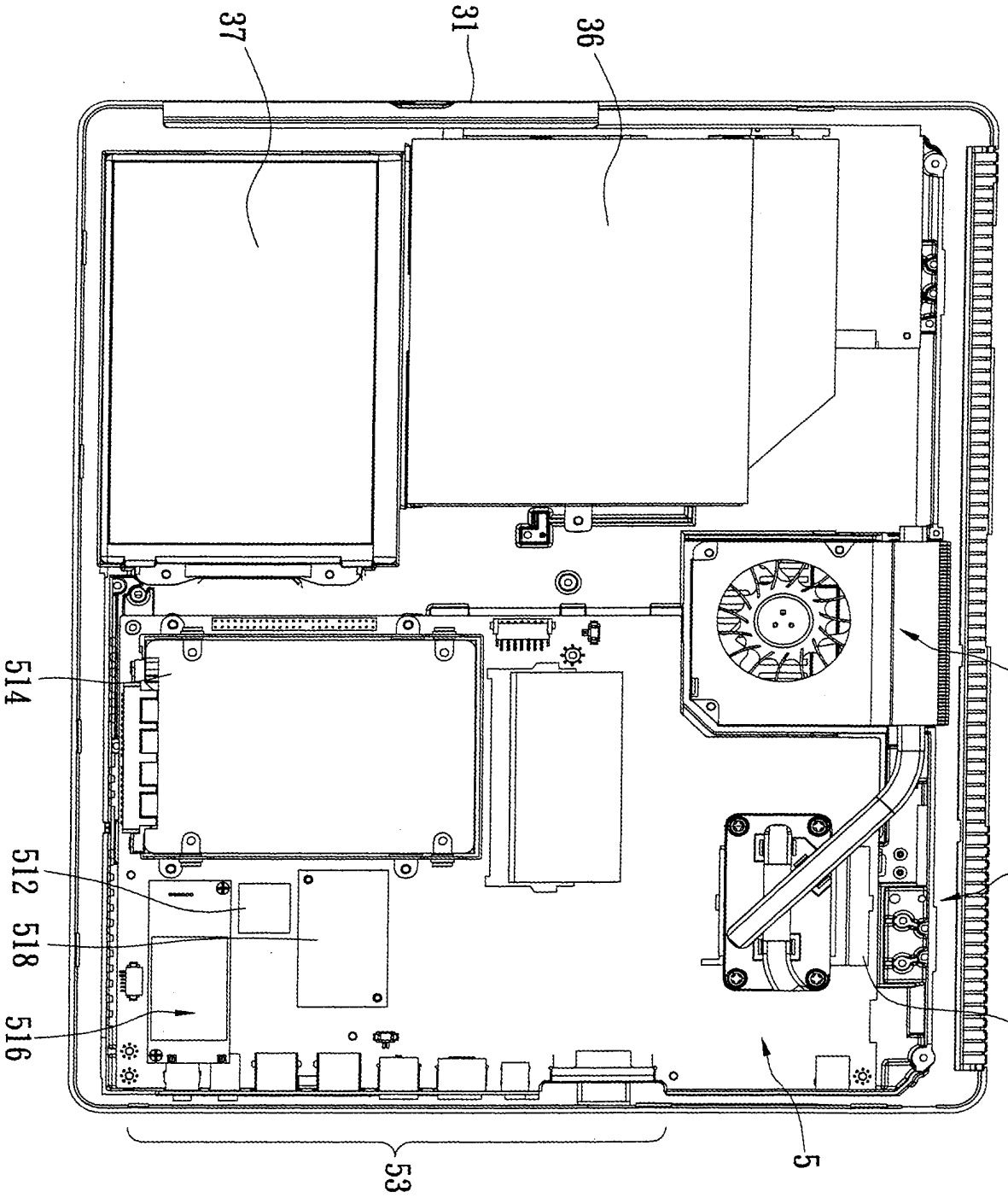
第三A圖

圖式



第四圖

圖式



第五圖

Electronic Acknowledgement Receipt

EFS ID:	26383335
Application Number:	14840063
International Application Number:	
Confirmation Number:	8903
Title of Invention:	POWER SUPPLY APPARATUS
First Named Inventor/Applicant Name:	Jian-Hong ZENG
Customer Number:	60589
Filer:	James Lynn O'Sullivan
Filer Authorized By:	
Attorney Docket Number:	TWT04064/US
Receipt Date:	18-JUL-2016
Filing Date:	31-AUG-2015
Time Stamp:	23:52:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	TWT04064US-IDSLetter-20160719.pdf	423932 cf30f09a46ebd1680b7da244b68c5715db23d197	no	3

Warnings:

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Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	TWT04064US-IDSForm-20160719.pdf	1035074 823d64e867211fb22f21b0c61f7976063f420fb1	no	4
Warnings:					
Information:					
3	Foreign Reference	GB2399684A.pdf	902157 20edf85883d5bd59cb70708928b53a60e1756ccb	no	10
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Information:					
4	Foreign Reference	TWM253836U.pdf	4196420 73f71fc009a871a0d18d8d96b5b39bbe24717220	no	24
Warnings:					
Information:					
			Total Files Size (in bytes):	6557583	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of：Jian-Hong ZENG	Confirmation No.：8903
Serial No.14/840,063	Group Art Unit：2115
Filed：August 31, 2015	Examiner：LEE, THOMAS C
	Docket No. TWT04064/US

For：POWER SUPPLY APPARATUS

INFORMATION DISCLOSURE STATEMENT

U.S. PATENT AND TRADEMARK OFFICE
Commissioner for Patents
P.O.BOX 1450
ALEXANDRIA, VA 22313-1450,
U.S.A.

Dear Sir,

This information disclosure statement is filed in accordance with 37 C.F.R.§§1.56, 1.97, and 1.98, and specifically：

☒ under 37 CFR 1.97(b), or
(with Three months of filing national application；or date of entry of international application；or before mailing date of first office action on the merits；or before the mailing of a first office action after the filing of a request for continued examination under §1.114；whichever occur last)

☐ under 37 CFR 1.97(c) together with either a：
- ☐ Statement Under 37 C.F.R.1.97(e), or
- ☐ a fee under 37 CFR 1.17(p), or

(After the CFR 1.97(b) time period, but before the final office action or notice of allowance, whichever occurs first)

☐ under 37 CFR1.97(d) together with a：
- ☐ Statement Under 37 C.F.R.1.97(e), and

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☐ a petition fee set forth in 37 CFR 1.17(p).

(Filed after final office action or notice of allowance, whichever occurs first, but before payment of the issue fee)

☒ At any time during the pendency of this application, please charge any fees required to Deposit Account pursuant to 37 CFR 1.25. The Commissioner is hereby requested to credit any overpayment to Deposit Account No. 504669.

☒ Applicant(s) submit herewith Form PTO SB/08A-08B-08a – Information Disclosure Statement by Applicant together with copies (where required) of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may or may not be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56. As required by 37 C.F.R. §1.98(a), a legible copy of each document is provided.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Forms SB/08A-08B-08a, as presently understood by the individual(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed in the form PTO SB/08A-08B-08a and is enclosed herewith.

The following rights are reserved by the Applicant(s)：the right to establish the patentability of the claimed invention over any of the listed document should they be applied as reference, and/or the right to prove that some of these documents may not be prior art, and/or the right to prove that some of these documents may not be enabling for the teachings they purport to offer.

This statement should not be construed as a representation that an exhaustive search has been made, or that information more material to the examination of the present application does not exist. Any statements or identifications regarding the relevance of any portion(s) of cited references should not be construed as a representation that the most relevant portion(s) have been identified, and the absence of such statements or identifications should not be construed as representations that there are no relevant portion(s). The Examiner is specifically requested not to rely solely on the materials submitted herewith. The Examiner is requested to conduct an

independent and thorough review of the documents, and to form independent opinion as to their significance.

It is requested that the information disclosed herein be made of record in this application and that the Examiner initial and return a copy of the enclosed PTO SB/08A-08B-08a to indicate the documents have been considered.

Respectfully submitted,

/James Lynn O'Sullivan /

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Agent for Applicant(s)

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中华人民共和国国家知识产权局
STATE INTELLECTUAL PROPERTY OFFICE
OF THE PEOPLE'S REPUBLIC OF CHINA

证　明

本证明之附件是向本局提交的下列专利申请文件副本。

申　　请　　号：201410442972.6

申　请　类　型：发明专利

发明 创造 名称：电源装置

申　　请　　日：2014 年 09 月 02 日

申　　请　　人：台达电子工业股份有限公司

发明人或设计人：曾剑鸿、言超、忽培青

局长

申长雨

2016 年 03 月 25 日

2014104429726

权 利 要 求 书 TWLB4955-14P1

1. 一种电源装置，其特征在于，包括：

控制单元与功率单元，堆叠设置且毗邻负载的位置，所述功率单元至少含一功率半导体器件，所述控制单元至少含一具备控制或者驱动能力的芯片；以及

引脚，电性连接所述控制单元和所述功率单元；所述控制单元用于控制所述功率单元，使所述功率单元供电给毗邻的所述负载。

2. 根据权利要求 1 所述的电源装置，其特征在于，所述控制单元与所述功率单元，堆叠设置设于主板上，所述主板还设有所述负载。

3. 根据权利要求 1 所述的电源装置，其特征在于，还包括：焊盘，分布于所述功率单元的侧面和所述控制单元的侧面，与所述引脚电性连接。

4.根据权利要求 3 所述的电源装置，其特征在于，所述引脚包括表面贴装引脚，分布于所述功率单元和所述控制单元的外表面并与所述焊盘电性连接。

5.根据权利要求 3 所述的电源装置，其特征在于，所述表面贴装引脚覆盖所述功率单元 30%以上外表面积。

6.根据权利要求 3 所述的电源装置，其特征在于，所述引脚还包括直插引脚，所述直插引脚配合所述表面贴装引脚实现所述功率单元/所述控制单元与所述主板的电性连接。

7.根据权利要求 3 所述的电源装置，其特征在于，所述焊盘还分布于所述功率单元与焊盘所在侧面垂直的面。

8.根据权利要求 3 所述的电源装置，其特征在于，所述功率单元包括主功率单元部分和次功率单元部分，所述主功率单元部分的侧面分布所述焊盘，所

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述次功率单元部分堆叠于所述主功率单元部分。

9.根据权利要求 1 所述的电源装置，其特征在于，所述功率单元与所述负载位于主板的同一面，所述控制单元位于主板与所述功率单元相对的另一面。

10. 根据权利要求 1 所述的电源装置，其特征在于，所述电源装置还包括一功率单元，所述两功率单元和所述控制单元相互之间堆叠设于主板，所述控制单元通过所述引脚控制所述两功率单元。

11. 根据权利要求 10 所述的电源装置，其特征在于，所述两功率单元分别为一第一级直流对直流变换器的功率单元和一第二级直流对直流变换器的功率单元；所述控制单元包括所述第一级直流对直流变换器的控制单元和所述第二级直流对直流变换器的控制单元。

12.根据权利要求 11 所述的电源装置，其特征在于，所述第一级直流对直流变换器为隔离型直流对直流变换器；所述第二级直流对直流变换器为非隔离调整型直流对直流变换器。

13.根据权利要求 12 所述的电源装置，其特征在于，所述非隔离调整型直流对直流变换器比所述隔离型直流对直流变换器靠近所述主板。

14. 根据权利要求 11 所述的电源装置，其特征在于，所述第一级直流对直流变换器为非隔离调整型直流对直流变换器；所述第二级直流对直流变换器为隔离非调整型直流对直流变换器。

15. 根据权利要求 14，其特征在于，所述第一级直流对直流变换器为升降压电路。

16. 根据权利要求 10 所述的电源装置，其特征在于，所述两功率单元中一所述功率单元包括一第一级直流对直流变换器的功率单元和一第二级直流

对直流变换器的功率单元。

17.根据权利要求 16 所述的电源装置，其特征在于，所述第一级直流对直流变换器为隔离型直流对直流变换器，第二级直流对直流变换器为非隔离调整型直流变换器。

18.根据权利要求 17 所述的电源装置，其特征在于，所述隔离型直流对直流变换器包括：隔离型变压器、若干原边开关管和副边开关管；所述非隔离调整型直流变换器为负载点降压直流变换器。

19.根据权利要求 18 所述的电源装置，其特征在于，所述隔离变压器、副边开关管、用于隔离直流对直流变换器的输出电容器和负载点直流变换器设置于同一个所述功率单元。

20.根据权利要求 18 所述的电源装置，其特征在于，所述原边开关管设置于所述控制单元，所述控制单元还包括原边开关管驱动电路、负载点直流变换器的控制驱动电路和控制芯片。

21.根据权利要求 20 所述的电源装置，其特征在于，所述原边开关管位于靠近所述控制单元侧面的位置。

22. 根据权利要求 10 所述的电源装置，其特征在于，所述功率单元之间、所述功率单元与所述控制单元之间填充有导热绝缘胶。

23. 根据权利要求 10 所述的电源装置，其特征在于，所述功率单元与所述控制单元电性连接的引脚之间以及所述功率单元与所述功率单元电性连接的引脚之间填充有导电焊接材料。

24. 根据权利要求 10 所述的电源装置，其特征在于，所述功率单元各包括一平面变压器，所述两个平面变压器共用一磁芯。

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25. 根据权利要求 24 所述的电源装置，其特征在于，所述磁芯的气隙设置于所述功率单元之间的堆叠间隙。

26.根据权利要求 3 所述的电源装置，其特征在于，所述功率单元包括若干开关器件以及承载所述开关器件的载板和包覆所述开关器件的绝缘封料；所述开关器件分布于靠近所述焊盘的位置。

27.根据权利要求 26 所述的电源装置，其特征在于，所述绝缘封料上设有配合所述引脚安装的凹部。

28.根据权利要求 26 所述的电源装置，其特征在于，所述功率单元还包括电感和电容，所述电感、所述电容及所述开关器件位于所述载板上靠近所述功率单元侧面的位置。

29. 根据权利要求 3 所述的电源装置，其特征在于，所述焊盘包括一次侧群焊盘与二次侧群焊盘，所述一次侧群焊盘与所述二次侧群焊盘之间至少间隔一安规距离。

30. 根据权利要求 29 所述的电源装置，其特征在于，所述一次侧群焊盘包括第一信号焊盘与第一功率焊盘，所述第一功率焊盘的截面积大于所述第一信号焊盘的截面积。

31. 根据权利要求 30 所述的电源装置，其特征在于，所述二次侧群焊盘包括第二信号焊盘与第二功率焊盘，所述第二功率焊盘的截面积大于所述第二信号焊盘的截面积。

32. 根据权利要求 31 所述的电源装置，其特征在于，所述第二功率焊盘的数量多于所述第一功率焊盘的数量。

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33. 一种电源装置，其特征在于，包括：

控制单元与功率单元，堆叠设置且毗邻设有数据处理芯片的负载的位置，所述功率单元至少含一功率半导体器件，所述控制单元至少含一具备控制或者驱动能力的芯片；以及

引脚，电性连接所述控制单元和所述功率单元；所述控制单元用于控制所述功率单元，使所述功率单元供电给毗邻的所述负载。

34. 根据权利要求 33 所述的电源装置，其特征在于，所述控制单元与所述功率单元，堆叠设置设于主板上，所述主板还设有所述数据处理芯片的所述负载。

35. 根据权利要求 33 所述的电源装置，其特征在于，还包括：焊盘，分布于所述功率单元的侧面和所述控制单元的侧面，与所述引脚电性连接。

36. 根据权利要求 33 所述的电源装置，其特征在于，所述电源输入操作最高电压高于 20V，

所述功率单元包含：

至少一变压器，所述变压器含至少一原边和至少一副边；

至少一同步整流组合和一输出电容组合；

高频能量从所述原边传递至所述副边，并通过所述同步整流组合整流为直流后传递至所述输出电容整合。

37. 根据权利要求 36 所述的电源装置，其特征在于，所述控制单元由嵌入式工艺实现，厚度低于 2 毫米。

38. 根据权利要求 37 所述的电源装置，其特征在于，所述功率单元为谐振型电路，操作频率高于 1MHZ。

39. 根据权利要求 37 所述的电源装置，其特征在于，所述控制单元上方更堆叠一输入滤波器。

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40. 根据权利要求 33 所述的电源装置，其特征在于，所述功率单元为一第一级直流对直流变换器；所述控制单元为和一第二级直流对直流变换器的功率单元。

41. 根据权利要求 40 所述的电源装置，其特征在于，所述第一级直流对直流变换器为非隔离调整型变换器；所述第二级直流对直流变换器为非调整隔离型变换器。

42. 根据权利要求 40 所述的电源装置，其特征在于，所述第一级直流对直流变换器为隔离型变换器；所述第二级直流对直流变换器为非隔离调整型变换器。

43. 根据权利要求 33 所述的电源装置，其特征在于，还包含至少一散热单元，该散热单元置于焊盘或者引脚组合上方，且与焊盘或者引脚间的热阻小于 5 摄氏度/瓦。

44.根据权利要求 43 所述的电源装置，其特征在于，所述散热单元与焊盘或者引脚组合之间有绝缘材料。

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电源装置

技术领域

本发明是有关于一种电源装置，且特别是有关于一种电源装置的内部结构。

背景技术

随着人类对智能生活要求的提升，社会对数据处理的需求日益旺盛。全球在数据处理上的能耗，平均每年达到数千亿甚至数万亿度；而一个大型数据中心的占地面积可以达到数万平方米。因此，高效率和高功率密度，是这一产业健康发展的关键指标。

数据中心的关键单元是服务器，其主板通常由 CPU、Chipsets、内存等等数据处理芯片和它们的供电电源及必要外围元件组成。随着单位体积服务器处理能力的提升，意味着这些处理芯片的数量、集成度也在提升，导致空间占用和功耗的提升。因此，为这些芯片供电的电源（因为与数据处理芯片同在一块主板上，又称主板电源），就被期望有更高的效率，更高的功率密度和更小的体积，来支持整个服务器乃至整个数据中心的节能和占地面积缩小。

在服务器的中，主板(Main Board PCB)用于进行能量和信号传递。主板上放置有数据处理芯片及其供电电源。服务器的外壳高度，通常为一个标准的数值，它可以用工业标准 U 来定义，如 1U、1.5U、2U 等（1U=1.75inch=44.45mm）。以 1U 即高度约 40mm(因为有装配工差等需要，1U 实际尺寸不尽相同)服务器为例，主板通常为 6～50 层的 PCB 板，其造价相当昂贵。在一定服务器外壳高度的限制下，保证效率期望的同时，减小主板电源所占用主板的面积也即主板电源水平面积，不仅能减小体积，增加功率密度，而且能降低成本。本文中，称电源单位水平面积的功率为“功率压强”。

当用同一技术能力设计功率为 Po 的电源时，通常电源的体积 V 越大，其效率越容易做到较高，也即电源效率与其体积 V 成正比关系。而体积 V 等于高度 H 乘以水平面积 S。功率压强 Pp 则为 Po/S。限定效率为固定目标，即效

率保持不变。即可得到功率压强 Pp 与高度 H 的关系：即 H 越大，Pp 就可以越大。也即，要提高 Pp，应当在高度 H 的利用上，思考解决方案。当然，如果是为了追求效率，根据前面的逻辑也应当充分利用高度。因此，如何利用高度是兼顾功率压强 Pp 和效率的关键所在。

主板电源的厚度或者说高度较好的可以做到 7mm 甚至更薄，因此，在一定的服务器高度的限制下，如 1U 高度，其上方仍可以有大于 20mm 的空间。而其效率可以高至 90%甚至以上，由于其功耗仅仅是数据处理芯片的几分之一（如 0.1 倍），事实上，有机会无需散热单元即可自行处理热问题。这样主板电源上的空间就没有充分的利用起来。

通常主板电源具体的做法一般包含两种。其一是以 PCB 为载体，采用分立元件组装而成。通过业界多年的努力，这种类型的主板电源实现了不错的效率和功率密度。但由于分立元件组装，需要必要的间隙、安规距离，影响了水平面积的进一步缩小，且高度不规则，也影响热的后续处理。

而主板电源的另一种做法为采用一定的封装技术，将电源各元件集成为一个很规则的元件。由于封装技术的使用，使得其功率密度显着提高，效率也不逊色，且规则的外形，有利于后续热的处理，是不错的解决方案。只是这种做法采用的封装技术，主要追求通过主板电源高度的降低来实现其体积的缩小及功率密度的提高，而一味的降低高度将限制其在占地面积上的进一步缩小。因此，该解决方案仅是追求功率密度的较好方案之一，但在追求数据中心主板电源的功率压强方面仍有较大欠缺。

发明内容

本发明即针对现有技术的不足之处，提出了新的解决方案，使得功率压强和效率得到最大兼顾，适合对水平面积有较大限制的应用场合，例如数据中心等数据处理场合对电源的需求。

本发明的一方面是在提供一种电源装置，其包括控制单元与功率单元，堆叠设置且毗邻负载的位置，功率单元至少含一功率半导体器件，所述控制单元至少含一具备控制或者驱动能力的芯片；引脚，电性连接控制单元和功率单元；控制单元用于控制功率单元，使功率单元供电给毗邻的负载。

于一实施例中，控制单元与功率单元，堆叠设置设于主板上，所述主板还

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设有所述负载。

于一实施例中，电源装置还包括：焊盘，分布于所述功率单元的侧面和所述控制单元的侧面，与所述引脚电性连接。

于一实施例中，引脚包括表面贴装引脚，分布于功率单元和控制单元的外表面并与焊盘电性连接。

于一实施例中，表面贴装引脚覆盖功率单元30%以上外表面积。

于一实施例中，引脚还包括直插引脚，直插引脚配合表面贴装引脚实现功率单元/控制单元与主板的电性连接。

于一实施例中，焊盘还分布于功率单元与焊盘所在侧面垂直的面。

于一实施例中，功率单元包括主功率单元部分和次功率单元部分，主功率单元部分的侧面分布焊盘，次功率单元部分堆叠于主功率单元部分。

于一实施例中，功率单元与负载位于主板的同一面，控制单元位于主板与功率单元相对的另一面。

于一实施例中，电源装置还包括一功率单元，两功率单元和控制单元相互之间堆叠设于主板，控制单元通过引脚控制两功率单元。

于一实施例中，两功率单元分别为一第一级直流对直流变换器的功率单元和一第二级直流对直流变换器的功率单元；控制单元包括第一级直流对直流变换器的控制单元和第二级直流对直流变换器的控制单元。

于一实施例中，第一级直流对直流变换器为隔离型直流对直流变换器；第二级直流对直流变换器为非隔离调整型直流对直流变换器。

于一实施例中，非隔离调整型直流对直流变换器比隔离型直流对直流变换器靠近主板。

于一实施例中，两功率单元中一功率单元包括一第一级直流对直流变换器的功率单元和一第二级直流对直流变换器的功率单元。

于一实施例中，第一级直流对直流变换器为隔离型直流对直流变换器，第二级直流对直流变换器为非隔离调整型直流变换器。

于一实施例中，隔离型直流对直流变换器包括：隔离型变压器、若干原边开关管和副边开关管；非隔离调整型直流变换器为负载点降压直流变换器。

于一实施例中，隔离变压器、副边开关管、用于隔离直流对直流变换器的输出电容器和负载点直流变换器设置于同一个功率单元。

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于一实施例中，原边开关管设置于控制单元，控制单元还包括原边开关管驱动电路、负载点直流变换器的控制驱动电路和控制芯片。

于一实施例中，原边开关管位于靠近控制单元侧面的位置。

于一实施例中，功率单元之间、功率单元与控制单元之间填充有导热绝缘胶。

于一实施例中，功率单元与控制单元电性连接的引脚之间以及功率单元与功率单元电性连接的引脚之间填充有导电焊接材料。

于一实施例中，功率单元各包括一平面变压器，两个平面变压器共用一磁芯。

于一实施例中，磁芯的气隙设置于功率单元之间的堆叠间隙。

于一实施例中，功率单元包括若干开关器件以及承载开关器件的载板和包覆开关器件的绝缘封料；开关器件分布于靠近焊盘的位置。

于一实施例中，绝缘封料上设有配合引脚安装的凹部。

于一实施例中，功率单元还包括电感和电容，电感、电容及开关器件位于载板上靠近功率单元侧面的位置。

于一实施例中，焊盘包括一次侧群焊盘与二次侧群焊盘，一次侧群焊盘与二次侧群焊盘之间至少间隔一安规距离。

于一实施例中，一次侧群焊盘包括第一信号焊盘与第一功率焊盘，第一功率焊盘的截面积大于第一信号焊盘的截面积。

于一实施例中，二次侧群焊盘包括第二信号焊盘与第二功率焊盘，第二功率焊盘的截面积大于第二信号焊盘的截面积。

于一实施例中，第二功率焊盘的数量多于第一功率焊盘的数量。

于一实施例中，第一级直流对直流变换器为非隔离调整型直流对直流变换器；第二级直流对直流变换器为隔离非调整型直流对直流变换器。

于一实施例中，第一级直流对直流变换器为升降压电路。

本发明的另一方面是在提供一种电源装置，电源装置包括：控制单元、功率单元与引脚。控制单元与功率单元堆叠设置且毗邻设有数据处理芯片的负载的位置，功率单元至少含一功率半导体器件，控制单元至少含一具备控制或者驱动能力的芯片；引脚电性连接控制单元和功率单元；控制单元用于控制功率单元，使功率单元供电给毗邻的负载。

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于一实施例中，控制单元与功率单元堆叠设置设于主板上，主板还设有数据处理芯片的所述负载。

于一实施例中，电源装置还包括：焊盘，分布于所述功率单元的侧面和所述控制单元的侧面，与所述引脚电性连接。

于一实施例中，电源输入操作最高电压高于 20V，功率单元包含：至少含一变压器，变压器含至少一原边和至少一副边；至少含一同步整流组合和一输出电容组合；高频能量从原边传递至副边，并通过同步整流组合整流为直流后传递至输出电容整合。

于一实施例中，控制单元由嵌入式工艺实现，厚度低于 2 毫米。

于一实施例中，功率单元为谐振型电路，操作频率高于 1MHZ。

于一实施例中，控制单元上方更堆叠一输入滤波器。

于一实施例中，功率单元为一第一级直流对直流变换器；控制单元为和一第二级直流对直流变换器的功率单元。

于一实施例中，第一级直流对直流变换器为非隔离调整型变换器；第二级直流对直流变换器为非调整隔离型变换器。

于一实施例中，第一级直流对直流变换器为隔离型变换器；第二级直流对直流变换器为非隔离调整型变换器。

于一实施例中，电源装置还包含至少散热单元，该散热单元置于焊盘或者引脚组合上方，且与焊盘或者引脚间的热阻小于 5 摄氏度/瓦。

于一实施例中，散热单元与焊盘或者引脚组合之间有绝缘材料。

综上所述，本发明的技术方案与现有技术相比具有明显的优点和有益效果。通过上述技术方案，可达到相当的技术进步，并具有产业上的广泛利用价值。由于本发明采用了堆叠的结构，电源的高度就可以更好利用，在一定体积下，实现了更小的占地面积；同时又有足够的体积保证高的效率，实现了高功率压强和高效率的兼顾。也为实现更高特性的数据处理设备提供了支持。

以下将以实施方式对上述的说明作详细的描述，并对本发明的技术方案提供更进一步的解释。

附图说明

为让本发明的上述和其它目的、特征、优点与实施例能更明显易懂，所附

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附图的说明如下：

图 1 是依照本发明一实施例的一种电源装置的侧视图；

图 2 至图 16 是依照本发明实施例所绘示的电源架构及堆叠内容分配；

图 17 至图 19 是依照本发明实施例所绘示的控制单元与功率单元可涵盖的内容；

图 20 至图 23 是依照本发明实施例所绘示的堆叠结构设计；

图 24 至图 34 是依照本发明实施例所绘示的引脚布置；

图 35 至图 40 是依照本发明实施例所绘示的散热处理架构；以及

图 41 至图 43 是依照本发明实施例所绘示的磁芯配置。

具体实施方式

为了使本发明的叙述更加详尽与完备，可参照所附的附图及以下所述各种实施例，附图中相同的号码代表相同或相似的组件。另一方面，众所周知的组件与步骤并未描述于实施例中，以避免对本发明造成不必要的限制。

于实施方式与权利要求书中，涉及“耦接(coupled with)”的描述，其可泛指一组件透过其它组件而间接连接至另一组件，或是一组件无须透过其它组件而直接连接至另一组件。

本发明的技术态样是一种电源装置，其可应用在服务器，或是广泛地运用在各种技术领域。值得一提的是，本技术态样的电源装置采用了堆叠的结构，电源的高度就可以更好利用，在一定体积下，实现了更小的占地面积。

图 1 是依照本发明一实施例的一种电源装置的侧视图。如图 1 所示，电源应用装置（如：电源装置）包括主板 110、功率单元 120、控制单元 130 与引脚 140。主板 110 上还设有负载 150，功率单元 120 位在主板 110 上，控制单元 130 与功率单元 120 堆叠设置于主板 110 上毗邻负载 150 的位置，引脚 140 电性耦接主板 110、控制单元 130 和功率单元 120，于本实施例中，引脚 140 的数量为多个且分别位于功率单元 120 与控制单元 130 中每一者的侧边，两功率单元 120 和控制单元 130 相互之间堆叠设于主板 110。控制单元 130 用于控制功率单元 120，具体而言，控制单元通过引脚 140 控制所述两功率单元 120，使功率单元 120 供电给毗邻的负载 150。负载 150 为数字处理 IC，如中央处理器(CPU)，中央处理器上有设有散热单元散热装置如散热器 151。功率单元 120

至少含一功率半导体器件（如：图 3 的开关管 S21、S22、S23、S24，图 11 的开关管 S21、S22、S23、S24、S31、S32、S33），控制单元 130 至少含一具备控制或者驱动能力的芯片（如：图 3 的控制电路 310，图 11 的控制电路 1100、DSP）。

于一实施例，电源装置设于主板 110 上，主板 110 还设有数据处理芯片(如：CPU)的负载 150，电源装置包括：功率单元 120、控制单元 130 与引脚 140。控制单元 130 与功率单元 120 堆叠设置于主板上毗邻负载 150 的位置，引脚电性连接主板 110、控制单元 130 和功率单元 120，控制单元 130 用于控制功率单元 120，使功率单元 120 供电给毗邻的负载 150。

总的而言，直流/直流电源包含了至少两个单元（即模块）：控制单元 130 及功率单元 120。这两个模块上下堆叠放置，通过导体(即引脚 140)进行彼此之间的电气连接以传递电信号。其中功率单元 120 至少包含一个主动开关元件，功率单元 120 接收输入功率通过主动开关元件的导通及关断产生相应的输出功率提供给负载 150，如数据处理芯片。控制单元 130 模块至少包含一个控制芯片，发送控制信号给功率单元 120 的主动开关元件以控制该元件的导通及关断。置于上方的单元，部分引脚通过置于下方的单元固定后，传递电信号至上述的主板 110(如：PCB 板)。

如此，由于采用了堆叠的结构，电源的高度就可以更好利用，在一定体积下，实现了更小的占地面积；同时又有足够的体积保证高的效率，实现了高功率压强和高效率的兼顾。也为实现更高特性的数据处理设备提供了支持。

涉及的电源架构及堆叠内容分配

如图 2，为一个服务器主板可能涉及的各种类型电源变换器（即主板电源 200）的示意图。该电源变换器输入通常为直流，其电压范围宽广，有高压，如 200～500V（以 400V 为例），中压，如 18～72V（以 48V 为例）以及低压，如 5～15V（以 12V 为例）。不管输入为什么电压，都需要有相应的 DC/DC 变换器，将其变换成所需要的输出，以提供给其负载 150，如数据处理芯片，像是中央处理器(CPU)及内存等。其输出的变化范围也很广泛以适应不同的负载要求，例如输出为低至 0.8V 甚至更低，高至 12 伏甚至更高。当负载 150 为 CPU 和内存时，输出电压通常在 0.8～2V 之间。因此，涉及的电源规格主要含以下几种：

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（1）变换器 210 将 400V 转 48V：输入为 200～500V（以 400V 为典型）之间的某一电压范围，输出为稳定输出或者与输入成固定比例，以 48V 附近为典型值，也可在 18V～72V 之间的某一电压范围。由于输出电压相对较高，通常不会直接接数据处理芯片负载，需在其后级联另一规格变换器，将电压调到适应负载可用的程度。

（2）另一变换器（图未示）将 400V 转 12V：输入为 200～500V（以 400V 为典型）之间的某一电压范围，输出为稳定输出或者与输入成固定比例，以 12V 附近为典型值。由于输出电压较低，可以接部分数据处理负载，如硬盘等。但当负载电压更低时，例如 0.5～5V，则需在其后级联另一规格 DC/DC 变换器，将电压调到适应负载可用的程度。

（3）又一变换器（图未示）将 400V 转 0.5～5V：输入为 200～500V（以 400V 为典型）之间的某一电压范围，输出为按需调整的稳定电压，例如 0.5～5V 之间。其输出可以直接接数据处理芯片，如 CPU、内存等。

以上（1）、（2）、（3）中的三类规格的变换器，由于是高压输入，需要符合高压安规绝缘要求，其绝缘电压高至直流电压 2000V 甚至以上。

（4）变换器 220 将 48V 转 12V：输入为 18～72V（以 48V 为典型）之间的某一电压范围，输出为稳定输出或者与输入成固定比例，以 12V 附近为典型值，也可在 3V～15V 之间的某一电压范围。该规格的变换器可以直接接某些数据处理负载，如硬盘等。

（5）变换器 230 将 48V 转 0.5～5V：输入为 18～72V（以 48V 为典型）之间的某一电压范围，输出为按需调整的稳定电压，例如在 0.5～5V 之间。且输出可直接接数据处理芯片，如 CPU、内存等。

（6）变换器 240 将 12V 转 0.5～5V：输入为 3V～15V（以 12V 为典型）之间的某一电压范围，输出为按需调整的稳定电压，以 0.5～5V 之间。其输出可以直接接数据处理芯片，如 CPU、内存等。由于是低压输入，不需要隔离。输出则直接接数据处理芯片，如 CPU、内存等。

以上（4）、（5）、（6）中的三类变换器，由于输入/输出电压均相对较低，则变换器的耐压需求较低，通常在直流电压 2000V 以下。

当变换器输出为 0.5～5V 时，由于输出可以直接接负载 150，例如数据处理芯片，需要电源变换器输出低压大电流并且要求有很高的动态响应能力，如

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当负载 150 为 CPU 时要求有 1000A/ns 的响应能力，这样就需要电源变换器就近放置在负载附近。因此这些电源被称为负载点电源(Point of the load)。其中尤以给 CPU 供电的叫电压调整模块（Voltage Regulated Module, VRM）需要就近供电。

如上各种输入输出规格的电源变换器，由于均设置在主板之上，因此，均适合用堆叠的方式来实现高功率压强和高效率的兼顾。当然，各种变换器的组合也适合采用堆叠的方式放置。

如上，400V 和 48V 输入的电源，由于输入输出压差较大，也通常有输入输出安规耐压需求，通常由变压器来隔离传递能量。当然，若有需要，例如为实现更宽的输入或者输出范围，低压输入电源如 12V 输入的电源也可以采用变压器来传递能量。

以上各种规格的变换器可以采用多种类型的拓扑来实现电能的变换，例如脉冲宽度调制(PWM)型的正向电路、全桥电路、移相全桥电路、半桥电路、反激式电路等。为了实现高的功率密度，通常需要工作频率较高，如 500kHZ、1MHZ，甚至 2MHZ 以上。为了在这么高的频率下实现高的效率，通常需要选择谐振型电路，即脉冲频率调制(PFM)型的 LLC 串联谐振变换器(LLC-SRC)、并联谐振变换器(PRC)等等。

图 3 所示为一半桥 LLC 电路。如图 3 所示，该电路包含了主电路以及控制电路 310。其中主电路包含了：输入电容器 C1、谐振电容器 C2、谐振电感器 L1、变压器 T1、一次侧开关管 S11、S12 与二次侧开关管 S21、S22、S23、S24，其中输入电容器 C1 连接一次侧开关管 S11、S12，一次侧开关管 S11、S12 连接由谐振电容器 C2、谐振电感器 L1、变压器 T1 的原边组成的串联回路，变压器 T1 的副边连接二次侧开关管 S21、S22、S23、S24，输出电容器 C3 连接所述二次侧开关管 S21、S22、S23、S24。一次侧开关管 S11、S12 接收输入功率并将直流输入信号转换为交流信号，该交流信号经过谐振电感器 L1，谐振电容器 C2 及变压器 T1 传送至二次侧，通过二次侧同步整流线路（如，二次侧开关管 S21、S22、S23、S24），在输出电容器 C3 上产生输出电压并提供输出功率给负载。特别提及的是，由于输出为低压大电流，为了减少损耗，通常需要涉及低压大电流的组件（如 T1 副边、副边整流管、输出电容）进行并联已获得低的低电阻。如由“一整流组合 S21、S22 与一副边形成的组合”

和“另一整流组合 S23、S24 与另一副边组成的组合”进行并联。由于输出电压各有不同，因此，变压器副边的结构并非限制于图 3 所示的中心抽头整流结构，也可以是其他如全桥整流结构。

控制电路 310 产生控制信号提供给驱动一次侧开关管 S11、S12 的驱动器 320，和驱动二次侧开关管 S21～S24 的驱动器 330 用以控制主电路中各开关元件，如开关管 S11、S12，S21～S24 等的开通及关断。当然控制电路 310 还有包含其他采样、保护、通信等等必要元件在图中并未展示，在此也不做赘述。

功率单元 120 由于在高频工作状态下，并且变换器的输出为低压大电流，通常变压器二次侧、输出同步整流线路及输出电容器三者组成的回路尽量的小，以适应高频需要。因此，变压器 T1、同步整流线路（即，二次侧开关管 S21、S22 等）、输出电容器 C3 必须放在同一单元电路（即，功率单元 120）中。

于一实施例，电源输入操作最高电压高于 20V，功率单元 120 包含：至少一变压器 T1，变压器 T1 含至少一原边和至少一副边；至少一同步整流组合（如：二次侧开关管 S21、S22）和一输出电容组合（如：输出电容器 C3）。高频能量从原边传递至副边，并通过同步整流组合整流为直流后传递至输出电容整合。

另一方面，控制电路 310 的周边通常有许多的外围电路，需要处理的信号通常很低，也要求就近放置以便提升抗干扰的能力。因此，控制电路 310 及其外围电路需在同一单元电路（即，控制单元 130）中。于一实施例，控制单元 130 由嵌入式工艺实现，厚度低于 2 毫米。功率单元为谐振型电路，操作频率高于 1MHZ。控制单元上方更堆叠一输入滤波器。

至于驱动电器 320、330、一次侧开关管 S11～S12、谐振电容器 C2、谐振电感器 L1，可以根据实际情况放置在功率单元 120 或者控制单元 130。输入电容器 C1 对一次侧开关管 S11～S12 有抑制电压尖峰的作用，因此最好与一次侧开关管 S11、S12 就近放置于同一单元中为佳。L1/C2 等可以与其他元件如 T1 集成而成。甚至 T1 的激磁电感也可以由一独立电感与变压器原边并联，以协助 T1 性能的优化。

如图 1 所示，整个功率电路采用控制单元 130 与功率单元 120 进行堆叠组合，将有效地减小该功率电路 120 的水平面积，在最后放置于主板 110 上时，

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减小占用主板 110 的面积。如图 1 中，控制单元 130 或功率单元 120 可以采用封装的技术，例如采用塑封料对其进行模制（molding），形成一模块。或者，两者也可以采用分立元件制作。无论何种方式，各单元都可以包含一载板，如：印刷电路板（PCB）或者陶瓷电路板（DBC）等等，用以承载该单元的器件，或者，也可以采用单元内器件直接堆叠的方式，如开关元件与电感、电容等元件直接堆叠的方式。当一次侧开关管 S11～S12、谐振电容器 C2、谐振电感器 L1 集成于功率单元时，控制单元中电路将主要处理控制信号，因此其高度可以变得很小，如 5mm、3mm 甚至 1mm 以下。

而在功率较大的场合，可以将图 3 所示的多个主电路进行输入输出的并联。这样整个电源装置在结构上可以采用一个主电路为一个功率单元，多个相同的功率单元，及控制单元进行堆叠的方式，如图 1 所示。控制单元 130 可以放置于下面，两个功率单元 120 堆叠于上面，或者控制单元放置于两个功率单元中间，又或者控制单元放置于两个功率单元之上。无论何种方式，均充分地利用了高度，实现了占地面积不变的状态下进行功率的提升。其中控制单元 130 可以为一个，用于控制两个功率单元 120 中开关元件的开通和关断，也可以为多个，例如两个分别控制相应功率单元中开关元件的开通与关断。当然，也可以将控制单元与其中一个功率单元集成在一起，这样最后变成了至少一个功率单元 120 与一个控制单元 130 堆叠在一起，其中该控制单元集成了至少一个主电路。如图 4 所示。电源模块包含了功率单元 120 与控制单元 130 上下堆叠，并通过引脚 140 彼此进行电气连接。其中功率单元 120 集成一个直流到直流变换器，控制单元 130 集成另一个直流到直流变换器及控制电路，控制电路控制这两个直流到直流变换器。

如前面所述，电源装置接收输入产生输出提供能量给负载。该电源装置可以采用单级的变换器，例如如图 3 所示电路，实现电压转换的要求，甚至于隔离。当然也可以采用多级的变换器。由于受器件特性的限制，单级电路通常不适合宽范围输入输出，因此，针对电压范围宽的负载，如服务器电源的应用中的 CPU、内存等负载，比较适宜的是采用两级架构的电源，即其中一级负责隔离，另一起负责调压，各司其职，以达到最优状态。举例说来如图 5 和图 6 所示。

如图 5 所示，输入电压 Vin 为一宽的电压范围，例如 38～60V，该输入电

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压通过前级电路例如一隔离非调整型直流对直流变换器，亦即：隔离变压模块DCX，（此处，“非调整型”是指在工作范围内的该电路的输入输出为固定比例关系，也即输出随输入成比例变化如 Vin/Vo=n，图中以 Vin/Vo=4 为例），实现高压隔离；然后通过后级电路例如一非隔离调整型直流对直流变换器提供输出给负载。举例来说，后级电路可为负载点变换单元 POL，其可以用来实现输出稳压和动态响应需求。由于后级电路具备调整能力，因此，前级电路可以不具备调整能力。但如果有需要，前级也可以具备或者部分具备调整能力，即为隔离型直流对直流变换器。

同时参照图 1、5，两功率单元 120 分别为第一级直流对直流变换器的功率单元和第二级直流对直流变换器的功率单元；控制单元 130 包括第一级直流对直流变换器的控制单元和第二级直流对直流变换器的控制单元。具体而言，第一级直流对直流变换器为隔离型直流对直流变换器；第二级直流对直流变换器为非隔离调整型直流对直流变换器(如图 5 所示)，非隔离调整型直流对直流变换器比所述隔离型直流对直流变换器靠近主板 110。或者，第一级直流对直流变换器为非隔离调整型直流对直流变换器，第二级直流对直流变换器为隔离非调整型直流对直流变换器。举例而言，第一级直流对直流变换器为升降压电路。

于一实施例，功率单元 120 为一第一级直流对直流变换器；控制单元 130 为和一第二级直流对直流变换器的功率单元。举例而言，第一级直流对直流变换器为非隔离调整型变换器；第二级直流对直流变换器为非调整隔离型变换器；或者，第一级直流对直流变换器为隔离型变换器；第二级直流对直流变换器为非隔离调整型变换器。

由于前级为非调整型的隔离变压模块 DCX，可以在设计上使该电路工作于其最佳工作点，从而使电路相对简单且效率很高。当隔离变压模块 DCX 为一谐振电路，则隔离变压模块 DCX 可以工作在谐振频率附近；而当直流变压器 DCX 为一 PWM 线路，如全桥线路，则可以工作在占空比最大的状态下。后级为调整的电路，例如负载点直流变换器 POL，通常由降压式变换电路（Buck 电路）来实现（如：负载点降压直流变换器），使得输出特性满足负载的要求，该线路简单，且输出电压范围很宽。两者结合，可以很容易地实现宽输入/输出电压范围以及高输出电压精度及动态响应特性等要求。当隔离变

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压模块 DCX 采用谐振电路时，例如 LLC-SRC 电路，则较容易实现电源的高频下的高效率，并有很高的功率密度。当然，由于后级有调整功能，DCX 若因为某种原因，如减少中间 BUS 电压范围，以减少中间 BUS 电容及相关功率器件的耐压幅值，而具备一定程度的输出电压调整能力，也不影响本实施例的实现和作用。

如图 6 所示，输入电压 Vin 为一宽的电压范围，例如 38～60V。该输入电压 Vin 通过前级电路例如一个非隔离调整型直流变换器，亦即：前级调压模块（Front Regulate Module）FRM，将变化输入的电压转换成一个需要的值，例如一恒定电压 48V，并可以响应负载的动态变化；再在其后串联使用隔离非调整型直流变换器，亦即隔离变压模块 DCX 来实现电压隔离，并实现降压需求。该架构下最终输出即后级电路的输出的稳压和动态响应均由前级电路实现。由于前级调压模块 FRM 无需隔离，所以可以用多种拓扑例如降压、升压或者降、升压电路等来实现，为了高频需要，可以加以软开关技术。因此前级调压模块 FRM 也可以有很高的功率密度，隔离变压模块 DCX 也是如此。

同时参照图 1、6，两功率单元 120 中一功率单元 120 包括第一级直流对直流变换器的功率单元和第二级直流对直流变换器的功率单元，第一级直流对直流变换器为隔离非调整型直流对直流变换器，第二级直流对直流变换器为非隔离调整型直流变换器(如图 6 所示)。

以上两种电源架构下，以一个输出功率为 200W 的主板电源为例，在 1/16 砖（1.3in*0.9in, 33mm*22.9mm）即可分别实现隔离变压模块 DCX 和负载点直流变换器 POL（图 5 架构）或是前级调压模块 FRM 和隔离变压模块 DCX（图 6 架构），因此，其功率压强也为 85.5W/inch2（实际由于两个单元的安装空隙等需要，其功率压强更低）。由于两者高度均可在 10mm 甚至 7mm 之内。如果用本发明的方法，将两者堆叠，如图 7 所示，控制单元与功率单元整合成隔离变压模块 DCX 与负载点直流变换器 POL 堆叠设置于主板 110 上；或者，如图 8 所示，控制单元与功率单元整合成前级调压模块 FRM 和隔离变压模块 DCX 堆叠设置于主板 110 上。借此，功率压强可以立即倍升至 171W/inch2，大大缩小对主板面积的占用。即便堆叠可能需要一些额外的高度，如散热处理等等原因，其总高度也可以在 25mm 以下，完全可以满足服务器的高度需求（可以高至 30mm）。

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为了减少内部互连引脚占用的体积，可以将上述隔离变压模块 DCX 与负载点直流变换器 POL 的功率级做在同一功率单元 120 中，再将两级的控制电路做在同一控制单元 130 中。这样就可以集中处理功率部分，以得到更优效率和更小占地面积。其功率单元部分，也可根据实际功率需要，选择一个或者多个并联，如图 9 所示，多个功率单元 120 并联且均包括隔离变压模块 DCX 与负载点直流变换器 POL 中的功率级，控制单元 130 包括隔离变压模块 DCX 与负载点直流变换器 POL 中的控制电路。

图 11 是图 5 中电路架构的原理图。它与图 3 不同之处在于，它在图 3 的基础上增加了后级电路---负载点直流变换器 POL 的电路，例如图 11 中的降压电路。因为输出是低压大电流，POL 的实现往往由多个降压电路并联而成。具体并联的数量由实际情况而定。图 11 以三个并联为例。隔离非调整型直流对直流变换器包括：隔离变压器 T1、若干原边开关管 S11、S12 和若干副边开关管 S21、S22 等；非隔离调整型直流变换器为负载点直流变换器 POL。其中，每个负载点直流变换器 POL 的电路都分别包含了开关管 S31、S32 及 S33 及与开关电路连接的滤波电感器 L21、L22 及 L23，从而相应组成了降压电路。各负载点直流变换器 POL 的电路的输出并联于电容器 C4 的两端，以产生输出功率提供给负载。控制芯片 1100 用以产生控制信号以控制负载点直流变换器 POL 中开关元件的开通与关断。为了实现高效率，功率单元 120 至少包含隔离变压模块 DCX 的隔离型变压器 T1、同步整流开关管 S21～S24、输出电容器 C3 和负载点直流变换器 POL 中的开关管 S31～S33。换言之，隔离变压器 T1、副边开关管 S21、S22、S23、S24、用于隔离直流对直流变换器的输出电容器 C3 和负载点直流变换器 POL 设置于同一个功率单元 120。当然，图 11 中还包含了,滤波电感器 L21～L23 以及输出电容器 C4。控制单元 130 至少包含一个控制芯片 1100 及其外围电路，例如图中的信号处理器 DSP 及控制器的外围线路(图中未显示)。原边开关管 S11、S12 设置于控制单元 130，控制单元 130 还包括原边开关管驱动电路、负载点直流变换器的控制驱动电路和控制芯片 1100。

而对于前级调压模块 FRM 和隔离变压模块 DCX 的架构，也可以如此实现，得到更高效率和更高功率压强的兼顾，如图 10 所示，多个功率单元 120 并联且均包括前级调压模块 FRM 和隔离变压模块 DCX 中的功率级，控制单

元 130 包括前级调压模块 FRM 和隔离变压模块 DCX 中的控制电路。

当然，上述的隔离变压模块 DCX 也可以是可调整的变换器或者半调整的变换器。其功能的变化，并不影响本发明对其效率和功率压强提升的贡献。

以上实施例，电源都采用了直流到直流(DC/DC)变换器。这些例子可以应用于例如直流电源直接输入到服务器主板的架构中。当然，随着技术的发展，也会出现有交流电源 AC 直接输入到服务器主板 1200。如图 12 所示，交流电源 AC(例如 220Vin)直接接入服务器主板 1200，通过由各级级联或并联的电源模块 1201～1205 组成的主板电源 1210 将输入功率传送给相应的负载。与前面直流输入的主板电源相比较，该结构下还多了前级级联的电磁干扰滤波器(EMI filter)1221、功率因数校正(PFC)电路 1222 以及辅助电源模块(Aux. Power Module) 1223 等等。在该架构下，同样可以采用前面所述的堆叠技术。

如图 13，为一电磁干扰滤波器 1310 后级联功率因数校正电路 1320 的示意图。如图所示，电磁干扰滤波器 1310 接收交流输入，如 VAC =220V,之后，提供一输出信号给后级的 PFC 电路进行功率因数校正。功率因数校正电路 1320 实际可以采用各种类型的拓扑，例如升压、降压、双升压以及如图所示的图腾柱式结构等等。以图中所示的图腾柱式功率因数校正电路为例，该功率因数校正电路 1320 的主电路中包含了高频电容器 C、功率因数校正电感器 L 以及功率开关器件，即由主动开关元件 S1、S2 串联所组成的第一桥臂及被动开关元件 D1、D2 串联所组成的第二桥臂。第一及第二桥臂与高频电容器 C 并联连接，功率开关器件和高频电容器 C 电性耦接功率因数校正电感器 L；两个桥臂的中点分别连接电磁干扰滤波器 1310 的输出或者通过输入电感连接滤波器的输出。相应的功率因数校正的驱动和控制电路 1330 用于控制功率开关器件，具体而言，功率因数校正的驱动和控制电路 1330 包含了输出采样分压电路(Voltage divider)1331 用于采样功率因数校正主电路的输出 VDC，输入采样分压电路 1332、1333、1334 用于采样输入电压 VAC-P 及 VAC-N，以及输入电流 IL 的采样等采样电路。输出电压采样分压电路 1335 的输出信号 VDC 与相应的参考信号 VDC-ref 比较后通过电压环控制器(voltage loop controller)1335 输出一信号与 VAC 进行运算得到了输入电流 IL 的参考信号 IL-ref，输入电流 IL 经过运算与 IL-ref 进行比较后通过电流环控制器(current loop controller)1336 后得到相应的控制信号 PWM-S1 及 PWM-S2 用以控制开关

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S1 及 S2。

图 14 所示为功率因数校正电路的堆叠结构示意图。可以将功率因数校正电路的主电路中的第一桥臂，第二桥臂，输出电容及相应的驱动，控制单元等集成于控制单元中，而将功率因数校正电感器 L 放置于功率单元 120 中，之后将功率单元 120 放置于控制单元 130 之上进行堆叠。这样就可以在控制单元 130 中优化电分布参数，得到更好特性，而把更多的体积留给电感，也有利于将效率提升至更高。当然，也可以将主电路都集成于功率单元 120 中，而将驱动和控制电路 1330 集成于控制单元 130 中。

如图 15 所示，则可以在图 14 的基础上，再堆叠一功率单元---电磁干扰滤波器单元。因为电磁干扰滤波主要是为功率因数校正电路服务，与功率因数校正电路就近堆叠，更有利于优化设计，实现更高特性。同样，辅助电源也可以采用与功率因数校正电路相似的堆叠方式。即将控制、驱动及一次侧的功率器件和高频电容等集成在控制单元中，而将变压器和输出整流、输出电容集成在功率单元中。如上各图所示的堆叠均可得到本发明兼顾功率密度和功率压强的好处。当然，其堆叠的顺序，可以根据实际需要而调整。

另一方面，本发明也适用于 DC/AC 场合，即逆变器(inverter)场合。图 16 所示为功率单元 120 包括一逆变器电路，直流输入 Vin 通过由主动开关元件 S1、S2 串联组成的第一桥臂以及主动开关元件 S3、S4 串联组成的第二桥臂后产生一交流信号，该信号通过滤波电路（包括滤波电感器 L、输出电容器 Co）之后在输出电容器 Co 上产生一输出电压 Vo。其具体的控制与驱动电路在该图中未显示。这样的逆变器也可以采用类似前面所述功率因数校正电路的堆叠结构。即控制单元中集成主电路的第一及第二桥臂，输入电容器 Cin 及控制驱动电路，而功率单元集成输出滤波电感器 L 及输出电容器 Co。当然，也可以将主电路的所有元件，即输出电容器 Cin, S1～S4、滤波电感器 L 及输出电容器 Co 都集成于功率单元 120 中，控制单元集成控制驱动电路等。

控制单元可涵盖的内容

控制单元以信号处理为主要目的，其大部分器件的高度较小，因此，为提升整体的空间利用率，该单元包含的元件可以以薄为评价指标。

如上所述，负责发送信号给驱动电路或者开关器件的控制器（某些特定应用下，驱动电路也可视为控制器的一部份）及其外围必要的电阻电容等元件一

定包含在控制单元内。但随着控制芯片集成度的提升，这些元器件全部放置后，空间上可能仍有一定的盈余。因此，可以增加更多元器件于控制单元中。以图3为例，如果将功率器件全部放置于功率单元120，摆放示意如图17所示。图17左侧为功率单元120的元器件位置摆放图，右侧为控制单元130的元器件位置摆放图。图17中方框表示元器件所摆放的载板1710、1720，该载板1710、1720上放置的元器件，其中左图的标识对应于图3中相应的元器件。如图17，如果功率单元120及控制单元130面积相同，也即两单元的载板1710、1720面积大小相同，则控制单元130的使用率明显偏低。为提高各单元面积的使用率，可以从功率单元挪移部分元器件到控制单元130中，如图18，原边开关管S11、S12位于靠近控制单元侧面的位置，即放置于控制单元130的载板1720上。所移元器件的选择标准除了薄之外，还应当不影响电特性甚至有更好的作用。

高压输入侧的一次侧开关管S11、S12由于是半导体，其厚度可以跟控制芯片相当甚至更薄，有机会放置于控制单元中。以一次侧开关管S11和S12为Mosfet为例，如果将其置于功率单元，如图3所示，功率单元120与控制单元130间则会有4个以上引脚（每个开关的门极以及源极）相互联接；如果将其放置于控制单元130中，则控制单元130与功率单元间的连接只需2个引脚，例如图11中的一次侧开关管S11和S12连接点与开关管S12的源极。而且，由于高压输入侧对电路的分布参数并不特别敏感，因此将其移至控制单元130，对电特性的影响完全在可接受范围内。当然，如果一次侧开关管S11和S12挪移，那么输入电容器C1及其驱动电路也需跟着挪至控制单元130。这样就近放置不仅可以减少一次侧开关管S11和S12的电压尖峰，且可以在功率单元减少不必要的引脚。

图18所示为部分开关器件摆放至控制单元130的示意图。控制单元130包括输入电容器C1、谐振电容器C2与一次侧开关管S11、S12；功率单元120包括若干开关器件以及承载开关器件（如：S11、S12）的载板1710和包覆开关器件的绝缘封料3430（绘示于图34）；开关器件分布于靠近焊盘3440（绘示于图34）的位置。功率单元120包括变压器T1、谐振电感器L1、输出电容器C3与二次侧开关管S21、S22、S23、S24。可以看出，右侧控制单元130的利用率显着提升，而电感（即，谐振电感器L1）、电容（即，输出电容器

C3）及开关器件（即，二次侧开关管 S21、S22、S23、S24）位于载板 1710 上靠近功率单元侧面的位置。左侧功率单元 120 则可以给更多的空间给磁性元件，这对效率的提升有显着意义。因此，可以更好的兼顾高效率和高功率压强。值得留意的是，由于开关管 S11、S12 不在功率单元 120 内，功率单元 120 的输入来源于控制单元 130，并且是经过开关 S11、S12 管调制的高频交流功率信号，如 500KHZ 甚至是 3MHZ 以上，幅值可以是 12V 以下到甚至 400V 以上。

如果在某些应用中，二次侧开关管 S21、S22、S23、S24 的位置对电特性不敏感的话，也可以将二次侧开关管 S21、S22、S23、S24、驱动器 330 及输出电容器 C3、Oring MOS 等设置于控制单元 130 中，这样可以更充分利用空间。

如图 10 所示等堆叠结构，如果将控制单元 130 设置于下方，控制单元 130 位于功率单元 120 与主板 110 之间，则功率单元 120 输出端到主板的引脚变长，可能会影响对负载变化的响应能力，特别是在负载为诸如 CPU 这样的数据处理芯片时。这时，就可以在控制单元 130 设置部分主电路的输出电容器 C3（或者，亦可如图 11 中对应的 POL 输出电容 C4），控制单元 130 包括输出电容器 C3，从而减小该引脚长度的影响，如图 19 所示。当然，这要求在设计时，使得输出电容器 C3 与引脚 140 有部分良好连接。

上面所举的实施例中，控制单元 130 包含了一个载板，例如印刷电路板或者线架(Lead frame)等。当然，整个控制单元也可以用嵌入(Embedded)技术实现。控制单元 130 也可以采用单元内元件相互堆叠，利用元件表面导体进行电气连接的方式。用嵌入(Embedded)技术实现，也即部分电气元件，例如控制 IC、电阻、电容甚至功率半导体等埋藏于载板中。这样可以使得控制单元非常薄且面积小，而且可以实现较为精细的内部和单元表面线路布线。由于 Embedded 技术可以轻易且不受位置限制地实现上下表面的互联，也就是说，可以直接实现相应的 Pin 脚而无需像图 34 所示的以侧面出 Pin。拿含变压器和同步整流器的电路，如桥式谐振型电路为例，可以用 Embedded 技术实现控制单元后，与含变压器和同步整流器的功率模块堆迭，其具备如下特征：功率单元至少含一变压器（Core 和 Winding），输出同步整流器，部分输出电容，SR MOS 的控制信号(可功率模块自行产生也可以由控制单元提供)，以实现功率级的高效

率；功率单元仍选用侧面出 Pin，Pin 至少含输出的正负极，已经过调制的输入侧高频脉冲的两极。控制单元至少内嵌有控制逻辑 IC，负责采样、控制信号及驱动信号生成、保护、以及与电源外部的必要通信，含至少一对高压侧功率元件，并生成传递给功率单元的输入侧高频脉冲；控制单元的 Pin 脚可以侧面排布也可以按需在任意位置穿透上下表面排布，也可以按需由内向表面连接并在一表面排布；由于 Embedded 以后，控制单元可以很薄，如 1mm 左右，Pin 脚以 SMD 为主，以增强 Pin 的连接强度。由于 Embedded 技术，可以轻易实现类似于 PCB 的布线能力，可以在表面实现更加丰富的互联，能支持内容更加丰富的堆叠组合，如将另外一些较难嵌入到控制单元中的必要元件，如输入电磁干扰滤波器，即输入电容，与功率单元一起放置在控制单元表面。由于可以实现很小的体积，更适合高频工作场合，如工作频率达到 1MHZ 以上。因此，变换电路也以谐振型工作的电路为宜。Embedded 实现的控制单元厚度也在 2mm 以下为佳。

控制单元 130 可以是前面例子中所述的控制电路的集合，可以是控制电路包含部分功率电路的元器件，甚至驱动电路，也可以是，如图 7 等所示的一个具备完整功能的电源变换器。这样，控制单元与功率单元堆叠，并通过引脚互相连接甚至通过引脚与主板连接的结构就变成了两个或多个功率单元互相堆叠的结构。只是其中至少一个功率单元内包含了控制单元的元器件。这种结构通常适用于多级功率单元并联或级联等系统架构中。

功率单元可涵盖的内容

总体来讲，功率单元可以是一个完整可独立工作的 DC/DC 或 AC/DC 电源变换器，如；隔离变压模块 DCX、负载点直流变换器 POL、前级调压模块 FRM、调节母线变换器(Regulated Bus Converter, RBC)、功率因数校正电路、辅助电源模块等即一个包含了功率级电路及控制电路的电源变换器，也可以只是它们的功率级电路，甚至如前面实施例中只是功率级电路中的一部份，例如最需要相互就近放置的那部分，如图 18 的变压器 T1、输出整流元件（如，二次侧开关管 S21、S22、S23、S24）及输出电容器 C3 这三个关键元件。功率单元可以像隔离变压模块 DCX、RBC 一样具备隔离的能力，即至少含一个变压器，也可以像负载点直流变换器 POL、前级调压模块 FRM、功率因数校正电路一样无需隔离，即至少含一个电感器。

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功率单元上的变压器和电感器可以是集成在一起的，也可以是独立的。

功率单元的输入可以是直流，也可以是工频的交流，也可以是如图 18 高频的交流。

功率单元的输出可以是 0.1～12V，12V 以上到 400V 的各种电压范围。负载可以是其他电源变换器、硬盘、内存、图形处理芯片、CPU、通信 ASIC 等等各种数据处理芯片。

此外，功率单元与控制单元一样可以包含一个载板，如印刷电路板或者线架等，通过载板上的走线(trace)实现功率单元器件间的电气连接，功率单元中的元器件可以摆放在载板上；也可以采用嵌入(Embedded)技术实现，也即部分电气元件，例如电阻，电容等埋藏于载板中。此外，功率单元也可以采用单元内元件相互堆叠，利用元件表面导体进行电气连接的方式。

当整个电路包含了两个或多个功率单元时，可以像图 19 由完全相同的功率单元进行并联已实现更大功率更大电流变换，或者是串联实现更大功率更高电压变换；也可以像图 8 一样，由不同的功率单元进行串联，实现更大的工作范围；或者由不同的功率单元，实现共用一个输入，提供多个输出的电源变换功能；或者由不同的功率单元，实现提供一个输出，接受多个输入的电源变换功能。

综上所述，本发明的使用范围非常广泛，可以协助服务器实现更高的性能。当然，本发明涉及的电源变换器实现方法，也可以适用于其他应用场合。

堆叠结构设计

本发明的一方面，是在服务器中，通过将一个电源变换器，分解成至少两个单元，即至少一个控制单元 130 和一个功率单元 120，再通过堆叠的方式，来更充分利用空间高度，实现高效率高功率压强的电源变换器，以实现更高性能的服务器。电源变换器堆叠的形式可以有如下几种。

1. 如图 19 所示，各单元 120、130 面积相当，上下直接堆叠后组成一电源变换器，再设置于主板 110 之上。

2. 如图 20 所示，控制单元与功率单元中面积较大者作为第一单元 2010 而面积较小者作为第二单元 2020，第一单元 2010 位于第二单元 2020 与主板 110 之间，各单元面 2010、2020 积有差异，面积小的堆叠放置于面积大的之上组成一电源变换器，再设置于主板 110 之上。如图 21 所示，控制单元与功

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率单元整合成隔离变压模块 DCX、前级调压模块 FRM，此为上述前级调压模块 FRM+隔离变压模块 DCX 架构的实现方式之一，只是为了得到更高的效率，将前级调压模块 FRM 的电感器 L 外置。将前级调压模块 FRM 及其外置电感器 L 设置于隔离变压模块 DCX 的上方后，组成一电源变换器，再设置于主板 110 之上。

3. 如图 22 所示，控制单元与功率单元中面积较大者作为第一单元 2010 而面积较小者作为第二单元 2020，第二单元 2020 位于第一单元 2010 与主板 110 之间，各单元 2010、2020 面积有差异，小的放置于大的下表面，组成一电源变换器，再设置于主板 110 之上。

4. 如图 23 所示，功率单元 120 与负载位于主板 110 的同一面，控制单元 130 位于主板 110 与功率单元 120 相对的另一面，功率单元 120 与控制单元 130 分别位于主板 110 的两相对表面，亦即将各单元 120、130 分别放置于主板 110 的上下表面，控制单元 130 通过主板 110 中的导电贯孔 2310 电性连接引脚 140，单元之间的投影面积重合的部分至少占本单元投影面积的 1/3。显然，为了散热和厚度的限制，控制单元 130 设置于主板下表面，功率单元 120 设置于主板 110 上表面为佳。

很显然，如上各种实现方式，均可有效利用高度，兼顾电源变换的高效率和高功率压强，实现更高性能的电源模块，尤其是在服务器电源的应用场合中。

焊盘布置和实现

一个电源变换器的引脚有很多。涉及到变换器与系统连接的引脚如变换器功率输入输出引脚，与系统的通信引脚，及内部互联即功率单元及控制单元间相互连接的引脚等。由于引脚在本申请中为其他的定义，在此处，载板上元器件的引出脚称之为焊盘。图 24，从电流量上来分，通常分为功率焊盘和信号焊盘两大类。功率焊盘是指变换器功率电流流过的焊盘，通常为功率电路中元器件间进行电气连接，它由于流过的电流大，焊盘通常比较粗，也即焊盘的截面积比较大。而信号焊盘则为变换器中传递信号的焊盘，例如，控制单元中的控制电路通常通过信号焊盘传递控制信号给驱动电路以控制功率元器件的导通及关断。通常控制焊盘流过的电流较小，焊盘比较细，则无需过大截面积，其尺寸由工艺能力决定。

当电源变换器为一隔离的电路时(隔离通常由功率电路中的变压器来实

现)，也即其输入输出有隔离安规电压要求。所以，焊盘按位置可分为一次侧群焊盘(即位于变压器一次侧的焊盘)和二次侧群焊盘(即位于变压器二次侧的焊盘)。这两个群焊盘需要让开一定的距离以符合安规的要求，例如为当变换器的输入为 400V 时，由于需要绝缘 2000V 以上，每个群中任意一个焊盘与另一群中任意一焊盘间至少相距 4～8mm 间距；而当输入为 36～72V，通常需要满足的安规绝缘电压为 1500V，则间距为 1～4mm。而一次侧群，由于输入相对高压，电流较小，焊盘的截面积相对较小。二次侧群则由于电压低，电流大，焊盘截面积相对较大。如 48V 转 1V，电流差异 48 倍，如果用同样电流密度来定义焊盘体积的话，就会差 48 倍，二次侧群显然需要更多的位置摆放。

功率单元四周都可以摆放焊盘，如图 24 和图 25 所示。图 24，一次侧群焊盘 2410 和二次侧群焊盘 2420 各占功率单元的两边，且两边相互平行，一次侧群焊盘 2410 包括第一信号焊盘 2411 与第一功率焊盘 2412，第一功率焊盘 2412 的截面积大于第一信号焊盘 2411 的截面积，二次侧群焊盘 2420 包括第二信号焊盘 2421 与第二功率焊盘 2422，第二功率焊盘 2422 的截面积大于第二信号焊盘 2421 的截面积，第二功率焊盘 2422 的数量多于所述第一功率焊盘 2412 的数量。图 24 的方式适合输出电流较低的场合。图 25 则适合大电流输出的应用，一次侧群焊盘 2410 分布于单元的一条边上，二次侧群焊盘 2420 分布于单元的剩下三条边，并与一次侧群焊盘 2410 让开一个安规距离 d。当电流比较大，同一个电气极性，需要使用多个焊盘时，也即复用焊盘时，通常可以采用正负极交错排列，例如：Vo+、Vo-，以实现尽量低的焊盘感抗，以便在应用类似于 CPU 负载时，有更好的动态响应，减少主板的电容使用量。

在本申请中，引脚是与焊盘电性连接的。图 26 显示的是引脚与焊盘连接并实现各单元互联后的正视图。图 26 例举的引脚为表面贴装引脚。该 L 型的表面贴装引脚 2610 将各单元 120、130 进行电连接后，组成表面贴装引脚的电源变换器，设置于主板 110 之上。而改用 I 型引后，则可实现如图 27 的 I 型的直插引脚 2710 的电源变换器。图 28 显示的是该电源变换器组装过程。先将各单元 120、130 堆叠后，将各引脚 2710 分别焊接至各单元 120、130 的焊盘，组成相应的电源变换器。

图 29 则显示的是另一种方式。即各个单元 120、130 先拥有属于自己的引脚，均以表面贴装引脚，且同一个引脚上下表面均有表贴式垫片（SMD Pad）

2910，每一引脚 140 的两端具有表贴式垫片 2910 延伸至对应的单元 120、130 的上、下表面，使焊接牢固和减少垫片导电损耗。这样就可以将各单元通过 SMD 焊接流程组装在一起形成表面贴装引脚的电源变换器。图 30 显示的则是将最下方的单元（如：控制单元 130），直插引脚 3010 在单元的表面为表贴式引脚，下方则出直插式接脚,这样就可以组成直插引脚的电源变换器。具体而言，多个引脚 140、140’中具有至少一引脚 140 设置于控制单元 130 与功率单元 120 中最接近主板 110 的单元（如：控制单元 130）的侧边，至少一引脚 140 的一端具有直插引脚 3010 插设至主板 110 中，至少一引脚 140 的另一端具有表贴式垫片 2910 延伸至最接近主板 110 的单元的上表面；多个引脚 140、140’中每一其余引脚 140’的两端具有表贴式垫片 2910 延伸至功率单元 120 与控制单元 130 中其余单元（如：功率单元 120）中对应者的上、下表面。简言之，引脚 140’为表面贴装引脚，直插引脚 3010 配合表面贴装引脚实现功率单元 120/控制单元 130 与主板的 110 电性连接，且利于安装。于一实施例中，功率单元 120 包括主功率单元部分（如，较下方的功率单元 120）和次功率单元部分（如，较上方的功率单元 120），主功率单元部分的侧面分布焊盘 3340（绘示于图 34），次功率单元部分堆叠于主功率单元部分。图 31 显示的则是组装的过程。先将各单元 120、120 与各自的引脚 140 组装后，在将各单元 120、120 组装在一起。

图 32 则显示的是，控制单元与功率单元整合成第一单元 2010、第二单元 2020 与外置电感器 L，第一单元 2010 位于第二单元 2020 与主板 110 之间，引脚 140 的一端具有直插引脚 3010 插设至主板 110 中，引脚 140 的另一端具有表贴式垫片 2910 延伸至第一单元 2010 的上表面，第一单元 2010 的下表面设有表面贴装引脚 3210 去连接主板 110，在下方单元（即，第一单元 2010）的上表面进行一定的布线，实现堆叠在其上表面的多个单元之间的相互电连接。也可以在下方单元的下表面，出更多的表面贴装引脚 3210，实现其侧面和下表面同时出引脚，以更充分利用空间，特别是面积很小的场合，如小于 1/32 砖，以便有足够空间布置引脚。图 33 显示的是，引脚 140 的两端具有表贴式垫片 2910 延伸至第一单元 2010 的上、下表面，第一单元的下表面设有表面贴装引脚 3210 去连接主板 110，该电源变换器直插引脚和表面贴装引脚复用的方式，以满足某些场合需要功率焊盘以直插形式的需求。

如上，表面贴装引脚具体实现时，需要保证各引脚 140 的平整度以方便组装和客户使用。因此，以图 31 为例，在组装引脚之前，如果各单元 120、130 表面规则，将更有利于组装引脚。那么，可以在组装引脚 140 前，将各单元 120、130 用 Molding(塑封)、Embedded(埋入)等封装工艺包覆起来，形成有规则的表面，例如图 31 所示的平面，或者图 34 所示的凹部 3410，由于绝缘封料 3430 上设有配合引脚 140 安装的凹部 3410，更有利于空间的精细使用，再在其上安装表面贴装引脚。具体而言，控制单元与功率单元中任一者具有载板 3420 与绝缘封料 3430，绝缘封料 3430 形成于载板 3420 的两相对表面，载板 3420 的侧面具有焊盘 3440，焊盘 3440 上的焊料 3450 焊接至引脚 140。绝缘封料 3430 的上、下表面的边缘具有凹部 3410，引脚 140 的两端具有表贴式垫片 2910 延伸至上、下表面的凹部 3410，凹部 3410 上具有胶料 3460 黏着于表贴式垫片 2910。

图 34 所示的单元可为上述的功率单元与/或控制单元，焊盘 3440 分布于功率单元的侧面和控制单元的侧面，引脚 140 与焊盘 3440 电性连接。引脚 140 为表面贴装引脚，分布于功率单元和控制单元的外表面并与焊盘 3440 电性连接。焊盘 3440’还分布于功率单元与焊盘 3440 所在侧面垂直的面，虽然图 34 中焊盘 3440’只分布于下表面，但此不限制本发明，于一实施例，焊盘分布于功率单元 120 的侧面和控制单元 130 的上下表面，引脚 140 与焊盘 3440 电性连接。

表面贴装引脚可以安装在单元的各个面上，但为得到更好的散热效果及使模块整体体积更小，以上例举的为焊盘位于各单元中载板的侧面，与表面贴装引脚进行焊接等工艺以便电连接单元中器件的引出脚和控制信号引出脚。然而在有些特殊情况下，如图 33，第一单元 2010 的焊盘也可在其第二单元 2020 和电感 L 堆叠的表面制作焊盘，通过引脚实现第一单元 2010 与第二单元 2020 和电感 L 之间的典型连接。引脚与焊盘的焊点之外的接触面，则可以使用胶水等工艺，将贴式引脚粘结于各单元的表面，以加强机械强度，提升可靠性。

散热处理

各单元堆叠成模块后，相比较于原先独立摆放设计的方式，散热途径发生了变化。

如图 35 所示，堆叠后上下各单元之间可以根据需要，留出足够的间隙，

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作为风道使用，换言之，控制单元 130 与功率单元 120 中任两相邻单元之间具有间隙以作为风道 3510。上下单元间距即风道厚度应该在 1～5mm 之间，少则散热效果不好，多则占用更多空间从而使模块体积变大。这样就可以尽量使用各单元的自身表面进行热交换。为达到有效散热，风道中的风速应该在 0.5 米/秒以上。

在很多应用中，可能较难给图 35 中的风道 3510 提供足够风速。因此，还是希望将热传递到整体堆叠后的各个表面。为更好的实现热均匀，可以在单元间空隙处填充导热绝缘胶，如图 36 所示，控制单元 130 与功率单元 120 中任两相邻单元之间的间隙被导热绝缘胶 3610 给填充，功率单元 120 之间、功率单元 120 与控制单元 130 之间填充有导热绝缘胶 3610。为有效实现导热能力，该导热绝缘胶的导热系数应当大于 1W/m.k。也可以在本需互联部分填充金属板，如铜板，以得到更好效果。而填充的面积该在该表面的 30%以上。当然，导热绝缘胶及金属板可以一起填充。

如图 37 所示，功率单元 120 中设有横向导热载板 3730（如：PCB），引脚 140 的两端具有引脚延伸层 3710 延伸至功率单元 120 与控制单元 130 中对应者的上、下表面，该上、下表面中至少一面被引脚延伸层 3710 占据 30%以上的面积，位于各单元下表面的引脚延伸层 3710 下方具有导电焊接材料 3720，换言之，功率单元 120 与控制单元 130 电性连接的引脚之间以及功率单元 120 与功率单元 120 电性连接的引脚之间填充有导电焊接材料 3720，导电焊接材料 3720 只在需要互联的地方进行焊接，各单元间电连接是可以通过此焊接方式达成的。焊接料的导热系数通常足够高。因此，可以将各表面贴装引脚的表面积增大，从而实现单元间隙间更多的金属填充，以实现热均匀。为达到有效散热，引脚的面积应当占该表面的 30%以上，举例而言，表面贴装引脚覆盖功率单元 30%以上外表面积，从而为高发热的功率单元进行有效率的散热。

此外，显然，各单元的热越均匀，各散热手段就越有效。而实际上，各单元的热点无法达到理想的均匀分布，因此，需要具备更好的热扩散能力。各单元中的电信号传递载板，通常含有导热导电的良导体，如铜或者银等。如果在设计时，让载板的金属含量尽量高，则有利于热的扩散，特别是横向扩散。因此，在本发明中，热比较集中的单元中的载板，金属含量应该在 10%以上。同理，如图 22-5，客户的电信号载板，如果金属含量也在 10%以上，那么有利

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于将电源变换器传递给它的热扩散到更大的面积，实现更好散热。

当然，高横向导热载板更有利于横向热扩散。各单元特别是损耗较大，发热比较明显的单元，例如功率单元，其覆盖/包覆材料如果可以是高导热绝缘胶，则会有利于上下垂直的热扩散。如使用导热系数在 1W/m.k 以上的覆盖/包覆材料。可以在包覆材料中添加陶瓷颗粒来实现。如添加陶瓷颗粒的塑封料。

如图 38，可以通过将各引脚 140 在侧面和上表面，扩大占用的面积，来实现更好的热交换能力。其覆盖面积，至少有一面占其所在单元所在面的 30%以上，尤以 50%以上为佳。此外，为了具备更好的扩散能力，引脚的平均厚度，应当在 0.2mm 以上，尤以 0.3mm 以上为佳。

图 39 和 40 则显示散热单元的安装方式。如图 39，电绝缘的散热单元 3910 设置在功率单元 120 上，功率单元 120 设置在控制单元 130 上，控制单元 130 设置在主板 110 上；或者，如图 40，电绝缘的散热单元 4010 设置在功率单元 120 与控制单元 130 的侧边。可以安装在组装后模块的上表面也可以安装在侧面。为避免影响电性能，该散热单元可以为电绝缘材料，如陶瓷。或者为导电材料，如铝、铜、石墨时，需要与引脚间有导热电绝缘材料，如陶瓷片等。散热单元均安装于焊盘或者引脚组合上方。为保证散热效果，散热单元与焊盘或者引脚组合之间的热阻应当小于 5 摄氏度/瓦。散热单元与焊盘或者引脚组合之间有绝缘材料。

其他优化实施例

在上述各实施例中，曾提到，可以通过多个功率单元堆叠来实现更大功率。这些功率单元通常会各自使用工作状态类似的磁性元件，如变压器或者电感。如图 41，功率单元 120 的数量为多个且堆叠于控制单元 130 上，每一功率单元 120 中均设有磁芯（Core）4110 及其绕组（Winding）4120，换言之，各磁性元件拥有类似的绕组和类似的磁芯。而实际上，其堆叠接触部位的两个横向柱中的磁通是有机会量相当而方向相反的。因此，可以用图 42 的方法，即功率单元 120 各包括一平面变压器，两个平面变压器共用一个磁芯 4210，这样就可以去掉堆叠接触部位的横向柱，既明显降低了高度，又减少了磁芯损耗，实现了效率和功率密度的双丰收。

更近一步的优化如图 43 所示。由于磁性元件通常有气隙 4320，而气隙 4320 漏出的磁通通常会对附近的导体进行感应加热而产生损耗。可以通过在堆叠时

共用磁芯 4310，磁芯 4310 的气隙 4320 设置于功率单元 120 之间的堆叠间隙 4330，就可以将气隙尽量避开导体，减少损耗。

以上所举实施例，功率单元与控制单元上下堆叠形成电源模块。事实上，该电源模块翻转 90 度后，即变成功率单元与控制单元左右堆叠，通过引脚进行彼此间以及彼此与主板间的电气连接，这种结构也能够得到很好的应用。因此，本发明功率单元与控制单元间不仅可以上下堆叠还可以在水平方向上进行左右堆叠。

综上，通过本发明所揭露的 Quasi-Cascade 器件、驱动优化、应用优化及封装优化，可用以提升电源变换器功率密度或者效率，可以获得与现有技术相比，更佳的电性能，高频性能与更高的可靠性。其可充分挖取器件的特性，采用封装方案后使用方便，非常有利于提高变换器功率密度或者效率。而本发明给出的具体驱动、应用、封装的实施方法，也非常可行有效。本发明非常适合用以提升电源变换器的整体性能和性价比。

虽然本发明已以实施方式揭露如上，然其并非用以限定本发明，任何熟悉此技艺者，在不脱离本发明的精神和范围内，当可作各种的更动与润饰，因此本发明的保护范围当视所附的权利要求书所界定的范围为准。

IPR2024-00715 EX. 2005

说 明 书 附 图 TWLB4955-14P1

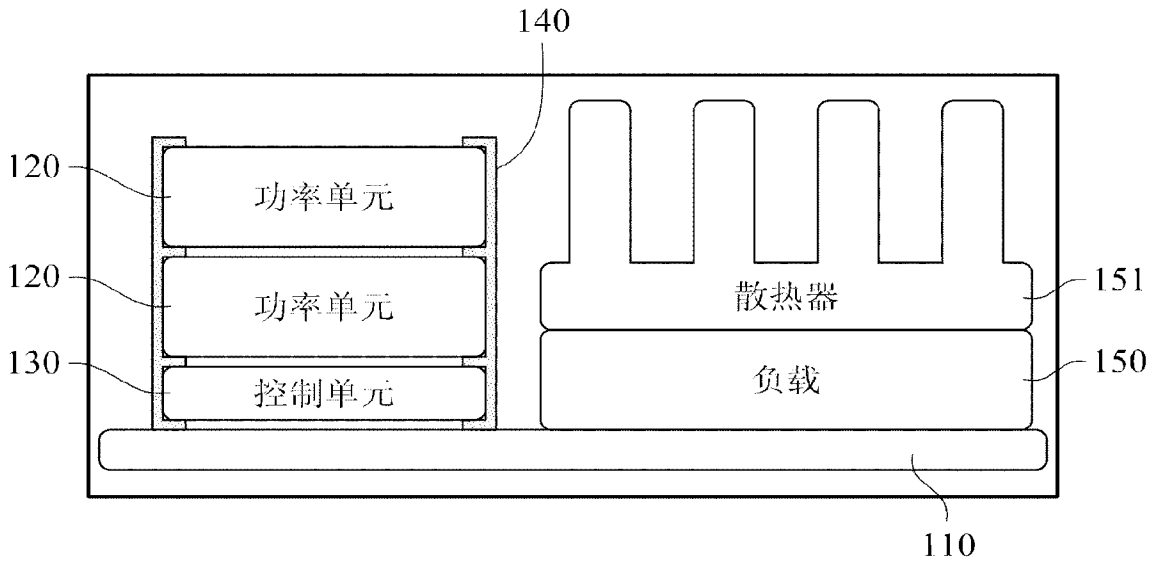


图 1

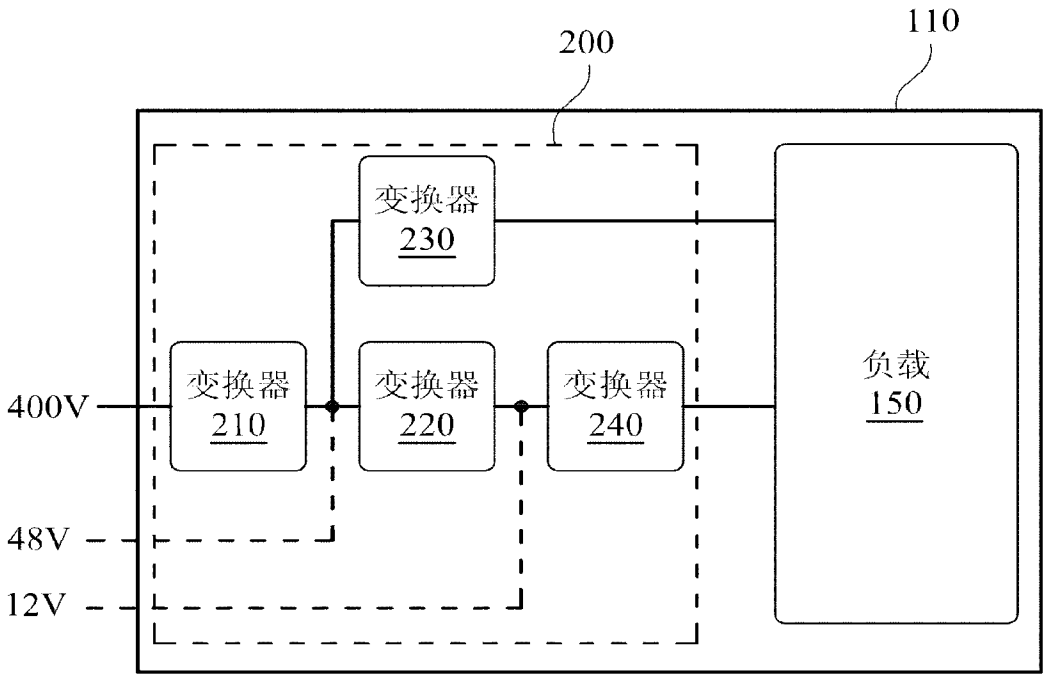


图 2

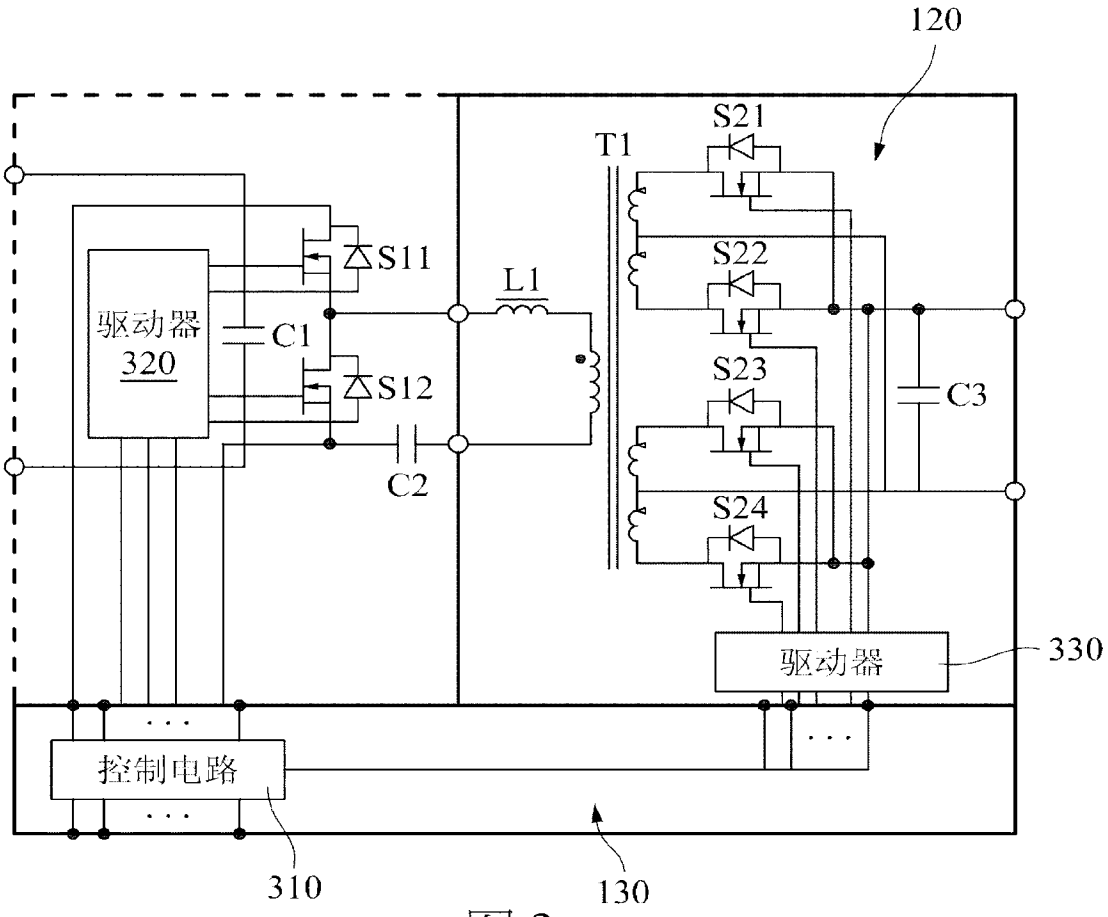

120
S21
T1
S11
L1
S22
驱动器
320
C1
S12
S23
C3
C2
S24
驱动器
330
控制电路
310
130

图 3

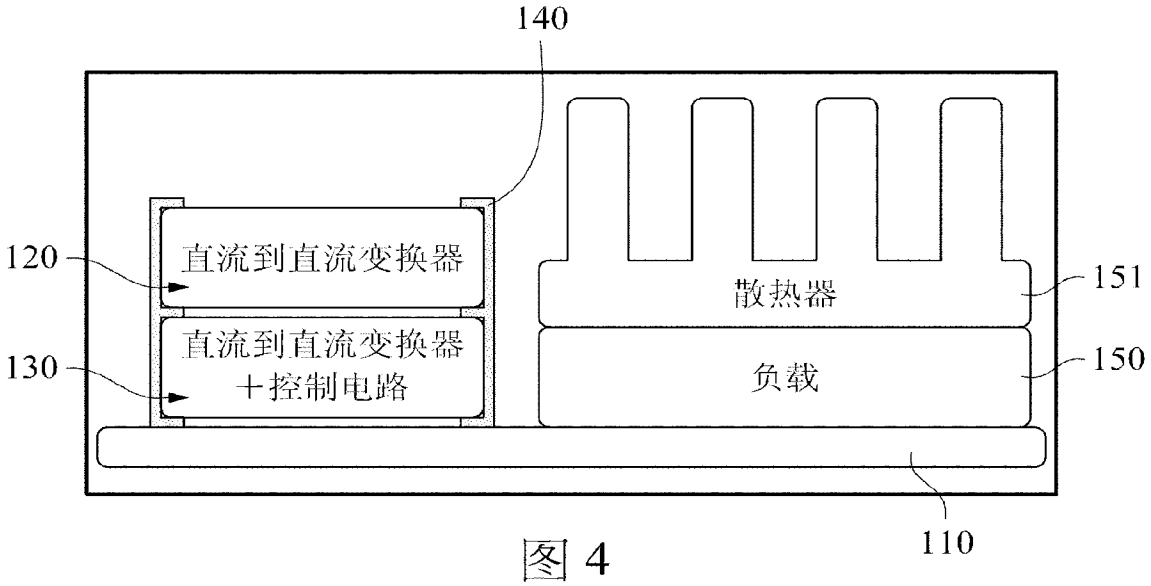

140
120
直流到直流变换器
散热器
151
直流到直流变换器
+控制电路
130
负载
150
110

图 4

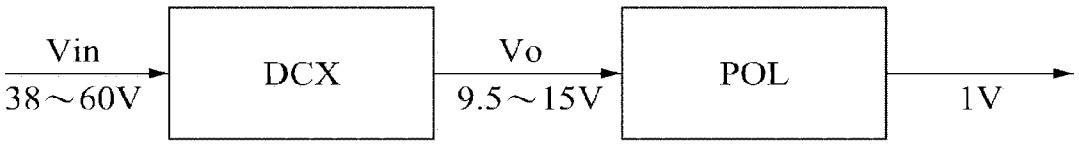

Vin
38～60V
DCX
Vo
9.5～15V
POL
1V

图 5

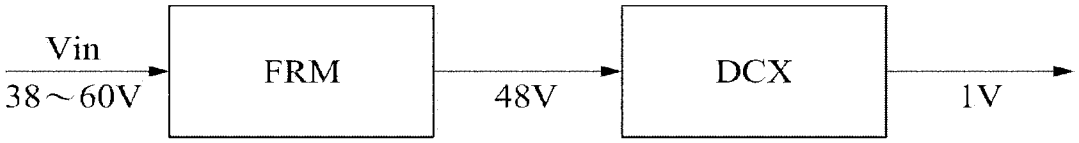

Vin
38～60V
FRM
48V
DCX
1V

图 6

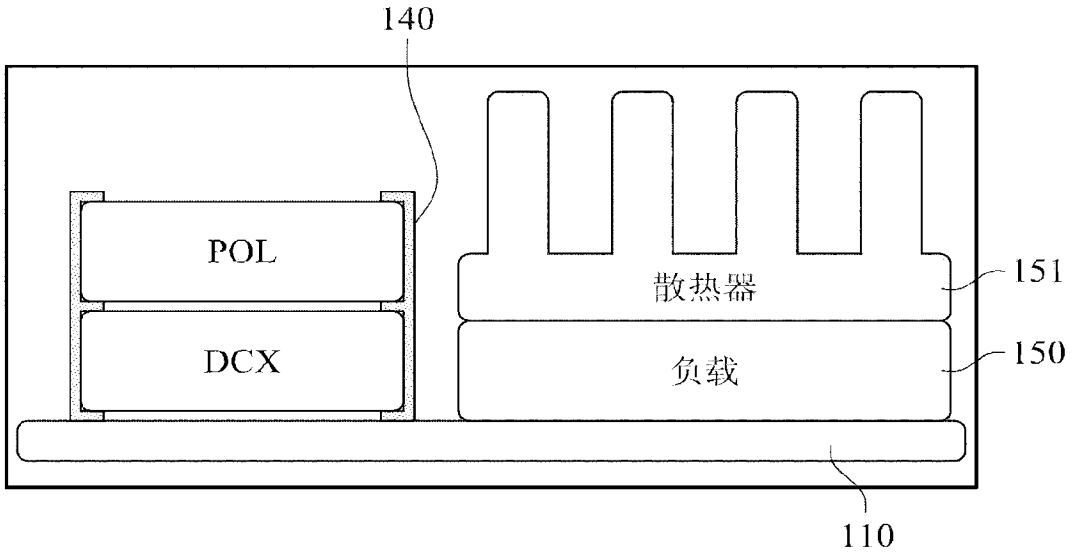

140
POL
DCX
散热器
负载
151
150
110

图 7

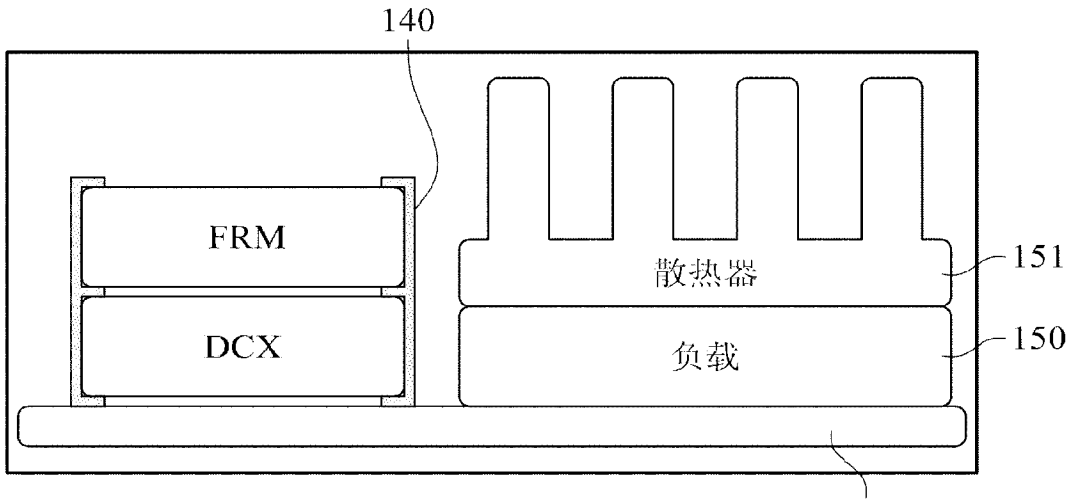

140
FRM
DCX
散热器
负载
151
150
110

图 8

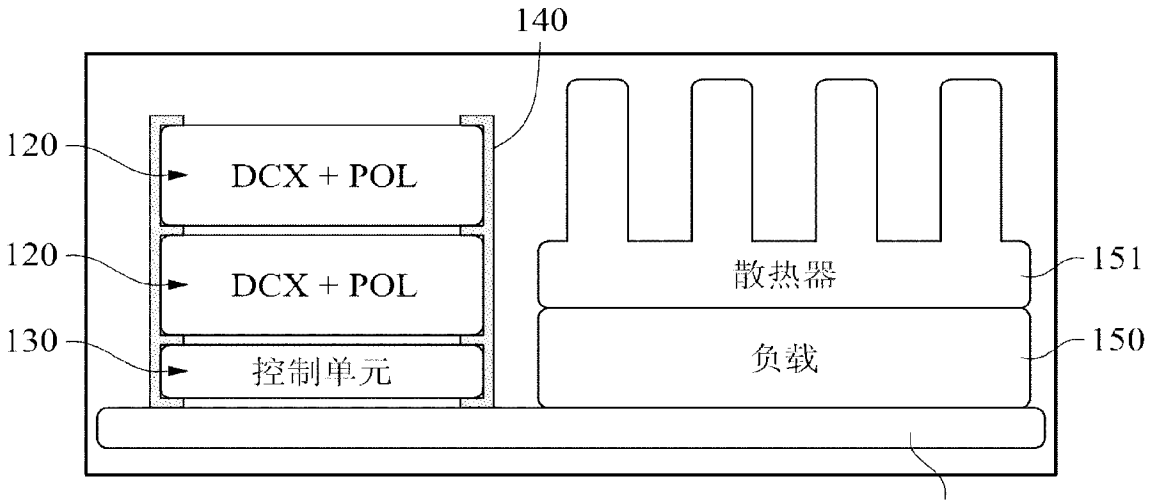

140
120
DCX + POL
120
DCX + POL
130
控制单元
散热器
负载
151
150
110

图 9

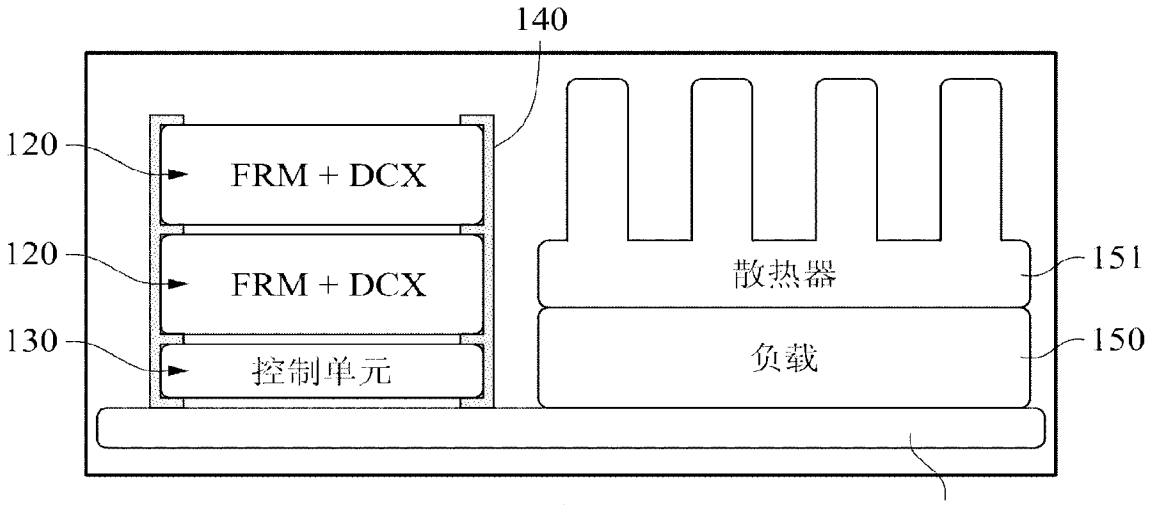

140
120
FRM + DCX
120
FRM + DCX
130
控制单元
散热器
负载
151
150
110

图 10

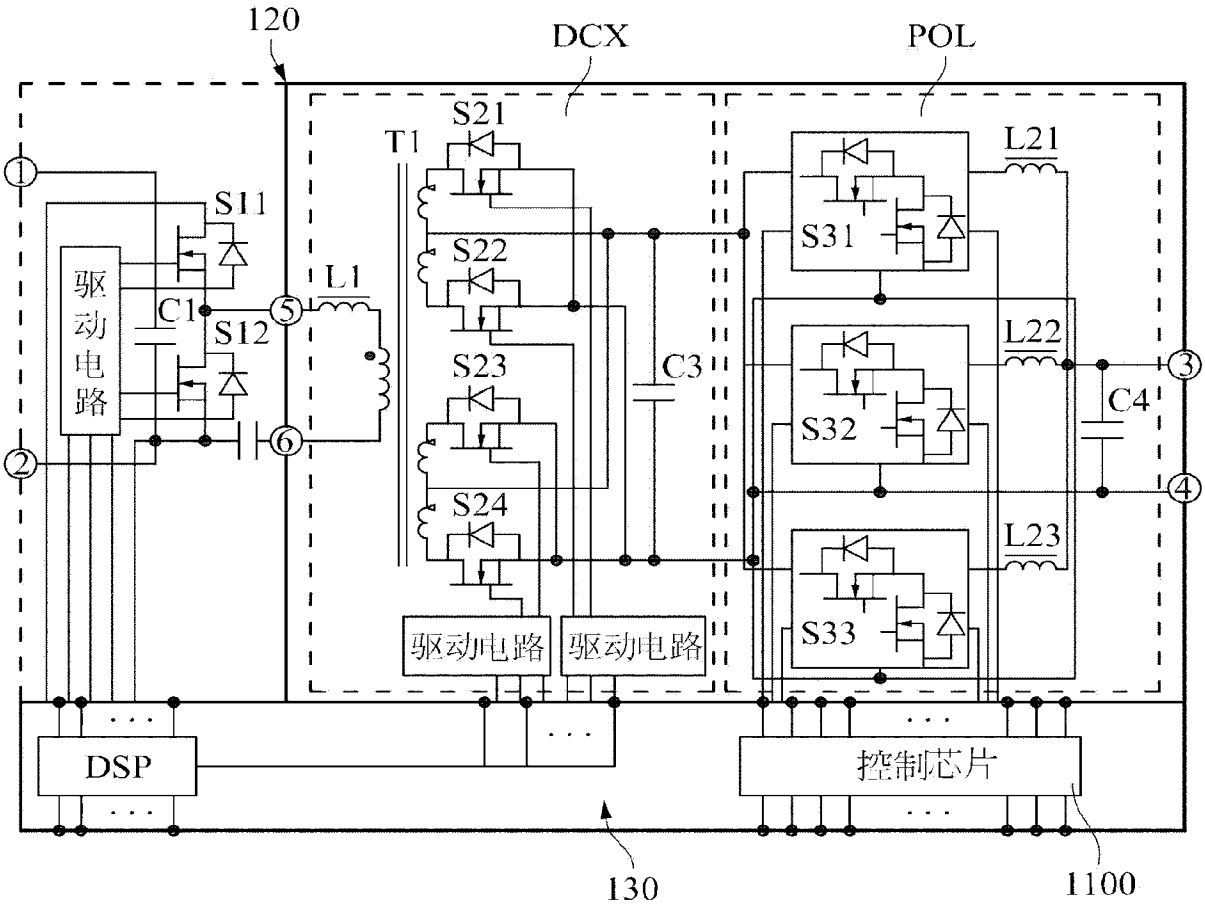

120
DCX
POL
S21
T1
L21
S11
S31
驱动电路
C1
S12
L1
S22
L22
S23
C3
C4
S32
S24
L23
S33
驱动电路
驱动电路
DSP
控制芯片
130
1100

图 11

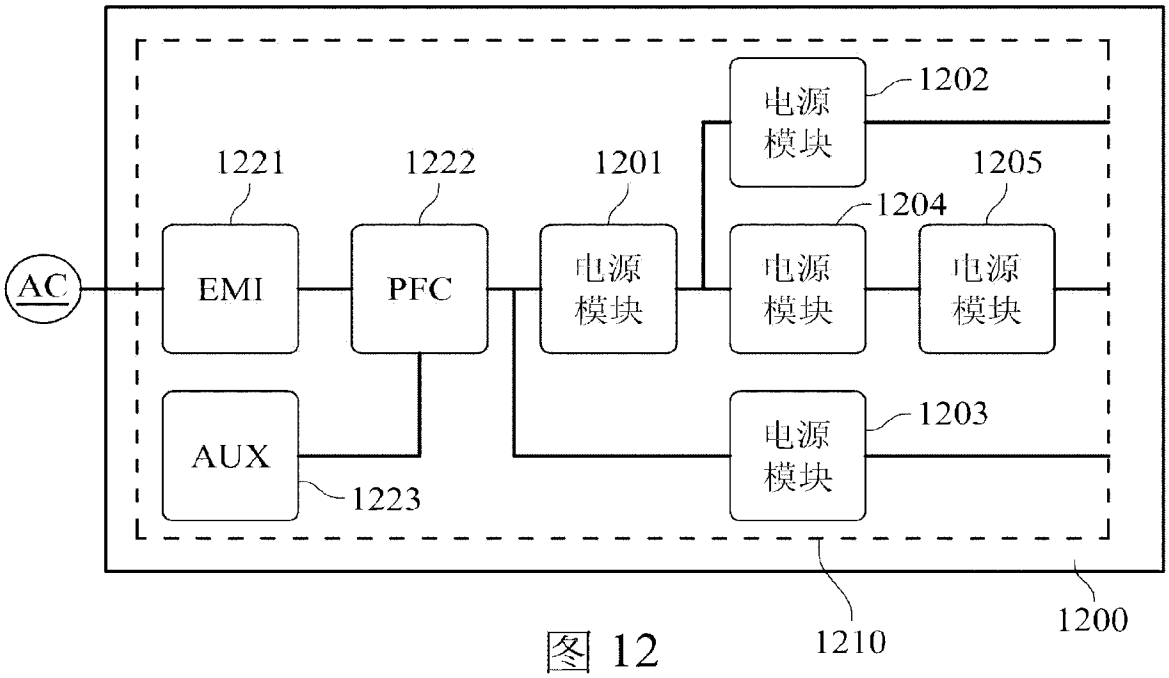

电源模块
1202
1221
1222
1201
1205
1204
AC
EMI
PFC
电源模块
电源模块
电源模块
AUX
电源模块
1203
1223
1210
1200

图 12

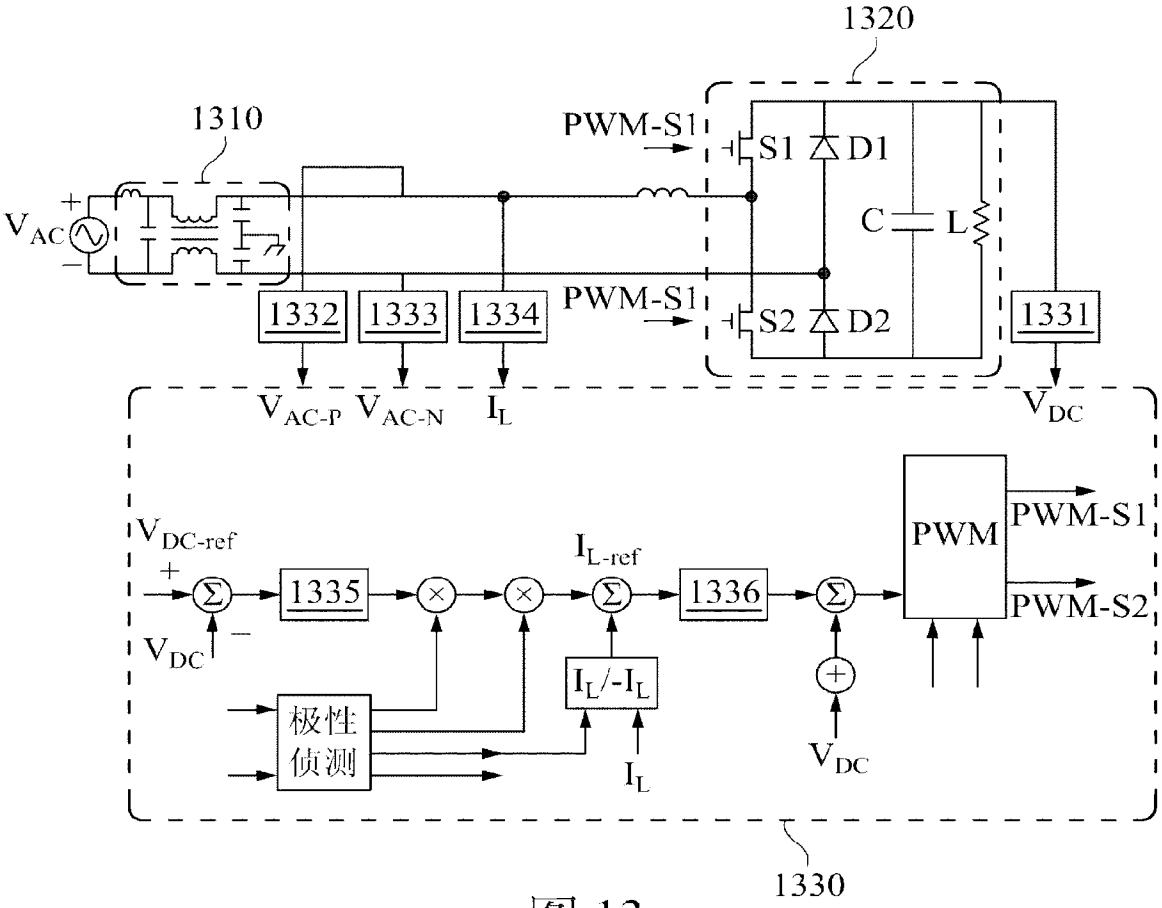

1320
1310
PWM-S1
S1
D1
C
L
V_{AC}
PWM-S1
S2
D2
1332
1333
1334
1331
V_{AC-P}
V_{AC-N}
I_L
V_{DC}
V_{DC-ref}
I_{L-ref}
1335
1336
PWM
PWM-S1
PWM-S2
V_{DC}
极性
侦测
$I_L/-I_L$
I_L
V_{DC}
1330

图 13

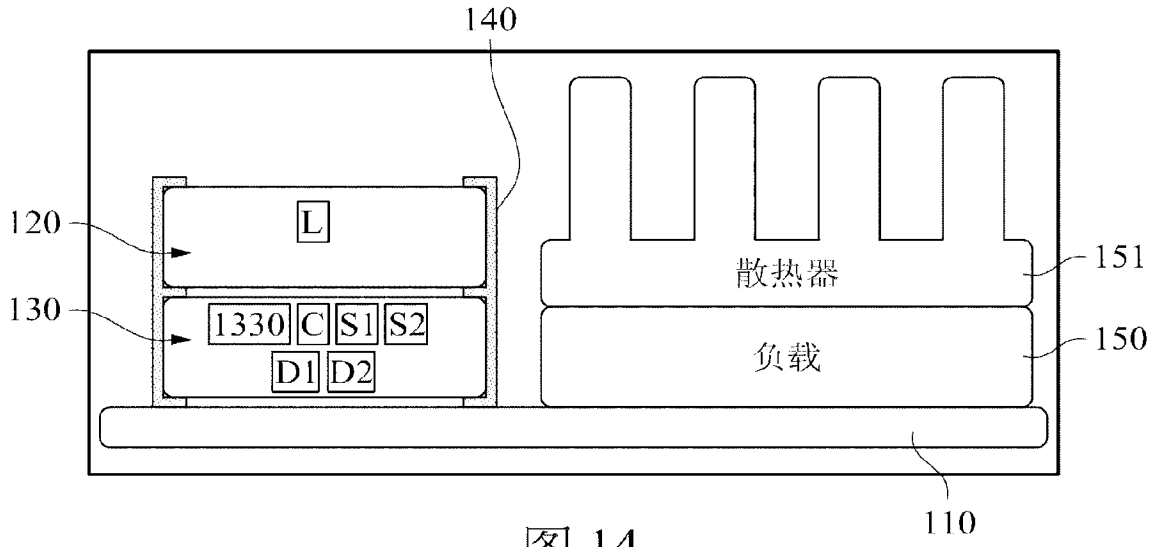

140
120
L
130
1330
C
S1
S2
D1
D2
散热器
151
负载
150
110

图 14

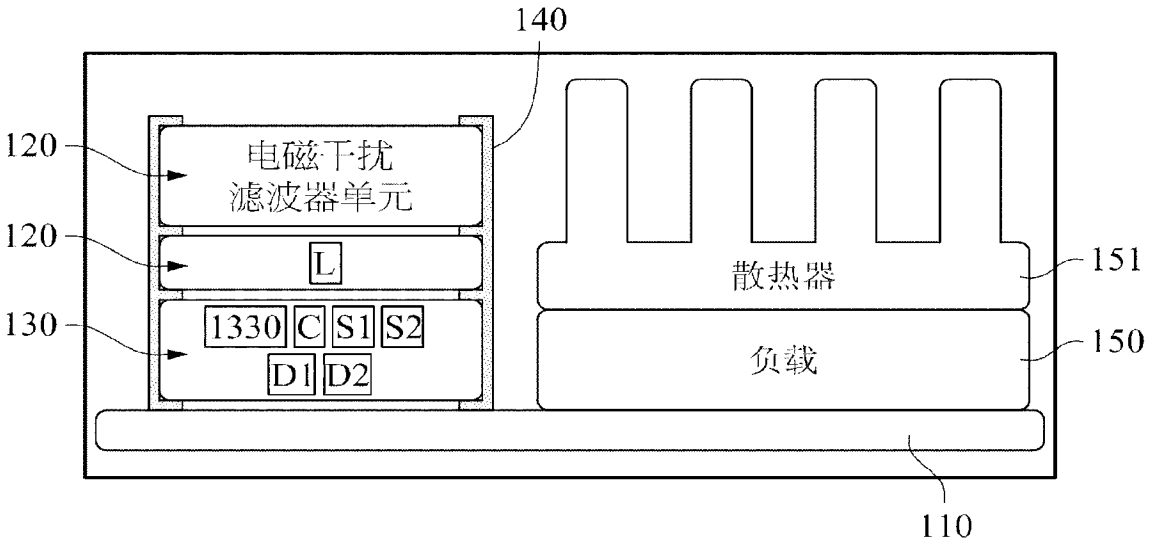

140
120
电磁干扰
滤波器单元
120
L
130
1330
C
S1
S2
D1
D2
散热器
151
负载
150
110

图 15

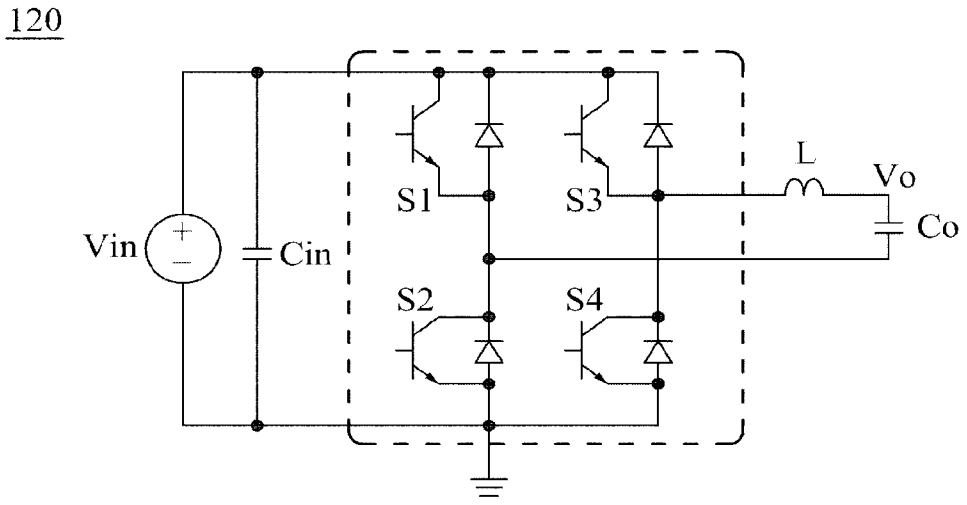

120
Vin
Cin
S1
S3
S2
S4
L
Vo
Co

图 16

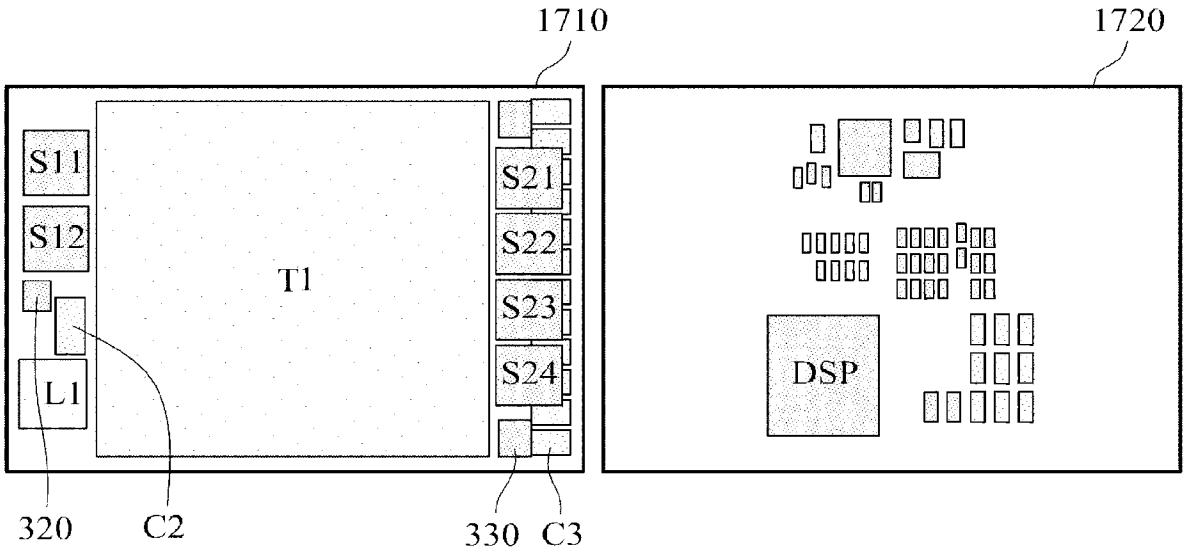

1710
1720
S11
S12
T1
L1
S21
S22
S23
S24
DSP
320
C2
330
C3

图 17

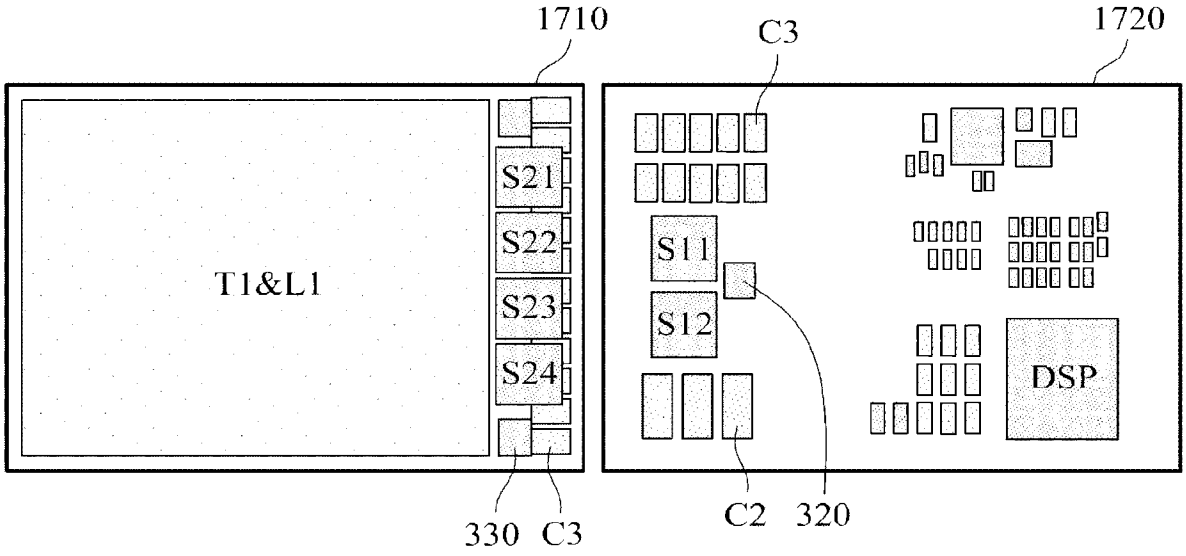

1710
C3
1720
T1&L1
S21
S22
S23
S24
S11
S12
DSP
330
C3
C2
320

图 18

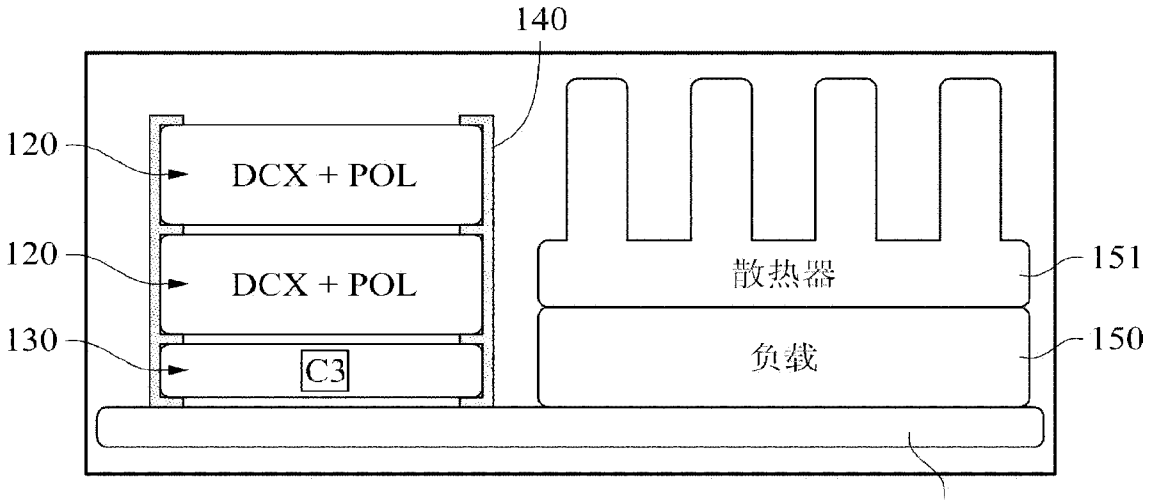

140
120
DCX + POL
120
DCX + POL
130
C3
散热器
151
负载
150
110

图 19

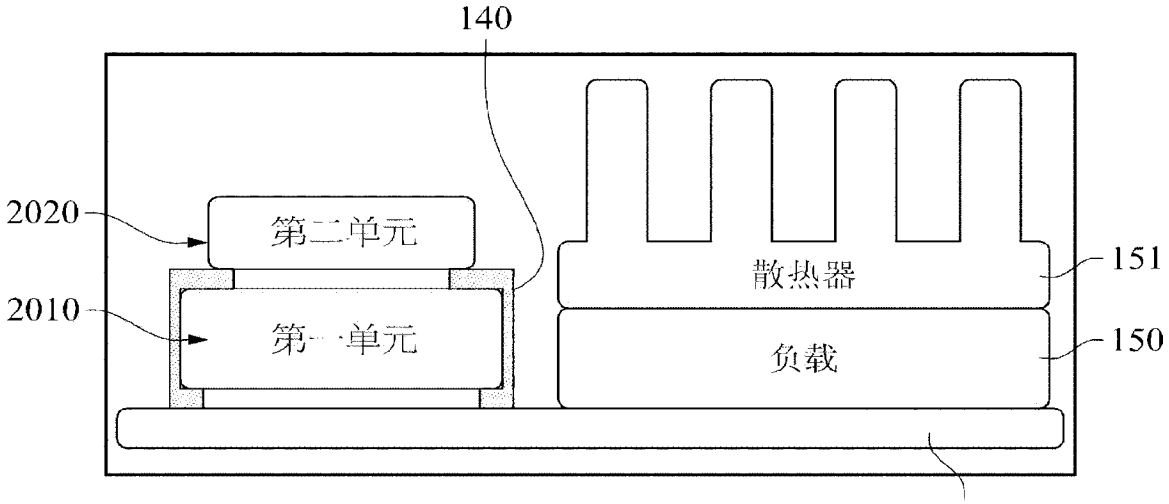

140
2020
第二单元
2010
第一单元
散热器
151
负载
150
110

图 20

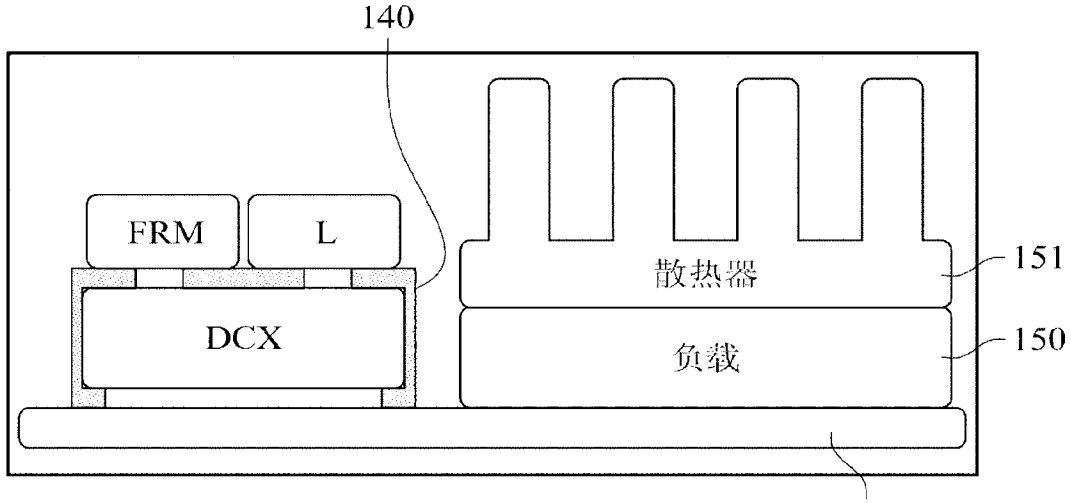

140
FRM
L
DCX
散热器
151
负载
150
110

图 21

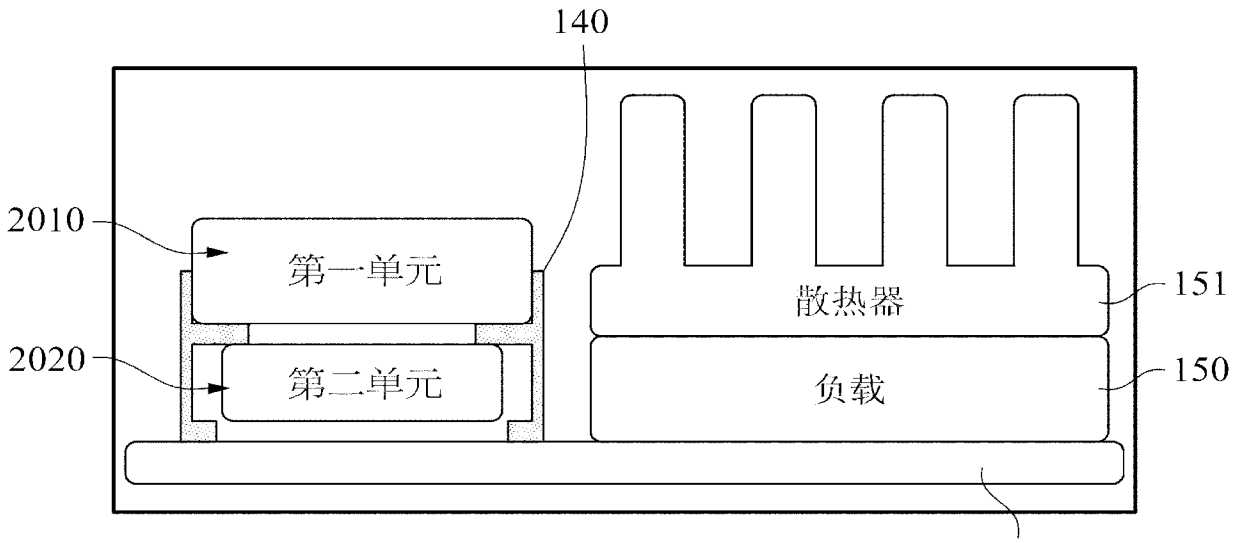

140
2010
第一单元
2020
第二单元
散热器
151
负载
150
110

图 22

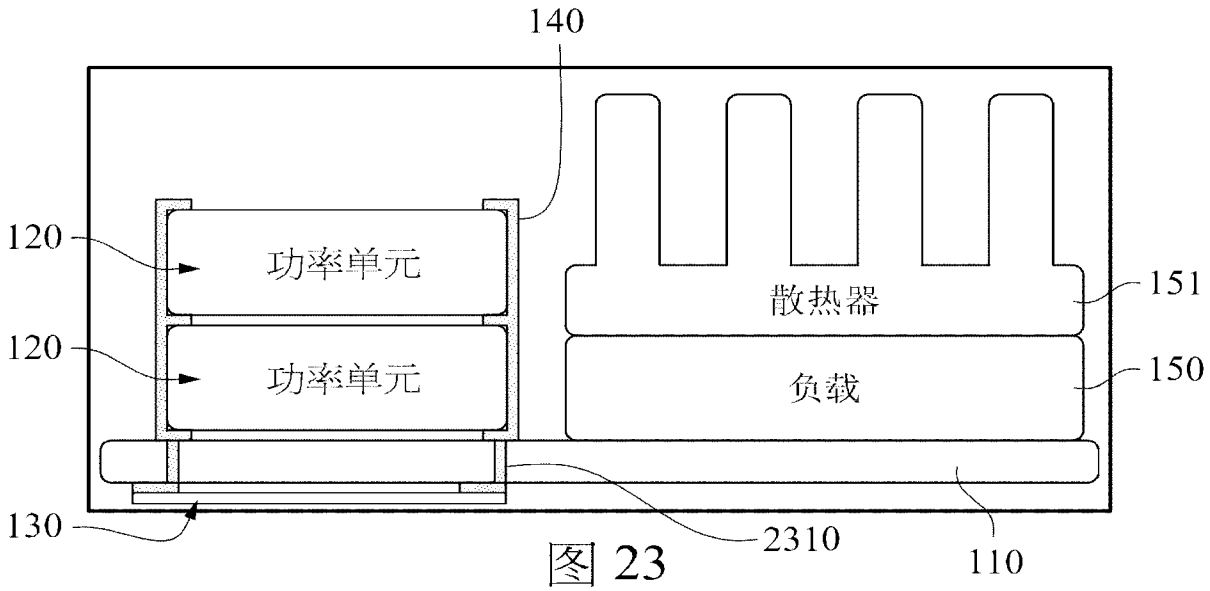

140
120
功率单元
120
功率单元
散热器
151
负载
150
130
2310
110

图 23

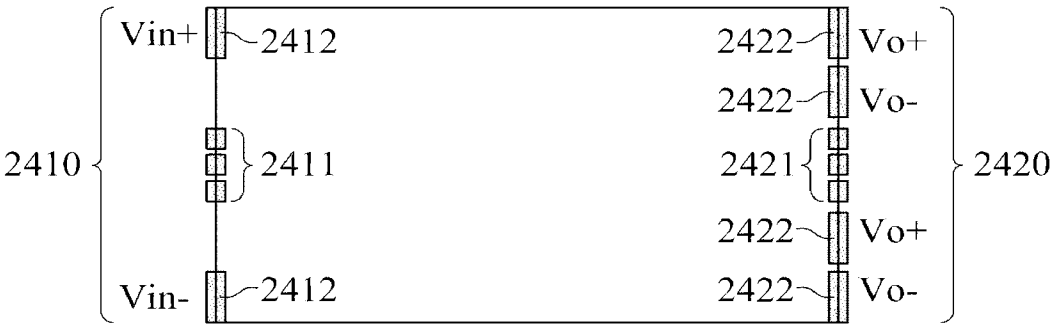

Vin+
2412
2410
2411
Vin-
2412
2422
Vo+
2422
Vo-
2421
2420
2422
Vo+
2422
Vo-

图 24

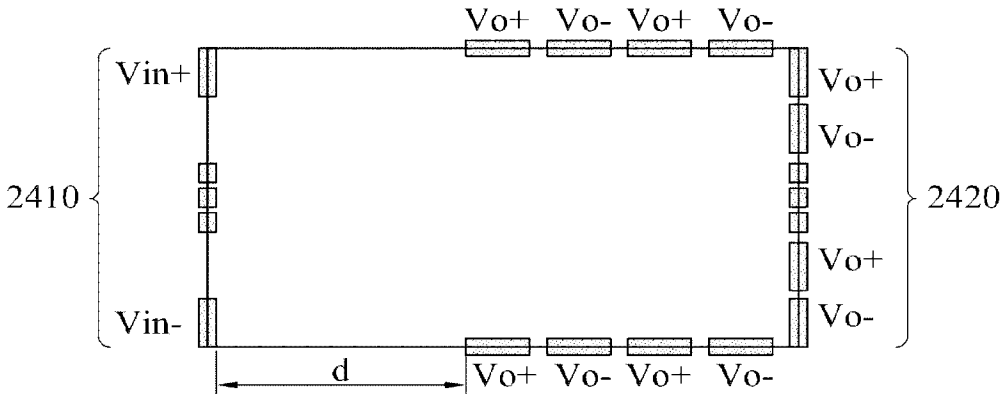

Vo+ Vo- Vo+ Vo-
Vin+
Vo+
Vo-
2410
2420
Vo+
Vo-
Vin-
d
Vo+ Vo- Vo+ Vo-

图 25

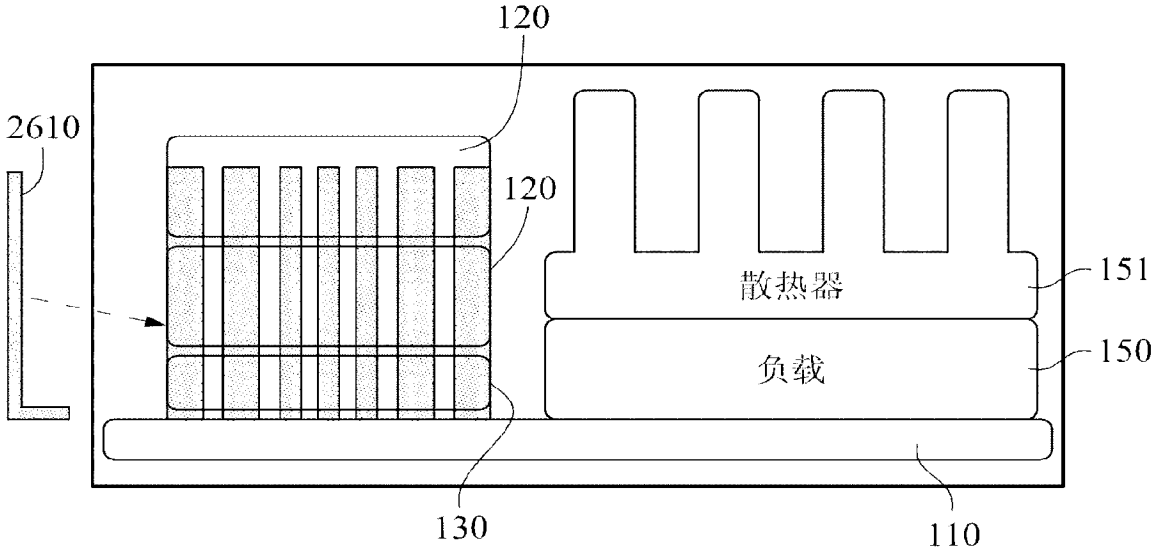

120
2610
120
散热器
151
负载
150
130
110

图 26

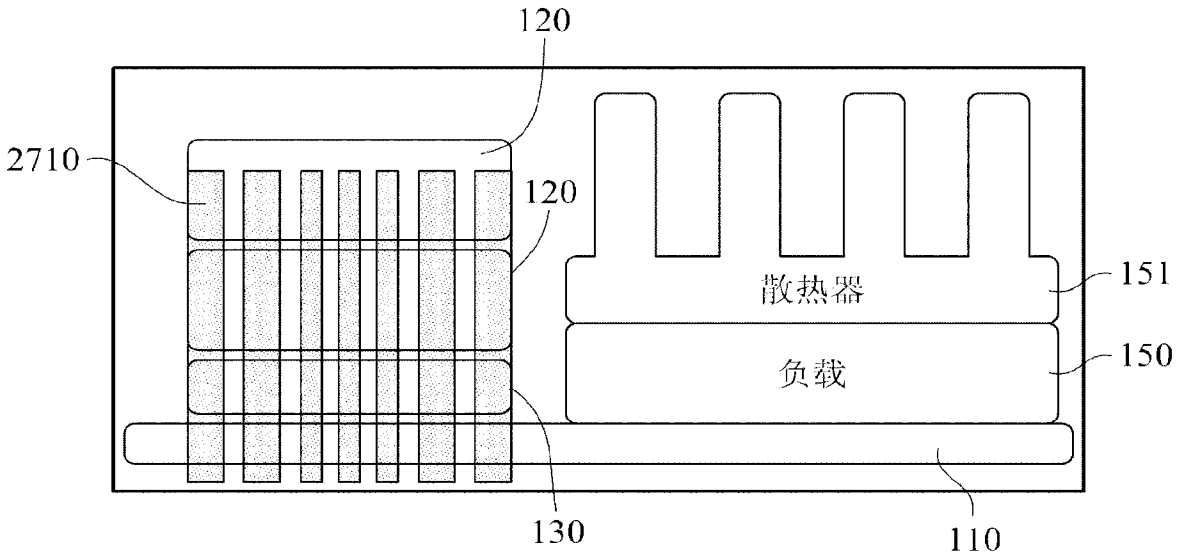

120
2710
120
散热器
151
负载
150
130
110

图 27

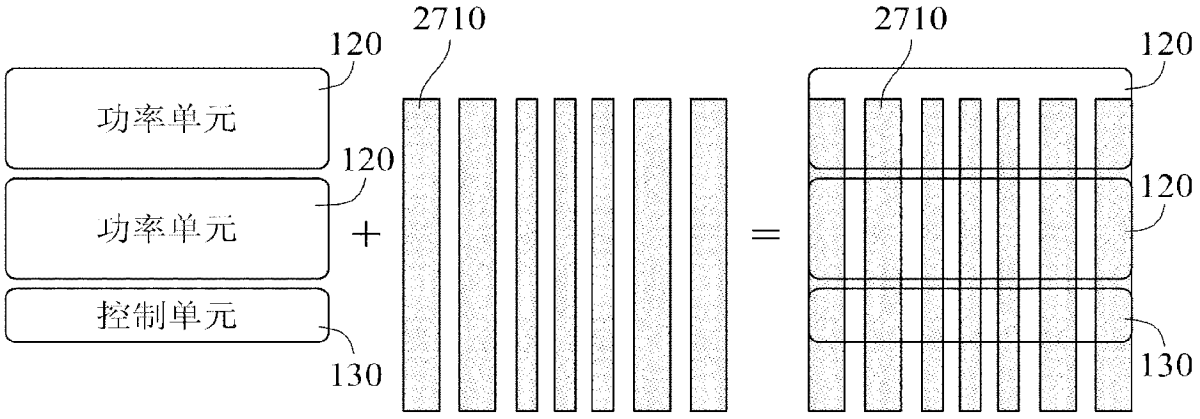

120
2710
功率单元
120
功率单元
+
控制单元
130
=
2710
120
120
130

图 28

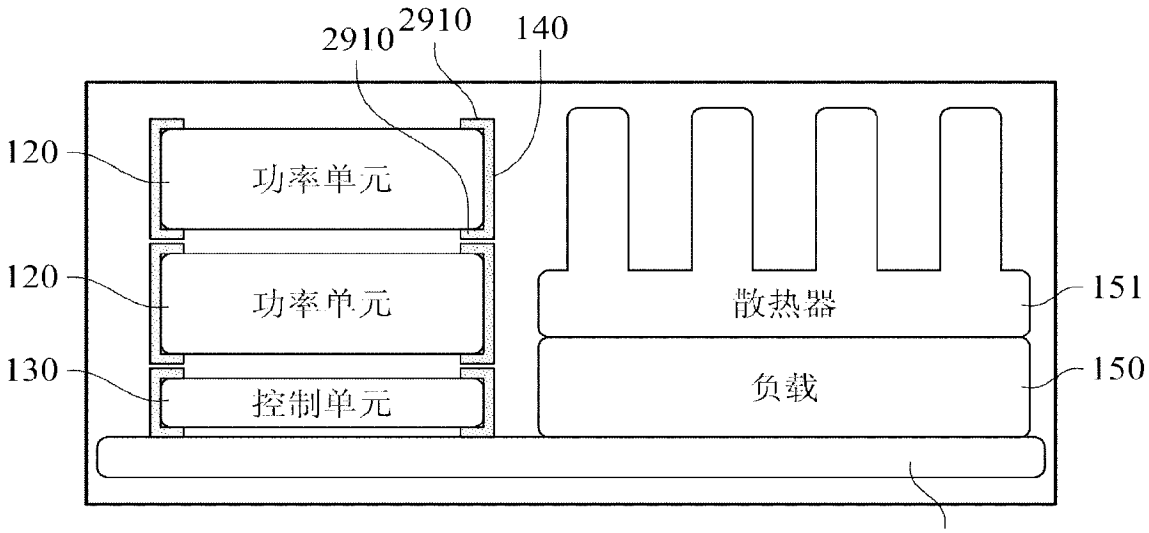

2910
2910
140
120
功率单元
120
功率单元
130
控制单元
散热器
151
负载
150
110

图 29

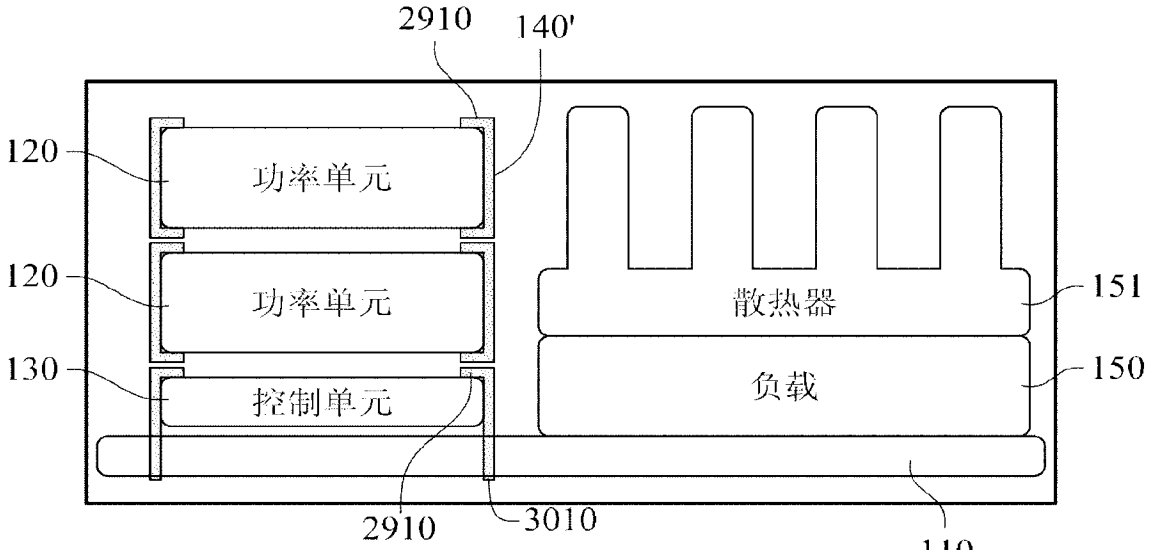

2910
140'
120
功率单元
120
功率单元
130
控制单元
散热器
151
负载
150
2910
3010
110

图 30

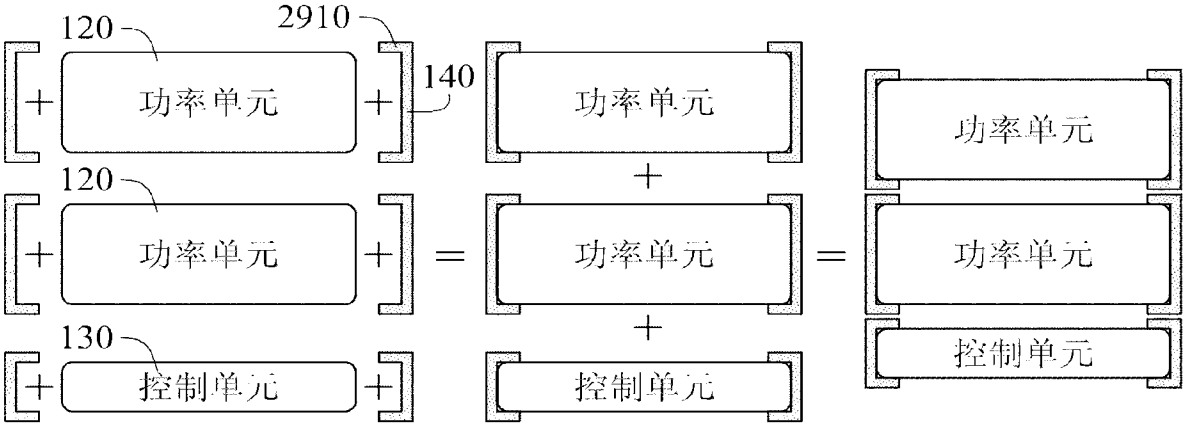

120
2910
140
功率单元
120
功率单元
130
控制单元
功率单元
功率单元
控制单元
功率单元
功率单元
控制单元

图 31

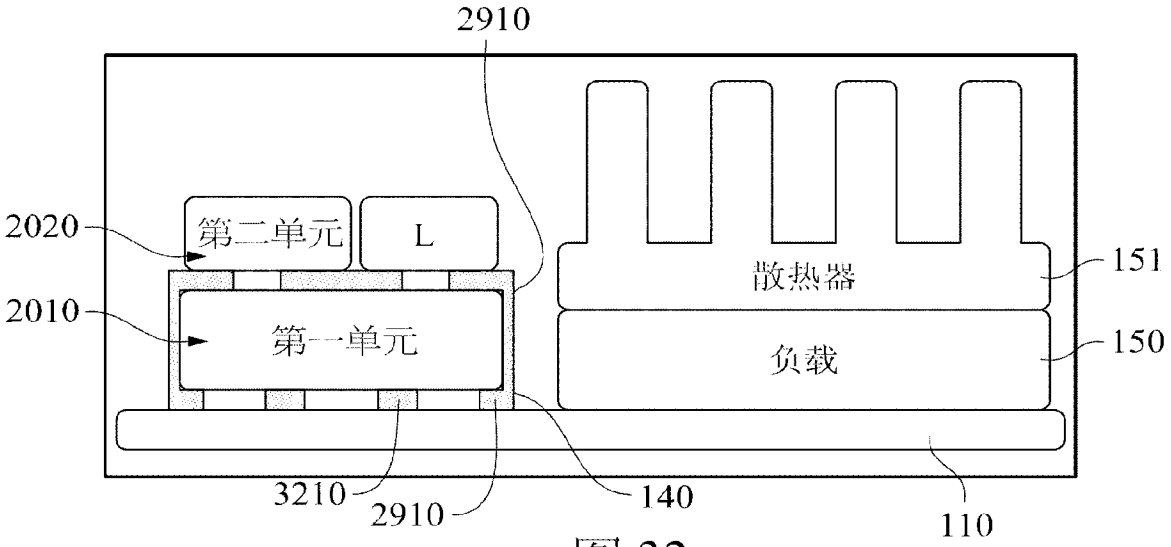

2910
2020
第二单元
L
2010
第一单元
散热器
151
负载
150
3210
2910
140
110

图 32

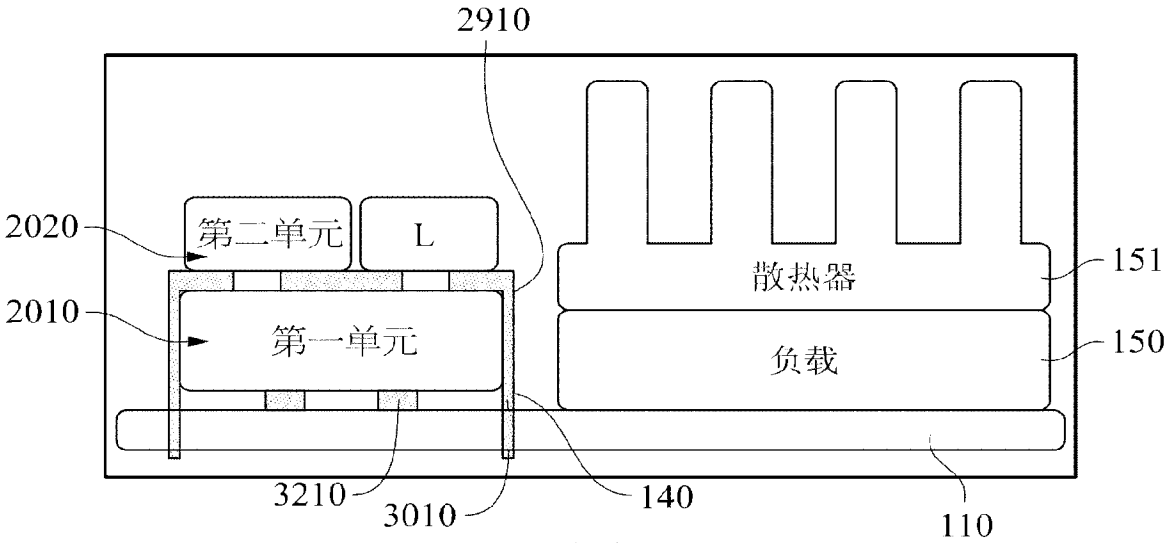

2910
2020
第二单元
L
2010
第一单元
散热器
151
负载
150
3210
3010
140
110

图 33

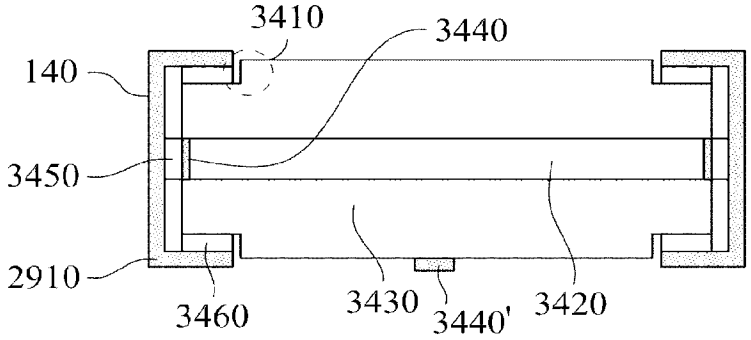

3410
3440
140
3450
2910
3460
3430
3440'
3420

图 34

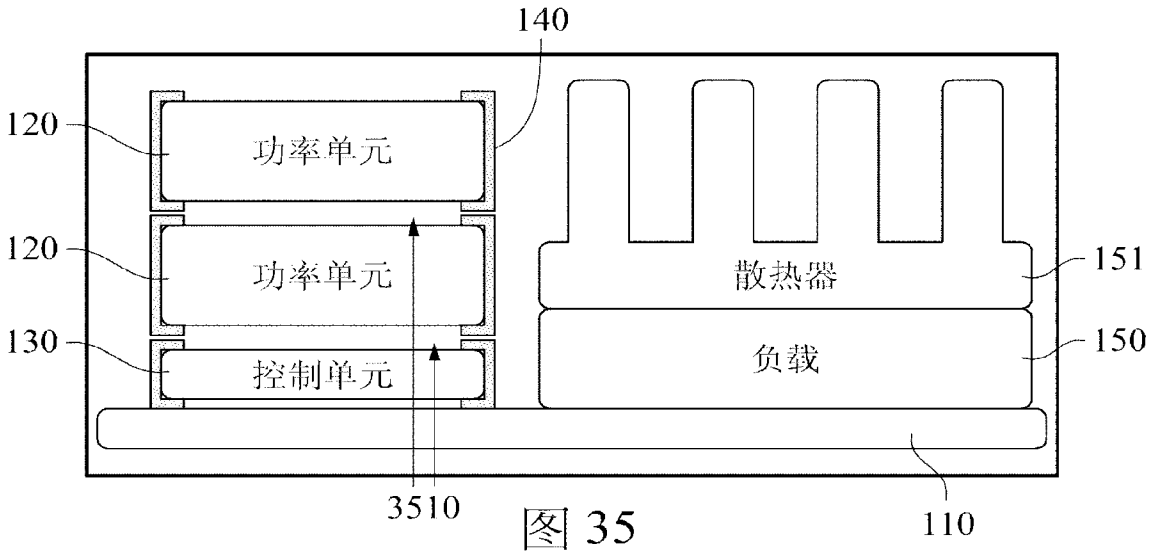

140
120
功率单元
120
功率单元
130
控制单元
散热器
151
负载
150
3510
110

图 35

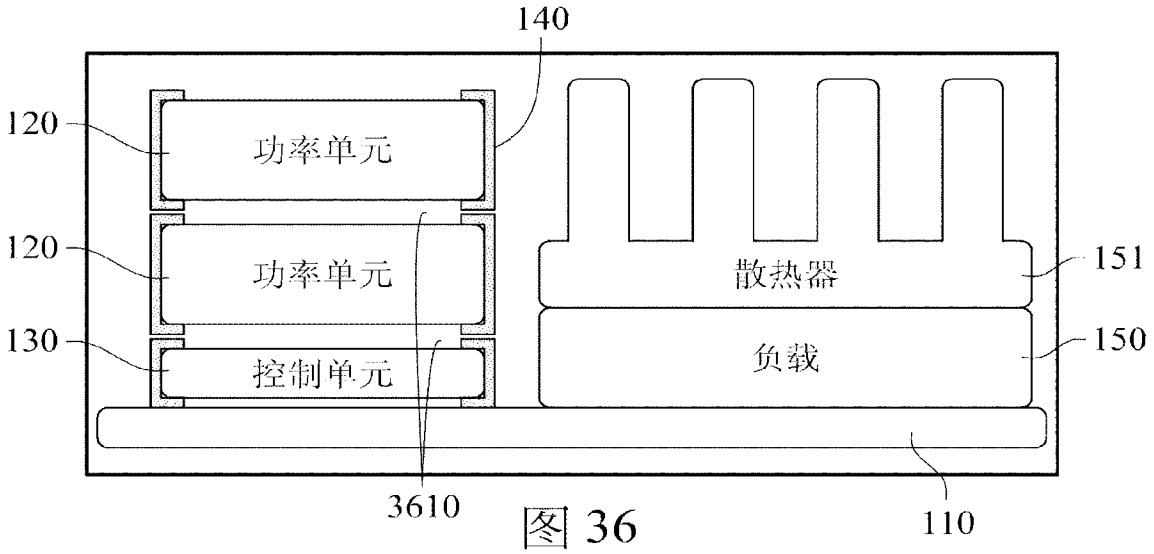

140
120
功率单元
120
功率单元
130
控制单元
散热器
151
负载
150
3610
110

图 36

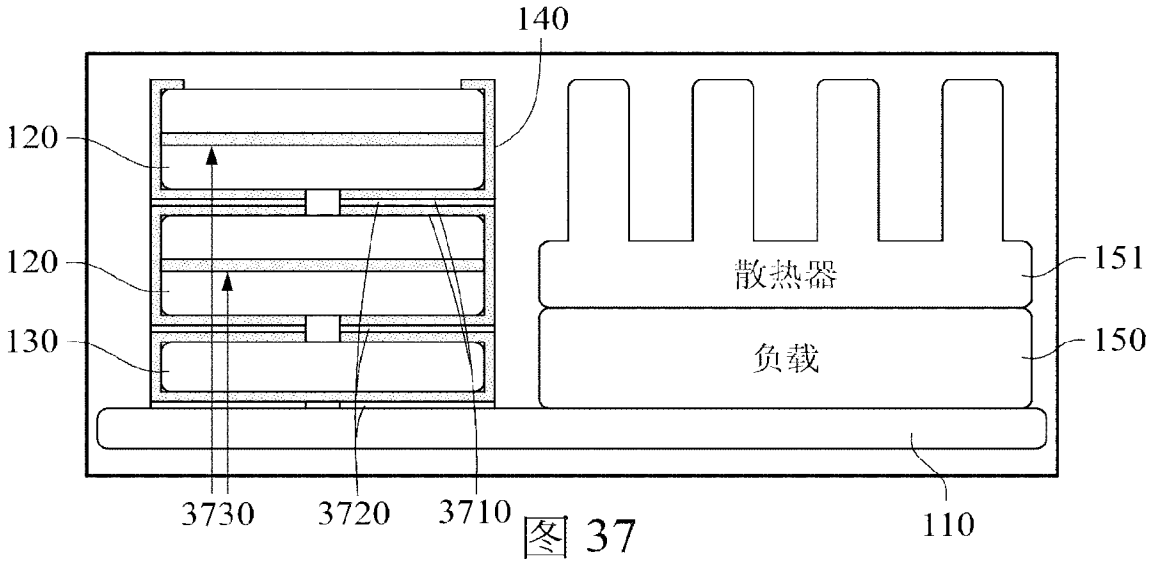

140
120
120
130
散热器
151
负载
150
3730
3720
3710
110

图 37

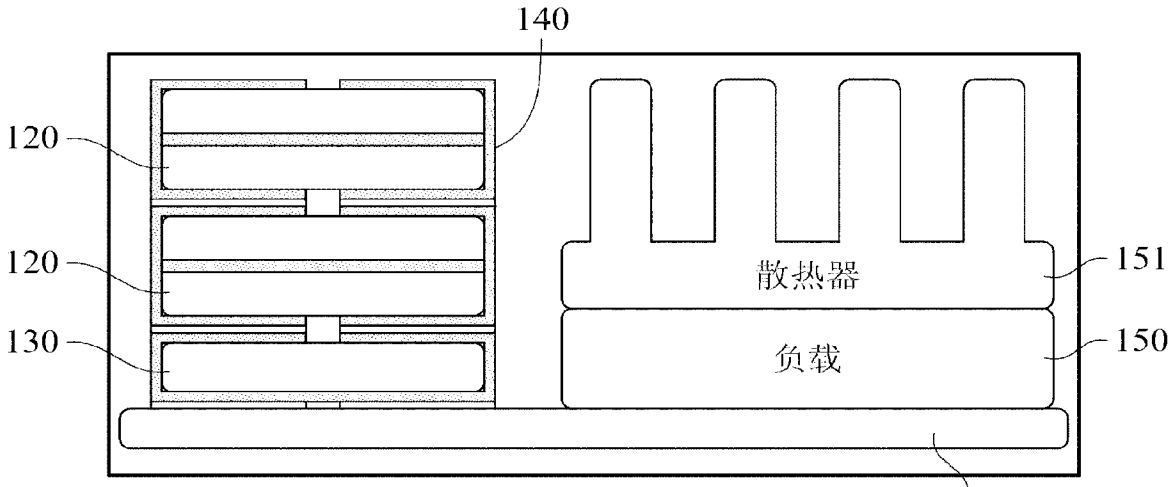

140
120
120
130
散热器
151
负载
150
110

图 38

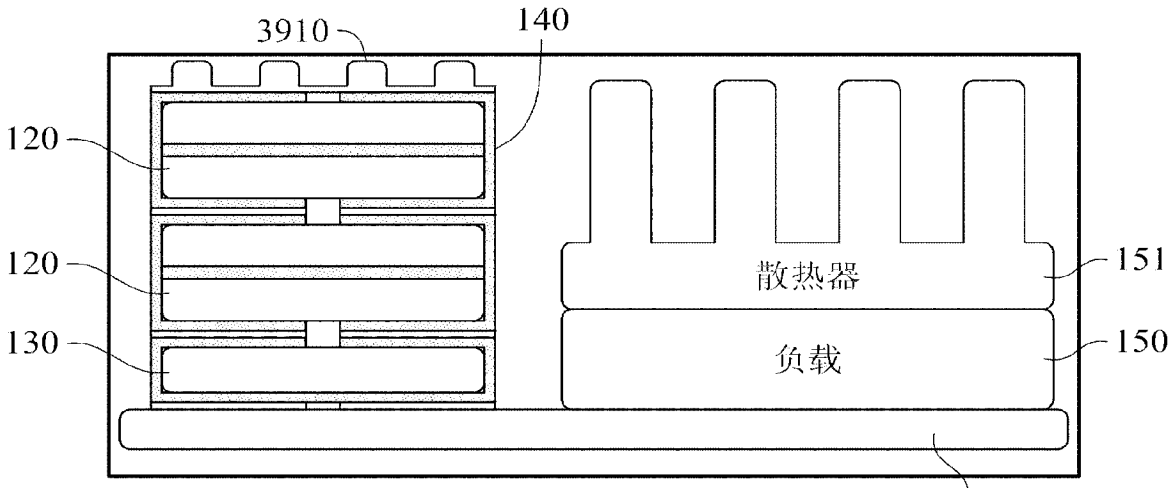

3910
140
120
120
130
散热器
151
负载
150
110

图 39

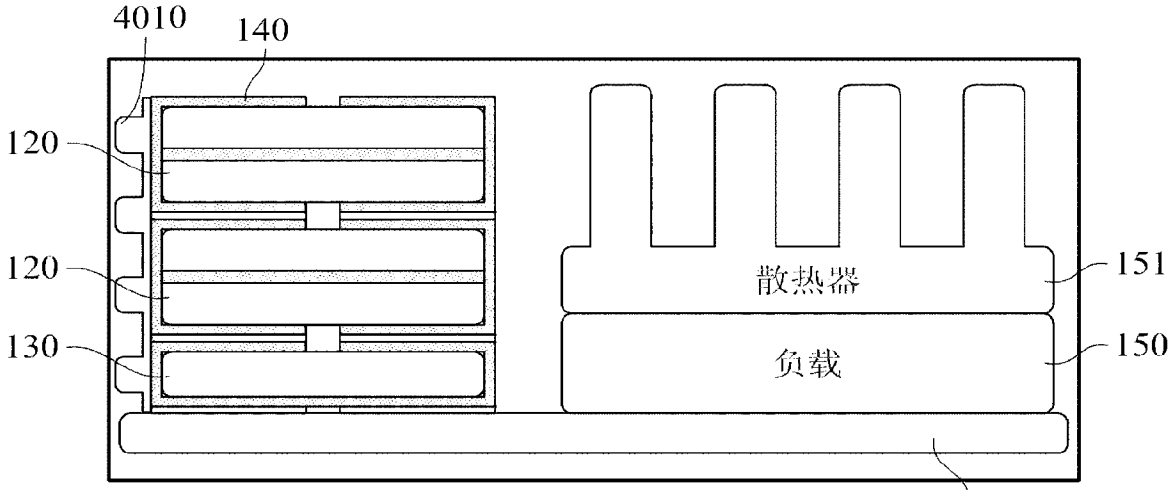

4010
140
120
120
130
散热器
151
负载
150
110

图 40

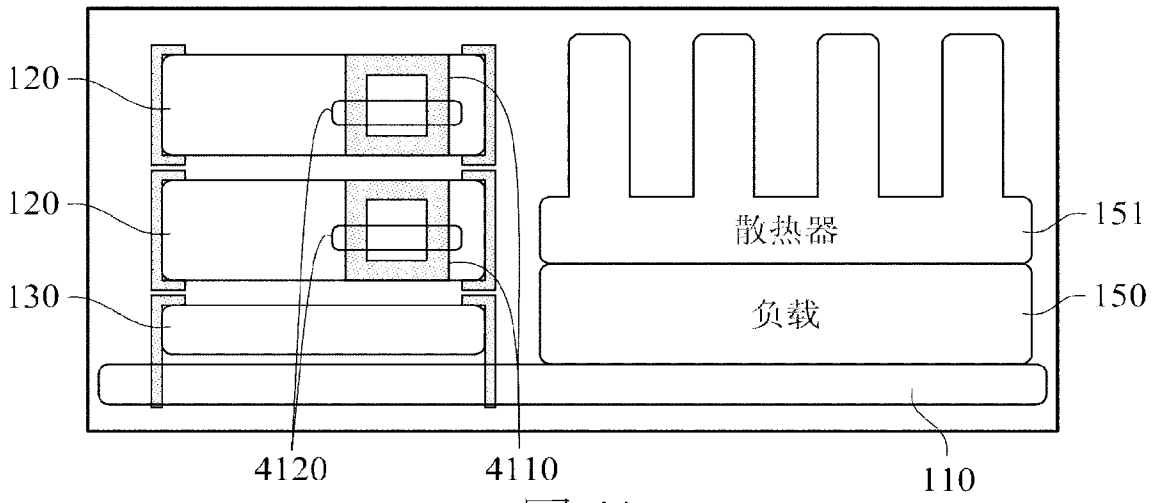

120
120
130
散热器
负载
151
150
4120
4110
110

图 41

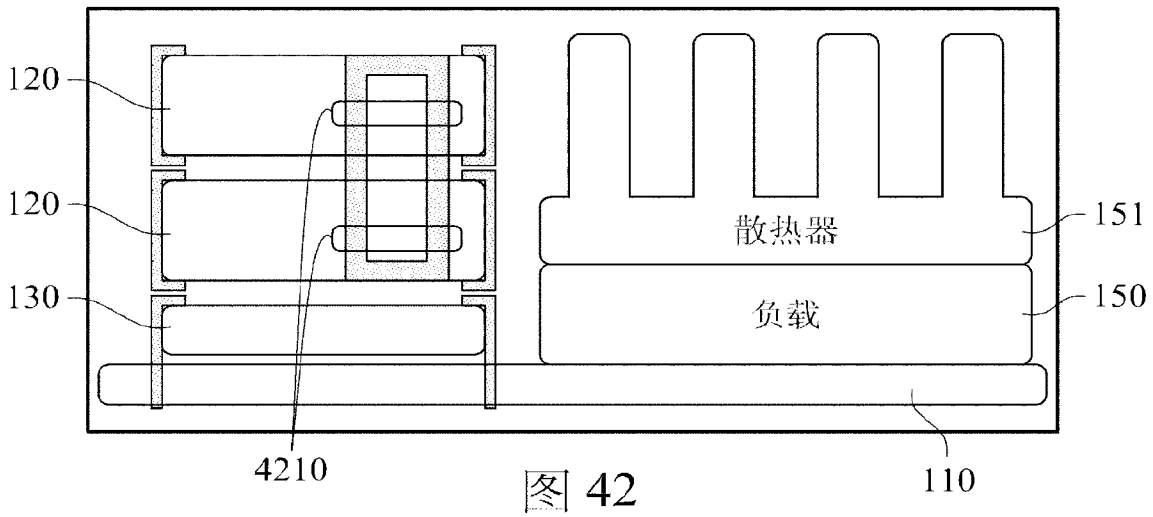

120
120
130
散热器
负载
151
150
4210
110

图 42

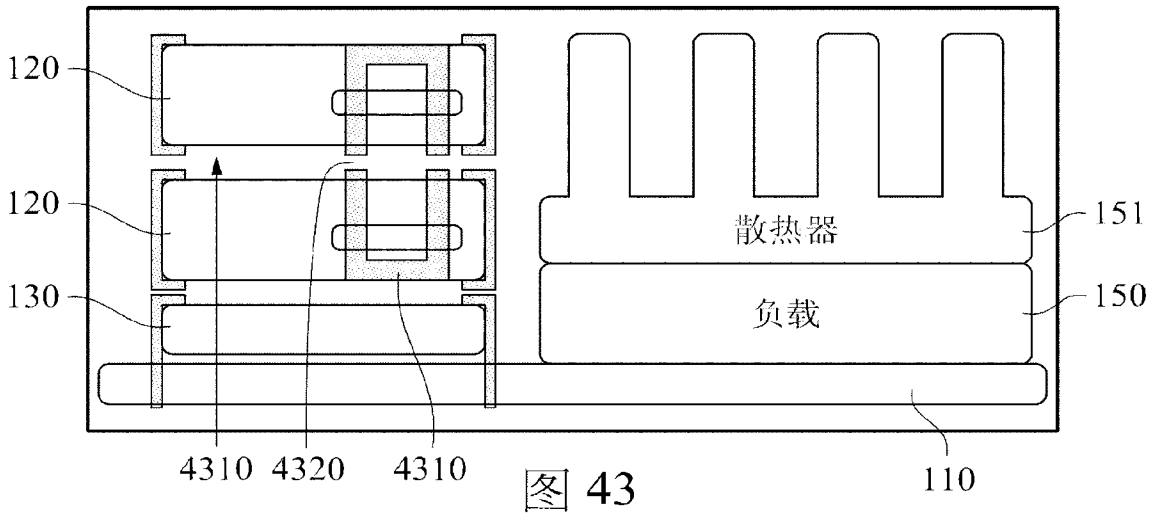

120
120
130
散热器
负载
151
150
4310
4320
4310
110

图 43

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证　明

本证明之附件是向本局提交的下列专利申请文件副本。

申　请　号：201410442972.6

申　类　型：发明专利

发　造　名称：电源装置

申　日：2014年09月02日

申　人：台达电子工业股份有限公司

发明　计人：曾剑鸿、言超、忽培青

局长
申长雨

2014 年 09 月 15 日

IPR2024-00715 EX. 2005

2014104429726

权 利 要 求 书 TWLB4955-14P1

1. 一种电源装置，其特征在于，包括：

控制单元与功率单元，堆叠设置且毗邻负载的位置，所述功率单元至少含一功率半导体器件，所述控制单元至少含一具备控制或者驱动能力的芯片；以及

引脚，电性连接所述控制单元和所述功率单元；所述控制单元用于控制所述功率单元，使所述功率单元供电给毗邻的所述负载。

2. 根据权利要求 1 所述的电源装置，其特征在于，所述控制单元与所述功率单元，堆叠设置设于主板上，所述主板还设有所述负载。

3. 根据权利要求 1 所述的电源装置，其特征在于，还包括：焊盘，分布于所述功率单元的侧面和所述控制单元的侧面，与所述引脚电性连接。

4.根据权利要求 3 所述的电源装置，其特征在于，所述引脚包括表面贴装引脚，分布于所述功率单元和所述控制单元的外表面并与所述焊盘电性连接。

5.根据权利要求 3 所述的电源装置，其特征在于，所述表面贴装引脚覆盖所述功率单元 30%以上外表面积。

6.根据权利要求 3 所述的电源装置，其特征在于，所述引脚还包括直插引脚，所述直插引脚配合所述表面贴装引脚实现所述功率单元/所述控制单元与所述主板的电性连接。

7.根据权利要求 3 所述的电源装置，其特征在于，所述焊盘还分布于所述功率单元与焊盘所在侧面垂直的面。

8.根据权利要求 3 所述的电源装置，其特征在于，所述功率单元包括主功率单元部分和次功率单元部分，所述主功率单元部分的侧面分布所述焊盘，所

述次功率单元部分堆叠于所述主功率单元部分。

9.根据权利要求 1 所述的电源装置，其特征在于，所述功率单元与所述负载位于主板的同一面，所述控制单元位于主板与所述功率单元相对的另一面。

10. 根据权利要求 1 所述的电源装置，其特征在于，所述电源装置还包括一功率单元，所述两功率单元和所述控制单元相互之间堆叠设于主板，所述控制单元通过所述引脚控制所述两功率单元。

11. 根据权利要求 10 所述的电源装置，其特征在于，所述两功率单元分别为一第一级直流对直流变换器的功率单元和一第二级直流对直流变换器的功率单元；所述控制单元包括所述第一级直流对直流变换器的控制单元和所述第二级直流对直流变换器的控制单元。

12.根据权利要求 11 所述的电源装置，其特征在于，所述第一级直流对直流变换器为隔离型直流对直流变换器；所述第二级直流对直流变换器为非隔离调整型直流对直流变换器。

13.根据权利要求 12 所述的电源装置，其特征在于，所述非隔离调整型直流对直流变换器比所述隔离型直流对直流变换器靠近所述主板。

14. 根据权利要求 11 所述的电源装置，其特征在于，所述第一级直流对直流变换器为非隔离调整型直流对直流变换器；所述第二级直流对直流变换器为隔离非调整型直流对直流变换器。

15. 根据权利要求 14，其特征在于，所述第一级直流对直流变换器为升降压电路。

16. 根据权利要求 10 所述的电源装置，其特征在于，所述两功率单元中一所述功率单元包括一第一级直流对直流变换器的功率单元和一第二级直流

对直流变换器的功率单元。

17.根据权利要求 16 所述的电源装置，其特征在于，所述第一级直流对直流变换器为隔离型直流对直流变换器，第二级直流对直流变换器为非隔离调整型直流变换器。

18.根据权利要求 17 所述的电源装置，其特征在于，所述隔离型直流对直流变换器包括：隔离型变压器、若干原边开关管和副边开关管；所述非隔离调整型直流变换器为负载点降压直流变换器。

19.根据权利要求 18 所述的电源装置，其特征在于，所述隔离变压器、副边开关管、用于隔离直流对直流变换器的输出电容器和负载点直流变换器设置于同一个所述功率单元。

20.根据权利要求 18 所述的电源装置，其特征在于，所述原边开关管设置于所述控制单元，所述控制单元还包括原边开关管驱动电路、负载点直流变换器的控制驱动电路和控制芯片。

21.根据权利要求 20 所述的电源装置，其特征在于，所述原边开关管位于靠近所述控制单元侧面的位置。

22. 根据权利要求 10 所述的电源装置，其特征在于，所述功率单元之间、所述功率单元与所述控制单元之间填充有导热绝缘胶。

23. 根据权利要求 10 所述的电源装置，其特征在于，所述功率单元与所述控制单元电性连接的引脚之间以及所述功率单元与所述功率单元电性连接的引脚之间填充有导电焊接材料。

24. 根据权利要求 10 所述的电源装置，其特征在于，所述功率单元各包括一平面变压器，所述两个平面变压器共用一磁芯。

25. 根据权利要求 24 所述的电源装置，其特征在于，所述磁芯的气隙设置于所述功率单元之间的堆叠间隙。

26.根据权利要求 3 所述的电源装置，其特征在于，所述功率单元包括若干开关器件以及承载所述开关器件的载板和包覆所述开关器件的绝缘封料；所述开关器件分布于靠近所述焊盘的位置。

27.根据权利要求 26 所述的电源装置，其特征在于，所述绝缘封料上设有配合所述引脚安装的凹部。

28.根据权利要求 26 所述的电源装置，其特征在于，所述功率单元还包括电感和电容，所述电感、所述电容及所述开关器件位于所述载板上靠近所述功率单元侧面的位置。

29. 根据权利要求 3 所述的电源装置，其特征在于，所述焊盘包括一次侧群焊盘与二次侧群焊盘，所述一次侧群焊盘与所述二次侧群焊盘之间至少间隔一安规距离。

30. 根据权利要求 29 所述的电源装置，其特征在于，所述一次侧群焊盘包括第一信号焊盘与第一功率焊盘，所述第一功率焊盘的截面积大于所述第一信号焊盘的截面积。

31. 根据权利要求 30 所述的电源装置，其特征在于，所述二次侧群焊盘包括第二信号焊盘与第二功率焊盘，所述第二功率焊盘的截面积大于所述第二信号焊盘的截面积。

32. 根据权利要求 31 所述的电源装置，其特征在于，所述第二功率焊盘的数量多于所述第一功率焊盘的数量。

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33. 一种电源装置，其特征在于，包括：

控制单元与功率单元，堆叠设置且毗邻设有数据处理芯片的负载的位置，所述功率单元至少含一功率半导体器件，所述控制单元至少含一具备控制或者驱动能力的芯片；以及

引脚，电性连接所述控制单元和所述功率单元；所述控制单元用于控制所述功率单元，使所述功率单元供电给毗邻的所述负载。

34. 根据权利要求 33 所述的电源装置，其特征在于，所述控制单元与所述功率单元，堆叠设置设于主板上，所述主板还设有所述数据处理芯片的所述负载。

35. 根据权利要求 33 所述的电源装置，其特征在于，还包括：焊盘，分布于所述功率单元的侧面和所述控制单元的侧面，与所述引脚电性连接。

36. 根据权利要求 33 所述的电源装置，其特征在于，所述电源输入操作最高电压高于 20V，

所述功率单元包含：

至少一变压器，所述变压器含至少一原边和至少一副边；

至少一同步整流组合和一输出电容组合；

高频能量从所述原边传递至所述副边，并通过所述同步整流组合整流为直流后传递至所述输出电容整合。

37. 根据权利要求 36 所述的电源装置，其特征在于，所述控制单元由嵌入式工艺实现，厚度低于 2 毫米。

38. 根据权利要求 37 所述的电源装置，其特征在于，所述功率单元为谐振型电路，操作频率高于 1MHZ。

39. 根据权利要求 37 所述的电源装置，其特征在于，所述控制单元上方更堆叠一输入滤波器。

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40. 根据权利要求 33 所述的电源装置，其特征在于，所述功率单元为一第一级直流对直流变换器；所述控制单元为和一第二级直流对直流变换器的功率单元。

41. 根据权利要求 40 所述的电源装置，其特征在于，所述第一级直流对直流变换器为非隔离调整型变换器；所述第二级直流对直流变换器为非调整隔离型变换器。

42. 根据权利要求 40 所述的电源装置，其特征在于，所述第一级直流对直流变换器为隔离型变换器；所述第二级直流对直流变换器为非隔离调整型变换器。

43. 根据权利要求 33 所述的电源装置，其特征在于，还包含至少一散热单元，该散热单元置于焊盘或者引脚组合上方，且与焊盘或者引脚间的热阻小于 5 摄氏度/瓦。

44.根据权利要求 43 所述的电源装置，其特征在于，所述散热单元与焊盘或者引脚组合之间有绝缘材料。

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电源装置

技术领域

本发明是有关于一种电源装置，且特别是有关于一种电源装置的内部结构。

背景技术

随着人类对智能生活要求的提升，社会对数据处理的需求日益旺盛。全球在数据处理上的能耗，平均每年达到数千亿甚至数万亿度；而一个大型数据中心的占地面积可以达到数万平方米。因此，高效率和高功率密度，是这一产业健康发展的关键指标。

数据中心的关键单元是服务器，其主板通常由 CPU、Chipsets、内存等等数据处理芯片和它们的供电电源及必要外围元件组成。随着单位体积服务器处理能力的提升，意味着这些处理芯片的数量、集成度也在提升，导致空间占用和功耗的提升。因此，为这些芯片供电的电源（因为与数据处理芯片同在一块主板上，又称主板电源），就被期望有更高的效率，更高的功率密度和更小的体积，来支持整个服务器乃至整个数据中心的节能和占地面积缩小。

在服务器的中，主板(Main Board PCB)用于进行能量和信号传递。主板上放置有数据处理芯片及其供电电源。服务器的外壳高度，通常为一个标准的数值，它可以用工业标准 U 来定义，如 1U、1.5U、2U 等（1U=1.75inch=44.45mm）。以 1U 即高度约 40mm(因为有装配工差等需要，1U 实际尺寸不尽相同)服务器为例，主板通常为 6～50 层的 PCB 板，其造价相当昂贵。在一定服务器外壳高度的限制下，保证效率期望的同时，减小主板电源所占用主板的面积也即主板电源水平面积，不仅能减小体积，增加功率密度，而且能降低成本。本文中，称电源单位水平面积的功率为“功率压强”。

当用同一技术能力设计功率为 Po 的电源时，通常电源的体积 V 越大，其效率越容易做到较高，也即电源效率与其体积 V 成正比关系。而体积 V 等于高度 H 乘以水平面积 S。功率压强 Pp 则为 Po/S。限定效率为固定目标，即效

率保持不变。即可得到功率压强 Pp 与高度 H 的关系：即 H 越大，Pp 就可以越大。也即，要提高 Pp，应当在高度 H 的利用上，思考解决方案。当然，如果是为了追求效率，根据前面的逻辑也应当充分利用高度。因此，如何利用高度是兼顾功率压强 Pp 和效率的关键所在。

主板电源的厚度或者说高度较好的可以做到 7mm 甚至更薄，因此，在一定的服务器高度的限制下，如 1U 高度，其上方仍可以有大于 20mm 的空间。而其效率可以高至 90%甚至以上，由于其功耗仅仅是数据处理芯片的几分之一（如 0.1 倍），事实上，有机会无需散热单元即可自行处理热问题。这样主板电源上的空间就没有充分的利用起来。

通常主板电源具体的做法一般包含两种。其一是以 PCB 为载体，采用分立元件组装而成。通过业界多年的努力，这种类型的主板电源实现了不错的效率和功率密度。但由于分立元件组装，需要必要的间隙、安规距离，影响了水平面积的进一步缩小，且高度不规则，也影响热的后续处理。

而主板电源的另一种做法为采用一定的封装技术，将电源各元件集成为一个很规则的元件。由于封装技术的使用，使得其功率密度显着提高，效率也不逊色，且规则的外形，有利于后续热的处理，是不错的解决方案。只是这种做法采用的封装技术，主要追求通过主板电源高度的降低来实现其体积的缩小及功率密度的提高，而一味的降低高度将限制其在占地面积上的进一步缩小。因此，该解决方案仅是追求功率密度的较好方案之一，但在追求数据中心主板电源的功率压强方面仍有较大欠缺。

发明内容

本发明即针对现有技术的不足之处，提出了新的解决方案，使得功率压强和效率得到最大兼顾，适合对水平面积有较大限制的应用场合，例如数据中心等数据处理场合对电源的需求。

本发明的一方面是在提供一种电源装置，其包括控制单元与功率单元，堆叠设置且毗邻负载的位置，功率单元至少含一功率半导体器件，所述控制单元至少含一具备控制或者驱动能力的芯片；引脚，电性连接控制单元和功率单元；控制单元用于控制功率单元，使功率单元供电给毗邻的负载。

于一实施例中，控制单元与功率单元，堆叠设置设于主板上，所述主板还

设有所述负载。

于一实施例中，电源装置还包括：焊盘，分布于所述功率单元的侧面和所述控制单元的侧面，与所述引脚电性连接。

于一实施例中，引脚包括表面贴装引脚，分布于功率单元和控制单元的外表面并与焊盘电性连接。

于一实施例中，表面贴装引脚覆盖功率单元30%以上外表面积。

于一实施例中，引脚还包括直插引脚，直插引脚配合表面贴装引脚实现功率单元/控制单元与主板的电性连接。

于一实施例中，焊盘还分布于功率单元与焊盘所在侧面垂直的面。

于一实施例中，功率单元包括主功率单元部分和次功率单元部分，主功率单元部分的侧面分布焊盘，次功率单元部分堆叠于主功率单元部分。

于一实施例中，功率单元与负载位于主板的同一面，控制单元位于主板与功率单元相对的另一面。

于一实施例中，电源装置还包括一功率单元，两功率单元和控制单元相互之间堆叠设于主板，控制单元通过引脚控制两功率单元。

于一实施例中，两功率单元分别为一第一级直流对直流变换器的功率单元和一第二级直流对直流变换器的功率单元；控制单元包括第一级直流对直流变换器的控制单元和第二级直流对直流变换器的控制单元。

于一实施例中，第一级直流对直流变换器为隔离型直流对直流变换器；第二级直流对直流变换器为非隔离调整型直流对直流变换器。

于一实施例中，非隔离调整型直流对直流变换器比隔离型直流对直流变换器靠近主板。

于一实施例中，两功率单元中一功率单元包括一第一级直流对直流变换器的功率单元和一第二级直流对直流变换器的功率单元。

于一实施例中，第一级直流对直流变换器为隔离型直流对直流变换器，第二级直流对直流变换器为非隔离调整型直流变换器。

于一实施例中，隔离型直流对直流变换器包括：隔离型变压器、若干原边开关管和副边开关管；非隔离调整型直流变换器为负载点降压直流变换器。

于一实施例中，隔离变压器、副边开关管、用于隔离直流对直流变换器的输出电容器和负载点直流变换器设置于同一个功率单元。

于一实施例中，原边开关管设置于控制单元，控制单元还包括原边开关管驱动电路、负载点直流变换器的控制驱动电路和控制芯片。

于一实施例中，原边开关管位于靠近控制单元侧面的位置。

于一实施例中，功率单元之间、功率单元与控制单元之间填充有导热绝缘胶。

于一实施例中，功率单元与控制单元电性连接的引脚之间以及功率单元与功率单元电性连接的引脚之间填充有导电焊接材料。

于一实施例中，功率单元各包括一平面变压器，两个平面变压器共用一磁芯。

于一实施例中，磁芯的气隙设置于功率单元之间的堆叠间隙。

于一实施例中，功率单元包括若干开关器件以及承载开关器件的载板和包覆开关器件的绝缘封料；开关器件分布于靠近焊盘的位置。

于一实施例中，绝缘封料上设有配合引脚安装的凹部。

于一实施例中，功率单元还包括电感和电容，电感、电容及开关器件位于载板上靠近功率单元侧面的位置。

于一实施例中，焊盘包括一次侧群焊盘与二次侧群焊盘，一次侧群焊盘与二次侧群焊盘之间至少间隔一安规距离。

于一实施例中，一次侧群焊盘包括第一信号焊盘与第一功率焊盘，第一功率焊盘的截面积大于第一信号焊盘的截面积。

于一实施例中，二次侧群焊盘包括第二信号焊盘与第二功率焊盘，第二功率焊盘的截面积大于第二信号焊盘的截面积。

于一实施例中，第二功率焊盘的数量多于第一功率焊盘的数量。

于一实施例中，第一级直流对直流变换器为非隔离调整型直流对直流变换器；第二级直流对直流变换器为隔离非调整型直流对直流变换器。

于一实施例中，第一级直流对直流变换器为升降压电路。

本发明的另一方面是在提供一种电源装置，电源装置包括：控制单元、功率单元与引脚。控制单元与功率单元堆叠设置且毗邻设有数据处理芯片的负载的位置，功率单元至少含一功率半导体器件，控制单元至少含一具备控制或者驱动能力的芯片；引脚电性连接控制单元和功率单元；控制单元用于控制功率单元，使功率单元供电给毗邻的负载。

于一实施例中，控制单元与功率单元堆叠设置设于主板上，主板还设有数据处理芯片的所述负载。

于一实施例中，电源装置还包括：焊盘，分布于所述功率单元的侧面和所述控制单元的侧面，与所述引脚电性连接。

于一实施例中，电源输入操作最高电压高于 20V，功率单元包含：至少含一变压器，变压器含至少一原边和至少一副边；至少含一同步整流组合和一输出电容组合；高频能量从原边传递至副边，并通过同步整流组合整流为直流后传递至输出电容整合。

于一实施例中，控制单元由嵌入式工艺实现，厚度低于 2 毫米。

于一实施例中，功率单元为谐振型电路，操作频率高于 1MHZ。

于一实施例中，控制单元上方更堆叠一输入滤波器。

于一实施例中，功率单元为一第一级直流对直流变换器；控制单元为和一第二级直流对直流变换器的功率单元。

于一实施例中，第一级直流对直流变换器为非隔离调整型变换器；第二级直流对直流变换器为非调整隔离型变换器。

于一实施例中，第一级直流对直流变换器为隔离型变换器；第二级直流对直流变换器为非隔离调整型变换器。

于一实施例中，电源装置还包含至少散热单元，该散热单元置于焊盘或者引脚组合上方，且与焊盘或者引脚间的热阻小于 5 摄氏度/瓦。

于一实施例中，散热单元与焊盘或者引脚组合之间有绝缘材料。

综上所述，本发明的技术方案与现有技术相比具有明显的优点和有益效果。通过上述技术方案，可达到相当的技术进步，并具有产业上的广泛利用价值。由于本发明采用了堆叠的结构，电源的高度就可以更好利用，在一定体积下，实现了更小的占地面积；同时又有足够的体积保证高的效率，实现了高功率压强和高效率的兼顾。也为实现更高特性的数据处理设备提供了支持。

以下将以实施方式对上述的说明作详细的描述，并对本发明的技术方案提供更进一步的解释。

附图说明

为让本发明的上述和其它目的、特征、优点与实施例能更明显易懂，所附

附图的说明如下：

图 1 是依照本发明一实施例的一种电源装置的侧视图；

图 2 至图 16 是依照本发明实施例所绘示的电源架构及堆叠内容分配；

图 17 至图 19 是依照本发明实施例所绘示的控制单元与功率单元可涵盖的内容；

图 20 至图 23 是依照本发明实施例所绘示的堆叠结构设计；

图 24 至图 34 是依照本发明实施例所绘示的引脚布置；

图 35 至图 40 是依照本发明实施例所绘示的散热处理架构；以及

图 41 至图 43 是依照本发明实施例所绘示的磁芯配置。

具体实施方式

为了使本发明的叙述更加详尽与完备，可参照所附的附图及以下所述各种实施例，附图中相同的号码代表相同或相似的组件。另一方面，众所周知的组件与步骤并未描述于实施例中，以避免对本发明造成不必要的限制。

于实施方式与权利要求书中，涉及“耦接(coupled with)”的描述，其可泛指一组件透过其它组件而间接连接至另一组件，或是一组件无须透过其它组件而直接连接至另一组件。

本发明的技术态样是一种电源装置，其可应用在服务器，或是广泛地运用在各种技术领域。值得一提的是，本技术态样的电源装置采用了堆叠的结构，电源的高度就可以更好利用，在一定体积下，实现了更小的占地面积。

图 1 是依照本发明一实施例的一种电源装置的侧视图。如图 1 所示，电源应用装置（如：电源装置）包括主板 110、功率单元 120、控制单元 130 与引脚 140。主板 110 上还设有负载 150，功率单元 120 位在主板 110 上，控制单元 130 与功率单元 120 堆叠设置于主板 110 上毗邻负载 150 的位置，引脚 140 电性耦接主板 110、控制单元 130 和功率单元 120，于本实施例中，引脚 140 的数量为多个且分别位于功率单元 120 与控制单元 130 中每一者的侧边，两功率单元 120 和控制单元 130 相互之间堆叠设于主板 110。控制单元 130 用于控制功率单元 120，具体而言，控制单元通过引脚 140 控制所述两功率单元 120，使功率单元 120 供电给毗邻的负载 150。负载 150 为数字处理 IC，如中央处理器(CPU)，中央处理器上有设有散热单元散热装置如散热器 151。功率单元 120

至少含一功率半导体器件（如：图 3 的开关管 S21、S22、S23、S24，图 11 的开关管 S21、S22、S23、S24、S31、S32、S33），控制单元 130 至少含一具备控制或者驱动能力的芯片(如：图 3 的控制电路 310，图 11 的控制电路 1100、DSP）。

于一实施例，电源装置设于主板 110 上，主板 110 还设有数据处理芯片(如：CPU)的负载 150，电源装置包括：功率单元 120、控制单元 130 与引脚 140。控制单元 130 与功率单元 120 堆叠设置于主板上毗邻负载 150 的位置，引脚电性连接主板 110、控制单元 130 和功率单元 120，控制单元 130 用于控制功率单元 120，使功率单元 120 供电给毗邻的负载 150。

总的而言，直流/直流电源包含了至少两个单元（即模块）：控制单元 130 及功率单元 120。这两个模块上下堆叠放置，通过导体(即引脚 140)进行彼此之间的电气连接以传递电信号。其中功率单元 120 至少包含一个主动开关元件，功率单元 120 接收输入功率通过主动开关元件的导通及关断产生相应的输出功率提供给负载 150，如数据处理芯片。控制单元 130 模块至少包含一个控制芯片，发送控制信号给功率单元 120 的主动开关元件以控制该元件的导通及关断。置于上方的单元，部分引脚通过置于下方的单元固定后，传递电信号至上述的主板 110(如：PCB 板)。

如此，由于采用了堆叠的结构，电源的高度就可以更好利用，在一定体积下，实现了更小的占地面积；同时又有足够的体积保证高的效率，实现了高功率压强和高效率的兼顾。也为实现更高特性的数据处理设备提供了支持。

涉及的电源架构及堆叠内容分配

如图 2，为一个服务器主板可能涉及的各种类型电源变换器（即主板电源 200）的示意图。该电源变换器输入通常为直流，其电压范围宽广，有高压，如 200～500V（以 400V 为例），中压，如 18～72V（以 48V 为例）以及低压，如 5～15V（以 12V 为例）。不管输入为什么电压，都需要有相应的 DC/DC 变换器，将其变换成所需要的输出，以提供给其负载 150，如数据处理芯片，像是中央处理器(CPU)及内存等。其输出的变化范围也很广泛以适应不同的负载要求，例如输出为低至 0.8V 甚至更低，高至 12 伏甚至更高。当负载 150 为 CPU 和内存时，输出电压通常在 0.8～2V 之间。因此，涉及的电源规格主要含以下几种：

（1）变换器 210 将 400V 转 48V：输入为 200～500V（以 400V 为典型）之间的某一电压范围，输出为稳定输出或者与输入成固定比例，以 48V 附近为典型值，也可在 18V～72V 之间的某一电压范围。由于输出电压相对较高，通常不会直接接数据处理芯片负载，需在其后级联另一规格变换器，将电压调到适应负载可用的程度。

（2）另一变换器（图未示）将 400V 转 12V：输入为 200～500V（以 400V 为典型）之间的某一电压范围，输出为稳定输出或者与输入成固定比例，以 12V 附近为典型值。由于输出电压较低，可以接部分数据处理负载，如硬盘等。但当负载电压更低时，例如 0.5～5V，则需在其后级联另一规格 DC/DC 变换器，将电压调到适应负载可用的程度。

（3）又一变换器（图未示）将 400V 转 0.5～5V：输入为 200～500V（以 400V 为典型）之间的某一电压范围，输出为按需调整的稳定电压，例如 0.5～5V 之间。其输出可以直接接数据处理芯片，如 CPU、内存等。

以上（1）、（2）、（3）中的三类规格的变换器，由于是高压输入，需要符合高压安规绝缘要求，其绝缘电压高至直流电压 2000V 甚至以上。

（4）变换器 220 将 48V 转 12V：输入为 18～72V（以 48V 为典型）之间的某一电压范围，输出为稳定输出或者与输入成固定比例，以 12V 附近为典型值，也可在 3V～15V 之间的某一电压范围。该规格的变换器可以直接接某些数据处理负载，如硬盘等。

（5）变换器 230 将 48V 转 0.5～5V：输入为 18～72V（以 48V 为典型）之间的某一电压范围，输出为按需调整的稳定电压，例如在 0.5～5V 之间。且输出可直接接数据处理芯片，如 CPU、内存等。

（6）变换器 240 将 12V 转 0.5～5V：输入为 3V～15V（以 12V 为典型）之间的某一电压范围，输出为按需调整的稳定电压，以 0.5～5V 之间。其输出可以直接接数据处理芯片，如 CPU、内存等。由于是低压输入，不需要隔离。输出则直接接数据处理芯片，如 CPU、内存等。

以上（4）、（5）、（6）中的三类变换器，由于输入/输出电压均相对较低，则变换器的耐压需求较低，通常在直流电压 2000V 以下。

当变换器输出为 0.5～5V 时，由于输出可以直接接负载 150，例如数据处理芯片，需要电源变换器输出低压大电流并且要求有很高的动态响应能力，如

当负载 150 为 CPU 时要求有 1000A/ns 的响应能力，这样就需要电源变换器就近放置在负载附近。因此这些电源被称为负载点电源(Point of the load)。其中尤以给 CPU 供电的叫电压调整模块（Voltage Regulated Module, VRM）需要就近供电。

如上各种输入输出规格的电源变换器，由于均设置在主板之上，因此，均适合用堆叠的方式来实现高功率压强和高效率的兼顾。当然，各种变换器的组合也适合采用堆叠的方式放置。

如上，400V 和 48V 输入的电源，由于输入输出压差较大，也通常有输入输出安规耐压需求，通常由变压器来隔离传递能量。当然，若有需要，例如为实现更宽的输入或者输出范围，低压输入电源如 12V 输入的电源也可以采用变压器来传递能量。

以上各种规格的变换器可以采用多种类型的拓扑来实现电能的变换，例如脉冲宽度调制(PWM)型的正向电路、全桥电路、移相全桥电路、半桥电路、反激式电路等。为了实现高的功率密度，通常需要工作频率较高，如 500kHZ、1MHZ，甚至 2MHZ 以上。为了在这么高的频率下实现高的效率，通常需要选择谐振型电路，即脉冲频率调制(PFM)型的 LLC 串联谐振变换器(LLC-SRC)、并联谐振变换器(PRC)等等。

图 3 所示为一半桥 LLC 电路。如图 3 所示，该电路包含了主电路以及控制电路 310。其中主电路包含了：输入电容器 C1、谐振电容器 C2、谐振电感器 L1、变压器 T1、一次侧开关管 S11、S12 与二次侧开关管 S21、S22、S23、S24，其中输入电容器 C1 连接一次侧开关管 S11、S12，一次侧开关管 S11、S12 连接由谐振电容器 C2、谐振电感器 L1、变压器 T1 的原边组成的串联回路，变压器 T1 的副边连接二次侧开关管 S21、S22、S23、S24，输出电容器 C3 连接所述二次侧开关管 S21、S22、S23、S24。一次侧开关管 S11、S12 接收输入功率并将直流输入信号转换为交流信号，该交流信号经过谐振电感器 L1，谐振电容器 C2 及变压器 T1 传送至二次侧，通过二次侧同步整流线路（如，二次侧开关管 S21、S22、S23、S24），在输出电容器 C3 上产生输出电压并提供输出功率给负载。特别提及的是，由于输出为低压大电流，为了减少损耗，通常需要涉及低压大电流的组件（如 T1 副边、副边整流管、输出电容）进行并联已获得低的低电阻。如由“一整流组合 S21、S22 与一副边形成的组合”

和“另一整流组合 S23、S24 与另一副边组成的组合”进行并联。由于输出电压各有不同，因此，变压器副边的结构并非限制于图 3 所示的中心抽头整流结构，也可以是其他如全桥整流结构。

控制电路 310 产生控制信号提供给驱动一次侧开关管 S11、S12 的驱动器 320，和驱动二次侧开关管 S21～S24 的驱动器 330 用以控制主电路中各开关元件，如开关管 S11、S12，S21～S24 等的开通及关断。当然控制电路 310 还有包含其他采样、保护、通信等等必要元件在图中并未展示，在此也不做赘述。

功率单元 120 由于在高频工作状态下，并且变换器的输出为低压大电流，通常变压器二次侧、输出同步整流线路及输出电容器三者组成的回路尽量的小，以适应高频需要。因此，变压器 T1、同步整流线路（即，二次侧开关管 S21、S22 等）、输出电容器 C3 必须放在同一单元电路（即，功率单元 120）中。

于一实施例，电源输入操作最高电压高于 20V，功率单元 120 包含：至少一变压器 T1，变压器 T1 含至少一原边和至少一副边；至少一同步整流组合（如：二次侧开关管 S21、S22）和一输出电容组合（如：输出电容器 C3）。高频能量从原边传递至副边，并通过同步整流组合整流为直流后传递至输出电容整合。

另一方面，控制电路 310 的周边通常有许多的外围电路，需要处理的信号通常很低，也要求就近放置以便提升抗干扰的能力。因此，控制电路 310 及其外围电路需在同一单元电路（即，控制单元 130）中。于一实施例，控制单元 130 由嵌入式工艺实现，厚度低于 2 毫米。功率单元为谐振型电路，操作频率高于 1MHZ。控制单元上方更堆叠一输入滤波器。

至于驱动电器 320、330、一次侧开关管 S11～S12、谐振电容器 C2、谐振电感器 L1，可以根据实际情况放置在功率单元 120 或者控制单元 130。输入电容器 C1 对一次侧开关管 S11～S12 有抑制电压尖峰的作用，因此最好与一次侧开关管 S11、S12 就近放置于同一单元中为佳。L1/C2 等可以与其他元件如 T1 集成而成。甚至 T1 的激磁电感也可以由一独立电感与变压器原边并联，以协助 T1 性能的优化。

如图 1 所示，整个功率电路采用控制单元 130 与功率单元 120 进行堆叠组合，将有效地减小该功率电路 120 的水平面积，在最后放置于主板 110 上时，

减小占用主板 110 的面积。如图 1 中，控制单元 130 或功率单元 120 可以采用封装的技术，例如采用塑封料对其进行模制（molding），形成一模块。或者，两者也可以采用分立元件制作。无论何种方式，各单元都可以包含一载板，如：印刷电路板（PCB）或者陶瓷电路板（DBC）等等，用以承载该单元的器件，或者，也可以采用单元内器件直接堆叠的方式，如开关元件与电感、电容等元件直接堆叠的方式。当一次侧开关管 S11～S12、谐振电容器 C2、谐振电感器 L1 集成于功率单元时，控制单元中电路将主要处理控制信号，因此其高度可以变得很小，如 5mm、3mm 甚至 1mm 以下。

而在功率较大的场合，可以将图 3 所示的多个主电路进行输入输出的并联。这样整个电源装置在结构上可以采用一个主电路为一个功率单元，多个相同的功率单元，及控制单元进行堆叠的方式，如图 1 所示。控制单元 130 可以放置于下面，两个功率单元 120 堆叠于上面，或者控制单元放置于两个功率单元中间，又或者控制单元放置于两个功率单元之上。无论何种方式，均充分地利用了高度，实现了占地面积不变的状态下进行功率的提升。其中控制单元 130 可以为一个，用于控制两个功率单元 120 中开关元件的开通和关断，也可以为多个，例如两个分别控制相应功率单元中开关元件的开通与关断。当然，也可以将控制单元与其中一个功率单元集成在一起，这样最后变成了至少一个功率单元 120 与一个控制单元 130 堆叠在一起，其中该控制单元集成了至少一个主电路。如图 4 所示。电源模块包含了功率单元 120 与控制单元 130 上下堆叠，并通过引脚 140 彼此进行电气连接。其中功率单元 120 集成一个直流到直流变换器，控制单元 130 集成另一个直流到直流变换器及控制电路，控制电路控制这两个直流到直流变换器。

如前面所述，电源装置接收输入产生输出提供能量给负载。该电源装置可以采用单级的变换器，例如如图 3 所示电路，实现电压转换的要求，甚至于隔离。当然也可以采用多级的变换器。由于受器件特性的限制，单级电路通常不适合宽范围输入输出，因此，针对电压范围宽的负载，如服务器电源的应用中的 CPU、内存等负载，比较适宜的是采用两级架构的电源，即其中一级负责隔离，另一起负责调压，各司其职，以达到最优状态。举例说来如图 5 和图 6 所示。

如图 5 所示，输入电压 Vin 为一宽的电压范围，例如 38～60V，该输入电

压通过前级电路例如一隔离非调整型直流对直流变换器，亦即：隔离变压模块DCX，（此处，“非调整型”是指在工作范围内的该电路的输入输出为固定比例关系，也即输出随输入成比例变化如 Vin/Vo=n，图中以 Vin/Vo=4 为例），实现高压隔离；然后通过后级电路例如一非隔离调整型直流对直流变换器提供输出给负载。举例来说，后级电路可为负载点变换单元 POL，其可以用来实现输出稳压和动态响应需求。由于后级电路具备调整能力，因此，前级电路可以不具备调整能力。但如果有需要，前级也可以具备或者部分具备调整能力，即为隔离型直流对直流变换器。

同时参照图 1、5，两功率单元 120 分别为第一级直流对直流变换器的功率单元和第二级直流对直流变换器的功率单元；控制单元 130 包括第一级直流对直流变换器的控制单元和第二级直流对直流变换器的控制单元。具体而言，第一级直流对直流变换器为隔离型直流对直流变换器；第二级直流对直流变换器为非隔离调整型直流对直流变换器(如图 5 所示)，非隔离调整型直流对直流变换器比所述隔离型直流对直流变换器靠近主板 110。或者，第一级直流对直流变换器为非隔离调整型直流对直流变换器，第二级直流对直流变换器为隔离非调整型直流对直流变换器。举例而言，第一级直流对直流变换器为升降压电路。

于一实施例，功率单元 120 为一第一级直流对直流变换器；控制单元 130 为和一第二级直流对直流变换器的功率单元。举例而言，第一级直流对直流变换器为非隔离调整型变换器；第二级直流对直流变换器为非调整隔离型变换器；或者，第一级直流对直流变换器为隔离型变换器；第二级直流对直流变换器为非隔离调整型变换器。

由于前级为非调整型的隔离变压模块 DCX，可以在设计上使该电路工作于其最佳工作点，从而使电路相对简单且效率很高。当隔离变压模块 DCX 为一谐振电路，则隔离变压模块 DCX 可以工作在谐振频率附近；而当直流变压器 DCX 为一 PWM 线路，如全桥线路，则可以工作在占空比最大的状态下。后级为调整的电路，例如负载点直流变换器 POL，通常由降压式变换电路（Buck 电路）来实现（如：负载点降压直流变换器），使得输出特性满足负载的要求，该线路简单，且输出电压范围很宽。两者结合，可以很容易地实现宽输入/输出电压范围以及高输出电压精度及动态响应特性等要求。当隔离变

压模块 DCX 采用谐振电路时，例如 LLC-SRC 电路，则较容易实现电源的高频下的高效率，并有很高的功率密度。当然，由于后级有调整功能，DCX 若因为某种原因，如减少中间 BUS 电压范围，以减少中间 BUS 电容及相关功率器件的耐压幅值，而具备一定程度的输出电压调整能力，也不影响本实施例的实现和作用。

如图 6 所示，输入电压 Vin 为一宽的电压范围，例如 38～60V。该输入电压 Vin 通过前级电路例如一个非隔离调整型直流变换器，亦即：前级调压模块（Front Regulate Module）FRM，将变化输入的电压转换成一个需要的值，例如一恒定电压 48V，并可以响应负载的动态变化；再在其后串联使用隔离非调整型直流变换器，亦即隔离变压模块 DCX 来实现电压隔离，并实现降压需求。该架构下最终输出即后级电路的输出的稳压和动态响应均由前级电路实现。由于前级调压模块 FRM 无需隔离，所以可以用多种拓扑例如降压、升压或者降、升压电路等来实现，为了高频需要，可以加以软开关技术。因此前级调压模块 FRM 也可以有很高的功率密度，隔离变压模块 DCX 也是如此。

同时参照图 1、6，两功率单元 120 中一功率单元 120 包括第一级直流对直流变换器的功率单元和第二级直流对直流变换器的功率单元，第一级直流对直流变换器为隔离非调整型直流对直流变换器，第二级直流对直流变换器为非隔离调整型直流变换器(如图 6 所示)。

以上两种电源架构下，以一个输出功率为 200W 的主板电源为例，在 1/16 砖（1.3in*0.9in, 33mm*22.9mm）即可分别实现隔离变压模块 DCX 和负载点直流变换器 POL（图 5 架构）或是前级调压模块 FRM 和隔离变压模块 DCX（图 6 架构），因此，其功率压强也为 85.5W/inch2（实际由于两个单元的安装空隙等需要，其功率压强更低）。由于两者高度均可在 10mm 甚至 7mm 之内。如果用本发明的方法，将两者堆叠，如图 7 所示，控制单元与功率单元整合成隔离变压模块 DCX 与负载点直流变换器 POL 堆叠设置于主板 110 上；或者，如图 8 所示，控制单元与功率单元整合成前级调压模块 FRM 和隔离变压模块 DCX 堆叠设置于主板 110 上。借此，功率压强可以立即倍升至 171W/inch2，大大缩小对主板面积的占用。即便堆叠可能需要一些额外的高度，如散热处理等等原因，其总高度也可以在 25mm 以下，完全可以满足服务器的高度需求（可以高至 30mm）。

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为了减少内部互连引脚占用的体积，可以将上述隔离变压模块 DCX 与负载点直流变换器 POL 的功率级做在同一功率单元 120 中，再将两级的控制电路做在同一控制单元 130 中。这样就可以集中处理功率部分，以得到更优效率和更小占地面积。其功率单元部分，也可根据实际功率需要，选择一个或者多个并联，如图 9 所示，多个功率单元 120 并联且均包括隔离变压模块 DCX 与负载点直流变换器 POL 中的功率级，控制单元 130 包括隔离变压模块 DCX 与负载点直流变换器 POL 中的控制电路。

图 11 是图 5 中电路架构的原理图。它与图 3 不同之处在于，它在图 3 的基础上增加了后级电路---负载点直流变换器 POL 的电路，例如图 11 中的降压电路。因为输出是低压大电流，POL 的实现往往由多个降压电路并联而成。具体并联的数量由实际情况而定。图 11 以三个并联为例。隔离非调整型直流对直流变换器包括：隔离变压器 T1、若干原边开关管 S11、S12 和若干副边开关管 S21、S22 等；非隔离调整型直流变换器为负载点直流变换器 POL。其中，每个负载点直流变换器 POL 的电路都分别包含了开关管 S31、S32 及 S33 及与开关电路连接的滤波电感器 L21、L22 及 L23，从而相应组成了降压电路。各负载点直流变换器 POL 的电路的输出并联于电容器 C4 的两端，以产生输出功率提供给负载。控制芯片 1100 用以产生控制信号以控制负载点直流变换器 POL 中开关元件的开通与关断。为了实现高效率，功率单元 120 至少包含隔离变压模块 DCX 的隔离型变压器 T1、同步整流开关管 S21～S24、输出电容器 C3 和负载点直流变换器 POL 中的开关管 S31～S33。换言之，隔离变压器 T1、副边开关管 S21、S22、S23、S24、用于隔离直流对直流变换器的输出电容器 C3 和负载点直流变换器 POL 设置于同一个功率单元 120。当然，图 11 中还包含了,滤波电感器 L21～L23 以及输出电容器 C4。控制单元 130 至少包含一个控制芯片 1100 及其外围电路，例如图中的信号处理器 DSP 及控制器的外围线路(图中未显示)。原边开关管 S11、S12 设置于控制单元 130，控制单元 130 还包括原边开关管驱动电路、负载点直流变换器的控制驱动电路和控制芯片 1100。

而对于前级调压模块 FRM 和隔离变压模块 DCX 的架构，也可以如此实现，得到更高效率和更高功率压强的兼顾，如图 10 所示，多个功率单元 120 并联且均包括前级调压模块 FRM 和隔离变压模块 DCX 中的功率级，控制单

元 130 包括前级调压模块 FRM 和隔离变压模块 DCX 中的控制电路。

当然，上述的隔离变压模块 DCX 也可以是可调整的变换器或者半调整的变换器。其功能的变化，并不影响本发明对其效率和功率压强提升的贡献。

以上实施例，电源都采用了直流到直流(DC/DC)变换器。这些例子可以应用于例如直流电源直接输入到服务器主板的架构中。当然，随着技术的发展，也会出现有交流电源 AC 直接输入到服务器主板 1200。如图 12 所示，交流电源 AC(例如 220Vin)直接接入服务器主板 1200，通过由各级级联或并联的电源模块 1201～1205 组成的主板电源 1210 将输入功率传送给相应的负载。与前面直流输入的主板电源相比较，该结构下还多了前级级联的电磁干扰滤波器(EMI filter)1221、功率因数校正(PFC)电路 1222 以及辅助电源模块(Aux. Power Module) 1223 等等。在该架构下，同样可以采用前面所述的堆叠技术。

如图 13，为一电磁干扰滤波器 1310 后级联功率因数校正电路 1320 的示意图。如图所示，电磁干扰滤波器 1310 接收交流输入，如 VAC =220V,之后，提供一输出信号给后级的 PFC 电路进行功率因数校正。功率因数校正电路 1320 实际可以采用各种类型的拓扑，例如升压、降压、双升压以及如图所示的图腾柱式结构等等。以图中所示的图腾柱式功率因数校正电路为例，该功率因数校正电路 1320 的主电路中包含了高频电容器 C、功率因数校正电感器 L 以及功率开关器件，即由主动开关元件 S1、S2 串联所组成的第一桥臂及被动开关元件 D1、D2 串联所组成的第二桥臂。第一及第二桥臂与高频电容器 C 并联连接，功率开关器件和高频电容器 C 电性耦接功率因数校正电感器 L；两个桥臂的中点分别连接电磁干扰滤波器 1310 的输出或者通过输入电感连接滤波器的输出。相应的功率因数校正的驱动和控制电路 1330 用于控制功率开关器件，具体而言，功率因数校正的驱动和控制电路 1330 包含了输出采样分压电路(Voltage divider)1331 用于采样功率因数校正主电路的输出 VDC，输入采样分压电路 1332、1333、1334 用于采样输入电压 VAC-P 及 VAC-N，以及输入电流 IL 的采样等采样电路。输出电压采样分压电路 1335 的输出信号 VDC 与相应的参考信号 VDC-ref 比较后通过电压环控制器(voltage loop controller)1335 输出一信号与 VAC 进行运算得到了输入电流 IL 的参考信号 IL-ref，输入电流 IL 经过运算与 IL-ref 进行比较后通过电流环控制器(current loop controller)1336 后得到相应的控制信号 PWM-S1 及 PWM-S2 用以控制开关

S1 及 S2。

图 14 所示为功率因数校正电路的堆叠结构示意图。可以将功率因数校正电路的主电路中的第一桥臂，第二桥臂，输出电容及相应的驱动，控制单元等集成于控制单元中，而将功率因数校正电感器 L 放置于功率单元 120 中，之后将功率单元 120 放置于控制单元 130 之上进行堆叠。这样就可以在控制单元 130 中优化电分布参数，得到更好特性，而把更多的体积留给电感，也有利于将效率提升至更高。当然，也可以将主电路都集成于功率单元 120 中，而将驱动和控制电路 1330 集成于控制单元 130 中。

如图 15 所示，则可以在图 14 的基础上，再堆叠一功率单元---电磁干扰滤波器单元。因为电磁干扰滤波主要是为功率因数校正电路服务，与功率因数校正电路就近堆叠，更有利于优化设计，实现更高特性。同样，辅助电源也可以采用与功率因数校正电路相似的堆叠方式。即将控制、驱动及一次侧的功率器件和高频电容等集成在控制单元中，而将变压器和输出整流、输出电容集成在功率单元中。如上各图所示的堆叠均可得到本发明兼顾功率密度和功率压强的好处。当然，其堆叠的顺序，可以根据实际需要而调整。

另一方面，本发明也适用于 DC/AC 场合，即逆变器(inverter)场合。图 16 所示为功率单元 120 包括一逆变器电路，直流输入 Vin 通过由主动开关元件 S1、S2 串联组成的第一桥臂以及主动开关元件 S3、S4 串联组成的第二桥臂后产生一交流信号，该信号通过滤波电路（包括滤波电感器 L、输出电容器 Co）之后在输出电容器 Co 上产生一输出电压 Vo。其具体的控制与驱动电路在该图中未显示。这样的逆变器也可以采用类似前面所述功率因数校正电路的堆叠结构。即控制单元中集成主电路的第一及第二桥臂，输入电容器 Cin 及控制驱动电路，而功率单元集成输出滤波电感器 L 及输出电容器 Co。当然，也可以将主电路的所有元件，即输出电容器 Cin, S1～S4、滤波电感器 L 及输出电容器 Co 都集成于功率单元 120 中，控制单元集成控制驱动电路等。

控制单元可涵盖的内容

控制单元以信号处理为主要目的，其大部分器件的高度较小，因此，为提升整体的空间利用率，该单元包含的元件可以以薄为评价指标。

如上所述，负责发送信号给驱动电路或者开关器件的控制器（某些特定应用下，驱动电路也可视为控制器的一部份）及其外围必要的电阻电容等元件一

定包含在控制单元内。但随着控制芯片集成度的提升，这些元器件全部放置后，空间上可能仍有一定的盈余。因此，可以增加更多元器件于控制单元中。以图3为例，如果将功率器件全部放置于功率单元120，摆放示意如图17所示。图17左侧为功率单元120的元器件位置摆放图，右侧为控制单元130的元器件位置摆放图。图17中方框表示元器件所摆放的载板1710、1720，该载板1710、1720上放置的元器件，其中左图的标识对应于图3中相应的元器件。如图17，如果功率单元120及控制单元130面积相同，也即两单元的载板1710、1720面积大小相同，则控制单元130的使用率明显偏低。为提高各单元面积的使用率，可以从功率单元挪移部分元器件到控制单元130中，如图18，原边开关管S11、S12位于靠近控制单元侧面的位置，即放置于控制单元130的载板1720上。所移元器件的选择标准除了薄之外，还应当不影响电特性甚至有更好的作用。

高压输入侧的一次侧开关管S11、S12由于是半导体，其厚度可以跟控制芯片相当甚至更薄，有机会放置于控制单元中。以一次侧开关管S11和S12为Mosfet为例，如果将其置于功率单元，如图3所示，功率单元120与控制单元130间则会有4个以上引脚（每个开关的门极以及源极）相互联接；如果将其放置于控制单元130中，则控制单元130与功率单元间的连接只需2个引脚，例如图11中的一次侧开关管S11和S12连接点与开关管S12的源极。而且，由于高压输入侧对电路的分布参数并不特别敏感，因此将其移至控制单元130，对电特性的影响完全在可接受范围内。当然，如果一次侧开关管S11和S12挪移，那么输入电容器C1及其驱动电路也需跟着挪至控制单元130。这样就近放置不仅可以减少一次侧开关管S11和S12的电压尖峰，且可以在功率单元减少不必要的引脚。

图18所示为部分开关器件摆放至控制单元130的示意图。控制单元130包括输入电容器C1、谐振电容器C2与一次侧开关管S11、S12；功率单元120包括若干开关器件以及承载开关器件（如：S11、S12）的载板1710和包覆开关器件的绝缘封料3430（绘示于图34）；开关器件分布于靠近焊盘3440（绘示于图34）的位置。功率单元120包括变压器T1、谐振电感器L1、输出电容器C3与二次侧开关管S21、S22、S23、S24。可以看出，右侧控制单元130的利用率显着提升，而电感（即，谐振电感器L1）、电容（即，输出电容器

C3）及开关器件（即，二次侧开关管 S21、S22、S23、S24）位于载板 1710 上靠近功率单元侧面的位置。左侧功率单元 120 则可以给更多的空间给磁性元件，这对效率的提升有显着意义。因此，可以更好的兼顾高效率和高功率压强。值得留意的是，由于开关管 S11、S12 不在功率单元 120 内，功率单元 120 的输入来源于控制单元 130，并且是经过开关 S11、S12 管调制的高频交流功率信号，如 500KHZ 甚至是 3MHZ 以上，幅值可以是 12V 以下到甚至 400V 以上。

如果在某些应用中，二次侧开关管 S21、S22、S23、S24 的位置对电特性不敏感的话，也可以将二次侧开关管 S21、S22、S23、S24、驱动器 330 及输出电容器 C3、Oring MOS 等设置于控制单元 130 中，这样可以更充分利用空间。

如图 10 所示等堆叠结构，如果将控制单元 130 设置于下方，控制单元 130 位于功率单元 120 与主板 110 之间，则功率单元 120 输出端到主板的引脚变长，可能会影响对负载变化的响应能力，特别是在负载为诸如 CPU 这样的数据处理芯片时。这时，就可以在控制单元 130 设置部分主电路的输出电容器 C3（或者，亦可如图 11 中对应的 POL 输出电容 C4），控制单元 130 包括输出电容器 C3，从而减小该引脚长度的影响，如图 19 所示。当然，这要求在设计时，使得输出电容器 C3 与引脚 140 有部分良好连接。

上面所举的实施例中，控制单元 130 包含了一个载板，例如印刷电路板或者线架(Lead frame)等。当然，整个控制单元也可以用嵌入(Embedded)技术实现。控制单元 130 也可以采用单元内元件相互堆叠，利用元件表面导体进行电气连接的方式。用嵌入(Embedded)技术实现，也即部分电气元件，例如控制 IC、电阻、电容甚至功率半导体等埋藏于载板中。这样可以使得控制单元非常薄且面积小，而且可以实现较为精细的内部和单元表面线路布线。由于 Embedded 技术可以轻易且不受位置限制地实现上下表面的互联，也就是说，可以直接实现相应的 Pin 脚而无需像图 34 所示的以侧面出 Pin。拿含变压器和同步整流器的电路，如桥式谐振型电路为例，可以用 Embedded 技术实现控制单元后，与含变压器和同步整流器的功率模块堆迭，其具备如下特征：功率单元至少含一变压器（Core 和 Winding），输出同步整流器，部分输出电容，SR MOS 的控制信号(可功率模块自行产生也可以由控制单元提供)，以实现功率级的高效

率；功率单元仍选用侧面出 Pin，Pin 至少含输出的正负极，已经过调制的输入侧高频脉冲的两极。控制单元至少内嵌有控制逻辑 IC，负责采样、控制信号及驱动信号生成、保护、以及与电源外部的必要通信，含至少一对高压侧功率元件，并生成传递给功率单元的输入侧高频脉冲；控制单元的 Pin 脚可以侧面排布也可以按需在任意位置穿透上下表面排布，也可以按需由内向表面连接并在一表面排布；由于 Embedded 以后，控制单元可以很薄，如 1mm 左右，Pin 脚以 SMD 为主，以增强 Pin 的连接强度。由于 Embedded 技术，可以轻易实现类似于 PCB 的布线能力，可以在表面实现更加丰富的互联，能支持内容更加丰富的堆叠组合，如将另外一些较难嵌入到控制单元中的必要元件，如输入电磁干扰滤波器，即输入电容，与功率单元一起放置在控制单元表面。由于可以实现很小的体积，更适合高频工作场合，如工作频率达到 1MHZ 以上。因此，变换电路也以谐振型工作的电路为宜。Embedded 实现的控制单元厚度也在 2mm 以下为佳。

控制单元 130 可以是前面例子中所述的控制电路的集合，可以是控制电路包含部分功率电路的元器件，甚至驱动电路，也可以是，如图 7 等所示的一个具备完整功能的电源变换器。这样，控制单元与功率单元堆叠，并通过引脚互相连接甚至通过引脚与主板连接的结构就变成了两个或多个功率单元互相堆叠的结构。只是其中至少一个功率单元内包含了控制单元的元器件。这种结构通常适用于多级功率单元并联或级联等系统架构中。

功率单元可涵盖的内容

总体来讲，功率单元可以是一个完整可独立工作的 DC/DC 或 AC/DC 电源变换器，如：隔离变压模块 DCX、负载点直流变换器 POL、前级调压模块 FRM、调节母线变换器(Regulated Bus Converter, RBC)、功率因数校正电路、辅助电源模块等即一个包含了功率级电路及控制电路的电源变换器，也可以只是它们的功率级电路，甚至如前面实施例中只是功率级电路中的一部份，例如最需要相互就近放置的那部分，如图 18 的变压器 T1、输出整流元件（如，二次侧开关管 S21、S22、S23、S24）及输出电容器 C3 这三个关键元件。功率单元可以像隔离变压模块 DCX、RBC 一样具备隔离的能力，即至少含一个变压器，也可以像负载点直流变换器 POL、前级调压模块 FRM、功率因数校正电路一样无需隔离，即至少含一个电感器。

功率单元上的变压器和电感器可以是集成在一起的，也可以是独立的。

功率单元的输入可以是直流，也可以是工频的交流，也可以是如图 18 高频的交流。

功率单元的输出可以是 0.1～12V，12V 以上到 400V 的各种电压范围。负载可以是其他电源变换器、硬盘、内存、图形处理芯片、CPU、通信 ASIC 等等各种数据处理芯片。

此外，功率单元与控制单元一样可以包含一个载板，如印刷电路板或者线架等，通过载板上的走线(trace)实现功率单元器件间的电气连接，功率单元中的元器件可以摆放在载板上；也可以采用嵌入(Embedded)技术实现，也即部分电气元件，例如电阻，电容等埋藏于载板中。此外，功率单元也可以采用单元内元件相互堆叠，利用元件表面导体进行电气连接的方式。

当整个电路包含了两个或多个功率单元时，可以像图 19 由完全相同的功率单元进行并联已实现更大功率更大电流变换，或者是串联实现更大功率更高电压变换；也可以像图 8 一样，由不同的功率单元进行串联，实现更大的工作范围；或者由不同的功率单元，实现共用一个输入，提供多个输出的电源变换功能；或者由不同的功率单元，实现提供一个输出，接受多个输入的电源变换功能。

综上所述，本发明的使用范围非常广泛，可以协助服务器实现更高的性能。当然，本发明涉及的电源变换器实现方法，也可以适用于其他应用场合。

堆叠结构设计

本发明的一方面，是在服务器中，通过将一个电源变换器，分解成至少两个单元，即至少一个控制单元 130 和一个功率单元 120，再通过堆叠的方式，来更充分利用空间高度，实现高效率高功率压强的电源变换器，以实现更高性能的服务器。电源变换器堆叠的形式可以有如下几种。

1. 如图 19 所示，各单元 120、130 面积相当，上下直接堆叠后组成一电源变换器，再设置于主板 110 之上。

2. 如图 20 所示，控制单元与功率单元中面积较大者作为第一单元 2010 而面积较小者作为第二单元 2020，第一单元 2010 位于第二单元 2020 与主板 110 之间，各单元面 2010、2020 积有差异，面积小的堆叠放置于面积大的之上组成一电源变换器，再设置于主板 110 之上。如图 21 所示，控制单元与功

率单元整合成隔离变压模块 DCX、前级调压模块 FRM，此为上述前级调压模块 FRM+隔离变压模块 DCX 架构的实现方式之一，只是为了得到更高的效率，将前级调压模块 FRM 的电感器 L 外置。将前级调压模块 FRM 及其外置电感器 L 设置于隔离变压模块 DCX 的上方后，组成一电源变换器，再设置于主板 110 之上。

3. 如图 22 所示，控制单元与功率单元中面积较大者作为第一单元 2010 而面积较小者作为第二单元 2020，第二单元 2020 位于第一单元 2010 与主板 110 之间，各单元 2010、2020 面积有差异，小的放置于大的下表面，组成一电源变换器，再设置于主板 110 之上。

4. 如图 23 所示，功率单元 120 与负载位于主板 110 的同一面，控制单元 130 位于主板 110 与功率单元 120 相对的另一面，功率单元 120 与控制单元 130 分别位于主板 110 的两相对表面，亦即将各单元 120、130 分别放置于主板 110 的上下表面，控制单元 130 通过主板 110 中的导电贯孔 2310 电性连接引脚 140，单元之间的投影面积重合的部分至少占本单元投影面积的 1/3。显然，为了散热和厚度的限制，控制单元 130 设置于主板下表面，功率单元 120 设置于主板 110 上表面为佳。

很显然，如上各种实现方式，均可有效利用高度，兼顾电源变换的高效率和高功率压强，实现更高性能的电源模块，尤其是在服务器电源的应用场合中。

焊盘布置和实现

一个电源变换器的引脚有很多。涉及到变换器与系统连接的引脚如变换器功率输入输出引脚，与系统的通信引脚，及内部互联即功率单元及控制单元间相互连接的引脚等。由于引脚在本申请中为其他的定义，在此处，载板上元器件的引出脚称之为焊盘。图 24，从电流量上来分，通常分为功率焊盘和信号焊盘两大类。功率焊盘是指变换器功率电流流过的焊盘，通常为功率电路中元器件间进行电气连接，它由于流过的电流大，焊盘通常比较粗，也即焊盘的截面积比较大。而信号焊盘则为变换器中传递信号的焊盘，例如，控制单元中的控制电路通常通过信号焊盘传递控制信号给驱动电路以控制功率元器件的导通及关断。通常控制焊盘流过的电流较小，焊盘比较细，则无需过大截面积，其尺寸由工艺能力决定。

当电源变换器为一隔离的电路时(隔离通常由功率电路中的变压器来实

现)，也即其输入输出有隔离安规电压要求。所以，焊盘按位置可分为一次侧群焊盘(即位于变压器一次侧的焊盘)和二次侧群焊盘(即位于变压器二次侧的焊盘)。这两个群焊盘需要让开一定的距离以符合安规的要求，例如为当变换器的输入为 400V 时，由于需要绝缘 2000V 以上，每个群中任意一个焊盘与另一群中任意一焊盘间至少相距 4～8mm 间距；而当输入为 36～72V，通常需要满足的安规绝缘电压为 1500V，则间距为 1～4mm。而一次侧群，由于输入相对高压，电流较小，焊盘的截面积相对较小。二次侧群则由于电压低，电流大，焊盘截面积相对较大。如 48V 转 1V，电流差异 48 倍，如果用同样电流密度来定义焊盘体积的话，就会差 48 倍，二次侧群显然需要更多的位置摆放。

功率单元四周都可以摆放焊盘，如图 24 和图 25 所示。图 24，一次侧群焊盘 2410 和二次侧群焊盘 2420 各占功率单元的两边，且两边相互平行，一次侧群焊盘 2410 包括第一信号焊盘 2411 与第一功率焊盘 2412，第一功率焊盘 2412 的截面积大于第一信号焊盘 2411 的截面积，二次侧群焊盘 2420 包括第二信号焊盘 2421 与第二功率焊盘 2422，第二功率焊盘 2422 的截面积大于第二信号焊盘 2421 的截面积，第二功率焊盘 2422 的数量多于所述第一功率焊盘 2412 的数量。图 24 的方式适合输出电流较低的场合。图 25 则适合大电流输出的应用，一次侧群焊盘 2410 分布于单元的一条边上，二次侧群焊盘 2420 分布于单元的剩下三条边，并与一次侧群焊盘 2410 让开一个安规距离 d。当电流比较大，同一个电气极性，需要使用多个焊盘时，也即复用焊盘时，通常可以采用正负极交错排列，例如：Vo+、Vo-，以实现尽量低的焊盘感抗，以便在应用类似于 CPU 负载时，有更好的动态响应，减少主板的电容使用量。

在本申请中，引脚是与焊盘电性连接的。图 26 显示的是引脚与焊盘连接并实现各单元互联后的正视图。图 26 例举的引脚为表面贴装引脚。该 L 型的表面贴装引脚 2610 将各单元 120、130 进行电连接后，组成表面贴装引脚的电源变换器，设置于主板 110 之上。而改用 I 型引后，则可实现如图 27 的 I 型的直插引脚 2710 的电源变换器。图 28 显示的是该电源变换器组装过程。先将各单元 120、130 堆叠后，将各引脚 2710 分别焊接至各单元 120、130 的焊盘，组成相应的电源变换器。

图 29 则显示的是另一种方式。即各个单元 120、130 先拥有属于自己的引脚，均以表面贴装引脚，且同一个引脚上下表面均有表贴式垫片（SMD Pad）

2910，每一引脚 140 的两端具有表贴式垫片 2910 延伸至对应的单元 120、130 的上、下表面，使焊接牢固和减少垫片导电损耗。这样就可以将各单元通过 SMD 焊接流程组装在一起形成表面贴装引脚的电源变换器。图 30 显示的则是将最下方的单元（如：控制单元 130），直插引脚 3010 在单元的表面为表贴式引脚，下方则出直插式接脚,这样就可以组成直插引脚的电源变换器。具体而言，多个引脚 140、140’中具有至少一引脚 140 设置于控制单元 130 与功率单元 120 中最接近主板 110 的单元（如：控制单元 130）的侧边，至少一引脚 140 的一端具有直插引脚 3010 插设至主板 110 中，至少一引脚 140 的另一端具有表贴式垫片 2910 延伸至最接近主板 110 的单元的上表面；多个引脚 140、140’中每一其余引脚 140’的两端具有表贴式垫片 2910 延伸至功率单元 120 与控制单元 130 中其余单元（如：功率单元 120）中对应者的上、下表面。简言之，引脚 140’为表面贴装引脚，直插引脚 3010 配合表面贴装引脚实现功率单元 120/控制单元 130 与主板的 110 电性连接，且利于安装。于一实施例中，功率单元 120 包括主功率单元部分（如，较下方的功率单元 120）和次功率单元部分（如，较上方的功率单元 120），主功率单元部分的侧面分布焊盘 3340（绘示于图 34），次功率单元部分堆叠于主功率单元部分。图 31 显示的则是组装的过程。先将各单元 120、120 与各自的引脚 140 组装后，在将各单元 120、120 组装在一起。

图 32 则显示的是，控制单元与功率单元整合成第一单元 2010、第二单元 2020 与外置电感器 L，第一单元 2010 位于第二单元 2020 与主板 110 之间，引脚 140 的一端具有直插引脚 3010 插设至主板 110 中，引脚 140 的另一端具有表贴式垫片 2910 延伸至第一单元 2010 的上表面，第一单元 2010 的下表面设有表面贴装引脚 3210 去连接主板 110，在下方单元（即，第一单元 2010）的上表面进行一定的布线，实现堆叠在其上表面的多个单元之间的相互电连接。也可以在下方单元的下表面，出更多的表面贴装引脚 3210，实现其侧面和下表面同时出引脚，以更充分利用空间，特别是面积很小的场合，如小于 1/32 砖，以便有足够空间布置引脚。图 33 显示的是，引脚 140 的两端具有表贴式垫片 2910 延伸至第一单元 2010 的上、下表面，第一单元的下表面设有表面贴装引脚 3210 去连接主板 110，该电源变换器直插引脚和表面贴装引脚复用的方式，以满足某些场合需要功率焊盘以直插形式的需求。

如上，表面贴装引脚具体实现时，需要保证各引脚 140 的平整度以方便组装和客户使用。因此，以图 31 为例，在组装引脚之前，如果各单元 120、130 表面规则，将更有利于组装引脚。那么，可以在组装引脚 140 前，将各单元 120、130 用 Molding(塑封)、Embedded(埋入)等封装工艺包覆起来，形成有规则的表面，例如图 31 所示的平面，或者图 34 所示的凹部 3410，由于绝缘封料 3430 上设有配合引脚 140 安装的凹部 3410，更有利于空间的精细使用，再在其上安装表面贴装引脚。具体而言，控制单元与功率单元中任一者具有载板 3420 与绝缘封料 3430，绝缘封料 3430 形成于载板 3420 的两相对表面，载板 3420 的侧面具有焊盘 3440，焊盘 3440 上的焊料 3450 焊接至引脚 140。绝缘封料 3430 的上、下表面的边缘具有凹部 3410，引脚 140 的两端具有表贴式垫片 2910 延伸至上、下表面的凹部 3410，凹部 3410 上具有胶料 3460 黏着于表贴式垫片 2910。

图 34 所示的单元可为上述的功率单元与/或控制单元，焊盘 3440 分布于功率单元的侧面和控制单元的侧面，引脚 140 与焊盘 3440 电性连接。引脚 140 为表面贴装引脚，分布于功率单元和控制单元的外表面并与焊盘 3440 电性连接。焊盘 3440’ 还分布于功率单元与焊盘 3440 所在侧面垂直的面，虽然图 34 中焊盘 3440’ 只分布于下表面，但此不限制本发明，于一实施例，焊盘分布于功率单元 120 的侧面和控制单元 130 的上下表面，引脚 140 与焊盘 3440 电性连接。

表面贴装引脚可以安装在单元的各个面上，但为得到更好的散热效果及使模块整体体积更小，以上例举的为焊盘位于各单元中载板的侧面，与表面贴装引脚进行焊接等工艺以便电连接单元中器件的引出脚和控制信号引出脚。然而在有些特殊情况下，如图 33，第一单元 2010 的焊盘也可在其第二单元 2020 和电感 L 堆叠的表面制作焊盘，通过引脚实现第一单元 2010 与第二单元 2020 和电感 L 之间的典型连接。引脚与焊盘的焊点之外的接触面，则可以使用胶水等工艺，将贴式引脚粘结于各单元的表面，以加强机械强度，提升可靠性。

散热处理

各单元堆叠成模块后，相比较于原先独立摆放设计的方式，散热途径发生了变化。

如图 35 所示，堆叠后上下各单元之间可以根据需要，留出足够的间隙，

作为风道使用，换言之，控制单元 130 与功率单元 120 中任两相邻单元之间具有间隙以作为风道 3510。上下单元间距即风道厚度应该在 1～5mm 之间，少则散热效果不好，多则占用更多空间从而使模块体积变大。这样就可以尽量使用各单元的自身表面进行热交换。为达到有效散热，风道中的风速应该在 0.5 米/秒以上。

在很多应用中，可能较难给图 35 中的风道 3510 提供足够风速。因此，还是希望将热传递到整体堆叠后的各个表面。为更好的实现热均匀，可以在单元间空隙处填充导热绝缘胶，如图 36 所示，控制单元 130 与功率单元 120 中任两相邻单元之间的间隙被导热绝缘胶 3610 给填充，功率单元 120 之间、功率单元 120 与控制单元 130 之间填充有导热绝缘胶 3610。为有效实现导热能力，该导热绝缘胶的导热系数应当大于 1W/m.k。也可以在本需互联部分填充金属板，如铜板，以得到更好效果。而填充的面积该在该表面的 30%以上。当然，导热绝缘胶及金属板可以一起填充。

如图 37 所示，功率单元 120 中设有横向导热载板 3730（如：PCB），引脚 140 的两端具有引脚延伸层 3710 延伸至功率单元 120 与控制单元 130 中对应者的上、下表面，该上、下表面中至少一面被引脚延伸层 3710 占据 30%以上的面积，位于各单元下表面的引脚延伸层 3710 下方具有导电焊接材料 3720，换言之，功率单元 120 与控制单元 130 电性连接的引脚之间以及功率单元 120 与功率单元 120 电性连接的引脚之间填充有导电焊接材料 3720，导电焊接材料 3720 只在需要互联的地方进行焊接，各单元间电连接是可以通过此焊接方式达成的。焊接料的导热系数通常足够高。因此，可以将各表面贴装引脚的表面积增大，从而实现单元间隙间更多的金属填充，以实现热均匀。为达到有效散热，引脚的面积应当占该表面的 30%以上，举例而言，表面贴装引脚覆盖功率单元 30%以上外表面积，从而为高发热的功率单元进行有效率的散热。

此外，显然，各单元的热越均匀，各散热手段就越有效。而实际上，各单元的热点无法达到理想的均匀分布，因此，需要具备更好的热扩散能力。各单元中的电信号传递载板，通常含有导热导电的良导体，如铜或者银等。如果在设计时，让载板的金属含量尽量高，则有利于热的扩散，特别是横向扩散。因此，在本发明中，热比较集中的单元中的载板，金属含量应该在 10%以上。同理，如图 22-5，客户的电信号载板，如果金属含量也在 10%以上，那么有利

于将电源变换器传递给它的热扩散到更大的面积，实现更好散热。

当然，高横向导热载板更有利于横向热扩散。各单元特别是损耗较大，发热比较明显的单元，例如功率单元，其覆盖/包覆材料如果可以是高导热绝缘胶，则会有利于上下垂直的热扩散。如使用导热系数在 1W/m.k 以上的覆盖/包覆材料。可以在包覆材料中添加陶瓷颗粒来实现。如添加陶瓷颗粒的塑封料。

如图 38，可以通过将各引脚 140 在侧面和上表面，扩大占用的面积，来实现更好的热交换能力。其覆盖面积，至少有一面占其所在单元所在面的 30%以上，尤以 50%以上为佳。此外，为了具备更好的扩散能力，引脚的平均厚度，应当在 0.2mm 以上，尤以 0.3mm 以上为佳。

图 39 和 40 则显示散热单元的安装方式。如图 39，电绝缘的散热单元 3910 设置在功率单元 120 上，功率单元 120 设置在控制单元 130 上，控制单元 130 设置在主板 110 上；或者，如图 40，电绝缘的散热单元 4010 设置在功率单元 120 与控制单元 130 的侧边。可以安装在组装后模块的上表面也可以安装在侧面。为避免影响电性能，该散热单元可以为电绝缘材料，如陶瓷。或者为导电材料，如铝、铜、石墨时，需要与引脚间有导热电绝缘材料，如陶瓷片等。散热单元均安装于焊盘或者引脚组合上方。为保证散热效果，散热单元与焊盘或者引脚组合之间的热阻应当小于 5 摄氏度/瓦。散热单元与焊盘或者引脚组合之间有绝缘材料。

其他优化实施例

在上述各实施例中，曾提到，可以通过多个功率单元堆叠来实现更大功率。这些功率单元通常会各自使用工作状态类似的磁性元件，如变压器或者电感。如图 41，功率单元 120 的数量为多个且堆叠于控制单元 130 上，每一功率单元 120 中均设有磁芯（Core）4110 及其绕组（Winding）4120，换言之，各磁性元件拥有类似的绕组和类似的磁芯。而实际上，其堆叠接触部位的两个横向柱中的磁通是有机会量相当而方向相反的。因此，可以用图 42 的方法，即功率单元 120 各包括一平面变压器，两个平面变压器共用一个磁芯 4210，这样就可以去掉堆叠接触部位的横向柱，既明显降低了高度，又减少了磁芯损耗，实现了效率和功率密度的双丰收。

更近一步的优化如图43所示。由于磁性元件通常有气隙4320，而气隙4320漏出的磁通通常会对附近的导体进行感应加热而产生损耗。可以通过在堆叠时

共用磁芯 4310，磁芯 4310 的气隙 4320 设置于功率单元 120 之间的堆叠间隙 4330，就可以将气隙尽量避开导体，减少损耗。

以上所举实施例，功率单元与控制单元上下堆叠形成电源模块。事实上，该电源模块翻转 90 度后，即变成功率单元与控制单元左右堆叠，通过引脚进行彼此间以及彼此与主板间的电气连接，这种结构也能够得到很好的应用。因此，本发明功率单元与控制单元间不仅可以上下堆叠还可以在水平方向上进行左右堆叠。

综上，通过本发明所揭露的 Quasi-Cascade 器件、驱动优化、应用优化及封装优化，可用以提升电源变换器功率密度或者效率，可以获得与现有技术相比，更佳的电性能，高频性能与更高的可靠性。其可充分挖取器件的特性，采用封装方案后使用方便，非常有利于提高变换器功率密度或者效率。而本发明给出的具体驱动、应用、封装的实施方法，也非常可行有效。本发明非常适合用以提升电源变换器的整体性能和性价比。

虽然本发明已以实施方式揭露如上，然其并非用以限定本发明，任何熟悉此技艺者，在不脱离本发明的精神和范围内，当可作各种的更动与润饰，因此本发明的保护范围当视所附的权利要求书所界定的范围为准。

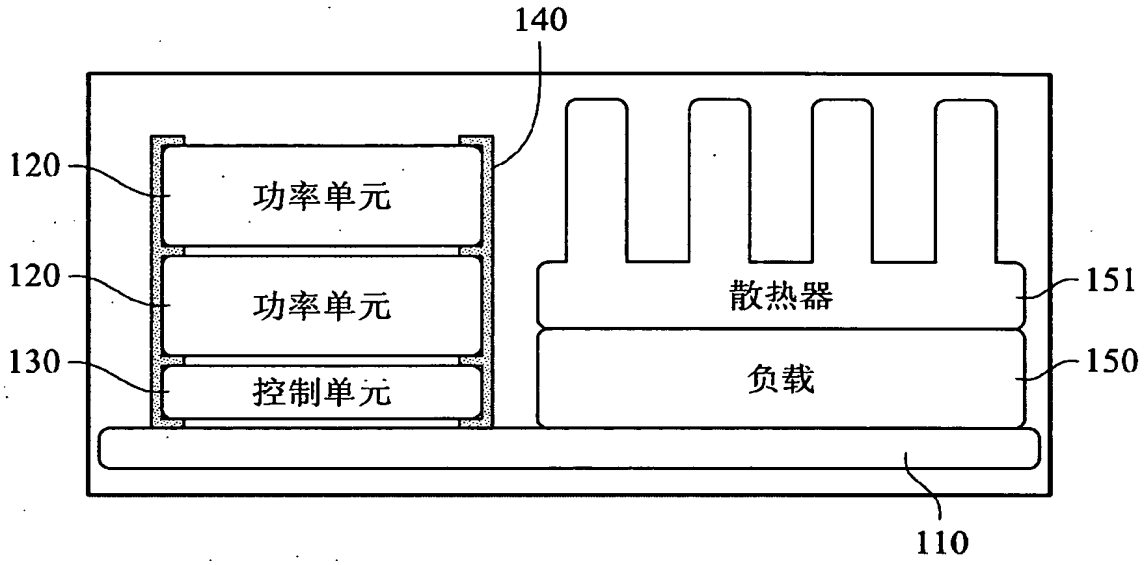

140
120
功率单元
120
功率单元
130
控制单元
散热器
151
负载
150
110

图 1

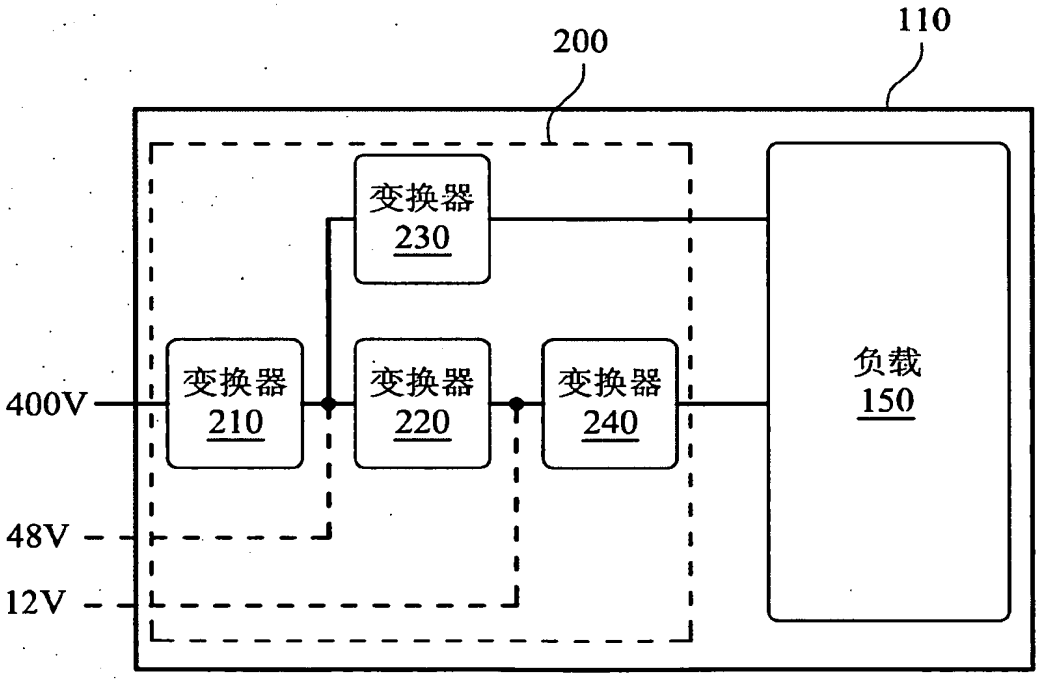

110
200
变换器
230
变换器
210
变换器
220
变换器
240
负载
150
400V
48V
12V

图 2

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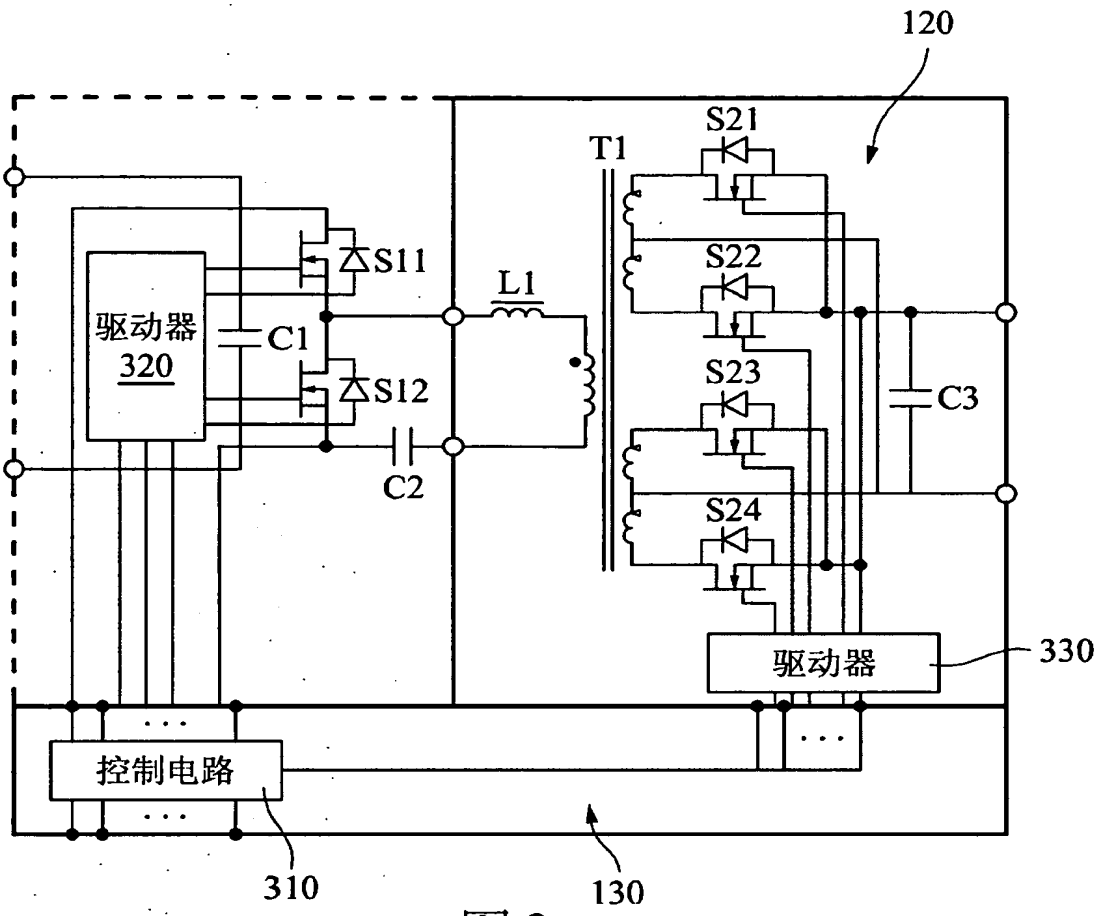


图 3

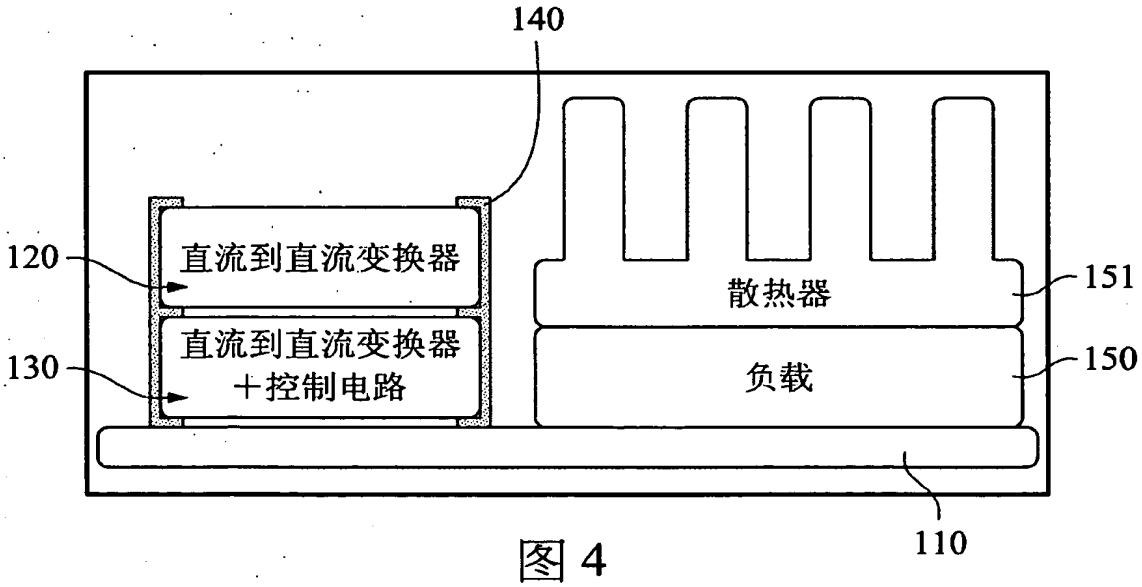


图 4

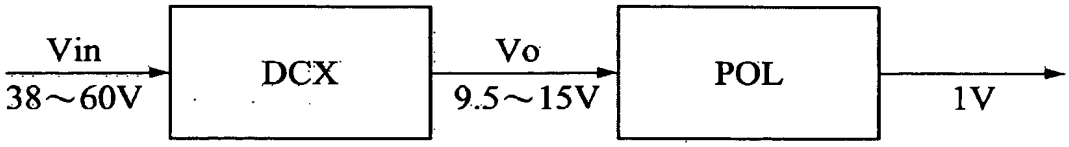

Vin
38～60V
DCX
Vo
9.5～15V
POL
1V

图 5

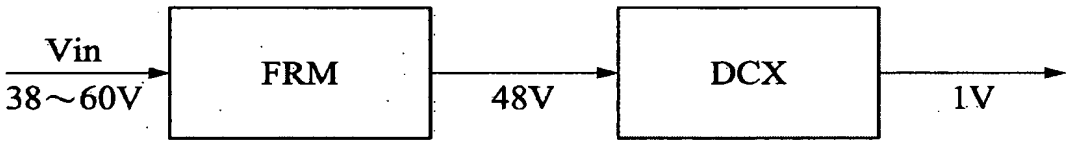

Vin
38～60V
FRM
48V
DCX
1V

图 6

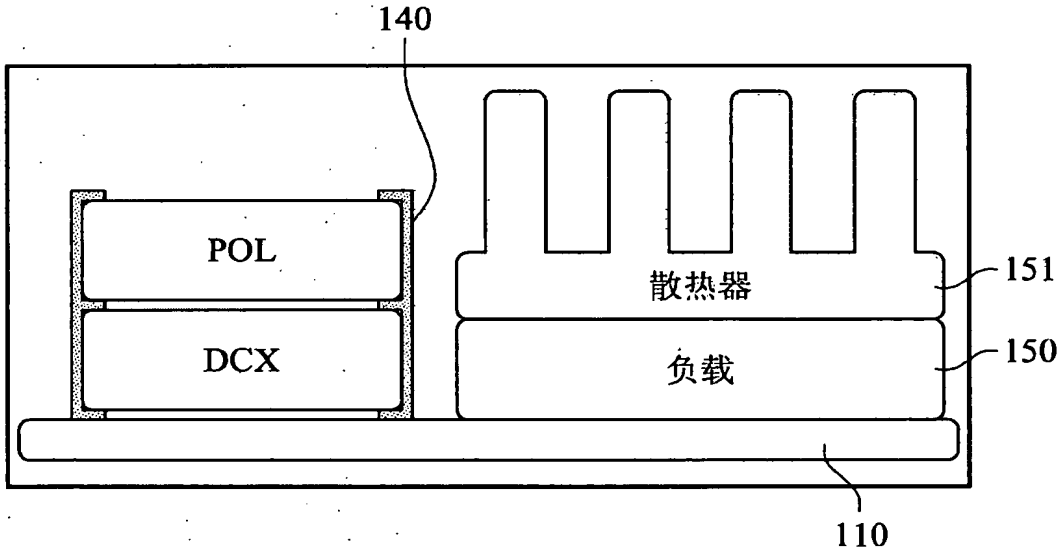

140
POL
DCX
散热器
负载
151
150
110

图 7

2014104429726

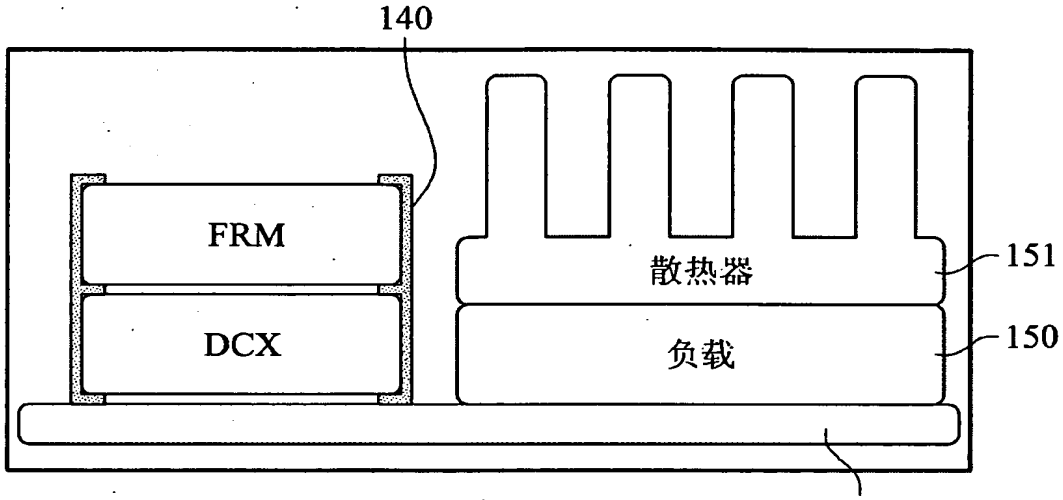


图 8

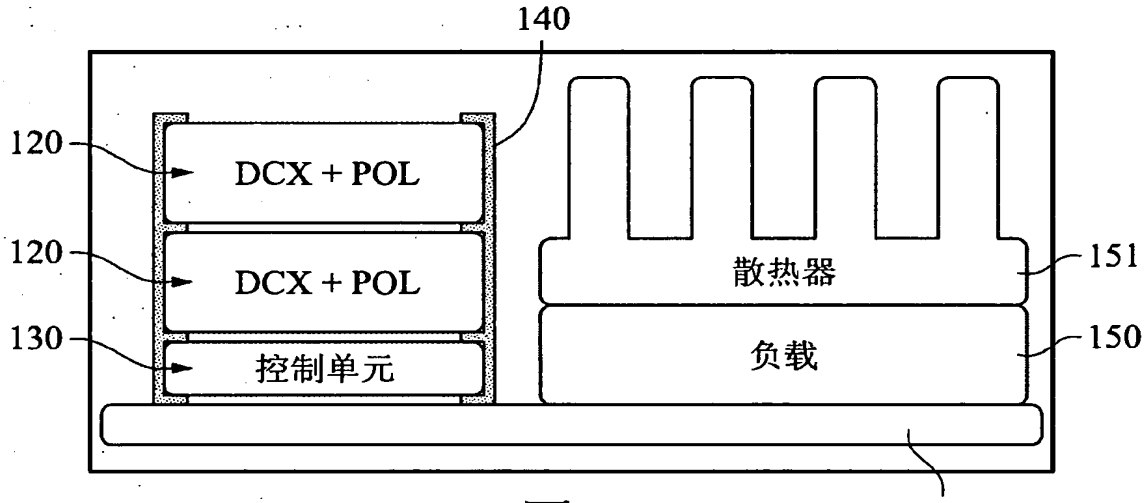


图 9

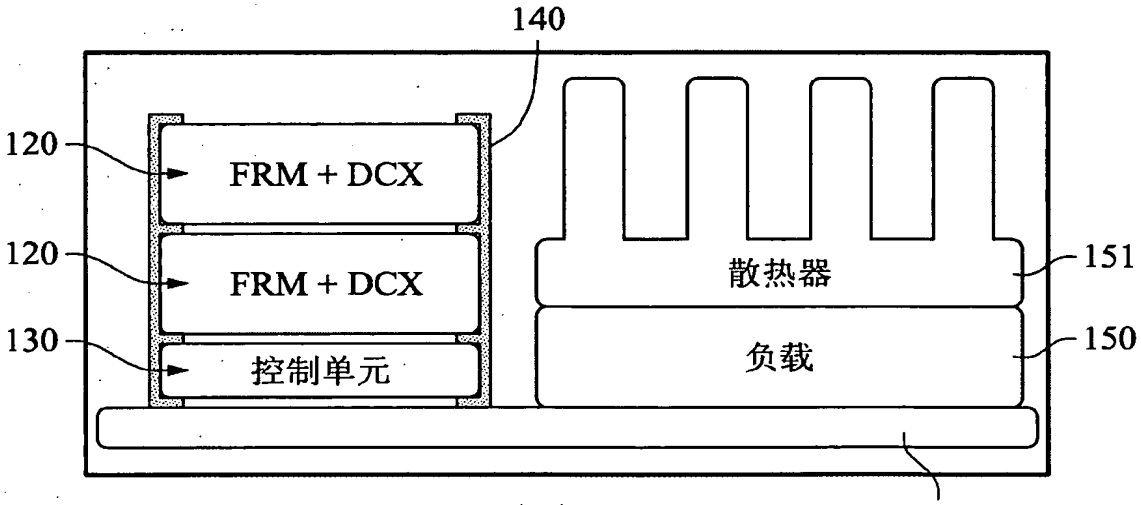


图 10

2014104429726

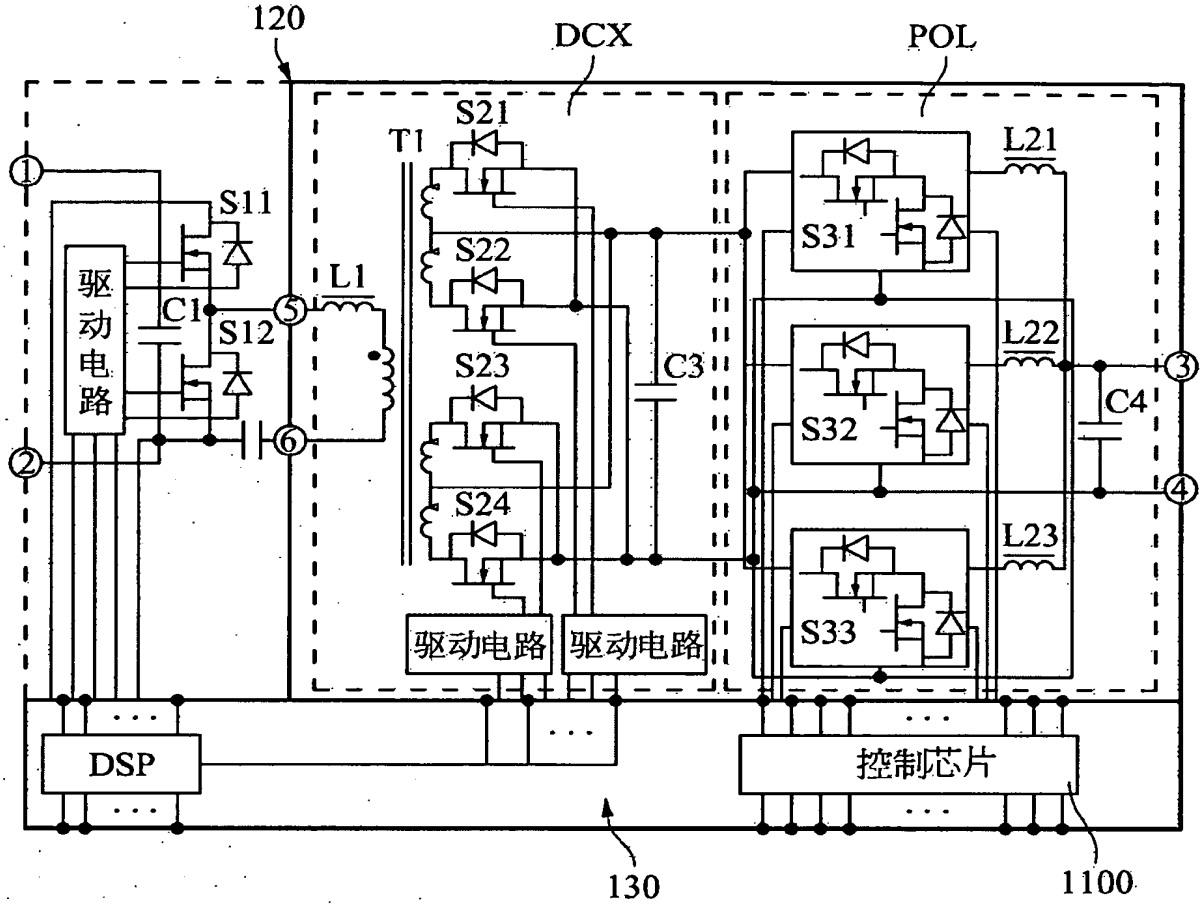


图 11

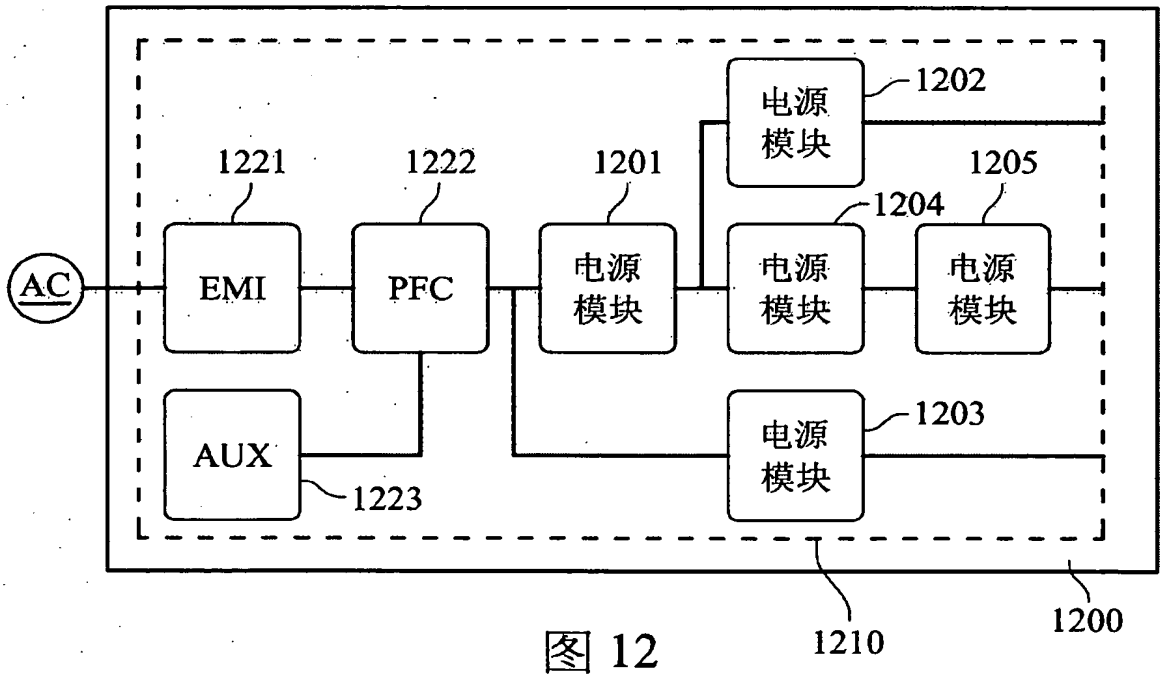


图 12

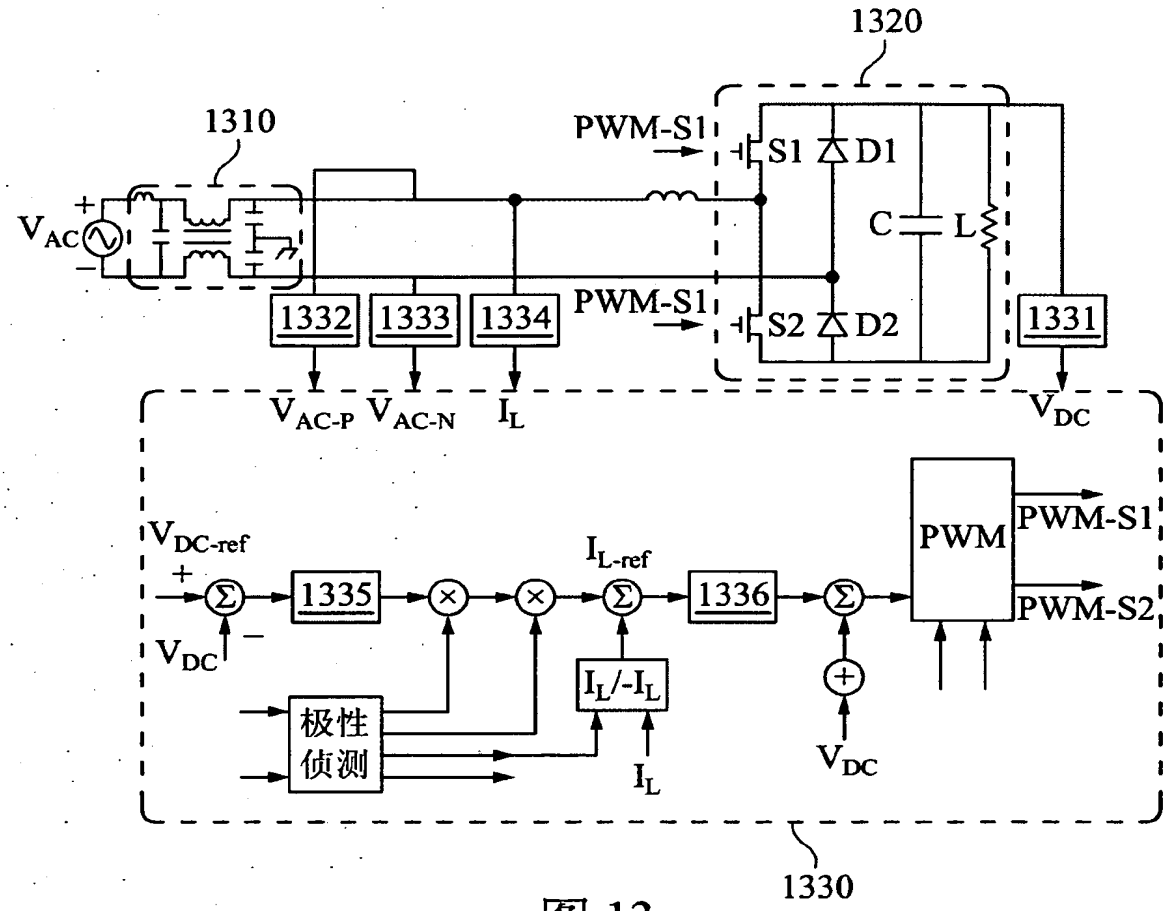

1320
1310
PWM-S1
S1
D1
C
L
V_{AC}
PWM-S1
S2
D2
1332
1333
1334
1331
V_{AC-P}
V_{AC-N}
I_L
V_{DC}
V_{DC-ref}
I_{L-ref}
PWM
PWM-S1
PWM-S2
1335
1336
V_{DC}
$I_L/-I_L$
极性
侦测
I_L
V_{DC}
1330

图 13

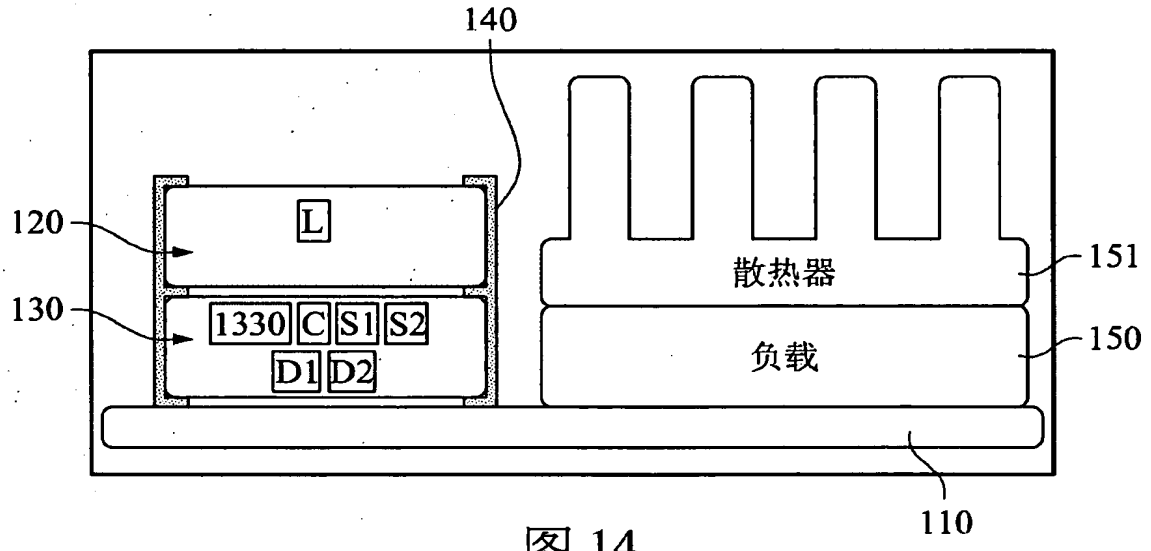

140
120
L
130
1330
C
S1
S2
D1
D2
散热器
151
负载
150
110

图 14

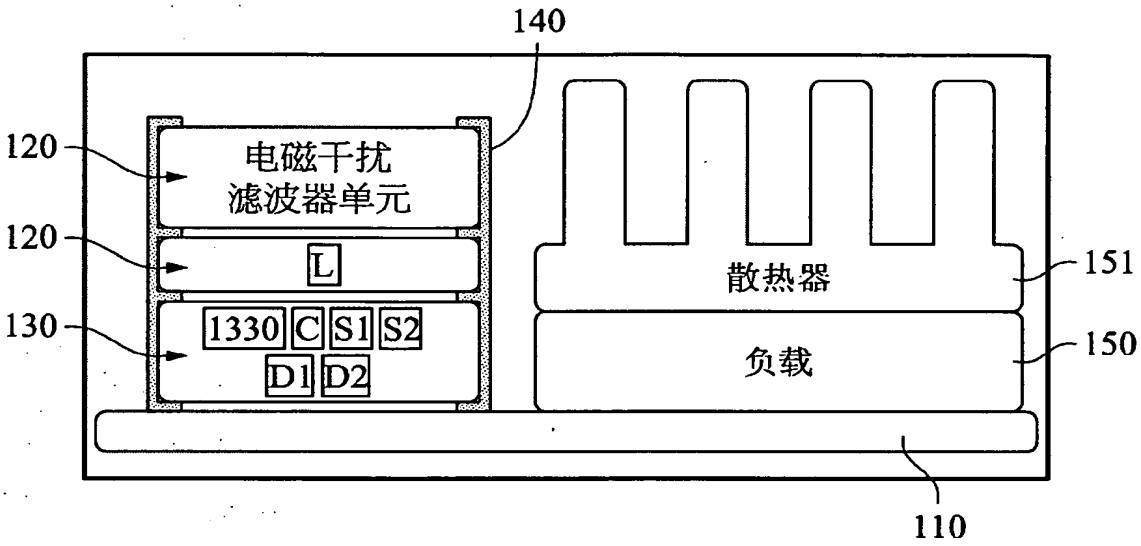

140
120
电磁干扰
滤波器单元
120
L
130
1330
C
S1
S2
D1
D2
散热器
151
负载
150
110

图 15

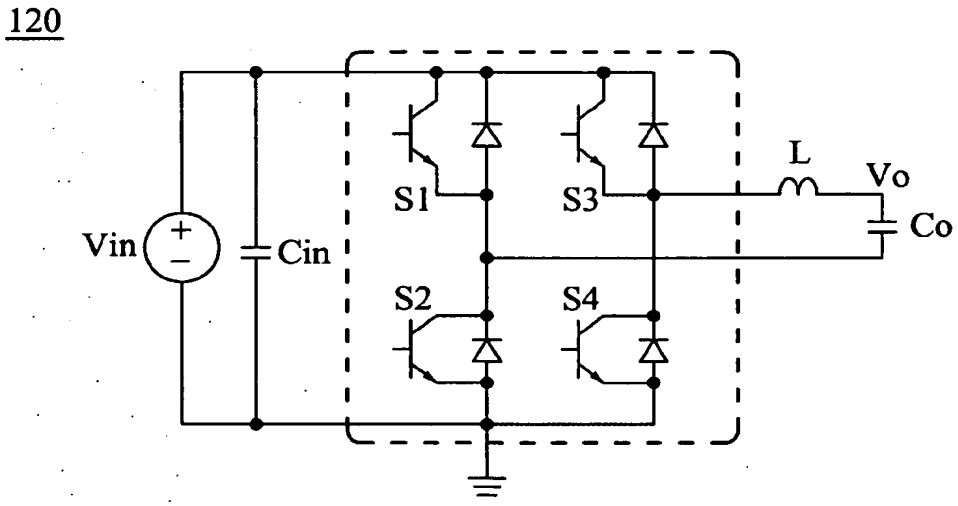

120
Vin
Cin
S1
S3
S2
S4
L
Vo
Co

图 16

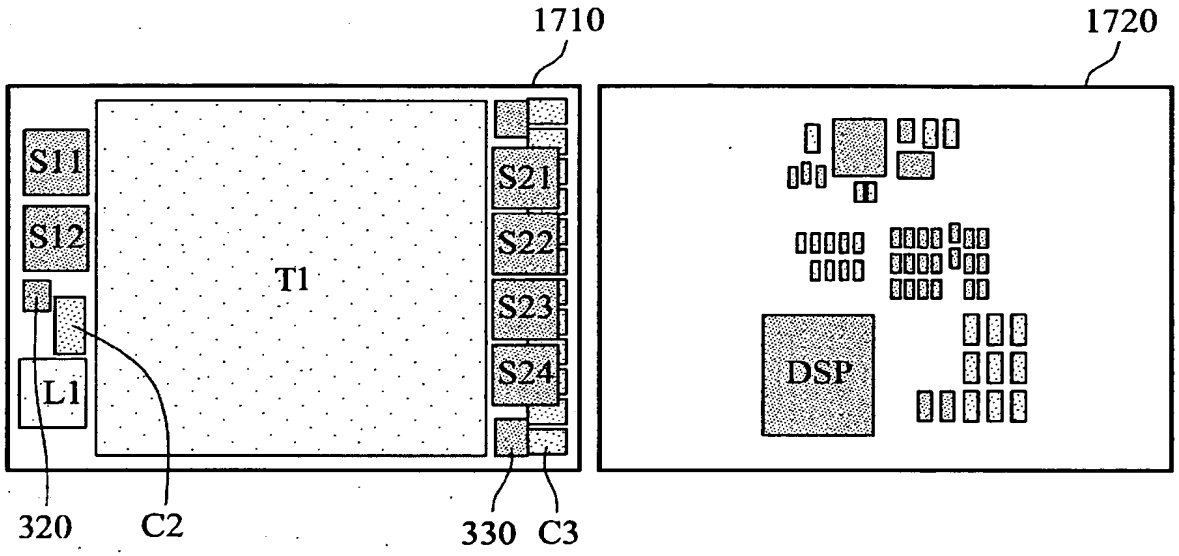

1710
1720
S11
S12
T1
S21
S22
S23
S24
L1
DSP
320
C2
330
C3

图 17

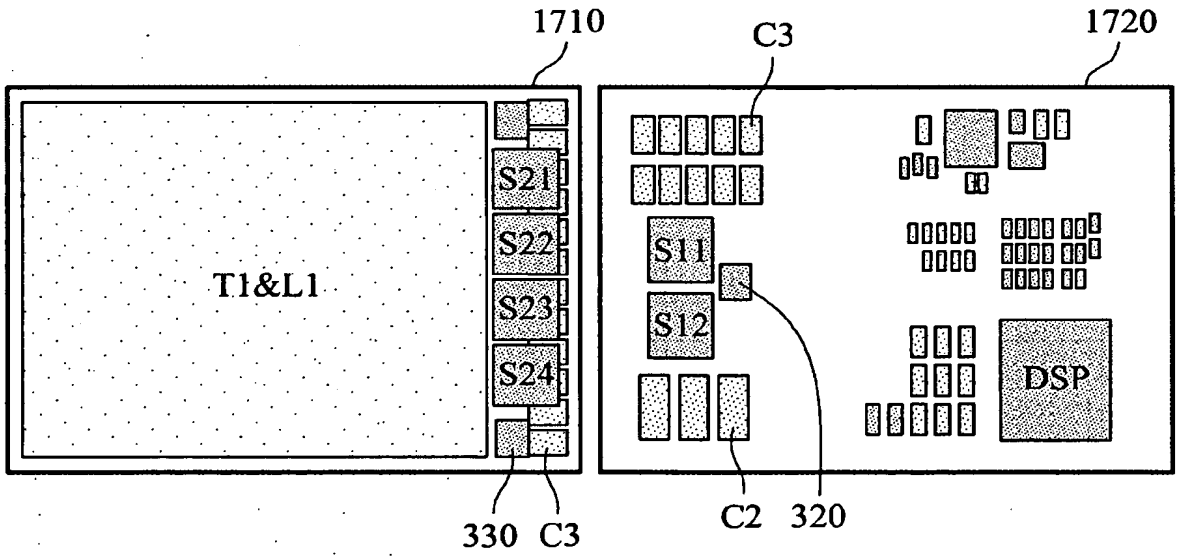

1710
C3
1720
T1&L1
S21
S22
S23
S24
S11
S12
DSP
330
C3
C2
320

图 18

2014104429726

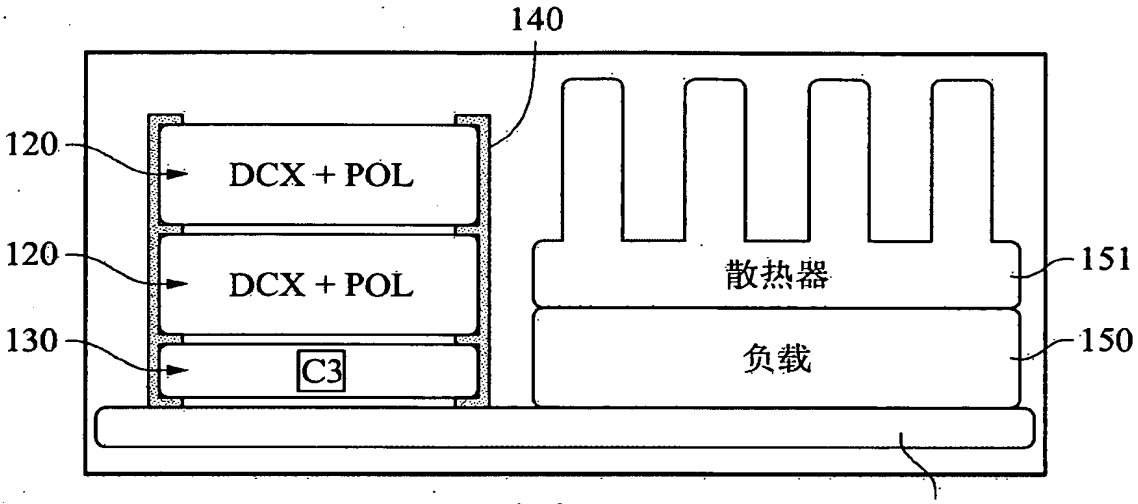


图 19

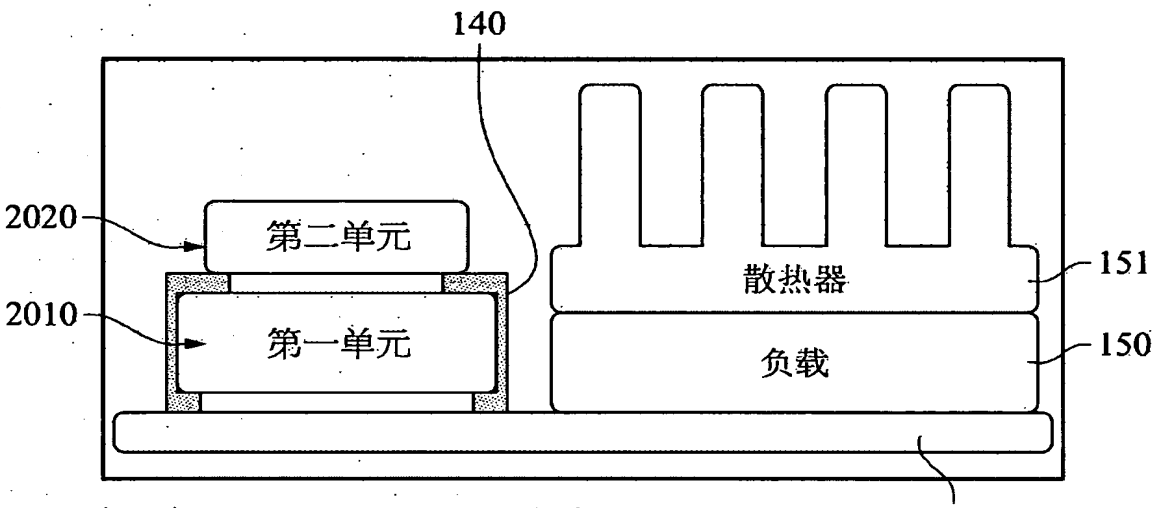


图 20

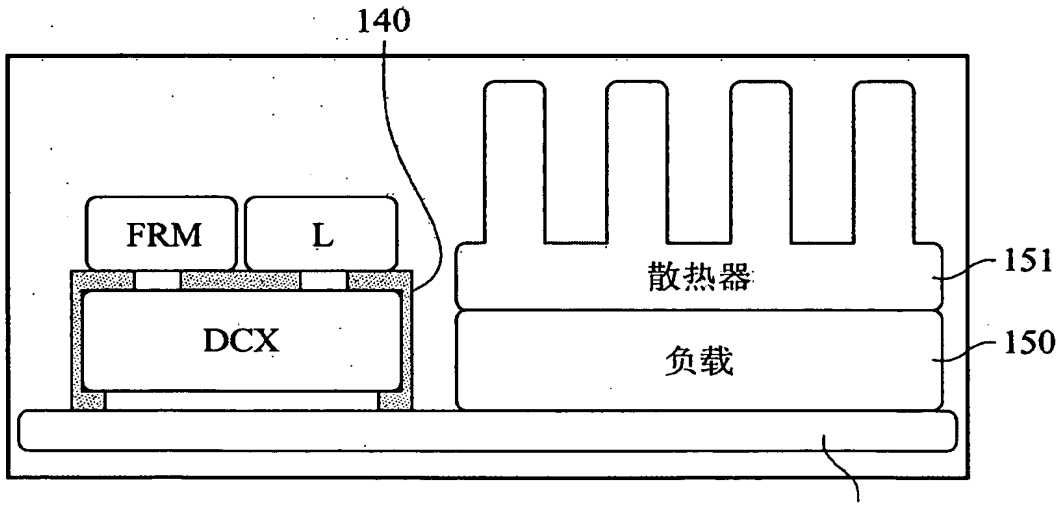


图 21

2014104429726

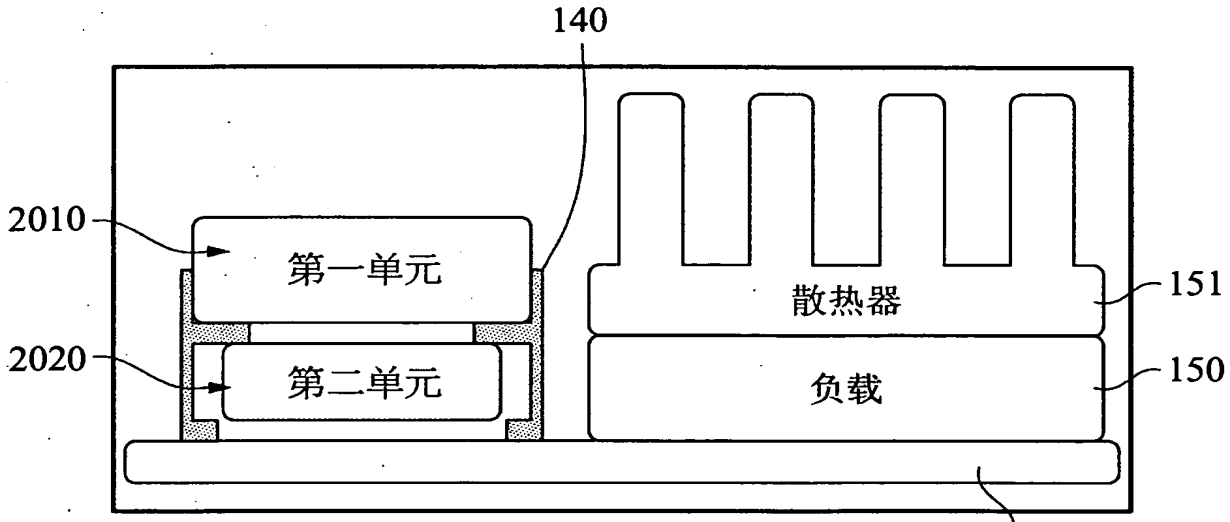


图 22

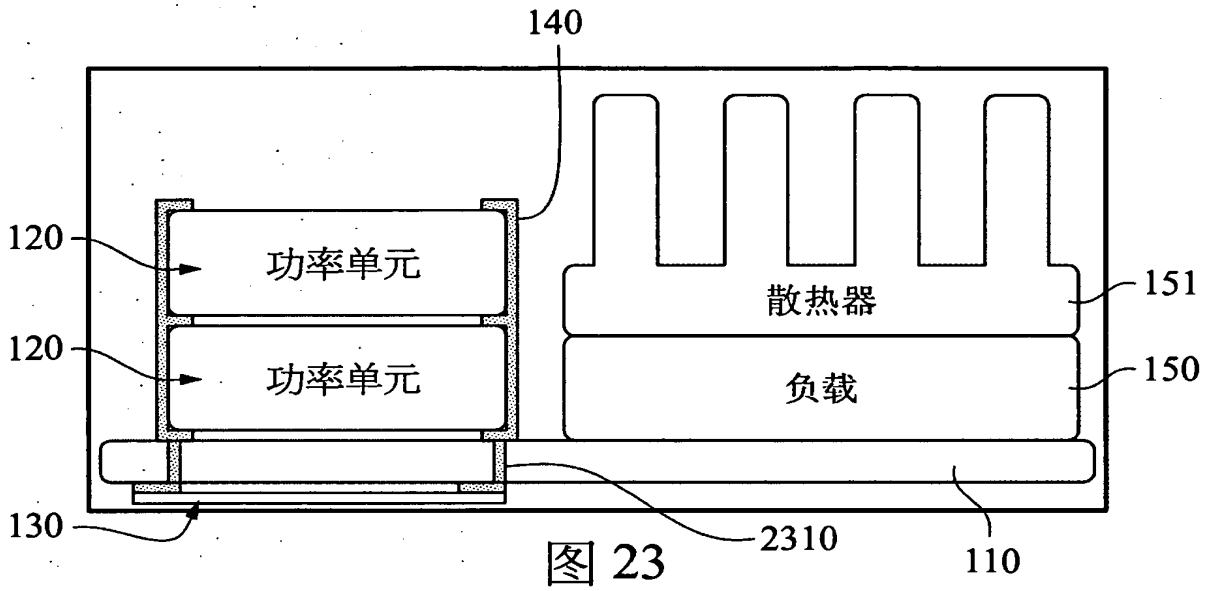


图 23

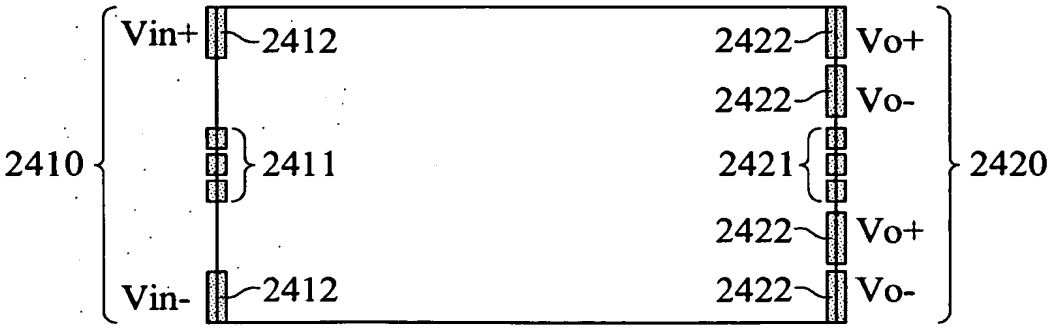


图 24

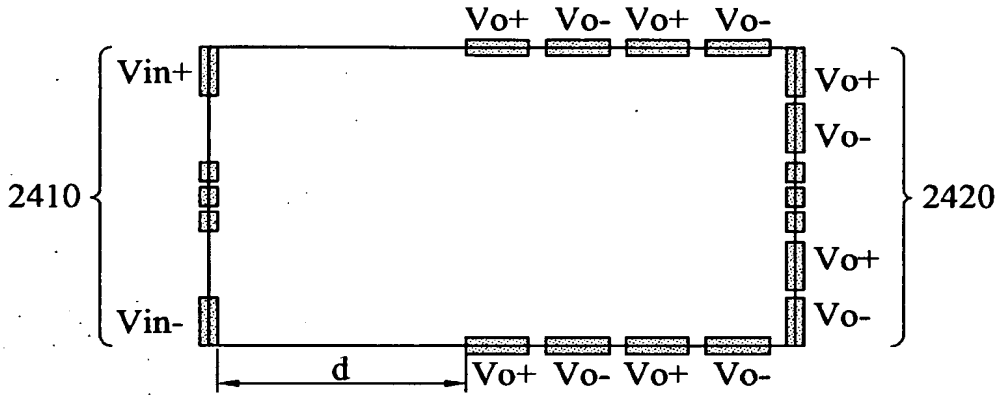

Vo+ Vo- Vo+ Vo-
Vin+
Vo+
Vo-
2410
2420
Vo+
Vo-
Vin-
d
Vo+ Vo- Vo+ Vo-

图 25

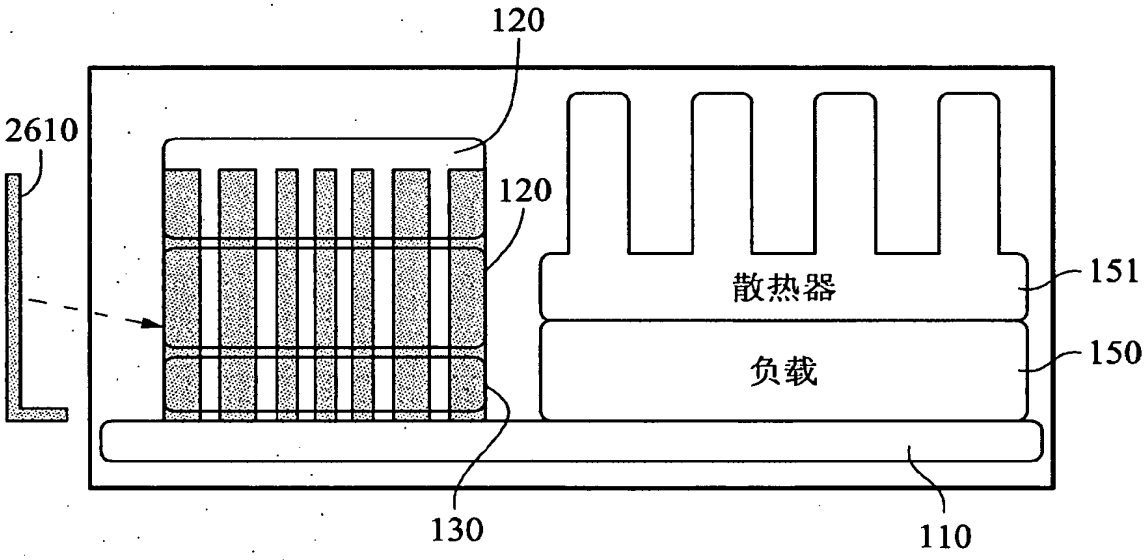

120
2610
120
散热器
151
负载
150
130
110

图 26

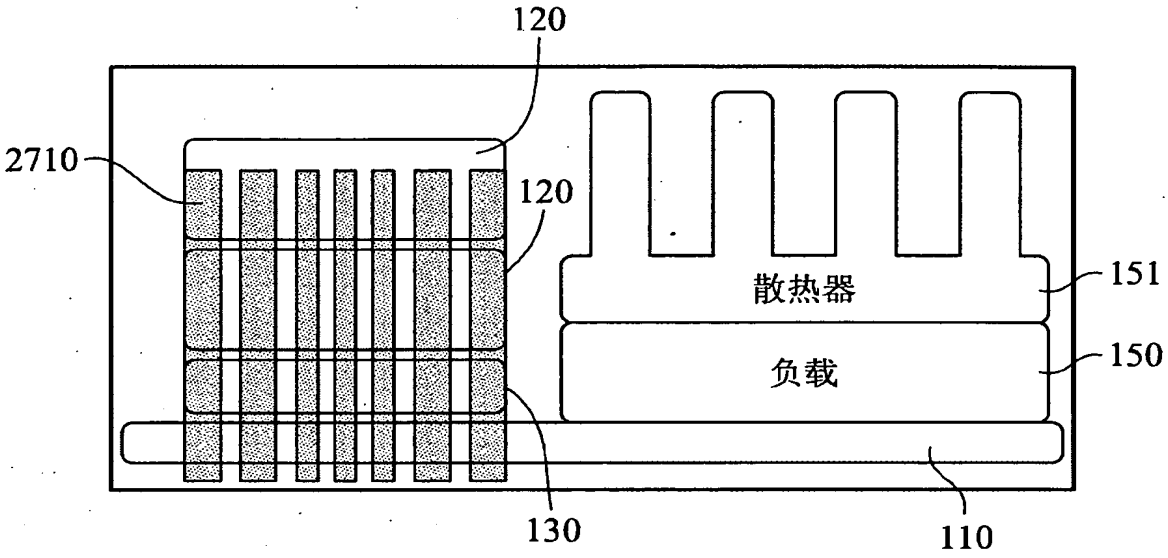

120
2710
120
散热器
151
负载
150
130
110

图 27

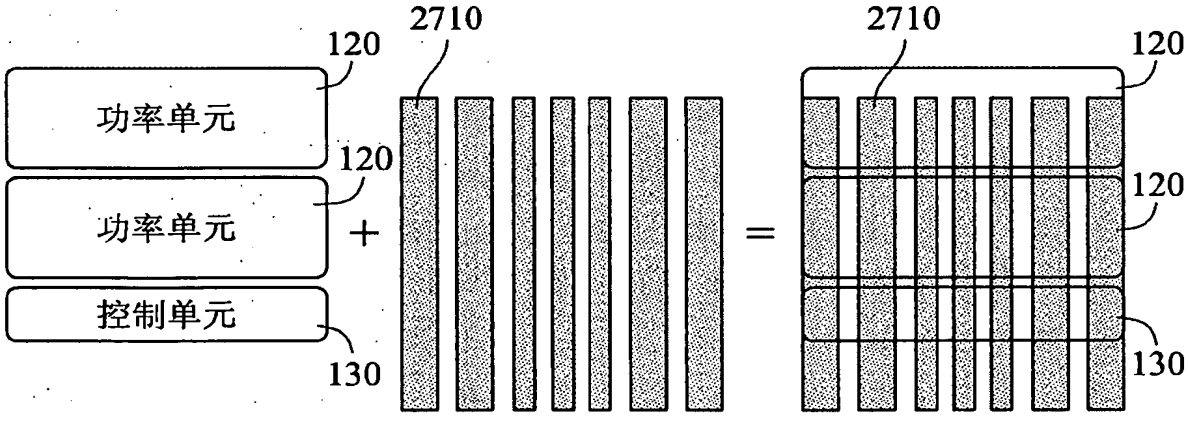

120
2710
功率单元
120
功率单元
+
控制单元
130
=
2710
120
120
130

图 28

2014104429726

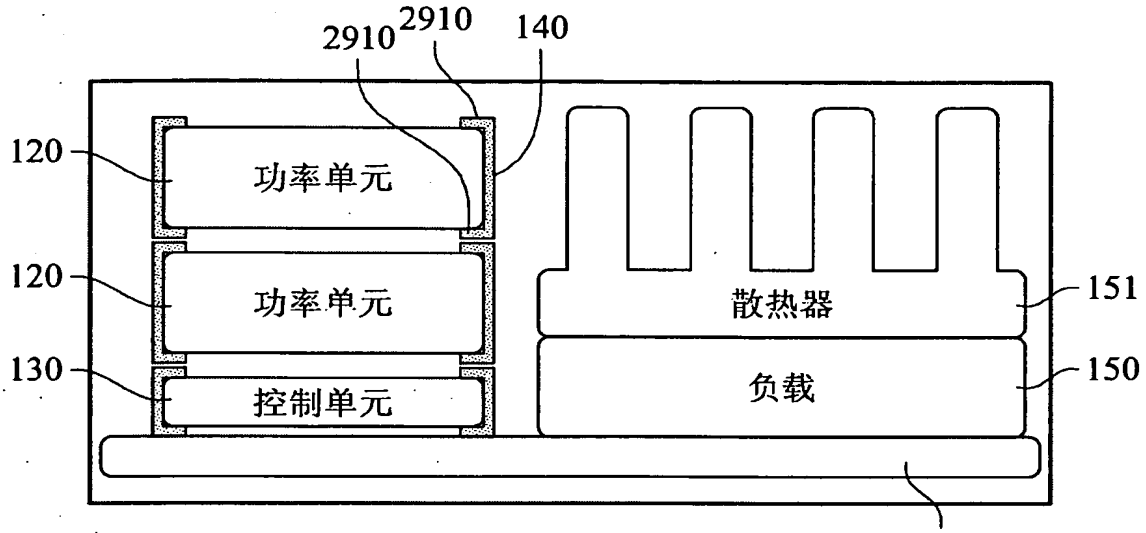


图 29

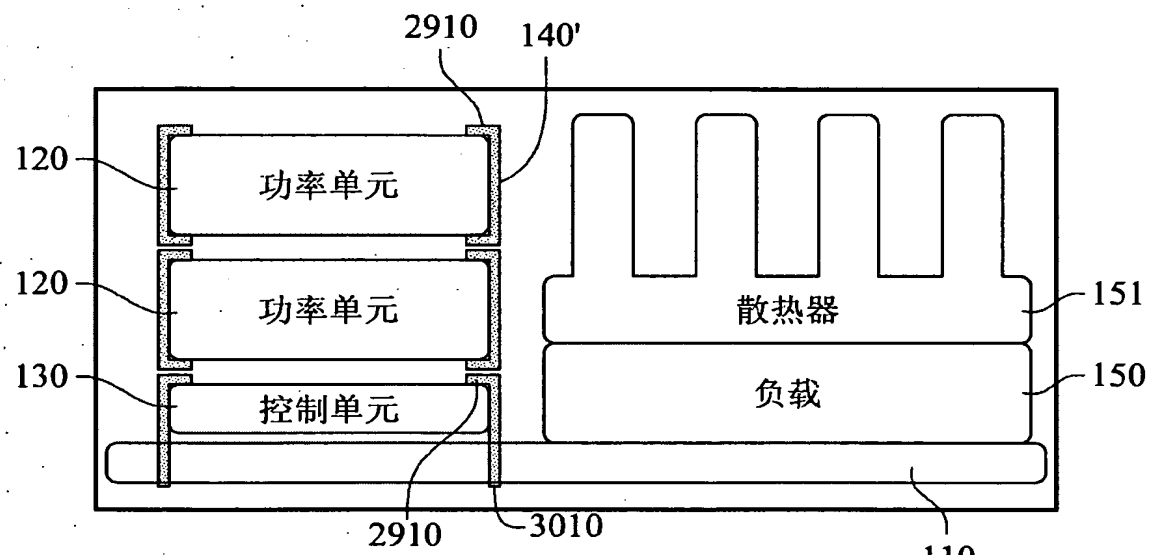


图 30

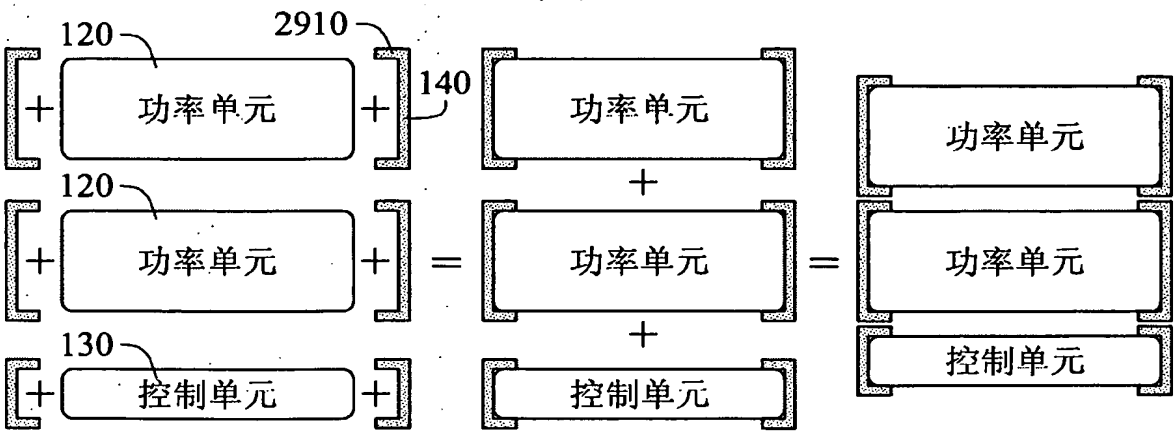


图 31

2014104429726

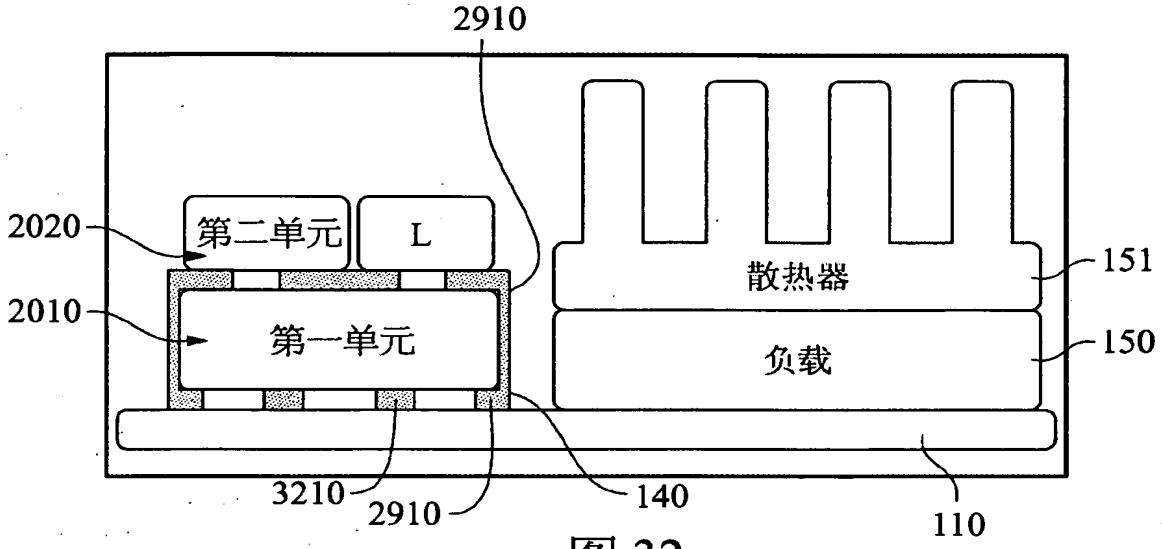


图 32

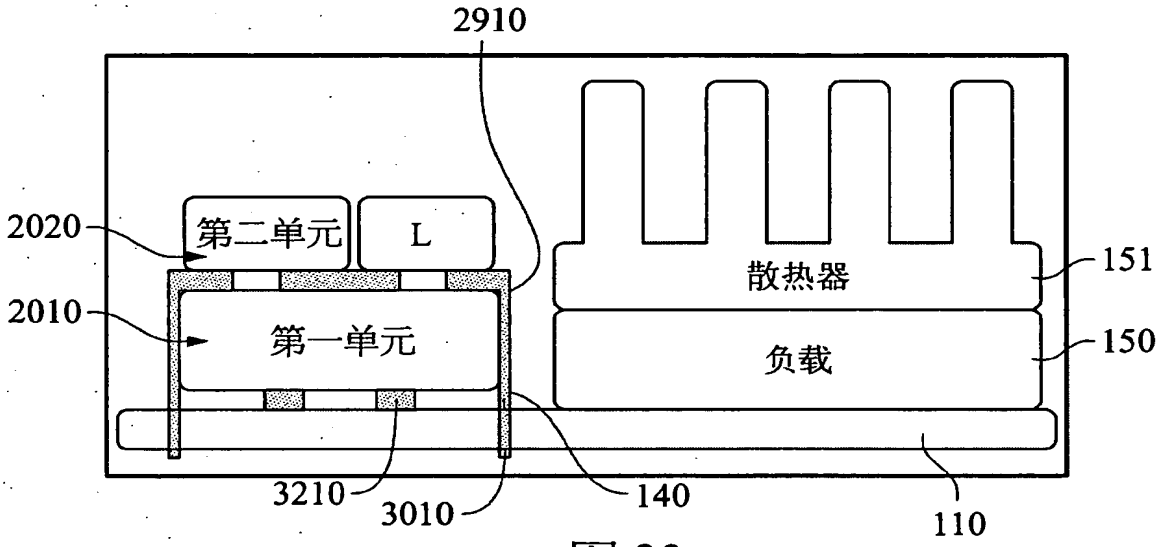


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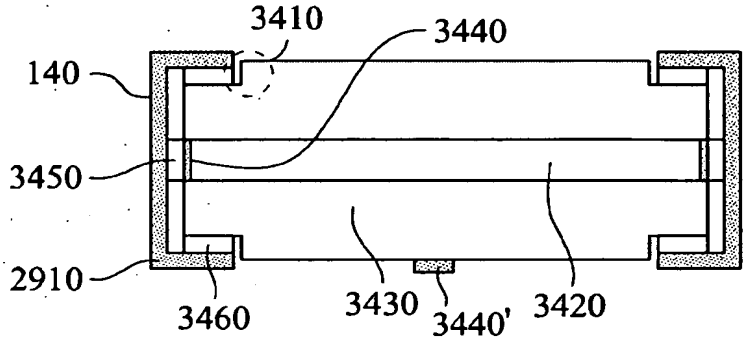


图 34

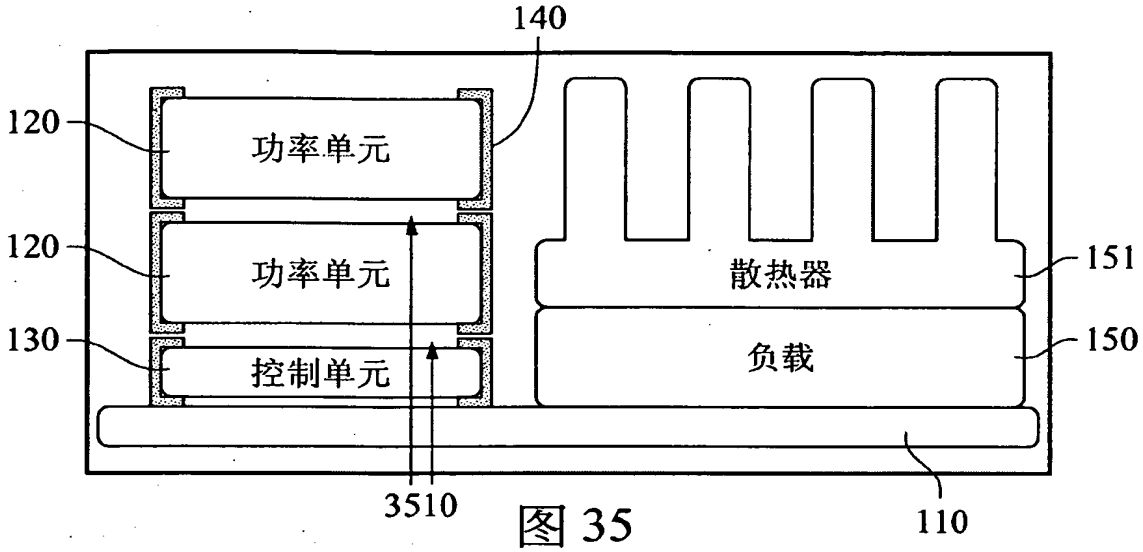

140
120
功率单元
120
功率单元
130
控制单元
散热器
151
负载
150
3510
110

图 35

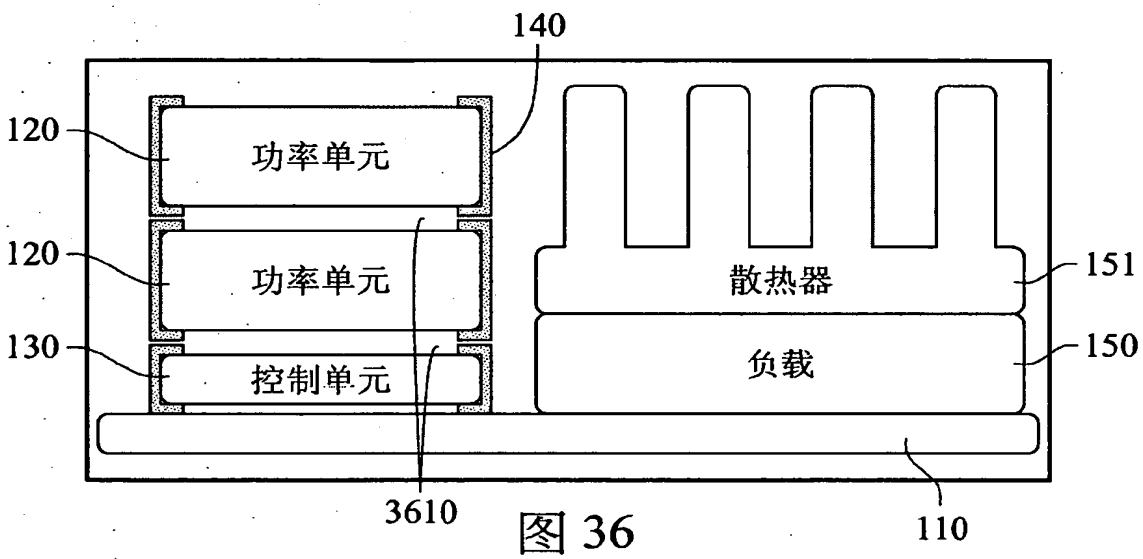

140
120
功率单元
120
功率单元
130
控制单元
散热器
151
负载
150
3610
110

图 36

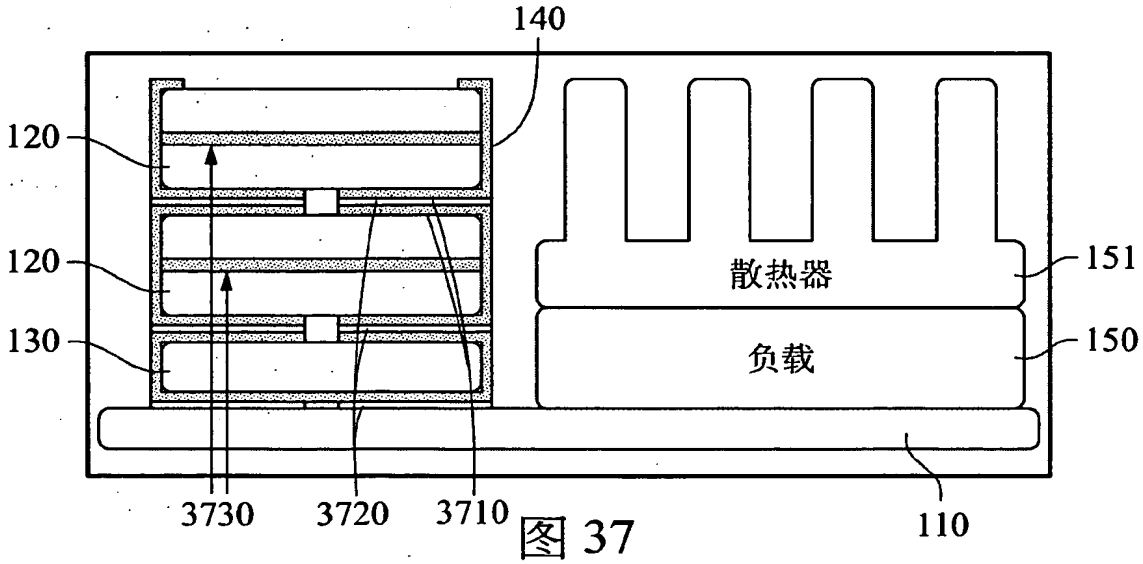

140
120
120
130
散热器
151
负载
150
3730
3720
3710
110

图 37

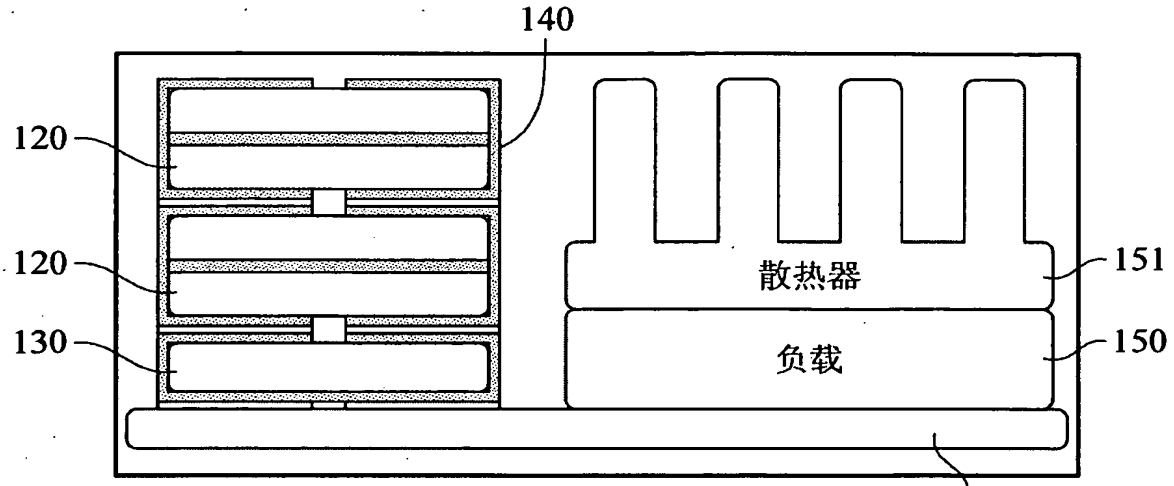

140
120
120
130
散热器
151
负载
150
110

图 38

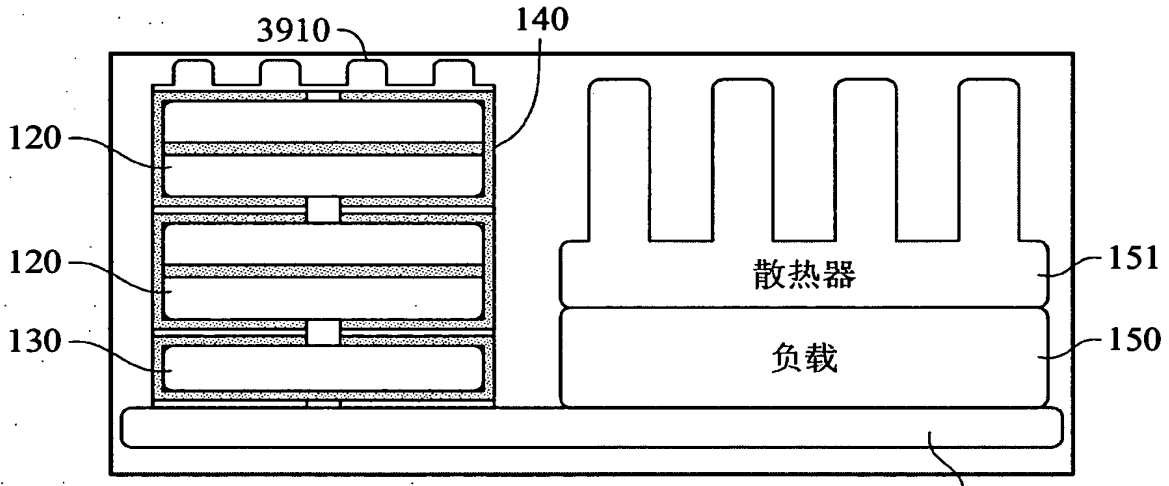

3910
140
120
120
130
散热器
151
负载
150
110

图 39

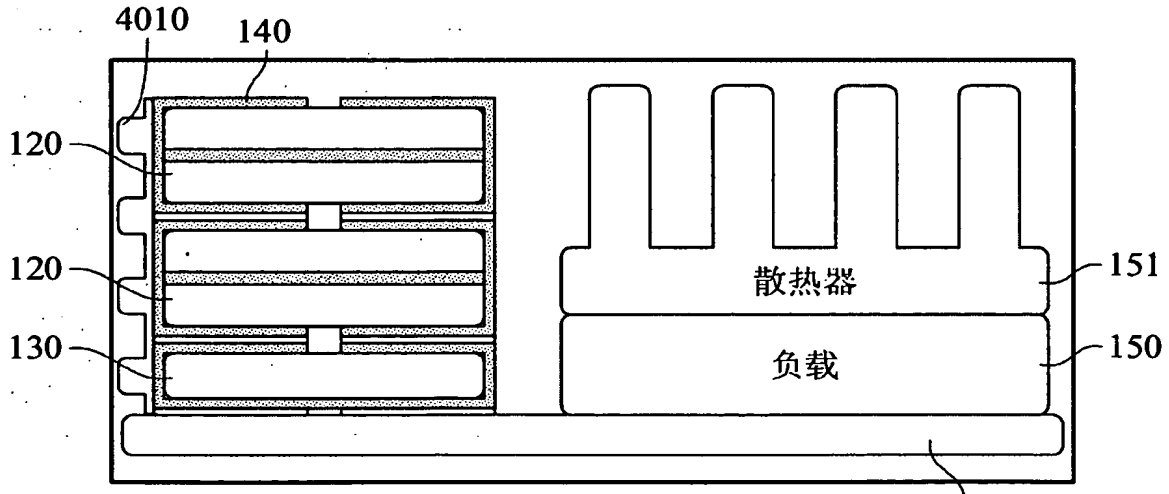

4010
140
120
120
130
散热器
151
负载
150
110

图 40

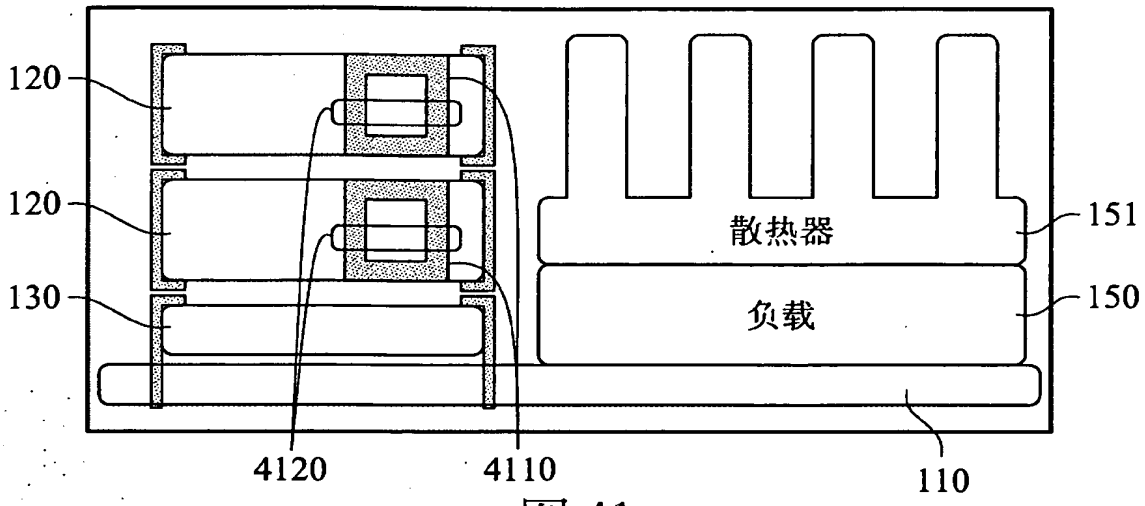

120
120
130
散热器
负载
151
150
4120
4110
110

图 41

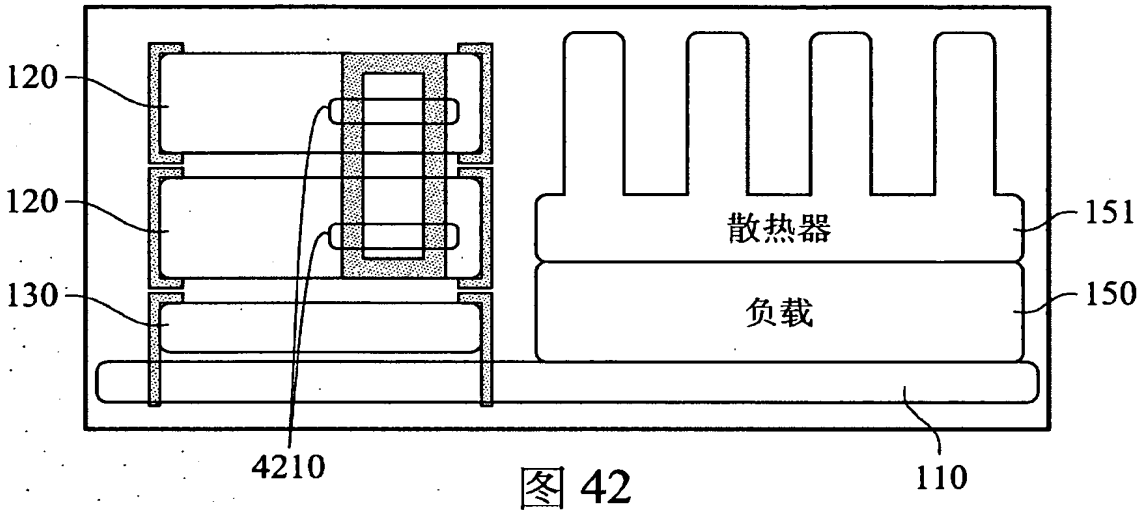

120
120
130
散热器
负载
151
150
4210
110

图 42

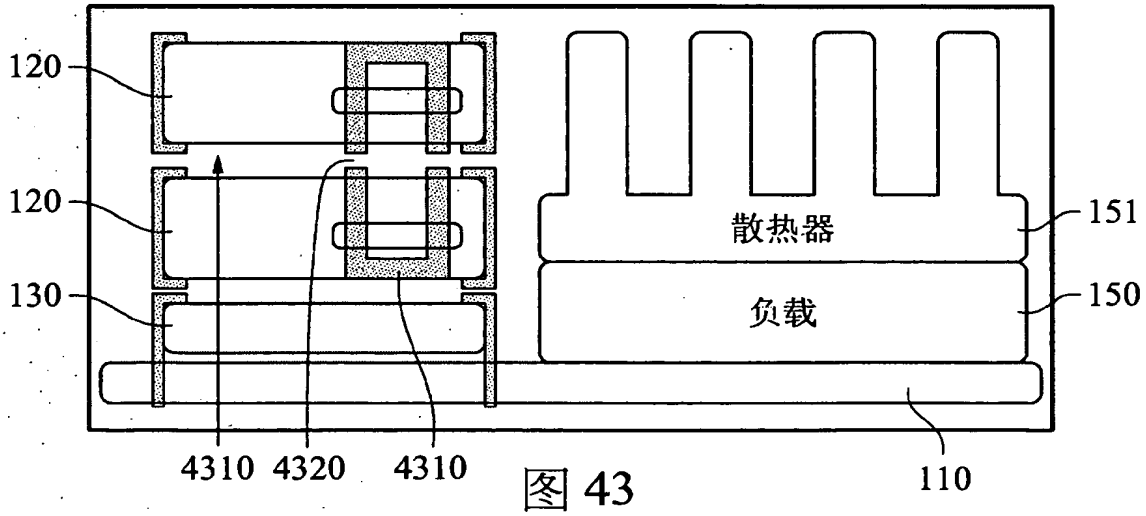

120
120
130
散热器
负载
151
150
4310
4320
4310
110

图 43

Doc Code: TRAN.LET
Document Description: Transmittal Letter

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SEP 28 2015
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(to be used for all correspondence after initial filing)

Application Number	14/840,063
Filing Date	August 31, 2015
First Named Inventor	Jian-Hong ZENG
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	TWT04064/US

Total Number of Pages in This Submission

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  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
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- ☐ Information Disclosure Statement
- ☑ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation
- ☐ Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) (please Identify below):

Remarks

CN 201410442972.6

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	CKC & Partners Co., Ltd.		
Signature	/James Lynn O'Sullivan/		
Printed name	James Lynn O'Sullivan		
Date	2015-08-31	Reg. No.	65618

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IPR2024-00715 EX. 2005

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 14/840,063

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	19 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
14/840,063	08/31/2015	2872	1600	TWT04064/US	19	3

CONFIRMATION NO. 8903

FILING RECEIPT

60589
JAMES O"SULLIVAN
12th Floor, Ruttonjee House
11 Duddell Street
Hong Kong,
HONG KONG

OC000000077421432

Date Mailed: 09/16/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jian-Hong ZENG, Taoyuan City, TAIWAN;
Chao YAN, Taoyuan City, TAIWAN;
Pei-Qing HU, Taoyuan City, TAIWAN;

Applicant(s)

DELTA ELECTRONICS, INC., Taoyuan City, TAIWAN;

Power of Attorney: The patent practitioners associated with Customer Number 60589

Domestic Applications for which benefit is claimed - None.
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
CHINA 201410442972.6 09/02/2014

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 09/14/2015
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/840,063**
Projected Publication Date: 03/03/2016

Non-Publication Request: No

Early Publication Request: No

Title

POWER SUPPLY APPARATUS

Preliminary Class

359

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PTO/AIA/80 (07-12)
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☑ Practitioners associated with Customer Number: 60589

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 60589

OR

☐	Firm or Individual Name		
	Address		
	City		
	Country		
	Telephone		Email

Assignee Name and Address: DELTA ELECTRONICS, INC.
No.252, Shanying Rd., Guishan Dist., Taoyuan City 333, Taiwan, R.O.C.

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record
The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	C. C. Ting	Date	2015/3/12
Name	TING CHAOPING	Telephone	886-2-8797-2088
Title	General Counsel		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IPR2024-00715 EX. 2005

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	POWER SUPPLY APPARATUS

As the below named inventor, I hereby declare that:

This declaration is directed to:

■ The attached application, or

☐ United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Jian-Hong ZENG Date (Optional): 2015/08/26

Signature: Jian-Hong ZENG

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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This declaration is directed to:

- [■] The attached application, or
- [ ] United States application or PCT international application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: Chao YAN Date (Optional): 2018/08/26

Signature: Chao YAN

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Title of Invention	POWER SUPPLY APPARATUS

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ■ The attached application, or
- ☐ United States application or PCT international application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: Pei-Qing HU Date (Optional): 2015/08/26

Signature: Pei Qing Hu

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	TWT04064/US
	Application Number	
Title of Invention	POWER SUPPLY APPARATUS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jian-Hong		ZENG	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Taoyuan City	Country of Residence [i]	TW

Mailing Address of Inventor:

Address 1	No.252, Shanying Rd., Guishan Dist.		
Address 2			
City	Taoyuan City	State/Province	
Postal Code	333	Country [i]	TW

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Chao		YAN	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Taoyuan City	Country of Residence [i]	TW

Mailing Address of Inventor:

Address 1	No.252, Shanying Rd., Guishan Dist.		
Address 2			
City	Taoyuan City	State/Province	
Postal Code	333	Country [i]	TW

Inventor 3 Remove

Legal Name

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	TWT04064/US
	Application Number	
Title of Invention	POWER SUPPLY APPARATUS	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Pei-Qing		HU	

Residence Information (Select One) ◯ US Residency ◉ Non US Residency ◯ Active US Military Service

City	Taoyuan City	Country of Residence [i]	TW

Mailing Address of Inventor:

Address 1	No.252, Shanying Rd., Guishan Dist.		
Address 2			
City	Taoyuan City	**State/Province**	
Postal Code	333	**Country** [i]	TW

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	60589		
Email Address	info@ckc-ip.com	Add Email	Remove Email

Application Information:

Title of the Invention	POWER SUPPLY APPARATUS		
Attorney Docket Number	TWT04064/US	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)		**Suggested Figure for Publication (if any)**	

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For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country [i]

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	TWT04064/US
	Application Number	
Title of Invention	POWER SUPPLY APPARATUS	

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Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201410442972.6	CN	2014-09-02	

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

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POWER SUPPLY APPARATUS

RELATED APPLICATIONS

[0001] This application claims priority to China Application Serial Number 201410442972.6, filed September 2, 2014, which is herein incorporated by reference.

BACKGROUND

Field of Invention

[0002] The present invention relates to a power supply apparatus. More particularly, the present invention relates to the internal structure of a power supply apparatus.

Description of Related Art

[0003] With people's increased demand to the intelligent life, the society's need to data processing is also growing. The global energy consumption spent on data processing averages thousands or even tens of thousands kilowatt-hour (KWH); and a large scale data center may occupy tens of thousands square meters. Therefore, a greater efficiency and higher power density are the key index for the healthy development of this industry.

[0004] The key component of the data center is the server, which has a main board that usually composed of data processing chips such as CPU, chipsets, memory, etc., and the power supply and necessary peripheral components thereof. With the improvement of the processing capability of the server unit

volume, the numbers of these chips and the integration level thereof are also increased, which results in the increase of the space occupied and the power consumption. Therefore, the power supply for supplying these chips (also referred to as the main board power supply because it is disposed on the same main board as the data processing chip is) is expected to exhibit greater efficiency, higher power density and more compact volume, so as to realize the energy-saving of the whole server or event the whole data center and reduction of the floor space.

[0005] In the server, the main board PCB is configured to transmit the energy and signal. On the main board PCB, a data processing chip and a power supply thereof are disposed. The height of the casing of the server is often a standard value, which is defined using the industrial standard "U"; for example, 1U, 1.5U, 2U, etc. (1U = 1.75 inch = 44.45mm). For example, for a server with a height of 1U (about 40 mm; the actual size of the 1U device may vary due to the fit tolerance), the main board is a PCB consisting of 6 to 50 layers, which is very expensive to manufacture. In the case where the height of the server casing is limited, in order to ensure the expected efficiency, by reducing the area that the main board power supply occupies on the main board (that is, the horizontal area of the main board power supply), it is possible to reduce the over volume, increase the power density, and accordingly, lower the manufacturing cost. In the present disclosure, the power of the power supply unit horizontal area is referred to as the "power pressure".

[0006] When using the same technology level in designing a power supply having a power of Po, the greater the volume (V) of the power supply, the

easier to achieve a higher efficiency; that is, the power efficiency is positively proportional to the volume (V). The volume (V) equals to the product of the height (H) and the horizontal area (S). The power pressure (Pp) equals to Po/S. If the efficiency is fixed at a specific level (meaning the efficiency is kept the same), the following relationship between the power pressure (Pp) and the height (H) could be derived: the greater the H, the greater the Pp. In other words, to improve Pp, we should focus on the utilization of the height (H) for a solution. Of course, if the goal is to pursue the efficiency, the height should be properly utilized based on the foregoing rationale. Therefore, how to utilize the height is the key to address both the power pressure (Pp) and the efficiency.

[0007] The thickness or height of the main board power supply can be as thin as 7 mm or even less; hence, when the height of the server is limited to, say 1U, there are more than 20 mm of space height above the power. In this case, the efficiency can be 90% or higher, since the power consumption thereof is only a fraction (such as 10%) of the data processing chip, in fact, it is possible for it to handle the heat dissipation issue without using a heat dissipation unit. In this way, the space above the main board power supply is not adequately utilized.

[0008] Generally, there two ways to manufacture the main board power supply. The first one uses a PCB as the bearer on which individual components are installed. After years of efforts, this type of main board power supply achieves satisfactory efficiency and power density. Yet, since the components are individually installed, there should be necessary space or safety distance between components, thereby limiting the further size reduction of the

horizontal area; also, the uneven height would affect the subsequent handling of the heat.

[0009] The other way to manufacture the main board power supply is to use certain packaging technique to integrate each components of the power supply into a quite regular element. By using such packaging techniques, the power density is significantly increased with satisfactory efficiency; also, such regular shape is advantageous for the subsequent handling of the heat; thereby providing an appropriate solution. However, said packaging technique realize the volume reduction and power density improvement by lowering the height of the main board power supply, and hence, it focuses on decreasing the height based on the original horizontal area. Therefore, this solution is only one of the solution for pursuing a better power density; however, it cannot adequately address the improvement regarding the power pressure of the main board power supply.

SUMMARY

[0010] The following presents a simplified summary of the disclosure in order to provide a basic understanding to the reader. This summary is not an extensive overview of the disclosure and it does not identify key/critical components of the present invention or delineate the scope of the present invention. Its sole purpose is to present some concepts disclosed herein in a simplified form as a prelude to the more detailed description that is presented later.

[0011] The present invention addresses the deficiency of the prior art and provides a novel solution that deals with both the power pressure and the

efficiency; it is suitable for use in application settings requiring a larger horizontal area; such as the demand for power supply in data processing settings like the data center.

[0012] In one embodiment, a power supply apparatus includes a power unit electrically connected with a motherboard, comprising a first base plate, at least a power switch chip allocated at the first base plate and a plurality of pads; a control unit stacked with the power unit, comprising a second base plate and at least a control chip for controlling the power switch chip turn on/ off in the power unit and a plurality of pads; a plurality of pins for electrically connecting the power unit to the control unit and mother board and allocated at periphery of the power unit and control unit, wherein the plurality of pads of the power unit and control unit are allocated on side facet of the first base plate and second base plate respectively, both plurality of pads of the power unit and control unit are electrically connected with the plurality of pins so that the power unit and the control unit could electrically connected with each other, the power supply apparatus provides a power source for a load in the neighborhood thereof on the motherboard.

[0013] In one embodiment, a power supply apparatus includes a first stage power converter received a power source from a mother board and configured with a plurality of pads located on side facet thereof; a second stage power converter configured with a plurality of pads located on side facet thereof and stacked with the first stage power converter to receive an output of the first stage power converter to provide a power to a load in adjacent area thereof on the motherboard; and a plurality of pins connected with the pads of the first

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or/and second stage power converter and the motherboard to realize the electrical connection therebetween.

[0014] In one embodiment, a power supply apparatus includes a first unit electrically connected with a motherboard, comprising a first base plate, at least a power switch chip allocated at the first base plate and a plurality of pads; a second unit stacked with the first unit, having a plurality of connection pads for electrical connection; and a plurality of pins for electrically connecting the first unit to the second unit and mother board and allocated at periphery of the first unit, wherein the plurality of pads of the first unit are allocated on side facet of the first base plate, both plurality of pads of the first unit and plurality of connection pads of the second unit are electrically connected with the plurality of pins so that the first unit and the second unit could electrically connected with each other, the power supply apparatus provides a power source for a load in the neighborhood thereof on the motherboard.

[0015] In view of the foregoing, the technical solutions of the present disclosure result in significant advantageous and beneficial effects, compared with existing techniques. The implementation of the above-mentioned technical solutions achieves substantial technical improvements and provides utility that is widely applicable in the industry. The present disclosure provides a stack structure so that the height of the power supply can be properly utilize; when the volume is fixed, it is possible to achieve a smaller floor space; meanwhile, it retains sufficient volume to ensure a higher efficiency, thereby addressing both the high power pressure and high efficiency. Also, it supports the data processing apparatus with better performances.

[0016] Many of the attendant features will be more readily appreciated, as the same becomes better understood by reference to the following detailed description considered in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The present description will be better understood from the following detailed description read in light of the accompanying drawing, wherein:

[0018] Figure 1 is a lateral view illustrating a power supply apparatus according to one embodiment of the present disclosure;

[0019] Figure 2 to Figure 14 illustrate the infrastructure and distribution of stack component of the power supply according to embodiments of the present disclosure;

[0020] Figure 15 to Figure 16 illustrate the embodiments covered by the control unit and the power unit according to embodiments of the present disclosure;

[0021] Figure 17 to Figure 20 illustrate the stack structure design according to embodiments of the present disclosure;

[0022] Figure 21 to Figure 25 illustrate the pin arrangement according to embodiments of the present disclosure;

[0023] Figure 26 illustrates the infrastructure for heat dissipation according to embodiments of the present disclosure; and

[0024] Figure 27 illustrates the arrangement of the magnetic core according to embodiments of the present disclosure.

DETAILED DESCRIPTION

[0025] In the following detailed description, for purposes of explanation, numerous specific details are set forth in order to attain a thorough understanding of the disclosed embodiments. In accordance with common practice, like reference numerals and designations in the various drawings are used to indicate like elements/parts. Moreover, well-known elements or method steps are schematically shown or omitted in order to simplify the drawing and to avoid unnecessary limitation to the claimed invention.

[0026] In the detailed description and appended claims, the term "coupled with" applies generally to that one component is indirectly connected to another component via other component(s), or one component is directly connected to another component without any other component.

[0027] On technical aspect of the present invention is a power supply apparatus, which can be used in a server or more generally in various technical fields. It should be noted that the power supply apparatus according to this aspect uses the stack structure, and therefore, the height of the power supply can be properly utilized so that a smaller floor space can be realized when the volume is fixed.

[0028] Figure 1 is a lateral view illustrating a power supply apparatus according to one embodiment of the present disclosure. As illustrated in Figure 1, the power supply application device (e.g., a power supply apparatus) comprises a main board 110, a power unit 120, a control unit 130, and a pin 140. The main board 110 further has a load 150 disposed thereon; the power unit 120 is disposed on the main board 110; the control unit 130 and the power unit 120

are stacked on the main board 110 at a position in adjacent to the load 150; the pin 140 is electrically coupled to the main board 110, the control unit 130, and the power unit 120; in the present embodiment, there are multiple pins 140 and these pins are respectfully disposed on a lateral side of each of the power unit 120 and the control unit 130; the two power units 120 and the control unit 130 are stacked with one another on the main board 110. The control unit 130 is configured to control the power unit 120; specifically, the control unit controls the two power units 120 via the pins 140, so that the power unit 120 supply the electricity to the adjacent load 150. The load 150 is a digital processing IC, such as a central processing unit (CPU), and the CPU has a heat dissipation unit/heat dissipation device such as a heat dissipator 151 disposed thereon. The power unit 120 comprises at least one power semiconductor device (such as, switch tubes S21, S22, S23, S24 in Figure 3, switch tubes S21, S22, S23, S24, S31, S32, S33 in Figure 11); the control unit 130 comprises at least one chip having the control or driving ability (such as, the control circuit 310 in Figure 3, the control circuit 1100 in Figure 11, DSP).

[0029] In one embodiment, the power supply apparatus is disposed on the main board 110; the main board 110 further has a load 150 of a data processing chip (such as, CPU) disposed thereon; the power supply apparatus comprises: the power unit 120, the control unit 130 and pins 140. The control unit 130 and the power unit 120 are stacked on the main board at a position in adjacent to the load 150; the pins are electrically coupled to the main board 110, the control unit 130 and the power unit 120; the control unit 130 is configured to control the power unit 120, so that the power unit 120 supplies the electricity to the adjacent load 150.

[0030] In sum, the DC /DC power supply comprises at least two units (i.e., modules): the control unit 130 and the power unit 120. Said two modules are vertically stacked, and the electric connection therebetween is realized via the conductors (i.e., pins 140) so as to transmit the electric signal. The power unit 120 comprises at least one active switching element; the power unit 120 receives the input power and generates a corresponding output power by the conduction and turning-off of the active switching element and then supplies the output power to the load 150, such as the data processing chip. The control unit module 130 comprises at least one control chip for sending a control signal to the active switching element of the power unit 120 so as to control the conduction and turning-off of said element. The unit disposed at the upper position and a portion of the pins are fixed by the unit disposed at the lower position, and then transmits the electric signal to the above-mentioned main board 110 (such as, the PCB).

[0031] In this way, due to the stack structure adopted herein, the height of the power supply can be more properly utilized so as to realize a smaller floor space at a given volume; while retaining sufficient volume to ensure a higher efficiency; accordingly, it accomplishes both the high power pressure and high efficiency. Also, it supports the data processing apparatus with better performances.

[0032] Infrastructure and distribution of stack component of the power supply

[0033] Figure 2 is a schematic diagram illustrating various types of power supply converter (i.e., the main board power supply 200) that may involve in a server

main board. The input of the power supply converter is often a direct current with a wide range of voltage, including high voltage of 200 to 500 V (for example, 400 V), middle voltage of 18 to 72 V (for example, 48 V) and low voltage of 5 to 15 V(for example, 12 V). No matter what kind of voltage is being inputted, a corresponding DC/DC converter is required to convert the input into a desired output to be supplied to the load 150, such as the data processing chip, like a central processing unit (CPU) and memory. The variation range of the output is also wide so as to adapt to the demands of various loads; for example, the output can be as low as 0.8 V or even lower, or as high as 12 V or even higher. When the load 150 is a CPU and memory, the output voltage is often in the range of 0.8 to 2 V. Therefore, the power supply specification involved includes, mainly:

[0034] (1) Converter 210 converts 400 V to 48 V: the input voltage is in a range of 200 to 500 V (for example, 400 V) which is outputted as a stable output voltage or at a fixed ratio to the input voltage; for example, the output voltage can be around 48 V or a voltage un the range of 18 V to 72 V. Since the output voltage is higher, it will not be directly connected to the data processing chip load; instead, another specification converter should be cascaded thereafter to adjust the voltage to a level that can be used by the load.

[0035] (2) Another a converter (not shown in the drawing) coverts 400 V to 12 V: the input voltage is in a range of 200 to 500 V (for example, 400 V) which is outputted as a stable output voltage or at a fixed ratio to the input voltage; for example, the output voltage can be around 12 V. Since the output voltage is lower, it can be connected to some data processing loads, such as a hard drive.

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However, when the load voltage is even lower; for example, 0.5 to 5 V, another specification DC/DC converter should be cascaded thereafter to adjust the voltage to a level that can be used by the load.

[0036] (3) Yet another converter (not shown in the drawing) converts 400 V to 0.5 to 5 V: the input voltage is in a range of 200 to 500 V (for example, 400 V) which is outputted as a stable output voltage depending on the actual need; for example, the output voltage is in the range of 0.5 to 5 V. The output voltage can be directly connected to the data processing chip, such as the CPU, memory, etc.

[0037] The converts according to the above-mentioned specification (1) to (3) use a high-voltage input, and hence, they should meet the requirements for high voltage safety insulation, and the insulation voltage should be around a DC voltage of 2000 V, or even higher.

[0038] (4) Converter 220 converts 48 V to 12 V: the input voltage is in a range of 18 to 72 V (for example, 48 V), which is outputted as a stable output voltage or at a fixed ratio to the input voltage; for example, the output voltage can be around 12 V, or in the range of 3 to 15 V. The converter of this specification can be directly connected to some data processing loads, such as a hard drive.

[0039] (5) Converter 230 converts 48 V to 0.5 to 5 V: the input voltage is in a range of 18 to 72 V (for example, 48 V) which is outputted as a stable output voltage depending on the actual need; for example, the output voltage is in the range of 0.5 to 5 V. The output voltage can be directly connected to the data processing chip, such as the CPU, memory, etc.

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[0040] (6) Converter 240 converts 12 V to 0.5 to 5 V: the input voltage is in a range of 3 V to 15 V (for example, 12 V) which is outputted as a stable output voltage depending on the actual need; for example, the output voltage is in the range of 0.5 to 5 V. The output voltage can be directly connected to the data processing chip, such as the CPU, memory, etc. Since this converter uses the low-voltage input, there is no need for insulation, and the output can be directly connected to the data processing chip, such as the CPU, memory, etc.

[0041] The converts according to the above-mentioned specification (4) to (6) use a low-voltage input, and hence, the voltage-bearing demand of the converters is lower, which is generally less than a DC voltage of 2000 V.

[0042] When the output of the converter is 0.5 to 5 V, since the output can be directly connected to the load 150, such as the data processing chip, the power supply converter is required to output a low-voltage high current, and a high dynamic responsive ability is required, for example, when the load 150 is a CPU, a responsive ability of 1000 A/ns is required; and in this case, the power supply converter should be disposed in adjacent to the load. Therefore, such power supplies are referred to as the "point of the load". Among them, the power supply for supplying the CPU (also known as the voltage regulated module (VRM)) is required to supply the electricity from an adjacent position.

[0043] The power supply converters having the above-mentioned input/output specifications are all disposed on the main board; hence, they can be stacked to achieve the goals of high power pressure and high efficiency. Of course, the combination of various converters is also appropriate for the stack arrangement.

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[0044] As described above, the power supply having an input of 400 V or 48V often requires an input/output safety pressure tolerance due to the greater pressure difference between the input and output, and it often uses a transformer to isolate and transmit the energy. Of course, if necessary, for example, to realize a wider input or output range, a low-voltage input power supply (such as a power supply having an input of 12 V) can also use a transformer to transmit the energy.

[0045] The converters according to the above-mentioned specifications can employ various type of topology to achieve the conversion of the electric energy, for example, the pulse-width modulation (PWM)-based forward circuit, full-bridge circuit, phase-shift full-bridge circuit, half-bridge circuit, fly-back circuit, etc. To realize a higher power density, a higher operation frequency is often required, for example, 500 kHZ, 1 MHZ, or even more than 2 MHZ. To achieve a high efficiency under such high frequency, a resonant circuit (that is, a pulse-frequency modulation (PFM)-type LLC series resonant converter (LLC-SRC), parallel resonant converter (PRC), etc.) is often selected.

[0046] Figure 3 illustrates a half-bridge LLC circuit. As illustrated in Figure 3, the circuit comprises a main circuit and a control circuit 310. The main circuit comprises: an input capacitor C1, a resonant capacitor C2, a resonant inductor L1, a transformer T1, primary side switch tubes S11, S12 and secondary side switch tubes S21, S22, S23, S24, wherein the input capacitor C1 is connected with the primary side switch tubes S11, S12; the primary side switch tubes S11, S12 is connected with a series circuit composed of the resonant capacitor C2, the resonant inductor L1, the primary winding of the transformer T1; the

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secondary winding of the transformer T1 is connected with the secondary side switch tubes S21, S22, S23, S24; the output capacitor C3 is connected with the secondary side switch tubes S21, S22, S23, S24. The primary side switch tubes S11, S12 receive the input power and convert the DC input signal into a AC signal; the AC signal is transmitted to the secondary side via the resonant inductor L1, the resonant capacitor C2 and the transformer T1, and then passed through the secondary side synchronous rectifying circuit (such as, the secondary side switch tubes S21, S22, S23, S24), and generates an output voltage on the output capacitor C3 and supplies the output power to the load. It should be noted that since the output is a low-voltage high current, to reduce the loss, the elements with low-voltage high current (such as the T1 secondary winding, the secondary rectifier, the output capacitor) are often in parallel connection to obtain a low resistance. For example, "an assembly of a rectifying assembly S21, S22 and a secondary winding" and "an assembly of another rectifying assembly S23, S24 and another secondary winding" are in parallel connection. Since the output voltage may vary, the structure of the transformer secondary winding is not limited to the central tap rectifying structure illustrated in Figure 3; rather, it could be any other structure such as the full-bridge rectifying structure.

[0047] The control circuit 310 generates a control signal that is supplied to the driver 320 for driving the primary side switch tubes S11, S12, and the driver 330 for driving the secondary side switch tubes S21 to S24, so as to control the conduction or turning-off of each switch element (e.g., switch tubes S11, S12, S21 to S24) in the main circuit. Of course, the control circuit 310 may further

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comprise other elements necessary for sampling, protection and communication; these elements or not illustrated in the drawing, and hence will not be discussed in detail herein.

[0048] Since the power unit 120 is under the high-frequency operating status, and the output of the converter is a low-voltage high current, generally, the circuit composed of the secondary side of the transformer, the output synchronous rectifying circuit and the output capacitor should be as small as possible so as to adapt for the need of the high frequency. Therefore, the transformer T1, the synchronous rectifying circuit (i.e., secondary side switch tubes S21, S22 等), the output capacitor C3 have to be disposed in a single unit circuit (i.e., the power unit 120).

[0049] In one embodiment, the maximum operating voltage of the power supply input is greater than 20 V, the power unit 120 comprises: at least one transformer T1, in which the transformer T1 comprises at least one primary side and at least one secondary side; at least one synchronous rectifying assembly (such as, the secondary side switch tubes S21, S22) and an output capacitor assembly (such as, the output capacitor C3). The high frequency energy id delivered from the primary side to the secondary side, and rectified by the synchronous rectifying assembly into a direct current, which is then transmitted to the output capacitor for integration.

[0050] On the other hand, the peripheral of the control circuit 310 often comprises many peripheral circuits, and the signal required to be processed is low, and hence, they should be placed in proximity to increase the anti-interference ability. Therefore, the control circuit 310 and the peripheral

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circuits thereof should be placed in a single unit circuit (i.e., the control unit 130). In one embodiment, the control unit 130 is implemented by an embedding technique and the thickness thereof is less than 2 mm. The power unit (e.g., power supply converting circuit) is a resonant circuit with an operating frequency greater than 1MHZ. The control unit (e.g., control power supply) has an input filter stacked thereabove.

[0051] Regarding the driver 320, 330, the primary side switch tubes S11 to S12, the resonant capacitor C2, and the resonant inductor L1 can be disposed in the power unit 120 or the control unit 130 depending on the actual needs. The input capacitor C1 can inhibit the voltage peak of the primary side switch tubes S11 to S12, and accordingly, it should be preferably disposed with the primary side switch tubes S11, S12 in a single unit. The L1/C2 can be obtained by integrating with other elements such as the T1. Moreover, the T1 exciter inductor can be an individual inductor that in parallel connection with the transformer primary, so as to facilitate the optimization of the performance of the T1.

[0052] As illustrated in Figure 1, the overall power circuit is formed by stacking the control unit 130 and the power unit 120, which will effectively reduce the horizontal area of the power circuit 120; and hence, when the power circuit is placed on the main board 110, the space that it occupies on the main board 110 is reduced. In Figure 1, the control unit 130 or the power unit 120 can be manufactured by a packaging technique, e.g., using a plastic material in a molding process, so as to form a module. Alternatively, the two units can be manufactured as individual elements. Either way, each unit may comprise a

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bearing plate, such as, the printed circuit board (PCB) or the direct bonding circuit (DBC), etc., for bearing the components of the unit; alternatively, the components can be directly stacked within the unit, for example, the switch element and elements such as the inductor and the capacitor can be directly stacked with one another. When the primary side switch tubes S11 to S12, the resonant capacitor C2, the resonant inductor L1 are integrated in the power unit, the circuit in the control unit mainly handles the control signal, and hence, the height of the control unit can be very small, such as less than 5 mm, 3 mm, or even 1 mm.

[0053] In the case where the size of the power is bigger, it is possible to connect several main circuits illustrated in Figure 3 using the parallel connection of the input/output. In this way, the overall structure of the power supply apparatus can use one main circuit as a power unit, and stacks several identical power units and a control unit, as illustrated in Figure 1. The control unit 130 can be disposed at the lower position with two power units 120 stacking thereon, or the control unit can be sandwiched between two power units, or the control unit can be placed above the two power units. Either way, the structure takes full advantage of the height so as to achieve the goal of increasing the power without changing the floor space. In this embodiment, the number of the control unit 130 can be one, and it is configured to control the conduction and turning-off of the switch elements of the two power units 120; or there can be multiple control units, for example, two, for respectively controlling the conduction and turning-off of the switch elements of the two power units. Of course, it is possible to integrate the control unit and one of the power units, so that at least one power unit 120 and one control unit 130 are stacked together,

in which the control unit is integrated from at least one main circuit. As illustrated in Figure 4. The power supply module comprises the power unit 120 and the control unit 130 that are stacked together and are electrically connected via the pins 140. In this embodiment, the power unit 120 is integrated from an DC/DC converter, and the control unit 130 is integrated from another DC/DC converter and a control circuit, in which the control circuit controls said two DC/DC converter.

[0054] As discussed above, the power supply apparatus receives an input, generates an output and provides the energy to the load. The power supply apparatus may use the single-stage converter, such as the circuit illustrated in Figure 3, to achieve the requirement for voltage conversion, or even isolation. Of course, multiple-stage converter can be used. Due to the limitation of the characteristics of the component, usually, the single-stage circuit is not suitable for wide-range input/output; hence, for a load with a wide voltage range, such as the CPU, memory and other loads applied in the server power supply, it is more appropriate to use a two-stage power supply; in this case, one of the which is responsible for isolation, while another one is responsible for voltage adjustment; each responsible for its own function so as to achieve the optimal performance. For example, structure like this is illustrated in Figure 5 or Figure 6.

[0055] As illustrated in Figure 5, the input voltage Vin is a wide voltage range, such as 38 to 60 V, the input voltage uses a front-stage circuit (such as an isolated non-regulated DC/DC converter; i.e., an isolated transforming module DCX; as used herein, the term "non-regulated" means that the input/output of a

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circuit in the operating range is fixed at a constant ratio; that is, the output varies in proportion to the input, such as Vin/Vo=n; for example, in Figure 5, Vin/Vo = 4) to achieve high-voltage isolation; and then uses a post-stage circuit (such as a non-isolated regulated DC/DC converter) to provide the output to the load. For example, the post-stage circuit could be a point-of-load (POL) converting unit that could be used to fulfill the needs for outputting stabilized voltage and dynamic response. Since the post-stage circuit has the adjusting capability, and therefore, the front-stage circuit doesn't need to have the adjusting capability. However, if needed the front-stage circuit may have the full or partial adjusting capability; for example, the front-stage circuit can be an isolated DC/DC converter.

[0056] Referring to both Figure 1 and Figure 5, the two power units 120 can respectively be a power unit of the primary DC/DC converter and the power unit of the secondary DC/DC converter; the control unit 130 comprises the control unit of the primary DC/DC converter and the control unit of the secondary DC/DC converter. Specifically, the primary DC/DC converter is an isolated DC/DC converter; secondary DC/DC converter is a non-isolated regulated DC/DC converter (such as the one illustrated in Figure 5), the non-isolated regulated DC/DC converter is closer to the main board 110 than the isolated DC/DC converter is. Alternatively, the primary DC/DC converter is a non-isolated regulated DC/DC converter; the secondary DC/DC converter is an isolated non-regulated DC/DC converter. For example, the primary DC/DC converter is a buck-boost circuit.

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[0057] In one embodiment, the power unit 120 is a primary DC/DC converter; the control unit 130 is a power unit of a secondary DC/DC converter. For example, the primary DC/DC converter is a non-isolated regulated converter; the secondary DC/DC converter is a non-regulated isolated converter; or, the primary DC/DC converter is an isolated converter; the secondary DC/DC converter is a non-isolated regulated converter.

[0058] Since the front-stage circuit is a non-regulated isolated transforming module DCX, it is possible to design it so that the circuit operates at the optimal operating point, thereby making the circuit relatively simple with a high efficiency. When the isolated transforming module DCX is a resonant circuit, the isolated transforming module DCX may operate around the resonant frequency; and when the DC transformer DCX is a PWM circuit, such as a full-bridge circuit, it can operate under the condition with the greatest mark-space ratio. The post-stage circuit is a regulated circuit, such as a point-of-load (POL) DC converter which is usually implemented by a buck circuit (such as, POL buck DC converter), so that the characteristics of the output fulfills the requirement of the load; in this case, the circuit is simple, and the output voltage range is quite wide. Combining the two, it will be easy to achieve the requirements of wide input/output voltage range, high output voltage accuracy, and dynamic response property. When the isolated transforming module DCX uses the resonant circuit, such as the LLC-SRC circuit, it is easier to achieve a power supply with high efficiency and high power density under high frequency. Of course, since the post-stage circuit has the regulation capability, if the DCX reduces the voltage-withstand value of the intermediate BUS capacitor and associated power component, due to certain

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reason, such as the reduction of the intermediate BUS voltage range, so that the DCX has certain level of output voltage regulation capability, it will not affect the implementation and function of the present invention.

[0059] As illustrated in Figure 6, the input voltage Vin is a wide voltage range, such as 38 to 60 V. The input voltage Vin uses a front-stage circuit (such as a non-isolated regulated DC converter; i.e., a front regulate module (FRM)) to convert the input voltage into a desired value, such as a constant voltage of 48V, and to respond to the dynamic change of the load; and an isolated non-regulated DC converter (i.e., an isolated transforming module DCX) is connected thereafter in parallel connection to achieve the voltage isolation, and the requirement for bucking. Under this structure, the stabilized voltage and dynamic response of the final output (i.e., the output of the post-stage circuit) are implemented by the front-stage circuit. Since the front regulate module (FRM) does not require isolation, it could be implemented with various topologies, such as, buck, boost or buck-boost circuit; for high frequency ap0plicaiton, it is possible to implement the soft switching technique. Therefore, the front regulate module (FRM) may have a very high power density, and so does the isolated transforming module DCX.

[0060] Referring to both Figure 1 and Figure 6, one power unit 120of the two power units 120 comprises the power unit of the primary DC/DC converter and the power unit of the secondary DC/DC converter; the primary DC/DC converter is an isolated non-regulated DC/DC converter, while the secondary DC/DC converter is a non-isolated regulated DC converter (as illustrated in Figure 6).

[0061] Using the above-discussed two power supply structures, take main board power supply with the output power of 200 W as an example, it is possible to implement the isolated transforming module DCX and point-of-load (POL) DC converter (the structure of Figure 5) or the front regulate module (FRM) and isolated transforming module DCX (the structure of Figure 6) within a floor space of 1/16 brick (1.3 in * 0.9 in, or 33 mm * 22.9 mm); therefore, the power pressure is 85.5W/inch^2 (in fact, due to the installation space required between two units, the power pressure is even lower). Since the height of the two units is less than 10 mm or even 7 mm, if the two units are stacked according to the method provided by the present disclosure (as illustrated in Figure 7), the control unit and the power unit are integrated as an isolated transforming module DCX which is stacked with the point-of-load (POL) DC converter on the main board 110; or, as illustrated in Figure 8, the control unit and the power unit are integrated as a front regulate module (FRM) which is stacked with an isolated transforming module DCX on the main board 110. In this way, the power pressure can be immediately doubled to 171 W/inch^2, thereby greatly reducing the required space on the main board. Even though the stacking may require some additional height for reasons such as heat dissipation, the overall height thereof can be less than 25 mm, which fully complies with the requirement for the height of the server (which could be as high as 30 mm).

[0062] To reduce the volume occupied by the pins for interconnection, the power stages of the above-mentioned isolated transforming module DCX and point-of-load (POL) DC converter can be manufactured in a single power unit 120, and the control circuits of two stages are manufactured in a single control unit 130. In this way, the handle of the power parts can be centralized, so as

to achieve a better efficiency and smaller floor space. Depending on actual needs, said power unit part, can be one parts or multiple parts in parallel connection, as illustrated in Figure 9; multiple power units 120 are in parallel connection and each comprises the power stages of an isolated transforming module DCX and point-of-load (POL) DC converter, the control unit 130 comprises the control circuits of the isolated transforming module DCX and point-of-load (POL) DC converter.

[0063] Figure 11 illustrates the principle of the circuit structure of Figure 5. Figure 11 differs from Figure 3 in that it has an additional post-stage circuit – the circuit of the circuit point-of-load (POL) DC converter, such as the buck circuit illustrated in Figure 11, in addition to the parts illustrated Figure 3. Since the output is a low-voltage high current, the POL is usually implemented using several buck circuits in parallel connection. The specific number of the circuits in parallel connection depends on the actual condition. For example, in Figure 11, there buck circuits are in parallel connection. The isolated non-regulated DC/DC converter comprises: an isolated transformer T1, a plurality of primary switch tube S11, S12 and a plurality of secondary switch tubes S21, S22; the non-isolated regulated DC converter is a point-of-load (POL) DC converter. The circuit of each point-of-load (POL) DC converter respectively comprises the switch tubes S31, S32 and S33 and filtering inductors L21, L22 and L23and connected with the switch circuits, which form the corresponding buck circuit. The output of the circuit in each point-of-load (POL) DC converter is in parallel connection with the two terminals of the capacitor C4, so as to generate the output power and provided the same to the load. The control chip 1100 is configured to generate the control signal for controlling the conduction and

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turning-off of the switch elements in the point-of-load (POL) DC converter. To achieve a high efficiency, the power unit 120 comprises the isolated transformer T1, the synchronous rectifying switch tubes S21 to S24, and the output capacitor C3 of the isolated transforming module DCX, and the switch tubes S31 to S33 of the point-of-load (POL) DC converter. In other words, the isolated transformer T1, the secondary switch tubes S21, S22, S23, S24, the output capacitor C3 for isolating the DC/DC converter, and the point-of-load (POL) DC converter are disposed within a single power unit 120. Of course, the structure in Figure 11 further comprises the filtering inductors L21 to L23 and the output capacitor C4. The control unit 130 comprises a control chip 1100 and the peripheral circuit thereof, such as the signal processor DSP illustrated in Figure 11 and the peripheral circuit of the controller (not shown). The primary switch tubes S11, S12 are disposed in the control unit 130, and the control unit 130 further comprises the primary switch tube driving circuit, the control driving circuit of the POL DC converter, and the control chip 1100.

[0064] The structure for the front regulate module (FRM) and isolated transforming module DCX can also be implemented in this way, so as to achieve both the higher efficiency and higher power pressure; as illustrated in Figure 10, multiple power units 120 are in parallel connection, and each of which comprises the power stages of the front regulate module (FRM) and the isolated transforming module DCX; the control unit 130 comprises the control circuits of the front regulate module (FRM) and the isolated transforming module DCX.

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[0065] Of course, the above-mentioned isolated transforming module DCX can also be a regulated converter or semi-regulated converter. The variation in function will not affect its contribution to the improvement of the efficiency and the power pressure.

[0066] In the above embodiments, all of the power supplies use the DC to DC (DC/DC) converter. These embodiments can be applied in structures such as where the DC power supply directly inputs to the server main board. Of course, with the advancement of the technology, there might be the case where the AC power supply AC directly inputs to the server main board 1200. As illustrated in Figure 12, the AC power supply AC (such as 220 Vin) directly connects to the server main board 1200, and provides the input power to the corresponding load through the main board power supply 1210 composed of cascaded or parallel-connected power supply modules 1201 to 1205. In comparison to the above-mentioned main board power supply of the DC input, this structure further comprises front-stage cascaded electromagnetic interference (EMI) filter 1221, the power factor correction (PFC) circuit 1222 and the auxiliary power module 1223, etc. In this structure, the above-mentioned stacking techniques can also be used.

[0067] Figure 13 is a schematic diagram illustrating a EMI filter 1310 cascaded with a post-stage PFC circuit 1320. As illustrated in Figure 13, after the EMI filter 1310 receives the AC input, e.g., V_{AC} = 220 V, it provides an output signal to the post-stage cascaded PFC circuit for power factor correction. In practice, the PFC circuit 1320 can be implemented in various topologies, such as the boost, buck, dual-boost and the totem pole structure illustrated in Figure 13.

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Take the totem pole PFC circuit illustrated in Figure 13 as an example, the main circuit in the PFC circuit 1320 comprises a high frequency capacitor C, a PFC inductor L and power switch devices (that is, a first bridge-arm composed of serially connected active switching elements S1, S2, and a second bridge-arm composed of serially connected passive switch elements D1, D2). The first and second bridge-arms and the high frequency capacitor C are in parallel connection; the power switch devices and the high frequency capacitor C are electrically coupled to the PFC inductor L; two middle points of the two bridge-arms are respectively connected with the output of the EMI filter 1310 or are connected with the output of the filter via the input inductor. The corresponding driving and control circuit 1330 of the PFC is configured to control the power switch devices; specifically, the corresponding driving and control circuit 1330 of the PFC comprises an output sampling voltage divider 1331 that is configured to sample the output V_{DC} of the PFC main circuit; input sampling voltage dividers 1332, 1333, 1334 are configured to sample the input voltage V_{AC-P} and V_{AC-N}, and a sampling circuit for sampling the input current I_L. After being compared with the corresponding reference signal V_{DC-ref}, the output signal V_{DC} of the output voltage sampling voltage divider 1335 is outputted by a voltage loop controller 1335 as a signal, which is calculated with the V_{AC} to obtain a reference signal I_{L-ref} of the input current I_L; after the input current I_L is calculated and compared with the I_{L-ref}, it passes a current loop controller 1336 to obtain a corresponding control signal PWM-S1 and PWM-S2 for controlling the switches S1 and S2.

[0068] The present disclosure is also suitable to be used in the DC/AC setting, such as the inverter. Figure 14 illustrates a power unit 120 comprising an

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inverter circuit; the DC input Vin passes a first bridge-arm composed of serially-connected active switching elements S1, S2 and a second bridge-arm composed of serially-connected active switching elements S3, S4 to give an AC signal; the signal passes a filtering circuit (comprising a filtering inductor L and an output capacitor Co) and then generates an output voltage Vo on the output capacitor Co. The specific control and driving circuit is not shown herein. Such inverter can also adopt a stacking structure that is similar to those described above regarding the PFC circuit. That is, the control unit is integrated from the first and second bridge-arms, the input capacitor Cin and the control driving circuit of the main circuit, while the power unit is integrated from the output filtering inductor L and the output capacitor Co. Of course, it is also feasible to integrate all elements of the main circuit (i.e., the output capacitor Cin, the S1 to S4, the filtering inductor L and the output capacitor Co) to form the power unit 120, and integrate the control unit to form the control and driving circuit.

[0069] Examples of control unit

[0070] The main purpose of the control unit is signal processing, and the height of most components thereof is smaller; hence, to improve the overall utilization percentage of the space, it is possible to use the thinness of the elements comprised in the unit as an evaluation index.

[0071] As discussed hereinabove, the controller (under certain specific application, the driving circuit can be viewed as part of the controller) responsible for sending the signal to the driving circuit or switch devices and elements necessary to the peripheral circuit thereof (such as the resistor,

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capacitor, etc.) must be comprised in the control unit. However, with the improvement of the integration level of the control chip, after these components/elements are disposed, there might be certain space left thereon. Accordingly, it is possible to add more components/elements in the control unit. Take Figure 3 as an example; if all the power components are disposed in the power unit 120, the layout of these components is illustrated in Figure 15. In Figure 15, the left-hand side illustrates the layout of the components/elements of the power unit 120, and the right-hand side illustrates the layout of the components/elements of the control unit 130. In Figure 15, the square box indicates the bearing plates 1710, 1720 on which the components/elements are placed; as to the components/elements disposed on the bearing plate 1710, 1720, those illustrate4d in the left-hand side correspond to components/elements illustrated in Figure 3. As illustrated in Figure 15, if the area of the power unit 120 and the area of the control unit 130 are the same (that is, the areas of the bearing plates 1710, 1720 of the two units are the same), apparently, the utilization percentage of the control unit 130 is low. To increase the utilization percentage of the area of each unit, it is feasible to move some components/elements from the power unit to the control unit 130; as illustrated in Figure 16, the primary switch tube S11, S12 is disposed at a position in adjacent to the lateral side of the control unit (i.e., they are disposed on the bearing plate 1720 of the control unit 130. In addition to the thinness, the standard for selecting the components/elements to be moved also includes whether it will affect the electric characteristics and whether it will achieve better functions.

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[0072] The primary side switch tubes S11, S12 at the high-voltage input side are semiconductors, as such, the thickness thereof is similar to or even thinner than the control chip, and hence, they could be placed in the control unit. For example, when the switch tubes S11 and S12 at the primary side are MOSFETs, if they are placed in the power unit, as illustrated in Figure 3, there are more than 4 pins (the gate electrode and source electrode for each switch) for the interconnection of the power unit 120 and control unit 130; if they are placed in the control unit 130, there is only two pins for the interconnection of the control unit 130 and the power unit, such as the connection point of the switch tubes S11 and S12 at the primary side and the source electrode of the switch tube S12, as illustrated in Figure 11. Moreover, since the high-voltage input side is not particularly sensitive to the distribution parameter of the circuits, the effect to the electric characteristics resulted from moving them to the control unit 130 is within the acceptable range. Of course, if the switch tubes S11 and S12 at the primary side are moved, the input capacitor C1 and the driving circuit thereof should also be moved to the control unit 130. Putting these elements in close proximity will not only reduce the voltage peak of the switch tubes S11 and S12 at the primary side, but also reduce unnecessary pins in the power unit.

[0073] Figure 16 is a schematic diagram illustrating an embodiment where some of the switch devices are disposed in the control unit 130. The control unit 130 comprises an input capacitor C1, the resonant capacitor C2 and the primary side switch tubes S11, S12; the power unit 120 comprises a plurality of switch devices and a bearing plate 1710 for bearing the switch devices (such as, S11, S12), as well as an insulation material 3430 (illustrated in Figure 25) for encapsulating the switch devices; the switch devices are distributed at a

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position along the pads 3440 (illustrated in Figure 25). The power unit 120 comprises a transformer T1, a resonant inductor L1, an output capacitor C3 and secondary side switch tubes S21, S22, S23, S24. As could be seen, the utilization percentage of the left-hand side of the control unit 130 is significantly increased, while the inductor (i.e., the resonant inductor L1), the capacitor (i.e., the output capacitor C3) and switch devices (i.e., secondary side switch tubes S21, S22, S23, S24) are disposed at a position on the bearing plate 1710 in adjacent to the lateral side of the power unit. On the left-hand side of the power unit 120, more space is left for the magnetic element, which is significant to the increase of the efficiency. Accordingly, embodiments of the present disclosure may take care of both the high efficiency and high power pressure. It should be noted that since the switch tubes S11, S12 are not disposed in the power unit 120, the input of the power unit 120 comes from the control unit 130, and is a high frequency AC power signal modulated by the switch tubes S11, S12; for example the frequency of the signal is about 500 KHZ or even higher than 3 MHZ, and the value may be less than 12 V to more than 400 V.

[0074] If, in certain applications, the positions of the secondary side switch tubes S21, S22, S23, S24 are not sensitive to the electric characteristics, it is also possible to dispose the secondary side switch tubes S21, S22, S23, S24, the driver 330 and the output capacitor C3, as well as the Oring MOS in the control unit 130 so as to further increase the space utilization percentage.

[0075] Regarding the stacking structure illustrated in Figure 10, if the control unit 130 is disposed at the lower position, the control unit 130 will be sandwiched between the power unit 120 and the main board 110; then the pins from the

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output terminal of the power unit 120 to the main board become longer, which might affect its ability to response to the variation of load, in particularly in cases where the load is a data processing chip like the CPU. In this case, it is possible to dispose part of the output capacitor C3 (or the corresponding POL output capacitor C4 illustrated in Figure 11) of the main circuit in the control unit 130; in this case, the control unit 130 comprises the output capacitor C3, thereby reducing the effect resulted from the length of the pins. Of course, to do this, it is a requisite that there is a good connection between part of the output capacitor C3 and pins 140.

[0076] In the above-mentioned embodiments, the control unit 130 comprises a bearing plate, such as the printed circuit board or the lead frame, etc. Of course, the whole control unit 130 can be implemented by an embedding technique. The control unit 130 can also uses inter-stacking elements within the unit, so that the surface conductors of the elements are used for electric connection. Using the embedding technique, some electric elements, such as the control IC, the resistor, the capacitor and even the power semiconductor are embedded in the bearing plate. In this way, the control unit is very thin and the area thereof is very small; also, a more delicate circuit wiring at the internal and surface of the unit can be achieved. By using the embedding techniques, one can easily achieve the interconnection between the upper and lower surfaces without limited by the position; that is, it can directly use the corresponding pins without using the pins injected from the lateral side, which is illustrated in Figure 25. For example, a circuit comprising a transformer and a synchronous rectifier, such as a bridge resonant circuit, can be used to implement a control unit using the embedding technique then, the control unit is stacked with a

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power module comprising the transformer and synchronous rectifier, and the resultant circuit is characterized in that: the power unit comprises at least one transformer (Core and Winding), the output synchronous rectifier, part of the output capacitor, the control signal of the SR MOS (generated by the power module or provided by the control unit), so as to achieve a high efficiency of the power stage; the power unit still uses the pins (Pin) injected from the lateral side, the Pin comprises the positive and negative electrodes of the output, and the two electrodes of the high frequency pulse at the input side that has been modulated. The control unit comprises an embedded control logic IC, responsible for sampling, controlling signal and driving the signal generation, protecting, and necessary communication to the outside of the power supply, as well as at least one pair of power elements at the high-voltage side, responsible for generating the input-side high frequency pulse to be transmitted to the power unit; the pins of the control unit can be arranged at the lateral side or passing through the upper or lower surface, depending on the need, or can be arranged to form the connection from the internal position to the surface and arranged at the surface as needed; after the embedding, the control unit is very thin, e.g., about 1 mm; accordingly, the Pins can be mainly the SMD pins, so as to enhance the connection strength of the Pins. By using the embedding technique, one can easily achieve the wiring capability similar to the PCB, so as to implement more complex interconnection at the surface, and support the stacking combination with more content, for example, disposing some necessary elements that is difficult to be embedded in the control unit, e.g., the input EMI filter (i.e., the input capacitor) together with the power unit at the surface of the control unit. This embodiment achieve a very small size, and

hence, it is more suitable in high-frequency operating settings, such as the one with an operation frequency of more than 1 MHZ. Hence, the converting circuit is preferably a resonant-type circuit. The thickness of the embedded-type control unit is preferably less than 2 mm.

[0077] The control unit 130 can be the assembly of the control circuits according to the above-mentioned examples, can be a control circuit comprising some components/elements of the power circuit, and even the driving circuit; alternatively, it can also be a power supply converter with full function, such as the one as illustrated in Figure 7. In this way, the control unit and the power unit are stacked together, and connected through pins, as well as connected to the main board through the pins, thereby achieving a structure with two or more inter-stacking power units. Nonetheless, at least one of the power units comprises the components/elements of the control unit. Such structure is often suitable for use in a system infrastructure with multi-stage power unit in parallel connection or cascaded connection.

[0078] Examples of power unit

[0079] In sum, the power unit can be a complete DC/DC or AC/DC power supply converter that can operate on its own, such as, the isolated transforming module DCX, the point-of-load (POL) DC converter, the front regulate module (FRM), the regulated bus converter (RBC), the PFC circuit, the auxiliary power supply module, etc.; that is, one power supply converter that comprises the power stage circuit and the control circuit; alternatively, it could be only the power stage circuit thereof, or even a portion of the power stage circuit such as those described in the above embodiments; said portion can be the part that

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should be placed in proximity, such as the three key elements illustrated in Figure 16, that is, the transformer T1, the output rectifying element (e.g., the secondary side switch tubes S21, S22, S23, S24) and the output capacitor C3. The power unit may have the isolation capability of the isolated transforming module DCX, RBC; that is, it comprises at least one transformer; or it may not require the isolation, like the point-of-load (POL) DC converter, the front regulate module (FRM), and the PFC circuit; that is, it comprises at least one inductor.

[0080] The transformer and inductor on the power unit can be integrated or separated.

[0081] The input of the power unit can be a direct current or an industrial-frequency alternating current, or the high-frequency alternating current illustrated in Figure 16.

[0082] The output of the power unit can be within various voltage ranges, such as 0.1 to 12 V, or 12 V to 400 V. The load can be another power supply converter, the hard drive, the memory, the graphic processing chip, the CPU, the communication ASIC, or other data processing chips.

[0083] Moreover, the power unit, just like the control unit, may comprise a bearing plate, such as the printed circuit board or the lead frame, and the electric connection among the components of the power unit is achieved by the trace on the bearing plate, the components/elements of the power unit can also be placed on the bearing plate; or can be implemented by the embedding technique; that is, the electric element, such as the transistor and the capacitor are embedded in the bearing plate. Moreover, the power unit can also uses

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inter-stacking elements within the unit, so that the surface conductors of the elements are used for electric connection

[0084] When the whole circuit comprises two or more power units, it is possible to use identical power units that are in parallel connection to implement a conversion of higher power and higher current; or they can be serially connected to implement a conversion of higher power and higher voltage; alternatively, different power units that are serially connected (as illustrated in Figure 8) are used to achieve a greater operating range; or different power units can be used, in which they share a common input to provide the power supply conversion of multiple outputs; or different power units can be so that one output can receive the power supply conversion from multiple inputs.

[0085] In view of the foregoing, the application range of the present disclosure is quite broad; it may enhance the performance of the server. Of course, the method for implementing the power converter is also suitable for use in other application settings.

[0086] Design of stack structure

[0087] In one aspect of the present invention, in one server, a power supply converter is divided into at least two units, i.e., at least one control unit 130 and one power unit 120, that are stacked to take full advantage of the height, thereby providing a power supply converter with high efficiency and high power pressure, so as to provide a server with better performance. The stacking of the power supply converter are as follows.

[0088] As illustrated in Figure 17, the unit with a greater area among the control unit and the power unit is used as the first unit 2010, while the one with the

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smaller area is used as the second unit 2020; the first unit 2010 is disposed between the second unit 2020 and the main board 110; the area of each unit 2010, 2020 differs, and the smaller one is stacked on the bigger one to form a power supply converter which is then disposed on the main board 110. As illustrated in Figure 18, the control unit and the power unit are integrated as an isolated transforming module DCX, and front regulate module (FRM); this is one implementation of the above-mentioned front regulate module (FRM)+isolated transforming module DCX infrastructure; however, to achieve a higher efficiency, the external inductor L of the front regulate module (FRM) is disposed outside. The front regulate module (FRM) and the external inductor L are then disposed above the isolated transforming module DCX to form a power supply converter, which is then disposed on the main board 110.

[0089] As illustrated in Figure 19, the unit with a greater area among the control unit and the power unit is used as the first unit 2010, while the one with the smaller area is used as the second unit 2020; the second unit 2020 is disposed between the first unit 2010 and the main board 110; the area of each unit 2010, 2020 differs, and the smaller one is stacked at the lower surface of the bigger one to form a power supply converter which is then disposed on the main board 110.

[0090] As illustrated in Figure 20, the power unit 120 and the load are disposed at one side of the main board 110, while the control unit 130 is disposed on the main board 110 at a side that is opposite to the power unit 120; the power unit 120 and the control unit 130 are respectively disposed at the opposite surfaces of the main board 110; that is, each unit 120, 130 is respectively disposed at the

upper and lower surfaces of the main board 110; the control unit 130 is electrically connected to the pins 140 via the conducting through holes 2310 of the main board 110; the overlapping part of the projection areas of the units accounts for at least one-third of the projection area of said unit. Apparently, due to the limitation of dissipation and the thickness, it is preferably that the control unit 130 is disposed at the lower surface of the main board, and the power unit 120 is disposed at the upper surface of the main board 110.

[0091] Obviously, the above-mentioned implementation means can effectively utilize the height, so as to achieve both the high efficiency and high power pressure of the power supply, to give a power supply module with better performance, especially in applications such as the server power supply.

[0092] Pads arrangement and implementation

[0093] A power supply converter comprises many pins. Pins involved in the connection between the converter and the system include, for example, converter power input/output pins, and pins for system communication, and pins for internal interconnection, such as the connection between the power unit and the control unit. Since the terms pins has a specific definition, here, the pins injected from the components/elements on the bearing plate is referred to as the pads. Referring to Figure 21, the pads can be divided into two main types, the power pads and the signal pads, depending on the current level. The power pads are the pads that the converter power current passes pads, which is generally responsible for the electric connection between components/elements of the power circuit; since the current level passing them is higher, these pads are often thicker; that is, the cross-sectional area of the

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pad is bigger. The signal pads are the pads responsible for transmitting the signal in the converter; for example, the control circuit in the control unit often transmits the control signal to the driving circuit through the signal pads so as to control the conduction and turning-off of the power components/elements. Generally, the current level passing through control pads is lower, and hence, the pads are thinner; that is, the cross-sectional area thereof should not be too big, and the size often depends on the capability required.

[0094] When the power supply converter is an isolated circuit (the isolation is often achieved by the transformer of the power circuit); that is, the input/output thereof has the requirement of isolated safety voltage. Hence, depending on the position thereof, the pads can divided as the primary lateral group pads (i.e., the pads disposed at the primary side of the transformer) and secondary lateral group pads (i.e., the pads disposed at the secondary side of the transformer). The two groups of pads should be separated by a specific distance to meet the safety requirement; for example, when the input of the converter is 400 V, an isolation of at least 2000 V is required and hence, any pads in one group should be separated from any pads in the other groups by at least 4 to 8 mm; while when the input is 36 to 72 V, an safety isolation voltage of 1500 V is often required, and the distance is 1 to 4 mm. Regarding the primary lateral group, since the voltage of the input is relatively high, the current is smaller, and the cross-sectional area of such pads is relatively small. For the secondary lateral group, since the voltage is lower, the current is higher, and hence, the cross-sectional area of the pads is greater. For example, for the 48 V to 1 V converter, the difference of the current is 48 folds, if the same current density is used to define the volume of the pads, there would be a 48-fold difference, and

it is obvious that the secondary lateral group requires more position for the disposition.

[0095] The pads can be disposed at the four sides of the power unit, as illustrated in Figure 21 and Figure 22. In Figure 21, the primary lateral group pads 2410 and the secondary lateral group pads 2420 respectively occupy the two sides of the power unit, and said two sides are parallel to each other; the primary lateral group pads 2410 comprises first signal pads 2411 and first power pads 2412, the cross-sectional area of the first power pads 2412 is greater than the cross-sectional area of the first signal pads 2411; the secondary lateral group pads 2420 comprises second signal pads 2421 and second power pads 2422, the cross-sectional area of the second power pads 2422 is greater than the cross-sectional area of the second signal pads 2421, the number of the second power pads 2422 is greater than the number of the first power pads 2412. The arrangement in Figure 21 is suitable for applications with lower output current. Figure 22, on the other hand, is suitable for use in application with higher current output; the primary lateral group pads 2410 are distributed along one side of the unit, and the secondary lateral group pads 2420 are distributed along the remaining three sides of the unit, and are spaced from the primary lateral group pads 2410 by a safety distance d. When the current is higher, a single pad has a great electrical characteristics; when multiple pads are required, i.e. multiplex pads, they can be arranged in alternating positive and negative electrodes, such as, Vo+, Vo-, so that the induction resistance of the pads is as low as possible; in this way, when applied in loads like CPU, there is a better dynamic response and reduce the utilization rate of the capacitor of the main board.

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[0096] In the present application, the pins are electrically coupled with the pads. Figure 24 is a front view illustrating the connection of the pins and pads for implementing the interconnection of each unit. In Figure 24, the exemplified pins are surface-mount pins. The L-shaped surface-mount pins 2610 electrically connects each unit 120, 130 to form a power supply converter with the surface-mount pins, which is then disposed on the main board 110. After changing the pins to the I-shaped pins, the power supply converter with the I-shaped in-line pins 2710 (as illustrated in Figure 23) is formed.

[0097] Figure 25

[0098] Before the assembly of the pins 140, each unit 120, 130 can be encapsulated with the packaging technique such as molding or embedding to for a regular surface, such as the recess 3410 illustrated un Figure 25; since the insulation material 3430 has the recess 3410 disposed thereon for fitting the installation of the pins 140, it is more advantageous to the delicate utilization of the space, and then the surface-mount pins are installed thereon. Specifically, any one of the control unit and the power unit comprises a bearing plate 3420 and insulation material 3430; the insulation material 3430 is formed on the two opposite surfaces of the bearing plate 3420l the lateral side of the bearing plate 3420 is disposed with the pads 3440; the soldering material 3450 on the pads 3440 is soldered to the pins 140. At the edge of the upper and lower surface of the insulation material 3430, there is a recess 3410; the two terminals of each pin 140 has the SMD pad 2910 extending to the recess 3410 at the upper and lower surfaces, the recess 3410 has the bonding material 3460 disposed thereon for bonding with the SMD pads 2910.

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[0099] The unit illustrated in Figure 25 can be any of the above-mentioned power unit and/or control unit; the pads 3440 are distributed along the lateral side of the power unit and the lateral side of the control unit; the pins 140 and pads 3440 are electrically coupled. The pins 140 are surface-mount pins, and are distributed along the outer surface of the power unit and control unit, and are electrically coupled to the pads 3440. The pads 3440' are further distributed along a side of the power unit that is perpendicular to the side at which the and pads 3440 are disposed; although in Figure 25, the pads 3440' are only distributed along the lower surface; the present invention is not limited thereto; in one embodiment, pads are distributed along the lateral side of the power unit 120 and the upper and lower surfaces of the control unit 130, and the pins 140 and pads 3440 are electrically coupled.

[00100] The surface-mount pins can be installed on each surface of the unit, but in order to achieve a better dissipation effect and to further reduce the overall size of the module, in the above examples, the pads are disposed at the lateral side of the bearing plate in each unit, and the surface-mount pins are soldered to connect with in injected pins of the components of the unit and the control signal injected pins. However, under certain special circumstances, as illustrated in Figure 33, the pads in the first unit 2010 can also be disposed at the stacking surface of the second unit 2020 and the inductor L, and the pins are used to implement the typical connection between the first unit 2010 and the second unit 2020 and the inductor L. The contact surface other than the solder points of the pins and pads can be applied with glues or the like, so that the pins are bonded to the surface of each unit, thereby increasing the mechanical strength and the reliability.

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[00101] Heat dissipation

[00102] After stacking each unit to form a module, the heat dissipation pathway is altered, as compared with the conventional design in which the units are individually disposed.

[00103] Figure 26 illustrates the installation of the heat dissipation unit. As illustrated in Figure 26, the electrically-isolated heat dissipation unit 3910 is disposed on the power unit 120; the power unit 120 is disposed on the control unit 130; the control unit 130 is disposed on the main board 110; or, as illustrated in Figure 40, the electrically-isolated heat dissipation unit 4010 is disposed on the lateral sides of the power unit 120 and the control unit 130. It can be disposed at the upper surface or the lateral side of the assembled module. To avoid affecting the electric characteristics of the module, the heat dissipation unit can be an electric insulation material, such as the ceramic. Alternatively, when the heat dissipation unit is a conducting material such as aluminum, copper, graphite, etc., thereby should be a thermal-conducting and electrical-insulation material (such as the ceramic sheet or the like) between the heat dissipation unit and the pins. The heat dissipation units are all disposed above the pad or pin assembly. To ensure the heat dissipation effect, the thermal resistance between the heat dissipation unit and the pad or pin assembly should be less than 5°C/Watt. There is an insulation material between the heat dissipation unit and the pad or pin assembly.

[00104] Other optimized embodiments

[00105] According to the above-mentioned example, it is feasible to achieve a greater power by stacking multiple power units. Generally, these power units

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use the magnetic elements with the similar using/operating condition, such as a transformer or an inductor.

[00106] As illustrated in Figure 43, since the magnetic element often has an air space 4320, and the conductor nearby is often inducted and heated by the magnetic flux leaked from the air space 4320, thereby causing loss. By sharing the magnetic core 4310 through stacking, the air space 4320 of the magnetic core 4310 can be disposed at the stacking space 4330 between the power units 120, thereby keeping the air space from the conductor so as to reduce the loss.

[00107] According to the above-mentioned embodiments, the power unit and the control unit are vertically stacked to form a power supply module. In fact, if the power supply is rotated by 90 degrees so that the power unit and the control unit are stacked horizontally, and are interconnected with each other and are respectively connected with the main board through the pins, this structure also has desirable applicability. Therefore, according to embodiments of the present disclosure, the power unit and the control unit can not only stack above each other, but also stack to the left or right of each other in the horizontal direction.

[00108] In view of the foregoing, using the Quasi-Cascade components, optimized driving, optimized application and optimized packaging disclosed herein, it is possible to increase the power density or efficiency of the power supply converter, thereby achieving a better electric performance, higher frequency performance and greater reliability, as compared with conventional technology. In this way, the characteristics of the components can be fully

utilized, and it is more convenient to use the apparatus with the present packaging solution; therefore, the present disclosure facilitate the improvement of the power density or efficiency. The specific driving, application and packaging means provided by the present disclosure are quite feasible and effective. The present invention is suitable for improving the overall performance and the cost/performance ratio of the power supply converter.

[00109] Although various embodiments of the invention have been described above with a certain degree of particularity, or with reference to one or more individual embodiments, they are not limiting to the scope of the present disclosure. Those with ordinary skill in the art could make numerous alterations to the disclosed embodiments without departing from the spirit or scope of this invention. Accordingly, the protection scope of the present disclosure shall be defined by the accompany claims.

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WHAT IS CLAIMED IS:

1. A power supply apparatus, comprising:

a power unit electrically connected with a motherboard, comprising a first base plate, at least a power switch chip allocated at the first base plate and a plurality of pads;

a control unit stacked with the power unit, comprising a second base plate and at least a control chip for controlling the power switch chip turn on/ off in the power unit and a plurality of pads; and

a plurality of pins for electrically connecting the power unit to the control unit and mother board and allocated at periphery of the power unit and control unit;

wherein the plurality of pads of the power unit and control unit are allocated on side facet of the first base plate and second base plate respectively, both plurality of pads of the power unit and control unit are electrically connected with the plurality of pins so that the power unit and the control unit could electrically connected with each other, the power supply apparatus provides a power source for a load in the neighborhood thereof on the motherboard.

2. The power supply apparatus of claim 1, wherein the first base plate and the second base plate are in approximate sizes.

3. The power supply apparatus of claim 1, wherein the second base plate integrates a power switch chip to improve area utilization thereof.

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4. The power supply apparatus of claim 1, further comprising molding material, wherein the molding material encapsulates the power unit and control unit respectively, the plurality of pads of the power unit and control unit emerges from molding material respectively.

5. The power supply apparatus of claim 4, wherein the molding material of the control unit has a plurality of recesses reserved for connection with the pins thereof.

6. The power supply apparatus of claim 4, wherein the molding material encapsulates two sides of the power unit.

7. The power supply apparatus of claim 6, wherein the power unit further comprises bottom pads emerged from one side of power unit that is encapsulated by the molding material for adjacent electrical connection thereof.

8. The power supply apparatus of claim 1, further comprising another power unit stacked with the power unit and the control unit, wherein the another power unit is parallel connected with the power unit and controlled by the control unit.

9. The power supply apparatus of claim 8, wherein each of the power unit and the another power unit has a magnetic device, the magnetic devices of the power unit and the another power unit share the same magnetic core.

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10. The power supply apparatus of claim 1, wherein the plurality of pins cover outer surface of the power unit and the control unit respectively as much as possible to expand the surface area thereof.

11. The power supply apparatus of claim 1, wherein the power unit is the one close to the motherboard, the control unit is the other one stacked on the power unit.

12. The power supply apparatus of claim 1, wherein the power unit and control unit are allocated on two opposite sides of the motherboard respectively, the pins pass through the motherboard to connect the power unit with control unit.

13. The power supply apparatus of claim 1, further comprising:

a heat sink, attached with the power unit to improve heat dissipation.

14. A power supply apparatus, comprising:

a first stage power converter received a power source from a mother board and configured with a plurality of pads located on side facet thereof;

a second stage power converter configured with a plurality of pads located on side facet thereof and stacked with the first stage power converter to receive an output of the first stage power converter to provide a power to a load in adjacent area thereof on the motherboard; and

a plurality of pins connected with the pads of the first or/and second stage power converter and the motherboard to realize the electrical connection therebetween.

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15. The power supply apparatus of claim 14, wherein the output voltage of the second stage power converter is lower than the output voltage of the first stage power converter.

16. The power supply apparatus of claim 14, wherein the first stage converter and the second stage converter are configured in approximate sizes.

17. A power supply apparatus, comprising:

a first unit electrically connected with a motherboard, comprising a first base plate, at least a power switch chip allocated at the first base plate and a plurality of pads;

a second unit stacked with the first unit, having a plurality of connection pads for electrical connection; and

a plurality of pins for electrically connecting the first unit to the second unit and mother board and allocated at periphery of the first unit ;

wherein the plurality of pads of the first unit are allocated on side facet of the first base plate, both plurality of pads of the first unit and plurality of connection pads of the second unit are electrically connected with the plurality of pins so that the first unit and the second unit could electrically connected with each other, the power supply apparatus provides a power source for a load in the neighborhood thereof on the motherboard.

18. The power supply apparatus of claim 17, wherein the connection pads of the second unit allocates on the surface that stacked on the first unit.

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19. The power supply apparatus of claim 18, wherein the pins extends along the out surface of the first unit to connect the connection pad of the second unit with the first unit.

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ABSTRACT OF THE DISCLOSURE

Disclosed herein is a power supply apparatus that includes a main board, a power unit, a control unit, pads and a pin. The control unit and the power unit are stacked on the main board and at a position in adjacent to a load; the plurality of pads are distributed along the lateral side of the power unit and the lateral side of the control unit; the plurality of pins and pads are electrically coupled and electrically coupled with the main board, the control unit and the power unit; the control unit is configured to control the power unit, so that the power unit supplies electricity to the adjacent load.

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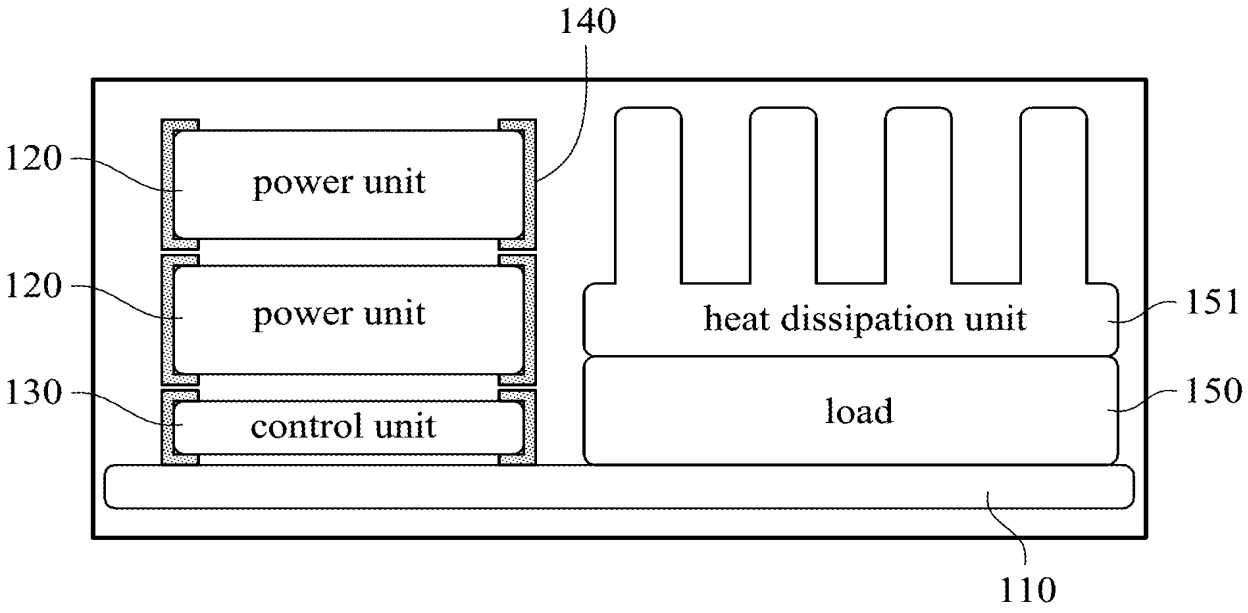


Fig. 1

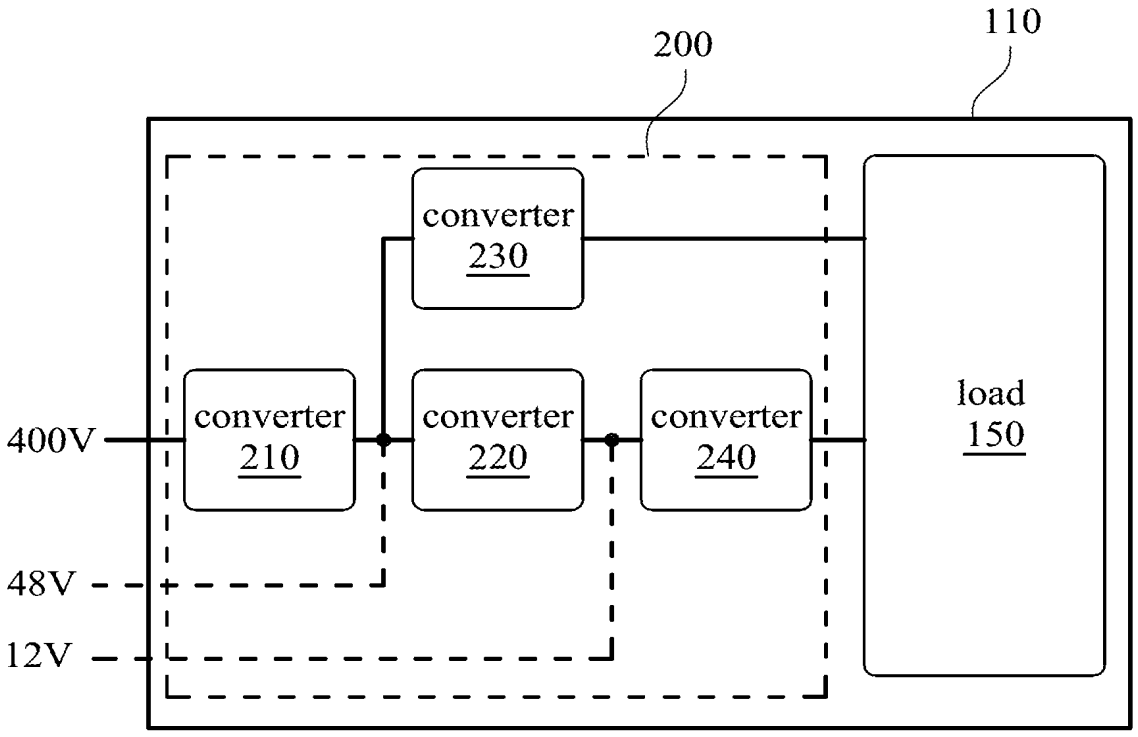


Fig. 2

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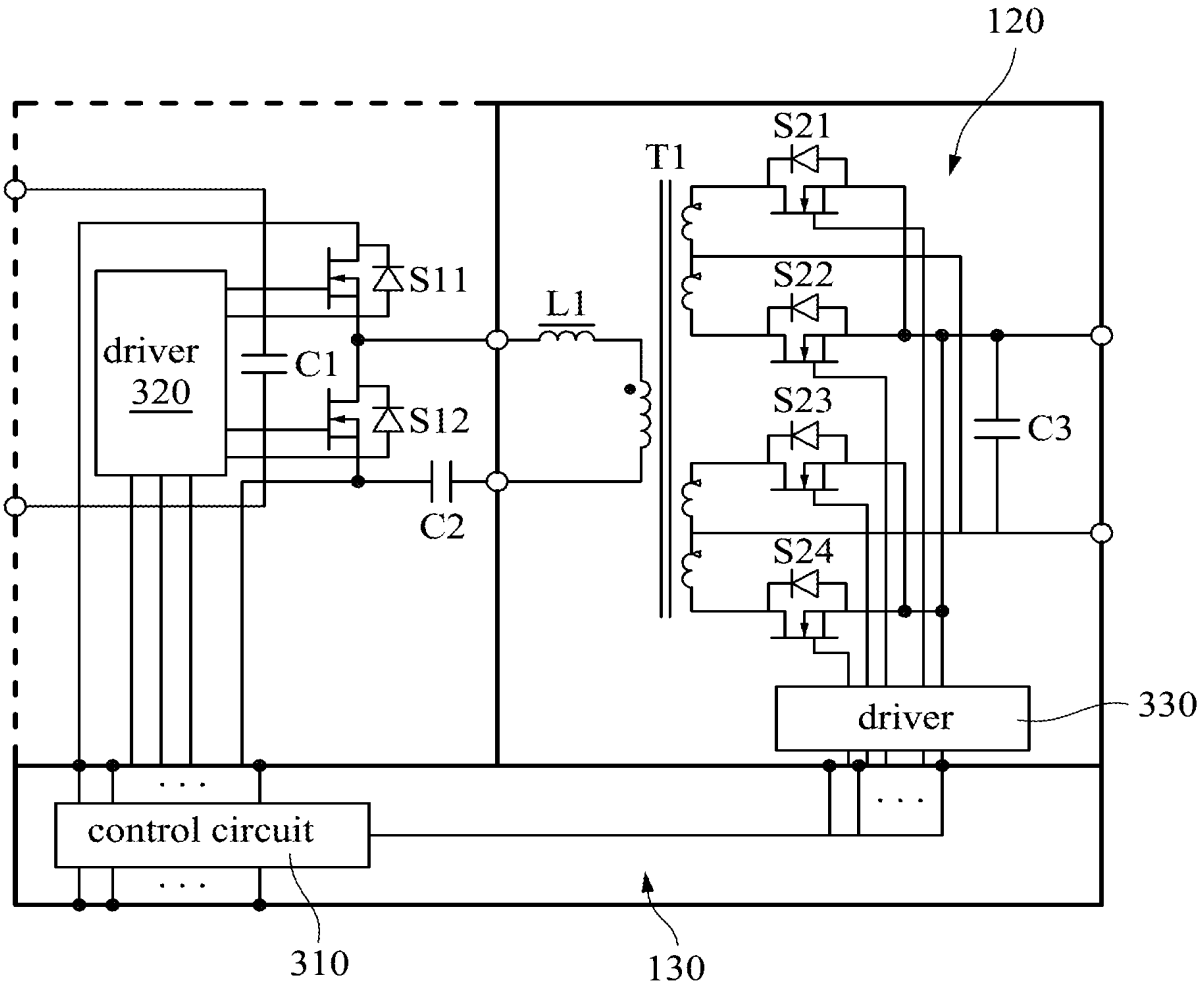


Fig. 3

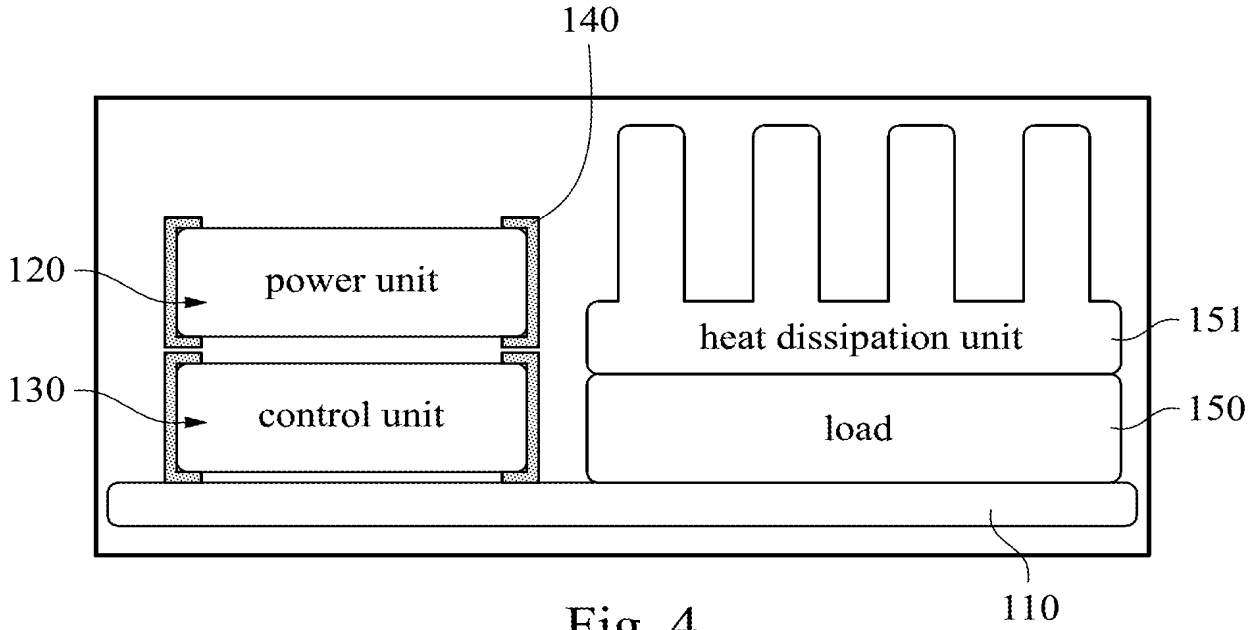


Fig. 4

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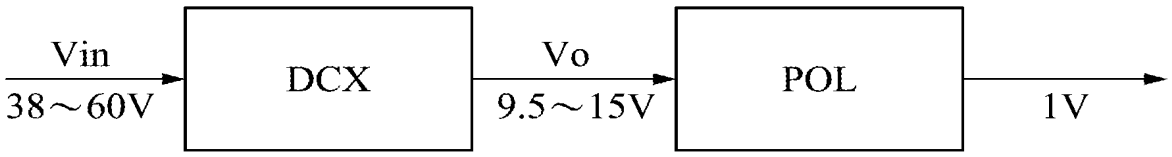


Fig. 5

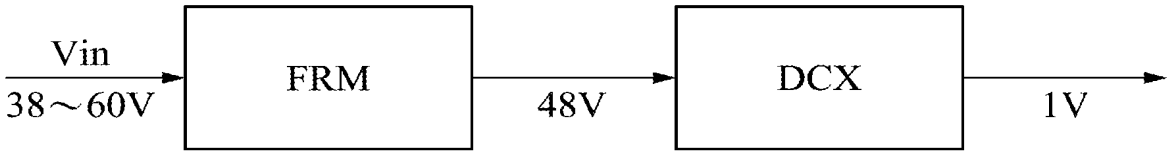


Fig. 6

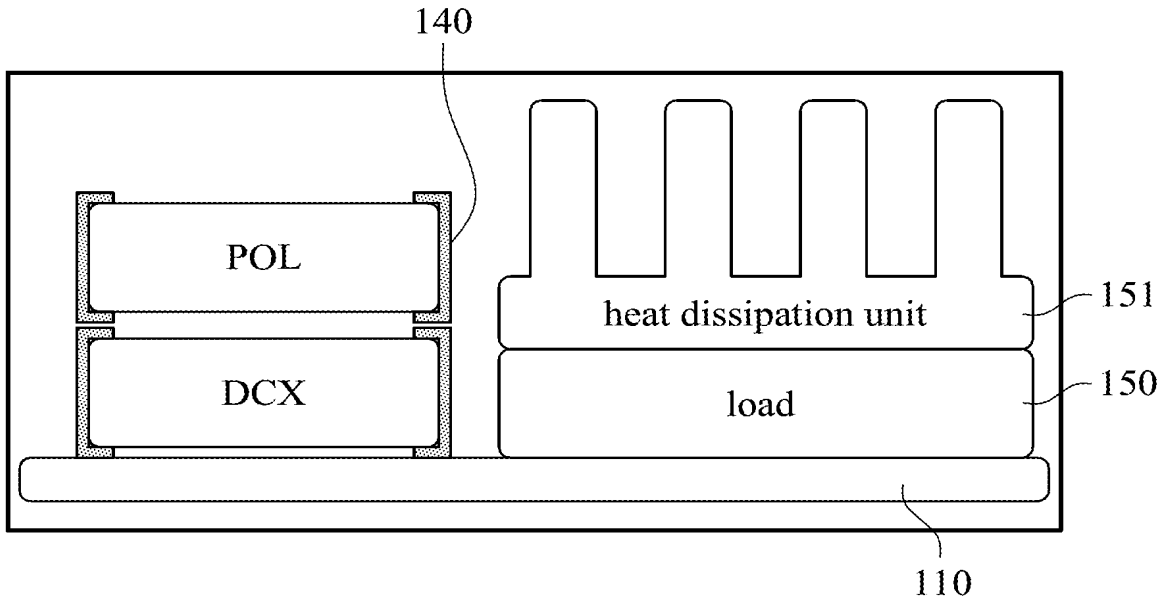


Fig. 7

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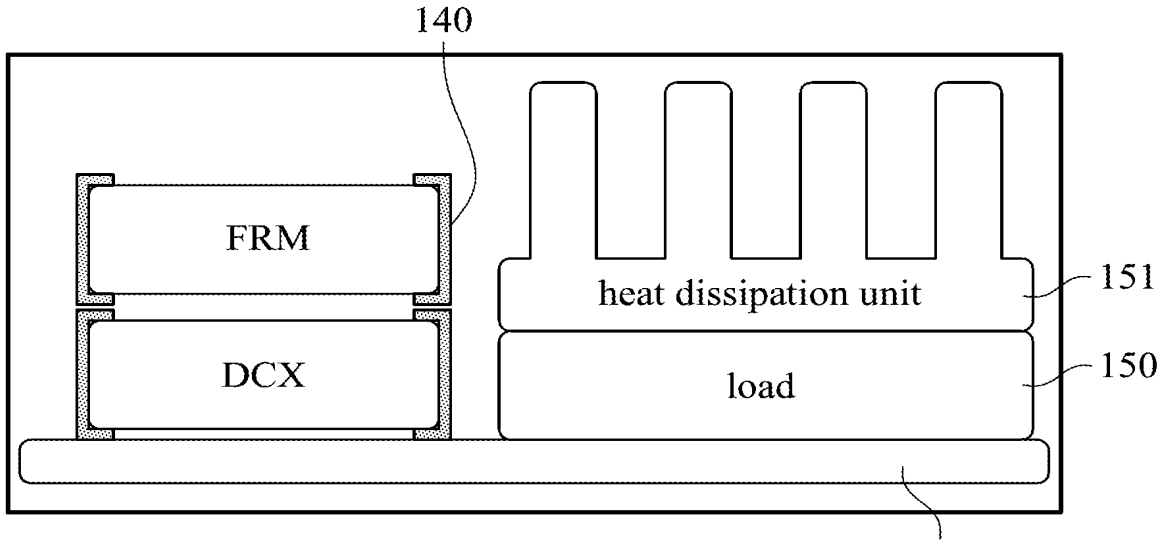


Fig. 8

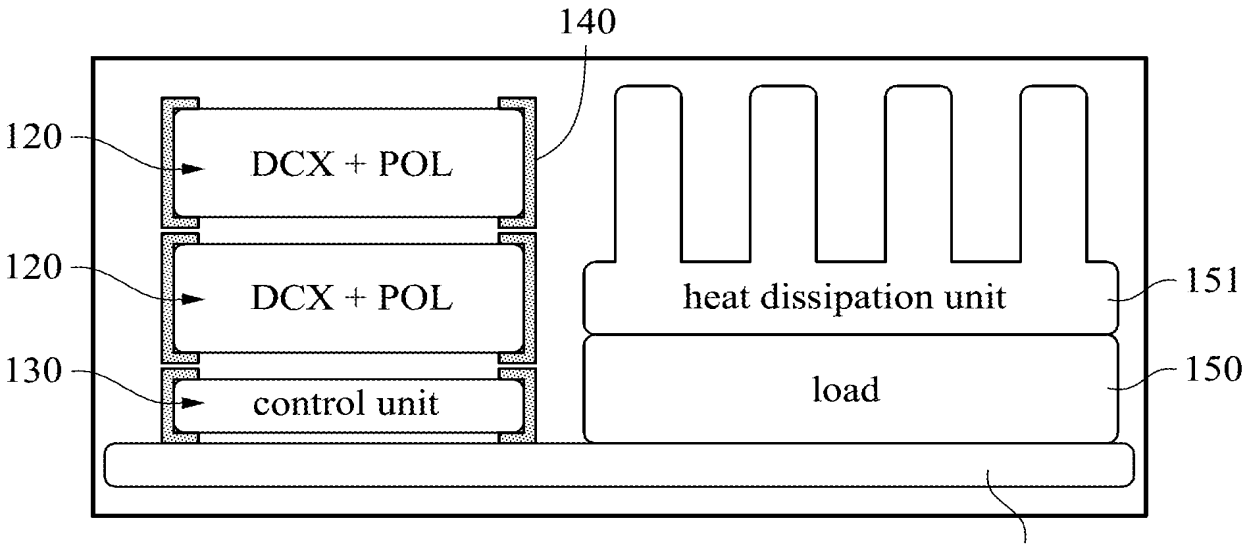


Fig. 9

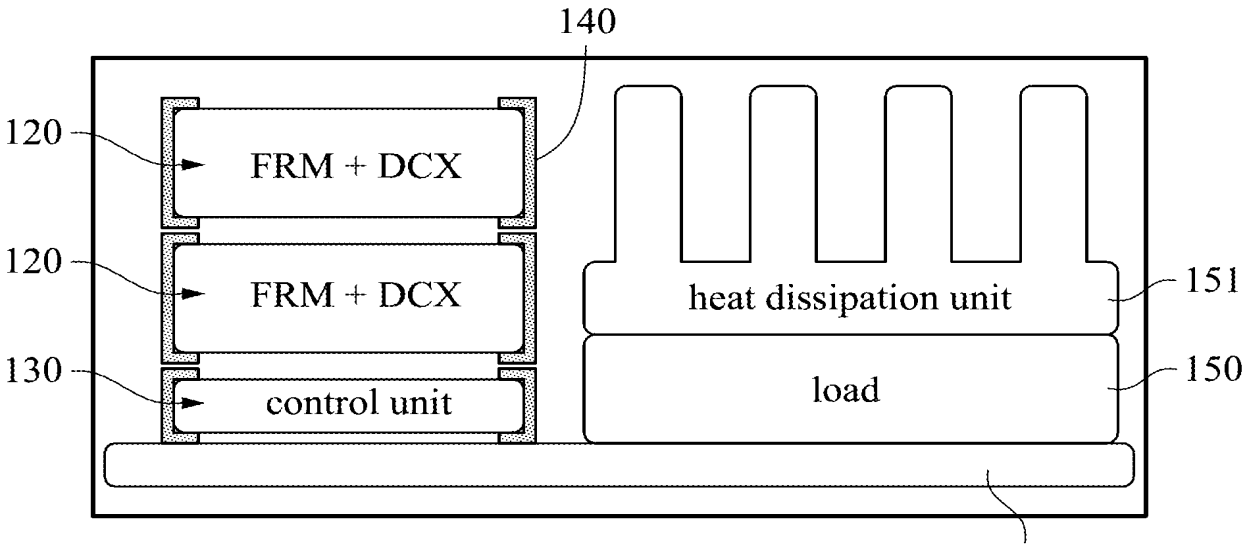


Fig. 10

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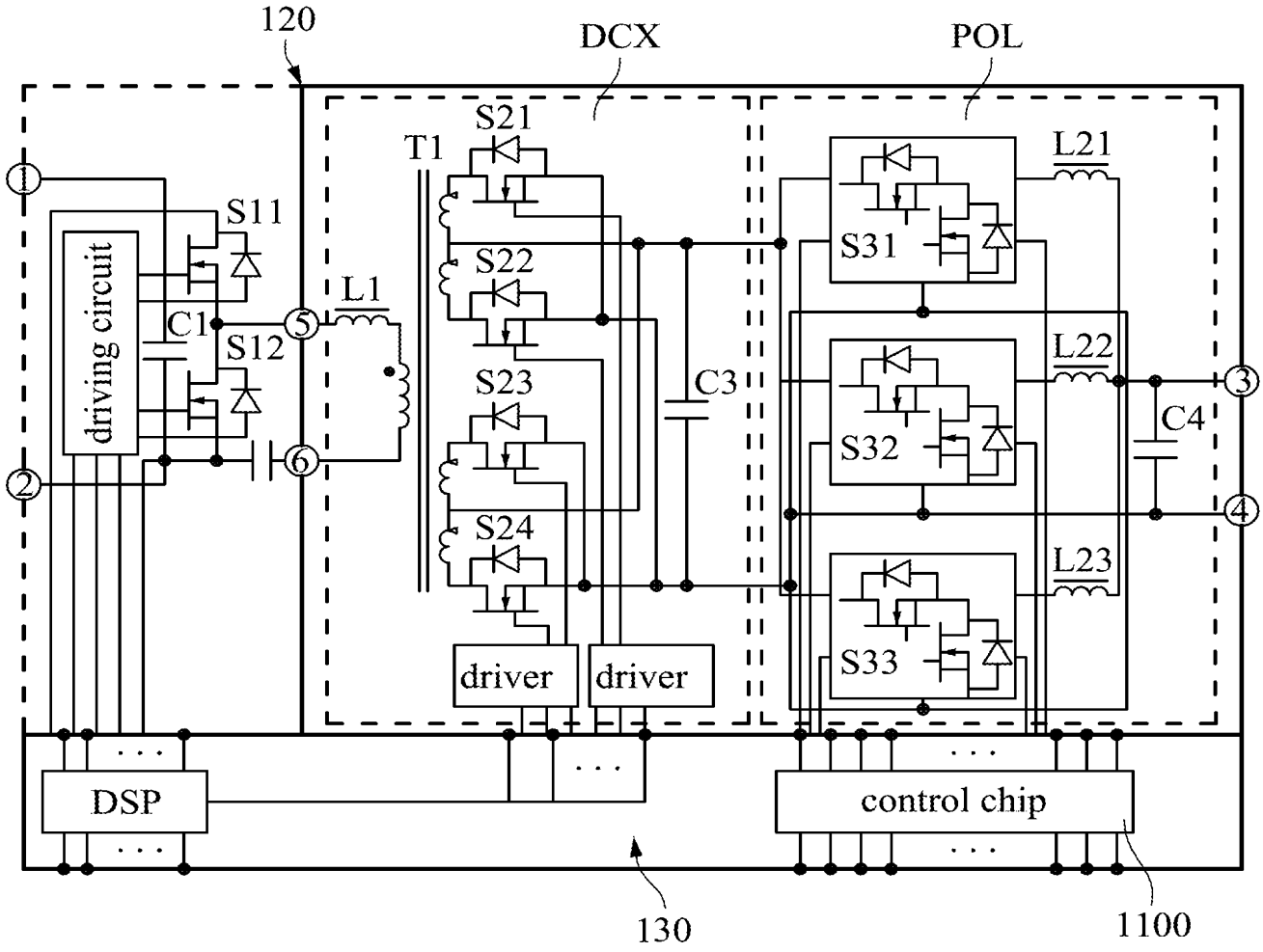


Fig. 11

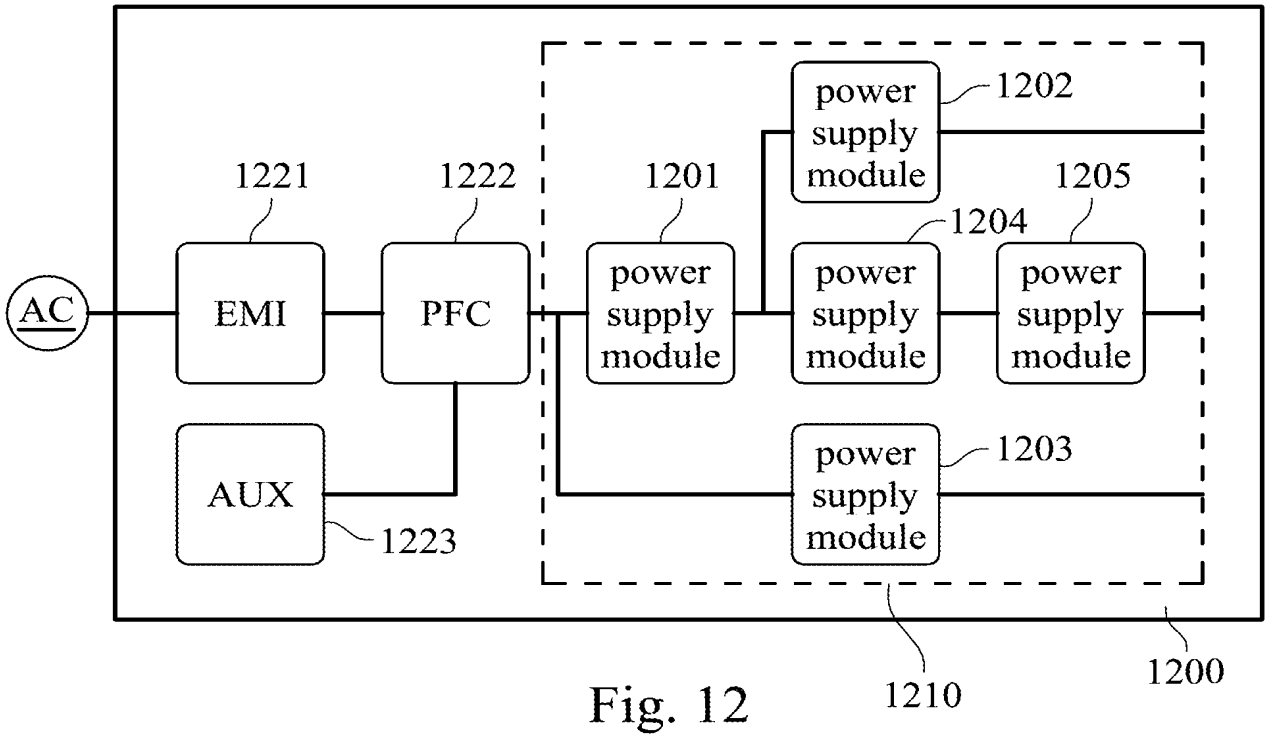


Fig. 12

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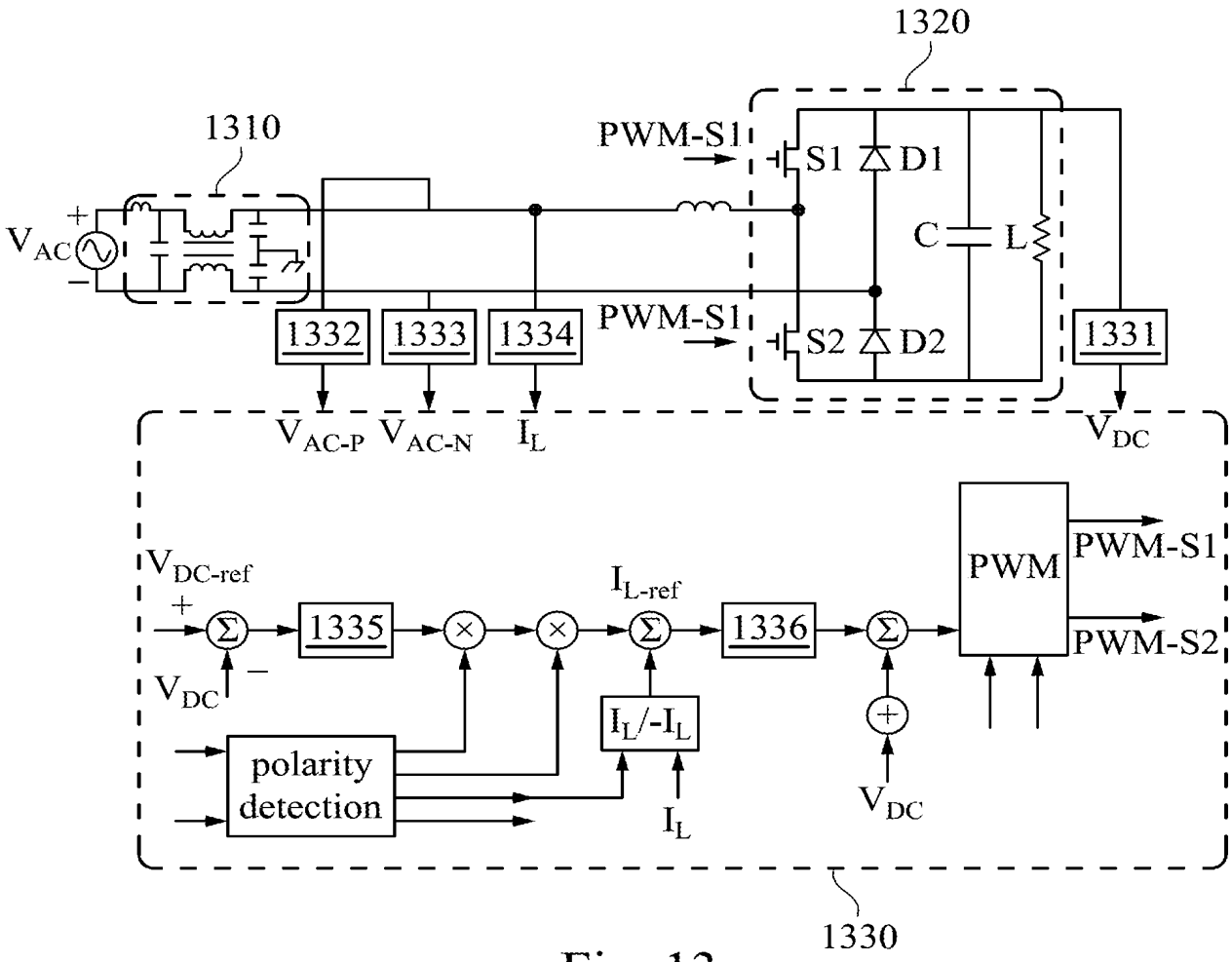


Fig. 13

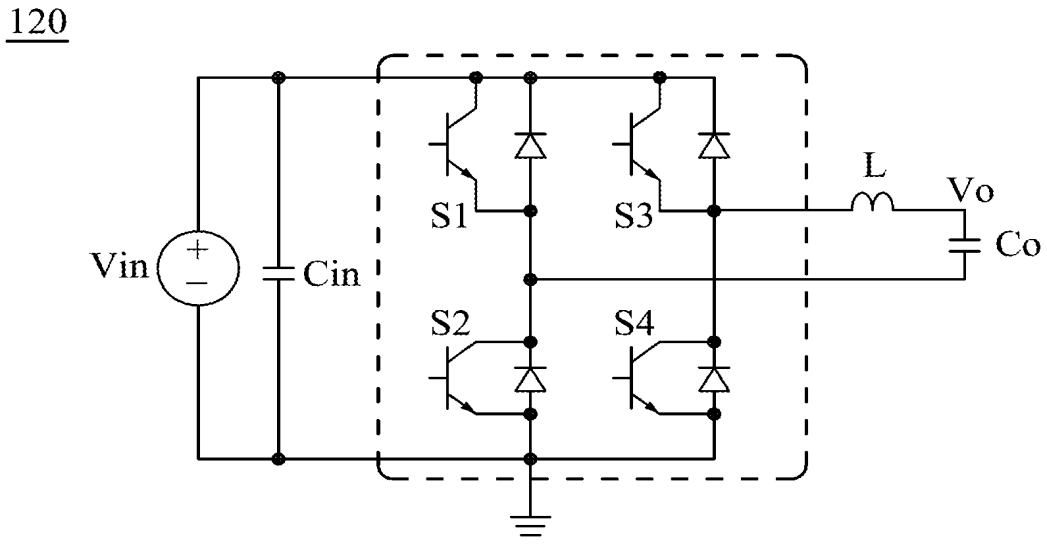


Fig. 14

IPR2024-00715 EX. 2005

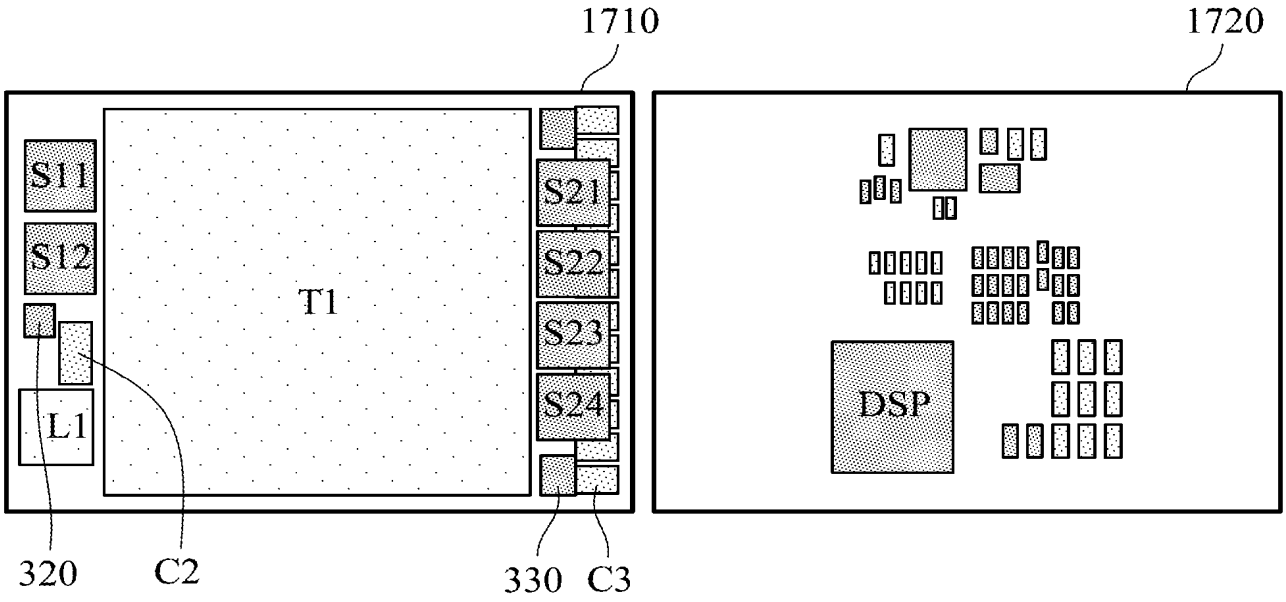


Fig. 15

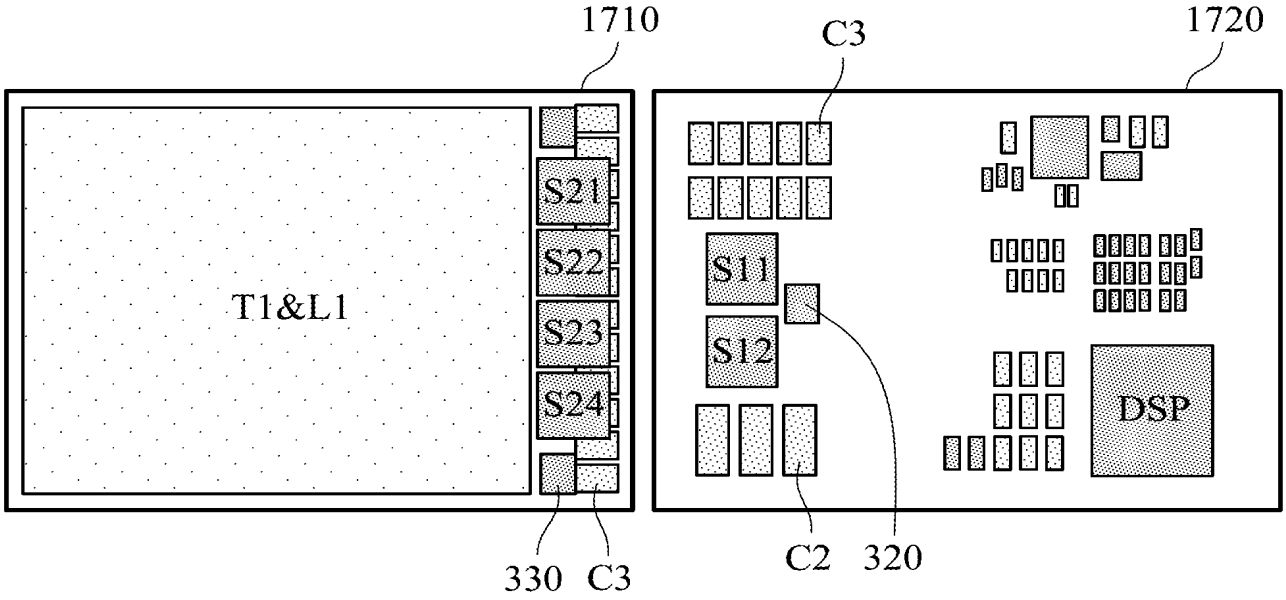


Fig. 16

IPR2024-00715 EX. 2005

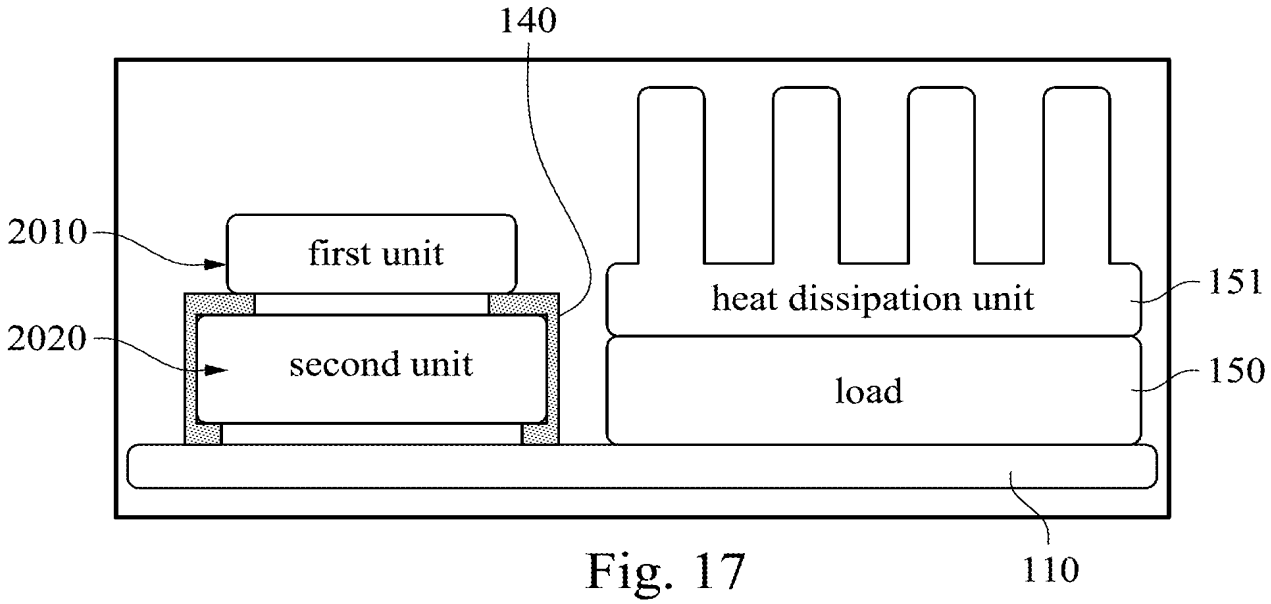


Fig. 17

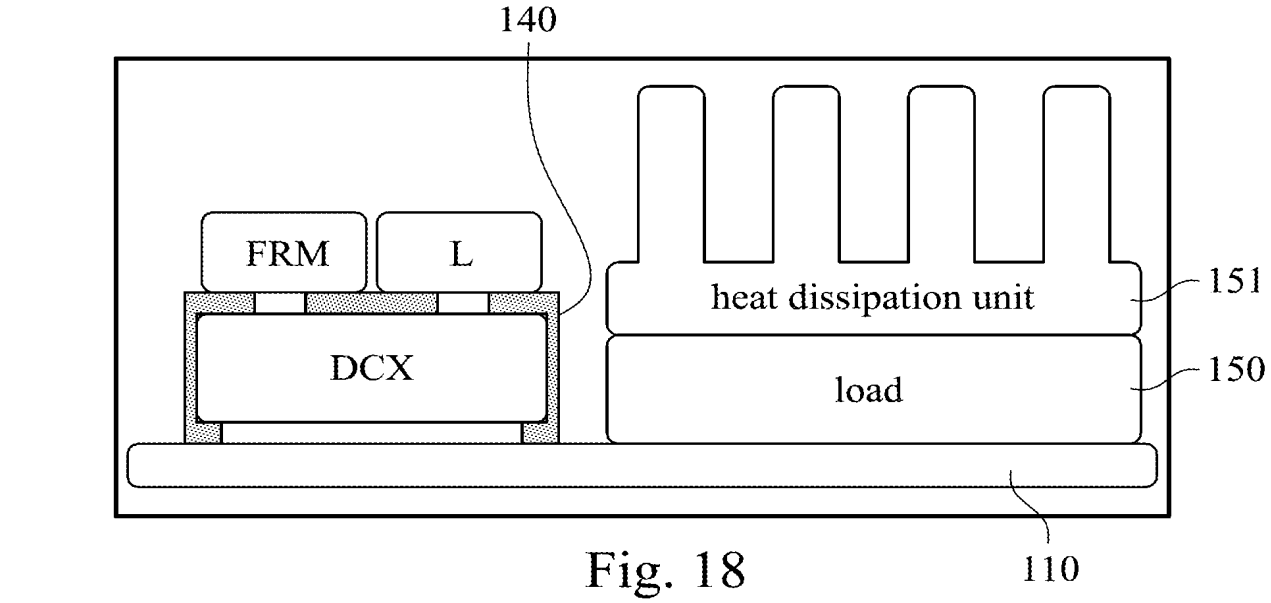


Fig. 18

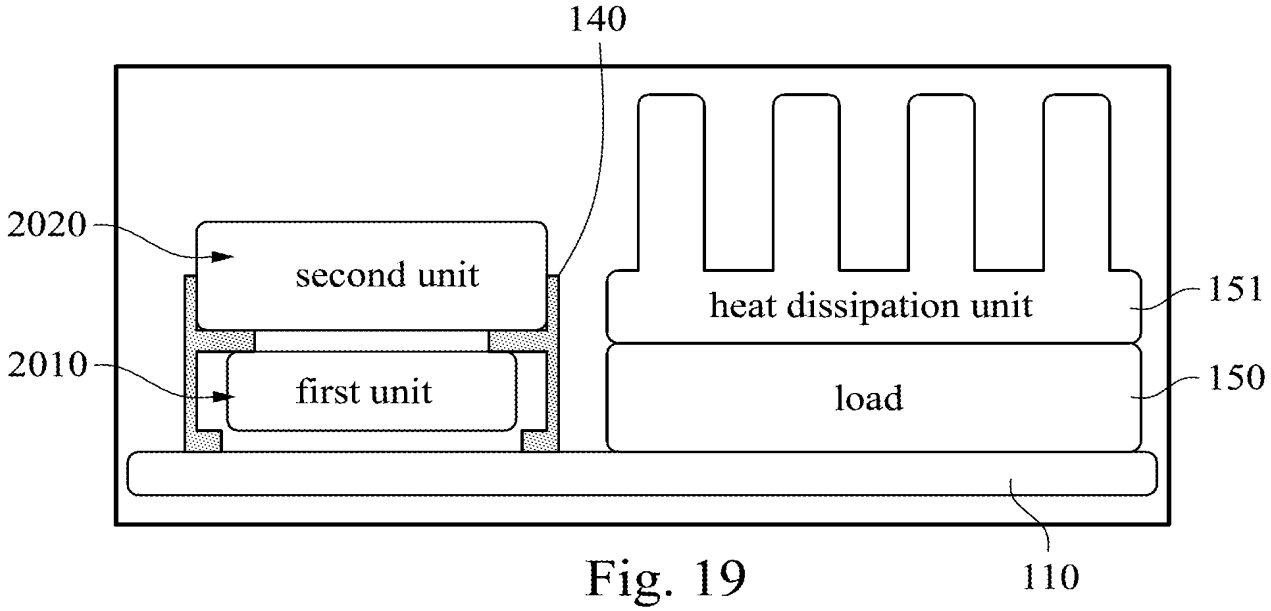


Fig. 19

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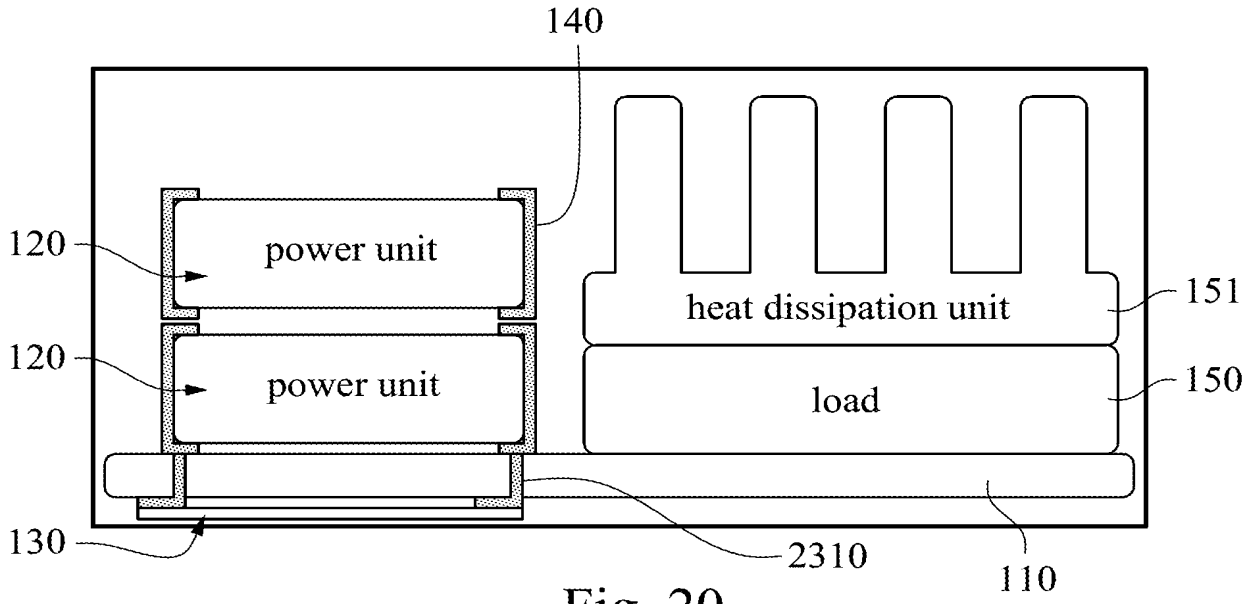


Fig. 20

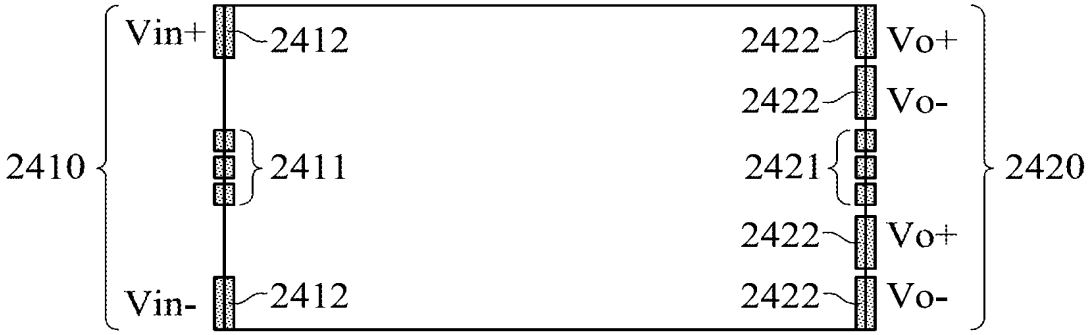


Fig. 21

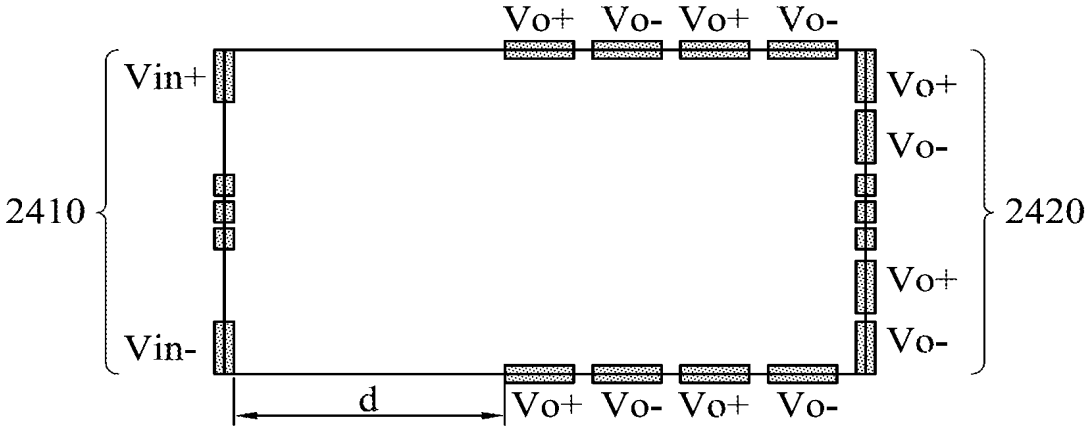


Fig. 22

IPR2024-00715 EX. 2005

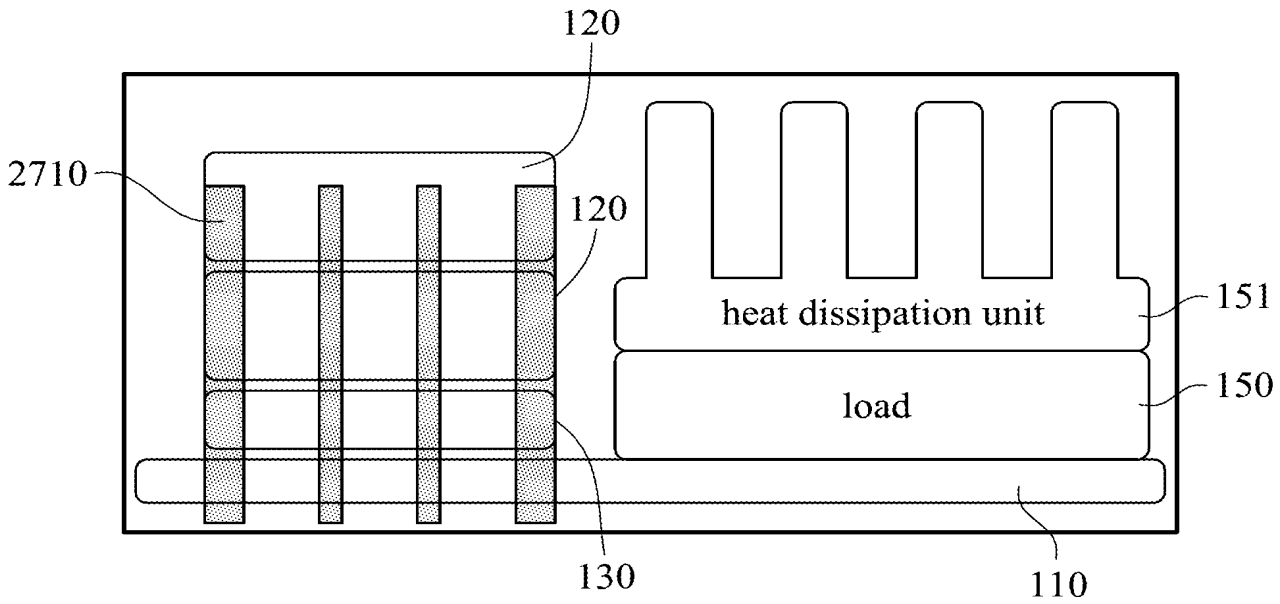


Fig. 23

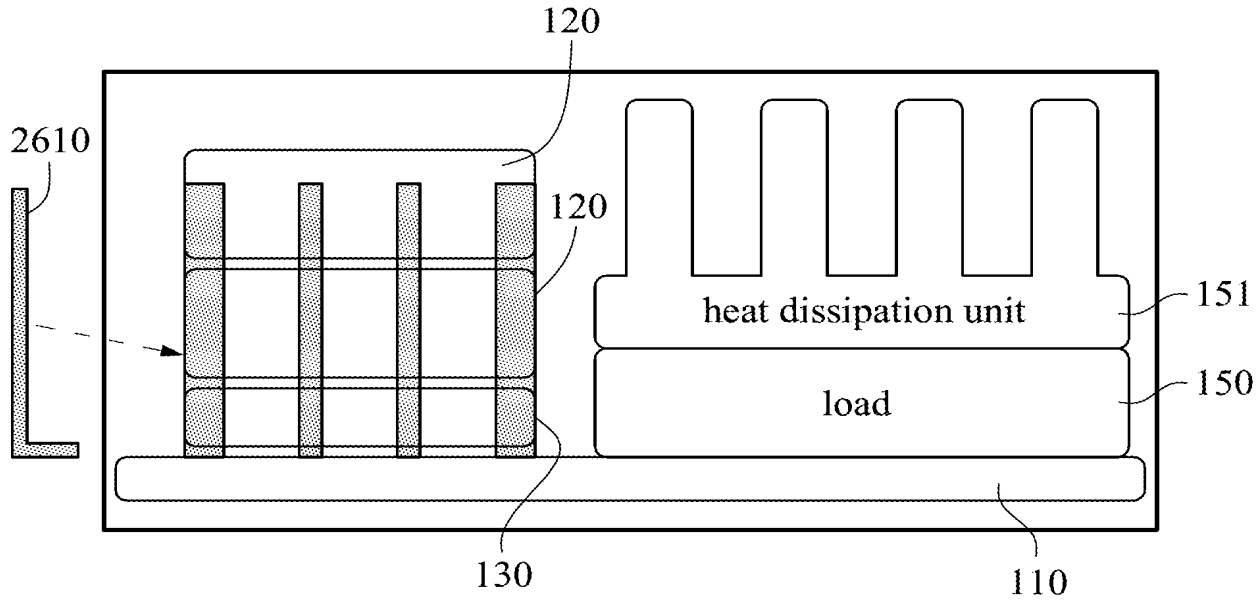


Fig. 24

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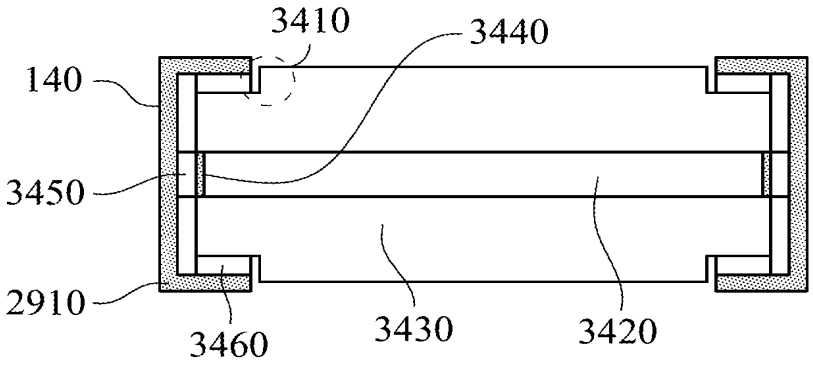


Fig. 25

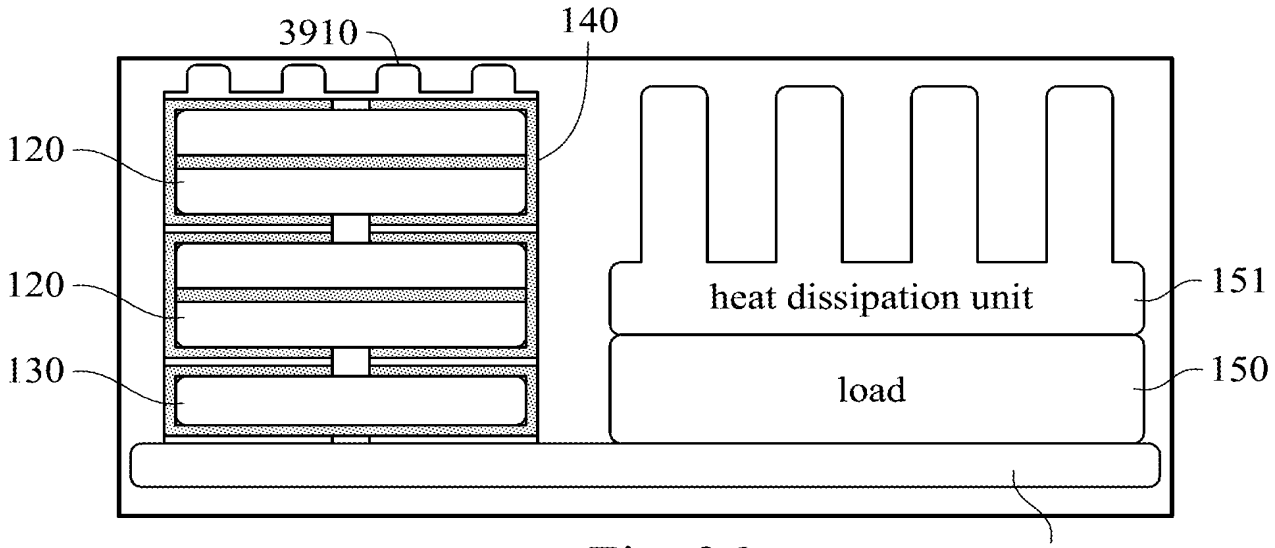


Fig. 26

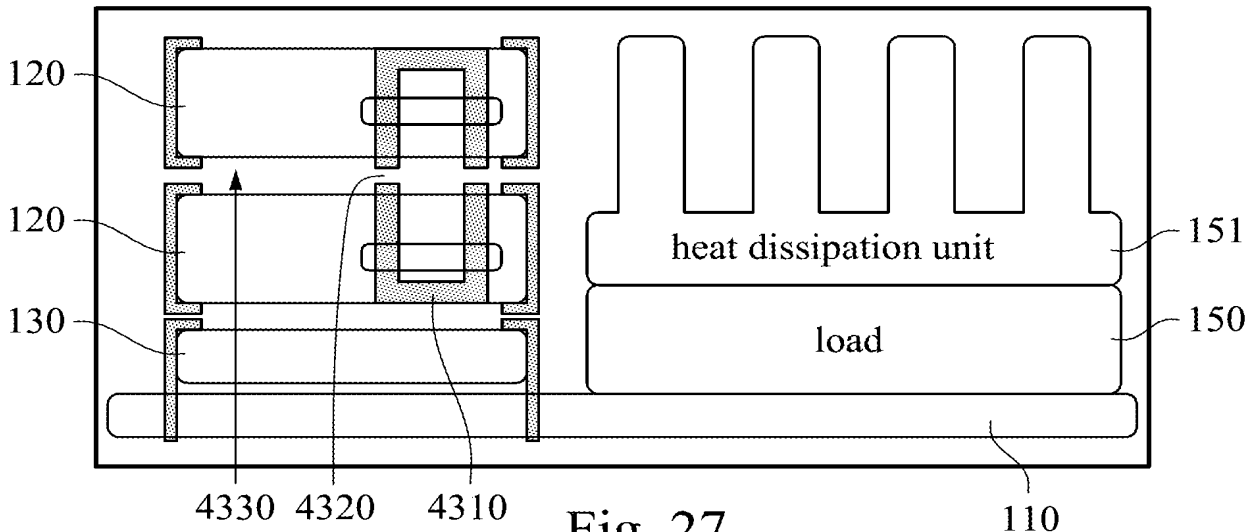


Fig. 27

IPR2024-00715 EX. 2005

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	POWER SUPPLY APPARATUS
First Named Inventor/Applicant Name:	Jian-Hong ZENG
Filer:	James Lynn O'Sullivan/Anny TENG
Attorney Docket Number:	TWT04064/US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1600**

Electronic Acknowledgement Receipt

EFS ID:	23350969
Application Number:	14840063
International Application Number:	
Confirmation Number:	8903
Title of Invention:	POWER SUPPLY APPARATUS
First Named Inventor/Applicant Name:	Jian-Hong ZENG
Customer Number:	60589
Filer:	James Lynn O'Sullivan
Filer Authorized By:	
Attorney Docket Number:	TWT04064/US
Receipt Date:	31-AUG-2015
Filing Date:	
Time Stamp:	05:10:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1600
RAM confirmation Number	8178
Deposit Account	504669
Authorized User	O'SULLIVAN, JAMES

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA-DELTA_ELECTRONICS_INC.pdf	392823 182ebf64605e375f33bdb8dfc9e67ea7ba73b18c	no	1
Warnings:					
Information:					
2	Oath or Declaration filed	TWT04064US-Declaration.pdf	1452255 2e3689ec2f6c305cc133016b83b0c6537ae270c3	no	3
Warnings:					
Information:					
3	Application Data Sheet	TWT04064US-ADS.pdf	1819020 276f595a40c64f93ac09dd252e88e6b334abbeba	no	7
Warnings:					
Information:					
4		TWT04064US-spec.pdf	7820896 9c8232355083d48e43410124fd76b81b74cc43ed	yes	51

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	45
Claims	46	50
Abstract	51	51

Warnings:					
Information:					
5	Drawings-only black and white line drawings	TWT04064US-figs.pdf	1185601 3785df59f4ba94414a960b1ca248d89218885046	no	11
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	34945 e58fdeb6f7bfb060ab21456ba2f494ac949b6fe6	no	2

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Total Files Size (in bytes):	12705540

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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	23350969
Application Number:	14840063
International Application Number:	
Confirmation Number:	8903
Title of Invention:	POWER SUPPLY APPARATUS
First Named Inventor/Applicant Name:	Jian-Hong ZENG
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Filer:	James Lynn O'Sullivan
Filer Authorized By:	
Attorney Docket Number:	TWT04064/US
Receipt Date:	31-AUG-2015
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Time Stamp:	05:10:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1600
RAM confirmation Number	8178
Deposit Account	504669
Authorized User	O'SULLIVAN, JAMES

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Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	POA-DELTA_ELECTRONICS_INC.pdf	392823 182ebf64605e375f33bdb8dfc9e67ea7ba73b18c	no	1
Warnings:					
Information:					
2	Oath or Declaration filed	TWT04064US-Declaration.pdf	1452255 2e3689ec2f6c305cc133016b83b0c6537ae270c3	no	3
Warnings:					
Information:					
3	Application Data Sheet	TWT04064US-ADS.pdf	1819020 276f595a40c64f93ac09dd252e88e6b334abbeba	no	7
Warnings:					
Information:					
4		TWT04064US-spec.pdf	7820896 9c8232355083d48e43410124fd76b81b74cc43ed	yes	51

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	45
Claims	46	50
Abstract	51	51

Warnings:					
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5	Drawings-only black and white line drawings	TWT04064US-figs.pdf	1185601 3785df59f4ba94414a960b1ca248d89218885046	no	11
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6	Fee Worksheet (SB06)	fee-info.pdf	34945 e58fdeb6f7bfb060ab21456ba2f494ac949b6fe6	no	2

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Total Files Size (in bytes):	12705540

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PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 14/840,063	Filing Date 08/31/2015	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	**280**
☒ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	**600**
☒ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	**720**
TOTAL CLAIMS (37 CFR 1.16(i))	19 minus 20 =	* 0	x $80 =	**0**
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	* 0	x $420 =	**0**
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	**1600**

APPLICATION AS AMENDED – PART II

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LDRC
/EVA GILLIS/

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