

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Hoberman et al.
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Title: POWER MANAGERS FOR AN INTEGRATED CIRCUIT

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 7,996,811 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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LIST OF EXHIBITS

- MTK-1001 U.S. Patent No. 7,996,811 to Hoberman et al. (“the ’811 patent”)
- MTK-1002 Excerpts from the Prosecution History of the ’811 patent
- MTK-1003 Declaration of Tajana Rosing, Ph.D.
- MTK-1004 “A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling” by Nowka, et al. (“Nowka”)
- MTK-1005 June Munford Declaration
- MTK-1006 U.S. Patent No. 6,484,265 to Borkar et al. (“Borkar”)
- MTK-1007 U.S. Patent No. 6,188,211 to Rincon-Mora et al. (“Rincon-Mora”)
- MTK-1008 U.S. Patent No. 6,141,762 to Nicol, et al. (“Nicol”)
- MTK-1009 Complaint for Patent Infringement Against MediaTek, Inc. in *Mosaid Technologies Inc. v. MediaTek Inc., MediaTek USA, Inc.*, Case No. 2:23-cv-00129 (E.D. Tex. March 2023)
- MTK-1010 Affidavit of Service On MediaTek USA, Inc. in *Mosaid Technologies Inc. v. MediaTek Inc., MediaTek USA, Inc.*, Case No. 2:23-cv-00129 (March 30, 2023)
- MTK-1011 Claim Construction Order in *Mosaid Technologies Inc. v. Freescale Semiconductor, Inc.*, Case No. 6:11-cv-00173 (E.D. Tex. April 29, 2013)
- MTK-1012 Claim Construction Order in *Conversant Intellectual Property Management Inc., et al. v. Xilinx, Inc.*, Case No. 6:12-cv-00847 (E.D. Tex. January 9, 2015)
- MTK-1013 Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, Katherine K. Vidal (USPTO June 21, 2022)

MTK-1014 Stipulation

MTK-1015 “Semiconductor Device Fundamentals” by Pierret (“Pierret”)

MTK-1016 “Variable Supply-Voltage Scheme for Low-Power High-Speed CMOS Digital Design” by Kuroda et al. (“Kuroda”)

MTK-1017 “Dynamic Power Management: Design Techniques and CAD Tools” by Benini & De Micheli (“Dynamic Power Management”)

MTK-1018 “A Survey of Design Techniques for System-Level Dynamic Power Management” by Benini, et al. (“Benini Survey”)

MTK-1019 “Managing Power and Performance for System-on-Chip Designs using Voltage Islands” by Lackey, et al. (“Lackey”)

MTK-1020 “Policy Optimization for Dynamic Power Management” by Benini et al., (“Benini Policy Optimization”)

MTK-1021 “Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling” by Semeraro et al. (“Semeraro”)

MTK-1022 U.S. Patent No. 5,300,824 to Iyengar (“Iyengar”)

LISTING OF CHALLENGED CLAIMS

Claim 1	
1[p]	A system comprising:
1[a]	an integrated circuit;
1[b]	a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions adapted to be independently controlled; and
1[c]	a power manager to control the power consumptions;
1[d]	at least one of the power islands adapted to have the power manager control its associated power consumption by a) the at least one of the power islands being configured to have one of plural threshold voltages of variable threshold transistors selected, and b) the system being configured to perform, during operation, an action on the at least one of the power islands, the action including changing a frequency of operation or changing a supply voltage.
Claim 2	
2	The system as claimed in claim 1 wherein the power manager comprises a programmable processor.
Claim 3	
3	The system as claimed in claim 1 wherein the integrated circuit is configured to perform, during operation, both changing the frequency of operation and changing the supply voltage.
Claim 4	
4	The system as claimed in claim 1 wherein the system is configured to have the supply voltage provided by an external regulator.
Claim 5	
5	The system as claimed in claim 4 wherein the external regulator is configured to be controlled by the power manager.
Claim 6	
6	The system as claimed in claim 1 further comprising an internal regulator to provide the supply voltage.

Claim 7	
7	The system as claimed in claim 6 wherein the internal regulator is configured to be controlled by the power manager.
Claim 8	
8	The system as claimed in claim 1 wherein the at least one of the power islands is configured to have the one of plural threshold voltages selected during operation of the integrated circuit.
Claim 9	
9	The system as claimed in claim 1 wherein the integrated circuit is configured to have the supply voltage changed by regulation of a voltage provided to the at least one of the power islands from a source external to the integrated circuit.
Claim 10	
10	The system as claimed in claim 9 further comprising an internal regulator to perform the regulation.
Claim 11	
11	The system as claimed in claim 9 wherein the regulation is performed by an external regulator.
Claim 12	
12	The system as claimed in claim 1 further comprising a dropout voltage regulator to provide the supply voltage.
Claim 13	
13	The system as claimed in claim 1 wherein the integrated circuit is configured to have the supply voltage controlled by Vdd multiplexing in relation to the at least one of the power islands.
Claim 14	
14	The system as claimed in claim 1 wherein the integrated circuit is configured to have the one of plural threshold voltage selected by back biasing.
Claim 15	
15	The system as claimed in claim 1 wherein the integrated circuit comprises the power manager and the plurality of power islands.

Claim 16	
16	The system as claimed in claim 1 wherein the power manager is configured to monitor one or more of the associated power consumptions using temperature or power dissipation measurement.
Claim 17	
17[p]	A system comprising:
17[a]	an integrated circuit;
17[b]	a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions adapted to be independently controlled;
17[c]	a power manager to control the power consumptions; and
17[d]	an internal regulator, the system being configured to have a supply voltage provided by the internal regulator, and
17[e]	at least one of the power islands adapted to have the power manager control its associated power consumption in that the system is configured to have: a supply voltage to the at least one of the power islands changed, and a frequency of operation of the at least one of the power islands changed.
Claim 18	
18	The system as claimed in claim 17 wherein the power manager comprises a programmable processor.
Claim 19	
19	The system as claimed in claim 17 wherein the system is configured to permit a clock to be stopped during operation of the integrated circuit so that the power manager can control the associated power consumption of the at least one of the power islands.
Claim 20	
20	The system as claimed in claim 17 wherein the system is configured to have the supply voltage controlled by Vdd multiplexing in relation to the at least one of the power islands.

Claim 21	
21	The system as claimed in claim 17 wherein the system is configured to have a clock stopped by clock gating.
Claim 22	
22	The system as claimed in claim 17 wherein the integrated circuit comprises the power manager and the plurality of power islands.
Claim 23	
23	The system as claimed in claim 17 wherein the power manager is configured to monitor one or more of the associated power consumptions using temperature or power dissipation measurement.
Claim 24	
24[p]	The integrated circuit as claimed in claim 23 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.
24[a]	employing a power manager processor within an integrated circuit to control power consumptions of a plurality of power islands of the integrated circuit, each having an associated power consumption, each of the power consumptions being independently controlled; and
24[b]	controlling the power consumption of at least one of the power islands by: a) selecting a threshold voltage of variable threshold transistors, and b) changing during operation at least one of the following: i) a frequency of operation, and ii) a supply voltage.
Claim 25	
25	The processor implemented method as claimed in claim 24 wherein the threshold voltage of variable threshold transistors is selected during operation of the integrated circuit.
Claim 26	
26	The processor implemented method as claimed in claim 24 wherein the supply voltage is changed, and the changing of the supply voltage includes regulating a voltage provided to the at least one of the power islands from a source external to the integrated circuit.

Claim 27	
27	The processor implemented method as claimed in claim 24 wherein the supply voltage is changed, and the changing of the supply voltage includes Vdd multiplexing in relation to the at least one of the power islands.
Claim 28	
28	The processor implemented method as claimed in claim 24 wherein the selecting the threshold voltage includes back biasing.
Claim 29	
29	The processor implemented method as claimed in claim 24 wherein the power manager monitors one or more of the power consumptions using temperature or power dissipation measurement.
Claim 30	
30[p]	A system comprising:
30[a]	An integrated circuit;
30[b]	a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions adapted to be independently controlled, and a first of the power islands being configured to communicate synchronously and asynchronously with a second of the power islands; and
30[c]	a power manager to control the power consumptions, and
30[d]	at least one of the power islands adapted to have the power manager control its associated power consumption in that the system is configured to have: a supply voltage to the at least one of the power islands changed, and a frequency of operation of the at least one of the power islands changed.
Claim 31	
31	The system as claimed in claim 30 wherein the power manager comprises a programmable processor.
Claim 32	
32	The system as claimed in claim 30 wherein the system is configured to permit a clock to be stopped during operation of the integrated circuit

	so that the power manager can control the associated power consumption of the at least one of the power islands.
Claim 33	
33	The system as claimed in claim 30 wherein the integrated circuit is configured to have the supply voltage changed by regulation of a voltage provided to the at least one of the power islands from a source external to the integrated circuit.
Claim 34	
34	The system as claimed in claim 33 further comprising an internal regulator to perform the regulation.
Claim 35	
35	The system as claimed in claim 33 wherein the regulation is performed by an external regulator.
Claim 36	
36	The system as claimed in claim 33 further comprising a dropout voltage regulator to perform the regulation.
Claim 37	
37	The system as claimed in claim 30 wherein the system is configured to have the supply voltage controlled by Vdd multiplexing in relation to the at least one of the power islands.
Claim 38	
38	The system as claimed in claim 30 wherein the system is configured to have a clock stopped by clock gating.
Claim 39	
39	The system as claimed in claim 30 wherein the system is configured to have the supply voltage changed by an external regulator.
Claim 40	
40	The system as claimed in claim 39 wherein the external regulator is configured to be controlled by the power manager.
Claim 41	
41	The system as claimed in claim 30 further comprising an internal regulator to change the supply voltage.

Claim 42	
42	The system as claimed in claim 41 wherein the internal regulator is configured to be controlled by the power manager.
Claim 43	
43	The system as claimed in claim 30 wherein the integrated circuit comprises the power manager and the plurality of power islands.
Claim 44	
44	The system as claimed in claim 30 wherein the power manager is configured to monitor one or more of the associated power consumptions using temperature or power dissipation measurement.
Claim 45	
45[p]	A system comprising:
45[a]	an integrated circuit;
45[b]	a plurality of power islands of the integrated circuit; and
45[c]	a power manager to control power consumptions of the power islands, each of the power consumptions being independently controllable, and
45[d]	at least one of the power islands capable of having the power manager control a power consumption of the at least one of the power islands by a) the at least one of the power islands selecting one of plural threshold voltages of variable threshold transistors, and b) the system performing, during operation, an action on the at least one of the power islands, the action including changing a frequency of operation or changing a supply voltage.
Claim 46	
46	The system as claimed in claim 45 wherein the power manager comprises a programmable processor.
Claim 47	
47	The system as claimed in claim 45 wherein changing the frequency of operation and changing the supply voltage are performed during operation.

Claim 48	
48	The system as claimed in claim 45 wherein the system is capable of having the supply voltage changed by an external regulator.
Claim 49	
49	The system as claimed in claim 48 wherein the external regulator is controllable by the power manager.
Claim 50	
50	The system as claimed in claim 45 further comprising an internal regulator to change the supply voltage.
Claim 51	
51	The system as claimed in claim 50 wherein the internal regulator is controllable by the power manager.
Claim 52	
52	The system as claimed in claim 45 wherein the at least one of the power islands selects the one of plural threshold voltages during operation of the system.
Claim 53	
53	The system as claimed in claim 45 wherein the supply voltage is changeable by regulation of a voltage provided to the at least one of the power islands from a source external to the system.
Claim 54	
54	The system as claimed in claim 53 further comprising an internal regulator to perform the regulation.
Claim 55	
55	The system as claimed in claim 53 wherein the regulation is performed by an external regulator.
Claim 56	
56	The system as claimed in claim 53 further comprising a dropout voltage regulator to perform the regulation.
Claim 57	
57	The system as claimed in claim 53 further comprising a dropout voltage regulator to perform the regulation.

Claim 58	
58	The system as claimed in claim 45 wherein the one of plural threshold voltages is selectable by back biasing.
Claim 59	
59	The system as claimed in claim 45 wherein the integrated circuit comprises the power manager and the plurality of power islands.
Claim 60	
60	The system as claimed in claim 45 wherein the power manager is configured to monitor one or more of the power consumptions using temperature or power dissipation measurement.
Claim 61	
61[p]	A system comprising:
61[a]	an integrated circuit;
61[b]	a plurality of power islands of the integrated circuit, a first of the power islands capable of communicating synchronously and asynchronously with a second of the power islands; and
61[c]	a power manager to control power consumptions of the power islands, each of the power consumptions being independently controllable, and in order that a power consumption of at least one of the power islands is capable of being controlled by the power manager, the system is capable of having: a supply voltage to the at least one of the power islands changed, and a frequency of operation of the at least one of the power islands changed.
Claim 62	
62	The system as claimed in claim 61 wherein the power manager comprises a programmable processor.
Claim 63	
63	The system as claimed in claim 61 wherein the supply voltage is changeable by regulation of a voltage provided to the at least one of the power islands from a source external to the system.

Claim 64	
64	The system as claimed in claim 63 further comprising an internal regulator to perform the regulation.
Claim 65	
65	The system as claimed in claim 63 wherein the regulation is performed by an external regulator.
Claim 66	
66	The system as claimed in claim 63 further comprising a dropout voltage regulator to perform the regulation.
Claim 67	
67	The system as claimed in claim 61 wherein the supply voltage is controllable by Vdd multiplexing.
Claim 68	
68	The system as claimed in claim 61 wherein a clock is capable of being stopped by clock gating.
Claim 69	
69	The system as claimed in claim 61 wherein the system is capable of having the supply voltage changed by an external regulator.
Claim 70	
70	The system as claimed in claim 69 wherein the external regulator is controllable by the power manager.
Claim 71	
71	The system as claimed in claim 61 further comprising an internal regulator to perform regulation of the supply voltage.
Claim 72	
72	The system as claimed in claim 71 wherein the internal regulator is controllable by the power manager.
Claim 73	
73	The system as claimed in claim 61 wherein the integrated circuit comprises the power manager and the plurality of power islands.

Claim 74	
74	The system as claimed in claim 61 wherein the power manager is configured to monitor one or more of the power consumptions using temperature or power dissipation measurement.

MediaTek, Inc. (“Petitioner”) petitions for *Inter Partes* Review (“IPR”) of claims 1-74 (“Challenged Claims”) of U.S. Patent No. 7,996,811 (“the ’811 patent”).

I. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the ’811 patent is available for IPR. Petitioner is not barred or estopped from requesting this review of the Challenged Claims. The present Petition is filed within one year of service of a complaint against Petitioner in *Mosaid Technologies Inc. v. MediaTek Inc., MediaTek USA, Inc.*, Case No. 2:23-cv-00129 (E.D. Tex. March 2023). MTK-1010.

B. Challenge and Relief Requested

Petitioner requests IPR and cancellation of the Challenged Claims on the grounds below. Dr. Tajana Rosing provides complementary explanations in her Declaration (MTK-1003) cited throughout this petition.

Ground	Claims	Basis	References
1A	1-11, 14-19, 21-26, 28-35, 38-55, 58-65, 68-74	§103	Nowka and Borkar
1B	12, 36, 56, 66	§103	Nowka, Borkar and Rincon-Mora
1C	13, 20, 27, 37, 57, 67	§103	Nowka, Borkar and Iyengar
2A	1-11, 14-19, 21-26, 28-35, 38-55, 58-65, 68-74	§103	Nicol and Borkar

Ground	Claims	Basis	References
2B	12, 36, 56, 66	§103	Nicol, Borkar and Rincon-Mora
2C	13, 20, 27, 37, 57, 67	§103	Nicol, Borkar and Iyengar

Each reference pre-dates the '811 patent's earliest possible priority date (May 7, 2003; "Critical Date") and qualifies as prior art.¹

Reference	Date	Prior Art Under
Nowka	11/2002 (published)	§102(a)
Nicol	10/31/2000 (published)	§102(b)
Borkar	11/2002 (published)	§102(a)/(e)
Rincon-Mora	2/13/2001 (published)	§102(b)
Iyengar	4/5/1994 (published)	§102(b)

II. THE '811 PATENT

A. Brief Description

The '811 patent relates to managing power on an integrated circuit ("IC") using power islands. MTK-1001, Abstract, 1:25-27; MTK-1003, ¶35. The '811 patent explains that reducing power consumption in integrated circuits is a known design goal that is increasing in importance as ICs become more complex and power consuming. MTK-1001, 1:29-36, 2:11-20. One alleged problem in the existing art, according to the '811 patent, is "that power consumption is not

¹ Petitioner does not concede that the '811 patent is entitled to the Critical Date.

efficiently utilized.” MTK-1001, 2:1-2. “For example, the entire integrated circuit may operate at a maximum frequency just to support an application needing that maximum frequency, while other portions of the integrated circuit can operate at a lower frequency.” MTK-1001, 2:2-6.

The ’811 Patent explains that while “[s]ome prior integrated circuits have employed voltage islands or multiple clocks to lower power consumption,” “the voltages in the power island and the frequencies of the multiple clocks are static;” “[t]he voltages and frequencies do not dynamically change based on the needs and operation of the integrated circuit.” MTK-1001, 2:21-27.

The ’811 patent proposes a method and apparatus for managing the power consumption of an integrated circuit (“IC”) using power islands whose power consumption is independently controlled. MTK-1001, Abstract, 2:31-34; MTK-1003, ¶37. A power island is “any section, delineation, partition, or division of the integrated circuit 110 where power consumption is controlled within the section, delineation, partition, or division.” MTK-1001, 3:59-62.

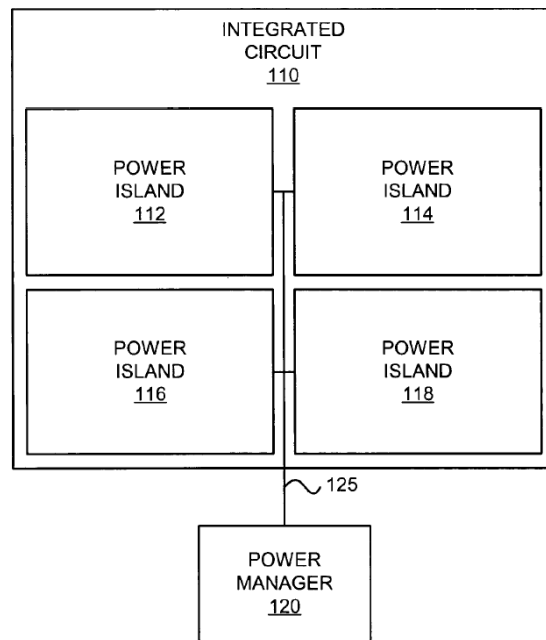


FIG. 1
MTK-1001, Fig. 1.

The system has a “power manager” that determines a target power level for one of the power islands and then determines an action to change the power consumption for one of the islands to the target power level. MTK-1001, Abstract, 2:32-39. The action to change the power consumption can be selecting a clock frequency or modifying a voltage for one of the power islands. MTK-1001, 4:53-60.

B. Summary of the Prosecution History

U.S. Application 12/332,529, which resulted in the '811 patent, was filed December 11, 2008. The '811 patent claims priority to provisional application 60/468,742, filed May 7, 2003. MTK-1001, 1. The Patent Office issued one non-final rejection during prosecution on ineligibility and nonstatutory double patenting

grounds. MTK-1002, 235-238. The Office never issued a rejection based on prior art grounds. While Nowka and Nicol appear on the face of the '811 Patent, they were never the subject of a substantive rejection. Nowka, Nicol, Burd, Borkar, Rincon-Mora, and Iyengar render the challenged claims obvious, as discussed below.

C. Level of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSITA”) would have had at least a bachelor of science degree in electrical engineering, computer engineering, computer science, or a related field, and at least two years of experience in the research, design, development, or testing of electronic circuits or components, or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa. MTK-1003, ¶21.

D. Claim Construction

Claim terms generally should be given their ordinary and customary meaning according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. For purposes of this proceeding only, Petitioner submits that no claim terms require a formal construction for purposes of addressing the Grounds in this Petition. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011). Petitioner notes for the Board that there have been prior litigations involving the '811 Patent, two of which had a claim

construction order before voluntary dismissal, attached as MTK-1011 and MTK-1012. Petitioner submits that the Board does not need to address any of the prior constructions to resolve the patentability disputes before the PTAB, and that none of the constructions impact the invalidity analysis in this Petition.

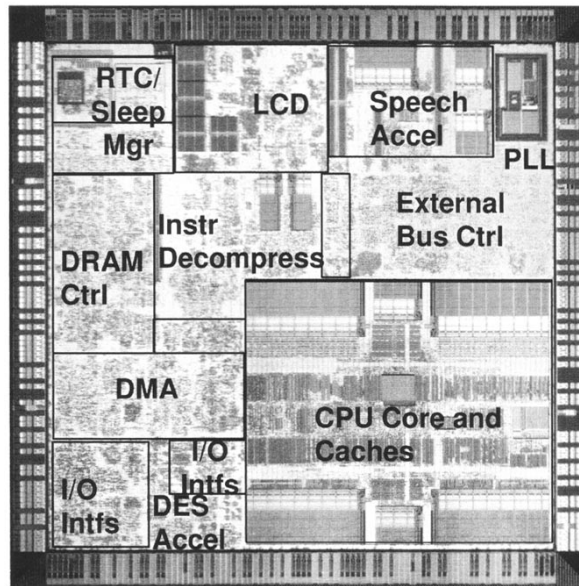
Petitioner reserves the right to respond to any constructions offered/adopted by Patent Owner/Board. Furthermore, Petitioner does not concede that each challenged claim satisfies all statutory requirements and does not waive any arguments concerning grounds that can only be raised in district court.

III. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1A—Claims 1-11, 14-19, 21-26, 28-35, 38-55, 58-65, 68-74 are obvious over Nowka and Borkar

1. Overview of Nowka

Nowka is titled “A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling.” MTK-1004, Title. Nowka describes a PowerPC system-on-a-chip (“SOC”) processor that “makes use of dynamic voltage and frequency scaling to adapt to the dynamically changing performance demands and power consumption constraints of high-content, battery powered applications.” MTK-1004, Abstract; MTK-1003, ¶44. Nowka’s SOC consists of a high performance 32-bit processor core, also referred to as the “CPU core,” which is fully compliant with the PowerPC specification. MTK-1004, 1441. Figure 2 below shows the physical layout of the SOC.

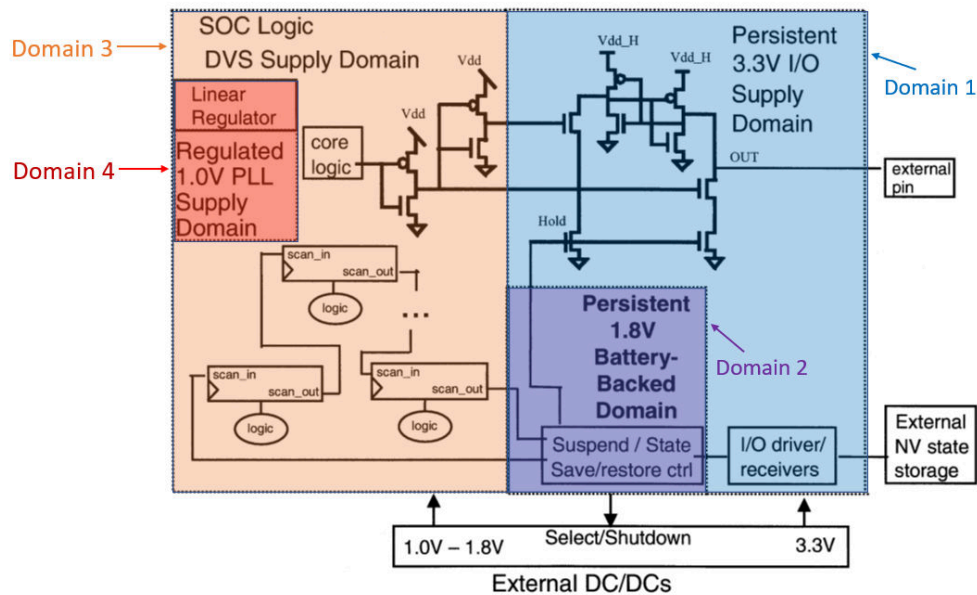


MTK-1004, Fig. 2.

Nowka explains that during “active computation,” the SOC’s “required performance tends to vary widely and quickly as a function of the workload” and that while peak performance demands high power consumption, periods of inactivity allow for minimization of power consumption. MTK-1004, 1441. To “match the performance and power consumption of this device to the application,” Nowka uses dynamic voltage scaling (DVS). According to Nowka, “DVS systems adjust the supply voltage dynamically to meet the performance demands while minimizing power consumption.” MTK-1004, 1442, 1444. Nowka also implements dynamic frequency scaling, clock gating, and standby modes to dynamically adjust power consumption. MTK-1004, Sections V, VI, VII.

Nowka’s SOC “is divided into four distinct domains” to enable dynamic

voltage and frequency scaling. These domains—two persistent voltage domains, one dynamically voltage-scaled and frequency-scaled logic domain, and one internally derived domain—are shown in Figure 3. MTK-1004, 1442. The I/O drivers and receivers are in the persistent 3.3V domain (domain 1 below); the real-time clock and the logic controlling the voltage of the cores is in the persistent 1.8V domain (domain 2 below); the logic supply for the processor core, caches, SOC cores and accelerators in the 1-1.8V domain (domain 3 below); and the PLL is in the constant 1V domain (domain 4 below). The operating frequency of the variable voltage domain (domain 3) can also be altered for additional active power reduction. MTK-1004, 1444. (“When the performance demands of the application decrease, the system software can lower the operating frequency.”)



MTK-1004, Fig. 3²

During operation, the logic supply is controlled by an “on-chip supervisor” that, under software control, “requests changes to the logic supply and requests shutdown of the logic supply during hibernation.” MTK-1004, 1442. The supply voltage to the logic can change between 1V and 1.8V and the frequency can be varied to reduce power consumption. Nowka states that the “ability to change the output clock divider on-the-fly, without pausing the processor, allows the SOC to operate over an extremely broad range of frequencies. This allows the power consumption to be determined by the system on a very fine time scale.” MTK-1004, 1446. Nowka’s SOC also uses clock gating and standby modes to reduce power consumption by the logic elements. MTK-1004, 1445-46.

2. Overview of Borkar

Borkar is titled “Software control of transistor body bias in controlling chip parameters.” MTK-1006, Title. Borkar relates to controlling various circuit parameters, such as performance, power consumption, and temperature in integrated circuits. MTK-1006, 2:2-3. Borkar discusses controlling these parameters by changing the clock frequency, supply voltage, and threshold voltage (via body bias signals). MTK-1006, 2:49-54, Figs. 1-3, 5, 7, 9; MTK-1003, ¶49.

² All annotations to the figures have been added unless otherwise noted herein.

Borkar discloses some embodiments that are a single-processor system (Figs. 1-4) and some embodiments with multiple “domains” (Figs. 5, 7). MTK-1003, ¶50.

Borkar’s “domains” shown in Figures 5 and 7, also called “functional unit blocks,” are groups of transistors, which can be controlled independently of each other.

MTK-1006, 9:48-59, 10:34-36; MTK-1003, ¶50.

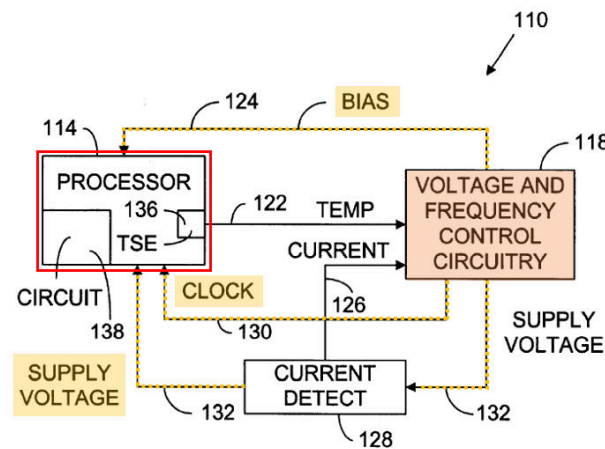


FIG. 1

MTK-1006, Fig. 1 (single-processor embodiment).

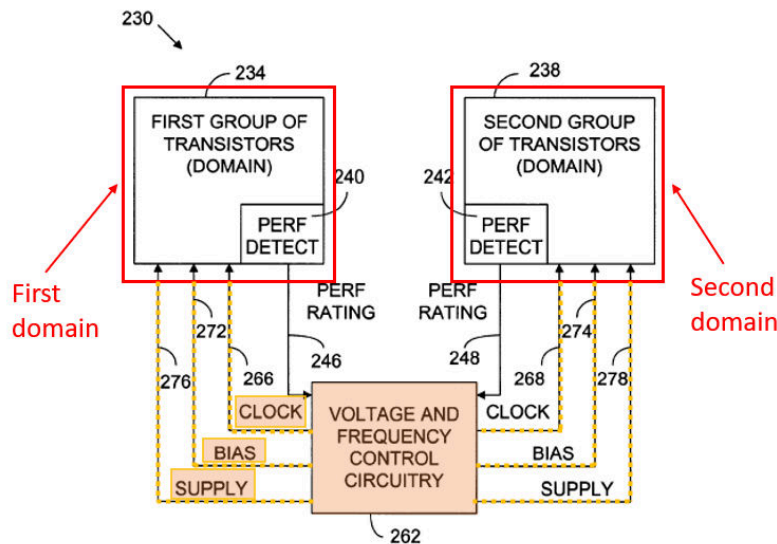


FIG. 5

MTK-1006, Fig. 5 (multiple-domain embodiment).

3. The Nowka-Borkar Combination

A POSITA would have been motivated to combine Nowka and Borkar for a number of reasons. First, Nowka and Borkar are related to the same field: power management of integrated circuits on a chip. Nowka describes a “PowerPC system-on-a-chip processor which makes use of dynamic voltage scaling and on-the-fly frequency scaling to adapt to the dynamically changing performance demands and power consumption constraints of high-content, battery powered applications.” MTK-1004, Abstract; MTK-1006, 2:49-57 (“The invention involves changing body bias signals applied to transistors in an integrated circuit in response to changing conditions to at least partially control a parameter of the integrated circuit... A parameter of the integrated circuit is a characteristic of the

integrated circuit which can vary during performance including temperature, power consumption, and performance.”); MTK-1003, ¶53.

Further, Nowka and Borkar address the same known problem, the need to balance performance with power consumption in electronic systems. MTK-1004, 1441 (“While [devices’] peak performance demands tend to be significant, they are also highly power constrained.”), MTK-1006, 1:20-21 (“The performance, power consumption, and temperature [of an integrated circuit] are typically related.”), 5:45-46 (“The user may specify certain power conditions or a power versus performance tradeoff.”); MTK-1003, ¶54. Both Nowka and Borkar teach the known solution of using distinct units on an integrated circuit whose power can be independently controlled. MTK-1004, 1442 (“To support DVS in this SOC, the power distribution has been divided into four distinct domains as shown in Fig. 3), Fig. 3; MTK-1006, 10:34-39 (“The first and second groups of transistors may be different function unit blocks (FUBS) on the same chip...”); MTK-1003, ¶55. Both Nowka and Borkar also suggest the identified, predictable solution of dynamically changing variables such as frequency and voltage according to certain needs and operation of the integrated circuit. MTK-1004, 1442 (“The primary means of matching the performance and power consumption of this device to the application is through the use of dynamic voltage scaling (DVS).”); MTK-1006, 6:48-53 (““The process of selecting the body bias, supply voltage, and/or clock settings in

control circuitry 114 and 144 may be iterative process involving feedback from signals indicative of levels of the parameters (such as temperature and current) and other signals indicating preference[.]”); MTK-1003, ¶56.

Because Nowka and Borkar provide similar solutions to a similar problem within the same field of endeavor, a POSITA would have naturally looked at, and been motivated to combine, the two references when selecting a method for Nowka’s dynamic power management mechanism. MTK-1003, ¶57. For example, Nowka does not explicitly disclose changing a threshold voltage to control the power consumption. However, Nowka explains that “[s]tatic power due to reverse-biased junction current, sub-threshold leakage, gate leakage and analog current sources can limit the operating lifetime of battery-powered systems. Decreasing the standby power of the IC increases shelf-life as well as overall energy efficiency.” MTK-1004, 1446. Thus, a POSITA would have been motivated to look to Borkar’s threshold voltage-tuning solution to alleviate static power in Nowka’s SOC. MTK-1003, ¶57.

4. Claim 1

(a) 1[p]

To the extent the preamble is limiting,³ the Nowka-Borkar combination renders obvious a system. A POSITA would have understood that Nowka discloses a system because it is a “PowerPC system-on-a-chip (SOC).” MTK-1004, 1441, MTK-1003, ¶58. The ’811 patent states that a system “includes an integrated circuit 110 and a power manager 120. The integrated circuit 110 is any electronic device that is instantiated into silicon and/or related manufacturing materials. One example of the integrated circuit 110 is a system-on-a-chip.” MTK-1001, 3:47-50. A POSITA would have also understood Borkar to disclose a system. MTK-1006, 1:59-60 (“In some embodiments, the invention includes a *system* having a processor and control circuitry.”), 2:13-36 (“FIG. 1 is a block diagram representation of a computer *system* according to some embodiments of the invention.... FIG. 5 is a block diagram representation of a *system*[.]”), 2:61-65, 4:60-64, 5:1-2. MTK-1003, ¶58.

(b) 1[a]

The Nowka-Borkar combination renders obvious an integrated circuit.

³ Petitioner reserves the right to argue in counterpart litigation that the preamble is not limiting.

Nowka discloses a “PowerPC system-on-a-chip [SOC] processor,” which is an integrated circuit. MTK-1004, Abstract; MTK-1003, ¶59. Figure 1 shows the PowerPC SOC structure.

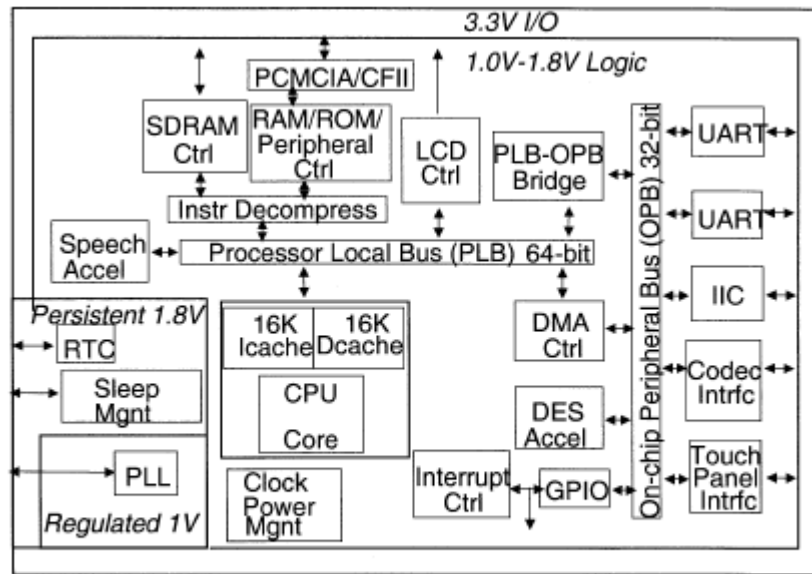


Fig. 1. PowerPC SOC structure.

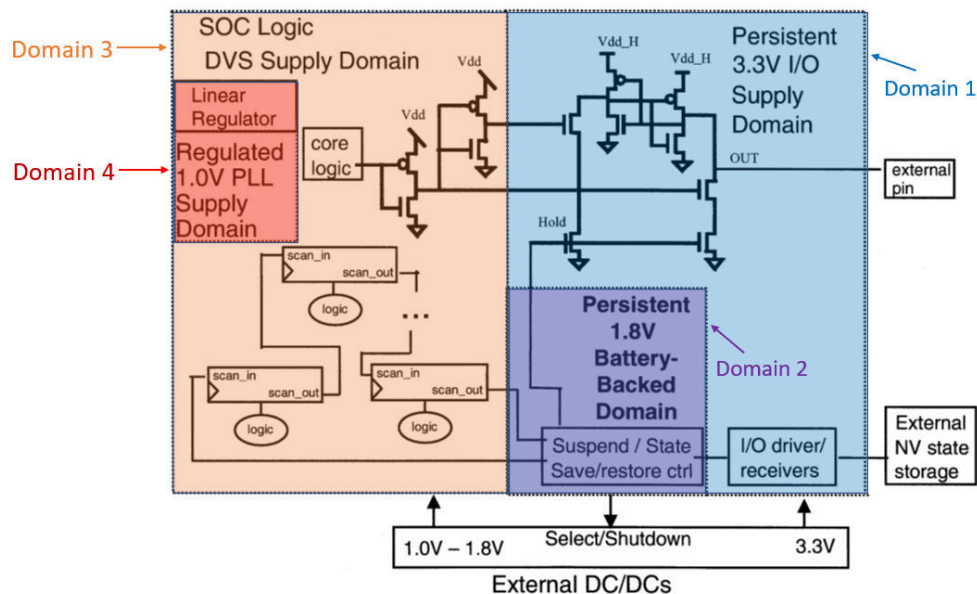
MTK-1004, Fig. 1.

Borkar also discloses an integrated circuit. MTK-1006, 2:49-60 (“The invention involves changing body bias signals applied to transistors in an *integrated circuit*...”), 4:5-9; MTK-1003, ¶60.

(c) 1[b]

The Nowka-Borkar combination renders obvious a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions adapted to be independently controlled. For example, Nowka discloses multiple power domains on the IC, namely the “four distinct domains”

supplied different voltages, depicted in Figure 3. MTK-1004, 1442. Domain 1 is powered by a persistent 3.3V supply; domain 2 is powered by a persistent, battery-backed 1.8V supply; domain 3 receives a dynamic supply varied between 1.0-1.8V which is controlled by external DC/DC converter; domain 4 is powered by an on-chip linear regulator and receives a constant 1V supply from the dynamically-varying logic supply. MTK-1004, 1442. The four domains constitute power islands on an IC because they are each a “section, delineation, partition, or division” on the SOC where “power consumption is controlled within the section, delineation, partition, or division.” MTK-1001, 3:59-62; MTK-1003, ¶62. These domains further have power consumptions adapted to be independently controlled because they receive separate voltage supplies which can be independently controlled. MTK-1004, 1442; MTK-1003, ¶63.



MTK-1004, Fig. 3.

To the extent that it is argued that Nowka does not disclose or render obvious this limitation, Borkar discloses and renders obvious this limitation. Borkar discloses multiple “domains,” or groups of transistors, which have distinct power parameters. MTK-1006, 9:19-24 (“The invention...is not restricted to single chip, but rather control circuitry 114 and peripheral [] interface [] and voltage control circuitry 178 may also be used to control the settings for more than one chip (e.g., *multiple processors*).”), 9:48-52 (“For example, a *first domain* as a whole may perform differently than a *second domain* as a whole.”), 9:58-59, 10:34-39 (“The first and second groups of transistors may be different function unit blocks (FUBS) on the same chip. Because of transistor parameter variations, certain performance and/or power parameters of the first domain 234 may be different than that of the second domain 238.”). Exemplary embodiments are shown in Figures 5 and 7. A POSITA would have understood these domains to be power islands because they are a “section, delineation, partition, or division of the integrated circuit.” MTK-1003, ¶64.

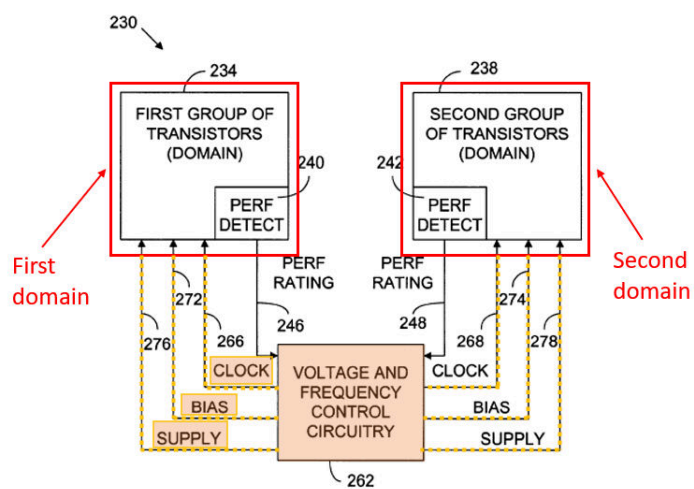


FIG. 5

MTK-1006, Fig. 5.

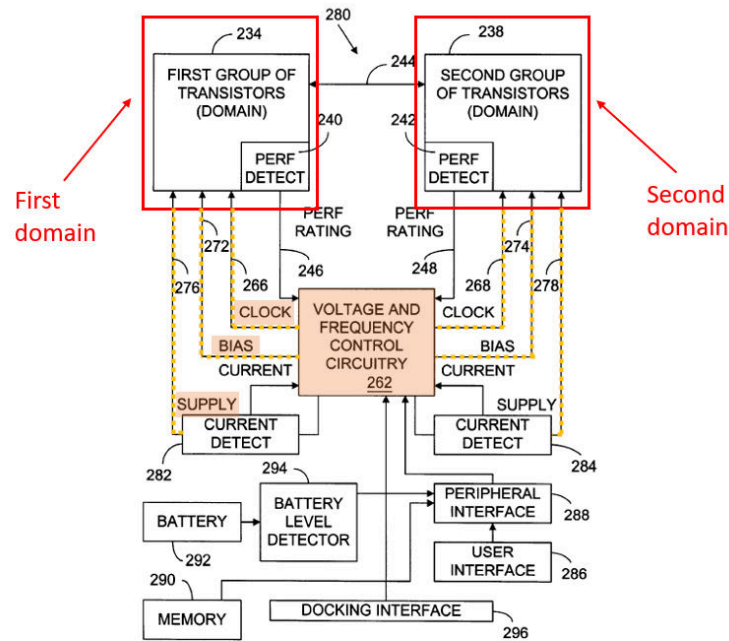


FIG. 7

MTK-1006, Fig. 7.

Borkar further discloses controlling the supply voltage, and clock frequency of each domain individually. MTK-1006, 11:25-37 (describing controlling clock frequency of domains), 11:55-64 (describing controlling supply voltage of domains), *see also* MTK-1006, 12:10-15, 13:4-6, 13:35-37 (“Control circuitry 262 can make the body bias, **supply voltage**, and **clock frequency** settings so as to keep at a temperature or temperature range.”), Figs. 5, 7. Accordingly, a POSITA would have understood and found obvious that Borkar’s domains are a plurality of power islands, each with a power consumption adapted to be independently controlled. MTK-1003, ¶65.

(d) 1[c]

The Nowka-Borkar combination renders obvious a power manager to control the power consumptions. Nowka discloses a “power manager” comprised of an “on-chip supervisor” and “system software.” MTK-1004, 1442; MTK-1003, ¶66. The “on-chip supervisor controls the external DC/DC converter, which provides the logic supply” and “requests changes to the logic supply and requests shutdown of the logic supply during hibernation.” MTK-1004, 1442. In addition, Nowka discloses that the power supervisor, “in response to software commands and timeout and interrupt events, manages the clocks, internal state and external power supply to the control the standby power,” and during freeze mode, “the supervisor software first sets a low operating frequency and then lowers the supply.” MTK-1004, 1446; MTK-1003, ¶67.

Borkar also discloses a “power manager” that controls the power consumptions: Borkar’s “control circuitry controls the setting responsive to processor signal resulting for execution of software. The control circuitry may further control settings of a supply voltage signal and a clock signal to control settings of a supply voltage signal and a clock signal to control the parameter.” MTK-1006, 1:63-2:1; *see also* MTK-1006, 2:63-3:11, 4:3-11, 4:20-33, 5:47-64, 6:12-53, 11:25-67, Figs. 1-5, 7. A POSITA would have understood Borkar’s “control circuitry” to be a power manager because it controls the power

consumption of the relevant processor(s) or domain(s). MTK-1003, ¶68.

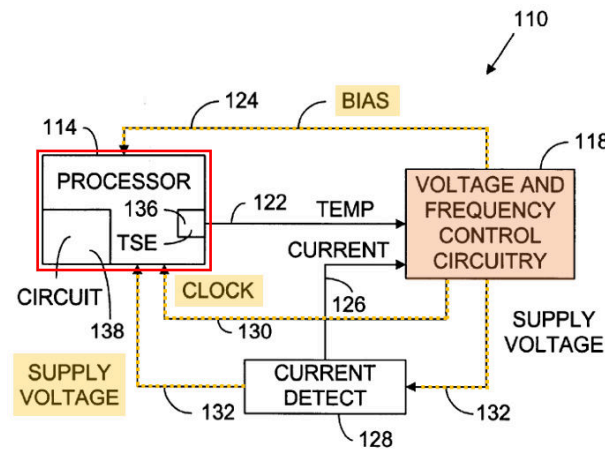


FIG. 1

MTK-1006, Fig. 1.

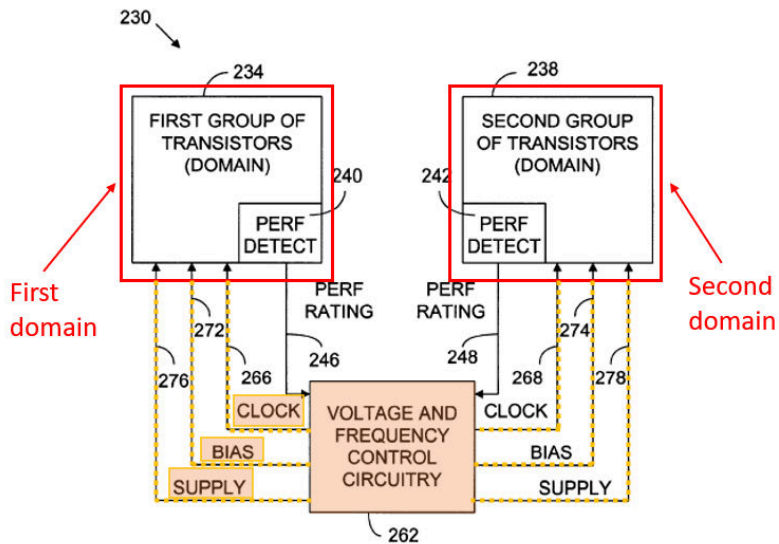


FIG. 5

MTK-1006, Fig. 5.

(e) 1[d]

The Nowka-Borkar combination renders obvious at least one of the power

islands adapted to have the power manager control its associated power consumption by a) the at least one of the power islands being configured to have one of plural threshold voltages of variable threshold transistors selected, and b) the system being configured to perform, during operation, an action on the at least one of the power islands, the action including changing a frequency of operation or changing a supply voltage. Borkar discloses controlling power consumption of a power island by selecting a threshold voltage, as well as changing a frequency of operation or supply voltage during operation. For example, “[i]n some embodiments, when the battery level signal is below a certain level, the supply voltage is lowered, the frequency of a processor clock is lowered, and/or the bias signals are changed to raise the *threshold voltages* of some or all of the transistors. This will reduce the power consumption to maintain the battery.” MTK-1006, 5:25-30; *see also* MTK-1006, 3:46-57, 4:26-28, 5:25-34, 6:15-24, 6:31-40, 12:39-42; MTK-1003, ¶70. A POSITA would have been motivated to combine Nowka and Borkar for the reasons previously explained. *Supra*, Section III.A.3.

Further, Nowka discloses the actions of changing the frequency of operation or changing the supply voltage. MTK1004, 1442 (“An on-chip supervisor controls the external DC/DC converter, which provides the logic supply. Under software control, the supervisor requests changes to the logic supply and requests shutdown of the logic supply during hibernation.”), 1444 (describing the effects on power

consumption of voltage scaling in Figures 5 and 6), 1444 (describing effects on power consumption of dynamic voltage and frequency scaling); MTK-1003, ¶¶71-72. In addition, Nowka discloses that these actions can take place during operation. MTK-1004, 1442 (“The primary means of matching the performance and power consumption of the device to the application is through the use of dynamic voltage scaling (DVS).”), 1445 (“The ability to change the output clock divider on-the-fly, *without pausing the processor*, allows the SOC to operate over an extremely broad range of frequencies. This allows the power consumption to be determined by the system on a very fine time scale.”); MTK-1003, ¶72. Further, as explained in 1[b], incorporated herein, Borkar also discloses changing frequency of operation or supply voltage of a power island during operation. MTK-1003, ¶73.

5. Claim 2

The Nowka-Borkar combination renders obvious wherein the power manager comprises a programmable processor. A POSITA would have understood and found obvious that Nowka’s “on-chip supervisor” is a programmable processor because Nowka discloses “system software,” which a POSITA would have understood to program the processor to execute power management functions. MTK-1004, 1442 (“An on-chip supervisor controls the external DC/DC converter, which provides the logic supply. Under software control, the supervisor requests changes to the logic supply and requests shutdown of the logic supply

during hibernation.”); MTK-1003, ¶74. Further, a POSITA would have understood and found obvious that the control circuitry in Borkar was a programmable processor because it can be programmed to manage power in various ways. *See, e.g.*, MTK-1006, 4:47-56, 6:1-7, 6:41-53; MTK-1003, ¶74.

6. Claim 3

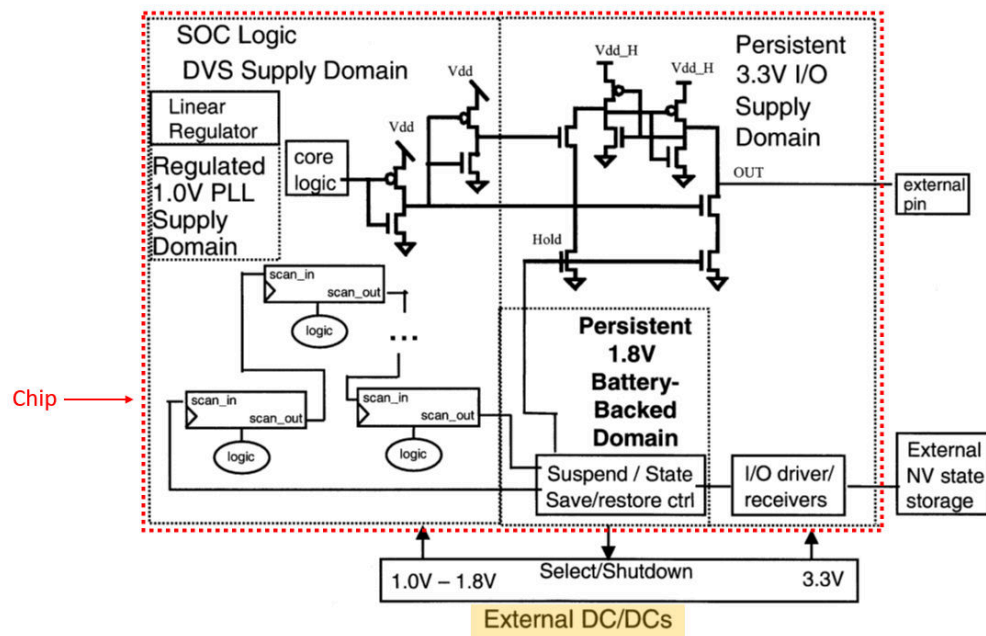
The Nowka-Borkar combination renders obvious wherein the integrated circuit is configured to perform, during operation, both changing the frequency of operation and changing the supply voltage. As discussed above for limitation 1[b] and 1[d], incorporated herein, Nowka discloses changing supply voltage and operating frequency during operation. MTK-1003, ¶75.

Borkar also discloses changing frequency and supply voltage during operation. MTK-1006, 2:52-57 (“The invention may also include changing clock frequency signals and supply voltage signals to at least partially control a parameter. A parameter of the integrated circuit is a characteristic of the integrated circuit which can vary during performance including temperature, power consumption, and performance.”), 4:21-32, 5:25-34, 10:27-29; MTK-1003, ¶76.

7. Claim 4

The Nowka-Borkar combination renders obvious wherein the system is configured to have the supply voltage provided by an external regulator. Nowka discloses an “external DC/DC converter, which provides the logic supply,” as

shown in Figure 3. MTK-1004, 1442, Fig. 3. The DC/DC converter is external to the chip, and supplies multiple voltages to the SOC, including a 1.0-1.8V variable supply depending on the needs of the circuit, and a persistent 3.3V supplied to the I/O drivers and receivers. MTK-1004, 1442; MTK-1003, ¶77. A POSITA would have understood Nowka's DC/DC converter to be an external regulator that provides the supply voltage. MTK-1003, ¶78.



MTK-1004, Figure 3.

Additionally, Borkar discloses an external regulator that provides the supply voltage. While Figure 3 depicts the “voltage control circuitry” inside of the chip, Borkar also discloses that “[v]oltage control circuitry 178 may be on the same chip (e.g., chip 186) as is processor 174 *or on a different chip.*” MTK-1006, 7:5-7. When the control circuitry is on a different chip than the processor, it would

necessarily be external to the chip that contains the processor, thus making it an external regulator. MTK-1003, ¶79.

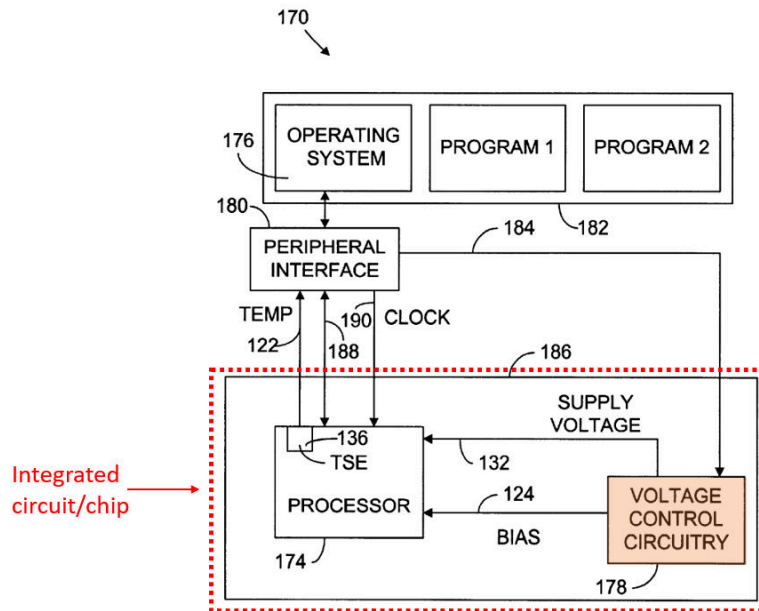


FIG. 3

MTK-1006, Fig. 3.

8. Claim 5

The Nowka-Borkar combination renders obvious wherein the external regulator is configured to be controlled by the power manager. Nowka discloses that “an on-chip supervisor controls the external DC/DC converter, which provides the logic supply.” MTK-1004, 1442. Therefore, a POSITA would have understood that the external DC/DC converter (external regulator) is configured to be controlled by the on-chip supervisor (“power manager”). MTK-1003, ¶80.

9. Claim 6

The Nowka-Borkar combination renders obvious an internal regulator to

provide the supply voltage. First, in the combination, Borkar's "voltage and frequency control circuitry" is an internal regulator that provides the supply voltage. MTK-1006, 1:66-67 ("control circuitry may further control settings of a supply voltage signal."), 11:58-60 ("the supply voltage signals may be the actual supply voltage Vcc (sometimes called Vdd) applied to the transistors."); MTK-1003, ¶81. As shown in Figure 3, voltage control circuitry 178 is internal to the integrated circuit. MTK-1006, Fig. 3, 7:5-7 ("Voltage control circuitry may be on the same chip, (e.g., chip 186) as is processor 174[.]").

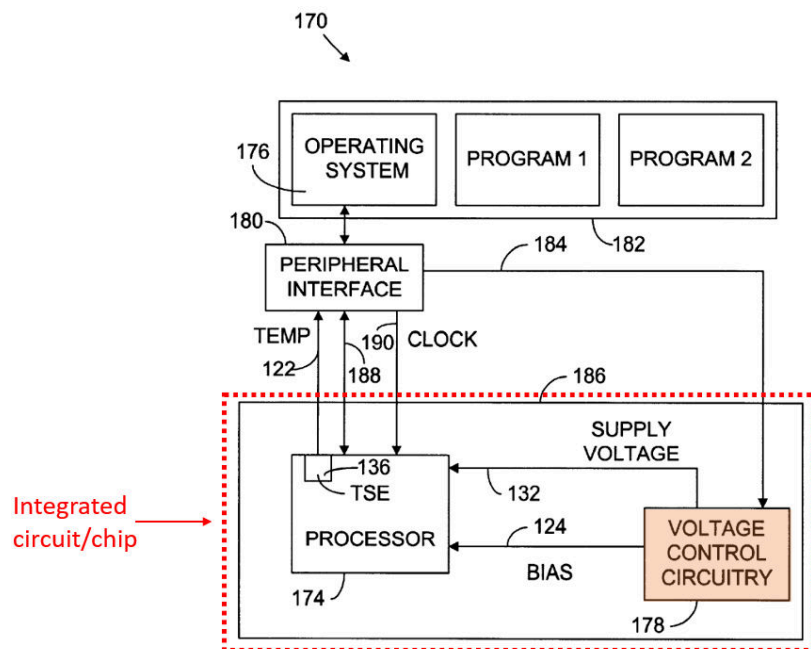


FIG. 3

MTK-1006, Fig. 3.

Borkar also discloses "supply voltage generating circuitry 320 which provides one or more supply voltage signals in response to one or more supply

voltage signals on conductor(s) 132 is included in processor 114.” MTK-1006, 13:57-60. This “supply voltage generating circuitry” is also an internal regulator (in this case, internal to the processor) that provides the supply voltage. MTK-1006, 11:58-60; MTK-1003, ¶82.

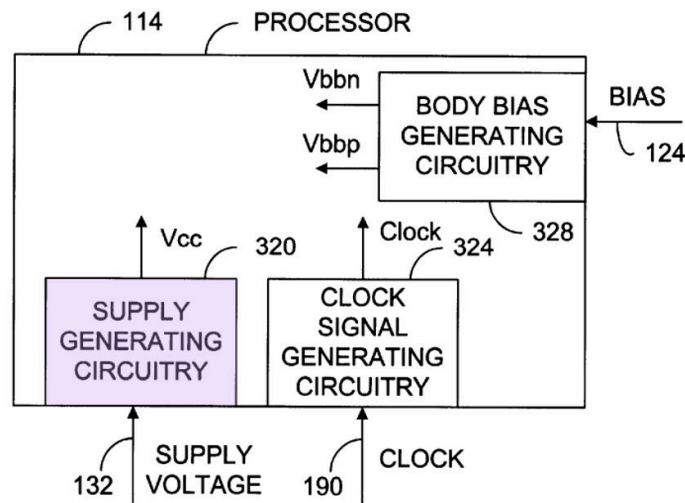


FIG. 9
MTK-1006, Fig. 9.

10. Claim 7

The Nowka-Borkar combination renders obvious wherein the internal regulator is configured to be controlled by the power manager. Borkar’s “supply generating circuitry” shown in Figure 9, which is an internal regulator as explained for claim 6, is configured to be controlled by the “control circuitry” (power manager). For example, Borkar explains that “supply voltage generating circuitry 320” “provides one or more supply voltage signals in response to one or more supply voltage signals on conductor(s) 132 is included in processor 114.” MTK-

1006, 13:57-60; *see also* MTK-1006, 11:58-60. As depicted in Figure 9, the supply generating circuitry receives “supply voltage” which comes from voltage and frequency control circuitry, and thus is controlled by the control circuitry. MTK-1006, 3:12-16, Fig. 9; MTK-1003, ¶¶83-84.

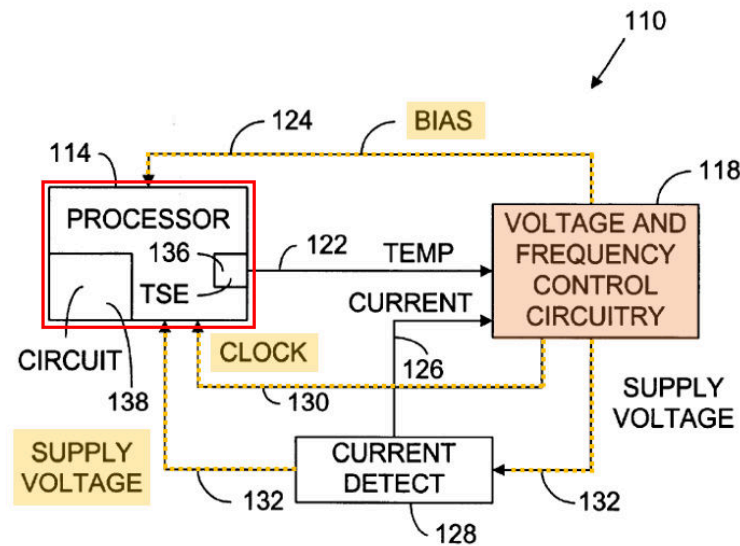


FIG. 1

MTK-1006, Fig. 1.

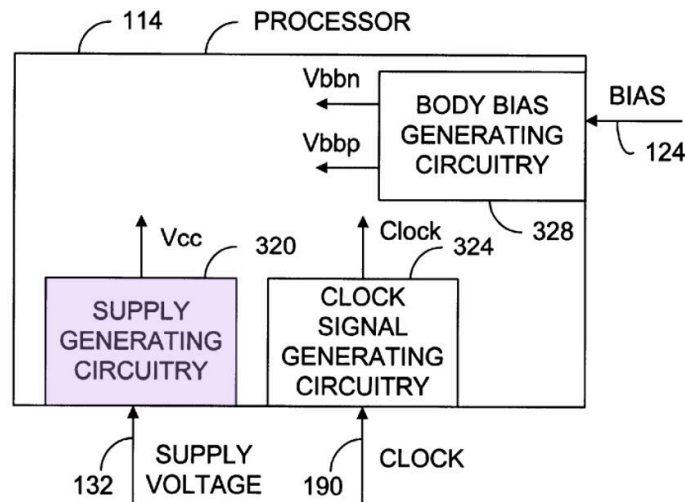


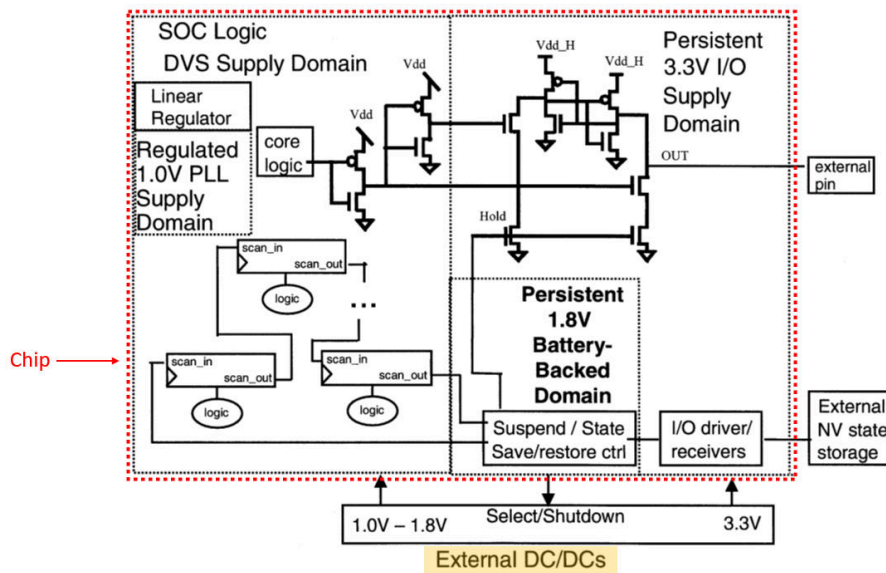
FIG. 9
MTK-1006, Fig. 9.

11. Claim 8

The Nowka-Borkar combination renders obvious wherein the at least one of the power islands is configured to have the one of plural threshold voltages selected during operation of the integrated circuit. As discussed for element 1[d], incorporated herein, Borkar discloses changing power consumption of a power island (processor or domain) by selecting a threshold voltage during operation. For example, “[i]n some embodiments, when the battery level signal is below a certain level, the supply voltage is lowered, the frequency of a processor clock is lowered, and/or the bias signals are changed to raise the threshold voltages of some or all of the transistors. This will reduce the power consumption to maintain the battery.” MTK-1006, 5:25-30; *see also* MTK-1006, 3:46-57, 4:21-32, 5:25-34, 6:15-25, 6:31-40, 12:39-42 (similar); MTK-1003, ¶¶85-86.

12. Claim 9

The Nowka-Borkar combination renders obvious wherein the integrated circuit is configured to have the supply voltage changed by regulation of a voltage provided to the at least one of the power islands from a source external to the integrated circuit. As explained for claim 4, Nowka discloses an “external DC/DC converter” which a POSITA would understand to regulate a voltage from a source external to the integrated circuit before providing the appropriate supply voltages to the power islands (power domains). MTK-1004, 1442, Fig. 3; MTK-1003, ¶87.



MTK-1004, Figure 3.

Further, Nowka discloses that the SOC was developed “to address the high-content battery-powered market segment. This segment includes information appliances such as Web pads, advanced PDAs, cell phones and small formfactor PCs.” MTK-1004, 1441. A POSITA would have understood that a battery would

constitute a “source external to the integrated circuit.” MTK-1003, ¶88.

Additionally, Borkar discloses embodiments where an external battery provides the supply voltage. “Referring to FIG. 2 ... computer system 140 includes a battery level detector 152 to detect the voltage level of a battery 156.” MTK-1006, 5:1-4, Fig. 2; *see also* MTK-1006, Figs. 4, 7, 7:36-59, 13:8-36; MTK-1003, ¶89. For example, Borkar explains that in the embodiment shown in Figure 2, battery level detector 152 provides a “battery level signal” to voltage and frequency control circuitry. MTK-1006, 5:1-6. A POSITA would have understood that in these embodiments, Borkar uses power from the battery, which is a source external to the integrated circuit. MTK-1003, ¶89.

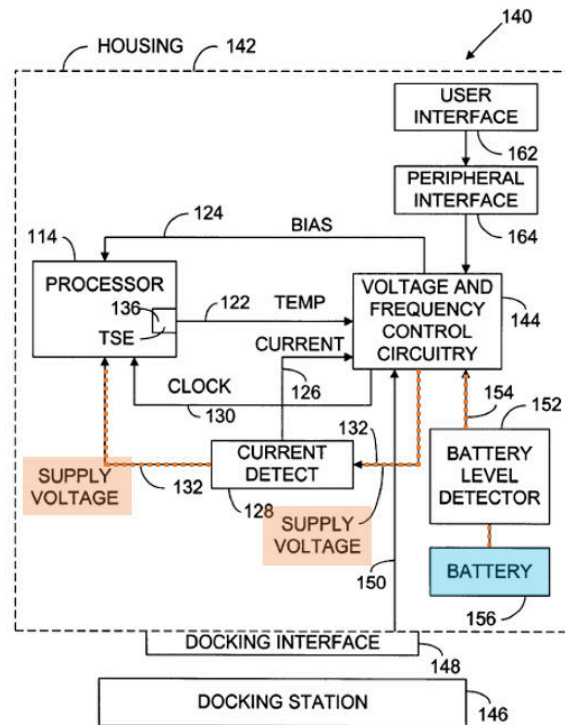


FIG. 2
MTK-1006, Fig. 2.

Further, Borkar explains that “[w]hen housing 142 is interfaced to docking station 146, *electrical power is being provided by an external source* rather than by battery 156.” MTK-1006, 5:53-55. Therefore, in addition to the supply voltage coming from the battery, Borkar discloses this additional “external source” when the device is interfaced to a docking station. MTK-1003, ¶90.

Both the voltage from the battery and the “external source” in Borkar are regulated to be changed. First, in some embodiments, the voltage passes through “voltage and frequency control circuitry” which controls the supply voltage. MTK-1006, 1:66-67 (“control circuitry may further control settings of a supply voltage signal.”), 11:58-60 (“the supply voltage signals may be the actual supply

voltage Vcc (sometimes called Vdd) applied to the transistors.”), Fig. 3; MTK-1003, ¶91. Second, the voltage can also be regulated through “supply generating circuitry” which also controls the supply voltage. MTK-1006, 11:58-60, 13:57-60, Fig. 9; MTK-1003, ¶91.

13. Claim 10

The Nowka-Borkar combination renders obvious an internal regulator to perform the regulation. First, Borkar’s “voltage and frequency control circuitry” is an internal regulator that performs regulation of the supply voltage. MTK-1006, 1:66-67 (“control circuitry may further control settings of a supply voltage signal.”), 11:58-60 (“the supply voltage signals may be the actual supply voltage Vcc (sometimes called Vdd) applied to the transistors.”); MTK-1003, ¶92. As shown in Figure 3, voltage control circuitry 178 is internal to the integrated circuit. MTK-1006, Fig. 3, 7:5-7 (“Voltage control circuitry may be on the same chip, (e.g., chip 186) as is processor 174[.]”).

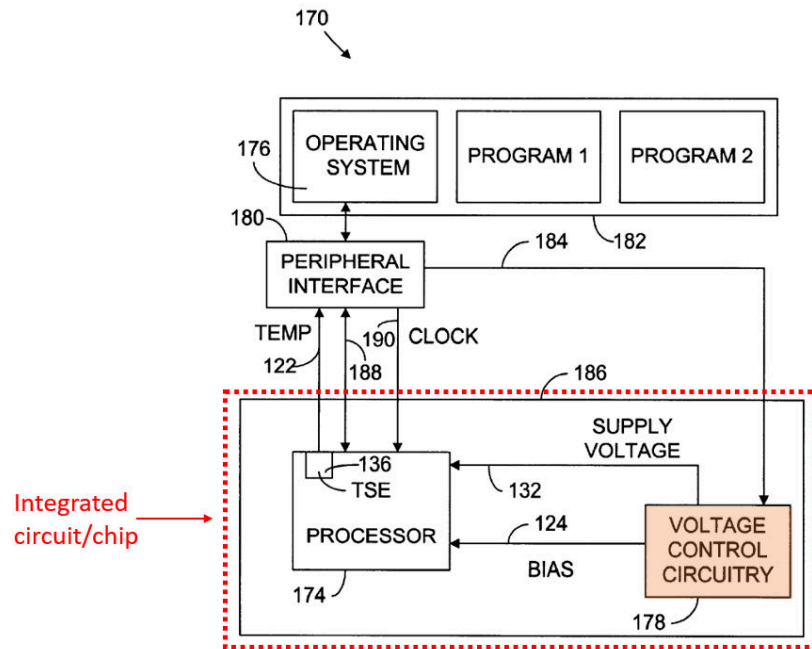


FIG. 3

MTK-1006, Fig. 3.

In addition, Borkar's Figure 9 shows "supply voltage generating circuitry 320 which provides one or more supply voltage signals in response to one or more supply voltage signals on conductor(s) 132 is included in processor 114." MTK-1006, 13:57-60; MTK-1003, ¶93. A POSITA would have understood that because the supply generating circuitry is included in processor 140, it is an internal voltage regulator that regulates the supply voltage. MTK-1003, ¶93.

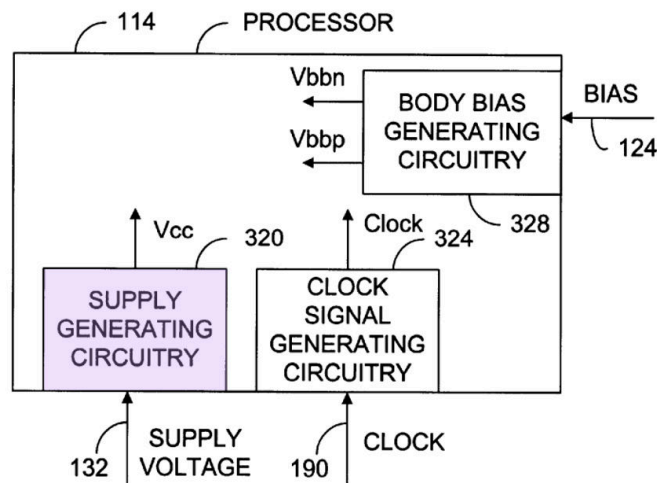
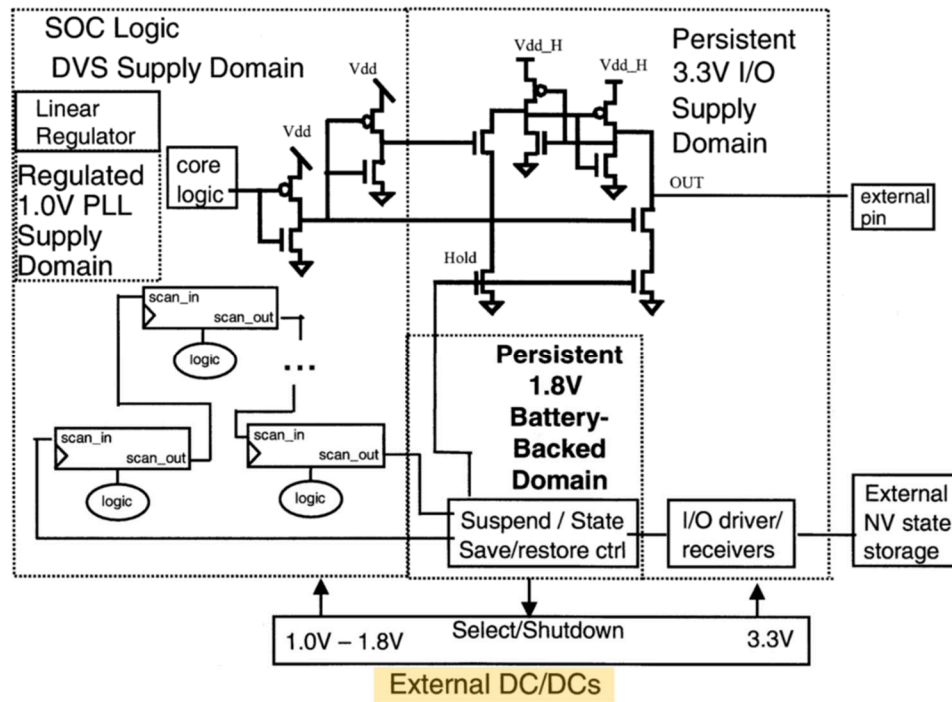


FIG. 9

MTK-1006, Figure 9.

14. Claim 11

The Nowka-Borkar combination renders obvious wherein the regulation is performed by an external regulator. In the combination, Nowka discloses an external “DC/DC converter, which controls the logic supply,” as shown in Figure 3. MTK-1004, 1442. The DC/DC converter is external to the chip, and supplies multiple voltages to the SOC, including a 1.0-1.8V variable supply depending on the needs of the circuit, and a persistent 3.3V supplied to the I/O drivers and receivers. MTK-1004, 1442. Accordingly, Nowka discloses wherein regulation is performed by an external regulator. MTK-1003, ¶94.



MTK-1004, Figure 3.

15. Claim 14

The Nowka-Borkar combination renders obvious wherein the integrated circuit is configured to have the one of plural threshold voltage selected by back biasing. As discussed for claim element 1[d], incorporated herein, Borkar discloses varying the threshold voltage of variable threshold transistors. Borkar discloses controlling the “transistor body bias” which refers to “the relationship between voltage of the source (V_{source}) of a field effect transistor (FET transistor) and voltage of the body (V_{bb}) of the FET transistor.” MTK-1006, 3:34-36; *see also* MTK-1006, 3:36-55; MTK-1003, ¶95. A POSITA would have understood that Borkar’s “body bias” includes “back biasing” of the ’811 patent because “body biasing” refers to applying a voltage to the body of a transistor, and “back

biasing” is a type of body biasing where the voltage is applied to the back side of a wafer. *See* MTK-1015, 680-681 (“Reverse biasing the ***back contact*** or bulk of a MOS transistor relative to the source is another method that has been employed to adjust the threshold potential. This electrical method of adjustment, which predates ion implantation, makes use of the so-called ***body effect*** or substrate-bias effect.”); MTK-1003, ¶95. To the extent that Borkar’s “body bias” does not explicitly disclose “back biasing,” it would have been obvious to a POSITA to implement back biasing as it is one of the basic modes of body biasing. MTK-1015, 680-681 MTK-1003, ¶95.

16. Claim 15

The Nowka-Borkar combination renders obvious wherein the integrated circuit comprises the power manager and the plurality of power islands. As discussed for claim elements 1[b] and 1[c], the Nowka-Borkar combination discloses an integrated circuit that comprises a power manager and plurality of power islands. MTK-1003, ¶96.

17. Claim 16

The Nowka-Borkar combination renders obvious wherein the power manager is configured to monitor one or more of the associated power consumptions using temperature or power dissipation measurement. In the combination, Borkar explicitly discloses that “control circuitry 118 ***monitors a***

temperature signal on conductor(s) 122.” MTK-1006, 4:13-14, Figs. 1-4; *see also* MTK-1006, 4:14-56; MTK-1003, ¶¶97-99.

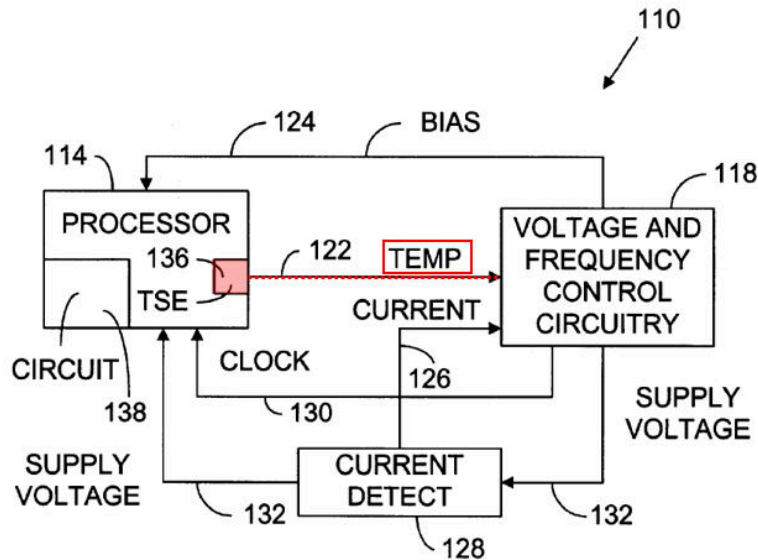


FIG. 1

MTK-1006, Fig. 1.

18. Claim 17

(a) 17[p]

Supra Ground 1A, claim 1[p]. MTK-1003, ¶100.

(b) 17[a]

Supra Ground 1A, claim 1[a]. MTK-1003, ¶101.

(c) 17[b]

Supra Ground 1A, claim 1[b]. MTK-1003, ¶102.

(d) 17[c]

Supra Ground 1A, claim 1[c]. MTK-1003, ¶103.

(e) 17[d]

Supra Ground 1A, claims 1, 6. MTK-1003, ¶104.

(f) 17[e]

Supra Ground 1A, claim 1[d]. MTK-1003, ¶105.

19. Claim 18

Supra Ground 1A, claims 2, 17. MTK-1003, ¶106.

20. Claim 19

The Nowka-Borkar combination renders obvious wherein the system is configured to permit a clock to be stopped during operation of the integrated circuit so that the power manager can control the associated power consumption of the at least one of the power islands. In the combination, Nowka discloses standby modes called “Freeze, Hibernation and Cryo modes.” MTK-1004, 1446. In Freeze mode, “*the system clock is stopped* and the logic supply is decreased to its minimum value of 1.0V.” MTK-1004, 1446. Similarly, in Cryo mode “the suspend controller *stops the clocks*, freezes the I/O drivers, scans the register state out through the IIC interface to nonvolatile storage, removes logic power and waits for a wakeup event.” MTK-1004, 1446; MTK-1003, ¶107.

21. Claim 21

The Nowka-Borkar combination renders obvious wherein the system is configured to have a clock stopped by clock gating. Nowka discloses “[t]he active

power consumption is reduced when resources demands are low through the use of dynamic voltage scaling, dynamic frequency scaling, *unit and register level functional clock gating*.” MTK-1004, 1442. Further, Nowka discloses that “dynamic power is saved in this design by *gating off* inactive latches [12] and units. Approximately 80% of the processor registers and 50% of the SOC core registers are functionally *clock gated* when they are not accessed.” MTK-1004, 1445; MTK-1003, ¶108.

22. Claim 22

Supra Ground 1A, claims 15, 17. MTK-1003, ¶109.

23. Claim 23

Supra Ground 1A, claims 16, 17. MTK-1003, ¶110.

24. Claim 24

(a) 24[p]

Supra Ground 1A, element 1[p]. MTK-1003, ¶111.

(b) 24[a]

Supra Ground 1A, elements 1[a], 1[b], 1[c], claim 2. MTK-1003, ¶112.

(c) 24[b]

Supra Ground 1A, element 1[d]. MTK-1003, ¶113.

25. Claim 25

Supra Ground 1A, claims 8, 24. MTK-1003, ¶114.

26. Claim 26

Supra Ground 1A, claims 9, 24. MTK-1003, ¶115.

27. Claim 28

Supra Ground 1A, claims 14, 24. MTK-1003, ¶116.

28. Claim 29

Supra Ground 1A, claims 16, 24. MTK-1003, ¶117.

29. Claim 30

(a) 30[p]

Supra Ground 1A, element 1[p]. MTK-1003, ¶118.

(a) 30[a]

Supra Ground 1A, element 1[a]. MTK-1003, ¶119.

(b) 30[b]

Supra Ground 1A, element 1[b]. MTK-1003, ¶120. The Nowka-Borkar combination further provides a first of the power islands being configured to communicate synchronously and asynchronously with a second of the power islands. Borkar discloses that some domains “may run off the same clock signal or otherwise need to run synchronously.” MTK-1006, 10:6-7. “Indeed, there can be reasons ...[that] groups of transistors that run off a different clock signal or that are asynchronous.” MTK-1006, 10:16-18. From this disclosure, a POSITA would have understood and found obvious that Borkar’s domains can communicate synchronously or asynchronously. MTK-1006, 10:6-18; MTK-1003, ¶121.

On the terms “synchronously” and “asynchronously,” Petitioner notes that in a prior litigation involving the ’811 patent, the court construed the term “synchronously” as “with coordination between components (i.e., power islands) before communication transmission begins,” “asynchronously” as “without coordination between components (i.e., power islands) before transmission begins.” MTK-1011 at 45. For purposes of this Petition, Petitioner submits that there is no construction necessary because the plain and ordinary meaning suffices. MTK-1003, ¶122. However, the Nowka-Borkar combination also renders this element obvious under the prior court’s construction because Borkar describes domains that communicate synchronously (with coordination between components before transmission begins) and asynchronously (without coordination between components before transmission begins). MTK-1003, ¶122.

(c) 30[c]

Supra Ground 1A, element 1[c]. MTK-1003, ¶123.

(d) 30[d]

Supra Ground 1A, element 1[d]. MTK-1003, ¶124.

30. Claim 31

Supra Ground 1A, claims 2, 30. MTK-1003, ¶125.

31. Claim 32

Supra Ground 1A, claims 19, 30. MTK-1003, ¶126.

32. Claim 33

Supra Ground 1A, claims 9, 30. MTK-1003, ¶127.

33. Claim 34

Supra Ground 1A, claims 10, 33. MTK-1003, ¶128.

34. Claim 35

Supra Ground 1A, claims 11, 33. MTK-1003, ¶129.

35. Claim 38

Supra Ground 1A, claims 21, 30. MTK-1003, ¶130.

36. Claim 39

Supra Ground 1A, claims 4, 30. MTK-1003, ¶131.

37. Claim 40

Supra Ground 1A, claims 5, 39. MTK-1003, ¶132.

38. Claim 41

Supra Ground 1A, claims 6, 30. MTK-1003, ¶133.

39. Claim 42

Supra Ground 1A, claims 7, 41. MTK-1003, ¶134.

40. Claim 43

Supra Ground 1A, claims 15, 30. MTK-1003, ¶135.

41. Claim 44

Supra Ground 1A, claims 16, 30. MTK-1003, ¶136.

42. Claim 45

(a) 45[p]

Supra Ground 1A, element 1[p]. MTK-1003, ¶137.

(b) 45[a]

Supra Ground 1A, element 1[a]. MTK-1003, ¶138.

(c) 45[b]

Supra Ground 1A, element 1[b]. MTK-1003, ¶139.

(d) 45[c]

Supra Ground 1A, elements 1[b], 1[c]. MTK-1003, ¶140.

(e) 45[d]

Supra Ground 1A, element 1[d]. MTK-1003, ¶141.

43. Claim 46

Supra Ground 1A, claims 2, 45. MTK-1003, ¶142.

44. Claim 47

Supra Ground 1A, claims 3, 45. MTK-1003, ¶143.

45. Claim 48

Supra Ground 1A, claims 4, 45. MTK-1003, ¶144.

46. Claim 49

Supra Ground 1A, claims 5, 48. MTK-1003, ¶145.

47. Claim 50

Supra Ground 1A, claims 6, 45. MTK-1003, ¶146.

48. Claim 51

Supra Ground 1A, claims 7, 50. MTK-1003, ¶147.

49. Claim 52

Supra Ground 1A, claims 5, 45. MTK-1003, ¶148.

50. Claim 53

Supra Ground 1A, claims 9, 45. MTK-1003, ¶149.

51. Claim 54

Supra Ground 1A, claims 10, 53. MTK-1003, ¶150.

52. Claim 55

Supra Ground 1A, claims 11, 53. MTK-1003, ¶151.

53. Claim 58

Supra Ground 1A, claims 14, 45. MTK-1003, ¶152.

54. Claim 59

Supra Ground 1A, claims 15, 45. MTK-1003, ¶153.

55. Claim 60

Supra Ground 1A, claims 16, 45. MTK-1003, ¶154.

56. Claim 61

(a) 61[p]

Supra Ground 1A, claims 1[p]. MTK-1003, ¶155.

(a) 61[a]

Supra Ground 1A, claims 1[a]. MTK-1003, ¶156.

(b) 61[b]

Supra Ground 1A, claims 30[b]. MTK-1003, ¶157.

(c) 61[c]

Supra Ground 1A, claims 1[b], 1[c], 1[d]. MTK-1003, ¶158.

57. Claim 62

Supra Ground 1A, claims 2, 61. MTK-1003, ¶159.

58. Claim 63

Supra Ground 1A, claims 9, 61. MTK-1003, ¶160.

59. Claim 64

Supra Ground 1A, claims 10, 63. MTK-1003, ¶161.

60. Claim 65

Supra Ground 1A, claims 11, 63. MTK-1003, ¶162.

61. Claim 68

Supra Ground 1A, claims 21, 61. MTK-1003, ¶163.

62. Claim 69

Supra Ground 1A, claims 4, 61. MTK-1003, ¶164.

63. Claim 70

Supra Ground 1A, claims 5, 69. MTK-1003, ¶165.

64. Claim 71

Supra Ground 1A, claims 10, 61. MTK-1003, ¶166.

65. Claim 72

Supra Ground 1A, claims 7, 71. MTK-1003, ¶167.

66. Claim 73

Supra Ground 1A, claims 15, 61. MTK-1003, ¶168.

67. Claim 74

Supra Ground 1A, claims 16, 61. MTK-1003, ¶169.

B. GROUND 1B —Claims 12, 36, 56, 66 are obvious over Nowka-Borkar and Rincon-Mora

1. Overview of Rincon-Mora

Rincon-Mora relates to voltage regulator circuits of the low dropout type. MTK-1007, 1:11-13. Rincon-Mora explains that “voltage regulator circuits are commonly used circuits for generating a stable voltage from an input voltage supply that may vary over time, and over varying load conditions.” MTK-1007, 1:13-16. Further, “in battery-powered systems, the demand is high for voltage regulators that can generate a low-noise stable output voltage with a minimum difference in potential between the input voltage and the regulated output voltage (the minimum potential difference is referred to as the “drop-out” voltage).” MTK-1007, 1:17-22. To meet this need, Rincon-Mora describes “a voltage regulator circuit in which load regulation, transient response, and power efficiency may be optimized.” MTK-1007, 2:15-17.

2. The Nowka-Borkar-Rincon-Mora Combination

A POSITA would have been motivated to modify the Nowka-Borkar system to incorporate the teachings of Rincon-Mora with reasonable expectation of success. Nowka, Borkar, and Rincon-Mora are in the same field of endeavor: integrated circuit applications, such as battery powered devices. MTK-1004, Abstract (“PowerPC system-on-a-chip processor which makes use of dynamic voltage scaling and on-the-fly frequency scaling to adapt to the dynamically changing performance demands and power consumption constraints of high-content, battery powered applications.”); MTK-1006, 1:53-56 (“The switching rate can also lead to an increase in power consumption rate because more instructions can be executed in a shorter amount of time. This is particularly a problem with battery driven processor”); MTK-1007, 2:25-28 (“It is a further object of the present invention to provide such a voltage regulator circuit which is suitable for use in low power supply voltage applications, such as in battery-powered systems.”).

Thus, Rincon-Mora is pertinent art in the same field as Nowka and Borkar, and it would have been obvious to implement the teachings of Rincon-Mora in the Nowka-Borkar combination’s integrated circuit. MTK-1003, ¶172. A POSITA would have been motivated to incorporate Rincon-Mora’s low dropout regulator in the Nowka-Borkar system to improve the stability and noise of the regulated

voltage. MTK-1003, ¶172. For example, Nowka's SOC includes an "external DC/DC converter" used to "provide the logic supply." MTK-1004, 1442. Rincon-Mora discloses that "[c]onventional DC-DC converter circuitry typically produces power supply voltages that are somewhat noisy, and that fluctuate to some extent." MTK-1007, 10:44-46. A POSITA would have understood that Rincon-Mora's low dropout voltage regulator would provide a low-noise and stable supply voltage for use in the Nowka-Borkar combination integrated circuit. MTK-1003, ¶172.

Further, Rincon-Mora discloses that the voltage regulator "is suitable for implementation as part of an overall larger integrated circuit or, alternatively, may be realized as a separate stand-alone integrated circuit." MTK-1007, 3:2-5. It would have been obvious to use a low dropout voltage regulator to generate the variable supply voltage used in a variable power domain. MTK-1003, ¶173. A POSITA would have understood that the type of regulator used in a circuit, such as a low dropout voltage regulator, is merely a design choice. MTK-1003, ¶173.

1. Claim 12

The Nowka-Borkar-Rincon-Mora combination renders obvious a dropout voltage regulator to provide the supply voltage. Rincon-Mora discloses a "low drop-out (LDO) voltage regulator and system." MTK-1007, Abstract. Further, Rincon-Mora discloses that the "voltage regulator circuit according to this embodiment of the invention also provides these advantages in a circuit which may

be efficiently implemented into an integrated circuit according to conventional technology, and is contemplated to be quite stable and robust in operation.” MTK-1007, 9:15-19. Therefore, a low drop-out voltage regulator such as that described in Rincon-Mora would have been efficiently and easily incorporated into an integrated circuit like the Nowka-Borkar system, specifically to operate with Nowka’s external DC/DC converter to provide the voltage supply to the SOC. MTK-1004, 1442; MTK-1003, ¶174.

2. Claim 36

Supra Ground 1B, claims 12, 33. MTK-1003, ¶175.

3. Claim 56

Supra Ground 1B, claims 12, 53. MTK-1003, ¶176.

4. Claim 66

Supra Ground 1B, claims 12, 63. MTK-1003, ¶177.

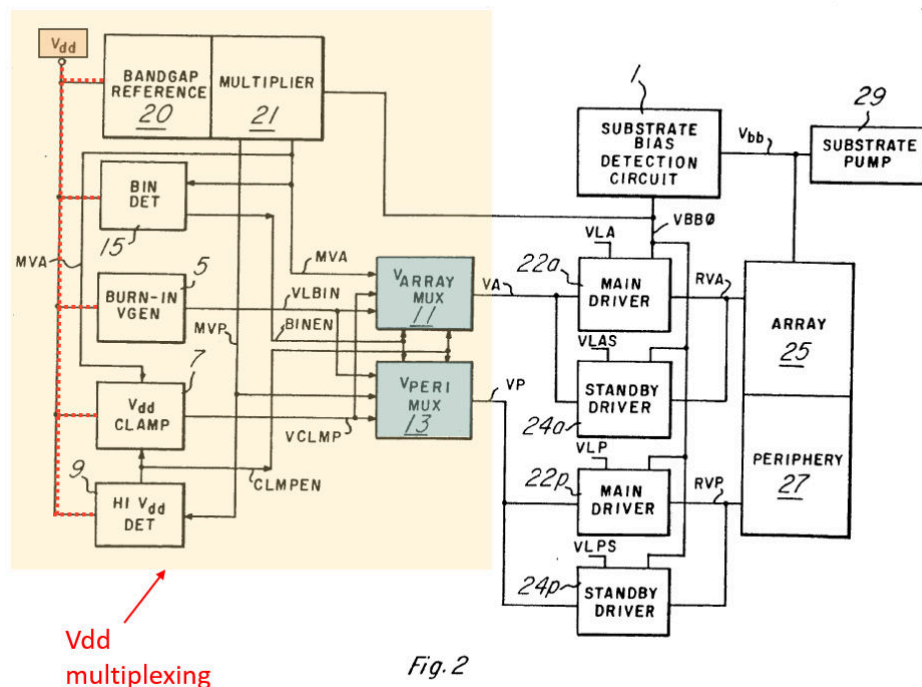
C. GROUND 1C – Claims 13, 20, 27, 37, 57, 67 are obvious over Nowka-Borkar and Iyengar

1. Overview of Iyengar

Iyengar explains: “[T]he power supply voltages applied to such high density VLSI devices including dRAMs, other memories, and logic devices, are preferably reduced as the feature sizes decrease.” MTK-1022, 1:65-2:1. “It should therefore be evident that the [prior art] provides quite limited flexibility to the designer of the circuit using such a power regulation system, especially in selecting a stress

voltage.” MTK-1022, 3:64-67. “It is therefore an object of this invention to provide an on-chip system for regulating the power supply voltage applied to various portions of a large scale integrated circuit.” MTK-1022, 4:11-15.

Relevant to this petition, Iyengar discloses a voltage multiplexer. Specifically, two multiplexers shown in Figure 2 perform Vdd multiplexing. MTK-1022, Fig. 2. V_{ARRAY} multiplexer and V_{PERI} multiplexer select between different voltage sources based on the condition of the power supply voltage Vdd. MTK-1022, 19:22-52.



MTK-1022, Fig. 2.

2. The Nowka-Borkar-Iyengar Combination

A POSITA would have been motivated to modify Nowka’s SOC to

incorporate the teachings of Iyengar with reasonable expectation of success.

Nowka, Borkar, and Iyengar are in the same field of endeavor: power management on an integrated circuit. MTK-1004, Abstract (“PowerPC system-on-a-chip processor which makes use of dynamic voltage scaling and on-the-fly frequency scaling to adapt to the dynamically changing performance demands and power consumption constraints of high-content, battery powered applications.”); MTK-1006, 2:50-57 (“The invention may also include changing clock frequency signals and supply voltage signals to at least partially control a parameter. A parameter of the integrated circuit is a characteristic of the integrated circuit which can vary during performance including temperature, power consumption, and performance.”); MTK-1022, 1:11-13 (“This invention is in the field of integrated circuits and is more specifically directed to on-chip power supply control.”).

Thus, Iyengar is pertinent art in the same field as Nowka and Borkar, and it would have been obvious to implement the teachings of Iyengar in the Nowka-Borkar combination’s integrated circuit. For example, Iyengar explains that due to the increasing complexity and density of circuit design, “the power supply voltages applied to such high density VLSI devices including dRAMs, other memories, and logic devices, are preferably reduced[.]” MTK-1022, 1:65-2:1; MTK-1003, ¶181. In its proposed solution, Iyengar provides an embodiment with two multiplexers, V_{ARRAY} multiplexer and V_{PERI} multiplexer, which choose the appropriate voltage

signal for the array and peripheral circuitry, respectively, based on control signals.

MTK-1022, 6:18-26. A POSITA would have been motivated to implement a similar multiplexer in the Nowka-Borkar system, for example to provide the variable voltage in the 1.0-1.8V logic domain. MTK-1004, 1442 (“The logic supply for the processor core, caches, SOC cores and accelerators is dynamically varied between 1 and 1.8 V.”), Fig. 3; MTK-1003, ¶181.

3. Claim 13

The Nowka-Borkar-Iyengar combination renders obvious wherein the integrated circuit is configured to have the supply voltage controlled by Vdd multiplexing in relation to the at least one of the power islands. A POSITA would have been motivated to incorporate Iyengar’s voltage multiplexer in the Nowka-Borkar system to provide the variable voltage. For example, the DC/DC converter in Nowka would have been configured to provide multiple Vdd levels (similar to the discussion of multiple independent power supply pins in the DC/DC converter in the ’811 patent, MTK-1001, 8:45-49, Fig. 7), and a multiplexer such as that in Iyengar would have been used to select among those different voltage levels. MTK-1003, ¶182. Employing a multiplexer in this way to allow for varying voltage supply would have been a simple design choice. MTK-1003, ¶182.

4. Claim 20

Supra Ground 1C, claims 13, 17. MTK-1003, ¶183.

5. Claim 27

Supra Ground 1C, claims 13, 24. MTK-1003, ¶184.

6. Claim 37

Supra Ground 1C, claims 13, 30. MTK-1003, ¶185.

7. Claim 57

Supra Ground 1C, claims 13, 45. MTK-1003, ¶186.

8. Claim 67

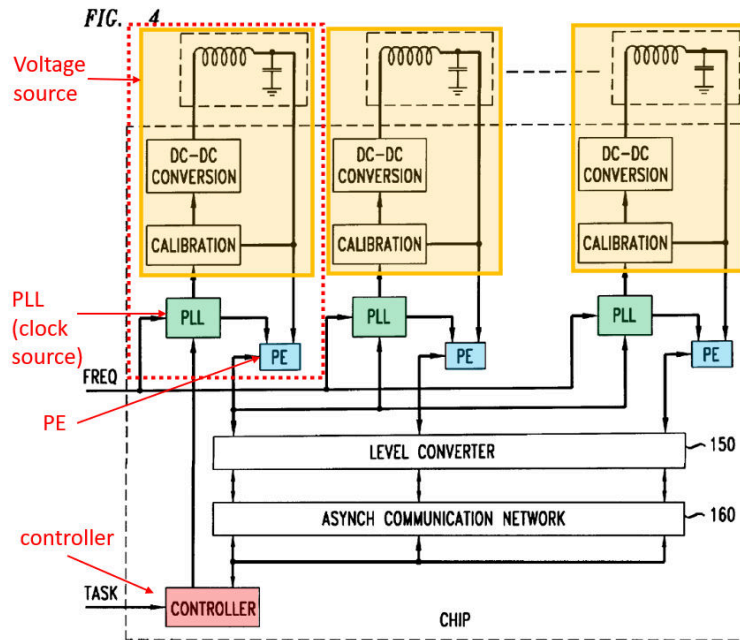
Supra Ground 1C, claims 13, 61. MTK-1003, ¶187.

D. GROUND 2A—Claims 1-11, 14-19, 21-26, 28-35, 38-55, 58-65, 68-74 are obvious over Nicol and Borkar

1. Overview of Nicol

Nicol discloses a dynamic load-balancing mechanism in a multiprocessor chip which divides tasks among multiple processors (or “processing elements,” “PEs”), and then adjusts the frequency and voltage of those processors to minimize power consumption. MTK-1008, Abstract; MTK-1003, ¶¶189-191. Nicol explains that there are “tasks that cannot be partitioned into concurrent evenly-loaded threads and, therefore, some PE within the multiprocessor would require a higher operating frequency and a higher operating voltage.” MTK-1008, 5:60-65; MTK-1003, ¶192. To address this limitation, Figure 4 shows each PE with its own associated clock source and voltage source to allow “the operating system to independently program the lowest operating frequency and corresponding lowest

supply voltage for each PE.” MTK-1008, 5:66-6:3, Fig. 4; MTK-1003, ¶¶192-193.



MTK-1008, Fig. 4.

2. Overview of Borkar

Supra Ground 1A, Overview of Borkar. MTK-1003, ¶194.

3. The Nicol-Borkar Combination

A POSITA would have been motivated to modify Nicol’s integrated circuit to incorporate the teachings of Borkar with reasonable expectation of success.

Nicol and Borkar are in the same field of endeavor: power management on an integrated circuit. Nicol relates to “electronic circuits and, more particularly to power consumption within electronic circuits.” MTK-1008, Abstract, 1:6-7

Similarly, Borkar describes changing body bias, clock frequency and supply voltage to “control a parameter of the processor.... Examples of the parameters

include performance, power consumption, and temperature.” MTK-1006, 1:60-2:3; MTK-1003, ¶196.

Further, Nicol and Borkar address the same known problem, the need to balance performance with power consumption in electronic systems. MTK-1008, 2:65-3:9 (discussing how power consumption and performance should match the load in order to optimize power savings), MTK-1006, 1:20-21 (“The performance, power consumption, and temperature [of an integrated circuit] are typically related.”), 5:45-46 (“The user may specify certain power conditions or a power versus performance tradeoff.”); MTK-1003, ¶197. Both Nicol and Borkar also suggest the solution of dynamically controlling variables such as frequency and voltage in response to changing needs and operations. MTK-1008, 4:64-66 (“The reduced load permits lowering the clock frequency to 100 MHz and lowering the supply voltage to 2.1V.”), 5:66-6:2; MTK-1006, 5:25-29 (“In some embodiments, when the battery level signal is below a certain level, the supply voltage is lowered, the frequency of a processor clock is lowered, and/or the bias signals are changed to raise the threshold voltages of some or all of the transistors.”), 2:52-54; MTK-1003, ¶198.

The similarities across Nicol and Borkar’s disclosures would have led a POSITA to incorporate Borkar’s teachings in Nicol’s dynamic power management. For example, Nicol discusses the need to adjust to temperature variations “to

achieve high performance at varying operating temperatures and process corners.”

MTK-1008, 1:41-44, 1:65-67. A POSITA would have understood that the discussion of temperature variation is closely related to the need to monitor power consumption because, as Borkar teaches, “performance, power consumption, and temperature are typically related.” MTK-1006, 1:19-20; MTK-1003, ¶199. A POSITA would have understood that Borkar’s power consumption monitoring mechanism would provide an additional check on the adverse effects of high power consumption (which causes high temperature) that Nicol discusses. MTK-1003, ¶199.

4. Claim 1

(a) 1[p]

To the extent the preamble is limiting, the Nicol-Borkar combination renders obvious a system. For example, Nicol describes its embodiments as a “system.” MTK-1008, 1:56-67, 3:20-27, 5:23-24, 6:16-20; MTK-1003, ¶200. Also, Borkar discloses a “system.” MTK-1006, 1:59-60, 2:61-65, 4:60-64, 5:1-2; MTK-1003, ¶200.

(b) 1[a]

The Nicol-Borkar combination renders obvious an integrated circuit. Nicol discloses improving performance of multi-processor chips. MTK-1008, Abstract, 2:18-22. The “chip” refers to an integrated circuit, while “multi-processor” refers

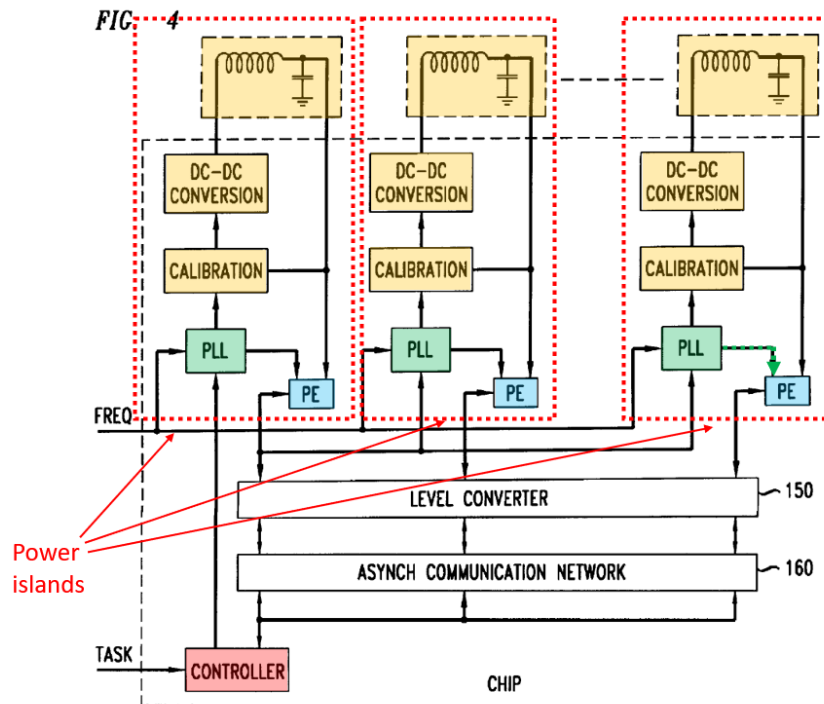
to multiple processors, or processing elements (PEs), on the integrated circuit.

MTK-1008, 6:6-9 (“As shown in FIG. 4, all of the controllers are embodied in a single controller 200, which may be just another *processing element* of the *integrated circuit* that contains the other processing elements.”), cl. 5 (“The method of claim 1, wherein said steps are executed in a *multiprocessor integrated circuit*.”), Figs. 2, 4; MTK-1003, ¶201. Borkar also discloses managing power on an integrated circuit. MTK-1006, 2:49-60 (“The invention involves changing body bias signals applied to transistors *in an integrated circuit* in response to changing conditions to at least partially control a parameter of the *integrated circuit*....”), 4:5-9; MTK-1003, ¶201.

(c) 1[b]

The Nicol-Borkar combination renders obvious a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions adapted to be independently controlled. The ’811 patent defines “power island” as “any section, delineation, partition, or division of the integrated circuit [] where power consumption is controlled within the section, delineation, partition, or division.” MTK-1001, 3:59-62. In the embodiment shown in Figure 4 of Nicol, “[a] separate power supply for each PE in a chip...[allows] the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.” MTK-1008, 5:66-6:2, Fig. 4.

Thus, a POSITA would have understood and found obvious that Nicol's plurality of processing elements is a plurality of power islands, each with a power consumption adapted to be independently controlled. MTK-1003, ¶¶203-204.



MTK-1008, Fig. 4.

To the extent it is argued that Nicol does not explicitly disclose a plurality of power islands, Borkar also discloses and renders obvious a plurality of power islands, each with a power consumption independently controllable by changing a supply voltage and operating frequency. For example, Borkar discloses multiple “domains,” or groups of transistors, which have distinct power parameters. MTK-1006, 9:48-52, 9:58-59, 10:34-36. Body bias, supply voltage, and clock frequency of the each domain can be controlled individually. MTK-1006, 10:24:29.

Exemplary embodiments are shown in Figures 5 and 7. Accordingly, a POSITA would have understood and found obvious that Borkar's domains are a plurality of power islands, each with a power consumption that is independently controllable by changing supply voltage and frequency. MTK-1003, ¶¶205-206.

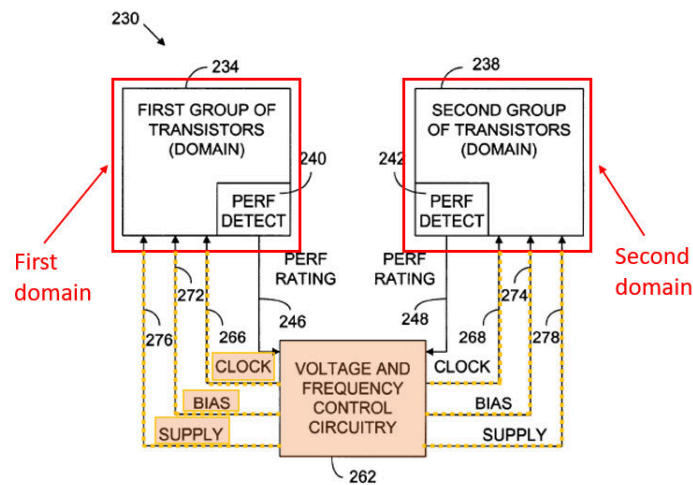


FIG. 5

MTK-1006, Fig. 5.

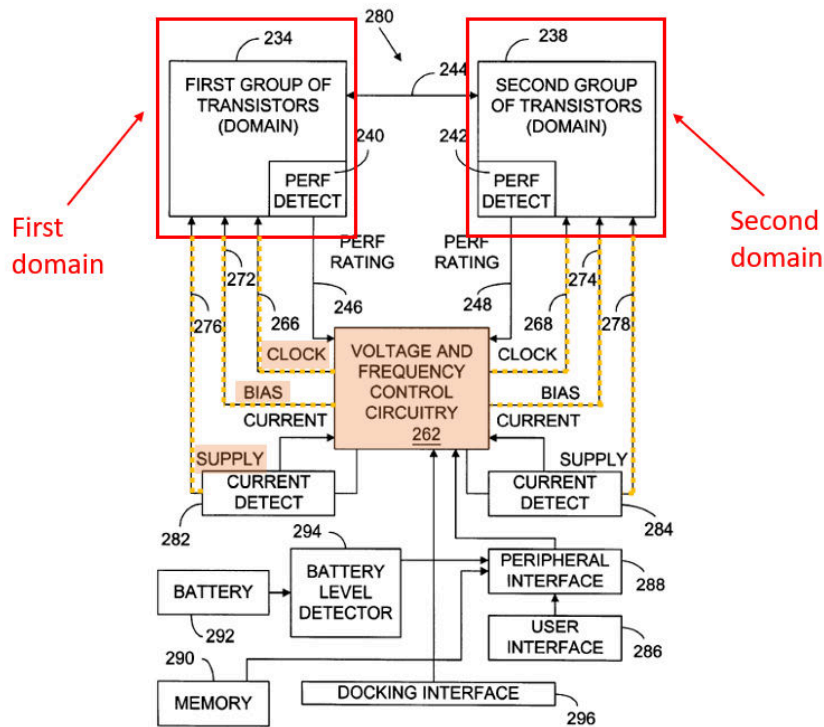


FIG. 7

MTK-1006, Fig. 7.

(d) 1[c]

The Nicol-Borkar combination renders obvious a power manager to control the power consumptions. First, a POSITA would have understood that Nicol’s “controller” PE was a power manager because it allocates tasks among the other PEs, and adjusts their frequencies and voltages accordingly to change their power consumptions. Nicol’s “controller” PE (or “PE 200”) “allocates tasks to the other PEs” and “consider[s] the PE with the tasks that require the most time to carry out, and adjust[s] the clock frequency to insure that the most heavily loaded PE carries out its assigned tasks within the required completion time. Once the frequency is

thus determined, a minimum supply voltage can be determined.” MTK-1008, 2:53-54, 3:66-4:10; MTK-1003, ¶207.

Borkar also discloses a “power manager” that controls the power consumptions: Borkar’s “control circuitry controls the setting responsive to processor signal resulting for execution of software. The control circuitry may further control settings of a supply voltage signal and a clock signal to control settings of a supply voltage signal and a clock signal to control the parameter.” MTK-1006, 1:63-2:1; *see also* MTK-1006, 2:63-3:11, 4:3-11, 4:20-33, 5:47-64, 6:12-53, 11:25-67, Figs. 1-5, 7. A POSITA would have understood Borkar’s “control circuitry” to be a power manager because it controls the power consumption of the relevant processor(s) or domain(s). MTK-1003, ¶208.

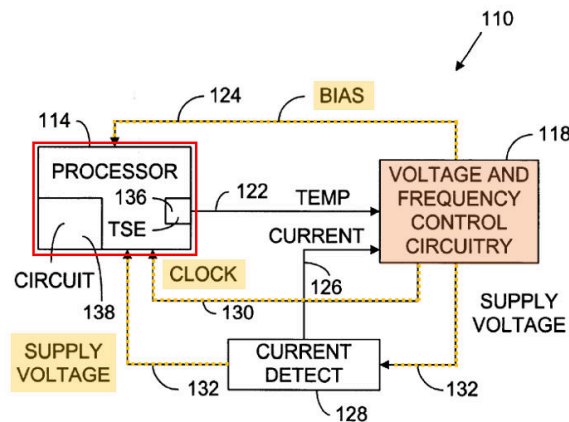


FIG. 1

MTK-1006, Fig. 1.

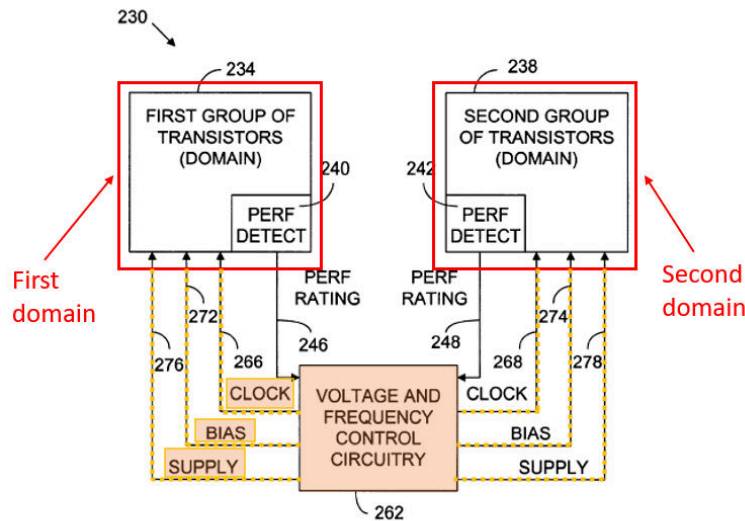


FIG. 5

MTK-1006, Fig. 5.

(a) 1[d]

The Nicol-Borkar combination renders obvious at least one of the power islands adapted to have the power manager control its associated power consumption by a) the at least one of the power islands being configured to have one of plural threshold voltages of variable threshold transistors selected, and b) the system being configured to perform, during operation, an action on the at least one of the power islands, the action including changing a frequency of operation or changing a supply voltage.

Nicol discusses existing techniques in the art “tuning the threshold voltages” to “ensure that the leakage current...does not become too large,” MTK-1008, 2:3-10, which would motivate a POSITA to implement selecting one of plural

threshold voltages, either in light of Nicol alone, or in view of Borkar as explained below. MTK-1003, ¶209.

Borkar discloses controlling power consumption of a power island by selecting a threshold voltage, as well as changing a frequency of operation or supply voltage during operation. For example, “[i]n some embodiments, when the battery level signal is below a certain level, the supply voltage is lowered, the frequency of a processor clock is lowered, and/or the bias signals are changed to raise the threshold voltages of some or all of the transistors. This will reduce the power consumption to maintain the battery.” MTK-1006, 5:25-30; *see also* MTK-1006, 5:30-34, 6:15-24, 6:31-40; MTK-1003, ¶211. A POSITA would have been motivated to combine Nicol and Borkar for the reasons previously explained. *Supra*, Section III.D.3. MTK-1003, ¶210.

As detailed for element 1[b], Nicol discloses the actions of changing the frequency of operation or changing the supply voltage during operation. “A separate power supply for each PE in a chip...[allows] the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.” MTK-1008, 5:66-6:2, Fig. 4; MTK-1003, ¶¶212-213. Further, as explained in 1[b], incorporated herein, Borkar also discloses changing frequency of operation or supply voltage of a power island during operation. MTK-1003, ¶214.

5. Claim 2

The Nicol-Borkar combination renders obvious wherein the power manager comprises a programmable processor. A POSITA would have understood and found obvious that Nicol's "controller" is a programmable processor. MTK-1008, 2:53-54, 3:66-4:10, 5:23-28, 6:6-13; MTK-1003, ¶215. Further, a POSITA would have understood and found obvious that the control circuitry in Borkar was a programmable processor because it can be programmed to manage power in various ways. *See, e.g.*, MTK-1006, 4:47-56, 6:1-7, 6:41-53; MTK-1003, ¶216.

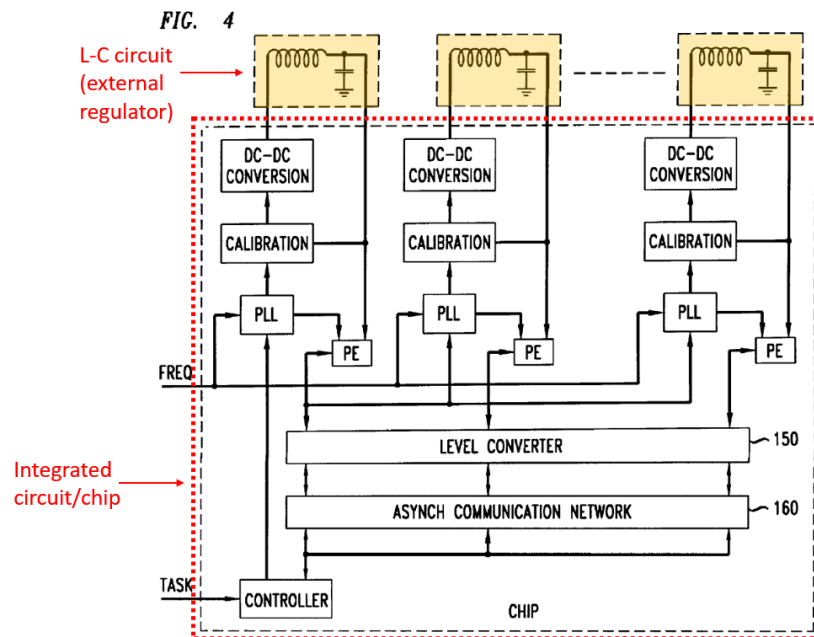
6. Claim 3

The Nicol-Borkar combination renders obvious wherein the integrated circuit is configured to perform, during operation, both changing the frequency of operation and changing the supply voltage. As discussed above for limitation 1[b] and 1[d], Nicol discloses changing supply voltage and operating frequency during operation. MTK-1003, ¶217.

Borkar also discloses changing frequency and supply voltage during operation. MTK-1006, 2:52-57 ("The invention may also include changing clock frequency signals and supply voltage signals to at least partially control a parameter. A parameter of the integrated circuit is a characteristic of the integrated circuit which can vary during performance including temperature, power consumption, and performance."); MTK-1003, ¶218.

7. Claim 4

The Nicol-Borkar combination renders obvious wherein the system is configured to have the supply voltage provided by an external regulator. Nicol discloses that “there has been considerable interest in integrating much of the buck controller circuit onto the chip. The only off-chip components are the inductor [] and capacitor [] used in the buck converter.” MTK-1008, 1:56-60. Figure 4 illustrates such a divided buck controller circuit: the L-C circuit (inductor-capacitor) is external to the chip, while the calibration circuit and DC-DC conversion are internal to the chip. MTK-1008, 4:28-37, Fig. 4; MTK-1003, ¶219.



MTK-1008, Fig. 4.

A POSITA would have understood that Nicol’s L-C circuit to be an “external regulator” that provides the supply voltage. The plain meaning of the

claim language requires that the regulator be “external” and provide the supply voltage, which the L-C circuit is and does. MTK-1008, 4:31-36 (“...to cause the combination of converter [] and L-C circuit [] to *create the supply voltage Vdd-local*, which is...applied to all of the PEs.”); MTK-1003, ¶220.

Additionally, Borkar discloses an external regulator that provides the supply voltage. While Figure 3 depicts the “voltage control circuitry” inside of the chip, Borkar also discloses that “Voltage control circuitry 178 may be on the same chip (e.g., chip 186) as is processor 174 *or on a different chip.*” MTK-1006, 7:5-7. When the control circuitry is on a different chip than the processor, it would necessarily be external to the chip that contains the processor, thus making it an external regulator. MTK-1003, ¶221.

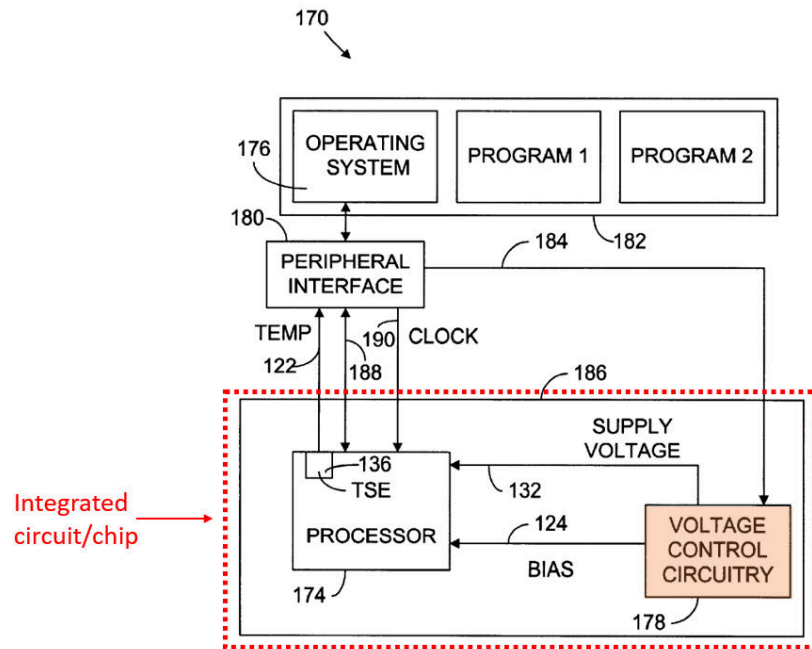


FIG. 3

MTK-1006, Fig. 3.

8. Claim 5

The Nicol-Borkar combination renders obvious wherein the external regulator is configured to be controlled by the power manager. Nicol discloses that “the operating system [] independently program[s] the lowest operating frequency and corresponding lowest supply voltage for each PE” and “[t]he supply voltage command is applied to dc-dc converter 130 followed by L-C circuit 140 to cause the combination of converter 130 and L-C circuit 140 to create the supply voltage Vdd-local[.]” MTK-1008, 5:66-6:2, 4:31-32. Therefore, a POSITA would have understood that the L-C circuit (external regulator) is configured to be controlled by the “controller” (“power manager”). MTK-1008, 6:6-9; MTK-1003, ¶222.

9. Claim 6

The Nicol-Borkar combination renders obvious an internal regulator to provide the supply voltage. In the combination, Borkar's "voltage and frequency control circuitry" is an internal regulator that provides the supply voltage. MTK-1006, 1:66-67 ("control circuitry may further control settings of a supply voltage signal."), 11:58-60 ("the supply voltage signals may be the actual supply voltage Vcc (sometimes called Vdd) applied to the transistors."); MTK-1003, ¶223. As shown in Figure 3, voltage control circuitry 178 is internal to the integrated circuit. MTK-1006, Fig. 3, 7:5-7 ("Voltage control circuitry may be on the same chip, (e.g., chip 186) as is processor 174[.]").

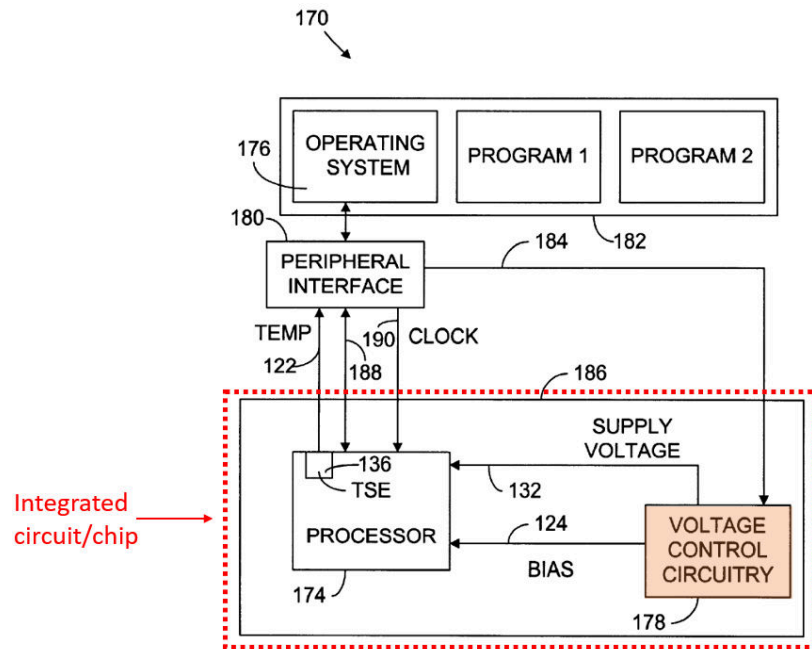


FIG. 3

MTK-1006, Fig. 3.

In addition, Borkar's Figure 9 shows "supply voltage generating circuitry 320 which provides one or more supply voltage signals in response to one or more supply voltage signals on conductor(s) 132 is included in processor 114." MTK-1006, 13:57-60. This "supply voltage generating circuitry" is also an internal regulator (in this case, internal to the processor) that provides the supply voltage. MTK-1006, 11:58-60 ("the supply voltage signals may be the actual supply voltage Vcc (sometimes called Vdd) applied to the transistors."); MTK-1003, ¶224.

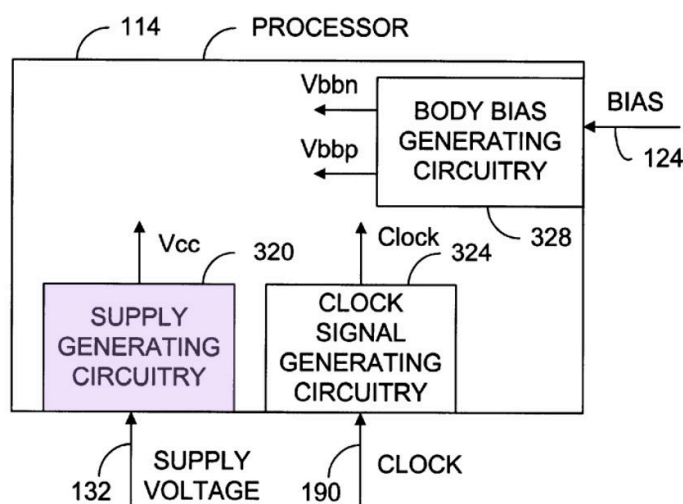


FIG. 9
MTK-1006, Fig. 9.

10. Claim 7

The Nicol-Borkar combination renders obvious wherein the internal regulator is configured to be controlled by the power manager. Borkar's "supply generating circuitry" shown in Figure 9, which is an internal regulator as explained in claim 6, is configured to be controlled by the "control circuitry" (power manager). For example, Borkar explains that "supply voltage generating circuitry 320" "provides one or more supply voltage signals in response to one or more supply voltage signals on conductor(s) 132 is included in processor 114." MTK-1006, 13:57-60; *see also* MTK-1006, 11:58-60. As depicted in Figure 9, the supply generating circuitry receives "supply voltage" which comes from voltage and frequency control circuitry, and thus is controlled by the control circuitry. MTK-1006, 3:12-16, Fig. 9; MTK-1003, ¶¶225-226.

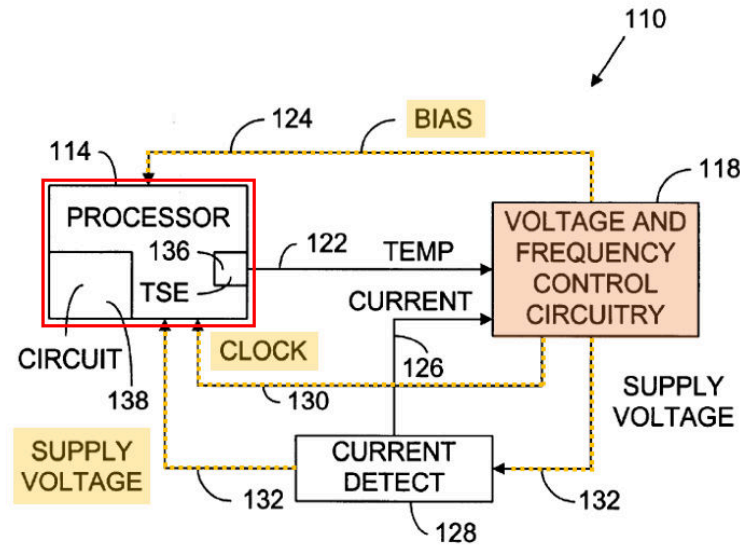


FIG. 1

MTK-1006, Fig. 1.

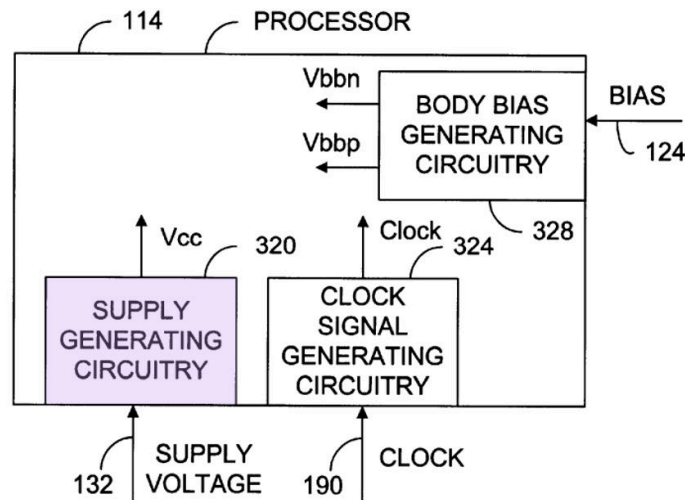


FIG. 9

MTK-1006, Fig. 9.

11. Claim 8

The Nicol-Borkar combination renders obvious wherein the at least one of the power islands is configured to have the one of plural threshold voltages

selected during operation of the integrated circuit. Borkar discloses changing power consumption of a power island (processor or domain) by selecting a threshold voltage. For example, “[i]n some embodiments, when the battery level signal is below a certain level, the supply voltage is lowered, the frequency of a processor clock is lowered, and/or the bias signals are changed to raise the threshold voltages of some or all of the transistors. This will reduce the power consumption to maintain the battery.” MTK-1006, 5:25-30; *see also* MTK-1006, 3:46-57, 4:21-32, 5:25-34, 6:15-25, 6:31-40, 12:39-42 (similar); MTK-1003, ¶¶227-228.

12. Claim 9

The Nicol-Borkar combination renders obvious wherein the integrated circuit is configured to have the supply voltage changed by regulation of a voltage provided to the at least one of the power islands from a source external to the integrated circuit. Borkar discloses embodiments where an external battery provides the supply voltage. “Referring to FIG. 2 ... computer system 140 includes a battery level detector 152 to detect the voltage level of a battery 156.” MTK-1006, 5:1-4, Fig. 2; *see also* MTK-1006, Figs. 4, 7, 7:36-59, 13:8-36; MTK-1003, ¶229. For example, Borkar explains that in the embodiment shown in Figure 2, battery level detector 152 provides a “battery level signal” to voltage and frequency control circuitry. MTK-1006, 5:1-6. A POSITA would have

understood that in these embodiments, Borkar uses power from the battery, which is a source external to the integrated circuit. MTK-1003, ¶229.

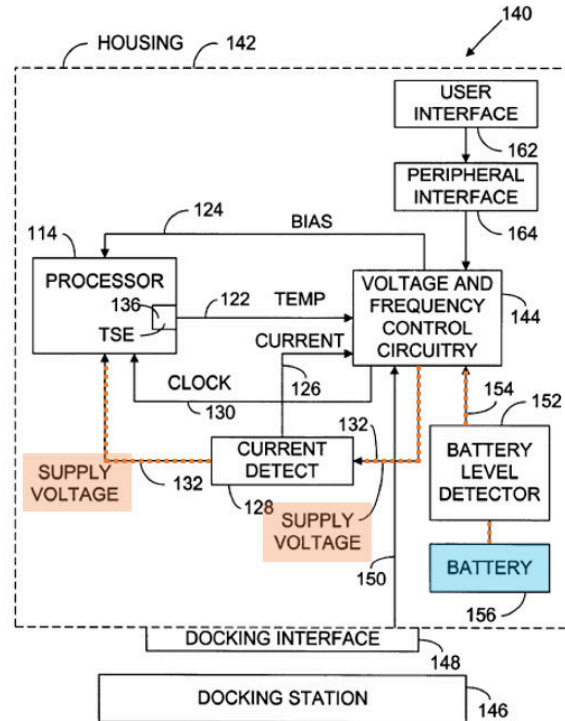


FIG. 2
MTK-1006, Fig. 2.

Further, Borkar explains that “[w]hen housing 142 is interfaced to docking station 146, *electrical power is being provided by an external source* rather than by battery 156.” MTK-1006, 5:53-55. Therefore, in addition to the supply voltage coming from the battery, which a POSITA would have understood to be external to the integrated circuit, Borkar discloses this additional “external source” when the device is interfaced to a docking station. MTK-1003, ¶230.

Both the voltage from the battery and the “external source” in Borkar are regulated to be changed. First, in some embodiments, the voltage passes through

“voltage and frequency control circuitry” which controls the supply voltage.

MTK-1006, 1:66-67 (“control circuitry may further control settings of a supply voltage signal.”), 11:58-60 (“the supply voltage signals may be the actual supply voltage Vcc (sometimes called Vdd) applied to the transistors.”), Fig. 3; MTK-1003, ¶231. Second, the voltage can also be regulated through “supply generating circuitry” which also controls the supply voltage. MTK-1006, 11:58-60, 13:57-60, Fig. 9; MTK-1003, ¶231.

13. Claim 10

The Nicol-Borkar combination renders obvious an internal regulator to perform the regulation. First, Borkar’s “voltage and frequency control circuitry” is an internal regulator that performs regulation of the supply voltage. MTK-1006, 1:66-67 (“control circuitry may further control settings of a supply voltage signal.”), 11:58-60 (“the supply voltage signals may be the actual supply voltage Vcc (sometimes called Vdd) applied to the transistors.”); MTK-1003, ¶232. As shown in Figure 3, voltage control circuitry 178 is internal to the integrated circuit. MTK-1006, Fig. 3, 7:5-7 (“Voltage control circuitry may be on the same chip, (e.g., chip 186) as is processor 174[.]”).

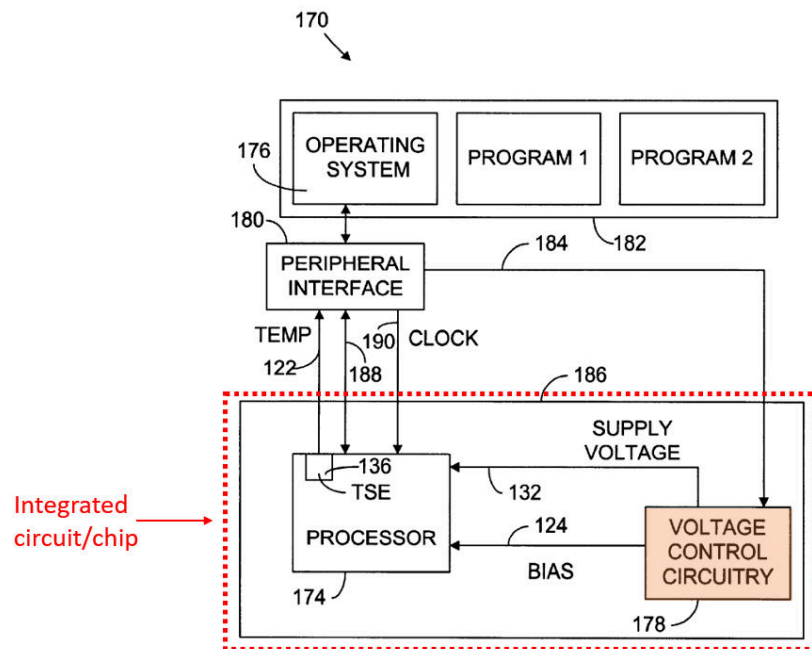


FIG. 3

MTK-1006, Fig. 3.

In addition, Borkar's Figure 9 shows "supply voltage generating circuitry 320 which provides one or more supply voltage signals in response to one or more supply voltage signals on conductor(s) 132 is included in processor 114." MTK-1006, 13:57-60. A POSITA would have understood that because the supply generating circuitry is included in processor 140, it is an internal voltage regulator that regulates the supply voltage. MTK-1003, ¶233.

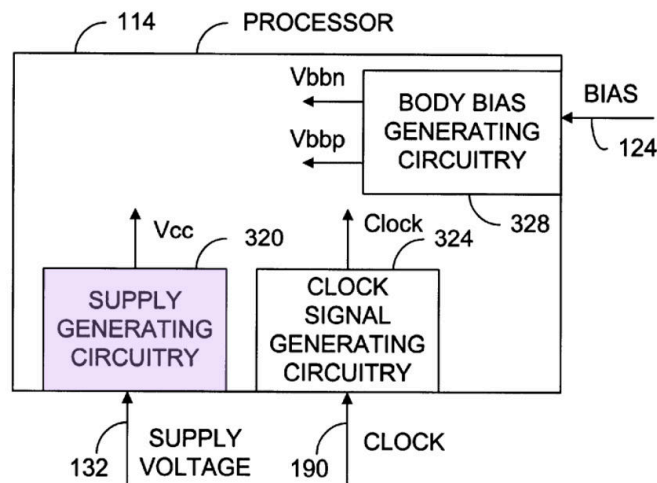
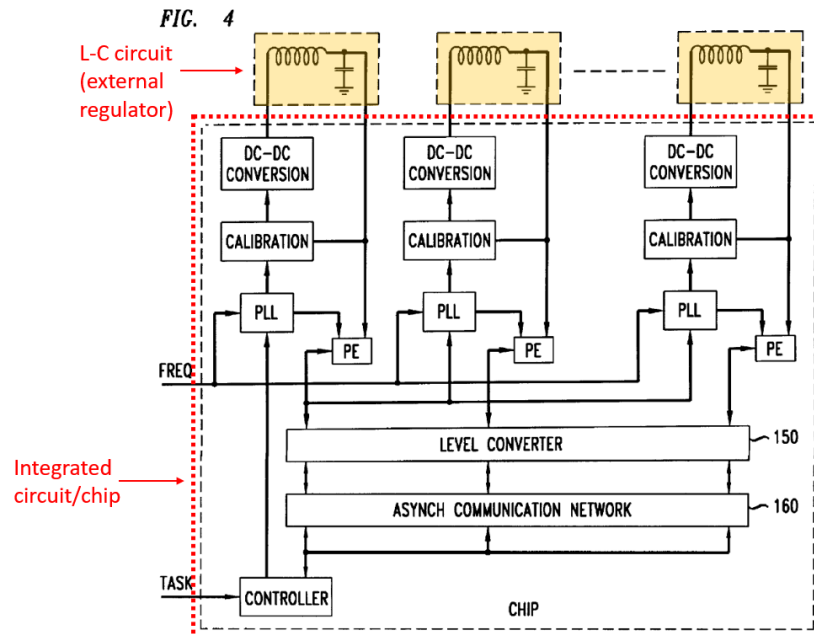


FIG. 9

MTK-1006, Figure 9.

14. Claim 11

The Nicol-Borkar combination renders obvious wherein the regulation is performed by an external regulator. Nicol discloses that “the operating system [] independently program[s] the lowest operating frequency and corresponding lowest supply voltage for each PE” and “[t]he supply voltage command is applied to dc-dc converter 130 followed by L-C circuit 140 to cause the combination of converter 130 and L-C circuit 140 to create the supply voltage $V_{dd-local}[]$ ” MTK-1008, 5:66-6:2, 4:31-32. Accordingly, Nicol discloses wherein regulation is performed by an external regulator. MTK-1003, ¶¶234-235.



MTK-1008, Fig. 4.

15. Claim 14

The Nicol-Borkar combination renders obvious wherein the integrated circuit is configured to have the one of plural threshold voltage selected by back biasing. As discussed for claim element 1[d], incorporated herein, Borkar discloses varying the threshold voltage of variable threshold transistors. Borkar discloses controlling the “transistor body bias” which refers to “the relationship between voltage of the source (V_{source}) of a field effect transistor (FET transistor) and voltage of the body (V_{bb}) of the FET transistor.” MTK-1006, 3:34-36; *see also* MTK-1006, 3:36-55; MTK-1003, ¶236. A POSITA would have understood that Borkar’s “body bias” includes “back biasing” of the ’811 patent because “body biasing” refers to applying a voltage to the body of a transistor, and “back

biasing” is a type of body biasing where the voltage is applied to the back side of a wafer. *See* MTK-1015, 680-681 (“Reverse biasing the ***back contact*** or bulk of a MOS transistor relative to the source is another method that has been employed to adjust the threshold potential. This electrical method of adjustment, which predates ion implantation, makes use of the so-called ***body effect*** or substrate-bias effect.”); MTK-1003, ¶236. To the extent that Borkar’s “body bias” does not explicitly disclose “back biasing,” it would have been obvious to a POSITA to implement back biasing as it is one of the basic modes of body biasing. MTK-1015, 680-681 MTK-1003, ¶236.

16. Claim 15

The Nicol-Borkar combination renders obvious wherein the integrated circuit comprises the power manager and the plurality of power islands. As discussed for claim elements 1[b] and 1[c], the Nicol-Borkar discloses an integrated circuit that comprises a power manager and plurality of power islands. MTK-1003, ¶237.

17. Claim 16

The Nicol-Borkar combination renders obvious wherein the power manager is configured to monitor one or more of the associated power consumptions using temperature or power dissipation measurement. In the combination, Borkar explicitly discloses that “control circuitry 118 ***monitors a temperature signal*** on

conductor(s) 122.” MTK-1006, 4:13-14, Figs. 1-4; *see also* MTK-1006, 4:14-56;
MTK-1003, ¶238.

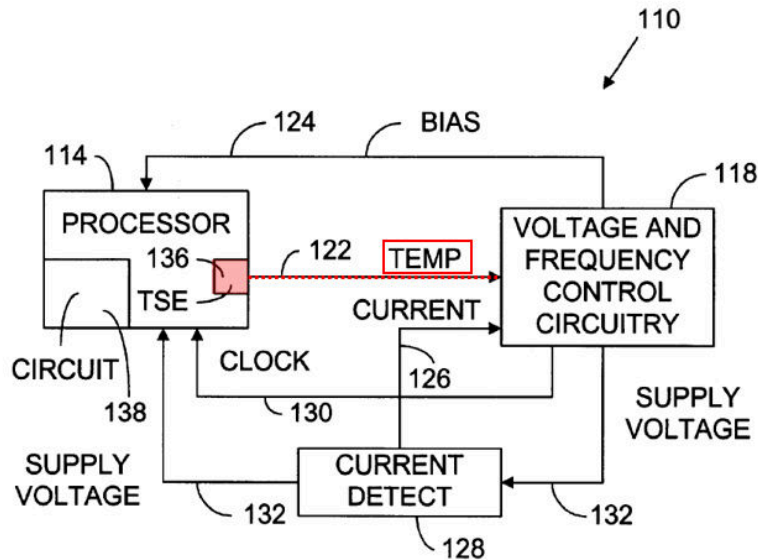


FIG. 1

MTK-1006, Fig. 1.

18. Claim 17

(a) 17[p]

Supra Ground 2A, claim 1[p]. MTK-1003, ¶239.

(b) 17[a]

Supra Ground 2A, claim 1[a]. MTK-1003, ¶240.

(c) 17[b]

Supra Ground 2A, claim 1[b]. MTK-1003, ¶241.

(d) 17[c]

Supra Ground 2A, claim 1[c]. MTK-1003, ¶242.

(e) 17[d]

Supra Ground 2A, claims 1, 6. MTK-1003, ¶243.

(f) 17[e]

Supra Ground 2A, claim 1[d]. MTK-1003, ¶244.

19. Claim 18

Supra Ground 2A, claims 2, 17. MTK-1003, ¶245.

20. Claim 19

The Nicol-Borkar combination renders obvious wherein the system is configured to permit a clock to be stopped during operation of the integrated circuit so that the power manager can control the associated power consumption of the at least one of the power islands. Nicol discloses “gated clocking techniques to ‘shut down’ PEs that are not needed.” MTK-1008, 5:42-44; MTK-1003, ¶246.

21. Claim 21

The Nicol-Borkar combination renders obvious wherein the system is configured to have a clock stopped by clock gating. Nicol discloses “gated clocking techniques to ‘*shut down*’ PEs that are not needed.” MTK-1008, 5:42-44; MTK-1003, ¶247.

22. Claim 22

Supra Ground 2A, claims 15, 17. MTK-1003, ¶248.

23. Claim 23

Supra Ground 2A, claims 16, 17. MTK-1003, ¶249.

24. Claim 24

(a) 24[p]

Supra Ground 2A, element 1[p]. MTK-1003, ¶250.

(b) 24[a]

Supra Ground 2A, element 1[a], 1[b], 1[c], claim 2. MTK-1003, ¶251.

(c) 24[b]

Supra Ground 2A, elements 1[d]. MTK-1003, ¶252.

25. Claim 25

Supra Ground 2A, claims 8, 24. MTK-1003, ¶253.

26. Claim 26

Supra Ground 2A, claims 9, 24. MTK-1003, ¶254.

27. Claim 28

Supra Ground 2A, claims 14, 24. MTK-1003, ¶255.

28. Claim 29

Supra Ground 2A, claims 16, 24. MTK-1003, ¶256.

29. Claim 30

(a) 30[p]

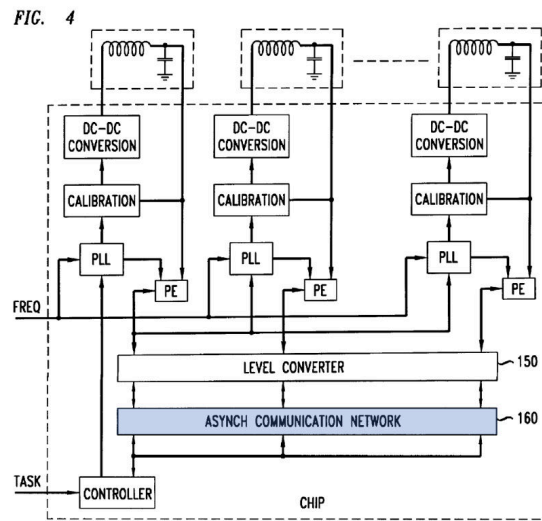
Supra Ground 2A, element 1[p]. MTK-1003, ¶257.

(b) 30[a]

Supra Ground 2A, element 1[a]. MTK-1003, ¶258.

(c) 30[b]

Supra Ground 2A, element 1[b]. MTK-1003, ¶259. The Nicol-Borkar combination further provides a first of the power islands being configured to communicate synchronously and asynchronously with a second of the power islands. Nicol discloses asynchronous communication between its PEs, which can operate at different frequencies. MTK-1008, 6:14-21; MTK-1003, ¶260. “[E]ach PE within the FIG. 4 arrangement is connection [*sic*] to an arrangement comprising elements 150. Level converter 150 converts the variable voltage swings of the PEs to a fixed level swing, and network 160 resolves the issue of different clock domains.” *See* MTK-1008, 6:29-33, Fig. 4. A POSITA would have understood that the PEs are communicating asynchronously because they are operating at different frequencies and voltages, necessitating the level converter and asynchronous communication network. MTK-1003, ¶260.



MTK-1008, Fig. 4.

To the extent it is argued that Nicol does not render obvious this claim, Borkar discloses and renders obvious this claim. Borkar discloses that some domains “may run off the same clock signal or otherwise need to run synchronously.” MTK-1006, 10:6-7. “Indeed, there can be reasons ...[that] groups of transistors that run off a different clock signal or that are asynchronous.” MTK-1006, 10:16-18. From this disclosure, a POSITA would have understood and found obvious that Borkar’s domains can communicate synchronously or asynchronously. MTK-1006, 10:6-18; MTK-1003, ¶261.

On the terms “synchronously” and “asynchronously,” Petitioner notes that in a prior litigation involving the ’811 patent, the court construed the term “synchronously” as “with coordination between components (i.e., power islands) before communication transmission begins,” “asynchronously” as “without coordination between components (i.e., power islands) before transmission

begins.” MTK-1011 at 45. For purposes of this Petition, Petitioner submits that there is no construction necessary because the plain and ordinary meaning suffices. MTK-1003, ¶262. However, the Nicol-Borkar combination also renders this element obvious under the prior court’s construction because Borkar describes domains that communicate synchronously (with coordination between components before transmission begins) and asynchronously (without coordination between components before transmission begins). MTK-1003, ¶262.

(d) 30[c]

Supra Ground 2A, element 1[c]. MTK-1003, ¶263.

(e) 30[d]

Supra Ground 2A, element 1[d]. MTK-1003, ¶264.

30. Claim 31

Supra Ground 2A, claims 2, 30. MTK-1003, ¶265.

31. Claim 32

Supra Ground 2A, claims 19, 30. MTK-1003, ¶266.

32. Claim 33

Supra Ground 2A, claims 9, 30. MTK-1003, ¶267.

33. Claim 34

Supra Ground 2A, claims 10, 33. MTK-1003, ¶268.

34. Claim 35

Supra Ground 2A, claims 11, 33. MTK-1003, ¶269.

35. Claim 38

Supra Ground 2A, claims 21, 30. MTK-1003, ¶270.

36. Claim 39

Supra Ground 2A, claims 4, 30. MTK-1003, ¶271.

37. Claim 40

Supra Ground 2A, claims 5, 39. MTK-1003, ¶272.

38. Claim 41

Supra Ground 2A, claims 6, 30. MTK-1003, ¶273.

39. Claim 42

Supra Ground 2A, claims 7, 41. MTK-1003, ¶274.

40. Claim 43

Supra Ground 2A, claims 15, 30. MTK-1003, ¶275.

41. Claim 44

Supra Ground 2A, claims 16, 30. MTK-1003, ¶276.

42. Claim 45

(a) 45[p]

Supra Ground 2A, element 1[p]. MTK-1003, ¶277.

(b) 45[a]

Supra Ground 2A, element 1[a]. MTK-1003, ¶278.

(c) 45[b]

Supra Ground 2A, element 1[b]. MTK-1003, ¶279.

(d) 45[c]

Supra Ground 2A, elements 1[b], 1[c]. MTK-1003, ¶280.

(e) 45[d]

Supra Ground 2A, element 1[d]. MTK-1003, ¶281.

43. Claim 46

Supra Ground 2A, claims 2, 31. MTK-1003, ¶282.

44. Claim 47

Supra Ground 2A, claims 3, 45. MTK-1003, ¶283.

45. Claim 48

Supra Ground 2A, claims 4, 45. MTK-1003, ¶284.

46. Claim 49

Supra Ground 2A, claims 5, 48. MTK-1003, ¶285.

47. Claim 50

Supra Ground 2A, claims 6, 45. MTK-1003, ¶286.

48. Claim 51

Supra Ground 2A, claims 7, 50. MTK-1003, ¶287.

49. Claim 52

Supra Ground 2A, claims 5, 45. MTK-1003, ¶288.

50. Claim 53

Supra Ground 2A, claims 9, 45. MTK-1003, ¶289.

51. Claim 54

Supra Ground 2A, claims 10, 53. MTK-1003, ¶290.

52. Claim 55

Supra Ground 2A, claims 11, 53. MTK-1003, ¶291.

53. Claim 58

Supra Ground 2A, claims 14, 45. MTK-1003, ¶292.

54. Claim 59

Supra Ground 2A, claims 15, 45. MTK-1003, ¶293.

55. Claim 60

Supra Ground 2A, claims 16, 45. MTK-1003, ¶294.

56. Claim 61

(a) 61[p]

Supra Ground 2A, claim 1[p]. MTK-1003, ¶295.

(b) 61[a]

Supra Ground 2A, claim 1[a]. MTK-1003, ¶296.

(c) 61[b]

Supra Ground 2A, claim 30[b]. MTK-1003, ¶297.

(d) 61[c]

Supra Ground 2A, claims 1[b], 1[c], 1[d]. MTK-1003, ¶298.

57. Claim 62

Supra Ground 2A, claims 2, 61. MTK-1003, ¶299.

58. Claim 63

Supra Ground 2A, claims 9, 61. MTK-1003, ¶300.

59. Claim 64

Supra Ground 2A, claims 10, 63. MTK-1003, ¶301.

60. Claim 65

Supra Ground 2A, claims 11, 63. MTK-1003, ¶302.

61. Claim 68

Supra Ground 2A, claims 21, 61. MTK-1003, ¶303.

62. Claim 69

Supra Ground 2A, claims 4, 61. MTK-1003, ¶304.

63. Claim 70

Supra Ground 2A, claims 5, 69. MTK-1003, ¶305.

64. Claim 71

Supra Ground 2A, claims 10, 61. MTK-1003, ¶306.

65. Claim 72

Supra Ground 2A, claims 7, 71. MTK-1003, ¶307.

66. Claim 73

Supra Ground 2A, claims 15, 61. MTK-1003, ¶308.

67. Claim 74

Supra Ground 2A, claims 16, 61. MTK-1003, ¶309.

E. GROUND 2B —Claims 12, 36, 56, 66 are obvious over Nicol-Borkar and Rincon-Mora

1. Overview of Rincon-Mora

Supra Ground 1B, Overview of Rincon-Mora. MTK-1003, ¶310.

2. The Nicol-Borkar-Rincon-Mora Combination

A POSITA would have been motivated to modify Nicol’s integrated circuit to incorporate the teachings of Rincon-Mora with reasonable expectation of success. Nicol, Borkar, and Rincon-Mora are in the same field of endeavor: integrated circuit applications, such as battery powered devices. MTK-1008, 2:18-22 (“Improved performance of multi-processor chips is achieved by dynamically controlling the processing load of chips...as to minimize overall power consumption.”); MTK-1006, 1:53-56 (“The switching rate can also lead to an increase in power consumption rate because more instructions can be executed in a shorter amount of time. This is particularly a problem with battery driven processor”); MTK-1007, 2:25-28 (“It is a further object of the present invention to provide such a voltage regulator circuit which is suitable for use in low power supply voltage applications, such as in battery-powered systems.”).

Thus, Rincon-Mora is pertinent art in the same field as Nicol and Borkar, and it would have been obvious to implement the teachings of Rincon-Mora in the Nicol-Borkar combination’s integrated circuit. MTK-1003, ¶312. A POSITA would have been motivated to incorporate Rincon-Mora’s low dropout regulator in

the Nicol-Borkar system to improve the stability and noise of the regulated voltage. MTK-1003, ¶312. For example, Rincon-Mora discloses that “[c]onventional DC-DC converter circuitry typically produces power supply voltages that are somewhat noisy, and that fluctuate to some extent.” MTK-1007, 10:44-46. A POSITA would have understood that Rincon-Mora’s low dropout voltage regulator would provide a low-noise and stable supply voltage for use in the Nicol-Borkar combination integrated circuit. MTK-1003, ¶312.

Further, Rincon-Mora discloses that the voltage regulator “is suitable for implementation as part of an overall larger integrated circuit or, alternatively, may be realized as a separate stand-alone integrated circuit.” MTK-1007, 3:2-5. It would have been obvious to use a low dropout voltage regulator to generate the variable supply voltage used in a variable power domain. MTK-1003, ¶313. A POSITA would have understood that the type of regulator used in a circuit, such as a low dropout voltage regulator, is merely a design choice. MTK-1003, ¶313.

3. Claim 12

The Nicol-Borkar-Rincon-Mora combination renders obvious a dropout voltage regulator to provide the supply voltage. Rincon-Mora discloses a “low drop-out (LDO) voltage regulator and system.” MTK-1007, Abstract. Further, Rincon-Mora discloses that the “voltage regulator circuit according to this embodiment of the invention also provides these advantages in a circuit which may

be efficiently implemented into an integrated circuit according to conventional technology, and is contemplated to be quite stable and robust in operation.” MTK-1007, 9:15-19. Therefore, a low drop-out voltage regulator such as that described in Rincon-Mora would have been efficiently and easily incorporated into an integrated circuit like the Nicol-Borkar system, specifically to operate with Nicol’s voltage circuitry to provide the voltage supply to the SOC. MTK-1008, Fig. 4; MTK-1003, ¶314.

4. Claim 36

Supra Ground 2B, claims 12, 33. MTK-1003, ¶315.

5. Claim 56

Supra Ground 2B, claims 12, 53. MTK-1003, ¶316.

6. Claim 66

Supra Ground 2B, claims 12, 63. MTK-1003, ¶317.

F. GROUND 2C – Claims 13, 20, 27, 37, 57, 67 are obvious over Nicol-Borkar and Iyengar

1. Overview of Iyengar

Supra Ground 1C, Overview of Iyengar. MTK-1003, ¶318.

2. The Nicol-Borkar-Iyengar Combination

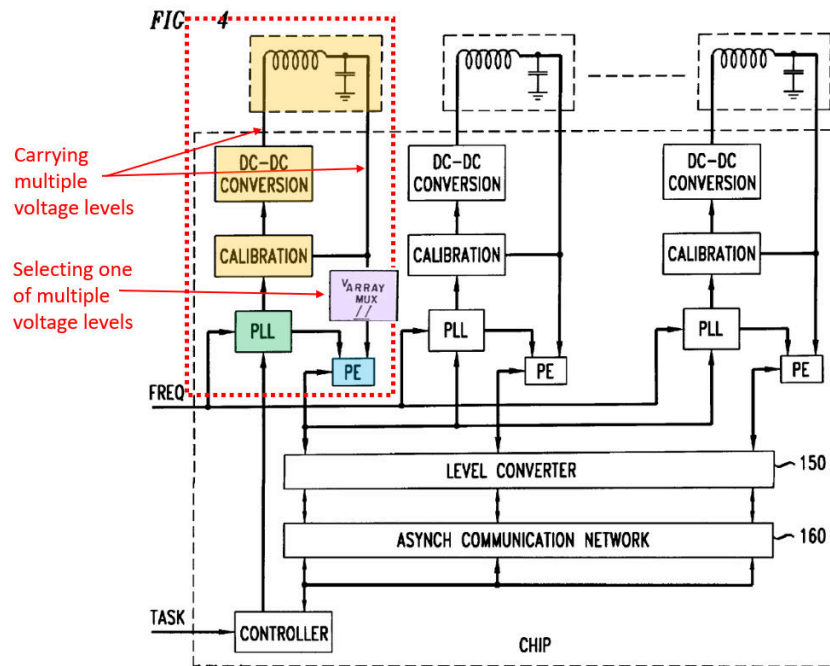
A POSITA would have been motivated to modify the Nicol-Borkar system to incorporate the teachings of Iyengar with reasonable expectation of success. Nicol, Borkar, and Iyengar are in the same field of endeavor: integrated circuit

applications, such as battery powered devices. MTK-1008, Abstract (“This invention relates to electronic circuits and, more particularly to power consumption within electronic circuits.”); MTK-1006, 1:53-56 (“The switching rate can also lead to an increase in power consumption rate because more instructions can be executed in a shorter amount of time. This is particularly a problem with battery driven processor”); MTK-1022, 1:11-13 (“This invention is in the field of integrated circuits and is more specifically directed to on-chip power supply control.”).

Thus, Iyengar is pertinent art in the same field as Nicol and Borkar, and it would have been obvious to implement the teachings of Iyengar in the Nicol-Borkar combination’s integrated circuit. For example, Iyengar explains that due to the increasing complexity and density of circuit design, “the power supply voltages applied to such high density VLSI devices including dRAMs, other memories, and logic devices, are preferably reduced[.]” MTK-1022, 1:65-2:1; MTK-1003, ¶320. In its proposed solution, Iyengar provides an embodiment with two multiplexers, V_{ARRAY} multiplexer and V_{PERI} multiplexer, which choose the appropriate voltage signal for the array and peripheral circuitry, respectively, based on control signals. MTK-1022, 6:18-26. A POSITA would have been motivated to implement a similar multiplexer in the Nicol-Borkar system, for example to provide the dynamic voltage to the PEs. MTK-1008, 4:54-5:2, Fig. 3; MTK-1003, ¶320.

3. Claim 13

The Nicol-Borkar-Iyengar combination renders obvious wherein the integrated circuit is configured to have the supply voltage controlled by Vdd multiplexing in relation to the at least one of the power islands. A POSITA would have been motivated to incorporate Iyengar's voltage multiplexer in the Nicol-Borkar system to provide the variable voltage. For example, the Nicol DC/DC converter would have been configured to provide multiple Vdd levels (similar to the discussion of multiple independent power supply pins in the DC/DC converter in the '811 patent, MTK-1001, 8:45-49, Fig. 7), which would be stabilized through the L-C circuit, and a multiplexer such as that in Iyengar would have been used to select among those different voltage levels. Employing a multiplexer in this way to allow for varying voltage supply would have been a simple design choice. MTK-1003, ¶321.



MTK-1008, Fig. 4 (modified with Iyengar's multiplexer).

4. Claim 20

Supra Ground 2C, claims 13, 17. MTK-1003, ¶322.

5. Claim 27

Supra Ground 2C, claims 13, 24. MTK-1003, ¶323.

6. Claim 37

Supra Ground 2C, claims 13, 30. MTK-1003, ¶324.

7. Claim 57

Supra Ground 2C, claims 13, 45. MTK-1003, ¶325.

8. Claim 67

Supra Ground 2C, claims 13, 61. MTK-1003, ¶326.

IV. THE BOARD SHOULD CONSIDER THE PETITION ON THE MERITS AND NOT EXERCISE ITS DISCRETION TO DENY INSTITUTION

A. Discretionary denial under §325(d) is not warranted

Advanced Bionics and the *Becton* factors strongly favor institution.

Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential); *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential as to Section III.C.5, first paragraph).

This Petition presents new prior art and arguments for which there is no indication in the file history that the Office ever previously considered in connection with the '811 patent. While Nowka (MTK-1004) and Nicol (MTK-1008) appear on the face of the '811 patent, the Examiner never substantively addressed it during prosecution. Indeed, the Examiner never issued a rejection over any prior art reference. Furthermore, Nowka was never considered in combination with Borkar (MTK-1006), which was not before the Examiner during prosecution.

The '811 patent's prosecution did not involve negotiation between the applicant and the Examiner regarding the teachings of the prior art applied in the instant Petition, thus, exercise of the Board's discretion under § 325(d) is unwarranted. *See* IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential)

(citing IPR2017-01586 Pap. 8 (PTAB Dec. 15, 2017) (precedential)).

B. Discretionary Denial under Section 314(a) Is Not Warranted

Given this is the first ever petition to be filed against the '811 Patent, the *General Plastic* factors do not apply. *General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357—01361, Paper 19 (PTAB Sept. 6, 2017) (precedential)

C. The *Fintiv* Factors Weigh Against Exercising Discretion To Deny Institution

The PTAB considers a set of non-exclusive factors (the *Fintiv* factors) in determining whether to institute an IPR proceeding where there is parallel district court litigation. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (designated precedential May 5, 2020). On June 21, 2022, Director Vidal issued “binding agency guidance” entitled “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation.” MTK-1013 (hereinafter the “Interim Guidance”). This Interim Guidance presents “several clarifications... to the PTAB’s... application of *Fintiv* to discretionary institution where there is parallel litigation.” *Id.*, 2.

One clarification provided by the Interim Guidance specifies the effect of particular types of stipulations presented by petitioners on the Board’s application of the *Fintiv* framework. *Id.*, 3, 7-8. In particular, the Interim Guidance

unequivocally states that “*the PTAB will not discretionarily deny institution* of an IPR or PGR in view of parallel district court litigation where a petitioner stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition.” *Id.*, 7 (emphasis added) (citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020)). In the present case, Petitioner presents a stipulation not to pursue in the parallel district court proceeding the same grounds as in the present Petition or any grounds that could have reasonably been raised in the present Petition. *See* MTK-1014. Accordingly, based on the Interim Guidance, institution of the present Petition *should not* be discretionarily denied in view of the parallel district court proceeding. *See* MTK-1013, 7.

V. CONCLUSION

As demonstrated herein, the Challenged Claims are unpatentable. Accordingly, Petitioner respectfully requests that the Board institute IPR.

VI. PAYMENT OF FEES

Petitioner authorizes charge of fees to Deposit Account 06-1050.

VII. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

MediaTek Inc. is petitioner and real party-in-interest. MediaTek USA Inc. is an additional real party-in-interest. No other parties had access to or control over

the present Petition, and no other parties funded the present Petition.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

Petitioner is not aware of any disclaimers or reexamination certificates regarding the '811 Patent. MOSAID—the alleged Patent Owner—filed a complaint asserting the '811 Patent against Petitioner on March 28, 2023 in the U.S. District Court for the Eastern District of Texas (Civil Action No. 2:23-CV-00129-JRG). The '811 Patent was asserted in four district court infringement actions (*Mosaid Technologies Inc. v. Freescale Semiconductor, Inc.*, Case. No. 6:11-cv-00173 (Apr. 8, 2011, E.D. Tex.); *MOSAID Technologies Inc. v. Xilinx, Inc.*, Case. No. 6:12-cv-00847 (Nov. 5, 2012, E.D. Tex.); *MOSAID Technologies Inc. v. ST-Ericsson, Inc.*, Case. No. 6:12-cv-00845 (Nov. 5, 2012, E.D. Tex.)); *Conversant Intellectual Property Management Inc. v. Samsung Electronics Co., Ltd., et al*, Case No. 2:15-cv-00281 (Feb. 26, 2015) (E.D. Tex.) and subject to one declaratory judgment action (*ARM Ltd. v. MOSAID Technologies, Inc.*, Case No. 3:11-cv-03869 (Aug. 5, 2011, N.D. Cal.), transferred to *ARM Ltd. v. MOSAID Technologies, Inc.*, Case No. 6:12-cv-00008 (Jan. 9, 2012, E.D. Tex), which were all voluntarily dismissed based on settlement.

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

Lead Counsel	Backup counsel
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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR44508-0023IP4@fr.com.

Respectfully submitted,

Dated: March 25, 2024

/Timothy W. Riffe/

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,387 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: March 25, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on March 25, 2024, a complete and entire copy of this Petition for *Inter partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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