AO 120 (Rev. 3/04)

TO:	Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following ☑ Patents or ☐ Trademarks:

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:15-cv-281	2/26/2015	Eastern District of Texas

PLAINTIFF	DEFENDANT
Conversant Intellectual Property Management, Inc. et al	Samsung Electronics Co., Ltd., et al

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,223,331	4/24/2001	Conversant Intellectual Property Management, Inc.
2	7,915,933	3/29/2011	Conversant Intellectual Property Management, Inc.
3	7,940,081	5/10/2011	Conversant Intellectual Property Management, Inc.
4	7,945,885	5/17/2011	Conversant Intellectual Property Management, Inc.
5	7,982,532	7/19/2011	Conversant Intellectual Property Management, Inc.

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,996,811	8/9/2011	Conversant Intellectual Property Management, Inc.
2	8,253,438	8/28/2012	Conversant Intellectual Property Management, Inc.
3	RE44,218	5/14/2013	Conversant IP NB 868 Inc.
4	5,796,675	8/18/1998	Conversant IP NB 868 Inc.
5	6,107,138	8/22/2000	Conversant IP NB 868 Inc.

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 3/04)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following ☑ Patents or ☐ Trademarks:

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:15-cv-281	2/26/2015	Eastern District of Texas

PLAINTIFF	DEFENDANT
Conversant Intellectual Property Management, Inc. et al	Samsung Electronics Co., Ltd., et al

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	6,209,056	3/27/2001	Conversant IP NB 868 Inc.
2	6,306,743	10/23/2001	Conversant IP NB 868 Inc.
3	6,313,029	11/6/2001	Conversant IP NB 868 Inc.
4	6,943,602	9/13/2005	Conversant IP NB 868 Inc.
5	7,101,791	9/5/2006	Conversant IP NB 868 Inc.

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court for the Eastern District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:11-cv-173	4/7/2011	for the Eastern District of Texas

PLAINTIFF	DEFENDANT
MOSAID TECHNOLOGIES, INC.	FREESCALE SEMICONDUCTOR, INC. ET AL.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1			
2			
3			
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☑ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading		
8/15/2011			
	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	7,945,885 B2	5/17/2011	MOSAID TECHNOLOGIES, INC.
2	7,996,811 B2	8/9/2011	MOSAID TECHNOLOGIES, INC.
3			
4			
5			

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director **Copy 3—Upon termination of action, mail this copy to Director**
Copy 2—Upon filing document adding patent(s), mail this copy to Director **Copy 4—Case file copy**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/176,645	05/17/2011	7945885	2037.2079-010	3003

21005 7590 04/27/2011

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 397 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Barry Alan HOBERMAN, Cupertino, CA;
Daniel L. HILLMAN, San Jose, CA;
Jon SHIELL, San Jose, CA;

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

21005 7590 03/31/2011
HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/176,645	07/21/2008	Barry Alan HOBERMAN	2037.2079-010	3003

TITLE OF INVENTION: POWER MANAGERS FOR AN INTEGRATED CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$0	$0	$1510	$0	06/30/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
LIN, SUN J	2825	716-133000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Hamilton, Brook, Smith & Reynolds, P.C.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: MOSAID Technologies Incorporated

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Ottawa, Ontario, Canada

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 08-0380 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 4/6/11

Typed or printed name James M. Smith Registration No. 28,043

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2825
Filed:	July 21, 2008	Examiner:	Lin, Sun J.
Confirmation No:	3003		
For:	Power Managers For An Integrated Circuit		

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or is being facsimile transmitted to the United States Patent and Trademark Office on:

_____ _____
Date Signature

_____
Typed or printed name of person signing certificate

IDENTIFICATION OF LITIGATION

Mail Stop: ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

United States Patents 7,051,306 and 7,415,680, to which the present application claims priority, are the subject of Mosaid Technologies Inc. v. Freescale Semiconductor, Inc., Interphase Corporation, and Nvidia Corporation, filed in the United States District Court for the Eastern District of Texas, Tyler Division on April 7, 2011. A copy of the Complaint is attached.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By /James M. Smith, Reg. No. 28,043/
James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Date: April 7, 2011

IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
TYLER DIVISION

MOSAID TECHNOLOGIES INC.,	§	
	§	
Plaintiff,	§	
	§	
v.	§	Civil Action No. _____
	§	
FREESCALE SEMICONDUCTOR, INC.,	§	JURY TRIAL DEMANDED
INTERPHASE CORPORATION, and	§	
NVIDIA CORPORATION,	§	
	§	
Defendants.	§	

ORIGINAL COMPLAINT

Plaintiff MOSAID Technologies Inc. ("MOSAID") brings this action for patent infringement and alleges as follows:

THE PARTIES

1. Plaintiff MOSAID is a Canadian corporation, with its principal place of business at 11 Hines Road, Suite 203, Ottawa, Ontario K2K 2X1, Canada. Plaintiff MOSAID's United States principal place of business is located at 101 E. Park Blvd., Suite 600, Plano, Texas 75074.

2. Defendant Freescale Semiconductor, Inc. ("Freescale") is a Delaware corporation with its principal place of business at 6501 William Cannon Drive West, Austin, Texas 78735.

3. Defendant Interphase Corporation ("Interphase") is a Texas corporation with its principal place of business at 2901 North Dallas Parkway, Suite 200, Plano, Texas 75093.

4. Defendant NVIDIA Corporation ("NVIDIA") is a Delaware corporation with its principal place of business at 2701 San Tomas Expressway, Santa Clara, California 95050.

JURISDICTION

5. This Court has subject matter jurisdiction over this dispute under 28 U.S.C. §§ 1331 and 1338(a).

6. This Court has personal jurisdiction over Defendants Freescale, Interphase, and NVIDIA, which have conducted and continue to conduct business in the State of Texas and in this Judicial District. Defendants Freescale, Interphase, and NVIDIA directly and/or through intermediaries make, offer for sale, sell, and/or advertise (including through a website) products and services in the State of Texas and in this Judicial District. Defendants Freescale, Interphase, and NVIDIA committed acts of patent infringement alleged herein within the State of Texas and, more particularly, within this Judicial District. Defendants Freescale, Interphase, and NVIDIA purposefully and voluntarily placed their infringing products into the stream of commerce with the expectation that they will be purchased by consumers in the State of Texas and in this Judicial District. These infringing products have been and continue to be purchased by consumers in the State of Texas and in this Judicial District.

VENUE

7. Venue is proper in this Judicial District under 28 U.S.C. §§ 1391(b) and 1400(b) because acts and transactions constituting at least a subset of the violations alleged herein occurred in this Judicial District and/or because one or more of Defendants Freescale, Interphase, and NVIDIA transact business in this Judicial District. Venue is also proper in this Judicial District under 28 U.S.C. § 1391(c) because Defendants Freescale, Interphase, and NVIDIA are subject to personal jurisdiction in this District.

ASSERTED PATENTS

8. On May 23, 2006, United States Patent No. 7,051,306 (the "'306 Patent," entitled "Managing Power on Integrated Circuits Using Power Islands") duly and legally issued. The '306 Patent relates to, among other things, power consumption management in integrated circuits. MOSAID is the owner of the '306 Patent and has all rights to enforce the '306 Patent with respect to the Defendants. A copy of the '306 Patent is attached as Exhibit A.

9. On August 19, 2008, United States Patent No. 7,415,680 (the "'680 Patent," entitled "Power Managers for an Integrated Circuit") duly and legally issued. The '680 Patent relates to, among other things, power consumption management in integrated circuits. MOSAID is the owner of the '680 Patent and has all rights to enforce the '680 Patent with respect to the Defendants. A copy of the '680 Patent is attached as Exhibit B.

10. On November 19, 1996, United States Patent No. 5,577,230 (the "'230 Patent," entitled "Apparatus and Method for Computer Processing Using an Enhanced Harvard Architecture Utilizing Dual Memory Buses and the Arbitration for Data/Instruction Fetch") duly and legally issued. The '230 Patent relates to, among other things, computer processors and memory architectures. MOSAID is the exclusive licensee of the '230 Patent and is the current owner of all rights to enforce the '230 Patent with respect to the Defendants. A copy of the '230 Patent is attached as Exhibit C.

11. On March 3, 1998, United States Patent No. 5,724,505 (the "'505 Patent," entitled "Apparatus and Method for Real-Time Program Monitoring via a Serial Interface") duly and legally issued. The '505 Patent relates to, among other things, monitoring computer program execution in microprocessor devices. MOSAID is the exclusive licensee of the '505 Patent and

is the current owner of all rights to enforce the '505 Patent with respect to the Defendants. A copy of the '505 Patent is attached as Exhibit D.

12. On September 28, 1999, United States Patent No. 5,958,036 (the "'036 Patent," entitled "Circuit for Arbitrating Interrupts with Programmable Priority Levels") duly and legally issued. The '036 Patent relates to, among other things, interrupt priority arbitration in computer devices. MOSAID is the exclusive licensee of the '036 Patent and is the current owner of all rights to enforce the '036 Patent with respect to the Defendants. A copy of the '036 Patent is attached as Exhibit E.

13. On October 31, 2000, United States Patent No. 6,141,762 (the "'762 Patent," entitled "Power Reduction in a Multiprocessor Digital Signal Processor based on Processor Load") duly and legally issued. The '762 Patent relates to, among other things, power consumption within electronic circuits. MOSAID is the exclusive licensee of the '762 Patent and is the current owner of all rights to enforce the '762 Patent with respect to the Defendants. A copy of the '762 Patent is attached as Exhibit F.

14. On July 3, 2001, United States Patent No. 6,256,725 (the "'725 Patent," entitled "Shared Datapath Processor Utilizing Stack-Based and Register-Based Storage Spaces") duly and legally issued. The '725 Patent relates to, among other things, computer processor architectures. MOSAID is the exclusive licensee of the '725 Patent and is the current owner of all rights to enforce the '725 Patent with respect to the Defendants. A copy of the '725 Patent is attached as Exhibit G. The '306 Patent, '680 Patent, '230 Patent, '505 Patent, '036 Patent, '762 Patent, and '725 Patent are collectively referred to as the "Asserted Patents."

GENERAL ALLEGATIONS

15. Defendants Freescale, Interphase, and NVIDIA have directly infringed and continue to directly infringe one or more of the Asserted Patents by making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the Asserted Patents. The infringing devices include, but are not limited to, processors, mobile products, microcontrollers, communications equipment, and system-on-chip devices.

16. Defendants Freescale, Interphase, and NVIDIA have indirectly infringed and continue to indirectly infringe one or more of the Asserted Patents by contributing to and actively inducing infringement of one or more of the claims of the Asserted Patents. Defendants Freescale, Interphase, and NVIDIA have notice of the Asserted Patents. The infringing devices are known by Defendants Freescale, Interphase, and NVIDIA to be especially made or especially adapted for use in an infringement of one or more of the Asserted Patents, and are not staple articles or commodities of commerce suitable for substantial noninfringing uses. Defendants Freescale, Interphase, and NVIDIA contribute to the infringement of one or more of the Asserted Patents by selling or importing the infringing devices to third parties, such as end-users, resellers, partners, and distributors who incorporate the infringing devices into their products and/or practice one or more claims of the Asserted Patents. Defendants Freescale, Interphase, and NVIDIA actively induce infringement by encouraging the use of the infringing devices by the third parties in ways that infringe one or more of the claims of the Asserted Patents. Defendants Freescale, Interphase, and NVIDIA knew or should have known that such encouragement would induce infringement. Such induced and/or contributory infringement has occurred at least since Defendants Freescale, Interphase, and NVIDIA became aware of the Asserted Patents.

17. As a result, Defendants Freescale, Interphase, and NVIDIA have been and still are infringing one or more of the claims of the Asserted Patents as defined by 35 U.S.C. § 271. MOSAID has suffered damage by reason of such infringement and will continue to suffer additional damage until this Court enjoins the infringing conduct.

18. Defendants Freescale, Interphase, and NVIDIA have continued their infringing activities after receiving notice of the Asserted Patents and, therefore, such infringement is willful, entitling MOSAID to the recovery of increased damages under 35 U.S.C. § 284.

19. Infringement of one or more of the Asserted Patents by Defendants Freescale, Interphase, and NVIDIA is an "exceptional case" justifying an award of attorneys' fees and costs to MOSAID under 35 U.S.C. § 285.

20. MOSAID believes that Defendants Freescale, Interphase, and NVIDIA will continue to infringe one or more of the Asserted Patents unless enjoined by this Court. Such infringing activity causes MOSAID irreparable harm and will continue to cause such harm without the issuance of an injunction.

COUNT ONE
Freescale's Infringement of the '306 Patent

21. MOSAID incorporates by reference each of the foregoing paragraphs of this Complaint as though fully set forth herein.

22. Defendant Freescale has been and is still directly infringing one or more of the claims of the '306 Patent. Defendant Freescale's infringing acts include, but are not limited to, making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the '306 Patent, such as processors and microcontrollers, including but not limited to one or more of the i.MX series of processors and the MPC560xx series of microcontrollers, including the i.MX37 Multimedia Applications Processor and the MPC5606S Microcontroller.

Defendant Freescale has been and is still contributing to the infringement of and/or actively inducing third parties, such as end users, that directly infringe one or more of the claims of the '306 Patent. Defendant Freescale's actions are in violation of one or more of the provisions of 35 U.S.C. § 271(a), (b), (c), (f), and (g).

COUNT TWO
Freescale's Infringement of the '230 Patent

23. MOSAID incorporates by reference each of the foregoing paragraphs of this Complaint as though fully set forth herein.

24. Defendant Freescale has been and is still directly infringing one or more of the claims of the '230 Patent. Defendant Freescale's infringing acts include, but are not limited to, making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the '230 Patent, such as processors, mobile products, and microcontrollers, including but not limited to one or more of the i.MX series of processors, the MXC series of mobile products, and the MPC551x series of microcontrollers, including the i.MX31 Multimedia Applications Processor, the i.MX31L Multimedia Applications Processor, the MXC300-30 Mobile Extreme Convergence product, and the MPC5510 Microcontroller. Defendant Freescale has been and is still contributing to the infringement of and/or actively inducing third parties, such as end users, that directly infringe one or more of the claims of the '230 Patent. Defendant Freescale's actions are in violation of one or more of the provisions of 35 U.S.C. § 271(a), (b), (c), (f), and (g).

COUNT THREE
Freescale's Infringement of the '505 Patent

25. MOSAID incorporates by reference each of the foregoing paragraphs of this Complaint as though fully set forth herein.

26. Defendant Freescale has been and is still directly infringing one or more of the claims of the '505 Patent. Defendant Freescale's infringing acts include, but are not limited to, making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the '505 Patent, such as processors, mobile products, and microcontrollers, including but not limited to one or more of the i.MX series of processors, the MXC series of mobile products, the MPC551x series of microcontrollers, and the Kinetis series of microcontrollers, including the i.MX31 Multimedia Applications Processor, the i.MX31L Multimedia Applications Processor, the i.MX 6 Multimedia Applications Processor, the MXC300-30 Mobile Extreme Convergence product, the MPC5510 Microcontroller, and the Kinetis K10, K20, K30, K40, and K60 Microcontrollers. Defendant Freescale has been and is still contributing to the infringement of and/or actively inducing third parties, such as end users, that directly infringe one or more of the claims of the '505 Patent. Defendant Freescale's actions are in violation of one or more of the provisions of 35 U.S.C. § 271(a), (b), (c), (f), and (g).

COUNT FOUR
Freescale's Infringement of the '036 Patent

27. MOSAID incorporates by reference each of the foregoing paragraphs of this Complaint as though fully set forth herein.

28. Defendant Freescale has been and is still directly infringing one or more of the claims of the '036 Patent. Defendant Freescale's infringing acts include, but are not limited to, making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the '036 Patent, such as processors and microcontrollers, including but not limited to one or more of the MPC8xxx series of processors, the MPC56xxx series of microcontrollers, the i.MX series of processors, and the Kinetis series of microcontrollers, including the MPC8260 Processor, the MPC5606S Microcontroller, the i.MX 6 Multimedia Applications Processor, and

the Kinetis K10, K20, K30, K40, and K60 Microcontrollers. Defendant Freescale has been and is still contributing to the infringement of and/or actively inducing third parties, such as end users, that directly infringe one or more of the claims of the '036 Patent. Defendant Freescale's actions are in violation of one or more of the provisions of 35 U.S.C. § 271(a), (b), (c), (f), and (g).

COUNT FIVE
Freescale's Infringement of the '762 Patent

29. MOSAID incorporates by reference each of the foregoing paragraphs of this Complaint as though fully set forth herein.

30. Defendant Freescale has been and is still directly infringing one or more of the claims of the '762 Patent. Defendant Freescale's infringing acts include, but are not limited to, making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the '762 Patent, such as processors, including but not limited to one or more of the i.MX series of processors, including the i.MX31 Multimedia Applications Processor, the i.MX31L Multimedia Applications Processor, the i.MX35 Multimedia Applications Processor, and the i.MX37 Multimedia Applications Processor. Defendant Freescale has been and is still contributing to the infringement of and/or actively inducing third parties, such as end users, that directly infringe one or more of the claims of the '762 Patent. Defendant Freescale's actions are in violation of one or more of the provisions of 35 U.S.C. § 271(a), (b), (c), (f), and (g).

COUNT SIX
Freescale's Infringement of the '725 Patent

31. MOSAID incorporates by reference each of the foregoing paragraphs of this Complaint as though fully set forth herein.

32. Defendant Freescale has been and is still directly infringing one or more of the claims of the '725 Patent. Defendant Freescale's infringing acts include, but are not limited to,

making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the '725 Patent, such as processors and system-on-chip devices, including but not limited to one or more of the i.MX series of processors and the STMP37xx series of system-on-chip devices, including the i.MX21 Multimedia Applications Processor, the i.MX21S Multimedia Applications Processor, the i.MX27 Multimedia Applications Processor, the i.MX27L Multimedia Applications Processor, the i.MX31 Multimedia Applications Processor, the i.MX31L Multimedia Applications Processor, the i.MX37 Multimedia Applications Processor, the STMP3700 System-on-Chip, and the STMP3738 System-on-Chip. Defendant Freescale has been and is still contributing to the infringement of and/or actively inducing third parties, such as end users, that directly infringe one or more of the claims of the '725 Patent. Defendant Freescale's actions are in violation of one or more of the provisions of 35 U.S.C. § 271(a), (b), (c), (f), and (g).

COUNT SEVEN
NVIDIA's Infringement of the '306 Patent

33. MOSAID incorporates by reference each of the foregoing paragraphs of this Complaint as though fully set forth herein.

34. Defendant NVIDIA has been and is still directly infringing one or more of the claims of the '306 Patent. Defendant NVIDIA's infringing acts include, but are not limited to, making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the '306 Patent, such as processors, including but not limited to one or more of the GeForce series of processors, including the GeForce 9400MG processor. Defendant NVIDIA has been and is still contributing to the infringement of and/or actively inducing third parties, such as end users, that directly infringe one or more of the claims of the '306 Patent. Defendant

NVIDIA's actions are in violation of one or more of the provisions of 35 U.S.C. § 271(a), (b), (c), (f), and (g).

COUNT EIGHT
NVIDIA's Infringement of the '680 Patent

35. MOSAID incorporates by reference each of the foregoing paragraphs of this Complaint as though fully set forth herein.

36. Defendant NVIDIA has been and is still directly infringing one or more of the claims of the '680 Patent. Defendant NVIDIA's infringing acts include, but are not limited to, making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the '680 Patent, such as processors, including but not limited to one or more of the GeForce series of processors, including the GeForce GT240 processor and the GeForce GT330M processor. Defendant NVIDIA has been and is still contributing to the infringement of and/or actively inducing third parties, such as end users, that directly infringe one or more of the claims of the '680 Patent. Defendant NVIDIA's actions are in violation of one or more of the provisions of 35 U.S.C. § 271(a), (b), (c), (f), and (g).

COUNT NINE
NVIDIA's Infringement of the '230 Patent

37. MOSAID incorporates by reference each of the foregoing paragraphs of this Complaint as though fully set forth herein.

38. Defendant NVIDIA has been and is still directly infringing one or more of the claims of the '230 Patent. Defendant NVIDIA's infringing acts include, but are not limited to, making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the '230 Patent, such as processors, including but not limited to one or more of the GoForce and Tegra series of processors, including the GoForce 6100 and Tegra APX processors. Defendant NVIDIA has been and is still contributing to the infringement of and/or actively

inducing third parties, such as end users, that directly infringe one or more of the claims of the '230 Patent. Defendant NVIDIA's actions are in violation of one or more of the provisions of 35 U.S.C. § 271(a), (b), (c), (f), and (g).

COUNT TEN
NVIDIA's Infringement of the '505 Patent

39. MOSAID incorporates by reference each of the foregoing paragraphs of this Complaint as though fully set forth herein.

40. Defendant NVIDIA has been and is still directly infringing one or more of the claims of the '505 Patent. Defendant NVIDIA's infringing acts include, but are not limited to, making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the '505 Patent, such as processors, including but not limited to one or more of the Tegra series of processors, including the Tegra 2 processor. Defendant NVIDIA has been and is still contributing to the infringement of and/or actively inducing third parties, such as end users, that directly infringe one or more of the claims of the '505 Patent. Defendant NVIDIA's actions are in violation of one or more of the provisions of 35 U.S.C. § 271(a), (b), (c), (f), and (g).

COUNT ELEVEN
NVIDIA's Infringement of the '036 Patent

41. MOSAID incorporates by reference each of the foregoing paragraphs of this Complaint as though fully set forth herein.

42. Defendant NVIDIA has been and is still directly infringing one or more of the claims of the '036 Patent. Defendant NVIDIA's infringing acts include, but are not limited to, making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the '036 Patent, such as processors, including but not limited to one or more of the Tegra series of processors, including the Tegra 2 processor. Defendant NVIDIA has been and is still contributing to the infringement of and/or actively inducing third parties, such as end users,

that directly infringe one or more of the claims of the '036 Patent. Defendant NVIDIA's actions are in violation of one or more of the provisions of 35 U.S.C. § 271(a), (b), (c), (f), and (g).

COUNT TWELVE
NVIDIA's Infringement of the '762 Patent

43. MOSAID incorporates by reference each of the foregoing paragraphs of this Complaint as though fully set forth herein.

44. Defendant NVIDIA has been and is still directly infringing one or more of the claims of the '762 Patent. Defendant NVIDIA's infringing acts include, but are not limited to, making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the '762 Patent, such as processors, including but not limited to one or more of the GeForce series of processors, including the GeForce 8M processor, the GeForce GT240 processor, and the GeForce GT330M processor. Defendant NVIDIA has been and is still contributing to the infringement of and/or actively inducing third parties, such as end users, that directly infringe one or more of the claims of the '762 Patent. Defendant NVIDIA's actions are in violation of one or more of the provisions of 35 U.S.C. § 271(a), (b), (c), (f), and (g).

COUNT THIRTEEN
NVIDIA's Infringement of the '725 Patent

45. MOSAID incorporates by reference each of the foregoing paragraphs of this Complaint as though fully set forth herein.

46. Defendant NVIDIA has been and is still directly infringing one or more of the claims of the '725 Patent. Defendant NVIDIA's infringing acts include, but are not limited to, making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the '725 Patent, such as processors, including but not limited to one or more of the GoForce series of processors, including the GoForce 6100 processor. Defendant NVIDIA has been and is still contributing to the infringement of and/or actively inducing third parties, such as

end users, that directly infringe one or more of the claims of the '725 Patent. Defendant NVIDIA's actions are in violation of one or more of the provisions of 35 U.S.C. § 271(a), (b), (c), (f), and (g).

COUNT FOURTEEN
Interphase's Infringement of the '036 Patent

47. MOSAID incorporates by reference each of the foregoing paragraphs of this Complaint as though fully set forth herein.

48. Defendant Interphase has been and is still directly infringing one or more of the claims of the '036 Patent. Defendant Interphase's infringing acts include, but are not limited to, making, using, offering to sell, selling, or importing devices within the scope of one or more of the claims of the '036 Patent, such as communications equipment, including but not limited to one or more of the iSPAN series of communications controllers, including the iSPAN 5639 PCI Express Communications Controller. Defendant Interphase has been and is still contributing to the infringement of and/or actively inducing third parties, such as end users, that directly infringe one or more of the claims of the '036 Patent. Defendant Interphase's actions are in violation of one or more of the provisions of 35 U.S.C. § 271(a), (b), (c), (f), and (g).

JURY DEMAND

49. Pursuant to Fed. R. Civ. P. 38(b), MOSAID demands a jury trial on all issues triable by a jury raised in this Complaint.

REQUEST FOR RELIEF

MOSAID requests that the Court find in its favor and against Defendants Freescale, Interphase, and NVIDIA and that the Court grant the following relief:

A. Judgment that one or more of the claims of the Asserted Patents have been infringed, either literally and/or under the doctrine of equivalents, by Defendants Freescale, Interphase, and NVIDIA;

B. Judgment in favor of MOSAID for the full amount of its actual damages caused by infringing activities of Defendants Freescale, Interphase, and NVIDIA, including an assessment of interest and costs;

C. Judgment for increased damages for willful infringement under 35 U.S.C. § 284;

D. Judgment that this is an "exceptional case" and awarding MOSAID its reasonable attorneys' fees and costs under 35 U.S.C. § 285;

E. Judgment that Defendants Freescale, Interphase, and NVIDIA be permanently enjoined from further activity or conduct that infringes the claims of the MOSAID Patents; and

F. Judgment that the Court award MOSAID any and all other relief as is just and proper under the circumstances.

Dated: April 7, 2011

Respectfully submitted,

/s/ David M. Schlitz

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ATTORNEYS FOR PLAINTIFF
MOSAID TECHNOLOGIES INC.

Electronic Acknowledgement Receipt	
EFS ID:	9827302
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	21005
Filer:	James M. Smith/Jill Kane
Filer Authorized By:	James M. Smith
Attorney Docket Number:	2037.2079-010
Receipt Date:	07-APR-2011
Filing Date:	21-JUL-2008
Time Stamp:	15:37:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	20372079010_IF.pdf	159966 26293361950756 2a980b18867f9842577fb9a60c	no	1

Warnings:
Information:

2	Miscellaneous Incoming Letter	20372079010_Ident_of_Litigation.pdf	666092 689d96abd0a423381aecaa334df0c99b4cf1ed6d	no	17
Warnings:					
Information:					
			Total Files Size (in bytes):	826058	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

OPAP 1A23 APR 07 2011 PATENT & TRADEMARK OFFICE

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

21005 7590 03/31/2011
HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/176,645	07/21/2008	Barry Alan HOBERMAN	2037.2079-010	3003

TITLE OF INVENTION: POWER MANAGERS FOR AN INTEGRATED CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$0	$0	$1510	$0	06/30/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
LIN, SUN J	2825	716-133000

04/08/2011 HVUONG2 00000019 080380 12176645
01 FC:1501 1510.00 DA

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 Hamilton, Brook, Smith & Reynolds, P.C.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: MOSAID Technologies Incorporated
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Ottawa, Ontario, Canada

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 08-0380 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 4/6/11
Typed or printed name James M. Smith Registration No. 28,043

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Adjustment date: 04/08/2011 HVUONG2
04/07/2011 INTEFSU 00002639 080380 12176645
01 FC:1501 1510.00 CR

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

21005 7590 03/31/2011
HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

EXAMINER
LIN, SUN J

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/31/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/176,645	07/21/2008	Barry Alan HOBERMAN	2037.2079-010	3003

TITLE OF INVENTION: POWER MANAGERS FOR AN INTEGRATED CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$0	$0	$1510	$0	06/30/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

21005 7590 03/31/2011
HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/176,645	07/21/2008	Barry Alan HOBERMAN	2037.2079-010	3003

TITLE OF INVENTION: POWER MANAGERS FOR AN INTEGRATED CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$0	$0	$1510	$0	06/30/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
LIN, SUN J	2825	716-133000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/176,645	07/21/2008	Barry Alan HOBERMAN	2037.2079-010	3003

21005 7590 03/31/2011

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/31/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 438 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 438 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/176,645	HOBERMAN ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE filed on 03/04/2011*.

2. ☒ The allowed claim(s) is/are *76-139, renumbered (37 CFR 1.126)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 3/4/11
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicants' submission filed on *03/04/2011* regarding application 12/176,645 filed on *07/21/2008* has been entered. IDS accompanying applicants' submission has been reviewed.

Claims 1 – 75 have previously been cancelled, and Claims 132 – 139 have previously been added. Claims 76 – 139 remain pending in the application.

Reasons for Allowance

2. Claims 76 – 139 are allowed over the prior art of record. An examiner's statement of reasons for allowance is given in the following:

Claims 76 – 139 are allowed due to allowable subject matter cited in the *Office Action* mailed *02/17/2011*.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (571) 272–1899. The examiner can normally be reached on Monday to Friday from 9:00am to 6:00pm.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (in USA or CANADA) or 571-272-1000.

/Sun J. Lin/
Primary Examiner, Art Unit 2825

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12176645	HOBERMAN ET AL.
	Examiner	**Art Unit**
	Sun J Lin	2825

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
716	133	G	0	6	F	17 / 50 (2006.01.01)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
716	100	126	127	132	

☐ Claims renumbered in the same order as presented by applicant ☒ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	76	19	92	37	108	56	124								
2	77	20	93	39	109	57	125								
3	78	21	94	40	110	58	126								
4	79	23	95	41	111	59	127								
5	80	24	96	42	112	60	128								
6	81	25	97	43	113	61	129								
8	82	26	98	44	114	62	130								
9	83	27	99	45	115	63	131								
10	84	28	100	46	116	64	132								
11	85	29	101	48	117	7	133								
12	86	31	102	49	118	15	134								
13	87	32	103	50	119	22	135								
14	88	33	104	51	120	30	136								
16	89	34	105	52	121	38	137								
17	90	35	106	53	122	47	138								
18	91	36	107	54	123	55	139								

NONE (Assistant Examiner) (Date)	**Total Claims Allowed:** 64	
/Sun J Lin/ Primary Examiner.Art Unit 2825 03/27/2011 (Primary Examiner) (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 2

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12176645	HOBERMAN ET AL.
	Examiner	Art Unit
	Sun J Lin	2825

SEARCHED			
Class	Subclass	Date	Examiner
716	100,126,127,132,133	2/9/11	/JSL/

SEARCH NOTES		
Search Notes	Date	Examiner
EAST [US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB]	2/9/11	/JSL/
EAST [US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB]	3/27/11	/JSL/

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
716	133	2/9/11	/JSL/
716	100	2/9/11	/JSL/
716	126	2/9/11	/JSL/
716	127	2/9/11	/JSL/
716	132	2/9/11	/JSL/

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12176645	HOBERMAN ET AL.
	Examiner	**Art Unit**
	Sun J Lin	2825

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☒ CPA ☒ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/19/2010	02/09/2011	03/27/2011						
	1	-	-	-						
	2	-	-	-						
	3	-	-	-						
	4	-	-	-						
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	34	-	-	-						
	35	-	-	-						
	36	-	-	-						

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CLAIM		DATE								
Final	Original	12/19/2010	02/09/2011	03/27/2011						
	37	-	-	-						
	38	-	-	-						
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	68	-	-	-						
	69	-	-	-						
	70	-	-	-						
	71	-	-	-						
	72	-	-	-						

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CLAIM		DATE								
Final	Original	12/19/2010	02/09/2011	03/27/2011						
	73	-	-	-						
	74	-	-	-						
	75	-	-	-						
1	76	✓	=	=						
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3	78	✓	=	=						
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32	103	✓	=	=						
33	104	✓	=	=						
34	105	✓	=	=						
35	106	✓	=	=						
36	107	✓	=	=						
37	108	✓	=	=						

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12176645	HOBERMAN ET AL.
	Examiner	**Art Unit**
	Sun J Lin	2825

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CLAIM		DATE								
Final	Original	12/19/2010	02/09/2011	03/27/2011						
39	109	✓	=	=						
40	110	✓	=	=						
41	111	✓	=	=						
42	112	✓	=	=						
43	113	✓	=	=						
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45	115	✓	=	=						
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30	136		=	=						
38	137		=	=						
47	138		=	=						
55	139		=	=						

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **March 4, 2011** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

U.S. PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
/JSL/	A8	6,438,635 B1	08-20-2002	Date et al.

Copies of issued U.S. Patents and Published U.S. Applications are not required and are not being provided. We are not listing separately any prior U.S. Patent Office communications regarding the cited documents because the Examiner has access to any such actions through PAIR.

EXAMINER	DATE CONSIDERED
/Sun J. Lin/	03/07/2011

1066299.1

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **March 4, 2011** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

FOREIGN PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Country Code-Number-Kind Code (if known)	DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
/JSL/	B3	JP 11-045225	02-16-1999	Canon Inc
	B4			
	B5			
	B6			
	B7			
	B8			
	B9			
	B10			
	B11			
	B12			
	B13			
	B14			
	B15			
	B16			
	B17			
	B18			
	B19			

EXAMINER	/Sun J. Lin/	DATE CONSIDERED	03/07/2011

1066299.1

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	("6438635").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/27 11:32
L2	0	("6438635") and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj amage $4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/27 11:37
L3	0	((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage$4) and ("6438635")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/27 11:38

L4	0	((power or voltage) adj island $2) and ((power adj consumption $2) same (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage$4) and ("6438635")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/03/27 11:40
S1	6	716/100	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:14
S2	6	716/126	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:14
S3	2	716/127	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:15
S4	1	716/132	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:15
S5	2	716/133	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:15

S6	0	(716/100).ccls. and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj amage $4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:28
S7	0	(716/126).ccls. and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj amage $4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:29
S8	0	(716/127).ccls. and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj amage $4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:29

S9	0	(716/132).ccls. and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj amage $4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:29
S10	0	(716/133).ccls. and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj amage $4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:29
S11	0	("716"/$).ccls. and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj amage $4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:29

S12	0	((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj amage $4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:30
S13	0	(716/100).ccls. and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:31
S14	0	(716/126).ccls. and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:31

S15	0	(716/127).ccls. and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:31
S16	1	(716/132).ccls. and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:32
S17	0	(716/133).ccls. and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:33

S18	1	("716"/$).ccls. and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:33
S19	6	((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:33
S20	0	(((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage$4)).CLM.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:40
S21	8	((power or voltage) adj island $2) and ((power adj consumption $2) same (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:42

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S22	0	("716"/$).ccls. and ((power or voltage) adj island$2) and ((power adj consumption$2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj amage $4)	USPAT; UPAD	OR	OFF	2010/12/08 12:29
S23	0	((power or voltage) adj island$2) and ((power adj consumption$2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj amage $4)	USPAT; UPAD	OR	OFF	2010/12/08 12:30
S24	0	("716"/$).ccls. and ((power or voltage) adj island$2) and ((power adj consumption$2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage $4)	USPAT; UPAD	OR	OFF	2010/12/08 12:33

S25	2	((power or voltage) adj island$2) and ((power adj consumption$2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage $4)	USPAT; UPAD	OR	OFF	2010/12/08 12:39
S26	0	(((power or voltage) adj island $2) and ((power adj consumption $2) with (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage $4)).CLM.	USPAT; UPAD	OR	OFF	2010/12/08 12:40
S27	4	((power or voltage) adj island$2) and ((power adj consumption$2) same (signal or level)) and (supply adj voltage) and (operat$3 adj frequenc$3) and (power adj manage $4)	USPAT; UPAD	OR	OFF	2010/12/08 12:44

3/27/11 11:41:29 AM
C:\Documents and Settings\SLin1\My Documents\EAST\workspaces\CASE672.wsp

UNITED STATES PATENT AND TRADEMARK OFFICE

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530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD MA 01742-9133

MAILED

MAR 07 2011

OFFICE OF PETITIONS

In re Application of	:	
Barry Allan Hoberman, et al.	:	
Application No. 12/176,645	:	DECISION GRANTING PETITION
Filed: July 21, 2008	:	UNDER 37 CFR 1.313(c)(2)
Attorney Docket No. 2037.2079-010	:	

This is a decision on the petition under 37 CFR 1.313(c)(2), filed March 4, 2011, to withdraw the above-identified application from issue after payment of the issue fee.

The petition is **GRANTED**.

The above-identified application is withdrawn from issue for consideration of a submission under 37 CFR 1.114 (request for continued examination). *See* 37 CFR 1.313(c)(2).

Petitioner is advised that the issue fee paid on February 18, 2011 cannot be refunded. If, however, this application is again allowed, petitioner may request that it be applied towards the issue fee required by the new Notice of Allowance.[1]

Telephone inquiries regarding this decision should be directed to undersigned at (571) 272-1642. All other inquiries concerning the examination or status of this application should be directed to the Technology Center.

This application is being referred to Technology Center AU 2825 for processing of the request for continued examination under 37 CFR 1.114 and for consideration of the concurrently filed information disclosure statement.

/AMW/
April M. Wise
Petitions Examiner
Office of Petitions

[1] *The request to apply the issue fee to the new Notice may be satisfied by completing and returning the new Part B – Fee(s) Transmittal Form (along with any balance due at the time of submission). Petitioner is advised that the Issue Fee Transmittal Form* ***must*** *be completed and timely submitted to avoid abandonment of the application.*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell

Application No.: 12/176,645 Group: 2825

Filed: July 21, 2008 Examiner: Lin, Sun J.

Confirmation No.: 3003

For: Power Managers For An Integrated Circuit

PETITION UNDER 37 CFR § 1.313(c)(2)

Office of Petitions
Madison West Building, 7th Floor
600 Dulany Street
Alexandria, VA 22314

Sir:

A Notice of Allowance and Issue Fee Due was mailed in the above-captioned case on February 17, 2011 and the Issue Fee was submitted in the amount of $1,510 on February 18, 2011.

Applicant respectfully petitions the U.S. Patent and Trademark Office under 37 CFR § 1.313(c)(2) to withdraw the instant application from issue for consideration of a Request for Continuing Examination in compliance with 37 CFR § 1.114, with the following submission(s):

- ☒ Supplemental Information Disclosure Statement
- ☐ amendment to the written description, claims, or drawings
- ☐ new arguments
- ☐ new evidence in support of patentability
- ☐ other [___]

The instant application was filed on or after June 8, 1995 and is therefore eligible for Section 1.114 practice.

Authorization is hereby granted to charge the fee of $810 set forth in Section 1.17(e) for filing the Request for Continued Examination, the Petition fee of $130 set forth in Section 1.17(h), as well as any other fees which may be due in this matter, to Deposit Account No. 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By /James M. Smith, Reg. No. 28,043/
James M. Smith
Registration No. 28,043
Telephone (978) 341-0036
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Concord, Massachusetts 01742-9133
Dated: March 4, 2011

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **March 4, 2011** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

U.S. PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
	A8	6,438,635 B1	08-20-2002	Date et al.

Copies of issued U.S. Patents and Published U.S. Applications are not required and are not being provided. We are not listing separately any prior U.S. Patent Office communications regarding the cited documents because the Examiner has access to any such actions through PAIR.

EXAMINER	DATE CONSIDERED

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **March 4, 2011** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

FOREIGN PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Country Code-Number-Kind Code (if known)	DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
	B3	JP 11-045225	02-16-1999	Canon Inc
	B4			
	B5			
	B6			
	B7			
	B8			
	B9			
	B10			
	B11			
	B12			
	B13			
	B14			
	B15			
	B16			
	B17			
	B18			
	B19			

EXAMINER	DATE CONSIDERED

PATENT ABSTRACTS OF JAPAN

(11)Publication number : **11-045225**
(43)Date of publication of application : **16.02.1999**

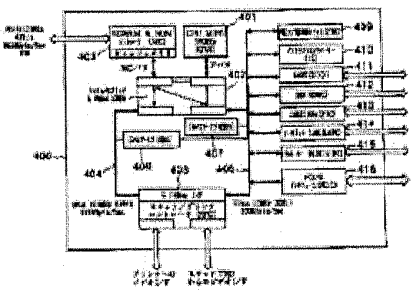
(51)Int.Cl. **G06F 13/362**
G06F 13/16
G06F 13/36

(21)Application number : **09-200570**
(22)Date of filing : **25.07.1997**

(71)Applicant : **CANON INC**
(72)Inventor : **DATE ATSUSHI**
FUJIWARA TAKASHI
MAEDA TADAAKI
YOKOYAMA NOBORU
KATO KATSUNORI

(54) BUS MANAGEMENT DEVICE AND CONTROLLER FOR COMPOUND EQUIPMENT HAVING THE SAME

(57)Abstract:
PROBLEM TO BE SOLVED: To efficiently process a large amount of data such as image data.
SOLUTION: A P bus from a CPU 401 a MC bus from a system memory, an IO bus to which input/output equipment is connected and a G bus for transferring image data of a printer controller 408 are connected to a system bus bridge (SSB) 402. The SSB 402 connects one of the P bus, G bus, and IO bus as a master and one of the MC bus and IO bus at a master's request. At this time, the P bus and IO bus, and G bus and MC bus can be connected in parallel. Consequently, access to the memory by the scanner printer controller is possible in parallel to the use of the input/output equipment by the CPU.



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(51)Int.Cl.[6]		識別記号	FI		
Ｇ０６Ｆ	13/362	５１０	Ｇ０６Ｆ	13/362	５１０Ｄ
	13/16	５２０		13/16	５２０Ｃ
	13/36	５３０		13/36	５３０Ｂ

審査請求　未請求　請求項の数26　ＯＬ　（全 60 頁）

(21)出願番号　特願平9－200570

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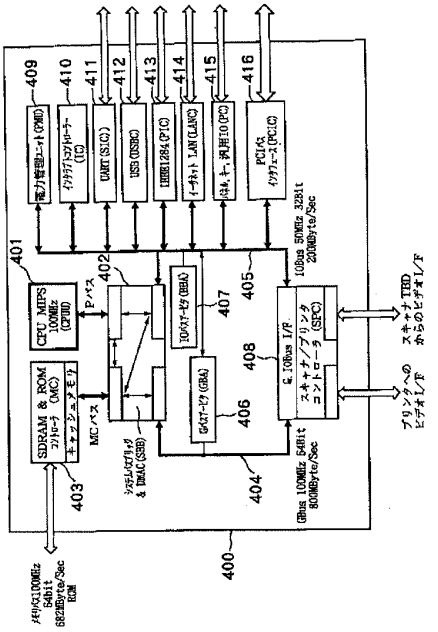
(72)発明者　前田　忠昭
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(74)代理人　弁理士　大塚　康徳　（外２名）

最終頁に続く

(54)【発明の名称】　バス管理装置及びそれを有する複合機器の制御装置

(57)【要約】
【課題】画像データ等、大量のデータを効率良く処理する。
【解決手段】システムバスブリッジ（ＳＳＢ）４０２には、ＣＰＵ４０１からのPバス、システムメモリからのＭＣバス、入出力機器が接続されたＩＯバス、スキャナプリンタコントローラ４０８の画像データを転送するＧバスが接続され、ＳＳＢ４０２は、マスタとしてPバス、Ｇバス、ＩＯバスのいずれか、スレーブとしてＭＣバス、ＩＯバスのいずれかをマスタの要求に応じて接続する。この際。PバスとＩＯバス、ＧバスとＭＣバスは、並列に接続することができる。そのため、ＣＰＵによる入出力機器の使用と並行して、スキャナプリンタコントローラによるメモリのアクセスを行うことができる。



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【特許請求の範囲】

【請求項１】　少なくとも１つのバスと、
該バスに接続された複数のバスマスタと、
前記複数のバスマスタそれぞれに対してバス使用権の付与の開始条件と終了条件とを記憶する手段と、
前記複数のバスマスタからバスの使用要求があると、前記条件にしたがって前記複数のバスマスタのバス使用権の付与を開始し、終了するバス調停手段とを備えることを特徴とするバス管理装置。

【請求項２】　前記複数のバスマスタの順序を記憶する第２の記憶手段を更に備え、前記バス調停手段は、前記順序と前記開始条件とを満足したバスマスタにバス使用権の付与を開始し、バス使用権を与えられており、前記終了条件を満足したバスマスタのバス使用権の付与を終了することを特徴とする請求項１に記載のバス管理装置。

【請求項３】　優先順次モードと完全順次モードとを表すモード設定手段を更に備え、前記バス調停手段は、優先順次モードにおいては、前記記憶手段にバス使用権の付与の開始条件と終了条件とが記憶されたバスマスタを、それ以外のバスマスタに対して優先的にバスの使用権を付与し、完全順次モードにおいては、前記記憶手段にバス使用権の付与の開始条件と終了条件とが記憶されていないバスマスタに対してはバスの使用権を付与しないことを特徴とする請求項１または２に記載のバス管理装置。

【請求項４】　少なくとも４つのバスと、
前記バスに接続されたバスマスタと、
前記バス同士の接続を、前記バスのそれぞれに接続されたバスマスタのバスの要求に応じて切り替える切り替え手段とを備えることを特徴とするバス管理装置。

【請求項５】　前記少なくとも４つのバスの内のひとつにはメモリが、他のバスにはそれぞれ少なくとも１つのバスマスタが接続されていることを特徴とする請求項４に記載のバス管理装置。

【請求項６】　前記バスは、メモリに接続されたバスと、プロセッサに接続されたバスと、入出力機器に接続された少なくとも２つのバスを含み、前記切り替え手段は、プロセッサに接続されたバスと入出力機器に接続されたバスとからの接続要求を調停することを特徴とする請求項５に記載のバス管理装置。

【請求項７】　前記切り替え手段は、前記メモリに接続されたバスと前記入出力機器に接続された一方のバスと、前記プロセッサに接続されたバスと前記入出力機器に接続された他方のバスとのそれぞれを、並列的に接続することを特徴とする請求項６に記載のバス管理装置。

【請求項８】　前記切り替え手段は、前記プロセッサからのメモリあるいは入出力に対する接続要求と、前記入出力バスそれぞれからメモリに対する接続要求とを調停し、バス同士の接続を切り替えることを特徴とする請求項６に記載のバス管理装置。

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【請求項９】　画像データの入力及び出力を行う画像入出力機器を制御する制御部を更に備え、該制御部は、前記入出力機器に接続された２つのバスに接続され、選択的にいずれかを用いることを特徴とする請求項４に記載のバス管理装置。

【請求項１０】　それぞれにバスマスタを備えた少なくとも２つのバスと、
前記バスを介してアクセスされるメモリと、
前記バスそれぞれに接続され、当該バスのバスマスタによるバス要求を調停し、そのいずれかにバス使用権を付与する調停手段と、
前記バスそれぞれについてバス使用権を付与された複数のバスマスタが同一のあて先に書き込みを行う場合、それらバスマスタのうち、もっとも早くバス要求を出したバスマスタ以外のバスマスタに対するバス使用権を停止させるよう、前記調停手段に対して通知するバス同期手段とを備えることを特徴とするバス管理装置。

【請求項１１】　前記バス同期手段は、前記各バスのバスマスタがバス要求を出した時刻を記憶し、バス要求とともに指定されたアドレスを比較して一致した場合には前記記憶された時刻を比較し、もっとも速い時刻のバス要求でないバス要求を出したバスマスタを停止させることを特徴とする請求項１０に記載のバス管理装置。

【請求項１２】　それぞれがバスの調停手段を有する少なくとも２つのバスと、
前記バスに接続されたバスマスタと、
前記バスの状態と、前記バスマスタから出されるバス要求の情報とを判定し、前記バスのうちいずれを使用するか決定する決定手段とを備えることを特徴とするバス管理装置。

【請求項１３】　前記バス要求の情報には、バス要求の優先度とデータの転送先と転送サイズとを含み、前記バスの状態には、各バスの使用状態を含み、前記決定手段は、要求された前記転送先と転送サイズとが許されるバスがひとつの場合にはそのバスを使用するものと決定し、複数ある場合には、転送速度の速い方のバスを優先的に使用するよう決定することを特徴とする請求項１２に記載のバス管理装置。

【請求項１４】　単一の半導体基板上に形成されてなることを特徴とする請求項１乃至１３のいずれかに記載のバス管理装置。

【請求項１５】　連続したロケーションへのデータ転送を行うバーストモードを支援するメモリと、
前記メモリの前段にあって、該メモリと交換されるデータを一旦蓄積するキャッシュメモリを備えたメモリ制御手段とを備え、
前記メモリ制御手段は、前記メモリへのデータ転送がバーストモードであればキャッシュを介さずに直接前記メモリへデータを転送し、シングルモードであれば一旦キ

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ャッシュにデータを書き込むようキャッシュメモリを制御することを特徴とするメモリ管理装置。

【請求項１６】　連続したロケーションへのデータ転送を行うバーストモードを支援するメモリと、

前記メモリの前段にあって、該メモリと交換されるデータを一旦蓄積するキャッシュメモリを備えたメモリ制御手段と、

前記メモリへアクセスする複数のバスマスタとを備え、

前記メモリ制御手段は、前記メモリへのデータ転送をしようとするバスマスタに応じて、キャッシュを介さずに直接前記メモリへデータを転送するか、一旦キャッシュにデータを書き込んでメモリへデータを転送するか制御することを特徴とするメモリ管理装置。

【請求項１７】　前記メモリ制御手段は、前記バスマスタの識別子と、それに対応して、キャッシュを介さずに直接前記メモリへデータを転送するか、一旦キャッシュにデータを書き込んでメモリへデータを転送するかの別を記憶する再書込み可能なテーブルを備えることを特徴とする請求項１６に記載のメモリ管理装置。

【請求項１８】　前記メモリは、シンクロナスＤＲＡＭであることを特徴とする請求項１５乃至１７のいずれかに記載のメモリ管理装置。

【請求項１９】　前記メモリ制御手段は、単一の半導体基板上に形成された電気回路であることを特徴とする請求項１５乃至１８のいずれかに記載のメモリ管理装置。

【請求項２０】　制御部により制御された複数の回路ブロックを含む電気回路の消費電力を制御する電力管理装置であって、

各ブロックの動作状態を監視する状態監視手段と、

動作状態にあるブロックの消費電力を加算する加算手段と、

加算された電力を所定の閾値と比較し、閾値を越えたことを前記制御部に通知する通報手段とを備えることを特徴とする電力管理装置。

【請求項２１】　前記通報手段は、前記閾値として互いに異なる複数の値を有し、各閾値ごとの比較結果に応じて、通知を行うことを特徴とする請求項２０に記載の電力管理装置。

【請求項２２】　経過時間を測定する計時手段を更に備え、前記通報手段は、前記通知を行ってから、各ブロックの動作状態が変わらないまま所定時間経過すると再度通知を繰り返すことを特徴とする請求項２０または２１に記載の電力管理装置。

【請求項２３】　前記閾値は、前記制御部により書き換えられることを特徴とする請求項２０に記載の電力管理装置。

【請求項２４】　請求項１乃至１４のいずれかに記載のバス管理装置を備え、該バス管理装置により、画像入力装置及び画像出力装置が接続されたバスを管理することを特徴とする複合機器の制御装置。

【請求項２５】　請求項１５乃至１９のいずれかに記載のメモリ管理装置を備えることを特徴とする複合機器の制御装置。

【請求項２６】　請求項２０乃至２３のいずれかに記載の電力管理装置を備えることを特徴とする複合機器の制御装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、スキャナ等の画像入力装置と、プリンタ等の画像出力装置とを効率的に制御する複合機器の制御装置に関する。

【０００２】

【従来の技術】従来、スキャナなどの画像入力装置と、プリンタなどの画像出力装置を組み合わせた、複写機やファクシミリ、あるいはそれらを単体として備えたコンピュータシステムなどが実用化されている。こういったシステムでは、画像データを扱うために、膨大な量のデータを効率的に処理する必要がある。

【０００３】

【発明が解決しようとする課題】こういったシステムにおいては、データ転送のために複数のバスマスタによるDMA転送が用いられる。複数のバスマスタが順次に処理を行うことが必要な場合、例えば、メモリ上のデータに対して、処理Ａ（バスマスタ１）を行った後、処理Ｂ（バスマスタ２）を行い、その処理後のデータをバスマスタ４に送るといった一連の処理を考える。

【０００４】通常このような処理を行う場合、それぞれバスマスタが、メモリからデータをリードし、処理後のデータをメモリに書き戻すというDMA機能があれば、ソフトウェアはまず、バスマスタ１に対して処理Ａを行うようにDMAをセットする。バスマスタ１はすべての処理を終了後、プロセッサに対して割り込みを上げ、処理の終了を行うようにDMAをセットし、処理の終了後、今度はバスマスタ４に対してメモリからデータをリードするようにセットを行う。このように一連の処理を行うためには、ソフトウェアによりひとつの処理が終了したのを確認してから次の処理をスタートさせるというように処理を行っていく必要があった。

【０００５】このようにこれまではそれぞれの処理を行う度にソフトウェアが介入する必要があり、また処理毎にいちいちメモリに書き戻してやる必要があり、無駄な処理が多いという第１の問題があった。

【０００６】また、大量のデータを扱うために、単一のバスではバスの転送能力がボトルネックとなっていた。これを解消するために、バスを２重化して転送能力の増強を図ったシステムもあった。

【０００７】しかしながら、複数のバスを有するシステムであっても、バスの構成が柔軟でなく、大量のデータを転送する場合などには、十分な転送能力が引き出されてはいなかったという第２の問題点があった。

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【０００８】また、従来のバスは単一であるのが普通であり、複数のバスマスタが同一のメモリアドレスに書き込みを行おうとした場合、バス使用権を獲得した順にメモリへデータを書き込むことが保証できた。

【０００９】しかしながら、複数のバスが存在し、これらのバスのバス調停（アービトレーション）と、複数のバスのどれかひとつのバスをメモリへ接続することを独立に制御するシステム構成では、複数のバスの接続された複数のバスマスタが同時に同一のメモリ空間へ書き込みを行う可能性があり、書き込みの順序は、バスの調停によりバスの使用権を得た順序とはならない可能性があるという第３の問題点があった。

【００１０】更に、データを効率的に処理するために、従来キャッシュメモリの使用が行われている。

【００１１】しかしながら従来のキャッシュ制御は、転送先メモリのアドレス情報を基にキャッシュのオン／オフが行われていた。このため、大量のデータをキャッシュ許可のメモリ空間に転送すると、この大量のデータがキャッシュされ、すべて新たなデータで書き換えられてしまい、他のデバイスがメモリにアクセスする場合にはキャッシュミスとなる可能性が高い。これはキャッシュの容量を増やせば解決するかに見えるが、それは大幅な製造コストの上昇につながる。また、特に、プリント時などには、読み出された大量の画像データはそのままプリンタエンジンに渡されてそのデータがキャッシュされたとしても２度と使用されることはない。このようにむやみにキャッシュすることは、逆にキャッシュヒット率を低下させることになる。このように、キャッシュを効率良く利用することができない場合があるという第４の問題点があった。

【００１２】さらに、複数のバスを用いたシステムでは、複数のバスを使用できるバスマスタは、どのバスを使用するか決定する必要がある。従来はアクセスする相手先が決まればそれに応じてバスも決定していた。

【００１３】しかしながら、使用するバスが相手先に応じて固定されているため、各バスの転送速度や使用率等を考慮した効率的なバスの使用が行えないという第５の問題点があった。

【００１４】さらに、このようなシステムをひとつの半導体チップに集積すると大量の熱が発生し、パッケージが熱で破壊されるおそれがあるという第６の問題点があった。

【００１５】本発明は上記第１の問題に鑑みてなされたもので、処理毎のソフトウェアの介入が必要なく全体としての処理速度を向上させるバス管理装置及びそれを有する複合機器の制御装置を提供することを第１の目的とする。

【００１６】また、本発明は上記第２の問題に鑑みてなされたもので、バスの構成を柔軟にし、最適なバスを選んでデータの転送を行えるバス管理装置及びそれを有する複合機器の制御装置を提供することを第２の目的とする。

【００１７】また、本発明は上記第３の問題に鑑みてなされたもので、複数のバスのそれぞれに接続されたバスマスタからのバスの使用権を得た順にメモリにアクセスできるバス管理装置及びそれを有する複合機器の制御装置を提供することを第３の目的とする。

【００１８】また、本発明は上記第４の問題に鑑みてなされたもので、キャッシュの使用効率を向上させるメモリ管理装置及びそれを有する複合機器の制御装置を提供することを第４の目的とする。

【００１９】また、本発明は上記第５の問題に鑑みてなされたもので、各バスマスタが使用するバスを動的に決定してバスの効率を向上させたバス管理装置及びそれを有する複合機器の制御装置を提供することを第５の目的とする。

【００２０】また、本発明は上記第６の問題に鑑みてなされたもので、回路の動作状態を監視して消費電力を抑制し、大量の熱を発生を抑制する電力管理装置及びそれを有する複合機器の制御装置を提供することを第６の目的とする。

【００２１】

【課題を解決するための手段】上記の問題を解決するために、本発明のバス管理装置は次のような構成からなる。すなわち、少なくとも１つのバスと、該バスに接続された複数のバスマスタと、前記複数のバスマスタそれぞれに対してバス使用権の付与の開始条件と終了条件とを記憶する手段と、前記複数のバスマスタからバスの使用要求があると、前記条件にしたがって前記複数のバスマスタのバス使用権を付与を開始し、終了するバス調停手段とを備える。

【００２２】あるいは、少なくとも４つのバスと、前記バスに接続されたバスマスタと、前記バス同士の接続を、前記バスのそれぞれに接続されたバスマスタのバスの要求に応じて切り替える切り替え手段とを備える。

【００２３】あるいは、それぞれにバスマスタを備えた少なくとも２つのバスと、前記バスを介してアクセスされるメモリと、前記バスそれぞれに接続され、当該バスのバスマスタによるバス要求を調停し、そのいずれかにバス使用権を付与する調停手段と、前記バスそれぞれについてバス使用権を付与された複数のバスマスタが同一のあて先に書き込みを行う場合、それらバスマスタのうち、もっとも早くバス要求を出したバスマスタ以外のバスマスタに対するバス使用権を停止させるよう、前記調停手段に対して通知するバス同期手段とを備える。

【００２４】あるいは、それぞれがバスの調停手段を有する少なくとも２つのバスと、前記バスに接続されたバスマスタと、前記バスの状態と、前記バスマスタから出されるバス要求の情報とを判定し、前記バスのうちいずれを使用するか決定する決定手段とを備える。

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【００２５】あるいは、本発明のメモリ管理装置は次のような構成からなる。すなわち、連続したロケーションへのデータ転送を行うバーストモードを支援するメモリと、前記メモリの前段にあって、該メモリと交換されるデータを一旦蓄積するキャッシュメモリを備えたメモリ制御手段とを備え、前記メモリ制御手段は、前記メモリへのデータ転送がバーストモードであればキャッシュを介さずに直接前記メモリへデータを転送し、シングルモードであれば一旦キャッシュにデータを書き込むようキャッシュメモリを制御する。

【００２６】あるいは、連続したロケーションへのデータ転送を行うバーストモードを支援するメモリと、前記メモリの前段にあって、該メモリと交換されるデータを一旦蓄積するキャッシュメモリを備えたメモリ制御手段と、前記メモリへアクセスする複数のバスマスタとを備え、前記メモリ制御手段は、前記メモリへのデータ転送をしようとするバスマスタに応じて、キャッシュを介さずに直接前記メモリへデータを転送するか、一旦キャッシュにデータを書き込んでメモリへデータを転送するか制御する。

【００２７】あるいは、本発明の電力管理装置は次のような構成からなる。すなわち、制御部により制御された複数の回路ブロックを含む電気回路の消費電力を制御する電力管理装置であって、各ブロックの動作状態を監視する状態監視手段と、動作状態にあるブロックの消費電力を加算する加算手段と、加算された電力を所定の閾値と比較し、閾値を越えたことを前記制御部に通知する通報手段とを備える。

【００２８】あるいは、本発明の複合機器の制御装置は次のような構成からなる。すなわち、上記いずれかに記載のバス管理装置を備え、該バス管理装置により、画像入力装置及び画像出力装置が接続されたバスを管理する。

【００２９】あるいは、上記いずれかに記載のメモリ管理装置を備える。

【００３０】あるいは、上記いずれかに記載の電力管理装置を備える。

【００３１】

【発明の実施の形態】次に本発明の実施の形態として、プロセッサコア、プロセッサ周辺コントローラ、メモリコントローラ、スキャナー／プリンタコントローラ、ＰＣＩインターフェースなどを内蔵したシングルチップ・スキャニング・プリンティングエンジンである“ＤｏＥｎｇｉｎｅ”を説明する。

【００３２】１．ＤｏＥｎｇｉｎｅ概要

ＤｏＥｎｇｉｎｅは、ＭＩＰＳテクノロジー社のＲ４０００プロセッサとコンパチブルなプロセッサコア、プロセッサ周辺コントローラ、メモリコントローラ、スキャナー／プリンタコントローラ、ＰＣＩインターフェースなどを内蔵したシングルチップ・スキャニング・プリンティングエンジンである。高速並列動作、ビルディングブロック手法を採用し実装される。

【００３３】プロセッサシェル（プロセッサコアを含むプロセッサ周辺回路の総称）内には最大でインストラクション、データそれぞれ１６Ｋバイトの計３２Ｋバイトのキャッシュメモリ、ＦＰＵ（浮動小数点演算ユニット）、ＭＭＵ（メモリ管理ユニット）、ユーザー定義可能なコプロセッサなどを内蔵することが可能である。

【００３４】ＰＣＩバスインターフェースを有するので、ＰＣＩバススロットを有するコンピュータシステムと共に用いることができる。また、ＰＣＩサテライト構成に加え、ＰＣＩホストバスブリッジ構成にてＰＣＩバスコンフィギュレーションを発行することが可能であり、安価なＰＣＩ周辺デバイスと組み合わせることにより、マルチファンクションペリフェラル（複合機能周辺機器）のメインエンジンとして使用することも可能である。さらにＰＣＩバスインターフェースを有するレンダリングエンジン、圧縮・伸長エンジンと組み合わせることも可能である。

【００３５】チップ内部に汎用ＩＯコアを接続するＩＯバス、及び、画像データ転送に最適化したグラフィックバス（Ｇバス:Graphics Bus)の２系統の独立したバスを有し、メモリ、プロセッサとこれらのバスをクロスバスイッチを介して接続することにより、マルチファンクションシステムにおける同時動作に必須の、並列性の高い高速データ転送を実現している。

【００３６】メモリには、画像データに代表される、連続したデータ列のアクセスに対し、最高のコストパフォーマンスを有するシンクロナスＤＲＡＭ（ＳＤＲＡＭ）をサポートし、ＳＤＲＡＭのバーストアクセス高速データ転送のメリットを享受できない小さなデータ単位でのランダムアクセスにおける性能低下を最小に抑えるために、８Ｋバイトの２ウェイセットアソシアティブ・メモリフロントキャッシュをメモリコントローラ内に備える。メモリフロントキャッシュは、すべてのメモリライトに対するバススヌープが難しい、クロスバスイッチを採用したシステム構成においても、複雑な機構なしに、キャッシュメモリによる高性能化が達成出来る方式である。また、リアルタイムデータ転送（機器制御）が可能な、プリンタ及びスキャナーとのデータインターフェース(Video Interface)を有し、さらにハードウェアによる、機器間同期のサポート及び画像処理を行う事により、スキャナ、プリンタ分離型の構成においても、高品質で高速なコピー動作の実現が可能な構成となっている。

【００３７】なお、ＤｏＥｎｇｉｎｅは、コアが３．３Ｖで動作し、ＩＯは５Ｖトレラントである。

【００３８】図１及び図２，図３は、ＤｏＥｎｇｉｎｅを用いた装置あるいはシステムの構成例を示している。図１は分離構成型であり、パーソナルコンピュータ１０

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２には、それが備えるＰＣＩインターフェースを介してＤｏＥｎｇｉｎｅを備えたローカルボード１０１が装着される。ローカルボード１０１にはＤｏＥｎｇｉｎｅのほか、後述するメモリバスを介してＤｏＥｎｇｉｎｅと接続されたメモリと、色処理回路（チップ）が設けられている。このローカルボード１０１を介して、高速スキャナ１０３とカラー／モノクロプリンタ１０４とがパーソナルコンピュータ１０２に接続される。この構成により、パーソナルコンピュータの制御のもとで，ローカルボード１０１により、スキャナ１０３から入力された画像情報を処理し、プリンタ１０４から出力させることができる。

【００３９】また、図２及び図３はスキャナ２０３とプリンタ２０２とを一体に組み込んだ例で、図２は通常の複写機に類する構成を、図３（ａ）はファクシミリ装置などの構成を示している。図３（ｂ）は、図３（ａ）をコントロールするコンピュータを示している。

【００４０】これらのうち、図１，２は、ＰＣＩインターフェースを介して接続された外部のＣＰＵによりＤｏＥｎｇｉｎｅが制御されるというスレーブモードで使用されている例であり、図３は、ＤｏＥｎｇｉｎｅのＣＰＵが主体となり、ＰＣＩインターフェースを介して接続されたデバイスを制御するマスタモードで使用されている例である。

【００４１】表１として、ＤｏＥｎｇｉｎｅの仕様を示す。外部インターフェースとして、ＰＣＩ，メモリバス，ビデオ，汎用入出力，ＩＥＥＥ１２８４，ＲＳ２３２Ｃ，１００ｂａｓｅＴ／１０ｂａｓｅＴ，ＬＣＤパネル及びキーを備えるが、更にＵＳＢを有していてもよい。内蔵ブロックとして、ＣＰＵコアに加えて、１次キャッシュ，キャッシュ付きメモリコントローラ，コピーエンジン，ＩＯバスアービタ，グラフィックバスアービタなどを備えている。また、DMAコントローラはチャネル数が５であり、グラフィックバス，ＩＯバスともにアービトレーションは、優先度付きの先着順処理方式で行われる。

【００４２】

【表１】

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項　目	概　要	スペック
チップ	動作周波数	内部100MHz、内部バス及びメモリバス100MHz
	パッケージ	313ピンBGA
	外部インターフェース	PCI
		メモリバス
		ビデオ
		汎用入出力
		IEEE1284
		RS232C
		(USB)
		LAN 100／10 baseT
		LCDパネル&キー
	内蔵ブロック	CPUコア
		1次キャッシュ
		MMU
		ICU
		システムバスブリッジ
		キャッシュ付メモリコントローラ
		COPYエンジン
		PLL
		電源制御ユニット
		IOバスアービタ
		グラフィックバスアービタ
DMAコントローラ	チャネル数	5チャネル
	最大転送速度（ピーク）	200M byte／Sec@50MHz
	転送可能経路	内部出力ブロック↔ローカルメモリ
メモリ及びバス	サポートメモリ	SDRAM
制御	データ幅	64ビット
	最大メモリ容量	1Gbyte
	最大メモリバス転送速度	682M byte／Sec
グラフィックバス	アービトレーション方式	優先度付先着値処理
	最大バス転送速度	800M byte／Sec
	バス幅	64Bit,100MHz
PCIバス	PCIバス形式	Rev2.1,32Bit,33M PCI
	マスター時転送速度	Read 96MByte／Sec,Write 88MByte／Sec
	スレーブ時転送速度	Read 101MByte／Sec,Write 111MByte／Sec
IOバス	アービトレーション方式	優先度付先着値処理
	最大バス転送速度	200M byte／Sec
	バス幅	32Bit,50MHz

【００４３】２．ＤｏＥｎｇｉｎｅの構成及び動作
本章では、ＤｏＥｎｇｉｎｅ の総論に加え、各機能ブロック毎のブロック図、概要、詳細、コアインターフェース、タイミング図などを解説する。
【００４４】２．１．ＤｏＥｎｇｉｎｅのチップ構成
図４として、ＤｏＥｎｇｉｎｅのブロック図を示す。ＤｏＥｎｇｉｎｅ４００は次世代複合機能周辺機器（システム）(MFP:Multi Function Peripheral or MFS:Multi Function System)の主たるコントローラとして設計、開発された。
【００４５】ＣＰＵ（プロセッサコア）４０１として、ＭＩＰＳテクノロジー社のＭＩＰＳＲ４０００コアを採用する。プロセッサコア４０１内には、８Ｋバイトずつのインストラクション，データのキャッシュメモリ、ＭＭＵなどが実装される。プロセッサコア４０１は、６４ビットのプロセッサバス（Ｐバス）を介して、システム

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・バス・ブリッジ（ＳＢＢ）４０２に接続される。ＳＢＢ４０２は４×４の６４ビットクロスバスイッチであり、プロセッサコア４０１の他に、キャッシュメモリを備えたＳＤＲＡＭやＲＯＭを制御するメモリコントローラ４０３と専用のローカルバス（ＭＣバス）で接続されており、さらに、グラフィックバスであるＧバス４０４、ＩＯバスであるＩＯバス４０５と接続され、全部で４つのバスに接続される。システムバスブリッジ４０２は、これら４モジュール間を、可能な限り、同時平行接続を確保することができるように設計されている。

【００４６】Ｇバス４０４はＧバスアービタ（ＧＢＡ）４０６により協調制御されており、スキャナやプリンタと接続するためのスキャナ／プリンタコントローラ（ＳＰＣ）４０８に接続される。また、ＩＯバス４０５は、ＩＯバスアービタ（ＢＢＡ）４０７により協調制御されており、ＳＰＣ４０８のほか、電力管理ユニット（ＰＭＵ）４０９，インタラプトコントローラ（ＩＣ）４１０，ＵＡＲＴを用いたシリアルインターフェースコントローラ（ＳＩＣ）４１１，ＵＳＢコントローラ４１２，ＩＥＥＥ１２８４を用いたパラレルインターフェースコントローラ（ＰＩＣ）４１３，イーサネットを用いたＬＡＮコントローラ（ＬＡＮＣ）４１４，ＬＣＤパネル，キー，汎用入出力コントローラ（ＰＣ）４１５，ＰＣＩバスインターフェース（ＰＣＩＣ）４１６にも接続されている。

【００４７】２．２．プロセッサシェル

プロセッサシェルとは、プロセッサコアに加えＭＭＵ（Memory Management Unit)、命令キャッシュ、データキャッシュ、ライトバックバッファ及び掛け算ユニットを含んだブロックを指す。

＜キャッシュメモリ＞図５に示したように、キャッシュメモリコントローラは、無効（Invalid)，有効かつクリーン（Valid Clean：キャッシュが更新されていない)，有効かつダーティ(Valid Dirty：キャッシュが更新されている)の３つのステートキャッシュを管理する。この状態に応じて、キャッシュは制御される。

【００４８】２．３．インタラプトコントローラ

図６にインタラプトコントローラ４１０のブロック図を示す。

【００４９】インタラプトコントローラ４１０は、ＩＯバスインターフェース６０５を介してＩＯバス４０５に接続され、ＤｏＥｎｇｉｎｅチップ内の各機能ブロック及び、チップ外部からのインタラプトを集積し、ＣＰＵコア４０１がサポートする、６レベルの外部インタラプト及び、ノンマスカブルインタラプト（ＮＭＩ）に再分配する。各機能ブロックとは、電力管理ユニット４０９，シリアルインターフェースコントローラ４１１，ＵＳＢコントローラ４１２，パラレルインターフェースコントローラ４１３，イーサネットコントローラ４１４，汎用ＩＯコントローラ４１５，ＰＣＩインターフェースコントローラ４１６，スキャナ／プリンタコントローラ４０８などである。

【００５０】この際、ソフトウェアコンフィギュレーション可能なマスクレジスタ(Int Mask Logic 0－5)６０２により、各要因毎に割り込みをマスクをすることが可能である。また、外部インタラプト入力は、選択的エッジ検出回路６０１により、信号線ごとに、エッジセンス／レベルセンスを選択することが出来る。要因レジスタ（Detect and set Cause Reg 0－5）６０３は、各レベルごとに、どのインタラプトがアサートされているかを示すとともに、ライト動作を行うことで、レベルごとにクリアを行う事が出来る。

【００５１】各レベルの割込み信号は、各レベル毎に少なくともひとつの割り込みがあれば割込み信号を出力すべく、論理和回路６０４により論理和として出力される。なお、各レベル内での複数要因間のレベル付けはソフトウェアにて行う。

【００５２】２．４．メモリコントローラ

図７は、メモリコントローラ４０３のブロック図である。メモリコントローラ４０３は、メモリコントローラ専用のローカルバスであるＭＣバスにＭＣバスインターフェース７０１を介して接続され、最大１ギガバイトのシンクロナスＤＲＡＭ（ＳＤＲＡＭ）と、３２メガバイトのフラッシュＲＯＭあるいはＲＯＭをサポートする。ＳＤＲＡＭの特徴であるバースト転送時の高速性を活かすため、６４（１６×４）バースト転送を実現する。また、ＣＰＵやＩＯバスよりの連続したアドレスのシングル転送を考慮し、メモリコントローラ内にＳＲＡＭ（メモリフロントキャッシュ）７０２を内蔵し、ＳＤＲＡＭへ直接シングル転送を行うことを可能な限り回避して転送効率を向上させる。メモリコントローラーＳＤＲＡＭ間のデータバス幅は、信号ramData及びramParをあわせて７２ビット（このうち８ビットの信号ramParはパリティ）、フラッシュＲＯＭ間のデータバスfntromData，prgromDataの幅は３２ビットとする。

【００５３】２．４．２．構成及び動作

メモリコントローラの各部はこれから説明するような構成となっている。

＜ＭＣバスインターフェース（７０１）＞ＭＣバスは、ＳＢＢ４０２－メモリコントローラ４０３間の専用のバスであり、またＳＢＢ内部の基本バスとして用いられている。

【００５４】ＣＰＵ４０１とバスブリッジ４０２とを接続する専用バスＰＢｕｓのバースト転送が４バーストのみ規定しているのに対し、ＭＣバスにおいては１６バースト×４までの転送を追加している。このためにバースト長を示す信号としてｍＴＴｙｐｅ［６：０］を新たに定義した。

（ＭＣバス信号の定義）

ＭＣバスの各信号は下記の通り定義される。

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・mClk（出力）　　…　ＭＣバスクロック
・mAddr[31:0]（出力）　…　ＭＣバスアドレス
32ビットのアドレスバスであり、mTs_L　がアサートされた時点からmBRdy_Lがアサートされるまで保持される。
・mDataOut[63:0]（出力）…　ＭＣバスデータ出力
64ビットの出力データバスであり、mDataOe_Lがアサートされている時のみ有効である。
・mDataOe_L（出力）　　…　ＭＣバスデータ出力イネーブル
mDataOut[63:0]が有効であることを示す。またその転送がWriteであることを示す。
・mDataIn[63:0]（入力）　…　ＭＣバスデータ入力
64ビットの入力データバスであり、mBRdy_LがアサートされているmClkの立ち上がりでサンプリングされる。
・mTs_L（出力）　　…　ＭＣバストランザクション開始ストローブ
転送が開始したことを示す。転送の最初の１クロックの間だけアサートされる。転送が１クロックで終了し、次の転送がすぐに始められるのならばmTs_Lは引続きアサートされたままになる。
・mTType[6:0]（出力）　…　ＭＣバストランザクションタイプ
ＭＣバス上の転送のタイプを示す。シングル転送時はその転送の間、バースト転送時は最初の転送(beat）の間保持される。上位３ビットがソース（マスタ）をあらわし、下位ビットがシングル／バースト長をあらわす。タイプには次のようなものがある。

mTType[6:4]	信号源
001	ＣＰＵ
010	ＩＯバス
100	Ｇバス

mTType[3:0]	シングル／バースト長
1xxx	シングル（１－８ｂｙｔｅ）
0001	２バースト
0010	４バースト
0011	６バースト
0100	８バースト
0101	１６バースト
0110	２×１６バースト
0111	３×１６バースト
0000	４×１６バースト

・mBE_L[7:0]（出力）　　…　ＭＣバストランザクションバイトイネーブルシングル転送時、64ビットデータバス上の有効なバイトレーンを示す。バースト転送時はWrite時のみ有効であり、Read時は無視される。
・mBRdy_L（入力）　　…ＭＣバスレディ

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現在の転送(beat)が終了したことを示す。
・mTPW_L（出力）　　…　次トランザクションがIn-page write（ページ内書き込み）
次の転送が同じページ（同じRowアドレス)のWriteであることを示し、最大４個までのWriteを続けることができる。ページサイズはあらかじめコンフィギュレーションレジスタに設定しておく。
・mBPWA_L（入力）　　…　バスのページ内書き込み許可
ＭＣバススレーブ（メモリコントローラ）がページ内書き込みトランザクションを許可するかどうかを示し、mBRdy_Lと同じクロックでサンプリングされる。この時mBPWA_LがディアサートされていればmTPW_Lは無意味となる。
・mBRty_L（入力）　　…　バスリトライ
ＭＣバススレーブ（メモリコントローラ）がアクセスを未実行のまま終了させる場合にアサートし、少なくとも１サイクル以上のアイドルの後に再試行しなければならないことを示す。（もしmBRdy_LとmBRty_Lが同時にアサートされた場合は、mBRty_Lが優先される。）
・mBerr_L（入力）　　…　バスエラー
パリティエラーやその他のバスエラーが発生した場合にアサートされる。
【００５５】なお、上述した入出力の別はＳＢＢからみての定義である。
（ＭＣバストランザクション）ＭＣバス上のトランザクションとしては、以下のトランザクションをサポートする。
❶ベーシックトランザクション(1,2,3,4,8バイト Read/Write)
mBE_L[7:0]信号に従い、１，２，３，４，８バイトのシングルトランザクションをサポートする。
❷バーストトランザクション
（CPUからの）4-ダブルワードバーストまでのトランザクションをサポートする。
❸Ｇバスからの16-ダブルワードバースト x4までのトランザクションをサポートする。
❹In-page write（ページ内書き込み）トランザクション
mTPW_Lで示される同一ページ内の書き込みに関して、連続的なWriteアクセスをサポートする。
❺バスリトライ
メモリコントローラ内の制限によりメモリアクセスができない場合は、mBRty_L信号をアサートし、バスリトライを通知する。
＜ＳＤＲＡＭコントローラ（７０５）＞メモリコントローラ４０３は、次のような構成を有するＳＤＲＡＭを以下のように制御する。
【００５６】（ＤＲＡＭ構成）ＤＲＡＭの構成としては、x4,x8,x16ビットタイプの１６／６４メガビットＳ

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ＤＲＡＭを64ビットデータバスで８バンク制御すること ＊【００５７】
ができる。 ＊ 【表２】

バンク内のデバイス数	デバイス構成	Rowビット(バンク選択ビットを含む)×Columnビット	バンクサイズ	最大メモリ(8バンク)
16(64Mbit Type)	16M×4	14×10	128 Mbyte	1 Gbyte
8(64Mbit Type)	8M×8,9	14×9	64 Mbyte	512 Mbyte
4(64Mbit Type)	4M×16,18	14×8	32 Mbyte	256 Mbyte
16(16Mbit Type)	4M×4	12×10	32 Mbyte	256 Mbyte
8(16Mbit Type)	2M×8,9	12×9	16 Mbyte	128 Mbyte
4(16Mbit Type)	1M×16,18	12×8	8 Mbyte	64 Mbyte

【００５８】（ＤＲＡＭアドレスビット構成）ＤＲＡＭ ※場合にはMA[11:0]を使用する。
のアドレスビットの割付けについては、６４ビットＳＤ 【表３】
ＲＡＭの場合にはMA[13:0]を、１６ビットＳＤＲＡＭの※

64 Mbit SDRAM

31 30	29…27	26 25	24 …11	10 … 3	2 … 0
0 0	CS	C9 C8	R13－R0	C7－C0	BS

16 Mbit SDRAM

31 28	27…25	24 23	22 …11	10 … 3	2 … 0
0 0	CS	C9 C8	R11…R0	C7－C0	BS

0 Zero
CS Chip Select
C9－C0 Column Address
×8bit SDRAMの場合、C8は無視
×16bit SDRAMの場合、C9,C8は無視
R13－R0 Row Address
16M SDRAMのR11はSDRAM内のバンクセレクトに用いられる。
64M SDRAMで4Bank構成の場合R12,R13が
2Bank構成の場合R13がバンクセレクトに用いられる。
BS Byte Select

（ＳＤＲＡＭプログラマブル構成（モードレジスタ））
ＳＤＲＡＭは内部にモードレジスタを持ち、モードレジスタ設定コマンドを用いて下記の項目を設定する。
①バースト長
バースト長は、１，２，４，８，フルページのいずれかが設定可能であるが、CPUからのバースト転送長が４であることから、バースト長４が最適である。Ｇバスからの１６バースト以上の転送は、Read/Writeコマンド（オートプリチャージ無し）を連続して発行することにより実現する。
②ラップタイプ（Wrap Type）
バースト転送時のアドレスのインクリメント順を設定する。「シーケンシャル」または「インターリーブ」のどちらかが設定可能である。
③CASレーテンシ
CASレーテンシは、１，２，３のいずれかが設定可能であり、使用するＳＤＲＡＭのグレードと動作クロックにより決定される。
【００５９】（ＳＤＲＡＭコマンド）ＳＤＲＡＭに対して以下のコマンドをサポートする。各コマンドの詳細は、ＳＤＲＡＭデータブックに記載されている。
・モードレジスタ設定コマンド
・アクティブコマンド
・プリチャージコマンド
・ライトコマンド
・リードコマンド
・CBR(Auto)リフレッシュコマンド
・セルフリフレッシュ開始コマンド
・バーストストップコマンド
・NOPコマンド
（ＳＤＲＡＭリフレッシュ）ＳＤＲＡＭは、2048サイクル/32ms(4096/64ms)であるので、16,625nsおきにCBRリフレッシュコマンドを発行する。メモリコントローラは設定可能なリフレッシュカウンタを持ち、自動的にCBRリフレッシュコマンドを発行する。Ｇバスからの16-バーストx nの転送中は、リフレッシュ要求を受け付けない。したがって、リフレッシュカウンタは16-バーストx 4転送の時間だけ余裕を持った値を設定しなければならない。また、セルフリフレッシュをサポートする。このコマンドを発行すると、パワーダウンモード(ramclke_L=Low)時にセルフリフレッシュが続行される。
【００６０】（ＳＤＲＡＭ初期化）メモリコントローラはパワーオンリセット後、ＳＤＲＡＭに対して以下の初期化を行なう。すなわち、電源投入後100μｓのポーズ期間をおいて、
①プリチャージウコマンドを用いて全バンクをプリチャージする。
②ＳＤＲＡＭのモードレジスタを設定する。

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❸オートリフレッシュコマンドを用いて、リフレッシュを８回行う。

＜フラッシュＲＯＭコントローラ（７０４）＞フラッシュＲＯＭコントローラ７０４は、romAddr[23:2]のアドレス信号と４個のチップセレクト(romCs_L[3:0])信号をサポートする。アドレス信号romAddr2～romAddr9はパリティ信号ramPar0～ramPar7とマルチプレクスされ、アドレス信号romAddr10～romAddr23は、ＤＲＡＭアドレスramAddr0～ramAddr13とマルチプレクスされている。

＜ＳＲＡＭコントロール（メモリフロントキャッシュ）＞メインメモリとして用いられるＳＤＲＡＭは、バースト転送は非常に高速であるが、シングル転送においてはその高速性が発揮できない。そこで、メモリコントローラ内にメモリフロントのキャッシュを実装し、シングル転送の高速化をはかる。メモリフロントキャッシュは、キャッシュコントローラ７０６とＳＲＡＭ７０２より構成される。ＭＣバスに定義されたmTType[6:0]信号により、その転送マスターと転送長を知ることができるので、各マスターごと、あるいは転送長ごとにキャッシュのオン／オフが設定可能である。キャッシュの方式は、次の通りである。なお、以下、特に断らない限り、単なるキャッシュあるいはキャッシュメモリという呼称は、プロセッサコアに内蔵されたキャッシュではなく、メモリコントローラが内蔵するメモリフロントキャッシュを指すものとする。

・２ウェイセットアソシアティブ
・8kバイトデータＲＡＭ
・128 x 21 x 2 タグＲＡＭ
・ＬＲＵ(Least Recently Used)アルゴリズム
・ライトスルー
・No Write Allocate

次にキャッシュコントローラ７０６を中心とする詳細なブロック図を図８に示す。

【００６１】（キャッシュの動作）ここで、ＭＣバスよりメモリリード／ライト転送が要求された場合のキャッシュの動作を図８のブロック図と、図９及び図１０に示すフローチャートを用いて説明する。

【００６２】ＭＣバスよりデータ転送が開始されると、その転送の最初にＭＣバス上で示されるmTType[6:0]によって、その転送がキャッシュオンでおこなうか、オフでおこなうかの判断がおこなわれる。この説明では、転送がシングル転送であればオン、バースト転送であればオフと判断することにする（ステップＳ９０１）。すなわち、mTType(3)が“１”ｈであれば、シングル転送をあらわすのでキャッシュオンで、“０”ｈであればバースト転送をあらわすのでキャッシュオフで転送を行う。

【００６３】シングル転送（キャッシュオン）の場合、アドレスlmaddr[31:0]が与えられると、lmaddr[11:5]がインデックスとしてb1_tag_ram８０１，b2_tag_ram８０２，b1_data_ram７０２－ａ，b2_data_ram７０２－ｂ，lru８０３へ与えられ、それぞれのブロックから、入力されたインデックスに対応するバリッドビット"v"及びb1_tag_addr，バリッドビット"v"及びb2_tag_addr，b1_out_data，b2_out_data，lru_inがそれぞれ出力される（ステップＳ９０２）。

【００６４】b1_tag_ram８０１とb2_tag_ram８０２より出力されたb1_tag_addrとb2_tag_addrがそれぞれb1_comparater８０４，b2_comparater８０５でアドレスlmaddr[31:12]と比較され、その結果、すなわちヒットか否かがb1_hit_miss_L,b2_hit_miss_L信号によりキャッシュコントローラ７０６へ知らされ、判定される（ステップＳ９０３）。

【００６５】ここでヒットであれば、リードかライトかが判定される（ステップＳ９０４）。ヒットであるとは、b1_tag_addrとb2_tag_addrのいずれかにアドレスlmaddr[31:12]と一致するものがある場合である。ヒットかつリードの場合にはつぎのようになる。すなわち、b1がヒットであり、要求された転送がリードであった場合は、すでに読み出されているb1_out_dataとb2_out_dataのうちb1_out_dataを選択し、lmaddr[4:3]で示される8バイトのデータをＭＣバスへ出力する（ステップＳ９０５）。同時にそのインデックスに対応するlruを“０”(=b1ヒット)に書き換えて、転送が終了する。b2がヒットであり、要求された転送がリードであった場合は、すでに読み出されているb1_out_dataとb2_out_dataのうちb2_out_dataを選択し、lmaddr[4:3]で示される8バイトのデータをＭＣバスへ出力する（ステップＳ９０５）。同時にそのインデックスに対応するlruを“１”ｈ（=b2ヒット)に書き換えて、転送が終了する。

【００６６】一方、ヒットかつライトの場合にはつぎのようになる。すなわち、b1がヒットであり、要求された転送がライトであった場合は、インデックスで示されるb1_data_ram７０２－ａのlmaddr[4:3]で示される8バイトのデータのうちmBE_L[7:0]で示される有効なバイトレーンのみを書き換え、同時にそのインデックスに対応するlruを“０”ｈ(=b1ヒット)に書き換える。またＳＤＲＡＭも同様に書き換えて転送が終了する（ステップＳ９０６）。b2がヒットであり、要求された転送がライトであった場合は、インデックスで示されるb2_data_ram７０２－ｂのlmaddr[4:3]で示される8バイトのデータのうちmBE_L[7:0]で示される有効なバイトレーンのみを書き換え、同時にそのインデックスに対応するlruを“１”ｈ(=b2ヒット)に書き換える。またＳＤＲＡＭも同様に書き換えて転送が終了する（ステップＳ９０６）。

【００６７】一方、b1,b2ともにミスである場合にも、リードかライトか判定される（ステップＳ１００１）。要求された転送がリードであった場合は、そのlmaddr[31:3]で示される8バイトのデータがＳＤＲＡＭより読み出され（ステップＳ１００３）、ＭＣバスへ出力される（ステップＳ１００４）。同時にそのインデックスに対

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応するlruが読み出され、“０”ｈであった場合はb2_data_ramへＳＤＲＡＭからのデータを書きlruも“１”ｈへ書き換える。lruが“１”ｈであった場合はb1_data_ramへＳＤＲＡＭからのデータを書き、lruも“０”ｈへ書き換え終了する（ステップＳ１００５）。b1,b2ともにミスであり、要求された転送がライトであった場合は、ＳＤＲＡＭに書き込むだけで転送が終了する（ステップＳ１００２）。

【００６８】ステップＳ９０１においてバースト転送（キャッシュオフ）の場合、リード、ライトともＳＤＲＡＭに対してだけ行われ（ステップＳ９０７－Ｓ９０９）、キャッシュデータやタグの書き換え等は行わない。

＜ＲＯＭ／ＲＡＭインターフェース（７０７）＞ＲＯＭ／ＲＡＭコントローラ７０７の構成を図１１に示す。ブロック１１０１～ブロック１１０４により、ＳＤＲＡＭのデータ信号、アドレス信号、パリティ信号が、フラッシュＲＯＭのデータ信号、アドレス信号と多重化される。

【００６９】２．４．３．タイミングダイアグラム

上述したメモリコントローラ４０３によるデータの読み出し・書き込み等の処理のタイミングを、図１２～図１９を用いて説明する。

【００７０】図１２は、ＣＰＵからのバースト読み出しのタイミングを示す。バースト長は４、ＣＡＳレイテンシは３である。図９のステップＳ９０９における処理に相当する。

【００７１】図１３は、ＣＰＵからのバースト書き込みのタイミングを示す。バースト長は４、ＣＡＳレイテンシは３である。図９のステップＳ９０８における処理に相当する。

【００７２】図１４は、Ｇバスデバイスからのバースト読み出しのタイミングを示す。Ｇバスのバースト長は１６、ＳＤＲＡＭのバースト長は４、ＣＡＳレイテンシは３である。図９のステップＳ９０９における処理に相当する。

【００７３】図１５は、Ｇバスデバイスからのバースト書き込みのタイミングを示す。Ｇバスのバースト長は１６、ＳＤＲＡＭのバースト長は４、ＣＡＳレイテンシは３である。図９のステップＳ９０８における処理に相当する。

【００７４】図１６は、メモリフロントキャッシュにヒットした場合のシングル読み出しのタイミングを示す。読み出されるデータmDataIn[63:0]としては、キャッシュメモリであるb1_data_ram７０２－ａあるいはb2_data_ram７０２－bから読み出されたb1/b2_out_dataが出力される。ＳＤＲＡＭのバースト長は４、ＣＡＳレイテンシは３である。図９のステップＳ９０５における処理に相当する。

【００７５】図１７は、メモリフロントキャッシュにヒットしなかった場合のシングル読み出しのタイミングを示す。読み出されるデータmDataIn[63:0]としては、ＳＤＲＡＭから読み出されたデータramData[63:0]が出力される。また、このデータはb1/b2_in_dataとしてキャッシュメモリであるb1_data_ram７０２－ａあるいはb2_data_ram７０２－bにも書き込まれる。ＳＤＲＡＭのバースト長は４、ＣＡＳレイテンシは３である。図１０のステップＳ１００４及びＳ１００５における処理に相当する。

【００７６】図１８は、メモリフロントキャッシュにヒットした場合のシングル書き込みのタイミングを示す。書き込まれるデータmDataOut[63:0]は、キャッシュメモリであるb1_data_ram７０２－ａあるいはb2_data_ram７０２－bに書き込まれるとともに、ＳＤＲＡＭにも書き込まれる。ＳＤＲＡＭのバースト長は４、ＣＡＳレイテンシは３である。図９のステップＳ９０６における処理に相当する。

【００７７】図１９は、メモリフロントキャッシュにヒットしなかった場合のシングル書き込みのタイミングを示す。書き込まれるデータmDataOut[63:0]は、キャッシュメモリであるb1_data_ram７０２－ａあるいはb2_data_ram７０２－bには書き込まれず、ＳＤＲＡＭに対してだけ書き込まれる。ＳＤＲＡＭのバースト長は４、ＣＡＳレイテンシは３である。図１０のステップＳ１００２における処理に相当する。

【００７８】なお、ここでは、ＭＣバスよりデータ転送が開始されると、その転送の最初にＭＣバス上で示されるmTType[6:0]によって、転送がシングル転送であればオン、バースト転送であればオフと判断しているが、バースト転送の場合に、さらにバースト長を判定し、バースト長がキャッシュの１ラインよりも小さい場合にはキャッシュオンとし、そうでない場合にはキャッシュオフとして動作するようにしてもよい。

【００７９】また、ＭＣバスに、メモリへのデータ転送を要求したバスマスタの識別子を示す信号を含ませることで、メモリコントローラがその識別子を判定し、識別子に応じてキャッシュオン／キャッシュオフの制御を行うこともできる。この場合には、識別子とキャッシュオン／オフの別とを対応させた書換え可能なテーブルを用意し、それを参照してキャッシュのオンオフを切り替えることもできる。このテーブルは、例えば特定のアドレスを割り当ててＣＰＵ４０１などから書換え可能にすることもできる。

【００８０】２．５．システムバスブリッジ（ＳＢＢ）及びＩＯバス，Ｇバス

図２０としてシステムバスブリッジ（ＳＢＢ）４０２のブロック図を示す。

【００８１】ＳＢＢ４０２は、ＩＯバス（入出力バス），Ｇバス（グラフィックバス），Ｐバス（プロセッサローカルバス）及びＭＣバス間の相互接続をクロスバス

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イッチを用いて提供する、マルチチャネル双方向バスブリッジである。クロスバスイッチにより、２系統の接続を同時に確立することが出来、並列性の高い高速データ転送を実現出来る。

【００８２】ＳＢＢ４０２は、ＩＯバス４０５と接続するためのＩＯバスインターフェース２９０６と、Ｇバス４０４と接続するためのＧバスインターフェース２００６と、プロセッサコア４０１と接続するためのＣＰＵインターフェーススレーブポート２００２と、メモリコントローラ４０３と接続するためのメモリインターフェースマスターポートを備えるほか、アドレスバスを接続するアドレススイッチ２００３，データバスを接続するデータスイッチ２００４を含む。また、プロセッサコアのキャッシュメモリを無効化するキャッシュ無効化ユニット２００５を備えている。

【００８３】ＩＯバスインターフェース２００９には、ＩＯバスデバイスからのDMAライトを高速化するライトバッファと、ＩＯバスデバイスのリードを効率化するリードプリフェッチキューを実装する。これらのキュー内に一時的に存在するデータに関するコヒーレンシ管理はハードウェアにて行う。なお、ＩＯバスに接続されたデバイスをデバイスと呼ぶ。

【００８４】プロセッサコアは３２ビットバスに対するダイナミックバスサイジングをサポートしているが、ＳＢＢ４０２ではこれをサポートしない、将来、バスサイジングをサポートしないプロセッサを用いる場合にもＳＢＢに必要な改造を最小限におさえるためである。

【００８５】２．５．１．ＳＢＢ及び各バスの構成及び動作

＜ＩＯバスインターフェース＞図２１は、ＩＯバスインターフェースのブロック図である。

【００８６】ＩＯバスインターフェース２００９は、ＩＯバスとＭＣバス間の双方向ブリッジ回路である。ＩＯバスはＤｏＥｎｇｉｎｅの内部汎用バスである。

【００８７】ＩＯバスインターフェース２００９内には、マスタコントロールブロック２０１１、スレーブコントロールブロック２０１０、データインターフェース２０１２、DMAC２０１３、ＩＯバスバッファの５ブロックが含まれる。図２１上で、DMAC２０１３は、機能上３個のシーケンサとレジスタブロックに分割される。それら３つのシーケンサのうち、DMAメモリアクセスシーケンサはＩＯバススレーブコントロールブロック２０１０に、DMAｒｅｇシーケンサはＩＯバスマスターコントロールブロック２０１１に内蔵される。レジスタブロックであるDMAレジスタはＩＯバスデータインターフェース２０１２部に内蔵される。

【００８８】またＩＯバスインターフェース２００９はＩＯバス側からのメモリへの書き込み時、及びDMAによるデバイスからメモリへの転送が起こった時に、キャッシュ無効化インターフェースを介してCPUシェル内のデータ、命令両キャッシュの無効化の制御を行う。

【００８９】なお、CPUライト時のライトバックバッファはＩＯバスインターフェースには実装しないが、ＩＯバス上の外部マスタライト時のライトバッファを実装する。これにより、バースト転送でない、連続した外部マスタからの書き込みが高速化される。このライトバッファのフラッシュは、ＩＯバスアービタ４０７によるメモリへの接続が許された時点で行われる。ＩＯバスマスタリードのライトバッファバイパスは行わない。

【００９０】また、外部マスタのリードプリフェッチキューを実行する。これにより、外部マスタからの連続した、データストリームの読み出しの高速化を図る。リードバッファの無効化は、

１．ＩＯバスの新たなリードがバッファにヒットしなかった場合。

２．CPUからメモリへのライトが行われた場合。

３．Ｇバスからメモリへのライトが行われた場合。

４．ＩＯバスからメモリへのライトが行われた場合。

に行われる。

【００９１】またＩＯバスインターフェース２００９にはＩＯバス４０５上の各デバイスとメモリ間のDMAコントローラ２０１３が内蔵される。システムバスブリッジ４０２にDMAコントローラを内蔵することにより、ブリッジ双方へ、同時にアクセス要求が発行出来、効率的なDMA転送が実現出来る。

【００９２】ＩＯバスインターフェース２００９はプロセッサ４０１からのアクセス要求に対して、ダイナミックバスサイジングの使用を要求しない。またＩＯバスマスタからのメモリアクセス要求時に、メモリコントローラ４０３からのバスサイジングにも対応しない。すなわち、メモリコントローラはバスサイジングを期待すべきではない。

＜ＩＯバス＞

ＩＯバスはＤｏＥｎｇｉｎｅ内の汎用ＩＯバスであり、以下の仕様を持つ。

・アドレス、データ分離型３２ビットバス。

・任意のウェイトサイクルを挿入可能、最短はノーウェイト。

・バーストトランザクションのサポート。

・最大転送速度は、クロックが50MHz時に200Mbyte/Sec。

・バスエラーとバスリトライのサポート。

・複数バスマスタのサポート。

【００９３】（ＩＯバス信号定義）以下にバス信号の定義を説明する。各信号毎に、「信号名（英語呼称）：入力元＞出力先　（，3States）…信号の説明」の要領で記載されている。なお、３ステートの項は３ステートの信号に限り記載した。

【００９４】bAddr[31:2]（IOBus Address Bus）：Master>Slabe，3State…　IOBusアドレスバス。

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【００９５】bData[31:0] (IOBus Data Bus) ：DataDriver>DataReceiver, 3State … IOBusデータバス。

【００９６】b(Datadrivername)DataOeReq (IOBus Data Output Enable Request) ：Datadriver>DefaultDriverLogic … 後述する双方向ＩＯバスを実現するため、デフォルトドライバーコントロールロジックへの出力信号である。Datadrivernameを持つデバイスが、バス上にデータをドライブするための要求信号である。データの出力を許可されたデバイスには、デフォルトドライバーコントロールロジックよりb(Datadrivername)DataOe_Lが出力される。Datadriverの例：Pci,Sbb,Jpeg,Spu。

【００９７】b(Datadrivername)DataOe_L (IOBus Data Output Enable) ： dfaultDriverLogic>Datadriver … b(Datadrivername)DataOeReqを出力したデバイスに対し、デフォルトドライバーロジックがデータバスへのデータのドライブを許す場合b(Datadrivername)DataOe_L信号をそのデバイスに対して返す。

【００９８】bError_L (IOBus Bus Error) ：Slave>Master 3State … ＩＯバストランザクションがエラーで終了したことを示す。

【００９９】b(Mastername)BGnt_L (IOBus Grant) ：Arbiter>Master … バスアービトレーションにより当マスタがバスの使用権を得たことを示す。Masternameの例：Pci,Sbb,Jpeg,Spu。

【０１００】blnstNotData (IOBus Instruction/Data Output Indicator) ：Master>Slave, 3State … ＩＯバスマスタがインストラクションフェッチをＩＯバススレーブに対して行う場合にHighにドライブする。データトランザクションの場合はLowにドライブする。

【０１０１】b(Mastername)CntlOeReq (IOBus Master Control Output Enable Request) ：Master>DefaultDriverLogic … ＩＯバスマスタが、bStart_L,bTx_L,bWr_L,vInstNotDataとbAddr[31:2]を３ステートバス上にドライブしたい場合に、IOBus Output Control Logicに対してアサートする。IOBus Output Control Logic は各マスタからの、bMCntlOeReqに基づきドライブを許すマスタに対し、b(Mastername)CntlOe_L信号を返す。

【０１０２】b(Mastername)CntlOe_L (IOBus Master Control Output Enable) ：DefaultDriverLogic>Master … b(Mastername)CntlOeReqを出力したマスタに対し、デフォルトドライバーロジックがドライブを許す場合b(Mastername)CntlOe_L信号をそのマスタに対して返す。

【０１０３】bRdy_L (IOBus Ready) ：Slave>Master, 3State … ＩＯバススレーブは、現在のＩＯバスデータトランザクションが現在のクロックサイクルを最後に終了することを示すためにこの信号をアサートする。ＩＯバスマスタは、この信号により、現在のトランザクションがこのクロックサイクルで終了することを知る。

【０１０４】b(Mastername)BReq_L (IOBus Bus Request) ：Master>Arbiter … ＩＯバスマスタが、ＩＯバスアービタに対し、バスの使用権要求を行う事を示す。

【０１０５】bRetry_L (IOBus Bus Retry) ：Slave>Master 3State … ＩＯバススレーブがマスタに対し、バストランザクションの最実行を要求する。

【０１０６】b(Slavename)RdyOeReq (IOBus Slave Ready Output Enable Request) ：Slave>DefaultDriverLogic … ＩＯバススレーブが、bRdy_L,bWBurstReq_L,bBurstAck_Lを３ステートバス上にドライブしたい場合に、IOBus Output Control Logicに対してアサートする。IOBus DefaultDriverLogicは各マスタからの、b(Slavename)RdyOeReqに基づきドライブを許すスレーブに対し、b(Slavename)RdyOe_L信号を返す。

【０１０７】b(Slavename)RdyOe_L (IOBus Slave Ready Output Enable) ：DefaultDriverLogic>Slave … b(Slavename)RdyOeReqを出力したマスタに対し、デフォルトドライバーロジックがドライブを許す場合b(Slavename)RdyOe_L信号をそのマスタに対して返す。

【０１０８】bSnoopWait (IOBus Snoop Wait) ：SBB>NextMaster … ＩＯバスインターフェースがＩＯバスに接続された他のデバイスに対し、キャッシュのスヌーピング実行中であることを示す。ＩＯバスに接続されたデバイスはこの信号がアサートされている間は新たなトランザクションを発行できない。

【０１０９】bStart_L (IOBus Transaction START) ：Master >Slave 3State … ＩＯバスマスタがＩＯバストランザクションをスタートすることを示す信号、ＩＯバススレーブは、この信号を監視することにより、ＩＯバストランザクションのスタートを知ることが出来る。

【０１１０】bTx_L (IOBus Transaction Indicator Input) ：Master>Slave 3State …ＩＯバスマスタがＩＯバススレーブに対し、ＩＯバストランザクションが現在実行中である事を示すためにアサートする。

【０１１１】bWBurstGnt_L (IOBus Burst Write Grant) ：Master>Slave, 3State … ＩＯバスマスタが、ＩＯバスバーストライトのリクエストに対し、バーストライト実行することを示すためにドライブする。

【０１１２】bWBurstReq_L (IOBus Burst Write Request) ：Slave >Master, 3Stete …ＩＯバススレーブがＩＯバスマスタに対し、バースとライトを要求する場合にアサートする。

【０１１３】bWr_L (IOBus Write Transaction Indicater) ：Master>Slave, 3State …ＩＯバスマスタが、ＩＯバススレーブに対し、現在のトランザクションがライトである事を示すためにアサートする。

【０１１４】bByteEn[3:0] (IOBus Byte Enables) ：DataDriver>DataReceiver, 3State… ＩＯバス上にデータをドライブするエージェントが、各ビットに対応したbData[31:0]上のバイトレーンが有効である事を示すためにHighにドライブする。本信号の各ラインとbDataのバイトレーンは表４の対応関係にある。

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【０１１５】　＊　＊【表４】

Byte Enable	Corresponding bData [31 : 0]
bByte En3	[31 : 24]
bByte En2	[23 : 16]
bByte En1	[15 : 8]
bByte En0	[7 : 0]

【０１１６】bBurst_L（IOBus Extended Burst Request）：Master>Slave, 3Sate …　ＩＯバスマスタが拡張バーストを行いたい事を示す。アサート、ネゲートタイミングはbTx_Lと同一。

【０１１７】bBurstAck_L（IOBus Extended Burst Acknowledge）：Slave>Maste, 3State…　ＩＯバススレーブが拡張バーストを行える事を示す。アサート、ネゲートタイミングはbRdy_Lと同一。

※【０１１８】bBurstShortNotLong_L（IOBus Burst Length）：Master>Slave, 3State …ＩＯバスマスタが拡張バーストを行う場合のバースト長を示す。アサート、ネゲートタイミングはbTx_Lと同一であり、信号値とバースト長との対応は表５に示したとおりである。

【０１１９】

【表５】　※

bBurst Short Not Long_L	Burst Length
H	4 beats
L	8 beats

【０１２０】ＩＯバス信号は上述の通りである。ＤｏＥｎｇｉｎｅ内部のバスである、ＩＯバス（及びGバス）は接続される機能ブロック数が１０以上になるので、In Out分離バスですべてのブロックを接続することは、困難である。ＤｏＥｎｇｉｎｅでは、チップ内双方向バスを採用する。

＜Gバスインターフェース＞図２２にGバスインターフェース２００６のブロック図を示す。この概要は下記の通りである。

【０１２１】（Gバス概要）Gバスは、MFP用１チップコントローラＤｏＥｎｇｉｎｅ内部において、各画像データ処理部間のデータ転送を高速に実行するために定義されたバスである。６４ビットのデータバスをもち、4G byte(128byte boundary)のアドレス空間をサポートする。１６ビート(128byte=64ビット x 16) を１ロングバーストとした転送を基本とし、連続して４ロングバースト(512byte=16ビート x 4) までを可能とする。（シングルビートなど１６ビート以下の転送はサポートしない）

（Gバス信号定義）信号の定義に用いる記号をまず定めておく。信号名の直後には、必要に応じて信号の方向が記述されている。それは次のように定める。

In（Input signal）　…　バスエージェントに対する入力信号

Out（Output signal）　…　バスエージェントからの出力信号

InOut（Bi-Directional Tri-State signal）　…　双方向の信号で、複数のバスエージェントがドライブする。一度にひとつのエージェントだけがドライブする。信号をドライブする各エージェントのイネーブルリクエスト信号をデフォルトドライバで集中管理し、どのエージェントがドライブするかはデフォルトドライバが決定する。どのエージェントもイネーブルリクエストを出さない場合や、複数のエージェントが同時にイネーブルリクエストを出している場合はデフォルトドライバ信号をドライブする。エージェントは、信号をロウにドライブする場合は、前後１クロックの間ハイにドライブしなければならない。信号のアサートはドライブを初めてから１クロック以上経過してからしか行えない。基本的に信号のリリースはネゲートした次のクロックで行う。

【０１２２】なお、各信号名の後の“_L”はその信号がローアクティブであることを示す。信号の記述のしかたは、ほぼＩＯバス信号の記述に準ずる。説明は、システム信号、アドレス及びデータ信号、インターフェース制御信号、アービトレーション信号に分けて行う。また、バスエージェントとは、バスに接続されるバスマスタやバススレーブの総称である。

【０１２３】（システム信号）

gClk（G-Bus Clock）　…　Gバス上のすべてのトランザクションについてタイミングを提供し、すべてのデバイスに対して入力となる。

【０１２４】gRst_L（G-Bus Reset）　…　Gバス上のすべてのデバイスをリセットする。すべての内部レジスタはクリアーされ、すべての出力信号はネゲートされる。

【０１２５】（アドレスおよびデータ信号）

gAddr[31:7], InOut,（G-Bus Address）：Master>Slave …　Gバス上のデータ転送はすべて128byte（１６ビート）単位で行われるため、gAddr[31]～gAddr[7]の２５ビットで4Gbyteのアドレス空間をサポートする。

drive:gTs_Lと同時にマスターがドライブ

assert:ドライブした次のクロック

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negate:gAack_Lのアサートを確認したクロック。
【０１２６】g(Mastename)AddrOeReq (G-Bus Address OutPut Enable Request) :Master>DefaultDriverLogic … 双方向Gバスを実現するための、デフォルトドライバロジックへの出力信号。バスマスタがアドレスバスをドライブするための要求信号。
【０１２７】g(Masternname)AddrOe_L (G-Bus Address OutPut Enablet) :DefaultDriveLogic>Master … g(Masternname)AddrOeReqを出力したバスマスタに対し、デフォルトドライバロジックがアドレスバスのドライブを許可することを示す信号。
【０１２８】gData[63:0], InOut, (G-Bus Data) :DataDriver>DataReceiver … 64ビットデータバスで、ライト時はマスタがドライブ、リード時はスレーブがドライブ。
【０１２９】［ライト］drive:gTs_Lと同時にマスタがドライブ。ただし、gSlvBsy_Lがアサートされている時はネゲートされるまで待ってドライブ。
assert:ドライブした次のクロック。
change:gAack_Lのアサートを確認したクロック、その後は毎クロック。
negate:転送終了時、またはgTrStp_Lによる転送停止要求を確認した場合は、gAack_Lのアサートを確認したクロック。
【０１３０】［リード］drive：gAack_Lと同時にスレーブがドライブ。
assert:スレーブがReadyであればドライブした次のクロックで、Readyでなければreadyになるまで待ってアサートされる。
change:gAack_Lのアサートを確認したクロック、その後は毎クロック。リードの場合はアサートしたクロックから毎クロック。
negate:転送終了時。
release:ネゲートの１クロック後、またはgTrStp_Lによる転送停止要求を確認したクロック。
【０１３１】g(DataDrivername)DataOeReq (G-Bus Data OutPut Enable Request) :DataDriver>DefaultDriverLogic … データドライバがデータバスをドライブするための要求信号。
【０１３２】g(DataDrivername)DataOe_L (G-Bus Data OutPut Enablet) :DefaultDriverLogic>DataDriver … g(DataDrivername)DataOeReqを出力したデータドライバに対し、デフォルトドライバロジックがデータバスのドライブを許可することを示す信号。
【０１３３】（インターフェース制御信号）
gTs_L (InOut G-Bus Transaction Sart) :Master>Slave … マスターにより１クロックの間Lowにアサートされ、転送の開始（アドレスフェーズ）をあらわす。マスターはgTs_Lと共に、gAddr,gRdNotWr,gBstCntをドライブし、転送の種類、データ量を明確にする。マスタは、ライトの場合ここで明確にした転送データ量をウェイトなしで出せることを保証しなければならない。また、リードの場合は明確にした転送データ量をウェイトなしで受けることを保証しなければならない。スレーブは途中でデータ転送ができなくなった場合はgBsStep_Lにより、次の１６ビートの転送をキャンセルすることがある。ただし、１６ビートの途中でキャンセルすることはない。
drive:gGnt_Lのアサートを確認したクロックでドライブ。
assert:ドライブした次のクロック。
negate:１クロックアサート後にネゲートされる。
【０１３４】g(Masternname)TsOeReq (G-Bus Transaction Start OutPut Enable Request) :Master>DefaultDriverLogic … バスマスタがgTs_Lをドライブするための要求信号。
【０１３５】g(Masternname)TsOe_L (G-Bus Transaction Start OutPut Enablet) :DefaultDriverLogic>Master … g(Masternname)TsOeReqを出力したバスマスタに対し、デフォルトドライバクロックがgTs_Lのドライブを許可することを示す信号。
【０１３６】gAack_L, InOut, (G-Bus Address Acknowledge) :Slave>Master … スレーブにより１クロックの間Lowにドライブされる。該当するスレーブが、転送を認識し、バスが空いていることを確認して、データ転送がスタートできることをマスターに知らせる。ライトの場合、スレーブはマスタから要求された転送データ量をウェイトなしで受けることを保証しなければならない。またリードの場合は、要求された転送データ量をウェイトなしで出せることを保証しなければならない。万が一、途中でデータ転送ができなくなった場合は、gBstStp_Lにより、次の１６ビートの転送をキャンセルすることができる。ただし、１６ビートの途中でキャンセルすることはできない。
drive:アドレスデコードビット時、gTs_Lのアサートを確認したクロックでドライブが開始される。ただし、gSlvBsy_Lがアサートされている時はネゲートされるまで待ってドライブされる。また、データバス使用中のため、まだドライブされていなかった場合は、gTrStp_Lによる転送停止要求を確認したクロックでドライブ開始される。
assert:スレーブがReadyであればドライブした次のクロックで、Readyでなければreadyになるまで待ってアサートされる。gTrStp_Lによる転送停止に対する応答のときには、ドライブした次のクロックでアサートされる。
negate:ドライブ後にgTrStp_Lがアサートされた場合は、gTrStp_Lを確認したクロックでアサートされる。また、１クロックアサート後にネゲートされる。
【０１３７】g(Slavename)AackOeReq (G-Bus Address Acknowledge OutPut Enable Request) :Slave>DefaultD

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riverLogic … スレーブがgAack_Lをドライブするための要求信号。

【０１３８】g(Slavename)AackOe_L (G-Bus Address Acknowledge OutPut Enablet) ：DefaultDriverLogic>Slave … g(Slavename)AackOeReqを出力したスレーブに対し、デフォルトドライバロジックがgAack_Lのドライブを許可することを示す信号。

【０１３９】gSlvBsy_L, InOut, (G-Bus Slave Busy) ：Slave>Master … スレーブがドライブし、データバスでデータを転送中であることをあらわす。

drive：アドレスデコードヒット時、gTs_Lのアサートを確認したクロックでドライブ開始。ただし、gSlvBsy_Lがアサートされている時はネゲートされるまで待ってドライブ。

assert:スレーブがReadyであればドライブした次のクロックで、Readyでなければreadyになるまで待ってアサート。

negate:転送終了時にネゲート。

release:ネゲートの１クロック後、またはgTrStp_Lによる転送停止要求を確認したクロック。

【０１４０】g(Slavename)SlvBsyOeReq (G-Bus Slave Busy OutPut Enable Request) ：Slave>DefaultDriverLogic … スレーブがgSlvBsy_Lをドライブするための要求信号

g(Slavename)SlvBsyOe_L (G-Bus Slave Busy OutPut Enable) ：DefaultDriverLogic>Slave … g(Slavename)SlvBsyOeReqを出力したスレーブに対し、デフォルトドライバロジックがgSlvBsy_Lのドライブを許可すること ＊

＊を示す信号。

【０１４１】gRdNotWr, InOut, (G-Bus Read(High)/Write(Low)) ：Master>Slave … マスターによりドライブされ、HighでREAD、LOWでWRITEをあらわす。ドライブする期間はGAと同じである。

derive：gTs_Lと同時にマスターがドライブ。

assert：ドライブした次のクロック。

negate：gAack_Lのアサートを確認したクロック。

【０１４２】g(Masternname)RdNotWrOeReq (G-Bus Read/Write OutPut Enable Reques) ：Master>DefaultDriverLogic … バスマスタがgRdNotWrをドライブするための要求信号。

【０１４３】g(Masternname)RdNotWrOe_L (G-Bus Read/Write OutPut Enablet) ：DefaultDriverLogic>Master … g(Masternname)RdNotWrOeReqを出力したバスマスタに対し、デフォルトドライバロジックがgRdNotWrのドライブを許可することを示す信号。

【０１４４】gBstCnt[1:0], InOut, (G-Bus Burst Counter) ：Master>Slave … マスターによりドライブされ、連続して行うバースト転送の数（１～４）をあらわす。信号の値とバースト転送するバイト数との対応は表６のようになる。

derive：gTs_Lと同時にマスターがドライブ。

assert：ドライブした次のクロック。

negate：gAack_Lのアサートを確認したクロック。

【０１４５】

【表６】

gBst Cnt [1 : 0]		転送バイト数
01	16ビート×1	64bit×16×1＝128byte
10	16ビート×2	64bit×16×2＝256byte
11	16ビート×3	64bit×16×3＝384byte
00	16ビート×4	64bit×16×4＝512byte

【０１４６】g(Masternname)BstCntOeReq (G-Bus Burst Counter OutPut Enable Request) ：Master>DefaultDriverLogic … バスマスタがgBstCntをドライブするための要求信号。

【０１４７】g(Masternname)BstCntOe_L (G-Bus Burst Counter OutPut Enablet) ：DefaultDriverLogic>Master … g(Masternname)BstCntOeReqを出力したバスマスタに対し、デフォルトドライバロジックがgBstCntのドライブを許可することを示す信号。

【０１４８】gBstStp_L, InOut, (G-Bus Burst Stop) ：Slave>Master … スレーブによりドライブされ、連続する次のバースト転送を受付不可であることをあらわす。１バースト（１６ビート）の転送の１５ビート目にアサートする。ストップしない場合にはドライブしない。

drive：１４ビート目。

assert：１５ビート目。

negate：１クロックアサート後

g(Slavename)BstStpOeReq (G-Bus Burst Stop OutPut Enable Request) ：Slave> DefaultDriverLogic … スレーブがgBstStp_L上をドライブするための要求信号。

【０１４９】g(Slavename)BstStpOe_L (G-Bus Burst Stop OutPut Enablet) ：DefaultDriverlogic>Slave … g(Slavename)BstStpOeReqを出力したスレーブに対し、デフォルトドライバロジックがgBstStp_Lのドライブを許可することを示す信号。

【０１５０】（アービトレーション信号）

g(Masternname)Req_L, Out, (G-Bus Request) ：Master>Arbiter … マスターによりドライブされ、アービタに対してバスを要求する。各マスターデバイスごとに専用のgReq_Lを持つ。

assert：データ転送が必要なマスターがアサート

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negate：gGnt_Lを受ければネゲート
g(Mastername)Gnt_L, In, (G-Bus GNT) ：Arbiter>Master … アービタによりドライブされ、バス要求に対して次のバス権を与える。各マスタデバイスごとに専用のgGnt_Lを持つ。プライオリティーの高いバスマスタから順にバス権を与える。同じプライオリティーのマスタに対しては、バス要求のあった順番にバス権を与える。
assert：他のマスターにgGnt_Lを与えていない時、または次のクロックで他のマスタに与えていたgGnt_Lをネゲートする時に、アービトレーションによって選ばれたマスタに対してアサートする。
negate：gAack_Lのアサートを確認したクロック
gTrStp_L, In, (G-Bus Transuaction Stop) ：Arbiter>Master,Slave …アービタによりドライブされ、gGnt_Lによりすでにアドレスフェーズを開始されたトランザクションを中止する。ただ、すでにgAack_Lによりデータフェーズを開始してしまったトランザクションについては中止できない。また、この信号はgAack_Lによりマスクがかけられており、gAack_Lがアサートされた時には、たとえアサートしていてもネゲートされ出力される。
assert：すでにアドレスフェーズを開始したトランザクションよりも高いプライオリティのマスタからバス要求がきた時。
negate：gAack_Lのアサートを確認したクロック
（Gバスライトサイクル）Gバスのライトサイクルは次のようになる。
❶マスタがバス要求、gReq_Lアサート。
❷アービタが許可、gGnt_Lアサート。gReq_Lネゲート。
❸gGnt_Lを受けて、マスタはgTs_L,gAddr,gRdNotWr,gBstCnt,をドライブ。
ライト動作の場合、gSlvBsy_Lがアサートされていなければ、同時にgDataもドライブする。gSlvBsy_Lがドライブされていれば、gSlvBsy_Lがフリーになるのを待ってドライブする。
❹スレーブはgTs_Lがアサートされている時にアドレスをデコードし、ヒットすれば自分に対する転送であることを認識する。この時gSlvBsy_Lが他のスレーブによりアサートされていなければ、gSlvBsy_LとgAack_Lのドライブを始める。また、リードの場合はgDataもドライブする。gSlvBsy_Lが他のスレーブによりアサートされていれば、データバスは使用中であるということなので、ネゲートされるまで待ってドライブを始める。gSlvBsy_L,gAack_L,(gData)のドライブ開始後、スレーブがデータ転送の準備ができれば、それぞれの信号をアサートし、データ転送を開始する。
❺gAack_Lがアサートされた時点でアドレスフェーズは終了し、マスタはgAddr,gRdNotWr,gBstCntをネゲートする。また、その時点からマスタはライトデータを毎クロック切り替え、gBstCntで指定されたデータ量だけ転送

を行う。マスタとスレーブは、それぞれ自分でクロックをカウントして、データ転送の終了を知らなければならない。

【０１５１】スレーブは転送の途中でマスタから要求されたデータ転送量を転送できなくなった場合は、bStStp_Lを１５ビート目でアサートすることで、次の１６ビートの転送をキャンセルすることがただし、１６ビートの途中でキャンセルすることはできない。

【０１５２】マスタおよびスレーブは、gBstStp_Lがアサートされれば、次のクロックでデータの転送を終了させなければならない。

【０１５３】＜キャッシュインバリデーションユニット（ＣＩＵ）＞キャッシュインバリデーションユニット（以下CIU）２００５は、ＩＯバスからメモリへのライトトランザクションを監視し、これが起こった場合は、メモリへの書込が終了する前に、ＣＰＵシェルのキャッシュインバリデーションインターフェースを用い、ＣＰＵシェルに内蔵されたキャッシュの無効化を行う。

【０１５４】ＣＰＵシェルは、次の３種類の信号を使用する。

・SnoopADDR[31:5] (Cache Invalidation Address)
・DCINV (Dcache (データキャッシュ) Invalidation Strobe)
・ICINV (Icache (インストラクションキャッシュ) Invalidation Strobe)

キャッシュの無効化は最大３クロックで行われる、ＩＯバスからメモリへのライトは３クロックで終了することはないので、キャッシュインバリデーションユニット２００５は、CPUシェル４０１から出力されるStop_L信号を用いて無効化終了のハンドシェイクを行うことはしない。但し、将来の変更に備え、ＩＯバス上にはbSnoopWaitをStop_Lと同一サイクルだけドライブする。

【０１５５】なお、現在のインプリメンテーションでは、ＩＯバスからのライトが起こった場合は、安全のためにIcacheもインバリデーションしている、もし、ＯＳでセルフモディファイングコードを禁止し、インストラクションとして使われる可能性のあるデータのローディング時に、意図的にインストラクションキャッシュのインバリデーションを行うなら、Icacheのインバリデーションはいらない。この場合は若干のパフォーマンスアップが望める。

【０１５６】＜メモリマップ＞図２３及び図２４にメモリマップを示す。図２３は、左から順に、仮想メモリマップ、物理メモリマップ、Ｇバスのアドレス空間でのメモリマップ、ＩＯバスのアドレス空間でのメモリマップである。また、図２４は、レジスタ等を含む図２３における斜線部の５１２メガバイトを示すマップである。

【０１５７】プロセッサコアのメモリモデルはR3000をベースにしている。プロセッサコアの物理アドレス空間は３２ビットアドレッシングにより４Ｇバイトある。仮

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想空間も同様に３２ビットアドレッシングを行なう。ユーザープロセスの最大サイズは２Ｇバイトである。アドレスマッピングはカーネルモードとユーザーモードで異なる。図はＭＭＵを使用しない場合のメモリマップである。

【０１５８】（ユーザーモード仮想アドレッシング）ユーザーモードの仮想アドレッシングでは２Ｇバイトのユーザ仮想アドレス空間(kuseg)が有効となる。このユーザーセグメントのアドレスは0x00000000から始まり、すべての有効なアクセスは０にクリアされたmsbを持つ。ユーザーモードにおいてmsbをセットしたアドレスの参照はアドレスエラー例外処理を引き起こす。TLBはkusegへのすべての参照をユーザーモードとカーネルモードで同様にマッピングする。また、キャッシャブルである。kusegは通常ユーザーコードやデータを保持するために使用される。

【０１５９】（カーネルモード仮想アドレッシング）カーネルモードの仮想アドレス空間には４つのアドレスセグメントを持っている。

・kuseg　仮想アドレスの0x00000000から２Ｇバイト。ページと単位としたキャッシングとマッピングが可能。このセグメントはカーネルメモリアクセスとユーザーメモリアクセスでオーバーラップしている。

・kseg0　仮想アドレスの0x80000000から５１２Ｍバイト。物理メモリの最初の５１２Ｍバイトにダイレクトにマップされる。参照はキャッシュされるが、アドレス変換にはTLBは使われない。kseg0は通常カーネルの実行コードやカーネルデータのために使用される。

・kseg1　仮想アドレスの0xA0000000から５１２Ｍバイト。物理メモリの最初の５１２Ｍバイトにダイレクトにマップされる。参照はキャッシュされず、アドレス変換にはTLBは使われない。kseg1は通常ＯＳによって、I/Oレジスタ、ＲＯＭコード、ディスクバッファのために使用される。

・kseg2　仮想アドレスの0xC0000000から１Ｇバイト。kusegと同様、TLBにより仮想アドレスから物理アドレスにマップされる。キャッシングは自由。ＯＳは通常kseg2をスタックやコンテキストスイッチによるリマップが必要なプロセス毎のデータのために使用する。

【０１６０】（仮想アドレスメモリマップ（図２３（ａ），図２４（ａ））仮想アドレス空間は４Ｇバイトあり、システム上のすべてのメモリ、I/Oがアクセス可能である。kusegにはSYSTEM MEMORY(1GB)が存在する。

【０１６１】kseg0には内蔵ＲＡＭ(16MB)が存在する。これは、例外処理のベクタをプログラミングしたい場合にインプリメントし、例外ベクタベースアドレスを0x80000000に設定する。このアドレスは物理アドレス空間の0x00000000にマッピングされる。

【０１６２】kseg1にはＲＯＭ，Ｉ／Ｏ，レジスタが存在し、ブートＲＯＭ(16MB)，ＳＢＢ内部レジスタとＭＣ内部レジスタ(16MB)，IOBusI/01(16MB:Ｇバスアービタ内部レジスタ、ＩＯバスアービタ内部レジスタ、PMU内部レジスタなどのプリミティブなＩＯバスレジスタ)，IOBusI/02(16MB)，IOBusMEM(16MB)，Gbus MEM(32MB)，FONT ROM(240MB)、FONT ROM or RAM(16MB)が含まれる。

【０１６３】kseg2にはPCI I/O(512MB)，PCI MEM(512MB)が存在する。

【０１６４】kseg0，kseg1はどちらも物理アドレス空間の最初の512Mバイトにマッピングされるため、kseg0，kseg1とkusegの最初の512Mバイトはすべて同じ物理アドレス空間を参照していることになる。

【０１６５】（物理アドレスメモリマップ（図２３（ｂ），図２４（ｂ））物理アドレス空間も仮想アドレス空間と同様４Ｇバイトあり、システム上のすべてのメモリ、I/Oがアクセス可能である。

【０１６６】PCI I/O，PCI MEM，SYSTEM MEMORYについては仮想アドレスメモリマップと同一である。

【０１６７】kseg1，kseg2はどちらも物理アドレス空間の最初の512Mバイトにマッピングされるので、ROM，I/O，Regは0x00000000からの空間に存在している。

【０１６８】（Ｇバスメモリマップ（図２３（ｃ），図２４（ｃ））Ｇバスアドレス空間は４Ｇバイトあり、SYSTEM MEMORY，GBus MEM，FONTのみがアクセス可能である。

【０１６９】（ＩＯバスメモリマップ（図２３（ｄ），図２４（ｄ））ＩＯバスアドレス空間は４Ｇバイトあり、PCI I/O，PCI MEM，SYSTEM MEMORY，IOBusI/02，IOBus MEM，FONTのみがアクセス可能である。

【０１７０】IOBus I/01はプリミティブなレジスタのため、0x1C000000から0x20000000までの空間はPCIからプロテクトがかけられており、PCIからアクセスできない。

【０１７１】<アドレススイッチ>アドレススイッチ２００３は、Ｐバス，Ｇバス，ＩＯバス，ＭＣバス間のデータ転送を行なうために、マスターとなるバスからスレーブとなるバスへ、ＳＢＢ４０２を経由してアドレス信号を送るためのものである。ＳＢＢ４０２を経由する転送において、マスターとなり得るバスは、Ｐバス，Ｇバス，ＩＯバスであり、スレーブとなり得るバスはＩＯバス，ＭＣバスである。ＭＣバスに対してはＰバス，Ｇバス，ＩＯバス，のいずれかがマスターとなり、ＩＯバスへはＰバスのみがマスターとなってアドレス信号を送る。

【０１７２】また、Ｐバス-ＩＯバス間の転送と、Ｇバス-ＭＣバス間の転送は同時に行なうことができる。

【０１７３】図２５に、アドレススイッチ２００３のブロック図を示す。スイッチシーケンサ２００３ａにより、スイッチ２００３ｂを切り替えてスレーブをＩＯバスとＭＣバスとで切り換え、スイッチ２００３ｃを切り替えてマスタをＰバス，Ｇバス，ＩＯバスで切り換え

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る。この構成により、ＭＣバスに対してはＰバス,Ｇバス,ＩＯバス,のいずれかがマスターとなり、ＩＯバスへはＰバスのみがマスターとなり、また、Ｐバス-ＩＯバス間の転送と、Ｇバス-ＭＣバス間の転送は同時に行なうことができる。

【０１７４】<データスイッチ>データスイッチはＰバス,Ｇバス,ＩＯバス,ＭＣバス間のデータ転送を行なう際に,ＳＢＢ内でデータの流れを切り替えるものである。ライト時はマスターからスレーブ、リード時はスレ＊

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＊ーブからマスターへデータが送られる。

【０１７５】図２６にデータスイッチ２００４のブロック図を示す。この構成において、セレクタＡ－１～Ａ－３及びＢ－１，Ｂ－２を表７のように切り替えることで、Ｐバス，Ｇバス，ＩＯバスのいずれかをマスタとし、ＩＯバス，ＭＣバスのいずれかをスレーブとして、書き込みあるいは読み出しを行うように制御できる。

【０１７６】

【表７】

Master	Slave	W／R	Dataの流れ	Ａ－１	Ａ－２	Ａ－３	Ｂ－１	Ｂ－２
PBus	IOBus	Write	P→IO		b			
		Read	IO→P					b
	MCBus	Write	P→MC	b			a	
		Read	MC→P		a			a
Gbus	MCBus	Write	G→MC			a	b	
		Read	MC→G	a				
IOBus	MCBus	Write	IO→MC			b	b	
		Read	MC→IO		a			

【０１７７】<アービトレーション>ＳＢＢ４０２内のスイッチシーケンサ２００３ａは、各スイッチを切り替えるにあたって、ＳＢＢ外部からの以下の３種類の接続要求間のアービトレーションを行う。

１．ＣＰＵ

２．Ｇバスバスマスタ

３．ＩＯバスバスマスタ

このアービトレーションは、現在のバススイッチ接続状況、及び、あらかじめ設定された優先順位により決定され、その結果アドレススイッチ、データスイッチの接続が切り替えられる。

【０１７８】<タイミングダイアグラム>図２７～図３２にタイミング図を示す。図２７はＧバスからの書き込み／読み出しサイクルのタイミング図、図２８はＧバスのバースト停止サイクルのタイミング図、図２９～図３２は、Ｇバスのトランザクション停止サイクルのタイミング図である。

【０１７９】２．６．ＰＣＩバスインターフェース

図３３は、ＰＣＩバスインターフェース４１６のブロック図である。

【０１８０】PCIバスインターフェース４１６は、ＤｏＥｎｇｉｎｅ内部汎用IOバスであるＩＯバスと、チップ外部IOバスであるPCIバスの間をインターフェースするブロックである。入力ピン設定により、リセット時にPCIバスコンフィギュレーション発行可能な、ホストブリッジ構成と、PCIバスコンフィギュレーションは発行しないターゲット構成とを切り替えることができる。

【０１８１】ＩＯバスインターフェースのマスタDMAコントローラ３３０１は、PCIバスシグナルインターフェース３３０２を介してPCIバスマスタからＤｏＥｎｇｉｎｅ内部のリソースにアクセス要求があった場合に、ＩＯバスマスタとしてこのアクセス要求をＩＯバス内部にブリッジする。

【０１８２】更に、このマスタDMAコントローラ３３０１は、PCIバス上でマッピングされるメモリからＤｏＥｎｇｉｎｅMemoryへのDMA転送を行う事が出来る。この際、プログラマが意図したＩＯバスDMAと、ＧバスDMAのアクセスの順番を守って動作させるために、転送先アドレス(bPciAddr[31:0])と、PCIマスターコントローラ３３０１のID信号(bPciID)を、ＩＯバスとアービトレーションシーケンサに対して、バスリクエストと同時に発行する。

【０１８３】マスタDMAコントローラ３３０１はバスグラント(bPciBGnt_L)を受け取り、バスを使用しデータ転送が終了した時点で、ID信号(bPciID) のアサートを取りやめる。

【０１８４】なお、ＰＣＩバスは、33MHz,32ビット,PCI 2.1準拠とする。

【０１８５】２．７．Ｇバスアービタ

図３４は、ＧバスアービタＧＢＡ）４０６のブロック図である。

【０１８６】Ｇバスのアービトレーションは、中央アービトレーション方式であり、各バスマスタに対して専用のリクエスト信号(g(mastername)Req_L)とグラント信号(g(mastername)Gnt_L)を持つ。図３４は、masternameはM1～M4となっている。Busアービタ４０６は、Ｇバス上のバスマスタを４つまでサポートしており、以下のような特徴を持つ。

・アービタ内部のレジスタ３４０１ａの設定によりアービタをプログラミングすることが出来る。レジスタ設定

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はＩＯバスより行なう。

・すべてのバスマスタを同じ優先権として、公平にバス権を与える公平アービトレーションモードと、いずれかひとつのバスマスタの優先権を上げ、優先的にバスを使用させる優先アービトレーションモードがある。どのバスマスタに優先権を与えるかはレジスタ３４０１ｂの設定により決定される。

・優先バスマスタが連続してバスを使用することができる回数を設定することが可能。

・すでにアドレスフェーズを開始したが、データフェーズをまだ開始していないトランザクションについて、そのトランザクションをストップするためのトランザクションストップサイクルをサポート。

・複数のバスマスタにおける順序処理のプログラミングができる（後述）。プログラムされた順序は、レジスタテーブル３４０１ａに格納される。

・ＧバスマスタとＩＯバスマスタが同一メモリアドレスに順次書き込みを発行した場合に、プログラマの意図したアクセス順序を維持するための機構として、同期ユニットからのマスタID信号、ストップ信号に基づき、特定のマスタに対し、バス使用許可を与えることを保留する機構を持つ。

【０１８７】なお、レジスタへのプログラミングは、ＩＯバスを介してＣＰＵ４０１から行われる。

【０１８８】（アービトレーションシーケンサ）Ｇバスアービタの中核となるアービトレーションシーケンサ３４０２ａ，ｂは、１つの優先マスタとその他の４つの非優先マスタの間で５つのマスタによるアービトレーションを行なう。４つのバスマスタからのリクエスト信号とグラント信号を、リクエストディスパッチ回路３４０３とグラントディスパッチ回路３４０４によって４つの非優先マスタに割り付けることにより、公平アービトレーションモードが実現される。また、４つのバスマスタのうちのひとつを、高優先アービトレーションシーケンサ３４０２ａの優先マスタに割り付けることで、優先アービトレーションモードとして動作する。これらの割り付けは、レジスタ３４０１ａ，ｂの設定にしたがって行われる。これにより、優先バスマスタは、他のマスタより高い確率でバスの使用権を取得することが出来る。

【０１８９】さらに、バスの取得機会確率の調整に加え、高優先シーケンサ３４０２ａに割り当てられたマスタは、連続してバスを使用する事が出来、連続して使用出来る回数をプログラマブルなレジスタにより可変する事ができる。これは、バスの占有率を調整出来、ある特定のマスタにより多くバスを使用させる様に出来ることを意味する。

【０１９０】（公平アービトレーションモード）このモードでは、すべてのバスマスタは同じ優先順位にあり、バス権を与えられる機会は公平である。バスがフリーの時は、一番最初にリクエストを出したバスマスタがバス権を得ることができる。また、複数のバスマスタが同時にリクエストを出した場合は、あらかじめ決められた順序にしたがって順次バス権が与えられる（ラウンドロビン方式）。例えば、Ｍ１からＭ４までのすべてのバスマスタが同じクロックでリクエストを出した場合は、Ｍ１→Ｍ２→Ｍ３→Ｍ４といった順序でバス権が与えられる。Ｍ４のトランザクションの終了時に再びすべてのバスマスタがリクエストを出している場合は、Ｍ１→Ｍ２→Ｍ３→Ｍ４→Ｍ１→Ｍ２…というように、同様の順序でバス権を与えていく。一部のバスマスタがリクエストを出している場合は、Ｍ４からＭ１へラウンドラップするとして、最後にバスを使用したマスタにもっとも近い大きい番号を持ったマスタへグラントを与える。

【０１９１】一度バス権が他のバスマスタに移ると、他にリクエストを出しているすべてのバスマスタにバス権を与えた後でないと再びバス権を得ることができない。

【０１９２】（優先アービトレーション）このモードでは、ひとつのバスマスタ（レジスタ３４０１ｂに登録されたバスマスタ）が他のバスマスタよりも高い優先権を持つ優先バスマスタになり、他のバスマスタに比べ優先的にバス権が与えられる。優先バスマスタ以外のバスマスタの優先順位はすべて同じである。

【０１９３】複数のバスマスタがリクエストを出しており、また優先バスマスタが連続したリクエストを行う場合、優先バスマスタと他の非優先バスマスタは交互にバス権を得る。

【０１９４】非優先バスマスタから他のバスマスタにバス権が移ると、他にリクエストを出しているすべてのバスマスタにバス権を与えた後でないと、その非優先バスマスタは再びバス権を得ることができない。

【０１９５】（トランザクション・ストップ・サイクル）優先アービトレーションモードにおいて、優先バスマスタがリクエストを出した時、すでに他のバスマスタがアドレスフェーズを開始していても、データフェーズをまだ開始していなければ、そのトランザクションをストップし、優先バスマスタがバス権を得ることができる。ただし、その直前に優先バスマスタがバス権を持っていた場合は、連続したバス権を得ることができる回数を超えることはできない。

【０１９６】優先バスマスタのトランザクションが終了した時、中止されたバスマスタがリクエストを出していれば、優先してバス権が与えられる。

【０１９７】（優先バスマスタの切り替え）優先バスマスタの切り替えを行なうには、レジスタ３４０１ｂを書き換えればよい。優先バスマスタを選択するレジスタが書き換えられると、その時に実行中のトランザクションの終了を待って、優先バスマスタが切り替えられる。アービタのステートはアイドル状態にもどり、その時点でリクエストを出していたバスマスタは、その時同時にリクエストを出したものとして、あらためてアービトレー

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ションが行われる。

【０１９８】優先バスマスタの切り替えには十分注意を払う必要がある。優先させるべきバスマスタのDMAが終了しないうちに、異なったバスマスタに優先バスマスタを切り替えてしまうと、最初の優先バスマスタのDMAの優先度が下がってしまう。もしも最初の優先バスマスタの優先度を下げたくないのであれば、DMAが終了したのを確認してから優先バスマスタの切り替えを行なう必要がある。

【０１９９】優先バスマスタ切り替えを、システムブート時のみでなく、システム稼働中も動的に行う必要のあるソフトウェアでは、優先バスマスタの切り替えは、いったんＧバス上に新たなDMAリクエストが発生しないよう、すべてのバスマスタ及びDMAコントローラに対する設定を中止し、その後、Ｇバスアービタ４０６内のレジスタに適切な値をセットし、さらに、Ｇバスアービタ４０６内のステータスレジスタをチェックし、バスマスタの優先権が切り替わったのを確認した上で新たなＧバス上へのアクセス及びDMAの起動を行うべきである。

【０２００】優先バスマスタの動的切り替えは、オペレーティングシステムの実時間保証、タスクの優先順位の設定を変化もしくは違反させてしまう可能性があり、十分な考慮の上行われなければならない。

【０２０１】（順序処理）図３５は、ＤｏＥｎｇｉｎｅ４００内におけるＧバス４０４を中心とする、Ｇバス上のバスマスタによるDMAに係るブロック図である。

【０２０２】複数のバスマスタが順次に処理を行うことが必要な場合、例えば、メモリ３５０１上のデータに対して、バスマスタ１により処理Ａを行った後、バスマスタ２により処理Ｂを行い、その処理後のデータをバスマスタ４に送るといった一連の処理を考える。

【０２０３】この処理を行うソフトウェア、すなわちＣＰＵ４０１により実行されるプログラムにより、ＩＯバス４０５を介して、バスアービタ４０６内のレジスタテーブル３４０１ａに、バスマスタがバスを使用する順序と、バス権の付与の開始条件と、終了条件がセットされる。この例では、

バスマスタ	：	開始条件	：	終了条件
１．バスマスタ１	：	gM2BufEmpty	：	gM1BufReady
２．バスマスタ２	：	gM1BufReady	：	gM1BufEmpty
３．バスマスタ４	：	gM2BufReady	：	gM2BufEmpty

というようにセットする。すなわち、Ｇバスアービタ４０６は、それぞれのバスマスタから、開始条件として設定された信号を受けるとそのバスマスタにバス使用権を与え、終了条件として設定された信号を受けるとバス使用権を奪う。

【０２０４】ソフトウェアはそれぞれのバスマスタにDMAをセットする。それによって、それぞれのマスタはＧバスアービタ４０４に対してリクエスト(g(mastername)Req_L)を発行する。Ｇバスアービタ４０４はレジスタテーブル３４０１ａに登録された順序に従ってバスマスタ１にバス権を与える(gM1Gnt_L)。バスマスタ１はメモリ３５０１からある単位のデータをリードし、処理Ａを行って、バスマスタ１内部のバッファにデータをライトする。バスマスタ１はひとつの単位の処理が終了し、バッファの準備ができたことをgM1BufReady信号によりアービタ４０６に対して通知する。

【０２０５】アービタ４０６はそれを受け、レジスタテーブル３４０１ａに登録された、バスマスタがバス権を与える条件とバス権を奪う条件にしたがって、バス権をバスマスタ１から奪いバスマスタ２に与える。バスマスタ２はバスマスタ１のバッファのデータをリードし、処理Ｂを行って、バスマスタ２内部のバッファにデータを格納する。この間にバスマスタ１のバッファが空になるとgM1BufEmptyがアサートされ、アービタ４０６はバスマスタ２にバス権を与えていたのを取りやめる。バスマスタ２は処理Ｂを行って、バッファの準備ができるとgM2BufReady信号により通知する。

【０２０６】アービタ４０６はそれを受け、レジスタ３４０１ａの内容にしたがって、今度はバスマスタ４にバス権を与える。バスマスタ４はバスマスタ２のバッファからデータをリードする。バスマスタ２のバッファが空になると、gM2BufEmptyによってアービタ４０６に通知し、アービタ４０６はそれを受け、レジスタ３４０１ａの内容に従って再びバスマスタ１にバス権を与え、次のデータの処理を始める。

【０２０７】それぞれのバスマスタにセットされたDMAがすべて終了すると、それぞれのバスマスタはプロセッサに割り込みによって通知する。ソフトウェアはすべてのバスマスタからの終了通知がそろったとき、一連の処理が終了したことを知る。

【０２０８】以上説明した動作は完全順次モードでの動作であり、順次処理に関わるバスマスタ以外のバスマスタは、バスを使用することができない。この順次処理中でも、順次処理に関係のないバスマスタがバスを使用することを可能にするために優先順次モードが用意されている。これらのモードの切り替えではアービタ４０６内部のレジスタにプログラミングすることによって行なう。優先順次モードでは、順次処理を行なうバスマスタは優先的にバスを使用できるが、順次処理に関わらないバスマスタであればバスを使用することが許される。順次処理を行なうバスマスタと関わらないバスマスタの間のアービトレーションは、前述した優先アービトレーションモードと同等である。当然、順次処理に係わるバスマスタで、バス権を与えられる条件が満足されずに自分の順番が回ってきていないバスマスタにはバス権は与えられない。

【０２０９】（アクセス順序を維持するための機構）信号stopSpcがアサートされた場合は、Ｇバスマスタのひ

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とつであるスキャナプリンタコントローラ４０８はアービトレーションの対象から除外され、たとえリクエストをアサートしていてもバス使用権を与えられることはない。アービトレーションはこのマスタを除外したマスタ間で行われる。詳細な説明はＩＯバスアービタの節で行なう。

【０２１０】＜タイミングダイアグラム＞図３６～図３９において、Ｇバスアービトレーションのタイミングを説明する。図３６は、連続してバスを使用する回数が、バスマスタ１～４のすべてについて１に設定されている場合の公平アービトレーションモード（フェアモード）の例である。バスマスタ１による２回目の（タイミング４から出されている）バス要求は、バス要求を出している他のバスマスタがすべて１回ずつ処理されるまで待たされている。

【０２１１】図３７は、連続してバスを使用する回数が、バスマスタ１についてのみ２であり、他のバスマスタは１に設定されている場合の公平アービトレーションモードの例である。バスマスタ１が出している２回目の（タイミング４から出されている）バス要求は１回目の要求に続いて直ちに許可され、他のバスマスタはその処理がすむまで待たされている。

【０２１２】図３８は、連続してバスを使用する回数がそれぞれ１ずつであり、バスマスタ１が優先バスマスタと設定されている場合の優先アービトレーションモードの例である。優先バスマスタと非優先バスマスタとは交互にバス使用権が認められるために、バスマスタ１の２回目のバス要求はバスマスタ２のバスの使用後に認められており、バスマスタ４のバス要求は、バスマスタ１の２回目のバスの使用後に認められている。また、バスマスタ２の２回目のバス要求は、バス要求を出している他のすべてのバスマスタ、図３８ではバスマスタ１及びバスマスタ４のバス使用が終了した後で認められている。

【０２１３】図３９は、バスマスタ１からのバス要求により、バスマスタ４のバス要求が許可されているにもかかわらず中断された例である。この場合、バスマスタ１のバス使用が終了すると、バスマスタ２のバス要求に優先してバスマスタ４のバス要求が認められる。

【０２１４】２．８．ＩＯバスアービタ

図４０は、ＩＯバスアービタ４０７のブロックである。

【０２１５】ＩＯバスアービタ４０７は、ＤｏＥｎｇｉｎｅ内部のＩＯ汎用バスであるＩＯバス４０５のバス使用要求を受け付け、調停の後、使用許可を選択された一つのマスタに対して与え、同時に２つ以上のマスタがバスアクセスを行う事を禁止する。

【０２１６】アービトレーション方式は、３段階のプライオリティを持ち、それぞれのプライオリティに複数のマスタをプログラマブルに割り当てられる構成になっている。割り当ては、それぞれ最大で、最高のプライオリティに３マスタ、中間に７マスタ、最低レベルに３マスタとなる。

【０２１７】また、ＧバスマスタとＩＯバスマスタが、同一メモリアドレスに順次書き込みを発行した場合に、プロブラマの意図したアクセス順序を維持するための機構として、同期ユニットからの、マスタＩＤ信号、ストップ信号に基づき、特定のマスタに対し、バス使用許可を与えることを保留する機構を持つ。

【０２１８】（アービトレーションシーケンサ）ＩＯバスアービタは３つのアービトレーションシーケンサ４００２，４００３，４００４から構成される。それぞれ、高優先権、中優先権、低優先権を持ち、それぞれのシーケンサ内に、３，７，３本のバスマスタ用アービトレーションシーケンサが内蔵される。ＩＯバス上のすべてのバスマスタになる可能性のあるユニットからのリクエスト信号とそれらへのグラント信号を、リクエストセレクタとグラントセレクタによって、これらの３つのシーケンサユニットに分配する。この分配は、ＢＢｕｓインタフェース４００５内のソフトウェアプログラマブルなレジスタ４００５ａにより、複数の組み合わせのなかから、一意の組み合わせを選択することが出来る。

【０２１９】たとえば、最大７つのマスタのリクエストを中優先アービトレーションシーケンサ４００３に接続することにより、７つのマスタ間で公平なアービトレーションが実現される。また、バスマスタのうちのいくつかを、高優先アービトレーションシーケンサ４００２に割り付けることで、これらのマスタは他のマスタより、より高い確率でバスの使用権を取得することが出来る。さらに、いくつかのリクエストを低優先シーケンサ４００４に接続することで、これらのバスの使用率を低く抑える事が出来る。さらに、バスの取得機会確率の調整に加え、高優先シーケンサ４００２に割り当てられたマスタは、連続してバスを使用する事ができ、連続して使用出来る回数をプログラマブルなレジスタ４００５ａにより可変する事ができる。これは、バスの占有率を調整でき、ある特定のマスタにより多くの時間バスを使用させる様に出来る事を意味する。

【０２２０】（公平バスアービトレーション方式）中優先シーケンサ４００３を例にとり、公平アービトレーションの実現方法を説明する。一つのシーケンサに接続されたすべてのバスマスタは同じ優先順位にあり、バス権を与えられる機会は公平である。バスがフリーの時は、一番最初にリクエストを出したバスマスタがバス権を得ることができる（ファーストカムファーストサーブ）。また、複数のバスマスタが同時にリクエストを出した場合は、あらかじめ決められた順序にしたがって順次バス権が与えられる（同時リクエスト発行時ラウンドロビン）。例えば、Ｍ１からＭ７までのすべてのバスマスタが同じクロックでリクエストを出した場合は、Ｍ１→Ｍ２→Ｍ３→Ｍ４→Ｍ５→Ｍ６→Ｍ７といった順序でバス権が与えられる。Ｍ７のトランザクションの終了時に再

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びすべてのバスマスタがリクエストを出している場合は、Ｍ１→Ｍ２→Ｍ３→Ｍ４→Ｍ５→Ｍ６→Ｍ７→Ｍ１→Ｍ２というように、同様の順序でバス権を与えていく。一部のバスマスタがリクエストを出している場合は、Ｍ７からＭ１へラウンドラップするとして、最後にバスを使用したマスタにもっとも近い大きい番号を持ったマスタへグラントを与える。

【０２２１】（優先アービトレーション）ＩＯバスインターフェースは、高優先、中優先、低優先の３つのアービトレーションシーケンサが存在する。優先順位をつけたアービトレーションは、複数のバスリクエストを選択的に、高優先、低優先、のアービタに割り振ることにより実現される。

【０２２２】たとえば、ひとつのマスタを高優先に割り当て、残りを中優先に割り当てることにより、ひとつのバスマスタが他のバスマスタよりも高い優先権を持つ優先バスマスタになり、他のバスマスタに比べ優先的にバス権が与えられる。同じ優先権のアービトレーションシーケンサに割り当てられたバスマスタの優先順位はすべて同じである。

【０２２３】複数のバスマスタがリクエストを出しており、また優先バスマスタが連続してリクエストを行う場合、優先バスマスタと他のバスマスタは交互にバス権を得る。Ｍ３が優先マスタでＭ１，Ｍ２，Ｍ３，Ｍ４がリクエストを出し続けた場合Ｍ３→Ｍ１→Ｍ３→Ｍ２→Ｍ３→Ｍ４→Ｍ３→Ｍ１の順でバス使用権を与える。

【０２２４】また、高優先バスマスタは、アービタ内のプログラマブルなレジスタにあらかじめ設定された回数だけ連続したバス権を得ることができる。連続したバスを使用出来る回数は最大で４回である。

【０２２５】優先バスマスタ以外のバスマスタから他のバスマスタにバス権が移ると、そのバスマスタは、他にリクエストを出しているすべてのバスマスタにバス権を与えた後でないと再びバス権を得ることができない。ひとつのバスマスタが連続してリクエストを行う場合、他にリクエストを行っているバスマスタがいなければ、連続してバス権を得ることができるが、他のバスマスタがリクエストを行っていれば、そのバスマスタはあらかじめ設定された回数だけ連続してバス権を得ることができる。一度バス権が他のバスマスタに移ると、他にリクエストを出しているすべてのバスマスタにバス権を与えた後でないと再びバス権を得ることができない。

【０２２６】低優先アービトレーションシーケンサ４００４には最大３本のリクエストを割り当てる事が出来る。低優先シーケンサ４００４に割り当てられたマスタへは、中優先、高優先シーケンサに割り当てられた、すべてのマスタのリクエストがなくならないと、バスの使用権が与えられない。このシーケンサへのバスマスタの割り当ては十分な注意を持って行われなければならない。

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【０２２７】（優先バスマスタの切り替え）優先バスマスタの切り替えを行なうには、アービタ内のレジスタを書き換えればよい。優先バスマスタを選択するレジスタが書き換えられると、その時に実行中のトランザクションの終了を待って、優先バスマスタが切り替えられる。アービタのステートはアイドル状態にもどり、その時点でリクエストを出していたバスマスタは、その時同時にリクエストを出したものとして、あらためてアービトレーションが行われる。

【０２２８】切り替えには十分注意を払う必要がある。優先させるべきバスマスタのDMAが終了しないうちに、異なったバスマスタに優先バスマスタを切り替えてしまうと、最初の優先バスマスタのDMAの優先度が下がってしまう。もしも最初の優先バスマスタの優先度を下げたくないのであれば、DMAが終了したのを確認してから優先バスマスタの切り替えを行なう必要がある。

【０２２９】優先バスマスタ切り替えを、システムブート時のみでなく、システム稼働中も動的に行なう必要のあるソフトウェアでは、優先バスマスタの切り替えは、いったんＩＯバス上に新たなDMAリクエストが発生しないよう、すべてのバスマスタ及びDMAコントローラに対する設定を中止し、その後、ＩＯバスアービタ４０７内のレジスタに適切な値をセットし、さらに、ＩＯバスアービタ内のステータスレジスタをチェックし、バスマスタの優先権が切り替わったのを確認した上で新たなＩＯバス上へのアクセス及びDMAの起動を行うべきである。

【０２３０】優先バスマスタの動的切り替えは、オペレーティングシステムの実時間保証、タスクの優先順位の設定を変化もしくは、違反させてしまう可能性があり、十分な考慮の上行われなければならない。

【０２３１】（アクセス順序制御機構）ＩＯバスアービタ４０７はアクセス順序制御機構を含む。アクセス順序制御機構は、同期ユニット４００１と、ＩＯバスアービタ４０７，Ｇバスアービタ４０６内に組み込まれたバス使用権発行抑制機構によって実現される。ＩＯバスアービタ４０７内に組み込まれたバス使用権発行抑制機構は、Ｇバスアービタのそれと同様に動作する。つまり、stopPci信号が入力された場合は、Pciバスマスタからのバスリクエストが発行され、アービトレーションの結果、このマスタにバスの使用権を与えることが可能な状態でも、バスの使用権発行は行わず、他のマスタへバス使用権をあたえる。具体的には、stopPci信号が入力された場合は、直ちにbPciReq_Lをマスクすることにこれを行う。

【０２３２】LANコントローラ４１４からのバスリクエストおよび、ストップ信号の場合もまったく同様に動作する。図４１に同期ユニット４００１のブロック図を示す。同期ユニット内には複数のDMAマスタ間すべての組み合わせに関して、それぞれコンペアユニット４１０１～４１０３が接続される、ＤｏＥｎｇｉｎｅでは、Ｇbu

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s上のDMAマスタはスキャナ／プリンタコントローラ４０８のみ存在する。ＩＯバス上には、DMAPCIユニット、LANユニットの二つが存在する。ＳＢＢ内のＩＯバスインターフェースはＩＯバス上のバスマスタであるが、メモリには直接アクセスしないので、同期ユニット４００１にはＩＤと転送先アドレスを出力しない。

【０２３３】図４２に同期ユニット内の一つコンペアユニット（Comparation Unit 1)を以下に示す。他のコンペアユニットも同様の構成を有する。

【０２３４】PCIインターフェース４１６に付属するDMAブロックもしくは、スキャナ／プリンタコントローラ４０８から、同期ユニット４００１に対し、DMAライトがプログラミングされた時点で、転送先のアドレスとそのDMAブロック固有のリクエスト信号が通知される。

【０２３５】各コンペアユニットは、各DMAブロックからリクエストが出力された時点で、アドレスを内部に持つタイマによる現在時刻とともに記憶する、次に他のDMAブロックから、DMAライトに関するアドレスとリクエストが入力された時点で、コンペアユニットは両アドレスを比較する。一致した場合にはさらに、それぞれのレジスタに格納された時間を比較し、時間的に後からDMAライトの要求を出してきたDMAブロックが接続されたバスのバスアービタに対し、このマスタに対するバス使用強化を与えないようにする。これは、stop(ID)という信号により各バスのバスアービタに通知される。

【０２３６】各バスアービタはstop(ID)信号により通知されたマスタに対しては、アービトレーションによるバス使用権の割り当てを行わない。

【０２３７】時間が経過し、先にアクセス要求を行ったバスマスタにより当該メモリアドレスへのDMAライトが終了すると、先のマスタは、同期ユニットに対するリクエストを取り下げる、同期ユニットは、２番目にDMAライトの要求を出した、DMAブロックの接続するバスのバスアービタに対し、このDMAブロックへの、バス使用権許可禁止信号の発行をとりさげる。そして、後からDMAライトを行うべきマスタのDMAライトが行われる。

【０２３８】双方のDMAライトが終了し、双方のリクエストが取り下げられると、タイマーがリセットされる。タイマーのカウントアップは再度どちらかのマスタからのリクエストが出力された時点で再度行われる。

【０２３９】２．９．スキャナ／プリンタコントローラ
図４３は、スキャナ／プリンタコントローラ４０８のブロック図である。

【０２４０】図において、スキャナ／プリンタコントローラ４０８は、VideoI/Fによってスキャナおよびプリンタと接続され、内部バスGバスおよびＩＯバスにインターフェースするブロックである。大別して以下の８つのブロックから構成される。

１．スキャナ制御ユニット４３０３…ビデオI/Fを介してスキャナの動作制御を行う。

２．プリンタ制御ユニット４３０４…ビデオI/Fを介してプリンタの動作制御を行う。

３．スキャナ系画像処理ユニット４３０５…スキャナから入力される画像データに対して画像処理を行う。

４．プリンタ系画像処理ユニット４３０８…プリンタに出力する画像データに対して画像処理を行う。

５．スキャナ／ビデオ同期ユニット４３０６…スキャナから入力する画像データに対して、入力の同期タイミングを生成する。

６．プリンタ／ビデオ同期ユニット４３０７…プリンタに出力する画像データに対して、出力タイミングを生成する。プリンタとスキャナが同期可能な組み合わせの場合、スキャナ／ビデオ同期制御ユニット４３０６とともにコピー動作のビデオタイミングを生成する。

７．データ転送制御ユニット４３０２…データ転送の動作制御を行う。DMA動作ではマスターおよびスレーブの両動作をサポートする。

８．Gバス/ＩＯバス インターフェースユニット４３０１…GバスおよびＩＯバスとスキャナ、プリンタコントローラを接続するインターフェースユニットである。データ転送制御ユニット４３０２とLバスによって接続される。

【０２４１】＜スキャナ／ビデオ同期制御ユニット４３０６＞図４４にスキャナ／ビデオ同期制御ユニット４３０６のブロック図を示す。

【０２４２】（スキャナ／ビデオ同期制御ユニットの概要）スキャナ／ビデオ同期制御ユニット４３０６は、スキャナから入力される画像データの垂直同期信号（ＳＶＳＹＮＣ）、水平同期信号（ＳＨＳＹＮＣ）、画像データ同期クロック（ＳＶＣＬＫ）により、画像データの取り込みタイミング信号、画像処理のためのタイミング信号、転送バッファであるＦＩＦＯへ書き込みタイミング信号（ＳＣＦＷＲ）を生成する。

【０２４３】また、画像データの主走査方向の遅延、取り込みピクセル数、副走査方向の遅延、取り込みライン数を管理する。設定量の画像データ取込を終了したタイミングでの状態信号（ＳＡＬＬＥＮＤ）を生成する。ラインカウンタ４４０１は副走査方向の遅延と取り込みライン数を管理して、画像読み取り有効ラインの垂直同期信号（ＳＥＦＨＳＹＮＣ）を生成する。ピクセルカウンタ４４０２は主走査方向の画像取り込み遅延と取り込み画素数を管理する。取り込んだ画像データをＦＩＦＯに格納するための書き込みタイミング信号（ＳＣＦＷＲ）を生成する。ページカウンタ４４０３は入力される画像データページ単位で管理する。設定されたページ数分の画像データ入力を終了すると、終了信号（ＳＡＬＬＰＥＮＤ）を生成する。

【０２４４】ラインカウンタ４４０１，ピクセルカウンタ４４０２，ページカウンタ４４０３の各設定値はコントロールレジスタ４３１０によって読み書きされる。

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・ライトデータ　　：ＩＦＷＤＡＴＡ[31:0]
・リードデータ　　：ＩＦＲＤＡＴＡ[31:0]
・ラインカウンタライト信号　：ＳＬＣＳＥＴ
・ラインカウンタリード信号　：ＳＬＣＲＤ
・ピクセルカウンタライト信号：ＳＰＣＳＥＴ
・ピクセルカウンタリード信号：ＳＰＣＲＤ
・ページカウンタライト信号　：ＳＰＡＧＥＳＥＴ
・ページカウンタリード信号　：ＳＰＡＧＥＲＤ

＜プリンタ／ビデオ同期制御ユニット４３０７＞図４５は、プリンタ／ビデオ同期制御ユニット４３０７のブロック図である。

【０２４５】（プリンタ／ビデオ同期制御ユニットの概要）プリンタ／ビデオ同期制御ユニット４３０７は、プリンタから入力される画像データの垂直同期信号（ＰＶＳＹＮＣ）、水平同期信号（ＰＨＳＹＮＣ）、画像データ同期クロック（ＰＶＣＬＫ）により、画像データの取り込みタイミング信号、画像処理のためのタイミング信号、転送バッファであるＦＩＦＯからの読み出しタイミ＊

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＊ング信号（ＰＲＦＲＤ）を生成する。

【０２４６】また、画像データの主走査方向の遅延、取り込みピクセル数、副走査方向の遅延、取り込みライン数を管理する。設定量の画像データ取り込みを終了したタイミングでの状態信号（ＰＬＥＮＤ）を生成する。ラインカウンタ４５０１は副走査方向の遅延と出力ライン数を管理して、画像出力有効ラインの垂直同期信号（ＰＥＦＨＳＹＮＣ）を生成する。ピクセルカウンタ４５０２は主走査方向の画像出力遅延と出力画素数を管理する。出力画像データをＦＩＦＯから読み出すための読み出しタイミング信号（ＰＲＦＲＤ）を生成する。ページカウンタ４５０３は出力数画像データをページ単位で管理する。設定されたページ数分の画像出力が終了すると、終了信号（ＰＡＬＬＰＥＮＤ）を生成する。

【０２４７】ラインカウンタ４５０１,ピクセルカウンタ４５０２,ページカウンタ４５０３の各設定値はコントロールレジスタ４３１０によって読み書きされる。

・ライトデータ　　：ＩＦＷＤＡＴＡ[31:0]
・リードデータ　　：ＩＦＲＤＡＴＡ[31:0]
・ラインカウンタライト信号　：ＰＬＣＳＥＴ
・ラインカウンタリード信号　：ＰＬＣＲＤ
・ピクセルカウンタライト信号　：ＰＰＣＳＥＴ
・ピクセルカウンタリード信号　：ＰＰＣＲＤ
・ページカウンタライト信号　：ＰＰＡＧＥＳＥＴ
・ページカウンタリード信号　：ＰＰＡＧＥＲＤ

＜スキャナＦＩＦＯコントローラ４３１１＞図４６は、スキャナＦＩＦＯコントローラのブロック図である。スキャナＦＩＦＯコントローラ４３１２（図４３参照）は、スキャナから入力された画像データをＧバスもしくはＩＯバスを介して転送するためのバッファとしてのＦＩＦＯと、そのＦＩＦＯをコントロールする回路を含む。容量1024バイト、データ幅24ビット（Ｒ，Ｇ，Ｂ各8ビット）の2系統のＦＩＦＯ４６０２，４６０３を備える。これらのＦＩＦＯは、Ｇバス/ＩＯバスのデータ転送動作とスキャナからの画像データ入力動作を交互に行うダブルバッファとして動作する。ＦＩＦＯのデータ入出力は、スキャナＦＩＦＯセレクタ４６０１がＦＩＦＯのフルフラグ（ＦＦ）とエンプティーフラグ（ＥＦ）により制御する。

【０２４８】＜プリンタＦＩＦＯコントローラ４３１２＞図４７は、プリンタＦＩＦＯコントローラ４３１２（図４３）のブロック図である。プリンタＦＩＦＯコントローラ４３１２は、プリンタへ出力する画像データをＧバスもしくはＩＯバスを介して転送するためのバッファとしてのＦＩＦＯと、そのＦＩＦＯをコントロールする回路を含む。容量1024バイト、データ幅24ビット（Ｒ，Ｇ，Ｂ各8ビット）のＦＩＦＯを2系統備える。これらは、Ｇバス/ＩＯバスのデータ転送動作とプリンタへの画像データ出力動作を交互に行うダブルバッファーとして動作する。ＦＩＦＯのデータ入出力は、プリンタＦＩＦＯセレクタ４７０１がＦＩＦＯのフルフラグ（ＦＦ）とエンプティーフラグ（ＥＦ）により制御する。

【０２４９】スキャナプリンタコントローラ４０８は、スキャナとプリンタとを同期動作させ、コピー動作をおこなうために、図４３に示すように、スキャナデータを直接プリンタへ出力するデータパスを備える。また、スキャナからの入力データとプリンタへの出力データをＦＩＦＯにより同期させるデータパスも備える。それらのデータパスはスキャナとプリンタのデータ入出力の同期関係で選択可能とする。

【０２５０】＜データ転送制御ユニット４３０２＞図４８は、データ転送制御ユニット４３０２のブロック図である。データ転送制御ユニット４３０２は、Ｌバスへのデータの入出力を制御するブロックで、チェインコントローラ４８０１、マスタDMAコントローラ４８０２、転送アービタ４８０３等を含む。

【０２５１】データ転送制御ユニットは、マスタとしては以下の動作を制御する。

１．スキャナからの画像データDMA転送およびチェインテーブル参照

２．プリンタへの画像データDMA転送およびチェインテーブル参照

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スレーブとしては以下の動作を制御する。
１．内部レジスタのライト・リード
２．スキャナからの画像データ転送
３．プリンタへの画像データ転送
（チェインコントローラ）図４９は、チェインコントローラ４８０１のブロック図である。チェインコントローラは、チェインテーブルを示すアドレスポインタブロックとDMAの転送先を示すアドレスポインタブロックから構成される。スキャナ、プリンタコントローラがマスタとしてDMAを行う際の転送先アドレス発生ブロックであり、チェインDMAをサポートする。スキャナデータ転送、プリンタデータ転送の２系統が独立で動作する。
【０２５２】＜Ｌバス＞Ｇバス/ＩＯバスインターフェースユニットとデータ転送ユニットを接続するスキャナ、プリンタコントローラ内のローカルなバスである。次のような信号を含む。なお、以下、信号の入出力は、データ転送制御ユニット４３０２からＧバス/ＩＯバスインターフェースユニット４３０１に出力する信号をOUT、Ｇバス/ＩＯバスインターフェースユニット４３０１からデータ転送制御ユニット４３０２に入力する信号をINで示す。
・IFCLK （IN）… Ｌバスの基本クロック
・IFRDATA[63:0]（OUT）… データ転送制御ユニットからＧバス/ＩＯバスインターフェースユニットに出力される64ビットのデータバスである。データ転送制御ユニットがマスタとスレーブのどちらの動作においても使用される。
・IFWDATA[63:0]（IN）… Ｇバス/ＩＯバスインターフ

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＊ェースユニット からデータ転送制御ユニットに出力される64ビットのデータバスである。データ転送制御ユニットがマスタとスレーブのどちらの動作においても使用される。
・IFMDTREQ（OUT）… データ転送制御ユニットがマスタとしてデータ転送の要求とデータおよびアドレスの有効状態を示す。“High”でデータの転送要求とアドレスバスIFMAD[3:12]の有効状態を示す。
・IFMAD[31:2]（OUT）… データ転送制御ユニットがマスタ動作時、目的アドレスを示すアドレスバス。IFMDTREQ信号がアクティブ状態“High”で有効なアドレスを出力する。
・IFMRW（OUT）… データ転送制御ユニットがマスタ動作時、データの入出力を示す信号。“High”のときデータ転送制御ユニットはIFWDATA[63:0]からデータを入力する。“Low”のときデータ転送制御ユニットはIFRDATA[63:0]にデータを出力する。
・IFMDTACK（IN）… データ転送制御ユニットがマスタ動作時、IFMDTREQに対する応答信号、Ｇバス/ＩＯバスインターフェースユニットから出力される。“High”のときIFRDATA[63:0）またはIFWDATA[63:0]が有効データであることを示す。
・PRIOR[3:0]（OUT）… データ転送制御ユニットがマスタ動作時、データ転送の優先度を示す。優先度は表８のように定義される。
【０２５３】
【表８】

PRIOR3	PRIOR2	PRIOR1	PRIOR0	優先度
1	1	1	1	高 い
1	1	1	0	↑
		⋮		
0	0	0	1	↓
0	0	0	0	低 い

【０２５４】・MTSIZE[2:0]（OUT）… データ転送制御ユニットがマスタ動作時、転送の単位サイズを示す。この単位サイズの転送中、IFMDTREQは“High”のアクティ※ ※ブ状態のままとなる。サイズは表９のように示される。
【０２５５】
【表９】

MSIZE2	MSIZE1	MSIZE0	転送単位サイズ
1	1	1	64bit × 64
1	1	0	64bit × 48
1	0	1	64bit × 32
1	0	0	64bit × 16
0	1	1	64bit × 4
0	1	0	64bit × 2
0	0	1	64bit
0	0	0	32bit

【０２５６】・IFSDTREQ（IN）… データ転送制御ユニ ットがスレーブ動作時、Ｇバス/ＩＯバスインターフェ

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ースユニットからのデータ転送要求とデータおよびアドレスの有効状態をしめす。“High”でデータ転送要求とアドレスバスIFSAD[6:2]の有効状態を示す。

・IFSAD[6:2]（IN）…　データ転送制御ユニットがスレーブ動作時、目的アドレスを示すアドレスバス。IFSDTREQ信号がアクティブ状態“HIGH”で有効なアドレスを出力する。

・IFSRW（IN）…　データ転送制御ユニットがスレーブ動作時、データの入出力を示す信号。“High”のときデータ転送制御ユニットはIFRDATA[63:0]にデータを出力する。“Low”のときデータ転送制御ユニットはIFWDATA[63:0]からデータを入力する。

・IFSDTACK（OUT）…　データ転送制御ユニットがスレーブ動作時、IFSDTREQに対する応答信号。データ転送制御ユニットから出力される。“High”のときIFRDATA[63:0]またはIFWDATA[63:0]が有効データであることを示す。

・STSIZE（IN）…　データ転送制御ユニットがスレーブ動作時、Gバス/ＩＯバスインターフェースユニットからのデータ幅を示す。“High”でIFRDATA[63:0]またはIFWDATA[63:0]が有効となる。“Low”でIFRDATA[31:0]またはIFWDATA[31:0]が有効となる。

【０２５７】＜Gバス／ＩＯバスインターフェースユニット＞図５０は、Gバス/ＩＯバスインターフェースユニット４３０１のブロック図である。Gバス/ＩＯバスインターフェースユニットは、コピーエンジン内部の内部バス（Ｌバス）と外部バス(Gバス/ＩＯバス)とのインターフェース部分である。このユニットは、他の機能ブロックで使えるように実現されるが、本実施の形態ではコピーエンジンが使用する。なお、コピーエンジンとは、スキャナ／プリンタコントローラ４０８及びそれにより制御されるスキャナとプリンタとを含めた総称である。

【０２５８】Gバス/ＩＯバスインターフェースユニットは、大きくバスセレクタユニット，ＩＯバスコントローラ５００２，Gバスコントローラ５００３の三つの部分から構成される。

【０２５９】バスセレクタユニット５００１は、コピーエンジンがDMAマスタの時には、Ｌバスのバースト転送可能な転送量、優先度（緊急度）、転送先のアドレスと、さらに各バス(GバスとＩＯバス）の空き情報を基にして、動的にバスの選択を行い、対応するコントローラ（Gバスコントローラ５００３かＩＯバスコントローラ５００２）に、多少の前処理を施してＬバスを接続する。コピーエンジンがDMAスレーブの時には、各バス（GバスとＩＯバス）からの要求を調停し、優先順位の高いバスとＬバスを接続する。

【０２６０】Gバスコントローラ５００３とＩＯバスコントローラ５００２は、Ｌバスと対応するバス（GバスとＩＯバス）のバスの変換を行う。以下に、各部の説明をする。

【０２６１】コピーエンジンは、Gバス/ＩＯバスの両方のバスに対してDMA可能なDMAマスタであり、Gバス/ＩＯバスインターフェースユニット４３０１は、DMA転送する際に使用するバスを決定する。従来のシステムでは、転送先（アドレス）によりバスを切り替えているが、各バスの転送速度や使用率等を考慮しなければ、システム全体として良い性能が得られない。

【０２６２】バスセレクタユニット５００１は、Ｌバスのバースト転送可能な転送量、優先度（緊張度）、転送先のアドレスと、さらに各バス（GバスとＩＯバス）の空き情報を基にして、動的に効率的なバスの選択を行い、対応するコントローラ(Gバスコントローラ５００３かＩＯバスコントローラ５００２）に、多少の前処理を施して、Ｌバスを接続する。

【０２６３】Gバスコントローラ５００３とＩＯバスコントローラ５００２は、Ｌバスと対応するバス（GバスとＩＯバス）同期ユニットへ、書き込みアドレスと機能ブロック（ここでは、コピーエンジン）のＩＤを送り出す。以下に、各部の説明をする。

【０２６４】（バスセレクタユニット）図５１は、バスセレクタユニット５００１のブロック図である。その動作を以下に説明する。

[コピーエンジンのマスター時の動作] コピーエンジンがマスターの場合は、主に、バスセレクタユニットのＬバスマスタシーケンサ５１０１で制御される。Ｌバスマスタシーケンサ５１０１は、コピーエンジンからIFMDTREQ（マスターデータ要求信号）を受けることにより、コピーエンジンのマスター動作の要求を知る。

【０２６５】コピーエンジンは、IFMDTREQアサートと同時に、IFMAD[31:2]（マスター転送アドレス信号）、MTSIZE[2:0]（マスター転送長信号）、IFMRW（マスター・リード・ライト信号）をバスセレクタユニット５００１に出力する。転送アドレスはアドレスカウンタ５１０２に、転送長は長さカウンタ５１０３に、それぞれラッチされる。

【０２６６】Ｌバスマスタシーケンサ５１０１は、外部バストの転送を開始する時点でGバスを使用するか、ＩＯバスを使用するかを、アドレスカウンタ，長さカウンタ，プライオリティ，各バスのビジー状態から決定する。アドレスカウンタの下位ビット５がすべて０ではない場合、あるいは長さカウンタが６４ビット×４未満の場合は、Gバスでの転送は不可能なので、ＩＯバスを選択する。それ以外は、高プライオリティかつGバスが使用中かつＩＯバスが空いている、という場合を除き、Gバスを選択する。外部バスへの転送サイクルを終了した時点で、アドレスカウンタ５１０２と長さカウンタ５１０３を更新し、長さカウンタが０でなければ、上記の動作を繰り返す。バスの選択の基準を表１０に示す。

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【表１０】

アドレスカウンタ［4：0］＝0 & 長さカウンタ≧64bit×4	プライオリティ	バスの状態		選択するバス
		IOバス	Gバス	
No	—	—	—	IOバス
Yes	低　い	—	—	Gバス
	高　い	Ready	Ready	Gバス
		Ready	Busy	IOバス
		Busy	Ready	Gバス
		Busy	Busy	Gバス

【０２６８】コピーエンジンから外部バスへの転送では、Ｌバスマスタシーケンサ５１０１は、データＦＩＦＯ５１０４がフルでない限り、コピーエンジンへIFMDTACK信号をアサートし、転送データを要求し、得たデータをＦＩＦＯ５１０４に書き込む。また、データＦＩＦＯがエンプティでない限り、外部バスコントローラ（ＩＯバスコントローラ５００２かＧバスコントローラ５００３）へマスター転送要求信号（LbMReqかLgMReq）をアサートし、データ転送を要求する。外部バスコントローラ（ＩＯバスコントローラかＧバスコントローラ）は、データＦＩＦＯ５１０４のデータを転送し、転送終了で、マスター転送通知信号（LbMAckかLgMAck）をアサートするので、Ｌバスマスタシーケンサ５１０１は、外部バスへの転送の終了を知ることができる。

【０２６９】外部バスからコピーエンジンへの転送では、Ｌバスマスタシーケンサ５１０１は、データＦＩＦＯがフルでない限り、外部バスコントローラ（ＩＯバスコントローラかＧバスコントローラ）へマスター転送要求信号（LbMReqかLgMReq）をアサートし、データ転送を要求し、データをデータＦＩＦＯに書き込み、データＦＩＦＯがエンプティでない限り、コピーエンジンへIFMDTACK信号をアサートし、転送データを要求し、得たデータＦＩＦＯのデータを書き込む。

【０２７０】（ＩＯバスコントローラ）図５２は、ＩＯバスコントローラ５００２のブロック図である。

【０２７１】ＩＯバスコントローラ５００２は、ＬバスとＩＯバスのインターフェース部分である。

【０２７２】ＩＯバスマスタシーケンサ５２０１は、ＩＯバスマスター時の動作を、ＩＯバススレーブシーケンサ５２０２は、ＩＯバススレーブの時の動作を、それぞれ制御する。

［コピーエンジンのマスター時の動作］バスセレクタユニット５００１からのLbMReq信号のアサートにより、データ転送は開始される。転送の方向は、LbMReq信号と同時にアサートされるバスセレクタユニット５００１からのLbMRdNotWr信号により決まる。転送のサイズは、LbMReq信号と同時にアサートされるバスセレクタユニット５００１からのLbBstCnt[1:0]信号により決まる。また、転送のアドレスはLbMReq信号と同時にアサートされるバスセレクタユニット５００１からのLbMAddr[31:2]信号により決まる。

【０２７３】ＩＯバスからの転送(LbMRdNotWr信号が０の時）は、読み込み用データＦＩＦＯがフルであれば（bRFifoFullがアサート）、フルでなくなるのを待ち、ＩＯバスマスタシーケンサは、決められたＩＯバスの転送を開始し、得たデータは、バスセレクタユニット５００１ のデータＦＩＦＯに書き込む。

【０２７４】ＩＯバスへの転送（LbMRdNotWr信号が１の時）は、書き込み用データＦＩＦＯがエンプティであれば（bWFifoEmptがアサート）、エンプティでなくなるのを待ち、ＩＯバスマスタシーケンサは、決められたＩＯバスの転送を開始し、バスセレクタユニット５００１のデータＦＩＦＯから得たデータをＩＯバス上に送る。

【０２７５】（Ｇバスコントローラ）図５３は、Ｇバスコントローラ５００３のブロック図である。

【０２７６】Ｇバスコントローラ５００３は、ＬバスとＧバスのインターフェース部分である。

【０２７７】Ｇバスマスタシーケンサ５３０１は、Ｇバスマスター時の動作を、Ｇバススレーブシーケンサ５３０２は、Ｇバススレーブの時の動作を、それぞれ制御する。

［コピーエンジンのマスター時の動作］バスセレクタユニット５００１からのLbMReq信号のアサートにより、データ転送は開始される。転送の方向は、LbMReq信号と同時にアサートされるバスセレクタユニット５００１からのLbMRdNotWr信号により決まる。転送のサイズは、LbMReq信号と同時にアサートされるバスセレクタユニット５００１からのLbBstCnt[1:0]信号により決まる。また、転送のアドレスはLbMReq信号と同時にアサートされるバスセレクタユニット５００１からのLbMAddr[31:2]信号により決まる。

【０２７８】Ｇバスからの転送(LgMRdNotWr信号が０の

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時）は、読み込み用データＦＩＦＯがフルであれば（gR FifoFullがアサート）フルでなくなるのを待ち、Ｇバスマスタシーケンサは、決められたＧバスの転送を開始し、得たデータは、バスセレクタユニット５００１のデータＦＩＦＯに書き込む。

【０２７９】Ｇバスへの転送（LgMRdNotWr信号が１の時）は、書き込み用データＦＩＦＯがエンプティであれば（bWFifoEmptがアサート）、エンプティでなくなるのを待ち、Ｇバスマスタシーケンサは、決められたＧバスの転送を開始し、バスセレクタユニット５００１のデータＦＩＦＯから得たデータをＧバス上に送る。

【０２８０】２．１０．電力管理ユニット

図５４は、電力管理ユニット４０９のブロック図である。

【０２８１】ＤｏＥｎｇｉｎｅはＣＰＵを内蔵した大規模なＡＳＩＣである。このため、内部のロジックが全部同時に動作してしまうと、大量の熱を発生し、チップ自体が破壊されてしまう恐れがある。これを防ぐために、ＤｏＥｎｇｉｎｅは、ブロック毎の電力の管理、すなわちパワーマネジメントを行ない、更にチップ全体の消費電力量の監視を行なう。

【０２８２】パワーマネージメントは、それぞれのブロックが各自個別に行なう。各ブロックの消費電力量の情報は、パワーマネージメントレベルとして、電力管理ユニット（ＰＭＵ）４０９に集められる。ＰＭＵ４０９では、各ブロックの消費電力量を合計し、その値が限界消費電力を超えないように、ＤｏＥｎｇｉｎｅの各ブロックの消費電力量を一括して監視する。

【０２８３】＜動作＞電力管理ブロックの動作は次の通りである。

・各ブロックは、４段階のパワーマネジメントレベルを持つ。

・ＰＭＵは、それぞれのレベルにおける消費電力の値をレジスタとして持つ。このレベル構成及び消費電力の値は、ＰＭ構成レジスタ５４０１に保持される。

・ＰＭＵは、各ブロックからパワーマネジメントレベルを２ビットのステータス信号として受け取り（後述）、レジスタ５４０１に設定された値と照合させて各ブロックの消費電力を知る。

・ＰＭＵは各ブロックの消費電力を加算器５４０３で加算し、ＤｏＥｎｇｉｎｅ全体の消費電力量をリアルタイムに計算する。

・算出された消費電力量は、構成レジスタ５４０１に設定された消費電力のリミット値（ＰＭリミット）と比較器５４０４で比較され、これを超えた場合には割込発生器５４０５から割り込み信号を発行する。

・このリミット値は２段階設定することができる。１段階目は、本当の限界から少し余裕を持たせた値を設定しておく。この値を超えると、通常の割込み信号が発行される。ソフトウェアはこれを受けて、新たにブロックを起動するような転送は始めないようにする。ただ、２段階目のリミット値に達しない範囲内では、ソフトウェアの管理の元で、新たなブロックを起動することができる。２段階目のリミット値は、デバイスが破壊される恐れのある値を設定しておく。万が一、この値を超えてしまった時には、ＮＭＩ（割込マスクが設定できない割り込み）を発行して安全のためにシステムを停止させる。

・割込み信号は、ＰＭＵの状態レジスタ５４０２をリードすることで解除される。この状態レジスタ５４０２をリードした時点からタイマカウントを始め、タイマがエクスパイアするまで消費電力量が戻らなければ、再び割込み信号を発行する。このタイマの値の設定はＰＭＵの構成レジスタ５４０１に設定される。

【０２８４】＜各ブロックのパワーマネージメント＞各ブロックのパワーマネージメント制御は、ブロック毎に自由に構成してよい。構成例の例を示す。

【０２８５】（構成例１）この例では、内部ロジックへのクロックをオン／オフすることにより、パワーマネジメントを行なっているので、消費電力のレベルは２段階しか持っていない。このレベルをステータス信号として電力管理ユニット４０９に送る。図５５にバスエージェントのブロック図を示す。

・バスエージェント５５０１は、各ユニット毎の内部ロジック５５０２、アドレスをデコードするデコーダ５５０３、クロックコントロール部５５０４、クロックゲート５５０５を含む。

・デコーダ５５０３とクロックコントロール部５５０４は常に動作しており、パワーマネージメントコントロールとして、バスのアクティビティーの監視、内部ロジックへのクロックのゲーティングを行なっている。

【０２８６】＜クロックコントロール＞

・バスエージェントは、バスのアクティビティーを検出し、クロックのオン／オフを自動で行なう。

・バスエージェントには、Sleep, Wake Up, Waitの３つのステートがある。

・Sleepはバスエージェントにアクティビティーがなく、クロックゲートクロックを停止させている状態である。

・Sleepの状態でも、デコーダ部５５０３、クロックコントロール部５５０４は動作しており、バスをモニタリングして、要求を待っている。

・デコーダ５５０３が自分のアドレスを検出すると、クロックゲート５５０５を開き、内部ロジックのクロックを動作させ、バスの要求に応える。ステートはWake Upに移行する。また、この状態を電力管理ユニット４０９に通知する。

・データ転送が終了すると、Waitステートに移行し、次の要求を待つ。この時クロックは動作したままである。要求があれば、Wake Upステートに戻り、転送を行なう。また、要求を待っている間はタイマによりカウント

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を行ない、要求がないままカウンタがタイムアップした場合は、Sleepステートへ移り、クロックを停止させる。この状態も電力管理ユニット４０９に通知される。

【０２８７】以上のようにして、消費電力が所定値を越えないように管理している。

［その他の構成例］図９及び図１０で示したキャッシュの動作手順は、図５６及び図５７のようなものであってもよい。

【０２８８】図５６においては、ＭＣバスよりデータ転送が開始されると、その最初にＭＣバスで示されるｍＴＴｙｐｅ［６０：０］によってその転送をキャッシュオンで行うかオフで行うか判断される。ここでは、転送がバースト転送の時、そのバースト転送データ量がキャッシュの１ラインのデータ量より大か小かによって判断する。なお、キャッシュの１ラインは２５６ビット＝４バースト分である。

【０２８９】図５６において、メモリコントローラは転送の開始でｍＴＴｙｐｅ［３：０］をチェックし、ｍＴＴｙｐｅが示すバースト長が１／２／４であれば、キャッシュオンで動作し、６／８／１６／２×１６／３×１６／４×１６の場合はキャッシュオフで動作する。キャッシュオンあるいはオフ後の動作は、図９及び図１０と同様である。

【０２９０】また、図５８及び図５９のように、デバイスによってキャッシュのオンオフを切り替えることもできる。図５８において、メモリコントローラは転送の開始でｍＴＴｙｐｅ［６：４］をチェックすることにより転送要求デバイスを識別し、そのデバイスの転送要求をキャッシュオンで動作するか、オフで動作するかを判断するために、あらかじめ設定されている構成レジスタの値を参照し、キャッシュオンで動作するか、オフで動作するか決定する。キャッシュオンあるいはオフ後の動作は、図９及び図１０と同様である。構成レジスタの設定は、ハードウエア的に決定（変更不可）していも良いし、ソフトウエアで書換え可能にしてもよい。

【０２９１】

【発明の効果】以上説明したように、本発明では、DMAを連続して行う場合に、ソフトウェアがバスマスタが変わる都度介入するのではなく、最初に一括してソフトウェアがバスアービタにDMAの開始させる条件と終了させる条件とを設定しておき、バスマスタにもDMAの設定を行っておくことで、後はバスアービタが順序をコントロールしながら一連の処理を行うことができる。これにより、処理毎のソフトウェアの介入が必要なくなる。また、いちいちメモリに書き戻す必要がないため、データがバスを使用する回数が少なくなり、全体としての処理速度が向上する。

【０２９２】また、クロスバススイッチにより要求に応じて接続するバスを切り替え、最適なバスを選んでデータの転送を行うことができる。さらに、バスの構成を柔軟にし、更にマスタとスレーブとが重複しないのであれば、複数のバスの接続を並列に行えるようにして、バスの使用効率を向上させることができる。

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【０２９３】また、複数のバスのそれぞれに接続されたバスマスタについて、それらがバスの使用権を得た順にメモリにアクセスするように制御することができる。そのため、時間経過に伴う処理順序を適正に保つことができる。

【０２９４】また、転送速度が高速なバーストモードではキャッシュを用いず、シングルモードでキャッシュを使用するため、キャッシュされた大量のデータが無駄になる事態を防止してキャッシュの使用効率を向上させ、メモリへのデータ転送速度が向上する。

【０２９５】また、各バスマスタが使用するバスを、バスの使用状況やバス要求の優先度、バスの性能、転送するデータがバスに適合するか否かなどを動的に決定して選択するため、バスの効率を向上させることができる。

【０２９６】また、回路の各ブロックの動作状態を監視して消費電力を抑制し、さらに、予備的な警告と危険な事態とで別々な割込み信号で通報するため、大量の熱の発生を抑制し、装置の熱による破壊を防止することができる。

【０２９７】

【図面の簡単な説明】

【図１】ＤｏＥｎｇｉｎｅを用いた装置あるいはシステムの構成例の図である。

【図２】ＤｏＥｎｇｉｎｅを用いた装置あるいはシステムの構成例の図である。

【図３】ＤｏＥｎｇｉｎｅを用いた装置あるいはシステムの構成例の図である。

【図４】ＤｏＥｎｇｉｎｅのブロック図である

【図５】キャッシュメモリコントローラの３つのステートを示す図である。

【図６】インタラプトコントローラ４１０のブロック図である。

【図７】メモリコントローラ４０３のブロック図である。

【図８】キャッシュコントローラ７０６を中心とする詳細なブロック図である。

【図９】ＭＣバスよりメモリリード／ライト転送が要求された場合のキャッシュの動作を示すフローチャートである。

【図１０】ＭＣバスよりメモリリード／ライト転送が要求された場合のキャッシュの動作を示すフローチャートである。

【図１１】ＲＯＭ／ＲＡＭコントローラ７０７の構成を示す図である。

【図１２】ＣＰＵからのバースト読み出しのタイミングを示すタイミング図である。

【図１３】ＣＰＵからのバースト書き込みのタイミング

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を示すタイミング図である。
【図１４】Ｇバスデバイスからのバースト読み出しのタイミングを示すタイミング図である。
【図１５】Ｇバスデバイスからのバースト書き込みのタイミングを示すタイミング図である。
【図１６】メモリフロントキャッシュにヒットした場合のシングル読み出しのタイミングを示すタイミング図である。
【図１７】メモリフロントキャッシュにヒットしなかった場合のシングル読み出しのタイミングを示すタイミング図である。
【図１８】メモリフロントキャッシュにヒットした場合のシングル書き込みのタイミングを示すタイミング図である。
【図１９】メモリフロントキャッシュにヒットしなかった場合のシングル書き込みのタイミングを示すタイミング図である。
【図２０】システムバスブリッジ（ＳＢＢ）４０２のブロック図である。
【図２１】ＩＯバスインターフェースのブロック図である。
【図２２】Ｇバスインターフェース２００６のブロック図である。
【図２３】仮想メモリマップ、物理メモリマップ、Ｇバスのアドレス空間でのメモリマップ、ＩＯバスのアドレス空間でのメモリマップの図である。
【図２４】レジスタ等を含む図２３における斜線部の５１２メガバイトを示すマップの図である。
【図２５】アドレススイッチ２００３のブロック図である。
【図２６】データスイッチ２００４のブロック図である。
【図２７】Ｇバスからの書き込み／読み出しサイクルのタイミング図である。
【図２８】Ｇバスのバースト停止サイクルのタイミング図である。
【図２９】Ｇバスのトランザクション停止サイクルのタイミング図である。
【図３０】Ｇバスのトランザクション停止サイクルのタイミング図である。
【図３１】Ｇバスのトランザクション停止サイクルのタイミング図である。
【図３２】Ｇバスのトランザクション停止サイクルのタイミング図である。
【図３３】ＰＣＩバスインターフェース４１６のブロック図である。
【図３４】Ｇバスアービタ（ＧＢＡ）４０６のブロック図である。
【図３５】ＤｏＥｎｇｉｎｅ４００内におけるＧバス４０４を中心とする、Ｇバス上のバスマスタによるDMAに係るブロック図である。
【図３６】連続してバスを使用する回数が、バスマスタ１～４のすべてについて１に設定されている場合の公平アービトレーションモード（フェアモード）の例を示す図である。
【図３７】連続してバスを使用する回数が、バスマスタ１についてのみ２であり、他のバスマスタは１に設定されている場合の公平アービトレーションモードの例を示す図である。
【図３８】連続してバスを使用する回数がそれぞれ１ずつであり、バスマスタ１が優先バスマスタと設定されている場合の優先アービトレーションモードの例を示す図である。
【図３９】バスマスタ１からのバス要求により、バスマスタ４のバス要求が許可されているにもかかわらず中断された例を示す図である。
【図４０】ＩＯバスアービタ４０７のブロック図である。
【図４１】同期ユニット４００１のブロック図である。
【図４２】同期ユニット内の一つコンペアユニットの図である。
【図４３】スキャナ／プリンタコントローラ４０８のブロック図である。
【図４４】スキャナ／ビデオ同期制御ユニット４３０６のブロック図である。
【図４５】プリンタ／ビデオ同期制御ユニット４３０７のブロック図である。
【図４６】スキャナＦＩＦＯコントローラのブロック図である。
【図４７】プリンタＦＩＦＯコントローラ４３１２のブロック図である。
【図４８】データ転送制御ユニット４３０２のブロック図である。
【図４９】チェインコントローラ４８０１のブロック図である。
【図５０】Ｇバス/ＩＯバスインターフェースユニット４３０１のブロック図である。
【図５１】バスセレクタユニット５００１のブロック図である。
【図５２】ＩＯバスコントローラ５００２のブロック図である。
【図５３】Ｇバスコントローラ５００３のブロック図である。
【図５４】電力管理ユニット４０９のブロック図である。
【図５５】バスエージェントのブロック図である。
【図５６】ＭＣバスよりメモリリード／ライト転送が要求された場合のキャッシュの動作の他の例を示すフローチャートである。
【図５７】ＭＣバスよりメモリリード／ライト転送が要

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求された場合のキャッシュの動作の他の例を示すフローチャートである。

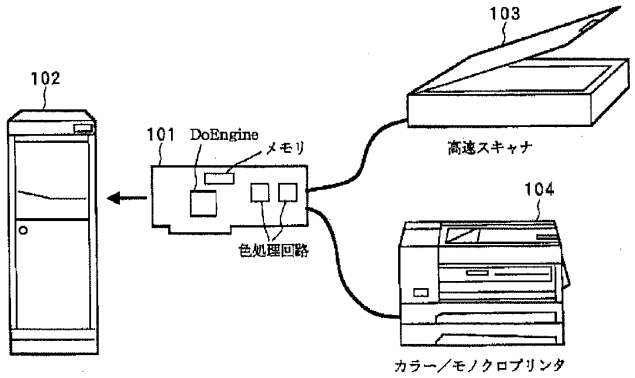
【図５８】ＭＣバスよりメモリリード／ライト転送が要求された場合のキャッシュの動作の他の例を示すフロー＊チャートである。

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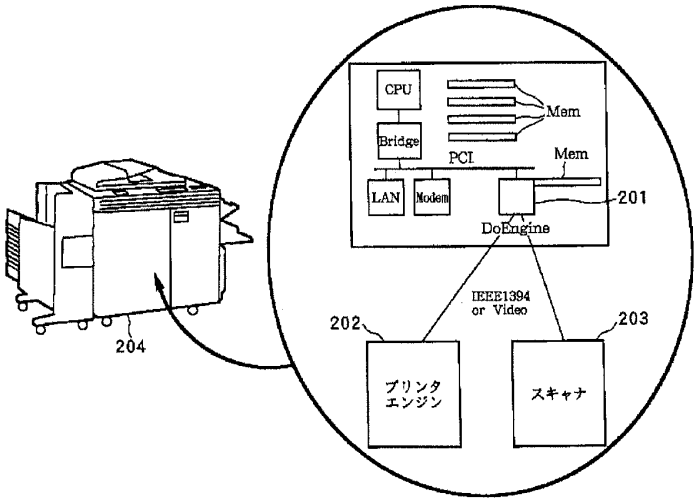
＊チャートである。

【図５９】ＭＣバスよりメモリリード／ライト転送が要求された場合のキャッシュの動作の他の例を示すフローチャートである。

【図１】

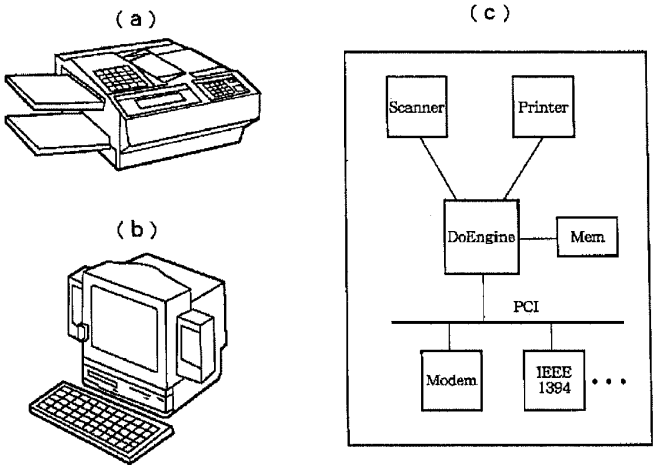


【図２】

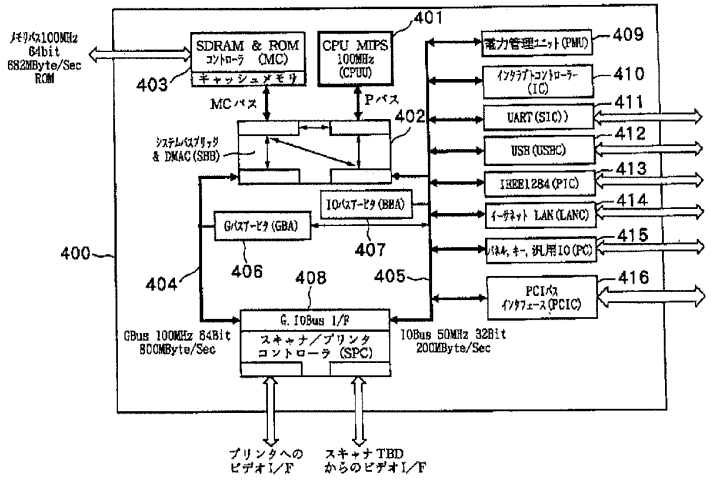


B3

【図３】

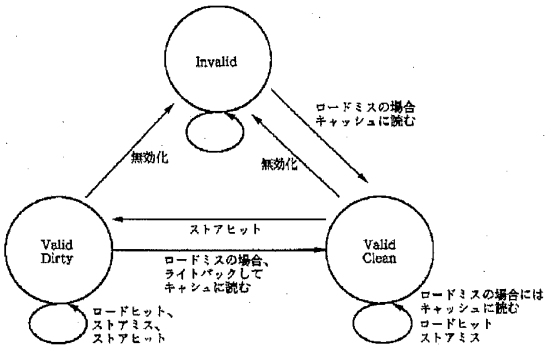

(a)
(b)
(c)
Scanner
Printer
DoEngine
Mem
PCI
Modem
IEEE 1394

【図４】

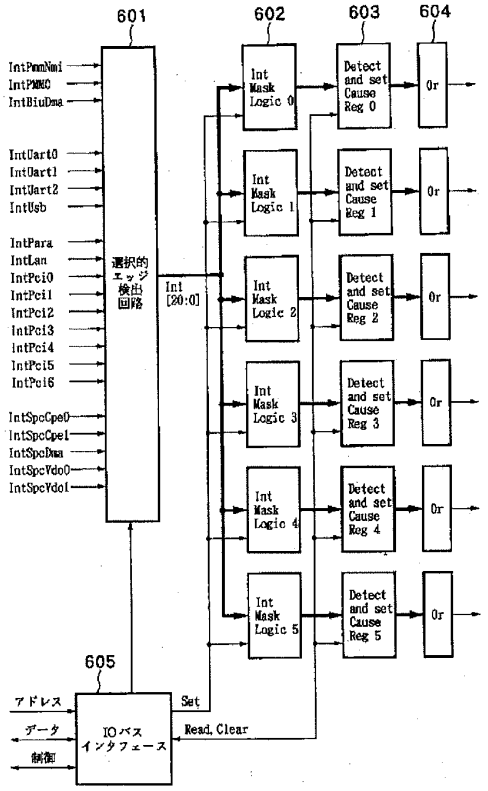

401
SDRAM & ROM コントローラ (MC)
CPU MIPS 100MHz (CPUU)
キャッシュメモリ
403
MCバス
Pバス
402
システムバスブリッジ & DMAC (SHB)
IOバスブリッジ (BBA)
Gバスブリッジ (GBA)
400
404
406
407
408
405
G. IOBus I/F
スキャナ／プリンタ コントローラ (SPC)
GBus 100MHz 64Bit 800MByte/Sec
IOBus 50MHz 32Bit 200MByte/Sec
プリンタへの ビデオI/F
スキャナTBD からのビデオI/F
電力管理ユニット (PMU)
409
インタラプトコントローラ (IC)
410
UART (SIO)
411
USB (USBC)
412
IEEE1284 (PIC)
413
イーサネット LAN (LANC)
414
パネル, キー, 汎用IO (PC)
415
PCIバス インタフェース (PCIC)
416

B3

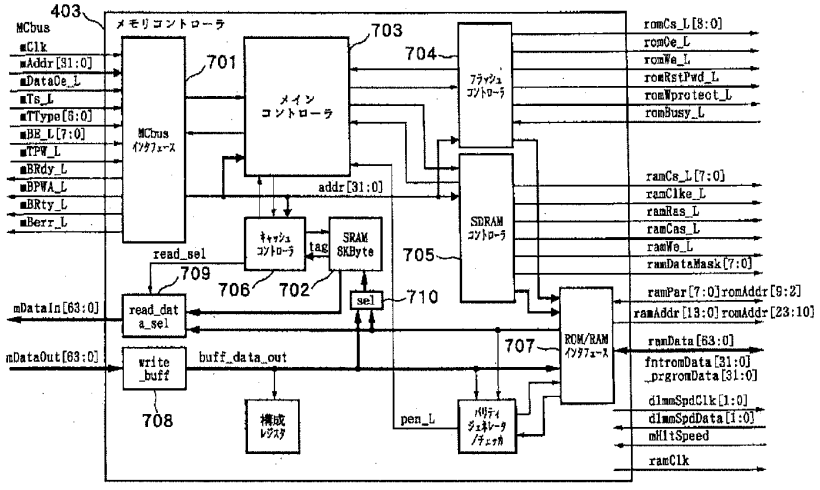
【図５】


Invalid
ロードミスの場合
キャッシュに読む
無効化
無効化
ストアヒット
Valid
Dirty
Valid
Clean
ロードミスの場合、
ライトバックして
キャッシュに読む
ロードヒット、
ストアミス、
ストアヒット
ロードミスの場合には
キャッシュに読む
ロードヒット
ストアミス

【図６】

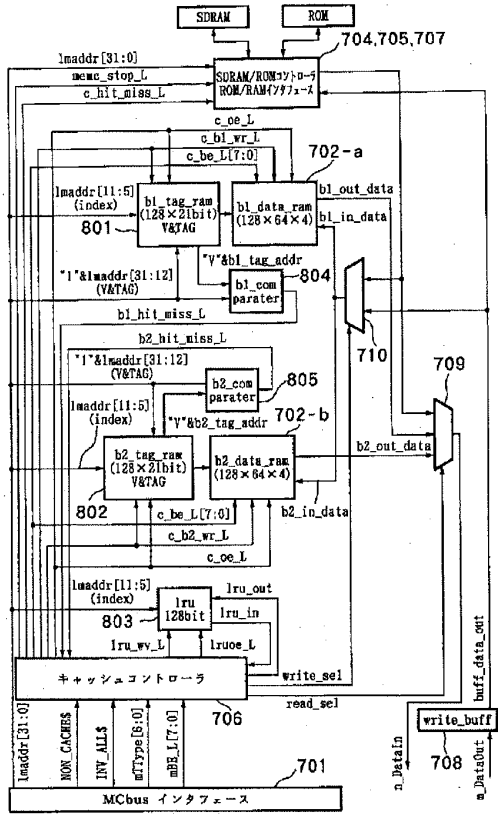

601
602
603
604
IntPwmNmi
IntPMMC
IntBiuDma
IntUart0
IntUart1
IntUart2
IntUsb
IntPara
IntLan
IntPci0
IntPci1
IntPci2
IntPci3
IntPci4
IntPci5
IntPci6
IntSpcCpe0
IntSpcCpe1
IntSpcDma
IntSpcVdo0
IntSpcVdo1
選択的
エッジ
検出
回路
Int
[20:0]
Int
Mask
Logic 0
Int
Mask
Logic 1
Int
Mask
Logic 2
Int
Mask
Logic 3
Int
Mask
Logic 4
Int
Mask
Logic 5
Detect
and set
Cause
Reg 0
Detect
and set
Cause
Reg 1
Detect
and set
Cause
Reg 2
Detect
and set
Cause
Reg 3
Detect
and set
Cause
Reg 4
Detect
and set
Cause
Reg 5
Or
Or
Or
Or
Or
Or
605
アドレス
データ
制御
IOバス
インタフェース
Set
Read, Clear

【図７】

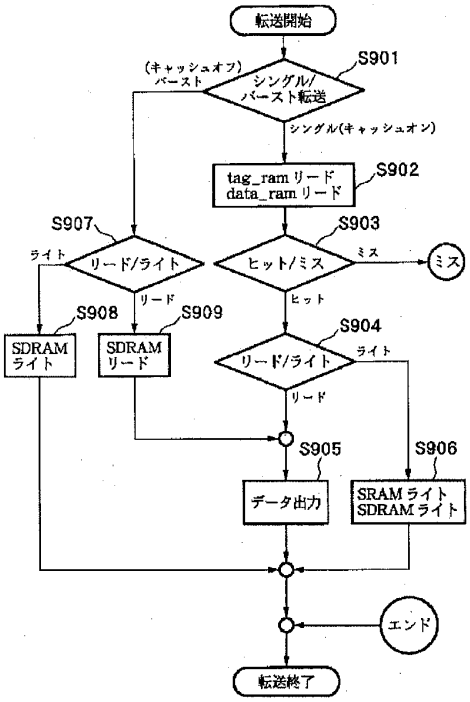

403
メモリコントローラ
MCbus
mClk
mAddr[31:0]
mDataOe_L
mTs_L
mTType[5:0]
mBE_L[7:0]
mTPW_L
mBRdy_L
mBPWA_L
mBRty_L
mBerr_L
MCbus
インタフェース
701
メイン
コントローラ
703
704
フラッシュ
コントローラ
addr[31:0]
SDRAM
コントローラ
キャッシュ
コントローラ
tag
SRAM
8KByte
705
read_sel
709
706
702
sel
710
mDataIn[63:0]
read_dat
a_sel
mDataOut[63:0]
write
_buff
buff_data_out
708
構成
レジスタ
pen_L
パリティ
ジェネレータ
/チェッカ
707
ROM/RAM
インタフェース
romCs_L[3:0]
romOe_L
romWe_L
romRstPwd_L
romWprotect_L
romBusy_L
ramCs_L[7:0]
ramClke_L
ramRas_L
ramCas_L
ramWe_L
ramDataMask[7:0]
ramPar[7:0]romAddr[9:2]
ramAddr[13:0]romAddr[23:10]
ramData[63:0]
fntromData[31:0]
_prgromData[31:0]
dimmSpdClk[1:0]
dimmSpdData[1:0]
mHltSpeed
ramClk

B3

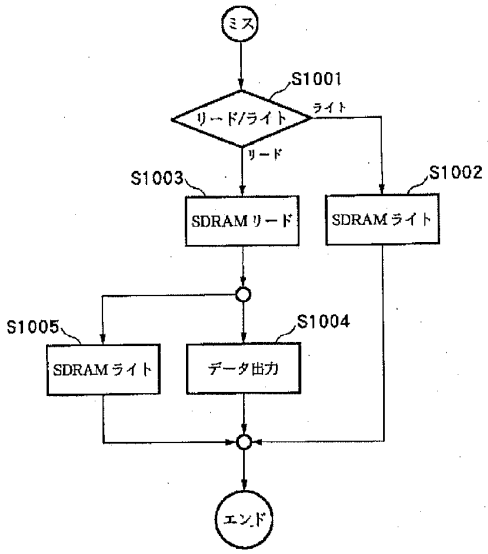
【図８】


SDRAM
ROM
704,705,707
SDRAM/ROMコントローラ
ROM/RAMインタフェース
lmaddr[31:0]
memc_stop_L
c_hit_miss_L
c_oe_L
c_bl_wr_L
c_be_L[7:0]
702-a
lmaddr[11:5]
(index)
bl_tag_ram
(128×21bit)
V&TAG
bl_data_ram
(128×64×4)
bl_out_data
bl_in_data
801
"1"&lmaddr[31:12]
(V&TAG)
"Y"&bl_tag_addr
bl_com
parater
804
bl_hit_miss_L
b2_hit_miss_L
"1"&lmaddr[31:12]
(V&TAG)
b2_com
parater
805
709
710
lmaddr[11:5]
(index)
"Y"&b2_tag_addr
702-b
b2_tag_ram
(128×21bit)
V&TAG
b2_data_ram
(128×64×4)
b2_out_data
802
c_be_L[7:0]
b2_in_data
c_b2_wr_L
c_oe_L
lmaddr[11:5]
(index)
lru
128bit
lru_out
lru_in
803
lru_wv_L
lruoe_L
キャッシュコントローラ
write_sel
read_sel
706
buff_data_out
write_buff
708
lmaddr[31:0]
NON_CACHES
INV_ALL$
mFType[6:0]
mBB_L[7:0]
m_DataIn
m_DataOut
701
MCbus インタフェース

【図９】

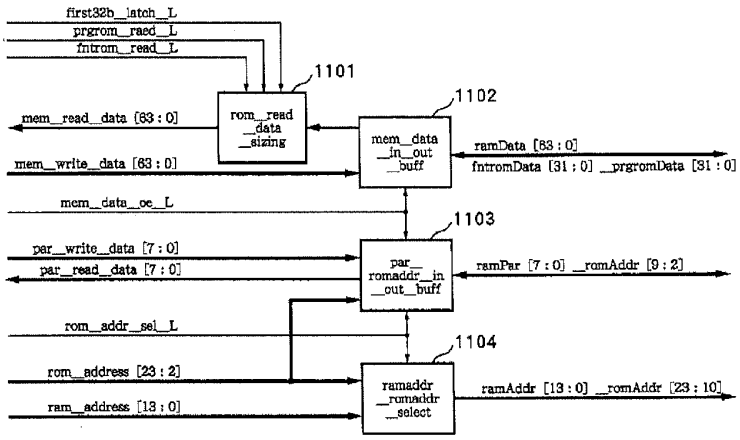

転送開始
S901
(キャッシュオフ)
バースト
シングル/
バースト転送
シングル(キャッシュオン)
tag_ram リード
data_ram リード
S902
S903
S907
ライト
リード/ライト
ヒット/ミス
ミス
ミス
リード
ヒット
S908
S909
S904
SDRAM
ライト
SDRAM
リード
リード/ライト
ライト
リード
S905
S906
データ出力
SRAM ライト
SDRAM ライト
エンド
転送終了

【図１０】

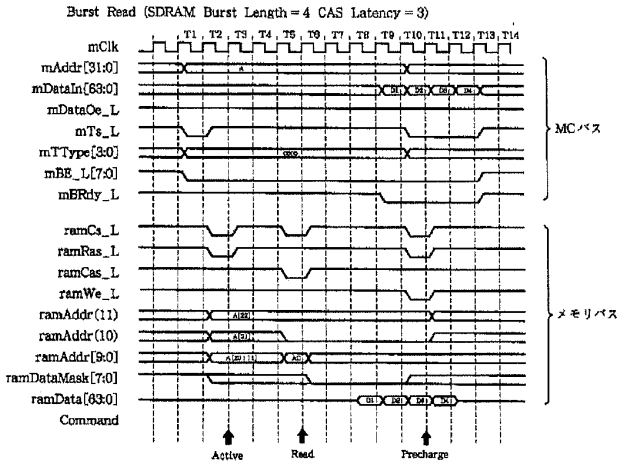

ミス
S1001
リード/ライト
ライト
リード
S1003
S1002
SDRAM リード
SDRAM ライト
S1005
S1004
SDRAM ライト
データ出力
エンド

B3

【図１１】

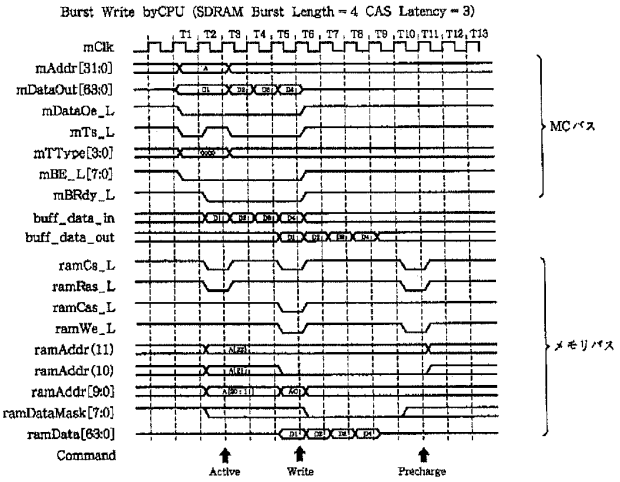

first32b_latch_L
prgrom_raed_L
fntrom_read_L
1101
rom_read_data_sizing
mem_read_data [63:0]
mem_write_data [63:0]
1102
mem_data_in_out_buff
ramData [63:0]
fntromData [31:0] _prgromData [31:0]
mem_data_oe_L
1103
par_write_data [7:0]
par_read_data [7:0]
par_romaddr_in_out_buff
ramPar [7:0] _romAddr [9:2]
rom_addr_sel_L
1104
rom_address [23:2]
ram_address [13:0]
ramaddr_romaddr_select
ramAddr [13:0] _romAddr [23:10]

【図１２】

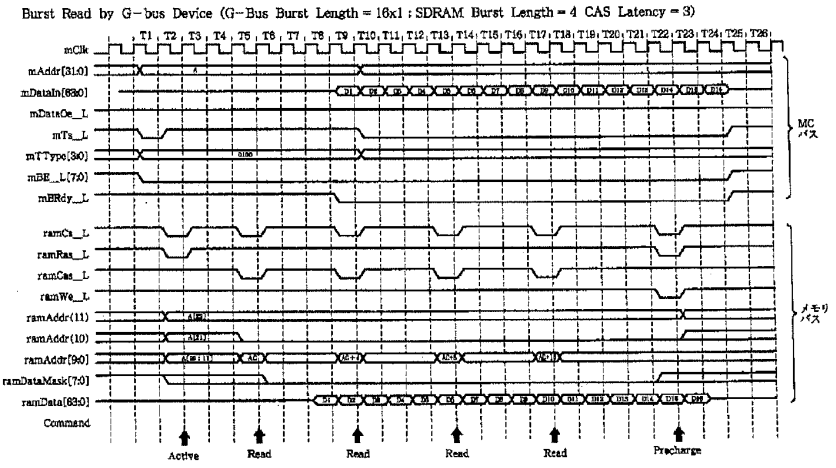

Burst Read (SDRAM Burst Length = 4 CAS Latency = 3)
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14
mClk
mAddr[31:0]
mDataIn[63:0]
mDataOe_L
mTs_L
mTType[3:0]
mBE_L[7:0]
mBRdy_L
MCバス
ramCs_L
ramRas_L
ramCas_L
ramWe_L
ramAddr(11)
ramAddr(10)
ramAddr[9:0]
ramDataMask[7:0]
ramData[63:0]
メモリバス
Command
Active
Read
Precharge

B3

【図１３】

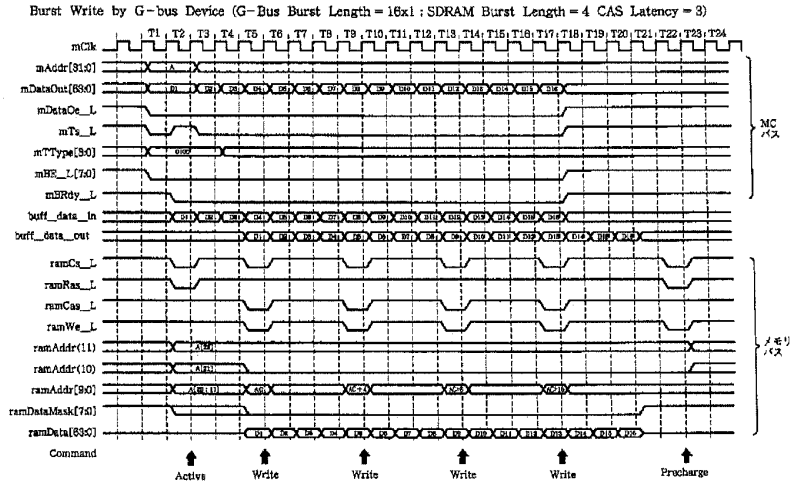

Burst Write byCPU (SDRAM Burst Length = 4 CAS Latency = 3)
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13
mClk
mAddr[31:0]
mDataOut[63:0]
mDataOe_L
mTs_L
mTType[3:0]
mBE_L[7:0]
mBRdy_L
buff_data_in
buff_data_out
ramCs_L
ramRas_L
ramCas_L
ramWe_L
ramAddr(11)
ramAddr(10)
ramAddr[9:0]
ramDataMask[7:0]
ramData[63:0]
Command
Active
Write
Precharge
MCバス
メモリバス

【図１４】

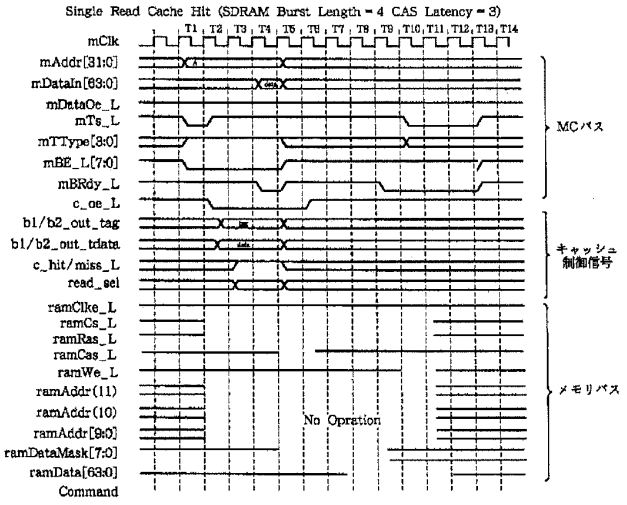

Burst Read by G−bus Device (G−Bus Burst Length = 16x1 : SDRAM Burst Length = 4 CAS Latency = 3)
mClk
mAddr[31:0]
mDataIn[63:0]
mDataOe_L
mTs_L
mTType[3:0]
mBE_L[7:0]
mBRdy_L
ramCs_L
ramRas_L
ramCas_L
ramWe_L
ramAddr(11)
ramAddr(10)
ramAddr[9:0]
ramDataMask[7:0]
ramData[63:0]
Command
Active
Read
Read
Read
Read
Precharge
MC
バス
メモリ
バス

B3

【図１５】

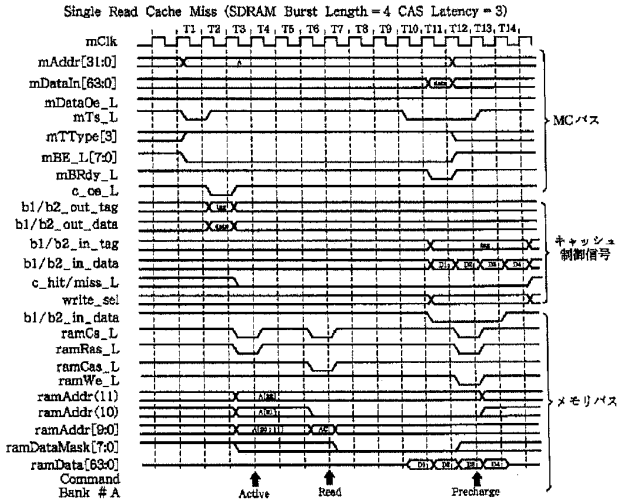

Burst Write by G-bus Device (G-Bus Burst Length = 16x1 ; SDRAM Burst Length = 4 CAS Latency = 3)
mClk
mAddr[31:0]
mDataOut[63:0]
mDataOe_L
mTs_L
mTType[3:0]
mBE_L[7:0]
mBRdy_L
buff_data_in
buff_data_out
ramCs_L
ramRas_L
ramCas_L
ramWe_L
ramAddr(11)
ramAddr(10)
ramAddr[9:0]
ramDataMask[7:0]
ramData[63:0]
Command
MC バス
メモリ バス
Active
Write
Write
Write
Write
Precharge

【図１６】

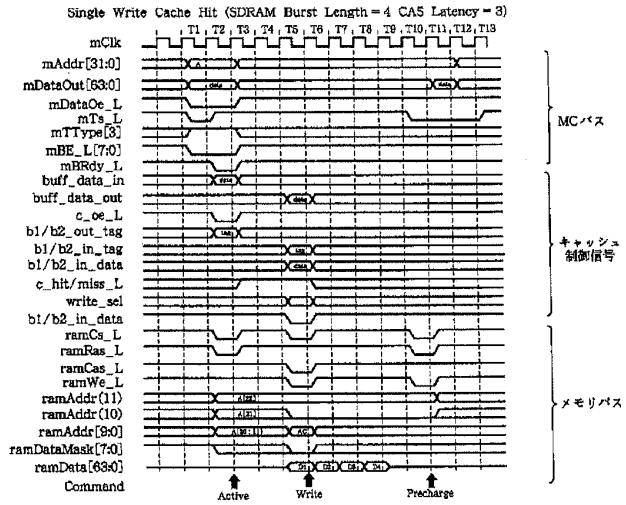

Single Read Cache Hit (SDRAM Burst Length = 4 CAS Latency = 3)
mClk
mAddr[31:0]
mDataIn[63:0]
mDataOe_L
mTs_L
mTType[3:0]
mBE_L[7:0]
mBRdy_L
c_oe_L
b1/b2_out_tag
b1/b2_out_tdata
c_hit/miss_L
read_sel
ramClke_L
ramCs_L
ramRas_L
ramCas_L
ramWe_L
ramAddr(11)
ramAddr(10)
ramAddr[9:0]
ramDataMask[7:0]
ramData[63:0]
Command
No Opration
MCバス
キャッシュ 制御信号
メモリバス

B3

【図１７】

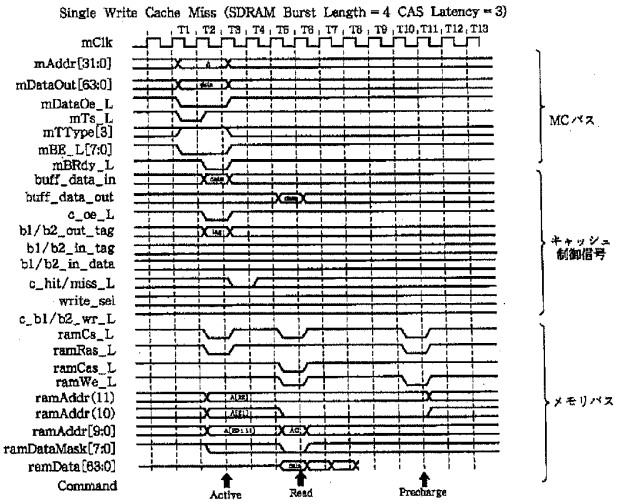

Single Read Cache Miss (SDRAM Burst Length = 4 CAS Latency = 3)
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14
mClk
mAddr[31:0]
mDataIn[63:0]
mDataOe_L
mTs_L
mTType[3]
mBE_L[7:0]
mBRdy_L
c_oe_L
b1/b2_out_tag
b1/b2_out_data
b1/b2_in_tag
b1/b2_in_data
c_hit/miss_L
write_sel
b1/b2_in_data
ramCs_L
ramRas_L
ramCas_L
ramWe_L
ramAddr(11)
ramAddr(10)
ramAddr[9:0]
ramDataMask[7:0]
ramData[63:0]
Command
Bank # A
Active
Read
Precharge
MCバス
キャッシュ制御信号
メモリバス

【図１８】

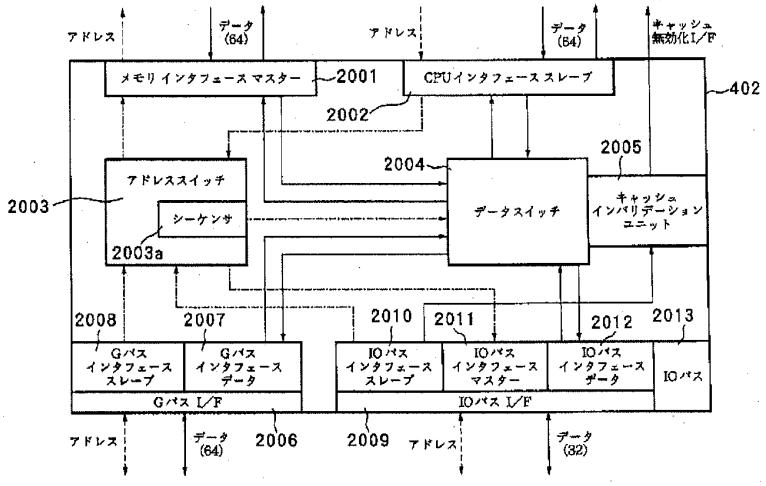

Single Write Cache Hit (SDRAM Burst Length = 4 CAS Latency = 3)
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13
mClk
mAddr[31:0]
mDataOut[63:0]
mDataOe_L
mTs_L
mTType[3]
mBE_L[7:0]
mBRdy_L
buff_data_in
buff_data_out
c_oe_L
b1/b2_out_tag
b1/b2_in_tag
b1/b2_in_data
c_hit/miss_L
write_sel
b1/b2_in_data
ramCs_L
ramRas_L
ramCas_L
ramWe_L
ramAddr(11)
ramAddr(10)
ramAddr[9:0]
ramDataMask[7:0]
ramData[63:0]
Command
Active
Write
Precharge
MCバス
キャッシュ制御信号
メモリバス

B3

【図１９】

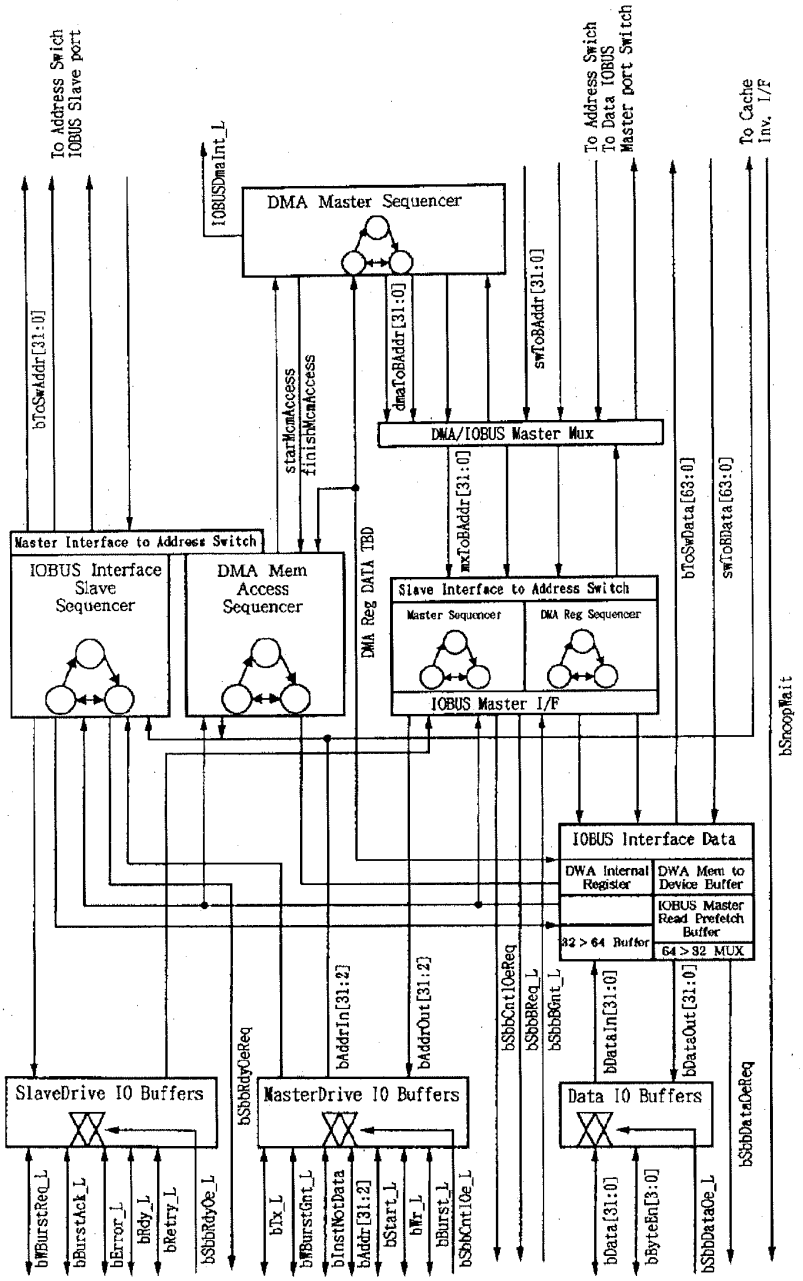

Single Write Cache Miss (SDRAM Burst Length = 4 CAS Latency = 3)
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13
mClk
mAddr[31:0]
mDataOut[63:0]
mDataOe_L
mTs_L
mTType[3]
mBE_L[7:0]
mBRdy_L
buff_data_in
buff_data_out
c_oe_L
b1/b2_out_tag
b1/b2_in_tag
b1/b2_in_data
c_hit/miss_L
write_sel
c_b1/b2_wr_L
ramCs_L
ramRas_L
ramCas_L
ramWe_L
ramAddr(11)
ramAddr(10)
ramAddr[9:0]
ramDataMask[7:0]
ramData[63:0]
Command
Active
Read
Precharge
MCバス
キャッシュ制御信号
メモリバス

【図２０】


アドレス
データ (64)
アドレス
データ (64)
キャッシュ無効化I/F
メモリインタフェースマスター
2001
CPUインタフェーススレーブ
402
2002
2004
2005
2003
アドレススイッチ
シーケンサ
2003a
データスイッチ
キャッシュインバリデーションユニット
2008
2007
2010
2011
2012
2013
Gバス インタフェース スレーブ
Gバス インタフェース データ
IOバス インタフェース スレーブ
IOバス インタフェース マスター
IOバス インタフェース データ
IOバス
Gバス I/F
IOバス I/F
アドレス
データ (64)
2006
2009
アドレス
データ (32)

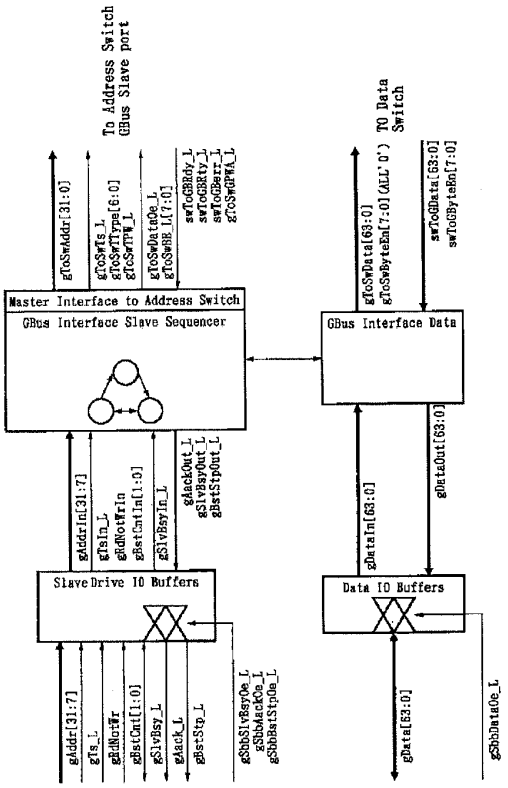
B3

【図２１】

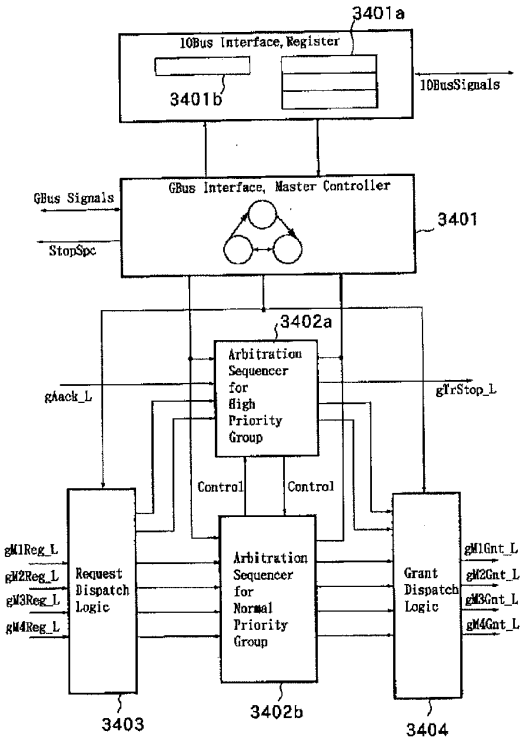

To Address Swich
IOBUS Slave port
IOBUSDmaInt_L
DMA Master Sequencer
To Address Swich
To Data IOBUS
Master port Switch
To Cache
Inv. I/F
bToSwAddr[31:0]
startMemAccess
finishMemAccess
dmaToBAddr[31:0]
swToBAddr[31:0]
DMA/IOBUS Master Mux
mxToBAddr[31:0]
bToSwData[63:0]
swToBData[63:0]
Master Interface to Address Switch
IOBUS Interface
Slave
Sequencer
DMA Mem
Access
Sequencer
DMA Reg DATA TBD
Slave Interface to Address Switch
Master Sequencer
DMA Reg Sequencer
IOBUS Master I/F
bSnoopWait
IOBUS Interface Data
DWA Internal
Register
DWA Mem to
Device Buffer
IOBUS Master
Read Prefetch
Buffer
32 > 64 Buffer
64 > 32 MUX
bSbbCntlOeReq
bSbbBReq_L
bSbbBGnt_L
bDataIn[31:0]
bDataOut[31:0]
bAddrIn[31:2]
bAddrOut[31:2]
bSbbRdyOeReq
SlaveDrive IO Buffers
MasterDrive IO Buffers
Data IO Buffers
bMBurstReq_L
bBurstAck_L
bError_L
bRdy_L
bRetry_L
bSbbRdyOe_L
bTx_L
bMBurstGnt_L
bInstNotData
bAddr[31:2]
bStart_L
bMr_L
bBurst_L
bSbbCntlOe_L
bData[31:0]
bByteEn[3:0]
bSbbDataOe_L
bSbbDataOeReq

B3

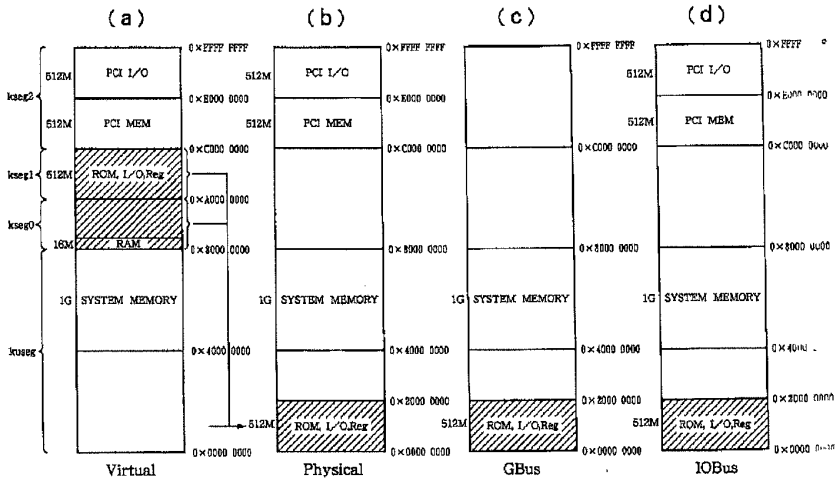
【図２２】



【図３４】

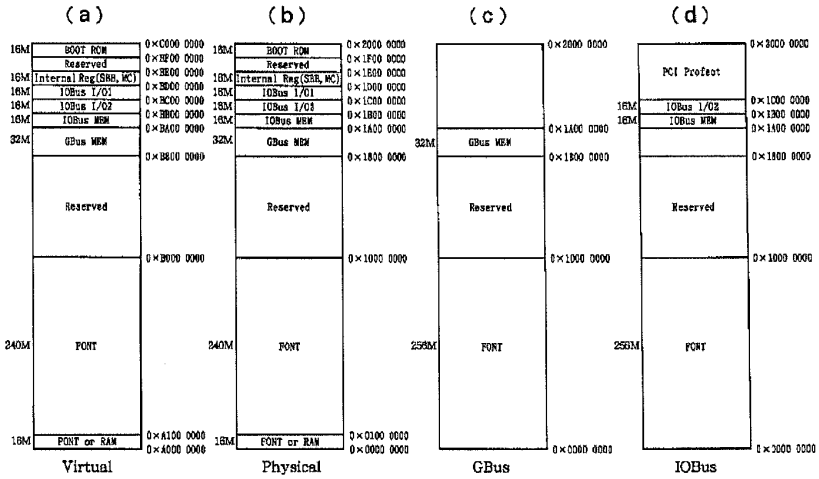


【図２３】

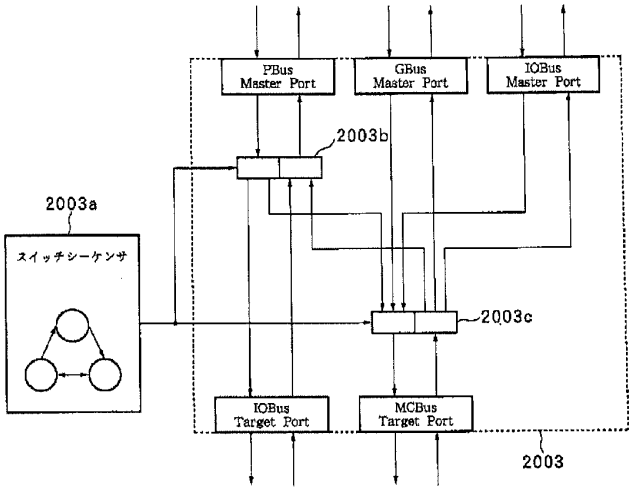


B3

【図２４】

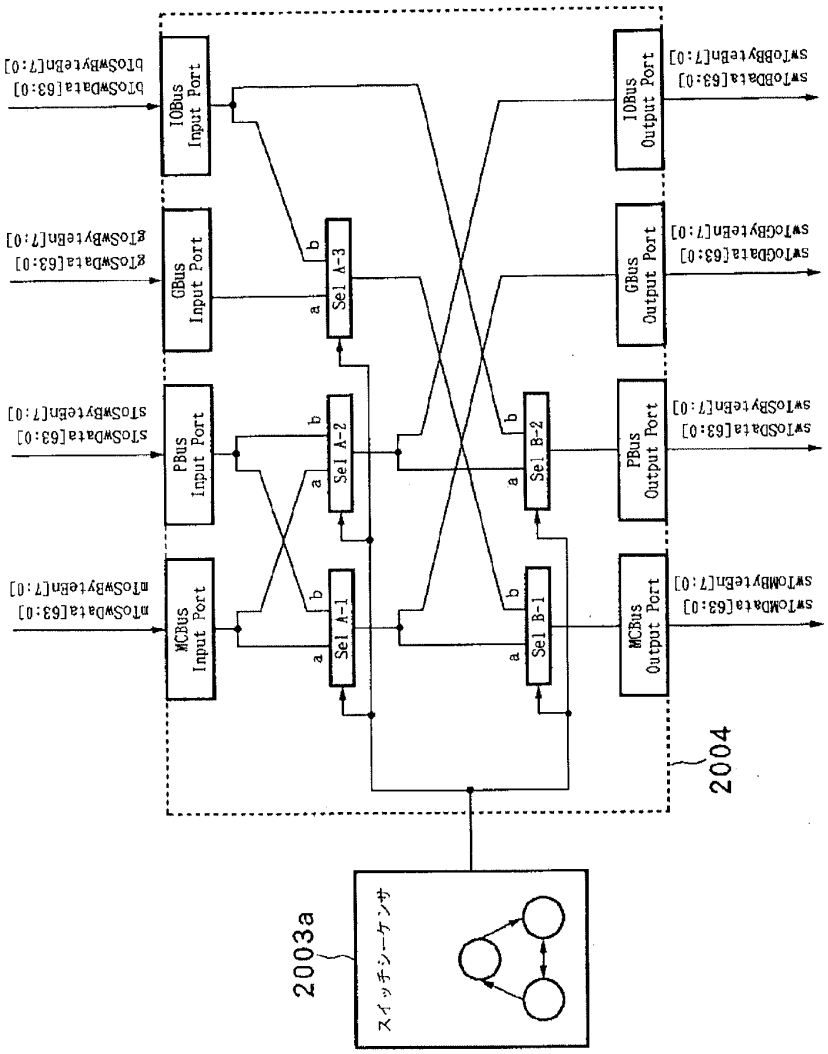

(a)
(b)
(c)
(d)
BOOT ROM
Reserved
Internal Reg(SBR, MC)
IOBus I/O1
IOBus I/O2
IOBus MEM
GBus MEM
Reserved
FONT
FONT or RAM
PCI Prefect
Virtual
Physical
GBus
IOBus

【図２５】


PBus Master Port
GBus Master Port
IOBus Master Port
2003b
2003a
スイッチシーケンサ
2003c
IOBus Target Port
MCBus Target Port
2003

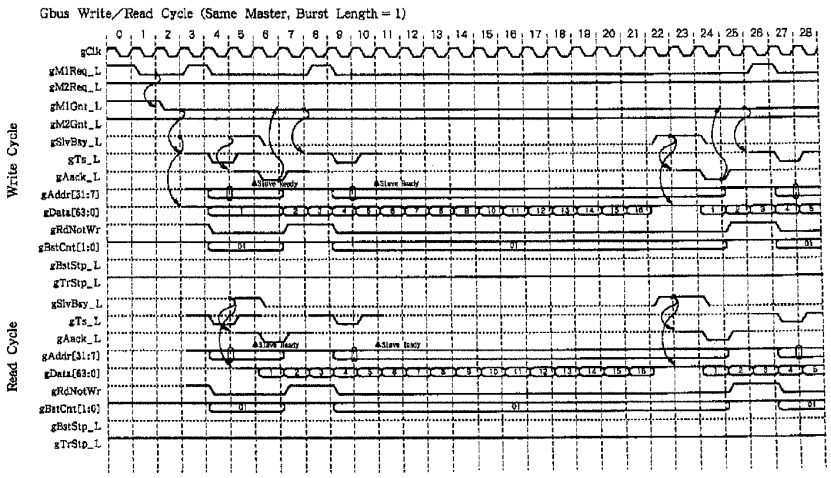
B3

【図２６】

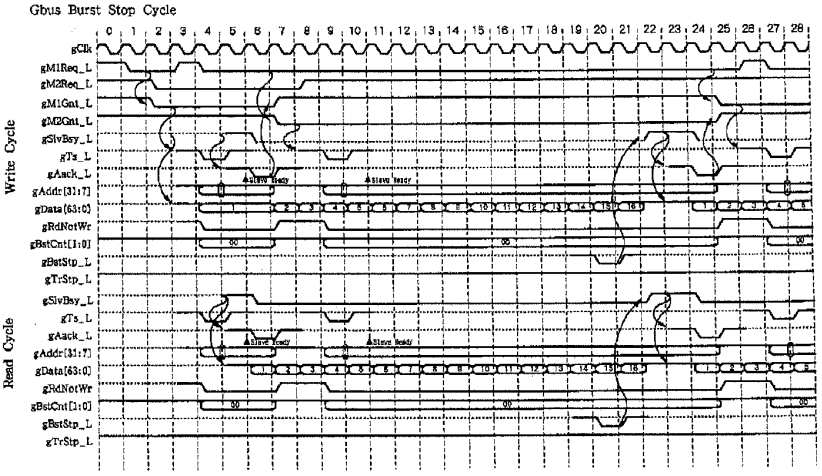

bToSwData[63:0]
bToSwByteBn[7:0]
IOBus Input Port
gToSwData[63:0]
gToSwByteBn[7:0]
GBus Input Port
sToSwData[63:0]
sToSwByteBn[7:0]
PBus Input Port
mToSwData[63:0]
mToSwByteBn[7:0]
MCBus Input Port
Sel A-3
Sel A-2
Sel A-1
Sel B-2
Sel B-1
IOBus Output Port
GBus Output Port
PBus Output Port
MCBus Output Port
swToBData[63:0]
swToBByteBn[7:0]
swToGData[63:0]
swToGByteBn[7:0]
swToSData[63:0]
swToSByteBn[7:0]
swToMData[63:0]
swToMByteBn[7:0]
2004
2003a
スイッチシーケンサ

B3

【図２７】

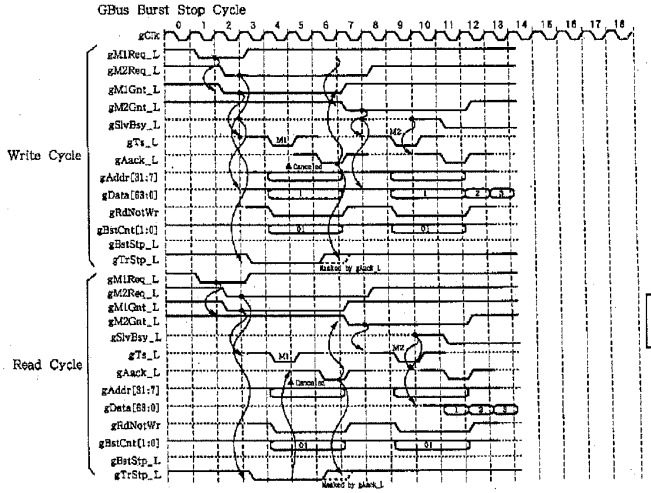

Gbus Write/Read Cycle (Same Master, Burst Length = 1)
Write Cycle
Read Cycle
gClk
gM1Req_L
gM2Req_L
gM1Gnt_L
gM2Gnt_L
gSlvBsy_L
gTs_L
gAack_L
gAddr[31:7]
gData[63:0]
gRdNotWr
gBstCnt[1:0]
gBstStp_L
gTrStp_L

【図２８】

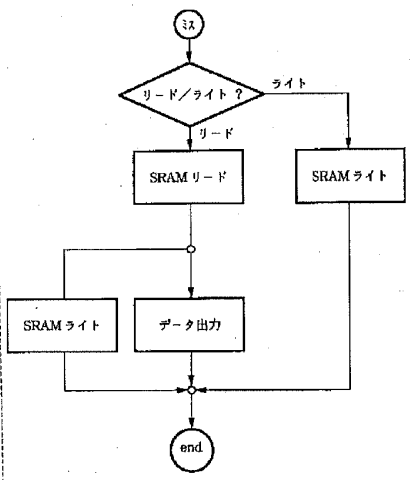

Gbus Burst Stop Cycle
Write Cycle
Read Cycle
gClk
gM1Req_L
gM2Req_L
gM1Gnt_L
gM2Gnt_L
gSlvBsy_L
gTs_L
gAack_L
gAddr[31:7]
gData[63:0]
gRdNotWr
gBstCnt[1:0]
gBstStp_L
gTrStp_L

B3

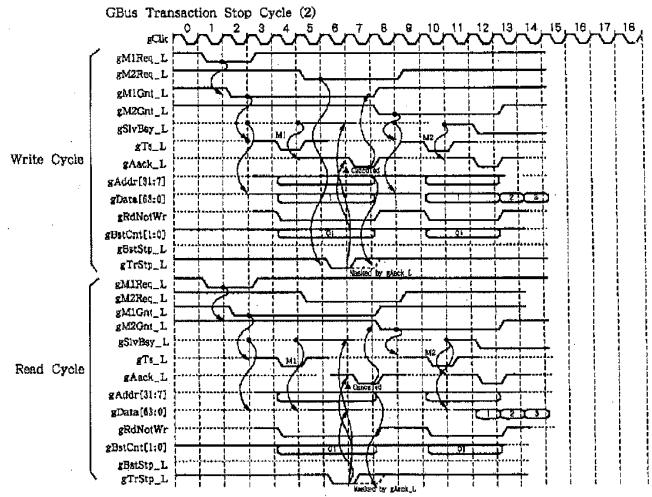
【図２９】



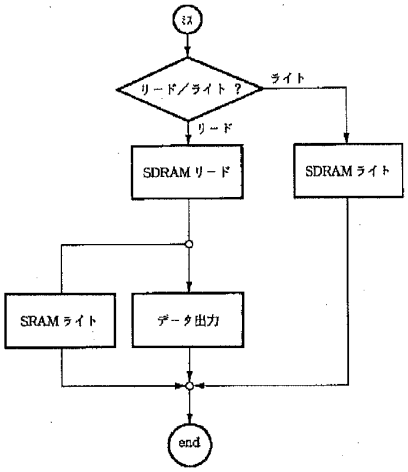
【図５７】



【図３０】

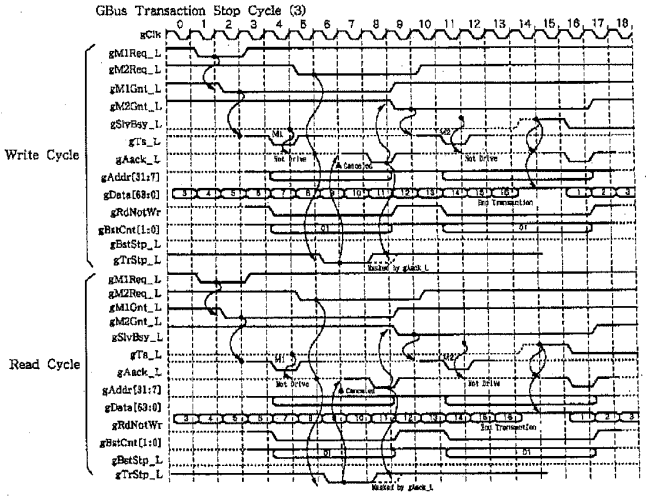


【図５９】

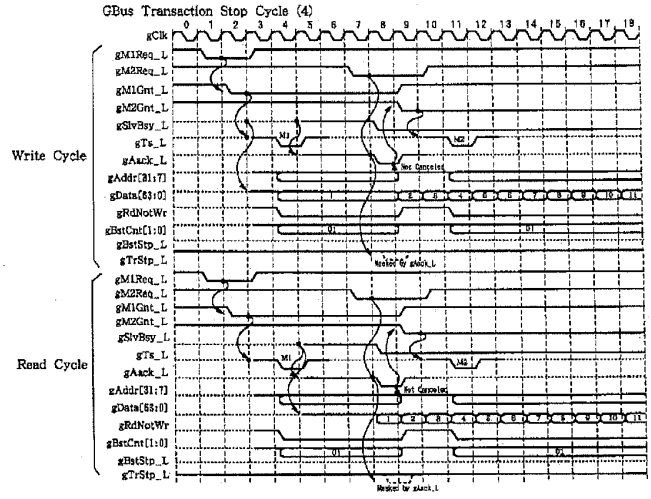


B3

【図３１】

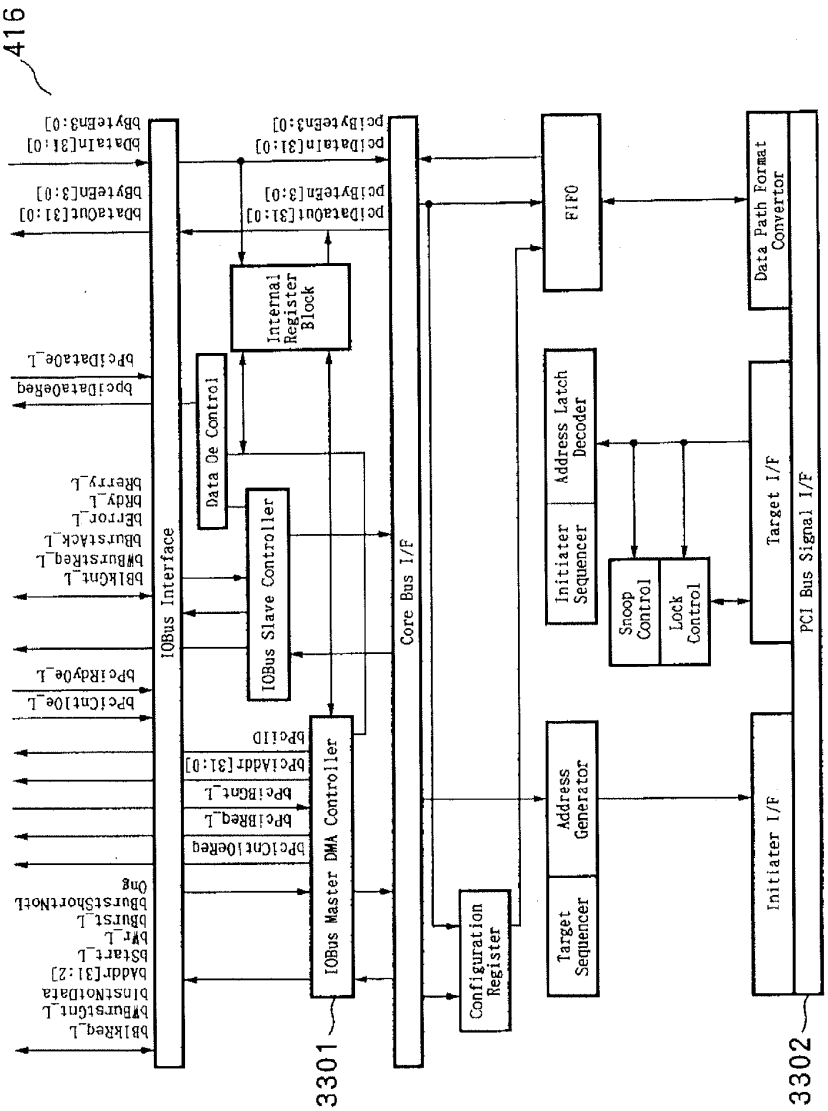

GBus Transaction Stop Cycle (3)
Write Cycle
Read Cycle
gClk
gM1Req_L
gM2Req_L
gM1Gnt_L
gM2Gnt_L
gSlvBsy_L
gTs_L
gAack_L
gAddr[31:7]
gData[63:0]
gRdNotWr
gBstCnt[1:0]
gBstStp_L
gTrStp_L

【図３２】


GBus Transaction Stop Cycle (4)
Write Cycle
Read Cycle
gClk
gM1Req_L
gM2Req_L
gM1Gnt_L
gM2Gnt_L
gSlvBsy_L
gTs_L
gAack_L
gAddr[31:7]
gData[63:0]
gRdNotWr
gBstCnt[1:0]
gBstStp_L
gTrStp_L

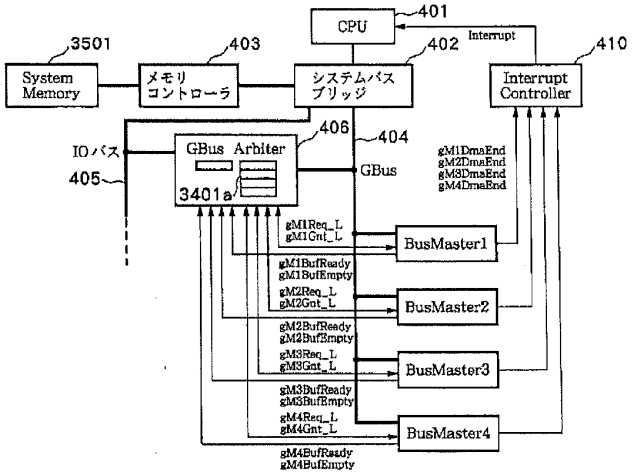
B3

【図３３】

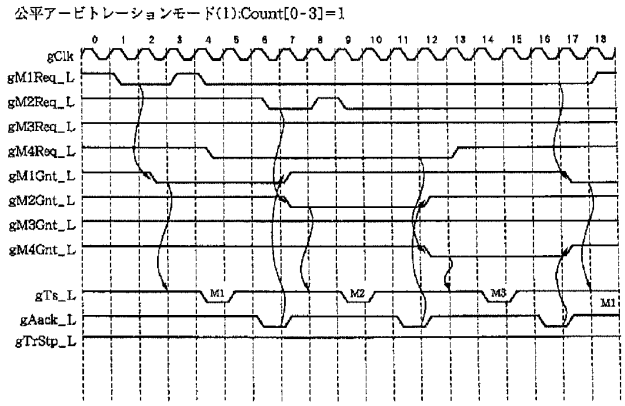

416
IOBus Interface
Core Bus I/F
IOBus Slave Controller
IOBus Master DMA Controller
Data Oe Control
Internal Register Block
FIFO
Data Path Format Convertor
Address Latch Decoder
Initiater Sequencer
Snoop Control
Lock Control
Target I/F
PCI Bus Signal I/F
Address Generator
Target Sequencer
Configuration Register
Initiater I/F
3301
3302

B3

【図３５】


CPU
401
Interrupt
3501
403
402
410
System Memory
メモリ コントローラ
システムバス ブリッジ
Interrupt Controller
406
404
IOバス
405
GBus Arbiter
GBus
3401a
gM1DmaEnd
gM2DmaEnd
gM3DmaEnd
gM4DmaEnd
gM1Req_L
gM1Gnt_L
BusMaster1
gM1BufReady
gM1BufEmpty
gM2Req_L
gM2Gnt_L
BusMaster2
gM2BufReady
gM2BufEmpty
gM3Req_L
gM3Gnt_L
BusMaster3
gM3BufReady
gM3BufEmpty
gM4Req_L
gM4Gnt_L
BusMaster4
gM4BufReady
gM4BufEmpty

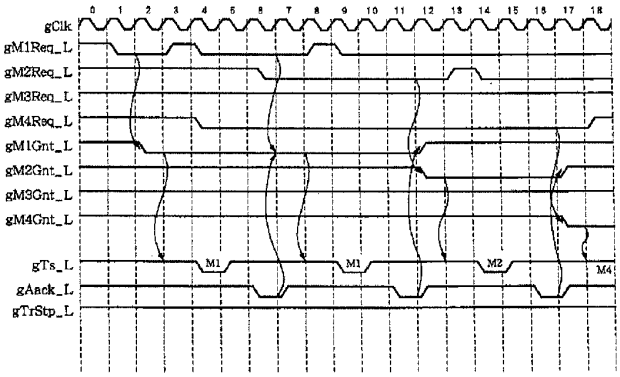
【図３６】


公平アービトレーションモード(1):Count[0-3]=1
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
gClk
gM1Req_L
gM2Req_L
gM3Req_L
gM4Req_L
gM1Gnt_L
gM2Gnt_L
gM3Gnt_L
gM4Gnt_L
gTs_L
gAack_L
gTrStp_L
M1
M2
M3
M1

B3

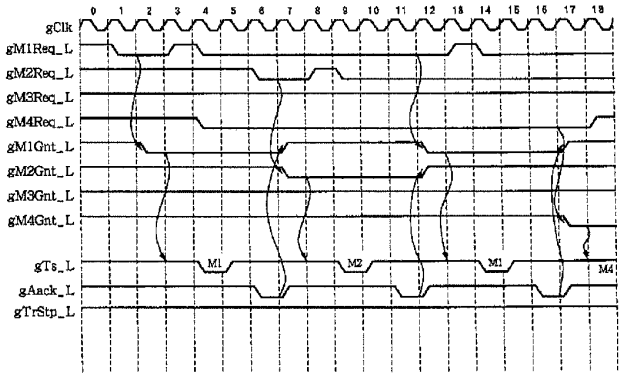
【図３７】

公平アービトレーションモード(2):Count[0]=2,Count[1-3]=1



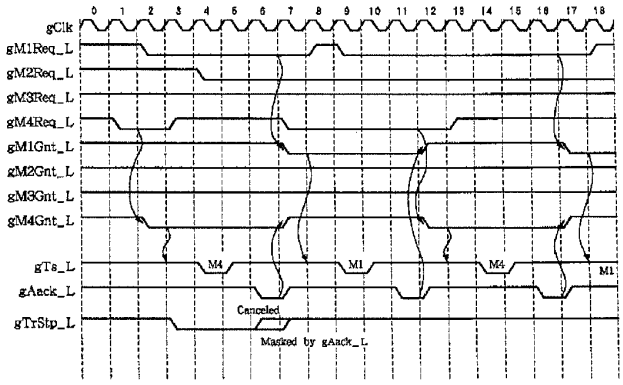
【図３８】

優先アービトレーションモード(1):High Priority Bus Master=[0],Count[0-3]=1



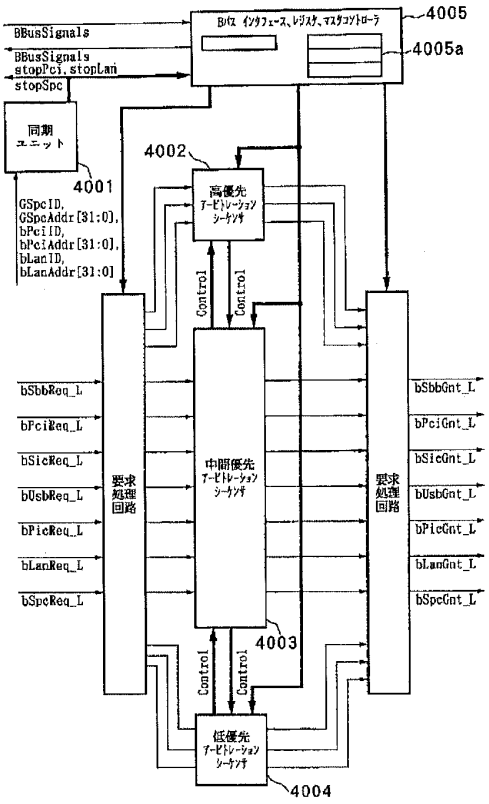
【図３９】

トランザクションストップサイクル(1):High Priority Bus Master=[0]

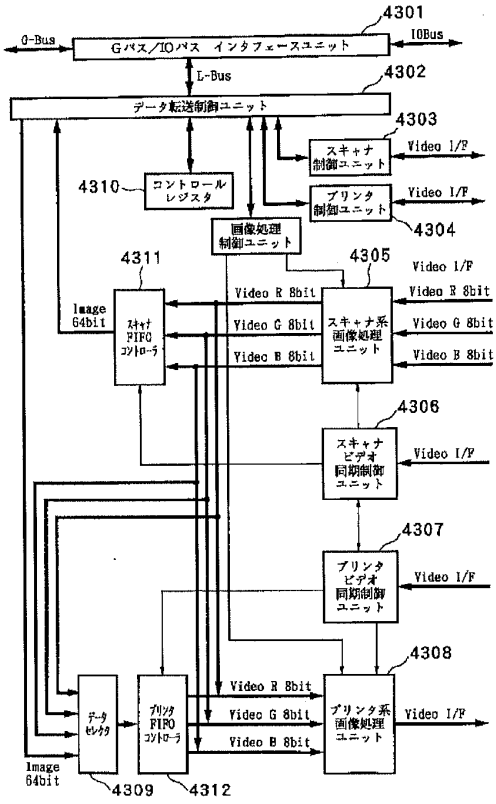


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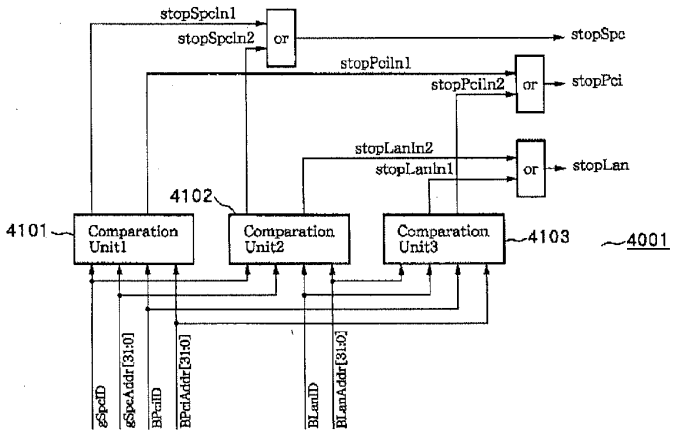
【図４０】



【図４３】

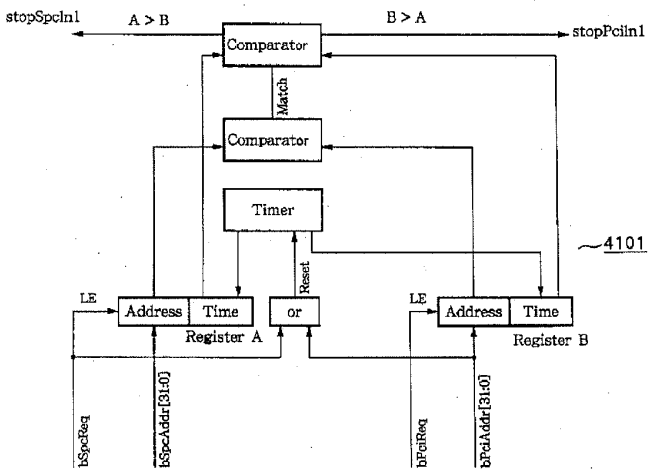


【図４１】

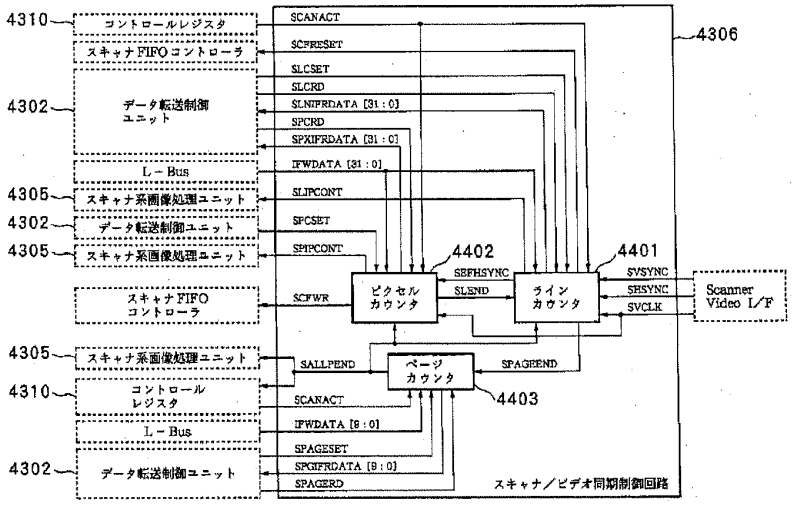


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【図４２】

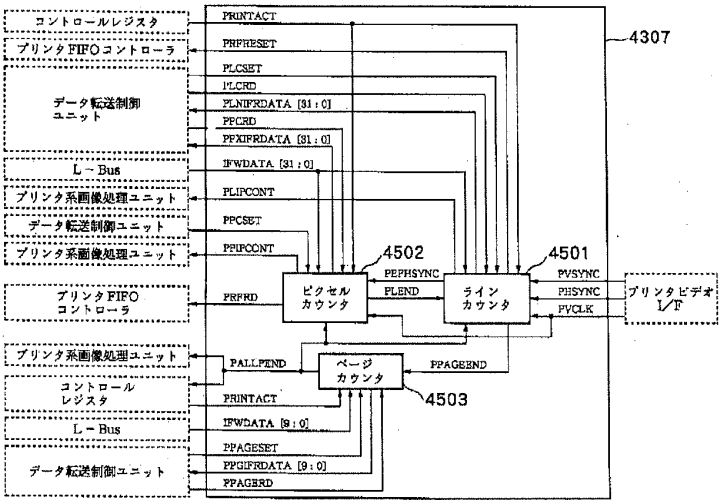

stopSpcin1
A > B
B > A
stopPciin1
Comparator
Match
Comparator
Timer
4101
Reset
LE
Address
Time
or
Register A
LE
Address
Time
Register B
bSpcReq
bSpcAddr[31:0]
bPciReq
bPciAddr[31:0]

【図４４】

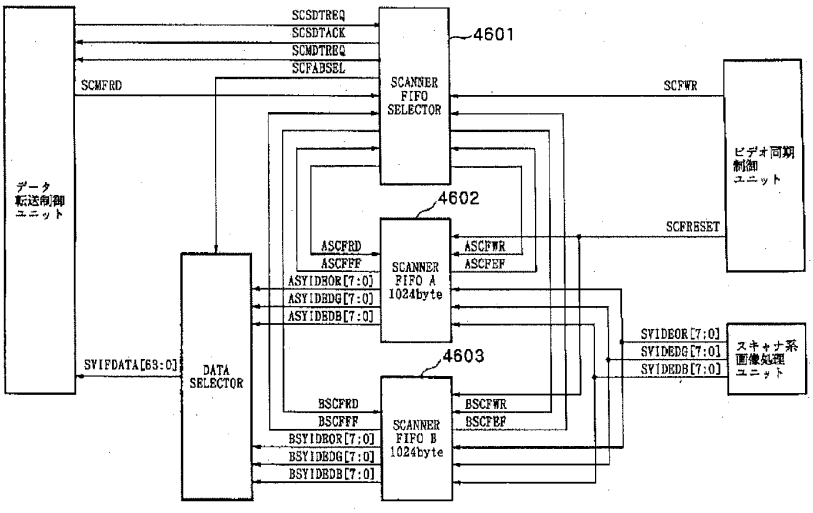

4310
コントロールレジスタ
スキャナFIFOコントローラ
4302
データ転送制御ユニット
L－Bus
4305
スキャナ系画像処理ユニット
4302
データ転送制御ユニット
4305
スキャナ系画像処理ユニット
スキャナFIFOコントローラ
4305
スキャナ系画像処理ユニット
4310
コントロールレジスタ
L－Bus
4302
データ転送制御ユニット
SCANACT
SCFRESET
SLCSET
SLCRD
SLNIFRDATA [31:0]
SPCRD
SPXIFRDATA [31:0]
IFWDATA [31:0]
SLIPCONT
SFCSET
SMPCONT
SCFWR
SALLPEND
SCANACT
IFWDATA [9:0]
SPAGESET
SPGIFRDATA [9:0]
SPAGERD
4306
4402
4401
SEFHSYNC
SLEND
ピクセルカウンタ
ラインカウンタ
SVSYNC
SHSYNC
SVCLK
Scanner Video I/F
ページカウンタ
SPAGEEND
4403
スキャナ／ビデオ同期制御回路

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【図４５】

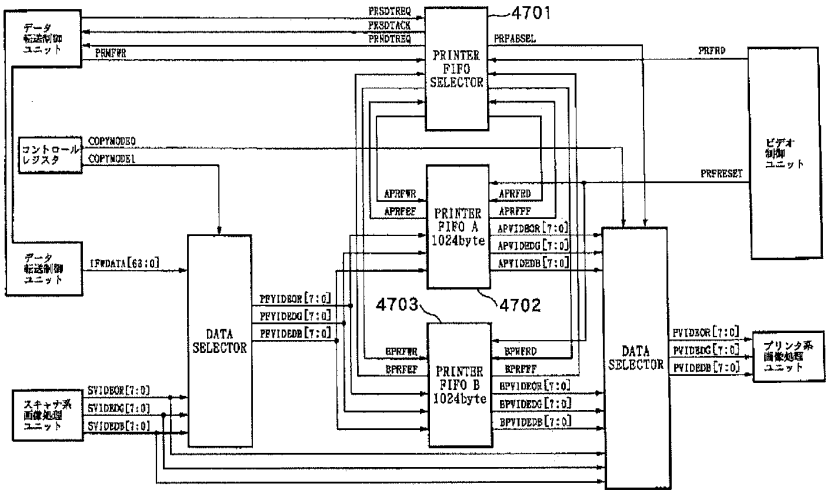

コントロールレジスタ
プリンタFIFOコントローラ
データ転送制御ユニット
L－Bus
プリンタ系画像処理ユニット
データ転送制御ユニット
プリンタ系画像処理ユニット
プリンタFIFOコントローラ
プリンタ系画像処理ユニット
コントロールレジスタ
L－Bus
データ転送制御ユニット
PRINTACT
PRFRESET
PLCSET
PLCRD
PLNIFRDATA [31:0]
PPCRD
PPXIFRDATA [31:0]
IFWDATA [31:0]
PLIFCONT
PPCSET
PPIFCONT
PRFRD
PALLPEND
PRINTACT
IFWDATA [9:0]
PPAGESET
PPGIFRDATA [9:0]
PPAGERD
4307
4502
4501
ピクセルカウンタ
ラインカウンタ
PEPHSYNC
PLEND
PVSYNC
PHSYNC
PVCLK
プリンタビデオI/F
ページカウンタ
PPAGEEND
4503

【図４６】

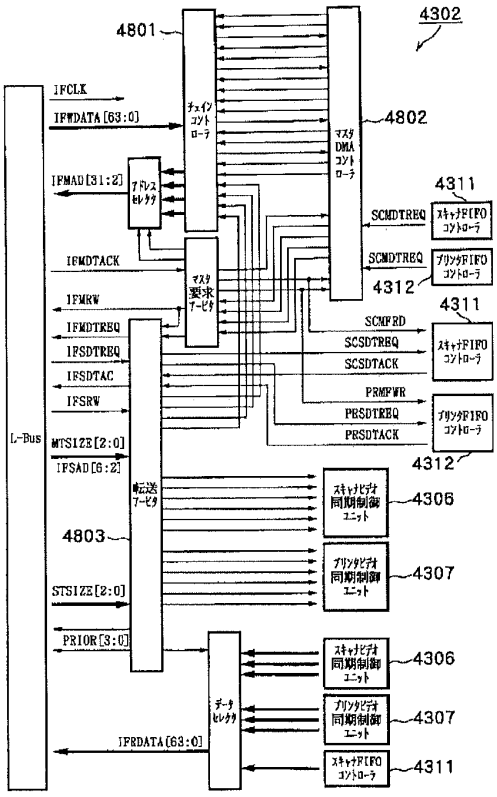

データ転送制御ユニット
SCSDTREQ
SCSDTACK
SCMDTREQ
SCFABSEL
SCMFRD
SCANNER FIFO SELECTOR
4601
SCFWR
ビデオ同期制御ユニット
SCFRESET
4602
ASCFRD
ASCFFF
ASCFWR
ASCFEF
SCANNER FIFO A 1024byte
ASYIDEOR[7:0]
ASYIDEDG[7:0]
ASYIDEDB[7:0]
SVIDEOR[7:0]
SVIDEDG[7:0]
SVIDEDB[7:0]
スキャナ系画像処理ユニット
4603
SVIFDATA[63:0]
DATA SELECTOR
BSCFRD
BSCFFF
BSCFWR
BSCFEF
SCANNER FIFO B 1024byte
BSYIDEOR[7:0]
BSYIDEDG[7:0]
BSYIDEDB[7:0]

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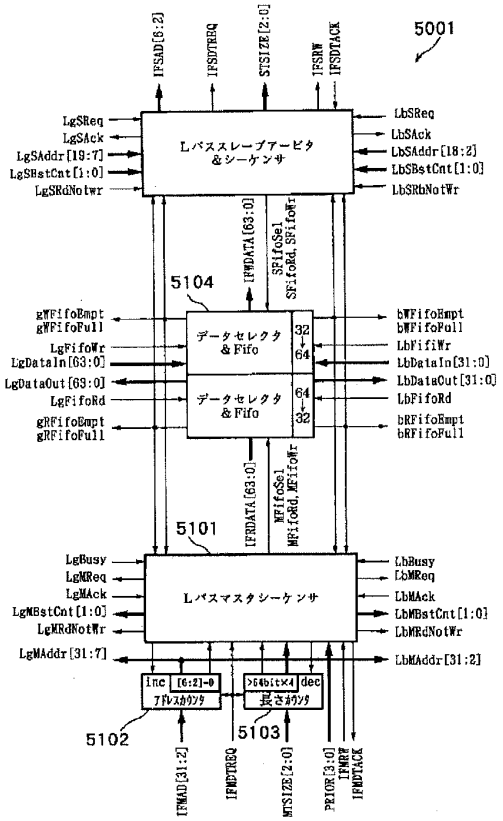
【図４７】



【図４８】

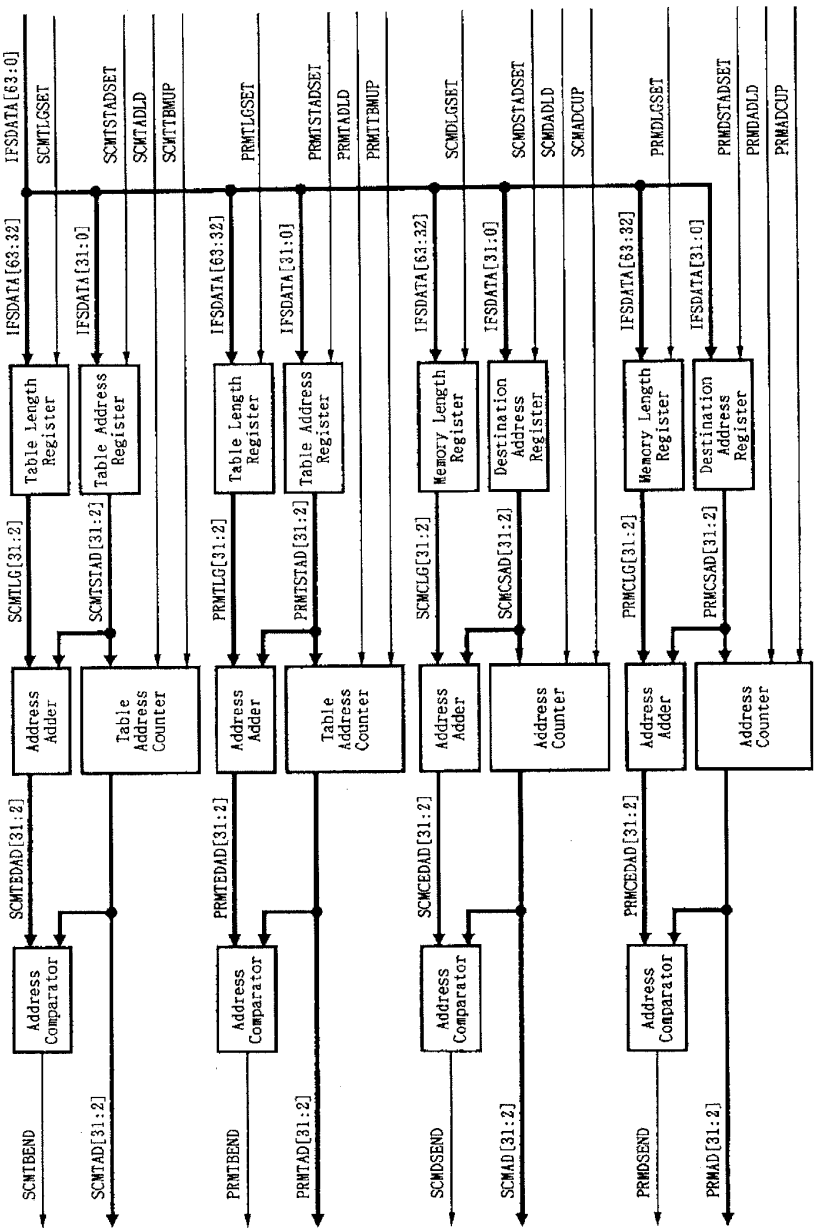


【図５１】



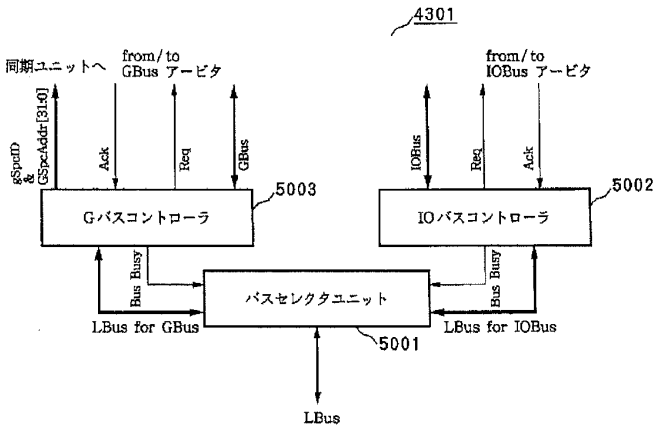
B3

【図４９】

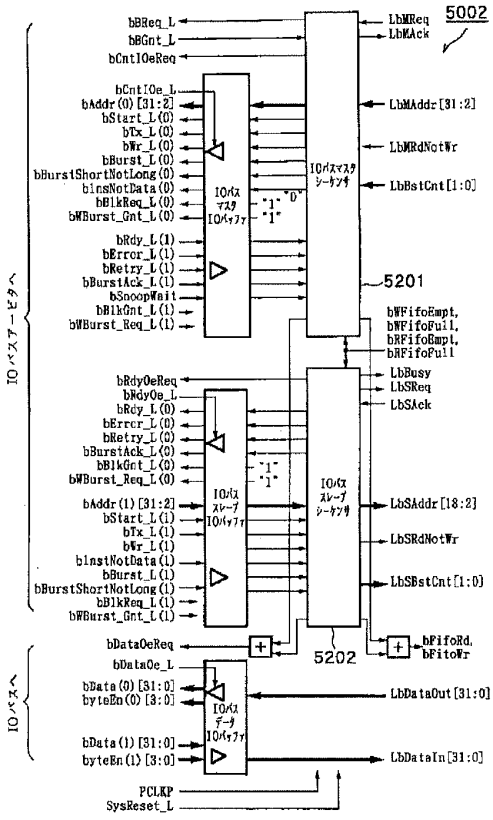

IFSDATA[63:0]
SCMTLGSET
SCMTSTADSET
SCMTADLD
SCMTTBMUP
PRMTLGSET
PRMTSTADSET
PRMTADLD
PRMTTBMUP
SCMDLGSET
SCMDSTADSET
SCMDADLD
SCMADCUP
PRMDLGSET
PRMDSTADSET
PRMDADLD
PRMADCUP
IFSDATA[63:32]
IFSDATA[31:0]
Table Length Register
Table Address Register
Memory Length Register
Destination Address Register
SCMTLG[31:2]
SCMTSTAD[31:2]
PRMTLG[31:2]
PRMTSTAD[31:2]
SCMCLG[31:2]
SCMCSAD[31:2]
PRMCLG[31:2]
PRMCSAD[31:2]
Address Adder
Table Address Counter
Address Counter
SCMTEDAD[31:2]
PRMTEDAD[31:2]
SCMCEDAD[31:2]
PRMCEDAD[31:2]
Address Comparator
SCMTBEND
SCMTAD[31:2]
PRMTBEND
PRMTAD[31:2]
SCMDSEND
SCMAD[31:2]
PRMDSEND
PRMAD[31:2]

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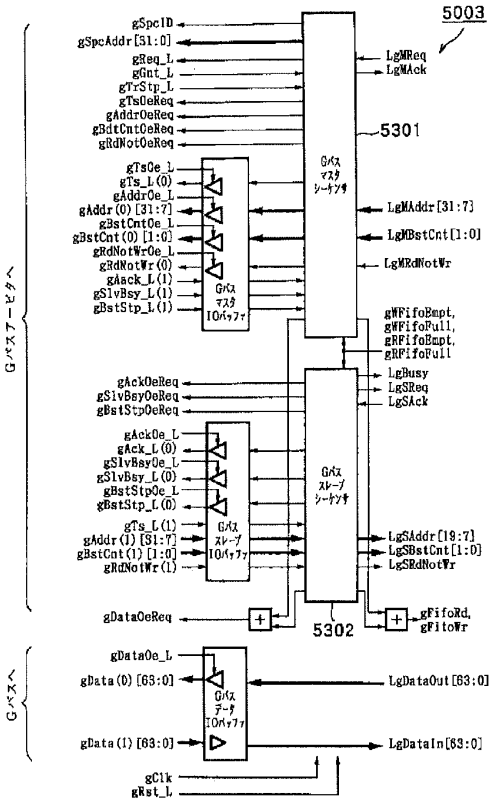
【図５０】



【図５２】

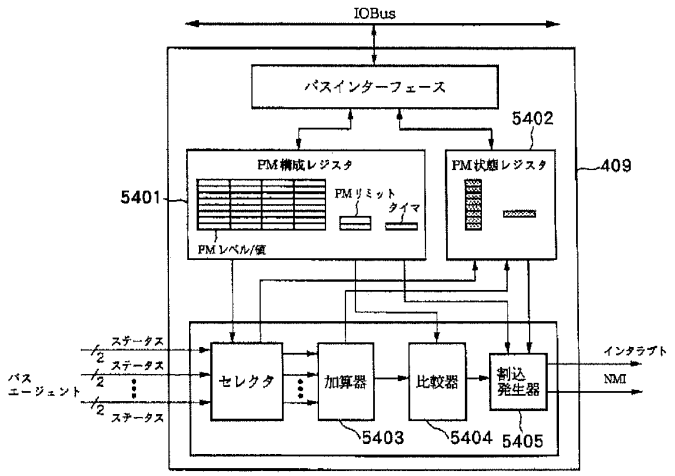


【図５３】

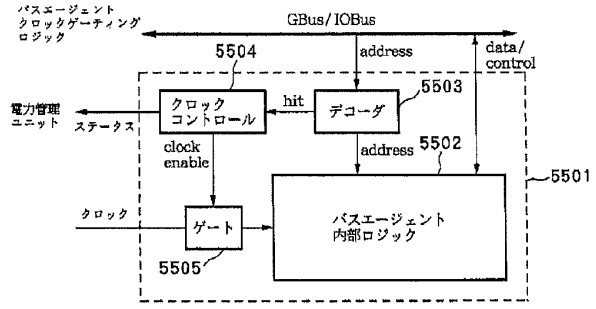


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【図５４】



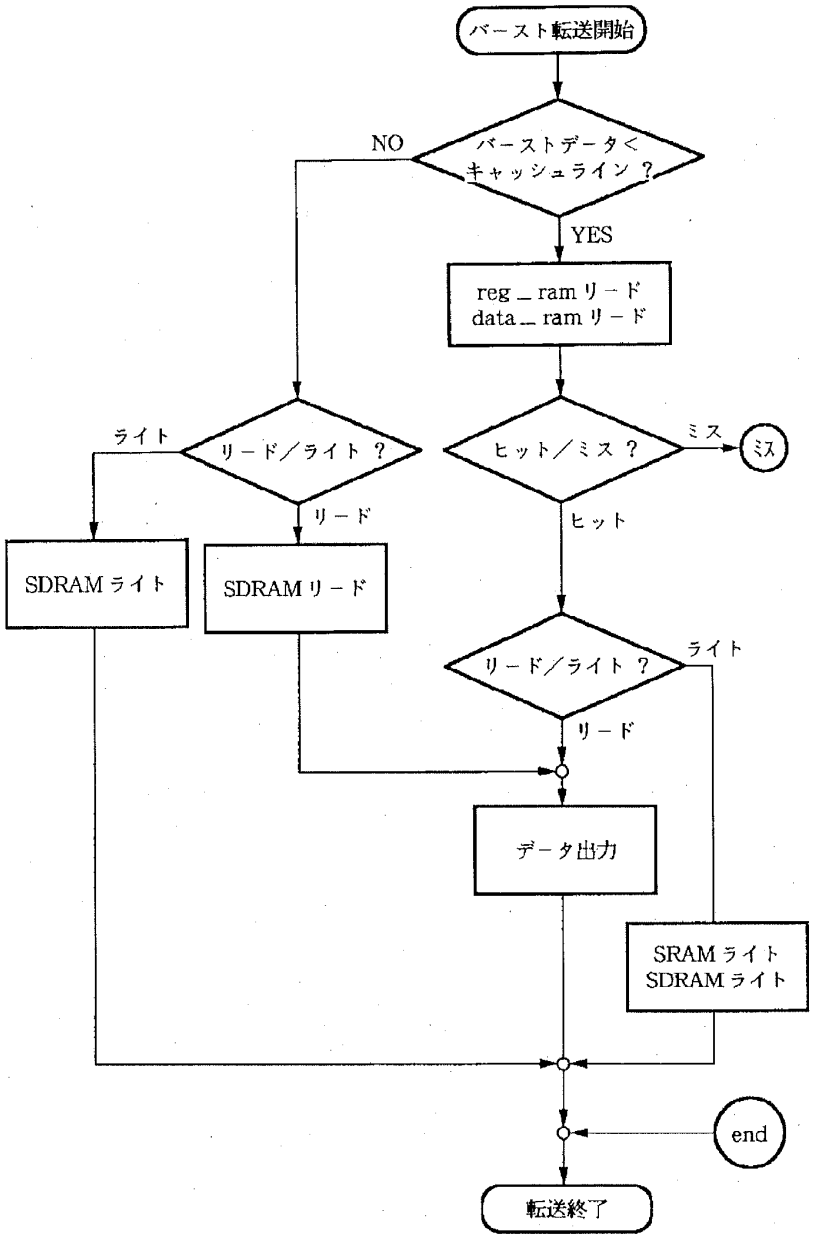
【図５５】



(クロックコントロール)
・BusのAgentは、Busのアクティビティーを検出し、クロックのOn/Offを自動で行なう。
・Sleep、WakeUp、Waitの3つのステートがある。
・SleepはBusAgentにアクティビティーがなく、クロックを停止させている状態である。
・Sleepの状態でも、デコーダー部、クロックコントロール部は動作しており、バスをモニタリング して、要求を待っている。
・デコーダーが自分のアドレスを検出すると、クロックゲートを開き、内部ロジックのクロックを動作させ、バスの要求に答える。ステートはWakeUpに移行する。
・データ転送が終了すると、Waitステートに移行し、次の要求を待つ。この時クロックは動作したままである。要求があれば、WakeUpステートに戻り、転送を行なう。また、要求を待っている間はタイマによりカウントを行ない、要求がないままカウンタがタイムアップした場合は、Sleepステートへ移り、クロックを停止させる。

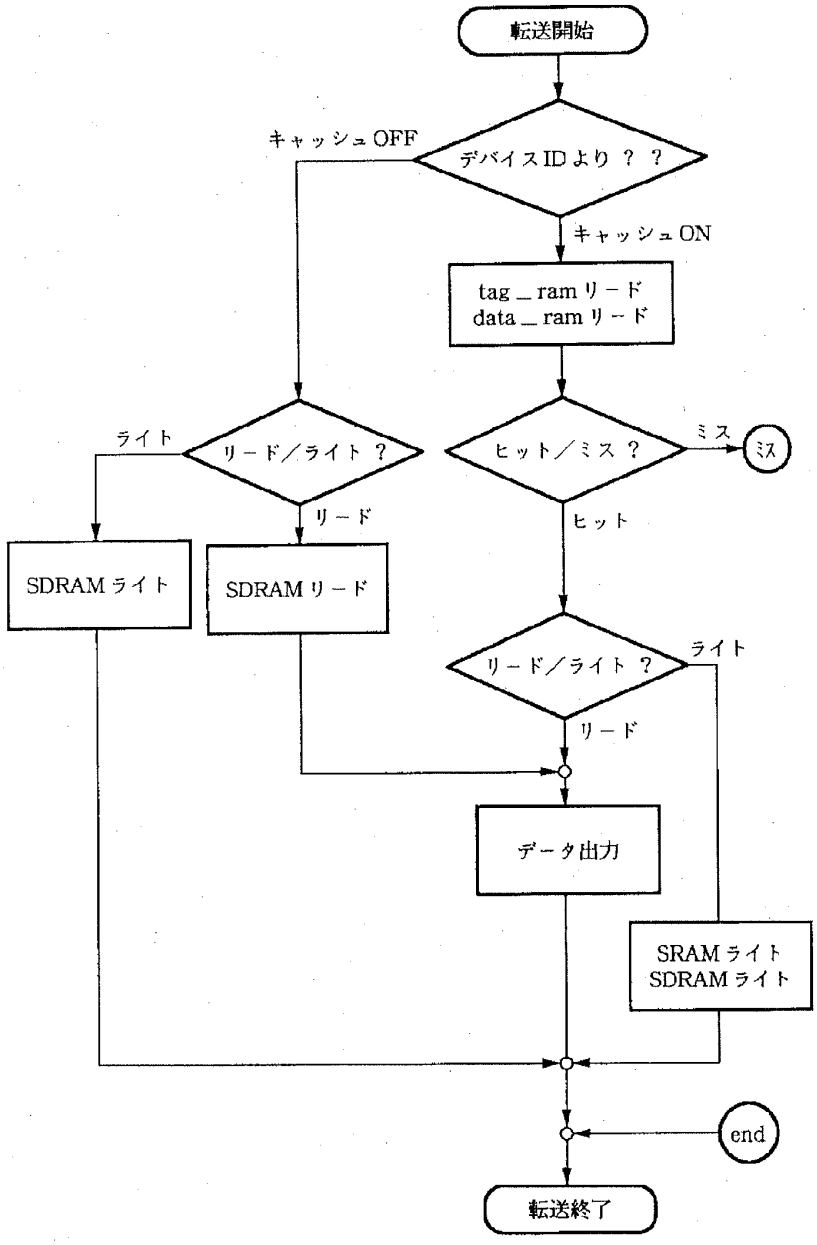
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【図５６】


バースト転送開始
バーストデータ＜
キャッシュライン ？
NO
YES
reg _ ram リード
data _ ram リード
リード／ライト ？
ライト
リード
ヒット／ミス ？
ミス
ミス
ヒット
SDRAM ライト
SDRAM リード
リード／ライト ？
ライト
リード
データ出力
SRAM ライト
SDRAM ライト
end
転送終了

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【図５８】



フロントページの続き

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Electronic Patent Application Fee Transmittal

Application Number:	12176645
Filing Date:	21-Jul-2008
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Filer:	James M. Smith/Jill Kane
Attorney Docket Number:	2037.2079-010

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Petition fee- 37 CFR 1.17(h) (Group III)	1464	1	130	130
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for continued examination	1801	1	810	810
		Total in USD ($)		**940**

Electronic Acknowledgement Receipt	
EFS ID:	9588488
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	21005
Filer:	James M. Smith/Jill Kane
Filer Authorized By:	James M. Smith
Attorney Docket Number:	2037.2079-010
Receipt Date:	04-MAR-2011
Filing Date:	21-JUL-2008
Time Stamp:	16:29:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$940
RAM confirmation Number	2932
Deposit Account	080380
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Petition to Withdraw from Issue	20372079010_Petition.pdf	58344 69ade77d2c7e1215464866b16a04c601150eac18	no	2
Warnings:					
Information:					
2	Request for Continued Examination (RCE)	20372079010_RCE.pdf	44117 2b96615f6303d197db4248be049a5171d05e8d0b	no	1
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
3	Transmittal Letter	20372079010_SIDS.pdf	74087 e4ab39c9351df4aac04663dd6f41c390877c9a57	no	3
Warnings:					
Information:					
4	Information Disclosure Statement (IDS) Filed (SB/08)	20372079010_LOR.pdf	66979 226078bdea13a7a5db7f259630254a4ec7727fbe	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
5	Foreign Reference	20372079010_B3.pdf	6273796 a7ede88a810dd601a41452d7a147abf7ee42dc8c	no	61
Warnings:					
Information:					
6	Fee Worksheet (PTO-875)	fee-info.pdf	32521 be810da0afd95d76ab52e293bb254d05c2804c72	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	6549844		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Subsection (b) of 35 U.S.C. § 132, effective on May 29, 2000, provides for continued examination of a utility or plant application filed on or after June 8, 1995. See The American Inventors Protection Act of 1999 (AIPA)

Application Number	12/176,645
Filing Date	July 21, 2008
Confirmation Number	3003
First Named Inventor	Barry Alan Hoberman
Group Art Unit	2825
Examiner Name	Lin, Sun J.
Attorney Docket Number	2037.2079-010

This is a Request for Continued Examination (RCE) under 37 CFR § 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR § 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

a. ☐ Previously submitted
   i. ☐ Consider the amendment(s)/reply under 37 CFR § 1.116 previously filed on [ ]. (Any unentered amendment(s) referred to above will be entered).
   ii ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on [ ].
   iii. ☐ Other - - [ ]

b. ☐ Please do not enter the amendment(s)/reply under 37 CFR § 1.116 previously filed on [ ]

c. ☒ Enclosed
   i. ☐ Amendment/Reply
   ii. ☐ Affidavit(s)/Declaration(s)
   iii. ☒ Supplemental Information Disclosure Statement (SIDS)
   iv. ☐ Petition for Extension of Time - [ ] month(s) - **[**separate sheet**] [**included in amend. fee trans.**]**
   v. ☒ Other - - Petition Under 37 CFR § 1.313(c)(2)

2. Miscellaneous

a. ☐ Suspension of action on the above-identified application is requested under 37 CFR § 1.103(c) for a period of [ ] months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR § 1.17(i) **required**)

b. ☐ Other - - [ ]

3. Fees The RCE fee under 37 CFR § 1.17(e) is required by 37 CFR § 1.114 when the RCE is filed.

a. ☐ A check is enclosed for the fees indicated in b. in the total amount of $[ ]
   OR
   ☒ Authorization is granted to charge the fees indicated in b. in the total amount of $940 to Deposit Account No. 08-0380.

b. i. ☒ RCE fee required under 37 CFR § 1.17(e) ($810)
   ii. ☐ Extension of time fee (37 CFR §§ 1.136 and 1.17)
   iii. ☐ Amendment Fee
   iv. ☒ Other - - Petition Fee required under 37 CFR § 1.17(h) ($130)

c. ☒ Authorization is hereby granted to charge any deficiency in fees or credit any overpayments to Deposit Account No. 08-0380.

SIGNATURE OF APPLICANT, ATTORNEY OR AGENT REQUIRED

Signature	/James M. Smith, Reg. No. 28,043/	Registration No. (Attorney/Agent)	28,043
Name (Print/Type)	James M. Smith	Date	March 4, 2011

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first class mail in an envelope addressed: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or facsimile transmitted to the US Patent & Trademark Office on the date shown below:

Signature			
Name (Print/Type)		Date	

1066319.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2825
Filed:	July 21, 2008	Examiner:	Lin, Sun J.
Confirmation No.:	3003		
For:	Power Managers For An Integrated Circuit		

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or is being facsimile transmitted to the United States Patent and Trademark Office on:

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TRANSMITTAL LETTER FOR SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Information Disclosure Statement is submitted:

☒ under 37 CFR 1.97(b), or
(Within any one of the following time periods: three months of filing national application (other than a CPA) or date of entry of the national stage in an international application; or before the mailing date of a first office action on the merits; or before the mailing of a first office action after the filing of a Request for Continued Examination).

☐ under 37 CFR 1.97(c) together with either:
- ☐ a Statement under 37 CFR 1.97(e), as checked below, or
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(After the 37 CFR 1.97(b) time period, but before any of a final action, notice of allowance, or an action that closes prosecution, whichever occurs first)

☐ under 37 CFR 1.97(d) together with:
- ☐ a Statement under 37 CFR 1.97(e), as checked below, and
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(Filed after final action, notice of allowance, whichever occurs first, or if prosecution otherwise closes, but on or before payment of the issue fee)

☐ under 37 CFR 1.97(i):
Applicant requests that the IDS and cited reference(s) be placed in the application file.
(Filed after payment of issue fee)

Statement Under 37 CFR 1.97(e)

☐ Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement; or

☐ No item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

Statement Under 37 CFR 1.704(d) (Patent Term Adjustment)
Applies to original applications (other than design) filed on or after May 29, 2000

☐ Each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in § 1.56(c) more than thirty days prior to the filing of the Information Disclosure Statement.

☒ Enclosed herewith is a Listing of References. Copies of the cited references are enclosed except as indicated below or in the attached Listing of References.

☐ Copies of the cited references submitted with an Information Disclosure Statement in prior application, U.S. Application No. [ ], to which priority under 35 U.S.C. 120 is claimed, are not required under 37 CFR 1.98(d)(1) and (2) and are thus not provided.

☐ The listed references were cited in the enclosed Search Report in counterpart foreign application [add application number], which is listed in the attached Listing of References.

☒ The "concise explanation" requirement (non-English references) for reference B3 under 37 CFR 1.98(a)(3) is satisfied by:

- ☐ the explanation provided on the attached sheet.
- ☐ the explanation provided in the Specification.
- ☐ submission of the enclosed International Search Report.
- ☐ submission of the enclosed English-language version of a foreign Search Report and/or foreign Office Action.
- ☒ the enclosed English language abstract.

Method of payment:

☐ Authorization is NOT granted to charge any fees which may be due in this matter to our Deposit Account.

☐ Please charge Deposit Account 08-0380 in the amount of $[ ].

☐ A check for the fee noted above is enclosed, or the fee has been included in the check with the accompanying Reply.

☒ Please charge any deficiency in fees and credit any overpayment to Deposit Account 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By /James M. Smith, Reg. No. 28,043/
James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Dated: March 4, 2011

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/176,645	07/21/2008	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	03/04/2011	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 64	Minus	** 64	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 8	Minus	***10	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/VICTORIA BROWN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

21005 7590 02/17/2011
HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/176,645	07/21/2008	Barry Alan HOBERMAN	2037.2079-010	3003

TITLE OF INVENTION: POWER MANAGERS FOR AN INTEGRATED CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	05/17/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
LIN, SUN J	2825	716-133000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Hamilton, Brook, Smith & Reynolds, P.C.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: MOSAID Technologies Incorporated

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Ottawa, Ontario, Canada

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 08-0380 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date 2/18/11

Typed or printed name James M. Smith Registration No. 28,043

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Electronic Patent Application Fee Transmittal	
Application Number:	12176645
Filing Date:	21-Jul-2008
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Filer:	James M. Smith/Jill Kane
Attorney Docket Number:	2037.2079-010
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1810**

Electronic Acknowledgement Receipt	
EFS ID:	9476468
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	21005
Filer:	James M. Smith/Jill Kane
Filer Authorized By:	James M. Smith
Attorney Docket Number:	2037.2079-010
Receipt Date:	18-FEB-2011
Filing Date:	21-JUL-2008
Time Stamp:	16:04:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1810
RAM confirmation Number	2639
Deposit Account	080380
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Issue Fee Payment (PTO-85B)	20372079010_IF.pdf	168979 4c9c0a7e28b9c66aae878b9ba0189441933 5d4bf	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	32174 32cdfc01c865f4010a86ef1520f595d68b65 b6cc	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	201153		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

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530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

EXAMINER
LIN, SUN J

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/17/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/176,645	07/21/2008	Barry Alan HOBERMAN	2037.2079-010	3003

TITLE OF INVENTION: POWER MANAGERS FOR AN INTEGRATED CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	05/17/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/176,645	07/21/2008	Barry Alan HOBERMAN	2037.2079-010	3003

TITLE OF INVENTION: POWER MANAGERS FOR AN INTEGRATED CIRCUIT

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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EXAMINER	ART UNIT	CLASS-SUBCLASS
LIN, SUN J	2825	716-133000

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❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
❑ Issue Fee
❑ Publication Fee (No small entity discount permitted)
❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
❑ A check is enclosed.
❑ Payment by credit card. Form PTO-2038 is attached.
❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/176,645	07/21/2008	Barry Alan HOBERMAN	2037.2079-010	3003

21005 7590 02/17/2011

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/17/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 438 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 438 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/176,645	HOBERMAN ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment & Remarks filed on 01/26/2011*.

2. ☒ The allowed claim(s) is/are *76-139, renumbered (37 CFR 1.126)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☒ Examiner's Comment Regarding Requirement for Deposit of Biological Material 12/22/10,1/5/11,2/15/11
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This office action is in response to *Amendment and Remarks* filed on *01/26/2011* regarding patent application *12/176,645* filed on *07/21/2008*. Claims 1 – 75 were cancelled. Claims 132 – 139 are newly added. Claims 76 – 139 remain pending in the application.

Reasons for Allowance

2. Claims 76 – 139 are allowed over the prior art of record. An examiner's statement of reasons for allowance is given in the following:

Claims 76 – 139 are allowed because the prior art does not teach or fairly suggest the following subject matter:

- An integrated circuit comprising: *a integrated circuit chip; a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency; and a power management processor (i.e., power manager) disposed on the integrated circuit chip and coupled to each of the power islands configured to monitor one or more power consumption signals to individually control each of the power consumptions, and the power management processor (i.e., power manger) being configured to change power consumption in at least one of the power islands in response to a power consumption change request* in combination with other limitations cited in independent ***Claim 76***, ***Claim 82***, ***Claim 89*** and ***Claim 95***, respectively;
- A system comprising: *an integrated circuit; a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency; and a power management processor (i.e., power manager) coupled to each of the power islands configured to monitor one or more power consumption signals to individually control each of the power consumptions, and the power management processor (i.e., power manger) being configured to change power consumption in at least one of the power islands in response to a power consumption change request* in combination

with other limitations cited in independent ***Claim 102***, ***Claim 109***, ***Claim 117*** and ***Claim 124***, respectively.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (571) 272−1899. The examiner can normally be reached on Monday to Friday from 9:00am to 6:00pm.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (in USA or CANADA) or 571-272-1000.

/Sun J. Lin/
Primary Examiner, Art Unit 2825

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12176645	HOBERMAN ET AL.
	Examiner	Art Unit
	Sun J Lin	2825

SEARCHED			
Class	Subclass	Date	Examiner
716	100,126,127,132,133	2/9/11	/JSL/

SEARCH NOTES		
Search Notes	Date	Examiner
EAST [US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB]	2/9/11	/JSL/

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
716	133	2/9/11	/JSL/
716	100	2/9/11	/JSL/
716	126	2/9/11	/JSL/
716	127	2/9/11	/JSL/
716	132	2/9/11	/JSL/

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	17	716/100	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:01
L2	25	716/126	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:01
L3	3	716/127	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:01
L4	7	716/132	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:01
L5	4	716/133	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:01

L6	0	(716/100).ccls. and (integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with signal$2) and ((supply adj voltage) with (operat$3 adj frequency)) and (power adj manage$4) and (processor) and (change adj request)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:09
L7	0	(716/126).ccls. and (integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with signal$2) and ((supply adj voltage) with (operat$3 adj frequency)) and (power adj manage$4) and (processor) and (change adj request)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:10
L8	0	(716/127).ccls. and (integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with signal$2) and ((supply adj voltage) with (operat$3 adj frequency)) and (power adj manage$4) and (processor) and (change adj request)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:10

L9	0	(716/132).ccls. and (integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with signal$2) and ((supply adj voltage) with (operat$3 adj frequency)) and (power adj manage$4) and (processor) and (change adj request)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:10
L10	0	(716/133).ccls. and (integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with signal$2) and ((supply adj voltage) with (operat$3 adj frequency)) and (power adj manage$4) and (processor) and (change adj request)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:10
L11	0	("716"/$).ccls. and (integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with signal$2) and ((supply adj voltage) with (operat$3 adj frequency)) and (power adj manage$4) and (processor) and (change adj request)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:10

L12	0	(integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with signal$2) and ((supply adj voltage) with (operat$3 adj frequency)) and (power adj manage$4) and (processor) and (change adj request)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:12
L14	0	(integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal$2 or level$2)) and ((supply adj voltage) with (operat$3 adj frequenc$3)) and (power adj manage$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:18
L15	8	(integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal$2 or level$2)) and ((supply adj voltage) and (operat$3 adj frequenc$3)) and (power adj manage$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:20

L17	0	((integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal$2 or level$2)) and ((supply adj voltage) and (operat$3 adj frequenc$3)) and (power adj manage$4)). CLM.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:22
L18	0	(integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal$2 or level$2)) and ((supply adj voltage) and (operat$3 adj frequenc$3)) and (power adj manage$4) and (change adj request)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:24
L21	0	(integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal$2 or level$2)) and ((supply adj voltage) with (operat$3 adj frequenc$3)) and (power adj manage$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:29

L22	1	(integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal$2 or level$2)) and ((supply adj voltage) same (operat$3 adj frequenc$3)) and (power adj manage$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:31
L24	1	(integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal$2 or level$2)) and ((supply adj voltage) same (operat$3 adj frequenc$3)) and (power adj manage$4) and (change or request)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:34
L25	2	(integrated adj circuit) and ((power or voltage) adj island $2) and ((power adj consumption $2) with (signal$2 or level$2)) and ((supply adj voltage) and (operat$3 adj frequenc$3)) and (power adj manage$4) and (request)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/02/09 17:35

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L13	0	(integrated adj circuit) and ((power or voltage) adj island$2) and ((power adj consumption$2) with signal$2) and ((supply adj voltage) with (operat$3 adj frequency)) and (power adj manage $4) and (processor) and (change adj request)	USPAT; UPAD	OR	OFF	2011/02/09 17:12
L16	3	(integrated adj circuit) and ((power or voltage) adj island$2) and ((power adj consumption$2) with (signal$2 or level$2)) and ((supply adj voltage) and (operat$3 adj frequenc$3)) and (power adj manage $4)	USPAT; UPAD	OR	OFF	2011/02/09 17:22
L19	0	(integrated adj circuit) and ((power or voltage) adj island$2) and ((power adj consumption$2) with (signal$2 or level$2)) and ((supply adj voltage) and (operat$3 adj frequenc$3)) and (power adj manage $4) and (change adj request)	USPAT; UPAD	OR	OFF	2011/02/09 17:24

L20	0	(integrated adj circuit) and ((power or voltage) adj island$2) and ((power adj consumption$2) with (signal$2 or level$2)) and ((supply adj voltage) with (operat$3 adj frequenc$3)) and (power adj manage $4) and (change adj request)	USPAT; UPAD	OR	OFF	2011/02/09 17:29
L23	1	(integrated adj circuit) and ((power or voltage) adj island$2) and ((power adj consumption$2) with (signal$2 or level$2)) and ((supply adj voltage) same (operat$3 adj frequenc$3)) and (power adj manage $4)	USPAT; UPAD	OR	OFF	2011/02/09 17:33
L26	0	(integrated adj circuit) and ((power or voltage) adj island$2) and ((power adj consumption$2) with (signal$2 or level$2)) and ((supply adj voltage) and (operat$3 adj frequenc$3)) and (power adj manage $4) and (request)	USPAT; UPAD	OR	OFF	2011/02/09 17:38

2/9/11 5:38:58 PM
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12176645	HOBERMAN ET AL.
	Examiner	Art Unit
	Sun J Lin	2825

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☒ CPA ☒ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	12/19/2010	02/09/2011							
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CLAIM		DATE								
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CLAIM		DATE								
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29	101	✓	=							
31	102	✓	=							
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33	104	✓	=							
34	105	✓	=							
35	106	✓	=							
36	107	✓	=							
37	108	✓	=							

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CLAIM		DATE								
Final	Original	12/19/2010	02/09/2011							
39	109	✓	=							
40	110	✓	=							
41	111	✓	=							
42	112	✓	=							
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15	134		=							
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30	136		=							
38	137		=							
47	138		=							
55	139		=							

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12176645	HOBERMAN ET AL.
	Examiner	**Art Unit**
	Sun J Lin	2825

ORIGINAL		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
716	133	G	0	6	F	17 / 50 (2006.01.01)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
716	100	126	127	132	

☐ Claims renumbered in the same order as presented by applicant ☒ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	76	19	92	37	108	56	124								
2	77	20	93	39	109	57	125								
3	78	21	94	40	110	58	126								
4	79	23	95	41	111	59	127								
5	80	24	96	42	112	60	128								
6	81	25	97	43	113	61	129								
8	82	26	98	44	114	62	130								
9	83	27	99	45	115	63	131								
10	84	28	100	46	116	64	132								
11	85	29	101	48	117	7	133								
12	86	31	102	49	118	15	134								
13	87	32	103	50	119	22	135								
14	88	33	104	51	120	30	136								
16	89	34	105	52	121	38	137								
17	90	35	106	53	122	47	138								
18	91	36	107	54	123	55	139								

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	64	
/Sun J Lin/ Primary Examiner.Art Unit 2825	02/09/2011	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **January 5, 2011** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry A. Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

U.S. PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
	A4	5,996,084	11-30-1999	Watts
	A5	6,307,281 B1	10-23-2001	Houston

Copies of issued U.S. Patents and Published U.S. Applications are not required and are not being provided. We are not listing separately any prior U.S. Patent Office communications regarding the cited documents because the Examiner has access to any such actions through PAIR.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JSL/

EXAMINER	/Sun J. Lin/	DATE CONSIDERED	02/12/2011

Supp LOR (Jan 2011)

1048916.1

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **December 22, 2010** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

U.S. PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
/JSL/	A3	6,523,150 B1	02-18-2003	Buffet, et al.
	A4			
	A5			
	A6			
	A7			
	A8			
	A9			
	A10			
	A11			
	A12			
	A13			
	A14			
	A15			
	A16			
	A17			
	A18			

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EXAMINER	DATE CONSIDERED
/Sun J. Lin/	02/12/2011

1045377.1

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **December 22, 2010** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

FOREIGN PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Country Code-Number-Kind Code (if known)	DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
/JSL/	B2	CN 1353454 A	06-12-2002	IBM
	B3			
	B4			
	B5			
	B6			
	B7			
	B8			
	B9			
	B10			
	B11			
	B12			
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	B16			
	B17			
	B18			
	B19			

EXAMINER	/Sun J. Lin/	DATE CONSIDERED	02/12/2011

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **December 22, 2010** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

Examiner's Initials	Ref. No.	**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent Pages, Etc.)*
/JSL/	C5	Search Report: ROC (Taiwan) Patent Application No. 093112998 (Translation), completed October 31, 2010.
	C6	
	C7	
	C8	
	C9	
	C10	
	C11	
	C12	
	C13	
	C14	
	C15	
	C16	
	C17	
	C18	
	C19	
	C20	

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EXAMINER	DATE CONSIDERED
/Sun J. Lin/	/Sun J. Lin/

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **February 15, 2011** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

U.S. PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
/JSL/	A6	6,779,169 B1	08-17-2004	Singh, et al.
/JSL/	A7	6,883,152 B2	04-19-2005	Bednar, et al.

Copies of issued U.S. Patents and Published U.S. Applications are not required and are not being provided. We are not listing separately any prior U.S. Patent Office communications regarding the cited documents because the Examiner has access to any such actions through PAIR.

EXAMINER	DATE CONSIDERED
/Sun J. Lin/	02/16/2011

1060632.1

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **February 15, 2011** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

Examiner's Initials	Ref. No.	**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent Pages, Etc.)*
/JSL/	C6	U.S. Office Action mailed February 14, 2011 for U.S. Application No. 12/332,529 (Attorney Docket No. 2037.2079-012).

***Copies of any U.S. Office Communications or non-published U.S. Patent Applications are not being provided because the examiner has access to such documents through PAIR. We are not listing separately any prior U.S. Patent Office communications regarding the cited documents because the Examiner has access to any such actions through PAIR**

EXAMINER /Sun J. Lin/	DATE CONSIDERED 02/16/2011

1060632.1

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **February 15, 2011** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

U.S. PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
	A6	6,779,169 B1	08-17-2004	Singh, et al.
	A7	6,883,152 B2	04-19-2005	Bednar, et al.

Copies of issued U.S. Patents and Published U.S. Applications are not required and are not being provided. We are not listing separately any prior U.S. Patent Office communications regarding the cited documents because the Examiner has access to any such actions through PAIR.

EXAMINER	DATE CONSIDERED

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **February 15, 2011** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

Examiner's Initials	Ref. No.	**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent Pages, Etc.)*
	C6	U.S. Office Action mailed February 14, 2011 for U.S. Application No. 12/332,529 (Attorney Docket No. 2037.2079-012).

***Copies of any U.S. Office Communications or non-published U.S. Patent Applications are not being provided because the examiner has access to such documents through PAIR. We are not listing separately any prior U.S. Patent Office communications regarding the cited documents because the Examiner has access to any such actions through PAIR**

EXAMINER	DATE CONSIDERED

Electronic Patent Application Fee Transmittal	
Application Number:	12176645
Filing Date:	21-Jul-2008
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Filer:	James M. Smith/Jill Kane
Attorney Docket Number:	2037.2079-010
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt	
EFS ID:	9447367
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	21005
Filer:	James M. Smith/Jill Kane
Filer Authorized By:	James M. Smith
Attorney Docket Number:	2037.2079-010
Receipt Date:	15-FEB-2011
Filing Date:	21-JUL-2008
Time Stamp:	14:49:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	1212
Deposit Account	080380
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Transmittal Letter	20372079010_SIDS.pdf	74055 b26f5b64a0eb83f34bc35ba8638820162030dfb2	no	3
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Filed (SB/08)	20372079010_LOR.pdf	83279 01e85e1a836720497b69c3237b9413e59ea047c5	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Fee Worksheet (PTO-875)	fee-info.pdf	30581 a228e6f7c0d68e3c3d249d147e76f8b2b2873329	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	187915		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2825
Filed:	July 21, 2008	Examiner:	Lin, Sun J.
Confirmation No.:	3003		
For:	Power Managers For An Integrated Circuit		

CERTIFICATE OF MAILING OR TRANSMISSION

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_____ _____
Date Signature

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Typed or printed name of person signing certificate

TRANSMITTAL LETTER FOR SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Information Disclosure Statement is submitted:

☐ under 37 CFR 1.97(b), or
(Within any one of the following time periods: three months of filing national application (other than a CPA) or date of entry of the national stage in an international application; or before the mailing date of a first office action on the merits; or before the mailing of a first office action after the filing of a Request for Continued Examination).

☒ under 37 CFR 1.97(c) together with either:
- ☐ a Statement under 37 CFR 1.97(e), as checked below, or
- ☒ a $180.00 fee under 37 CFR 1.17(p), or
(After the 37 CFR 1.97(b) time period, but before any of a final action, notice of allowance, or an action that closes prosecution, whichever occurs first)

☐ under 37 CFR 1.97(d) together with:
- ☐ a Statement under 37 CFR 1.97(e), as checked below, and
- ☐ a $180.00 fee under 37 CFR 1.17(p), or
(Filed after final action, notice of allowance, whichever occurs first, or if prosecution otherwise closes, but on or before payment of the issue fee)

☐ under 37 CFR 1.97(i):
Applicant requests that the IDS and cited reference(s) be placed in the application file.
(Filed after payment of issue fee)

Statement Under 37 CFR 1.97(e)

☐ Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement; or

☐ No item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

Statement Under 37 CFR 1.704(d) (Patent Term Adjustment)
Applies to original applications (other than design) filed on or after May 29, 2000

☐ Each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in § 1.56(c) more than thirty days prior to the filing of the Information Disclosure Statement.

☒ Enclosed herewith is a Listing of References. Copies of the cited references are enclosed except as indicated below or in the attached Listing of References.

☐ Copies of the cited references submitted with an Information Disclosure Statement in prior application, U.S. Application No. [ ], to which priority under 35 U.S.C. 120 is claimed, are not required under 37 CFR 1.98(d)(1) and (2) and are thus not provided.

☐ The listed references were cited in the enclosed Search Report in counterpart foreign application [add application number], which is listed in the attached Listing of References.

☐ The "concise explanation" requirement (non-English references) for reference(s) [ ] under 37 CFR 1.98(a)(3) is satisfied by:

- ☐ the explanation provided on the attached sheet.
- ☐ the explanation provided in the Specification.
- ☐ submission of the enclosed International Search Report.
- ☐ submission of the enclosed English-language version of a foreign Search Report and/or foreign Office Action.
- ☐ the enclosed English language abstract.

Method of payment:

☐ Authorization is NOT granted to charge any fees which may be due in this matter to our Deposit Account.

☒ Please charge Deposit Account 08-0380 in the amount of $180.

☐ A check for the fee noted above is enclosed, or the fee has been included in the check with the accompanying Reply.

☒ Please charge any deficiency in fees and credit any overpayment to Deposit Account 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By /James M. Smith, Reg. No. 28,043/

James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Dated: February 15, 2011

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	12/176,645	HOBERMAN ET AL.	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : January 26, 2011	**This patent is subject to a Terminal Disclaimer**	

Approved/Disapproved by:
Henry D. Jefferson

U.S. Patent and Trademark Office

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2825
Filed:	July 21, 2008	Examiner:	Lin, Sun J.
Confirmation No:	3003		
For:	Power Managers for an Integrated Circuit		

CERTIFICATE OF MAILING OR TRANSMISSION

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_____ _____
Date Signature

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Typed or printed name of person signing certificate

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Amendment is being filed in response to the Office Action mailed from the U.S. Patent and Trademark Office on December 23, 2010 in the above-identified application. Reconsideration and further examination are requested.

Please amend the application as follows:

Amendments to the Specification

Please replace the paragraph at page 1, paragraph [0001] with the following amended paragraph:

This application is a continuation of U.S. application Ser. No. 11/336,097 filed on ~~Jan.~~ January 20, 2006 entitled "Power Managers for an Integrated Circuit" and which issued on _____ August 19, 2008 as U.S. Patent No. 7,415,680, ~~patent Ser. No. _____~~, which is a continuation of U.S. application Ser. No. 10/840,893 filed on May 7, 2004 and entitled "Managing Power on Integrated Circuits Using Power Islands" and which issued on May 23, 2006 as U.S. Pat. No. 7,051,306 which claims the benefit of U.S. Provisional Application Ser. No. 60/468,742 titled "System and Method for Managing Power in Integrated Circuits," filed May 7, 2003, which are each hereby incorporated by reference.

Please replace the paragraph at page 1, paragraph [0003] with the following amended paragraph:

One design goal for integrated circuits is to reduce power consumption. Devices with batteries such as cell phones and laptops especially need a reduction in power consumption in the integrated circuit to extend the charge of the battery. Additionally, a reduction in power consumption prevents overheating and lowers the heat dissipation ~~heafdissipation~~ of the integrated circuit, which in some cases, eliminates or simplifies the heat sinks and/or fans for the integrated circuit.

Amendments to the Claims

Please amend Claims 76, 80, 82, 87, 89, 93, 95, 100, 102, 106, 109, 114, 117, 121, 124 and 129. Please add new Claims 132-139. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1-75. (Cancelled).

76. (Currently Amended) An integrated circuit comprising:

an integrated circuit chip;

a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

one or more power consumption signals indicating one or more of the power consumptions;

a power management processor disposed on the integrated circuit chip and coupled to each of the power islands configured to monitor the one or more power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

77. (Previously Presented) The integrated circuit as claimed in Claim 76 wherein the power management software is embedded firmware in the integrated circuit.

78. (Previously Presented) The integrated circuit as claimed in Claim 77 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

79. (Previously Presented) The integrated circuit as claimed in Claim 77 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

80. (Currently Amended) The integrated circuit as claimed in Claim 76 wherein each of the power consumptions is further controlled by stopping [[the]] a clock.

81. (Previously Presented) The integrated circuit as claimed in Claim 80 wherein stopping the clock comprises clock gating.

82. (Currently Amended) An integrated circuit comprising:

an integrated circuit chip;

a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

one or more power consumption signals indicating one or more of the power consumptions;

a power manager disposed on the integrated circuit chip and coupled to each of the power islands configured to monitor the one or more power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

83. (Previously Presented) The integrated circuit as claimed in Claim 82 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.

84. (Previously Presented) The integrated circuit as claimed in Claim 83 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

85. (Previously Presented) The integrated circuit as claimed in Claim 83 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

86. (Previously Presented) The integrated circuit as claimed in Claim 82 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.

87. (Currently Amended) The integrated circuit as claimed in Claim 82 wherein each of the power consumptions is further controlled by stopping [[the]] a clock.

88. (Previously Presented) The integrated circuit as claimed in Claim 87 wherein stopping the clock comprises clock gating.

89. (Currently Amended) An integrated circuit comprising:

an integrated circuit chip;

a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

a power management processor disposed on the integrated circuit chip and coupled to each of the power islands and configured to monitor the power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

90. (Previously Presented) The integrated circuit as claimed in Claim 89 wherein the power management software is embedded firmware in the integrated circuit.

91. (Previously Presented) The integrated circuit as claimed in Claim 90 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

92. (Previously Presented) The integrated circuit as claimed in Claim 90 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

93. (Currently Amended) The integrated circuit as claimed in Claim 89 wherein each of the power consumptions is further controlled by stopping [[the]] a clock.

94. (Previously Presented) The integrated circuit as claimed in Claim 93 wherein stopping the clock comprises clock gating.

95. (Currently Amended) An integrated circuit comprising:

a integrated circuit chip;

a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

a power manager disposed on the integrated circuit chip coupled to each of the power islands and configured to monitor the power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

96. (Previously Presented) The integrated circuit as claimed in Claim 95 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.

97. (Previously Presented) The integrated circuit as claimed in Claim 96 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

98. (Previously Presented) The integrated circuit as claimed in Claim 96 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

99. (Previously Presented) The integrated circuit as claimed in Claim 95 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.

100. (Currently Amended) The integrated circuit as claimed in Claim 95 wherein each of the power consumptions is further controlled by stopping [[the]] a clock.

101. (Previously Presented) The integrated circuit as claimed in Claim 100 wherein stopping the clock comprises clock gating.

102. (Currently Amended) A system ~~for an integrated circuit, the system~~ comprising:

an integrated circuit;

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

one or more power consumption signals indicating one or more of the power consumptions;

a power management processor coupled to each of the power islands configured to monitor the one or more power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

103. (Previously Presented) The system as claimed in Claim 102 wherein the power management software is embedded firmware.

104. (Previously Presented) The system as claimed in Claim 103 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

105. (Previously Presented) The system circuit as claimed in Claim 103 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

106. (Currently Amended) The system as claimed in Claim 102 wherein each of the power consumptions is further controlled by stopping [[the]] a clock.

107. (Previously Presented) The system as claimed in Claim 106 wherein stopping the clock comprises clock gating.

108. (Previously Presented) The system as claimed in Claim 102 wherein the system is configured to have the supply voltage provided by an external regulator.

109. (Currently Amended) A system ~~for an integrated circuit, the system~~ comprising:

an integrated circuit;

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

one or more power consumption signals indicating one or more of the power consumptions;

a power manager coupled to each of the power islands configured to monitor the one or more power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being

configured to change power consumption in at least one of the power islands in response to a power consumption change request.

110. (Previously Presented) The system as claimed in Claim 109 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.

111. (Previously Presented) The system as claimed in Claim 110 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

112. (Previously Presented) The system as claimed in Claim 110 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

113. (Previously Presented) The system as claimed in Claim 109 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.

114. (Currently Amended) The system as claimed in Claim 109 wherein each of the power consumptions is further controlled by stopping [[the]] a clock.

115. (Previously Presented) The system as claimed in Claim 114 wherein stopping the clock comprises clock gating.

116. (Previously Presented) The system as claimed in Claim 109 wherein the system is configured to have the supply voltage provided by an external regulator.

117. (Currently Amended) A system ~~for an integrated circuit, the system~~ comprising:

an integrated circuit;

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

a power management processor coupled to each of the power islands configured to monitor the power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

118. (Previously Presented) The system as claimed in Claim 117 wherein the power management software is embedded firmware.

119. (Previously Presented) The system as claimed in Claim 118 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

120. (Previously Presented) The system as claimed in Claim 118 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

121. (Currently Amended) The system as claimed in Claim 117 wherein each of the power consumptions is further controlled by stopping [[the]] a clock.

122. (Previously Presented) The system as claimed in Claim 121 wherein stopping the clock comprises clock gating.

123. (Previously Presented) The system as claimed in Claim 117 wherein the system is configured to have the supply voltage provided by an external regulator.

124. (Currently Amended) A system ~~for an integrated circuit, the system~~ comprising:

an integrated circuit;

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

a power manager coupled to each of the power islands configured to monitor the power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

125. (Previously Presented) The system as claimed in Claim 124 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.

126. (Previously Presented) The system as claimed in Claim 125 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

127. (Previously Presented) The system as claimed in Claim 125 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

128. (Previously Presented) The system as claimed in Claim 124 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.

129. (Currently Amended) The system as claimed in Claim 124 wherein each of the power consumptions is further controlled by stopping [[the]] a clock.

130. (Previously Presented) The system as claimed in Claim 129 wherein stopping the clock comprises clock gating.

131. (Previously Presented) The system as claimed in Claim 124 wherein the system is configured to have the supply voltage provided by an external regulator.

132. (New) The integrated circuit as claimed in Claim 124 wherein each of the power consumption signals includes temperature or power dissipation measurement.

133. (New) The integrated circuit as claimed in Claim 76 wherein the one or more power consumption signals include temperature or power dissipation measurement.

134. (New) The integrated circuit as claimed in Claim 82 wherein the one or more power consumption signals include temperature or power dissipation measurement.

135. (New) The integrated circuit as claimed in Claim 89 wherein each of the power consumption signals includes temperature or power dissipation measurement.

136. (New) The integrated circuit as claimed in Claim 95 wherein each of the power consumption signals includes temperature or power dissipation measurement.

137. (New) The system as claimed in Claim 102 wherein the one or more power consumption signals include temperature or power dissipation measurement.

138. (New) The system as claimed in Claim 109 wherein the one or more power consumption signals include temperature or power dissipation measurement.

139. (New) The system as claimed in Claim 117 wherein each of the power consumption signals includes temperature or power dissipation measurement.

REMARKS

The specification and claims have been amended to address the objections presented at pages 2 and 3 of the Office Action. Note that the objection to the second of each pair of claims referenced by the Examiner is believed to be overcome by the amendment to the first. Thus for example, Claim 80 is amended to recite "stopping a clock" and Claim 81 finds antecedent basis for "stopping the clock" in Claim 80 from which it depends.

Without acquiescing to the double patenting rejection, but to expedite issuance, a Terminal Disclaimer with respect to parent patents 7,051,306 and 7,415,680 is attached.

Applicant notes with appreciation the Examiner's finding that the Claims would be allowable with filing of the Terminal Disclaimer. Although further amendments have been made to the claims, those amendments should not affect allowability.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By /James M. Smith, Reg. No. 28,043/
James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA01742-9133
Date: January 25, 2011

1052477.1

JMS/jmk
January 25, 2011

PATENT APPLICATION
DOCKET NO. 2037.2079-010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2825
Filed:	July 21, 2008	Examiner:	Lin, Sun J.
Confirmation No.:	3003		
For:	Power Managers for an Integrated Circuit		

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or is being facsimile transmitted to the United States Patent and Trademark Office on:

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Date Signature

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Typed or printed name of person signing certificate

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith are an Amendment and Terminal Disclaimer for filing in the above-identified application.

☐ Small entity status of this application under 37 CFR 1.9 and 1.27 has been established by a Small Entity Statement previously submitted.

☐ A Small Entity Statement to establish small entity status under 37 CFR 1.9 and 1.27 is enclosed.

1054404.1

The claims fee has been calculated as shown below:

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDIT. FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDIT. FEE
TOTAL	64	MINUS	* 60	4	X $ 26	$		X $52	$ 208
INDEP	8	MINUS	** 10	0	X $110	$		X $220	$ 0
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM					+ $195	$		+ $390	$ 0
					TOTAL =	$ 0		TOTAL =	$ 208

* not fewer than 20
** not fewer than 3

The Application Size Fee has been calculated as shown below:
(Effective for cases filed on or after December 8, 2004)

Actual Sheets (Including current amendment)	Highest No. of Sheets Paid For (At least 100)	No. of Additional Units Required (Increments of 50 sheets)	SMALL ENTITY Rate	SMALL ENTITY Total Amount Owed	OTHER THAN SMALL ENTITY Rate	OTHER THAN SMALL ENTITY Total Amount Owed	Payment Sufficient for up to
52	100	0	X $135	$[ ]	X $270	$0	100 Sheets

Petition for Extension of Time

☐ Applicant hereby petitions to extend the time to respond to the [ ] dated [ ] for [ ] month(s) from [ ] to [ ]. The appropriate fee is set forth below.

☐ *[For action-specific language in an extension of time, select the appropriate option from the Firm Templates]*

Please charge Deposit Account No. 08-0380 for the following fees:

☐	Petition for [ ] month Extension of Time	$	
☒	Claims Fee	$	208
☐	Application Size Fee	$	
☒	Other Fees:		
	Terminal Disclaimer	$	140
		$	
	TOTAL:	$	348

A check is enclosed in payment of the following fees:

☐	Petition for [ ] month Extension of Time	$	
☐	Claims Fee	$	
☐	Application Size Fee	$	
☐	Other Fees:		
		$	
		$	
	TOTAL:	$	

☒ Please charge any deficiency or credit any overpayment in the fees that may be due in this matter to Deposit Account No. 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By /James M. Smith, Reg. No. 28,043/
James M. Smith
Registration No.: 28,043
Telephone (978) 341-0036
Facsimile (978) 341-0136

Concord, Massachusetts 01742-9133
Dated: January 25, 2011

1054404.1

Electronic Patent Application Fee Transmittal	
Application Number:	12176645
Filing Date:	21-Jul-2008
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Filer:	James M. Smith/Jill Kane
Attorney Docket Number:	2037.2079-010
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1202	4	52	208
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Statutory or terminal disclaimer	1814	1	140	140
		Total in USD ($)		**348**

Electronic Acknowledgement Receipt	
EFS ID:	9307303
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	21005
Filer:	James M. Smith/Jill Kane
Filer Authorized By:	James M. Smith
Attorney Docket Number:	2037.2079-010
Receipt Date:	26-JAN-2011
Filing Date:	21-JUL-2008
Time Stamp:	12:09:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$348
RAM confirmation Number	10544
Deposit Account	080380
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Terminal Disclaimer Filed	20372079010_TD.pdf	50619 3515456043a84cd2e9b6cdd919aed9bde91d0097	no	1
Warnings:					
Information:					
2		20372079010_Amendment.pdf	84928 338b3d00a7909cfb5a3b48e4dc7e75a3914f3d7d	yes	13

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Specification	2	2
	Claims	3	12
	Applicant Arguments/Remarks Made in an Amendment	13	13

Warnings:					
Information:					
3	Transmittal Letter	20372079010_Transmittal.pdf	101112 4d89bec8f6586c7565c7d623fcdd47f91738d2e7	no	3
Warnings:					
Information:					
4	Fee Worksheet (PTO-875)	fee-info.pdf	32140 4ac96834c893dfbc677c74257b609e0315a561e1	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	268799		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DOCKET NO. 2037.2079-010

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A PRIOR PATENTS

In re Application of: Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell

Application No. 12/176,645

Filed: July 21, 2008

Confirmation No.: 3003

For: Power Managers for an Integrated Circuit

The owner, MOSAID Technologies Incorporated of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. 154 and 173, as presently shortened by any terminal disclaimer, of prior Patent Nos. 7,051,306 and 7,415,680. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the prior patent, as presently shortened by any terminal disclaimer, in the event that the prior patent later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims cancelled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

The terminal disclaimer fee under 37 CFR 1.20(d) is enclosed.

The undersigned is an attorney or agent of record.

January 25, 2011
Date

/James M. Smith, Reg. No. 28,043/
James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

1052655.1

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/176,645	07/21/2008	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	01/26/2011	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 64	Minus	** 60	= 4	X $ =		OR	X $52=	208
	Independent (37 CFR 1.16(h))	* 8	Minus	***10	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	208

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DEBORAH SCOTT/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **January 5, 2011** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry A. Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

U.S. PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
	A4	5,996,084	11-30-1999	Watts
	A5	6,307,281 B1	10-23-2001	Houston

Copies of issued U.S. Patents and Published U.S. Applications are not required and are not being provided. We are not listing separately any prior U.S. Patent Office communications regarding the cited documents because the Examiner has access to any such actions through PAIR.

EXAMINER	DATE CONSIDERED

Supp LOR (Jan 2011)

1048916.1

Electronic Patent Application Fee Transmittal	
Application Number:	12176645
Filing Date:	21-Jul-2008
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Filer:	James M. Smith/Jill Kane
Attorney Docket Number:	2037.2079-010
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt	
EFS ID:	9168170
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	21005
Filer:	James M. Smith/Jill Kane
Filer Authorized By:	James M. Smith
Attorney Docket Number:	2037.2079-010
Receipt Date:	05-JAN-2011
Filing Date:	21-JUL-2008
Time Stamp:	16:25:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	2850
Deposit Account	080380
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Transmittal Letter	20372079010_SIDS.pdf	74081 a1232ae6b4ff287498b2d99d35f7bfb008810c40	no	3
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Filed (SB/08)	20372079010_LOR.pdf	64597 746d840e976cdb2701eb6032e636828ea58c193d	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Fee Worksheet (PTO-875)	fee-info.pdf	30580 42a7d12559e5d4889d64d5f9bba1f93016c18139	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	169258		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2825
Filed:	July 21, 2008	Examiner:	Lin, Sun J.
Confirmation No.:	3003		
For:	Power Managers For An Integrated Circuit		

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or is being facsimile transmitted to the United States Patent and Trademark Office on:

_____ _____
Date Signature

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Typed or printed name of person signing certificate

TRANSMITTAL LETTER FOR SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Information Disclosure Statement is submitted:

☐ under 37 CFR 1.97(b), or
(Within any one of the following time periods: three months of filing national application (other than a CPA) or date of entry of the national stage in an international application; or before the mailing date of a first office action on the merits; or before the mailing of a first office action after the filing of a Request for Continued Examination).

☒ under 37 CFR 1.97(c) together with either:
- ☐ a Statement under 37 CFR 1.97(e), as checked below, or
- ☒ a $180.00 fee under 37 CFR 1.17(p), or
(After the 37 CFR 1.97(b) time period, but before any of a final action, notice of allowance, or an action that closes prosecution, whichever occurs first)

☐ under 37 CFR 1.97(d) together with:
- ☐ a Statement under 37 CFR 1.97(e), as checked below, and
- ☐ a $180.00 fee under 37 CFR 1.17(p), or
(Filed after final action, notice of allowance, whichever occurs first, or if prosecution otherwise closes, but on or before payment of the issue fee)

☐ under 37 CFR 1.97(i):
Applicant requests that the IDS and cited reference(s) be placed in the application file.
(Filed after payment of issue fee)

Statement Under 37 CFR 1.97(e)

☐ Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement; or

☐ No item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

Statement Under 37 CFR 1.704(d) (Patent Term Adjustment)
Applies to original applications (other than design) filed on or after May 29, 2000

☐ Each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in § 1.56(c) more than thirty days prior to the filing of the Information Disclosure Statement.

☒ Enclosed herewith is a Listing of References. Copies of the cited references are enclosed except as indicated below or in the attached Listing of References.

☐ Copies of the cited references submitted with an Information Disclosure Statement in prior application, U.S. Application No. [ ], to which priority under 35 U.S.C. 120 is claimed, are not required under 37 CFR 1.98(d)(1) and (2) and are thus not provided.

☐ The listed references were cited in the enclosed Search Report in counterpart foreign application [add application number], which is listed in the attached Listing of References.

☐ The "concise explanation" requirement (non-English references) for reference(s) [ ] under 37 CFR 1.98(a)(3) is satisfied by:

- ☐ the explanation provided on the attached sheet.
- ☐ the explanation provided in the Specification.
- ☐ submission of the enclosed International Search Report.
- ☐ submission of the enclosed English-language version of a foreign Search Report and/or foreign Office Action.
- ☐ the enclosed English language abstract.

Method of payment:

☐ Authorization is NOT granted to charge any fees which may be due in this matter to our Deposit Account.

☒ Please charge Deposit Account 08-0380 in the amount of $180.

☐ A check for the fee noted above is enclosed, or the fee has been included in the check with the accompanying Reply.

☒ Please charge any deficiency in fees and credit any overpayment to Deposit Account 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By /James M. Smith, Reg. No. 28,043/

James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Dated: January 5, 2011

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/176,645	07/21/2008	Barry Alan HOBERMAN	2037.2079-010	3003

21005 7590 12/23/2010

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
12/23/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/176,645	HOBERMAN ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/21/2008, 06/14/2010 and 10/07/2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *76-131* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *76-131* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/16/08,8/18/08,7/21/09,7/28/09,12/24/09,2/3/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to two *Preliminary Amendments* filed on *6/14/2010* & *10/07/2010* regarding application 12/176,645 filed on *07/21/2008*. Claims 1 – 75 have been cancelled. Claims 76 – 131 are newly added. Claims 76 – 131 remain pending in the application.

Specification Objections

2. The specification is objected to because of following informalities:

Page 1, Paragraph 0001, line 4 – 5, update status of *issue day* (i.e., 08/19/2008) and *U.S. Patent number* (i.e., 7,415,680).
Page 1, Paragraph 0003, line 5, change "heafdissipation" to **—heat dissipation—**.

Appropriate corrections are required.

Claim Objections

3. Claims listed below are objected to because of the following informalities:

Claim 80, line 2, change "the clock" to —a clock—.
Claim 81, line 1, change "stopping the clock" to —the stopping a clock—.
Claim 87, line 2, change "the clock" to —a clock—.
Claim 88, line 1, change "stopping the clock" to —the stopping a clock—.
Claim 93, line 2, change "the clock" to —a clock—.
Claim 94, line 1, change "stopping the clock" to —the stopping a clock—.
Claim 100, line 2, change "the clock" to —a clock—.
Claim 101, line 1, change "stopping the clock" to —the stopping a clock—.
Claim 106, line 2, change "the clock" to —a clock—.
Claim 107, line 1, change "stopping the clock" to —the stopping a clock—.
Claim 114, line 2, change "the clock" to —a clock—.
Claim 115, line 1, change "stopping the clock" to —the stopping a clock—.
Claim 121, line 2, change "the clock" to —a clock—.
Claim 122, line 1, change "stopping the clock" to —the stopping a clock—.
Claim 129, line 2, change "the clock" to —a clock—.

Claim 130, line 1, change “stopping the clock” to —the stopping a clock—.

Appropriate corrections are required.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 76 – 131 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims of U.S. Patent No. 7,051,306 B2 and U.S. Patent No. 7,415,680 B2. Although the conflicting claims are not word-to-word identical, they are not patentably distinct from each other because they have similar limitations: *an integrated circuit comprising and/or a system comprising a plurality of power islands, power consumption of each power island controlled by changing a supply voltage and operating frequency, power manager(i.e., power management processor), clock gating etc.*

Examiner's Remarks

6. Based on results of preliminary prior art searches, Claims 76 – 131 contain allowable subject matters. Claims 76 – 131 will be allowed pending on a timely filed *terminal disclaimer* in compliance with 37 CFR 1.321(c) to overcome the double patenting rejection as explained in the "***Double Patenting***" given above.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Sun James Lin* whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Jack Chiang* can be reached on (571) 272 - 7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (in USA or CANADA) or 571-272-1000.

All responses to this Office Action should be mailed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 or faxed to 571-273-8300.

/Sun J Lin/
Primary Examiner, Art Unit 2825

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BIB DATA SHEET

CONFIRMATION NO. 3003

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/176,645	07/21/2008	~~257~~ 716	2825	2037.2079-010

APPLICANTS

Barry Alan HOBERMAN, Cupertino, CA;
Daniel L. HILLMAN, San Jose, CA;
Jon SHIELL, San Jose, CA;

**** CONTINUING DATA ************************** YES /JSL/

This application is a CON of 11/336,097 01/20/2006 PAT 7,415,680
which is a CON of 10/840,893 05/07/2004 PAT 7,051,306
which claims benefit of 60/468,742 05/07/2003

**** FOREIGN APPLICATIONS ************************** NONE /JSL/

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
07/29/2008

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☑ No	/SUN J LIN/ Examiner's Signature	☐ Initials	CA	13	~~26~~ 56	8

ADDRESS

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133
UNITED STATES

TITLE

POWER MANAGERS FOR AN INTEGRATED CIRCUIT

FILING FEE RECEIVED		
4512	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
12176645	12176645	HOBERMAN ET AL.
	Examiner	Art Unit
	Sun J Lin	2825

SEARCHED			
Class	Subclass	Date	Examiner
716	100,126,127,132,133	12/8/10	/JSL/

SEARCH NOTES		
Search Notes	Date	Examiner
EAST [US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB]	12/8/10	/JSL/

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

Substitute for form 1449B/PTO **INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **July 15, 2009** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER ~~Not Yet Assigned~~ Lin, Sun J.	CONFIRMATION NO. 3003	GROUP ~~2811~~ 2825

Examiner's Initials	Ref. No.	**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent Pages, Etc.)*
/JSL/	C1	Nowka, *et al.*, "A 0.9V to 1.95V Dynamic Voltage-Scalable and Frequency-Scalable 32b PowerPC Processor," *IEEE International Solid-State Circuits Conference 20.4* (February 6, 2002).
	C2	
	C3	
	C4	
	C5	
	C6	
	C7	
	C8	
	C9	
	C10	
	C11	
	C12	
	C13	
	C14	
	C15	
	C16	
	C17	
	C18	
	C19	
	C20	

EXAMINER	DATE CONSIDERED
/Sun J. Lin/	10/25/2010

906517_1

PTO/SB/08a (03-08)
Approved for use through 05/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	12176645
Filing Date	2008-07-21
First Named Inventor	Barry HOBERMAN
Art Unit	2825
Examiner Name	Lin, Sun J.
Attorney Docket Number	50908.36.P13US04

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6462976		2002-10-08	OLEJNICZAK et al.	
	2	6631502		2003-10-07	BUFFET et al.	
	3	6667648		2003-12-23	STOUT et al.	
	4	6779163		2004-08-17	BEDNAR et al.	
	5	6820240		2004-11-16	BEDNAR et al.	
	6	6598148		2003-07-22	MOORE et al.	
	7	7279956		2007-10-09	CAPLAN et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12176645
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	1							☐

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	"Solving the Power Management Dilemma in System-On-Chip ASIC Design," April 2002, IBM Technology Group.	☐
	2	LACKEY et al., "Managing Power and Performance for System-on-Chip Designs using Voltage Islands," IEEE International Conference on Computer Aided Design, Technical Paper, Nov. 2002, pp. 195 - 202.	☐
	3	SEMERARO et al., "Dynamic Frequency and Voltage Control for Multiple Clock Domain Microarchitecture," 35th Annual IEEE/ACM International Symposium on Microarchitecture, Proceedings, Nov. 2002, pp. 356 - 367.	☐
	4	AKUI et al., "Dynamic Voltage and Frequency Management for Low-Power Embedded Microprocessor," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, Feb. 2004, vol. 1, pp. 64-513.	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JSL/

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	Attorney Docket Number	50908.36.P13US04

	5	TALPES et al., "Toward a Multiple Clock/Voltage Island Design Style for Power-Aware Processors," IEEE Transactions on Very Large Scale Integration (VLSI) system, May 2005, pp. 591-603, v. 13, iss. 5.	☐
	6	GUPTA, R. et al., "Low Power Wireless Networked System Design," HotChips, Aug. 18, 2002, Stanford, CA.	☐
	7	TSAI, Y-F et al., "Implications of Technology Scaling on Leakage Reduction Techniques," DAC 2003, Jun. 2-6, 2003, ACM, Anaheim, CA, USA.	☐
	8	LI, L. et al., "Managing Leakage Energy in Cache Hierarchies," Journal of Instruction-Level Parallelism, 2003, pp. 1-24, vol. 5.	☐
	9	HU, J. S. et al., "Using Dynamic Branch Behavior for Power-Efficient Instruction Fetch," Proc. of IEEECS Annual Symposium on VLSI ((ISVLSI 2003), Feb. 20-21, 2003, Tampa, FL.	☐
	10	ZHANG, W. et al., "Compiler Support for Reducing Leakage Energy Consumption," Proceedings of the 6th Design Automation and Test in Europe Conference (DATE-03), Mar. 2003, Munich, Germany.	☐
	11	DEGALAHAL, V. et al., "Analyzing Soft Errors in Leakage Optimized SRAM Design," Proceedings of the 16th International Conference on VLSI Design, Jan. 2003, New Delhi, India.	☐
	12	LI, L. et al., "Leakage Energy Management in Cache Hierarchies," 11th International Conference on Parallel Architectures and Compilation Techniques (PACT '02), Sep. 2002.	☐
	13	DUARTE, D. et al., "Impact of Scaling on the Effectiveness of Dynamic Power Reduction Schemes," Proceedings of the 20th International Conference on Computer Design (ICCD), Sep. 16-18, 2002, Frieberg, Germany.	☐
	14	DUARTE, D. et al., "Impact of Technology Scaling and Packaging on Dynamic Voltage Scaling Techniques," Proceedings of the 15th Annual IEEE International ASIC/SOC Conference, Sep. 25-28, 2002, Rochester, NY.	☐
	15	KIM, S. et al., "Predictive Precharging for Bitline Leakage Energy Reduction," Proceedings of 15th Annual IEEE International ASIC/SOC Conference, Sep. 25-28, 2002, Rochester, NY.	☐

EFS Web 2.1.1

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	16	RAMANARAYANAN, R. et al., "Characterizing Dynamic and Leakage Power Behavior in Flip Flops," Proceedings of the 15th Annual IEEE International ASIC/SOC Conference, Sep. 2002.	☐
	17	CHEN, G. et al., "Adaptive Garbage Collection for Battery-Operated Environments," Proceedings of USENIX JVM02 Symposium, Aug. 2002.	☐
	18	CHEN, G. et al., "Energy Savings Through Compression in Embedded JavaEnvironments," Proceedings of the CODES 02, Jun. 2002.	☐
	19	DE LA LUZ, V. et al., "Hardware and Software Techniques for Controlling DRAM Power Modes," IEEE Transaction on Computers, Nov. 2001, vol. 50.	☐
	20	DE LA LUZ, V. et al., "Scheduler-Based DRAM Energy Management," DAC 2002, Jun. 10-14, 2002, New Orleans, LA USA, ACM.	☐
	21	KIM, S. et al., "Partitioned Instruction Cache Architecture for Energy Efficiency," ACM Transactions on Computational Logic, Jul. 2002, pp 1-23, vol. V, No. N.	☐
	22	DE LA LUZ, V. et al., "Automatic Data Migration for Reducing Energy Consumption in Multi-Bank Memory Systems," DAC 2002, Jun. 10-14, 2002, New Orleans, LA, USA.	☐
	23	DUARTE, D. et al., "Impact of Technology Scaling in the Clock System Power," Proceedings of the IEEE Computer Society Annual Symposium on VLSI, Apr. 25-26, 2002, Pittsburgh, PA.	☐
	24	DUARTE, D. et al., "A Complete Phase-Locked Loop Power Consumption Model," Proceedings of the 2002 Design, Automation and Test in Europe Conference and Exhibition (DATE '02), 2002, IEEE.	☐
	25	DUARTE, D. et al., "Evaluating Run-Time Techniques for Leakage Power Reduction," Proceedings of the 15th International Conference on VLSI Design (VLSID '02) 2002, IEEE.	☐
	26	ZHANG, W., "Exploiting VLIW Schedule Slacks for Dynamic and Leakage Energy Reduction," Proceedings of the 34th Anual International Symposium on Microarchitecture (MICRO '01), Dec. 2001.	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JSL/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2008-07-21
	First Named Inventor	Barry HOBERMAN
	Art Unit	2825
	Examiner Name	Lin, Sun J.
	Attorney Docket Number	50908.36.P13US04

	27	KIM, S. et al., "Energy Efficient Instruction Cache Using Page-Based Placement," Proceedings of International Conference on Compilers, Architectures and Synthesis for Embedded Systems, CASES '01, Nov. 1-17, 2001, Atlanta, GA, USA.	☐
	28	HEZAVEI, J. et al., "Input Sensitive High-Level Power Analysis," Proceedings of the 2001 IEEE Workshop on Signal Processing Systems (SiPS), Sep. 2001, pp. 149-156.	☐
	29	KIM, S. et al. "Power-Aware Partitioned Cache Architectures," Proceedings of ACM/IEEE International Symposium on Low Power Electronics and Design, 2001, ILSPED '01, Aug 6-7, 2001, Huntington Beach, CA.	☐
	30	DE LA LUZ, V., "DRAM Energy Management Using Software and Hardware Directed Power Mode Control," Proceedings of the 7th International Symposium on High Performance Computer Architecture, Jan. 20-24, 2001, Monterrey, Mexico.	☐
	31	DE MICHELI, G. et al., "System-Level Power Optimization: Techniques and Tools ," DATE 2000.	☐
	32	MANNE, S. et al., "Cool Chips Tutorial," 32nd Annual International Symposium on Microarchitecture, Nov. 15, 1999, Haifa, Israel.	☐
	33	FILSETH, E., "Tally Power into Cost of 'Free' Silicon," EETimes, Jan. 11, 1999, located at http://www.eetimes.com/story/speakout/OEG19990111S028.	☐
	34	FRENKIL, J., "A Multi-Level Approach to Low-Power IC Design," IEEE Spectrum, Feb. 1998, Vol. 35, No. 2.	☐
	35	"Managing Power in Ultra Deep Submicron ASIC/IC Design," May 2002, Synopsys, Inc.	☐
	36	PANGRLE, B. "Low-Power Design: A Holistic Approach in an Era of New Semiconductor Technologies," San Diego Telecom Council Semiconductor SIG, Nov. 14, 2002.	☐
	37	RABAEY, J., "Design Aids for Low Power: Part II Architecture and System Levels," 1997.	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /JSL/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	12176645
	Filing Date	2008-07-21
	First Named Inventor	Barry HOBERMAN
	Art Unit	2825
	Examiner Name	Lin, Sun J.
	Attorney Docket Number	50908.36.P13US04

	38	GRUNWALD, D. et al., "Kool Chips Workshop," MICRO33, Dec. 10, 2000, Monterey, CA.	☐
	39	FLYNN, J. et al., "Power Management in Complex SoC Design," Synopsys, Apr. 2004, located at http://www.synopsis.com/sps.	☐
	40	HALTER et al., "A Gate-Level Leakage Power Reduction Method for Ultra-Low-Power CMOS Circuits," in Proc. IEEE Custom Integrated Circuits Conf., 1997, pp. 475-478.	☐
	41	HORIGUCHI et al., "Switched-Source-Impedance CMOS Circuit for Low Standby Subthreshold Current Giga-Scale LSI's," IEEE Journal of Solid-State Circuits, Nov. 1993, vol. 28, No. 11.	☐
	42	KAO et al., "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits," IEEE Journal of Solid-State Circuits, Jul. 2000, vol. 35, No. 7.	☐
	43	MUTOH, "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS," IEEE Journal of Solid-State Circuits, Aug. 1995, vol. 35, NO. 8.	☐

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EXAMINER SIGNATURE

Examiner Signature	/Sun J. Lin/	Date Considered	10/25/2010

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **December 23, 2009** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER ~~Not Yet Assigned~~ Lin, Sun J.	CONFIRMATION NO. 3003	GROUP ~~2811~~ 2825

U.S. PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
/JSL/	A2	7,111,178 B2	09-19-2006	Rusu, et al.

We are not listing separately any prior U.S. Patent Office communications regarding the cited application(s) because the Examiner has access to any such actions through PAIR.

EXAMINER	DATE CONSIDERED
/Sun J. Lin/	10/25/2010

PTO/SB/08a (03-08)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	12176645
Filing Date	2008-07-21
First Named Inventor	Barry HOBERMAN
Art Unit	2825
Examiner Name	Lin, Sun J.
Attorney Docket Number	50908.36.P13US04

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/JSL/	1	20080088358		2008-04-17	CAPLAN et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2008-07-21
	First Named Inventor	Barry HOBERMAN
	Art Unit	2825
	Examiner Name	Lin, Sun J.
	Attorney Docket Number	50908.36.P13US04

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

FILED ON 07/28/2009

Substitute for form 1449B/PTO **INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **July 28, 2009** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER ~~Not Yet Assigned~~ Lin, Sun J.	CONFIRMATION NO. 3003	GROUP ~~2811~~ 2825

U.S. PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
/JSL/	A1	5,778,237	07-07-1998	Yamamoto, et al.
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Substitute for form 1449B/PTO **INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **July 28, 2009** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER ~~Not Yet Assigned~~ Lin, Sun J.	CONFIRMATION NO. 3003	GROUP ~~2811~~ 2825

Examiner's Initials	Ref. No.	**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent Pages, Etc.)*
/JSL/	C2	Nowka, et al., "A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling," *IEEE Journal of Solid-State Circuits,* Vol. 37, No. 11, pp. 1441-1447 (November 2002).
/JSL/	C3	Nowka, et al., "The Design and Application of the PowerPC 405LP Energy-Efficient System-on-a-Chip," *IBM J. Res. & Dev.,* Vol. 47. No. 5/6, pp. 631-639 (September/November 2003).
/JSL/	C4	Semeraro, et al., "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling," *Proceedings of the Eighth International Symposium on High-Performance Computer Architecture* (2002).
	C5	
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EXAMINER	DATE CONSIDERED
/Sun J. Lin/	10/25/2010

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FILED ON 02/03/2010

Substitute for form 1449B/PTO **INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **February 3, 2010** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER ~~Not Yet Assigned~~ Lin, Sun J.	CONFIRMATION NO. 3003	GROUP ~~2811~~ 2825

FOREIGN PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Country Code-Number-Kind Code (if known)	DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT	TRANSLATION YES	TRANSLATION NO
/JSL/	B1	JP 2003-108260	04-11-2003	Hitachi Ltd.	X	
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EXAMINER	DATE CONSIDERED
/Sun J. Lin/	10/25/2010

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
12176645	12176645	HOBERMAN ET AL.
	Examiner	Art Unit
	Sun J Lin	2825

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☒ CPA ☐ T.D. ☐ R.1.47

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12176645	12176645	HOBERMAN ET AL.
	Examiner	Art Unit
	Sun J Lin	2825

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☐ Claims renumbered in the same order as presented by applicant ☒ CPA ☐ T.D. ☐ R.1.47

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	Examiner	Art Unit
	Sun J Lin	2825

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
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☐ Claims renumbered in the same order as presented by applicant ☒ CPA ☐ T.D. ☐ R.1.47

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
12176645	12176645	HOBERMAN ET AL.
	Examiner	Art Unit
	Sun J Lin	2825

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☒ CPA ☐ T.D. ☐ R.1.47

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EAST Search History

EAST Search History (Prior Art)

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S1	6	716/100	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:14
S2	6	716/126	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:14
S3	2	716/127	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:15
S4	1	716/132	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:15
S5	2	716/133	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/08 12:15

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EAST Search History (Interference)

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Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **December 22, 2010** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

U.S. PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
	A3	6,523,150 B1	02-18-2003	Buffet, et al.
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EXAMINER	DATE CONSIDERED

1045377.1

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **December 22, 2010** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

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Examiner's Initials	Ref. No.	DOCUMENT NUMBER Country Code-Number-Kind Code (if known)	DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
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EXAMINER	DATE CONSIDERED

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **December 22, 2010** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Lin, Sun J.	CONFIRMATION NO. 3003	GROUP 2825

Examiner's Initials	Ref. No.	**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent Pages, Etc.)*
	C5	Search Report: ROC (Taiwan) Patent Application No. 093112998 (Translation), completed October 31, 2010.
	C6	
	C7	
	C8	
	C9	
	C10	
	C11	
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EXAMINER	DATE CONSIDERED

Design method of semiconductor chip

Publication number: CN1353454 (A)
Publication date: 2002-06-12
Inventor(s): KOHN J M [US]; DIANE A A [US]; HASAWE D J [US] +
Applicant(s): IBM [US] +
Classification:
- international: *G06F17/50; H01L21/82;* G06F17/50; H01L21/70; (IPC1-7): H01L21/70; H01L27/00
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Application number: CN20011038538 20011115
Priority number(s): US20000713629 20001115

Also published as:
CN100419999 (C)
EP1207470 (A2)
EP1207470 (A3)
US6792582 (B1)
TW231436 (B)
more >>

Abstract not available for CN 1353454 (A)
Abstract of corresponding document: **EP 1207470 (A2)**

Both logical and physical construction of voltage islands is disclosed. A semiconductor chip design is partitioned into "bins", which are areas of the design. In this way, a semiconductor chip design may be "sliced" into various areas and the areas may then be assigned to various voltage levels. Each bin may be thought of as a voltage island. Circuits in the design can be added to or removed from the various bins, thereby increasing or decreasing the speed and power of the circuits: the speed and power increase if a circuit is placed into a bin assigned a higher voltage, and the speed and power decrease if a circuit is placed into a bin having a lower voltage. The size and location of the bins may also be changed. By iterating these steps, the optimum power consumption may be met while still meeting speed constraints and other criteria.; The present invention is applicable to any placement environment, such as an annealing placement tool, that proceeds through successive refinement of the locations of the circuits on the design and in which the placement process may be interrupted to make changes in placement of the logic.

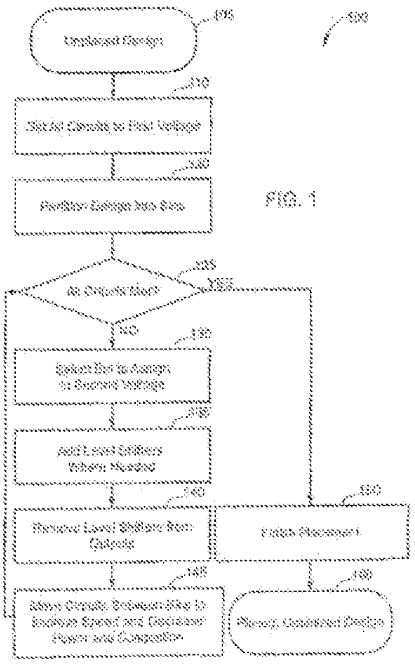


FIG. 1

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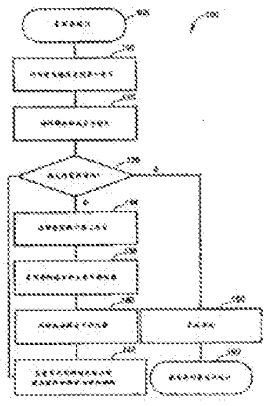
代理人 黄小临 王志森

权利要求书7页 说明书18页 附图页数12页

[54]发明名称 半导体芯片设计方法

[57]摘要

公开了电压岛的逻辑和物理构形。半导体芯片结构被分割成作为设计区域的仓室。半导体芯片结构可被切割成各个区域,并被赋予各种电压电平。每个仓室可看作电压岛。设计中的电路被加到各个仓室中或从中移出,由此提高或降低电路的速率和功率;如电路置于被赋予较高电压的仓室,则速率和功率提高,如放到具有较低电压的仓室,则降低速率和功率。也可以改变仓室的尺寸和位置。通过重复这些步骤,可满足最佳功耗,同时满足速率限制和其它标准。本发明可适用于诸如退火布局工具之类的任何布局环境,它是通过在设计上连续精细调整电路位置而进行的,并且该布局处理可被中断以改变逻辑布局。



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权 利 要 求 书

1、一种用于进行半导体芯片设计的方法，其特征在于，包括以下步骤：

给一组电路赋予多个电压电平的第一电压电平；

将该组电路分割成多个仓室；

给仓室之一赋予多个电压电平的第二电压电平；和

给一个仓室内的电路赋予第二电压电平。

2、如权利要求 1 的方法，其特征在于，第二电压电平高于第一电压电平。

3、如权利要求 1 的方法，其特征在于，第二电压电平低于第一电压电平。

4、如权利要求 2 的方法，其特征在于，给仓室之一赋予多个电压电平的第二电压电平的步骤包括在该组电路中确定最坏松弛路径的步骤和分配具有在最坏松弛路径中的至少一个电路的仓室作为所述一个仓室的步骤。

5、如权利要求 2 的方法，其特征在于，给仓室之一赋予多个电压电平的第二电压电平的步骤包括分配具有预定数量的低转换电路的仓室作为所述一个仓室的步骤。

6、如权利要求 3 的方法，其特征在于，给仓室之一赋予多个电压电平的第二电压电平的步骤包括分配具有预定数量的高转换电路的仓室作为所述一个仓室的步骤。

7、如权利要求 1 的方法，其特征在于，给仓室之一赋予多个电压电平的第二电压电平的步骤包括分配随机仓室作为所述一个仓室的步骤。

8、如权利要求 2 的方法，其特征在于，给仓室之一赋予多个电压电平的第二电压电平的步骤包括确定很多延迟路径会聚的位置的步骤和分配具有该位置的仓室作为所述一个仓室的步骤。

9、如权利要求 2 的方法，其特征在于，给仓室之一赋予多个电压电平的第二电压电平的步骤包括以下步骤：确定多个关键路径；如果每个仓室中的电路被赋予第二电压，则确定具有在关键路径中的电路的每个仓室的延迟改进量；如果这个仓室中的电路被赋予第二电压电平，则确定有最大延迟改进的仓室为关键路径的至少一个仓室，和分配这个仓室作为所述一个仓室。

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10、如权利要求 1 的方法，其特征在于，给仓室之一赋予多个电压电平的第二电压电平的步骤包括确定具有直接给锁存电路供电的预定量输入端的仓室和分配该仓室作为所述一个仓室的步骤。

11、如权利要求 1 的方法，其特征在于，还包括以下步骤：

重复以下步骤，直到满足预定标准为止：

给附加仓室赋予第二电压电平；

给附加仓室内的电路赋予第二电压电平；和

在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路。

12、如权利要求 11 的方法，其特征在于在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路的步骤包括从被赋予第二电压电平的仓室移动至少一个电路到被赋予第一电压电平的仓室的步骤。

13、如权利要求 11 的方法，其特征在于在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路的步骤包括将至少一个电路从被赋予第二电压电平的仓室移动到被赋予第一电压电平的仓室的步骤。

14、如权利要求 11 的方法，其特征在于预定标准包括在性能限制基础上使功率最小化。

15、如权利要求 11 的方法，其特征在于预定标准包括在功率限制基础上使性能最大化。

16、如权利要求 1 的方法，其特征在于，给一个仓室内的电路赋予第二电压电平的步骤包括将电平移位器添加到该一个仓室内的一个电路的输入端的步骤，并且该输入端穿过将所述一个仓室与被赋予第一电压电平的相邻仓室分隔开的边界。

17、如权利要求 12 的方法，其特征在于第二电压电平大于第一电压电平，其中将至少一个电路从被赋予第二电压电平的仓室移动到被赋予第一电压电平的仓室的步骤包括将至少一个高转换电路从第二电压电平移动到第一电压电平的步骤，并且它如果处于非关键路径中，则只移动至少一个高转换电路。

18、如权利要求 11 的方法，其特征在于在被赋予第二电压电平的仓室

和被赋予第一电压电平的仓室之间移动至少一个电路的步骤包括在最小化电平移位器的标准基础上选择至少一个电路的步骤。

19、如权利要求 11 的方法，其特征在于在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路的步骤使得被赋予第二电压电平的第一仓室满足预定最小尺寸。

20、如权利要求 19 的方法，其特征在于第二电压电平高于第一电压电平，并且在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路的步骤还包括将至少一个低转换电路从被赋予第一电压电平的周围仓室移动到第一仓室的步骤。

21、如权利要求 19 的方法，其特征在于第二电压电平高于第一电压电平，并且在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路的步骤还包括将至少一个周围电路移动到第一仓室的步骤，其中所述至少一个周围电路处于被赋予第一电压电平的周围仓室中并由第一仓室中的关键路径供电。

22、如权利要求 19 的方法，其特征在于在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路的步骤包括在最小化电平移位器的基础上选择至少一个电路的步骤。

23、如权利要求 11 的方法，其特征在于在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路的步骤包括缓冲至少一个电路的步骤。

24、如权利要求 11 的方法，其特征在于在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路的步骤包括克隆至少一个电路的步骤。

25、一种用于进行半导体芯片设计的方法，其特征在于，该方法包括以下步骤：

给一组电路赋予多个电压电平的第一电压电平；

从该组电路中选择一籽晶电路；

给该籽晶电路赋予多个电压电平的第二电压电平；和

在该籽晶电路周围建立第二电压岛。

26、如权利要求 25 的方法，其特征在于第二电压电平高于第一电压电平。

27、如权利要求 25 的方法，其特征在于第二电压电平低于第一电压电平。

28、如权利要求 25 的方法，其特征在于，还包括在被赋予第一电压电平的该组电路的某些电路周围建立第一电压岛的步骤和在第一电压岛和第二电压岛之间移动至少一个电路以使满足预定标准的步骤。

29、如权利要求 28 的方法，其特征在于为满足预定标准而在第一电压岛和第二电压岛之间移动至少一个电路的步骤包括缓冲该至少一个电路的步骤。

30、如权利要求 28 的方法，其特征在于为满足预定标准而在第一电压岛和第二电压岛之间移动至少一个电路的步骤包括克隆该至少一个电路的步骤。

31、如权利要求 28 的方法，其特征在于第二电压高于第一电压，并且所述至少一个电路是非关键的高转换电路，所述至少一个电路从第二电压岛移动到第一电压岛。

32、如权利要求 28 的方法，其特征在于预定标准包括在性能限制下的最小化功率。

33、如权利要求 28 的方法，其特征在于预定标准包括在功率限制下的最大化性能。

34、如权利要求 28 的方法，其特征在于所述至少一个电路从第一电压岛移动到第二电压岛中，第二电压高于第一电压，并且所述至少一个电路是关键电路。

35、如权利要求 28 的方法，其特征在于，还包括重复以下步骤直到满足预定标准为止的步骤：从一组电路中选择一籽晶电路；给该籽晶电路赋予多个电压电平的第二电压电平；在籽晶电路周围建立第二电压岛；和在第一电压岛和第二电压岛之间移动至少一个电路以使满足预定标准。

36、如权利要求 35 的方法，其特征在于选择与被赋予第二电压电平的现有电压岛相邻的一个籽晶电路，在所述一个籽晶电路周围建立附加电压岛，并且该附加电压岛和现有电压岛合并构成更大的电压岛。

37、如权利要求 35 的方法，其特征在于重复步骤使一个第二电压岛下降到最小容量以下。

38、如权利要求 37 的方法，其特征在于第二电压高于第一电压，并且

该方法还包括将一相邻关键电路移到所述一个电压岛中的步骤。

39、如权利要求 37 的方法，其特征在于第二电压高于第一电压，并且该方法还包括将相邻低转换电路移到所述一个电压岛中的步骤。

40、一种程序产品，其特征在于，包括：

(A)包含集成电路设计工具的计算机程序，该集成电路设计工具给一组电路赋予多个电压电平的第一电压电平，将该组电路分割成多个仓室，给仓室之一赋予多个电压电平的第二电压电平，和给所述一个仓室内的电路赋予第二电压电平；

(B)承载计算机程序的信号承载介质。

41、如权利要求 40 的程序产品，其特征在于信号承载介质包括可记录介质。

42、如权利要求 40 的程序产品，其特征在于信号承载介质包括传输介质。

43、如权利要求 40 的程序产品，其特征在于第二电压电平高于第一电压电平。

44、如权利要求 40 的程序产品，其特征在于第二电压电平低于第一电压电平。

45、如权利要求 43 的程序产品，其特征在于通过在该组电路中确定最坏松弛路径和分配在最坏松弛路径中有至少一个电路的仓室作为所述一个仓室，集成电路设计工具给一个仓室赋予多个电压电平的第二电压电平。

46、如权利要求 43 的程序产品，其特征在于通过分配有预定数量低转换电路的仓室作为所述一个仓室，集成电路设计工具给仓室之一赋予多个电压电平的第二电压电平。

47、如权利要求 44 的程序产品，其特征在于通过分配有预定数量高转换电路的仓室作为所述一个仓室，集成电路设计工具给仓室之一赋予多个电压电平的第二电压电平。

48、如权利要求 40 的程序产品，其特征在于通过分配随机仓室作为所述一个仓室，集成电路设计工具给仓室之一赋予多个电压电平的第二电压电平。

49、如权利要求 43 的程序产品，其特征在于通过确定多个延迟路径会聚的位置和分配具有该位置的仓室作为所述一个仓室，集成电路设计工具

给仓室之一赋予多个电压电平的第二电压电平。

50、如权利要求 43 的程序产品，其特征在于通过确定多个关键路径；如果每个仓室中的电路被赋予第二电压，则确定用于在关键路径中的具有电路的每个仓室的延迟改进量；如果这个仓室中的电路被赋予第二电压电平，则确定有最大延迟改进的仓室为关键路径的至少一个仓室；和分配这个仓室作为所述一个仓室，而使集成电路设计工具给仓室之一赋予多个电压电平的第二电压电平。

51、如权利要求 40 的程序产品，其特征在于通过确定有直接馈送锁存电路的预定数量输入端的仓室和分配该仓室作为所述一个仓室而使集成电路设计工具给仓室之一赋予多个电压电平的第二电压电平。

52、如权利要求 40 的程序产品，其特征在于集成电路设计工具给附加仓室赋予第二电压电平，给附加仓室内的电路赋予第二电压电平，并且在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路，直到满足预定标准为止。

53、如权利要求 52 的程序产品，其特征在于通过从被赋予第二电压电平的仓室移动至少一个电路到被赋予第一电压电平的仓室，集成电路设计工具在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路。

54、如权利要求 52 的程序产品，其特征在于通过从被赋予第二电压电平的仓室移动至少一个电路到被赋予第一电压电平的仓室，集成电路设计工具在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路。

55、如权利要求 52 的程序产品，其特征在于预定标准包括在性能限制下最小化功率。

56、如权利要求 52 的程序产品，其特征在于预定标准包括在功率限制下最大化性能。

57、如权利要求 52 的程序产品，其特征在于通过在最小化电平移位器的标准基础上选择至少一个电路，集成电路设计工具在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路。

58、如权利要求 52 的程序产品，其特征在于集成电路设计工具在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电

路，使被赋予第二电压电平的第一仓室满足预定最小尺寸。

59、如权利要求 58 的程序产品，其特征在于第二电压电平高于第一电压电平，还通过将至少一个低转换电路从被赋予第一电压电平的周围仓室移到第一仓室中，集成电路设计工具在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路。

60、如权利要求 58 的程序产品，其特征在于第二电压电平高于第一电压电平，还通过将至少一个周围电路移到第一仓室中，集成电路设计工具在被赋予第二电压电平的仓室和被赋予第一电压电平的仓室之间移动至少一个电路，所述至少一个周围电路处于被赋予第一电压电平的周围仓室中，并且由第一仓室中的关键路径供电。

61、如权利要求 58 的程序产品，其特征在于集成电路设计工具在被赋予第二电压电平的一仓室和被赋予第一电压电平的一仓室之间移动至少一个电路包括根据最小化电平移位器的标准选择至少一个电路的步骤。

说　明　书

半导体芯片设计方法

技术领域

本发明一般涉及在半导体芯片上的计算机辅助电路布局(placement)，具体地涉及用于混合电源电压结构（design）的电压岛(voltage island)的并行逻辑和物理结构。

背景技术

数字电路的转换功率随着电源电压的平方增加而增加。这样，为减小电路功耗要求减小该电压。然而，减小电源电压也会降低电路性能。因此，要求在同一芯片上合并由较高电源电压驱动的电路和由较低电源电压驱动的电路(以下分别称为高和低压电路)。在需要实现所需电路性能的地方使用高压电路，在别处使用低压电路。

当高和低压电路通过这种方式合并在一个半导体芯片上时，要求将低压电路一起物理组合到低压岛，和分开地将高压电路一起组合到高压岛。这是优选的方案，因为高和低压电源分布在独立的分配网络上，并且通过将电路分组成岛，只有两个电源中之一需要分布在每个岛内。这就减小了为分配两个电源所要求的额外的布线资源的量，由此留下更多布线资源用于信号布线。主要优点是，这容许半导体芯片更小和/或需要更少的布线平面。

当高和低压电路合并在一个芯片上时，必须注意驱动从一个类型的电路到另一个类型电路的信号的网络(net)。通常，高压电路可直接驱动低压电路而无须特别插入电路，但是馈送高压电路的低压电路必须通过特定电平移位电路来驱动它们。这种电路增加了网络的面积、功率和延迟。因此，需要使它们的使用最小化。在很多种电路中，高压锁存电路可以用做电平移位器而不需要增加成本。因此，如果选择低压电路以使它们直接馈送给锁存电路，则可减少所需电平移位器的数量。通常是通过将紧密连接的电路组赋予高或低电压来减少所需电平移位器的数量。

总之，通常将高压电路放在高压岛上和将低压电路放在低压岛上可减

少使用的电平移位器的数量。这也减少了高和低压电源必须经历的位置数量，由此减少了功率分配成本。然而，这些岛对好的逻辑布局并无好处。例如，信号必须运行很长的距离才能到达高压岛，然后从高压岛返回使用该信号的电路。这实际上降低了性能而不是提高了性能。这样，应该是很好的布局却变成了很差的布局。

构成高和低压电路的另一种方法是逻辑簇集(logical clustering)。在逻辑簇集中，高和低压电路不被设计在以连通性为基础的电压岛中。将电路中要求较快的元件变为较高电压，而较慢的、非关键(non-critical)元件变为较低电压。这就解决了由高和低压岛簇集引起的布局的问题，而数据的路径没有移动。然而，必须到处分配不同的电源和逻辑簇集会大大增加电平移位器的数量。

这样，就需要限制电源路线和电平移位器的数量，并容许关键(critical)数据路径来满足定时要求。

发明内容

通过提供电压岛的逻辑和物理结构，本发明的优选实施例解决了这些问题。本发明的优选实施例合并了物理和逻辑合成以提供较少的电平移位器和较少的电源路线，但是仍然满足定时和其它要求。此外，通过对电压岛结构使用重复处理(iterative process)，使电源使用最小化，同时，特别是满足了速率限制。

在本发明的一个方案中，半导体芯片结构（chip design）被分割成多个仓室(bin)，它们是设计的区域。通过这种方式，半导体芯片结构被切割成各个区域，然后给这些区域加上各种电压电平。每个仓室可以被看作是一个电压岛。可给各个仓室增加设计中的电路或从各仓室去掉这些电路，由此提高或降低电路的速率和功率：如果电路置于被加上较高电压的仓室中，则速率和功率提高，如果电路放置到具有低电压的仓室中，则速率和功率降低。仓室的尺寸和位置也可以改变。通过重复这些步骤，可满足最佳功耗，同时仍然满足速率约束和其它标准。

这样，本发明不是只将电路加到电压岛上，或只确定哪些电路需要较高的电压并将这些电路变为较高电压电平，而是合并这两个原理。本发明使用电压岛的物理和逻辑结构，以便符合预定标准。

将半导体芯片结构分割成大量仓室只是在设计中安置电路的一种方法。本发明可适用于任何布局环境，即通过连续精心改进设计中的电路位置和为了改变逻辑布局而中断布局工艺来适应任何布局环境。

从下面结合附图对本发明优选实施例的更详细的说明使本发明的前述和其它特点更明显。

附图说明

图 1 是根据本发明的最佳实施例提供电压岛的逻辑和物理结构的最佳方法；

图 2 是在仓室之间移动电路以提高速率及降低功率和拥挤的最佳方法；

图 3 至图 7 是根据图 1 的方法在布局的各个阶段中的逻辑电路的例子；

图 8 和图 9 是在一示意布局上由本发明的最佳实施例实现的功率降低步骤的例子；

图 10 和图 11 是根据本发明的第二最佳方法的流程图；和

图 12 是本发明的计算机系统的框图。

具体实施方式

如上所述，本发明涉及在半导体芯片上的计算机辅助电路布局。对于不熟悉这个主题的人员来说，下面的概要部分将简要介绍与布局工艺相关的某些概念。在半导体芯片上的计算机辅助电路布局领域内的技术人员希望直接进行详细介绍。

综述

在设计半导体芯片时，使用计算机设计工具。这些工具工作并产生称为网表(netlist)的文件。这个网表包含所有门和它们之间的连接的说明。半导体芯片设计者通常用芯片的模拟逻辑布图工作。换句话说，半导体芯片将执行某个功能，设计者确保模拟芯片实际逻辑地执行该功能。当准备制作实际芯片时设计者使用采用原始网表并产生输出的布局工具。将网表、定时限制、布局限制和转换信息给予布局工具。此外，还可以将描述布线和门的定时及包含布局规则、门的尺寸和形状等的程序库给予布局工具。布局工具输出修改的网表和布局信息。然后把它们输送给布线工具，产生

用于在半导体晶片上实际产生芯片的掩模和其它信息。

有几种不同类型的布局系统。一个重要的系统被称为布局驱动合成或PDS。对于 PDS 的参考文献是《用于 Power PC 微处理器的定时关闭的集成布局和合成方法》(An Integrated Placement and Synthesis Approach for Timing Closure of the POWER PC Microprocessor), S. Hojat and D.Villarrubia, pages 206-210, International Conference on Computer Design, 1997, 这里引入供参考。PDS 系统容许在布局过程中对要制作的网络作逻辑改变。PDS 包括以切割为基础的布局程序和在切割之间进行的一系列操作。以切割为基础的布局程序将循环分割芯片区域和芯片上的电路。通常，首先将芯片分割成两部分(虽然将芯片分成四部分的四分法也是公知的)，然后将每半个部分各再分割成两部分等等。开始并不知道芯片上的这些电路最终位置，但在每次切割之后就会精细调整该电路位置。

在布局工艺中的任何点将芯片分割成的区域称为仓室。在 PDS 中，在系列布局切割之间进行各种逻辑合成行为(通常是修改网表的任何程序)，容许在目前可得到的电路布局的精细调整基础上对网络进行修改。典型的行为包括缓冲、克隆(复制电路并在原始电路和复制品之间分配其扇出)、分解、管脚交换等。有时候，也可以在仓室之间移动电路。

布局工具和方法的另一个例子是模拟退火安置器(placer)。这种布局工具是按照晶体的物理退火推论工作的，对布局做了很多试验性改变。这些试验性改变可以保留或放弃，这取决于布局的质量因素(例如被评价的布线拥挤情况)的某种量度的改进和有助于控制退火工艺的可变温度。该工艺在高温下开始，并随着布局进行而持续到低温。总是保留改进该量度的变化，同时也有可能保留劣化该量度的变化，这种保留的可能性将随着温度降低和布局量度劣化量的增加而降低。随着布局的进行，电路在可接受的布局改变内移动的平均距离减少。这样，芯片上的电路位置逐步更好确定。

详细说明

本发明的优选实施例合并了物理和逻辑合成以提供更少的电平移位器和更少的功率路线，但是仍然满足定时和其它要求。此外，使用重复工艺用于构成电压岛，可使功率使用最小化同时仍可满足速率限制。

在本发明的一个方案中，半导体芯片结构被分割成仓室，它们是设计区域。通过这种方式，半导体芯片结构可以被切割为各种区域，然后给这

些区域赋予各种电压电平。每个仓室可以被看作是一个电压岛。设计中的电路可以从各个仓室中去掉或加到各个仓室中，由此提高或降低电路的速率和功率：如果电路放置到被赋予较高电压的仓室，则速率和功率提高，如果电路被放置到具有较低电压的仓室，则速率和功率降低。仓室的尺寸和位置也可以改变。通过重复这些步骤，可满足最佳功耗，同时仍然满足速率限制和其它标准。

这样，只将电路加到电压岛上，或者只确定哪个电路需要较高电压和将这些电路变到更高电压电平，本发明组合了这两种概念。本发明使用电压岛的物理和逻辑结构以满足预定的标准。

将半导体芯片结构分割成多个仓室只是设计中安置电路的一种方式。本发明适用于任何布局环境，这种布局环境是通过在设计上连续精细调整电路位置而进行并且其中可以中断布局工艺以便改变逻辑布局。

在更详细地介绍最佳实施例之前，讨论一下术语是有利的。作为这里使用的，仓室是半导体芯片结构的一个区域。不必给每个仓室赋予特定电压。电压岛也是设计区域，但给它赋予特定电压。电压岛中的所有电路将由赋于电压岛的特定电压供电。

可使用任何布局系统进行这里所述的物理和逻辑合成。通常，这种布局系统将给一部分芯片结构上的一组电路赋予特定电压电平，选择芯片结构的区域，并且给该区域内的电路赋予不同电压电平。在较高和较低(或者中间)电压电平之间发生电路移动，以使设计最佳化。在本发明的最佳实施例中，芯片结构被分割成仓室。每个仓室将是电压岛并被赋予给特定电压。一些仓室将被赋予较高电压，一些仓室被赋予较低电压。这样进行物理合成。在这些物理约束中，电路从较高电压区域移动到较低电压区域，或者反之，以便满足功率、速率、和其它标准。这样也进行了逻辑合成。在本发明的其它实施例中，使用退火布局系统。在这个方案中，电压岛将被赋予特定位置，并且不使用仓室。物理和逻辑合成仍然进行。

现在参见图 12，图 12 表示本发明的计算机系统的方框图。本领域技术人员都清楚，本发明的机构和装置同样适用于任何计算机系统，无论该计算机系统是否是复杂的多用户计算设备或单用户工作站。如图 12 的部件分解图所示，计算机系统 1100 包括与主存储器 1120 连接的主或中心处理单元(CPU)1110，大容量存储器接口 1130，终端接口 1140，和网络接口 1150。

B2

这些系统部件通过使用系统总线 1160 互连。大容量存储器接口 1130 用于将大容量存储器件(如 DASD 器件 1155)连接到计算机系统 1100。一种特殊类型的 DASD 器件是软盘驱动器，可在软盘 1195 中储存数据和读取数据。

主存储器 1120 包含有一个或多个应用程序 1122、电路元件 1124、数据 1126 和操作系统 1128。计算机系统 1100 采用公知虚拟寻址机构，这种虚拟寻址机构容许计算机系统 1100 的程序只对大的、单个存储实体进行存取，而不对多个、小的存储机构如主存储器 1120 和 DASD 器件 1155 进行存取。因此，在所示应用程序 1122、电路元件 1124、数据 1126、和操作系统 1128 保存在主存储器 1120 中时，本领域技术人员将了解到这些部分不必同时全部包含在主存储器 1120 中。(还应当注意，这里使用的术语计算机系统存储器一般指计算机系统 100 的整个虚拟存储器。)

操作系统 1128 是任何合适的操作系统。本领域技术人员都清楚本发明的精神和范围不限于任何一种操作系统。保存在主存储器 1120 中的是由 CPU1110 执行的一个或多个应用程序 1122。这些应用程序之一是根据本发明的集成电路设计工具 1134。包含在主存储器 1120 中的还有被设计工具 1134 使用的电路元件 1124 的表达式(例如电和定时参数)。尽管所示的集成电路设计工具 1134 和电路元件 1124 驻留在主存储器 1120 中，它们可以存在于计算机 1100 的虚拟存储空间的任何位置。另外，在所示电路元件 1124 与设计工具 1134 分开时，这些电路元件 1124 还可提供作为集成电路设计工具 1134 的一个组成部分。如下面更详细的描述，集成电路设计工具 1134 最好是进行电路元件 1124 的布局驱动合成(PDS)的设计工具。如综述部分所述，PDS 将芯片结构分割成相对小的称为仓室的区域。在这个最佳实施例中，仓室被用做电压岛，并且使用标准来确定何时该设计已经适当安置。

虽然所示的计算机系统 1100 只包含单个主 CPU 和单个系统总线，但本领域技术人员都清楚可使用有多个 CPU 和/或多条总线的计算机系统来实现本发明。此外，用在优选实施例中使用的接口各包括用于从 CPU1110 卸载强化计算处理的分开的、全编程微处理器。然而，本领域技术人员都清楚本发明同样适用于简单使用 I/O 适配器以执行同样的功能的计算机系统。

终端接口 1140 用于将一个或多个终端 1165 直接连接到计算机系统 1100。可以是非智能的或全编程工作站的这些终端 1165 用来容许系统管理人员和用户与计算机系统 1100 通信。

网络接口 1150 将其它计算机系统和/或工作站(即图 1 中的 1175 和 1185)以联网形式连接到计算机系统 1100。无论是否存在网络接口 1150，本发明都适用。对于这里的最佳实施例的目的，存在网络接口 1150，无论这种连接是否是使用目前模拟和/或数字技术或通过将来的某些联网机构实现的，本发明都同样适用，而不管计算机系统 1100 是怎样连接到其它计算机系统和/或工作站的。而且重要的是应当指出计算机系统 1100 中存在网络接口 1150 意味着计算机系统 1100 可与一个或多个其它计算机系统或工作站配合协作处理。当然，这还意味着主存储器 1120 中示出的程序不必都驻留在计算机系统 1100 中。例如，应用程序 1112 的一个或多个程序可驻留于另一个系统上并且与驻留在计算机系统 1100 上的一个或多个程序配合协作处理。这个协作处理可通过使用诸如远程进程调用(RPC)之类的一种公知的客户机－服务器机构来完成。

关于这一点，重要的是应指出已经(并且将继续)在全功能计算机系统方面介绍了本发明，本领域技术人员都清楚本发明能够作为各种形式的程序产品来分销，并且无论是哪种特定类型的信号承载介质实际执行该分配，本发明都同样适用。信号承载介质的例子包括：可记录型介质，如软盘(即图 12 的软盘 1195)和 CD ROM；和传输型介质，如数字和模拟通信链路，包括无线通信链路。

现在回到图 1，图 1 示出了一种使用电压岛的物理和逻辑结构安置电路的方法。方法 100 最好用图 12 中所示的集成电路设计工具 1134 进行。当在电路元件布局过程中用集成电路设计工具 1134 执行时，方法 100 便于电路元件布局，结果导致功率和速率最佳组合并满足其它标准。

当未安置设计 105 给予布局工具时开始执行方法 100。未安置设计由网表描述，它是所有门和门之间的连接的说明。随着未安置设计，也将一组定时限制和/或功率和面积限制给予该工具。而且，在某位置需要某些电路(如输入/输出电路)时，也可能需要某些位置限制。最后，将描述布线和门定时和包含布局规则、门的尺寸和形状等的程序库给予布局工具。

首先，将所有电路设定到特定电压(步骤 110)。最好是，所有电路将设定到低电压，因为这趋于降低整个功率要求。如果电路开始设定到较高电压，则这些电路已经是很高的功率，而布局设计趋于为更高功率。如果使用两种以上的电压，则在该步骤选择最低电压是可取的。如果使用两种(高

和低)电压，则选择低压作为电压岛的起始电压。

在步骤 120，未安置设计被分割成仓室。在方法 100 中，每个仓室和电压岛是等效的。换言之，每个电压岛将是一个仓室。在这个分割(或切割)工艺过程中，将使用正常 PDS 合成行为以尽量满足性能目的，以便通过其他措施而不是建立电压岛来减小功率，并且满足其它设计目的。特别是，PDS 系统此时可以考虑全局路径限制。如果电压岛太小，功率路线的量增加。这可能对系统空间考虑有不利影响。

在步骤 125，进行有关是否满足所有设计标准的判定。正常情况下，设计标准主要是性能和功率的组合。例如，设计标准可以在满足性能限制基础上使功率最小化。对于这些标准，必须满足性能限制，满足性能标准的各种布局设计能导致不同的功耗。判断性能的一种方式是利用松弛(SLACK)。松弛是在信号绝对必须处于一个位置的时间和它实际到达那里的时间之间的时间量。如果存在有一正松弛，则信号在它必须到达之前到达。在其路径中可能有一个或多个电路是较低功率的。另一方面，如果存在有一负松弛，则信号没有准时到达。一般情况下，这意味着将路径中的一个或多个电路改变到较高功率能增加性能。对于在满足性能限制前提下最小化功率的标准，满足这些设计标准意味着满足了所有性能目标(即所有松弛是正的)并且布局设计具有可能设计布局的最低功率。

如果设计标准在满足功率限制前提下是最大化性能，满足这些标准意味着给任何多个仓室赋予高压将引起超出功率限制。

应该注意到功率和性能以外的标准可以在步骤 125 测试。例如，位置对于某些电路是很重要的，如输入/输出电路。在步骤 125 中满足标准将确保这些电路处于合适位置。此外，面积、噪声、可靠性和布线能力是可在步骤 125 中测试的其它标准。

如果满足了设计标准(步骤 125=是)，则在步骤 150 中完成布局。在该步骤中，给 PDS 系统以限制，电路不可以从低压仓室转移到高压仓室，反之亦然。在该步骤期间，输出修改的网表和布局信息。在输出布局信息之前，PDS 系统将在每个仓室中确定每个电路的精确位置，以便产生布局信息。最好是，在前面的步骤中，电路被简单地安置到特定仓室中。在步骤 150 期间，确定仓室内的每个电路的精确 X、Y 位置。一旦输出修改的网表和布局信息，该设计被布局并最佳化(步骤 160)。该设计可以传送给布线工具以

使产生实际制作芯片需要的掩模等。

如果一个或多个标准没有被满足(步骤 125=否)，则在步骤 130 中，PDS 系统给仓室赋予第二电压。所选择的仓室将变为处于第二电压的电压岛。最好是，第二电压比第一电压高。如果使用两种电压，即高和低压，则最好是给一仓室赋予高压。如果使用两种以上的电压，则最好是将次高电压赋予一仓室。例如，如果有三个电压(低、中和高)，则最好是开始给一仓室赋予中间电压。在第二次通过步骤 125 时，如果例如仓室内的电路的松弛仍然是负的，则给同一仓室赋予高压。给仓室赋予增加的电压，从低到高，通常可导致比给仓室赋予降低的电压(从高到低)实现的功率低的功率的布局设计。

在步骤 130，也选择特定仓室作为赋予第二电压的仓室。有很多方法确定哪个仓室被赋予第二电压。当第二电压是较高电压时，一般所选择的仓室将是含有在设计中的最差松弛路径上的电路的仓室。在这种情况下，增加电压将提高电路速率，由此减小或消除松弛。也可以随机选择所选仓室。选择仓室的另一方法(当第二电压是高压时)是选择低转换仓室，它含有不常用的网络或转换相对少次数的电路。因为增加转换等于增加功率，所以现有方法减少了功率。

另外，确定哪个仓室赋予第二电压可以尽量找到很多滞后路径会聚的点。下面文章中介绍了找到这些点的方法，这里引证供参考：K. Usami, et al.，《利用加到媒质处理器的多个电源电压的自动低功率技术》电气电子工程师协会固态电路杂志。(Automated Low-Power Technique Exploiting Multiple Supply Voltages Applied to a Media Processor, Institute of Electrical and Electronics Engineers Journal of Solid-State Circuits,) v. 33, no. 3, 463-472 (March, 1998)；和 L. Berman, et al.，《时间校正的有效技术》电路和系统 1990 国际会议文集(Efficient Techniques for Timing Correction, Proceeding of the 1990 International Symposium on Circuits and Systems) (May 1990)。

此外，所选仓室可以是在关键路径中有大量电路的仓室。对于这个选择，可以选择在关键路径中具有大量电路的仓室作为该仓室。或者，如果仓室包含的电路被赋予第二(较高)电压，可通过确定哪个仓室能使关键路径得到最大延迟改进来进行选择。最后，可通过选择具有直接馈送锁存电

路的大量输入的仓室来进行选择，因为这样的仓室将减少所需电平移位器。

应该注意到在步骤 130 中可选择多个仓室。然而，为简化起见，这里讨论的是只选择一个仓室。而且，在步骤 130，所选仓室和它的电路将被赋予第二电压。给电路赋予第二电压容许 PDS 工具再计算延迟、功耗、松弛和其它数据。然后使用这个信息确定是否满足标准。

在步骤 135，在需要的地方加上电平移位器。如果第二电压是较高电压，则所选仓室将被转换到高压岛。输出信号给高压岛(所选仓室)中的电路的低压电路将具有被加上低压信号的电平移位器。如果第二电压是较低电压，则在高压岛的电路和低压岛的电路之间不需要电平移位器。这是因为通常低压电路需要电平移位器以便给高压电路供电，但高压电路不一定需要电平移位器给低压电路供电。

在步骤 140 中，从不再需要电平移位器的电路输出去掉电平移位器。例如，如果低压电路具有馈送给高压电路的输出信号，则用于低压电路的输出信号将具有在它上的电平移位器。当含有该低压电路的仓室被制成高或更高压岛时，在低压电路的输出上不再需要电平移位器。

在步骤 145 中，电路在仓室之间移动以便提高速率及降低功率和拥挤。电路可以移动到所选仓室以便提高速率(如果所选仓室是较高电压仓室)，提高占用率，或者在相邻仓室中让出位置。电路可以移动到所选仓室以外，以便降低功率(如果所选仓室是较高电压仓室和电路移动到较低电压仓室)，降低拥挤，降低占用率，或者提高周围仓室占用率。

除了图 1 以外现在还参见图 2，图 2 更详细地描绘了步骤 145。本例中的步骤 145 中所选仓室是高或较高电压，并且一些周围仓室是较低电压。在介绍图 2 之后介绍再讨论这种情况和当所选仓室是较低电压和某些周围仓室是较高电压时的相反情况之间的不同。应该注意到即使方法 145 和 100 中的这些步骤是以特定顺序示出的，但这些步骤也可以不必按照这个顺序进行。

在方法 145 的每个步骤或操作之后，可以检测该电路以便观察是否它们违反定时限制、违反任何仓室容量、或违反仓室之间的切割线上的任何拥挤限制。如果是这样，将拒绝操作。可能由于电路移动而改变布线长度引起网络上增加了负载而违反定时限制。如果将过多的电路安置到仓室中，以至于电路和连接布线不能简单地与仓室面积相适应，则可能违反仓室容

量。注意到不同半导体技术可以有对电路的不同面积要求。如果由于过多的数据路径进入一仓室而有过多个布线，则可能违反拥挤限制。如果有太多数据路径进入一仓室，则该仓室将不能布线。在方法 145 中，电路移动也可以包括电路复制以减少对网络长度的影响。

仍参见图 2，当非关键电路从所选仓室移动到较低功率邻接仓室时，开始执行方法 145(步骤 210)。关键路径需要满足某些定时要求而且还趋于是最严格的满足定时要求。PDS 系统进行定时分析，并且从这个分析确定哪些路径是关键的。非关键电路是不在关键路径中的电路。相反，关键电路是在关键路径中的电路。步骤 210 通过将非关键电路移动到较低电源电压岛而减低了功率。如果需要，这些非关键电路的输出端上的电平移位器可移动到它们的输入端。对于该步骤，可以优先选择是给其它较低电压仓室中的电路馈电的源仓室输出的所选仓室中的电路。

另外，在步骤 210 中，可以优先选择被其它低电压仓室中的电路馈电的所选仓室中的电路。为减少所需电平移位器的数量，可以进行最大流量、最小切割程序。描述最大流量、最小切割程序的参考文献是：Graph Algorithms(图形算法)，Shimon Even，ComputerScience Press，1979，在这里引证供参考。在该程序中，流程图由被其它低压仓室中的电路供电的所选高电压仓室上的所有非关键仓室输入系列和所选仓室扇出锥中的非关键电路构成。通过流动网将确定最小切割。通过流动网确定最小切割中网络左面的所有电路。将这些左面的或供电电路移动到相邻低压仓室，将最小化在仓室输入端所需电平移位器的数量。实际上，这个程序试图产生从低电压到高电压的最少信号转换数量和最小化布线长度。该流程图是确定哪些电路应该移动到低电压的一种方式。

步骤 210 也可以优选移动仓室外的高转换电路。高转换电路是转换相对高次数的那些电路。这个相对高的转换量消耗更高的功率。这样，减少功率的一种方法是将高转换电路从高压仓室移出到较低压仓室。注意如果这些电路处于关键路径中，即使它们是高转换电路，这些电路也优选保留在高压仓室中。

在步骤 220 中，如果所选仓室下降到最小容量以下(步骤 220=是)，则由所选仓室中的电路输出供电的低压电路将加到所选仓室中(步骤 240)。可以优先选择通过这种方式移动的电路以便最小化由于这些电路是随着需要

电平移位器的输入端而要求添加的电平移位器数量。这个步骤试图通过给较高电压仓室添加由关键网供电的电路以最快速率保持关键网。这样，当所选仓室尺寸变小时，由关键网供电和处于较低功率仓室中的电路被加到较高功率所选仓室，并且从所选仓室移去非关键电路。或者，这个步骤可以将低转换电路从周围区域加到所选仓室中。这就使功率最小化，而且提高了所选仓室的容量。

如果所选仓室没有下降到最小容量以下(步骤 220=否)，判定是否所有非关键电路已经移出(步骤 225)。如果没有(步骤 225=否)，则该方法处理过程返回到步骤 210。如果所有关键电路已经被移动(步骤 225=是)，则给所选仓室中的关键电路供电的低压仓室中的关键电路被移动到所选仓室中(步骤 230)。这样，如果所选仓室中的关键电路仍然不满足定时限制，则给这些关键电路供电的电路从低功率移动到高功率。这加速了关键路径和提高定时。如果有电平移位器，电平移位器将从新增加电路的输出端移动到新增加电路的输入端。

在步骤 235 中，如果所选仓室下降到最小容量以下，则由所选仓室中的关键电路输出供电的低压电路将加到所选仓室中。步骤 235 与步骤 240 相似。优先选择通过这种方式移动的电路，以便使需要添加的电平移位器的数量最小化。步骤 235 试图通过将由关键网供电的电路加到较高电压仓室，以最快速率保持关键网。这样，当所选仓室尺寸变小时，由关键网供电和处于低压仓室中的电路被加到较高功率的所选仓室，并且从所选仓室移出非关键电路。

此外，在步骤 235，可能需要在相邻仓室中为从所选仓室移出的电路让出空间。为此，由所选仓室中的关键电路的输出供电的低压电路将被加到所选仓室中。再一次，将优先选择通过这方式移动的电路以便最小化要求添加的电平移位器的数量。

在步骤 255 中，确定是否这个仓室满足所有标准。根据用于芯片结构的性能和功率标准，这种标准最基本的是性能和功率标准。此外，可以检测其它标准，如超过容量或低于容量、路线或位置标准等。如果没有满足所有标准(步骤 255=否)，则方法 145 继续进行；如果满足了所有标准(步骤 255=是)，则在步骤 250 结束该方法。应该注意即使可能在步骤 255 之前满足性能和功率标准，方法 145 也可以进行多次以便在满足其它标准的同时

最大程度地减少功率。满足其它标准(特别是性能标准)的最低功率构形是最佳方案。

应注意到方法 145 可含有图 2 中所示的所有步骤或者只含有所示的某些步骤。例如，方法 145 可能只使用了步骤 210。最好是，使用所有步骤，这能以最小功率量提供最大性能。另外，如果方法 145 的任何步骤增加拥挤超出预定程度，电路可在仓室之间移动以便减少拥挤。

如图 2 所示的方法 145 可适用于所选仓室被赋予比相邻仓室高的电压的任何时候。如果所选仓室是低压，而相邻仓室是高压，方法 145 将稍有不同。在该实施例中，在步骤 210 中更有利的是将非关键电路从相邻仓室移动到所选仓室中并将关键电路移出所选仓室。在步骤 240，是非关键的输出电路优先移动到所选仓室中。这与步骤 230 和 235 相同：实际上，来自周围较高功率仓室的非关键电路被移动到较低功率仓室。

方法 100 的步骤 145 之后，再次进行方法 100 的步骤 125。方法 100 继续进行直到满足标准或直到该方法没有会聚为止。通常，后者被置为时间限制：如果该方法超过特定时间，则假定该方法没有会聚到一个解决方案。例如，如果为太高的性能标准选择太低的功率标准，就会这样。

除了图 1 和 2 之外，现在回到图 3-7，图 3-7 表示芯片结构的示意部分。图 3 表示完全未安置芯片结构，这个设计将存在于方法 100 的步骤 105 中。图 4-7 表示方法 100 和 145 的布局工艺的各个阶段中的同一芯片结构。

在图 3 中，示出了完全未安置芯片结构。未安置芯片结构 300 包括各个输入端 310-316 和输出端 320。未安置芯片结构 300 也包括大量电路：几个 NAND(与非)门 331 和 332、逻辑块 340 和 330、若干反相器 350-355、和 NOR(或非)门 360。未安置芯片结构 300 由网表描述。

在图 4 中，示出了部分安置设计 400。图中只示出了某些互连。在方法 100 的步骤 110 和 120 之后示出部分布局设计 400。每个仓室已经设定到低电压，由此产生低电压仓室/岛 410 和 420。边界 430 将两个岛 410 和 420 分离。在步骤 120 中，将使用正常 PDS 合成行为以便满足性能目的，并通过其它方式而不是建立岛来减少功率和满足其它设计目的。结果就产生了图 4 所示的部分布局设计 400。路径 370 是关键路径，网络 440 和 460 穿过边界 430。

在图 5 中，仓室 410 已经被赋予高电压仓室/岛 510。在步骤 125 中，

没有满足所有标准(步骤 125=否)，因此在步骤 130 中选择仓室 510 作为高电压仓室。仓室 520(图 4 中的 420)未被改变并且仍然是低压仓室。仓室 510 中的所有电路被赋予较高电压。选择仓室 510 作为高压仓室，是因为它在这个小设计(方法 100 的步骤 130)中的最坏松弛路径(路径 370)上有最多电路。电平移位器 470、480、和 490 分别加到网络 370、370 和 440 上，以便将这些信号转变到更高电压(步骤 135)。没有给网络 460 和路径 370 添加电平移位器，因为该路径 370 离开反相器 353 并连到反相器 354，因为这些是高压信号。这些信号应该能驱动低压电路。在步骤 140 中，没有去掉电平移位器。

可在这些步骤的任一个之后检测部分安置设计 400，以便确定是否满足功率、性能和其它标准。在仓室或高压岛 510 的情况下，网络相当拥挤：输入端 310-314 非常需要在仓室一侧的一位布线。此外，非关键电路(NAND 门 332)和非关键网络 450、440 和 460 是在高压仓室 510 中。而且，可假设关键路径 370 也没有满足定时要求，意味着松弛是负的。

在下面描述图 2 的方法 145 的步骤顺序过程中应当参照图 5 和 6。因为仓室 510 没有被最佳化，因此在方法 145 的步骤 210 中，输入端 314、电路 332 和网络 460 被移动到低压仓室/岛 520。不再需要电平移位器 490，因此去掉它。在步骤 220 中，所选仓室不低于最小容量，并且在步骤 224 中，已经移动所有低压电路。在步骤 230 中，关键电路 354 和 360 被移动到高压仓室/岛 510。不再需要电平移位器 470，但是增加了电平移位器 610 以便增加来自网络 620 的电压。

在步骤 255 中确定功率和性能标准。在本例中，假设满足功率和性能标准。但是，为了确定通过不同布局是否可产生功率和性能的更好组合，还进行方法 145 以便重复预定次数。除了图 1 和 2 之外，还参见图 6 和 7，在重复方法 145 之后，所得结果是图 7 的安置设计 700。应该注意到关键路径 370 的图 6 的布局在该路径正向产生松弛。因为满足了定时要求，因此在图 7 中路径 370 不再是关键的。然而，应该检测对该路径的任何改变以便确定与定时一致。在步骤 210 中，关键电路 350 从高压仓室/岛 510 移动到低压仓室/岛 520。这样的结果是有最低数量的电平移位器和最低功率，同时仍满足性能标准。在这个重复工艺过程中，关键电路 351、352 等也从仓室 510 移动到仓室 520。然而不满足性能标准。这样，布局设计 700 满足

B2

性能和功率标准。如果功率不作为标准，则电路 350 和或许电路 340 可加到高压仓室 510 上(假设没有违反容量要求)。

步骤 145 之后，在步骤 125-145 中将选择附加仓室并被最优化，直到最优化整个设计为止。在图 7 的简单例子中，仓室 520 可以被赋予高压。这将提供性能改进。然而，功率也提高了。因为被安置设计 700 满足了性能和功率要求，因此步骤 125 将表示满足所有标准。在步骤 150 中结束布局，并输出网表和布局信息。结果布局的、最优化的设计(步骤 160)。

方法 100 和 145 还可包括正常合成操作，如克隆和缓冲，以便进一步减小功率。图 8 和 9 表示在方法 145 过程中进行的克隆操作以便减小功率(通过最小化布线长度和消除电平移位器)。在图 8 中，部分安置设计 1000 包括通过边界 1040 与低压仓室 1030 分离的高压仓室 1020。在边界 1040 上的是两个电平移位器 1055 和 1060。电平移位器 1060 将电压从仓室 1030 的低压转变为仓室 1020 的较高电压，同时电平移位器 1055 倒置。依据所实施的技术，可以不需要电平移位器 1055。对于在图 8 中使用的特定技术，使用电平移位器 1055。路径 1090 是满足图 8 中的定时要求的关键路径。

高压仓室 1020 包括输入端 1010-1013、反相器 1070、1075、1080 和 1085、逻辑块 1050 和输出端 1091。低压仓室 1030 包括输入端 1014-1016、逻辑块 1045、NOR 门 1086 和反相器 1087。当在部分安置设计 1000 上运行方法 145 时，确定布线长度正好为高(特别是网络 1093 和 1094)并可去掉电平移位器 1055。为此，克隆反相器 G1 1070 和反相器 G2 1075，变为反相器 G1 Clone 1097 和反相器 G1 Clone 1096(见图 9)。这就减小了线长，因而该线长现在是网络 1091。另外，因为不需要电平移位器 1055，因此减少了电平移位器的数量。

使用 PDS 或布局驱动合成描述了前面的方法。还有其它布局工具和方法。本发明适用于通过在设计上连续细化电路位置而进行并且可中断布局工艺以便改变逻辑布局的任何布局环境。下面的论述集中在布局工具，并且方法是模拟的退火安置器。如在综述部分所述，这种布局工具是通过用晶体的物理退火模拟操作的，对布局做了很多试验性改变。

现在参见图 10，该图表示使用模拟的退火安置器的用于电压岛的并行逻辑和物理结构的方法 800。因为方法 800 与方法 100 非常相似，因此这里只介绍不同点，同时参见方法 800。在讨论过程中，参见图 1 用于对比是有

利的。

两种方法之间的一个不同点是在方法 800 的步骤 820 中。PDS 系统，如用于方法 100 的 PDS 系统，将芯片结构分成称为仓室的区域。模拟退火布局系统不用仓室。在步骤 820 中，代替分割芯片结构和在芯片上进行合成行为，进行正常退火布局工艺，直到电路移动的平均距离小于最小建议电压岛尺寸为止。这容许在增加电压岛的并行逻辑和物理结构之前完成正常退火布局工艺。

在步骤 830 中，选择一个电路作为籽晶电路。如上所述，最好是开始将所有电路设定为低电压。然后该籽晶电路被赋予高压并在籽晶电路周围产生高压岛。高压岛的尺寸增加或减小取决于岛中的电路数量。作为籽晶电路，可以优选选择靠近现有高压岛的电路。因此，移动物理上与现有高压岛相邻的籽晶电路将增加现有高压岛的尺寸。这样，代替有其中整个仓室所选为电压岛的仓室，方法 800 选择一个电路并在该电路周围产生电压岛。

在步骤 845 中，电路在区域之间(岛之间)移动，以便提高速率和降低功率和拥挤。步骤 845 在图 11 中作为方法 845 被具体公开，并且与图 2 的步骤 230-255 相似。对于步骤 930，给所选岛中的电路供电的低压岛中的关键电路移动到所选岛中。如果需要，可增加岛的尺寸。这样，如果所选岛中的关键电路和路径仍然不满足定时限制，则给这些关键电路供电的电路从低功率移动到高功率。这将加速关键路径和提高定时。如果可能，电平移位器将从新添加的电路的输出端移动到新增加电路的输入端。

在步骤 935 中，如果含有所选籽晶电路的岛下降到低于最小容量，则将所选岛中的关键电路输出供电的低压电路加到所选岛。按照这种方式移动的电路将被优选以便最小化要求的所加电平移位器的数量。步骤 940 试图通过给高压岛添加由关键网络供电的电路而以最快速率保持关键网络。这样，当所选岛尺寸变小时，由关键网络供电和处于低功率岛中的电路被添加给更高功率的所选岛，并且从所选岛移去非关键电路。

此外，在步骤 935 中，需要在相邻岛中为移出所选岛的电路让出位置。为此，由所选岛中的关键电路输出供电的低压电路将加到所选岛上。将优先选择按照这种方式移动的电路以便使所要求的附加的这种电平移位器的数量最小化。

在步骤 955 中，确定是否该岛满足所有标准。根据为芯片结构设定的性能和功率标准，这些标准最基本的是性能和功率标准。另外，可以检查其它标准，如超过容量或低于容量，路线或位置指标等。如果没有满足所有标准(步骤 955=否)，则再次进行方法 845；如果满足了所有标准(步骤 955=是)，则在步骤 950 结束该方法。应该注意到即使在步骤 955 之前满足性能和功率标准，也可以进行多次方法 945，以便最大程度地减小功率，同时仍然满足其它标准。满足其它标准的最低功率构形(特别是，性能标准)是最佳方案。

还应该注意到，如果该岛小于优选容量，步骤 955 可以给该岛添加附加电路。如果步骤 930 和 935 没有给该岛添加足够电路(是因为关键输入锥很小，或因为实现物理相邻要求的电路移动违反了其它限制)，则可选择其它邻近关键电路，它被赋予高电压并移动到该岛中。然后在新加电路的输入和输出端继续步骤 930 和 935。

注意，如参照图 2 的方法 145 所述，可以进行其它工作以便在步骤 845 中满足预定标准。例如，可使用缓冲或克隆以便提高速率，降低功率和/或降低拥挤。作为另外的例子，也可以在步骤 845 中使用下列最优法(参照方法 145 讨论的)：高转换电路可以移出高压岛并进入低压岛以便降低功率；如果电压岛太小，由所选高压岛中的关键路径或网络供电的周围低压岛中的电路可以移动进入高压岛(提高速率)；在最小化电平移位器的基础上，电路可以移动到所选电压岛中。

在图 10 的步骤 850 中，不允许使已经被确定的高压岛变得物理断开的改变。继续完成布局工艺，但是遵守不在高压岛之间产生物理断开的改变的规则。也在该步骤中确定电压岛内的电路的精确 X，Y 位置。

方法 800 和 845 同样适用于为低压岛选择籽晶电路。在这种情况下，给低压岛添加非关键网络和电路，并且关键网络和电路被传送到高压岛。

总之，提供电压岛的逻辑和物理构形的方法适合于各种布局算法。根据该方法，选择电压岛和向该岛添加电路或移出电路，以便最佳分析设计标准。两个基本标准是功率和性能标准。由于逻辑结构保持在岛内和周围岛上，因此产生岛的逻辑构形。因为电路移动到(或移出)物理电压岛，因此产生物理构形。当电路和物理电压布图的逻辑关系合并以便在需要时提高性能和在需要时降低功率时，产生最佳布局。该方法的重复性质可发现

这种组合相对容易。

已经示出的是提供电压岛的逻辑和物理构形的方法。本发明的优选实施例合并物理和逻辑合成以便提供最少的电平移位器和最少功率路线，但是仍然满足定时和其它要求。此外，使用用于电压岛结构的重复工艺，可以最小化功率使用，同时满足特别是速率限制。

这里列举的实施例和例子是为了最好地解释本发明及其实际应用，并由此使本领域技术人员制造和使用本发明。但是，本领域技术人员将认识到前面的说明和例子只是示意的和举例而已。前面的说明不是穷举的或将本发明限制到所公开的精确形式。同样，除非特殊说明，附图中或说明书中示出的方法的任何步骤顺序是作为可能的顺序例子给出的，不作为限制。鉴于上述教导，在不脱离所附权利要求书的精神和范围的情况下可以作出很多修改和改变。

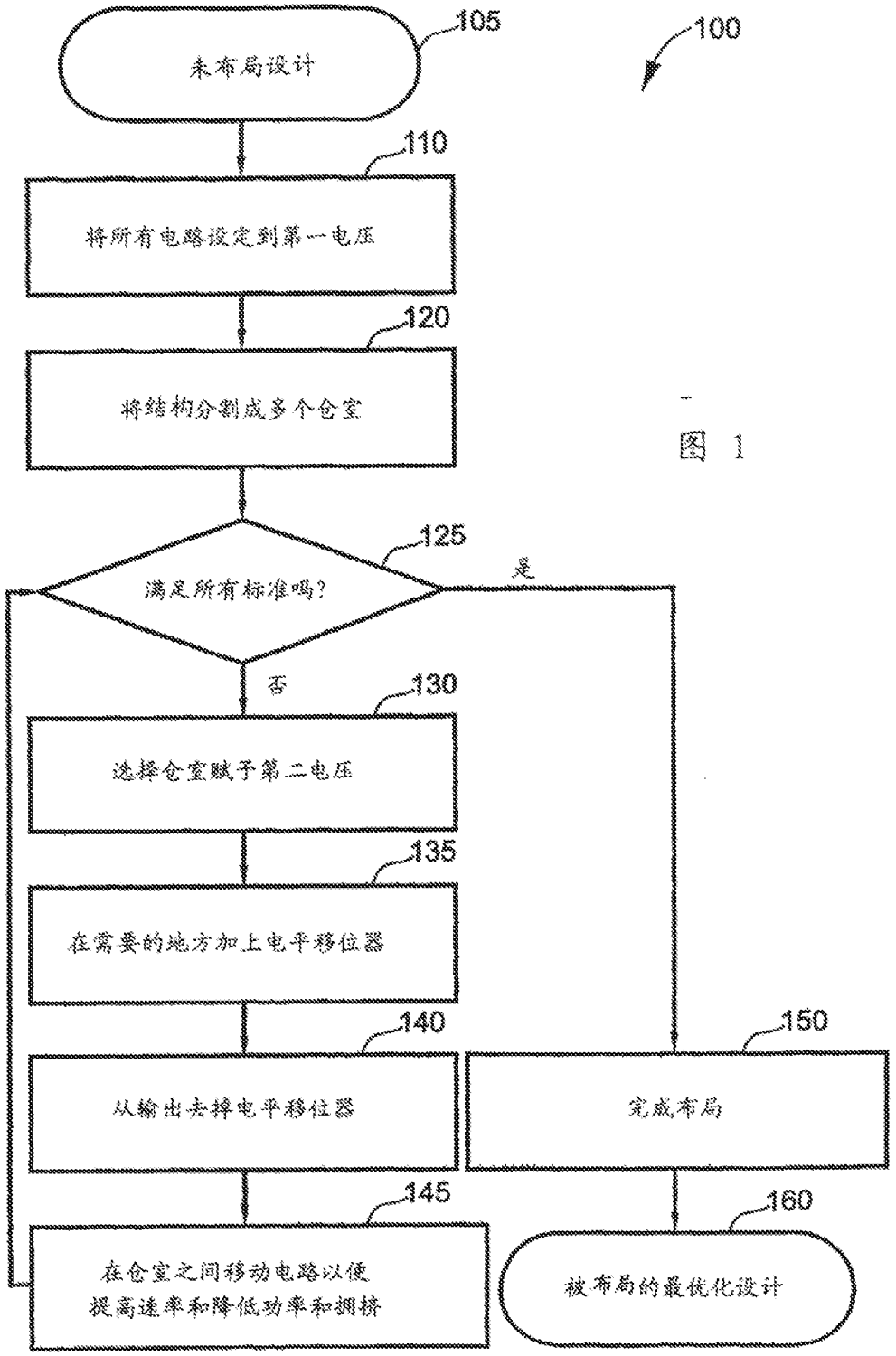

105
未布局设计
100
110
将所有电路设定到第一电压
120
将结构分割成多个仓室
125
满足所有标准吗?
是
否
130
选择仓室赋予第二电压
135
在需要的地方加上电平移位器
140
从输出去掉电平移位器
150
完成布局
145
在仓室之间移动电路以使
提高速率和降低功率和拥挤
160
被布局的最优化设计

图 1

B2

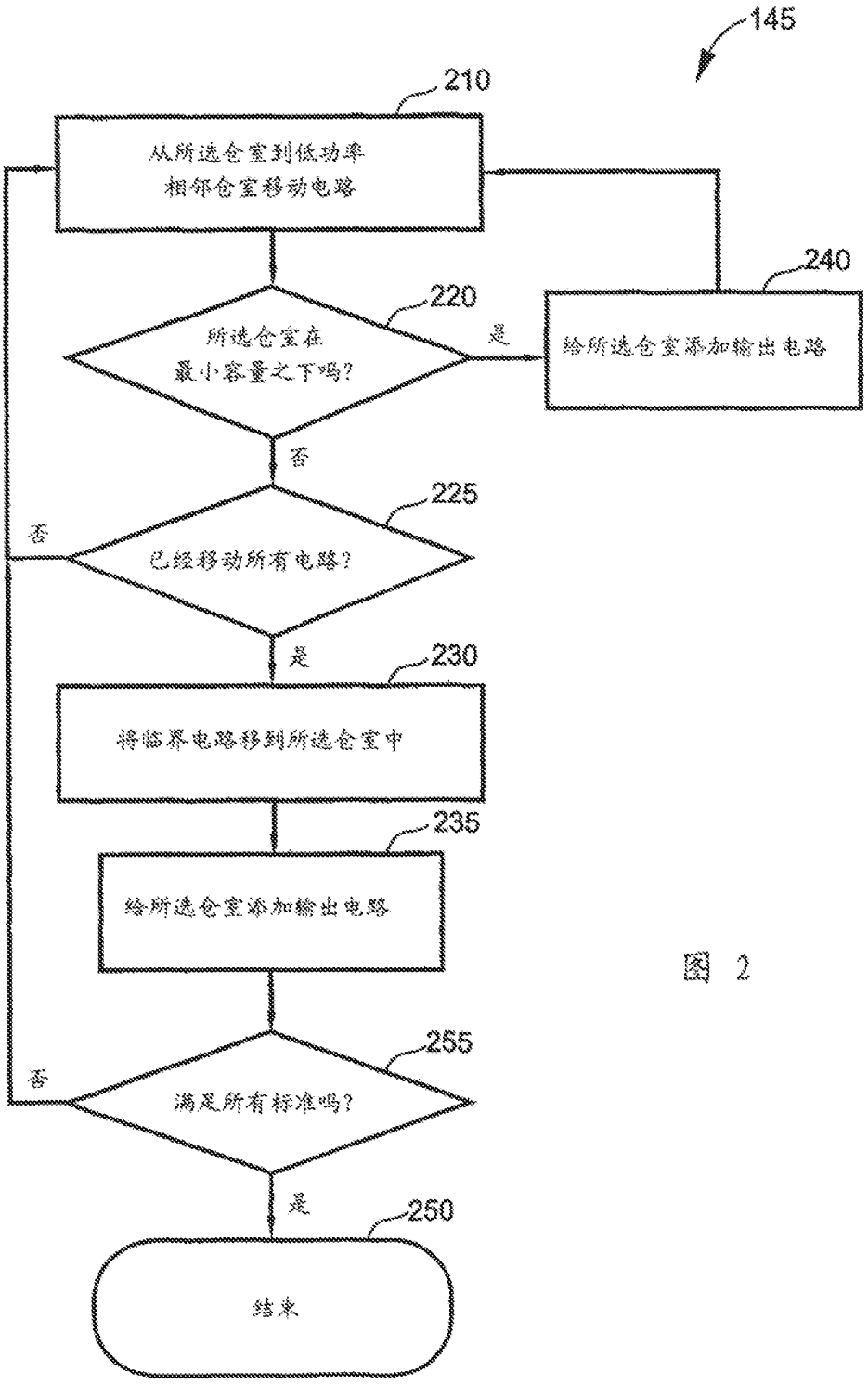

145
210
从所选仓室到低功率
相邻仓室移动电路
220
所选仓室在
最小容量之下吗?
是
240
给所选仓室添加输出电路
否
225
已经移动所有电路?
否
是
230
将临界电路移到所选仓室中
235
给所选仓室添加输出电路
255
满足所有标准吗?
否
是
250
结束

图 2

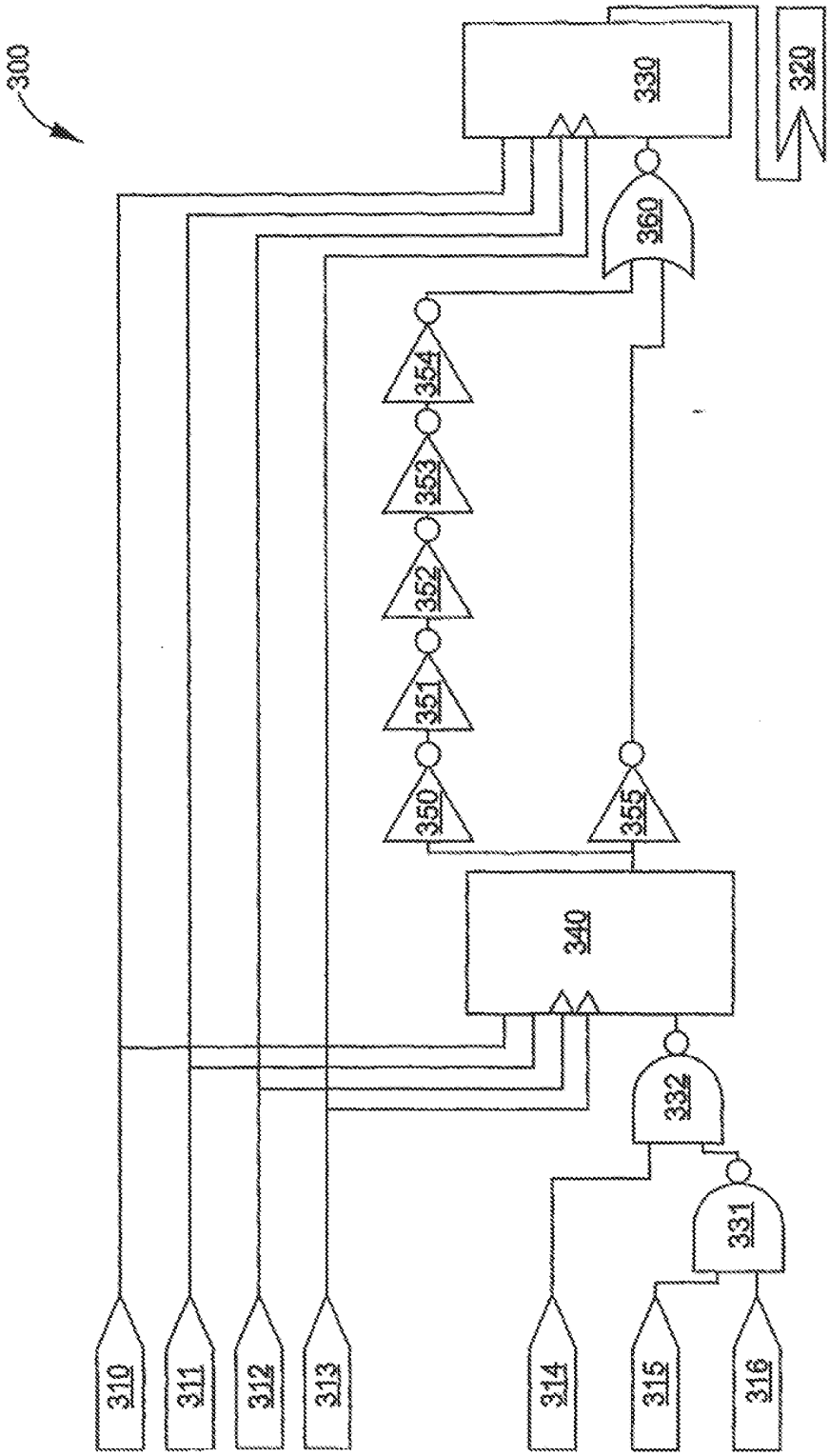

300
310
311
312
313
314
315
316
320
330
331
332
340
350
351
352
353
354
355
360

图 3

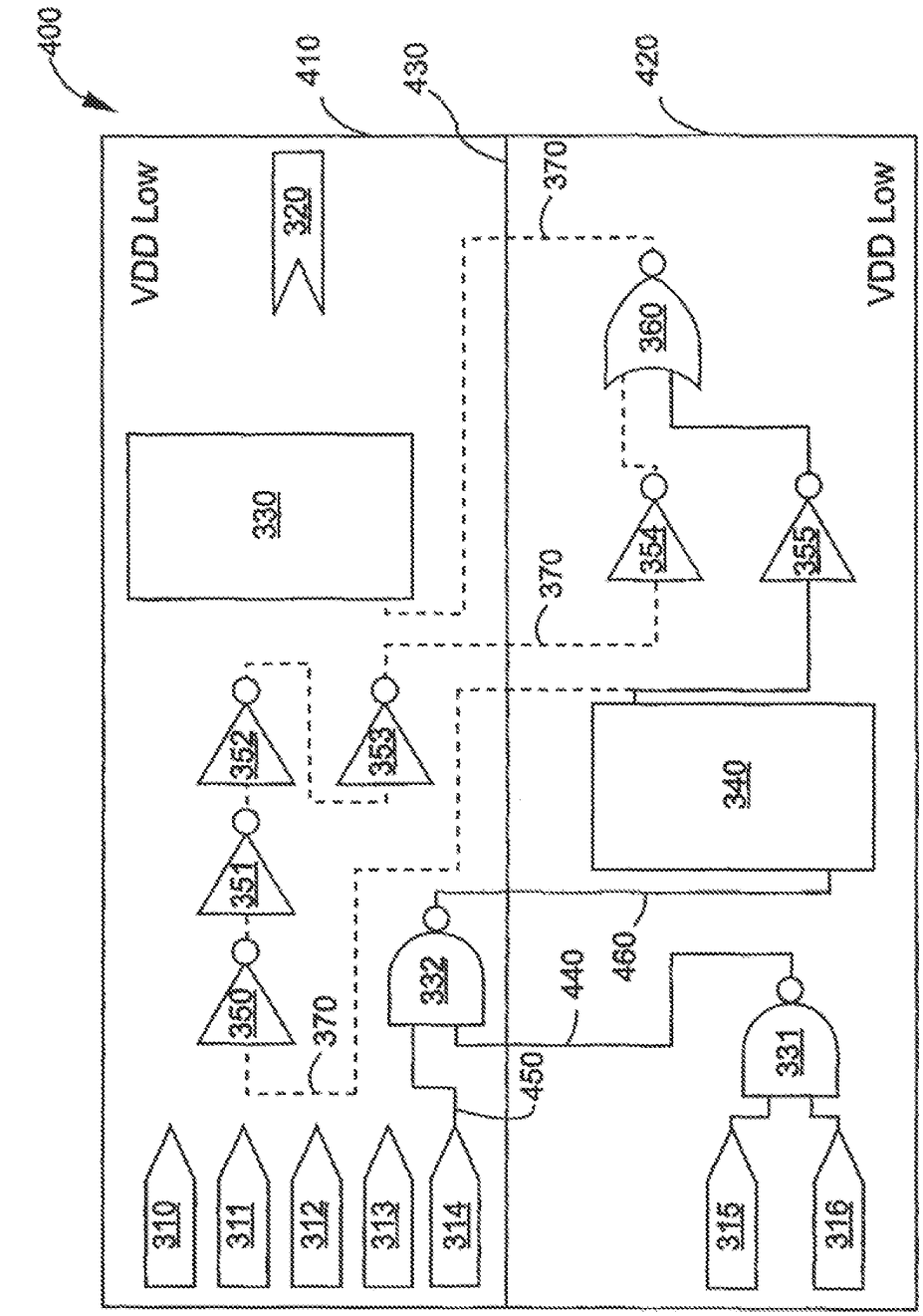

400
410
430
420
VDD Low
VDD Low
320
330
340
370
370
370
440
460
450
310
311
312
313
314
315
316
331
332
350
351
352
353
354
355
360

图 4

B2

400
510
430
520
VDD_High
VDD_Low
320
330
340
电平移位器
370
470
480
490
360
354
355
352
353
351
350
332
331
460
440
450
310
311
312
313
314
315
316

图 5

B2

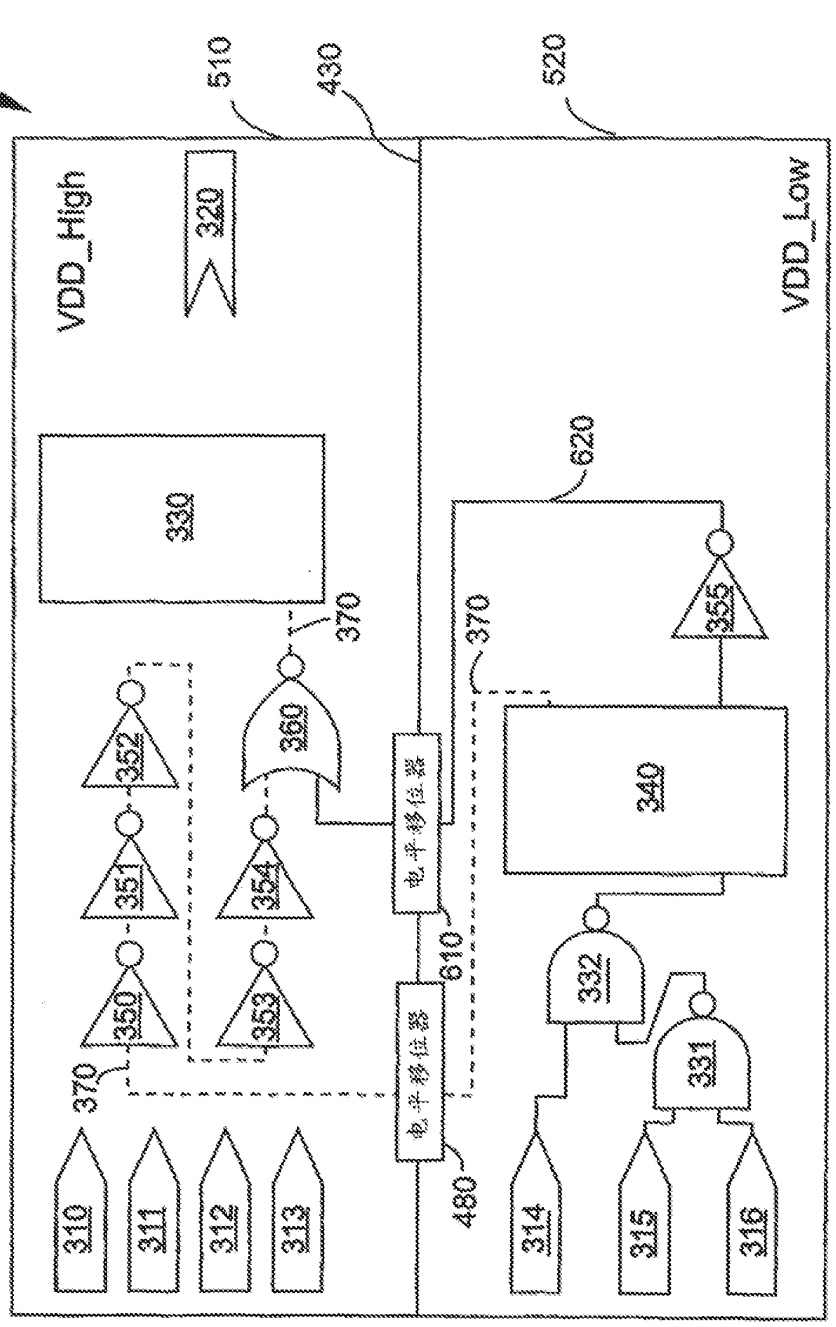

400
510
430
520
VDD_High
VDD_Low
320
330
620
370
370
370
352
351
350
354
353
360
355
240
电平移位器
电平移位器
610
480
332
331
310
311
312
313
314
315
316

图 6

B2

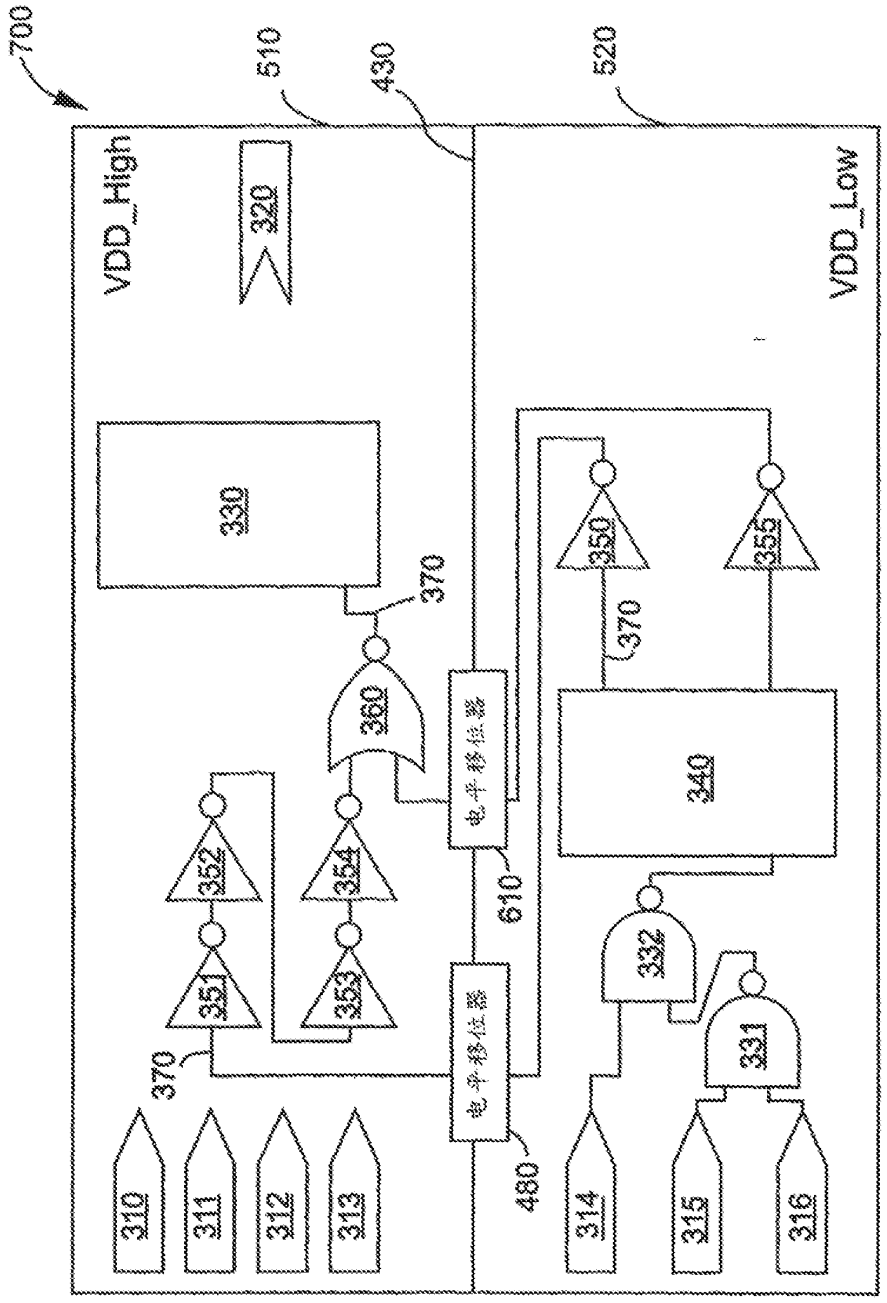

700
510
430
520
VDD_High
VDD_Low
320
330
370
360
352
354
351
353
370
电平移位器
610
480
350
355
370
340
332
331
310
311
312
313
314
315
316

图 7

B2

1000
1020
1040
1030
VDD_High
VDD_Low
1091
1050
1086
1087
1085
1090
1093
电平移位器
1094
1055
1080
1075
G2
1070
G1
1090
1045
1010
1011
1012
1013
1060
1014
1015
1016

图 8

1000
1020
1040
1030
VDD_High
VDD_Low
1091
1050
1086
1087
1096
G2
CLONE
1097
G1
CLONE
1099
1090
1085
1090
1080
1075
G2
1070
G1
1045
电平移位器
1060
1010
1011
1012
1013
1014
1015
1016

图 9

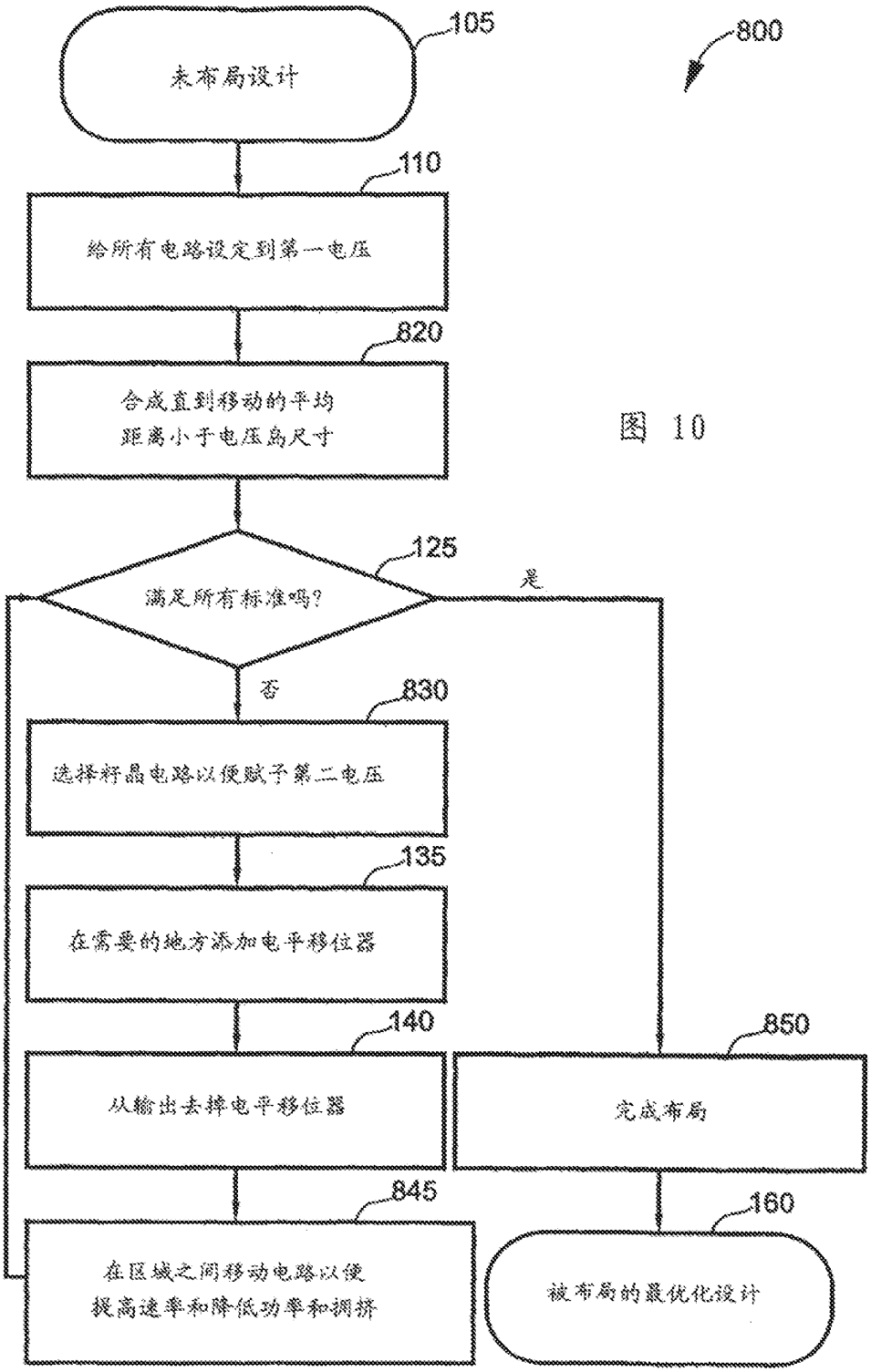

105
未布局设计
800
110
给所有电路设定到第一电压
820
合成直到移动的平均
距离小于电压岛尺寸
125
满足所有标准吗?
是
否
830
选择籽晶电路以便赋予第二电压
135
在需要的地方添加电平移位器
140
从输出去掉电平移位器
850
完成布局
845
在区域之间移动电路以便
提高速率和降低功率和拥挤
160
被布局的最优化设计

图 10

B2

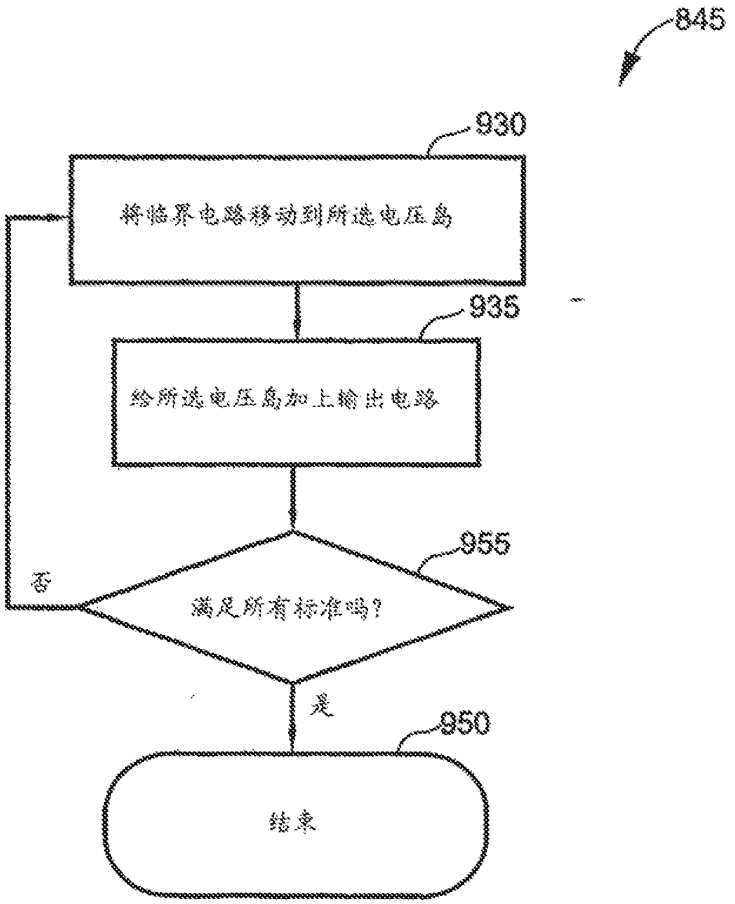

845
930
将临界电路移动到所选电压岛
935
给所选电压岛加上输出电路
955
否
满足所有标准吗?
是
950
结束

图 11

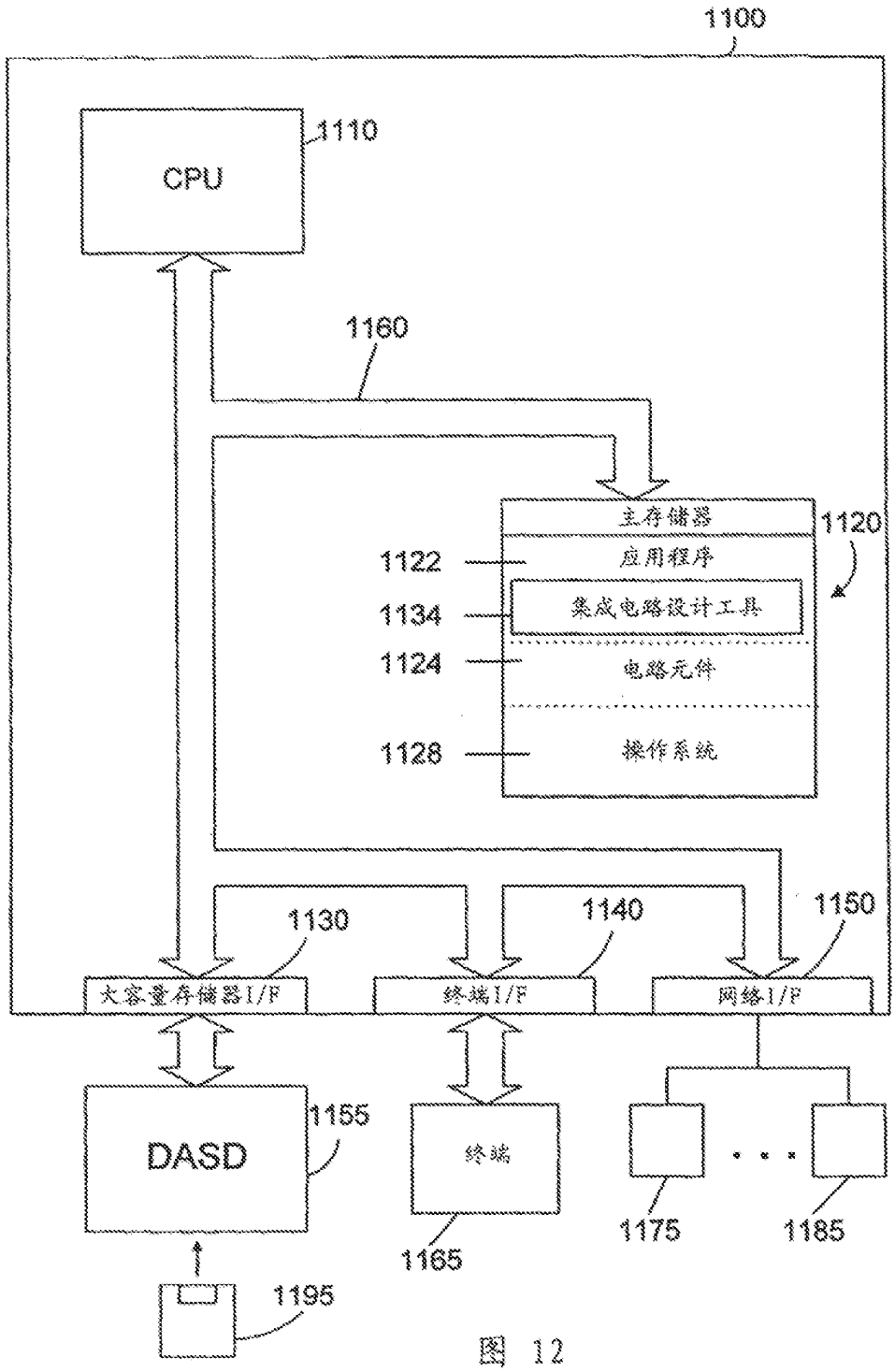

1100
CPU
1110
1160
主存储器
1120
1122
应用程序
1134
集成电路设计工具
1124
电路元件
1128
操作系统
1130
1140
1150
大容量存储器I/F
终端I/F
网络I/F
DASD
1155
终端
1165
1175
1185
1195

图 12

Electronic Acknowledgement Receipt

EFS ID:	9092583
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	21005
Filer:	James M. Smith/Jill Kane
Filer Authorized By:	James M. Smith
Attorney Docket Number:	2037.2079-010
Receipt Date:	22-DEC-2010
Filing Date:	21-JUL-2008
Time Stamp:	12:36:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	20372079010_SIDS.pdf	74066 5c8fc1fac0fc9a6e48313fe62b950cc56c711088	no	3

Warnings:	
Information:	

2	Information Disclosure Statement (IDS) Filed (SB/08)	20372079010_LOR.pdf	86377 8d32bef19f240325266f5941b9bbc295530f49e1	no	3
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Information:					
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3	Foreign Reference	20372079010_B2.pdf	7927481 f452fbcb32af1d6bbd19bc12022a24371645b8b0	no	39
Warnings:					
Information:					
4	NPL Documents	20372079010_C5.pdf	29366 ea523abc41afd9fd75d6069764a4eece74c45ba6	no	1
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Information:					
			Total Files Size (in bytes):	8117290	

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National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

JMS/jmk
December 21, 2010

PATENT APPLICATION
DOCKET NO.: 2037.2079-010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2825
Filed:	July 21, 2008	Examiner:	Lin, Sun J.
Confirmation No.:	3003		
For:	Power Managers For An Integrated Circuit		

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Date Signature

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Typed or printed name of person signing certificate

TRANSMITTAL LETTER FOR SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Information Disclosure Statement is submitted:

☒ under 37 CFR 1.97(b), or
(Within any one of the following time periods: three months of filing national application (other than a CPA) or date of entry of the national stage in an international application; or before the mailing date of a first office action on the merits; or before the mailing of a first office action after the filing of a Request for Continued Examination).

☐ under 37 CFR 1.97(c) together with either:
- ☐ a Statement under 37 CFR 1.97(e), as checked below, or
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(After the 37 CFR 1.97(b) time period, but before any of a final action, notice of allowance, or an action that closes prosecution, whichever occurs first)

☐ under 37 CFR 1.97(d) together with:
- ☐ a Statement under 37 CFR 1.97(e), as checked below, and
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(Filed after final action, notice of allowance, whichever occurs first, or if prosecution otherwise closes, but on or before payment of the issue fee)

☐ under 37 CFR 1.97(i):
Applicant requests that the IDS and cited reference(s) be placed in the application file.
(Filed after payment of issue fee)

Statement Under 37 CFR 1.97(e)

☐ Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement; or

☐ No item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

Statement Under 37 CFR 1.704(d) (Patent Term Adjustment)
Applies to original applications (other than design) filed on or after May 29, 2000

☐ Each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in § 1.56(c) more than thirty days prior to the filing of the Information Disclosure Statement.

☒ Enclosed herewith is a Listing of References. Copies of the cited references are enclosed except as indicated below or in the attached Listing of References.

☐ Copies of the cited references submitted with an Information Disclosure Statement in prior application, U.S. Application No. [ ], to which priority under 35 U.S.C. 120 is claimed, are not required under 37 CFR 1.98(d)(1) and (2) and are thus not provided.

☒ The listed references were cited in the enclosed Search Report in counterpart foreign application TW 093112998, which is listed in the attached Listing of References.

☒ The "concise explanation" requirement (non-English references) for reference B2 under 37 CFR 1.98(a)(3) is satisfied by:

- ☐ the explanation provided on the attached sheet.
- ☐ the explanation provided in the Specification.
- ☐ submission of the enclosed International Search Report.
- ☐ submission of the enclosed English-language version of a foreign Search Report and/or foreign Office Action.
- ☒ the enclosed English language abstract.

Method of payment:

☐ Authorization is NOT granted to charge any fees which may be due in this matter to our Deposit Account.

☐ Please charge Deposit Account 08-0380 in the amount of $[ ].

☐ A check for the fee noted above is enclosed, or the fee has been included in the check with the accompanying Reply.

☒ Please charge any deficiency in fees and credit any overpayment to Deposit Account 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By /James M. Smith, Reg. No. 28,043/
James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Dated: December 21, 2010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2825
Filed:	July 21, 2008	Examiner:	Sun J. Lin
Confirmation No:	3003		
For:	Power Managers for an Integrated Circuit		

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Date Signature

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SECOND PRELIMINARY AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please amend the application as follows:

Amendments to the Claims

Please cancel Claims 1-75. Please add new Claims 76-131. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1-75. (Cancelled).

76. (New) An integrated circuit comprising:

a plurality of power islands having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

one or more power consumption signals indicating one or more of the power consumptions;

a power management processor coupled to each of the power islands configured to monitor the one or more power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

77. (New) The integrated circuit as claimed in Claim 76 wherein the power management software is embedded firmware in the integrated circuit.

78. (New) The integrated circuit as claimed in Claim 77 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

79. (New) The integrated circuit as claimed in Claim 77 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

80. (New) The integrated circuit as claimed in Claim 76 wherein each of the power consumptions is further controlled by stopping the clock.

81. (New) The integrated circuit as claimed in Claim 80 wherein stopping the clock comprises clock gating.

82. (New) An integrated circuit comprising:

a plurality of power islands having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

one or more power consumption signals indicating one or more of the power consumptions;

a power manager coupled to each of the power islands configured to monitor the one or more power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

83. (New) The integrated circuit as claimed in Claim 82 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.

84. (New) The integrated circuit as claimed in Claim 83 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

85. (New) The integrated circuit as claimed in Claim 83 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

86. (New) The integrated circuit as claimed in Claim 82 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.

87. (New) The integrated circuit as claimed in Claim 82 wherein each of the power consumptions is further controlled by stopping the clock.

88. (New) The integrated circuit as claimed in Claim 87 wherein stopping the clock comprises clock gating.

89. (New) An integrated circuit comprising:

a plurality of power islands having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

a power management processor coupled to each of the power islands and configured to monitor the power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

90. (New) The integrated circuit as claimed in Claim 89 wherein the power management software is embedded firmware in the integrated circuit.

91. (New) The integrated circuit as claimed in Claim 90 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

92. (New) The integrated circuit as claimed in Claim 90 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

93. (New) The integrated circuit as claimed in Claim 89 wherein each of the power consumptions is further controlled by stopping the clock.

94. (New) The integrated circuit as claimed in Claim 93 wherein stopping the clock comprises clock gating.

95. (New) An integrated circuit comprising:

a plurality of power islands having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

a power manager coupled to each of the power islands and configured to monitor the power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

96. (New) The integrated circuit as claimed in Claim 95 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.

97. (New) The integrated circuit as claimed in Claim 96 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

98. (New) The integrated circuit as claimed in Claim 96 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

99. (New) The integrated circuit as claimed in Claim 95 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.

100. (New) The integrated circuit as claimed in Claim 95 wherein each of the power consumptions is further controlled by stopping the clock.

101. (New) The integrated circuit as claimed in Claim 100 wherein stopping the clock comprises clock gating.

102. (New) A system for an integrated circuit, the system comprising:

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

one or more power consumption signals indicating one or more of the power consumptions;

a power management processor coupled to each of the power islands configured to monitor the one or more power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

103. (New) The system as claimed in Claim 102 wherein the power management software is embedded firmware.

104. (New) The system as claimed in Claim 103 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

105. (New) The system circuit as claimed in Claim 103 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

106. (New) The system as claimed in Claim 102 wherein each of the power consumptions is further controlled by stopping the clock.

107. (New) The system as claimed in Claim 106 wherein stopping the clock comprises clock gating.

108. (New) The system as claimed in Claim 102 wherein the system is configured to have the supply voltage provided by an external regulator.

109. (New) A system for an integrated circuit, the system comprising:

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

one or more power consumption signals indicating one or more of the power consumptions;

a power manager coupled to each of the power islands configured to monitor the one or more power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

110. (New) The system as claimed in Claim 109 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.

111. (New) The system as claimed in Claim 110 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

112. (New) The system as claimed in Claim 110 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

113. (New) The system as claimed in Claim 109 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.

114. (New) The system as claimed in Claim 109 wherein each of the power consumptions is further controlled by stopping the clock.

115. (New) The system as claimed in Claim 114 wherein stopping the clock comprises clock gating.

116. (New) The system as claimed in Claim 109 wherein the system is configured to have the supply voltage provided by an external regulator.

117. (New) A system for an integrated circuit, the system comprising:

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

a power management processor coupled to each of the power islands configured to monitor the power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

118. (New) The system as claimed in Claim 117 wherein the power management software is embedded firmware.

119. (New) The system as claimed in Claim 118 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

120. (New) The system as claimed in Claim 118 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

121. (New) The system as claimed in Claim 117 wherein each of the power consumptions is further controlled by stopping the clock.

122. (New) The system as claimed in Claim 121 wherein stopping the clock comprises clock gating.

123. (New) The system as claimed in Claim 117 wherein the system is configured to have the supply voltage provided by an external regulator.

124. (New) A system for an integrated circuit, the system comprising:

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power islands having a power consumption signal indicating a

respective one of the power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

a power manager coupled to each of the power islands configured to monitor the power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

125. (New) The system as claimed in Claim 124 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.

126. (New) The system as claimed in Claim 125 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

127. (New) The system as claimed in Claim 125 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

128. (New) The system as claimed in Claim 124 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.

129. (New) The system as claimed in Claim 124 wherein each of the power consumptions is further controlled by stopping the clock.

130. (New) The system as claimed in Claim 129 wherein stopping the clock comprises clock gating.

131. (New) The system as claimed in Claim 124 wherein the system is configured to have the supply voltage provided by an external regulator.

REMARKS

In view of the above amendments, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By /James M. Smith Reg. No. 28,043/
James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Date: October 6, 2010

Electronic Acknowledgement Receipt	
EFS ID:	8576466
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	21005
Filer:	James M. Smith/Jill Kane
Filer Authorized By:	James M. Smith
Attorney Docket Number:	2037.2079-010
Receipt Date:	07-OCT-2010
Filing Date:	21-JUL-2008
Time Stamp:	15:08:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	20372079010_Fee_Trasmittal.pdf	101219 d31d82819fc17d8fa6c9a27001b984826bf33136	no	3
Warnings:					
Information:					

2		20372079010_Prelim_Amend.pdf	79058 394ea877e89c2a4ad41717975c9171fa89939810	yes	12

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Claims	2	11
	Applicant Arguments/Remarks Made in an Amendment	12	12

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New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2825
Filed:	July 21, 2008	Examiner:	Sun J. Lin
Confirmation No:	3003		
For:	Power Managers for an Integrated Circuit		

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Date Signature

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is a Second Preliminary Amendment for filing in the above-identified application.

☐ Small entity status of this application under 37 CFR 1.9 and 1.27 has been established by a Small Entity Statement previously submitted.

☐ A Small Entity Statement to establish small entity status under 37 CFR 1.9 and 1.27 is enclosed.

The claims fee has been calculated as shown below:

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDIT. FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDIT. FEE
TOTAL	56	MINUS	* 60	0	X $ 26	$		X $52	$ 0
INDEP	8	MINUS	** 10	0	X $110	$		X $220	$ 0
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM					+ $195	$		+ $390	$ 0
			* not fewer than 20 ** not fewer than 3		TOTAL =	$ 0		TOTAL =	$ 0

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(Effective for cases filed on or after December 8, 2004)

Actual Sheets (Including current amendment)	Highest No. of Sheets Paid For (At least 100)	No. of Additional Units Required (Increments of 50 sheets)	SMALL ENTITY Rate	SMALL ENTITY Total Amount Owed	OTHER THAN SMALL ENTITY Rate	OTHER THAN SMALL ENTITY Total Amount Owed	Payment Sufficient for up to
51	100	0	X $135	$[ ]	X $270	$0	100 Sheets

Petition for Extension of Time

☐ Applicant hereby petitions to extend the time to respond to the [ ] dated [ ] for [ ] month(s) from [ ] to [ ]. The appropriate fee is set forth below.

☐ *[For action-specific language in an extension of time, select the appropriate option from the Firm Templates]*

Please charge Deposit Account No. 08-0380 for the following fees:

☐	Petition for [ ] month Extension of Time	$
☐	Claims Fee	$
☐	Application Size Fee	$
☐	Other Fees:	
	_____	$
	_____	$
	TOTAL:	$

A check is enclosed in payment of the following fees:

☐	Petition for [ ] month Extension of Time	$
☐	Claims Fee	$
☐	Application Size Fee	$
☐	Other Fees:	
	_____	$
	_____	$
	TOTAL:	$

☒ Please charge any deficiency or credit any overpayment in the fees that may be due in this matter to Deposit Account No. 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By /James M. Smith Reg. No. 28,043/
James M. Smith
Registration No.: 28,043
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Concord, Massachusetts 01742-9133
Dated: October 6, 2010

1023760.1

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/176,645	07/21/2008	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☒ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☒ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	10/07/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 56	Minus	** 60	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	* 8	Minus	***10	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/ROBERT SHERMAN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2825
Filed:	July 21, 2008	Examiner:	Sun J. Lin
Confirmation No:	3003		
For:	Power Managers for an Integrated Circuit		

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or is being facsimile transmitted to the United States Patent and Trademark Office on:

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Date Signature

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Typed or printed name of person signing certificate

PRELIMINARY AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Please amend the application as follows:

Amendments to the Claims

Please add new Claim 75. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1. (Previously Presented) A software product for building an integrated circuit including a plurality of power islands, the software product comprising:

computer readable instructions stored on an at least one storage medium, the computer readable instructions configured for selecting blocks of predetermined circuits to form:

power control circuitry configured to control power for one of the power islands, and

a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, and determine at least one of actions including selecting a frequency for one of the power islands, selecting a voltage for one of the power islands, and selecting a transistor threshold voltage for one of the power islands, the at least one of the actions to change a power consumption level of the one of the power islands to the target power level, and the power manager configured to perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level.

2. (Original) The software product of claim 1 wherein the power islands are delineated based on geographic factors of the integrated circuit.

3. (Original) The software product of claim 1 wherein the power islands are delineated based on functional circuitry of the integrated circuit.

4. (Cancelled).

5. (Original) The software product of claim 1 wherein the power islands comprise multiple clock domains.

6. (Previously Presented) The software product of claim 1 wherein the actions further include performing clock gating for the one of the power islands.

7-9. (Cancelled).

10. (Previously Presented) The software product of claim 1 wherein the actions further include powering on the one of the power islands.

11. (Previously Presented) The software product of claim 10 wherein the actions further include powering off the one of the power islands.

12. (Previously Presented) The software product of claim 1 wherein the actions further include changing a mode of the one of the power islands to sleep.

13-15. (Cancelled).

16. (Previously Presented) A software product for building an integrated circuit including a plurality of power islands, the software product comprising:

computer readable instructions stored on an at least one storage medium, the computer readable instructions configured for writing a register transfer level description (RTL), the RTL representing:

power control circuitry configured to control power for one of the power islands, and

a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, and determine at least one of actions including selecting a frequency for one of the power islands, selecting a voltage for one of the power islands, and selecting a transistor threshold voltage for one

of the power islands, the at least one of the actions to change a power consumption level of the one of the power islands to the target power level, and the power manager configured to perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level.

17-18. (Cancelled).

19. (Previously Presented) The software product of claim 16 wherein the computer readable instructions further comprise code for adding annotations for the power manager.

20. (Original) The software product of claim 19 wherein the annotations include functionality options.

21-26. (Cancelled).

27. (Previously Presented) The software product of claim 1 wherein the predetermined circuits are in register transfer level description (RTL) form.

28. (Previously Presented) The software product of claim 1 wherein the actions further include controlling a sleep signal connected to an at least one standard cell of the one of the power islands.

29. (Previously Presented) The software product of claim 1 wherein the actions further include powering off the one of the power islands.

30. (Previously Presented) The software product of claim 16 further comprising additional computer readable instructions for adding annotations, at multiple steps in a design process, to a portion of the RTL representing the power manager.

31. (Previously Presented) An integrated circuit comprising:

a plurality of power islands having associated power consumptions, each of the power consumptions being independently controlled, and a power consumption in an at least one of the power islands being controlled by: a) selecting a threshold voltage of variable threshold transistors, and b) selecting at least one of the following: i) a frequency of operation, and ii) a supply voltage; and

a power manager which controls the power consumptions.

32. (Previously Presented) The integrated circuit as claimed in claim 31 wherein the supply voltage is selected, and the selecting of the supply voltage includes dynamic voltage selection.

33. (Previously Presented) The integrated circuit as claimed in claim 31 wherein the supply voltage is selected, and the selecting of the supply voltage includes regulating an externally provided voltage.

34. (Previously Presented) The integrated circuit as claimed in claim 33 wherein the regulating is performed with a dropout voltage regulator.

35. (Previously Presented) The integrated circuit as claimed in claim 31 wherein the supply voltage is selected, and the selecting of the supply voltage includes powering off the supply.

36. (Previously Presented) The integrated circuit as claimed in claim 31 wherein the selecting the threshold includes dynamic back biasing.

37. (Previously Presented) An integrated circuit comprising:

a plurality of power islands having associated power consumptions, each of the power consumptions being independently controlled, and a power consumption in an at

least one of the power islands being controlled by selecting a supply voltage, and by selecting a frequency of operation, including an option of stopping a clock; and

a power manager which controls the power consumptions.

38. (Previously Presented) The integrated circuit as claimed in claim 37 wherein the selecting of the supply voltage includes dynamic voltage selection.

39. (Previously Presented) The integrated circuit as claimed in claim 37 wherein the selecting of the supply voltage includes regulating an externally provided voltage.

40. (Previously Presented) The integrated circuit as claimed in claim 39 wherein the regulating is performed with a dropout voltage regulator.

41. (Previously Presented) The integrated circuit as claimed in claim 37 wherein the selecting of the supply voltage includes powering off the supply.

42. (Previously Presented) The integrated circuit as claimed in claim 37 wherein the selecting of the frequency of operation includes dynamic clock selection.

43. (Previously Presented) The integrated circuit as claimed in claim 37 wherein the selecting of the frequency of operation includes modifying a clock frequency.

44. (Previously Presented) The integrated circuit as claimed in claim 37 wherein the stopping of the clock is performed by clock gating.

45. (Previously Presented) An integrated circuit comprising:

a plurality of power islands having associated power consumptions, at least one of the power consumptions being independently controlled by way of a sleep signal connected to an at least one standard cell; and

a power manager which controls at least one or more of the power consumptions.

46. (Previously Presented) The integrated circuit as claimed in claim 45 wherein the at least one standard cell includes a MOS transistor having a source connected to a power supply terminal and a gate connected to the sleep signal.

47. (Previously Presented) The integrated circuit as claimed in claim 46 wherein the MOS transistor is an n-channel transistor.

48. (Previously Presented) The integrated circuit as claimed in claim 46 wherein the source of the MOS transistor is connected to a ground power supply terminal.

49. (Previously Presented) The integrated circuit as claimed in claim 45 wherein at least one of the power islands includes multiple voltage domain interface circuits.

50. (Previously Presented) The integrated circuit as claimed in claim 49 wherein the multiple voltage domain interface circuits include level shifter circuits.

51. (Previously Presented) The integrated circuit as claimed in claim 49 wherein the multiple voltage domain interface circuits include signal isolation circuits.

52. (Previously Presented) The integrated circuit as claimed in claim 45 wherein at least one of the power islands includes multiple threshold standard cells.

53. (Previously Presented) The integrated circuit as claimed in claim 52 wherein the multiple threshold standard cells include at least two of the following standard cells: standard Vt, high Vt, and low Vt.

54. (Previously Presented) The integrated circuit as claimed in claim 45 wherein at least one of the power islands includes variable Vt standard cells.

55. (Previously Presented) A computer-implemented method for building an integrated circuit that includes a plurality of power islands, the method comprising:

selecting first blocks of first predetermined circuits to form power control circuitry, the power control circuitry configured to control power for one of the power islands; and

selecting an at least one second block of an at least one second predetermined circuit to form a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, and determine at least one of actions including selecting a frequency for one of the power islands, selecting a voltage for one of the power islands, and selecting a transistor threshold voltage for one of the power islands, the at least one of the actions to change a power consumption level of the one of the power islands to the target power level, and the power manager configured to perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level.

56. (Previously Presented) The computer-implemented method of claim 55 wherein the actions further include performing clock gating for the one of the power islands.

57. (Previously Presented) The computer-implemented method of claim 55 wherein the actions further include powering on the one of the power islands.

58. (Previously Presented) The computer-implemented method of claim 55 wherein the actions further include powering off the one of the power islands.

59. (Previously Presented) The computer-implemented method of claim 55 wherein the actions further include changing a mode of the one of the power islands to sleep.

60. (Previously Presented) A method carried out within an integrated circuit having a plurality of power islands having associated power consumptions, the method comprising:

employing a power manager to control the power consumptions, each of the power consumptions being independently controlled; and

controlling a power consumption of an at least one of the power islands by: a) selecting a threshold voltage of variable threshold transistors, and b) selecting at least one of the following: i) a frequency of operation, and ii) a supply voltage.

61. (Previously Presented) The method as claimed in claim 60 wherein the supply voltage is selected, and the selecting of the supply voltage includes dynamic voltage selection.

62. (Previously Presented) The method as claimed in claim 60 wherein the supply voltage is selected, and the selecting of the supply voltage includes regulating an externally provided voltage.

63. (Previously Presented) The method as claimed in claim 60 wherein the supply voltage is selected, and the selecting of the supply voltage includes powering off the supply.

64. (Previously Presented) The method as claimed in claim 60 wherein the selecting the threshold includes dynamic back biasing.

65. (Previously Presented) A method carried out within an integrated circuit having a plurality of power islands having associated power consumptions, the method comprising:

employing a power manager to control the power consumptions, each of the power consumptions being independently controlled; and

controlling a power consumption of an at least one of the power islands by selecting a supply voltage and selecting a frequency of operation, including an option of stopping a clock.

66. (Previously Presented) The method as claimed in claim 65 wherein the selecting of the supply voltage includes dynamic voltage selection.

67. (Previously Presented) The method as claimed in claim 65 wherein the selecting of the supply voltage includes regulating an externally provided voltage.

68. (Previously Presented) The method as claimed in claim 65 wherein the selecting of the supply voltage includes powering off the supply.

69. (Previously Presented) The method as claimed in claim 65 wherein the selecting of the frequency of operation includes dynamic clock selection.

70. (Previously Presented) The method as claimed in claim 65 wherein the selecting of the frequency of operation includes modifying a clock frequency.

71. (Previously Presented) The method as claimed in claim 65 wherein the stopping of the clock is performed by clock gating.

72. (Previously Presented) A method carried out within an integrated circuit having a plurality of power islands having associated power consumptions, the method comprising:

employing a power manager to control the power consumptions, each of the power consumptions being independently controlled; and

controlling a power consumption of an at least one of the power islands by way of a sleep signal connected to an at least one standard cell of the at least one of the power islands.

73. (Previously Presented) The method as claimed in claim 72 further comprising generating the sleep signal.

74. (Previously Presented) The method as claimed in claim 72 wherein the sleep signal is connected to a gate of an NMOS transistor of the at least one standard cell.

75. (New) A system for an integrated circuit, the system comprising:

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions adapted to be independently controlled; and

a power manager to control the power consumptions;

at least one of the power islands adapted to have the power manager control its associated power consumption by a) the at least one of the power islands being configured to have one of plural threshold voltages of variable threshold transistors selected, and b) the system being configured to perform, during operation, an action on the at least one of the power islands, the action including changing a frequency of operation or changing a supply voltage.

REMARKS

New Claim 75 corresponds to Claim 21 of related application 11/588,835.

In view of the above amendments, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By /James M. Smith, Reg. No. 28,043/
James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Date: June 14, 2010

Electronic Patent Application Fee Transmittal

Application Number:	12176645
Filing Date:	21-Jul-2008
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Filer:	James M. Smith
Attorney Docket Number:	2037.2079-010

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1202	1	52	52
Independent claims in excess of 3	1201	1	220	220
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**272**

Electronic Acknowledgement Receipt	
EFS ID:	7807705
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	21005
Filer:	James M. Smith/Jill Kane
Filer Authorized By:	James M. Smith
Attorney Docket Number:	2037.2079-010
Receipt Date:	14-JUN-2010
Filing Date:	21-JUL-2008
Time Stamp:	16:51:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$272
RAM confirmation Number	3495
Deposit Account	080380
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Transmittal Letter	20372079010_Fee_Transmittal.pdf	101987 89bde76bfa911d28a00c240f245b3e8bb24b81e7	no	3
Warnings:					
Information:					
2		20372079010_Preliminary_Amend.pdf	84444 d397d9f2d71514ef01af4afdd57887a34d458aa7	yes	12

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Claims	2	11
	Applicant Arguments/Remarks Made in an Amendment	12	12

Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	31938 c02ed66f51887941fb942679a3cb193b124eeeba	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	218369		

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2825
Filed:	July 21, 2008	Examiner:	Sun J. Lin
Confirmation No:	3003		
For:	Power Managers for an Integrated Circuit		

CERTIFICATE OF MAILING OR TRANSMISSION

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Date Signature

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Typed or printed name of person signing certificate

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is a Preliminary Amendment for filing in the above-identified application.

☐ Small entity status of this application under 37 CFR 1.9 and 1.27 has been established by a Small Entity Statement previously submitted.

☐ A Small Entity Statement to establish small entity status under 37 CFR 1.9 and 1.27 is enclosed.

The claims fee has been calculated as shown below:

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	SMALL ENTITY RATE	SMALL ENTITY ADDIT. FEE	OR	OTHER THAN SMALL ENTITY RATE	OTHER THAN SMALL ENTITY ADDIT. FEE
TOTAL	60	MINUS	* 59	1	X $ 26	$		X $52	$ 52
INDEP	10	MINUS	** 9	1	X $110	$		X $220	$ 220
☐ FIRST PRESENTATION OF MULTIPLE DEP. CLAIM					+ $195	$		+ $390	$
			* not fewer than 20 ** not fewer than 3		TOTAL =	$ 0		TOTAL =	$ 272

The Application Size Fee has been calculated as shown below:
(Effective for cases filed on or after December 8, 2004)

Actual Sheets (Including current amendment)	Highest No. of Sheets Paid For (At least 100)	No. of Additional Units Required (Increments of 50 sheets)	SMALL ENTITY Rate	SMALL ENTITY Total Amount Owed	OTHER THAN SMALL ENTITY Rate	OTHER THAN SMALL ENTITY Total Amount Owed	Payment Sufficient for up to
42	100	0	X $135	$[ ]	X $270	$0	100 Sheets

Petition for Extension of Time

☐ Applicant hereby petitions to extend the time to respond to the [ ] dated [ ] for [ ] month(s) from [ ] to [ ]. The appropriate fee is set forth below.

☐ *[For action-specific language in an extension of time, select the appropriate option from the Firm Templates]*

Please charge Deposit Account No. 08-0380 for the following fees:

☐	Petition for [ ] month Extension of Time	$
☒	Claims Fee	$ 272
☐	Application Size Fee	$
☐	Other Fees:	
		$
		$
	TOTAL:	$ 272

A check is enclosed in payment of the following fees:

☐	Petition for [ ] month Extension of Time	$
☐	Claims Fee	$
☐	Application Size Fee	$
☐	Other Fees:	
		$
		$
	TOTAL:	$

☒ Please charge any deficiency or credit any overpayment in the fees that may be due in this matter to Deposit Account No. 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By /James M. Smith, Reg. No. 28,043/
James M. Smith
Registration No.: 28,043
Telephone (978) 341-0036
Facsimile (978) 341-0136

Concord, Massachusetts 01742-9133
Dated: June 14, 2010

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/176,645	07/21/2008	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	06/14/2010	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 60	Minus	** 59	= 1	X $ =		OR	X $52=	52
	Independent (37 CFR 1.16(h))	* 10	Minus	***9	= 1	X $ =		OR	X $220=	220
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	272

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

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The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/NICOLE LOVE-HENSLEY/

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Substitute for form 1449B/PTO **INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **February 3, 2010** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Not Yet Assigned	CONFIRMATION NO. 3003	GROUP 2811

FOREIGN PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Country Code-Number-Kind Code (if known)	DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT	TRANSLATION YES	TRANSLATION NO
	B1	JP 2003-108260	04-11-2003	Hitachi Ltd.	X	
	B2					
	B3					
	B4					
	B5					
	B6					
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	B8					
	B9					
	B10					
	B11					
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	B14					
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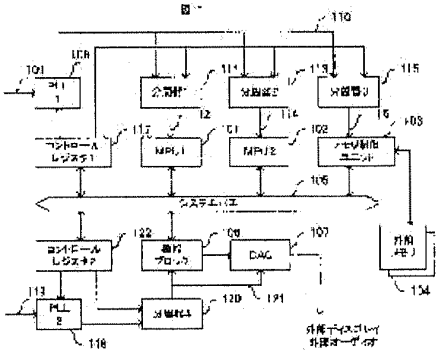
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(71)Applicant : **HITACHI LTD**
(72)Inventor : **KUROKAWA YOSHITAKE**
NISHIOKA KIYOKAZU
NAKADA KEIMEI
HOSOKI KOJI

(54) INFORMATION PROCESSER AND CONTROLLING METHOD THEREFOR

(57)Abstract:
PROBLEM TO BE SOLVED: To allow changing an operating frequency and a voltage enabling to operate at the minimum consumption power possible to achieve a processing capacity enough to perform an application.
SOLUTION: An apparatus for information processing comprises MPUs 101 and 102, a memory control unit 103, dividers 111, 113, 115 and 120 whose frequency-division ratios are individually controlled to a functional block 106 and vary those operating frequencies. An application on the apparatus prepares information on operating frequencies optimum to each MPU 101 and 102 and the functional block 106. A control means for controlling the information for a plurality of applications is prepared to acquire the present operating status from the control means when initiating the applications and allocates the processing capacity needed by the applications to be initiated to each MPU 101 and 102 and the functional block 106 to vary those operating frequencies, and the same operation is performed when exiting the applications.



B1

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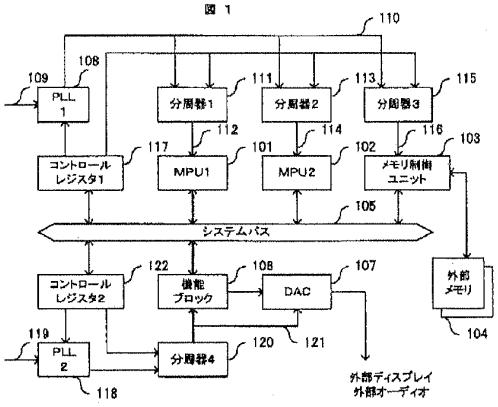
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最終頁に続く

(54)【発明の名称】　情報処理装置及び情報処理装置の制御方法

(57)【要約】
【課題】　アプリケーションに対して充分な処理能力が実現できる最小の消費電力で動作できる様に動作周波数、動作電圧を変更可能とする。
【解決手段】　ＭＰＵ１０１、１０２、メモリ制御ユニット１０３、機能ブロック１０６に対して、独立に分周比が制御される分周器１１１、１１３、１１５、１２０を持ち、それらの動作周波数を変更するする。また、情報処理装置上のアプリケーションが各ＭＰＵ、機能ブロックに最適な動作周波数情報を用意する。そして、複数のアプリケーションに対しこの情報を管理する手段を用意し、アプリケーションを開始したとき、現在の動作状況を管理手段から取得し、開始するアプリケーションに必要な処理能力を各ＭＰＵ、機能ブロックに割り振り、それらの動作周波数を変更する。アプリケーション終了時にも同様の動作を行う。

図１



【特許請求の範囲】
【請求項１】　１または複数のプロセッサ、専用論理を持つ１または複数の機能ブロックのいずれか１方あるいは両方を備える情報処理装置において、前記プロセッサ、機能ブロックのそれぞれの動作周波数を独立に変更する手段と、情報処理装置上で動作する１または複数のアプリケーションのそれぞれが持つプロセッサ、機能ブロックのそれぞれに最適な動作周波数情報に基づいて、前記プロセッサ、機能ブロックの動作周波数を決定し、前記動作周波数を変更する手段を制御する制御手段とを備えることを特徴とする情報処理装置。
【請求項２】　前記制御手段は、アプリケーションが開始されたとき、現在の情報処理装置の動作状況を管理している管理手段から動作状況を取得し、開始するアプリケーションに必要な処理能力をプロセッサ、機能ブロックに割り振り、前記プロセッサ、機能ブロックの動作周波数を変更することを特徴とする請求項１記載の情報処理装置。
【請求項３】　前記制御手段は、アプリケーションが終了されたとき、現在の情報処理装置の動作状況を管理している管理手段から動作状況を取得し、終了するアプリケーションに割り当てられていた処理能力をプロセッサ、機能ブロックから削除して、前記プロセッサ、機能ブロックの動作周波数を変更することを特徴とする請求項１記載の情報処理装置。
【請求項４】　バッテリ等の主電源と、その電圧を測定する測定手段とをさらに備え、前記制御手段は、前記プロセッサ、機能ブロックの動作周波数を、前記測定手段で測定された電源電圧で動作可能な周波数に設定することを特徴とする請求項１、２または３記載の情報処理装置。
【請求項５】　外部からのフォーマットされたデータ入力を受け付ける手段さらに備え、前記制御手段は、前記プロセッサ、機能ブロックの動作周波数を、前記データ入力のデータフォーマットに応じて、このデータフォーマットに適した動作周波数に設定することを特徴とする請求項１ないし４のうちいずれか１記載の情報処理装置。
【請求項６】　電源電圧を変更する手段をさらに備え、前記制御手段は、現在動作している１または複数のアプリケーションが必要としている動作周波数の総和で、前記前記プロセッサ、機能ブロックが動作することができるような電圧を、前記前記プロセッサ、機能ブロックに印加するように前記電源電圧を変更する手段を制御することを特徴とする請求項１ないし５のうちいずれか１記載の情報処理装置。
【請求項７】　１または複数のプロセッサ、専用論理を持つ１または複数の機能ブロックのいずれか１方あるいは両方を備える情報処理装置の制御方法において、情報処理装置上で動作する１または複数のアプリケーションのそれぞれが持つプロセッサ、機能ブロックのそれぞれに最適な動作周波数情報に基づいて、前記プロセッサ、機能ブロックの動作周波数を決定し、前記プロセッサ、機能ブロックのそれぞれの動作周波数を独立に変更することを特徴とする情報処理装置の制御方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、情報処理装置及び情報処理装置の制御方法に係り、特に、動作周波数を変更可能とした情報処理装置及び情報処理装置の制御方法に関する。
【０００２】
【従来の技術】近年、信号処理やメディア処理等の分野において、プロセッサや専用ハードウェアを使用した処理が行われるようになってきた。これらの処理は、その演算量が非常に大きく、また、一定時間内での処理終了が必須となるリアルタイム性が要求される。このため、これらの処理を実現する情報処理装置は、非常に高い処理性能が要求され、これを実現するために高い動作周波数が要求されている。
【０００３】一般に、プロセッサ等のＣＭＯＳトランジスタで構成されている半導体回路は、その動作周波数に比例して消費電力が増加する。これらの消費電力は、情報処理装置を構成する際の障害となるため、消費電力を低減するための種々の方法が提案されている。
【０００４】例えば、マルチプロセッサシステム等における消費電力の低減を図ることを可能にする従来技術として、例えば、特開平８－２０２４６８号公報等に記載された技術が知られている。この従来技術は、マルチプロセッサ構成のシステムにおいて、各プロセッサについて処理状態を検出し、使用していないかまたは負荷の軽いプロセッサを低消費電力モードに移行させ、システム全体の消費電力を押さえるというものである。
【０００５】また、端末の従来技術として、例えば、特開２０００－６６７７６号公報等に記載された技術が知られている。この従来技術は、システムのサブ回路の電力消費を制御する方法に関するもので、プロセッサに割り当てられた負荷に見合う動作周波数を割り出し、この周波数でプロセッサが動作することができる電源電圧を検出し、この電源電圧をプロセッサに印加することによって、その負荷を処理できる最小電力でプロセッサを動作させることを可能とするものである。
【０００６】前述したように、従来からマルチプロセッサシステムのような大規模な情報処理装置を構成するために、全体の消費電力を減らすという試みがなされてきた。
【０００７】一方、半導体回路の集積度が年々上がってきており、この結果、以前では複数の部品で構成されていた情報処理装置を１つの半導体回路に集積して構成することが可能となってきた。これによって、より小さな

情報処理装置の開発が可能となり、様々な小型機器への応用が行われている。特に、バッテリ等の電力供給源を使用することによって、携帯可能な情報処理装置の作成が可能となっている。従来、このような用途で半導体回路が使用される場合、電力供給源の容量に見合った最大消費電力を持つものを開発または選択してきたが、この方法は、前述したメディア処理等の高負荷の処理を行う情報処理装置を実現することが難しい。

【0008】

【発明が解決しようとする課題】前述したように、情報処理装置は、処理能力の増加が要求される一方で、バッテリ動作が可能である等の省電力化が要求されている。このため、情報処理装置には、これらの2つの要求を満たすために、ある情報処理装置が処理すべき対象であるアプリケーションに対して十分な処理能力を有し、かつ、その処理能力が実現できる最小の消費電力で動作することが要求されている。

【0009】しかし、前述した従来技術による情報処理装置は、前述したような2つの要求を同時に、かつ、充分に満足させることができるものではないという問題点を有している。

【0010】本発明の目的は、アプリケーションに対して充分な処理能力が実現できる最小の消費電力で動作できるように、動作周波数、動作電圧を変更することのできる高い処理能力を持ち、低消費電力化を図った情報処理装置及び情報処理装置の制御方法を提供することにある。

【0011】

【課題を解決するための手段】本発明によれば前記目的は、1または複数のプロセッサ、専用論理を持つ1または複数の機能ブロックのいずれか1方あるいは両方を備える情報処理装置において、前記プロセッサ、機能ブロックのそれぞれの動作周波数を独立に変更する手段と、情報処理装置上で動作する1または複数のアプリケーションのそれぞれが持つプロセッサ、機能ブロックのそれぞれに最適な動作周波数情報に基づいて、前記プロセッサ、機能ブロックの動作周波数を決定し、前記動作周波数を変更する手段を制御する制御手段とを備えることにより達成される。

【0012】また、前記目的は、1または複数のプロセッサ、専用論理を持つ1または複数の機能ブロックのいずれか1方あるいは両方を備える情報処理装置の制御方法において、情報処理装置上で動作する1または複数のアプリケーションのそれぞれが持つプロセッサ、機能ブロックのそれぞれに最適な動作周波数情報に基づいて、前記プロセッサ、機能ブロックの動作周波数を決定し、前記プロセッサ、機能ブロックのそれぞれの動作周波数を独立に変更することにより達成される。

【0013】

【発明の実施の形態】以下、本発明による情報処理装置の実施形態を図面により詳細に説明する。

【0014】図1は本発明の第1の実施形態による情報処理装置のハードウェア構成を示すブロック図、図2はアプリケーションプログラムの追加して起動したときに使用するプログラムの処理動作を説明するフローチャート、図3はアプリケーションプログラム終了時に使用するプログラムの処理動作を説明するフローチャート、図4は図2の処理で使用するクロックテーブルについて説明する図、図5は図2の処理でアプリケーションが追加起動された後のクロックテーブルの状態を説明する図、図6は図3処理でアプリケーションが終了させられた後のクロックテーブルの状態を説明する図であり、以下、これらの図を参照して本発明の第1の実施形態について説明する。

【0015】図1において、101、102は第1、第2のマイクロプロセッサユニット（以下、MPUという）、103は外部メモリ制御ユニット、104は外部メモリ、105はシステムバス、106は機能ブロック、107はデジタル－アナログコンバータ（以下、DACという）、108、118は第1、第2のフェイズロックドループ（以下、PLLという）、109、119は第1、第2のPLL用リファレンスクロック、110は第1のPLLの発振クロック、111、113、115、120は第1～第4の分周器、112、114は第1、第2のMPU用ローカルクロック、116はメモリ制御ユニット用ローカルクロック、117、122は第1、第2のコントロールレジスタ、121は機能ブロック及びDAC用ローカルクロックである。

【0016】図1に示す本発明の第1の実施形態において、第1のPLL108は、第1のコントロールレジスタ117の値を元にリファレンスクロック109を逓倍化して発振クロック110を作成する。この発振クロック110は、第1～第3の分周器111、113、115を通して、第1のMPU101、第2のMPU102及びメモリ制御ユニット103を駆動するためのローカルクロック112、114、116の生成のために使用される。分周器111、113、115のそれぞれは、第1のコントロールレジスタ117から値に基づいて独立に制御され、発振クロック110を分周して1／nの周波数に落とす。分周器111、113、115を、第1、第2のMPU101、102及びメモリ制御ユニット103の各ユニット毎に備えることより、各ユニットは、その動作周波数を発振クロック110の必要な1／n倍（nの値は分周器毎に異なってよい）に設定された周波数として受けることが可能となり、必要とする周波数で動作することができる。

【0017】第1、第2のMPU101、102は、外部メモリ104からプログラム及びデータを読み込み、演算を行い、また、システムバス105を通して機能ブロック106、第1、第2のコントロールレジスタ11

7、122を制御することが可能である。メモリ制御ユニット103は、第1、第2のMPU101、102、機能ブロック106のからの要求をシステムバス105を通して受けると、外部メモリ104を制御してデータの読み書きを行い、必要に応じて結果を要求元へ返信する。システムバス105は、これに接続されている全てのユニットに対し、要求元から要求先へ要求を伝え、結果を要求先から要求元へ返す。

【0018】説明している本発明の実施形態は、便宜上、システムバス105及びこれに接続されている各ユニット（101、102、103、106、117、122）の中でシステムバス105を制御している部分の全てが、メモリ制御ユニット103用のローカルクロック116で動作しているものとする。しかし、本発明は、システムバス105を、他のユニットのローカルクロックで動作させるようにしても、あるいは、システムバス専用のローカルクロックを新たに作成して動作させるようにしてもよい。

【0019】第2のPLL118は、第1のPLL108と同様の動作を行う。すなわち、第2のPLL118は、第2のコントロールレジスタ122の値を使用し、リファレンスクロック119を逓倍化して第4の分周器120に出力する。第4の分周器120は、第2のコントロールレジスタ122の値を使用して第4の分周器120からの逓倍化されクロックを分周し、ローカルクロック121を作成し、機能ブロック106及びDAC107に供給する。機能ブロック106は、第1、第2のMPU101、102では処理しきれない計算を行う処理に特化した専用論理により構成されている。そして、機能ブロック106は、第1のMPU101または第2のMPU102によって制御され、デジタルビデオ画像やデジタル音声のフィルタ処理、改ざん防止のためにソフトウェアでの実装が不可能な暗号処理等を行う。

【0020】前述した本発明の第1の実施形態は、第1、第2のMPU101、102に後述するプログラムを動作させ、コントロールレジスタ117、122を制御し、第1、第2のMPU101、102、メモリ制御ユニット103、機能ブロック106の動作周波数を変更することによって、システム全体の消費電力を押さえるように動作する。

【0021】なお、前述した図1に示す情報処理装置の例は、2台のMPUと1台の機能ブロックとを備えるとしているが、MPUと機能ブロックとは、それぞれ1または複数が設けられてよく、また、MPU、機能ブロックの一方だけが設けられてもよい。

【0022】次に、図2、図3を参照して、第1、第2のMPU101、102で使用するプログラムの動作を説明するが、これらのプログラムは、図1に示す外部メモリ104に格納され、必要に応じてMPUに読み込まれて処理される。また、これらのプログラムは、後述する図4～図6に示すクロックテーブルを使用するが、このテーブルも外部メモリ104に格納されていて、必要に応じてMPUに読み込まれて処理される。

【0023】図4に示すクロックテーブルは、アプリケーション番号の項目401、第1のMPUのクロック項目402、第2のMPUのクロック項目403、メモリ制御ブロックのクロック項目404、機能ブロック、DAC、ディスプレイのクロック項目405をパラメータとして持ち、これらが、システムのパラメータ欄406、第1のアプリケーションのパラメータ欄407、第2のアプリケーションのパラメータ欄408、総和値のパラメータ欄409、最大許容量のパラメータ欄410に格納されて構成される。また、このテーブルには、各パラメータの判定欄411が設けられる。

【0024】パラメータ欄406～408のクロック項目402～405の数値は、図1に示すリファレンスクロック109または119と、ローカルクロック112、114、116、121との比を示す値、すなわち、第1のPLLによる逓倍値と第1～第3の分周器の分周値との積に相当する値、及び、第2のPLLによる逓倍値と第4の分周器の分周値との積に相当する値であり、リファレンスクロック109または119の周波数にこれらの値を乗じたものが、システム及び第1、第2のアプリケーションが必要とする第1、第2のMPU、メモリ制御ユニット、DACでのクロック周波数を示している。ここで、クロック周波数を示す値が0の場合、対応するアプリケーションが、そのクロック項目のMPU等を使用しないことを意味する。

【0025】また、総和値のパラメータ欄409の各クロック項目の値は、この値にリファレンスクロック109または119の周波数を乗じた値が、システム及び第1、第2のアプリケーションが同時に動作する場合の第1、第2のMPU、メモリ制御ユニット、DACでの必要なクロック周波数となることを示している。さらに、最大許容量のパラメータ欄410の各値は、この値にリファレンスクロック109または119の周波数を乗じた値が、第1、第2のMPU、メモリ制御ユニット、DACが動作可能な最大のクロック周波数を示すことになり、判定欄411には、テーブルの状態で第1、第2のMPU、メモリ制御ユニット、DACが動作可能か否か示される。

【0026】そして、図2により後述する処理が実行され新たに第3のアプリケーションが追加して起動されると、図5に示すように、図4のテーブルに第3のアプリケーションに対するパラメータ欄501が設けられると共に、総和値のパラメータ欄409がアプリケーションの追加により変更され、パラメータ欄502に変更される。また、図3により後述する処理が実行され第2のアプリケーション終了されると、図6に示すように、図5に示すテーブルから第2のアプリケーションに対するパ

ラメータ欄４０８が削除されると共に、総和値のパラメータ欄がパラメータ欄６０１のように変更される。

【００２７】なお、第１、第２のアプリケーションが必要とする第１、第２のＭＰＵ、メモリ制御ユニット、ＤＡＣでのクロック周波数を決める値は、各アプリケーションが、その内部にそれぞれ有している。

【００２８】まず、図２に示すフローを参照して、本発明の実施形態において、アプリケーションプログラムを新たに追加して起動させる場合に使用するプログラムの処理動作を説明する。

【００２９】（１）この処理プログラムは、ユーザ等によりプログラムの起動要求が発生した場合にスタートし、まず、新たに起動するアプリケーション用にアプリケーション番号を取得する（ステップ２０１）。

【００３０】（２）次に、２０２で外部メモリ１０４に格納されている図４に示すクロックテーブルに新しい欄を作成し、新アプリケーション番号及びアプリケーションが持つ固有のパラメータ４０２、４０３、４０４、４０５を格納してクロックテーブルを更新する。図５に示すパラメータ欄５０１が新たに作成された新アプリケーション用の欄である（ステップ２０２）。

【００３１】（３）ステップ２０２で更新されたクロックテーブルについて、パラメータ４０２～４０５の各パラメータの総和を求め、総和値のパラメータ欄４０９を更新してパラメータ欄５０２とする（ステップ２０３）。

【００３２】（４）ステップ２０３の処理で更新したパラメータ欄５０２の各パラメータの全てが最大許容量欄４１０内の値を超えていないか否かを判定し、１つでも超えている場合、ステップ２０２で作成したクロックテーブルの新しい欄５０１を削除し、パラメータ値の総和の欄４０９を元の値に戻してここでの処理を終了する。この場合、起動要求があったアプリケーションは、現システム状態では動作が不可能と判定し起動しない（ステップ２０４、２０５）。

【００３３】（５）ステップ２０４の判定で、更新したパラメータ欄５０２の各パラメータの全てが最大許容量欄４１０内の値を超えていなかった場合、新たな各パラメータ総和値をテーブルに格納して、総和値パラメータ５０２に更新する（ステップ２０６）。

【００３４】（６）次に、ステップ２０６で更新された各パラメータの総和値に基づいて、各ＰＬＬ、分周器に対するコントロールレジスタの値を変更し、各ローカルクロック１１２、１１４、１１６、１２１の周波数を設定する。この後、新しいアプリケーション本体を起動する（ステップ２０７、２０８）。

【００３５】前述した処理の例は、２つのアプリケーションが動作している状態で、クロックテーブルが図４に示すような状態の場合に、もう１つのアプリケーションを追加して起動するとして説明したが、前述の説明から判るように、システムの立ち上げ時におけるクロックテーブルは、システムのパラメータ欄４０６、総和値のパラメータ欄４０９、最大許容量のパラメータ欄４１０、各パラメータの判定欄４１１だけが設けられる構成であり、アプリケーションが立ち上げられる度に、それらのアプリケーションに対応するパラメータ欄が追加されていく。

【００３６】次に、図３に示すフローを参照して、本発明の実施形態において、アプリケーションプログラムを終了させる場合に使用するプログラムの処理動作を説明する。ここでの処理は、図２により説明した処理の後に、第２のアプリケーションを終了させるものとした場合の例である。

【００３７】（１）この処理プログラムは、ユーザ等によって終了するアプリケーションが指定されると起動され、まず、終了するアプリケーションを使用し図５のクロックテーブルから該当するパラメータ欄を探し出し、次に、そのパラメータ欄をクロックテーブルから削除する（ステップ３０１、３０２）。

【００３８】（２）その後、パラメータ４０２～４０５の各パラメータの総和値を再計算して求め、総和値のパラメータ欄５０２を更新してパラメータ欄６０１とする（ステップ３０３）。

【００３９】（３）次に、指定されたアプリケーションプログラムを終了させ、各パラメータの総和値欄６０１から各ＰＬＬ、分周器に対するコントロールレジスタの値を更新し、各ローカルクロック１１２、１１４、１１６、１２１の周波数を所定の周波数に設定して処理を終了する（ステップ３０４、３０５）。

【００４０】前述した本発明の第１の実施形態によれば、各ＭＰＵ、ハードウェア機能ブロックを適正な動作周波数で動作することができるように設定することができ、かつ、システム全体の消費電力を押さえることが可能となる。

【００４１】図７は本発明の第２の実施形態による情報処理装置のハードウェア構成を示すブロック図、図８はストリームデータの処理を開始するときに使用するプログラムの処理動作を説明するフローチャート、図９は図８の処理でストリームデータの処理が開始された後のクロックテーブルの状態を説明する図であり、以下、これらの図を参照して本発明の第２の実施形態について説明する。図７において、７０１はストリームデータ入力ブロックであり、他の符号は図１の場合と同一である。

【００４２】図７に示す本発明の第２の実施形態は、図１に示す第１の実施形態による情報処理装置にストリームデータ入力ブロック７０１をシステムバス１０５に接続して加えて構成し、ストリームデータの処理を可能としたもので、その他の構成は、図１の場合と同一である。第２の実施形態で加えたストリームデータ入力ブロック７０１は、外部からのデジタル映像、音声等のデー

タ入力を随時受け付け、これをシステムバス１０５を経由して外部メモリ１０４に送付する処理を行うものである。

【００４３】外部からのデジタル映像、音声等のデータとしては、例えば、システム外部のデジタルＴＶチューナー、ラジオチューナ等が考えられる。これらのデータを以下ではストリームデータと呼ぶが、このようなストリームデータを処理する場合、発信側でストリームデータを作成したときに使用した形式に沿って処理を行う必要がある。これらの形式は、主にデータ量、発信側の都合等により選択されている。受信側を複数の形式に対応できるように構成した場合、このストリームがどの形式に対応するかを判定することができるように構成する必要がある。一般的に、この複数の形式は、形式毎に必要とする処理能力が異なる。

【００４４】本発明の第２の実施形態は、図８により説明する処理を実行するプログラムを使用することによって、ストリームの形式を変更する度に適切な動作周波数を設定することを可能としたものであり、次に、図８に示すフローを参照して、外部ストリームの処理が開始されたときの処理を説明する。この処理においても、図４により説明したクロックテーブルが使用されるものとし、また、このクロックテーブルの第１のアプリケーションに対するパラメータ欄が、この処理でのストリームデータ処理プログラムに相当するものとする。

【００４５】（１）この処理プログラムは、ストリームデータ処理プログラムと同時に起動され、まず、入力ストリーム形式が変更されたか否かの判定を行い、変更されていない場合、一定期間を置いて繰り返し判定を行う（ステップ８０１）。

【００４６】（２）ステップ８０１の判定で、入力ストリーム形式が変更されていた場合、該当アプリケーションの欄に新しい入力ストリーム形式のパラメータを格納する。この処理によって、図４の４０７に示した第１のアプリケーションのパラメータ欄は、図９に９０１として示すアプリケーション１ａのパラメータ欄のように変更してテーブルを更新する（ステップ８０２）。

【００４７】（３）次に、ステップ８０２で更新されたクロックテーブルについて、パラメータ４０２～４０５の各パラメータの総和を求め、総和値のパラメータ欄４０９を更新してパラメータ欄９０２とする（ステップ８０３）。

【００４８】（４）ステップ８０３の処理で更新したパラメータ欄９０２の各パラメータの全てが最大許容量欄４１０内の値を超えていないか否かを判定し、１つでも超えている場合、ステップ８０２で更新したクロックテーブルの更新した欄９０１を削除し、パラメータ値の総和の欄９０２の各パラメータの総和値をもう１度求め直して、クロックテーブル総和値の欄９０２を更新し、ここでの処理を終了する（ステップ８０４、８０５）。

【００４９】（５）ステップ８０４の判定で、全てのパラメータが最大許容量を超えていなかった場合、ステップ８０３で更新された総和値に基づいて、各ＰＬＬ、分周器に対するコントロールレジスタの値を変更し、各ローカルクロック１１２、１１４、１１６、１２１の周波数を所定の値に設定する。この後、新しいストリーム形式での処理動作を開始し、ステップ８０１からの処理に戻る（ステップ８０６、８０７）。

【００５０】前述した本発明の第２の実施形態によれば、第１の実施形態の効果に加え、さらに外部からの入力データのフォーマット変化に対応して動作周波数を変更することが可能となり、システム全体の消費電力を押さえることができる。

【００５１】図１０は本発明の第３の実施形態による情報処理装置のハードウェア構成を示すブロック図、図１１は電源電圧が変動したときに動作周波数を変更するために使用するプログラムの処理動作を説明するフローチャート、図１２は図１１の処理で動作周波数が変更された後のクロックテーブルの状態を説明する図であり、以下、これらの図を参照して本発明の第３の実施形態について説明する。図１０において、１００１はバッテリ、１００２は電圧計、１００３は電源モニタレジスタ、１００４は電圧保存レジスタであり、他の符号は図１の場合と同一である。

【００５２】図１０に示す本発明の第３の実施形態は、電源電圧が低下したときに処理装置全体の動作周波数を低下させて消費電力の低減を図ることを可能にしたもので、バッテリ１００１の電圧を測定する電圧計１００２と、電圧計１００２でのバッテリの測定電圧をモニタしてその信号をシステムバス１０５を介してシステムに与える電源モニタレジスタと、前回のクロックテーブルの更新時におけるバッテリの電圧値を保存している電圧保存レジスタ１００４とが、図１により説明した本発明の第１の実施形態に加えられて構成されており、その他の構成は、図１の場合と同一である。

【００５３】通常、バッテリ１００１は、電力を消費していくと、電圧が低下していく。電圧計１００２は、この電圧の低下を検知し、電源モニタレジスタ１００３に随時反映する。このレジスタ１００３は、システムバス１０５を経由し、第１、第２のＭＰＵ１０１、１０２から参照可能である。

【００５４】次に、図１１に示すフローを参照して、電源電圧が変動したときに動作周波数を変更する処理について説明する。なお、この処理においても、図４により説明したクロックテーブルが参照される。また、電圧保存レジスタ１００４には、前回のクロックテーブルの更新時、すなわち、クロックテーブルが図４に示す状態とされたときのバッテリの電圧値が保存されている。

【００５５】（１）この処理プログラムは、システムの起動時に起動され、起動されると、まず、電圧モニタレ

ジスタ１００３の値を読み出し、電圧モニタレジスタの値が更新されたか否かを判定する。電圧モニタレジスタ１００３には、バッテリ１００１の電圧変化が常時反映されていて、変化がない場合、一定間隔で更新されたか否かの判定を続ける（ステップ１１０１、１１０２）。

【００５６】（２）ステップ１１０２での判定で、電圧モニタレジスタの値が更新されていた場合、前回のクロックテーブルの更新時のバッテリの電圧値を保存している電圧保存レジスタ１００４の値と、更新されている電圧モニタレジスタの値とを比較し、電圧モニタレジスタの値が電圧保存レジスタの値より一定以上大きいか否かを判定する（ステップ１１０３）。

【００５７】（３）ステップ１１０３での判定で、電圧モニタレジスタの値が電圧保存レジスタの値より一定以上大きくなかった場合、電圧モニタレジスタの値が電圧保存レジスタの値より一定以上小さいか否かを判定し、一定以上小さくなかった場合、すなわち、差が一定値未満の場合、電圧の変化はクロックテーブルの設定値の変更を行うほど大きくなかったと判定し、何も変更せずに、ステップ１１０１からの処理に戻って処理を続ける（ステップ１１０７）。

【００５８】（４）ステップ１１０７での判定で、電圧モニタレジスタの値が電圧保存レジスタの値より一定以上小さかった場合、クロックテーブルの変更可能な各パラメータの値の２の商を求め、現在の値と置き換える。この結果、図４に示すクロックテーブルは、図１２に示すような状態となる。この場合、システムのパラメータ欄４０６の値、及び、ディスプレイのクロック項目４０５の値は変更不可能な値であり、第１、第２のアプリケーションのパラメータ欄の値が１２０１、１２０２に示すように変更され、最大許容量のパラメータ欄１２０４の値が２の商に変更され、総和値の欄１２０３が再計算されている（ステップ１１０８）。

【００５９】（５）この後、ステップ１１０８で再計算されたパラメータ値のうち、１つでも０があるか否かを判定し、ある場合、アプリケーションが必要としているＭＰＵのクロック項目の値の和が０、または、メモリ制御ブロックのクロック項目４０４の値が０であった場合、そのアプリケーションが動作不可能となったと判定して、そのアプリケーションを終了してここでの処理を終了する（ステップ１１０９、１１１０）。

【００６０】（６）ステップ１１０９の判定で値が０となったパラメータがなかった場合、ＰＬＬ、分周器に対するコントロールレジスタの値を更新してセットし、現在の電圧モニタレジスタの値を電圧保存レジスタ１００４に記憶し、その後、ステップ１１０１からの処理に戻って処理を続ける（ステップ１１１１）。

【００６１】（７）ステップ１１０３での判定で、電圧モニタレジスタの値が電圧保存レジスタの値より一定以上大きかった場合、電圧モニタレジスタの値が最大値となっているか否かを判定する（ステップ１１０４）。

【００６２】一般に、情報処理装置がバッテリ駆動されている場合、バッテリの電圧は、時間と共に低下していくので、前述までに説明したフローに従った処理が行われることになる。このため、ステップ１１０３での判定で、電圧モニタレジスタの値が電圧保存レジスタの値より一定以上大きかったという結果が得られる場合というのは、バッテリの交換が行われたとき、あるいは、バッテリが交流電源からフローティングされるようになったときである。

【００６３】（８）ステップ１１０４の判定で、電圧モニタレジスタの値が最大値となっていなかった場合、低下していた電圧の回復が図られたことになるので、クロックテーブル内の変更可能なパラメータ値を２倍にして現在値に置き換え、ステップ１１１１からの処理を続ける。この場合、前述したステップ１１０８の処理でパラメータ値が少なくとも１／２とされているので、ここでの処理で２倍としても問題を生じることはない（ステップ１１０６）。

【００６４】（９）ステップ１１０４の判定で、電圧モニタレジスタの値が最大値となっていた場合、クロックテーブルの各パラメータを初期値に戻し、ステップ１１１１からの処理を続ける（ステップ１１０５）。

【００６５】前述した本発明の第３の実施形態によれば、第１の実施形態の効果に加え、さらに外部電源の電圧変化に対して動作周波数を変更することが可能となり、システム全体の消費電力を押さえ、動作時間の延長を図ることができる。

【００６６】図１３は本発明の第４の実施形態による情報処理装置のハードウェア構成を示すブロック図、図１４は必要とされるクロック周波数により電源電圧を変更するプログラムの処理動作を説明するフローチャート、図１５は図１４の処理で使用するクロック－電圧テーブルの構成を説明する図であり、以下、これらの図を参照して本発明の第４の実施形態について説明する。図１３において、１３０１はＤＣ－ＤＣコンバータ、１３０２は電圧設定レジスタであり、他の符号は図１の場合と同一である。

【００６７】図１３に示す本発明の第４の実施形態は、前述までに説明したクロックテーブル内の総和値のパラメータ欄の値に基づいて処理装置を構成する各ブロックに供給する電圧を変更することにより、処理装置の消費電力の低減を図ることを可能にしたもので、図１により説明した本発明の第１の実施形態に、ＤＣ－ＤＣコンバータ１３０１と、電圧設定レジスタ１３０２とを設けて構成されている。ＤＣ－ＤＣコンバータ１３０１は、電圧設定レジスタ１３０２の設定値を使用して電源電圧を決定し、図１３に示している全ブロックへこの電圧を持つ電源を供給している。電圧設定レジスタ１３０２は、システムバス１０５を介して第１、第２のＭＰＵ１０

１、１０２からアクセスが可能とされ、これらのＭＰＵから制御可能とされている。

【００６８】次に、図１４に示すフローを参照して、必要とされるクロック周波数により電源電圧を変更するプログラムの処理動作を説明する。この処理では、図１５に示すクロック－電圧テーブルを使用する。図１５において、１５０１はクロックテーブル内の総和値のパラメータ欄内の最大値、１５０２は対応する電圧設定レジスタ値である。

【００６９】（１）この処理プログラムは、システムの起動時に起動され、起動されると、まず、図４により説明したクロックテーブルが更新されたか否かを判定し、更新が行われるまで、クロックテーブルが更新されたか否かの判定を繰り返す（ステップ１４０１）。

【００７０】（２）その後、クロックテーブル内の総和値のパラメータ欄４０９の中から最大値を選択する。このパラメータ欄４０９の中での最大値は１６であり、次に、図１５に示すクロック－電圧テーブルから前記最大値に対する電圧値を求める。この場合、図１５で最大値１６を超える総和値最大値１５０１の最小値が２０となっているので、これに対応する電圧設定レジスタ値１５０２から得られる電圧レジスタ設定値は１９となる（ステップ１４０２、１４０３）。

【００７１】（３）次に、ステップ１４０３で得た値が現在の電圧レジスタ設定値と同一であるか否かを判定し、同一の場合、ステップ１４０１の処理に戻って前述した処理を繰り返し、また、異なる場合、電圧設定レジスタに新しい値をセットする（ステップ１４０５）。

【００７２】前述した本発明の第４の実施形態によれば、第１の実施形態の効果に加え、さらに動作周波数にあわせて電源電圧を変更することが可能となり、更なるシステム全体の消費電力を押さえることができる。

【００７３】前述までに本発明の第１～第４の実施形態について説明したが、本発明は、これらの第１～第４の実施形態の複数を組み合わせて構成することもできる。

【００７４】

【発明の効果】以上説明したように本発明によれば、動作するアプリケーションに対して充分な処理能力を実現でき、最小の消費電力で動作できるように、ＭＰＵ等の機能ブロックを適正な周波数、作動電圧によって動作させることができ、情報処理装置の低消費電力化を図ることができる。

【図面の簡単な説明】

【図１】本発明の第１の実施形態による情報処理装置のハードウェア構成を示すブロック図である。

【図２】アプリケーションプログラムの追加して起動したときに使用するプログラムの処理動作を説明するフローチャートである。

【図３】アプリケーションプログラム終了時に使用するプログラムの処理動作を説明するフローチャートである。

【図４】図２の処理で使用するクロックテーブルについて説明する図である。

【図５】図２の処理でアプリケーションが追加起動された後のクロックテーブルの状態を説明する図である。

【図６】図３処理でアプリケーションが終了させられた後のクロックテーブルの状態を説明する図である。

【図７】本発明の第２の実施形態による情報処理装置のハードウェア構成を示すブロック図である。

【図８】ストリームデータの処理を開始するときに使用するプログラムの処理動作を説明するフローチャートである。

【図９】図８の処理でストリームデータの処理が開始された後のクロックテーブルの状態を説明する図である。

【図１０】本発明の第３の実施形態による情報処理装置のハードウェア構成を示すブロック図である。

【図１１】電源電圧が変動したときに動作周波数を変更するために使用するプログラムの処理動作を説明するフローチャートである。

【図１２】図１１の処理で動作周波数が変更された後のクロックテーブルの状態を説明する図である。

【図１３】本発明の第４の実施形態による情報処理装置のハードウェア構成を示すブロック図である。

【図１４】必要とされるクロック周波数により電源電圧を変更するプログラムの処理動作を説明するフローチャートである。

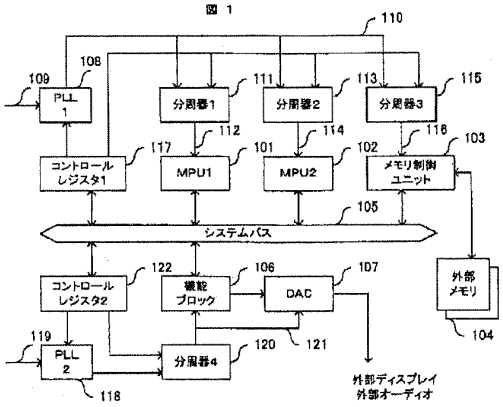
【図１５】図１４の処理で使用するクロック－電圧テーブルの構成を説明する図である。

【符号の説明】

１０１、１０２　第１、第２のマイクロプロセッサユニット（ＭＰＵ）
１０３　外部メモリ制御ユニット
１０４　外部メモリ
１０５　システムバス
１０６　機能ブロック
１０７　デジタル－アナログコンバータ（ＤＡＣ）
１０８、１１８　第１、第２のフェイズロックドループ（ＰＬＬ）
１１１、１１３、１１５、１２０　第１～第４の分周器
１１７、１２２　第１、第２のコントロールレジスタ
７０１　ストリームデータ入力ブロック
１００１　バッテリ
１００２　電圧計
１００３　電源モニタレジスタ
１００４　電圧保存レジスタ
１３０１　ＤＣ－ＤＣコンバータ
１３０２　電圧設定レジスタ

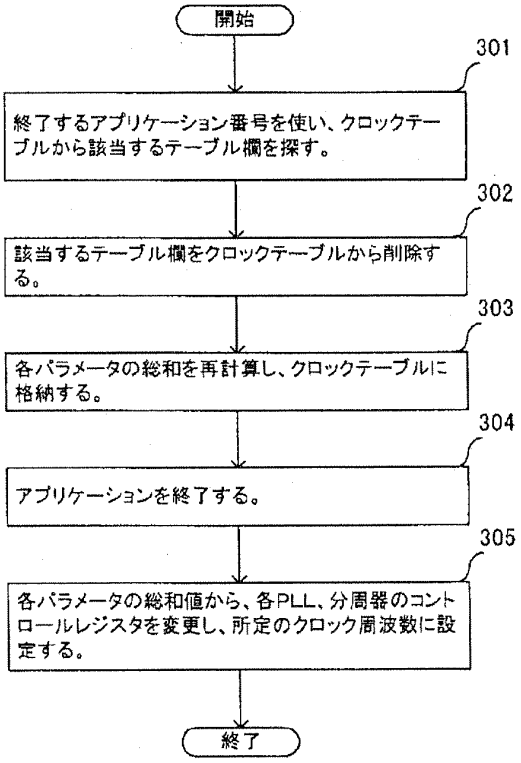
【図1】

図 1



【図3】

図 3



【図4】

図 4

	401 アプリケーション番号	402 MPU 1	403 MPU 2	404 メモリ	405 DAC
406	0(システム)	1	1	1	–
407	1	5	15	5	15
408	2	7	0	2	–
409	総和値	13	16	8	15
410	最大許容量	20	20	10	15
411	判定	可能	可能	可能	可能

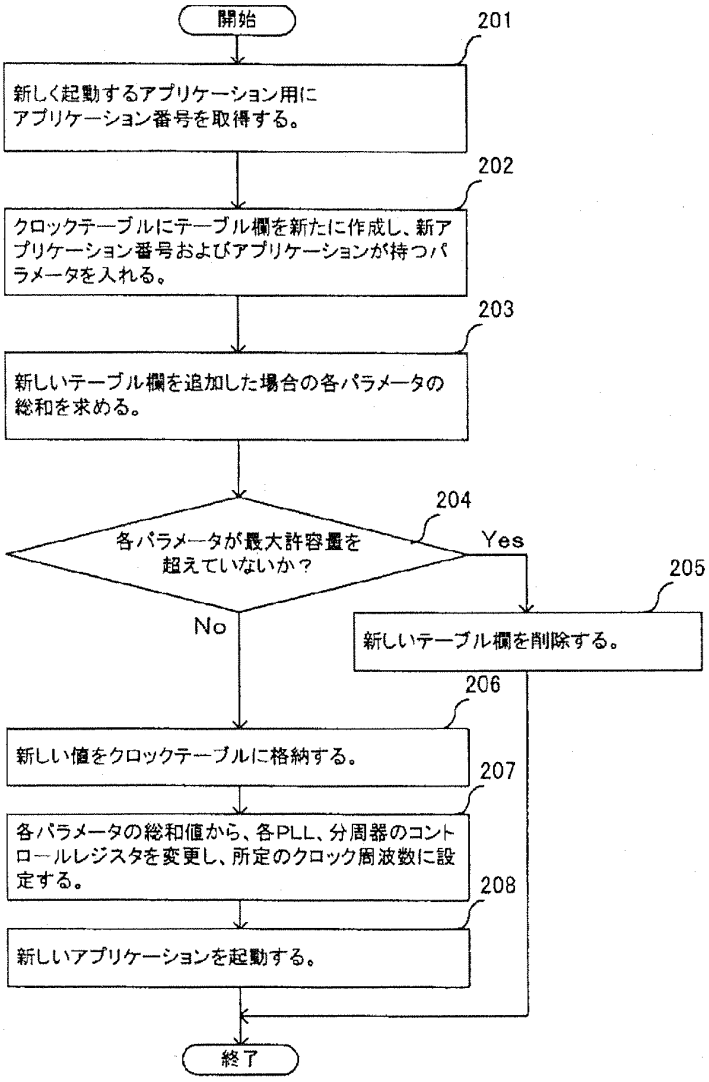
【図5】

図 5

	401 アプリケーション番号	402 MPU 1	403 MPU 2	404 メモリ	405 ディスプレイ
406	0(システム)	1	1	1	–
407	1	5	15	5	15
408	2	7	0	2	–
501	3	3	1	1	–
502	総和値	16	17	9	15
410	最大許容量	20	20	10	15
411	判定	可能	可能	可能	可能

【図2】

図 2



【図15】

図 15

1501	総和値最大値	10	15	20	15
1502	電圧設定レジスタ値	16	18	19	20

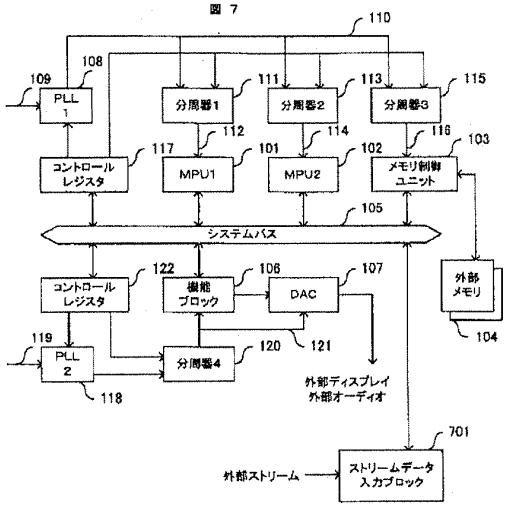
【図6】

図 6

	401 アプリケーション番号	402 MPU 1	403 MPU 2	404 メモリ	405 ディスプレイ
406	0(システム)	1	1	1	−
407	1	5	15	5	15
501	3	3	1	1	−
601	総和値	9	17	7	15
410	最大許容量	20	20	10	15
411	判定	可能	可能	可能	可能

【図7】

図 7



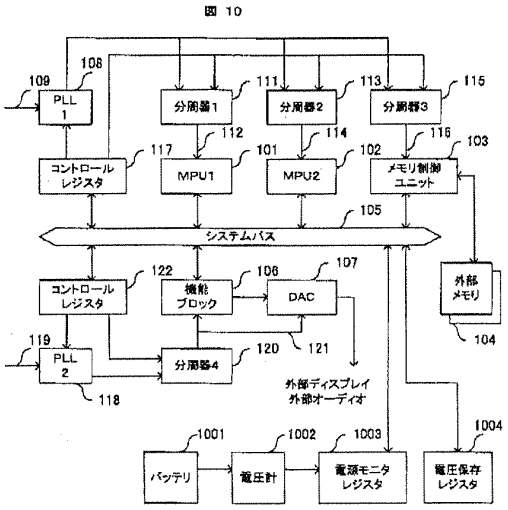
【図9】

図 9

	401 アプリケーション番号	402 MPU 1	403 MPU 2	404 メモリ	405 ディスプレイ
406	0(システム)	1	1	1	−
901	1a	5	10	2	8
408	2	7	0	2	−
902	トータル	13	11	5	8
410	最大許容量	20	20	10	15
411	判定	可能	可能	可能	可能

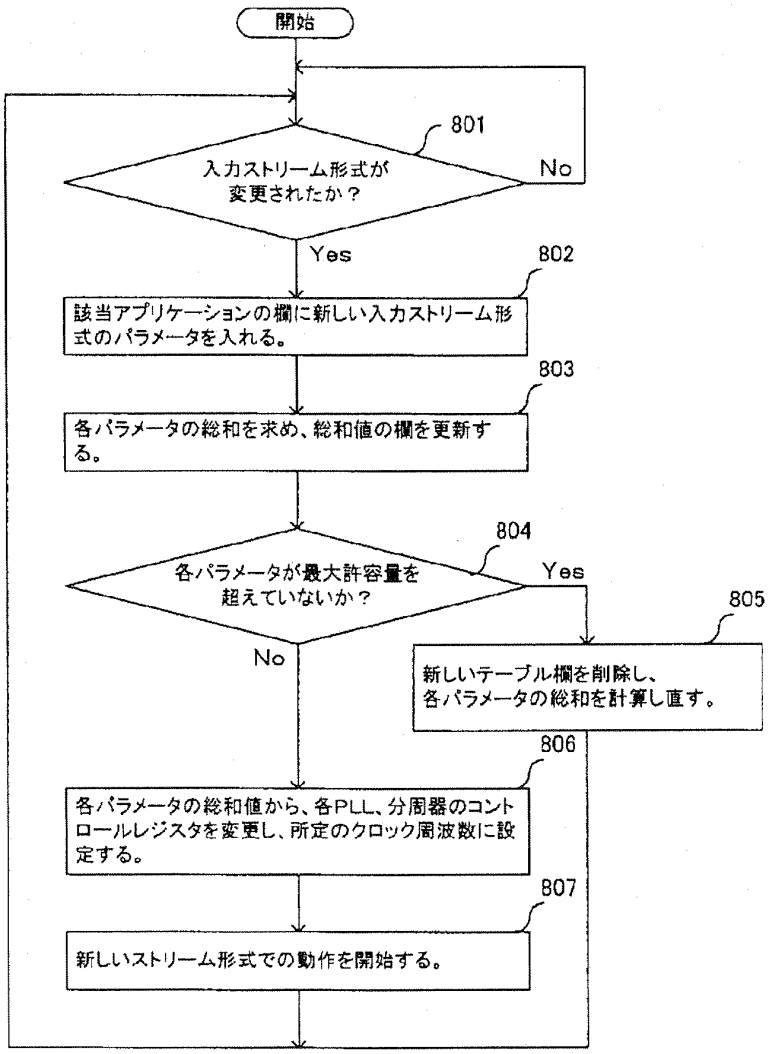
【図10】

図 10



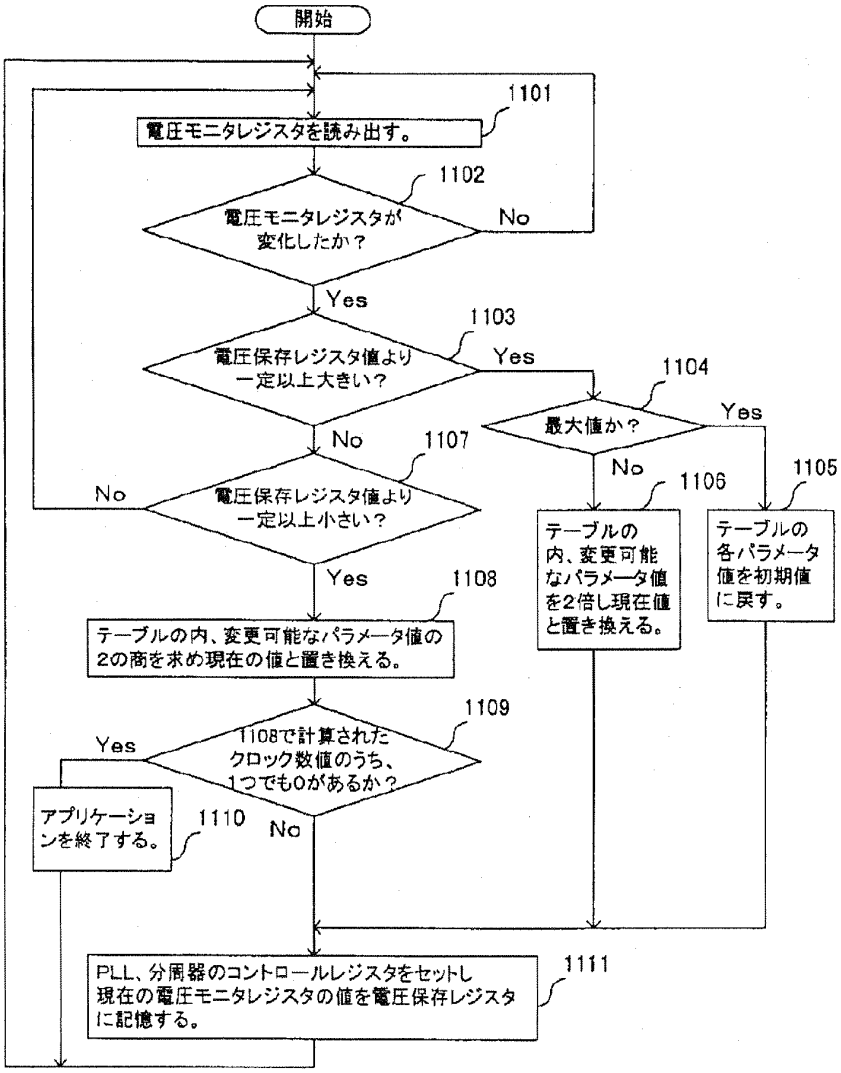
【図8】

図 8


開始
801
入力ストリーム形式が
変更されたか？
No
Yes
802
該当アプリケーションの欄に新しい入力ストリーム形式のパラメータを入れる。
803
各パラメータの総和を求め、総和値の欄を更新する。
804
各パラメータが最大許容量を
超えていないか？
Yes
No
805
新しいテーブル欄を削除し、
各パラメータの総和を計算し直す。
806
各パラメータの総和値から、各PLL、分周器のコントロールレジスタを変更し、所定のクロック周波数に設定する。
807
新しいストリーム形式での動作を開始する。

【図11】

図 11


開始
1101
電圧モニタレジスタを読み出す。
1102
電圧モニタレジスタが変化したか？
No
Yes
1103
電圧保存レジスタ値より一定以上大きい？
Yes
1104
最大値か？
Yes
No
1105
テーブルの各パラメータ値を初期値に戻す。
1106
テーブルの内、変更可能なパラメータ値を2倍し現在値と置き換える。
No
1107
電圧保存レジスタ値より一定以上小さい？
No
Yes
1108
テーブルの内、変更可能なパラメータ値の2の商を求め現在の値と置き換える。
1109
1108で計算されたクロック数値のうち、1つでも0があるか？
Yes
No
1110
アプリケーションを終了する。
1111
PLL、分周器のコントロールレジスタをセットし現在の電圧モニタレジスタの値を電圧保存レジスタに記憶する。

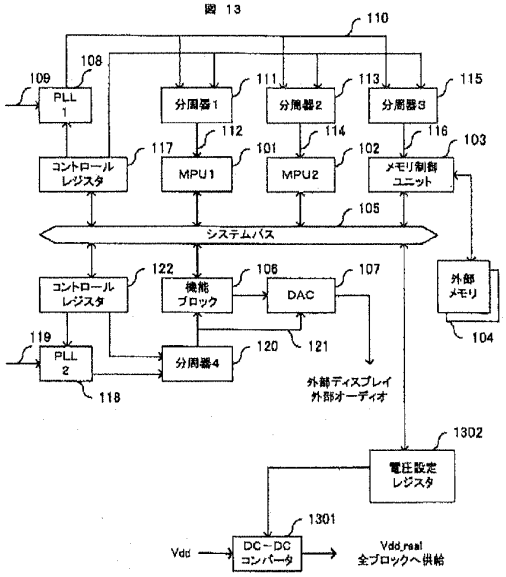
【図１２】

図 12

401 アプリケーション番号	402 MPU 1	403 MPU 2	404 メモリ	405 ディスプレイ
406 0(システム)	1	1	1	—
1201 1	2	7	2	15
1202 2	3	0	1	—
1203 トータル	6	8	4	15
1204 最大許容量	10	10	5	15
411 判定	可能	可能	可能	可能

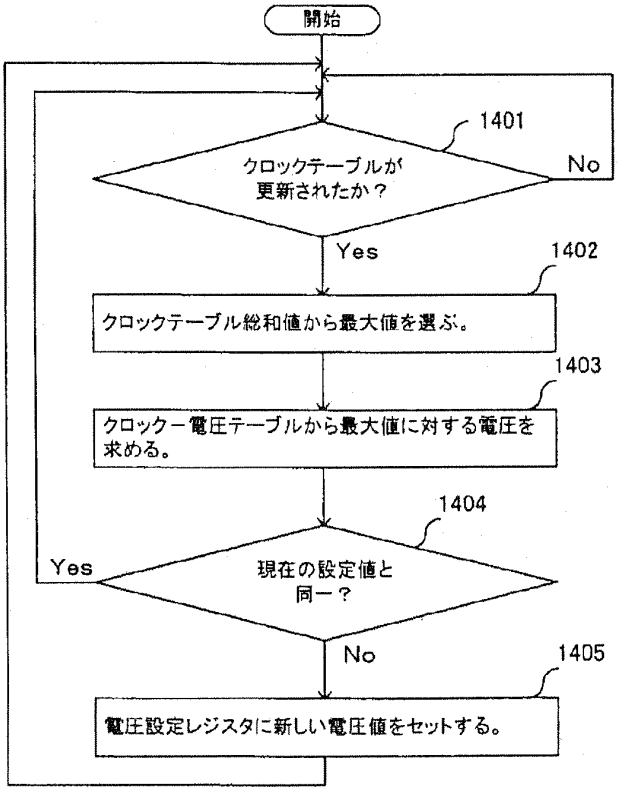
【図１３】

図 13



【図１４】

図 14



フロントページの続き

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Ｆターム(参考)　5B011 DA06 FF02 GG02 LL02 LL13
5B079 BA01 BC01

Translation of Japanese Patent Application Publication No.2003-108260

[Name of Invention] INFORMATION PROCESSING APPARATUS AND METHOD FOR CONTROLLING THE SAME

[Summary]

[Purpose]

To allow an operating frequency and an operating voltage to be changed so as to enable an operation with the minimum possible power consumption to achieve enough processing capacity to perform an application.

[Structure]

Frequency dividers 111, 113, 115 and 120 whose frequency-division ratios are individually controlled with respect to MPUs 101 and 102, a memory control unit 103, and a functional block 106 are provided to change operating frequencies of these elements.

An application on an information processing apparatus prepares information on operating frequencies optimal for each of the MPUs and functional block. A managing unit for managing this information for a plurality of applications is prepared. The current operating state is acquired from the managing unit when an application is started and a processing capacity needed for the started application is allocated to each of the MPUs and the functional block, thereby the operating frequencies of those are changed. The same operation is performed when ending the application.

[Scope of Claim]

[Claim 1]

An information processing apparatus including one or both of at least one processor and at least one functional block having a dedicated logic, said information processing apparatus comprising:

a changing unit configured to individually change respective operating frequencies of the processor and the functional block; and

a control unit configured to determine the operating frequencies of the processor and the functional block based on operating frequency information optimal for each of the processor and the functional block and control the changing unit, each of at least one application operating on the information processing apparatus having said operating frequency information.

[Claim 2]

The information processing apparatus as claimed in claim 1, wherein the control unit acquires an operating state from a managing unit which manages a current operating state of the information processing apparatus, allocates a processing capacity needed for an application to be started to the processor and the functional block, and changes the operating frequencies of the processor and the functional block.

[Claim 3]

The information processing apparatus as claimed in claim 1, wherein the control unit acquires an operating state from a managing unit which manages a current operating state of the information processing apparatus, deletes a processing capacity allocated to an application to be ended from the processor and the functional block, and changes the operating frequencies of the processor and the functional block.

[Claim 4]

The information processing apparatus as claimed in claim 1, 2, or 3, further comprising a main power source such as a battery and a measuring unit configured to measure a power source voltage of the main power source, wherein the control unit sets the operating frequencies of the processor and the functional block at frequencies at

which the processor and the functional block can operate with the power source voltage measured by the measuring unit.

[Claim 5]

The information processing apparatus as claimed in any one of claims 1 through 4, further comprising a unit configured to receive externally inputted formatted data, wherein the control unit sets the operating frequencies of the processor and the functional block, in accordance with a data format of the inputted data, at operating frequencies suitable for the data format.

[Claim 6]

The information processing apparatus as claimed in any one of claims 1 through 5, further comprising a changing unit configured to change a power source voltage, wherein the control unit controls the changing unit so that a voltage with which the processor and the functional block can operate at a sum of operating frequencies required by at least one currently operating application is applied to the processor and the functional block.

[Claim 7]

A method for controlling an information processing apparatus having one or both of at least one processor and at least one functional block having a dedicated logic, said method comprising:

determining operating frequencies of the processor and the functional block based on operating frequency information optimal for each of the processor and the functional block, each of at least one application operating on the information processing apparatus having said operating frequency information; and

individually changing the respective operating frequencies of the processor and

the functional block.

[Detailed Description of the Invention]

[0001]

[Field of Industrial Application]

The present invention relates to an information processing apparatus and a method for controlling the information processing apparatus. In particular, the present invention relates to an information processing apparatus capable of changing an operating frequency and a method for controlling the information processing apparatus.

[0002]

[Prior Art]

In recent years, processes using a processor and dedicated hardware have been performed in the field of signal processing, media processing, and the like. These processes manage a large amount of operations and require a real-time property, that is, the processes must be ended within a specified time. Therefore, an information processing apparatus which performs these processes is demanded to have quite a high processing performance and a high operating frequency to achieve the high processing performance.

[0003]

In general, in a semiconductor circuit formed of a CMOS transistor, such as a processor, power consumption increases in proportion to its operating frequency. Since this power consumption becomes a bottleneck in constituting an information processing apparatus, various methods have been suggested to reduce the power consumption.

[0004]

For example, as a conventional technique capable of reducing a power consumption of a multiprocessor system and the like, a technique disclosed in Japanese

Patent Application Publication No.8-202468 has been known. By this conventional technique, in a system having a multiprocessor configuration, a processing state of each processor is detected and an unused or lightly-loaded processor is switched to a low power consumption mode to suppress the total power consumption.

[0005]

In addition, as a conventional technique for a terminal, for example, there has been known a technique disclosed in Japanese Patent Application Publication No.2000-66776. This conventional technique relates to a method for controlling a power consumption of a sub-circuit of a system. By this technique, an operating frequency suitable for a load allocated to a processor is calculated, a power source voltage required for the processor to operate at the calculated frequency is detected, and the power source voltage is applied to the processor so that the processor is operated with a minimum possible power required to process the load.

[0006]

As described above, there have conventionally been the attempts to reduce the total power consumption in order to constitute a large scale information processing apparatus such as a multiprocessor system.

[0007]

On the other hand, an integration degree of a semiconductor circuit has been increasing year by year. As a result, an information processing apparatus that has conventionally been constituted by plural components can now be integrated in one semiconductor circuit. Consequently, a smaller information processing apparatus can be developed, which has been applied to various small devices. In particular, by using a battery and the like as a power supply source, a portable information processing apparatus can be formed. Conventionally, when a semiconductor circuit is used for such an application, such a semiconductor circuit that has maximum power consumption matching the capacity of the power supply source has been developed or

selected. However, it is difficult by this method to form an information processing apparatus that performs a highly-loaded process such as the media process described above.

[0008]

[Problems to be Solved by the Invention]

As described above, while the increase in processing capacity of an information processing apparatus is demanded, saving of more power by a battery operation and the like is demanded. Accordingly, to achieve these two demands, an information processing apparatus is demanded to have a processing capacity that is high enough for applications to be processed by the information processing apparatus; and to operate with minimum possible power consumption to achieve the processing capacity.

[0009]

However, the information processing apparatus by the above-described conventional technique has a problem in that it cannot satisfy the above-described two demands simultaneously and sufficiently.

[0010]

A purpose of the present invention is to provide an information processing apparatus which has a high processing capacity enough to change an operating frequency and an operating voltage so as to enable an operation with a minimum possible power consumption to achieve a sufficient processing capacity for applications and which consumes less power, and to provide a method for controlling the information processing apparatus.

[0011]

[Means for Solving the Problems]

According to the present invention, the above-described purpose can be achieved by an information processing apparatus including one or both of at least one processor and at least one functional block having a dedicated logic, which information

processing apparatus having a changing unit configured to individually change respective operating frequencies of the processor and the functional block; and a control unit configured to determine the operating frequencies of the processor and the functional block based on operating frequency information optimal for each of the processor and the functional block and control the changing unit, each of at least one application operating on the information processing apparatus having said operating frequency information.

[0012]

The purpose can be achieved by a method for controlling an information processing apparatus having one or both of at least one processor and at least one functional block having a dedicated logic, which method having the steps of determining operating frequencies of the processor and the functional block based on operating frequency information optimal for each of the processor and the functional block, each of at least one application operating on the information processing apparatus having said operating frequency information, and individually changing the respective operating frequencies of the processor and the functional block.

[0013]

[Embodiments]

Embodiments of an information processing apparatus of the present invention are described in detail below with reference to drawings.

[0014]

Fig. 1 is a block diagram showing a hardware configuration of an information processing apparatus according to a first embodiment of the present invention. Fig. 2 is a flowchart describing a processing operation of a program used when an application program is added and launched. Fig. 3 is a flowchart describing a processing operation of a program used when an application program is ended. Fig. 4 is a

diagram describing a clock table used in the process shown in Fig. 2. Fig. 5 is a diagram describing a state of a clock table after the application is added and launched in the process shown in Fig. 2. Fig. 6 is a diagram describing a state of the clock table after the application is ended in the process shown in Fig. 3. The first embodiment of the present invention is described below with reference to these drawings.

[0015]

In Fig. 1, reference numerals 101 and 102 denote first and second microprocessor units (hereinafter called MPUs), respectively; 103 denotes an external memory control unit; 104 denotes an external memory; 105 denotes a system bus; 106 denotes a functional block; 107 denotes a digital-analog converter (hereinafter called a DAC); 108 and 118 denote first and second phase locked loops (hereinafter called PLLs), respectively; 109 and 119 denote first and second PLL reference clocks, respectively; 110 denotes a first PLL oscillation clock; 111, 113, 115, and 120 denote first to fourth frequency dividers, respectively; 112 and 114 denote local clocks for the first and second MPUs, respectively; 116 denotes a local clock for the memory control unit; 117 and 122 denote first and second control registers, respectively; and 121 denotes a local clock for the functional block and DAC.

[0016]

In the first embodiment of the present invention shown in Fig. 1, the first PLL 108 multiplies the reference clock 109 based on a value of the first control register 117 to form an oscillation clock 110. The oscillation clock 110 is used for generating the local clocks 112, 114, and 116 for driving the first MPU 101, second MPU 102, and memory control unit 103 through the first to third frequency dividers 111, 113, and 115. Each of the frequency dividers 111, 113, and 115 is individually controlled based on a value from the first control register 117 to divide the oscillation clock 110 to be reduced in frequency to 1/n. By providing the frequency dividers 111, 113, and 115 for each unit of the first MPU 101, second MPU 102, and memory control unit 103, each unit

can receive an operating frequency that is set 1/n (a value of n may differ depending on the frequency dividers) times as high as a frequency required by the oscillation clock 110. Thus, each unit can operate at a required frequency.

[0017]

The first and second MPUs 101 and 102 read in a program and data from the external memory 104 and carry out an operation. In addition, the first and second MPUs 101 and 102 can control the functional block 106, first and second control registers 117, 122 through the system bus 105. The memory control unit 103, receiving a request from the first and second MPUs 101 and 102 and the functional block 106 through the system bus 105, reads and writes data by controlling the external memory 104 and sends a result back to the source of request as required. The system bus 105 transmits a request from a source to a destination of the request and sends a result back from the destination to the source of the request with respect to all the units connected to the system bus 105.

[0018]

In this embodiment of the present invention, for convenience, all the parts that control the system bus 105 in the system bus 105 and the units (101, 102, 103, 106, 117, and 122) connected to the system bus 105 are operated by the local clock 116 for the memory control unit 103. However, in the present invention, the system bus 105 may be operated by a local clock of another unit or operated by newly forming a local clock dedicated for the system bus.

[0019]

The second PLL 118 performs an operation similar to the first PLL 108. That is, the second PLL 118 uses a value of the second control register 112 to multiply the reference clock 119 and outputs the clock to the fourth frequency divider 120. The fourth frequency divider 120 divides the clock multiplied using the value of the second control register 122 to form the local clock 121 and supplies the local clock 121 to the

functional block 106 and DAC 107. The functional block 106 is constituted by a dedicated logic specialized for a process to perform a calculation that the first and second MPUs 101 and 102 cannot manage to process. The functional block 106 is controlled by the first or second MPU 101 or 102 and performs a filtering process of a digital video image and a digital audio, an encryption process that cannot be implemented by software to prevent tampering, and the like.

[0020]

In the above-described first embodiment of the present invention, the first and second MPUs 101 and 102 operate programs described below and the control registers 117 and 122 are controlled to change the operating frequencies of the first and second MPUs 101 and 102, memory control unit 103, and functional block 106, thereby to suppress the power consumption of the entire system.

[0021]

In the example of the above-described information processing apparatus shown in Fig. 1, two MPUs and one functional block are provided. However, there may be one or a plurality of each of the MPUs and functional blocks. Further, either of the MPU and functional block may be provided as well.

[0022]

Next, operations of the programs used by the first and second MPUs 101 and 102 are described with reference to Figs. 2 and 3. These programs are stored in the external memory 104 shown in Fig. 1 and read by the MPUs to be processed as required. These programs use a clock table shown in Figs. 4 to 6 described below. The table is also stored in the external memory 104 and read by the MPUs to be processed as required.

[0023]

The clock table shown in Fig. 4 has an application number item 401; a clock item 402 of the first MPU; a clock item 403 of the second MPU; a clock item 404 of the

memory control block; and a clock item 405 of the functional block, DAC, and display; as parameters. These are stored in a parameter section 406 of a system, a parameter section 407 of a first application, a parameter section 408 of a second application, a parameter section 409 of a sum value, and a parameter section 410 of a maximum allowable value. In this table, a determination section 411 of each parameter is also provided.

[0024]

Values of the clock items 402 to 405 in the parameter sections 406 to 408 are values indicating the ratios of the reference clock 109 or 119 and the local clocks 112, 114, 116, and 121 shown in Fig. 1, that is, values corresponding to products of the multiple value by the first PLL and dividing values of the first to third frequency dividers, and a value corresponding to a product of the multiple value by the second PLL and a dividing value of the fourth frequency divider. The reference clock 109 or 119 multiplied by these values indicate clock frequencies of the first and second MPUs, memory control unit, and DAC required by the system and first and second applications. Here, when the value indicating the clock frequency is 0, it means that a corresponding application does not use a MPU and the like of that clock item.

[0025]

A value of each clock item in the parameter section 409 of the sum value indicates that a value obtained by multiplying this value with the frequency of the reference clock 109 or 119 serves as a clock frequency required by the first and second MPUs, memory control unit, and DAC in the case where the system and first and second applications operate at the same time. Further, a value obtained by multiplying each value of the parameter section 410 of the maximum allowable value with the frequency of the reference clock 109 or 119 indicates a maximum clock frequency at which the first and second MPUs, memory control unit, and DAC can operate. The determination section 411 shows whether the first and second MPUs, memory control

unit, and DAC can operate or not in the state shown in the table.

[0026]

After a third application is added and launched by the execution of the process described below with reference to Fig. 2, a parameter section 501 for the third application is provided in the table shown in Fig. 4, as shown in Fig. 5. At the same time, the parameter 409 of the sum value is changed to a parameter section 502 by the addition of the application. After the second application is ended by the execution of the process described below with reference to Fig. 3, the parameter section 408 for the second application is deleted from the table shown in Fig. 5 and the parameter section of the sum value is changed to a parameter section 601 as shown in Fig. 6.

[0027]

Note that values that determine clock frequencies of the first and second MPUs, memory control unit, and DAC required by the first and second applications are included in each application.

[0028]

First, with reference to the flow shown in Fig. 2, a processing operation of a program used when an application program is newly added and launched is described in the embodiment of the present invention.

[0029]

(1) This processing program starts when there is a request to launch a program by a user and the like. First, the processing program acquires an application number for the application to be newly launched (step 201).

[0030]

(2) Next, in step 202, a new section is formed in the clock table shown in Fig. 4 stored in the external memory 104, and a new application number and unique parameters 402, 403, 404, and 405 that the application has are stored to update the clock table. The parameter section 501 shown in Fig. 5 is a newly formed section for the

new application (step 202).

[0031]

(3) In the clock table updated in step 202, a sum of each of the parameters 402 to 405 is calculated and the parameter section 409 of the sum value is updated to a parameter section 502 (step 203).

[0032]

(4) A determination is performed as to whether none of the parameters in the parameter section 502 updated in the process of step 203 exceed the values in the maximum allowable value section 410. If even one parameter exceeds the maximum allowable value, the new section 501 in the clock table formed in step 202 is deleted and the section 409 of the sum value of the parameter values is returned to the original values. Then, the process here is ended. In this case, the application which was requested to be launched is determined inoperable in the current system state and thus is not launched (steps 204, 205).

[0033]

(5) In the case where none of the parameters in the parameter section 502 exceed the values in the maximum allowable value section 410 in the determination of step 204, the new sum value of each parameter is stored in the table and updated to the sum value parameter 502 (step 206).

[0034]

(6) Next, values of the control registers for each of the PLLs and frequency dividers are changed on the basis of the sum value of each parameter updated in step 206 to set a frequency of each of the local clocks 112, 114, 116, and 121. After that, a new application body is launched (steps 207, 208).

[0035]

In the above-described example of the process, one more application is added and launched in the state where the two applications operate and the clock table is in the

state as shown in Fig. 4. However, as is clear from the above description, only the parameter section 406 of the system, the parameter section 409 of the sum value, the parameter section 410 of the maximum allowable value, and the determination section 411 of each parameter are provided in the clock table at the time of starting up the system. Every time an application is started, a parameter section corresponding to the application is added to the clock table.

[0036]

Next, a processing operation of a program used when an application program is ended is described in the embodiment of the present invention with reference to the flow shown in Fig. 3. In the process here, the second application is ended after the process described with reference to Fig. 2.

[0037]

(1) This processing program is launched when an application to be ended is specified by a user and the like. First, the processing program finds a corresponding parameter section from the clock table in Fig. 5 by using the application to be ended, and then deletes the found parameter section from the clock table (steps 301, 302).

[0038]

(2) Then, a sum value of each of the parameters 402 to 405 is calculated again. Then, the parameter section 502 of the sum value is updated to a parameter section 601 (step 303).

[0039]

(3) Next, the specified application program is ended and the values of the control registers for each of the PLLs and frequency dividers are updated by the parameter section 601 of the sum value and a frequency of each of the local clocks 112, 114, 116, and 121 is set at a predetermined frequency, and then the process is ended (steps 304, 305).

[0040]

According to the above-described first embodiment of the present invention, it is possible to set so that each of the MPUs and hardware functional block can operate at an appropriate operating frequency and suppress the power consumption of the entire system.

[0041]

Fig. 7 is a block diagram showing a hardware configuration of an information processing apparatus according to a second embodiment of the present invention. Fig. 8 is a flowchart describing a processing operation of a program used when starting processing stream data. Fig. 9 is a diagram describing a state of a clock table after the processing of the stream data is started by the process shown in Fig. 8. The second embodiment of the present invention is described below with reference to these drawings. In Fig. 7, a reference numeral 701 denotes a stream data input block, while other reference numerals are the same as those in Fig. 1.

[0042]

In the second embodiment of the present invention shown in Fig. 7, the stream data input block 701 is connected to the system bus 105 to be added to the information processing apparatus according to the first embodiment shown in Fig. 1 so as to enable processing of the stream data. Other constitutions are the same as those in Fig. 1. The stream data input block 701 added in the second embodiment performs a process to receive external inputs of data of digital image, audio, and the like as needed and sends them to the external memory 104 via the system bus 105.

[0043]

As the externally inputted data of digital image, audio, and the like, for example, there are a digital TV tuner, a radio tuner, and the like outside the system. These data are called stream data below. When processing such stream data, the processing is required to be performed in accordance with a format that the sender used in forming the stream data. These formats are selected mainly by a data amount, a

convenience of the sender, and the like. When constituting a receiver to be capable of accepting plural formats, the receiver is required to be constituted so that it can determine which stream corresponds to which format. In general, these plural formats require different processing capacities depending on the formats.

[0044]

In the second embodiment of the present invention, by using a program that executes a process described with reference to Fig. 8, appropriate operating frequencies can be set every time the format of the stream is changed. Next, a process when an external stream starts to be processed is described with reference to the flow shown in Fig. 8. In this process as well, the clock table described with reference to Fig. 4 is used. The parameter section of the first application of this clock table corresponds to a stream data processing program of this process.

[0045]

(1) This processing program is launched at the same time as the stream data processing program. First, the processing program determines whether an input stream format is changed or not. When the format is not changed, the processing program repeatedly performs a determination at a certain period of interval (step 801).

[0046]

(2) When the input stream format is changed in the determination of step 801, parameters of the new input stream format are stored in the section of the corresponding application. By this process, the table is updated such that the parameter section of the first application denoted by 407 in Fig. 4 is changed to a parameter section denoted by 901 of an application 1a in Fig. 9 (step 802).

[0047]

(3) Then, a sum of each of the parameters 402 to 405 is calculated in the clock table updated in step 802 to update the parameter section 409 of the sum value to a parameter section 902 (step 803).

[0048]

(4) A determination is performed as to whether none of the parameters in the parameter section 902 updated by the process of step 803 exceed the values in the maximum allowable value section 410. If even one parameter exceeds the maximum allowable value, the updated section 901 in the clock table updated in step 802 is deleted and a sum value of each parameter of the parameter section 902 of the sum values of the parameter values is calculated again, by which the section 902 of the sum value in the clock table is updated, and the process here is ended (steps 804, 805).

[0049]

(5) In the case where none of the parameters exceed the maximum allowable values in the determination of step 804, values of the control registers for each of the PLLs and frequency dividers are changed on the basis of the sum values updated in step 803, and the frequencies of the local clocks 112, 114, 116, and 121 are set at predetermined values. After that, a processing operation in the new stream format is started and returns to the process from step 801 (steps 806, 807).

[0050]

According to the above-described second embodiment of the present invention, the operating frequencies can be changed in response to a change in format of externally inputted data in addition to the effect of the first embodiment. Thus, the power consumption of the entire system can be suppressed.

[0051]

Fig. 10 is a block diagram showing a hardware configuration of an information processing apparatus according to a third embodiment of the present invention. Fig. 11 is a flowchart describing a processing operation of a program used for changing an operating frequency when a power source voltage is changed. Fig. 12 is a diagram describing a state of a clock table after the operating frequency is changed in the process shown in Fig. 11. The third embodiment of the present invention is described below

with reference to these drawings. In Fig. 10, reference numeral 1001 denotes a battery, 1002 denotes a voltmeter, 1003 denotes a power source monitor register, and 1004 denotes a voltage storing register. Other reference numerals are the same as those in Fig. 1.

[0052]

The third embodiment of the present invention enables to reduce the power consumption by reducing the operating frequency of the entire processing apparatus when the power source voltage is reduced. The voltmeter 1002 which measures a voltage of the battery 1001; a power source monitor register which monitors the voltage of the battery measured by the voltmeter 1002 and supplies the signal to the system via the system bus 105; and the voltage storing register 1004 which stores a voltage value of the battery of the time when the clock table was previously updated; are added to the first embodiment of the present invention described with reference to Fig. 1. Other constitutions are the same as those in Fig. 1.

[0053]

Normally, as the battery 1001 consumes power, its voltage is reduced. The voltmeter 1002 detects this reduction in voltage and reflects it to the power source monitor register 1003 as needed. This register 1003 can be referenced from the first and second MPUs 101 and 102 via the system bus 105.

[0054]

Next, a description is made, with reference to the flow shown in Fig. 11, of a process to change operating frequencies when a power source voltage is changed. In this process as well, the clock table described with reference to Fig. 4 is referenced. Further, the voltage storing register 1004 stores a voltage value of the battery of the time when the clock table was previously updated, namely, when the clock table is in the state as shown in Fig. 4.

[0055]

(1) This processing program is launched when the system is launched. When launched, the processing program first reads out a value of the voltage monitor register 1003 and determines whether the value of the voltage monitor register is updated. A voltage change of the battery 1001 is reflected to the voltage monitor register 1003 at all times. When there is no change in the voltage of the battery 1001, the processing program continues the determination of whether the value is updated, at a constant interval (steps 1101, 1102).

[0056]

(2) When the value of the voltage monitor register is updated in the determination of step 1102, a value of the voltage storing register 1004 which stores the voltage value of the battery of the time when the clock table was previously updated; and the value of the updated voltage monitor register are compared, and a determination is performed as to whether the value of the voltage monitor register is larger than the value of the voltage storing register by a certain value or more (step 1103).

[0057]

(3) When the value of the voltage monitor register is not larger than the value of the voltage storing register by the certain value or more in the determination of step 1103, a determination is performed as to whether the value of the voltage monitor register is smaller than the value of the voltage storing register by a certain value or more. When the value of the voltage monitor register is not smaller than the value of the voltage storing register by the certain value or more, that is, when the difference between these values is less than the certain value, it is determined that the change in the voltage was not so large as to change the set values of the clock table. Thus, with no change, the process returns to step 1101 to be continued (step 1107).

[0058]

(4) When the value of the voltage monitor register is smaller than the value of the voltage storing register by the certain value or more in the determination of step

1107, a quotient of each changeable parameter value of the clock table divided by 2 is obtained and the quotient replaces the current value. As a result, the clock table shown in Fig. 4 becomes as shown in Fig. 12. In this case, values of the parameter section 406 of the system and values of the clock item 405 of the display are unchangeable. The values in the parameter sections of the first and second applications are changed as denoted by 1201 and 1202, and values in the parameter section 1204 of the maximum allowable value are changed to quotients of division by 2, and a section 1203 of the sum value is calculated again (step 1108).

[0059]

(5) After that, a determination is performed as to whether there is 0 in the parameter values calculated again in step 1108. If there is, and when a sum of values of clock items of the MPU that an application requires is 0 or a value of the clock item 404 of the memory control block is 0, the application is determined inoperable. Then, the application is ended and the process here is ended (steps 1109, 1110).

[0060]

(6) When there is no parameter having a value of 0 in the determination of step 1109, the values of the control registers for the PLLs and frequency dividers are updated and set, and the current value of the voltage monitor register is recorded in the voltage storing register 1004. Then, the process returns to step 1101 to be continued (step 1111).

[0061]

(7) When the value of the voltage monitor register is larger than the value of the voltage storing register by the certain value or more in the determination of step 1103, a determination is performed as to whether the value of the voltage monitor register is a maximum value (step 1104).

[0062]

In general, when an information processing apparatus is driven by a battery, the

process in accordance with the flow as described above is performed since the voltage of the battery is reduced with time. Therefore, the value of the voltage monitor register is determined larger than the value of the voltage storing register by the certain value or more in step 1103 in the case where the battery is changed or the battery is floating from an alternating power source.

[0063]

(8) When the value of the voltage monitor register is not the maximum value in the determination of step 1104, it means that the reduced voltage was recovered. Thus, a changeable parameter value in the clock table is doubled to replace the current value. Then, the process from step 1111 is continued. In this case, the parameter value is at least 1/2 in the above-described process of step 1108. Therefore, no problem arises even by doubling the parameter value in the process here (step 1106).

[0064]

(9) When the value of the monitor register is the maximum value in the determination of step 1104, each parameter of the clock table is returned to the initial value, and then the process form step 1111 is continued (step 1105).

[0065]

According to the above-described third embodiment of the present invention, the operating frequency can be changed in response to the voltage change of the external power source in addition to the effect of the first embodiment, thereby the power consumption of the entire system can be suppressed and the operation time can be extended.

[0066]

Fig. 13 is a block diagram showing a hardware configuration of an information processing apparatus according to a fourth embodiment of the present invention. Fig. 14 is a flowchart describing a processing operation of a program to change a power source voltage by a required clock frequency. Fig. 15 is a diagram describing a

constitution of a clock-voltage table used in the process of Fig. 14. The fourth embodiment of the present invention is described with reference to these drawings. In Fig. 13, reference numeral 1301 denotes a DC-DC converter, 1302 denotes a voltage setting register, and other reference numerals are the same as those in Fig. 1.

[0067]

In the fourth embodiment of the present invention as shown in Fig. 13, a voltage supplied to each block that constitutes the processing apparatus is changed on the basis of the values of the parameter section of the sum value in the above-described clock table, thereby to reduce the power consumption of the processing apparatus. In the first embodiment of the present invention described with reference to Fig. 1, the DC-DC converter 1301 and the voltage setting register 1302 are provided. The DC-DC converter 1301 determines a power source voltage by using a set value of the voltage setting register 1302 and supplies a power source having this voltage to all the blocks shown in Fig. 13. The voltage setting register 1302 can be accessed by the first and second MPUs 101 and 102 via the system bus 105 and can be controlled by these MPUs.

[0068]

Next, a processing operation of a program to change the power source voltage by a required clock frequency is described with reference to the flow shown in Fig. 14. In this process, the clock-voltage table shown in Fig. 15 is used. In Fig. 15, reference numeral 1501 denotes maximum values in the parameter section of the sum value in the clock table and 1502 denotes corresponding voltage setting register values.

[0069]

(1) This processing program is launched at the time the system is launched. When launched, the processing program first determines whether the clock table described with reference to Fig. 4 is updated, and continues the determination whether the clock table is updated, until an update is performed (step 1401).

[0070]

(2) After that, a maximum value is selected from the parameter section 409 of the sum value in the clock table. In this parameter section 409, the maximum value is 16. Subsequently, a voltage value corresponding to the maximum value is obtained from the clock-voltage table shown in Fig. 15. In this case, a minimum value in the maximum sum value 1501 exceeding 16 is 20. Therefore, the corresponding voltage register setting value obtained from the voltage setting register value 1502 is 19 (steps 1402, 1403).

[0071]

(3) Next, a determination is performed as to whether the value obtained in step 1403 is the same as the current voltage register setting value. If they are the same, the above-described process is repeated from step 1401. If they are different, a new value is set in the voltage setting register (step 1405).

[0072]

According to the above-described fourth embodiment of the present invention, the power source voltage can further be changed in accordance with the operating frequency in addition to the effect of the first embodiment, thereby the power consumption of the entire system can further be suppressed.

[0073]

The first to fourth embodiments of the present invention have been described hitherto. The present invention can be constituted by combining a plurality of the first to fourth embodiments.

[0074]

[Effect of the Invention]

According to the present invention, as described above, a sufficient processing capacity for an operating application can be achieved, functional blocks such as MPUs can be operated at an appropriate frequency and operating voltage so that the

application can be operated with minimum power consumption, thereby the lower power consumption of the information processing apparatus can be achieved.

[Brief Description of the Drawings]

Fig. 1 is a block diagram showing a hardware configuration of an information processing apparatus according to the first embodiment of the present invention;

Fig. 2 is a flowchart describing a processing operation of a program used when an application program is added and launched;

Fig. 3 is a flowchart describing a processing operation of a program used when the application program is ended;

Fig. 4 is a diagram describing a clock table used in the process of Fig. 2;

Fig. 5 is a diagram describing a state of the clock table after the application is added and launched in the process of Fig. 2;

Fig. 6 is a diagram describing a state of the clock table after the application is ended in the process of Fig. 3;

Fig. 7 is a block diagram showing a hardware configuration of an information processing apparatus according to the second embodiment of the present invention;

Fig. 8 is a flowchart describing a processing operation of a program used when starting processing of stream data;

Fig. 9 is a diagram describing a state of the clock table after the processing of the stream data is started in the process of Fig. 8;

Fig. 10 is a block diagram showing a hardware configuration of an information processing apparatus according to the third embodiment of the present invention;

Fig. 11 is a flowchart describing a processing operation of a program used for changing an operating frequency when a power source voltage changes;

Fig. 12 is a diagram describing a state of the clock table after the operating frequency is changed in the process of Fig. 11;

Fig. 13 is a block diagram showing a hardware configuration of an information

processing apparatus according to the fourth embodiment of the present invention;

Fig. 14 is a flowchart describing a processing operation of a program to change a power source voltage according to a required clock frequency; and

Fig. 15 is a diagram describing a constitution of a clock-voltage table used in the process of Fig. 14.

[Description of Reference Numerals]

101, 102 ... first and second microprocessor units (MPUs)

103 ... external memory control unit

104 ... external memory

105 ... system bus

106 ... functional block

107 ... digital-analog converter (DAC)

108, 118 ... first and second phased locked loops (PLLs)

111, 113, 115, 120 ... first to fourth frequency dividers

117, 122 ... first and second control registers

701 ... stream data input block

1001 ... battery

1002 ... voltmeter

1003 ... power source monitor register

1004 ... voltage storing register

1301 ... DC-DC converter

1302 ... voltage setting register

Fig. 1

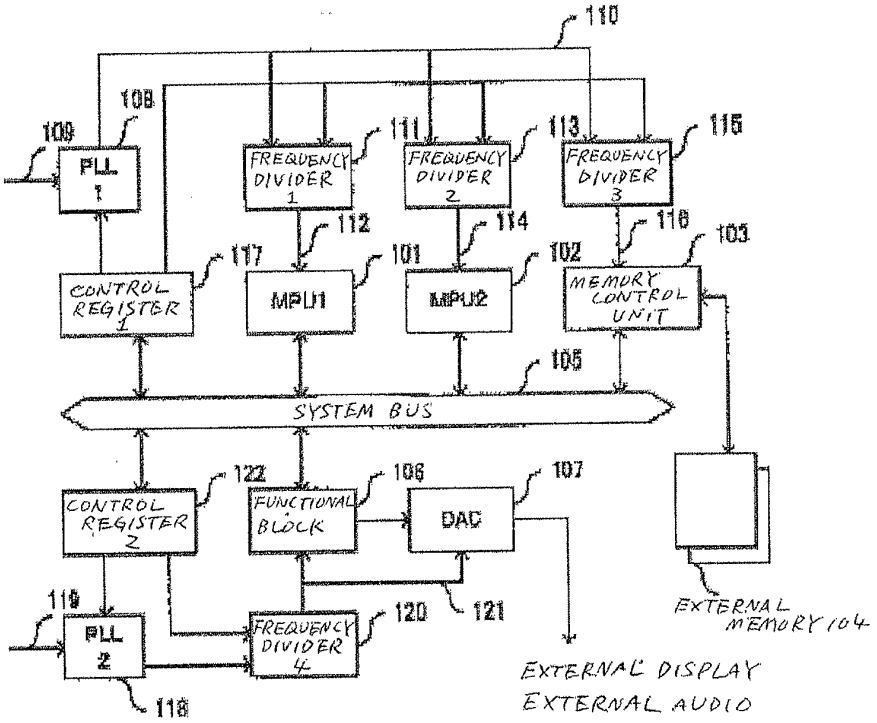

110
108
109
PLL 1
FREQUENCY DIVIDER 1
111
FREQUENCY DIVIDER 2
113
FREQUENCY DIVIDER 3
115
112
114
116
103
117
CONTROL REGISTER 1
MPU1
101
MPU2
102
MEMORY CONTROL UNIT
105
SYSTEM BUS
122
CONTROL REGISTER 2
FUNCTIONAL BLOCK
106
DAC
107
119
PLL 2
FREQUENCY DIVIDER 4
120
121
118
EXTERNAL MEMORY 104
EXTERNAL DISPLAY
EXTERNAL AUDIO

Fig. 2

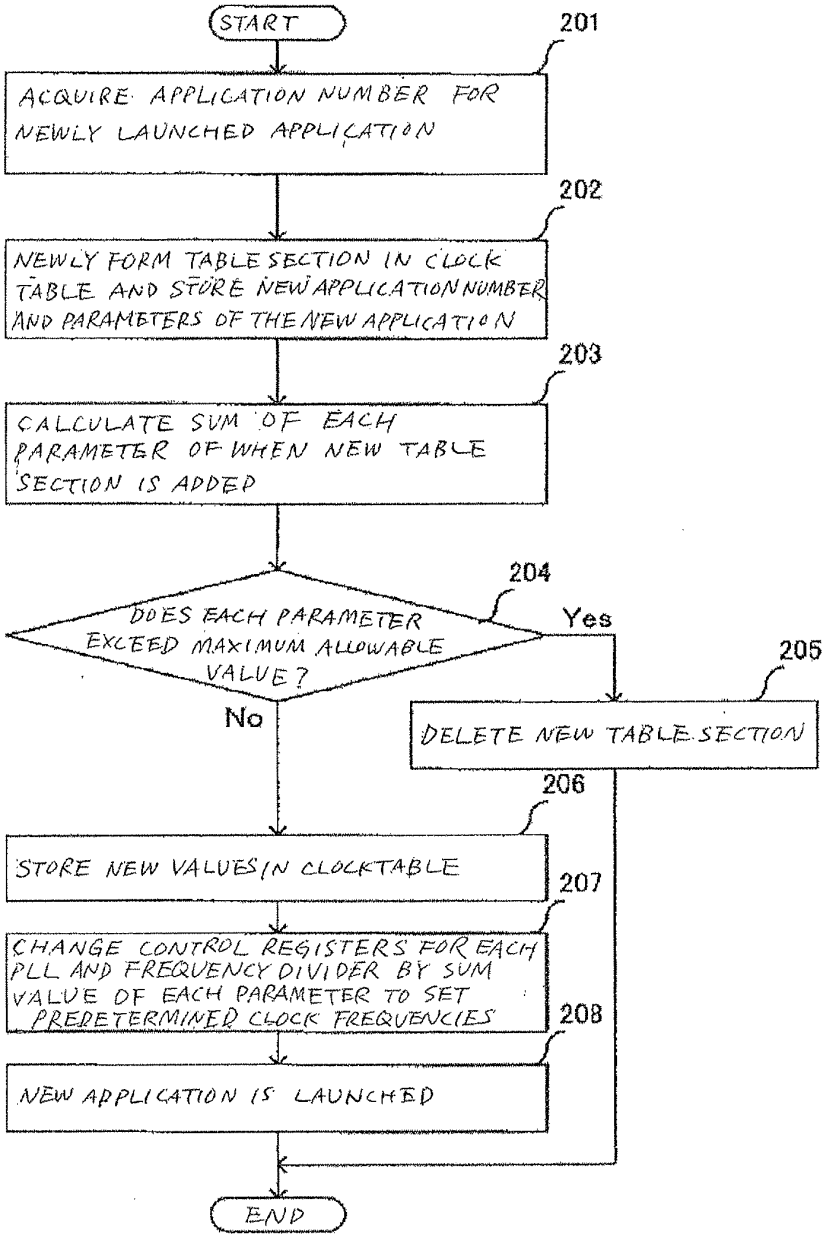

START
201
ACQUIRE APPLICATION NUMBER FOR NEWLY LAUNCHED APPLICATION
202
NEWLY FORM TABLE SECTION IN CLOCK TABLE AND STORE NEW APPLICATION NUMBER AND PARAMETERS OF THE NEW APPLICATION
203
CALCULATE SUM OF EACH PARAMETER OF WHEN NEW TABLE SECTION IS ADDED
204
DOES EACH PARAMETER EXCEED MAXIMUM ALLOWABLE VALUE?
Yes
No
205
DELETE NEW TABLE SECTION
206
STORE NEW VALUES IN CLOCKTABLE
207
CHANGE CONTROL REGISTERS FOR EACH PLL AND FREQUENCY DIVIDER BY SUM VALUE OF EACH PARAMETER TO SET PREDETERMINED CLOCK FREQUENCIES
208
NEW APPLICATION IS LAUNCHED
END

Fig. 3

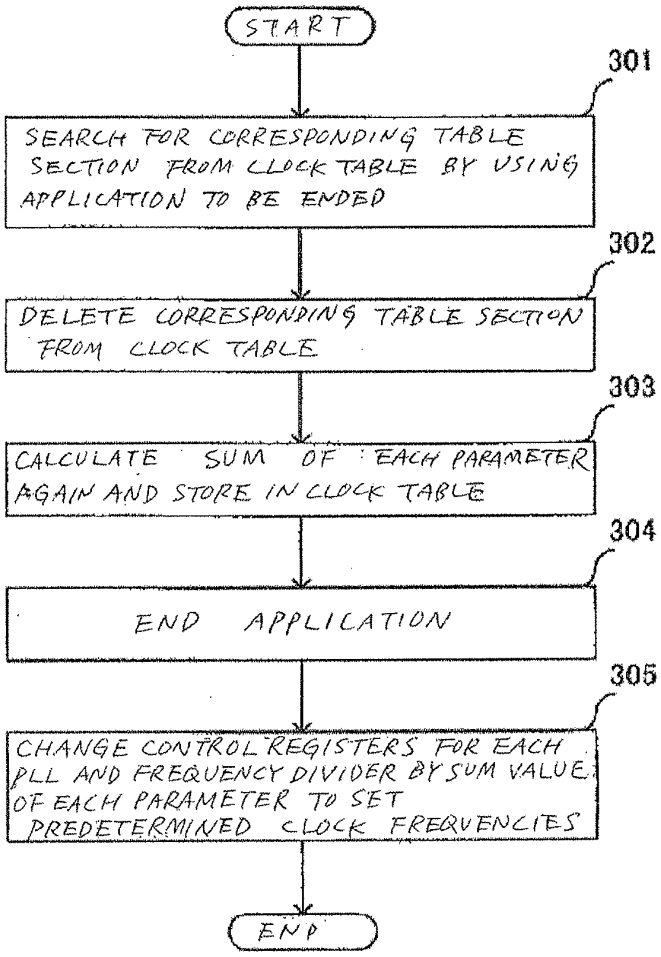

START
301
SEARCH FOR CORRESPONDING TABLE SECTION FROM CLOCK TABLE BY USING APPLICATION TO BE ENDED
302
DELETE CORRESPONDING TABLE SECTION FROM CLOCK TABLE
303
CALCULATE SUM OF EACH PARAMETER AGAIN AND STORE IN CLOCK TABLE
304
END APPLICATION
305
CHANGE CONTROL REGISTERS FOR EACH PLL AND FREQUENCY DIVIDER BY SUM VALUE OF EACH PARAMETER TO SET PREDETERMINED CLOCK FREQUENCIES
END

Fig. 4

	401 Application Number	402 MPU 1	403 MPU 2	404 Memory	405 DAC
406	0 (System)	1	1	1	-
407	1	5	15	5	15
408	2	7	0	2	-
409	SumValue	13	16	8	15
410	Maximum Allowable Value	20	20	10	15
411	Determination	Operable	Operable	Operable	Operable

Fig. 5

	401 Application Number	402 MPU 1	403 MPU 2	404 Memory	405 Display
406	0 (System)	1	1	1	-
407	1	5	15	5	15
408	2	7	0	2	-
501	3	3	1	1	-
502	Sum Value	16	17	9	15
410	Maximum Allowable Value	20	20	10	15
411	Determination	Operable	Operable	Operable	Operable

Fig. 6

	401 Application Number	402 MPU 1	403 MPU 2	404 Memory	405 Display
406	0 (System)	1	1	1	-
407	1	5	15	5	15
501	3	3	1	1	-
601	Sum Value	9	17	7	15
410	Maximum Allowable Value	20	20	10	15
411	Determination	Operable	Operable	Operable	Operable

Fig. 7

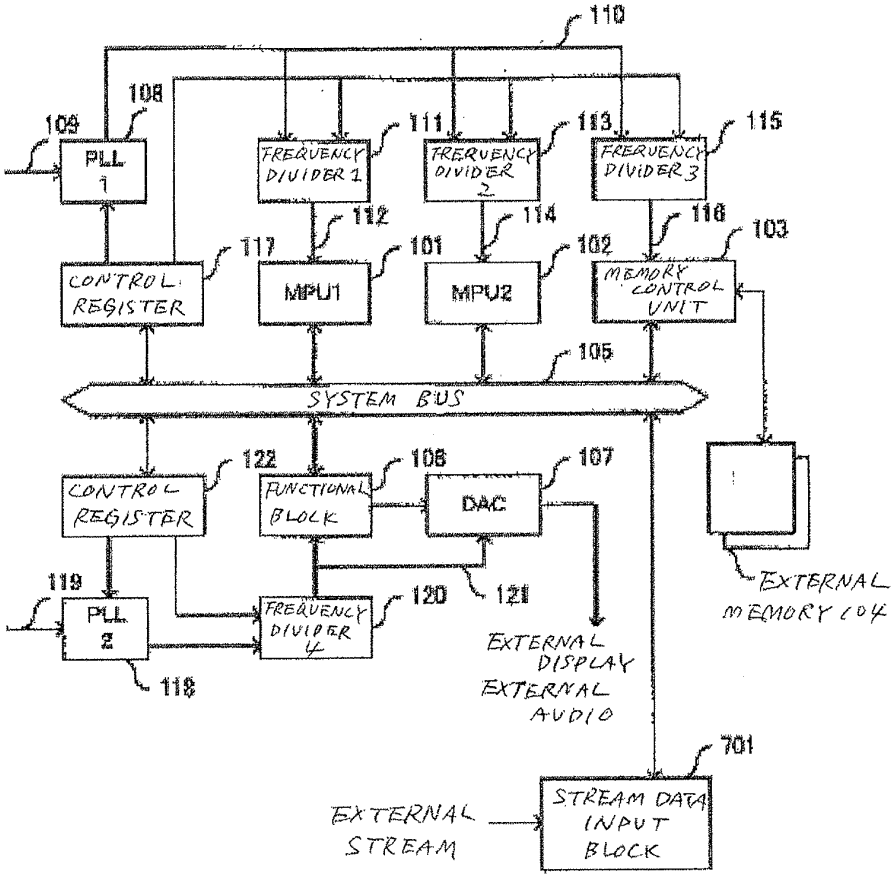

110
108
109
PLL 1
FREQUENCY DIVIDER 1
111
FREQUENCY DIVIDER 2
113
FREQUENCY DIVIDER 3
115
112
114
116
103
117
CONTROL REGISTER
101
MPU1
102
MPU2
MEMORY CONTROL UNIT
105
SYSTEM BUS
122
CONTROL REGISTER
106
FUNCTIONAL BLOCK
107
DAC
EXTERNAL MEMORY
119
PLL 2
120
FREQUENCY DIVIDER 4
121
118
EXTERNAL DISPLAY
EXTERNAL AUDIO
701
EXTERNAL STREAM
STREAM DATA INPUT BLOCK

Fig. 8

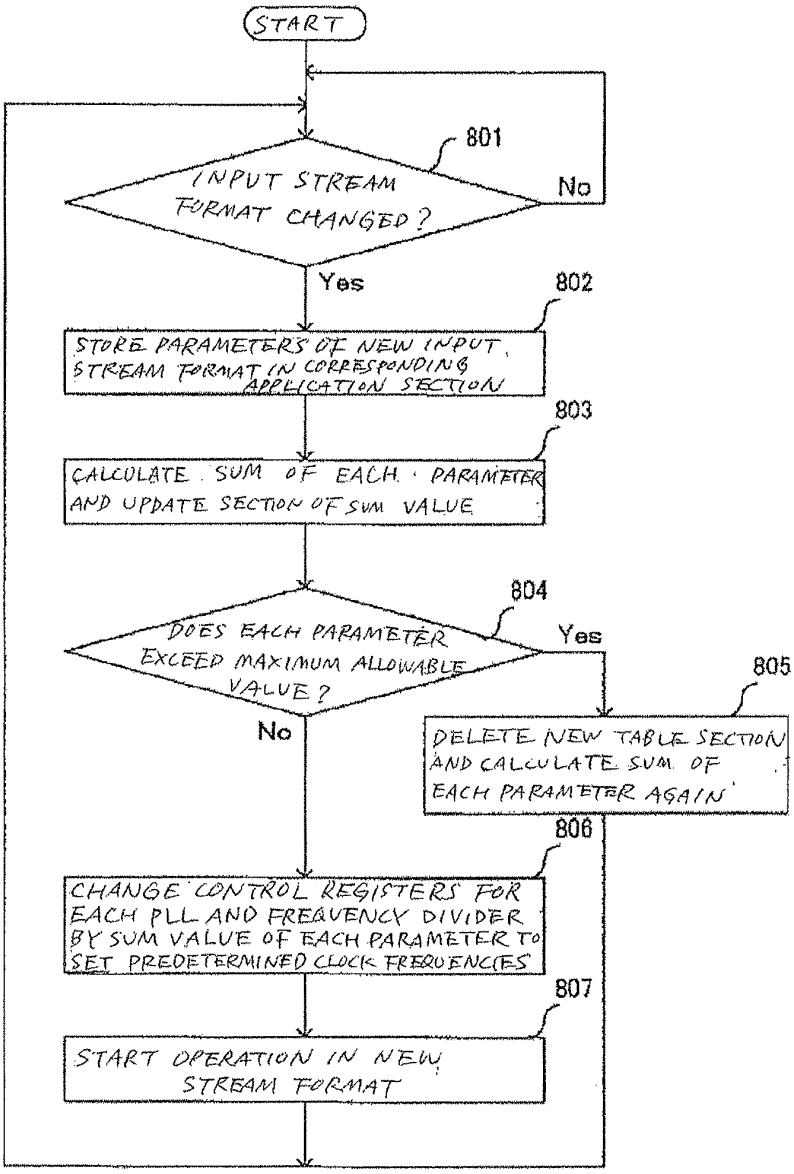

START
801
INPUT STREAM FORMAT CHANGED?
No
Yes
802
STORE PARAMETERS OF NEW INPUT STREAM FORMAT IN CORRESPONDING APPLICATION SECTION
803
CALCULATE SUM OF EACH PARAMETER AND UPDATE SECTION OF SUM VALUE
804
DOES EACH PARAMETER EXCEED MAXIMUM ALLOWABLE VALUE?
Yes
No
805
DELETE NEW TABLE SECTION AND CALCULATE SUM OF EACH PARAMETER AGAIN
806
CHANGE CONTROL REGISTERS FOR EACH PLL AND FREQUENCY DIVIDER BY SUM VALUE OF EACH PARAMETER TO SET PREDETERMINED CLOCK FREQUENCIES
807
START OPERATION IN NEW STREAM FORMAT

Fig. 9

	401 Application Number	402 MPU 1	403 MPU 2	404 Memory	405 Display
406	0 (System)	1	1	1	-
901	1a	5	10	2	8
408	2	7	0	2	-
902	Total	13	11	5	8
410	Maximum Allowable Value	20	20	10	15
411	Determination	Operable	Operable	Operable	Operable

Fig. 10

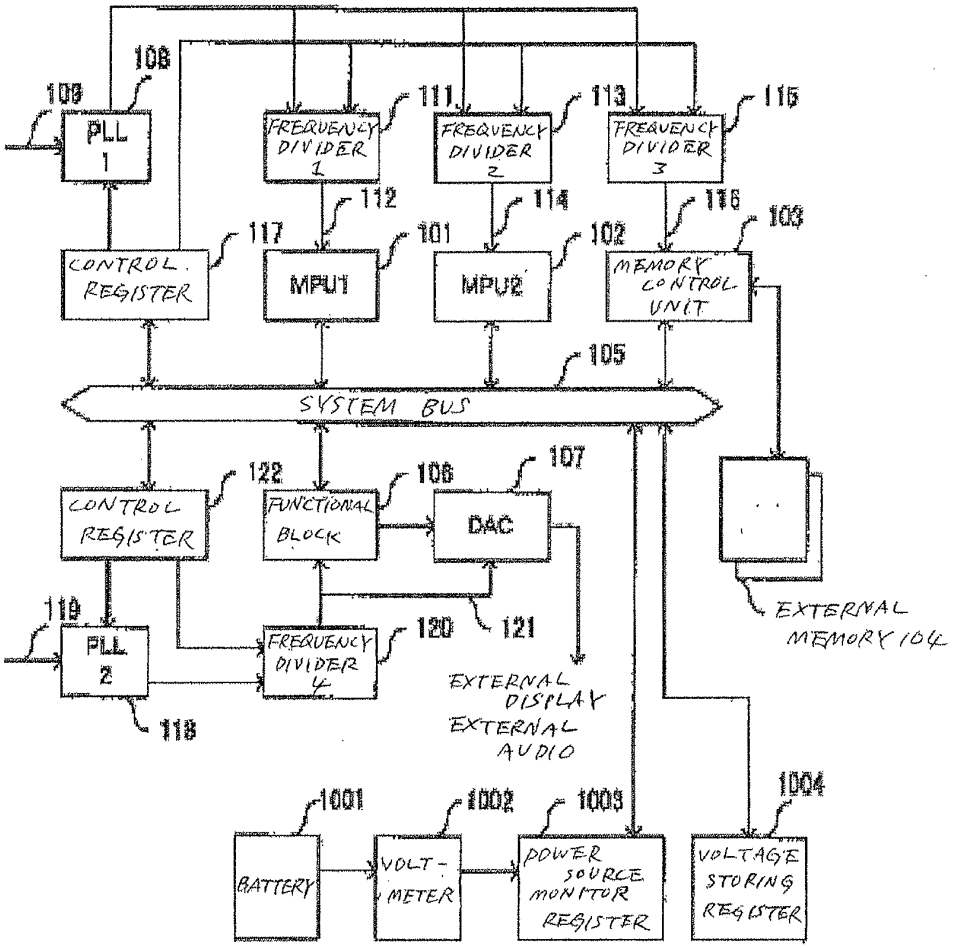

108
109
PLL 1
FREQUENCY DIVIDER 1
111
FREQUENCY DIVIDER 2
113
FREQUENCY DIVIDER 3
115
112
114
116
103
117
CONTROL REGISTER
MPU1
101
MPU2
102
MEMORY CONTROL UNIT
105
SYSTEM BUS
122
CONTROL REGISTER
FUNCTIONAL BLOCK
106
DAC
107
EXTERNAL MEMORY 104
119
PLL 2
FREQUENCY DIVIDER 4
120
121
EXTERNAL DISPLAY
EXTERNAL AUDIO
118
1001
BATTERY
1002
VOLT-METER
1003
POWER SOURCE MONITOR REGISTER
1004
VOLTAGE STORING REGISTER

Fig. 11

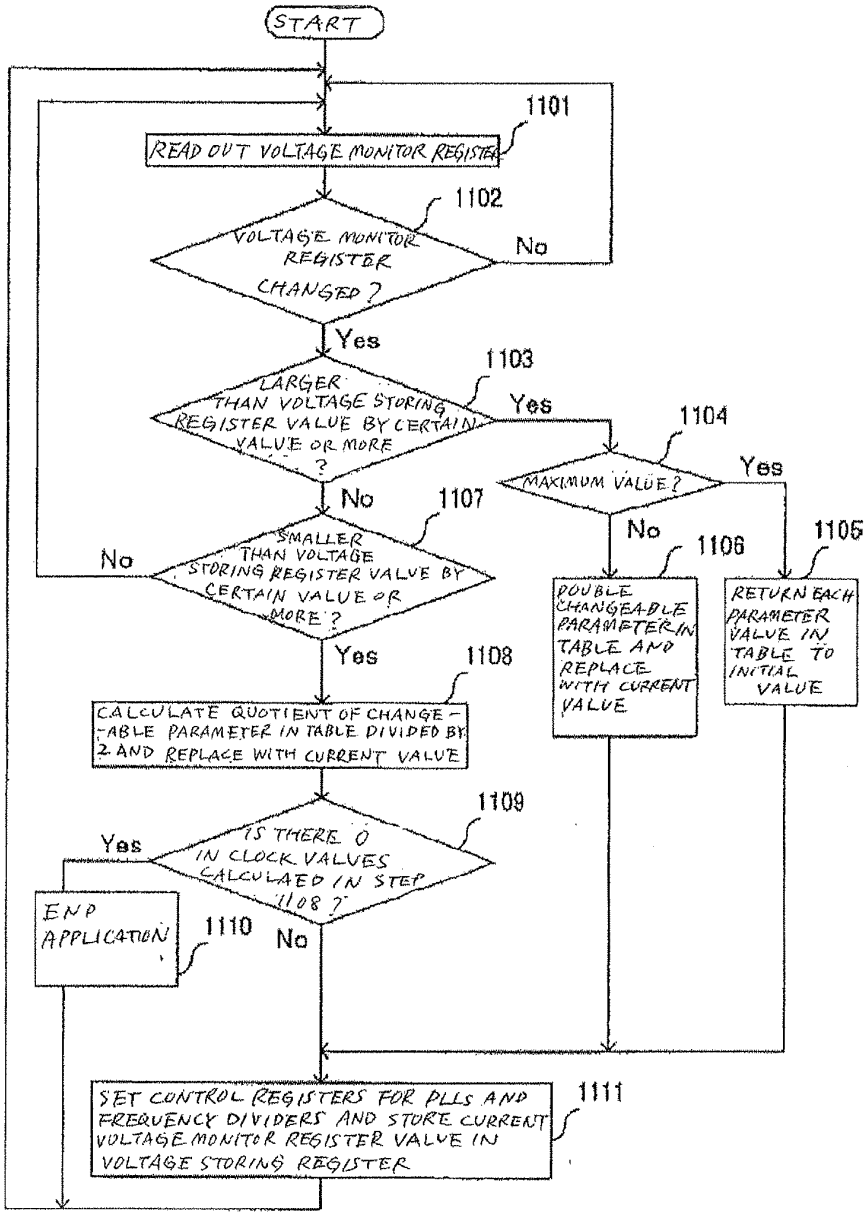

START
1101
READ OUT VOLTAGE MONITOR REGISTER
1102
VOLTAGE MONITOR REGISTER CHANGED ?
No
Yes
1103
LARGER THAN VOLTAGE STORING REGISTER VALUE BY CERTAIN VALUE OR MORE ?
Yes
1104
MAXIMUM VALUE ?
Yes
No
No
1107
SMALLER THAN VOLTAGE STORING REGISTER VALUE BY CERTAIN VALUE OR MORE ?
No
1106
DOUBLE CHANGEABLE PARAMETER IN TABLE AND REPLACE WITH CURRENT VALUE
1105
RETURN EACH PARAMETER VALUE IN TABLE TO INITIAL VALUE
Yes
1108
CALCULATE QUOTIENT OF CHANGEABLE PARAMETER IN TABLE DIVIDED BY 2 AND REPLACE WITH CURRENT VALUE
1109
IS THERE 0 IN CLOCK VALUES CALCULAED IN STEP 1108 ?
Yes
END APPLICATION
1110
No
1111
SET CONTROL REGISTERS FOR PLLS AND FREQUENCY DIVIDERS AND STORE CURRENT VOLTAGE MONITOR REGISTER VALUE IN VOLTAGE STORING REGISTER

Fig. 12

	401 Application Number	402 MPU 1	403 MPU 2	404 Memory	405 Display
406	0 (System)	1	1	1	-
1201	1	2	7	2	15
1202	2	3	0	1	-
1203	Total	6	8	4	15
1204	Maximum Allowable Value	10	10	5	15
411	Determination	Operable	Operable	Operable	Operable

Fig. 13

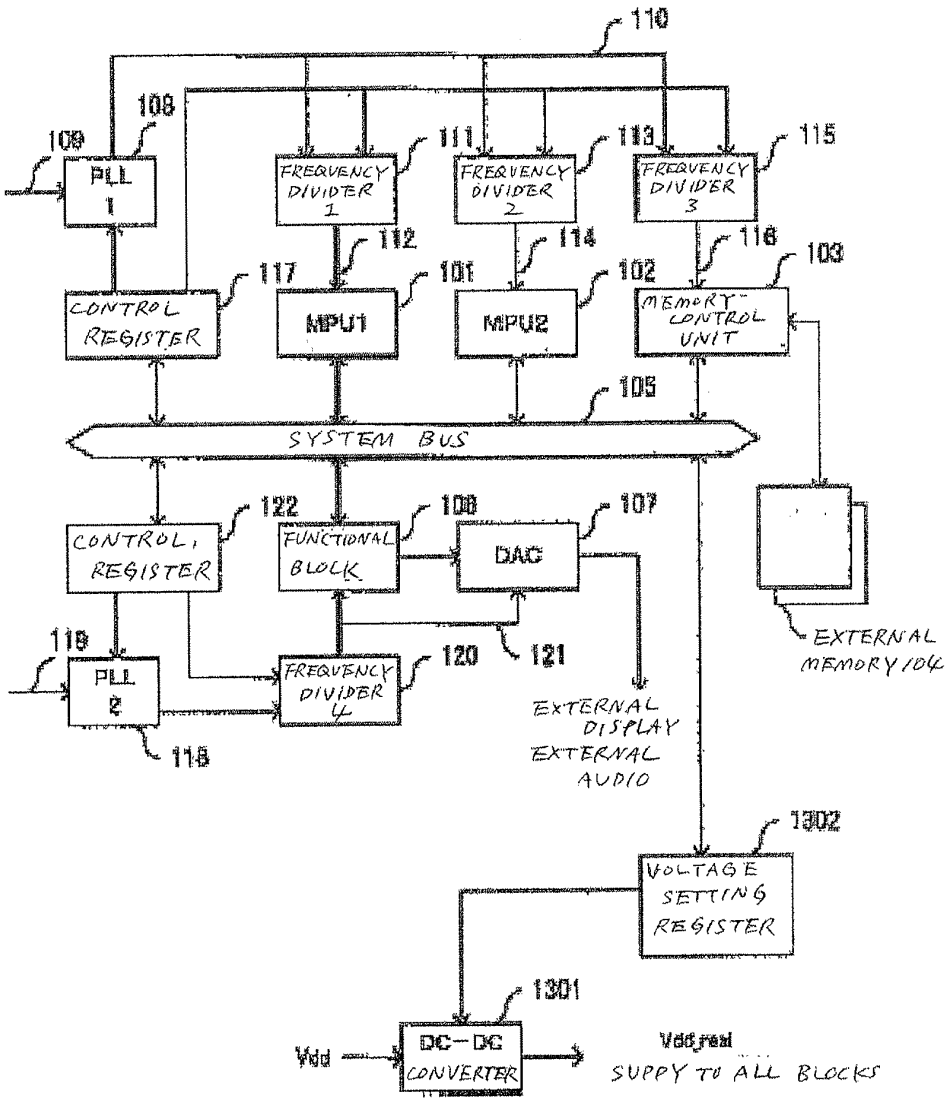

110
108
109
PLL 1
111
FREQUENCY DIVIDER 1
113
FREQUENCY DIVIDER 2
115
FREQUENCY DIVIDER 3
112
114
116
103
117
CONTROL REGISTER
101
MPU1
102
MPU2
MEMORY CONTROL UNIT
105
SYSTEM BUS
122
CONTROL REGISTER
FUNCTIONAL BLOCK
106
DAC
107
EXTERNAL MEMORY/IO
119
PLL 2
120
FREQUENCY DIVIDER 4
121
EXTERNAL DISPLAY
EXTERNAL AUDIO
118
1302
VOLTAGE SETTING REGISTER
1301
Vdd
DC-DC CONVERTER
Vdd,real
SUPPY TO ALL BLOCKS

Fig. 14

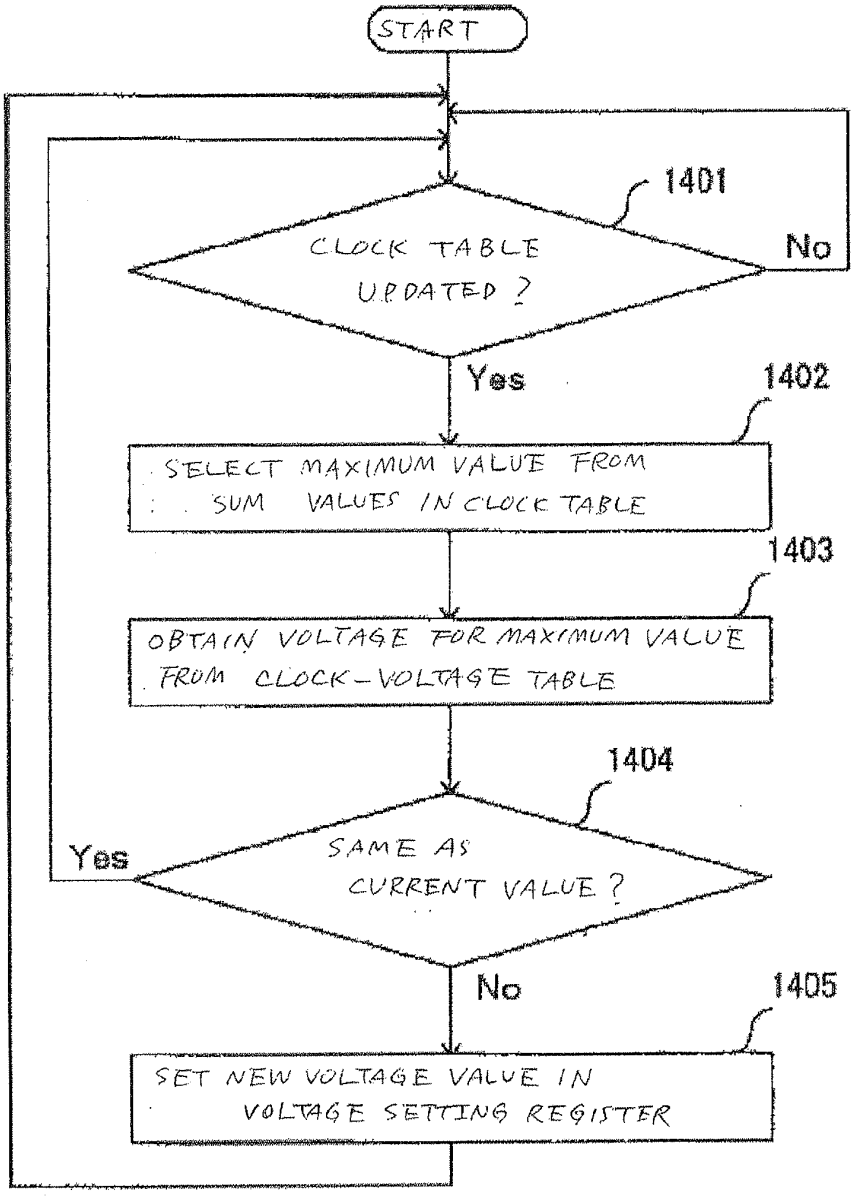

START
1401
CLOCK TABLE UPDATED ?
No
Yes
1402
SELECT MAXIMUM VALUE FROM SUM VALUES IN CLOCK TABLE
1403
OBTAIN VOLTAGE FOR MAXIMUM VALUE FROM CLOCK-VOLTAGE TABLE
1404
SAME AS CURRENT VALUE ?
Yes
No
1405
SET NEW VOLTAGE VALUE IN VOLTAGE SETTING REGISTER

Fig. 15

1501

Maximum Sum Value	10	15	20	15
Voltage Setting Register Value	16	18	19	20

1502

Electronic Acknowledgement Receipt	
EFS ID:	6938602
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	21005
Filer:	James M. Smith/Jill Kane
Filer Authorized By:	James M. Smith
Attorney Docket Number:	2037.2079-010
Receipt Date:	03-FEB-2010
Filing Date:	21-JUL-2008
Time Stamp:	15:38:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	20372079010_SIDS.pdf	151366 ed86ae5f632d341aadf7c2c471313a8d0ac155f0	no	3
Warnings:					
Information:					

2	Information Disclosure Statement (IDS) Filed (SB/08)	20372079010_Listing.pdf	57702 17aaa3955bc70e027ff9835a9dcdead381980e2c	no	1
Warnings:					
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3	Foreign Reference	20372079010_B1.pdf	2883203 9297601f0f6c8d6036c2a4eb23709d3c21814981	no	55
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2811
Filed:	July 21, 2008	Examiner:	Not Yet Assigned
Confirmation No.:	3003		
For:	Power Managers for an Integrated Circuit		

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Alexandria, VA 22313-1450

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- ☐ a Statement under 37 CFR 1.97(e), as checked below, or
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(After the 37 CFR 1.97(b) time period, but before any of a final action, notice of allowance, or an action that closes prosecution, whichever occurs first)

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- ☐ a Statement under 37 CFR 1.97(e), as checked below, and
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☐ under 37 CFR 1.97(i):
Applicant requests that the IDS and cited reference(s) be placed in the application file.
(Filed after payment of issue fee)

956748_1

Statement Under 37 CFR 1.97(e)

☐ Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement; or

☐ No item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

Statement Under 37 CFR 1.704(d) (Patent Term Adjustment)
Applies to original applications (other than design) filed on or after May 29, 2000

☐ Each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in § 1.56(c) more than thirty days prior to the filing of the Information Disclosure Statement.

☒ Enclosed herewith is a Listing of References:

- ☒ Copies of the cited references are enclosed except as indicated below.
- ☐ Copies of issued U.S. patents and published U.S. applications are not required and are not being provided.
- ☐ Copies of the cited references submitted with an Information Disclosure Statement in prior application, U.S. Application No. [ ], to which priority under 35 U.S.C. 120 is claimed, are not required under 37 CFR 1.98(d)(1) and (2) and are thus not provided.
- ☐ Pending non-published applications are not being provided, since the applications are available to the examiner.

☐ The listed references were cited in the enclosed Search Report in counterpart foreign application [add application number], which is listed in the attached Listing of References.

☐ The "concise explanation" requirement (non-English references) for reference [ ] under 37 CFR 1.98(a)(3) is satisfied by:

- ☐ the explanation provided on the attached sheet.
- ☐ the explanation provided in the Specification.
- ☐ submission of the enclosed International Search Report.
- ☐ submission of the enclosed English-language version of a foreign Search Report and/or foreign Office Action.
- ☐ the enclosed English language abstract.

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☐ Please charge Deposit Account 08-0380 in the amount of $[ ].

☒ Please charge any deficiency in fees and credit any overpayment to Deposit Account 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____

James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133

Dated: 2/3/10

Substitute for form 1449B/PTO **SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **December 23, 2009** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Not Yet Assigned	CONFIRMATION NO. 3003	GROUP 2811

U.S. PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
	A2	7,111,178 B2	09-19-2006	Rusu, et al.

We are not listing separately any prior U.S. Patent Office communications regarding the cited application(s) because the Examiner has access to any such actions through PAIR.

EXAMINER	DATE CONSIDERED

Electronic Acknowledgement Receipt

EFS ID:	6706184
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	21005
Filer:	James M. Smith/Jill Kane
Filer Authorized By:	James M. Smith
Attorney Docket Number:	2037.2079-010
Receipt Date:	24-DEC-2009
Filing Date:	21-JUL-2008
Time Stamp:	11:14:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	20372079010_SIDS.pdf	151005 eb941e32d95061659a16a07754166bc552fec3c0	no	3

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Information:	

2	Information Disclosure Statement (IDS) Filed (SB/08)	20372079010_Listing.pdf	64666 2be1b4d518aee06ee0e802f30a7c7cf14cfc6dae	no	1

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2811
Filed:	July 21, 2008	Examiner:	Not Yet Assigned
Confirmation No.:	3003		
For:	Power Managers for an Integrated Circuit		

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(After the 37 CFR 1.97(b) time period, but before any of a final action, notice of allowance, or an action that closes prosecution, whichever occurs first)

☐ under 37 CFR 1.97(d) together with:
- ☐ a Statement under 37 CFR 1.97(e), as checked below, and
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(Filed after final action, notice of allowance, whichever occurs first, or if prosecution otherwise closes, but on or before payment of the issue fee)

☐ under 37 CFR 1.97(i):
Applicant requests that the IDS and cited reference(s) be placed in the application file.
(Filed after payment of issue fee)

946761_1

Statement Under 37 CFR 1.97(e)

☐ Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement; or

☐ No item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

Statement Under 37 CFR 1.704(d) (Patent Term Adjustment)
Applies to original applications (other than design) filed on or after May 29, 2000

☐ Each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in § 1.56(c) more than thirty days prior to the filing of the Information Disclosure Statement.

☒ Enclosed herewith is a Listing of References:

- ☐ Copies of the cited references are enclosed except as indicated below.
- ☒ Copies of issued U.S. patents and published U.S. applications are not required and are not being provided.
- ☐ Copies of the cited references submitted with an Information Disclosure Statement in prior application, U.S. Application No. [ ], to which priority under 35 U.S.C. 120 is claimed, are not required under 37 CFR 1.98(d)(1) and (2) and are thus not provided.
- ☐ Pending non-published applications are not being provided, since the applications are available to the examiner.

☐ The listed references were cited in the enclosed Search Report in counterpart foreign application [add application number], which is listed in the attached Listing of References.

☐ The "concise explanation" requirement (non-English references) for reference(s) [ ] under 37 CFR 1.98(a)(3) is satisfied by:

- ☐ the explanation provided on the attached sheet.
- ☐ the explanation provided in the Specification.
- ☐ submission of the enclosed International Search Report.
- ☐ submission of the enclosed English-language version of a foreign Search Report and/or foreign Office Action.
- ☐ the enclosed English language abstract.

Method of payment:

☐ A check for the fee noted above is enclosed, or the fee has been included in the check with the accompanying Reply.

☐ Please charge Deposit Account 08-0380 in the amount of $[ ].

☒ Please charge any deficiency in fees and credit any overpayment to Deposit Account 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____

James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133

Dated: 12/25/9

946761_1

Substitute for form 1449B/PTO **INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **July 28, 2009** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Not Yet Assigned	CONFIRMATION NO. 3003	GROUP 2811

U.S. PATENT DOCUMENTS

Examiner's Initials	Ref. No.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
	A1	5,778,237	07-07-1998	Yamamoto, et al.
	A2			
	A3			
	A4			
	A5			
	A6			
	A7			
	A8			
	A9			
	A10			
	A11			
	A12			
	A13			
	A14			
	A15			
	A16			
	A17			
	A18			
	A19			
	A20			

We are not listing separately any prior U.S. Patent Office communications regarding the cited application(s) because the Examiner has access to any such actions through PAIR.

EXAMINER	DATE CONSIDERED

909684 1

Substitute for form 1449B/PTO **INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **July 28, 2009** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Not Yet Assigned	CONFIRMATION NO. 3003	GROUP 2811

Examiner's Initials	Ref. No.	**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent Pages, Etc.)*
	C2	Nowka, et al., "A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling," *IEEE Journal of Solid-State Circuits,* Vol. 37, No. 11, pp. 1441-1447 (November 2002).
	C3	Nowka, et al., "The Design and Application of the PowerPC 405LP Energy-Efficient System-on-a-Chip," *IBM J. Res. & Dev.,* Vol. 47. No. 5/6, pp. 631-639 (September/November 2003).
	C4	Semeraro, et al., "Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling," *Proceedings of the Eighth International Symposium on High-Performance Computer Architecture* (2002).
	C5	
	C6	
	C7	
	C8	
	C9	
	C10	
	C11	
	C12	
	C13	
	C14	
	C15	
	C16	
	C17	
	C18	
	C19	
	C20	

EXAMINER	DATE CONSIDERED

909684_1

Electronic Acknowledgement Receipt

EFS ID:	5780451
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	21005
Filer:	James M. Smith/Jill Kane
Filer Authorized By:	James M. Smith
Attorney Docket Number:	2037.2079-010
Receipt Date:	28-JUL-2009
Filing Date:	21-JUL-2008
Time Stamp:	14:27:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	20372079010_SIDS.pdf	153116 d0e2bf2ffe773e60755b96e6c52b3d2cb575684a	no	3
Warnings:					
Information:					

2	Information Disclosure Statement (IDS) Filed (SB/08)	20372079010_Listing.pdf	156676 53ee57de4d458033ca68f7202bd2af67fcd874d6	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	NPL Documents	203792079010_C2.pdf	1054735 a7c5000f002cd68cc0a30abb9a21627cf162dd2c	no	7
Warnings:					
Information:					
4	NPL Documents	20372079010_C3.pdf	1141194 ffa9324227be9738263246974b1f1b8f618b2d05	no	9
Warnings:					
Information:					
5	NPL Documents	20372079010_C4.pdf	1580821 b3c721723ad5d6dc31bc77126ff080ec9b389542	no	12
Warnings:					
Information:					
		Total Files Size (in bytes):	4086542		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2811
Filed:	July 21, 2008	Examiner:	Not Yet Assigned
Confirmation No.:	3003		
For:	Power Managers for an Integrated Circuit		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Information Disclosure Statement is submitted:

☒ under 37 CFR 1.97(b), or
(Within any one of the following time periods: three months of filing national application (other than a CPA) or date of entry of the national stage in an international application; or before the mailing date of a first office action on the merits; or before the mailing of a first office action after the filing of a Request for Continued Examination).

☐ under 37 CFR 1.97(c) together with either:
- ☐ a Statement under 37 CFR 1.97(e), as checked below, or
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(After the 37 CFR 1.97(b) time period, but before any of a final action, notice of allowance, or an action that closes prosecution, whichever occurs first)

☐ under 37 CFR 1.97(d) together with:
- ☐ a Statement under 37 CFR 1.97(e), as checked below, and
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(Filed after final action, notice of allowance, whichever occurs first, or if prosecution otherwise closes, but on or before payment of the issue fee)

☐ under 37 CFR 1.97(i):
Applicant requests that the IDS and cited reference(s) be placed in the application file.
(Filed after payment of issue fee)

Statement Under 37 CFR 1.97(e)

☐ Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement; or

☐ No item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

Statement Under 37 CFR 1.704(d) (Patent Term Adjustment)
Applies to original applications (other than design) filed on or after May 29, 2000

☐ Each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in § 1.56(c) more than thirty days prior to the filing of the Information Disclosure Statement.

☒ Enclosed herewith is a Listing of References:

- ☒ Copies of the cited references are enclosed except as indicated below.
- ☒ Copies of issued U.S. patents and published U.S. applications are not required and are not being provided.
- ☐ Copies of the cited references submitted with an Information Disclosure Statement in prior application, U.S. Application No. [ ], to which priority under 35 U.S.C. 120 is claimed, are not required under 37 CFR 1.98(d)(1) and (2) and are thus not provided.
- ☐ Pending non-published applications are not being provided, since the applications are available to the examiner.

☐ The listed references were cited in the enclosed Search Report in counterpart foreign application [add application number], which is listed in the attached Listing of References.

☐ The "concise explanation" requirement (non-English references) for reference(s) [ ] under 37 CFR 1.98(a)(3) is satisfied by:

- ☐ the explanation provided on the attached sheet.
- ☐ the explanation provided in the Specification.
- ☐ submission of the enclosed International Search Report.
- ☐ submission of the enclosed English-language version of a foreign Search Report and/or foreign Office Action.
- ☐ the enclosed English language abstract.

Method of payment:

☐ A check for the fee noted above is enclosed, or the fee has been included in the check with the accompanying Reply.

☐ Please charge Deposit Account 08-0380 in the amount of $[ ].

☒ Please charge any deficiency in fees and credit any overpayment to Deposit Account 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____

James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Dated: 7/28/9

909665_1

Substitute for form 1449B/PTO **INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION** **LISTING OF REFERENCES** **July 15, 2009** (Use several sheets if necessary)	ATTORNEY DOCKET NO. 2037.2079-010	APPLICATION NO. 12/176,645	
	FIRST NAMED INVENTOR Barry Alan Hoberman	FILING DATE July 21, 2008	
	EXAMINER Not Yet Assigned	CONFIRMATION NO. 3003	GROUP 2811

Examiner's Initials	Ref. No.	**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent Pages, Etc.)*
	C1	Nowka, *et al.*, "A 0.9V to 1.95V Dynamic Voltage-Scalable and Frequency-Scalable 32b PowerPC Processor," *IEEE International Solid-State Circuits Conference 20.4* (February 6, 2002).
	C2	
	C3	
	C4	
	C5	
	C6	
	C7	
	C8	
	C9	
	C10	
	C11	
	C12	
	C13	
	C14	
	C15	
	C16	
	C17	
	C18	
	C19	
	C20	

EXAMINER	DATE CONSIDERED

906517_1

Electronic Acknowledgement Receipt

EFS ID:	5738987
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	21005
Filer:	James M. Smith/Jill Kane
Filer Authorized By:	James M. Smith
Attorney Docket Number:	2037.2079-010
Receipt Date:	21-JUL-2009
Filing Date:	21-JUL-2008
Time Stamp:	14:43:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	20372079010_SIDS.pdf	148596 cf6328ac2a0b89f3447a905b84239d65d4436751	no	3

Warnings:	
Information:	

2	Information Disclosure Statement (IDS) Filed (SB/08)	20372079010_Lisitng.pdf	63487 107a5854867645227e5eb65d2e18ab28ebd4f74b	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	NPL Documents	20372079010_C1.pdf	480080 fa287456334fc2c8221185f7461250928ca77e47	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	692163		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2811
Filed:	July 21, 2008	Examiner:	Not Yet Assigned
Confirmation No.:	3003		
For:	Power Managers for an Integrated Circuit		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Supplemental Information Disclosure Statement is submitted:

☒ under 37 CFR 1.97(b), or
(Within any one of the following time periods: three months of filing national application (other than a CPA) or date of entry of the national stage in an international application; or before the mailing date of a first office action on the merits; or before the mailing of a first office action after the filing of a Request for Continued Examination).

☐ under 37 CFR 1.97(c) together with either:
- ☐ a Statement under 37 CFR 1.97(e), as checked below, or
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(After the 37 CFR 1.97(b) time period, but before any of a final action, notice of allowance, or an action that closes prosecution, whichever occurs first)

☐ under 37 CFR 1.97(d) together with:
- ☐ a Statement under 37 CFR 1.97(e), as checked below, and
- ☐ a $180.00 fee under 37 CFR 1.17(p), or

(Filed after final action, notice of allowance, whichever occurs first, or if prosecution otherwise closes, but on or before payment of the issue fee)

☐ under 37 CFR 1.97(i):
Applicant requests that the IDS and cited reference(s) be placed in the application file.
(Filed after payment of issue fee)

906516_1

Statement Under 37 CFR 1.97(e)

☐ Each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement; or

☐ No item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned, after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

Statement Under 37 CFR 1.704(d) (Patent Term Adjustment)
Applies to original applications (other than design) filed on or after May 29, 2000

☐ Each item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart application and this communication was not received by any individual designated in § 1.56(c) more than thirty days prior to the filing of the Information Disclosure Statement.

☒ Enclosed herewith is a Listing of References:

- ☒ Copies of the cited references are enclosed except as indicated below.
- ☐ Copies of issued U.S. patents and published U.S. applications are not required and are not being provided.
- ☐ Copies of the cited references submitted with an Information Disclosure Statement in prior application, U.S. Application No. [ ], to which priority under 35 U.S.C. 120 is claimed, are not required under 37 CFR 1.98(d)(1) and (2) and are thus not provided.
- ☐ Pending non-published applications are not being provided, since the applications are available to the examiner.

☐ The listed references were cited in the enclosed Search Report in counterpart foreign application [add application number], which is listed in the attached Listing of References.

☐ The "concise explanation" requirement (non-English references) for reference(s) [ ] under 37 CFR 1.98(a)(3) is satisfied by:

- ☐ the explanation provided on the attached sheet.
- ☐ the explanation provided in the Specification.
- ☐ submission of the enclosed International Search Report.
- ☐ submission of the enclosed English-language version of a foreign Search Report and/or foreign Office Action.
- ☐ the enclosed English language abstract.

Method of payment:

☐ A check for the fee noted above is enclosed, or the fee has been included in the check with the accompanying Reply.

☐ Please charge Deposit Account 08-0380 in the amount of $[ ].

☒ Please charge any deficiency in fees and credit any overpayment to Deposit Account 08-0380.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____

James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Dated: 7/21/9

906516_1

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/176,645	07/21/2008	Barry Alan HOBERMAN	2037.2079-010

CONFIRMATION NO. 3003

21005
HAMILTON, BROOK, SMITH & REYNOLDS, P.C.
530 VIRGINIA ROAD
P.O. BOX 9133
CONCORD, MA 01742-9133

POA ACCEPTANCE LETTER

OC000000034867699

Date Mailed: 03/09/2009

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/24/2009.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/vvan/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/176,645	07/21/2008	Barry Alan HOBERMAN	50908.36.P13US04

CONFIRMATION NO. 3003

59893
EATON PEABODY PATENT GROUP, LLC
P.O. BOX 5249
77 Sewall Street, Suite 3000
AUGUSTA, ME 04332-5249

POWER OF ATTORNEY NOTICE

OC000000034867679

Date Mailed: 03/09/2009

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/24/2009.

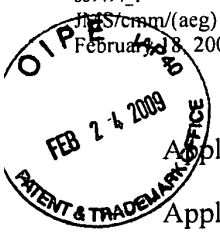
- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/vvan/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

LFW

869494_1
JMS/cmm/(aeg)
February 18, 2009



PATENT APPLICATION
Docket No.: 50908.36.P13US04 (2037.2079-010)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell		
Application No.:	12/176,645	Group:	2811
Filed:	July 21, 2008	Examiner:	Not yet assigned

Confirmation No.: 3003

For: POWER MANAGERS FOR AN INTEGRATED CIRCUIT

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or is being facsimile transmitted to the United States Patent and Trademark Office on:

2-20-09 Amy Green
Date Signature

Amy Green
Typed or printed name of person signing certificate

REQUEST FOR CHANGE OF DOCKET NUMBER AND CORRECTED FILING RECEIPT

Customer Correction Office
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant's attorney requests that the docket number of record for the above-referenced case be changed to 2037.2079-010. This request is made to better identify this application within our offices. Please provide a corrected Filing Receipt indicating the new attorney docket number.

Please charge Deposit Account No. 08-0380 for any fees that may be due in this matter.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____
James M. Smith
Registration No.: 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Dated: 2/18/9

OIPE
FEB 24 2009
U.S. PATENT & TRADEMARK OFFICE

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

REVOCATION OF POWER OF ATTORNEY WITH NEW POWER OF ATTORNEY and CHANGE OF CORRESPONDENCE ADDRESS

Application/Patent Number	12/176,645
Filing/Issue Date	July 21, 2008
First Named Inventor/Patentee	Barry Alan Hoberman
Confirmation Number	3003
Group Art Unit	2811
Examiner Name	Not Yet Assigned
Attorney Docket Number	2037.2079-010

Title POWER MANAGERS FOR AN INTEGRATED CIRCUIT

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ I hereby appoint the following practitioner(s): [Not to exceed 10]

OR

☒ I hereby appoint the practitioners associated with the Customer Number: **021005**

Please change the correspondence address for the above-identified application to:

☒ **Customer Number 021005**
Hamilton, Brook, Smith & Reynolds, P.C.
530 Virginia Road
P.O. Box 9133
Concord, Massachusetts 01742-9133

☐ Other

Please direct all telephone calls and facsimiles to:

Name James M. Smith, Esq. Tel. No. 978-341-0036 Fax No. 978-341-0136

I am the:

☐ Applicant/Inventor.

☒ Authorized representative of the Assignee, Mosaid Technologies Corporation, of the entire interest. See 37 CFR § 3.71. A Statement under 37 CFR § 3.73(b) is enclosed.

☐ Authorized representative of the Assignee, [FILL IN WITH NAME OF ASSIGNEE], together with [FILL IN WITH NAME OF ASSIGNEE], of the entire interest. A Statement under 37 CFR § 3.73(b) is enclosed.

SIGNATURE of Applicant or Assignee of Record

Signature	
Name & Title	Phil Shaer - Secretary
Date	February 11, 2009

861963_1

OIPE
FEB 24 2009
PATENT & TRADEMARK OFFICE
IAP40

Docket No. 2037.2079-010

STATEMENT UNDER 37 CFR § 3.73(b)

Applicant/Patentee: Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell

Application No./Patent No.: 12/176,645 Filed/Issue Date: July 21, 2008

For: POWER MANAGERS FOR AN INTEGRATED CIRCUIT

MOSAID Technologies Corporation (Name of Assignee), a corporation (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is

A. ☒ the assignee of the entire right, title and interest in the patent application identified above; or

B. ☐ an assignee together with [ ] of the entire right, title and interest in the patent application identified above.

The right, title and interest of the above-named assignee in the patent application identified above is established by virtue of:

A. ☐ An assignment from the inventor(s) of the patent application identified above. The assignment was recorded in the Patent and Trademark Office at Reel [ ], Frame [ ], or a copy thereof is attached.

OR

B. ☒ A chain of title from the inventor(s) of the patent application identified above, to the current assignee as shown below:

1. From: Barry Alan Hoberman, Daniel L. Hillman and Jon Shiell
   To: Virtual SiliconTechnology, Inc.
   The document was recorded in the United States Patent and Trademark Office at
   Reel 021669, Frames 0867-0870, or a copy thereof is attached.

2. From: Virtual SiliconTechnology, Inc. To: Mosaid Delaware, Inc.
   The document was recorded in the United States Patent and Trademark Office at
   Reel 021669, Frames 0871-0876, or a copy thereof is attached.

3. From: Mosaid Delaware, Inc. To: Mosaid Technologies Corporation
   The document was recorded in the United States Patent and Trademark Office at
   Reel 021669, Frame 0877-0879, or a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature

Name: Phil Shaer

Title: Secretary

Date: February 11, 2009

861969_1

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/176,645	07/21/2008	Barry Alan HOBERMAN	50908.36.P13US04

CONFIRMATION NO. 3003

59893
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PUBLICATION NOTICE



Title:POWER MANAGERS FOR AN INTEGRATED CIRCUIT

Publication No.US-2008-0276105-A1
Publication Date:11/06/2008

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

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In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Barry HOBERMAN et al.
Application No.:	12/176,645
Filed:	July 21, 2008
Title:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
Docket No.:	50908.36.P13US04
Art Unit:	2115
Examiner:	(not yet known)

August 21, 2008

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Applicant requests that the application be amended stating as follows:

Amendment to the Specification begins on page 2.
Amendment to the Claims begins on page 3.
Remarks begin on page 14.

Amendment to the Specification:

[0001] This application is a continuation of U.S. Application Serial Number 11/336,097 filed on January 20, 2006 entitled "Power Managers for an Integrated Circuit" and which ~~issued on _____ as U.S. Patent Number _____, which is a continuation~~ issued on August 19, 2008 as U.S. Patent Number 7,415,680 which is a continuation of U.S. Application Serial Number 10/840,893 filed on May 7, 2004 and entitled "Managing Power on Integrated Circuits Using Power Islands" and which issued on May 23, 2006 as U.S. Patent Number 7,051,306 which claims the benefit of U.S. Provisional Application Serial Number 60/468,742 titled "System and Method for Managing Power in Integrated Circuits," filed May 7, 2003, which are each hereby incorporated by reference.

Amendment to the Claims:

1. (currently amended) A software product for building an integrated circuit including a plurality of power islands, the software product comprising:

~~circuit design software operational when executed by a processor to direct the processor to select~~ computer readable instructions stored on an at least one storage medium, the computer readable instructions configured for selecting blocks of predetermined circuits to form:

power control circuitry configured to control power for one of the power islands, and

a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, and determine at least one of actions including selecting a frequency for one of the power islands, selecting a voltage for one of the power islands, and selecting a transistor threshold voltage for one of the power islands, the at least one of the actions to change a power consumption level of the one of the power islands to the target power level, and the power manager configured to perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level ~~where one of the actions is chosen from a group consisting of selecting a frequency for one of the power islands, selecting a voltage for one of the power islands, and selecting a transistor threshold voltage for one of the power islands~~.

2. (original) The software product of **Claim 1** wherein the power islands are delineated based on geographic factors of the integrated circuit.

3. (original) The software product of **Claim 1** wherein the power islands are delineated based on functional circuitry of the integrated circuit.

4. (canceled)

5. (original) The software product of **Claim 1** wherein the power islands comprise multiple clock domains.

6. (currently amended) The software product of **Claim 1** wherein ~~another one of~~ the actions further include ~~comprises selecting a~~ performing clock gating for the one of the power islands.

7. (canceled)

8. (canceled)

9. (canceled)

10. (currently amended) The software product of **Claim 1** wherein ~~another one of~~ the actions further include ~~comprises~~ powering on the one of the power islands.

11. (currently amended) The software product of **Claim 10** wherein ~~another one of~~ the actions ~~comprises~~ further include powering off the one of the power islands.

12. (currently amended) The software product of **Claim 1** wherein ~~another one of~~ the actions ~~comprises~~ further include changing a mode of the one of the power islands to ~~a~~ sleep ~~mode~~.

13. (canceled)

14. (canceled)

15. (canceled)

16. (currently amended) A software product for building an integrated circuit including a plurality of power islands, the software product comprising:

~~circuit design software operational when executed by a processor to direct the processor to~~

~~select blocks from a group of predetermined circuits;~~

computer readable instructions stored on an at least one storage medium, the computer readable instructions configured for writing ~~write~~ a register transfer level description (RTL) ~~formed from the blocks~~, the RTL representing:

power control circuitry configured to control power for one of the power islands, and

a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, and determine at least one of actions including selecting a frequency for one of the power islands, selecting a voltage for one of the power islands, and selecting a transistor threshold voltage for one of the power islands, the at least one of the actions to change a power consumption level of the one of the power islands to the target power level, and the power manager configured to perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level ~~where one of the actions is chosen from a group consisting of selecting a frequency for one of the power islands, selecting a voltage for one of the power islands, and selecting a transistor threshold voltage for one of the power islands;~~.

~~simulate and debug the RTL;~~

~~synthesize the RTL on a power island basis;~~

~~measure power island performance and update the RTL representing the power manager based upon the measured performance;~~

~~synthesize the RTL updated with regard to measured performance; and~~

~~forming the integrated circuit from the updated RTL.~~

17. (canceled)

18. (canceled)

19. (currently amended) The software product of **Claim 16** wherein the computer readable instructions further ~~compriseing~~ comprise code for adding annotations for the power manager.

20. (original) The software product of **Claim 19** wherein the annotations include functionality options.

21. (canceled)

22. (canceled)

23. (canceled)

24. (canceled)

25. (canceled)

26. (canceled)

27. (new) The software product of **Claim 1** wherein the predetermined circuits are in register transfer level description (RTL) form.

28. (new) The software product of **Claim 1** wherein the actions further include controlling a sleep signal connected to an at least one standard cell of the one of the power islands.

29. (new) The software product of **Claim 1** wherein the actions further include powering off the one of the power islands.

30. (new) The software product of **Claim 16** further comprising additional computer readable instructions for adding annotations, at multiple steps in a design process, to a portion of the RTL representing the power manager.

31. (new) An integrated circuit comprising:

a plurality of power islands having associated power consumptions, each of the power consumptions being independently controlled, and a power consumption in an at least one of the power islands being controlled by: a) selecting a threshold voltage of variable threshold transistors, and b) selecting at least one of the following: i) a frequency of operation, and ii) a supply voltage; and

a power manager which controls the power consumptions.

32. (new) The integrated circuit as claimed in **Claim 31** wherein the supply voltage is selected, and the selecting of the supply voltage includes dynamic voltage selection.

33. (new) The integrated circuit as claimed in **Claim 31** wherein the supply voltage is selected, and the selecting of the supply voltage includes regulating an externally provided voltage.

34. (new) The integrated circuit as claimed in **Claim 33** wherein the regulating is performed with a dropout voltage regulator.

35. (new) The integrated circuit as claimed in **Claim 31** wherein the supply voltage is selected, and the selecting of the supply voltage includes powering off the supply.

36. (new) The integrated circuit as claimed in **Claim 31** wherein the selecting the threshold includes dynamic back biasing.

37. (new) An integrated circuit comprising:

a plurality of power islands having associated power consumptions, each of the power consumptions being independently controlled, and a power consumption in an at least one of the power islands being controlled by selecting a supply voltage, and by selecting a frequency of operation, including an option of stopping a clock; and

a power manager which controls the power consumptions.

38. (new) The integrated circuit as claimed in **Claim 37** wherein the selecting of the supply voltage includes dynamic voltage selection.

39. (new) The integrated circuit as claimed in **Claim 37** wherein the selecting of the supply voltage includes regulating an externally provided voltage.

40. (new) The integrated circuit as claimed in **Claim 39** wherein the regulating is performed with a dropout voltage regulator.

41. (new) The integrated circuit as claimed in **Claim 37** wherein the selecting of the supply voltage includes powering off the supply.

42. (new) The integrated circuit as claimed in **Claim 37** wherein the selecting of the frequency of operation includes dynamic clock selection.

43. (new) The integrated circuit as claimed in **Claim 37** wherein the selecting of the frequency of operation includes modifying a clock frequency.

44. (new) The integrated circuit as claimed in **Claim 37** wherein the stopping of the clock is performed by clock gating.

45. (new) An integrated circuit comprising:

a plurality of power islands having associated power consumptions, at least one of the power consumptions being independently controlled by way of a sleep signal connected to an at least one standard cell; and

a power manager which controls at least one or more of the power consumptions.

46. (new) The integrated circuit as claimed in **Claim 45** wherein the at least one standard cell includes a MOS transistor having a source connected to a power supply terminal and a gate connected to the sleep signal.

47. (new) The integrated circuit as claimed in **Claim 46** wherein the MOS transistor is an n-channel transistor.

48. (new) The integrated circuit as claimed in **Claim 46** wherein the source of the MOS transistor is connected to a ground power supply terminal.

49. (new) The integrated circuit as claimed in **Claim 45** wherein at least one of the power islands includes multiple voltage domain interface circuits.

50. (new) The integrated circuit as claimed in **Claim 49** wherein the multiple voltage domain interface circuits include level shifter circuits.

51. (new) The integrated circuit as claimed in **Claim 49** wherein the multiple voltage domain interface circuits include signal isolation circuits.

52. (new) The integrated circuit as claimed in **Claim 45** wherein at least one of the power islands includes multiple threshold standard cells.

53. (new) The integrated circuit as claimed in **Claim 52** wherein the multiple threshold standard cells include at least two of the following standard cells: standard Vt, high Vt, and low Vt.

54. (new) The integrated circuit as claimed in **Claim 45** wherein at least one of the power islands includes variable Vt standard cells.

55. (new) A computer-implemented method for building an integrated circuit that includes a plurality of power islands, the method comprising:

selecting first blocks of first predetermined circuits to form power control circuitry, the power control circuitry configured to control power for one of the power islands; and

selecting an at least one second block of an at least one second predetermined circuit to form a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, and determine at least one of actions including selecting a frequency for one of the power islands, selecting a voltage for one of the power islands, and selecting a transistor

threshold voltage for one of the power islands, the at least one of the actions to change a power consumption level of the one of the power islands to the target power level, and the power manager configured to perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level.

56. (new) The computer-implemented method of **Claim 55** wherein the actions further include performing clock gating for the one of the power islands.

57. (new) The computer-implemented method of **Claim 55** wherein the actions further include powering on the one of the power islands.

58. (new) The computer-implemented method of **Claim 55** wherein the actions further include powering off the one of the power islands.

59. (new) The computer-implemented method of **Claim 55** wherein the actions further include changing a mode of the one of the power islands to sleep.

60. (new) A method carried out within an integrated circuit having a plurality of power islands having associated power consumptions, the method comprising:

employing a power manager to control the power consumptions, each of the power consumptions being independently controlled; and

controlling a power consumption of an at least one of the power islands by: a) selecting a threshold voltage of variable threshold transistors, and b) selecting at least one of the following: i) a frequency of operation, and ii) a supply voltage.

61. (new) The method as claimed in **Claim 60** wherein the supply voltage is selected, and the selecting of the supply voltage includes dynamic voltage selection.

62. (new) The method as claimed in **Claim 60** wherein the supply voltage is selected, and the selecting of the supply voltage includes regulating an externally provided voltage.

63. (new) The method as claimed in **Claim 60** wherein the supply voltage is selected, and the selecting of the supply voltage includes powering off the supply.

64. (new) The method as claimed in **Claim 60** wherein the selecting the threshold includes dynamic back biasing.

65. (new) A method carried out within an integrated circuit having a plurality of power islands having associated power consumptions, the method comprising:

employing a power manager to control the power consumptions, each of the power consumptions being independently controlled; and

controlling a power consumption of an at least one of the power islands by selecting a supply voltage and selecting a frequency of operation, including an option of stopping a clock.

66. (new) The method as claimed in **Claim 65** wherein the selecting of the supply voltage includes dynamic voltage selection.

67. (new) The method as claimed in **Claim 65** wherein the selecting of the supply voltage includes regulating an externally provided voltage.

68. (new) The method as claimed in **Claim 65** wherein the selecting of the supply voltage includes powering off the supply.

69. (new) The method as claimed in **Claim 65** wherein the selecting of the frequency of operation includes dynamic clock selection.

70. (new) The method as claimed in **Claim 65** wherein the selecting of the frequency of operation includes modifying a clock frequency.

71. (new) The method as claimed in **Claim 65** wherein the stopping of the clock is performed by clock gating.

72. (new) A method carried out within an integrated circuit having a plurality of power islands having associated power consumptions, the method comprising:

employing a power manager to control the power consumptions, each of the power consumptions being independently controlled; and

controlling a power consumption of an at least one of the power islands by way of a sleep signal connected to an at least one standard cell of the at least one of the power islands.

73. (new) The method as claimed in **Claim 72** further comprising generating the sleep signal.

74. (new) The method as claimed in **Claim 72** wherein the sleep signal is connected to a gate of an NMOS transistor of the at least one standard cell.

REMARKS

Applicants have previously paid for eight (8) independent claims and twenty-six (26) total claims. By way of this preliminary amendment, nine (9) independent claims and fifty-nine (59) total claims are now pending in the instant application. Accordingly, Applicants have further paid herewith the fees for one (1) further additional independent claim and thirty-three (33) further additional total claims.

Please charge any deficiency in fees and credit any overpayment to Deposit Account 503807.

Respectfully submitted,

BARRY HOBERMAN et al.

By: /Dennis R. Haszko, Reg. No. 39,575/

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Electronic Patent Application Fee Transmittal	
Application Number:	12176645
Filing Date:	21-Jul-2008
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Filer:	Dennis R. Haszko
Attorney Docket Number:	50908.36.P13US04
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1202	33	50	1650
Independent claims in excess of 3	1201	1	210	210
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1860**

Electronic Acknowledgement Receipt	
EFS ID:	3817727
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	59893
Filer:	Dennis R. Haszko
Filer Authorized By:	
Attorney Docket Number:	50908.36.P13US04
Receipt Date:	21-AUG-2008
Filing Date:	21-JUL-2008
Time Stamp:	14:44:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1860
RAM confirmation Number	162
Deposit Account	503807
Authorized User	HASZKO,DENNIS R.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		00375216.PDF	52009 41e3ae3d91529a54b846a11a161fcd1aaa768178	yes	14

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Preliminary Amendment	1	1
Specification	2	2
Claims	3	13
Applicant Arguments/Remarks Made in an Amendment	14	14

Warnings:

Information:

2	Fee Worksheet (PTO-06)	fee-info.pdf	32222 fff8e184160e81544197407769ffd66248792cd	no	2

Warnings:

Information:

Total Files Size (in bytes):	84231

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/176,645	07/21/2008	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☒ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	310
☒ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	510
☒ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	210
TOTAL CLAIMS (37 CFR 1.16(i))	26 minus 20 =	* 6	X $ =		OR	X $50 =	300
INDEPENDENT CLAIMS (37 CFR 1.16(h))	8 minus 3 =	* 5	X $ =			X $210 =	1050
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2380

APPLICATION AS AMENDED – PART II

AMENDMENT		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	08/21/2008	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 59	Minus	** 59	= 0	X $ =		OR	X $50=	0
	Independent (37 CFR 1.16(h))	* 9	Minus	***9	= 0	X $ =		OR	X $210=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1)		(Column 2)	(Column 3)	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA					
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/PAUL I. NEAL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Doc code :IDS
Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	12176645
	Filing Date	2008-07-21
	First Named Inventor	Barry HOBERMAN
	Art Unit	
	Examiner Name	
	Attorney Docket Number	50908.36.P13US04

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	1	20080088358		2008-04-17	CAPLAN et al.	
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☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Dennis R. Haszko, Reg. No. 39,575/	Date (YYYY-MM-DD)	2008-08-18
Name/Print	Dennis R. Haszko	Registration Number	39,575

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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EFS ID:	3793579
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	59893
Filer:	Dennis R. Haszko
Filer Authorized By:	
Attorney Docket Number:	50908.36.P13US04
Receipt Date:	18-AUG-2008
Filing Date:	21-JUL-2008
Time Stamp:	10:06:23
Application Type:	Utility under 35 USC 111(a)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Barry HOBERMAN et al.
Application No.:	12/176,645
Filed:	July 21, 2008
Title:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
Docket No.:	50908.36.P13US04

August 14, 2008

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Commissioner for Patents
P. O. Box 1450
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Information Disclosure Letter Submitted Under 37 C.F.R. §§1.97(b) and 1.98(d)

Sir:

Enclosed herewith is a listing of references within an EFS compatible Information Disclosure Statement.

As per 37 C.F.R. § 1.98(d), copies of the cited references were entered in prior applications: Application No. 11/336,097 filed 2006-01-20 (Patent 7,415, 680) which is a continuation of Application No. 10/840,893 filed 2004-05-07 (Patent 7,051,306), to which priority under 35 U.S.C. 120 is claimed. The earlier applications contain copies of the cited references.

It is requested that the information disclosed herein be made of record in this application.

Please charge any deficiency in fees and credit any overpayment to Deposit Account 503807.

Respectfully submitted,

BARRY HOBERMAN et al.

By: /Dennis R. Haszko, Reg. No. 39,575/

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	2	6631502		2003-10-07	BUFFET et al.	
	3	6667648		2003-12-23	STOUT et al.	
	4	6779163		2004-08-17	BEDNAR et al.	
	5	6820240		2004-11-16	BEDNAR et al.	
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	1	"Solving the Power Management Dilemma in System-On-Chip ASIC Design," April 2002, IBM Technology Group.	☐
	2	LACKEY et al., "Managing Power and Performance for System-on-Chip Designs using Voltage Islands," IEEE International Conference on Computer Aided Design, Technical Paper, Nov. 2002, pp. 195 - 202.	☐
	3	SEMERARO et al., "Dynamic Frequency and Voltage Control for Multiple Clock Domain Microarchitecture," 35th Annual IEEE/ACM International Symposium on Microarchitecture, Proceedings, Nov. 2002, pp. 356 - 367.	☐
	4	AKUI et al., "Dynamic Voltage and Frequency Management for Low-Power Embedded Microprocessor," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, Feb. 2004, vol. 1, pp. 64-513.	☐

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	5	TALPES et al., "Toward a Multiple Clock/Voltage Island Design Style for Power-Aware Processors," IEEE Transactions on Very Large Scale Integration (VLSI) system, May 2005, pp. 591-603, v. 13, iss. 5.	☐
	6	GUPTA, R. et al., "Low Power Wireless Networked System Design," HotChips, Aug. 18, 2002, Stanford, CA.	☐
	7	TSAI, Y-F et al., "Implications of Technology Scaling on Leakage Reduction Techniques," DAC 2003, Jun. 2-6, 2003, ACM, Anaheim, CA, USA.	☐
	8	LI, L. et al., "Managing Leakage Energy in Cache Hierarchies," Journal of Instruction-Level Parallelism, 2003, pp. 1-24, vol. 5.	☐
	9	HU, J. S. et al., "Using Dynamic Branch Behavior for Power-Efficient Instruction Fetch," Proc. of IEEECS Annual Symposium on VLSI ((ISVLSI 2003), Feb. 20-21, 2003, Tampa, FL.	☐
	10	ZHANG, W. et al., "Compiler Support for Reducing Leakage Energy Consumption," Proceedings of the 6th Design Automation and Test in Europe Conference (DATE-03), Mar. 2003, Munich, Germany.	☐
	11	DEGALAHAL, V. et al., "Analyzing Soft Errors in Leakage Optimized SRAM Design," Proceedings of the 16th International Conference on VLSI Design, Jan. 2003, New Delhi, India.	☐
	12	LI, L. et al., "Leakage Energy Management in Cache Hierarchies," 11th International Conference on Parallel Architectures and Compilation Techniques (PACT '02), Sep. 2002.	☐
	13	DUARTE, D. et al., "Impact of Scaling on the Effectiveness of Dynamic Power Reduction Schemes," Proceedings of the 20th International Conference on Computer Design (ICCD), Sep. 16-18, 2002, Frieberg, Germany.	☐
	14	DUARTE, D. et al., "Impact of Technology Scaling and Packaging on Dynamic Voltage Scaling Techniques," Proceedings of the 15th Annual IEEE International ASIC/SOC Conference, Sep. 25-28, 2002, Rochester, NY.	☐
	15	KIM, S. et al., "Predictive Precharging for Bitline Leakage Energy Reduction," Proceedings of 15th Annual IEEE International ASIC/SOC Conference, Sep. 25-28, 2002, Rochester, NY.	☐

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	16	RAMANARAYANAN, R. et al., "Characterizing Dynamic and Leakage Power Behavior in Flip Flops," Proceedings of the 15th Annual IEEE International ASIC/SOC Conference, Sep. 2002.	☐
	17	CHEN, G. et al., "Adaptive Garbage Collection for Battery-Operated Environments," Proceedings of USENIX JVM02 Symposium, Aug. 2002.	☐
	18	CHEN, G. et al., "Energy Savings Through Compression in Embedded JavaEnvironments," Proceedings of the CODES 02, Jun. 2002.	☐
	19	DE LA LUZ, V. et al., "Hardware and Software Techniques for Controlling DRAM Power Modes," IEEE Transaction on Computers, Nov. 2001, vol. 50.	☐
	20	DE LA LUZ, V. et al., "Scheduler-Based DRAM Energy Management," DAC 2002, Jun. 10-14, 2002, New Orleans, LA USA, ACM.	☐
	21	KIM, S. et al., "Partitioned Instruction Cache Architecture for Energy Efficiency," ACM Transactions on Computational Logic, Jul. 2002, pp 1-23, vol. V, No. N.	☐
	22	DE LA LUZ, V. et al., "Automatic Data Migration for Reducing Energy Consumption in Multi-Bank Memory Systems," DAC 2002, Jun. 10-14, 2002, New Orleans, LA, USA.	☐
	23	DUARTE, D. et al., "Impact of Technology Scaling in the Clock System Power," Proceedings of the IEEE Computer Society Annual Symposium on VLSI, Apr. 25-26, 2002, Pittsburgh, PA.	☐
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	26	ZHANG, W., "Exploiting VLIW Schedule Slacks for Dynamic and Leakage Energy Reduction," Proceedings of the 34th Anual International Symposium on Microarchitecture (MICRO '01), Dec. 2001.	☐

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	27	KIM, S. et al., "Energy Efficient Instruction Cache Using Page-Based Placement," Proceedings of International Conference on Compilers, Architectures and Synthesis for Embedded Systems, CASES '01, Nov. 1-17, 2001, Atlanta, GA, USA.	☐
	28	HEZAVEI, J. et al., "Input Sensitive High-Level Power Analysis," Proceedings of the 2001 IEEE Workshop on Signal Processing Systems (SiPS), Sep. 2001, pp. 149-156.	☐
	29	KIM, S. et al. "Power-Aware Partitioned Cache Architectures," Proceedings of ACM/IEEE International Symposium on Low Power Electronics and Design, 2001, ILSPED '01, Aug 6-7, 2001, Huntington Beach, CA.	☐
	30	DE LA LUZ, V., "DRAM Energy Management Using Software and Hardware Directed Power Mode Control," Proceedings of the 7th International Symposium on High Performance Computer Architecture, Jan. 20-24, 2001, Monterrey, Mexico.	☐
	31	DE MICHELI, G. et al., "System-Level Power Optimization: Techniques and Tools ," DATE 2000.	☐
	32	MANNE, S. et al., "Cool Chips Tutorial," 32nd Annual International Symposium on Microarchitecture, Nov. 15, 1999, Haifa, Israel.	☐
	33	FILSETH, E., "Tally Power into Cost of 'Free' Silicon," EETimes, Jan. 11, 1999, located at http://www.eetimes.com/story/speakout/OEG19990111S028.	☐
	34	FRENKIL, J., "A Multi-Level Approach to Low-Power IC Design," IEEE Spectrum, Feb. 1998, Vol. 35, No. 2.	☐
	35	"Managing Power in Ultra Deep Submicron ASIC/IC Design," May 2002, Synopsys, Inc.	☐
	36	PANGRLE, B. "Low-Power Design: A Holistic Approach in an Era of New Semiconductor Technologies," San Diego Telecom Council Semiconductor SIG, Nov. 14, 2002.	☐
	37	RABAEY, J., "Design Aids for Low Power: Part II Architecture and System Levels," 1997.	☐

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	38	GRUNWALD, D. et al., "Kool Chips Workshop," MICRO33, Dec. 10, 2000, Monterey, CA.	☐
	39	FLYNN, J. et al., "Power Management in Complex SoC Design," Synopsys, Apr. 2004, located at http://www.synopsis.com/sps.	☐
	40	HALTER et al., "A Gate-Level Leakage Power Reduction Method for Ultra-Low-Power CMOS Circuits," in Proc. IEEE Custom Integrated Circuits Conf., 1997, pp. 475-478.	☐
	41	HORIGUCHI et al., "Switched-Source-Impedance CMOS Circuit for Low Standby Subthreshold Current Giga-Scale LSI's," IEEE Journal of Solid-State Circuits, Nov. 1993, vol. 28, No. 11.	☐
	42	KAO et al., "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits," IEEE Journal of Solid-State Circuits, Jul. 2000, vol. 35, No. 7.	☐
	43	MUTOH, "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS," IEEE Journal of Solid-State Circuits, Aug. 1995, vol. 35, NO. 8.	☐

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Signature	/Dennis R. Haszko, Reg. No. 39,575/	Date (YYYY-MM-DD)	2008-08-15
Name/Print	Dennis R. Haszko	Registration Number	39,575

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	3790603
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	59893
Filer:	Dennis R. Haszko
Filer Authorized By:	
Attorney Docket Number:	50908.36.P13US04
Receipt Date:	16-AUG-2008
Filing Date:	21-JUL-2008
Time Stamp:	21:49:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement Letter	00372953.PDF	16471 aae4bceb4a5dcad60e58713e52bd4984756ac23e	no	1
Warnings:					
Information:					

2	Information Disclosure Statement (IDS) Filed (SB/08)	00372856.PDF	577509 4f1dfafa0249c62e781c5ba614427a70fddae721	no	8
Warnings:					
Information:					
			Total Files Size (in bytes):	593980	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/176,645	07/21/2008	Barry Alan HOBERMAN	50908.36.P13US04

CONFIRMATION NO. 3003

59893
EATON PEABODY PATENT GROUP, LLC
P.O. BOX 5249
77 Sewall Street, Suite 3000
AUGUSTA, ME 04332-5249

POWER OF ATTORNEY NOTICE

OC000000031473761

Date Mailed: 08/12/2008

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/04/2008.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/snguyen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/176,645	07/21/2008	Barry Alan HOBERMAN	50908.36.P13US04

CONFIRMATION NO. 3003

59893
EATON PEABODY PATENT GROUP, LLC
P.O. BOX 5249
77 Sewall Street, Suite 3000
AUGUSTA, ME 04332-5249

POA ACCEPTANCE LETTER

OC000000031473784

Date Mailed: 08/12/2008

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/04/2008.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/snguyen/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/SB/81 (01-06)
Approved for use through 12/31/2008. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY and CORRESPONDENCE ADDRESS INDICATION FORM

Application Number	12/176645
Filing Date	July 21, 2008
First Named Inventor	Hoberman, Barry
Title	Power Managers for an Integrated...
Art Unit	
Examiner Name	
Attorney Docket Number	50908.36.P13US04

I hereby revoke all previous powers of attorney given in the above-identified application.

I hereby appoint:

☑ Practitioners associated with the Customer Number: 59893

OR

☐ Practitioner(s) named below:

Name	Registration Number

as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to:

☑ The address associated with the above-mentioned Customer Number:

OR

☐ The address associated with Customer Number: 59893

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Applicant/Inventor.

☑ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

SIGNATURE of Applicant or Assignee of Record

Signature		Date	August 1, 2008
Name	Phillip Shaer	Telephone	(613) 599-9539
Title and Company	Secretary, MOSAID Technologies Corporation		

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 2 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/96 (01-08)
Approved for use through 07/31/2008. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Barry Hoberman/MOSAID Technologies Corporation

Application No./Patent No.: 12/176645 Filed/Issue Date: July 21, 2008

Entitled: POWER MANAGERS FOR AN INTEGRATED CIRCUIT

MOSAID Technologies Corporation, a corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☑ the assignee of the entire right, title, and interest; or

2. ☐ an assignee of less than the entire right, title and interest
(The extent (by percentage) of its ownership interest is_____ %)

in the patent application/patent identified above by virtue of either:

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

OR

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Barry Hoberman/Daniel Hillman/Jon Shiell To: Virtual Silicon Technology, Inc.
The document was recorded in the United States Patent and Trademark Office at
Reel 015345, Frame 0829, or for which a copy thereof is attached.

2. From: Virtual Silicon TEchnology, Inc. To: MOSAID Delaware, Inc.
The document was recorded in the United States Patent and Trademark Office at
Reel 017100, Frame 0155, or for which a copy thereof is attached.

3. From: MOSAID Delaware, Inc. To: MOSAID Technologies Corporation
The document was recorded in the United States Patent and Trademark Office at
Reel 017203, Frame 0427, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☑ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature	August 1, 2008 Date
Phillip Shaer Printed or Typed Name	(613) 599-9539 Telephone Number
Secretary Title	

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	3721044
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Alan HOBERMAN
Customer Number:	59893
Filer:	Dennis R. Haszko
Filer Authorized By:	
Attorney Docket Number:	50908.36.P13US04
Receipt Date:	04-AUG-2008
Filing Date:	21-JUL-2008
Time Stamp:	08:35:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		00365936.PDF	46732 07bef1f8cd8fb0a567140ca70f69848100d35cfb	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Power of Attorney	1	1
	Assignee showing of ownership per 37 CFR 3.73(b).	2	2
Warnings:			
Information:			
	Total Files Size (in bytes):	46732	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/176,645	07/21/2008	2811	2380	50908.36.P13US04	26	8

CONFIRMATION NO. 3003

59893
EATON PEABODY PATENT GROUP, LLC
P.O. BOX 5249
77 Sewall Street, Suite 3000
AUGUSTA, ME 04332-5249

FILING RECEIPT

OC000000031265987

Date Mailed: 07/30/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Barry Alan HOBERMAN, Cupertino, CA;
Daniel L. HILLMAN, San Jose, CA;
Jon SHIELL, San Jose, CA;

Assignment For Published Patent Application

MOSAID TECHNOLOGIES CORPORATION, Santa Clara, CA

Power of Attorney: The patent practitioners associated with Customer Number 22830

Domestic Priority data as claimed by applicant

This application is a CON of 11/336,097 01/20/2006 PAT 7,415,680
which is a CON of 10/840,893 05/07/2004 PAT 7,051,306
which claims benefit of 60/468,742 05/07/2003

Foreign Applications

If Required, Foreign Filing License Granted: 07/29/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/176,645**

Projected Publication Date: 11/06/2008

Non-Publication Request: No

Early Publication Request: No

Title

POWER MANAGERS FOR AN INTEGRATED CIRCUIT

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

PTO/SB/05 (04-05)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office. U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	50908.36.P13US04
First Inventor	Barry HOBERMAN
Title	Power Managers for an Integrated...
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☐ **Fee Transmittal Form** (e.g., PTO/SB/17)
   (Submit an original and a duplicate for fee processing)
2. ☐ **Applicant claims small entity status.**
   See 37 CFR 1.27.
3. ☑ **Specification** [*Total Pages* 25]
   Both the claims and abstract must start on a new page
   (For information on the preferred arrangement, see MPEP 608.01(a))
4. ☑ **Drawing(s)** (*35 U.S.C. 113*) [*Total Sheets* 13]
5. **Oath or Declaration** [*Total Sheets* 3]
   a. ☐ Newly executed (original or copy)
   b. ☑ A copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 18 completed)
   i. ☐ DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☑ **Application Data Sheet.** See 37 CFR 1.76
7. ☐ **CD-ROM or CD-R** in duplicate, large table or Computer Program *(Appendix)*
   ☐ Landscape Table on CD
8. **Nucleotide and/or Amino Acid Sequence Submission**
   (if applicable, items a. – c. are required)
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ADDRESS TO: **Commissioner for Patents**
P.O. Box 1450
Alexandria VA 22313-1450

ACCOMPANYING APPLICATION PARTS

9. ☐ **Assignment Papers** (cover sheet & document(s))
   Name of Assignee_____
10. ☐ **37 CFR 3.73(b) Statement** *(when there is an assignee)* ☐ **Power of Attorney**
11. ☐ **English Translation Document** *(if applicable)*
12. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    ☐ Copies of citations attached
13. ☐ **Preliminary Amendment**
14. ☐ **Return Receipt Postcard** (MPEP 503)
    (*Should be specifically itemized)*
15. ☐ **Certified Copy of Priority Document(s)**
    (if foreign priority is claimed)
16. ☐ **Nonpublication Request** under 35 U.S.C. 122(b)(2)(B)(i).
    Applicant must attach form PTO/SB/35 or equivalent.
17. ☐ Other:_____

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:*

☑ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 11/366,097

Prior application information: *Examiner* Sun J. LIN *Art Unit:* 2825

19. CORRESPONDENCE ADDRESS

☑ The address associated with Customer Number: 59893 ***OR*** ☐ Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone		Email	

Signature	/Dennis R. Haszko, Reg. No. 39,575/		Date	21 JUL 2008	
Name (Print/Type)	Dennis R. Haszko			Registration No. (Attorney/Agent)	39,575

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/14 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	50908.36.P13US04
	Application Number	
Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority	◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Barry	Alan	HOBERMAN	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Cupertino	State/Province	CA	Country of Residence i	US

Citizenship under 37 CFR 1.41(b) i	US

Mailing Address of Applicant:

Address 1	10290 Palo Vista Road
Address 2	

City	Cupertino	State/Province	CA

Postal Code	95014	Country i	US

Applicant 2 Remove

Applicant Authority	◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Daniel	L.	HILLMAN	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Jose	State/Province	CA	Country of Residence i	US

Citizenship under 37 CFR 1.41(b) i	US

Mailing Address of Applicant:

Address 1	6607 Winterset Way
Address 2	

City	San Jose	State/Province	CA

Postal Code	95120	Country i	US

Applicant 3 Remove

Applicant Authority	◉ Inventor	○ Legal Representative under 35 U.S.C. 117	○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jon		SHIELL	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	San Jose	State/Province	CA	Country of Residence i	US

PTO/SB/14 (07-07)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	50908.36.P13US04
	Application Number	
Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT	

Citizenship under 37 CFR 1.41(b) [i]	US		
Mailing Address of Applicant:			
Address 1	801 Seabury Drive		
Address 2			
City	San Jose	**State/Province**	CA
Postal Code	95136	**Country** [i]	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	59893		
Email Address	dhaszko@eatonpeabody.com	Add Email	Remove Email
Email Address	kwroten@eatonpeabody.com	Add Email	Remove Email

Application Information:

Title of the Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT		
Attorney Docket Number	50908.36.P13US04	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	13	**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	50908.36.P13US04
	Application Number	
Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT	

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	59893		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	11336097	2006-01-20

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11336097	Continuation of	10840893	2004-05-07	7051306	2006-05-23

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
11336097	non provisional of	60468742	2003-05-07

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			○ Yes ◉ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

If the Assignee is an Organization check here. ☒	
Organization Name	MOSAID TECHNOLOGIES CORPORATION

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	50908.36.P13US04
	Application Number	
Title of Invention	POWER MANAGERS FOR AN INTEGRATED CIRCUIT	

Mailing Address Information:			
Address 1	3255 Scott Blvd., Suite 1-105		
Address 2			
City	Santa Clara	**State/Province**	CA
Country [i]	US	Postal Code	95054
Phone Number		Fax Number	
Email Address			
Additional Assignee Data may be generated within this form by selecting the **Add** button.		Add	

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/Dennis R. Haszko, Reg. No. 39,575/			Date (YYYY-MM-DD)	2008-07-21
First Name	Dennis R.	Last Name	Haszko	Registration Number	39575

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	
Filing Date:	
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Hoberman
Filer:	Dennis R. Haszko
Attorney Docket Number:	50908.36.P13US04
Filed as Large Entity	

Utility Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	310	310
Utility Search Fee	1111	1	510	510
Utility Examination Fee	1311	1	210	210
Pages:				
Claims:				
Claims in excess of 20	1202	6	50	300
Independent claims in excess of 3	1201	5	210	1050
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2380**

Electronic Acknowledgement Receipt	
EFS ID:	3646185
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Hoberman
Customer Number:	59893
Filer:	Dennis R. Haszko
Filer Authorized By:	
Attorney Docket Number:	50908.36.P13US04
Receipt Date:	21-JUL-2008
Filing Date:	
Time Stamp:	14:53:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$2380
RAM confirmation Number	148
Deposit Account	503807
Authorized User	HASZKO,DENNIS R.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Claims	00359978.PDF	23563 307159bd88758bbc172838256708688bbe96fef8	no	6
Warnings:					
Information:					
2		00360068.PDF	1412165 fa8732093b161e66f8fafa70d5a04c0dced568a8	yes	41

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	24
Abstract	25	25
Drawings-only black and white line drawings	26	38
Oath or Declaration filed	39	41

Warnings:					
Information:					
3	Transmittal of New Application	00360108.PDF	245737 d4eff1f0037455b8293c5748188f6b532eaa4f7a	no	2
Warnings:					
Information:					
4	Application Data Sheet	00360167.PDF	837616 9a5cd6333f890aa538ddcf139fbfb5cbc4ce6f4f	no	5
Warnings:					
Information:					
5	Fee Worksheet (PTO-06)	fee-info.pdf	8546 78834f4ff8bdab5241fd545cb01b886e4a549454	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2527627		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt	
EFS ID:	3646185
Application Number:	12176645
International Application Number:	
Confirmation Number:	3003
Title of Invention:	POWER MANAGERS FOR AN INTEGRATED CIRCUIT
First Named Inventor/Applicant Name:	Barry Hoberman
Customer Number:	59893
Filer:	Dennis R. Haszko
Filer Authorized By:	
Attorney Docket Number:	50908.36.P13US04
Receipt Date:	21-JUL-2008
Filing Date:	
Time Stamp:	14:53:41
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$2380
RAM confirmation Number	148
Deposit Account	503807
Authorized User	HASZKO,DENNIS R.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Claims	00359978.PDF	23563 307159bd88758bbc172838256708688bbe96fef8	no	6
Warnings:					
Information:					
2		00360068.PDF	1412165 fa8732093b161e66f8fafa70d5a04c0dced568a8	yes	41

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	24
Abstract	25	25
Drawings-only black and white line drawings	26	38
Oath or Declaration filed	39	41

Warnings:					
Information:					
3	Transmittal of New Application	00360108.PDF	245737 d4eff1f0037455b8293c5748188f6b532eaa4f7a	no	2
Warnings:					
Information:					
4	Application Data Sheet	00360167.PDF	837616 9a5cd6333f890aa538ddcf139fbfb5cbc4ce6f4f	no	5
Warnings:					
Information:					
5	Fee Worksheet (PTO-06)	fee-info.pdf	8546 78834f4ff8bdab5241fd545cb01b886e4a549454	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2527627		

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New Applications Under 35 U.S.C. 111
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National Stage of an International Application under 35 U.S.C. 371
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New International Application Filed with the USPTO as a Receiving Office
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What is claimed is:

1. A software product for building an integrated circuit including a plurality of power islands, the software product comprising:

circuit design software operational when executed by a processor to direct the processor to select blocks of predetermined circuits to form

power control circuitry configured to control power for one of the power islands and

a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions is chosen from a group consisting of selecting a frequency for one of the power islands, selecting a voltage for one of the power islands, and selecting a transistor threshold voltage for one of the power islands.

2. The software product of **Claim 1** wherein the power islands are delineated based on geographic factors of the integrated circuit.

3. The software product of **Claim 1** wherein the power islands are delineated based on functional circuitry of the integrated circuit.

4. The software product of **Claim 1** wherein the power islands comprise power sub-islands.

5. The software product of **Claim 1** wherein the power islands comprise multiple clock domains.

6. The software product of **Claim 1** wherein another one of the actions comprises selecting a clock for the one of the power islands.

7. The software product of **Claim 1** wherein another one of the actions comprises modifying a first voltage for the one of the power islands.

8. The software product of **Claim 7** wherein the first voltage comprises a source voltage.

9. The software product of **Claim 7** wherein the first voltage comprises a threshold voltage.

10. The software product of **Claim 1** wherein another one of the actions comprises powering on the one of the power islands.

11. The software product of **Claim 1** wherein another one of the actions comprises powering off the one of the power islands.

12. The software product of **Claim 1** wherein another one of the actions comprises changing the one of the power islands to a sleep mode.

13. The software product of **Claim 1** wherein the power management software is operational when executed by the processor to direct the processor to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the at least one of the actions based on the crossing of the threshold level.

14. The software product of **Claim 1** wherein the power management software is operational when executed by the processor to direct the processor to save a state of components within the one of the power islands.

15. The software product of **Claim 1** wherein the power management software is operational when executed by the processor to direct the processor to restore a state of components within the one of the power islands.

16. A software product for building an integrated circuit including a plurality of power islands, the software product comprising:

circuit design software operational when executed by a processor to direct the processor to

select blocks from a group of predetermined circuits;

write a register transfer level description (RTL) formed from the blocks, the RTL representing

power control circuitry configured to control power for one of the power islands, and

a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions is chosen from a group consisting of selecting a frequency for one of the power islands, selecting a voltage for one of the power islands, and selecting a transistor threshold voltage for one of the power islands;

simulate and debug the RTL;

synthesize the RTL on a power island basis;

measure power island performance and update the RTL representing the power manager based upon the measured performance;

synthesize the RTL updated with regard to measured performance; and

forming the integrated circuit from the updated RTL.

17. The software product of **Claim 16** wherein selecting blocks from the group of predetermined circuits further comprising applying custom logic.

18. The software product of **Claim 17** wherein applying custom logic further comprising specifying circuit operating specifications.

19. The software product of **Claim 16** further comprising adding annotations for the power manager.

20. The software product of **Claim 19** wherein the annotations include functionality options.

21. A system for an integrated circuit comprising a plurality of power islands, the system comprising:

a first power manager configured to manage a first power consumption for the integrated circuit based on needs and operation of the integrated circuit; and

a second power manager configured to communicate with the first power manager, to manage a second power consumption for one of the power islands, to register capabilities of the second power manager with the first power manager, and to restore the registered capabilities of the second power manager after power off periods.

22. A method for operating an integrated circuit comprising a plurality of power islands, the method comprising:

in a first power manager,

managing a first power consumption for the integrated circuit based on needs and operation of the integrated circuit;

communicating between the first power manager and a second power manager; and

in the second power manager,

managing a second power consumption for one of the power islands;

registering capabilities of the second power manager with the first power manager;

restoring the registered capabilities of the second power manager after power off periods.

23. A system for an integrated circuit comprising a plurality of power islands, the system comprising:

a first means for managing a first power consumption for the integrated circuit based on needs and operations of the integrated circuit; and

a second means for communicating with the first means, managing a second power consumption for one of the power islands, registering capabilities of the second power manager with the first power manager, and restoring the registered capabilities of the second power manager after power off periods.

24. A system for an integrated circuit comprising a plurality of power islands, the system comprising:

a first power manager configured to manage a first power consumption for the integrated circuit based on needs and operation of the integrated circuit; and

a second power manager configured to communicate with the first power manager, to manage a second power consumption for one of the power islands, to register capabilities of the second power manager with the first power manager, and to interface with a software for debugging the power island.

25. A method for operating an integrated circuit comprising a plurality of power islands, the method comprising:

in a first power manager,

managing a first power consumption for the integrated circuit based on needs and operation of the integrated circuit;

communicating between the first power manager and a second power manager; and

in the second power manager,

managing a second power consumption for one of the power islands;

registering capabilities of the second power manager with the first power manager;

interfacing with a software for debugging the power island.

26. A system for an integrated circuit comprising a plurality of power islands, the system comprising:

a first means for managing a first power consumption for the integrated circuit based on needs and operations of the integrated circuit; and

a second means for communicating with the first means, managing a second power consumption for one of the power islands, registering capabilities of the second power manager with the first power manager, and interfacing with a software for debugging the power island.

POWER MANAGERS FOR AN INTEGRATED CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Application Serial Number 11/336,097 filed on January 20, 2006 entitled "Power Managers for an Integrated Circuit" and which issued on _____ as U.S. Patent Number _____, which is a continuation of U.S. Application Serial Number 10/840,893 filed on May 7,2004 and entitled "Managing Power on Integrated Circuits Using Power Islands" and which issued on May 23, 2006 as U.S. Patent Number 7,051,306 which claims the benefit of U.S. Provisional Application Serial Number 60/468,742 titled "System and Method for Managing Power in Integrated Circuits," filed May 7, 2003, which are each hereby incorporated by reference.

BACKGROUND

1. Field of the Invention

[0002] The present invention relates generally to integrated circuits, and more particularly to managing power on integrated circuits using power islands.

2. Description of the Prior Art

[0003] One design goal for integrated circuits is to reduce power consumption. Devices with batteries such as cell phones and laptops especially need a reduction in power consumption in the integrated circuit to extend the charge of the battery. Additionally, a reduction in power consumption prevents overheating and lowers the heafdissipation of the integrated circuit, which in some cases, eliminates or simplifies the heat sinks and/or fans for the integrated circuit.

[0004] Some integrated circuits are designed using building blocks of library cells. These library cells are blocks of circuitry performing a function. Some examples of library cells are NAND gates, multiplexers, decoders, comparators, and memory.

[0005] In a "full-custom" flow, the integrated circuit is designed at the lowest level such as at the individual transistors, capacitors, and resistors level. The "full-custom" flow may use library cells that are internally developed. The integrated circuit can have optimal performance because the integrated circuit is designed in great detail at the lowest level. However, some problems with the "full-custom" flow are the long time and expensive costs associated with designing at such a detailed level. Furthermore, the "full-custom" flow is cumbersome because the design is at the lowest level.

[0006] In a "standard-cell" flow, the integrated circuit is designed using library cells acquired from a third party or other outside source. These library cells are standardized at the logic or function level. The design time for the standard-cell flow is reduced because the library cells are already pre-designed and pre-tested.

[0007] In one example for designing an integrated circuit, the library cells are selected, and the custom logic is specified to build the integrated circuit. The register transfer level (RTL) for the integrated circuit is then written for simulation and debugging. After simulation and debugging, the synthesis is run for the integrated circuit. Performance measurement software is executed to determine performance of the integrated circuit. The final synthesis of the integrated circuit can then be run based on the optimal performance of the integrated circuit.

[0008] One problem with many integrated circuits is that power consumption is not efficiently utilized. For example, the entire integrated circuit may operate at a maximum frequency just to support an application needing that maximum frequency, while other portions of the integrated circuit can operate at a lower frequency. In another example, inactive circuitry within the integrated

circuit consumes power and increases the likelihood of leakage. Inefficient power consumption may also adversely affect performance of the integrated circuit.

[0009] With the growing complexity of integrated circuits, the reduction of power consumption is even more important when the integrated circuit employs more functionality. One example of an integrated circuit is a system-on-a-chip that includes a microprocessor, memory, I/O interfaces, and an analog-to-digital converter all in a single chip. With many different types of functionality employed within a single chip, the system-on-a-chip consumes even more power than single function integrated circuits.

[00010] Some prior integrated circuits have employed voltage islands or multiple clocks to lower power consumption. One problem with these integrated circuits is that the voltages in the power island and the frequencies of the multiple clocks are static. The voltages and the frequencies do not dynamically change based on the needs and operation of the integrated circuit.

SUMMARY OF THE INVENTION

[00011] The invention addresses the above problems by providing power managers for an integrated circuit. A system for an integrated circuit comprising a plurality of power islands includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

[00012] The first power manager may determine power trade offs between the power islands. The second power manager may determine status information about the one of the power islands and may transmit the status information to the first power manager. The first power manager may receive the status information and may manage the first power consumption for the integrated circuit using the status information. The first power manager may determine status information about the integrated circuit and may transmit the status information to power interface software. The first power manager may receive a message from power interface software to change the first power consumption for the integrated circuit. The first power manager may transmit a message to the second power manager and the second power manager may receive and process the message to change the second power consumption for the one of the power islands. The second power manager may register capabilities of the second power manager with the first power manager.

BRIEF DESCRIPTION OF THE DRAWINGS

[00013] FIG. 1 is a block diagram of a system for managing power in an integrated circuit in an exemplary implementation of the invention;

[00014] FIG. 2 is a diagram of a system for managing power in an integrated circuit in an exemplary implementation of the invention;

[00015] FIG. 3 is an illustration for low leakage circuitry for a low power standard cell logic block in an exemplary implementation of the invention;

[00016] FIG. 4 is a diagram of a power island in an exemplary implementation of the invention;

[00017] FIG. 5 is a flowchart from an application request to a slave power manager action in an exemplary implementation of the invention;

[00018] FIG. 6 is an illustration of internal circuitry for a smart power unit in an exemplary implementation of the invention;

[00019] FIG. 7 is an illustration of external circuitry for a smart power unit in an exemplary implementation of the invention;

[00020] FIG. 8 is a flowchart from an application request to a smart power unit action in an exemplary implementation of the invention;

[00021] FIG. 9 is a flowchart for saving an IP unit's state prior to powering down and restoring the IP unit's state when powering up in an exemplary implementation of the invention;

[00022] FIG. 10 is diagram of a system on a chip and an extended local memory in an exemplary implementation of the invention;

[00023] FIG. 11 is a flowchart for generating a "hot spot" report from an intermediate power manager to a power management control layer in an exemplary implementation of the invention.

[00024] FIG. 12 is a diagram of a system on a chip in an exemplary implementation of the invention; and

[00025] FIG. 13 is a flowchart for building a chip with power islands in an exemplary implementation of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[00026] As shown in the exemplary drawings wherein like reference numerals indicate like or corresponding elements among the figures, exemplary embodiments of a system and method according to the present invention are described below in detail. It is to be understood, however, that the present invention may be embodied in various forms. Therefore, specific details disclosed herein are not to be interpreted as limiting, but rather as a basis for the claims and as a representative basis for teaching one skilled in the art to employ the present invention in virtually any appropriately detailed system, structure, method, process or manner.

[00027] FIG. 1 depicts a block diagram of a system 100 for managing power in an integrated circuit 110 in an exemplary implementation of the invention. The system 100 includes an integrated circuit 110 and a power manager 120. The integrated circuit 110 is any electronic device that is instantiated into silicon and/or related manufacturing materials. One example of the integrated circuit 110 is a system-on-a-chip. The integrated circuit 110 includes multiple IP units, which are blocks of circuitry performing specific functions.

[00028] The integrated circuit 110 includes four power islands 112, 114, 116, and 118. FIG. 1 only depicts four power islands 112, 114, 116, and 118 for the sake of simplicity. Other embodiments of the integrated circuit 110 include a plurality of power islands 112, 114, 116, and 118. The power islands 112, 114, 116, and 118 are coupled to a bus 125.

[00029] A power island 112, 114, 116, and 118 is any section, delineation, partition, or division of the integrated circuit 110 where power consumption is controlled within the section, delineation, partition, or division. In some embodiments, the power islands 112, 114, 116, and 118 are delineated based on geographic factors of the integrated circuit 110. In some embodiments, the power islands 112, 114, 116, and 118 are delineated based on functional IP units of the integrated circuit 110. In one example depicted in FIG. 10, power islands are delineated by memory, a

microprocessor, and separate IP blocks. In some embodiments, the power islands 112, 114, 116, and 118 are asynchronous or synchronous to each other. In some embodiments, the power islands 112, 114, 116, and 118 comprise sub-islands of power to provide further specificity in controlling power in the integrated circuit 110. In some embodiments, each of the power islands 112, 114, 116, and 118 supports multiple clock domains with its own control. In some embodiments, the clocks within the power islands 112, 114, 116, and 118 are variable.

[00030] In some embodiments, each of the power islands 112, 114, 116, and 118 includes power control circuitry. Power control circuitry is any circuitry configured to control power within one of the power islands 112, 114, 116, and 118. Some examples of power control circuitry include circuitry for level shifting, signal isolation, Vdd multiplexing, clock multiplexing, and dynamic back bias. In some embodiments, the power control circuitry is included in a standard cell library for standard cell design of the integrated circuit 110.

[00031] The power manager 120 is also coupled to the bus 125. One example of the bus 125 is a power command bus described in further detail below in FIG. 10. Other embodiments of the system 100 include numerous variations in which the power manager 120 and the power islands 112, 114, 116, and 118 are interconnected. The power manager 120 is any circuitry, device, or system configured to (1) determine a target power level for one of the power islands 112, 114, 116, and 118 where power consumption is independently controlled within each of the power islands 112, 114, 116, and 118, (2) determine action to change a consumption power level of the one of the power islands 112, 114, 116, and 118 to the target power level, and (3) perform the action to change the consumption power level of the one of the power islands 112, 114, 116, and 118 to the target power level. The power manager 120 can dynamically change the power consumption of the power islands 112, 114, 116, and 118 based on the needs and operation of the integrated circuit 110. The target power level is a desired, calculated, or specified power consumption of the power islands

112, 114, 116, and 118. Some examples of the power manager 120 are the slave power manager (SPM), the intermediate power manager (IPM), and the master power manager (MPM), which are described in further detail below. The power manager 120 may be a hierarchy or group of power managers 120. Although FIG. 1 depicts the power manager 120 as being located outside the integrated circuit 110, other embodiments may have the power manager 120 located in the integrated circuit 110. In other embodiments, the power manager 120 may be distributed among multiple power managers that are on or off the integrated circuit 110 or integrated with a CPU.

[00032] The action is any instruction, message, process, function, signal, or variable that controls power consumption in the power island 112, 114, 116, and 118. Some examples of actions are clock gating and dynamic clock selection. Another example of an action is modifying a clock frequency of one of the power islands 112, 114, 116, and 118. Another example of an action is to modify voltage of one of the power islands 112, 114, 116, and 118 such as dynamic voltage source, Vdd, selection. Another example of an action is to control dynamic leakage by controlling variable Vt transistors.

[00033] FIG. 2 depicts a diagram of a system 200 for managing power in an integrated circuit 250 in an exemplary implementation of the invention. The system 200 includes an embedded firmware stack 210 and an integrated circuit 250. The embedded firmware stack 210 includes software layers that run on a central processing unit (CPU). In some embodiments, the embedded firmware stack 210 may include an application layer 212, an operating system (OS) sub-system 216, a power management control layer (PMCL) 218, a real-time operating system (RTOS) 220, I/O drivers 222, and power manager (PM) firmware 224 for the MPM, IPM and/or SPM.

[00034] The integrated circuit 250 includes a power island 260, a power island 270, and a MPM 280. The power island 260 includes a low power standard cell logic block 262 and a SPM 264. The power island 270 includes a low power memory block 272 and a SPM 274. The low

power standard cell logic block 262 and the low power memory block are coupled to an interface 265. The MPM 280 is coupled to the PMCL 218, the SPM 264, and the SPM 274.

[00035] In some embodiments, the application layer 212 includes a global power application layer (GPAL) 214. This GPAL 214 may be useful for more complex applications. If the GPAL 214 is present, then all calls to the PMCL 218 application program interfaces (API) are first directed to the GPAL 214. Both the GPAL 214 and the PMCL 218 provide power management for the integrated circuit 250. In some embodiments, the GPAL 214 and/or the PMCL 218 monitor what load is on each power island 260 and 270. Also, the GPAL 214 and/or the PMCL 218 may build a history of power levels on the power island 260 and 270 and store the history data in a database. The GPAL 214 and the PMCL 218 may also provide data for on-demand resources interested in the power levels of the power islands 260 and 270.

[00036] In some embodiments when the GPAL 214 is present, the GPAL 214 provides guidance to the PMCL 218 in making local decisions for power management of the integrated circuit 250. In some embodiments, the GPAL 214 and the PMCL 218 include complex algorithms for a static schedule. The GPAL 214 and the PMCL 218 provide the facility for use code to interact and control power behavior and parameters including providing a database and statistics.

[00037] The PMCL 218 also collects information from the MPM 280 and provides commands to the MPM 280 for possible IPMs, SPMs 264 and 274, and the power islands 260 and 270. Some of the commands may be to power on/off, change the power level, or change the frequency of the power islands 260 and 270. In some embodiments with a smart power unit (SPU) 290, the GPAL 214 and the PMCL 218 are responsible for communication with the SPU 290 to implement a power policy and collect information on the actual power supply. The SPU 290 is described in further detail below in FIGS. 6-8. In some embodiments, the GPAL 214 and the PMCL 218 provides sockets for existing power management techniques.

[00038] The power manager firmware 224 is firmware executed by the master power manager 280, the intermediate power manager, and the slave power managers 264 and 274.

[00039] The MPM 280 is any circuitry configured to control the "global" power behavior of the entire integrated circuit 250. In some embodiments, there are multiple MPMs 280 that control the power behavior of the entire integrated circuit 250. In some embodiments, the MPM 280 communicates with existing IPMs and SPMs 264 and 274 to control power within the power islands 260 and 270. The MPM 280 may receive status information about the power islands 260 and 270 from the SPMs 264 and 274 and the IPMs. The MPM 280 may also determine power trade-offs between the IPMs and the SPMs 264 and 274.

[00040] The MPM 280 may also provide a main interface to the PMCL 218 firmware. In some embodiments, the MPM 280 communicates with the PMCL 218 to accept commands (e.g.. memory mapped commands) and provide status information about the power within the integrated circuit 250. In some embodiments, the MPM 280 communicates with the PMCL 218 through the main bus for the integrated circuit 250. The MPM 280 may also register each of the SPMs 264 and 274 and IPMs and capabilities with the PMCL 218. Some operations of the MPM 280 are described in further detail below in FIGS. 5, 8, 9, and 11. In some embodiments, the MPM 280 reads and writes scan chains for state save and restore along with the local logic analyzer ability.

[00041] Some embodiments may include an IPM (not shown) that coordinates SPMs 264 and 274 on behalf of the MPM 280. In some embodiments, the IPM controls and coordinates power behavior on portions of the area controlled by the MPM 280. In some embodiments, the IPM controls the SPMs 264 and 274 that are on a separate chip from the MPM 280.

[00042] The SPM 264 is any circuitry configured to control power within a power island 264 in the integrated circuit 250. One example of the SPM 264 is an IP block that controls power within a power island 264 in the integrated circuit 250. The SPM 264 may include signal buffering, level

shifting, and signal isolation. In some embodiments, the SPM 264 is integrated into scan chains to provide easier implementation and integration. Also, in some embodiments, the SPM 264 has a very small "footprint" with a low gate count and low power. In some embodiments, the SPM 264 comprises a command interface to communicate status information, service requests, and commands. Some of the commands are load, sleep, and idle. The SPM 264 may also recognize its own address to allow for multi-drop bussing.

[00043] In some embodiments, the SPM 264 has registration capabilities. For registration at power-up, the SPM 264 uses callback registration that is typically used for off chip SPMs and IPMs. For static registration when the integrated circuit is generated for on chip SPMs, the SPM 264 registers what the SPM 264 can do, what the IPM can do, and the type of commands that the SPM 264 or IPM can service. The SPM 264 may also have save and restore functions for power off periods. The SPM 264 may have watch-dog timer(s). In some embodiments, the SPM 264 has a debug interface coordination to the power island 260. The SPM 264 may also monitor local state and collect information for components within the power island 260. The SPM 264 may also locally control Vdd, clocks for frequency selection, and dynamic back biasing. The description for the SPM 264 also applies to the SPM 274 for the power island 270.

[00044] In some embodiments, the SPM 264 checks whether an event occurs when the collected information from the power island 260 crosses a threshold or exceeds a range. In some embodiments, the SPM 264, IPMs, or the MPM 280 monitors power consumption levels of the power island 260 to check whether the power consumption levels cross a threshold level or exceed a range. A power consumption level is any information, data, or statistic that indicate the power consumed in a power island 260. Some examples of power consumption levels are temperature and power. The threshold or range may be programmable. The SPM 264 may report the event asynchronously, or another element such as the MPM 280 may solicit whether an event has

occurred. The event may also be a multi-level test such as the conditions occur at a greater than a given, programmable frequency or exceed a given, programmable duration.

[00045] In some embodiments, the low power standard cell logic block 262 one example of a standard cell library that may be included in the power island 260. In some embodiments, the standard cell library is optimized for lower power. The standard cell library may be characterized over a range of operating voltages. In some embodiments, the standard cell library includes synchronous circuits and/or asynchronous circuits. In some embodiments, the standard cell library includes static circuits and/or encapsulated, dynamic logic circuits. The standard cell library may also include multiple voltage domain interface circuits such as level shifters and signal isolation circuits. The standard cell library may also have a multi-threshold design and characterization such as standard Vt, high Vt, low Vt, and variable Vt circuits. The standard cell library may also include data retention (shadow) circuits and anti-glitch circuits. The standard cell library may also include low leakage "sleep" circuits. FIG. 3 depicts an illustration of low leakage circuitry 300 for the low power standard cell logic block 262 in an exemplary implementation of the invention.

[00046] FIG. 4 depicts a diagram of the power island 270 in an exemplary implementation of the invention. The power island 270 includes a low power memory block 272 and the SPM 274. The low power memory block 272 includes banked architectures 410, 420, 430, and 440 for memories and sleep, power down circuitry 450. In some embodiments, the memory in the power island 270 is RAM and/or ROM. Some examples of the RAM are the SRAM compilers such as single-port, 2-port, and dual-port. Some examples of the ROM are ROM compilers. Some memories in the power island 270 are optimized for low power such as the low power memory block 272. In one embodiment, the low power memory block 272 includes multiple bank architectures via the compiler such as banked architectures 410, 420, 430, and 440. The memories in the power island 270 may also include sleep, power down circuitry 450 for low power modes such as sleep, nap, and

full power down. The memories in the power island 270 may also include programmable read/write ports. The memories in the power island 270 may also be an asynchronous and/or synchronous design.

[00047] In some embodiments, the system 200 also includes a smart power unit (SPU) 290. In some embodiments, the SPU 290 is off-chip to the integrated circuit 250. The SPU 290 is an external unit configured to control power and clock distribution to the integrated circuit. The circuitry of the SPU is described in further detail below in FIGS. 7 and 8.

[00048] FIG. 5 depicts a flowchart from an application request to an SPM action in an exemplary implementation of the invention. FIG. 5 begins in step 500. In step 502, an application is invoked such as playing a movie. In step 504, the application determines the required frequency for performance of an IP unit. For example, the application determines a specified frequency in MHz for IP unit for an MPEG decoder. In some embodiments, when the IP unit is totally asynchronous, the required frequency will be an artificial measure of performance. In some embodiments that have multiple clocks involved, the minimum performance for each clock is specified.

[00049] In step 506, the application invokes the PMCL 218 API call. One example of this call is "Set_Rate (unit Y, N MHz, degree of dynamic power management (DPM) allowed, DPM threshold, other information to allow DPM trade-offs, starting back bias for SPMs with dynamic bias, wait for power up flag)." In this example, the other information could be "no power off, use high Vt and clocks off instead" and "major waits are about 10 us, with a 400 ns threshold." In some embodiments with multiple clocks, the PMCL 218 API call allows the application to specify all required frequencies.

[00050] The PMCL 218 determines possible trade-offs available for the unit and selects a frequency rate, Vdd, and Vt if applicable for the unit that best meets the given requirements in step 508 and determines the applicable SPMs 264 and 274 in step 510. In some embodiments, the MPM

280 or IPM performs steps 508 and 510. In some embodiments for multiple clocks, the Vdd and Vt specified would allow for all specified clocks to meet or exceed their required frequencies.

[00051] In step 512, the PMCL 218 then writes the desired setting for the SPMs 264 and 274 to the MPM 280 (or IPM). In step 514, the MPM 280 (or IPM) converts the request into one or more commands for the SPMs 264 and 274 (or IPM) associated with the unit.

[00052] In step 516, if the application sets the wait for power up flag, the PMCL 218 then waits until the IP unit is fully powered up before returning from the call. Otherwise, the call returns as soon as the command is acknowledged, with status of 0 for okay, 1 for fast power-up, 2 for slow power-up, or 3+ for error conditions. The powered up state is when the unit is at the desired Vdd for the requested frequency, and not just that the unit is turned on.

[00053] In step 518, the MPM 280 (or IPM) sends the requests to the appropriate targets. In step 520, the MPM 280 waits for the receipt of the acknowledgements that indicate message received and executed or execution has begun. A NACK or negative acknowledgement may also be returned from the SPM 264 and 274.

[00054] In step 522, the SPM 264 receives the commands and performs the actions. Steps 524-528 are possible actions that the SPM 264 may perform. In step 524, the SPM 264 switches the Vdd mux. In step 526, the SPM 264 switches a clock mux. In some embodiments when the voltage goes down, step 526 is performed before step 524. In step 528, the SPM 264 changes the Vt on the associated transistors. After the SPM 264 performs the actions, the SPM 264 returns a status message upstream indicating acknowledgement or negative acknowledgement in step 530. FIG. 5 ends in step 532.

[00055] FIG. 6 depicts an illustration of internal circuitry 600 for an SPU 290 in an exemplary implementation of the invention. In this embodiment, the internal circuitry 600 for the SPU 290 is internal to the integrated circuit 250 of FIG. 2. The internal circuitry 600 includes an

external voltage 610, a dropout voltage regulator 620, a dropout voltage regulator 630, a logic block 640, and a logic block 650.

[00056] FIG. 7 depicts an illustration of external circuitry 700 for an SPU 290 in an exemplary implementation of the invention. In this embodiment, the external circuitry 700 for the SPU 290 is external to the integrated circuit 250 of FIG. 2. The internal circuitry 700 includes an external voltage 710, a power supply pin 720, a power supply pin 730, a power supply pin 740, a logic block 750, a logic block 760, and a logic block 770. The external circuitry 700 for the SPU 290 provides a DC/DC conversion. The DC/DC conversion provides multiple independent power supply pins 720, 730, and 740. The power supply pins 720, 730, and 740 have a variable voltage supply on each separate power pin. Also, in some embodiments, the variable voltage is within a range and in steps. In some embodiments, the PMCL 218 controls the voltage to power supply pins 720, 730, and 740.

[00057] FIG. 8 depicts a flowchart from an application request to an SPU action in an exemplary implementation of the invention. FIG. 8 begins in step 800. In step 802, an application is invoked. In step 804, the application determines the required frequency for performance of an IP unit. For example, the application determines a specified frequency in MHz for IP unit for an MPEG decoder.

[00058] In step 806, the application invokes the PMCL 218 API call. One example of this call is "Set_Rate (unit Y, N MHz, degree of dynamic power management (DPM) allowed, DPM threshold, other information to allow DPM trade-offs, starting back bias for SPMs with dynamic bias, wait for power up flag)." In this example, the other information could be "no power off, use high Vt and clocks off instead" and "major waits are about 10 us, with a 400 ns threshold."

[00059] The PMCL 218 determines possible trade-offs available for the unit and selects a the lowest possible Vdd that will support the requested frequency in step 808 and determines the SPMs 264 and 274 that will be affected and which power PINs to change in step 810.

[00060] In step 812, the PMCL 218 sends a command to the MPM 280 to have the SPMs 264 and 274 (and IPM) to prepare for a Vdd change. In step 814, the PMCL 218 waits for the acknowledgement from the MPM 280. In step 816, the PMCL 218 sends a command to the SPU 290 to change the Vdd on the selected power pins and waits for the affected area to "settle down." In step 818, the PMCL 218 then sends a "resume operation at a specified frequency" command to the MPM 280. In step 820, the MPM 280 propagates the resume command to all affected SPMs 264 and 274 (and IPMs). In step 822, one of the power managers (i.e. MPM 280, IPM, or SPMs 264 and 274) sets the specified frequency. In step 824, the IP unit operation resumes after the clock has settled. FIG. 8 ends in step 826. In some embodiments, the user application has the option of waiting for the entire operation to finish or to continue and either query the PMCL 218 as to the progress of the operation or wait for a "finished" interrupt from the PMCL 218.

[00061] FIG. 9 depicts a flowchart for saving an IP unit's state prior to powering down and restoring the IP unit's state when powering up in an exemplary implementation of the invention. FIG. 9 begins in step 900. In step 902, the user application requests that the PMCL 218 power off an IP unit and wants to save the IP unit's state. In some embodiments, the reconfiguration of the IP unit takes a long time. The request in step 902 may be accompanied by the address of an area to which the state should be saved.

[00062] In step 904, the PMCL 218 sends a "stop clock and read IP unit state" message to the MPM 280. The MPM 280 then propagates the "stop clock and read IP unit state" message to the SPMs 264 and 274 of the affected unit in step 906. In step 908, the MPM 280 uses the scan chain for the IP unit to read the state into a register or buffer for presentation to the PMCL 218. In step

910, if the PMCL 218 provided the MPM 280 with the address of the save area, the MPM 280 saves the state information directly in the specified area. In step 912, after all of the IP units' state has been saved, the PMCL 218 sends a "power off IP unit" message to the MPM 280. In step 914, the MPM 280 then propagates out the "power off IP unit" message. In step 916, the PMCL 218 returns the save state area to the user application. The save state area contains the state of the unit.

[00063] At a later time, in step 918, the user application requests that the PMCL 218 power the IP unit back up and restore the state of the IP unit. In some embodiments, the user application request includes the address of the area to which the state was saved. In step 920, the PMCL 218 sends a "power up IP unit with clocks off and restore state" message to the MPM 280. In step 922, the MPM 280 propagates the "power up IP unit with clocks off and restore state" message to the SPMs 264 and 274 of the affected IP unit. In step 924, after the IP unit is powered up, the MPM 280 uses the scan chain to reload the unit's state. In some embodiments, the reloading of the unit's state originates directly from the save area or from information passed to the MPM 280 from the PMCL 218. In step 926, the PMCL 218 sends a message to the MPM 280 to turn clock back on and report to user application that the IP unit is ready to continue operations. FIG. 9 ends in step 928.

[00064] In some embodiments, the same functionality of FIG. 9 can be used to implement an internal "logic analyzer" function, in which the IP unit in question would not be powered down after being read. If the associated SPMs 264 and 274 of the IP unit have the ability to single- or multi-step the clock, the local scan testing is performed by having the SPMs 264 and 274 "signal isolate" the IP unit. Then, use of a combination of the ability of single- or multi-step the clock and the ability to use the scan chain can read/write the IP unit's internal state.

[00065] FIG. 10 depicts a diagram of a system-on-a-chip (SOC) 1000 and an extended local memory 1004 in an exemplary implementation of the invention. The SOC 1000 is one example of the integrated circuit 250 and communicates with the embedded firmware stack 210 in FIG. 2 as

described above. The SOC 1000 includes a CPU 1010, a local memory 1020, a memory controller 1030, a mixed signal circuitry 1040, an application specific circuitry 1050, a PCI-X circuitry 1060, a MPM 1070, a real-time clock (RTC) 1075, an Ethernet circuitry 1080, and a USB circuitry 1090. The CPU 1010, the local memory 1020, the memory controller 1030, the mixed signal circuitry 1040, the application specific circuitry 1050, the PCI-X circuitry 1060, the Ethernet circuitry 1080, and the USB circuitry 1090 are all power islands in which power is controlled within the power islands by power managers. In this embodiment, the power islands are delineated by the functionality of a part of the SOC 1000.

[00066] The extended local memory 1004 includes an IPM 1006 that is coupled to the bus 1071. The CPU 1010 includes an SPM 1015 that is coupled to the bus 1071. The local memory 1020 includes an SPM 1025 that is also coupled to the bus 1071. The memory controller 1030 comprises an SPM 1035 that is coupled to the bus 1071. The mixed signal circuitry 1040 includes an SPM 1045 that is coupled to the bus 1071. The application specific circuitry 1050 includes an IPM 1055 and an SPM 1058 that are both coupled to the bus 1072. The PCI-X circuitry 1060 includes an SPM 1065 that is coupled to the bus 1072. The MPM 1070 is coupled to the bus 1071 and the bus 1072. The MPM 1070 is one example of the MPM 280 as described above. The Ethernet circuitry 1080 includes an SPM 1085 that is coupled to the bus 1072. The USB circuitry 1090 includes an SPM 1095 that is coupled to the bus 1072.

[00067] In this embodiment, power command buses comprise the bus 1071 and the bus 1072. The bus 1071 and 1072 are simple multi-drop serial buses that may cross chip boundaries and interconnect power managers. The power command bus may be a combination of serial busses, such as the bus 1071 and the bus 1072, with one per region of the chip and then multi-drop within the region. In other embodiments, the power command bus includes a parallel bus or a combination of serial and parallel busses. In some embodiments, the power command bus is the system bus. The

power command bus may contain messages with at least a unit ID with the associated payload. For a fixed point to point bus, the message does not need a unit ID only the payload.

[00068] In some embodiments, the power command bus uses an error detection scheme such as parity, ECC, or a redundant code. In some embodiments, the power command bus is a low performance bus that does not interfere with the integrated circuit design and is not visible to the user. In some embodiments, the communication between the PMCL 218 and the MPM 1070 is memory mapped and based on the main bus such as an AHB for an SOC 1000.

[00069] Some embodiments may include a separate bus for reporting status information between the power managers. In one example, this separate bus provides asynchronous "Alert" type status messages from SPMs to the MPM.

[00070] There can be various message formats for the power command bus. In one example for a basic format, the message format includes a start of message indicator, a power manager address, type code, basic command, and an end of message indicator. In one example for an extended format, the message format includes the basic format, an additional length, and additional information. In one example for a response message format, the message format includes a start of message reply indictor, a power manager address, a 3b ACK or NAK or return status (implied ACK), a payload length for return status messages, a payload for return status messages, a reason code for NAK, and an end of message indicator.

[00071] In some embodiments, the SPM 1015 or the IPM 1006 times out on replying to a command, and the MPM 1070 reissues the command a programmable number of times. If the SPM 1015 or the IPM 1006 still fails, the MPM 1070 marks the SPM 1015 or the IPM 1006 as unusable and reports back the failure to the PMCL 218. In one embodiment, the PMCL 218 has the MPM 1070 reinitialize the failing SPM 1015 or the IPM 1006 via the scan system and then retries sending the message. Other conditions such as invalid responses to commands or invalid status reports are

also handled by the re-initialization. In some embodiments, the state of the failing SPM 1015 or the IPM 1006 may be read out and saved for later analysis.

[00072] FIG. 11 depicts a flowchart for generating a "hot spot" report from an IPM 1055 to the PMCL 218 in an exemplary implementation of the invention. FIG. 11 begins in step 1100. In step 1102, the IPM 1055 monitors the temperature statistics of the SPMs. In step 1104, the IPM 1055 checks whether the mean temperature has exceeded a predetermined and programmed threshold. If the mean temperature has not exceeded the threshold, the IPM 1055 returns to step 1102 to keep monitoring. If the mean temperature has exceeded the threshold, the IPM 1055 then generates a problem ("hot spot") report message in step 1106. In step 1108, the IPM 1055 waits for the next status query the MPM 1070. In some embodiments, a logically separate bus is provided for asynchronous status reports to the MPM 280.

[00073] In step 1110, the MPM 1070 receives the hot spot report message. In step 1112, the MPM 1070 either waits for further confirmation (i.e. see that the "hot spot" last pasts a predetermined threshold) or immediately takes action to fix the problem depending on the internal logic of the MPM 1070. In some embodiments, in step 1114, the MPM 1070 takes action by posting an interrupt to the PMCL 280 that it needs attention. In other embodiments, if the PMCL 280 queries the MPM 1070 often enough, then the interrupt is not needed. In step 1116, the MPM 1070 (or IPM) fixes the problem by making a local trade-off, performing the action, or ordering the action to be performed. One example of fixing the problem is lowering the operating frequency of the hot spot area. In step 1118, the MPM 1070 reports both the problem and the fixing of the problem upstream.

[00074] In step 1120, the PMCL 218 reads the modified hot spot report from the MPM 1070. In step 1122, the PMCL 218 determines what action to take to fix the problem or notify the GPAL 214 of the problem. In step 1124, the PMCL 218 issues the appropriate commands to the MPM

1070 to fix the problem. In this step, the software will make the trade-off required to fix the problem. In some embodiments, if the GPAL 214 determines the high level fix, then the GPAL 214 sends it to the PMCL 280 to be converted into MPM commands. In step 1126, the PMCL 218 monitors the problem area for a specified time to check if the problem is fixed. FIG. 11 ends in step 1128.

[00075] In some embodiments, the type of functionality in FIG. 11 can be performed at other levels such as the PMCL 218. In one example, the PMCL 218 queries (via the MPM 1070) all the SPMs that have the desired measurement ability (and IPMs) as to their local conditions and can then, for example, build a "map" of power usage that it can then act on.

[00076] FIG. 12 depicts a diagram of a system-on-a-chip (SOC) 1200 in another exemplary implementation of the invention. The SOC 1200 is attached to a sensor link 1212, an RF link 1214, a control link 1216, a video link 1294, an audio link 1295, an interface link 1296, a control link 1297, and a power link 1298. The SOC 1200 includes clock and distribution management 1210, an IP block power island 1220, a memory power island 1230, a microprocessor power island 1240, an IP block power island 1250, a distribution power island 1260, an IP block power island 1270, an IP block power island 1280, and power and distribution management 1290.

[00077] The IP block power island 1220 includes a product standard interface IP block including an analog-to-digital converter (ADC) 1222, which includes an SPM 1224. The IP block power island 1230 includes a memory 1232, which includes an SPM 1234. The microprocessor power island 1240 includes a microprocessor 1242, which includes an SPM 1244. The IP block power island 1250 includes a product standard interface IP block including ADC 1252, which includes an SPM 1254. The distribution power island 1260 includes a data and signal distribution 1262, which includes an SPM 1264. The IP block power island 1270 includes a general purpose IP block including a digital signal processor (DSP) 1272, which includes an SPM 1274. The IP block

power island 1280 includes a product-specific IP block 1282, which includes an SPM 1284. The power and distribution management 1290 includes an MPM 1292.

[00078] FIG. 13 depicts a flowchart for building a chip with power islands in an exemplary implementation of the invention. FIG. 13 begins in step 1300. In step 1302, the IPs or library cells are selected, and the custom logic, if any, is specified to be used to build the chip. In some embodiments, the maximum and sub clock rate, % idle time, and minimum and maximum Vdd are specified. In step 1304, the register transfer level (RTL) is written. In step 1306, the RTL is simulated and debugged.

[00079] Either during or after the writing of the RTL, a software tool may be used to add annotations for the MPM, IPM, and/or SPM blocks in step 1308. In some embodiments, the desired functionality options are specified in the annotations. In some embodiments, the optional functionality is specified per SPM block. In some embodiments, the RTL is annotated with SPM configuration information on a per-module basis. In some embodiments, the proper annotation is inserted by hand on a per module basis during or after the RTL is written. In other embodiments, a separate table in the proper format is created with the module names and respective annotations. In some embodiments, a separate software tool provides the ability to interactively build the separate table. In some embodiments, the software tool adds the proper annotation to the un-annotated modules in the RTL using information from the table.

[00080] In step 1310, the synthesis is run on a power island basis, where power islands are not mixed. In step 1312, performance measurement software is run on each module for each Vdd and Vt option, and then the annotations for the MPM are added to the RTL. In some embodiments, the performance of the design is measured at all desired voltages and Vt combinations. The software tool then derives the actual frequency, Vdd, and Vt tables for each SPM and back annotates the MPM (or IPM) RTL of the SPM characteristics.

[00081] In step 1314, the final synthesis is run on a power island basis. In some embodiments, the modules are separately routed or by SPM. In step 1316, the software tool is run to hook up power and clocks to each SPM. Step 1318 is the rest of the steps to tape-out. In some embodiments, the software tool generates the finished net-list with all information. FIG. 13 ends in step 1320.

[00082] The above-described elements can be comprised of instructions that are stored on storage media. The instructions can be retrieved and executed by a processor. Some examples of instructions are software, program code, and firmware. Some examples of storage media are memory devices, tape, disks, integrated circuits, and servers. The instructions are operational when executed by the processor to direct the processor to operate in accord with the invention. Those skilled in the art are familiar with instructions, processor, and storage media.

[00083] The above description is illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

ABSTRACT OF THE DISCLOSURE

[00084] A system for an integrated circuit comprising a plurality of power islands includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

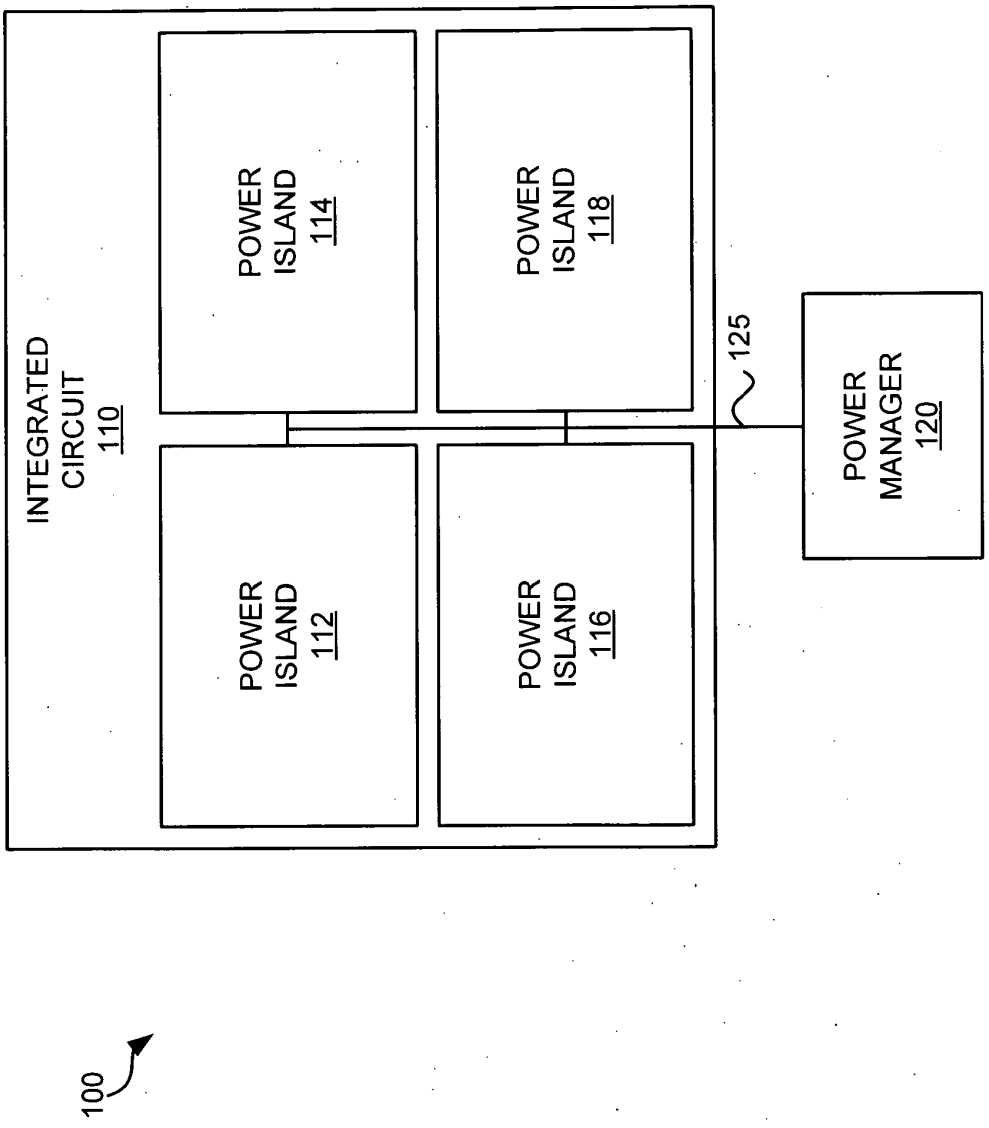

INTEGRATED CIRCUIT 110
POWER ISLAND 114
POWER ISLAND 118
POWER ISLAND 112
POWER ISLAND 116
125
POWER MANAGER 120
100

FIG. 1

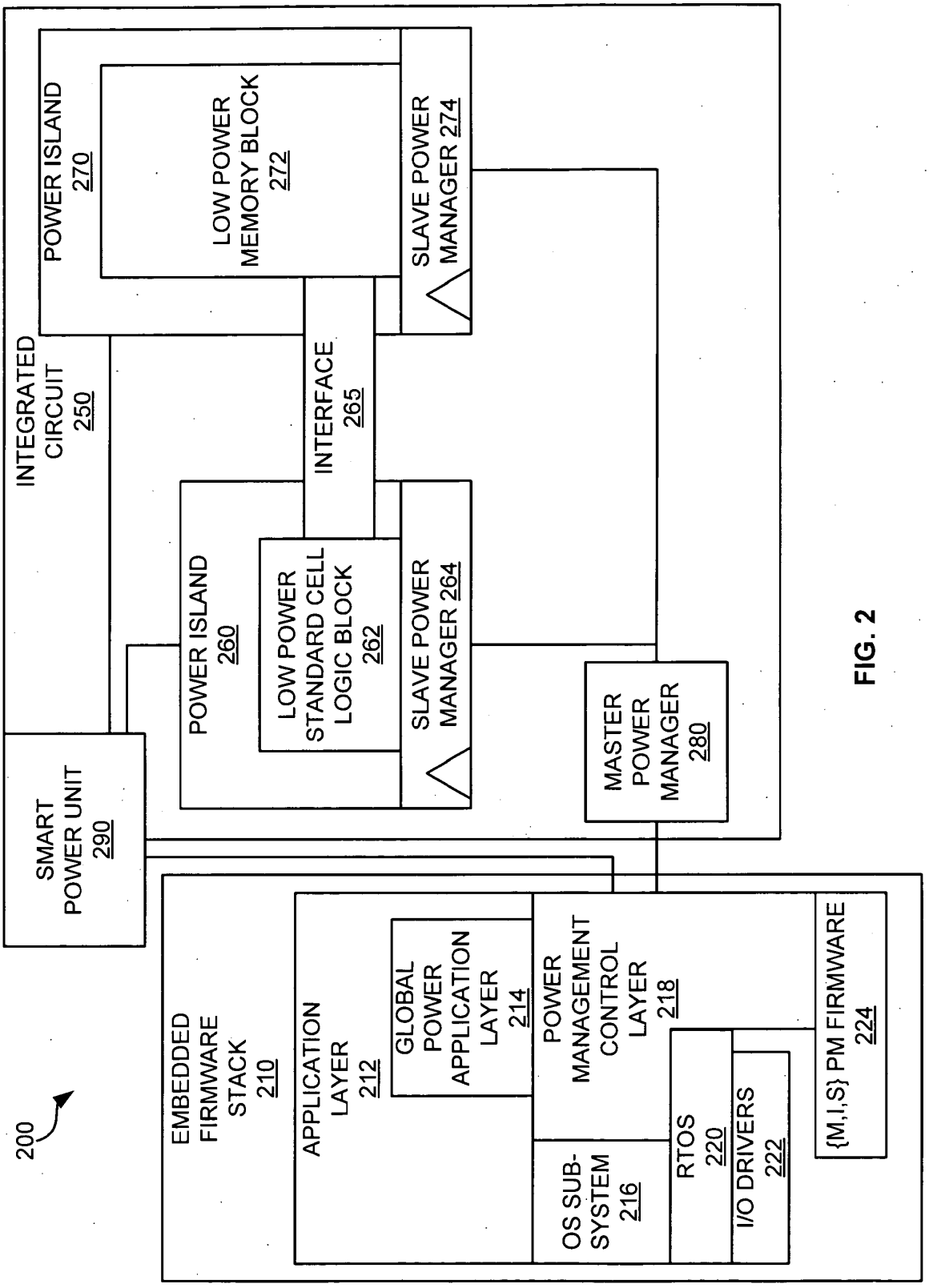

200
INTEGRATED CIRCUIT 250
POWER ISLAND 270
LOW POWER MEMORY BLOCK 272
SLAVE POWER MANAGER 274
INTERFACE 265
POWER ISLAND 260
LOW POWER STANDARD CELL LOGIC BLOCK 262
SLAVE POWER MANAGER 264
MASTER POWER MANAGER 280
SMART POWER UNIT 290
EMBEDDED FIRMWARE STACK 210
APPLICATION LAYER 212
GLOBAL POWER APPLICATION LAYER 214
POWER MANAGEMENT CONTROL LAYER 218
OS SUB-SYSTEM 216
RTOS 220
I/O DRIVERS 222
{M,I,S} PM FIRMWARE 224

FIG. 2

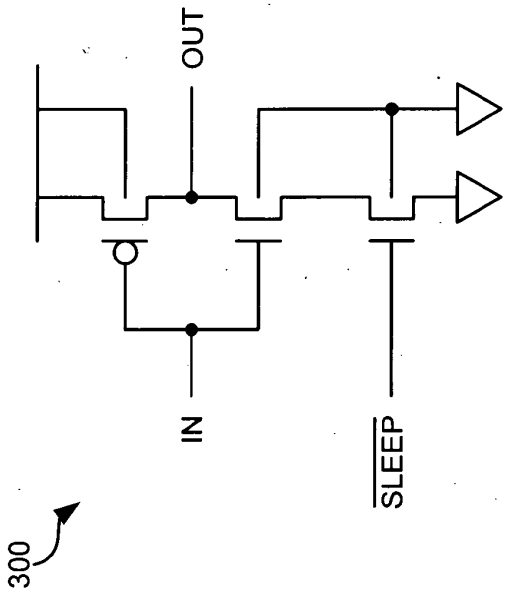


FIG. 3

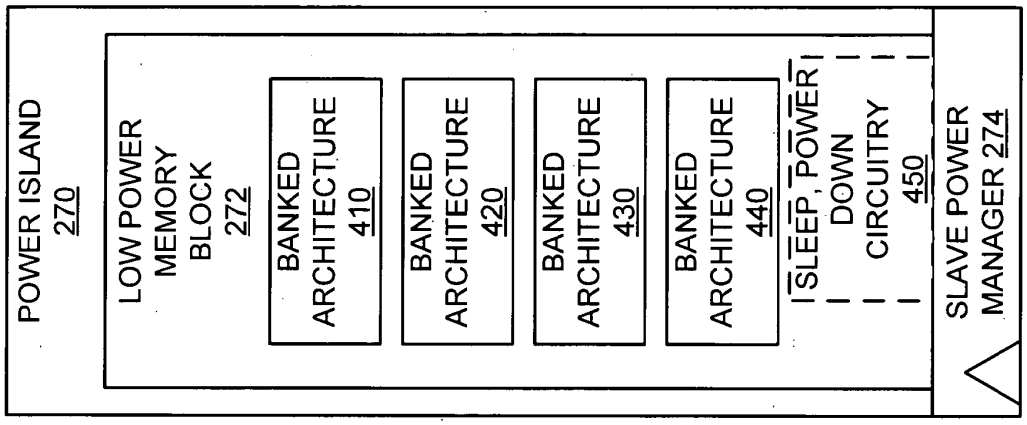

POWER ISLAND
270
LOW POWER
MEMORY
BLOCK
272
BANKED
ARCHITECTURE
410
BANKED
ARCHITECTURE
420
BANKED
ARCHITECTURE
430
BANKED
ARCHITECTURE
440
SLEEP, POWER
DOWN
CIRCUITRY
450
SLAVE POWER
MANAGER 274

FIG. 4

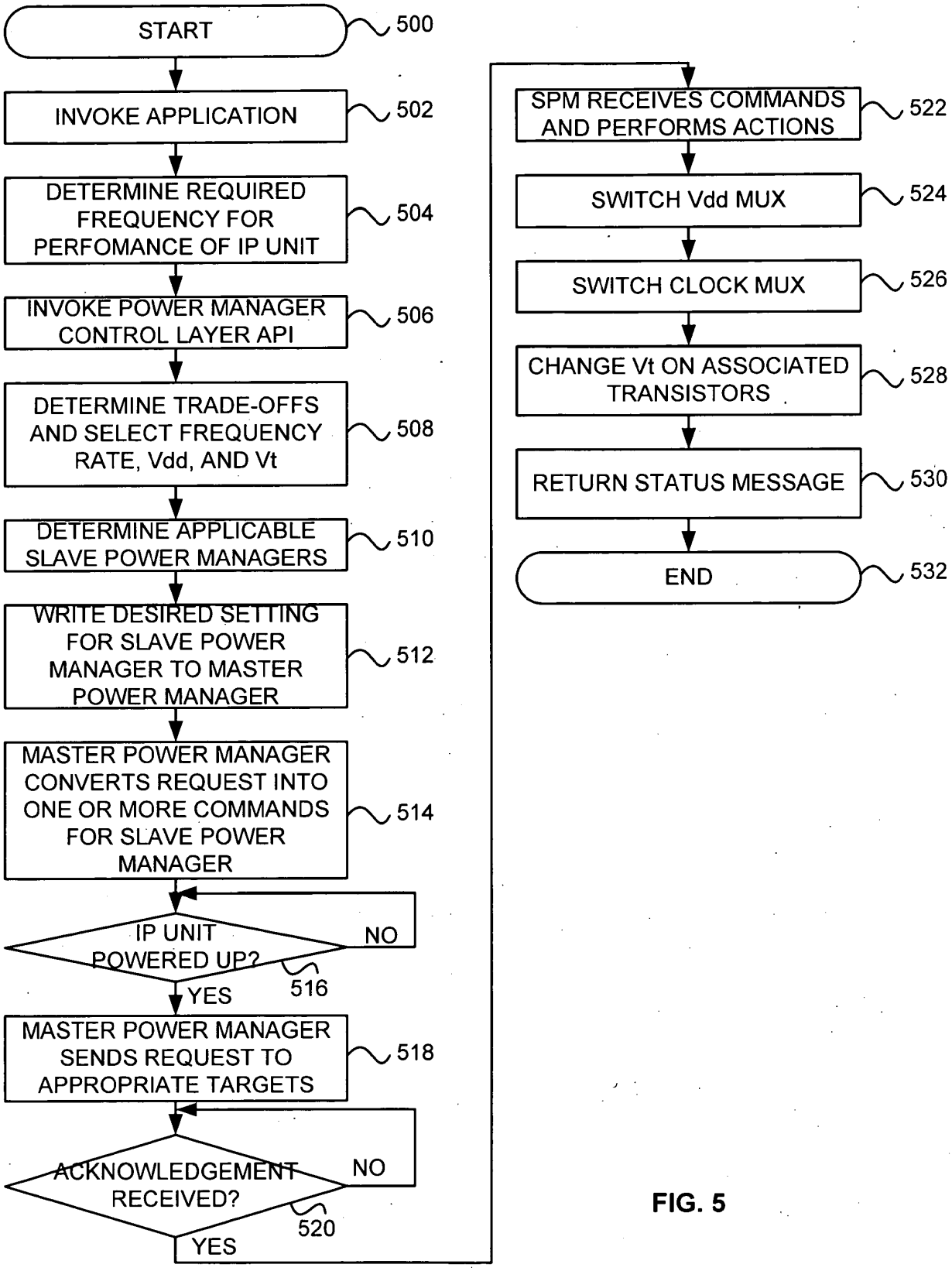

START
500
INVOKE APPLICATION
502
DETERMINE REQUIRED FREQUENCY FOR PERFOMANCE OF IP UNIT
504
INVOKE POWER MANAGER CONTROL LAYER API
506
DETERMINE TRADE-OFFS AND SELECT FREQUENCY RATE, Vdd, AND Vt
508
DETERMINE APPLICABLE SLAVE POWER MANAGERS
510
WRITE DESIRED SETTING FOR SLAVE POWER MANAGER TO MASTER POWER MANAGER
512
MASTER POWER MANAGER CONVERTS REQUEST INTO ONE OR MORE COMMANDS FOR SLAVE POWER MANAGER
514
IP UNIT POWERED UP?
NO
YES
516
MASTER POWER MANAGER SENDS REQUEST TO APPROPRIATE TARGETS
518
ACKNOWLEDGEMENT RECEIVED?
NO
YES
520
SPM RECEIVES COMMANDS AND PERFORMS ACTIONS
522
SWITCH Vdd MUX
524
SWITCH CLOCK MUX
526
CHANGE Vt ON ASSOCIATED TRANSISTORS
528
RETURN STATUS MESSAGE
530
END
532

FIG. 5

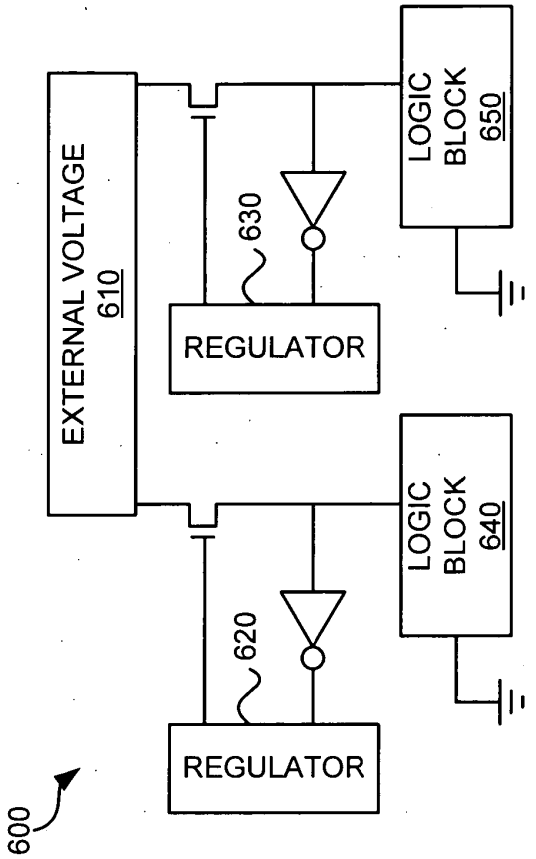

EXTERNAL VOLTAGE
610
630
REGULATOR
LOGIC
BLOCK
650
620
REGULATOR
LOGIC
BLOCK
640
600

FIG. 6

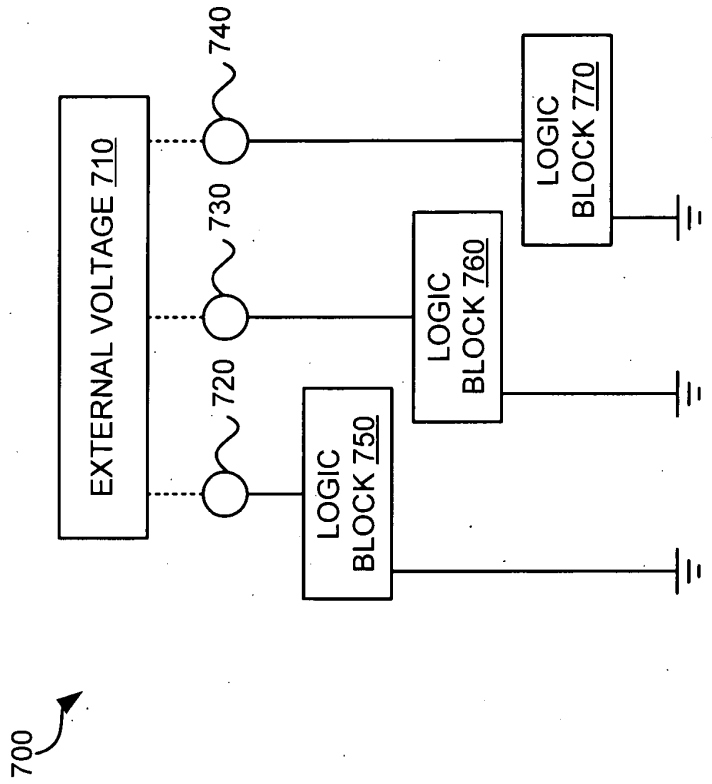

700
EXTERNAL VOLTAGE 710
740
730
720
LOGIC BLOCK 770
LOGIC BLOCK 760
LOGIC BLOCK 750

FIG. 7

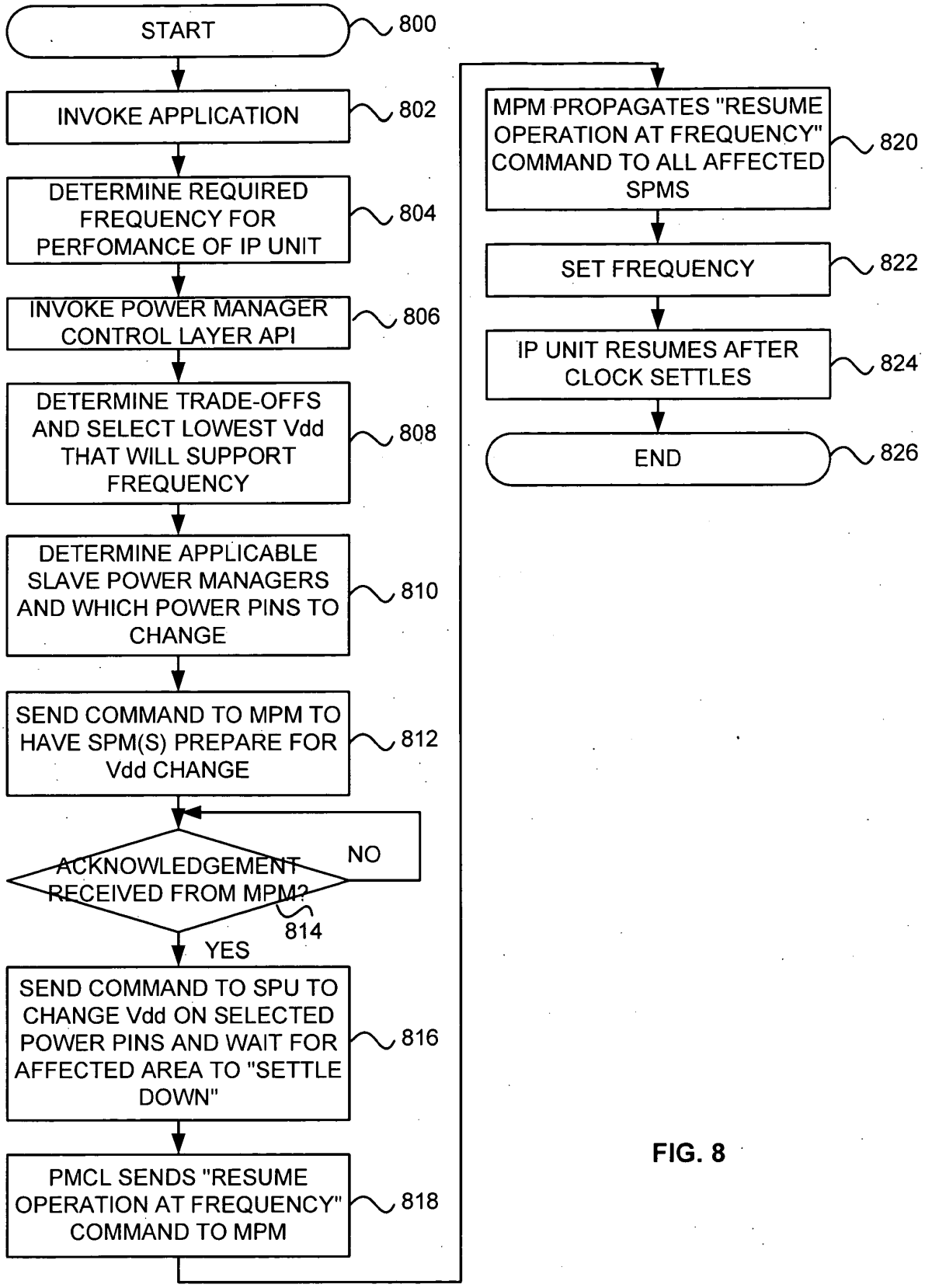

START
800
INVOKE APPLICATION
802
DETERMINE REQUIRED FREQUENCY FOR PERFOMANCE OF IP UNIT
804
INVOKE POWER MANAGER CONTROL LAYER API
806
DETERMINE TRADE-OFFS AND SELECT LOWEST Vdd THAT WILL SUPPORT FREQUENCY
808
DETERMINE APPLICABLE SLAVE POWER MANAGERS AND WHICH POWER PINS TO CHANGE
810
SEND COMMAND TO MPM TO HAVE SPM(S) PREPARE FOR Vdd CHANGE
812
ACKNOWLEDGEMENT RECEIVED FROM MPM?
814
NO
YES
SEND COMMAND TO SPU TO CHANGE Vdd ON SELECTED POWER PINS AND WAIT FOR AFFECTED AREA TO "SETTLE DOWN"
816
PMCL SENDS "RESUME OPERATION AT FREQUENCY" COMMAND TO MPM
818
MPM PROPAGATES "RESUME OPERATION AT FREQUENCY" COMMAND TO ALL AFFECTED SPMS
820
SET FREQUENCY
822
IP UNIT RESUMES AFTER CLOCK SETTLES
824
END
826

FIG. 8

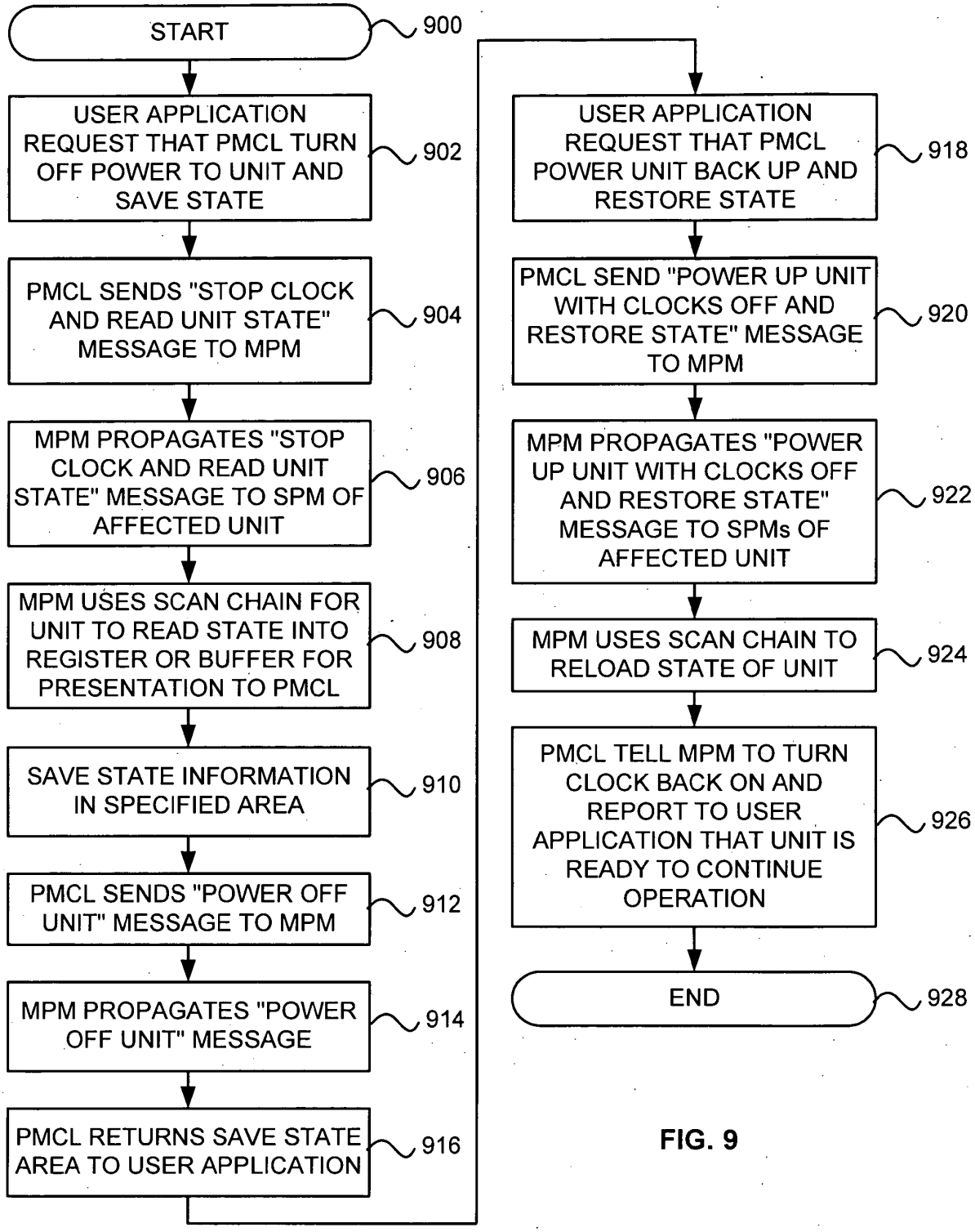

START
900
USER APPLICATION REQUEST THAT PMCL TURN OFF POWER TO UNIT AND SAVE STATE
902
PMCL SENDS "STOP CLOCK AND READ UNIT STATE" MESSAGE TO MPM
904
MPM PROPAGATES "STOP CLOCK AND READ UNIT STATE" MESSAGE TO SPM OF AFFECTED UNIT
906
MPM USES SCAN CHAIN FOR UNIT TO READ STATE INTO REGISTER OR BUFFER FOR PRESENTATION TO PMCL
908
SAVE STATE INFORMATION IN SPECIFIED AREA
910
PMCL SENDS "POWER OFF UNIT" MESSAGE TO MPM
912
MPM PROPAGATES "POWER OFF UNIT" MESSAGE
914
PMCL RETURNS SAVE STATE AREA TO USER APPLICATION
916
USER APPLICATION REQUEST THAT PMCL POWER UNIT BACK UP AND RESTORE STATE
918
PMCL SEND "POWER UP UNIT WITH CLOCKS OFF AND RESTORE STATE" MESSAGE TO MPM
920
MPM PROPAGATES "POWER UP UNIT WITH CLOCKS OFF AND RESTORE STATE" MESSAGE TO SPMs OF AFFECTED UNIT
922
MPM USES SCAN CHAIN TO RELOAD STATE OF UNIT
924
PMCL TELL MPM TO TURN CLOCK BACK ON AND REPORT TO USER APPLICATION THAT UNIT IS READY TO CONTINUE OPERATION
926
END
928

FIG. 9

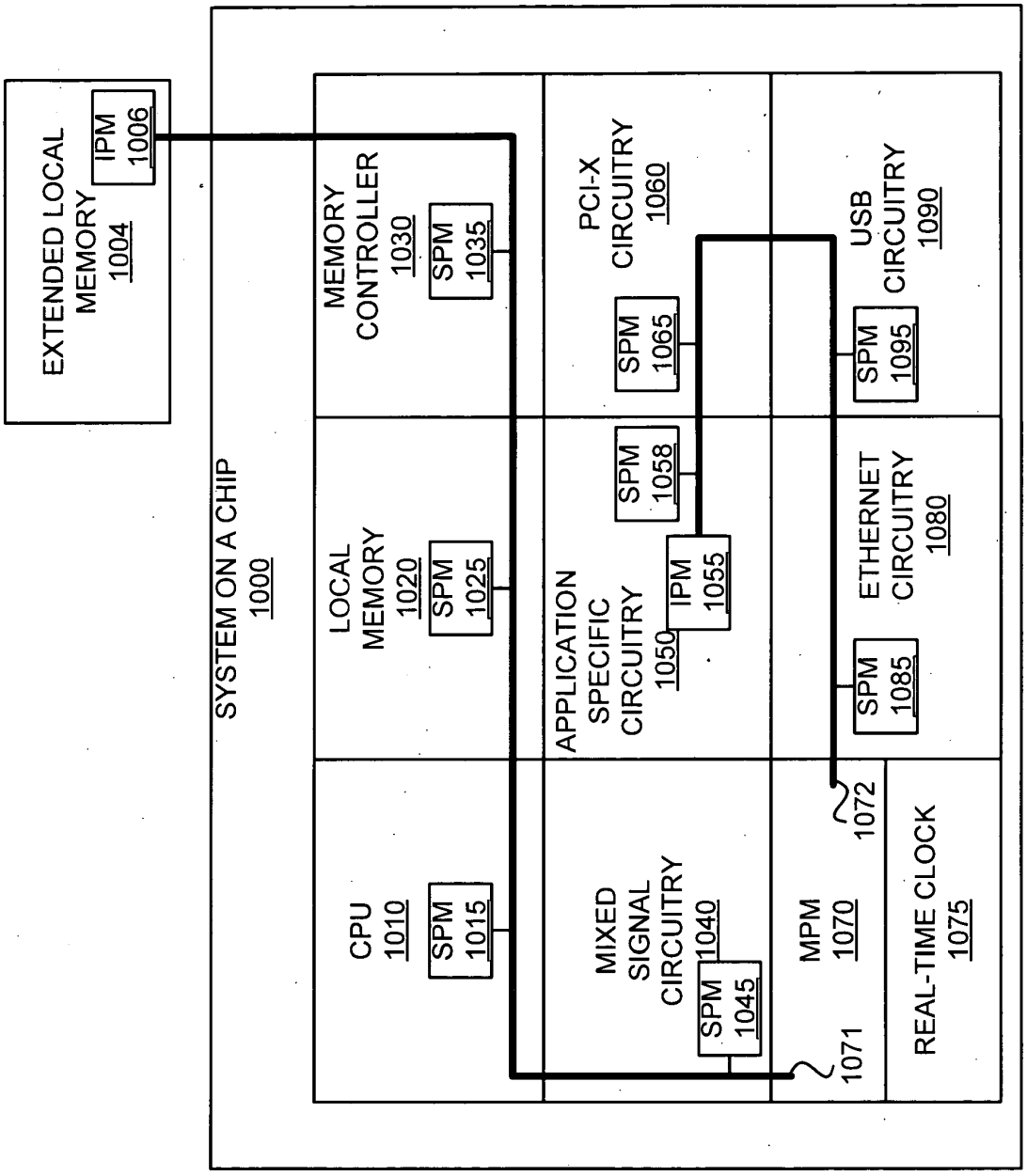

EXTENDED LOCAL MEMORY 1004
IPM 1006
SYSTEM ON A CHIP 1000
MEMORY CONTROLLER 1030
SPM 1035
PCI-X CIRCUITRY 1060
SPM 1065
USB CIRCUITRY 1090
SPM 1095
LOCAL MEMORY 1020
SPM 1025
APPLICATION SPECIFIC CIRCUITRY 1050
SPM 1058
IPM 1055
ETHERNET CIRCUITRY 1080
SPM 1085
CPU 1010
SPM 1015
MIXED SIGNAL CIRCUITRY
SPM 1040
SPM 1045
MPM 1070
1071
1072
REAL-TIME CLOCK 1075

FIG. 10

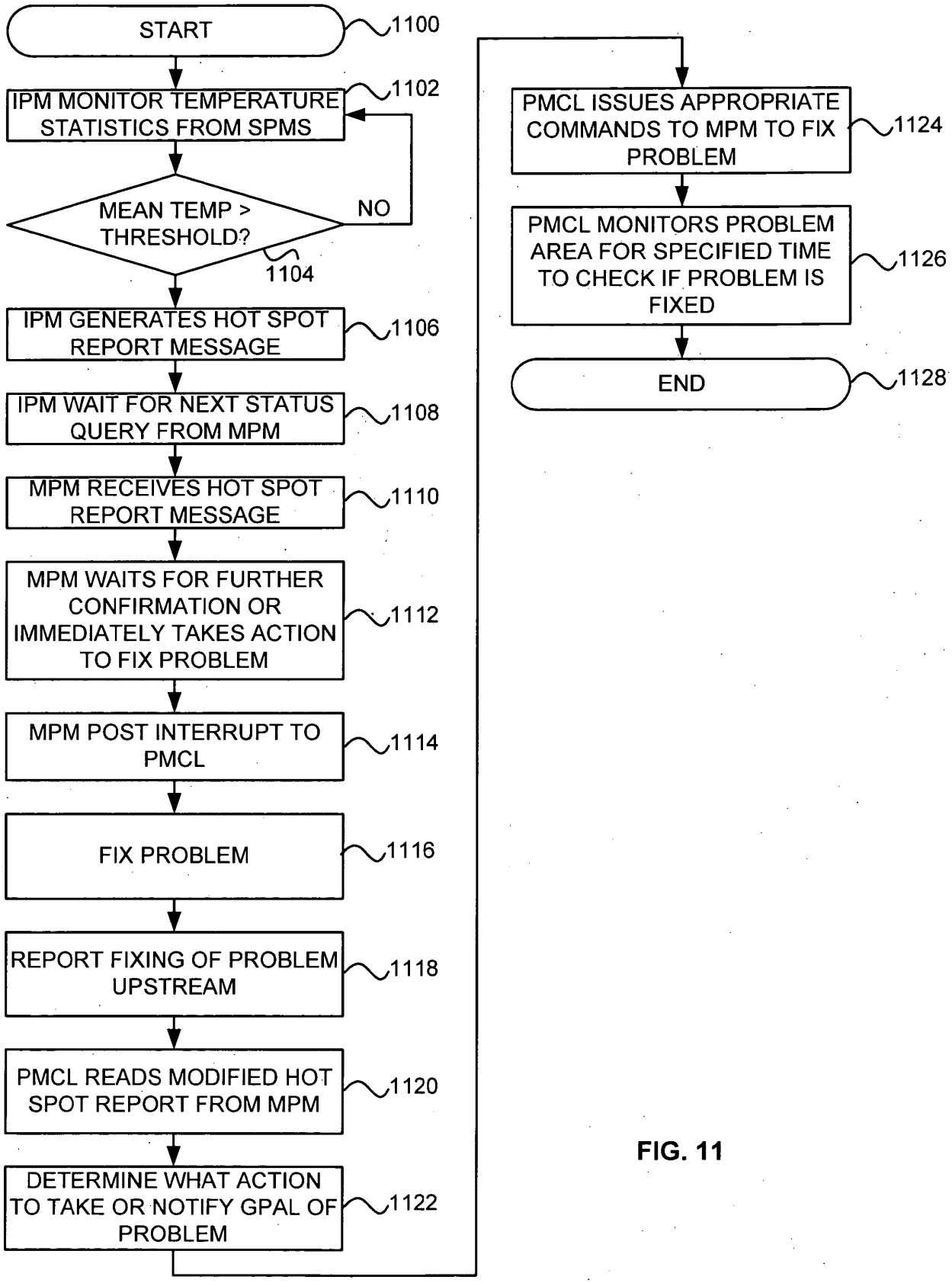

START
1100
IPM MONITOR TEMPERATURE STATISTICS FROM SPMS
1102
MEAN TEMP > THRESHOLD?
NO
1104
IPM GENERATES HOT SPOT REPORT MESSAGE
1106
IPM WAIT FOR NEXT STATUS QUERY FROM MPM
1108
MPM RECEIVES HOT SPOT REPORT MESSAGE
1110
MPM WAITS FOR FURTHER CONFIRMATION OR IMMEDIATELY TAKES ACTION TO FIX PROBLEM
1112
MPM POST INTERRUPT TO PMCL
1114
FIX PROBLEM
1116
REPORT FIXING OF PROBLEM UPSTREAM
1118
PMCL READS MODIFIED HOT SPOT REPORT FROM MPM
1120
DETERMINE WHAT ACTION TO TAKE OR NOTIFY GPAL OF PROBLEM
1122
PMCL ISSUES APPROPRIATE COMMANDS TO MPM TO FIX PROBLEM
1124
PMCL MONITORS PROBLEM AREA FOR SPECIFIED TIME TO CHECK IF PROBLEM IS FIXED
1126
END
1128

FIG. 11

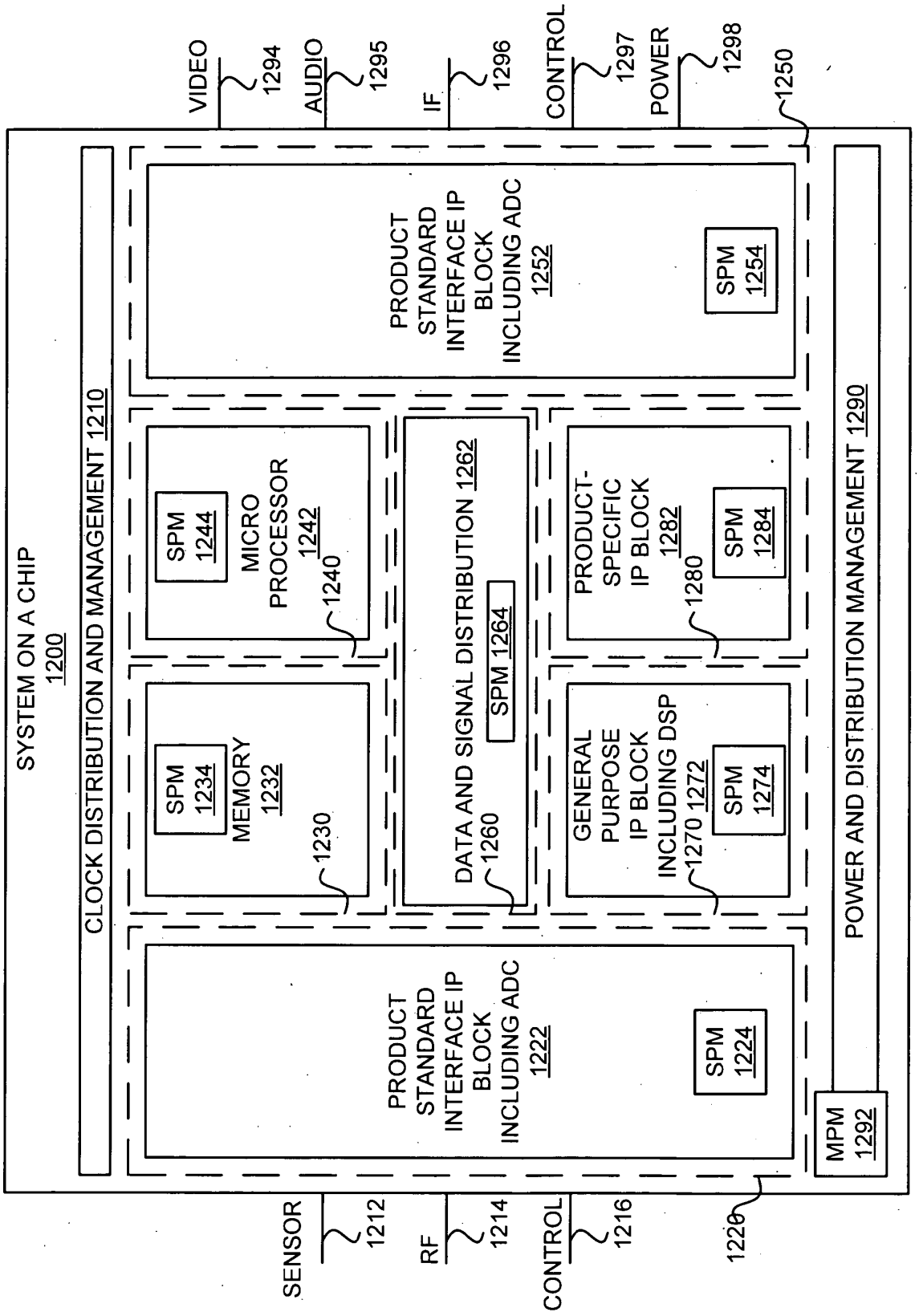

SYSTEM ON A CHIP
1200
CLOCK DISTRIBUTION AND MANAGEMENT 1210
PRODUCT STANDARD INTERFACE IP BLOCK INCLUDING ADC 1222
SPM 1224
MEMORY 1232
SPM 1234
1230
MICRO PROCESSOR 1242
SPM 1244
1240
DATA AND SIGNAL DISTRIBUTION 1262
SPM 1264
1260
GENERAL PURPOSE IP BLOCK INCLUDING DSP 1270 1272
SPM 1274
PRODUCT-SPECIFIC IP BLOCK 1282
SPM 1284
1280
PRODUCT STANDARD INTERFACE IP BLOCK INCLUDING ADC 1252
SPM 1254
POWER AND DISTRIBUTION MANAGEMENT 1290
MPM 1292
SENSOR 1212
RF 1214
CONTROL 1216
1220
VIDEO 1294
AUDIO 1295
IF 1296
CONTROL 1297
POWER 1298
1250

FIG. 12

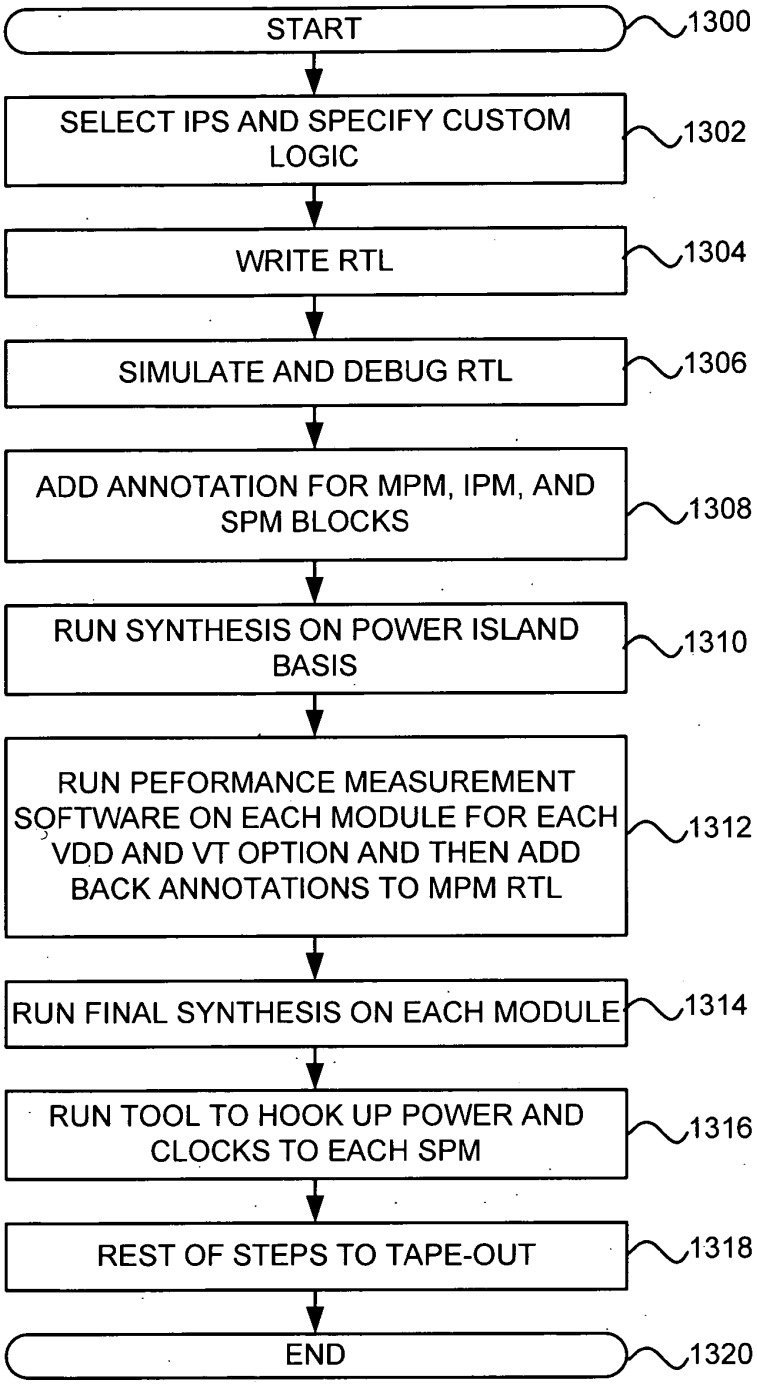

START
1300
SELECT IPS AND SPECIFY CUSTOM LOGIC
1302
WRITE RTL
1304
SIMULATE AND DEBUG RTL
1306
ADD ANNOTATION FOR MPM, IPM, AND SPM BLOCKS
1308
RUN SYNTHESIS ON POWER ISLAND BASIS
1310
RUN PEFORMANCE MEASUREMENT SOFTWARE ON EACH MODULE FOR EACH VDD AND VT OPTION AND THEN ADD BACK ANNOTATIONS TO MPM RTL
1312
RUN FINAL SYNTHESIS ON EACH MODULE
1314
RUN TOOL TO HOOK UP POWER AND CLOCKS TO EACH SPM
1316
REST OF STEPS TO TAPE-OUT
1318
END
1320

FIG. 13

ATTORNEY'S DOCKET NO.: PA2258US

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

"Managing Power on Integrated Circuits Using Power Islands"

which was filed in the United States Patent and Trademark Office on May 7, 2004 and assigned serial number 10/840,893.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under Title 35, United States Code §119(a)-(d) or (f) or §365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s):

Number	Country	Foreign Filing Date	Priority Claimed?	Certified Copy Attached?
_____ (Number)	_____ (Country)	_____ (MM/DD/YYYY)	☐ Yes ☐ No	☐ Yes ☐ No
_____ (Number)	_____ (Country)	_____ (MM/DD/YYYY)	☐ Yes ☐ No	☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code §119(e) of any United States provisional application(s) listed below.

Prior Provisional Applications:

60/468,742	May 7, 2003
(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

Prior U.S. or PCT Applications Designating the U.S.:

(Application Number)	(Filing Date)	(Status -- patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status -- patented, pending, abandoned)

POWER OF ATTORNEY: I hereby appoint the attorney(s) and/or agent(s) associated with the customer number **22830** to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

SEND ALL CORRESPONDENCE TO:

CARR & FERRELL *LLP*
2200 Geng Road
Palo Alto, CA 94303
TEL: (650) 812-3400
FAX: (650) 812-3444

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first inventor: Barry Alan Hoberman Citizenship: U.S.A.
Print First Name, Middle Name or Initial (if applicable), Last Name

Inventor's signature: [signature] Dated: 7/29/04
(Permanent ink only) *(Date of Signature)*

Mailing Address: 10290 Palo Vista Road, Cupertino, CA 95014
(Where the inventor customarily receives mail: Number, Street, City, State, Zip Code)

Residence Address: Same
(if the inventor lives at a location different than his/her mailing address)

Full name of second inventor: Daniel L. Hillman Citizenship: U.S.A.
Print First Name, Middle Name or Initial (if applicable), Last Name

Inventor's signature: [signature] Dated: 7-28-04
(Permanent ink only) *(Date of Signature)*

Mailing Address: 6607 Winterset Way, San Jose, CA 95120
(Where the inventor customarily receives mail: Number, Street, City, State, Zip Code)

Residence Address: Same
(if the inventor lives at a location different than his/her mailing address)

Full name of third inventor: Jon Shiell Citizenship: U.S.A.
Print First Name, Middle Name or Initial (if applicable), Last Name

Inventor's signature: [signature] Dated: 8-04-04
(Permanent ink only) *(Date of Signature)*

Mailing Address: 801 Seabury Drive, San Jose, CA 95136
(Where the inventor customarily receives mail: Number, Street, City, State, Zip Code)

Residence Address:
(if the inventor lives at a location different than his/her mailing address)

PTO/SB/06 (12-04)

Filing Date: 07/21/08

Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 12/176,645

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	310
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	510
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	210
TOTAL CLAIMS (37 CFR 1.16(i))	26 minus 20 =	6	X$ 25		OR	X$50	300
INDEPENDENT CLAIMS (37 CFR 1.16(h))	8 minus 3 =	* 5	X$105			X$210	1050
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $260 ($130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			185			370	
			TOTAL	0		TOTAL	2380

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
					TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X =		OR	X =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X =		OR	X =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
					TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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