

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

MOSAID TECHNOLOGIES INC.,	)	
	)	
Plaintiff,	)	
	)	Civil No. 2:23-cv-00129
v.	)	
	)	JURY TRIAL DEMANDED
MEDIATEK, INC.	)	
MEDIATEK USA, INC.,	)	
	)	
Defendants.	)	
	)	

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff MOSAID Technologies Inc. (“Plaintiff” or “MOSAID”) files this Complaint for Patent Infringement against Defendants MediaTek, Inc. (“MTK”) and MediaTek USA, Inc. (“MTK USA”) (MTK and MTK USA collectively, “MediaTek”), alleging as follows:

NATURE OF SUIT

1. This is a claim for patent infringement arising under the patent laws of the United States, Title 35 of the United States Code.

PARTIES, JURISDICTION, AND VENUE

2. This action arises under the patent laws of the United States, 35 U.S.C. § 101, *et seq.* This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

I. MOSAID

3. MOSAID (f/k/a Conversant Intellectual Property Management, Inc.) is a Canadian company having a principal place of business at 515 Legget Drive, Suite 100, Ottawa, ON, Canada. MOSAID’s subsidiary, Conversant Intellectual Property Management Corp., is located at 5830 Granite Parkway #100-247, Suite 247, Plano, Texas 75024.

4. MOSAID was founded in 1975 by engineers Richard Foss and Robert Harland. MOSAID focused its early efforts on inventing ways to improve Dynamic Random Access Memory (DRAM) semiconductor chips. MOSAID's engineers also designed and built test equipment for debugging prototype memory chips.

5. MOSAID is now a leading patent management company with a world-class licensing team and an enviable record of success. MOSAID's success is defined by the numerous licenses it has signed with industry leaders. MOSAID prides itself on its patent expertise, a determination to engage in meaningful negotiation, and a commitment to transparency and the principled enforcement of high-quality patents.

6. MOSAID is the assignee and owns all right, title, and interest to United States Patent No. 7,051,306 ("the '306 Patent"), United States Patent No. 7,945,885 ("the '885 Patent"), United States Patent No. 7,996,811 ("the '811 Patent"), United States Patent No. 8,253,438 ("the '438 Patent"), United States Patent No. 8,854,077 ("the '077 Patent"), United States Patent No. 9,350,349 ("the '349 Patent"), and United States Patent No. 7,224,563 ("the '563 Patent"). The '306 Patent, '885 Patent, '811 Patent, '438 Patent, '077 Patent, '349 Patent, and '563 Patent are collectively referred to herein as the "Asserted Patents."

II. MEDIATEK

7. Upon information and belief, Defendant MediaTek, Inc. is a corporation organized and existing under the laws of Taiwan, and is located at No. 1, Dusing Road 1, Hsinchu Science Park, Hsinchu City 30078, Taiwan.

8. Upon information and belief, MTK makes, uses, offers for sale, sells in the United States, and/or imports into the United States, a variety of semiconductor products. For example, MTK manufactures and sells semiconductors and/or processors for mobile phones and tablets, among other consumer products.

9. Upon information and belief, MTK makes, uses, offers for sale, sells in the United States, and/or imports into the United States, certain processors including at least the MT6755 (Helio P10), MT6797 (Helio X20), MT6853 (Dimensity 720), and the MT6983 (Dimensity 9000), among other substantially similar processors, (collectively, the “Infringing Products”) that utilize the inventions of the Asserted Patents.

10. MTK sells its Infringing Products to numerous companies in the United States.

11. MTK is subject to specific and general personal jurisdiction in this Court. This Court has personal jurisdiction over MTK because, upon information and belief, MTK has engaged in continuous, systematic, and substantial activities within this State, including substantial marketing and sales of products and services within this State and District. Furthermore, upon information and belief, this Court has personal jurisdiction over MTK because MTK has committed acts of infringement giving rise to MOSAID’s claims for patent infringement within and directed to this District.

12. On information and belief, MTK has conducted, and does conduct, substantial business in this District, directly and/or through subsidiaries, agents, representatives, or intermediaries, including, but not limited to: (i) at least a portion of the acts of infringement alleged herein; (ii) purposefully and voluntarily placing one or more Infringing Products into the stream of commerce with the expectation that they will be purchased by consumers in this District; and/or (iii) regularly doing or soliciting business, engaging in other persistent courses of conduct, or deriving substantial revenue from goods and services provided to individuals in this State and in this District. Thus, MTK is subject to this Court’s specific and general personal jurisdiction pursuant to due process and the Texas Long-Arm Statute. To the extent MTK is not subject to jurisdiction in any state’s courts of general jurisdiction, this Court has personal jurisdiction over

MTK pursuant to Federal Rule of Civil Procedure 4(k)(2) because MOSAID's claims arise under federal law and exercising jurisdiction is consistent with the United States Constitution and laws.

13. The exercise of personal jurisdiction over MTK would not offend traditional notions of fair play and substantial justice.

14. Under 28 U.S.C. §§ 1391(b)-(d) and 1400(b), venue is proper in this District as to MTK at least because MTK is a foreign corporation subject to personal jurisdiction in this District and has committed acts of infringement within this District giving rise to this action.

15. To the extent that there is no district in which an action may otherwise be brought against MTK, venue is proper in this District as to MTK under 28 U.S.C. § 1391(b)(3) because MTK is subject to personal jurisdiction in this Court.

16. Upon information and belief, MediaTek USA, Inc. is a corporation duly organized and existing under the laws of the state of Delaware, having a regular and established place of business in the Eastern District of Texas, including at 825 Watters Creek Blvd., Suite 265, Allen, Texas 75103. Upon information and belief, MTK USA also maintains other offices in the State of Texas, including in Irvine, Texas and Austin, Texas.

17. MTK USA is subject to specific and general personal jurisdiction in this Court. This Court has personal jurisdiction over MTK USA because it has engaged in continuous, systematic, and substantial activities within this State, including substantial marketing and sales of products and services within this State and District. Furthermore, upon information and belief, this Court has personal jurisdiction over MTK USA because MTK USA has committed acts of infringement giving rise to MOSAID's claims for patent infringement within and directed to this District.

18. Upon information and belief, MTK USA has conducted and does conduct substantial business in this District, directly and/or through subsidiaries, agents, representatives, or intermediaries, such substantial business including, but not limited to: (i) at least a portion of the acts of infringement alleged herein; (ii) purposefully and voluntarily placing one or more Infringing Products into the stream of commerce with the expectation that they will be purchased by consumers in this forum; and/or (iii) regularly doing or soliciting business, engaging in other persistent courses of conduct, or deriving substantial revenue from goods and services provided to individuals in Texas and in this District. Thus, MTK USA is subject to this Court's specific and general personal jurisdiction pursuant to due process and the Texas Long-Arm Statute.

19. The exercise of personal jurisdiction over MTK USA would not offend traditional notions of fair play and substantial justice.

20. Upon information and belief, MTK USA has committed acts of infringement in this District and has regular and established places of business within this District under 28 U.S.C. § 1400(b). Thus, venue is proper in this District as to MTK USA under 28 U.S.C. § 1400(b).

21. MTK USA maintains a permanent physical presence within this District. For example, it maintains regular and established places of business at 825 Watters Creek Blvd, Suite 265, Allen, Texas 75103.

22. Upon information and belief, MediaTek's locations in this District are regular and established places of business under 28 U.S.C. § 1391, 28 U.S.C. § 1400(b), and *In re Cray, Inc.*, 871 F.3d 1355, 1360 (Fed. Cir. 2017).

a. Upon information and belief, MediaTek's locations in this District are physical, geographical locations in this District. Each office location comprises one or more buildings or office spaces from which the business of MediaTek is carried out. Upon

information and belief, the locations are set apart for the purpose of carrying out MediaTek's business, including, but not limited to, making, using, selling, offering for sale, and/or supporting Infringing Products. Upon information and belief, MediaTek advertises its physical locations in this District as places of its business.

b. Upon information and belief, MediaTek's locations in this District are regular and established. MediaTek identifies on its website (<https://corp.mediatek.com/about/office-locations/mediatek-usa-offices>) its address in this District as a regular and established place of MediaTek's business.

c. Upon information and belief, MediaTek's locations in this District are places of business of MediaTek. Upon information and belief, MediaTek conducts business from its locations in this District, including but not limited to, making, using, selling, offering for sale, and/or supporting Infringing Products.

d. Upon information and belief, MediaTek's locations in this District are physical, geographical location(s) in this District from which MediaTek carries out its business.

e. Upon information and belief, MediaTek employees work at MediaTek's locations in this District. Upon information and belief, these MediaTek employees are regularly and physically present at MediaTek's locations during business hours and conduct MediaTek's business while working there.

FACTUAL ALLEGATIONS

I. PATENTS-IN-SUIT

23. United States Patent No. 7,051,306 ("the '306 Patent") is entitled "Managing Power on Integrated Circuits Using Power Islands". The United States Patent and Trademark

Office duly and legally issued the '306 Patent on May 23, 2006, from U.S. Patent Application No. 10/840,893, filed on May 7, 2004.

24. The '306 Patent is entitled to the benefit of U.S. Provisional Patent Application No. 60/468,742, entitled "System and Method for Managing Power in Integrated Circuits", filed on May 7, 2003.

25. MOSAID is the current owner of all rights, title, and interest in and to the '306 Patent, including the right to sue for past damages.

26. A true and correct copy of the '306 Patent is attached hereto as **Exhibit A** and is incorporated by reference herein.

27. The '306 Patent generally relates to systems and methods to manage power in an integrated circuit using power islands. The integrated circuit includes a plurality of power islands where power consumption is independently controlled within each of the power islands. A power manager determines a target power level for one of the power islands. The power manager then determines an action to change a consumption power level of the one of the power islands to the target power level. The power manager performs the action to change the consumption power level of the one of the power islands to the target power level.

28. Claim 16 is illustrative of the claimed invention of the '306 Patent. It is directed to:

16. A system for an integrated circuit comprising a plurality of power islands where power consumption is independently controlled within each of the power islands, the system comprising:

power control circuitry configured to control power for one of the power islands; and

a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.

29. Numerous companies enjoy a license to the '306 Patent. MediaTek previously enjoyed a limited license to the '306 Patent, but that license expired on March 7, 2016. MediaTek is not currently licensed to the '306 Patent.

30. United States Patent No. 7,945,885 ("the '885 Patent") is entitled "Power Managers for an Integrated Circuit". The United States Patent and Trademark Office duly and legally issued the '885 Patent on May 17, 2011, from U.S. Patent Application No. 12/176,645, filed on July 21, 2008.

31. The '885 Patent is a continuation of U.S. Patent Application No. 11/336,097, filed on January 20, 2006, entitled "Power Managers for an Integrated Circuit", and which issued on August 19, 2008 as U.S. Patent No. 7,415,680, which is a continuation of U.S. Patent Application No. 10/840,893, filed on May 7, 2004, entitled "Managing Power on Integrated Circuits Using Power Islands", and which issued on May 23, 2006 as the '306 Patent, which claims the benefit of U.S. Provisional Patent Application No. 60/468,742, titled "System and Method for Managing Power in Integrated Circuits", filed May 7, 2003.

32. MOSAID is the current owner of all rights, title, and interest in and to the '885 Patent, including the right to sue for past damages.

33. A true and correct copy of the '885 Patent is attached hereto as **Exhibit B** and is incorporated by reference herein.

34. The '885 Patent generally relates to a system for an integrated circuit comprising a plurality of power islands and includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

35. Claim 39 is illustrative of the claimed invention of the '885 Patent. It is directed to:

39. A system comprising:

an integrated circuit;

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

one or more power consumption signals indicating one or more of the power consumptions;

a power manager coupled to each of the power islands configured to monitor the one or more power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

36. Numerous companies enjoy a license to the '885 Patent. MediaTek previously enjoyed a limited license to the '885 Patent, but that license expired on March 7, 2016. MediaTek is not currently licensed to the '885 Patent.

37. United States Patent No. 7,996,811 ("the '811 Patent") is entitled "Power Managers for an Integrated Circuit". The United States Patent and Trademark Office duly and legally issued the '811 Patent on August 9, 2011, from U.S. Patent Application No. 12/332,529, filed on December 11, 2008.

38. The '811 Patent is a continuation of U.S. Patent Application No. 12/176,645, filed on July 21, 2008, entitled "Power Managers for an Integrated Circuit", and which issued May 17, 2011 as the '885 Patent, which is a continuation of U.S. Patent Application No. 11/336,097, filed on January 20, 2006, entitled "Power Managers for an Integrated Circuit", and which issued on August 19, 2008 as U.S. Patent No. 7,415,680, which is a continuation of U.S. Patent Application No. 10/840,893, filed on May 7, 2004, entitled "Managing Power on Integrated Circuits Using Power Islands", and which issued on May 23, 2006 as the '306 Patent, which claims the benefit of U.S. Provisional Patent Application No. 60/468,742, entitled "System and Method for Managing Power in Integrated Circuits", filed May 7, 2003.

39. MOSAID is the current owner of all rights, title, and interest in and to the '811 Patent, including the right to sue for past damages.

40. A true and correct copy of the '811 Patent is attached hereto as **Exhibit C** and is incorporated by reference herein.

41. The '811 Patent generally relates to a system for an integrated circuit comprising a plurality of power islands and includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

42. Claim 30 is illustrative of the claimed invention of the '811 Patent. It is directed to:

30. A system comprising:
an integrated circuit;

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions adapted to be independently controlled, and a first of the power islands being configured to communicate synchronously and asynchronously with a second of the power islands; and

a power manager to control the power consumptions, and

at least one of the power islands adapted to have the power manager control its associated power consumption in that the system is configured to have:

a supply voltage to the at least one of the power islands changed, and

a frequency of operation of the at least one of the power islands changed.

43. Numerous companies enjoy a license to the '811 Patent. MediaTek previously enjoyed a limited license to the '811 Patent, but that license expired on March 7, 2016. MediaTek is not currently licensed to the '811 Patent.

44. United States Patent No. 8,253,438 ("the '438 Patent") is entitled "Low Leakage and Data Retention Circuitry". The United States Patent and Trademark Office duly and legally issued the '438 Patent on August 28, 2012, from U.S. Patent Application No. 13/074,291, filed on March 29, 2011.

45. The '438 Patent is a continuation of U.S. Patent Application No. 12/542,352, filed August 17, 2009, which is a continuation of U.S. Patent Application No. 12/284,311, filed September 19, 2008 (now U.S. Patent No. 7,592,837), which is a continuation of U.S. Patent Application No. 11/998,725, filed November 30, 2007 (now U.S. Patent No. 7,443,197), which is a continuation of U.S. Patent Application No. 11/732,181, filed April 2, 2007 (now U.S. Patent No. 7,348,804), which is a divisional and claims the priority benefit of U.S. Patent Application No. 11/041,687, filed January 20, 2005 (now U.S. Patent No. 7,227,383), which claims the priority benefit of U.S. Provisional Application No. 60/546,574, filed February 19, 2004 and U.S. Provisional Application No. 60/586,565, filed July 9, 2004.

46. MOSAID is the current owner of all rights, title, and interest in and to the '438 Patent, including the right to sue for past damages.

47. A true and correct copy of the '438 Patent is attached hereto as **Exhibit D** and is incorporated by reference herein.

48. The '438 Patent generally relates to an integrated circuit that includes first circuitry and sleep transistor circuitry. The first circuitry receives input signals and processes the input signals. The first circuitry also retains data in a sleep state that has low leakage. The sleep transistor circuitry is coupled to the first circuitry and receives a sleep signal that has a negative voltage. The sleep circuitry reduces power consumption of the first circuitry in the sleep state to have low leakage based on the sleep signal while retaining the data in the first circuitry.

49. Claim 1 is illustrative of the claimed invention of the '438 Patent. It is directed to:

1. An integrated circuit comprising:

a plurality of power islands having associated power consumptions, each of the power islands including circuitries and sleep transistors in coupled relation with the circuitries, and the sleep transistors being included within the integrated circuit to facilitate reduction of power consumed by the circuitries;

a power island manager configured to dynamically change the power consumptions based on needs and operation of the integrated circuit, the power island manager in communication with at least one of the power islands; and

an adaptive leakage controller configured to control change of a variable voltage to be applied to the sleep transistors, and the power island manager configured to generate the variable voltage based on a control signal received from the adaptive leakage controller.

50. Numerous companies enjoy a license to the '438 Patent. MediaTek is not licensed to the '438 Patent.

51. United States Patent No. 8,854,077 ("the '077 Patent") is entitled "Low Leakage and Data Retention Circuitry". The United States Patent and Trademark Office duly and legally

issued the '077 Patent on October 7, 2014, from U.S. Patent Application No. 13/569,613, filed on August 8, 2012.

52. The '077 Patent is a continuation of U.S. Patent Application No. 13/074,291, filed March 29, 2011 (now the '438 Patent), which is a continuation of U.S. Patent Application No. 12/542,352, filed August 17, 2009 (now U.S. Patent No. 7,940,081), which is a continuation of U.S. Patent Application No. 12/284,311, filed September 19, 2008 (now U.S. Patent No. 7,592,837), which is a continuation of U.S. Patent Application No. 11/998,725, filed November 30, 2007 (now U.S. Patent No. 7,443,197), which is a continuation of U.S. Patent Application No. 11/732,181, filed April 2, 2007 (now U.S. Patent No. 7,348,804), which is a divisional and claims the priority benefit of U.S. Patent Application No. 11/041,687, filed January 20, 2005 (now U.S. Patent No. 7,227,383), which claims the priority benefit of U.S. Provisional Application No. 60/546,574, filed February 19, 2004 and U.S. Provisional Application No. 60/586,565, filed July 9, 2004.

53. MOSAID is the current owner of all rights, title, and interest in and to the '077 Patent, including the right to sue for past damages.

54. A true and correct copy of the '077 Patent is attached hereto as **Exhibit E** and is incorporated by reference herein.

55. The '077 Patent generally relates to an integrated circuit that includes first circuitry and sleep transistor circuitry. The first circuitry receives input signals and processes the input signals. The first circuitry also retains data in a sleep state that has low leakage. The sleep transistor circuitry is coupled to the first circuitry and receives a sleep signal that has a negative voltage. The sleep circuitry reduces power consumption of the first circuitry in the sleep state to have low leakage based on the sleep signal while retaining the data in the first circuitry.

56. Claim 1 is illustrative of the claimed invention of the '077 Patent. It is directed to:

1. A method carried out in an integrated circuit that includes an adaptive leakage controller, a power manager and a plurality of power islands, the method comprising:

receiving, at the power manager, a control signal from the adaptive leakage controller; and;

employing the power manager to dynamically change power consumptions of the plurality of power islands, the employing the power manager to dynamically change power consumptions including: generating a variable voltage based on the control signal; and providing the variable voltage to at least one of low leakage sleep circuits of the integrated circuit.

57. Numerous companies enjoy a license to the '077 Patent. MediaTek is not licensed to the '077 Patent.

58. United States Patent No. 9,350,349 ("the '349 Patent") is entitled "Low Leakage and Data Retention Circuitry". The United States Patent and Trademark Office duly and legally issued the '349 Patent on May 24, 2016, from U.S. Patent Application No. 14/480,143, filed on September 8, 2014.

59. The '349 Patent is a continuation of U.S. Patent Application No. 13/569,613, filed August 8, 2012, which is a continuation of U.S. Patent Application No. 13/074,291, filed March 29, 2011 (now the '438 Patent), which is a continuation of U.S. Patent Application No. 12/542,352, filed August 17, 2009 (now U.S. Patent No. 7,940,081), which is a continuation of U.S. Patent Application No. 12/284,311, filed September 19, 2008 (now U.S. Patent No. 7,592,837), which is a continuation of U.S. Patent Application No. 11/998,725, filed November 30, 2007 (now U.S. Patent No. 7,443,197), which is a continuation of U.S. Patent Application No. 11/732,181, filed April 2, 2007 (now U.S. Patent No. 7,348,804), which is a divisional and claims the priority benefit of U.S. Patent Application No. 11/041,687, filed January 20, 2005 (now U.S. Patent No.

7,227,383), which claims the priority benefit of U.S. Provisional Application No. 60/586,565, filed July 9, 2004, and U.S. Provisional Application No. 60/546,574, filed February 19, 2004.

60. MOSAID is the current owner of all rights, title, and interest in and to the '349 Patent, including the right to sue for past damages.

61. A true and correct copy of the '349 Patent is attached hereto as **Exhibit F** and is incorporated by reference herein.

62. The '349 Patent generally relates to an integrated circuit that includes first circuitry and sleep transistor circuitry. The first circuitry receives input signals and processes the input signals. The first circuitry also retains data in a sleep state that has low leakage. The sleep transistor circuitry is coupled to the first circuitry and receives a sleep signal that has a negative voltage. The sleep circuitry reduces power consumption of the first circuitry in the sleep state to have low leakage based on the sleep signal while retaining the data in the first circuitry.

63. Claim 1 is illustrative of the claimed invention of the '349 Patent. It is directed to:

1. An integrated circuit comprising:

a plurality of power islands having associated power consumptions capable of being dynamically changed, each of the power islands including circuitries and sleep transistors in coupled relation with the circuitries; and;

a sleep generator in communication with at least one of the power islands to provide a variable voltage, and

the sleep transistors being included within the integrated circuit to facilitate reduction of power consumed by the circuitries, and the sleep transistors being configured to receive the variable voltage that is:

i) generated by the sleep generator based on a control signal receivable from an adaptive leakage controller; and

ii) changed under control of the adaptive leakage controller.

64. Numerous companies enjoy a license to the '349 Patent. MediaTek is not licensed to the '349 Patent.

65. United States Patent No. 7,224,563 ("the '563 Patent") is entitled "Method and Device for Circuit Control". The United States Patent and Trademark Office duly and legally issued the '563 Patent on May 29, 2007, from U.S. Patent Application No. 10/651,360, filed on August 29, 2003.

66. The '563 Patent is entitled to the benefit of U.S. Provisional Application No. 60/480,056, filed June 20, 2003, entitled "A System for Rapid Adaptation of Clock Frequency to Voltage Transients".

67. MOSAID is the current owner of all rights, title, and interest in and to the '563 Patent, including the right to sue for past damages.

68. A true and correct copy of the '563 Patent is attached hereto as **Exhibit G** and is incorporated by reference herein.

69. The '563 Patent generally relates to circuit control that comprises sensing a delivered voltage to a portion of an integrated circuit, determining an appropriate frequency for the portion the integrated circuit, and providing the appropriate frequency to the integrated circuit.

70. Claim 1 is illustrative of the claimed invention of the '563 Patent. It is directed to:

1. A method of circuit control, comprising:
sensing a delivered voltage to a portion of an integrated circuit;
determining an appropriate frequency for the portion of the integrated circuit; and
providing the appropriate frequency to said portion of said integrated circuit.

71. Numerous companies enjoy a license to the '563 Patent. MediaTek is not licensed to the '563 Patent.

II. DEFENDANTS' KNOWLEDGE OF THE ASSERTED PATENTS

72. MediaTek had knowledge of the Asserted Patents prior to the filing of this suit.

73. On or about March 16, 2017, MOSAID (f/k/a Conversant Intellectual Property Management) sent a letter to David Su, Vice President and General Counsel of Defendant MediaTek, Inc., seeking to renew MediaTek's license to MOSAID's patent portfolio, including the Asserted Patents. (See **Exhibit H.**)

74. MOSAID's March 16, 2017 letter to MediaTek included exemplary claim charts exhibiting MediaTek's infringement of several patents, including the '306, '885, and '811 Patents.

75. On January 17, 2018, MOSAID met with MediaTek and provided MediaTek with exemplary claim charts exhibiting MediaTek's infringement of several patents, including each of the Asserted Patents.

76. Since January 17, 2018, MOSAID and MediaTek have engaged in numerous technical and business discussions relating to a license for MOSAID's patent portfolio, including each of the Asserted Patents. During those discussions, MOSAID offered to provide MediaTek with a license to the Asserted Patents. But to date, MediaTek has not made any offer to license MOSAID's patent portfolio, including the Asserted Patents.

77. Before filing this lawsuit, on November 29, 2022, MOSAID attempted one last time to resolve this dispute, and again, MOSAID offered to license its patent portfolio, including the Asserted Patents, to MediaTek on reasonable terms. But again, MediaTek refused.

III. THE INFRINGING PRODUCTS

78. MediaTek manufactures, uses, offers for sale and/or sells in the United States, and/or imports into the United States, processors, including the Infringing Products, for use in a variety of consumer electronics, including mobile phones and tablets. Consumer electronics

containing the Infringing Products have been, and continue to be, widely available for sale in the United States.

79. MediaTek's infringing products include at least the Infringing Products, or substantially similar processors, made, used, sold, or offered for sale in the United States, and/or imported into the United States.

80. MediaTek has and continues to advertise the Infringing Products on the MediaTek website.

81. MediaTek advertises the Helio P10 (MT6755) on its website at <https://www.mediatek.com/products/smartphones-2/mt6755-helio-p10>.

82. MediaTek advertises the Helio X20 (MT6797) on its website at [https://www.mediatek.com/products/smartphones-2/mt6797-helio-x20#:~:text=MediaTek%20Helio%20X20%20\(MT6797\)%20provides,performance%20and%20extended%20battery%20life](https://www.mediatek.com/products/smartphones-2/mt6797-helio-x20#:~:text=MediaTek%20Helio%20X20%20(MT6797)%20provides,performance%20and%20extended%20battery%20life).

83. MediaTek advertises the Dimensity 9000 (MT6983) on its website at <https://www.mediatek.com/products/smartphones-2/mediatek-dimensity-9000>.

84. MediaTek advertises the Dimensity 720 (MT6853) on its website at <https://www.mediatek.com/products/smartphones-2/dimensity-720>.

COUNT I: INFRINGEMENT OF THE '306 PATENT

85. MOSAID incorporates by reference and realleges paragraphs 1 through 84 as if specifically set forth herein.

86. In violation of 35 U.S.C. § 271(a), MediaTek is and has been directly infringing one or more of the claims of the '306 Patent, including at least Claim 16, either literally and/or under the doctrine of equivalents, by making, using, selling, and/or offering for sale in the United States, and/or importing into the United States, without authority, at least the Infringing Products.

87. During license discussions, MOSAID provided MediaTek with claim charts explaining in detail MediaTek's infringement of the '306 Patent, including at least Claim 16.

88. In violation of 35 U.S.C. § 271(b), MediaTek is and has been infringing one or more of the claims of the '306 Patent, including at least Claim 16, indirectly by inducing the infringement of one or more claims of the '306 Patent, including at least Claim 16, by third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, in this District and elsewhere in the United States. Direct infringement by, for example, MediaTek's customers and/or end-users of the Infringing Products, occurs by at least the use of the Infringing Products.

89. Upon information and belief, MediaTek supplies hardware, firmware, and/or software, including software drivers, that are especially made or especially adapted to practice the inventions claimed in the '306 Patent, including at least Claim 16 of the '306 Patent, to induce third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, to use the Infringing Products in a manner that would infringe one or more claims of the '306 Patent, including at least Claim 16 of the '306 Patent.

90. Upon information and belief, MediaTek furnishes instructive materials, technical support, and information concerning the operation and use of the Infringing Products, including with MediaTek's firmware or software drivers, and markets and advertises the Infringing Products on its website, to induce third parties, including MediaTek's customers and/or end-users of the Infringing Products, to use the Infringing Products in a manner that would infringe one or more claims of the '306 Patent, including at least Claim 16 of the '306 Patent.

91. MediaTek knew or should have known of the '306 Patent through a series of correspondence and meetings expressly notifying MediaTek of the '306 Patent and MediaTek's

infringement thereof. As a result, MediaTek knew it infringed one or more claims of the '306 Patent, including at least Claim 16 of the '306 Patent, at least as early as March 16, 2017. Despite this knowledge, MediaTek continued to induce third parties, including MediaTek's customers and/or end-users of the Infringing Products, to infringe one or more claims of the '306 Patent, including at least Claim 16 of the '306 Patent with the specific intent to cause infringement. MediaTek knew or should have known that those acts would induce actual infringement by third parties, including MediaTek's customers and/or end-users of the Infringing Products, of one or more of the claims of the '306 Patent, including at least Claim 16.

92. MediaTek has actual knowledge of the '306 Patent, and its infringement thereof, at least as of the date of filing of this Complaint.

93. Therefore, Defendants have induced infringement by others of one or more of the claims of the '306 Patent, including at least Claim 16, with the specific intent to induce acts that constitute infringement of the '306 Patent and with knowledge that such acts infringed one or more claims of the '306 Patent, including at least Claim 16 of the '306 Patent.

94. In violation of 35 U.S.C. § 271(c), MediaTek is and has been infringing one or more of the claims of the '306 Patent, including at least Claim 16, indirectly by contributing to the infringement of one or more of the claims of the '306 Patent, including at least Claim 16, by third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, in this District and elsewhere in the United States. Direct infringement by, for example, MediaTek's customers and/or end-users of the Infringing Products, occurs by at least the use of the Infringing Products.

95. MediaTek makes and sells hardware and/or software components (*e.g.* processors and/or software drivers) especially made or especially adapted to practice the invention claimed in

the '306 Patent, including at least Claim 16 of the '306 Patent, and that (i) is a material part of the invention and (ii) is not a staple article or commodity of commerce suitable for substantial non-infringing use at least because it is specifically designed to perform the claimed functionality. Any other use of such hardware and/or software would be unusual, far-fetched, illusory, impractical, occasional, aberrant, or experimental.

96. Therefore, Defendants have contributed to the infringement by others of one or more of the claims of the '306 Patent, including at least Claim 16.

97. MediaTek's infringement of one or more claims of the '306 Patent, including at least Claim 16 of the '306 Patent, has been, and continues to be, willful.

98. MediaTek had actual knowledge of the '306 Patent at least as early as March 16, 2017, when MOSAID notified MediaTek of the '306 Patent, and MediaTek's infringement thereof. Despite knowing of the '306 Patent as early as March 16, 2017, MediaTek did not cease its infringing activities.

99. As explained above, between March 16, 2017 and November 29, 2022, MOSAID notified MediaTek on several occasions of the '306 Patent and MediaTek's infringement of one or more claims of the '306 Patent, including at least Claim 16 of the '306 Patent.

100. Despite this knowledge, MediaTek continued to infringe one or more claims of the '306 Patent, including at least Claim 16 of the '306 Patent, in disregard of MOSAID's patent rights. As a result, MediaTek deliberately and intentionally infringed the '306 Patent, and continues to do so, after receiving express and actual knowledge of both the '306 Patent and its infringement thereof.

101. Therefore, MediaTek's infringement of the '306 Patent has been and continues to be willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or

characteristic of a pirate, entitling MOSAID to increased damages pursuant to 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action pursuant to 35 U.S.C. § 285.

COUNT II: INFRINGEMENT OF THE '885 PATENT

102. MOSAID incorporates by reference and realleges paragraphs 1 through 101 as if specifically set forth herein.

103. In violation of 35 U.S.C. § 271(a), MediaTek is and has been directly infringing one or more of the claims of the '885 Patent, including at least Claim 39, either literally and/or under the doctrine of equivalents, by making, using, selling, and/or offering for sale in the United States, and/or importing into the United States, without authority, at least the Infringing Products.

104. During license discussions, MOSAID provided MediaTek with claim charts explaining in detail MediaTek's infringement of the '885 Patent, including at least Claim 39.

105. In violation of 35 U.S.C. § 271(b), MediaTek is and has been infringing one or more of the claims of the '885 Patent, including at least Claim 39, indirectly by inducing the infringement of one or more claims of the '885 Patent, including at least Claim 39, by third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, in this District and elsewhere in the United States. Direct infringement by, for example, MediaTek's customers and/or end-users of the Infringing Products, occurs by at least the use of the Infringing Products.

106. Upon information and belief, MediaTek supplies hardware, firmware, and/or software, including software drivers, that are especially made or especially adapted to practice the inventions claimed in the '885 Patent, including at least Claim 39 of the '885 Patent, to induce third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, to use the Infringing Products in a manner that would infringe one or more claims of the '885 Patent, including at least Claim 39 of the '885 Patent.

107. Upon information and belief, MediaTek furnishes instructive materials, technical support, and information concerning the operation and use of the Infringing Products, including with MediaTek's firmware or software drivers, and markets and advertises the Infringing Products on its website, to induce third parties, including MediaTek's customers and/or end-users of the Infringing Products, to use the Infringing Products in a manner that would infringe one or more claims of the '885 Patent, including at least Claim 39.

108. MediaTek knew or should have known of the '885 Patent through a series of correspondence and meetings expressly notifying MediaTek of the '885 Patent and MediaTek's infringement thereof. As a result, MediaTek knew it infringed one or more claims of the '885 Patent, including at least Claim 39 of the '885 Patent, at least as early as March 16, 2017. Despite this knowledge, MediaTek continued to induce third parties, including MediaTek's customers and/or end-users of the Infringing Products, to infringe one or more claims of the '885 Patent, including at least Claim 39 of the '885 Patent, with the specific intent to cause infringement. MediaTek knew or should have known that those acts would induce actual infringement by third parties, including MediaTek's customers and/or end-users of the Infringing Products, of one or more of the claims of the '885 Patent, including at least Claim 39.

109. MediaTek has actual knowledge of the '885 Patent, and its infringement thereof, at least as of the date of filing of this Complaint.

110. Therefore, MediaTek has induced infringement by others of one or more of the claims of the '885 Patent, including at least Claim 39, with the specific intent to induce acts that constitute infringement of the '885 Patent and with knowledge that such acts infringed one or more claims of the '885 Patent, including at least Claim 39 of the '885 Patent.

111. In violation of 35 U.S.C. § 271(c), MediaTek is and has been infringing one or more of the claims of the '885 Patent, including at least Claim 39, indirectly by contributing to the infringement of one or more of the claims of the '885 Patent, including at least Claim 39, by third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, in this District and elsewhere in the United States. Direct infringement by, for example, MediaTek's customers and/or end-users of the Infringing Products, occurs by at least the use of the Infringing Products.

112. MediaTek makes and sells hardware and/or software components (*e.g.* processors and/or software drivers) especially made or especially adapted to practice the invention claimed in the '885 Patent, including at least Claim 39 of the '885 Patent, and that (i) is a material part of the invention and (ii) is not a staple article or commodity of commerce suitable for substantial non-infringing use at least because it is specifically designed to perform the claimed functionality. Any other use of such hardware and/or software would be unusual, far-fetched, illusory, impractical, occasional, aberrant, or experimental.

113. Therefore, MediaTek has contributed to the infringement by others of one or more of the claims of the '885 Patent, including at least Claim 39.

114. MediaTek's infringement of one or more claims of the '885 Patent, including at least Claim 39 of the '885 Patent, has been, and continues to be, willful.

115. MediaTek had actual knowledge of the '885 Patent at least as early as March 16, 2017, when MOSAID notified MediaTek of the '885 Patent, and MediaTek's infringement thereof. Despite knowing of the '885 Patent as early as March 16, 2017, MediaTek did not cease its infringing activities.

116. As explained above, between March 16, 2017 and November 29, 2022, MOSAID notified MediaTek on several occasions of the '885 Patent and MediaTek's infringement of one or more claims of the '885 Patent, including at least Claim 39 of the '885 Patent.

117. Despite this knowledge, MediaTek continued to infringe one or more claims of the '885 Patent, including at least Claim 39 of the '885 Patent, in disregard of MOSAID's patent rights. As a result, MediaTek deliberately and intentionally infringed the '885 Patent, and continues to do so, after receiving express and actual knowledge of both the '885 Patent and its infringement thereof.

118. Therefore, MediaTek's infringement of the '885 Patent has been and continues to be willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate, entitling MOSAID to increased damages pursuant to 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action pursuant to 35 U.S.C. § 285.

COUNT III: INFRINGEMENT OF THE '811 PATENT

119. MOSAID incorporates by reference and realleges paragraphs 1 through 118 as if specifically set forth herein.

120. In violation of 35 U.S.C. § 271(a), MediaTek is and has been directly infringing one or more of the claims of the '811 Patent, including at least Claim 30, either literally and/or under the doctrine of equivalents, by making, using, selling, and/or offering for sale in the United States, and/or importing into the United States, without authority, at least the Infringing Products.

121. During license discussions, MOSAID provided MediaTek with claim charts explaining in detail MediaTek's infringement of the '811 Patent, including at least Claim 30.

122. In violation of 35 U.S.C. § 271(b), MediaTek is and has been infringing one or more of the claims of the '811 Patent, including at least Claim 30, indirectly by inducing the infringement of one or more of the claims of the '811 Patent, including at least Claim 30, by third

parties, including for example MediaTek's customers and/or end-users of the Infringing Products, in this District and elsewhere in the United States. Direct infringement by, for example, MediaTek's customers and/or end-users of the Infringing Products, occurs by at least the use of the Infringing Products.

123. Upon information and belief, MediaTek supplies hardware, firmware, and/or software, including software drivers, that are especially made or especially adapted to practice the inventions claimed in the '811 Patent, including at least Claim 30 of the '811 Patent, to induce third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, to use the Infringing Products in a manner that would infringe one or more of the claims of the '811 Patent, including at least Claim 30 of the '811 Patent.

124. Upon information and belief, MediaTek furnishes instructive materials, technical support, and information concerning the operation and use of the Infringing Products, including with MediaTek's firmware or software drivers, and markets and advertises the Infringing Products on its website, to induce third parties, including MediaTek's customers and/or end-users of the Infringing Products, to use the Infringing Products in a manner that would infringe one or more claims of the '811 Patent, including at least Claim 30 of the '811 Patent.

125. MediaTek knew or should have known of the '811 Patent through a series of correspondence and meetings expressly notifying MediaTek of the '811 Patent and MediaTek's infringement thereof. As a result, MediaTek knew it infringed one or more of the claims of the '811 Patent, including at least Claim 30 of the '811 Patent, at least as early as March 16, 2017. Despite this knowledge, MediaTek continued to induce third parties, including MediaTek's customers and/or end-users of the Infringing Products, to infringe one or more claims of the '811 Patent, including at least Claim 30 of the '811 Patent, with the specific intent to cause

infringement. MediaTek knew or should have known that those acts would induce actual infringement by third parties, including MediaTek's customers and/or end-users of the Infringing Products, of one or more of the claims of the '811 Patent, including at least Claim 30.

126. MediaTek has actual knowledge of the '811 Patent, and its infringement thereof, at least as of the date of filing of this Complaint.

127. Therefore, MediaTek has induced infringement by others of one or more of the claims of the '811 Patent, including at least Claim 30, with the specific intent to induce acts that constitute infringement of the '811 Patent and with knowledge that such acts infringed one or more claims of the '811 Patent, including at least Claim 30 of the '811 Patent.

128. In violation of 35 U.S.C. § 271(c), MediaTek is and has been infringing one or more of the claims of the '811 Patent, including at least Claim 30, indirectly by contributing to the infringement of one or more of the claims of the '811 Patent, including at least Claim 30, by third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, in this District and elsewhere in the United States. Direct infringement by, for example, MediaTek's customers and/or end-users of the Infringing Products, occurs by at least the use of the Infringing Products.

129. MediaTek makes and sells hardware and/or software components (*e.g.* processors and/or software drivers) especially made or especially adapted to practice the invention claimed in the '811 Patent, including at least Claim 30 of the '811 Patent, and that (i) is a material part of the invention and (ii) is not a staple article or commodity of commerce suitable for substantial non-infringing use at least because it is specifically designed to perform the claimed functionality. Any other use of such hardware and/or software would be unusual, far-fetched, illusory, impractical, occasional, aberrant, or experimental.

130. Therefore, MediaTek has contributed to the infringement by others of one or more of the claims of the '811 Patent, including at least Claim 30.

131. MediaTek's infringement of one or more of the claims of the '811 Patent, including at least Claim 30 of the '811 Patent, has been, and continues to be, willful.

132. MediaTek had actual knowledge of the '811 Patent at least as early as March 16, 2017, when MOSAID notified MediaTek of the '811 Patent, and MediaTek's infringement thereof. Despite knowing of the '811 Patent as early as March 16, 2017, MediaTek did not cease its infringing activities.

133. As explained above, between March 16, 2017 and November 29, 2022, MOSAID notified MediaTek on several occasions of the '811 Patent and MediaTek's infringement of one or more of the claims of the '811 Patent, including at least Claim 30 of the '811 Patent.

134. Despite this knowledge, MediaTek continued to infringe one or more of the claims of the '811 Patent, including at least Claim 30 of the '811 Patent, in disregard of MOSAID's patent rights. As a result, MediaTek deliberately and intentionally infringed the '811 Patent, and continues to do so, after receiving express and actual knowledge of both the '811 Patent and its infringement thereof.

135. Therefore, MediaTek's infringement of the '811 Patent has been and continues to be willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate, entitling MOSAID to increased damages pursuant to 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action pursuant to 35 U.S.C. § 285.

COUNT IV: INFRINGEMENT OF THE '438 PATENT

136. MOSAID incorporates by reference and realleges paragraphs 1 through 135 as if specifically set forth herein.

137. In violation of 35 U.S.C. § 271(a), MediaTek is and has been directly infringing one or more of the claims of the '438 Patent, including at least Claim 1, either literally and/or under the doctrine of equivalents, by making, using, selling, and/or offering for sale in the United States, and/or importing into the United States, without authority, at least the Infringing Products.

138. During license discussions, MOSAID provided MediaTek with claim charts explaining in detail MediaTek's infringement of the '438 Patent, including at least Claim 1.

139. In violation of 35 U.S.C. § 271(b), MediaTek is and has been infringing one or more of the claims of the '438 Patent, including at least Claim 1, indirectly by inducing the infringement of one or more claims of the '438 Patent, including at least Claim 1, by third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, in this District and elsewhere in the United States. Direct infringement by, for example, MediaTek's customers and/or end-users of the Infringing Products, occurs by at least the use of the Infringing Products.

140. Upon information and belief, MediaTek supplies hardware, firmware, and/or software, including software drivers, that are especially made or especially adapted to practice the inventions claimed in the '438 Patent, including at least Claim 1 of the '438 Patent, to induce third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, to use the Infringing Products in a manner that would infringe one or more claims of the '438 Patent, including at least Claim 1 of the '438 Patent.

141. Upon information and belief, MediaTek furnishes instructive materials, technical support, and information concerning the operation and use of the Infringing Products, including with MediaTek's firmware or software drivers, and markets and advertises the Infringing Products on its website, to induce third parties, including MediaTek's customers and/or end-users of the

Infringing Products, to use the Infringing Products in a manner that would infringe one or more claims of the '438 Patent, including at least Claim 1 of the '438 Patent.

142. MediaTek knew or should have known of the '438 Patent through a series of correspondence and meetings expressly notifying MediaTek of the '438 Patent and MediaTek's infringement thereof. As a result, MediaTek knew it infringed one or more claims of the '438 Patent, including at least Claim 1 of the '438 Patent, at least as early as January 17, 2018. Despite this knowledge, MediaTek continued to induce third parties, including MediaTek's customers and/or end-users of the Infringing Products, to infringe one or more claims of the '438 Patent, including at least Claim 1 of the '438 Patent with the specific intent to cause infringement. MediaTek knew or should have known that those acts would induce actual infringement by third parties, including MediaTek's customers and/or end-users of the Infringing Products, of one or more of the claims of the '438 Patent, including at least Claim 1.

143. MediaTek has actual knowledge of the '438 Patent, and its infringement thereof, at least as of the date of filing of this Complaint.

144. Therefore, MediaTek has induced infringement by others of one or more of the claims of the '438 Patent, including at least Claim 1, with the specific intent to induce acts that constitute infringement of the '438 Patent and with knowledge that such acts infringed one or more claims of the '438 Patent, including at least Claim 1 of the '438 Patent.

145. In violation of 35 U.S.C. § 271(c), MediaTek is and has been infringing one or more of the claims of the '438 Patent, including at least Claim 1, indirectly by contributing to the infringement of one or more of the claims of the '438 Patent, including at least Claim 1, by third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, in this District and elsewhere in the United States. Direct infringement by, for example,

MediaTek's customers and/or end-users of the Infringing Products, occurs by at least the use of the Infringing Products.

146. MediaTek makes and sells hardware and/or software components (*e.g.* processors and/or software drivers) especially made or especially adapted to practice the invention claimed in the '438 Patent, including at least Claim 1 of the '438 Patent, and that (i) is a material part of the invention and (ii) is not a staple article or commodity of commerce suitable for substantial non-infringing use at least because it is specifically designed to perform the claimed functionality. Any other use of such hardware and/or software would be unusual, far-fetched, illusory, impractical, occasional, aberrant, or experimental.

147. Therefore, MediaTek has contributed to the infringement by others of one or more of the claims of the '438 Patent, including at least Claim 1.

148. MediaTek's infringement of one or more claims of the '438 Patent, including at least Claim 1 of the '438 Patent, has been, and continues to be, willful.

149. MediaTek had actual knowledge of the '438 Patent at least as early as January 17, 2018, when MOSAID notified MediaTek of the '438 Patent and MediaTek's infringement thereof. Despite knowing of the '438 Patent as early as January 17, 2018, MediaTek did not cease its infringing activities.

150. As explained above, between January 17, 2018 and November 29, 2022, MOSAID notified MediaTek on several occasions of the '438 Patent and MediaTek's infringement of one or more claims of the '438 Patent, including at least Claim 1 of the '438 Patent.

151. Despite this knowledge, MediaTek continued to infringe one or more claims of the '438 Patent, including at least Claim 1 of the '438 Patent, in disregard of MOSAID's patent rights. As a result, MediaTek deliberately and intentionally infringed the '438 Patent, and continues to do

so, after receiving express and actual knowledge of both the '438 Patent and its infringement thereof.

152. Therefore, MediaTek's infringement of the '438 Patent has been and continues to be willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate, entitling MOSAID to increased damages pursuant to 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action pursuant to 35 U.S.C. § 285.

COUNT V: INFRINGEMENT OF THE '077 PATENT

153. MOSAID incorporates by reference and realleges paragraphs 1 through 152 as if specifically set forth herein.

154. In violation of 35 U.S.C. § 271(a), MediaTek is and has been directly infringing one or more of the claims of the '077 Patent, including at least Claim 1, either literally and/or under the doctrine of equivalents, by making, using, selling, and/or offering for sale in the United States, and/or importing into the United States, without authority, at least the Infringing Products.

155. During license discussions, MOSAID provided MediaTek with claim charts explaining in detail MediaTek's infringement of the '077 Patent, including at least Claim 1.

156. In violation of 35 U.S.C. § 271(b), MediaTek is and has been infringing one or more of the claims of the '077 Patent, including at least Claim 1, indirectly by inducing the infringement of one or more claims of the '077 Patent, including at least Claim 1, by third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, in this District and elsewhere in the United States. Direct infringement by, for example, MediaTek's customers and/or end-users of the Infringing Products, occurs by at least the use of the Infringing Products.

157. Upon information and belief, MediaTek supplies hardware, firmware, and/or software, including software drivers, that are especially made or especially adapted to practice the

inventions claimed in the '077 Patent, including at least Claim 1 of the '077 Patent, to induce third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, to use the Infringing Products in a manner that would infringe one or more claims of the '077 Patent, including at least Claim 1 of the '077 Patent.

158. Upon information and belief, MediaTek furnishes instructive materials, technical support, and information concerning the operation and use of the Infringing Products, including with MediaTek's firmware or software drivers, and markets and advertises the Infringing Products on its website, to induce third parties, including MediaTek's customers and/or end-users of the Infringing Products, to use the Infringing Products in a manner that would infringe one or more claims of the '077 Patent, including at least Claim 1.

159. MediaTek knew or should have known of the '077 Patent through a series of correspondence and meetings expressly notifying MediaTek of the '077 Patent and MediaTek's infringement thereof. As a result, MediaTek knew it infringed one or more claims of the '077 Patent, including at least Claim 1 of the '077 Patent, at least as early as January 17, 2018. Despite this knowledge, MediaTek continued to induce third parties, including MediaTek's customers and/or end-users of the Infringing Products, to infringe one or more claims of the '077 Patent, including at least Claim 1 of the '077 Patent, with the specific intent to cause infringement. MediaTek knew or should have known that those acts would induce actual infringement by third parties, including MediaTek's customers and/or end-users of the Infringing Products, of one or more of the claims of the '077 Patent, including at least Claim 1.

160. MediaTek has actual knowledge of the '077 Patent, and its infringement thereof, at least as of the date of filing of this Complaint.

161. Therefore, MediaTek has induced infringement by others of one or more of the claims of the '077 Patent, including at least Claim 1, with the specific intent to induce acts that constitute infringement of the '077 Patent and with knowledge that such acts infringed one or more claims of the '077 Patent, including at least Claim 1 of the '077 Patent.

162. In violation of 35 U.S.C. § 271(c), MediaTek is and has been infringing one or more of the claims of the '077 Patent, including at least Claim 1, indirectly by contributing to the infringement of one or more of the claims of the '077 Patent, including at least Claim 1, by third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, in this District and elsewhere in the United States. Direct infringement by, for example, MediaTek's customers and/or end-users of the Infringing Products, occurs by at least the use of the Infringing Products.

163. MediaTek makes and sells hardware and/or software components (*e.g.* processors and/or software drivers) especially made or especially adapted to practice the invention claimed in the '077 Patent, including at least Claim 1 of the '077 Patent, and that (i) is a material part of the invention and (ii) is not a staple article or commodity of commerce suitable for substantial non-infringing use at least because it is specifically designed to perform the claimed functionality. Any other use of such hardware and/or software would be unusual, far-fetched, illusory, impractical, occasional, aberrant, or experimental.

164. Therefore, MediaTek has contributed to the infringement by others of one or more of the claims of the '077 Patent, including at least Claim 1.

165. MediaTek's infringement of one or more claims of the '077 Patent, including at least Claim 1 of the '077 Patent, has been, and continues to be, willful.

166. MediaTek had actual knowledge of the '077 Patent at least as early as January 17, 2018, when MOSAID notified MediaTek of the '077 Patent, and MediaTek's infringement thereof. Despite knowing of the '077 Patent as early as January 17, 2018, MediaTek did not cease its infringing activities.

167. As explained above, between January 17, 2018 and November 29, 2022, MOSAID notified MediaTek on several occasions of the '077 Patent and MediaTek's infringement of one or more claims of the '077 Patent, including at least Claim 1 of the '077 Patent.

168. Despite this knowledge, MediaTek continued to infringe one or more claims of the '077 Patent, including at least Claim 1 of the '077 Patent, in disregard of MOSAID's patent rights. As a result, MediaTek deliberately and intentionally infringed the '077 Patent, and continues to do so, after receiving express and actual knowledge of both the '077 Patent and its infringement thereof.

169. Therefore, MediaTek's infringement of the '077 Patent has been and continues to be willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate, entitling MOSAID to increased damages pursuant to 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action pursuant to 35 U.S.C. § 285.

COUNT VI: INFRINGEMENT OF THE '349 PATENT

170. MOSAID incorporates by reference and realleges paragraphs 1 through 169 as if specifically set forth herein.

171. In violation of 35 U.S.C. § 271(a), MediaTek is and has been directly infringing one or more of the claims of the '349 Patent, including at least Claim 1, either literally and/or under the doctrine of equivalents, by making, using, selling, and/or offering for sale in the United States, and/or importing into the United States, without authority, at least the Infringing Products.

172. During license discussions, MOSAID provided MediaTek with claim charts explaining in detail MediaTek's infringement of the '349 Patent, including at least Claim 1.

173. In violation of 35 U.S.C. § 271(b), MediaTek is and has been infringing one or more of the claims of the '349 Patent, including at least Claim 1, indirectly by inducing the infringement of one or more of the claims of the '349 Patent, including at least Claim 1, by third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, in this District and elsewhere in the United States. Direct infringement by, for example, MediaTek's customers and/or end-users of the Infringing Products, occurs by at least the use of the Infringing Products.

174. Upon information and belief, MediaTek supplies hardware, firmware, and/or software, including software drivers, that are especially made or especially adapted to practice the inventions claimed in the '349 Patent, including at least Claim 1 of the '349 Patent, to induce third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, to use the Infringing Products in a manner that would infringe one or more of the claims of the '349 Patent, including at least Claim 1 of the '349 Patent.

175. Upon information and belief, MediaTek furnishes instructive materials, technical support, and information concerning the operation and use of the Infringing Products, including with MediaTek's firmware or software drivers, and markets and advertises the Infringing Products on its website, to induce third parties, including MediaTek's customers and/or end-users of the Infringing Products, to use the Infringing Products in a manner that would infringe one or more claims of the '349 Patent, including at least Claim 1 of the '349 Patent.

176. MediaTek knew or should have known of the '349 Patent through a series of correspondence and meetings expressly notifying MediaTek of the '349 Patent and MediaTek's

infringement thereof. As a result, MediaTek knew it infringed one or more of the claims of the '349 Patent, including at least Claim 1 of the '349 Patent, at least as early as January 17, 2018. Despite this knowledge, MediaTek continued to induce third parties, including MediaTek's customers and/or end-users of the Infringing Products, to infringe one or more claims of the '349 Patent, including at least Claim 1 of the '349 Patent with the specific intent to cause infringement. MediaTek knew or should have known that those acts would induce actual infringement by third parties, including MediaTek's customers and/or end-users of the Infringing Products, of one or more of the claims of the '349 Patent, including at least Claim 1.

177. MediaTek has actual knowledge of the '349 Patent, and its infringement thereof, at least as of the date of filing of this Complaint.

178. Therefore, MediaTek has induced infringement by others of one or more of the claims of the '349 Patent, including at least Claim 1, with the specific intent to induce acts that constitute infringement of the '349 Patent and with knowledge that such acts infringed one or more claims of the '349 Patent, including at least Claim 1 of the '349 Patent.

179. In violation of 35 U.S.C. § 271(c), MediaTek is and has been infringing one or more of the claims of the '349 Patent, including at least Claim 1, indirectly by contributing to the infringement of one or more of the claims of the '349 Patent, including at least Claim 1, by third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, in this District and elsewhere in the United States. Direct infringement by, for example, MediaTek's customers and/or end-users of the Infringing Products, occurs by at least the use of the Infringing Products.

180. MediaTek makes and sells hardware and/or software components (*e.g.* processors and/or software drivers) especially made or especially adapted to practice the invention claimed in

the '349 Patent, including at least Claim 1 of the '349 Patent, and that (i) is a material part of the invention and (ii) is not a staple article or commodity of commerce suitable for substantial non-infringing use at least because it is specifically designed to perform the claimed functionality. Any other use of such hardware and/or software would be unusual, far-fetched, illusory, impractical, occasional, aberrant, or experimental.

181. Therefore, MediaTek has contributed to the infringement by others of one or more of the claims of the '349 Patent, including at least Claim 1.

182. MediaTek's infringement of one or more of the claims of the '349 Patent, including at least Claim 1 of the '349 Patent, has been, and continues to be, willful.

183. MediaTek had actual knowledge of the '349 Patent at least as early as January 17, 2018, when MOSAID notified MediaTek of the '349 Patent, and MediaTek's infringement thereof. Despite knowing of the '349 Patent as early as January 17, 2018, MediaTek did not cease its infringing activities.

184. As explained above, between January 17, 2018 and November 29, 2022, MOSAID notified MediaTek on several occasions of the '349 Patent and MediaTek's infringement of one or more of the claims of the '349 Patent, including at least Claim 1 of the '349 Patent.

185. Despite this knowledge, MediaTek continued to infringe one or more of the claims of the '349 Patent, including at least Claim 1 of the '349 Patent, in disregard of MOSAID's patent rights. As a result, MediaTek deliberately and intentionally infringed the '349 Patent, and continues to do so, after receiving express and actual knowledge of both the '349 Patent and its infringement thereof.

186. Therefore, MediaTek's infringement of the '349 Patent has been and continues to be willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or

characteristic of a pirate, entitling MOSAID to increased damages pursuant to 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action pursuant to 35 U.S.C. § 285.

COUNT VII: INFRINGEMENT OF THE '563 PATENT

187. MOSAID incorporates by reference and realleges paragraphs 1 through 186 as if specifically set forth herein.

188. In violation of 35 U.S.C. § 271(a), MediaTek is and has been directly infringing one or more of the claims of the '563 Patent, including at least Claim 1, either literally and/or under the doctrine of equivalents, by making, using, selling, and/or offering for sale in the United States, and/or importing into the United States, without authority, at least the Infringing Products.

189. During license discussions, MOSAID provided MediaTek with claim charts explaining in detail MediaTek's infringement of the '563 Patent, including at least Claim 1.

190. In violation of 35 U.S.C. § 271(b), MediaTek is and has been infringing one or more of the claims of the '563 Patent, including at least Claim 1, indirectly by inducing the infringement of one or more claims of the '563 Patent, including at least Claim 1, by third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, in this District and elsewhere in the United States. Direct infringement by, for example, MediaTek's customers and/or end-users of the Infringing Products, occurs by at least the use of the Infringing Products.

191. Upon information and belief, MediaTek supplies hardware, firmware, and/or software, including software drivers, that are especially made or especially adapted to practice the inventions claimed in the '563 Patent, including at least Claim 1 of the '563 Patent, to induce third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, to use the Infringing Products in a manner that would infringe one or more claims of the '563 Patent, including at least Claim 1 of the '563 Patent.

192. Upon information and belief, MediaTek furnishes instructive materials, technical support, and information concerning the operation and use of the Infringing Products, including with MediaTek's firmware or software drivers, and markets and advertises the Infringing Products on its website, to induce third parties, including MediaTek's customers and/or end-users of the Infringing Products, to use the Infringing Products in a manner that would infringe one or more claims of the '563 Patent, including at least Claim 1 of the '563 Patent.

193. MediaTek knew or should have known of the '563 Patent through a series of correspondence and meetings expressly notifying MediaTek of the '563 Patent and MediaTek's infringement thereof. As a result, MediaTek knew it infringed one or more claims of the '563 Patent, including at least Claim 1 of the '563 Patent, at least as early as January 17, 2018. Despite this knowledge, MediaTek continued to induce third parties, including MediaTek's customers and/or end-users of the Infringing Products, to infringe one or more claims of the '563 Patent, including at least Claim 1 of the '563 Patent with the specific intent to cause infringement. MediaTek knew or should have known that those acts would induce actual infringement by third parties, including MediaTek's customers and/or end-users of the Infringing Products, of one or more of the claims of the '563 Patent, including at least Claim 1.

194. MediaTek has actual knowledge of the '563 Patent, and its infringement thereof, at least as of the date of filing of this Complaint.

195. Therefore, MediaTek has induced infringement by others of one or more of the claims of the '563 Patent, including at least Claim 1, with the specific intent to induce acts that constitute infringement of the '563 Patent and with knowledge that such acts infringed one or more claims of the '563 Patent, including at least Claim 1 of the '563 Patent.

196. In violation of 35 U.S.C. § 271(c), MediaTek is and has been infringing one or more of the claims of the '563 Patent, including at least Claim 1, indirectly by contributing to the infringement of one or more of the claims of the '563 Patent, including at least Claim 1, by third parties, including for example MediaTek's customers and/or end-users of the Infringing Products, in this District and elsewhere in the United States. Direct infringement by, for example, MediaTek's customers and/or end-users of the Infringing Products, occurs by at least the use of the Infringing Products.

197. MediaTek makes and sells hardware and/or software components (*e.g.* processors and/or software drivers) especially made or especially adapted to practice the invention claimed in the '563 Patent, including at least Claim 1 of the '563 Patent, and that (i) is a material part of the invention and (ii) is not a staple article or commodity of commerce suitable for substantial non-infringing use at least because it is specifically designed to perform the claimed functionality. Any other use of such hardware and/or software would be unusual, far-fetched, illusory, impractical, occasional, aberrant, or experimental.

198. Therefore, MediaTek has contributed to the infringement by others of one or more of the claims of the '563 Patent, including at least Claim 1.

199. MediaTek's infringement of one or more claims of the '563 Patent, including at least Claim 1 of the '563 Patent, has been, and continues to be, willful.

200. MediaTek had actual knowledge of the '563 Patent at least as early as January 17, 2018, when MOSAID notified MediaTek of the '563 Patent, and MediaTek's infringement thereof. Despite knowing of the '563 Patent as early as January 17, 2018, MediaTek did not cease its infringing activities.

201. As explained above, between January 17, 2018 and November 29, 2022, MOSAID notified MediaTek on several occasions of the '563 Patent and MediaTek's infringement of one or more claims of the '563 Patent, including at least Claim 1 of the '563 Patent.

202. Despite this knowledge, MediaTek continued to infringe one or more claims of the '563 Patent, including at least Claim 1 of the '563 Patent, in disregard of MOSAID's patent rights. As a result, MediaTek deliberately and intentionally infringed the '563 Patent, and continues to do so, after receiving express and actual knowledge of both the '563 Patent and its infringement thereof.

203. Therefore, MediaTek's infringement of the '563 Patent has been and continues to be willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate, entitling MOSAID to increased damages pursuant to 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action pursuant to 35 U.S.C. § 285.

DAMAGES

204. MediaTek's acts of infringement have caused damages to MOSAID, and MOSAID is entitled to recover the damages it has sustained as a result of MediaTek's wrongful acts in an amount to be determined at trial.

205. MOSAID is entitled to, and now seeks to, recover damages in an amount not less than the maximum amount permitted by law caused by MediaTek's acts of infringement.

206. As a result of MediaTek's acts of infringement, MOSAID has suffered actual and consequential damages. To the fullest extent permitted by law, MOSAID seeks recovery of damages in an amount to compensate for MediaTek's infringement. MOSAID further seeks any other damages to which MOSAID would be entitled to in law or in equity.

INJUNCTIVE RELIEF

207. MediaTek's acts of infringement have caused—and unless restrained and enjoined, MediaTek's acts of infringement will continue to cause—irreparable injury and damage to MOSAID for which MOSAID has no adequate remedy at law. Unless enjoined by this Court, MediaTek will continue to infringe the claims of the Asserted Patents.

ATTORNEYS' FEES

208. MOSAID is entitled to recover reasonable and necessary attorneys' fees under applicable law.

DEMAND FOR JURY TRIAL

209. Pursuant to Rule 38 of the Federal Rules of Civil Procedure, MOSAID demands a trial by jury on all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, MOSAID prays for judgment and requests that the Court find in its favor and against MediaTek. MOSAID respectfully requests that the Court enter preliminary and final orders, declarations, and judgments against MediaTek as are necessary to provide MOSAID with the following relief:

- a. A judgment that MediaTek has infringed and/or is infringing one or more claims of the Asserted Patents, literally or under the doctrine of equivalents, as alleged above;
- b. A judgment that MediaTek has infringed and/or is infringing one or more claims of the Asserted Patents, directly, as alleged above;
- c. A judgment that MediaTek has infringed and/or is infringing one or more claims of the Asserted Patents, indirectly, as alleged above;

d. A judgment that MediaTek's infringement of the claims of the Asserted Patents has been willful;

e. An award for all damages and costs arising out of MediaTek's infringement, to adequately compensate MOSAID for MediaTek's infringement of the Asserted Patents, but in no event less than a reasonable royalty, including supplemental damages for any continuing post-verdict infringement up until entry of the final judgment, with an accounting, as needed;

f. Pre-judgment and post-judgment interest, jointly and severally, in an amount according to proof;

g. Treble damages based on MediaTek's willful infringement;

h. An accounting of damages and any future compensation due to MOSAID for MediaTek's infringement (past, present, or future) not specifically accounted for in a damages award (or other relief), and/or permanent injunctive relief;

i. A judgment that this case is exceptional and an award of reasonable attorneys' fees as provided by 35 U.S.C. § 285 and enhanced damages as provided by 35 U.S.C. § 284;

j. An award of costs of suit;

k. The entry of an order enjoining and restraining MediaTek and its parents, affiliates, subsidiaries, officers, agents, servants, employees, attorneys, successors, and assigns and all persons in active concert or participation therewith, from making, importing, using, offering for sale, selling, or causing to be sold any product falling within the scope of any claim of the Asserted Patents, or otherwise infringing or inducing infringement of any claim of the Asserted Patents; and

- l. All further relief in law or in equity as the Court may deem just and proper.

Dated: March 28, 2023

Respectfully submitted,

/s/ Jamie H. McDole

Jamie H. McDole

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CIVIL COVER SHEET

The JS 44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. (SEE INSTRUCTIONS ON NEXT PAGE OF THIS FORM.)

I. (a) PLAINTIFFS

MOSAID TECHNOLOGIES INC.

(b) County of Residence of First Listed Plaintiff Ottawa, ON Canada
(EXCEPT IN U.S. PLAINTIFF CASES)

(c) Attorneys (Firm Name, Address, and Telephone Number)

SEE ATTACHMENT

DEFENDANTS

MEDIATEK, INC.
MEDIATEK USA, INC.County of Residence of First Listed Defendant Taiwan
(IN U.S. PLAINTIFF CASES ONLY)NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF
THE TRACT OF LAND INVOLVED.

Attorneys (If Known)

II. BASIS OF JURISDICTION (Place an "X" in One Box Only)

- ☐ 1 U.S. Government Plaintiff ☒ 3 Federal Question
(U.S. Government Not a Party)
- ☐ 2 U.S. Government Defendant ☐ 4 Diversity
(Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES (Place an "X" in One Box for Plaintiff and One Box for Defendant)

- | | PTF | DEF | | PTF | DEF |
|---|----------------------------|----------------------------|---|----------------------------|----------------------------|
| Citizen of This State | ☐ 1 | ☐ 1 | Incorporated or Principal Place of Business In This State | ☐ 4 | ☐ 4 |
| Citizen of Another State | ☐ 2 | ☐ 2 | Incorporated and Principal Place of Business In Another State | ☐ 5 | ☐ 5 |
| Citizen or Subject of a Foreign Country | ☐ 3 | ☐ 3 | Foreign Nation | ☐ 6 | ☐ 6 |

IV. NATURE OF SUIT (Place an "X" in One Box Only)

Click here for: [Nature of Suit Code Descriptions.](#)

CONTRACT	TORTS	FORFEITURE/PENALTY	BANKRUPTCY	OTHER STATUTES
☐ 110 Insurance ☐ 120 Marine ☐ 130 Miller Act ☐ 140 Negotiable Instrument ☐ 150 Recovery of Overpayment & Enforcement of Judgment ☐ 151 Medicare Act ☐ 152 Recovery of Defaulted Student Loans (Excludes Veterans) ☐ 153 Recovery of Overpayment of Veteran's Benefits ☐ 160 Stockholders' Suits ☐ 190 Other Contract ☐ 195 Contract Product Liability ☐ 196 Franchise	PERSONAL INJURY ☐ 310 Airplane ☐ 315 Airplane Product Liability ☐ 320 Assault, Libel & Slander ☐ 330 Federal Employers' Liability ☐ 340 Marine ☐ 345 Marine Product Liability ☐ 350 Motor Vehicle ☐ 355 Motor Vehicle Product Liability ☐ 360 Other Personal Injury ☐ 362 Personal Injury - Medical Malpractice PERSONAL INJURY ☐ 365 Personal Injury - Product Liability ☐ 367 Health Care/Pharmaceutical Personal Injury Product Liability ☐ 368 Asbestos Personal Injury Product Liability PERSONAL PROPERTY ☐ 370 Other Fraud ☐ 371 Truth in Lending ☐ 380 Other Personal Property Damage ☐ 385 Property Damage Product Liability	☐ 625 Drug Related Seizure of Property 21 USC 881 ☐ 690 Other LABOR ☐ 710 Fair Labor Standards Act ☐ 720 Labor/Management Relations ☐ 740 Railway Labor Act ☐ 751 Family and Medical Leave Act ☐ 790 Other Labor Litigation ☐ 791 Employee Retirement Income Security Act IMMIGRATION ☐ 462 Naturalization Application ☐ 465 Other Immigration Actions	☐ 422 Appeal 28 USC 158 ☐ 423 Withdrawal 28 USC 157 INTELLECTUAL PROPERTY RIGHTS ☐ 820 Copyrights ☒ 830 Patent ☐ 835 Patent - Abbreviated New Drug Application ☐ 840 Trademark ☐ 880 Defend Trade Secrets Act of 2016 SOCIAL SECURITY ☐ 861 HIA (1395ff) ☐ 862 Black Lung (923) ☐ 863 DIWC/DIWW (405(g)) ☐ 864 SSID Title XVI ☐ 865 RSI (405(g)) FEDERAL TAX SUITS ☐ 870 Taxes (U.S. Plaintiff or Defendant) ☐ 871 IRS—Third Party 26 USC 7609	☐ 375 False Claims Act ☐ 376 Qui Tam (31 USC 3729(a)) ☐ 400 State Reapportionment ☐ 410 Antitrust ☐ 430 Banks and Banking ☐ 450 Commerce ☐ 460 Deportation ☐ 470 Racketeer Influenced and Corrupt Organizations ☐ 480 Consumer Credit (15 USC 1681 or 1692) ☐ 485 Telephone Consumer Protection Act ☐ 490 Cable/Sat TV ☐ 850 Securities/Commodities/Exchange ☐ 890 Other Statutory Actions ☐ 891 Agricultural Acts ☐ 893 Environmental Matters ☐ 895 Freedom of Information Act ☐ 896 Arbitration ☐ 899 Administrative Procedure Act/Review or Appeal of Agency Decision ☐ 950 Constitutionality of State Statutes
REAL PROPERTY ☐ 210 Land Condemnation ☐ 220 Foreclosure ☐ 230 Rent Lease & Ejectment ☐ 240 Torts to Land ☐ 245 Tort Product Liability ☐ 290 All Other Real Property	CIVIL RIGHTS ☐ 440 Other Civil Rights ☐ 441 Voting ☐ 442 Employment ☐ 443 Housing/Accommodations ☐ 445 Amer. w/Disabilities - Employment ☐ 446 Amer. w/Disabilities - Other ☐ 448 Education PRISONER PETITIONS Habeas Corpus: ☐ 463 Alien Detainee ☐ 510 Motions to Vacate Sentence ☐ 530 General ☐ 535 Death Penalty Other: ☐ 540 Mandamus & Other ☐ 550 Civil Rights ☐ 555 Prison Condition ☐ 560 Civil Detainee - Conditions of Confinement			

V. ORIGIN (Place an "X" in One Box Only)

- ☒ 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from Another District (specify) ☐ 6 Multidistrict Litigation - Transfer ☐ 8 Multidistrict Litigation - Direct File

VI. CAUSE OF ACTION

Cite the U.S. Civil Statute under which you are filing (Do not cite jurisdictional statutes unless diversity):
35 U.S.C. § 271Brief description of cause:
Patent Infringement

VII. REQUESTED IN COMPLAINT:

☐ CHECK IF THIS IS A CLASS ACTION UNDER RULE 23, F.R.Cv.P.

DEMAND \$

CHECK YES only if demanded in complaint:

JURY DEMAND: ☒ Yes ☐ No

VIII. RELATED CASE(S) IF ANY

(See instructions):

JUDGE

DOCKET NUMBER

DATE

Mar 28, 2023

SIGNATURE OF ATTORNEY OF RECORD

/s/ Jamie H. McDole

FOR OFFICE USE ONLY

RECEIPT # AMOUNT APPLYING IFP JUDGE MAG. JUDGE

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EXHIBIT A



US007051306B2

(12) **United States Patent**
Hoberman et al.

(10) **Patent No.:** **US 7,051,306 B2**
(45) **Date of Patent:** **May 23, 2006**

(54) **MANAGING POWER ON INTEGRATED CIRCUITS USING POWER ISLANDS**

6,667,648 B1 * 12/2003 Stout et al. 327/333
6,779,163 B1 * 8/2004 Bednar et al. 716/7
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(75) Inventors: **Barry Alan Hoberman**, Cupertino, CA (US); **Daniel L. Hillman**, San Jose, CA (US); **Jon Shiell**, San Jose, CA (US)

(73) Assignee: **MOSAID Technologies Corporation**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/840,893**

(22) Filed: **May 7, 2004**

(65) **Prior Publication Data**

US 2004/0268278 A1 Dec. 30, 2004

Related U.S. Application Data

(60) Provisional application No. 60/468,742, filed on May 7, 2003.

(51) **Int. Cl.**
G06F 17/50 (2006.01)

(52) **U.S. Cl.** **716/6; 716/1; 716/4; 716/5**

(58) **Field of Classification Search** **716/6, 716/5, 4, 1**

See application file for complete search history.

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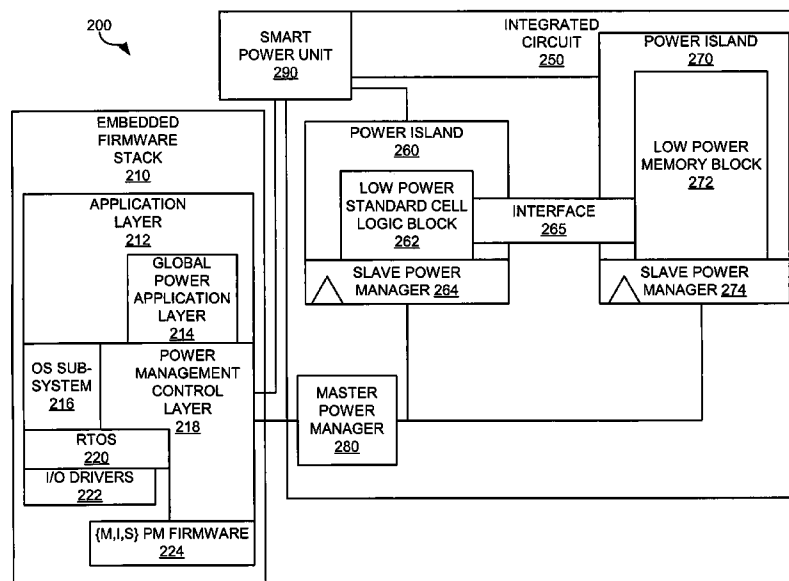
Primary Examiner—Sun James Lin

(74) *Attorney, Agent, or Firm*—Carr & Ferrell LLP

(57) **ABSTRACT**

Systems and methods manage power in an integrated circuit using power islands. The integrated circuit includes a plurality of power islands where power consumption is independently controlled within each of the power islands. A power manager determines a target power level for one of the power islands. The power manager then determines an action to change a consumption power level of the one of the power islands to the target power level. The power manager performs the action to change the consumption power level of the one of the power islands to the target power level.

51 Claims, 13 Drawing Sheets



US 7,051,306 B2

Page 2

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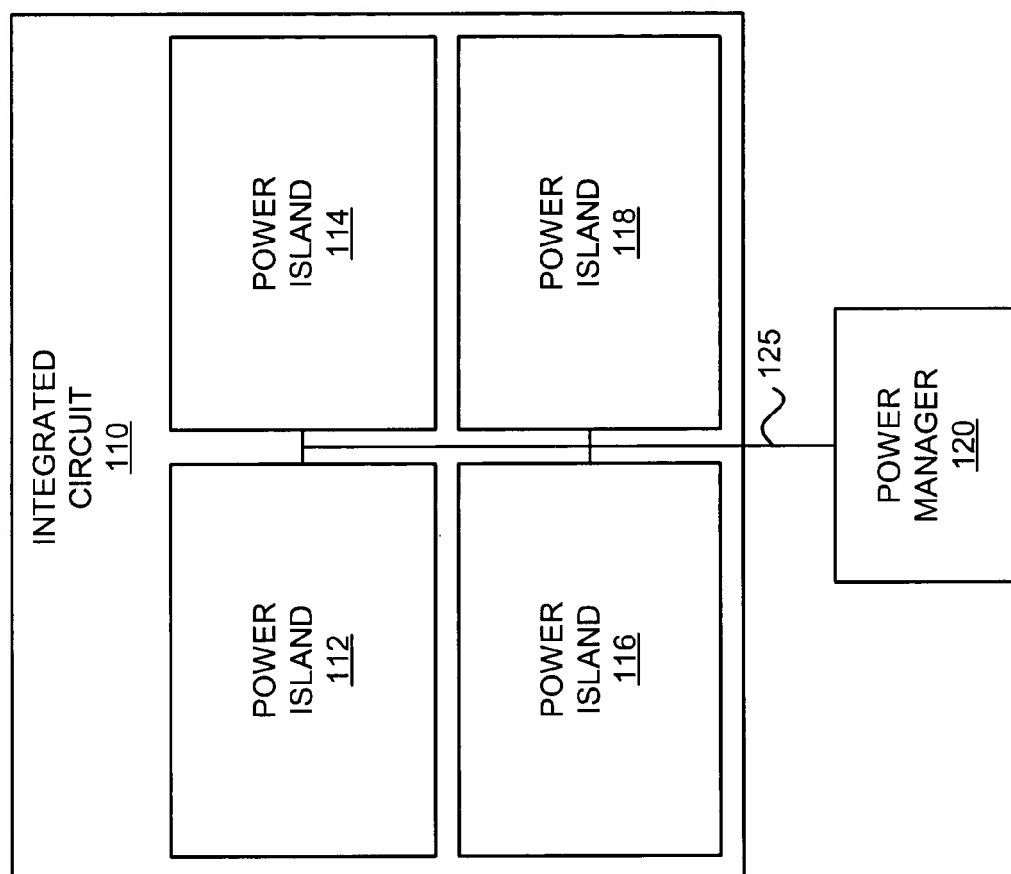


FIG. 1

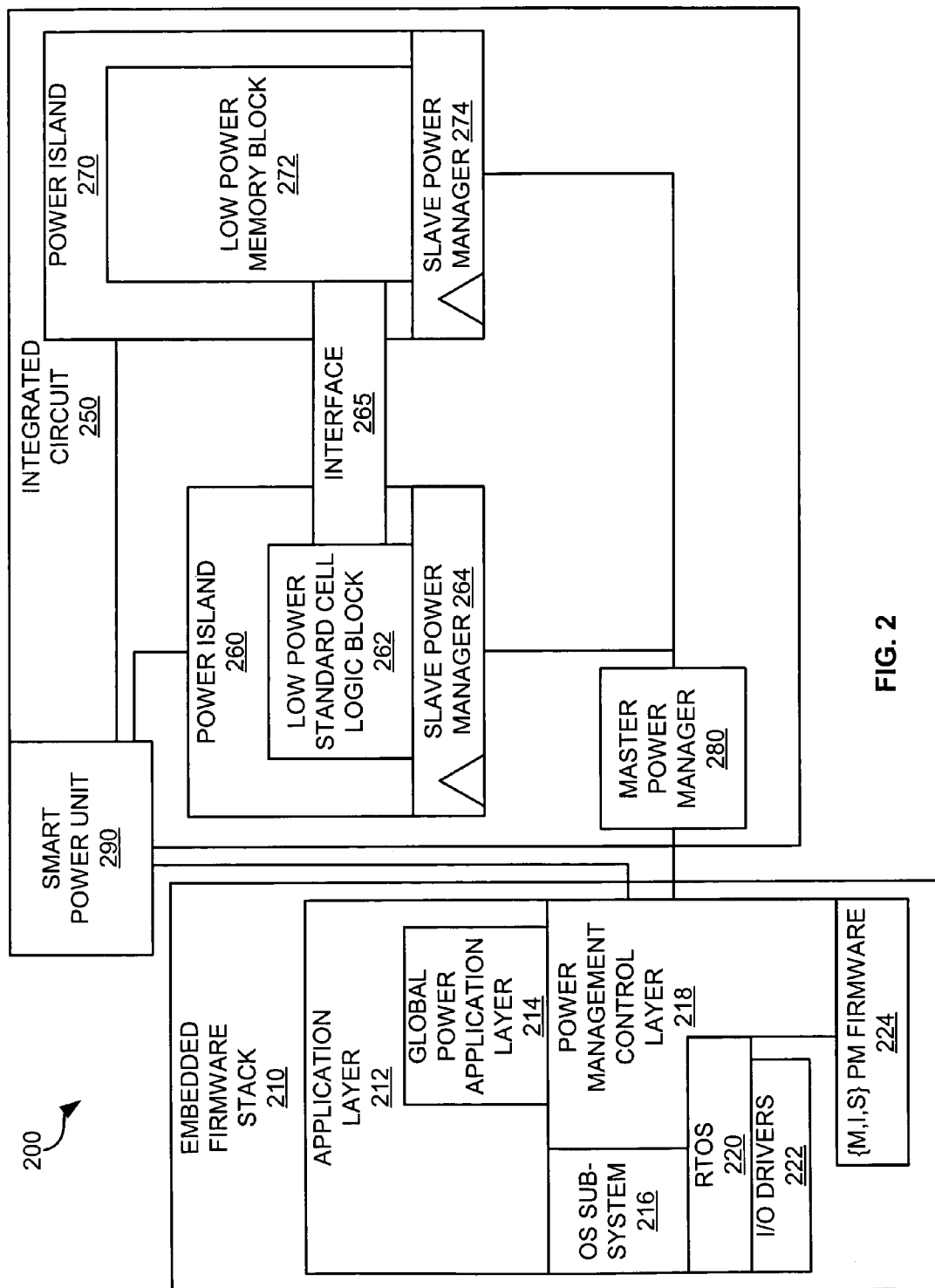


FIG. 2

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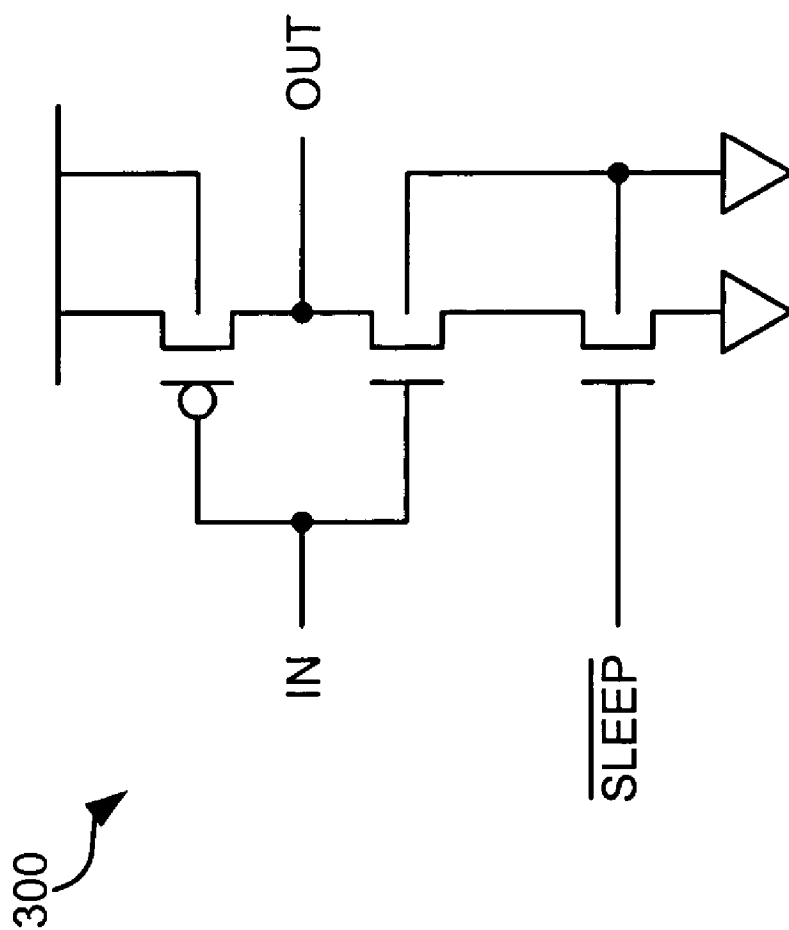


FIG. 3

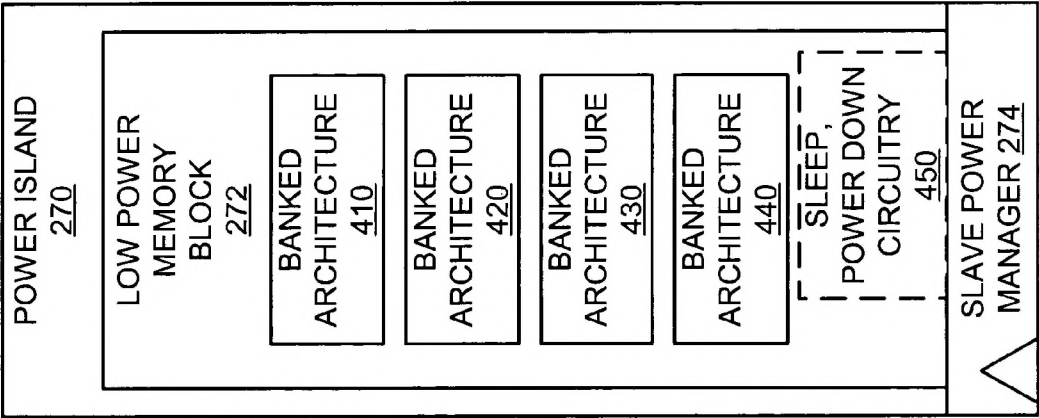


FIG. 4

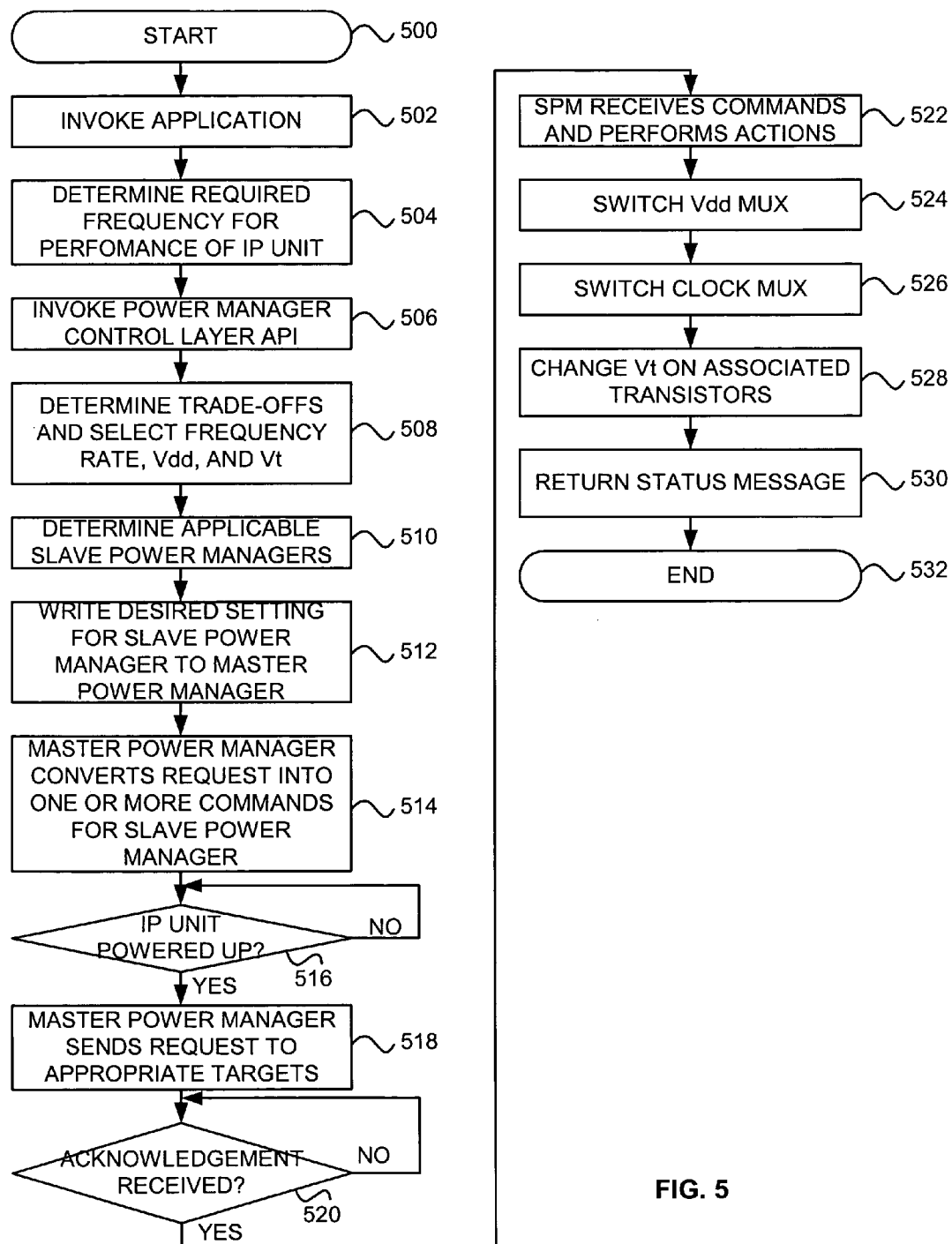


FIG. 5

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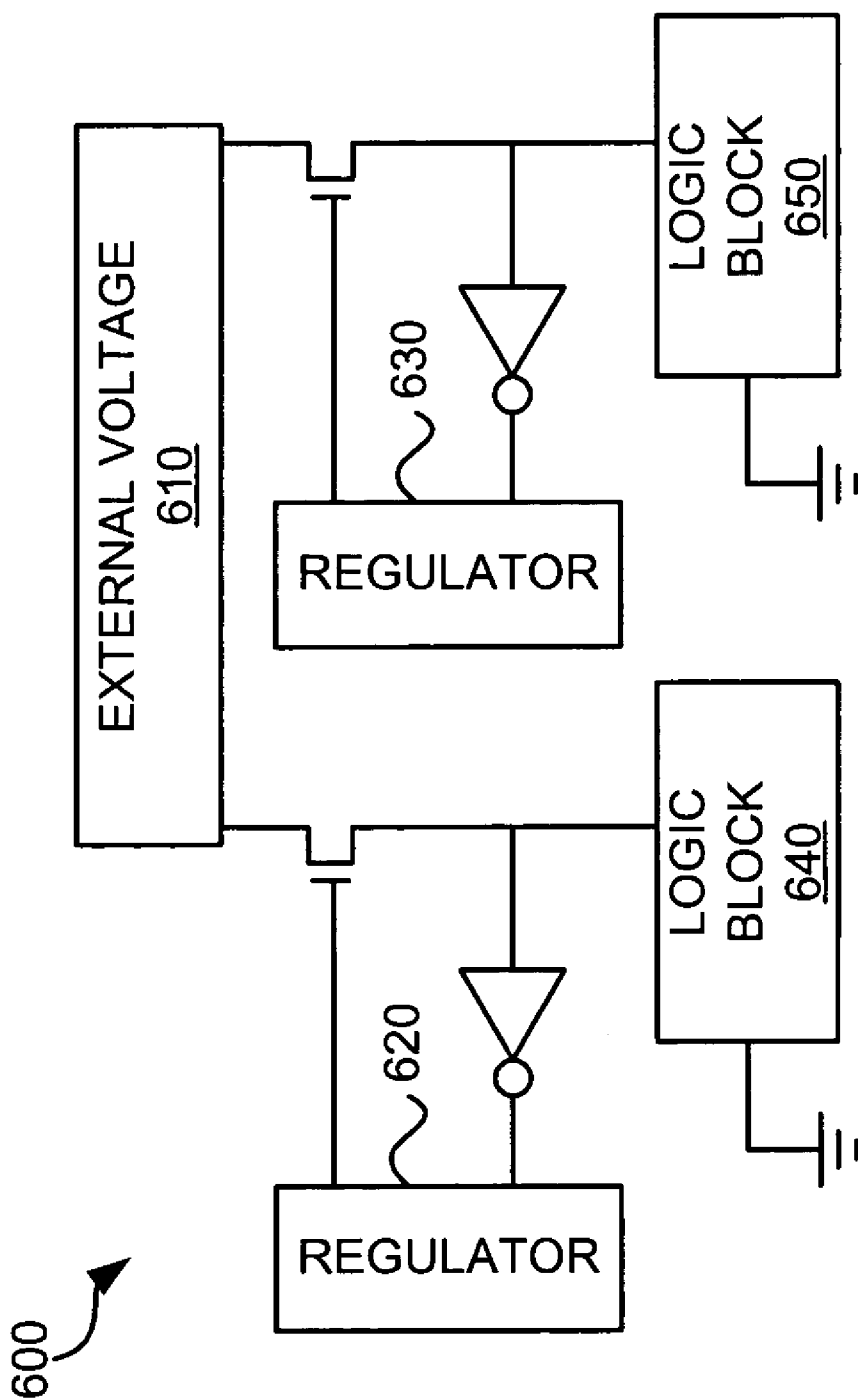


FIG. 6

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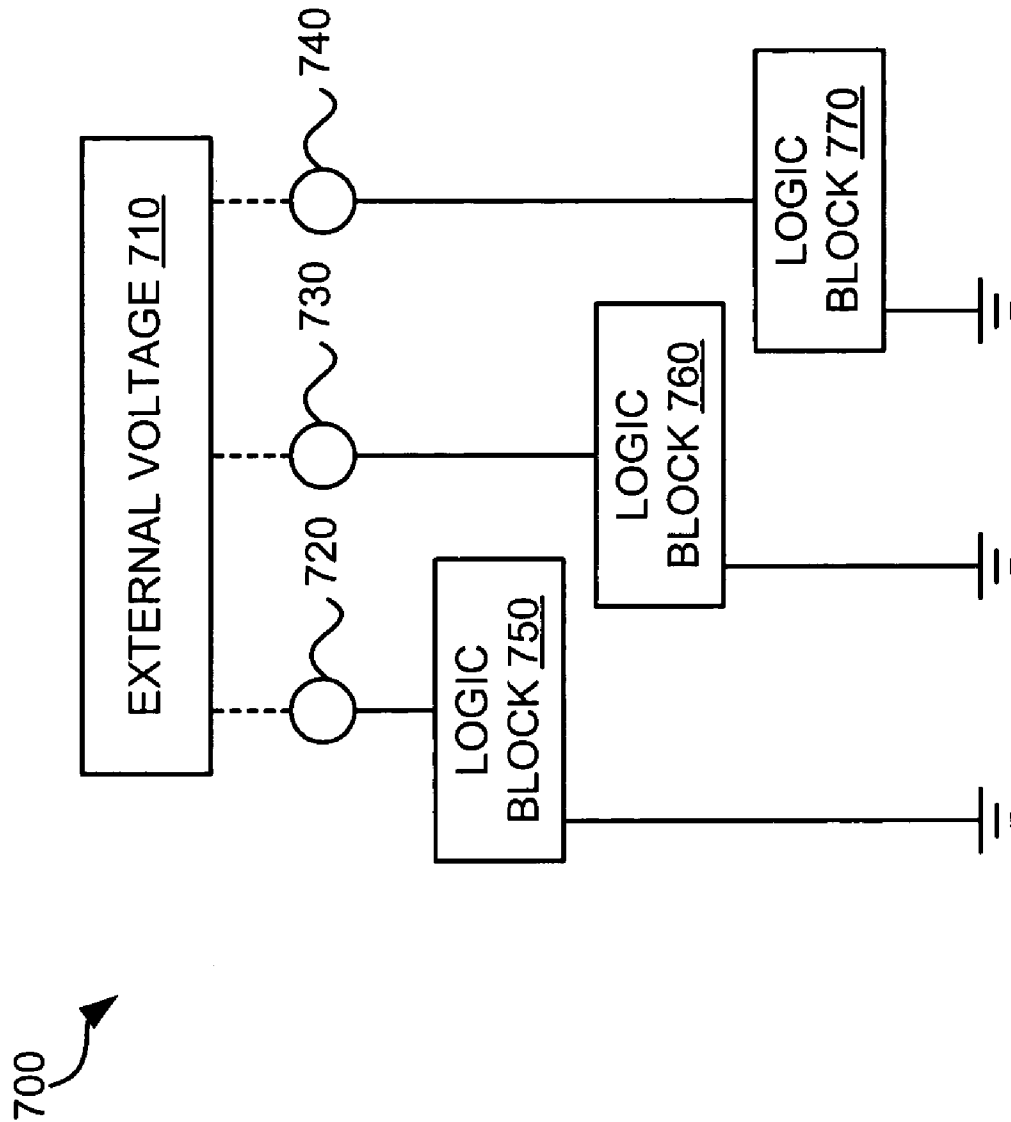


FIG. 7

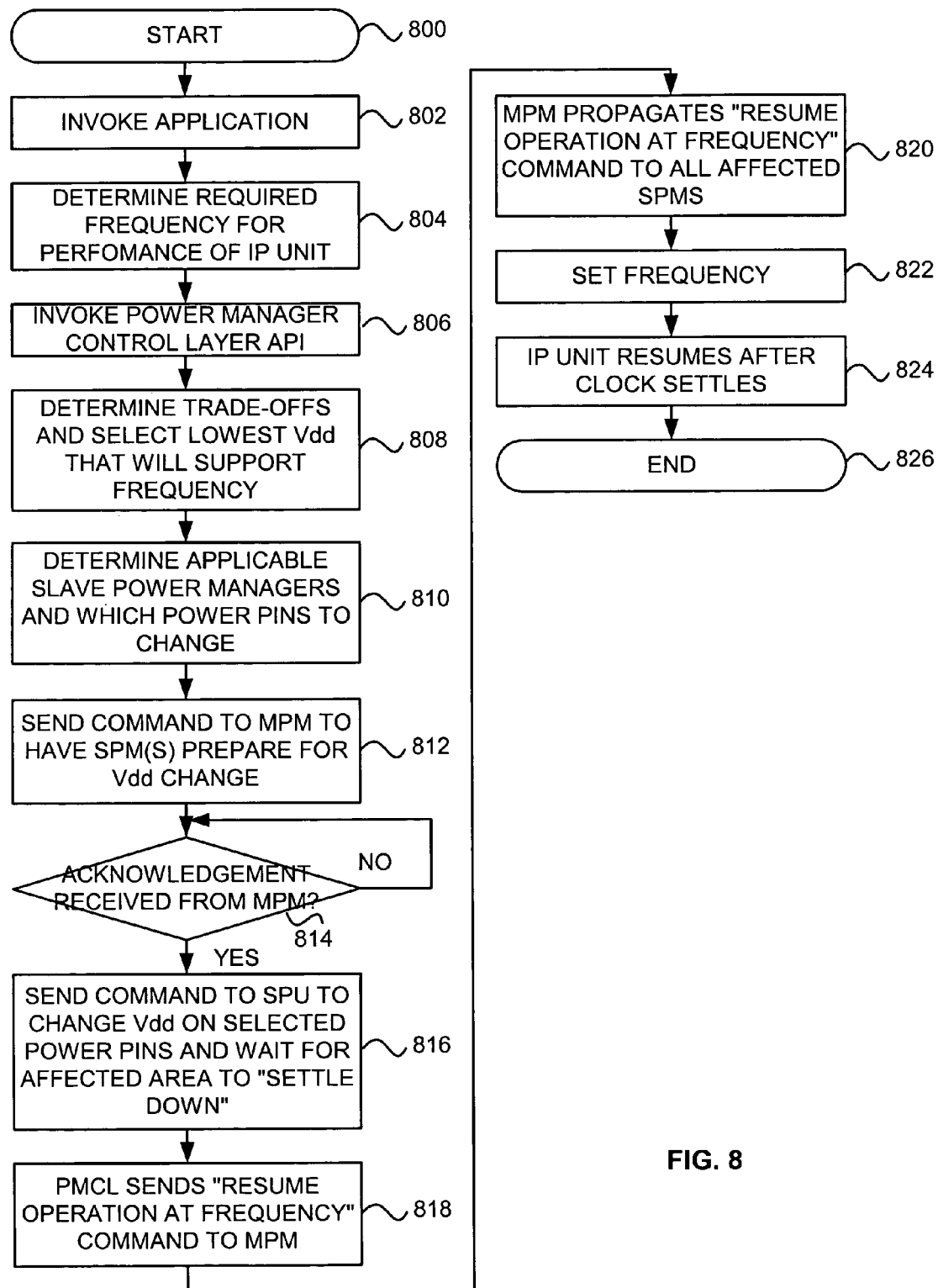


FIG. 8

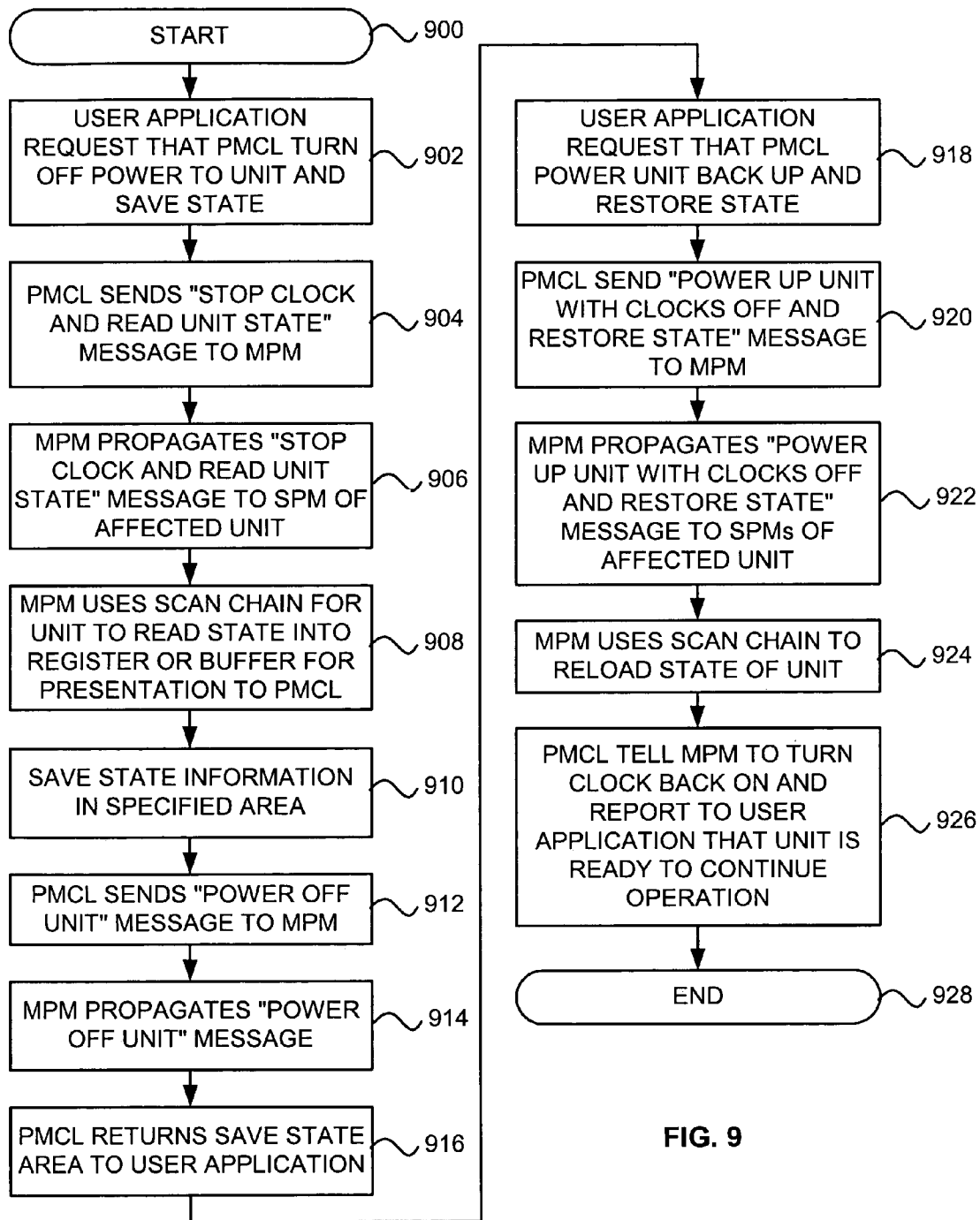


FIG. 9

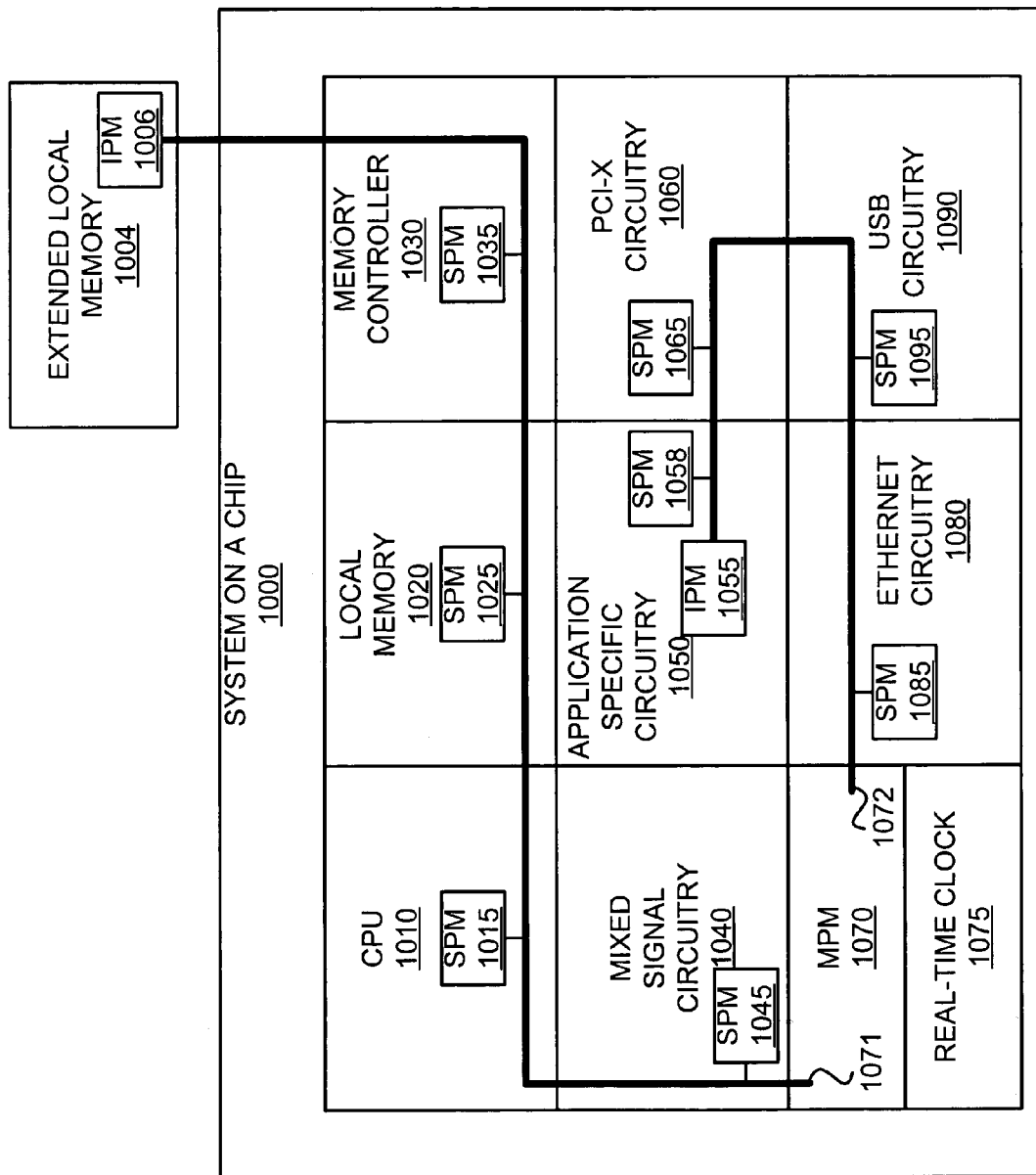


FIG. 10

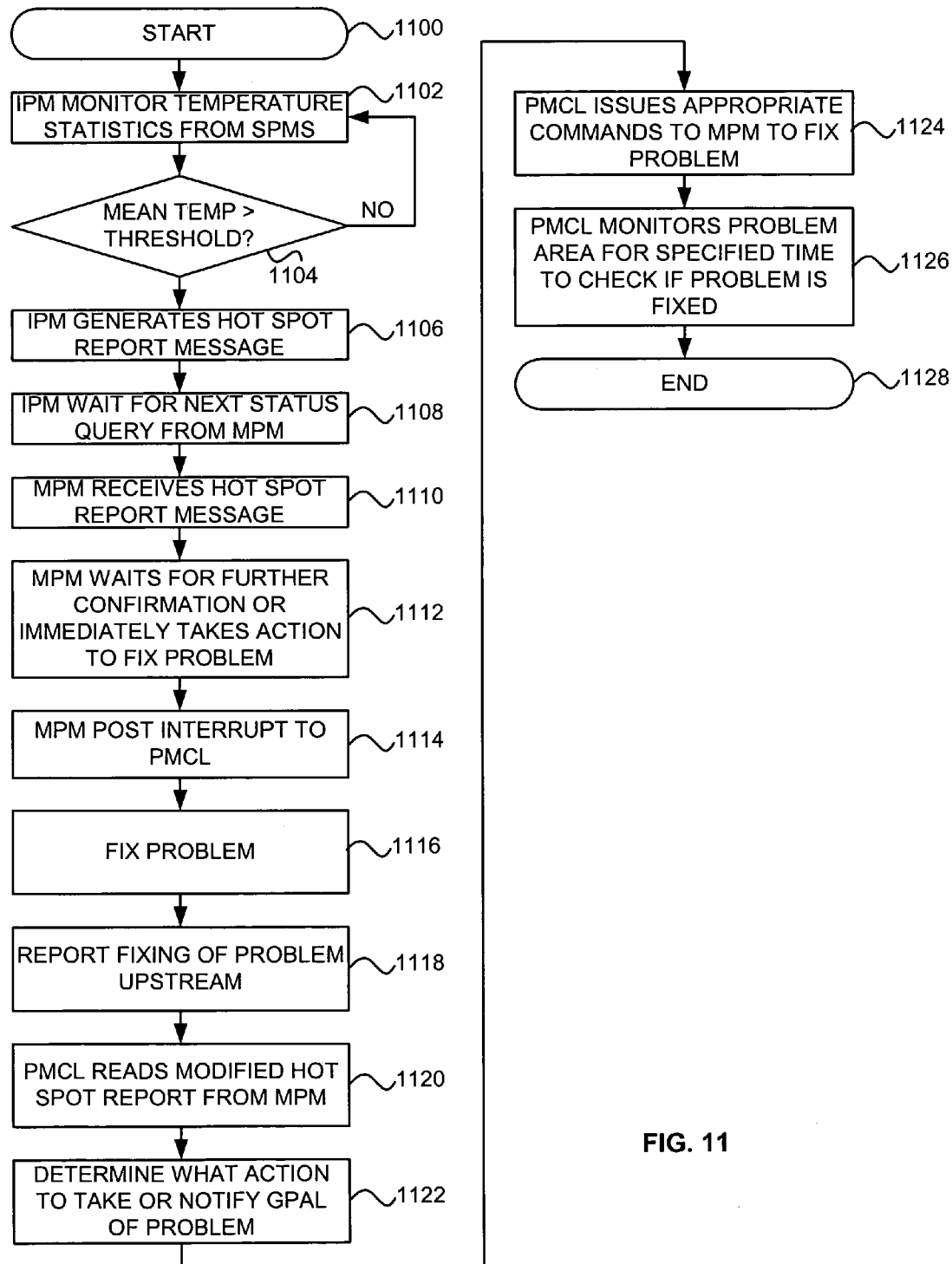


FIG. 11

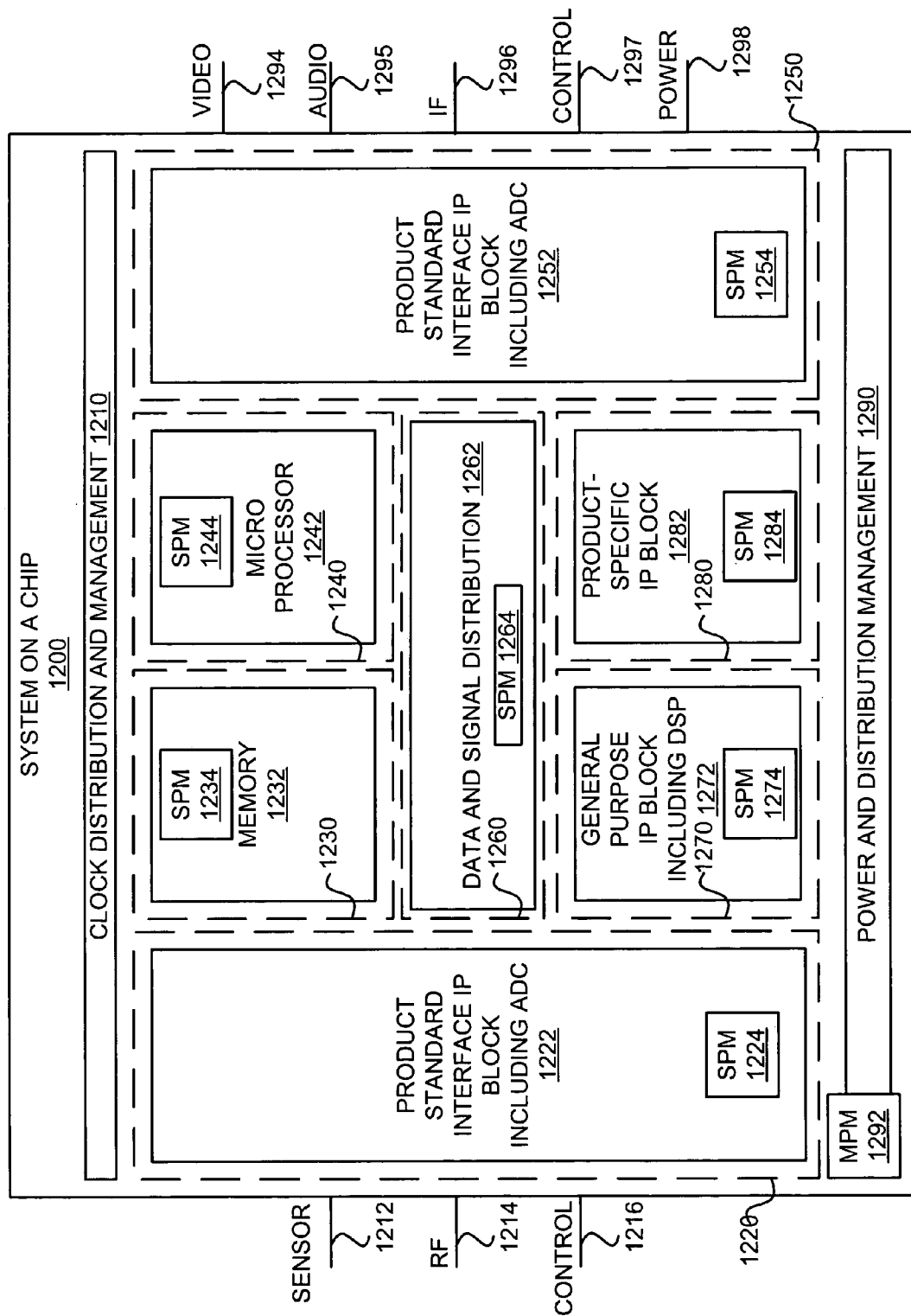


FIG. 12

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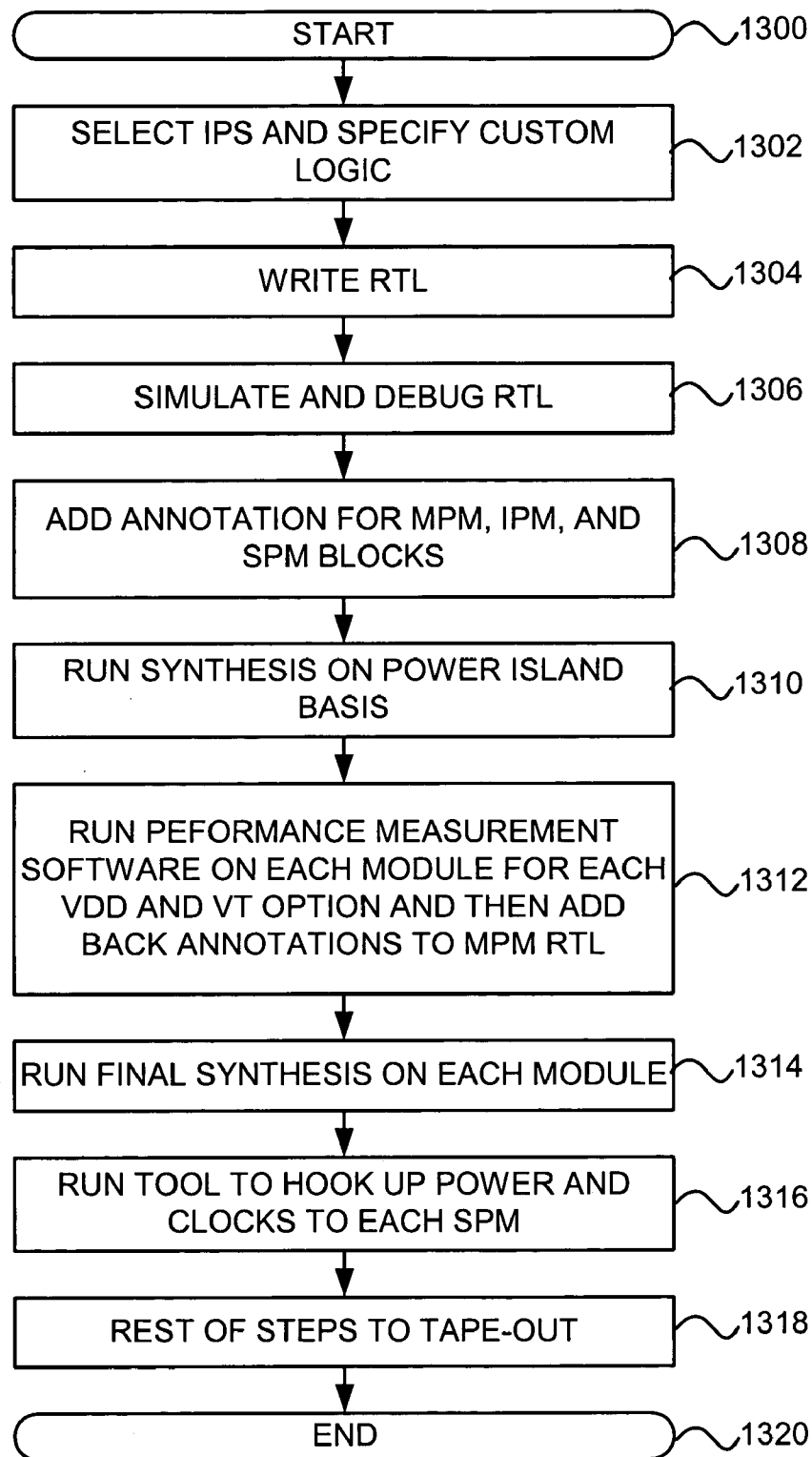


FIG. 13

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**MANAGING POWER ON INTEGRATED
CIRCUITS USING POWER ISLANDS****CROSS-REFERENCE TO RELATED
APPLICATIONS**

This application claims the benefit of U.S. Provisional Application Ser. No. 60/468,742 titled "System and Method for Managing Power in Integrated Circuits," filed May 7, 2003, which is hereby incorporated by reference.

BACKGROUND**1. Field of the Invention**

The present invention relates generally to integrated circuits, and more particularly to managing power on integrated circuits using power islands.

2. Description of the Prior Art

One design goal for integrated circuits is to reduce power consumption. Devices with batteries such as cell phones and laptops especially need a reduction in power consumption in the integrated circuit to extend the charge of the battery. Additionally, a reduction in power consumption prevents overheating and lowers the heat dissipation of the integrated circuit, which in some cases, eliminates or simplifies the heat sinks and/or fans for the integrated circuit.

Some integrated circuits are designed using building blocks of library cells. These library cells are blocks of circuitry performing a function. Some examples of library cells are NAND gates, multiplexers, decoders, comparators, and memory.

In a "full-custom" flow, the integrated circuit is designed at the lowest level such as at the individual transistors, capacitors, and resistors level. The "full-custom" flow may use library cells that are internally developed. The integrated circuit can have optimal performance because the integrated circuit is designed in great detail at the lowest level. However, some problems with the "full-custom" flow are the long time and expensive costs associated with designing at such a detailed level. Furthermore, the "full-custom" flow is cumbersome because the design is at the lowest level.

In a "standard-cell" flow, the integrated circuit is designed using library cells acquired from a third party or other outside source. These library cells are standardized at the logic or function level. The design time for the standard-cell flow is reduced because the library cells are already pre-designed and pre-tested.

In one example for designing an integrated circuit, the library cells are selected, and the custom logic is specified to build the integrated circuit. The register transfer level (RTL) for the integrated circuit is then written for simulation and debugging. After simulation and debugging, the synthesis is run for the integrated circuit. Performance measurement software is executed to determine performance of the integrated circuit. The final synthesis of the integrated circuit can then be run based on the optimal performance of the integrated circuit.

One problem with many integrated circuits is that power consumption is not efficiently utilized. For example, the entire integrated circuit may operate at a maximum frequency just to support an application needing that maximum frequency, while other portions of the integrated circuit can operate at a lower frequency. In another example, inactive circuitry within the integrated circuit consumes power and increases the likelihood of leakage. Inefficient power consumption may also adversely affect performance of the integrated circuit.

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With the growing complexity of integrated circuits, the reduction of power consumption is even more important when the integrated circuit employs more functionality. One example of an integrated circuit is a system-on-a-chip that includes a microprocessor, memory, I/O interfaces, and an analog-to-digital converter all in a single chip. With many different types of functionality employed within a single chip, the system-on-a-chip consumes even more power than single function integrated circuits.

Some prior integrated circuits have employed voltage islands or multiple clocks to lower power consumption. One problem with these integrated circuits is that the voltages in the power island and the frequencies of the multiple clocks are static. The voltages and the frequencies do not dynamically change based on the needs and operation of the integrated circuit.

SUMMARY OF THE INVENTION

The invention addresses the above problems by managing power in an integrated circuit using power islands. The integrated circuit includes a plurality of power islands where power consumption is independently controlled within each of the power islands. A power manager determines a target power level for one of the power islands. The power manager then determines an action to change a consumption power level of the one of the power islands to the target power level. The power manager performs the action to change the consumption power level of the one of the power islands to the target power level. Power control circuitry controls the power of the one of the power islands.

The power islands may be delineated based on geographic factors or functional circuitry of the integrated circuit. In some embodiments, the action is selecting a clock frequency for one of the power islands or selecting a clock for one of the power islands. In some embodiments, the action is modifying voltage for one of the power islands. The action may be powering on or off one of the power islands.

In some embodiments, the power manager monitors the power consumption level of one of the power islands, determines whether a threshold level was crossed based on the power consumption level, and performs the action based on the crossing of the threshold level. In some embodiments, the power manager saves and restores a state of components within one of the power islands.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a system for managing power in an integrated circuit in an exemplary implementation of the invention;

FIG. 2 is a diagram of a system for managing power in an integrated circuit in an exemplary implementation of the invention;

FIG. 3 is an illustration for low leakage circuitry for a low power standard cell logic block in an exemplary implementation of the invention;

FIG. 4 is a diagram of a power island in an exemplary implementation of the invention;

FIG. 5 is a flowchart from an application request to a slave power manager action in an exemplary implementation of the invention;

FIG. 6 is an illustration of internal circuitry for a smart power unit in an exemplary implementation of the invention;

FIG. 7 is an illustration of external circuitry for a smart power unit in an exemplary implementation of the invention;

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FIG. 8 is a flowchart from an application request to a smart power unit action in an exemplary implementation of the invention;

FIG. 9 is a flowchart for saving an IP unit's state prior to powering down and restoring the IP unit's state when powering up in an exemplary implementation of the invention;

FIG. 10 is diagram of a system on a chip and an extended local memory in an exemplary implementation of the invention;

FIG. 11 is a flowchart for generating a "hot spot" report from an intermediate power manager to a power management control layer in an exemplary implementation of the invention.

FIG. 12 is a diagram of a system on a chip in an exemplary implementation of the invention; and

FIG. 13 is a flowchart for building a chip with power islands in an exemplary implementation of the invention.

DETAILED DESCRIPTION OF THE INVENTION

As shown in the exemplary drawings wherein like reference numerals indicate like or corresponding elements among the figures, exemplary embodiments of a system and method according to the present invention are described below in detail. It is to be understood, however, that the present invention may be embodied in various forms. Therefore, specific details disclosed herein are not to be interpreted as limiting, but rather as a basis for the claims and as a representative basis for teaching one skilled in the art to employ the present invention in virtually any appropriately detailed system, structure, method, process or manner.

FIG. 1 depicts a block diagram of a system 100 for managing power in an integrated circuit 110 in an exemplary implementation of the invention. The system 100 includes an integrated circuit 110 and a power manager 120. The integrated circuit 110 is any electronic device that is instantiated into silicon and/or related manufacturing materials. One example of the integrated circuit 110 is a system-on-a-chip. The integrated circuit 110 includes multiple IP units, which are blocks of circuitry performing specific functions.

The integrated circuit 110 includes four power islands 112, 114, 116, and 118. FIG. 1 only depicts four power islands 112, 114, 116, and 118 for the sake of simplicity. Other embodiments of the integrated circuit 110 include a plurality of power islands 112, 114, 116, and 118. The power islands 112, 114, 116, and 118 are coupled to a bus 125.

A power island 112, 114, 116, and 118 is any section, delineation, partition, or division of the integrated circuit 110 where power consumption is controlled within the section, delineation, partition, or division. In some embodiments, the power islands 112, 114, 116, and 118 are delineated based on geographic factors of the integrated circuit 110. In some embodiments, the power islands 112, 114, 116, and 118 are delineated based on functional IP units of the integrated circuit 110. In one example depicted in FIG. 10, power islands are delineated by memory, a microprocessor, and separate IP blocks. In some embodiments, the power islands 112, 114, 116, and 118 are asynchronous or synchronous to each other. In some embodiments, the power islands 112, 114, 116, and 118 comprise sub-islands of power to provide further specificity in controlling power in the integrated circuit 110. In some embodiments, each of the power islands 112, 114, 116, and 118 supports multiple clock

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domains with its own control. In some embodiments, the clocks within the power islands 112, 114, 116, and 118 are variable.

In some embodiments, each of the power islands 112, 114, 116, and 118 includes power control circuitry. Power control circuitry is any circuitry configured to control power within one of the power islands 112, 114, 116, and 118. Some examples of power control circuitry include circuitry for level shifting, signal isolation, Vdd multiplexing, clock multiplexing, and dynamic back bias. In some embodiments, the power control circuitry is included in a standard cell library for standard cell design of the integrated circuit 110.

The power manager 120 is also coupled to the bus 125. One example of the bus 125 is a power command bus described in further detail below in FIG. 10. Other embodiments of the system 100 include numerous variations in which the power manager 120 and the power islands 112, 114, 116, and 118 are interconnected. The power manager 120 is any circuitry, device, or system configured to (1) determine a target power level for one of the power islands 112, 114, 116, and 118 where power consumption is independently controlled within each of the power islands 112, 114, 116, and 118, (2) determine action to change a consumption power level of the one of the power islands 112, 114, 116, and 118 to the target power level, and (3) perform the action to change the consumption power level of the one of the power islands 112, 114, 116, and 118 to the target power level. The power manager 120 can dynamically change the power consumption of the power islands 112, 114, 116, and 118 based on the needs and operation of the integrated circuit 110. The target power level is a desired, calculated, or specified power consumption of the power islands 112, 114, 116, and 118. Some examples of the power manager 120 are the slave power manager (SPM), the intermediate power manager (IPM), and the master power manager (MPM), which are described in further detail below. The power manager 120 may be a hierarchy or group of power managers 120. Although FIG. 1 depicts the power manager 120 as being located outside the integrated circuit 110, other embodiments may have the power manager 120 located in the integrated circuit 110. In other embodiments, the power manager 120 may be distributed among multiple power managers that are on or off the integrated circuit 110 or integrated with a CPU.

The action is any instruction, message, process, function, signal, or variable that controls power consumption in the power island 112, 114, 116, and 118. Some examples of actions are clock gating and dynamic clock selection. Another example of an action is modifying a clock frequency of one of the power islands 112, 114, 116, and 118. Another example of an action is to modify voltage of one of the power islands 112, 114, 116, and 118 such as dynamic voltage source, Vdd, selection. Another example of an action is to control dynamic leakage by controlling variable Vt transistors.

FIG. 2 depicts a diagram of a system 200 for managing power in an integrated circuit 250 in an exemplary implementation of the invention. The system 200 includes an embedded firmware stack 210 and an integrated circuit 250. The embedded firmware stack 210 includes software layers that run on a central processing unit (CPU). In some embodiments, the embedded firmware stack 210 may include an application layer 212, an operating system (OS) sub-system 216, a power management control layer (PMCL) 218, a real-time operating system (RTOS) 220, I/O drivers 222, and power manager (PM) firmware 224 for the MPM, IPM and/or SPM.

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The integrated circuit 250 includes a power island 260, a power island 270, and a MPM 280. The power island 260 includes a low power standard cell logic block 262 and a SPM 264. The power island 270 includes a low power memory block 272 and a SPM 274. The low power standard cell logic block 262 and the low power memory block are coupled to an interface 265. The MPM 280 is coupled to the PMCL 218, the SPM 264, and the SPM 274.

In some embodiments, the application layer 212 includes a global power application layer (GPAL) 214. This GPAL 214 may be useful for more complex applications. If the GPAL 214 is present, then all calls to the PMCL 218 application program interfaces (API) are first directed to the GPAL 214. Both the GPAL 214 and the PMCL 218 provide power management for the integrated circuit 250. In some embodiments, the GPAL 214 and/or the PMCL 218 monitor what load is on each power island 260 and 270. Also, the GPAL 214 and/or the PMCL 218 may build a history of power levels on the power island 260 and 270 and store the history data in a database. The GPAL 214 and the PMCL 218 may also provide data for on-demand resources interested in the power levels of the power islands 260 and 270.

In some embodiments when the GPAL 214 is present, the GPAL 214 provides guidance to the PMCL 218 in making local decisions for power management of the integrated circuit 250. In some embodiments, the GPAL 214 and the PMCL 218 include complex algorithms for a static schedule. The GPAL 214 and the PMCL 218 provide the facility for use code to interact and control power behavior and parameters including providing a database and statistics.

The PMCL 218 also collects information from the MPM 280 and provides commands to the MPM 280 for possible IPMs, SPMs 264 and 274, and the power islands 260 and 270. Some of the commands may be to power on/off, change the power level, or change the frequency of the power islands 260 and 270. In some embodiments with a smart power unit (SPU) 290, the GPAL 214 and the PMCL 218 are responsible for communication with the SPU 290 to implement a power policy and collect information on the actual power supply. The SPU 290 is described in further detail below in FIGS. 6-8. In some embodiments, the GPAL 214 and the PMCL 218 provides sockets for existing power management techniques.

The power manager firmware 224 is firmware executed by the master power manager 280, the intermediate power manager, and the slave power managers 264 and 274.

The MPM 280 is any circuitry configured to control the "global" power behavior of the entire integrated circuit 250. In some embodiments, there are multiple MPMs 280 that control the power behavior of the entire integrated circuit 250. In some embodiments, the MPM 280 communicates with existing IPMs and SPMs 264 and 274 to control power within the power islands 260 and 270. The MPM 280 may receive status information about the power islands 260 and 270 from the SPMs 264 and 274 and the IPMs. The MPM 280 may also determine power trade-offs between the IPMs and the SPMs 264 and 274.

The MPM 280 may also provide a main interface to the PMCL 218 firmware. In some embodiments, the MPM 280 communicates with the PMCL 218 to accept commands (e.g. memory mapped commands) and provide status information about the power within the integrated circuit 250. In some embodiments, the MPM 280 communicates with the PMCL 218 through the main bus for the integrated circuit 250. The MPM 280 may also register each of the SPMs 264 and 274 and IPMs and capabilities with the PMCL 218. Some operations of the MPM 280 are described in further detail

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below in FIGS. 5, 8, 9, and 11. In some embodiments, the MPM 280 reads and writes scan chains for state save and restore along with the local logic analyzer ability.

Some embodiments may include an IPM (not shown) that coordinates SPMs 264 and 274 on behalf of the MPM 280. In some embodiments, the IPM controls and coordinates power behavior on portions of the area controlled by the MPM 280. In some embodiments, the IPM controls the SPMs 264 and 274 that are on a separate chip from the MPM 280.

The SPM 264 is any circuitry configured to control power within a power island 264 in the integrated circuit 250. One example of the SPM 264 is an IP block that controls power within a power island 264 in the integrated circuit 250. The SPM 264 may include signal buffering, level shifting, and signal isolation. In some embodiments, the SPM 264 is integrated into scan chains to provide easier implementation and integration. Also, in some embodiments, the SPM 264 has a very small "footprint" with a low gate count and low power. In some embodiments, the SPM 264 comprises a command interface to communicate status information, service requests, and commands. Some of the commands are load, sleep, and idle. The SPM 264 may also recognize its own address to allow for multi-drop bussing.

In some embodiments, the SPM 264 has registration capabilities. For registration at power-up, the SPM 264 uses callback registration that is typically used for off chip SPMs and IPMs. For static registration when the integrated circuit is generated for on chip SPMs, the SPM 264 registers what the SPM 264 can do, what the IPM can do, and the type of commands that the SPM 264 or IPM can service. The SPM 264 may also have save and restore functions for power off periods. The SPM 264 may have watch-dog timer(s). In some embodiments, the SPM 264 has a debug interface coordination to the power island 260. The SPM 264 may also monitor local state and collect information for components within the power island 260. The SPM 264 may also locally control Vdd, clocks for frequency selection, and dynamic back biasing. The description for the SPM 264 also applies to the SPM 274 for the power island 270.

In some embodiments, the SPM 264 checks whether an event occurs when the collected information from the power island 260 crosses a threshold or exceeds a range. In some embodiments, the SPM 264, IPMs, or the MPM 280 monitors power consumption levels of the power island 260 to check whether the power consumption levels cross a threshold level or exceed a range. A power consumption level is any information, data, or statistic that indicate the power consumed in a power island 260. Some examples of power consumption levels are temperature and power. The threshold or range may be programmable. The SPM 264 may report the event asynchronously, or another element such as the MPM 280 may solicit whether an event has occurred. The event may also be a multi-level test such as the conditions occur at a greater than a given, programmable frequency or exceed a given, programmable duration.

In some embodiments, the low power standard cell logic block 262 one example of a standard cell library that may be included in the power island 260. In some embodiments, the standard cell library is optimized for lower power. The standard cell library may be characterized over a range of operating voltages. In some embodiments, the standard cell library includes synchronous circuits and/or asynchronous circuits. In some embodiments, the standard cell library includes static circuits and/or encapsulated, dynamic logic circuits. The standard cell library may also include multiple voltage domain interface circuits such as level shifters and

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signal isolation circuits. The standard cell library may also have a multi-threshold design and characterization such as standard V_t , high V_t , low V_t , and variable V_t circuits. The standard cell library may also include data retention (shadow) circuits and anti-glitch circuits. The standard cell library may also include low leakage “sleep” circuits. FIG. 3 depicts an illustration of low leakage circuitry 300 for the low power standard cell logic block 262 in an exemplary implementation of the invention.

FIG. 4 depicts a diagram of the power island 270 in an exemplary implementation of the invention. The power island 270 includes a low power memory block 272 and the SPM 274. The low power memory block 272 includes banked architectures 410, 420, 430, and 440 for memories and sleep, power down circuitry 450. In some embodiments, the memory in the power island 270 is RAM and/or ROM. Some examples of the RAM are the SRAM compilers such as single-port, 2-port, and dual-port. Some examples of the ROM are ROM compilers. Some memories in the power island 270 are optimized for low power such as the low power memory block 272. In one embodiment, the low power memory block 272 includes multiple bank architectures via the compiler such as banked architectures 410, 420, 430, and 440. The memories in the power island 270 may also include sleep, power down circuitry 450 for low power modes such as sleep, nap, and full power down. The memories in the power island 270 may also include programmable read/write ports. The memories in the power island 270 may also be an asynchronous and/or synchronous design.

In some embodiments, the system 200 also includes a smart power unit (SPU) 290. In some embodiments, the SPU 290 is off-chip to the integrated circuit 250. The SPU 290 is an external unit configured to control power and clock distribution to the integrated circuit. The circuitry of the SPU is described in further detail below in FIGS. 7 and 8.

FIG. 5 depicts a flowchart from an application request to an SPM action in an exemplary implementation of the invention. FIG. 5 begins in step 500. In step 502, an application is invoked such as playing a movie. In step 504, the application determines the required frequency for performance of an IP unit. For example, the application determines a specified frequency in MHz for IP unit for an MPEG decoder. In some embodiments, when the IP unit is totally asynchronous, the required frequency will be an artificial measure of performance. In some embodiments that have multiple clocks involved, the minimum performance for each clock is specified.

In step 506, the application invokes the PMCL 218 API call. One example of this call is “Set_Rate (unit Y, N MHz, degree of dynamic power management (DPM) allowed, DPM threshold, other information to allow DPM trade-offs, starting back bias for SPMs with dynamic bias, wait for power up flag).” In this example, the other information could be “no power off, use high V_t and clocks off instead” and “major waits are about 10 us, with a 400 ns threshold.” In some embodiments with multiple clocks, the PMCL 218 API call allows the application to specify all required frequencies.

The PMCL 218 determines possible trade-offs available for the unit and selects a frequency rate, V_{dd} , and V_t if applicable for the unit that best meets the given requirements in step 508 and determines the applicable SPMs 264 and 274 in step 510. In some embodiments, the MPM 280 or IPM performs steps 508 and 510. In some embodiments for

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multiple clocks, the V_{dd} and V_t specified would allow for all specified clocks to meet or exceed their required frequencies.

In step 512, the PMCL 218 then writes the desired setting for the SPMs 264 and 274 to the MPM 280 (or IPM). In step 514, the MPM 280 (or IPM) converts the request into one or more commands for the SPMs 264 and 274 (or IPM) associated with the unit.

In step 516, if the application sets the wait for power up flag, the PMCL 218 then waits until the IP unit is fully powered up before returning from the call. Otherwise, the call returns as soon as the command is acknowledged, with status of 0 for okay, 1 for fast power-up, 2 for slow power-up, or 3+ for error conditions. The powered up state is when the unit is at the desired V_{dd} for the requested frequency, and not just that the unit is turned on.

In step 518, the MPM 280 (or IPM) sends the requests to the appropriate targets. In step 520, the MPM 280 waits for the receipt of the acknowledgements that indicate message received and executed or execution has begun. A NACK or negative acknowledgement may also be returned from the SPM 264 and 274.

In step 522, the SPM 264 receives the commands and performs the actions. Steps 524–528 are possible actions that the SPM 264 may perform. In step 524, the SPM 264 switches the V_{dd} mux. In step 526, the SPM 264 switches a clock mux. In some embodiments when the voltage goes down, step 526 is performed before step 524. In step 528, the SPM 264 changes the V_t on the associated transistors. After the SPM 264 performs the actions, the SPM 264 returns a status message upstream indicating acknowledgement or negative acknowledgement in step 530. FIG. 5 ends in step 532.

FIG. 6 depicts an illustration of internal circuitry 600 for an SPU 290 in an exemplary implementation of the invention. In this embodiment, the internal circuitry 600 for the SPU 290 is internal to the integrated circuit 250 of FIG. 2. The internal circuitry 600 includes an external voltage 610, a dropout voltage regulator 620, a dropout voltage regulator 630, a logic block 640, and a logic block 650.

FIG. 7 depicts an illustration of external circuitry 700 for an SPU 290 in an exemplary implementation of the invention. In this embodiment, the external circuitry 700 for the SPU 290 is external to the integrated circuit 250 of FIG. 2. The internal circuitry 700 includes an external voltage 710, a power supply pin 720, a power supply pin 730, a power supply pin 740, a logic block 750, a logic block 760, and a logic block 770. The external circuitry 700 for the SPU 290 provides a DC/DC conversion. The DC/DC conversion provides multiple independent power supply pins 720, 730, and 740. The power supply pins 720, 730, and 740 have a variable voltage supply on each separate power pin. Also, in some embodiments, the variable voltage is within a range and in steps. In some embodiments, the PMCL 218 controls the voltage to power supply pins 720, 730, and 740.

FIG. 8 depicts a flowchart from an application request to an SPU action in an exemplary implementation of the invention. FIG. 8 begins in step 800. In step 802, an application is invoked. In step 804, the application determines the required frequency for performance of an IP unit. For example, the application determines a specified frequency in MHz for IP unit for an MPEG decoder.

In step 806, the application invokes the PMCL 218 API call. One example of this call is “Set_Rate (unit Y, N MHz, degree of dynamic power management (DPM) allowed, DPM threshold, other information to allow DPM trade-offs, starting back bias for SPMs with dynamic bias, wait for

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power up flag).” In this example, the other information could be “no power off, use high Vt and clocks off instead” and “major waits are about 10 us, with a 400 ns threshold.”

The PMCL 218 determines possible trade-offs available for the unit and selects a the lowest possible Vdd that will support the requested frequency in step 808 and determines the SPMs 264 and 274 that will be affected and which power PINs to change in step 810.

In step 812, the PMCL 218 sends a command to the MPM 280 to have the SPMs 264 and 274 (and IPM) to prepare for a Vdd change. In step 814, the PMCL 218 waits for the acknowledgement from the MPM 280. In step 816, the PMCL 218 sends a command to the SPU 290 to change the Vdd on the selected power pins and waits for the affected area to “settle down.” In step 818, the PMCL 218 then sends a “resume operation at a specified frequency” command to the MPM 280. In step 820, the MPM 280 propagates the resume command to all affected SPMs 264 and 274 (and IPMs). In step 822, one of the power managers (i.e. MPM 280, IPM, or SPMs 264 and 274) sets the specified frequency. In step 824, the IP unit operation resumes after the clock has settled. FIG. 8 ends in step 826. In some embodiments, the user application has the option of waiting for the entire operation to finish or to continue and either query the PMCL 218 as to the progress of the operation or wait for a “finished” interrupt from the PMCL 218.

FIG. 9 depicts a flowchart for saving an IP unit’s state prior to powering down and restoring the IP unit’s state when powering up in an exemplary implementation of the invention. FIG. 9 begins in step 900. In step 902, the user application requests that the PMCL 218 power off an IP unit and wants to save the IP unit’s state. In some embodiments, the reconfiguration of the IP unit takes a long time. The request in step 902 may be accompanied by the address of an area to which the state should be saved.

In step 904, the PMCL 218 sends a “stop clock and read IP unit state” message to the MPM 280. The MPM 280 then propagates the “stop clock and read IP unit state” message to the SPMs 264 and 274 of the affected unit in step 906. In step 908, the MPM 280 uses the scan chain for the IP unit to read the state into a register or buffer for presentation to the PMCL 218. In step 910, if the PMCL 218 provided the MPM 280 with the address of the save area, the MPM 280 saves the state information directly in the specified area. In step 912, after all of the IP units’ state has been saved, the PMCL 218 sends a “power off IP unit” message to the MPM 280. In step 914, the MPM 280 then propagates out the “power off IP unit” message. In step 916, the PMCL 218 returns the save state area to the user application. The save state area contains the state of the unit.

At a later time, in step 918, the user application requests that the PMCL 218 power the IP unit back up and restore the state of the IP unit. In some embodiments, the user application request includes the address of the area to which the state was saved. In step 920, the PMCL 218 sends a “power up IP unit with clocks off and restore state” message to the MPM 280. In step 922, the MPM 280 propagates the “power up IP unit with clocks off and restore state” message to the SPMs 264 and 274 of the affected IP unit. In step 924, after the IP unit is powered up, the MPM 280 uses the scan chain to reload the unit’s state. In some embodiments, the reloading of the unit’s state originates directly from the save area or from information passed to the MPM 280 from the PMCL 218. In step 926, the PMCL 218 sends a message to the MPM 280 to turn clock back on and report to user application that the IP unit is ready to continue operations. FIG. 9 ends in step 928.

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In some embodiments, the same functionality of FIG. 9 can be used to implement an internal “logic analyzer” function, in which the IP unit in question would not be powered down after being read. If the associated SPMs 264 and 274 of the IP unit have the ability to single- or multi-step the clock, the local scan testing is performed by having the SPMs 264 and 274 “signal isolate” the IP unit. Then, use of a combination of the ability of single- or multi-step the clock and the ability to use the scan chain can read/write the IP unit’s internal state.

FIG. 10 depicts a diagram of a system-on-a-chip (SOC) 1000 and an extended local memory 1004 in an exemplary implementation of the invention. The SOC 1000 is one example of the integrated circuit 250 and communicates with the embedded firmware stack 210 in FIG. 2 as described above. The SOC 1000 includes a CPU 1010, a local memory 1020, a memory controller 1030, a mixed signal circuitry 1040, an application specific circuitry 1050, a PCI-X circuitry 1060, a MPM 1070, a real-time clock (RTC) 1075, an Ethernet circuitry 1080, and a USB circuitry 1090. The CPU 1010, the local memory 1020, the memory controller 1030, the mixed signal circuitry 1040, the application specific circuitry 1050, the PCI-X circuitry 1060, the Ethernet circuitry 1080, and the USB circuitry 1090 are all power islands in which power is controlled within the power islands by power managers. In this embodiment, the power islands are delineated by the functionality of a part of the SOC 1000.

The extended local memory 1004 includes an IPM 1006 that is coupled to the bus 1071. The CPU 1010 includes an SPM 1015 that is coupled to the bus 1071. The local memory 1020 includes an SPM 1025 that is also coupled to the bus 1071. The memory controller 1030 comprises an SPM 1035 that is coupled to the bus 1071. The mixed signal circuitry 1040 includes an SPM 1045 that is coupled to the bus 1071. The application specific circuitry 1050 includes an IPM 1055 and an SPM 1058 that are both coupled to the bus 1072. The PCI-X circuitry 1060 includes an SPM 1065 that is coupled to the bus 1072. The MPM 1070 is coupled to the bus 1071 and the bus 1072. The MPM 1070 is one example of the MPM 280 as described above. The Ethernet circuitry 1080 includes an SPM 1085 that is coupled to the bus 1072. The USB circuitry 1090 includes an SPM 1095 that is coupled to the bus 1072.

In this embodiment, power command buses comprise the bus 1071 and the bus 1072. The bus 1071 and 1072 are simple multi-drop serial buses that may cross chip boundaries and interconnect power managers. The power command bus may be a combination of serial busses, such as the bus 1071 and the bus 1072, with one per region of the chip and then multi-drop within the region. In other embodiments, the power command bus includes a parallel bus or a combination of serial and parallel busses. In some embodiments, the power command bus is the system bus. The power command bus may contain messages with at least a unit ID with the associated payload. For a fixed point to point bus, the message does not need a unit ID only the payload.

In some embodiments, the power command bus uses an error detection scheme such as parity, ECC, or a redundant code. In some embodiments, the power command bus is a low performance bus that does not interfere with the integrated circuit design and is not visible to the user. In some embodiments, the communication between the PMCL 218 and the MPM 1070 is memory mapped and based on the main bus such as an AHB for an SOC 1000.

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Some embodiments may include a separate bus for reporting status information between the power managers. In one example, this separate bus provides asynchronous “Alert” type status messages from SPMs to the MPM.

There can be various message formats for the power command bus. In one example for a basic format, the message format includes a start of message indicator, a power manager address, type code, basic command, and an end of message indicator. In one example for an extended format, the message format includes the basic format, an additional length, and additional information. In one example for a response message format, the message format includes a start of message reply indicator, a power manager address, a 3b ACK or NAK or return status (implied ACK), a payload length for return status messages, a payload for return status messages, a reason code for NAK, and an end of message indicator.

In some embodiments, the SPM 1015 or the IPM 1006 times out on replying to a command, and the MPM 1070 reissues the command a programmable number of times. If the SPM 1015 or the IPM 1006 still fails, the MPM 1070 marks the SPM 1015 or the IPM 1006 as unusable and reports back the failure to the PMCL 218. In one embodiment, the PMCL 218 has the MPM 1070 reinitialize the failing SPM 1015 or the IPM 1006 via the scan system and then retries sending the message. Other conditions such as invalid responses to commands or invalid status reports are also handled by the re-initialization. In some embodiments, the state of the failing SPM 1015 or the IPM 1006 may be read out and saved for later analysis.

FIG. 11 depicts a flowchart for generating a “hot spot” report from an IPM 1055 to the PMCL 218 in an exemplary implementation of the invention. FIG. 11 begins in step 1100. In step 1102, the IPM 1055 monitors the temperature statistics of the SPMs. In step 1104, the IPM 1055 checks whether the mean temperature has exceeded a predetermined and programmed threshold. If the mean temperature has not exceeded the threshold, the IPM 1055 returns to step 1102 to keep monitoring. If the mean temperature has exceeded the threshold, the IPM 1055 then generates a problem (“hot spot”) report message in step 1106. In step 1108, the IPM 1055 waits for the next status query the MPM 1070. In some embodiments, a logically separate bus is provided for asynchronous status reports to the MPM 280.

In step 1110, the MPM 1070 receives the hot spot report message. In step 1112, the MPM 1070 either waits for further confirmation (i.e. see that the “hot spot” last pasts a predetermined threshold) or immediately takes action to fix the problem depending on the internal logic of the MPM 1070. In some embodiments, in step 1114, the MPM 1070 takes action by posting an interrupt to the PMCL 280 that it needs attention. In other embodiments, if the PMCL 280 queries the MPM 1070 often enough, then the interrupt is not needed. In step 1116, the MPM 1070 (or IPM) fixes the problem by making a local trade-off, performing the action, or ordering the action to be performed. One example of fixing the problem is lowering the operating frequency of the hot spot area. In step 1118, the MPM 1070 reports both the problem and the fixing of the problem upstream.

In step 1120, the PMCL 218 reads the modified hot spot report from the MPM 1070. In step 1122, the PMCL 218 determines what action to take to fix the problem or notify the GPAL 214 of the problem. In step 1124, the PMCL 218 issues the appropriate commands to the MPM 1070 to fix the problem. In this step, the software will make the trade-off required to fix the problem. In some embodiments, if the GPAL 214 determines the high level fix, then the GPAL 214

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sends it to the PMCL 280 to be converted into MPM commands. In step 1126, the PMCL 218 monitors the problem area for a specified time to check if the problem is fixed. FIG. 11 ends in step 1128.

In some embodiments, the type of functionality in FIG. 11 can be performed at other levels such as the PMCL 218. In one example, the PMCL 218 queries (via the MPM 1070) all the SPMs that have the desired measurement ability (and IPMs) as to their local conditions and can then, for example, build a “map” of power usage that it can then act on.

FIG. 12 depicts a diagram of a system-on-a-chip (SOC) 1200 in another exemplary implementation of the invention. The SOC 1200 is attached to a sensor link 1212, an RF link 1214, a control link 1216, a video link 1294, an audio link 1295, an interface link 1296, a control link 1297, and a power link 1298. The SOC 1200 includes clock and distribution management 1210, an IP block power island 1220, a memory power island 1230, a microprocessor power island 1240, an IP block power island 1250, a distribution power island 1260, an IP block power island 1270, an IP block power island 1280, and power and distribution management 1290.

The IP block power island 1220 includes a product standard interface IP block including an analog-to-digital converter (ADC) 1222, which includes an SPM 1224. The IP block power island 1230 includes a memory 1232, which includes an SPM 1234. The microprocessor power island 1240 includes a microprocessor 1242, which includes an SPM 1244. The IP block power island 1250 includes a product standard interface IP block including ADC 1252, which includes an SPM 1254. The distribution power island 1260 includes a data and signal distribution 1262, which includes an SPM 1264. The IP block power island 1270 includes a general purpose IP block including a digital signal processor (DSP) 1272, which includes an SPM 1274. The IP block power island 1280 includes a product-specific IP block 1282, which includes an SPM 1284. The power and distribution management 1290 includes an MPM 1292.

FIG. 13 depicts a flowchart for building a chip with power islands in an exemplary implementation of the invention. FIG. 13 begins in step 1300. In step 1302, the IPs or library cells are selected, and the custom logic, if any, is specified to be used to build the chip. In some embodiments, the maximum and sub clock rate, % idle time, and minimum and maximum Vdd are specified. In step 1304, the register transfer level (RTL) is written. In step 1306, the RTL is simulated and debugged.

Either during or after the writing of the RTL, a software tool may be used to add annotations for the MPM, IPM, and/or SPM blocks in step 1308. In some embodiments, the desired functionality options are specified in the annotations. In some embodiments, the optional functionality is specified per SPM block. In some embodiments, the RTL is annotated with SPM configuration information on a per-module basis. In some embodiments, the proper annotation is inserted by hand on a per module basis during or after the RTL is written. In other embodiments, a separate table in the proper format is created with the module names and respective annotations. In some embodiments, a separate software tool provides the ability to interactively build the separate table. In some embodiments, the software tool adds the proper annotation to the un-annotated modules in the RTL using information from the table.

In step 1310, the synthesis is run on a power island basis, where power islands are not mixed. In step 1312, performance measurement software is run on each module for each Vdd and Vt option, and then the annotations for the

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MPM are added to the RTL. In some embodiments, the performance of the design is measured at all desired voltages and Vt combinations. The software tool then derives the actual frequency, Vdd, and Vt tables for each SPM and back annotates the MPM (or IPM) RTL of the SPM characteristics.

In step 1314, the final synthesis is run on a power island basis. In some embodiments, the modules are separately routed or by SPM. In step 1316, the software tool is run to hook up power and clocks to each SPM. Step 1318 is the rest of the steps to tape-out. In some embodiments, the software tool generates the finished net-list with all information. FIG. 13 ends in step 1320.

The above-described elements can be comprised of instructions that are stored on storage media. The instructions can be retrieved and executed by a processor. Some examples of instructions are software, program code, and firmware. Some examples of storage media are memory devices, tape, disks, integrated circuits, and servers. The instructions are operational when executed by the processor to direct the processor to operate in accord with the invention. Those skilled in the art are familiar with instructions, processor, and storage media.

The above description is illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

What is claimed is:

1. A method of managing power on an integrated circuit including a plurality of power islands, the method comprising:

determining a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands;

determining at least one of actions to change a power consumption level of the one of the power islands to the target power level; and

performing the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.

2. The method of claim 1 wherein the power islands are delineated based on geographic factors of the integrated circuit.

3. The method of claim 1 wherein the power islands are delineated based on functional circuitry of the integrated circuit.

4. The method of claim 1 wherein the power islands comprise power sub-islands.

5. The method of claim 1 wherein the power islands comprise multiple clock domains.

6. The method of claim 1 wherein another one of the actions comprises selecting a clock for the one of the power islands.

7. The method of claim 1 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.

8. The method of claim 7 wherein the first voltage comprises a source voltage.

9. The method of claim 7 wherein the first voltage comprises a threshold voltage.

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10. The method of claim 1 wherein another one of the actions comprises powering on the one of the power islands.

11. The method of claim 1 wherein another one of the actions comprises powering off the one of the power islands.

12. The method of claim 1 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.

13. The method of claim 1 further comprising:

monitoring the power consumption level of the one of the power islands;

determining whether a threshold level was crossed based on the power consumption level; and

performing another one of the based on the crossing of the threshold level.

14. The method of claim 1 further comprising saving a state of components within the one of the power islands.

15. The method of claim 1 further comprising restoring a state of components within the one of the power islands.

16. A system for an integrated circuit comprising a plurality of power islands where power consumption is independently controlled within each of the power islands, the system comprising:

power control circuitry configured to control power for one of the power islands; and

a power manager configured to determine a target power level for the one of the power islands based on needs and operation of the integrated circuit, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands.

17. The system of claim 16 wherein the power islands are delineated based on geographic factors of the integrated circuit.

18. The system of claim 16 wherein the power islands are delineated based on functional circuitry of the integrated circuit.

19. The system of claim 16 wherein the power islands comprise power sub-islands.

20. The system of claim 16 wherein the power islands comprise multiple clock domains.

21. The system of claim 16 wherein another one of the actions comprises selecting a clock for the one of the power islands.

22. The system of claim 16 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.

23. The system of claim 22 wherein the first voltage comprises a source voltage.

24. The system of claim 22 wherein the first voltage comprises a threshold voltage.

25. The system of claim 16 wherein another one of the actions comprises powering on the one of the power islands.

26. The system of claim 16 wherein another one of the actions comprises powering off the one of the power islands.

27. The system of claim 16 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.

28. The system of claim 16 wherein the power manager is configured to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the at least one of the actions based on the crossing of the threshold level.

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29. The system of claim 16 wherein the power manager is configured to save a state of components within the one of the power islands.

30. The system of claim 16 wherein the power manager is configured to restore a state of components within the one of the power islands.

31. The system of claim 16 further comprising a bus coupled to the power manager and the power islands.

32. The system of claim 16 wherein the power manager comprises a master manager configured to control power of the integrated circuit.

33. The system of claim 16 wherein the power manager comprises a slave manager configured to control power of the one of the power islands.

34. The system of claim 16 wherein the power control circuitry includes clock multiplexing circuitry.

35. The system of claim 16 wherein the power control circuitry includes voltage multiplexing circuitry.

36. The system of claim 16 wherein the power control circuitry includes level shifting circuitry.

37. A software product for managing power on an integrated circuit including a plurality of power islands, the software product comprising:

power management software operational when executed by a processor to direct the processor to determine a target power level for one of the power islands based on needs and operation of the integrated circuit where power consumption is independently controlled within each of the power islands, determine at least one of actions to change a power consumption level of the one of the power islands to the target power level, and perform the at least one of the actions to change the power consumption level of the one of the power islands to the target power level where one of the actions comprises selecting a frequency for the one of the power islands; and

a software storage medium operational to store the power management software.

38. The software product of claim 37 wherein the power islands are delineated based on geographic factors of the integrated circuit.

39. The software product of claim 37 wherein the power islands are delineated based on functional circuitry of the integrated circuit.

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40. The software product of claim 37 wherein the power islands comprise power sub-islands.

41. The software product of claim 37 wherein the power islands comprise multiple clock domains.

42. The software product of claim 37 wherein another one of the actions comprises selecting a clock for the one of the power islands.

43. The software product of claim 37 wherein another one of the actions comprises modifying a first voltage for the one of the power islands.

44. The software product of claim 43 wherein the first voltage comprises a source voltage.

45. The software product of claim 43 wherein the first voltage comprises a threshold voltage.

46. The software product of claim 37 wherein another one of the actions comprises powering on the one of the power islands.

47. The software product of claim 37 wherein another one of the actions comprises powering off the one of the power islands.

48. The software product of claim 37 wherein another one of the actions comprises changing the one of the power islands to a sleep mode.

49. The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to monitor the power consumption level of the one of the power islands, determine whether a threshold level was crossed based on the power consumption level, and perform the at least one of the actions based on the crossing of the threshold level.

50. The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to save a state of components within the one of the power islands.

51. The software product of claim 37 wherein the power management software is operational when executed by the processor to direct the processor to restore a state of components within the one of the power islands.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

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APPLICATION NO. : 10/840893
DATED : May 23, 2006
INVENTOR(S) : Barry Alan Hoberman et al.

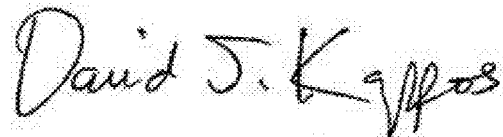
Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 14, Claim 12, line 6, before “comprises” insert --actions--.

In Column 14, Claim 13, line 13, after “one of the” insert --actions--.

Signed and Sealed this
Twenty-first Day of June, 2011

A handwritten signature in black ink that reads "David J. Kappos". The signature is written in a cursive, flowing style.

David J. Kappos
Director of the United States Patent and Trademark Office

EXHIBIT B



US007945885B2

(12) **United States Patent**
Hoberman et al.

(10) **Patent No.:** **US 7,945,885 B2**
(45) **Date of Patent:** ***May 17, 2011**

(54) **POWER MANAGERS FOR AN INTEGRATED CIRCUIT**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 397 days.

This patent is subject to a terminal disclaimer.

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(63) Continuation of application No. 11/336,097, filed on Jan. 20, 2006, now Pat. No. 7,415,680, which is a continuation of application No. 10/840,893, filed on May 7, 2004, now Pat. No. 7,051,306.

(60) Provisional application No. 60/468,742, filed on May 7, 2003.

(51) **Int. Cl.**
G06F 17/50 (2006.01)

(52) **U.S. Cl.** **716/133; 716/100; 716/126; 716/127; 716/132**

(58) **Field of Classification Search** **716/100, 716/126, 127, 132, 133**

See application file for complete search history.

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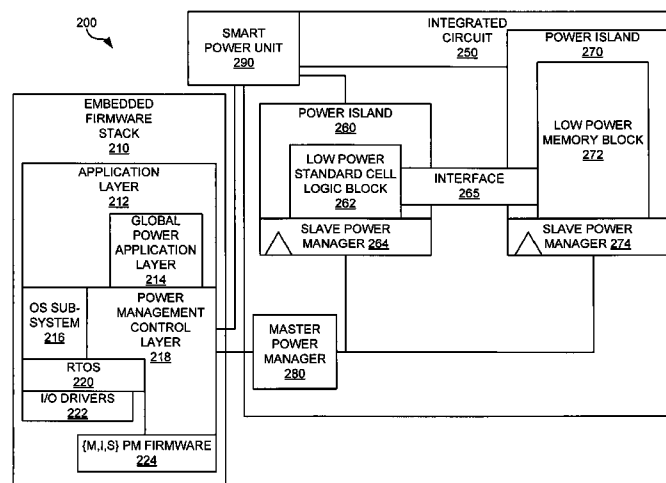
Primary Examiner — Sun J Lin

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(57) **ABSTRACT**

A system for an integrated circuit comprising a plurality of power islands includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

64 Claims, 13 Drawing Sheets



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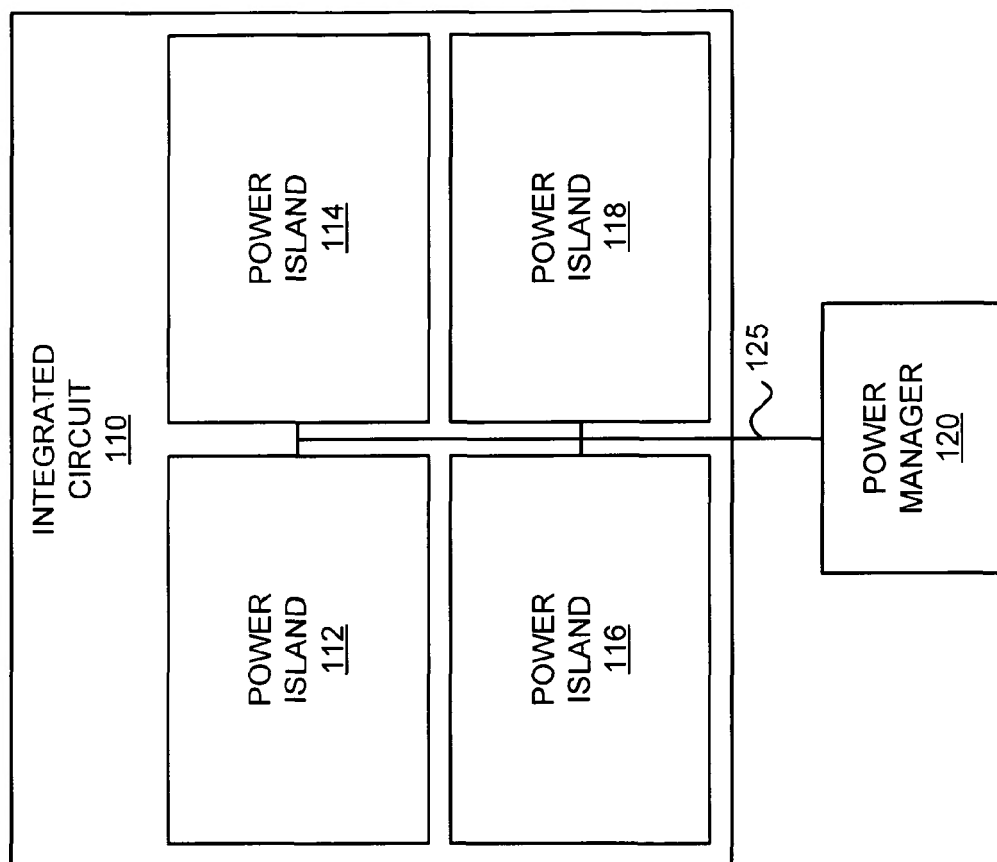


FIG. 1

100 ↗

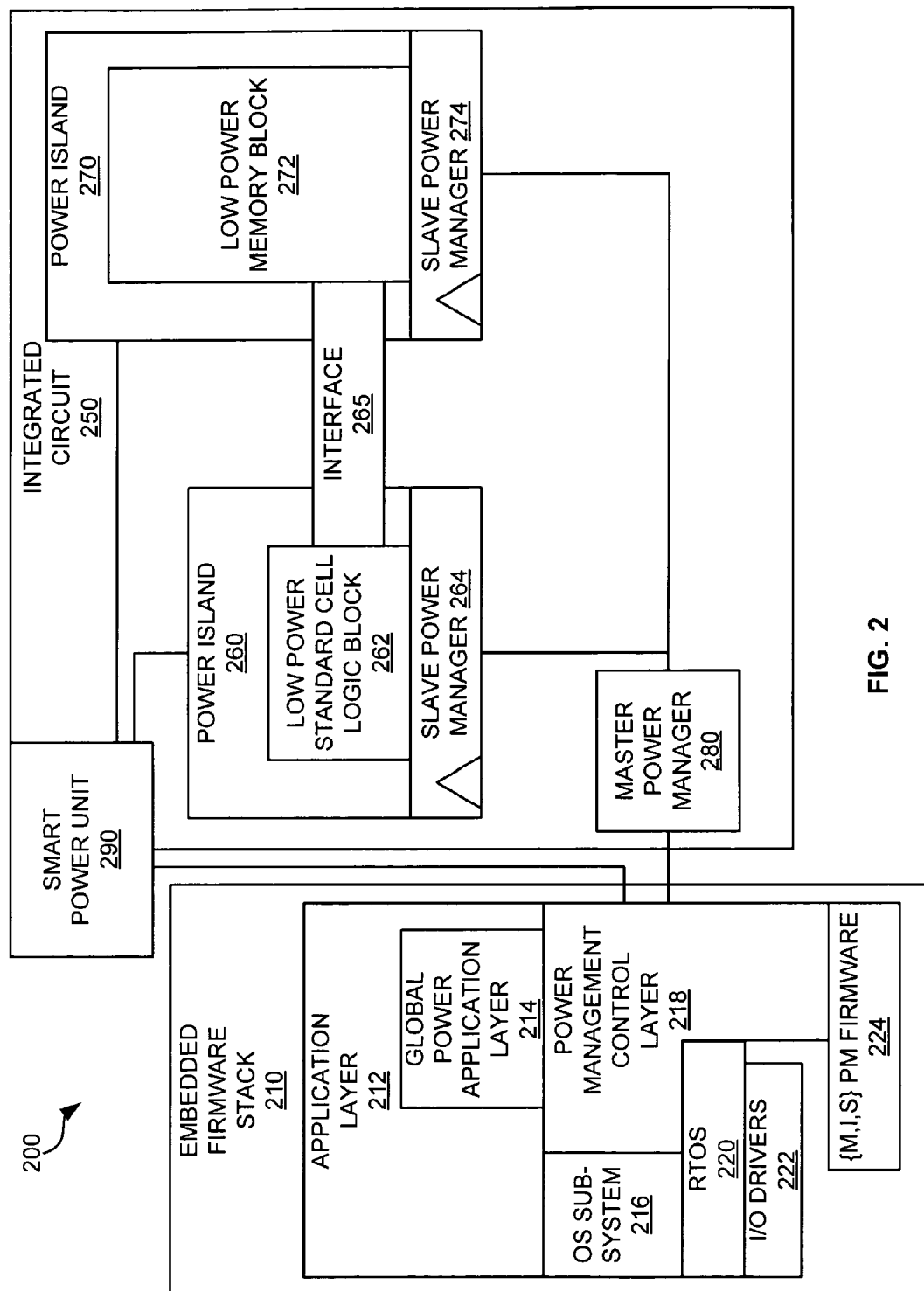


FIG. 2

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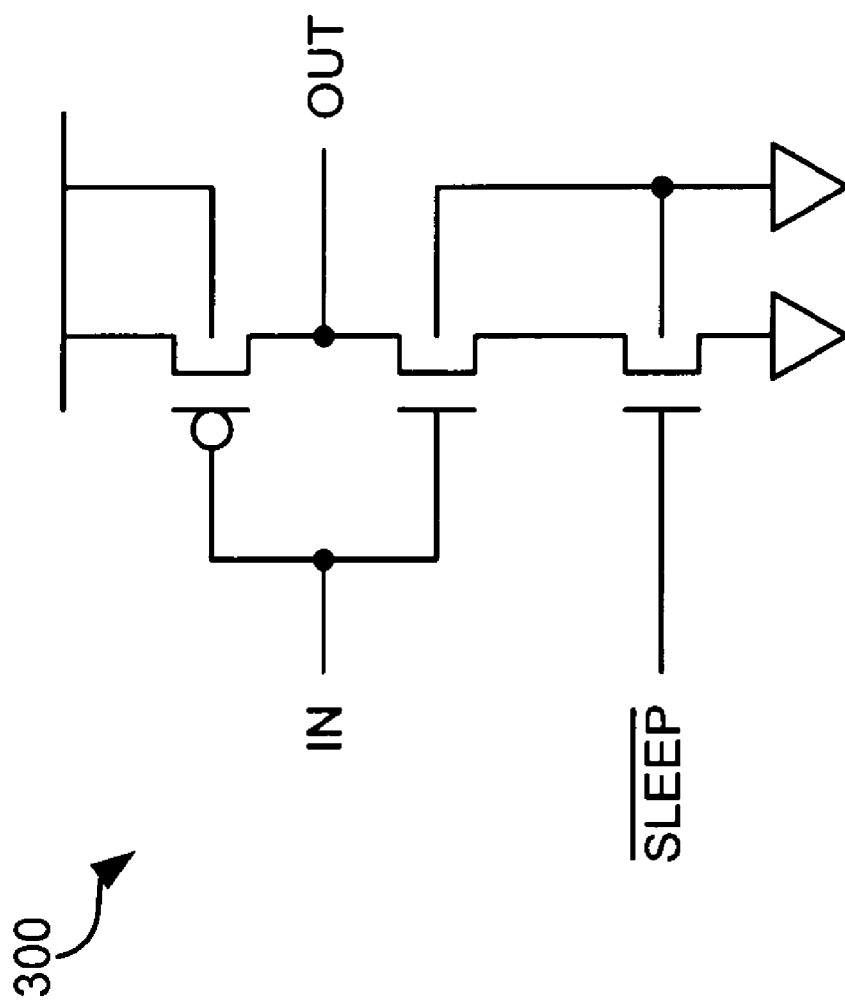


FIG. 3

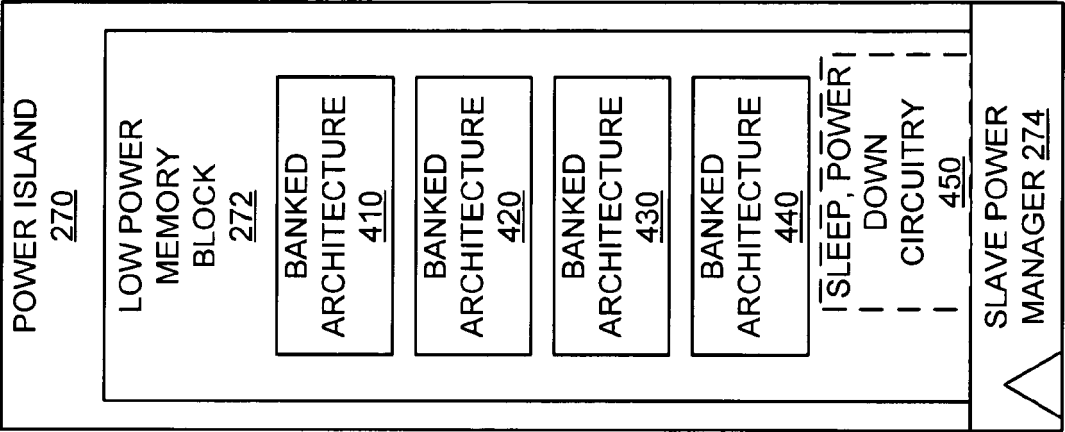


FIG. 4

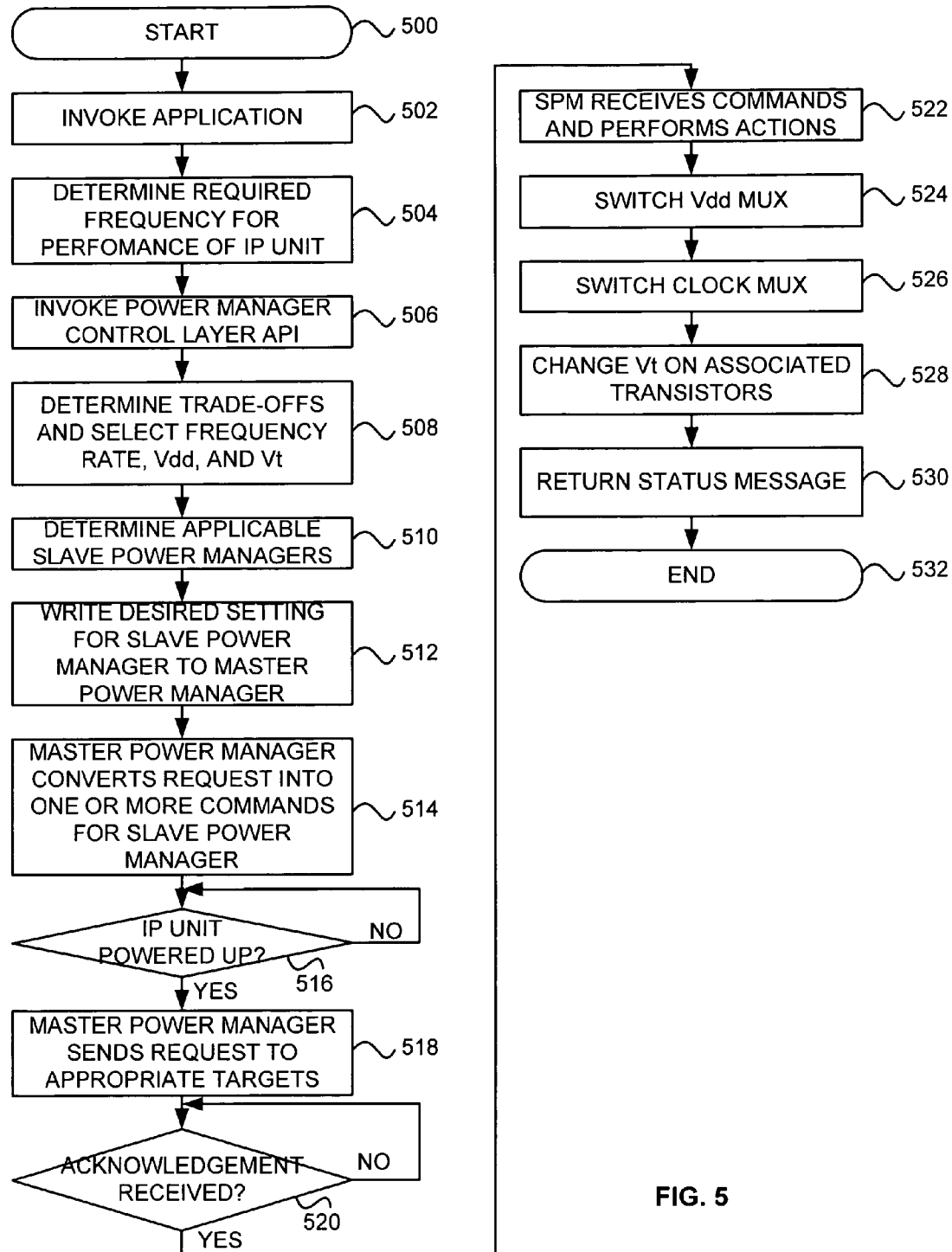


FIG. 5

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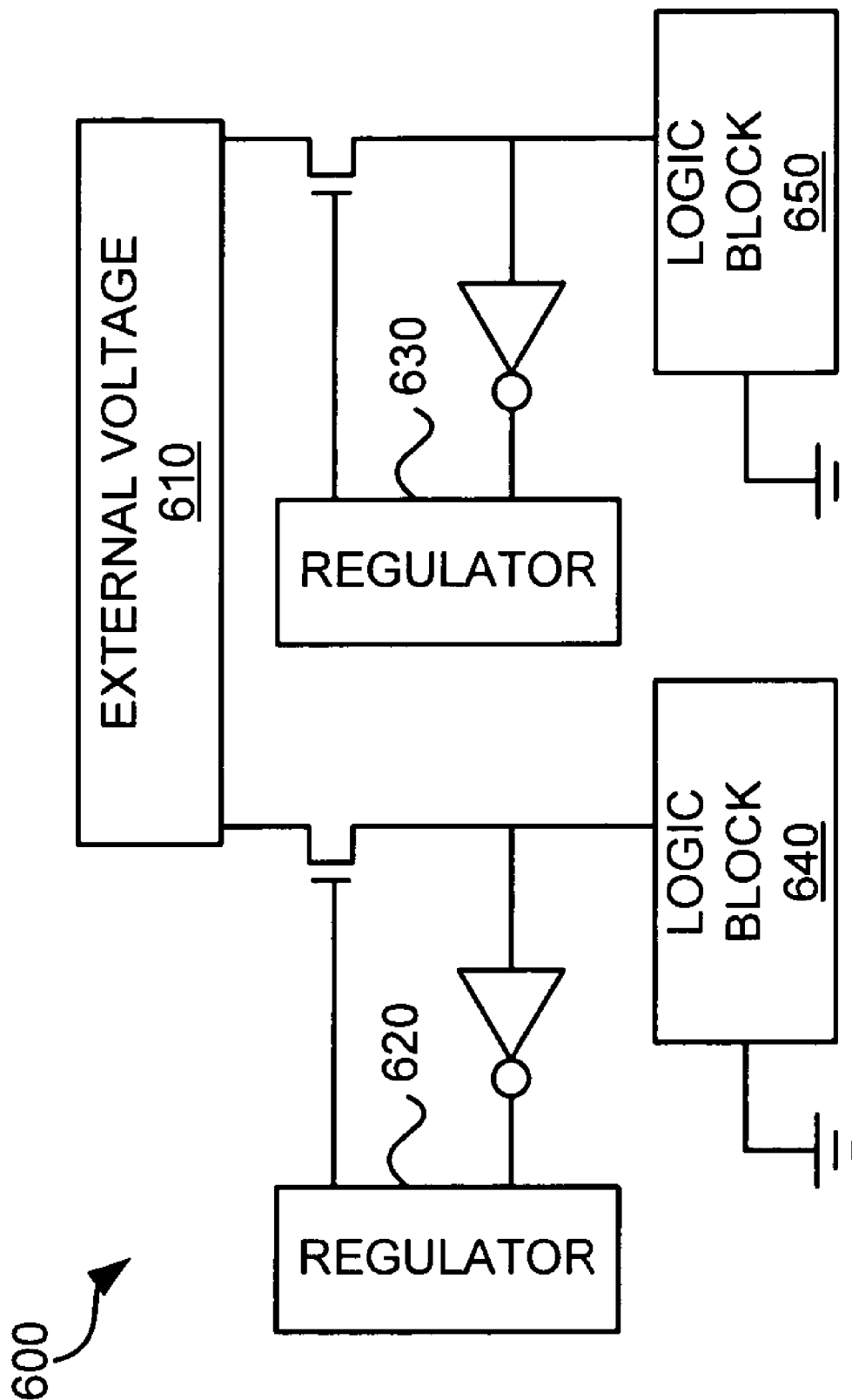


FIG. 6

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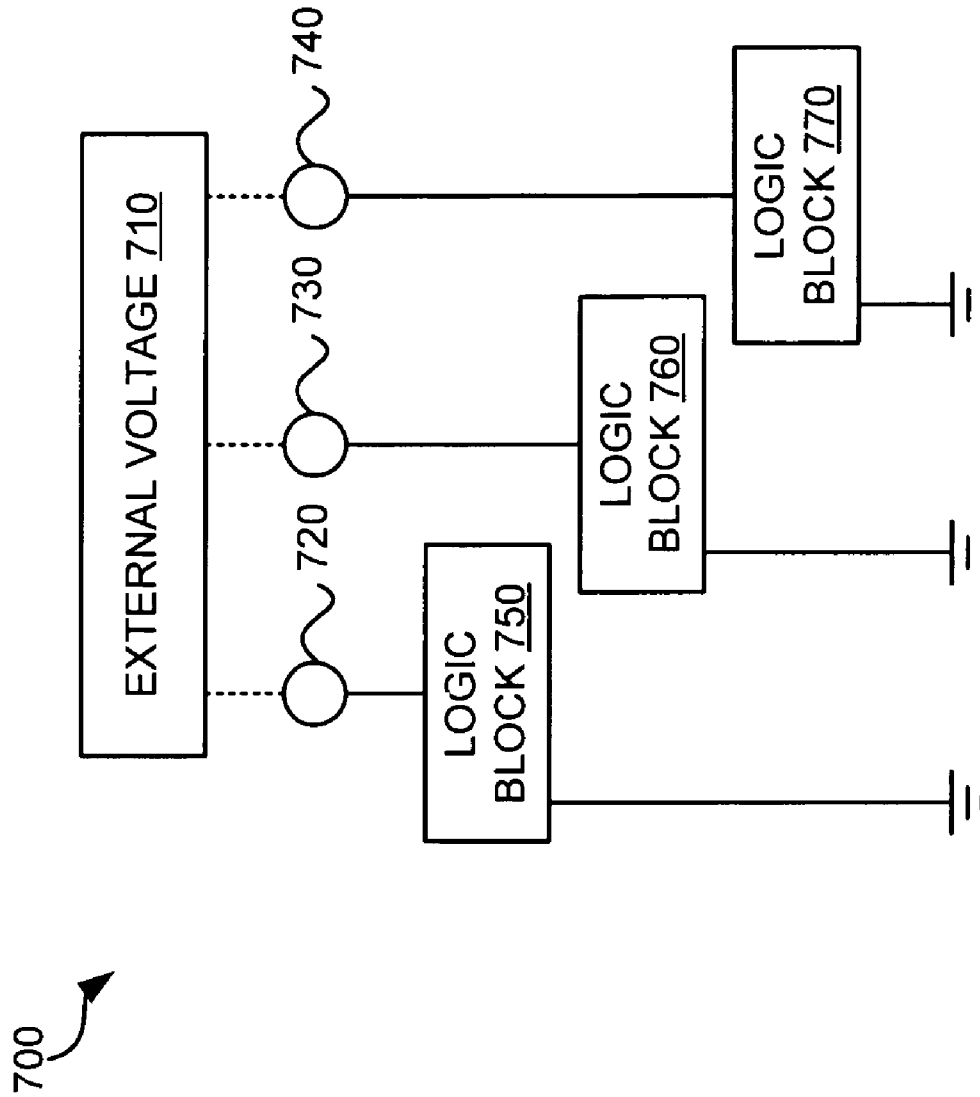


FIG. 7

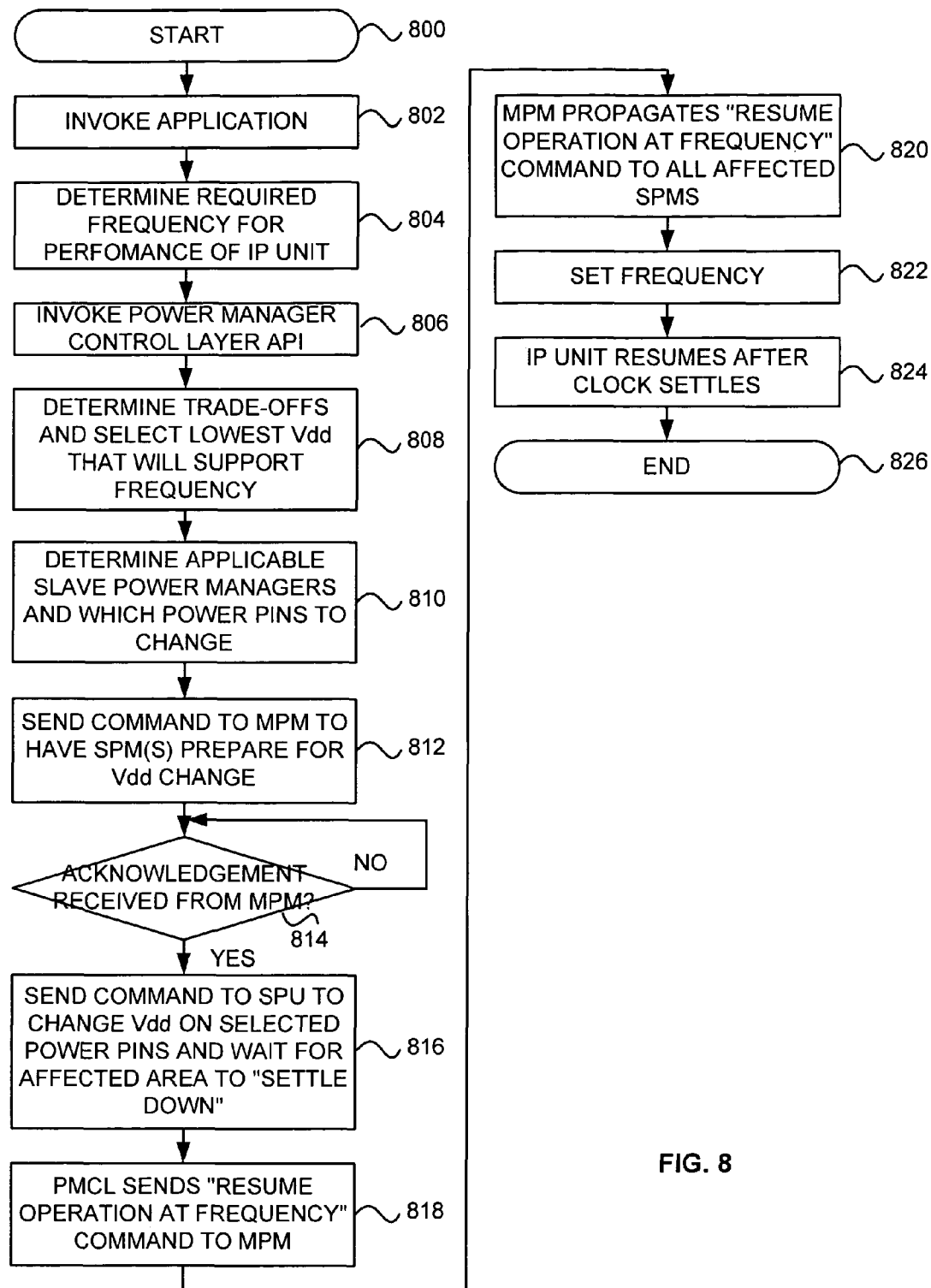


FIG. 8

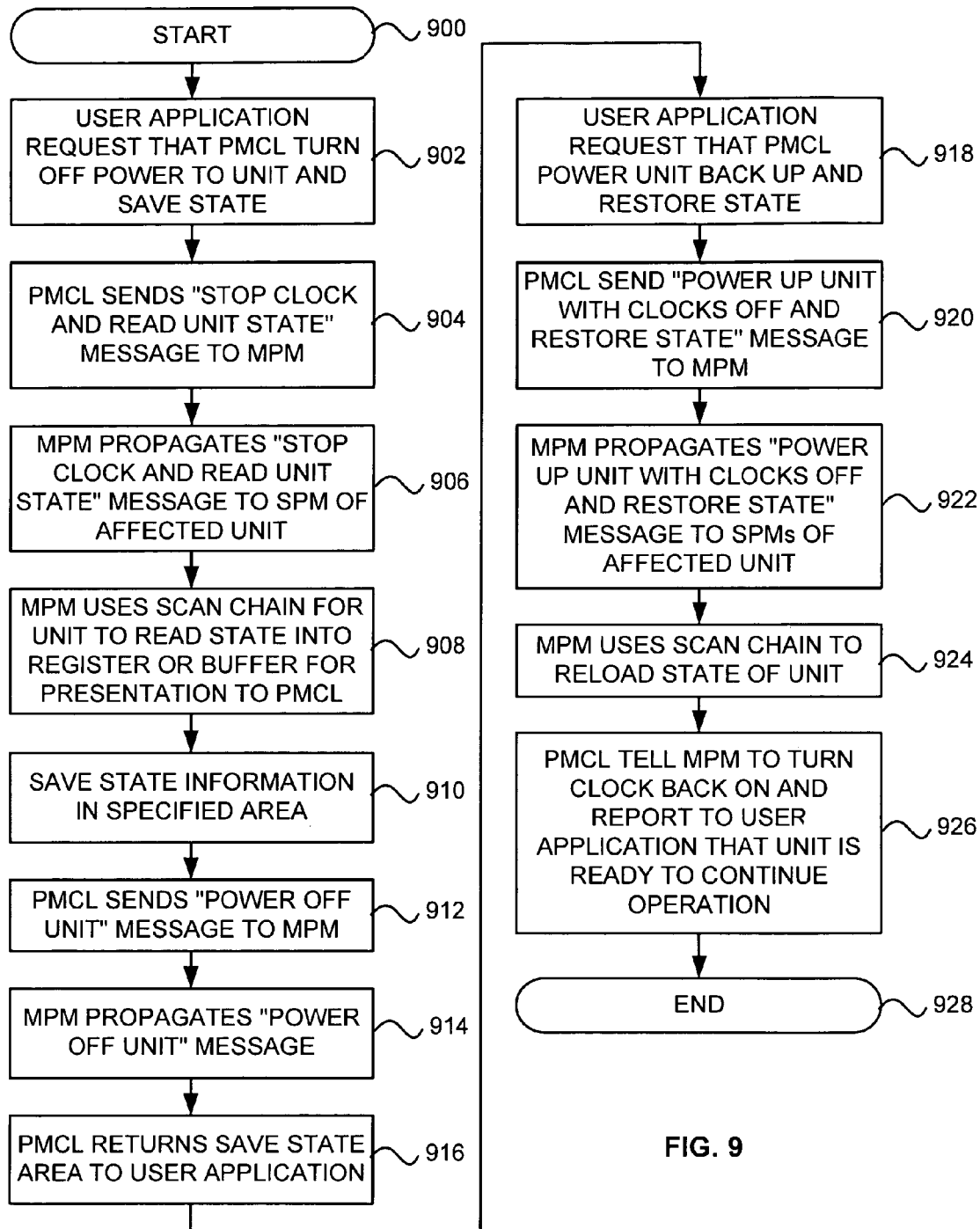


FIG. 9

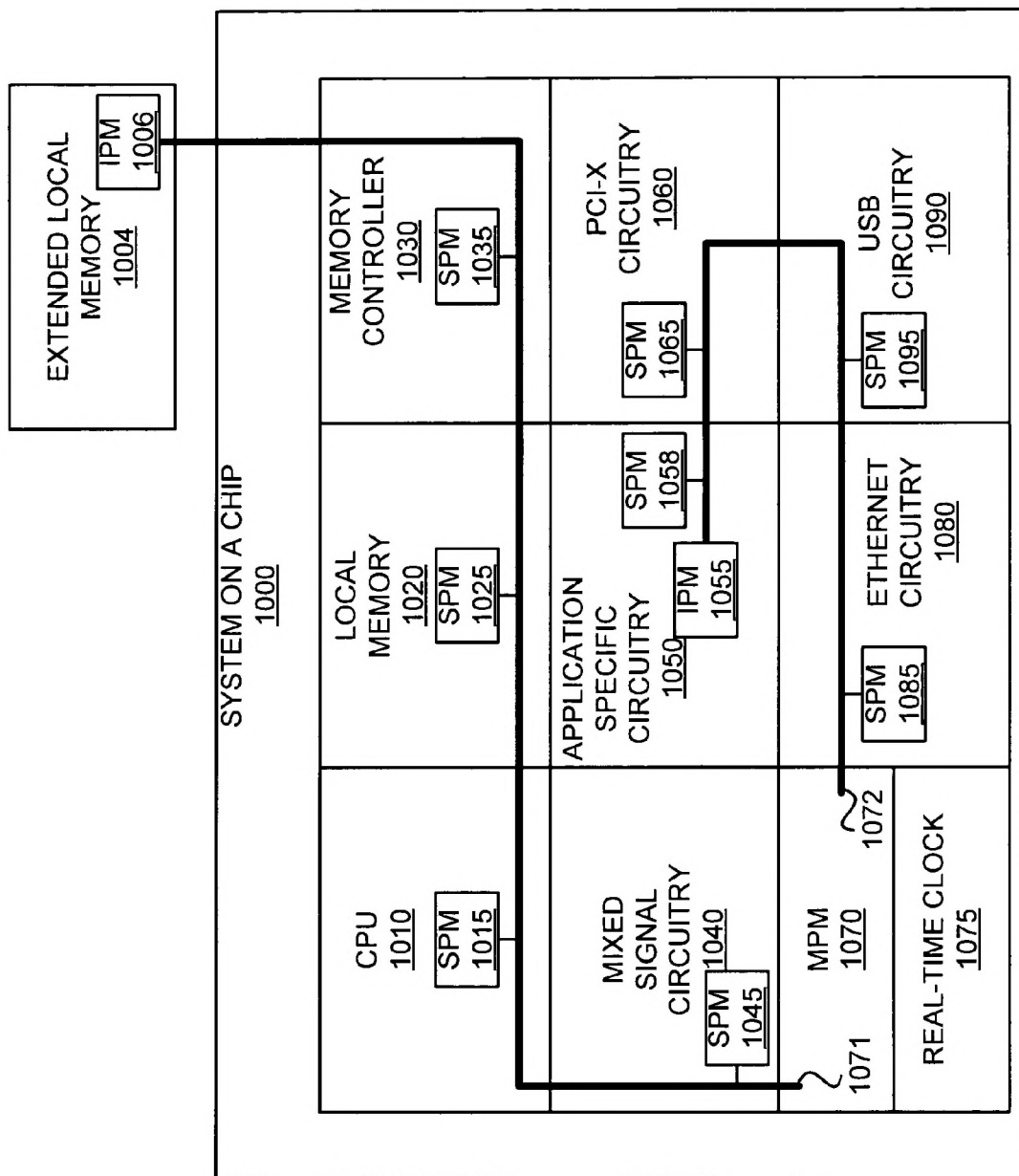


FIG. 10

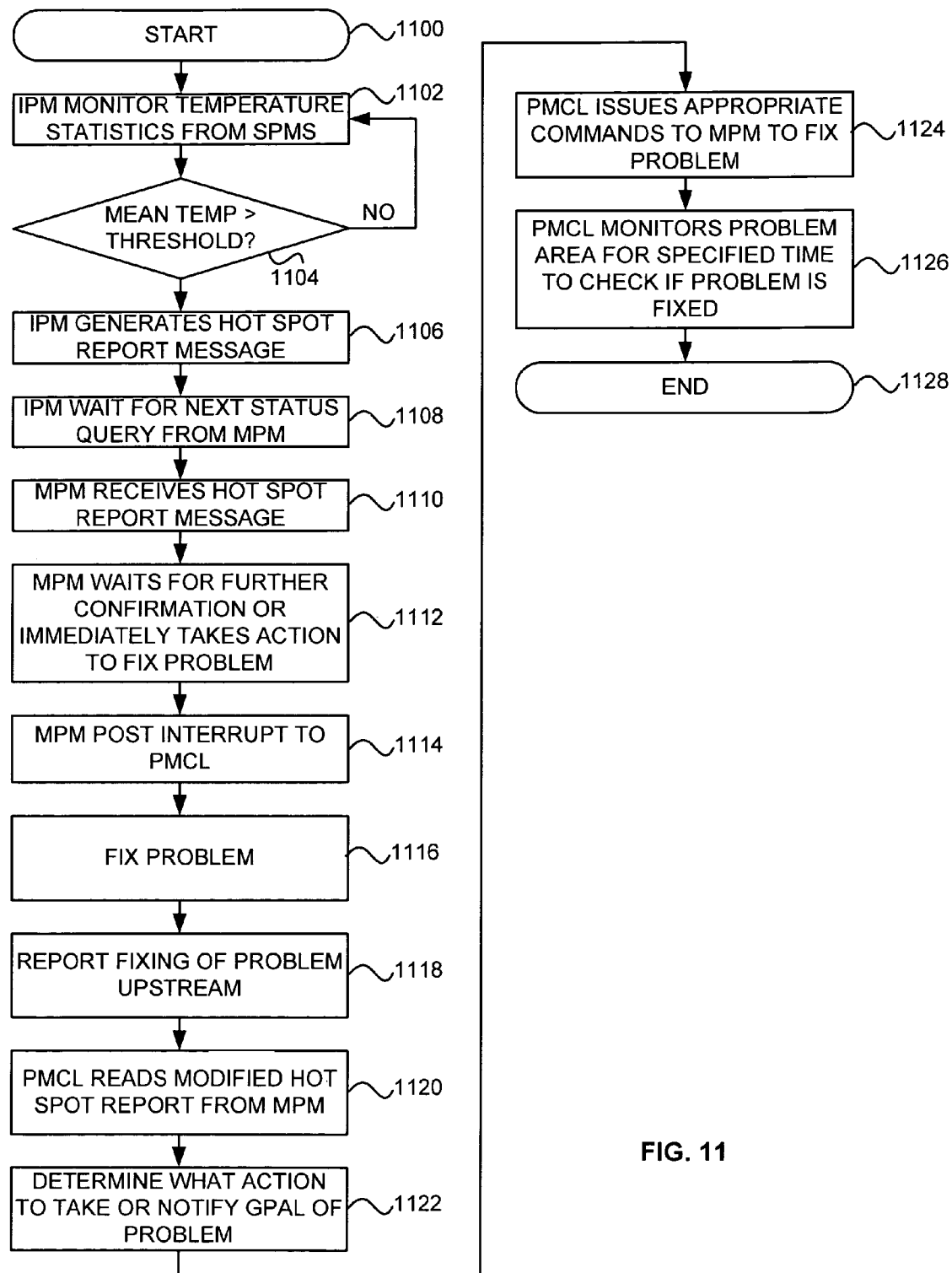


FIG. 11

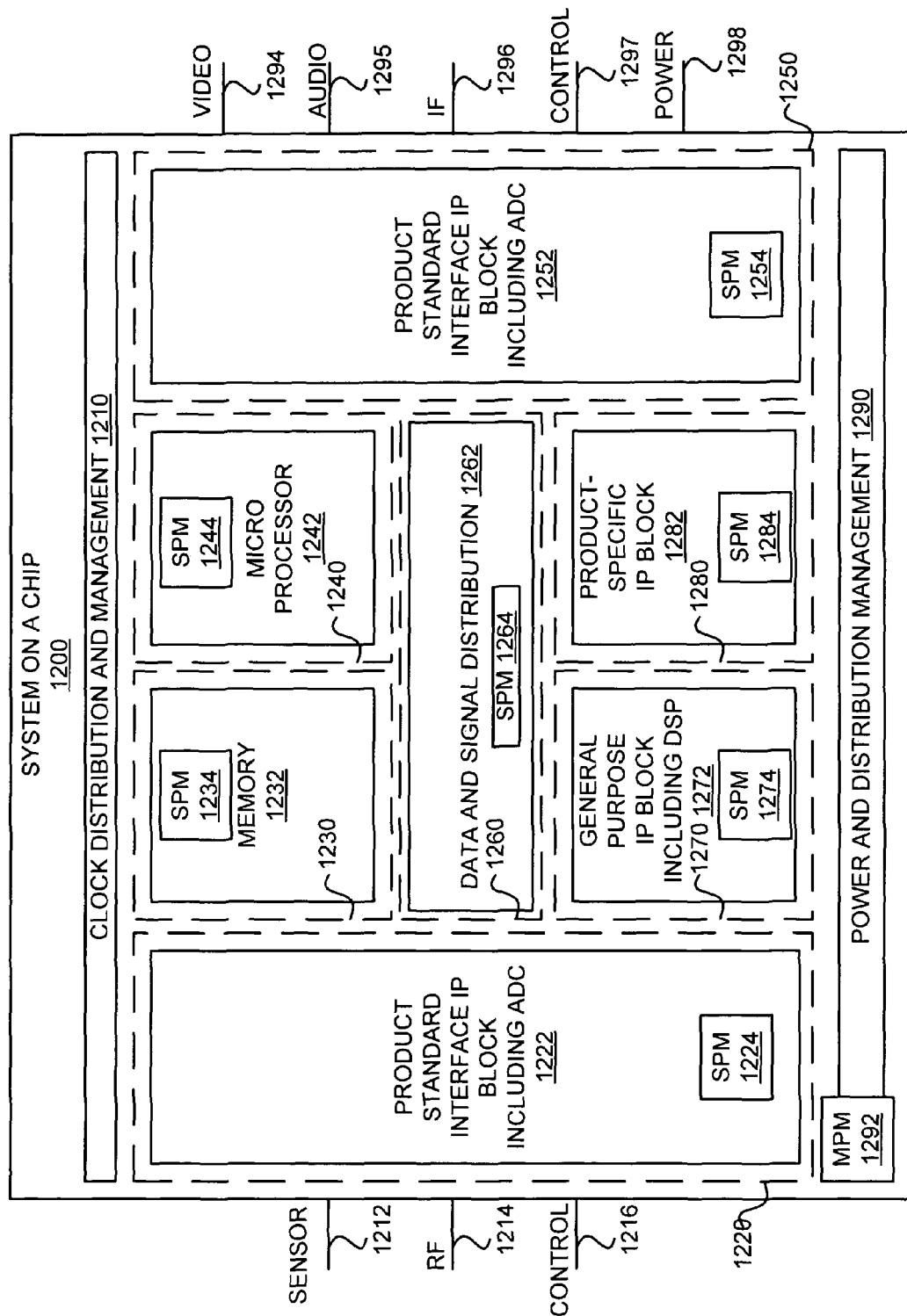


FIG. 12

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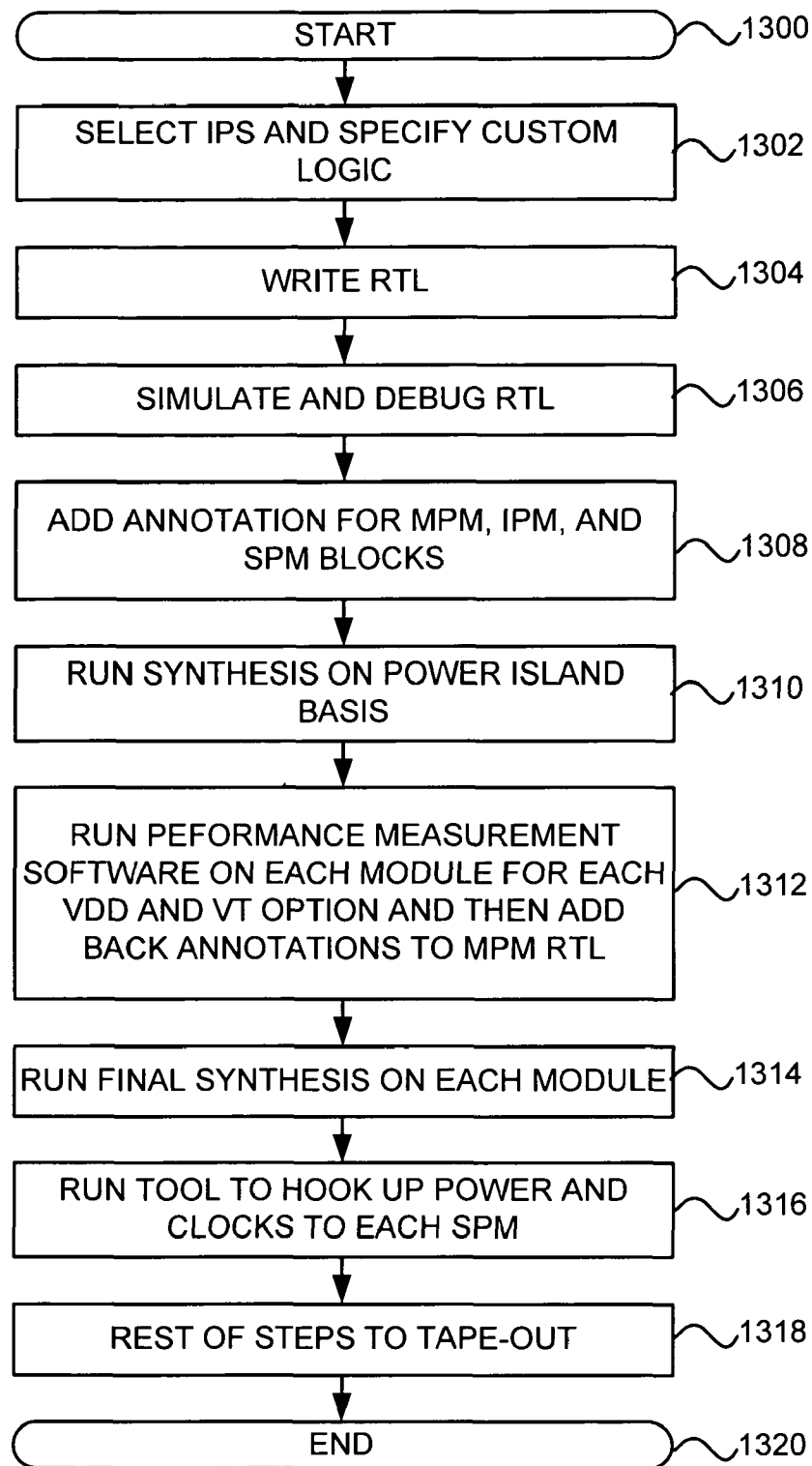


FIG. 13

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POWER MANAGERS FOR AN INTEGRATED CIRCUIT**CROSS-REFERENCE TO RELATED APPLICATIONS**

This application is a continuation of U.S. application Ser. No. 11/336,097 filed on Jan. 20, 2006 entitled "Power Managers for an Integrated Circuit" and which issued on Aug. 19, 2008 as U.S. Pat. No. 7,415,680, which is a continuation of U.S. application Ser. No. 10/840,893 filed on May 7, 2004 and entitled "Managing Power on Integrated Circuits Using Power Islands" and which issued on May 23, 2006 as U.S. Pat. No. 7,051,306 which claims the benefit of U.S. Provisional Application Ser. No. 60/468,742 titled "System and Method for Managing Power in Integrated Circuits," filed May 7, 2003, which are each hereby incorporated by reference.

BACKGROUND**1. Field of the Invention**

The present invention relates generally to integrated circuits, and more particularly to managing power on integrated circuits using power islands.

2. Description of the Prior Art

One design goal for integrated circuits is to reduce power consumption. Devices with batteries such as cell phones and laptops especially need a reduction in power consumption in the integrated circuit to extend the charge of the battery. Additionally, a reduction in power consumption prevents overheating and lowers the heat dissipation of the integrated circuit, which in some cases, eliminates or simplifies the heat sinks and/or fans for the integrated circuit.

Some integrated circuits are designed using building blocks of library cells. These library cells are blocks of circuitry performing a function. Some examples of library cells are NAND gates, multiplexers, decoders, comparators, and memory.

In a "full-custom" flow, the integrated circuit is designed at the lowest level such as at the individual transistors, capacitors, and resistors level. The "full-custom" flow may use library cells that are internally developed. The integrated circuit can have optimal performance because the integrated circuit is designed in great detail at the lowest level. However, some problems with the "full-custom" flow are the long time and expensive costs associated with designing at such a detailed level. Furthermore, the "full-custom" flow is cumbersome because the design is at the lowest level.

In a "standard-cell" flow, the integrated circuit is designed using library cells acquired from a third party or other outside source. These library cells are standardized at the logic or function level. The design time for the standard-cell flow is reduced because the library cells are already pre-designed and pre-tested.

In one example for designing an integrated circuit, the library cells are selected, and the custom logic is specified to build the integrated circuit. The register transfer level (RTL) for the integrated circuit is then written for simulation and debugging. After simulation and debugging, the synthesis is run for the integrated circuit. Performance measurement software is executed to determine performance of the integrated circuit. The final synthesis of the integrated circuit can then be run based on the optimal performance of the integrated circuit.

One problem with many integrated circuits is that power consumption is not efficiently utilized. For example, the

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entire integrated circuit may operate at a maximum frequency just to support an application needing that maximum frequency, while other portions of the integrated circuit can operate at a lower frequency. In another example, inactive circuitry within the integrated circuit consumes power and increases the likelihood of leakage. Inefficient power consumption may also adversely affect performance of the integrated circuit.

With the growing complexity of integrated circuits, the reduction of power consumption is even more important when the integrated circuit employs more functionality. One example of an integrated circuit is a system-on-a-chip that includes a microprocessor, memory, I/O interfaces, and an analog-to-digital converter all in a single chip. With many different types of functionality employed within a single chip, the system-on-a-chip consumes even more power than single function integrated circuits.

Some prior integrated circuits have employed voltage islands or multiple clocks to lower power consumption. One problem with these integrated circuits is that the voltages in the power island and the frequencies of the multiple clocks are static. The voltages and the frequencies do not dynamically change based on the needs and operation of the integrated circuit.

SUMMARY OF THE INVENTION

The invention addresses the above problems by providing power managers for an integrated circuit. A system for an integrated circuit comprising a plurality of power islands includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

The first power manager may determine power trade offs between the power islands. The second power manager may determine status information about the one of the power islands and may transmit the status information to the first power manager. The first power manager may receive the status information and may manage the first power consumption for the integrated circuit using the status information. The first power manager may determine status information about the integrated circuit and may transmit the status information to power interface software. The first power manager may receive a message from power interface software to change the first power consumption for the integrated circuit. The first power manager may transmit a message to the second power manager and the second power manager may receive and process the message to change the second power consumption for the one of the power islands. The second power manager may register capabilities of the second power manager with the first power manager.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a system for managing power in an integrated circuit in an exemplary implementation of the invention;

FIG. 2 is a diagram of a system for managing power in an integrated circuit in an exemplary implementation of the invention;

FIG. 3 is an illustration for low leakage circuitry for a low power standard cell logic block in an exemplary implementation of the invention;

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FIG. 4 is a diagram of a power island in an exemplary implementation of the invention;

FIG. 5 is a flowchart from an application request to a slave power manager action in an exemplary implementation of the invention;

FIG. 6 is an illustration of internal circuitry for a smart power unit in an exemplary implementation of the invention;

FIG. 7 is an illustration of external circuitry for a smart power unit in an exemplary implementation of the invention;

FIG. 8 is a flowchart from an application request to a smart power unit action in an exemplary implementation of the invention;

FIG. 9 is a flowchart for saving an IP unit's state prior to powering down and restoring the IP unit's state when powering up in an exemplary implementation of the invention;

FIG. 10 is diagram of a system on a chip and an extended local memory in an exemplary implementation of the invention;

FIG. 11 is a flowchart for generating a "hot spot" report from an intermediate power manager to a power management control layer in an exemplary implementation of the invention.

FIG. 12 is a diagram of a system on a chip in an exemplary implementation of the invention; and

FIG. 13 is a flowchart for building a chip with power islands in an exemplary implementation of the invention.

DETAILED DESCRIPTION OF THE INVENTION

As shown in the exemplary drawings wherein like reference numerals indicate like or corresponding elements among the figures, exemplary embodiments of a system and method according to the present invention are described below in detail. It is to be understood, however, that the present invention may be embodied in various forms. Therefore, specific details disclosed herein are not to be interpreted as limiting, but rather as a basis for the claims and as a representative basis for teaching one skilled in the art to employ the present invention in virtually any appropriately detailed system, structure, method, process or manner.

FIG. 1 depicts a block diagram of a system 100 for managing power in an integrated circuit 110 in an exemplary implementation of the invention. The system 100 includes an integrated circuit 110 and a power manager 120. The integrated circuit 110 is any electronic device that is instantiated into silicon and/or related manufacturing materials. One example of the integrated circuit 110 is a system-on-a-chip. The integrated circuit 110 includes multiple IP units, which are blocks of circuitry performing specific functions.

The integrated circuit 110 includes four power islands 112, 114, 116, and 118. FIG. 1 only depicts four power islands 112, 114, 116, and 118 for the sake of simplicity. Other embodiments of the integrated circuit 110 include a plurality of power islands 112, 114, 116, and 118. The power islands 112, 114, 116, and 118 are coupled to a bus 125.

A power island 112, 114, 116, and 118 is any section, delineation, partition, or division of the integrated circuit 110 where power consumption is controlled within the section, delineation, partition, or division. In some embodiments, the power islands 112, 114, 116, and 118 are delineated based on geographic factors of the integrated circuit 110. In some embodiments, the power islands 112, 114, 116, and 118 are delineated based on functional IP units of the integrated circuit 110. In one example depicted in FIG. 10, power islands are delineated by memory, a microprocessor, and separate IP blocks. In some embodiments, the power islands 112, 114, 116, and 118 are asynchronous or synchronous to each other.

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In some embodiments, the power islands 112, 114, 116, and 118 comprise sub-islands of power to provide further specificity in controlling power in the integrated circuit 110. In some embodiments, each of the power islands 112, 114, 116, and 118 supports multiple clock domains with its own control. In some embodiments, the clocks within the power islands 112, 114, 116, and 118 are variable.

In some embodiments, each of the power islands 112, 114, 116, and 118 includes power control circuitry. Power control circuitry is any circuitry configured to control power within one of the power islands 112, 114, 116, and 118. Some examples of power control circuitry include circuitry for level shifting, signal isolation, Vdd multiplexing, clock multiplexing, and dynamic back bias. In some embodiments, the power control circuitry is included in a standard cell library for standard cell design of the integrated circuit 110.

The power manager 120 is also coupled to the bus 125. One example of the bus 125 is a power command bus described in further detail below in FIG. 10. Other embodiments of the system 100 include numerous variations in which the power manager 120 and the power islands 112, 114, 116, and 118 are interconnected. The power manager 120 is any circuitry, device, or system configured to (1) determine a target power level for one of the power islands 112, 114, 116, and 118 where power consumption is independently controlled within each of the power islands 112, 114, 116, and 118, (2) determine action to change a consumption power level of the one of the power islands 112, 114, 116, and 118 to the target power level, and (3) perform the action to change the consumption power level of the one of the power islands 112, 114, 116, and 118 to the target power level. The power manager 120 can dynamically change the power consumption of the power islands 112, 114, 116, and 118 based on the needs and operation of the integrated circuit 110. The target power level is a desired, calculated, or specified power consumption of the power islands 112, 114, 116, and 118. Some examples of the power manager 120 are the slave power manager (SPM), the intermediate power manager (IPM), and the master power manager (MPM), which are described in further detail below. The power manager 120 may be a hierarchy or group of power managers 120. Although FIG. 1 depicts the power manager 120 as being located outside the integrated circuit 110, other embodiments may have the power manager 120 located in the integrated circuit 110. In other embodiments, the power manager 120 may be distributed among multiple power managers that are on or off the integrated circuit 110 or integrated with a CPU.

The action is any instruction, message, process, function, signal, or variable that controls power consumption in the power island 112, 114, 116, and 118. Some examples of actions are clock gating and dynamic clock selection. Another example of an action is modifying a clock frequency of one of the power islands 112, 114, 116, and 118. Another example of an action is to modify voltage of one of the power islands 112, 114, 116, and 118 such as dynamic voltage source, Vdd, selection. Another example of an action is to control dynamic leakage by controlling variable Vt transistors.

FIG. 2 depicts a diagram of a system 200 for managing power in an integrated circuit 250 in an exemplary implementation of the invention. The system 200 includes an embedded firmware stack 210 and an integrated circuit 250. The embedded firmware stack 210 includes software layers that run on a central processing unit (CPU). In some embodiments, the embedded firmware stack 210 may include an application layer 212, an operating system (OS) sub-system 216, a power management control layer (PMCL) 218, a real-time operating

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system (RTOS) 220, I/O drivers 222, and power manager (PM) firmware 224 for the MPM, IPM and/or SPM.

The integrated circuit 250 includes a power island 260, a power island 270, and a MPM 280. The power island 260 includes a low power standard cell logic block 262 and a SPM 264. The power island 270 includes a low power memory block 272 and a SPM 274. The low power standard cell logic block 262 and the low power memory block are coupled to an interface 265. The MPM 280 is coupled to the PMCL 218, the SPM 264, and the SPM 274.

In some embodiments, the application layer 212 includes a global power application layer (GPAL) 214. This GPAL 214 may be useful for more complex applications. If the GPAL 214 is present, then all calls to the PMCL 218 application program interfaces (API) are first directed to the GPAL 214. Both the GPAL 214 and the PMCL 218 provide power management for the integrated circuit 250. In some embodiments, the GPAL 214 and/or the PMCL 218 monitor what load is on each power island 260 and 270. Also, the GPAL 214 and/or the PMCL 218 may build a history of power levels on the power island 260 and 270 and store the history data in a database. The GPAL 214 and the PMCL 218 may also provide data for on-demand resources interested in the power levels of the power islands 260 and 270.

In some embodiments when the GPAL 214 is present, the GPAL 214 provides guidance to the PMCL 218 in making local decisions for power management of the integrated circuit 250. In some embodiments, the GPAL 214 and the PMCL 218 include complex algorithms for a static schedule. The GPAL 214 and the PMCL 218 provide the facility for use code to interact and control power behavior and parameters including providing a database and statistics.

The PMCL 218 also collects information from the MPM 280 and provides commands to the MPM 280 for possible IPMs, SPMs 264 and 274, and the power islands 260 and 270. Some of the commands may be to power on/off, change the power level, or change the frequency of the power islands 260 and 270. In some embodiments with a smart power unit (SPU) 290, the GPAL 214 and the PMCL 218 are responsible for communication with the SPU 290 to implement a power policy and collect information on the actual power supply. The SPU 290 is described in further detail below in FIGS. 6-8. In some embodiments, the GPAL 214 and the PMCL 218 provides sockets for existing power management techniques.

The power manager firmware 224 is firmware executed by the master power manager 280, the intermediate power manager, and the slave power managers 264 and 274.

The MPM 280 is any circuitry configured to control the “global” power behavior of the entire integrated circuit 250. In some embodiments, there are multiple MPMs 280 that control the power behavior of the entire integrated circuit 250. In some embodiments, the MPM 280 communicates with existing IPMs and SPMs 264 and 274 to control power within the power islands 260 and 270. The MPM 280 may receive status information about the power islands 260 and 270 from the SPMs 264 and 274 and the IPMs. The MPM 280 may also determine power trade-offs between the IPMs and the SPMs 264 and 274.

The MPM 280 may also provide a main interface to the PMCL 218 firmware. In some embodiments, the MPM 280 communicates with the PMCL 218 to accept commands (e.g. memory mapped commands) and provide status information about the power within the integrated circuit 250. In some embodiments, the MPM 280 communicates with the PMCL 218 through the main bus for the integrated circuit 250. The MPM 280 may also register each of the SPMs 264 and 274 and IPMs and capabilities with the PMCL 218. Some opera-

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tions of the MPM 280 are described in further detail below in FIGS. 5, 8, 9, and 11. In some embodiments, the MPM 280 reads and writes scan chains for state save and restore along with the local logic analyzer ability.

Some embodiments may include an IPM (not shown) that coordinates SPMs 264 and 274 on behalf of the MPM 280. In some embodiments, the IPM controls and coordinates power behavior on portions of the area controlled by the MPM 280. In some embodiments, the IPM controls the SPMs 264 and 274 that are on a separate chip from the MPM 280.

The SPM 264 is any circuitry configured to control power within a power island 264 in the integrated circuit 250. One example of the SPM 264 is an IP block that controls power within a power island 264 in the integrated circuit 250. The SPM 264 may include signal buffering, level shifting, and signal isolation. In some embodiments, the SPM 264 is integrated into scan chains to provide easier implementation and integration. Also, in some embodiments, the SPM 264 has a very small “footprint” with a low gate count and low power. In some embodiments, the SPM 264 comprises a command interface to communicate status information, service requests, and commands. Some of the commands are load, sleep, and idle. The SPM 264 may also recognize its own address to allow for multi-drop bussing.

In some embodiments, the SPM 264 has registration capabilities. For registration at power-up, the SPM 264 uses call-back registration that is typically used for off chip SPMs and IPMs. For static registration when the integrated circuit is generated for on chip SPMs, the SPM 264 registers what the SPM 264 can do, what the IPM can do, and the type of commands that the SPM 264 or IPM can service. The SPM 264 may also have save and restore functions for power off periods. The SPM 264 may have watch-dog timer(s). In some embodiments, the SPM 264 has a debug interface coordination to the power island 260. The SPM 264 may also monitor local state and collect information for components within the power island 260. The SPM 264 may also locally control Vdd, clocks for frequency selection, and dynamic back biasing. The description for the SPM 264 also applies to the SPM 274 for the power island 270.

In some embodiments, the SPM 264 checks whether an event occurs when the collected information from the power island 260 crosses a threshold or exceeds a range. In some embodiments, the SPM 264, IPMs, or the MPM 280 monitors power consumption levels of the power island 260 to check whether the power consumption levels cross a threshold level or exceed a range. A power consumption level is any information, data, or statistic that indicate the power consumed in a power island 260. Some examples of power consumption levels are temperature and power. The threshold or range may be programmable. The SPM 264 may report the event asynchronously, or another element such as the MPM 280 may solicit whether an event has occurred. The event may also be a multi-level test such as the conditions occur at a greater than a given, programmable frequency or exceed a given, programmable duration.

In some embodiments, the low power standard cell logic block 262 one example of a standard cell library that may be included in the power island 260. In some embodiments, the standard cell library is optimized for lower power. The standard cell library may be characterized over a range of operating voltages. In some embodiments, the standard cell library includes synchronous circuits and/or asynchronous circuits. In some embodiments, the standard cell library includes static circuits and/or encapsulated, dynamic logic circuits. The standard cell library may also include multiple voltage domain interface circuits such as level shifters and

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signal isolation circuits. The standard cell library may also have a multi-threshold design and characterization such as standard V_t, high V_t, low V_t, and variable V_t circuits. The standard cell library may also include data retention (shadow) circuits and anti-glitch circuits. The standard cell library may also include low leakage “sleep” circuits. FIG. 3 depicts an illustration of low leakage circuitry 300 for the low power standard cell logic block 262 in an exemplary implementation of the invention.

FIG. 4 depicts a diagram of the power island 270 in an exemplary implementation of the invention. The power island 270 includes a low power memory block 272 and the SPM 274. The low power memory block 272 includes banked architectures 410, 420, 430, and 440 for memories and sleep, power down circuitry 450. In some embodiments, the memory in the power island 270 is RAM and/or ROM. Some examples of the RAM are the SRAM compilers such as single-port, 2-port, and dual-port. Some examples of the ROM are ROM compilers. Some memories in the power island 270 are optimized for low power such as the low power memory block 272. In one embodiment, the low power memory block 272 includes multiple bank architectures via the compiler such as banked architectures 410, 420, 430, and 440. The memories in the power island 270 may also include sleep, power down circuitry 450 for low power modes such as sleep, nap, and full power down. The memories in the power island 270 may also include programmable read/write ports. The memories in the power island 270 may also be an asynchronous and/or synchronous design.

In some embodiments, the system 200 also includes a smart power unit (SPU) 290. In some embodiments, the SPU 290 is off-chip to the integrated circuit 250. The SPU 290 is an external unit configured to control power and clock distribution to the integrated circuit. The circuitry of the SPU is described in further detail below in FIGS. 7 and 8.

FIG. 5 depicts a flowchart from an application request to an SPM action in an exemplary implementation of the invention. FIG. 5 begins in step 500. In step 502, an application is invoked such as playing a movie. In step 504, the application determines the required frequency for performance of an IP unit. For example, the application determines a specified frequency in MHz for IP unit for an MPEG decoder. In some embodiments, when the IP unit is totally asynchronous, the required frequency will be an artificial measure of performance. In some embodiments that have multiple clocks involved, the minimum performance for each clock is specified.

In step 506, the application invokes the PMCL 218 API call. One example of this call is “Set_Rate (unit Y, N MHz, degree of dynamic power management (DPM) allowed, DPM threshold, other information to allow DPM trade-offs, starting back bias for SPMs with dynamic bias, wait for power up flag).” In this example, the other information could be “no power off, use high V_t and clocks off instead” and “major waits are about 10 us, with a 400 ns threshold.” In some embodiments with multiple clocks, the PMCL 218 API call allows the application to specify all required frequencies.

The PMCL 218 determines possible trade-offs available for the unit and selects a frequency rate, V_{dd}, and V_t if applicable for the unit that best meets the given requirements in step 508 and determines the applicable SPMs 264 and 274 in step 510. In some embodiments, the MPM 280 or IPM performs steps 508 and 510. In some embodiments for multiple clocks, the V_{dd} and V_t specified would allow for all specified clocks to meet or exceed their required frequencies.

In step 512, the PMCL 218 then writes the desired setting for the SPMs 264 and 274 to the MPM 280 (or IPM). In step

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514, the MPM 280 (or IPM) converts the request into one or more commands for the SPMs 264 and 274 (or IPM) associated with the unit.

In step 516, if the application sets the wait for power up flag, the PMCL 218 then waits until the IP unit is fully powered up before returning from the call. Otherwise, the call returns as soon as the command is acknowledged, with status of 0 for okay, 1 for fast power-up, 2 for slow power-up, or 3+ for error conditions. The powered up state is when the unit is at the desired V_{dd} for the requested frequency, and not just that the unit is turned on.

In step 518, the MPM 280 (or IPM) sends the requests to the appropriate targets. In step 520, the MPM 280 waits for the receipt of the acknowledgements that indicate message received and executed or execution has begun. A NACK or negative acknowledgement may also be returned from the SPM 264 and 274.

In step 522, the SPM 264 receives the commands and performs the actions. Steps 524-528 are possible actions that the SPM 264 may perform. In step 524, the SPM 264 switches the V_{dd} mux. In step 526, the SPM 264 switches a clock mux. In some embodiments when the voltage goes down, step 526 is performed before step 524. In step 528, the SPM 264 changes the V_t on the associated transistors. After the SPM 264 performs the actions, the SPM 264 returns a status message upstream indicating acknowledgement or negative acknowledgement in step 530. FIG. 5 ends in step 532.

FIG. 6 depicts an illustration of internal circuitry 600 for an SPU 290 in an exemplary implementation of the invention. In this embodiment, the internal circuitry 600 for the SPU 290 is internal to the integrated circuit 250 of FIG. 2. The internal circuitry 600 includes an external voltage 610, a dropout voltage regulator 620, a dropout voltage regulator 630, a logic block 640, and a logic block 650.

FIG. 7 depicts an illustration of external circuitry 700 for an SPU 290 in an exemplary implementation of the invention. In this embodiment, the external circuitry 700 for the SPU 290 is external to the integrated circuit 250 of FIG. 2. The internal circuitry 700 includes an external voltage 710, a power supply pin 720, a power supply pin 730, a power supply pin 740, a logic block 750, a logic block 760, and a logic block 770. The external circuitry 700 for the SPU 290 provides a DC/DC conversion. The DC/DC conversion provides multiple independent power supply pins 720, 730, and 740. The power supply pins 720, 730, and 740 have a variable voltage supply on each separate power pin. Also, in some embodiments, the variable voltage is within a range and in steps. In some embodiments, the PMCL 218 controls the voltage to power supply pins 720, 730, and 740.

FIG. 8 depicts a flowchart from an application request to an SPU action in an exemplary implementation of the invention. FIG. 8 begins in step 800. In step 802, an application is invoked. In step 804, the application determines the required frequency for performance of an IP unit. For example, the application determines a specified frequency in MHz for IP unit for an MPEG decoder.

In step 806, the application invokes the PMCL 218 API call. One example of this call is “Set_Rate (unit Y, N MHz, degree of dynamic power management (DPM) allowed, DPM threshold, other information to allow DPM trade-offs, starting back bias for SPMs with dynamic bias, wait for power up flag).” In this example, the other information could be “no power off, use high V_t and clocks off instead” and “major waits are about 10 us, with a 400 ns threshold.”

The PMCL 218 determines possible trade-offs available for the unit and selects a the lowest possible V_{dd} that will

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support the requested frequency in step 808 and determines the SPMs 264 and 274 that will be affected and which power pins to change in step 810.

In step 812, the PMCL 218 sends a command to the MPM 280 to have the SPMs 264 and 274 (and IPM) to prepare for a Vdd change. In step 814, the PMCL 218 waits for the acknowledgement from the MPM 280. In step 816, the PMCL 218 sends a command to the SPU 290 to change the Vdd on the selected power pins and waits for the affected area to “settle down.” In step 818, the PMCL 218 then sends a “resume operation at a specified frequency” command to the MPM 280. In step 820, the MPM 280 propagates the resume command to all affected SPMs 264 and 274 (and IPMs). In step 822, one of the power managers (i.e. MPM 280, IPM, or SPMs 264 and 274) sets the specified frequency. In step 824, the IP unit operation resumes after the clock has settled. FIG. 8 ends in step 826. In some embodiments, the user application has the option of waiting for the entire operation to finish or to continue and either query the PMCL 218 as to the progress of the operation or wait for a “finished” interrupt from the PMCL 218.

FIG. 9 depicts a flowchart for saving an IP unit’s state prior to powering down and restoring the IP unit’s state when powering up in an exemplary implementation of the invention. FIG. 9 begins in step 900. In step 902, the user application requests that the PMCL 218 power off an IP unit and wants to save the IP unit’s state. In some embodiments, the reconfiguration of the IP unit takes a long time. The request in step 902 may be accompanied by the address of an area to which the state should be saved.

In step 904, the PMCL 218 sends a “stop clock and read IP unit state” message to the MPM 280. The MPM 280 then propagates the “stop clock and read IP unit state” message to the SPMs 264 and 274 of the affected unit in step 906. In step 908, the MPM 280 uses the scan chain for the IP unit to read the state into a register or buffer for presentation to the PMCL 218. In step 910, if the PMCL 218 provided the MPM 280 with the address of the save area, the MPM 280 saves the state information directly in the specified area. In step 912, after all of the IP units’ state has been saved, the PMCL 218 sends a “power off IP unit” message to the MPM 280. In step 914, the MPM 280 then propagates out the “power off IP unit” message. In step 916, the PMCL 218 returns the save state area to the user application. The save state area contains the state of the unit.

At a later time, in step 918, the user application requests that the PMCL 218 power the IP unit back up and restore the state of the IP unit. In some embodiments, the user application request includes the address of the area to which the state was saved. In step 920, the PMCL 218 sends a “power up IP unit with clocks off and restore state” message to the MPM 280. In step 922, the MPM 280 propagates the “power up IP unit with clocks off and restore state” message to the SPMs 264 and 274 of the affected IP unit. In step 924, after the IP unit is powered up, the MPM 280 uses the scan chain to reload the unit’s state. In some embodiments, the reloading of the unit’s state originates directly from the save area or from information passed to the MPM 280 from the PMCL 218. In step 926, the PMCL 218 sends a message to the MPM 280 to turn clock back on and report to user application that the IP unit is ready to continue operations. FIG. 9 ends in step 928.

In some embodiments, the same functionality of FIG. 9 can be used to implement an internal “logic analyzer” function, in which the IP unit in question would not be powered down after being read. If the associated SPMs 264 and 274 of the IP unit have the ability to single- or multi-step the clock, the local scan testing is performed by having the SPMs 264 and

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274 “signal isolate” the IP unit. Then, use of a combination of the ability of single- or multi-step the clock and the ability to use the scan chain can read/write the IP unit’s internal state.

FIG. 10 depicts a diagram of a system-on-a-chip (SOC) 1000 and an extended local memory 1004 in an exemplary implementation of the invention. The SOC 1000 is one example of the integrated circuit 250 and communicates with the embedded firmware stack 210 in FIG. 2 as described above. The SOC 1000 includes a CPU 1010, a local memory 1020, a memory controller 1030, a mixed signal circuitry 1040, an application specific circuitry 1050, a PCI-X circuitry 1060, a MPM 1070, a real-time clock (RTC) 1075, an Ethernet circuitry 1080, and a USB circuitry 1090. The CPU 1010, the local memory 1020, the memory controller 1030, the mixed signal circuitry 1040, the application specific circuitry 1050, the PCI-X circuitry 1060, the Ethernet circuitry 1080, and the USB circuitry 1090 are all power islands in which power is controlled within the power islands by power managers. In this embodiment, the power islands are delineated by the functionality of a part of the SOC 1000.

The extended local memory 1004 includes an IPM 1006 that is coupled to the bus 1071. The CPU 1010 includes an SPM 1015 that is coupled to the bus 1071. The local memory 1020 includes an SPM 1025 that is also coupled to the bus 1071. The memory controller 1030 comprises an SPM 1035 that is coupled to the bus 1071. The mixed signal circuitry 1040 includes an SPM 1045 that is coupled to the bus 1071. The application specific circuitry 1050 includes an IPM 1055 and an SPM 1058 that are both coupled to the bus 1072. The PCI-X circuitry 1060 includes an SPM 1065 that is coupled to the bus 1072. The MPM 1070 is coupled to the bus 1071 and the bus 1072. The MPM 1070 is one example of the MPM 280 as described above. The Ethernet circuitry 1080 includes an SPM 1085 that is coupled to the bus 1072. The USB circuitry 1090 includes an SPM 1095 that is coupled to the bus 1072.

In this embodiment, power command buses comprise the bus 1071 and the bus 1072. The bus 1071 and 1072 are simple multi-drop serial buses that may cross chip boundaries and interconnect power managers. The power command bus may be a combination of serial busses, such as the bus 1071 and the bus 1072, with one per region of the chip and then multi-drop within the region. In other embodiments, the power command bus includes a parallel bus or a combination of serial and parallel busses. In some embodiments, the power command bus is the system bus. The power command bus may contain messages with at least a unit ID with the associated payload. For a fixed point to point bus, the message does not need a unit ID only the payload.

In some embodiments, the power command bus uses an error detection scheme such as parity, ECC, or a redundant code. In some embodiments, the power command bus is a low performance bus that does not interfere with the integrated circuit design and is not visible to the user. In some embodiments, the communication between the PMCL 218 and the MPM 1070 is memory mapped and based on the main bus such as an AHB for an SOC 1000.

Some embodiments may include a separate bus for reporting status information between the power managers. In one example, this separate bus provides asynchronous “Alert” type status messages from SPMs to the MPM.

There can be various message formats for the power command bus. In one example for a basic format, the message format includes a start of message indicator, a power manager address, type code, basic command, and an end of message indicator. In one example for an extended format, the message format includes the basic format, an additional length, and additional information. In one example for a response mes-

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sage format, the message format includes a start of message reply indicator, a power manager address, a 3b ACK or NAK or return status (implied ACK), a payload length for return status messages, a payload for return status messages, a reason code for NAK, and an end of message indicator.

In some embodiments, the SPM 1015 or the IPM 1006 times out on replying to a command, and the MPM 1070 reissues the command a programmable number of times. If the SPM 1015 or the IPM 1006 still fails, the MPM 1070 marks the SPM 1015 or the IPM 1006 as unusable and reports back the failure to the PMCL 218. In one embodiment, the PMCL 218 has the MPM 1070 reinitialize the failing SPM 1015 or the IPM 1006 via the scan system and then retries sending the message. Other conditions such as invalid responses to commands or invalid status reports are also handled by the re-initialization. In some embodiments, the state of the failing SPM 1015 or the IPM 1006 may be read out and saved for later analysis.

FIG. 11 depicts a flowchart for generating a “hot spot” report from an IPM 1055 to the PMCL 218 in an exemplary implementation of the invention. FIG. 11 begins in step 1100. In step 1102, the IPM 1055 monitors the temperature statistics of the SPMs. In step 1104, the IPM 1055 checks whether the mean temperature has exceeded a predetermined and programmed threshold. If the mean temperature has not exceeded the threshold, the IPM 1055 returns to step 1102 to keep monitoring. If the mean temperature has exceeded the threshold, the IPM 1055 then generates a problem (“hot spot”) report message in step 1106. In step 1108, the IPM 1055 waits for the next status query the MPM 1070. In some embodiments, a logically separate bus is provided for asynchronous status reports to the MPM 280.

In step 1110, the MPM 1070 receives the hot spot report message. In step 1112, the MPM 1070 either waits for further confirmation (i.e. see that the “hot spot” last pasts a predetermined threshold) or immediately takes action to fix the problem depending on the internal logic of the MPM 1070. In some embodiments, in step 1114, the MPM 1070 takes action by posting an interrupt to the PMCL 280 that it needs attention. In other embodiments, if the PMCL 280 queries the MPM 1070 often enough, then the interrupt is not needed. In step 1116, the MPM 1070 (or IPM) fixes the problem by making a local trade-off, performing the action, or ordering the action to be performed. One example of fixing the problem is lowering the operating frequency of the hot spot area. In step 1118, the MPM 1070 reports both the problem and the fixing of the problem upstream.

In step 1120, the PMCL 218 reads the modified hot spot report from the MPM 1070. In step 1122, the PMCL 218 determines what action to take to fix the problem or notify the GPAL 214 of the problem. In step 1124, the PMCL 218 issues the appropriate commands to the MPM 1070 to fix the problem. In this step, the software will make the trade-off required to fix the problem. In some embodiments, if the GPAL 214 determines the high level fix, then the GPAL 214 sends it to the PMCL 280 to be converted into MPM commands. In step 1126, the PMCL 218 monitors the problem area for a specified time to check if the problem is fixed. FIG. 11 ends in step 1128.

In some embodiments, the type of functionality in FIG. 11 can be performed at other levels such as the PMCL 218. In one example, the PMCL 218 queries (via the MPM 1070) all the SPMs that have the desired measurement ability (and IPMs) as to their local conditions and can then, for example, build a “map” of power usage that it can then act on.

FIG. 12 depicts a diagram of a system-on-a-chip (SOC) 1200 in another exemplary implementation of the invention.

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The SOC 1200 is attached to a sensor link 1212, an RF link 1214, a control link 1216, a video link 1294, an audio link 1295, an interface link 1296, a control link 1297, and a power link 1298. The SOC 1200 includes clock and distribution management 1210, an IP block power island 1220, a memory power island 1230, a microprocessor power island 1240, an IP block power island 1250, a distribution power island 1260, an IP block power island 1270, an IP block power island 1280, and power and distribution management 1290.

The IP block power island 1220 includes a product standard interface IP block including an analog-to-digital converter (ADC) 1222, which includes an SPM 1224. The IP block power island 1230 includes a memory 1232, which includes an SPM 1234. The microprocessor power island 1240 includes a microprocessor 1242, which includes an SPM 1244. The IP block power island 1250 includes a product standard interface IP block including ADC 1252, which includes an SPM 1254. The distribution power island 1260 includes a data and signal distribution 1262, which includes an SPM 1264. The IP block power island 1270 includes a general purpose IP block including a digital signal processor (DSP) 1272, which includes an SPM 1274. The IP block power island 1280 includes a product-specific IP block 1282, which includes an SPM 1284. The power and distribution management 1290 includes an MPM 1292.

FIG. 13 depicts a flowchart for building a chip with power islands in an exemplary implementation of the invention. FIG. 13 begins in step 1300. In step 1302, the IPs or library cells are selected, and the custom logic, if any, is specified to be used to build the chip. In some embodiments, the maximum and sub clock rate, % idle time, and minimum and maximum Vdd are specified. In step 1304, the register transfer level (RTL) is written. In step 1306, the RTL is simulated and debugged.

Either during or after the writing of the RTL, a software tool may be used to add annotations for the MPM, IPM, and/or SPM blocks in step 1308. In some embodiments, the desired functionality options are specified in the annotations. In some embodiments, the optional functionality is specified per SPM block. In some embodiments, the RTL is annotated with SPM configuration information on a per-module basis. In some embodiments, the proper annotation is inserted by hand on a per module basis during or after the RTL is written. In other embodiments, a separate table in the proper format is created with the module names and respective annotations. In some embodiments, a separate software tool provides the ability to interactively build the separate table. In some embodiments, the software tool adds the proper annotation to the un-annotated modules in the RTL using information from the table.

In step 1310, the synthesis is run on a power island basis, where power islands are not mixed. In step 1312, performance measurement software is run on each module for each Vdd and Vt option, and then the annotations for the MPM are added to the RTL. In some embodiments, the performance of the design is measured at all desired voltages and Vt combinations. The software tool then derives the actual frequency, Vdd, and Vt tables for each SPM and back annotates the MPM (or IPM) RTL of the SPM characteristics.

In step 1314, the final synthesis is run on a power island basis. In some embodiments, the modules are separately routed or by SPM. In step 1316, the software tool is run to hook up power and clocks to each SPM. Step 1318 is the rest of the steps to tape-out. In some embodiments, the software tool generates the finished net-list with all information. FIG. 13 ends in step 1320.

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The above-described elements can be comprised of instructions that are stored on storage media. The instructions can be retrieved and executed by a processor. Some examples of instructions are software, program code, and firmware. Some examples of storage media are memory devices, tape, disks, integrated circuits, and servers. The instructions are operational when executed by the processor to direct the processor to operate in accord with the invention. Those skilled in the art are familiar with instructions, processor, and storage media.

The above description is illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

What is claimed is:

1. An integrated circuit comprising:
an integrated circuit chip;
a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;
one or more power consumption signals indicating one or more of the power consumptions;
a power management processor disposed on the integrated circuit chip and coupled to each of the power islands configured to monitor the one or more power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.
2. The integrated circuit as claimed in claim 1 wherein the power management software is embedded firmware in the integrated circuit.
3. The integrated circuit as claimed in claim 2 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.
4. The integrated circuit as claimed in claim 2 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.
5. The integrated circuit as claimed in claim 1 wherein each of the power consumptions is further controlled by stopping a clock.
6. The integrated circuit as claimed in claim 5 wherein stopping the clock comprises clock gating.
7. The integrated circuit as claimed in claim 1 wherein the one or more power consumption signals include temperature or power dissipation measurement.
8. An integrated circuit comprising:
an integrated circuit chip;
a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;
one or more power consumption signals indicating one or more of the power consumptions;
a power manager disposed on the integrated circuit chip and coupled to each of the power islands configured to

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monitor the one or more power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

9. The integrated circuit as claimed in claim 8 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.

10. The integrated circuit as claimed in claim 9 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

11. The integrated circuit as claimed in claim 9 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

12. The integrated circuit as claimed in claim 8 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.

13. The integrated circuit as claimed in claim 8 wherein each of the power consumptions is further controlled by stopping a clock.

14. The integrated circuit as claimed in claim 13 wherein stopping the clock comprises clock gating.

15. The integrated circuit as claimed in claim 8 wherein the one or more power consumption signals include temperature or power dissipation measurement.

16. An integrated circuit comprising:

an integrated circuit chip;

a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

a power management processor disposed on the integrated circuit chip and coupled to each of the power islands and configured to monitor the power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

17. The integrated circuit as claimed in claim 16 wherein the power management software is embedded firmware in the integrated circuit.

18. The integrated circuit as claimed in claim 17 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

19. The integrated circuit as claimed in claim 17 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

20. The integrated circuit as claimed in claim 16 wherein each of the power consumptions is further controlled by stopping a clock.

21. The integrated circuit as claimed in claim 20 wherein stopping the clock comprises clock gating.

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22. The integrated circuit as claimed in claim 16 wherein each of the power consumption signals includes temperature or power dissipation measurement.

23. An integrated circuit comprising:

a integrated circuit chip;

a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

a power manager disposed on the integrated circuit chip coupled to each of the power islands and configured to monitor the power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

24. The integrated circuit as claimed in claim 23 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.

25. The integrated circuit as claimed in claim 24 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

26. The integrated circuit as claimed in claim 24 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

27. The integrated circuit as claimed in claim 23 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.

28. The integrated circuit as claimed in claim 23 wherein each of the power consumptions is further controlled by stopping a clock.

29. The integrated circuit as claimed in claim 28 wherein stopping the clock comprises clock gating.

30. The integrated circuit as claimed in claim 23 wherein each of the power consumption signals includes temperature or power dissipation measurement.

31. A system comprising:

an integrated circuit;

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

one or more power consumption signals indicating one or more of the power consumptions;

a power management processor coupled to each of the power islands configured to monitor the one or more power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

32. The system as claimed in claim 31 wherein the power management software is embedded firmware.

33. The system as claimed in claim 32 wherein one or more of the power consumptions is changed by selecting a non-zero

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supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

34. The system circuit as claimed in claim 32 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

35. The system as claimed in claim 31 wherein each of the power consumptions is further controlled by stopping a clock.

36. The system as claimed in claim 35 wherein stopping the clock comprises clock gating.

37. The system as claimed in claim 31 wherein the system is configured to have the supply voltage provided by an external regulator.

38. The system as claimed in claim 31 wherein the one or more power consumption signals include temperature or power dissipation measurement.

39. A system comprising:

an integrated circuit;

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

one or more power consumption signals indicating one or more of the power consumptions;

a power manager coupled to each of the power islands configured to monitor the one or more power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

40. The system as claimed in claim 39 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.

41. The system as claimed in claim 40 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

42. The system as claimed in claim 40 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

43. The system as claimed in claim 39 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.

44. The system as claimed in claim 39 wherein each of the power consumptions is further controlled by stopping a clock.

45. The system as claimed in claim 44 wherein stopping the clock comprises clock gating.

46. The system as claimed in claim 39 wherein the system is configured to have the supply voltage provided by an external regulator.

47. The system as claimed in claim 39 wherein the one or more power consumption signals include temperature or power dissipation measurement.

48. A system comprising:

an integrated circuit;

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

a power management processor coupled to each of the power islands configured to monitor the power consumption signals, the power management processor being dedicated to execute power management software

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to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

49. The system as claimed in claim 48 wherein the power management software is embedded firmware.

50. The system as claimed in claim 49 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

51. The system as claimed in claim 49 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

52. The system as claimed in claim 48 wherein each of the power consumptions is further controlled by stopping a clock.

53. The system as claimed in claim 52 wherein stopping the clock comprises clock gating.

54. The system as claimed in claim 48 wherein the system is configured to have the supply voltage provided by an external regulator.

55. The system as claimed in claim 48 wherein each of the power consumption signals includes temperature or power dissipation measurement.

56. A system comprising:
an integrated circuit;

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;

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a power manager coupled to each of the power islands configured to monitor the power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

57. The system as claimed in claim 56 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.

58. The system as claimed in claim 57 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.

59. The system as claimed in claim 57 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.

60. The system as claimed in claim 56 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.

61. The system as claimed in claim 56 wherein each of the power consumptions is further controlled by stopping a clock.

62. The system as claimed in claim 61 wherein stopping the clock comprises clock gating.

63. The system as claimed in claim 56 wherein the system is configured to have the supply voltage provided by an external regulator.

64. The integrated circuit as claimed in claim 56 wherein each of the power consumption signals includes temperature or power dissipation measurement.

* * * * *

EXHIBIT C



US007996811B2

(12) **United States Patent**
Hoberman et al.

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(45) **Date of Patent:** ***Aug. 9, 2011**

(54) **POWER MANAGERS FOR AN INTEGRATED CIRCUIT**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 359 days.

This patent is subject to a terminal disclaimer.

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(63) Continuation of application No. 12/176,645, filed on Jul. 21, 2008, which is a continuation of application No. 11/336,097, filed on Jan. 20, 2006, now Pat. No. 7,415,680, which is a continuation of application No. 10/840,893, filed on May 7, 2004, now Pat. No. 7,051,306.

(60) Provisional application No. 60/468,742, filed on May 7, 2003.

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G06F 17/50 (2006.01)

(52) **U.S. Cl.** **716/133; 716/100; 716/126; 716/127; 716/132**

(58) **Field of Classification Search** **716/100, 716/126, 127, 132, 133**

See application file for complete search history.

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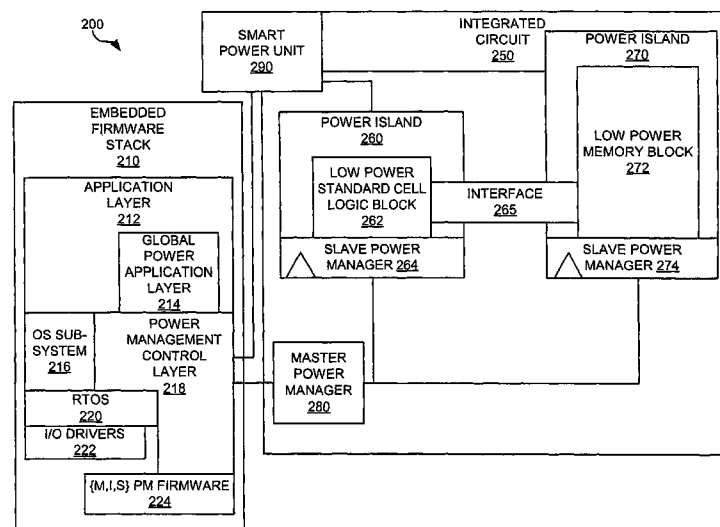
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(57) **ABSTRACT**

A system for an integrated circuit comprising a plurality of power islands includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

74 Claims, 13 Drawing Sheets



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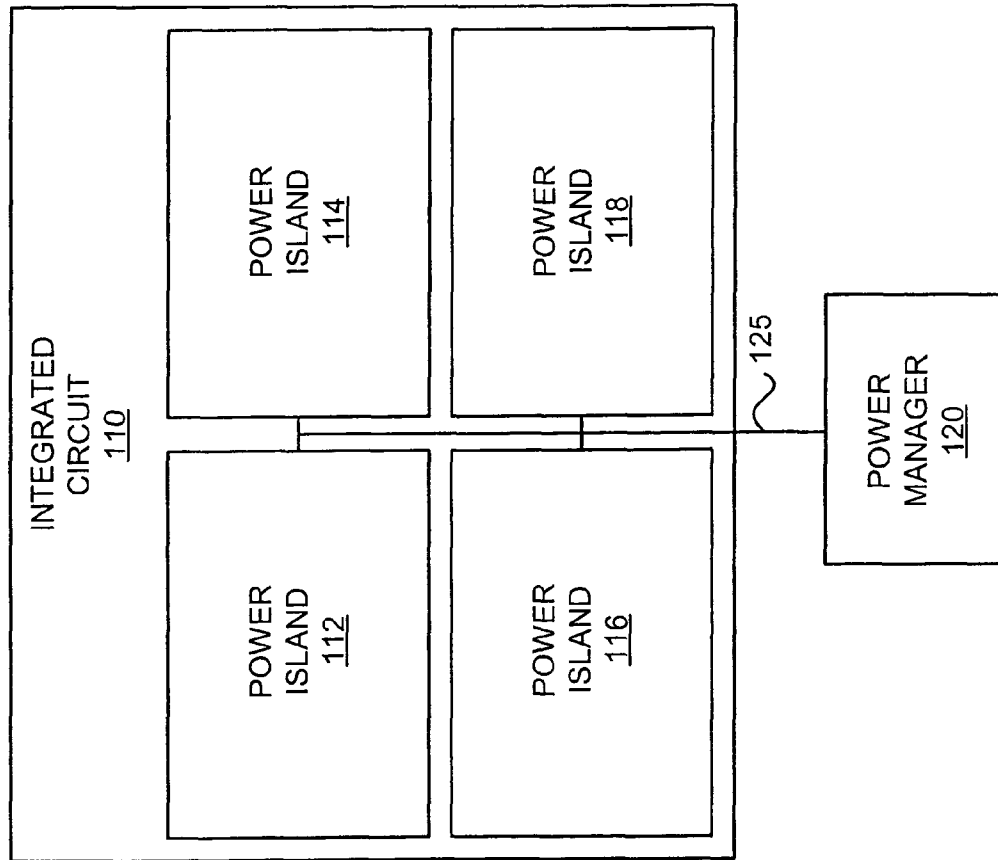


FIG. 1

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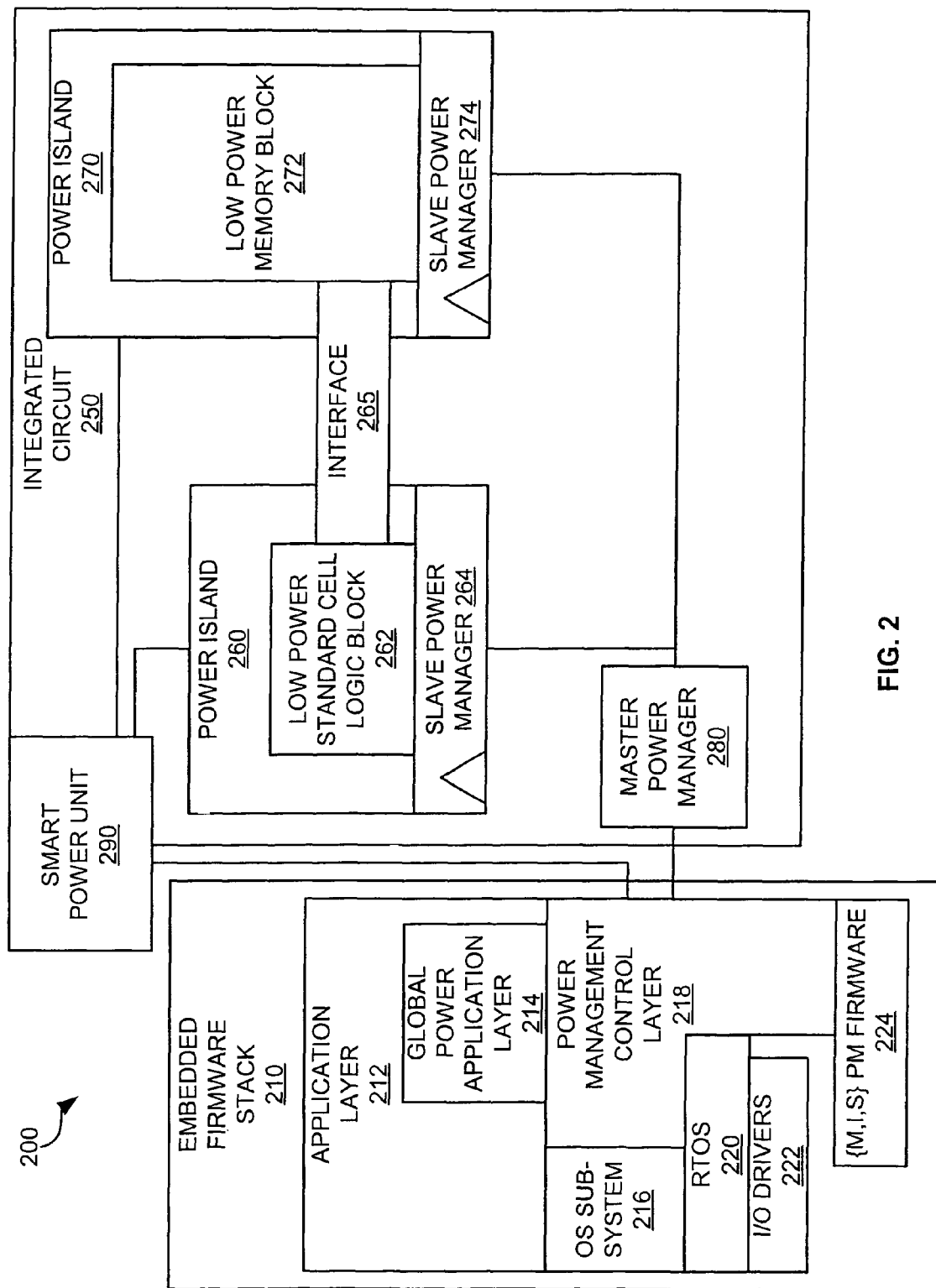


FIG. 2

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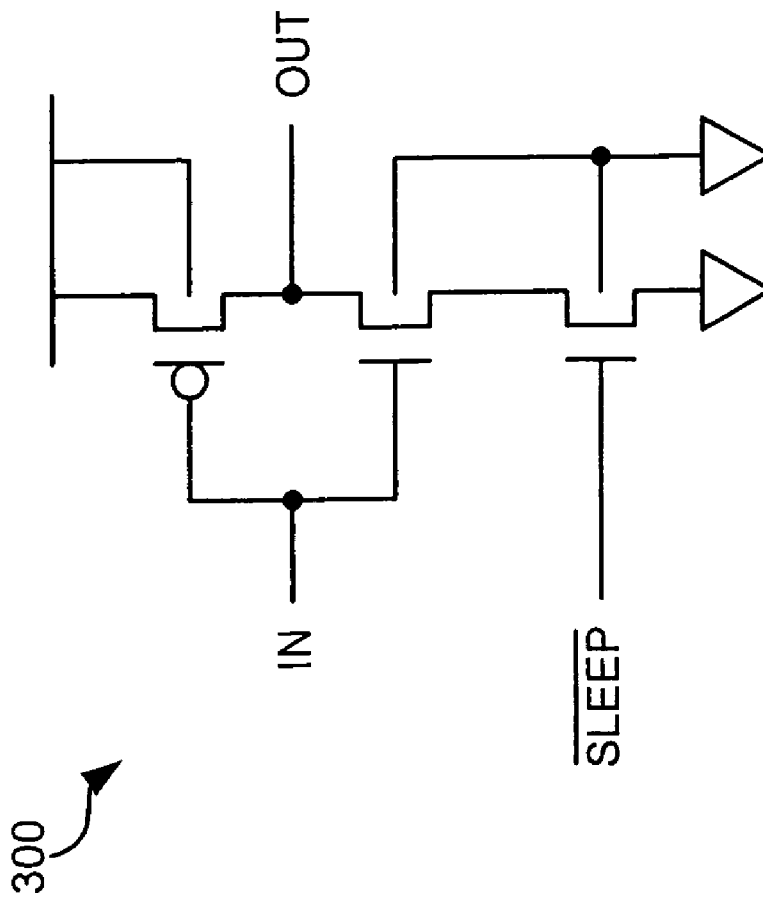


FIG. 3

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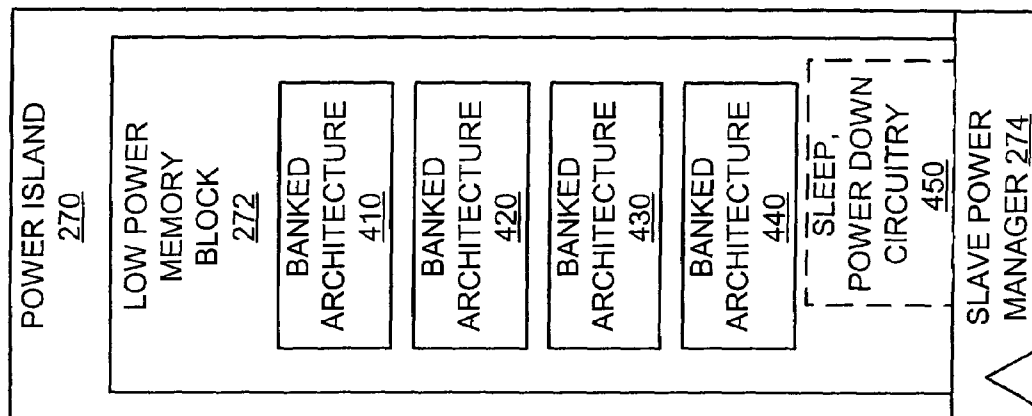


FIG. 4

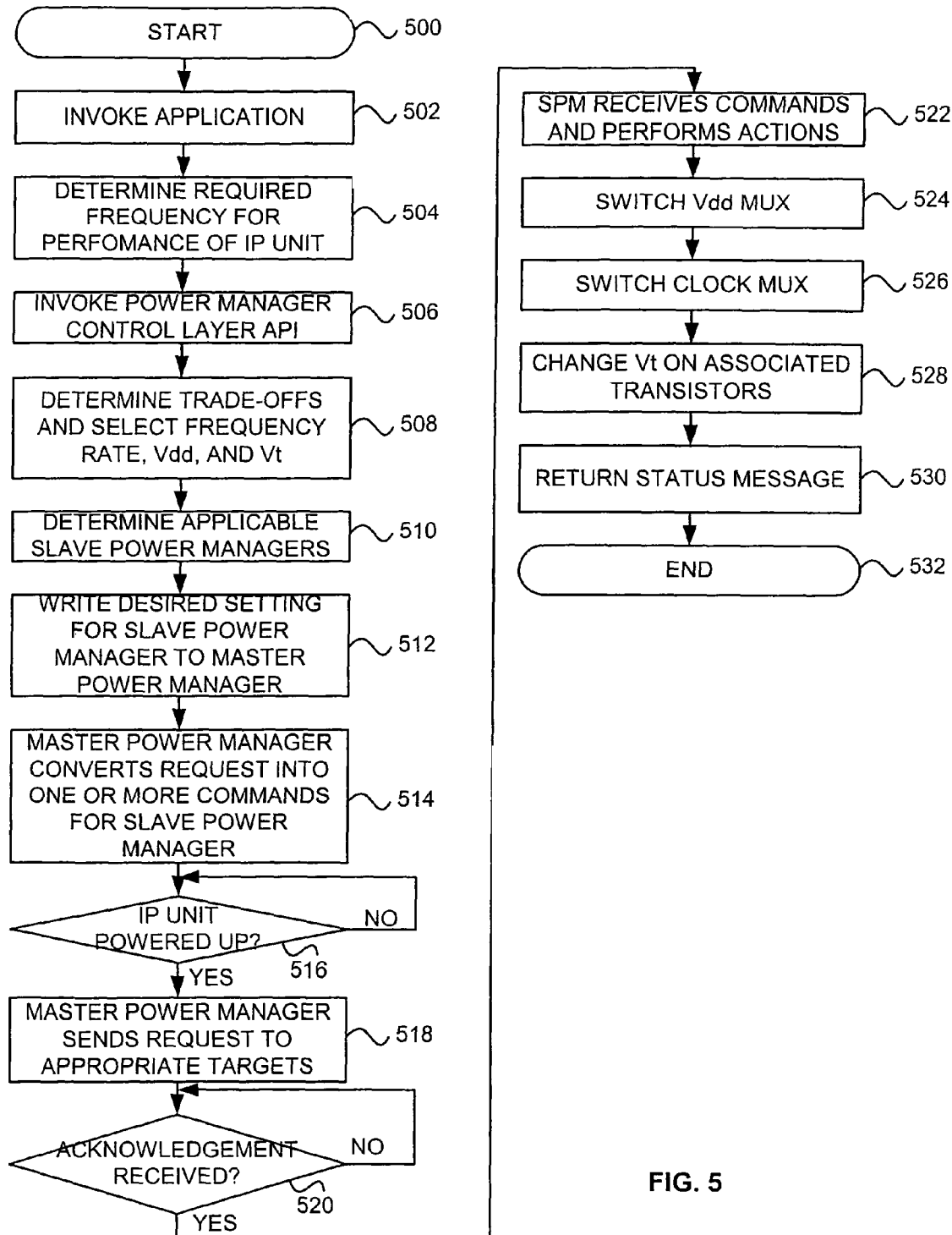


FIG. 5

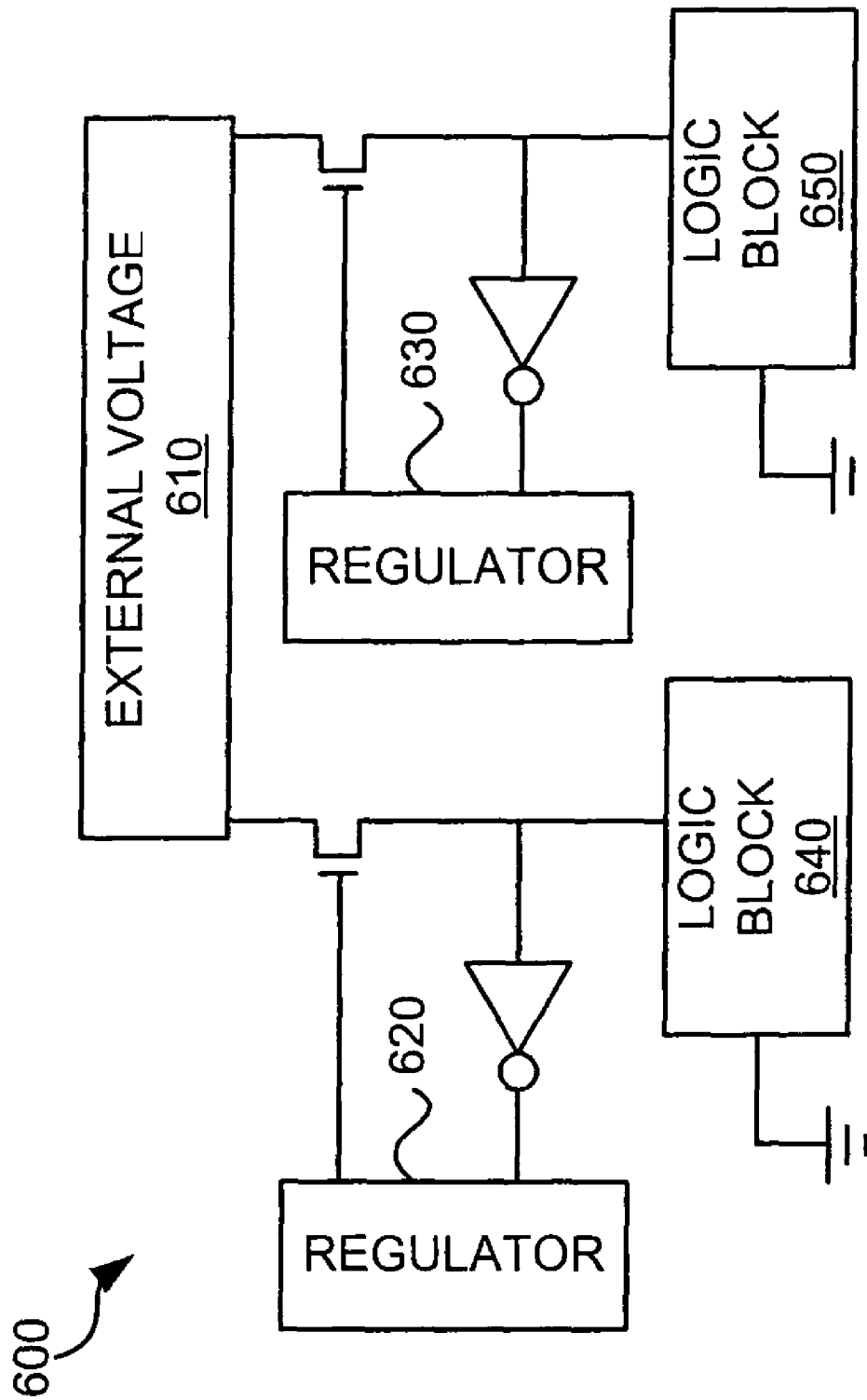


FIG. 6

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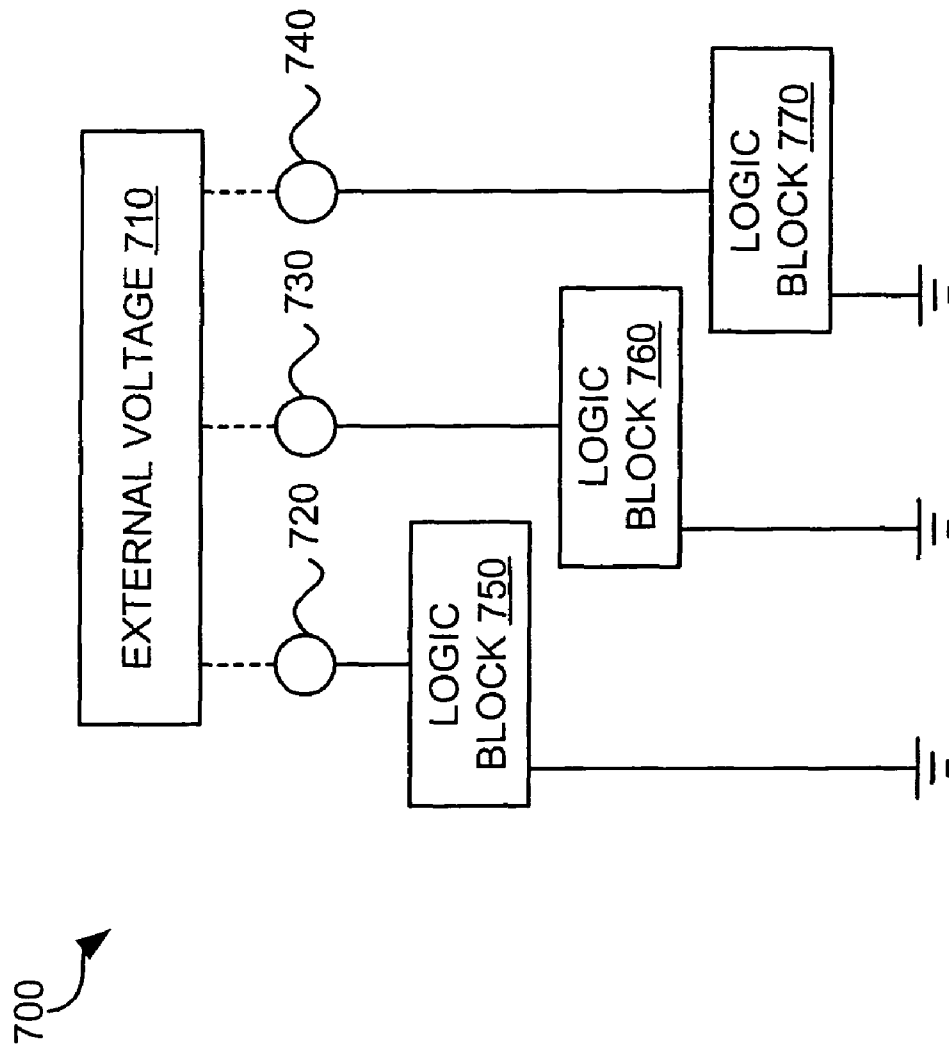


FIG. 7

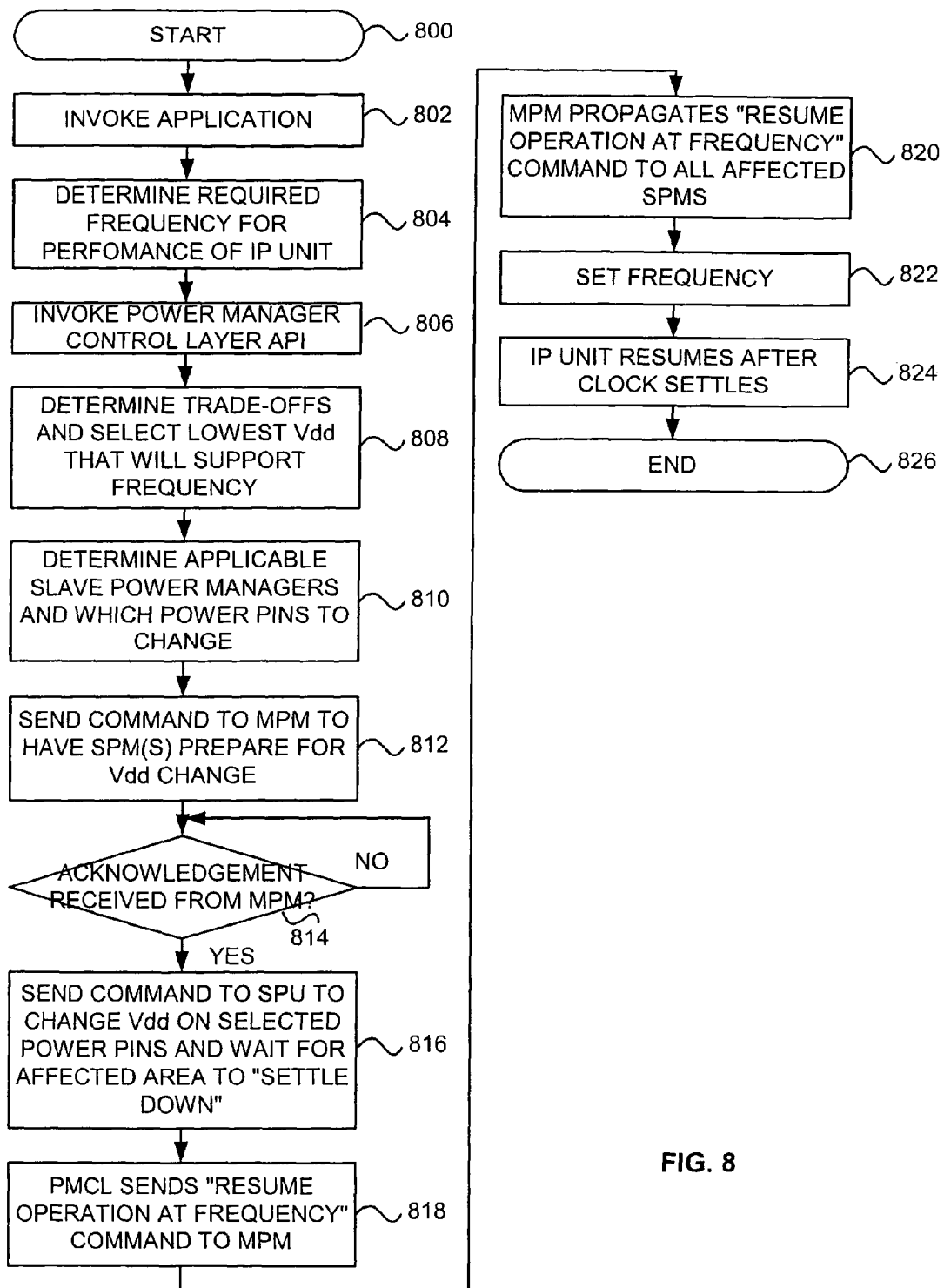


FIG. 8

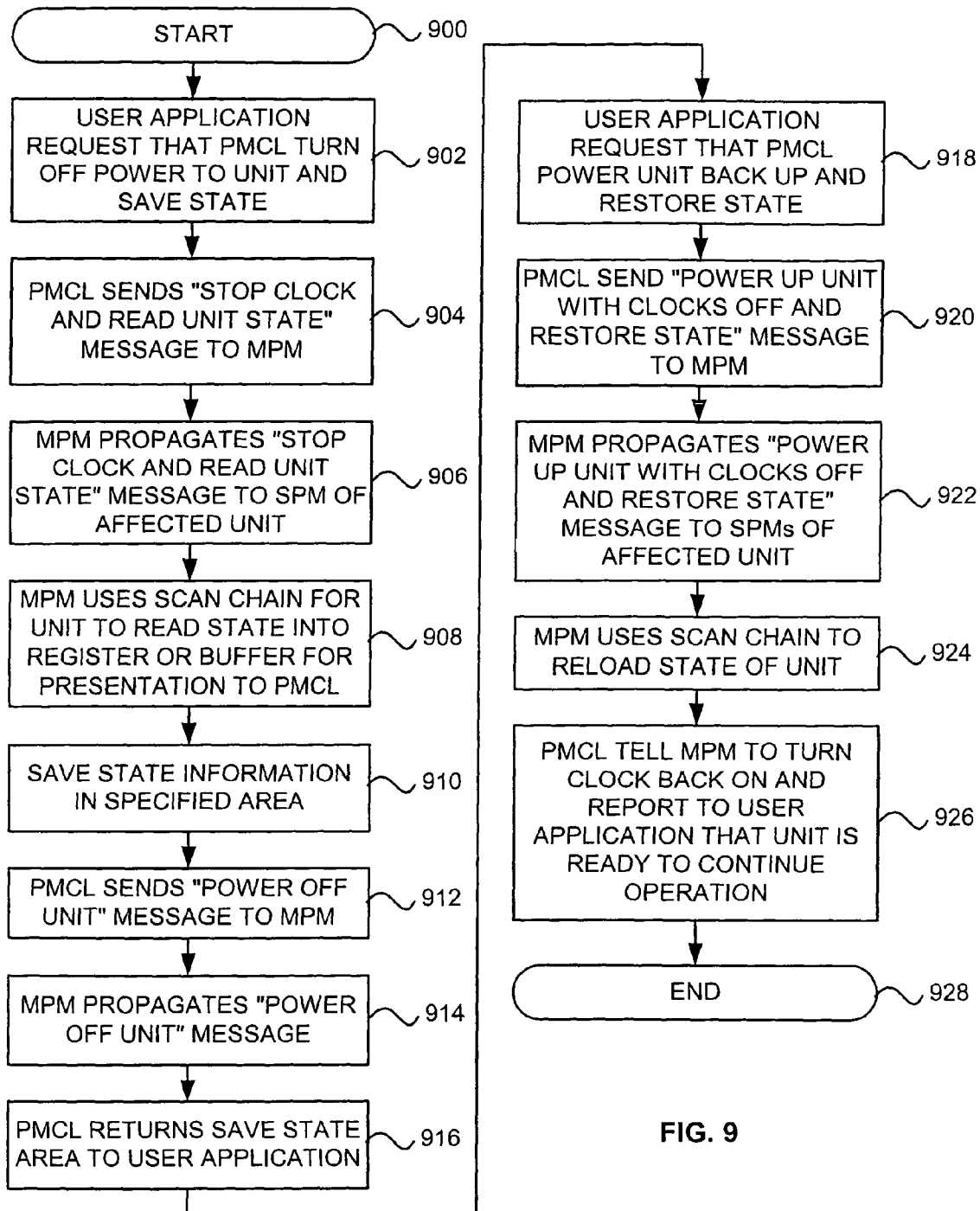


FIG. 9

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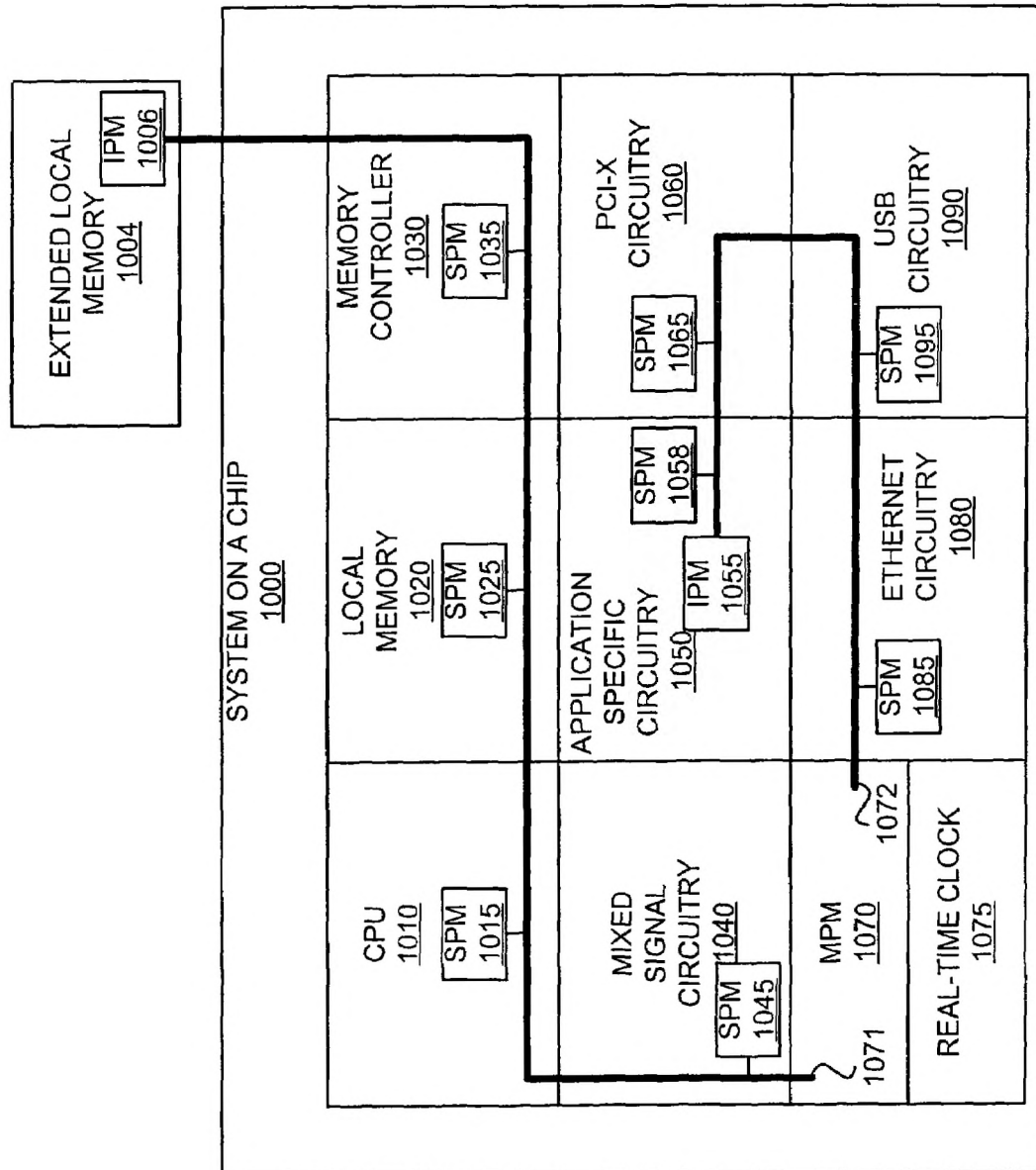


FIG. 10

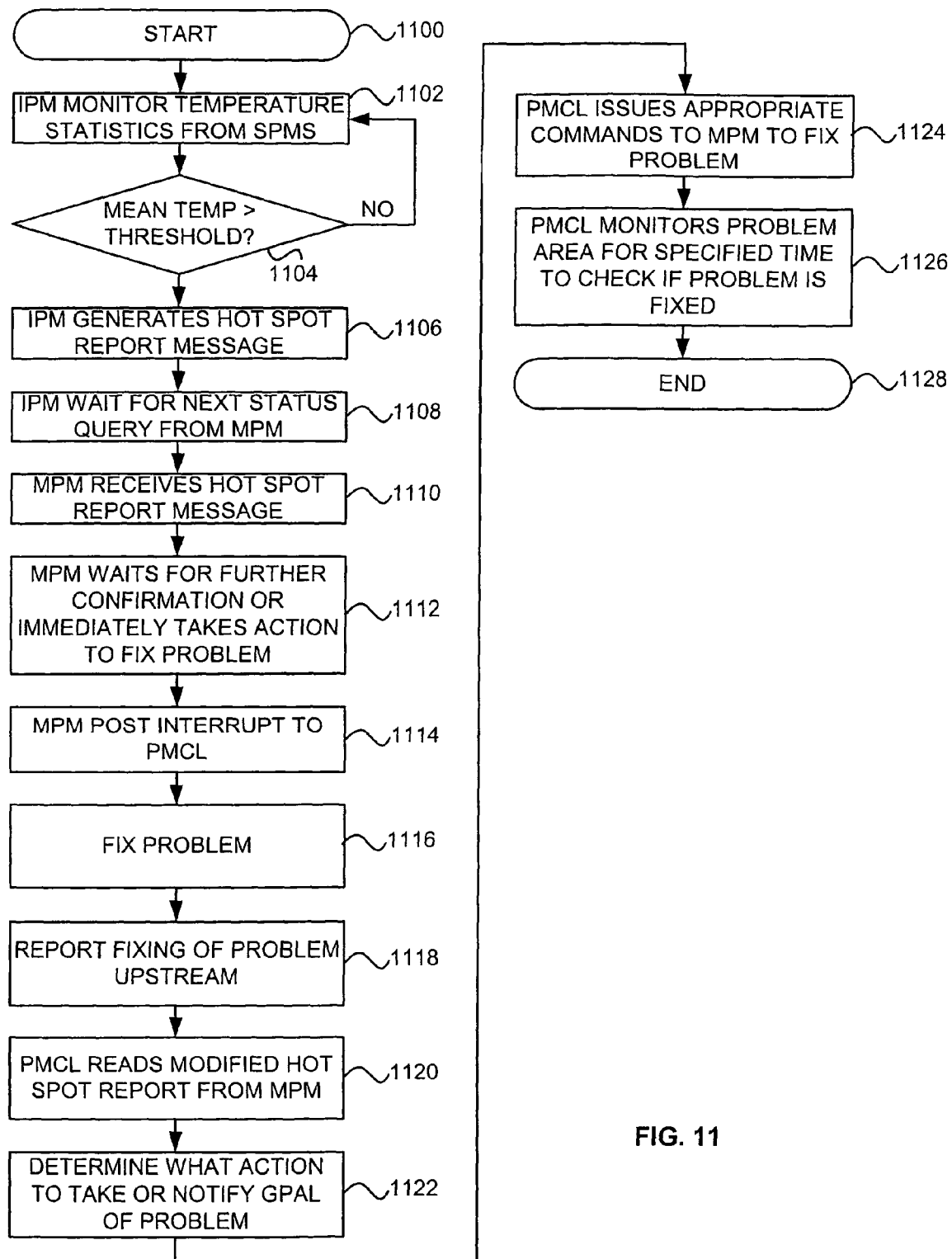


FIG. 11

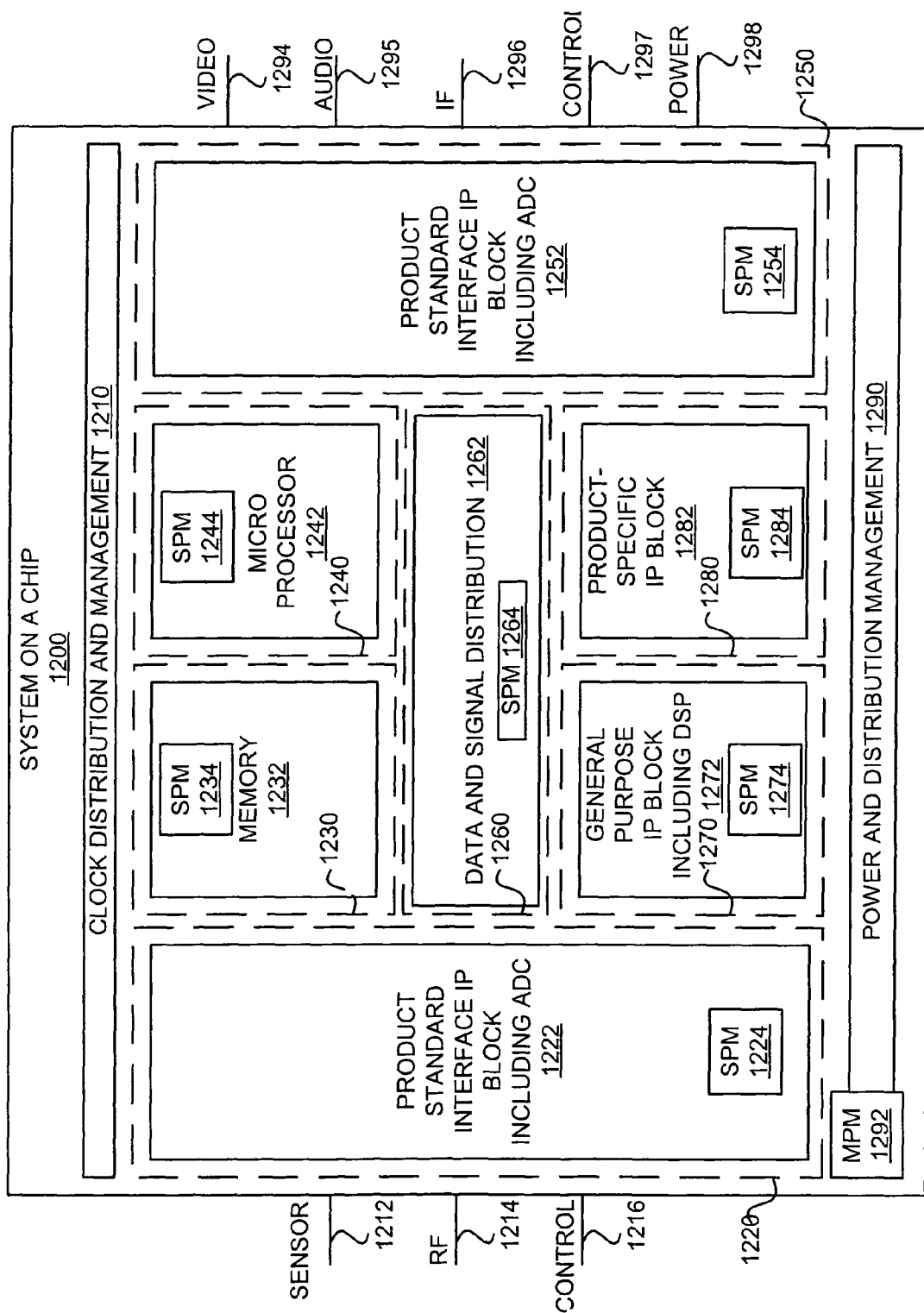


FIG. 12

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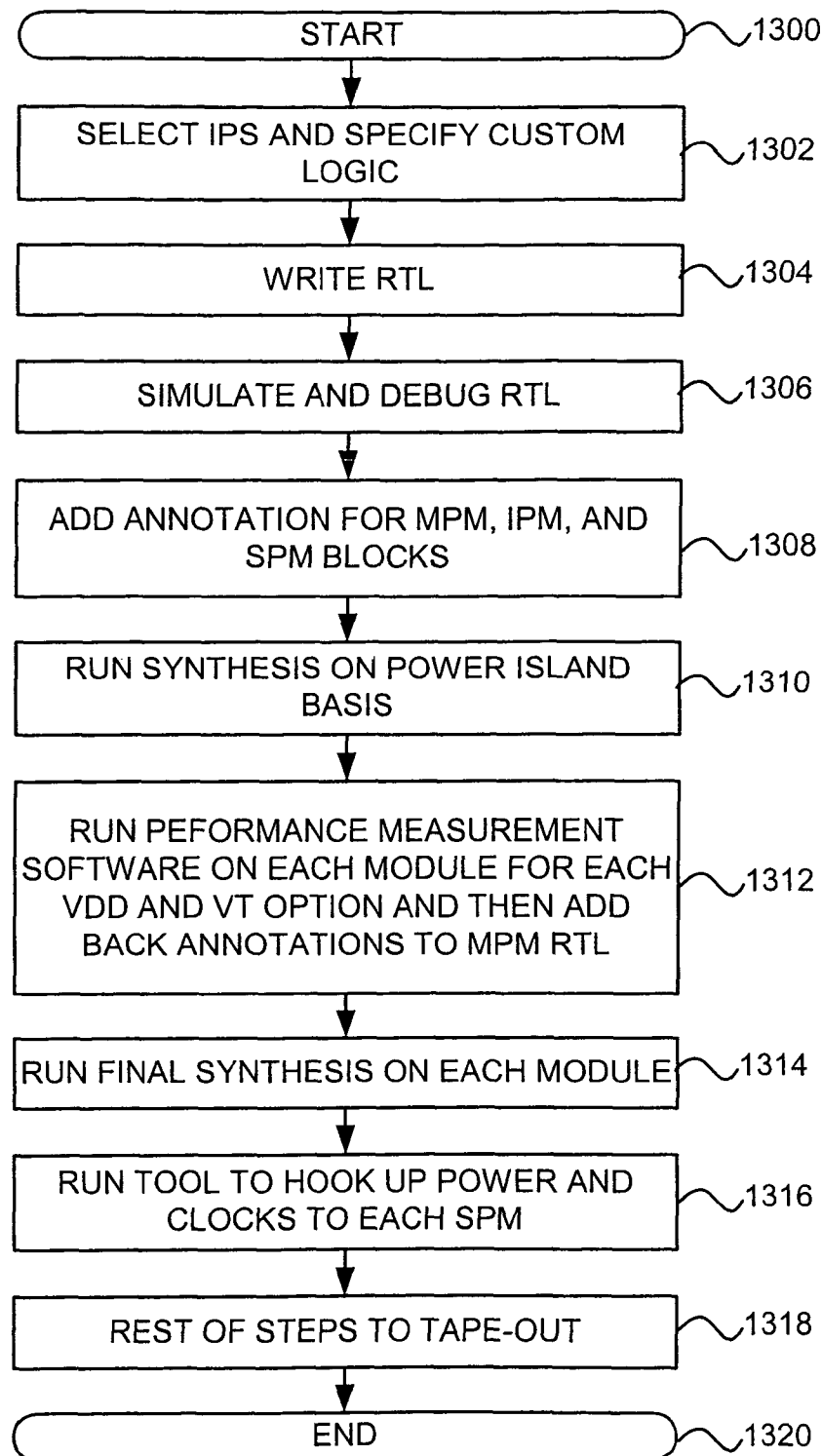


FIG. 13

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**POWER MANAGERS FOR AN INTEGRATED
CIRCUIT****CROSS-REFERENCE TO RELATED
APPLICATIONS**

This application is a continuation of U.S. application Ser. No. 12/176,645 filed on Jul. 21, 2008 entitled "Power Managers for an Integrated Circuit" and which is a continuation of U.S. application Ser. No. 11/336,097 filed on Jan. 20, 2006 entitled "Power Managers for an Integrated Circuit" and which issued on Aug. 19, 2008 as U.S. Pat. No. 7,415,680 which is a continuation of U.S. application Ser. No. 10/840,893 filed on May 7, 2004 and entitled "Managing Power on Integrated Circuits Using Power Islands" and which issued on May 23, 2006 as U.S. Pat. No. 7,051,306 which claims the benefit of U.S. Provisional Application Ser. No. 60/468,742 titled "System and Method for Managing Power in Integrated Circuits," filed May 7, 2003, which are each hereby incorporated by reference.

BACKGROUND**1. Field of the Invention**

The present invention relates generally to integrated circuits, and more particularly to managing power on integrated circuits using power islands.

2. Description of the Prior Art

One design goal for integrated circuits is to reduce power consumption. Devices with batteries such as cell phones and laptops especially need a reduction in power consumption in the integrated circuit to extend the charge of the battery. Additionally, a reduction in power consumption prevents overheating and lowers the heat dissipation of the integrated circuit, which in some cases, eliminates or simplifies the heat sinks and/or fans for the integrated circuit.

Some integrated circuits are designed using building blocks of library cells. These library cells are blocks of circuitry performing a function. Some examples of library cells are NAND gates, multiplexers, decoders, comparators, and memory.

In a "full-custom" flow, the integrated circuit is designed at the lowest level such as at the individual transistors, capacitors, and resistors level. The "full-custom" flow may use library cells that are internally developed. The integrated circuit can have optimal performance because the integrated circuit is designed in great detail at the lowest level. However, some problems with the "full-custom" flow are the long time and expensive costs associated with designing at such a detailed level. Furthermore, the "full-custom" flow is cumbersome because the design is at the lowest level.

In a "standard-cell" flow, the integrated circuit is designed using library cells acquired from a third party or other outside source. These library cells are standardized at the logic or function level. The design time for the standard-cell flow is reduced because the library cells are already pre-designed and pre-tested.

In one example for designing an integrated circuit, the library cells are selected, and the custom logic is specified to build the integrated circuit. The register transfer level (RTL) for the integrated circuit is then written for simulation and debugging. After simulation and debugging, the synthesis is run for the integrated circuit. Performance measurement software is executed to determine performance of the integrated circuit. The final synthesis of the integrated circuit can then be run based on the optimal performance of the integrated circuit.

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One problem with many integrated circuits is that power consumption is not efficiently utilized. For example, the entire integrated circuit may operate at a maximum frequency just to support an application needing that maximum frequency, while other portions of the integrated circuit can operate at a lower frequency. In another example, inactive circuitry within the integrated circuit consumes power and increases the likelihood of leakage. Inefficient power consumption may also adversely affect performance of the integrated circuit.

With the growing complexity of integrated circuits, the reduction of power consumption is even more important when the integrated circuit employs more functionality. One example of an integrated circuit is a system-on-a-chip that includes a microprocessor, memory, I/O interfaces, and an analog-to-digital converter all in a single chip. With many different types of functionality employed within a single chip, the system-on-a-chip consumes even more power than single function integrated circuits.

Some prior integrated circuits have employed voltage islands or multiple clocks to lower power consumption. One problem with these integrated circuits is that the voltages in the power island and the frequencies of the multiple clocks are static. The voltages and the frequencies do not dynamically change based on the needs and operation of the integrated circuit.

SUMMARY OF THE INVENTION

The invention addresses the above problems by providing power managers for an integrated circuit. A system for an integrated circuit comprising a plurality of power islands includes a first power manager and a second power manager. The first power manager manages a first power consumption for the integrated circuit based on needs and operation of the integrated circuit. The second power manager communicates with the first power manager and manages a second power consumption for one of the power islands.

The first power manager may determine power trade offs between the power islands. The second power manager may determine status information about the one of the power islands and may transmit the status information to the first power manager. The first power manager may receive the status information and may manage the first power consumption for the integrated circuit using the status information. The first power manager may determine status information about the integrated circuit and may transmit the status information to power interface software. The first power manager may receive a message from power interface software to change the first power consumption for the integrated circuit. The first power manager may transmit a message to the second power manager and the second power manager may receive and process the message to change the second power consumption for the one of the power islands. The second power manager may register capabilities of the second power manager with the first power manager.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a system for managing power in an integrated circuit in an exemplary implementation of the invention;

FIG. 2 is a diagram of a system for managing power in an integrated circuit in an exemplary implementation of the invention;

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FIG. 3 is an illustration for low leakage circuitry for a low power standard cell logic block in an exemplary implementation of the invention;

FIG. 4 is a diagram of a power island in an exemplary implementation of the invention;

FIG. 5 is a flowchart from an application request to a slave power manager action in an exemplary implementation of the invention;

FIG. 6 is an illustration of internal circuitry for a smart power unit in an exemplary implementation of the invention;

FIG. 7 is an illustration of external circuitry for a smart power unit in an exemplary implementation of the invention;

FIG. 8 is a flowchart from an application request to a smart power unit action in an exemplary implementation of the invention;

FIG. 9 is a flowchart for saving an IP unit's state prior to powering down and restoring the IP unit's state when powering up in an exemplary implementation of the invention;

FIG. 10 is diagram of a system on a chip and an extended local memory in an exemplary implementation of the invention;

FIG. 11 is a flowchart for generating a "hot spot" report from an intermediate power manager to a power management control layer in an exemplary implementation of the invention.

FIG. 12 is a diagram of a system on a chip in an exemplary implementation of the invention; and

FIG. 13 is a flowchart for building a chip with power islands in an exemplary implementation of the invention.

DETAILED DESCRIPTION OF THE INVENTION

As shown in the exemplary drawings wherein like reference numerals indicate like or corresponding elements among the figures, exemplary embodiments of a system and method according to the present invention are described below in detail. It is to be understood, however, that the present invention may be embodied in various forms. Therefore, specific details disclosed herein are not to be interpreted as limiting, but rather as a basis for the claims and as a representative basis for teaching one skilled in the art to employ the present invention in virtually any appropriately detailed system, structure, method, process or manner.

FIG. 1 depicts a block diagram of a system 100 for managing power in an integrated circuit 110 in an exemplary implementation of the invention. The system 100 includes an integrated circuit 110 and a power manager 120. The integrated circuit 110 is any electronic device that is instantiated into silicon and/or related manufacturing materials. One example of the integrated circuit 110 is a system-on-a-chip. The integrated circuit 110 includes multiple IP units, which are blocks of circuitry performing specific functions.

The integrated circuit 110 includes four power islands 112, 114, 116, and 118. FIG. 1 only depicts four power islands 112, 114, 116, and 118 for the sake of simplicity. Other embodiments of the integrated circuit 110 include a plurality of power islands 112, 114, 116, and 118. The power islands 112, 114, 116, and 118 are coupled to a bus 125.

A power island 112, 114, 116, and 118 is any section, delineation, partition, or division of the integrated circuit 110 where power consumption is controlled within the section, delineation, partition, or division. In some embodiments, the power islands 112, 114, 116, and 118 are delineated based on geographic factors of the integrated circuit 110. In some embodiments, the power islands 112, 114, 116, and 118 are delineated based on functional IP units of the integrated circuit 110. In one example depicted in FIG. 10, power islands

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are delineated by memory, a microprocessor, and separate IP blocks. In some embodiments, the power islands 112, 114, 116, and 118 are asynchronous or synchronous to each other. In some embodiments, the power islands 112, 114, 116, and 118 comprise sub-islands of power to provide further specificity in controlling power in the integrated circuit 110. In some embodiments, each of the power islands 112, 114, 116, and 118 supports multiple clock domains with its own control. In some embodiments, the clocks within the power islands 112, 114, 116, and 118 are variable.

In some embodiments, each of the power islands 112, 114, 116, and 118 includes power control circuitry. Power control circuitry is any circuitry configured to control power within one of the power islands 112, 114, 116, and 118. Some examples of power control circuitry include circuitry for level shifting, signal isolation, Vdd multiplexing, clock multiplexing, and dynamic back bias. In some embodiments, the power control circuitry is included in a standard cell library for standard cell design of the integrated circuit 110.

The power manager 120 is also coupled to the bus 125. One example of the bus 125 is a power command bus described in further detail below in FIG. 10. Other embodiments of the system 100 include numerous variations in which the power manager 120 and the power islands 112, 114, 116, and 118 are interconnected. The power manager 120 is any circuitry, device, or system configured to (1) determine a target power level for one of the power islands 112, 114, 116, and 118 where power consumption is independently controlled within each of the power islands 112, 114, 116, and 118, (2) determine action to change a consumption power level of the one of the power islands 112, 114, 116, and 118 to the target power level, and (3) perform the action to change the consumption power level of the one of the power islands 112, 114, 116, and 118 to the target power level. The power manager 120 can dynamically change the power consumption of the power islands 112, 114, 116, and 118 based on the needs and operation of the integrated circuit 110. The target power level is a desired, calculated, or specified power consumption of the power islands 112, 114, 116, and 118. Some examples of the power manager 120 are the slave power manager (SPM), the intermediate power manager (IPM), and the master power manager (MPM), which are described in further detail below. The power manager 120 may be a hierarchy or group of power managers 120. Although FIG. 1 depicts the power manager 120 as being located outside the integrated circuit 110, other embodiments may have the power manager 120 located in the integrated circuit 110. In other embodiments, the power manager 120 may be distributed among multiple power managers that are on or off the integrated circuit 110 or integrated with a CPU. The action is any instruction, message, process, function, signal, or variable that controls power consumption in the power island 112, 114, 116, and 118. Some examples of actions are clock gating and dynamic clock selection. Another example of an action is modifying a clock frequency of one of the power islands 112, 114, 116, and 118. Another example of an action is to modify voltage of one of the power islands 112, 114, 116, and 118 such as dynamic voltage source, Vdd, selection. Another example of an action is to control dynamic leakage by controlling variable Vt transistors.

FIG. 2 depicts a diagram of a system 200 for managing power in an integrated circuit 250 in an exemplary implementation of the invention. The system 200 includes an embedded firmware stack 210 and an integrated circuit 250. The embedded firmware stack 210 includes software layers that run on a central processing unit (CPU). In some embodiments, the embedded firmware stack 210 may include an application

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layer **212**, an operating system (OS) sub-system **216**, a power management control layer (PMCL) **218**, a real-time operating system (RTOS) **220**, I/O drivers **222**, and power manager (PM) firmware **224** for the MPM, IPM and/or SPM.

The integrated circuit **250** includes a power island **260**, a power island **270**, and a MPM **280**. The power island **260** includes a low power standard cell logic block **262** and a SPM **264**. The power island **270** includes a low power memory block **272** and a SPM **274**. The low power standard cell logic block **262** and the low power memory block are coupled to an interface **265**. The MPM **280** is coupled to the PMCL **218**, the SPM **264**, and the SPM **274**.

In some embodiments, the application layer **212** includes a global power application layer (GPAL) **214**. This GPAL **214** may be useful for more complex applications. If the GPAL **214** is present, then all calls to the PMCL **218** application program interfaces (API) are first directed to the GPAL **214**. Both the GPAL **214** and the PMCL **218** provide power management for the integrated circuit **250**. In some embodiments, the GPAL **214** and/or the PMCL **218** monitor what load is on each power island **260** and **270**. Also, the GPAL **214** and/or the PMCL **218** may build a history of power levels on the power island **260** and **270** and store the history data in a database. The GPAL **214** and the PMCL **218** may also provide data for on-demand resources interested in the power levels of the power islands **260** and **270**.

In some embodiments when the GPAL **214** is present, the GPAL **214** provides guidance to the PMCL **218** in making local decisions for power management of the integrated circuit **250**. In some embodiments, the GPAL **214** and the PMCL **218** include complex algorithms for a static schedule. The GPAL **214** and the PMCL **218** provide the facility for use code to interact and control power behavior and parameters including providing a database and statistics.

The PMCL **218** also collects information from the MPM **280** and provides commands to the MPM **280** for possible IPMs, SPMs **264** and **274**, and the power islands **260** and **270**. Some of the commands may be to power on/off, change the power level, or change the frequency of the power islands **260** and **270**. In some embodiments with a smart power unit (SPU) **290**, the GPAL **214** and the PMCL **218** are responsible for communication with the SPU **290** to implement a power policy and collect information on the actual power supply. The SPU **290** is described in further detail below in FIGS. 6-8. In some embodiments, the GPAL **214** and the PMCL **218** provides sockets for existing power management techniques.

The power manager firmware **224** is firmware executed by the master power manager **280**, the intermediate power manager, and the slave power managers **264** and **274**.

The MPM **280** is any circuitry configured to control the “global” power behavior of the entire integrated circuit **250**. In some embodiments, there are multiple MPMs **280** that control the power behavior of the entire integrated circuit **250**. In some embodiments, the MPM **280** communicates with existing IPMs and SPMs **264** and **274** to control power within the power islands **260** and **270**. The MPM **280** may receive status information about the power islands **260** and **270** from the SPMs **264** and **274** and the IPMs. The MPM **280** may also determine power trade-offs between the IPMs and the SPMs **264** and **274**.

The MPM **280** may also provide a main interface to the PMCL **218** firmware. In some embodiments, the MPM **280** communicates with the PMCL **218** to accept commands (e.g., memory mapped commands) and provide status information, about the power within the integrated circuit **250**. In some embodiments, the MPM **280** communicates with the PMCL **218** through the main bus for the integrated circuit **250**. The

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MPM **280** may also register each of the SPMs **264** and **274** and IPMs and capabilities with the PMCL **218**. Some operations of the MPM **280** are described in further detail below in FIGS. 5, 8, 9, and 11. In some embodiments, the MPM **280** reads and writes scan chains for state save and restore along with the local logic analyzer ability.

Some embodiments may include an IPM (not shown) that coordinates SPMs **264** and **274** on behalf of the MPM **280**. In some embodiments, the IPM controls and coordinates power behavior on portions of the area controlled by the MPM **280**. In some embodiments, the IPM controls the SPMs **264** and **274** that are on a separate chip from the MPM **280**.

The SPM **264** is any circuitry configured to control power within a power island **264** in the integrated circuit **250**. One example of the SPM **264** is an IP block that controls power within a power island **264** in the integrated circuit **250**. The SPM **264** may include signal buffering, level shifting, and signal isolation. In some embodiments, the SPM **264** is integrated into scan chains to provide easier implementation and integration. Also, in some embodiments, the SPM **264** has a very small “footprint” with a low gate count and low power. In some embodiments, the SPM **264** comprises a command interface to communicate status information, service requests, and commands. Some of the commands are load, sleep, and idle. The SPM **264** may also recognize its own address to allow for multi-drop bussing.

In some embodiments, the SPM **264** has registration capabilities. For registration at power-up, the SPM **264** uses call-back registration that is typically used for off chip SPMs and IPMs. For static registration when the integrated circuit is generated for on chip SPMs, the SPM **264** registers what the SPM **264** can do, what the IPM can do, and the type of commands that the SPM **264** or IPM can service. The SPM **264** may also have save and restore functions for power off periods. The SPM **264** may have watch-dog timer(s). In some embodiments, the SPM **264** has a debug interface coordination to the power island **260**. The SPM **264** may also monitor local state and collect information for components within the power island **260**. The SPM **264** may also locally control V_{dd}, clocks for frequency selection, and dynamic back biasing. The description for the SPM **264** also applies to the SPM **274** for the power island **270**.

In some embodiments, the SPM **264** checks whether an event occurs when the collected information from the power island **260** crosses a threshold or exceeds a range. In some embodiments, the SPM **264**, IPMs, or the MPM **280** monitors power consumption levels of the power island **260** to check whether the power consumption levels cross a threshold level or exceed a range. A power consumption level is any information, data, or statistic that indicate the power consumed in a power island **260**. Some examples of power consumption levels are temperature and power. The threshold or range may be programmable. The SPM **264** may report the event asynchronously, or another element such as the MPM **280** may solicit whether an event has occurred. The event may also be a multi-level test such as the conditions occur at a greater than a given, programmable frequency or exceed a given, programmable duration.

In some embodiments, the low power standard cell logic block **262** one example of a standard cell library that may be included in the power island **260**. In some embodiments, the standard cell library is optimized for lower power. The standard cell library may be characterized over a range of operating voltages. In some embodiments, the standard cell library includes synchronous circuits and/or asynchronous circuits. In some embodiments, the standard cell library includes static circuits and/or encapsulated, dynamic logic

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circuits. The standard cell library may also include multiple voltage domain interface circuits such as level shifters and signal isolation circuits. The standard cell library may also have a multi-threshold design and characterization such as standard Vt, high Vt, low Vt, and variable Vt circuits. The standard cell library may also include data retention (shadow) circuits and anti-glitch circuits. The standard cell library may also include low leakage “sleep” circuits. FIG. 3 depicts an illustration of low leakage circuitry 300 for the low power standard cell logic block 262 in an exemplary implementation of the invention.

FIG. 4 depicts a diagram of the power island 270 in an exemplary implementation of the invention. The power island 270 includes a low power memory block 272 and the SPM 274. The low power memory block 272 includes banked architectures 410, 420, 430, and 440 for memories and sleep, power down circuitry 450. In some embodiments, the memory in the power island 270 is RAM and/or ROM. Some examples of the RAM are the SRAM compilers such as single-port, 2-port, and dual-port. Some examples of the ROM are ROM compilers. Some memories in the power island 270 are optimized for low power such as the low power memory block 272. In one embodiment, the low power memory block 272 includes multiple bank architectures via the compiler such as banked architectures 410, 420, 430, and 440. The memories in the power island 270 may also include sleep, power down circuitry 450 for low power modes such as sleep, nap, and full power down. The memories in the power island 270 may also include programmable read/write ports. The memories in the power island 270 may also be an asynchronous and/or synchronous design.

In some embodiments, the system 200 also includes a smart power unit (SPU) 290. In some embodiments, the SPU 290 is off-chip to the integrated circuit 250. The SPU 290 is an external unit configured to control power and clock distribution to the integrated circuit. The circuitry of the SPU is described in further detail below in FIGS. 7 and 8.

FIG. 5 depicts a flowchart from an application request to an SPM action in an exemplary implementation of the invention. FIG. 5 begins in step 500. In step 502, an application is invoked such as playing a movie. In step 504, the application determines the required frequency for performance of an IP unit. For example, the application determines a specified frequency in MHz for IP unit for an MPEG decoder. In some embodiments, when the IP unit is totally asynchronous, the required frequency will be an artificial measure of performance. In some embodiments that have multiple clocks involved, the minimum performance for each clock is specified.

In step 506, the application invokes the PMCL 218 API call. One example of this call is “Set_Rate (unit Y, N MHz, degree of dynamic power management (DPM) allowed, DPM threshold, other information to allow DPM trade-offs, starting back bias for SPMs with dynamic bias, wait for power up flag).” In this example, the other information could be “no power off, use high Vt and clocks off instead” and “major waits are about 10 us, with a 400 ns threshold.” In some embodiments with multiple clocks, the PMCL 218 API call allows the application to specify all required frequencies.

The PMCL 218 determines possible trade-offs available for the unit and selects a frequency rate, Vdd, and Vt if applicable for the unit that best meets the given requirements in step 508 and determines the applicable SPMs 264 and 274 in step 510. In some embodiments, the MPM 280 or IPM performs steps 508 and 510. In some embodiments for multiple clocks, the Vdd and Vt specified would allow for all specified clocks to meet or exceed their required frequencies.

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In step 512, the PMCL 218 then writes the desired setting for the SPMs 264 and 274 to the MPM 280 (or IPM). In step 514, the MPM 280 (or IPM) converts the request into one or more commands for the SPMs 264 and 274 (or IPM) associated with the unit.

In step 516, if the application sets the wait for power up flag, the PMCL 218 then waits until the IP unit is fully powered up before returning from the call. Otherwise, the call returns as soon as the command is acknowledged, with status of 0 for okay, 1 for fast power-up, 2 for slow power-up, or 3+ for error conditions. The powered up state is when the unit is at the desired Vdd for the requested frequency, and not just that the unit is turned on.

In step 518, the MPM 280 (or IPM) sends the requests to the appropriate targets. In step 520, the MPM 280 waits for the receipt of the acknowledgements that indicate message received and executed or execution has begun. A NACK or negative acknowledgement may also be returned from the SPM 264 and 274.

In step 522, the SPM 264 receives the commands and performs the actions. Steps 524-528 are possible actions that the SPM 264 may perform. In step 524, the SPM 264 switches the Vdd mux. In step 526, the SPM 264 switches a clock mux. In some embodiments when the voltage goes down, step 526 is performed before step 524. In step 528, the SPM 264 changes the Vt on the associated transistors. After the SPM 264 performs the actions, the SPM 264 returns a status message upstream indicating acknowledgement or negative acknowledgement in step 530. FIG. 5 ends in step 532.

FIG. 6 depicts an illustration of internal circuitry 600 for an SPU 290 in an exemplary implementation of the invention. In this embodiment, the internal circuitry 600 for the SPU 290 is internal to the integrated circuit 250 of FIG. 2. The internal circuitry 600 includes an external voltage 610, a dropout voltage regulator 620, a dropout voltage regulator 630, a logic block 640, and a logic block 650.

FIG. 7 depicts an illustration of external circuitry 700 for an SPU 290 in an exemplary implementation of the invention. In this embodiment, the external circuitry 700 for the SPU 290 is external to the integrated circuit 250 of FIG. 2. The internal circuitry 700 includes an external voltage 710, a power supply pin 720, a power supply pin 730, a power supply pin 740, a logic block 750, a logic block 760, and a logic block 770. The external circuitry 700 for the SPU 290 provides a DC/DC conversion. The DC/DC conversion provides multiple independent power supply pins 720, 730, and 740. The power supply pins 720, 730, and 740 have a variable voltage supply on each separate power pin. Also, in some embodiments, the variable voltage is within a range and in steps. In some embodiments, the PMCL 218 controls the voltage to power supply pins 720, 730, and 740.

FIG. 8 depicts a flowchart from an application request to an SPU action in an exemplary implementation of the invention. FIG. 8 begins in step 800. In step 802, an application is invoked. In step 804, the application determines the required frequency for performance of an IP unit. For example, the application determines a specified frequency in MHz for IP unit for an MPEG decoder.

In step 806, the application invokes the PMCL 218 API call. One example of this call is “Set_Rate (unit Y, N MHz, degree of dynamic power management (DPM) allowed, DPM threshold, other information to allow DPM trade-offs, starting back bias for SPMs with dynamic bias, wait for power up flag).” In this example, the other information could be “no power off, use high Vt and clocks off instead” and “major waits are about 10 us, with a 400 ns threshold.”

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The PMCL 218 determines possible trade-offs available for the unit and selects a the lowest possible Vdd that will support the requested frequency in step 808 and determines the SPMs 264 and 274 that will be affected and which power PINs to change in step 810.

In step 812, the PMCL 218 sends a command to the MPM 280 to have the SPMs 264 and 274 (and IPM) to prepare for a Vdd change. In step 814, the PMCL 218 waits for the acknowledgement from the MPM 280. In step 816, the PMCL 218 sends a command to the SPU 290 to change the Vdd on the selected power pins and waits for the affected area to “settle down.” In step 818, the PMCL 218 then sends a “resume operation at a specified frequency” command to the MPM 280. In step 820, the MPM 280 propagates the resume command to all affected SPMs 264 and 274 (and IPMs). In step 822, one of the power managers (i.e. MPM 280, IPM, or SPMs 264 and 274) sets the specified frequency. In step 824, the IP unit operation resumes after the clock has settled. FIG. 8 ends in step 826. In some embodiments, the user application has the option of waiting for the entire operation to finish or to continue and either query the PMCL 218 as to the progress of the operation or wait for a “finished” interrupt from the PMCL 218.

FIG. 9 depicts a flowchart for saving an IP unit’s state prior to powering down and restoring the IP unit’s state when powering up in an exemplary implementation of the invention. FIG. 9 begins in step 900. In step 902, the user application requests that the PMCL 218 power off an IP unit and wants to save the IP unit’s state. In some embodiments, the reconfiguration of the IP unit takes a long time. The request in step 902 may be accompanied by the address of an area to which the state should be saved.

In step 904, the PMCL 218 sends a “stop clock and read IP unit state” message to the MPM 280. The MPM 280 then propagates the “stop clock and read IP unit state” message to the SPMs 264 and 274 of the affected unit in step 906. In step 908, the MPM 280 uses the scan chain for the IP unit to read the state into a register or buffer for presentation to the PMCL 218. In step 910, if the PMCL 218 provided the MPM 280 with the address of the save area, the MPM 280 saves the state information directly in the specified area. In step 912, after all of the IP units’ state has been saved, the PMCL 218 sends a “power off IP unit” message to the MPM 280. In step 914, the MPM 280 then propagates out the “power off IP unit” message. In step 916, the PMCL 218 returns the save state area to the user application. The save state area contains the state of the unit.

At a later time, in step 918, the user application requests that the PMCL 218 power the IP unit-back up and restore the state of the IP unit. In some embodiments, the user application request includes the address of the area to which the state was saved. In step 920, the PMCL 218 sends a “power up IP unit with clocks off and restore state” message to the MPM 280. In step 922, the MPM 280 propagates the “power up IP unit with clocks off and restore state” message to the SPMs 264 and 274 of the affected IP unit. In step 924, after the IP unit is powered up, the MPM 280 uses the scan chain to reload the unit’s state. In some embodiments, the reloading of the unit’s state originates directly from the save area or from information passed to the MPM 280 from the PMCL 218. In step 926, the PMCL 218 sends a message to the MPM 280 to turn clock back on and report to user application that the IP unit is ready to continue operations. FIG. 9 ends in step 928.

In some embodiments, the same functionality of FIG. 9 can be used to implement an internal “logic analyzer” function, in which the IP unit in question would not be powered down after being read. If the associated SPMs 264 and 274 of the IP

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unit have the ability to single- or multi-step the clock, the local scan testing is performed by having the SPMs 264 and 274 “signal isolate” the IP unit. Then, use of a combination of the ability of single- or multi-step the clock and the ability to use the scan chain can read/write the IP unit’s internal state.

FIG. 10 depicts a diagram of a system-on-a-chip (SOC) 1000 and an extended local memory 1004 in an exemplary implementation of the invention. The SOC 1000 is one example of the integrated circuit 250 and communicates with the embedded firmware stack 210 in FIG. 2 as described above. The SOC 1000 includes a CPU 1010, a local memory 1020, a memory controller 1030, a mixed signal circuitry 1040, an application specific circuitry 1050, a PCI-X circuitry 1060, a MPM 1070, a real-time clock (RTC) 1075, an Ethernet circuitry 1080, and a USB circuitry 1090. The CPU 1010, the local memory 1020, the memory controller 1030, the mixed signal circuitry 1040, the application specific circuitry 1050, the PCI-X circuitry 1060, the Ethernet circuitry 1080, and the USB circuitry 1090 are all power islands in which power is controlled within the power islands by power managers. In this embodiment, the power islands are delineated by the functionality of a part of the SOC 1000.

The extended local memory 1004 includes an IPM 1006 that is coupled to the bus 1071. The CPU 1010 includes an SPM 1015 that is coupled to the bus 1071. The local memory 1020 includes an SPM 1025 that is also coupled to the bus 1071. The memory controller 1030 comprises an SPM 1035 that is coupled to the bus 1071. The mixed signal circuitry 1040 includes an SPM 1045 that is coupled to the bus 1071. The application specific circuitry 1050 includes an IPM 1055 and an SPM 1058 that are both coupled to the bus 1072. The PCI-X circuitry 1060 includes an SPM 1065 that is coupled to the bus 1072. The MPM 1070 is coupled to the bus 1071 and the bus 1072. The MPM 1070 is one example of the MPM 280 as described above. The Ethernet circuitry 1080 includes an SPM 1085 that is coupled to the bus 1072. The USB circuitry 1090 includes an SPM 1095 that is coupled to the bus 1072.

In this embodiment, power command buses comprise the bus 1071 and the bus 1072. The bus 1071 and 1072 are simple multi-drop serial buses that may cross chip boundaries and interconnect power managers. The power command bus may be a combination of serial busses, such as the bus 1071 and the bus 1072, with one per region of the chip and then multi-drop within the region. In other embodiments, the power command bus includes a parallel bus or a combination of serial and parallel busses. In some embodiments, the power command bus is the system bus. The power command bus may contain messages with at least a unit ID with the associated payload. For a fixed point to point bus, the message does not need a unit ID only the payload.

In some embodiments, the power command bus uses an error detection scheme such as parity, ECC, or a redundant code. In some embodiments, the power command bus is a low performance bus that does not interfere with the integrated circuit design and is not visible to the user. In some embodiments, the communication between the PMCL 218 and the MPM 1070 is memory mapped and based on the main bus such as an AHB for an SOC 1000.

Some embodiments may include a separate bus for reporting status information between the power managers. In one example, this separate bus provides asynchronous “Alert” type status messages from SPMs to the MPM.

There can be various message formats for the power command bus. In one example for a basic format, the message format includes a start of message indicator, a power manager address, type code, basic command, and an end of message indicator. In one example for an extended format, the message

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format includes the basic format, an additional length, and additional information. In one example for a response message format, the message format includes a start of message reply indicator, a power manager address, a 3b ACK or NAK or return status (implied ACK), a payload length for return status messages, a payload for return status messages, a reason code for NAK, and an end of message indicator.

In some embodiments, the SPM 1015 or the IPM 1006 times out on replying to a command, and the MPM 1070 reissues the command a programmable number of times. If the SPM 1015 or the IPM 1006 still fails, the MPM 1070 marks the SPM 1015 or the IPM 1006 as unusable and reports back the failure to the PMCL 218. In one embodiment, the PMCL 218 has the MPM 1070 reinitialize the failing SPM 1015 or the IPM 1006 via the scan system and then retries sending the message. Other conditions such as invalid responses to commands or invalid status reports are also handled by the re-initialization. In some embodiments, the state of the failing SPM 1015 or the IPM 1006 may be read out and saved for later analysis.

FIG. 11 depicts a flowchart for generating a “hot spot” report from an IPM 1055 to the PMCL 218 in an exemplary implementation of the invention. FIG. 11 begins in step 1100. In step 1102, the IPM 1055 monitors the temperature statistics of the SPMs. In step 1104, the IPM 1055 checks whether the mean temperature has exceeded a predetermined and programmed threshold. If the mean temperature has not exceeded the threshold, the IPM 1055 returns to step 1102 to keep monitoring. If the mean temperature has exceeded the threshold, the IPM 1055 then generates a problem (“hot spot”) report message in step 1106. In step 1108, the IPM 1055 waits for the next status query the MPM 1070. In some embodiments, a logically separate bus is provided for asynchronous status reports to the MPM 280.

In step 1110, the MPM 1070 receives the hot spot report message. In step 1112, the MPM 1070 either waits for further confirmation (i.e. see that the “hot spot” last pasts a predetermined threshold) or immediately takes action to fix the problem depending on the internal logic of the MPM 1070. In some embodiments, in step 1114, the MPM 1070 takes action by posting an interrupt to the PMCL 280 that it needs attention. In other embodiments, if the PMCL 280 queries the MPM 1070 often enough, then the interrupt is not needed. In step 1116, the MPM 1070 (or IPM) fixes the problem by making a local trade-off, performing the action, or ordering the action to be performed. One example of fixing the problem is lowering the operating frequency of the hot spot area. In step 1118, the MPM 1070 reports both the problem and the fixing of the problem upstream.

In step 1120, the PMCL 218 reads the modified hot spot report from the MPM 1070. In step 1122, the PMCL 218 determines what action to take to fix the problem or notify the GPAL 214 of the problem. In step 1124, the PMCL 218 issues the appropriate commands to the MPM 1070 to fix the problem. In this step, the software will make the trade-off required to fix the problem. In some embodiments, if the GPAL 214 determines the high level fix, then the GPAL 214 sends it to the PMCL 280 to be converted into MPM commands. In step 1126, the PMCL 218 monitors the problem area for a specified time to check if the problem is fixed. FIG. 11 ends in step 1128.

In some embodiments, the type of functionality in FIG. 11 can be performed at other levels such as the PMCL 218. In one example, the PMCL 218 queries (via the MPM 1070) all the SPMs that have the desired measurement ability (and IPMs) as to their local conditions and can then, for example, build a “map” of power usage that it can then act on.

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FIG. 12 depicts a diagram of a system-on-a-chip (SOC) 1200 in another exemplary implementation of the invention. The SOC 1200 is attached to a sensor link 1212, an RF link 1214, a control link 1216, a video link 1294, an audio link 1295, an interface link 1296, a control link 1297, and a power link 1298. The SOC 1200 includes clock and distribution management 1210, an IP block power island 1220, a memory power island 1230, a microprocessor power island 1240, an IP block power island 1250, a distribution power island 1260, an IP block power island 1270, an IP block power island 1280, and power and distribution management 1290.

The IP block power island 1220 includes a product standard interface IP block including an analog-to-digital converter (ADC) 1222, which includes an SPM 1224. The IP block power island 1230 includes a memory 1232, which includes an SPM 1234. The microprocessor power island 1240 includes a microprocessor 1242, which includes an SPM 1244. The IP block power island 1250 includes a product standard interface IP block including ADC 1252, which includes an SPM 1254. The distribution power island 1260 includes a data and signal distribution 1262, which includes an SPM 1264. The IP block power island 1270 includes a general purpose IP block including a digital signal processor (DSP) 1272, which includes an SPM 1274. The IP block power island 1280 includes a product-specific IP block 1282, which includes an SPM 1284. The power and distribution management 1290 includes an MPM 1292.

FIG. 13 depicts a flowchart for building a chip with power islands in an exemplary implementation of the invention. FIG. 13 begins in step 1300. In step 1302, the IPs or library cells are selected, and the custom logic, if any, is specified to be used to build the chip. In some embodiments, the maximum and sub clock rate, % idle time, and minimum and maximum Vdd are specified. In step 1304, the register transfer level (RTL) is written. In step 1306, the RTL is simulated and debugged.

Either during or after the writing of the RTL, a software tool may be used to add annotations for the MPM, IPM, and/or SPM blocks in step 1308. In some embodiments, the desired functionality options are specified in the annotations. In some embodiments, the optional functionality is specified per SPM block. In some embodiments, the RTL is annotated with SPM configuration information on a per-module basis. In some embodiments, the proper annotation is inserted by hand on a per module basis during or after the RTL is written. In other embodiments, a separate table in the proper format is created with the module names and respective annotations. In some embodiments, a separate software tool provides the ability to interactively build the separate table. In some embodiments, the software tool adds the proper annotation to the un-annotated modules in the RTL using information from the table.

In step 1310, the synthesis is run on a power island basis, where power islands are not mixed. In step 1312, performance measurement software is run on each module for each Vdd and Vt option, and then the annotations for the MPM are added to the RTL. In some embodiments, the performance of the design is measured at all desired voltages and Vt combinations. The software tool then derives the actual frequency, Vdd, and Vt tables for each SPM and back annotates the MPM (or IPM) RTL of the SPM characteristics.

In step 1314, the final synthesis is run on a power island basis. In some embodiments, the modules are separately routed or by SPM. In step 1316, the software tool is run to hook up power and clocks to each SPM. Step 1318 is the rest

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of the steps to tape-out. In some embodiments, the software tool generates the finished net-list with all information. FIG. 13 ends in step 1320.

The above-described elements can be comprised of instructions that are stored on storage media. The instructions can be retrieved and executed by a processor. Some examples of instructions are software, program code, and firmware. Some examples of storage media are memory devices, tape, disks, integrated circuits, and servers. The instructions are operational when executed by the processor to direct the processor to operate in accord with the invention. Those skilled in the art are familiar with instructions, processor, and storage media.

The above description is illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

What is claimed is:

1. A system comprising:
an integrated circuit;
a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions adapted to be independently controlled; and
a power manager to control the power consumptions;
at least one of the power islands adapted to have the power manager control its associated power consumption by a) the at least one of the power islands being configured to have one of plural threshold voltages of variable threshold transistors selected, and b) the system being configured to perform, during operation, an action on the at least one of the power islands, the action including changing a frequency of operation or changing a supply voltage.
2. The system as claimed in claim 1 wherein the power manager comprises a programmable processor.
3. The system as claimed in claim 1 wherein the integrated circuit is configured to perform, during operation, both changing the frequency of operation and changing the supply voltage.
4. The system as claimed in claim 1 wherein the system is configured to have the supply voltage provided by an external regulator.
5. The system as claimed in claim 4 wherein the external regulator is configured to be controlled by the power manager.
6. The system as claimed in claim 1 further comprising an internal regulator to provide the supply voltage.
7. The system as claimed in claim 6 wherein the internal regulator is configured to be controlled by the power manager.
8. The system as claimed in claim 1 wherein the at least one of the power islands is configured to have the one of plural threshold voltages selected during operation of the integrated circuit.
9. The system as claimed in claim 1 wherein the integrated circuit is configured to have the supply voltage changed by regulation of a voltage provided to the at least one of the power islands from a source external to the integrated circuit.
10. The system as claimed in claim 9 further comprising an internal regulator to perform the regulation.
11. The system as claimed in claim 9 wherein the regulation is performed by an external regulator.
12. The system as claimed in claim 1 further comprising a dropout voltage regulator to provide the supply voltage.

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13. The system as claimed in claim 1 wherein the integrated circuit is configured to have the supply voltage controlled by Vdd multiplexing in relation to the at least one of the power islands.

14. The system as claimed in claim 1 wherein the integrated circuit is configured to have the one of plural threshold voltage selected by back biasing.

15. The system as claimed in claim 1 wherein the integrated circuit comprises the power manager and the plurality of power islands.

16. The system as claimed in claim 1 wherein the power manager is configured to monitor one or more of the associated power consumptions using temperature or power dissipation measurement.

17. A system comprising:

an integrated circuit;

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions adapted to be independently controlled;

a power manager to control the power consumptions; and
an internal regulator, the system being configured to have a supply voltage provided by the internal regulator, and
at least one of the power islands adapted to have the power manager control its associated power consumption in that the system is configured to have:

a supply voltage to the at least one of the power islands changed, and

a frequency of operation of the at least one of the power islands changed.

18. The system as claimed in claim 17 wherein the power manager comprises a programmable processor.

19. The system as claimed in claim 17 wherein the system is configured to permit a clock to be stopped during operation of the integrated circuit so that the power manager can control the associated power consumption of the at least one of the power islands.

20. The system as claimed in claim 17 wherein the system is configured to have the supply voltage controlled by Vdd multiplexing in relation to the at least one of the power islands.

21. The system as claimed in claim 17 wherein the system is configured to have a clock stopped by clock gating.

22. The system as claimed in claim 17 wherein the integrated circuit comprises the power manager and the plurality of power islands.

23. The system as claimed in claim 17 wherein the power manager is configured to monitor one or more of the associated power consumptions using temperature or power dissipation measurement.

24. A processor implemented method comprising:

employing a power manager processor within an integrated circuit to control power consumptions of a plurality of power islands of the integrated circuit, each having an associated power consumption, each of the power consumptions being independently controlled; and
controlling the power consumption of at least one of the power islands by: a) selecting a threshold voltage of variable threshold transistors, and b) changing during operation at least one of the following: i) a frequency of operation, and ii) a supply voltage.

25. The processor implemented method as claimed in claim 24 wherein the threshold voltage of variable threshold transistors is selected during operation of the integrated circuit.

26. The processor implemented method as claimed in claim 24 wherein the supply voltage is changed, and the changing of the supply voltage includes regulating a voltage

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provided to the at least one of the power islands from a source external to the integrated circuit.

27. The processor implemented method as claimed in claim 24 wherein the supply voltage is changed, and the changing of the supply voltage includes Vdd multiplexing in relation to the at least one of the power islands.

28. The processor implemented method as claimed in claim 24 wherein the selecting the threshold voltage includes back biasing.

29. The processor implemented method as claimed in claim 24 wherein the power manager monitors one or more of the power consumptions using temperature or power dissipation measurement.

30. A system comprising:

an integrated circuit;

a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions adapted to be independently controlled, and a first of the power islands being configured to communicate synchronously and asynchronously with a second of the power islands; and

a power manager to control the power consumptions, and at least one of the power islands adapted to have the power manager control its associated power consumption in that the system is configured to have:

a supply voltage to the at least one of the power islands changed, and

a frequency of operation of the at least one of the power islands changed.

31. The system as claimed in claim 30 wherein the power manager comprises a programmable processor.

32. The system as claimed in claim 30 wherein the system is configured to permit a clock to be stopped during operation of the integrated circuit so that the power manager can control the associated power consumption of the at least one of the power islands.

33. The system as claimed in claim 30 wherein the integrated circuit is configured to have the supply voltage changed by regulation of a voltage provided to the at least one of the power islands from a source external to the integrated circuit.

34. The system as claimed in claim 33 further comprising an internal regulator to perform the regulation.

35. The system as claimed in claim 33 wherein the regulation is performed by an external regulator.

36. The system as claimed in claim 33 further comprising a dropout voltage regulator to perform the regulation.

37. The system as claimed in claim 30 wherein the system is configured to have the supply voltage controlled by Vdd multiplexing in relation to the at least one of the power islands.

38. The system as claimed in claim 30 wherein the system is configured to have a clock stopped by clock gating.

39. The system as claimed in claim 30 wherein the system is configured to have the supply voltage changed by an external regulator.

40. The system as claimed in claim 39 wherein the external regulator is configured to be controlled by the power manager.

41. The system as claimed in claim 30 further comprising an internal regulator to change the supply voltage.

42. The system as claimed in claim 41 wherein the internal regulator is configured to be controlled by the power manager.

43. The system as claimed in claim 30 wherein the integrated circuit comprises the power manager and the plurality of power islands.

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44. The system as claimed in claim 30 wherein the power manager is configured to monitor one or more of the associated power consumptions using temperature or power dissipation measurement.

45. A system comprising:

an integrated circuit;

a plurality of power islands of the integrated circuit; and a power manager to control power consumptions of the power islands, each of the power consumptions being independently controllable, and

at least one of the power islands capable of having the power manager control a power consumption of the at least one of the power islands by a) the at least one of the power islands selecting one of plural threshold voltages of variable threshold transistors, and b) the system performing, during operation, an action on the at least one of the power islands, the action including changing a frequency of operation or changing a supply voltage.

46. The system as claimed in claim 45 wherein the power manager comprises a programmable processor.

47. The system as claimed in claim 45 wherein changing the frequency of operation and changing the supply voltage are performed during operation.

48. The system as claimed in claim 45 wherein the system is capable of having the supply voltage changed by an external regulator.

49. The system as claimed in claim 48 wherein the external regulator is controllable by the power manager.

50. The system as claimed in claim 45 further comprising an internal regulator to change the supply voltage.

51. The system as claimed in claim 50 wherein the internal regulator is controllable by the power manager.

52. The system as claimed in claim 45 wherein the at least one of the power islands selects the one of plural threshold voltages during operation of the system.

53. The system as claimed in claim 45 wherein the supply voltage is changeable by regulation of a voltage provided to the at least one of the power islands from a source external to the system.

54. The system as claimed in claim 53 further comprising an internal regulator to perform the regulation.

55. The system as claimed in claim 53 wherein the regulation is performed by an external regulator.

56. The system as claimed in claim 53 further comprising a dropout voltage regulator to perform the regulation.

57. The system as claimed in claim 45 wherein the supply voltage is controllable by Vdd multiplexing.

58. The system as claimed in claim 45 wherein the one of plural threshold voltages is selectable by back biasing.

59. The system as claimed in claim 45 wherein the integrated circuit comprises the power manager and the plurality of power islands.

60. The system as claimed in claim 45 wherein the power manager is configured to monitor one or more of the power consumptions using temperature or power dissipation measurement.

61. A system comprising:

an integrated circuit;

a plurality of power islands of the integrated circuit, a first of the power islands capable of communicating synchronously and asynchronously with a second of the power islands; and

a power manager to control power consumptions of the power islands, each of the power consumptions being independently controllable, and in order that a power consumption of at least one of the power islands is

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capable of being controlled by the power manager, the system is capable of having:

a supply voltage to the at least one of the power islands changed, and

a frequency of operation of the at least one of the power islands changed.

62. The system as claimed in claim 61 wherein the power manager comprises a programmable processor.

63. The system as claimed in claim 61 wherein the supply voltage is changeable by regulation of a voltage provided to the at least one of the power islands from a source external to the system.

64. The system as claimed in claim 63 further comprising an internal regulator to perform the regulation.

65. The system as claimed in claim 63 wherein the regulation is performed by an external regulator.

66. The system as claimed in claim 63 further comprising a dropout voltage regulator to perform the regulation.

67. The system as claimed in claim 61 wherein the supply voltage is controllable by Vdd multiplexing.

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68. The system as claimed in claim 61 wherein a clock is capable of being stopped by clock gating.

69. The system as claimed in claim 61 wherein the system is capable of having the supply voltage changed by an external regulator.

70. The system as claimed in claim 69 wherein the external regulator is controllable by the power manager.

71. The system as claimed in claim 61 further comprising an internal regulator to perform regulation of the supply voltage.

72. The system as claimed in claim 71 wherein the internal regulator is controllable by the power manager.

73. The system as claimed in claim 61 wherein the integrated circuit comprises the power manager and the plurality of power islands.

74. The system as claimed in claim 61 wherein the power manager is configured to monitor one or more of the power consumptions using temperature or power dissipation measurement.

* * * * *

EXHIBIT D



US008253438B2

(12) **United States Patent**
Hoberman et al.

(10) **Patent No.:** **US 8,253,438 B2**

(45) **Date of Patent:** **Aug. 28, 2012**

(54) **LOW LEAKAGE AND DATA RETENTION CIRCUITRY**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/074,291**

(22) Filed: **Mar. 29, 2011**

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(60) Continuation of application No. 12/542,352, filed on Aug. 17, 2009, now Pat. No. 7,940,081, which is a continuation of application No. 12/284,311, filed on Sep. 19, 2008, now Pat. No. 7,592,837, which is a continuation of application No. 11/998,725, filed on Nov. 30, 2007, now Pat. No. 7,443,197, which is a continuation of application No. 11/732,181, filed on Apr. 2, 2007, now Pat. No. 7,348,804, which is a division of application No. 11/041,687, filed on Jan. 20, 2005, now Pat. No. 7,227,383.

(60) Provisional application No. 60/546,574, filed on Feb. 19, 2004, provisional application No. 60/586,565, filed on Jul. 9, 2004.

(51) **Int. Cl.**
H03K 17/16 (2006.01)

(52) **U.S. Cl.** **326/27**; 326/38; 326/81

(58) **Field of Classification Search** 326/21, 326/26, 27, 37-41, 46, 80-83
See application file for complete search history.

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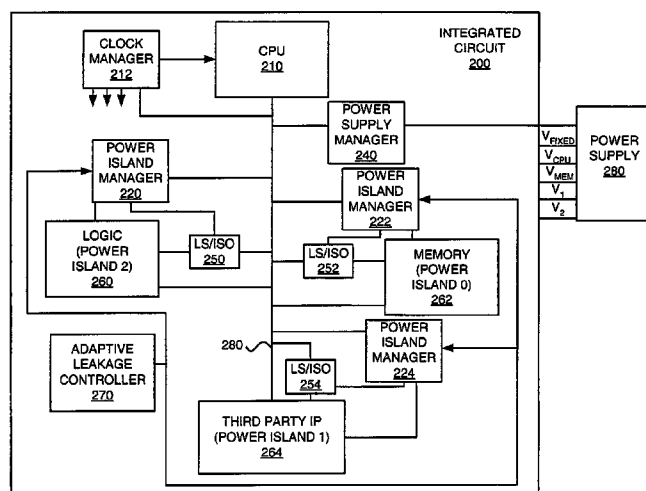
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(57) **ABSTRACT**

An integrated circuit includes first circuitry and sleep transistor circuitry. The first circuitry receives input signals and processes the input signals. The first circuitry also retains data in a sleep state that has low leakage. The sleep transistor circuitry is coupled to the first circuitry and receives a sleep signal that has a negative voltage. The sleep circuitry reduces power consumption of the first circuitry in the sleep state to have low leakage based on the sleep signal while retaining the data in the first circuitry.

19 Claims, 12 Drawing Sheets



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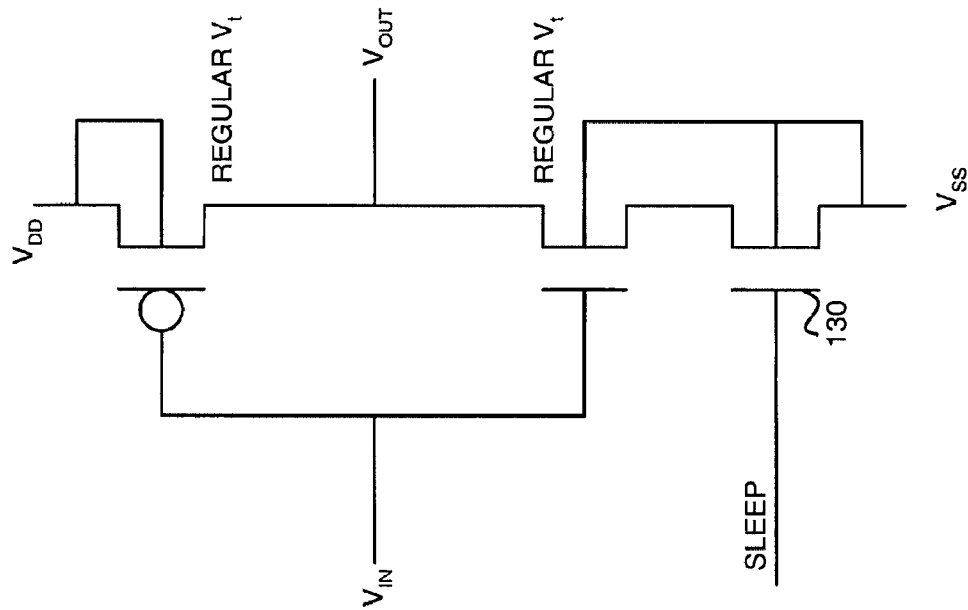


FIG. 1
PRIOR ART

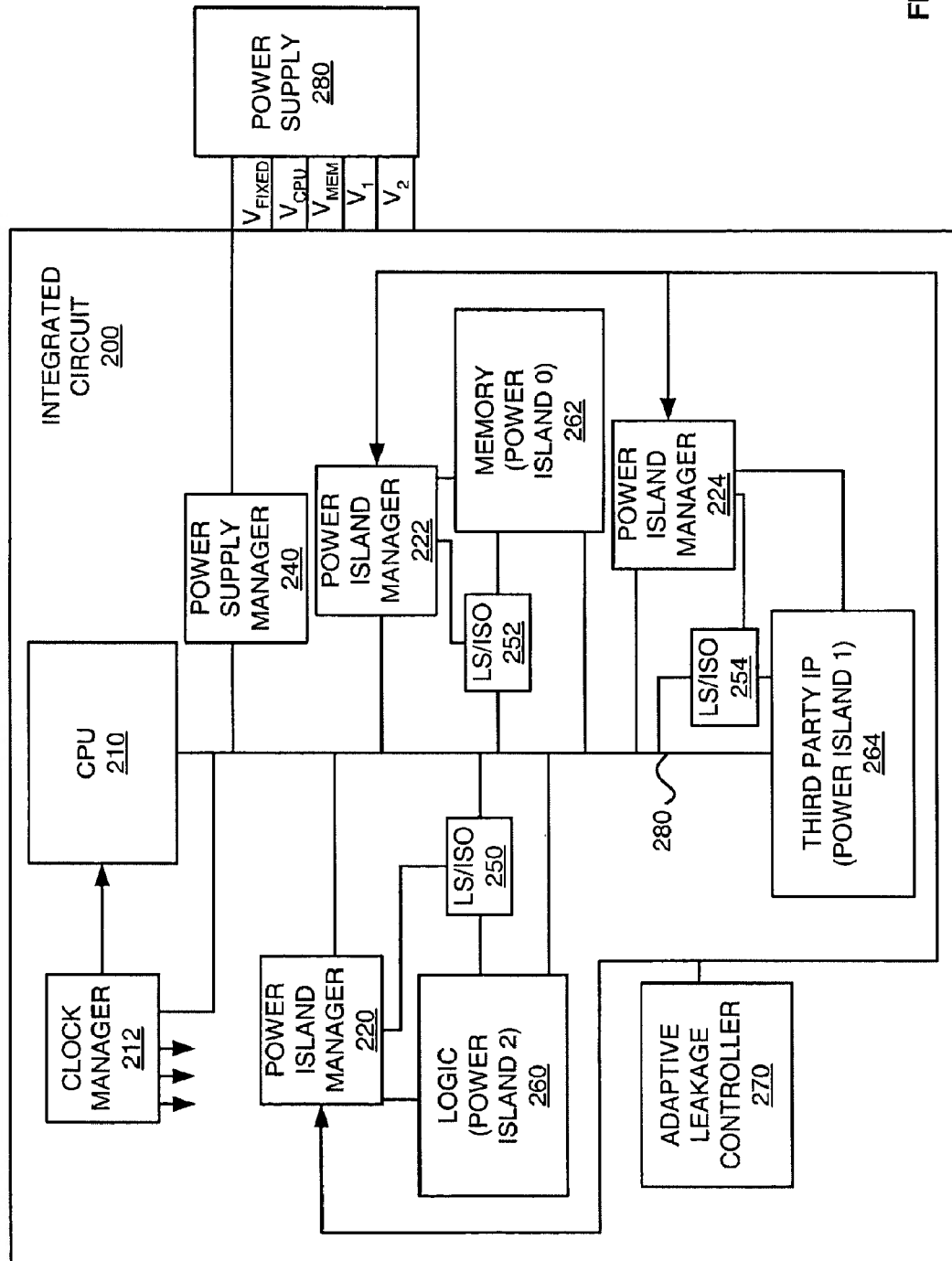


FIG. 2

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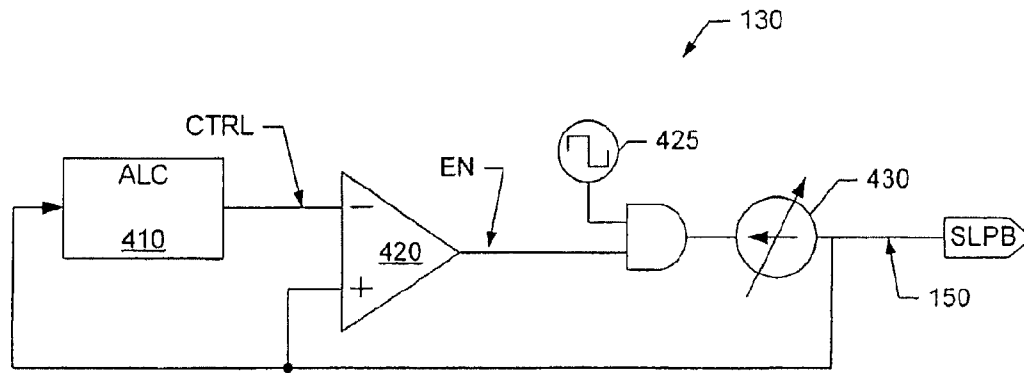


FIG. 2A

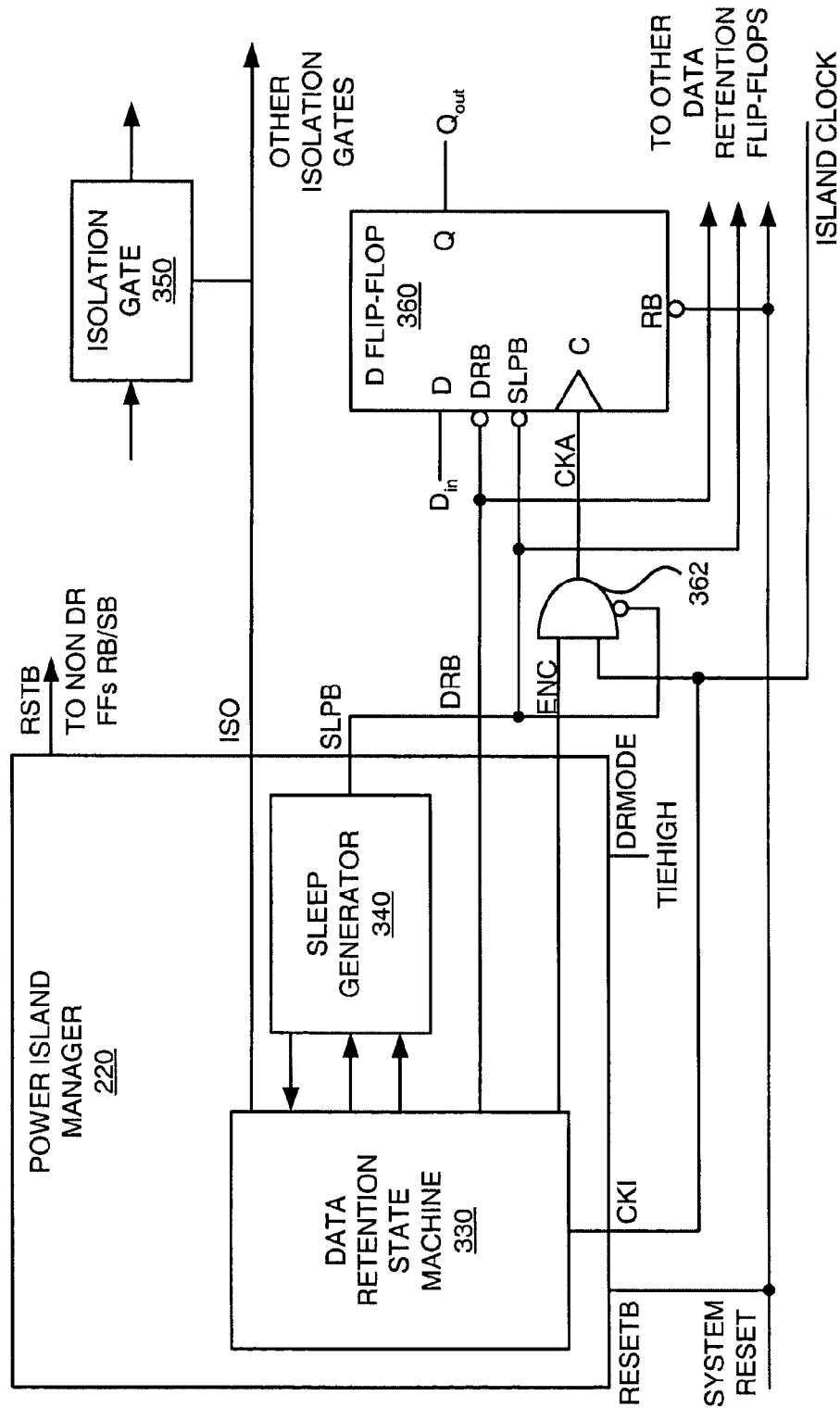


FIG. 3

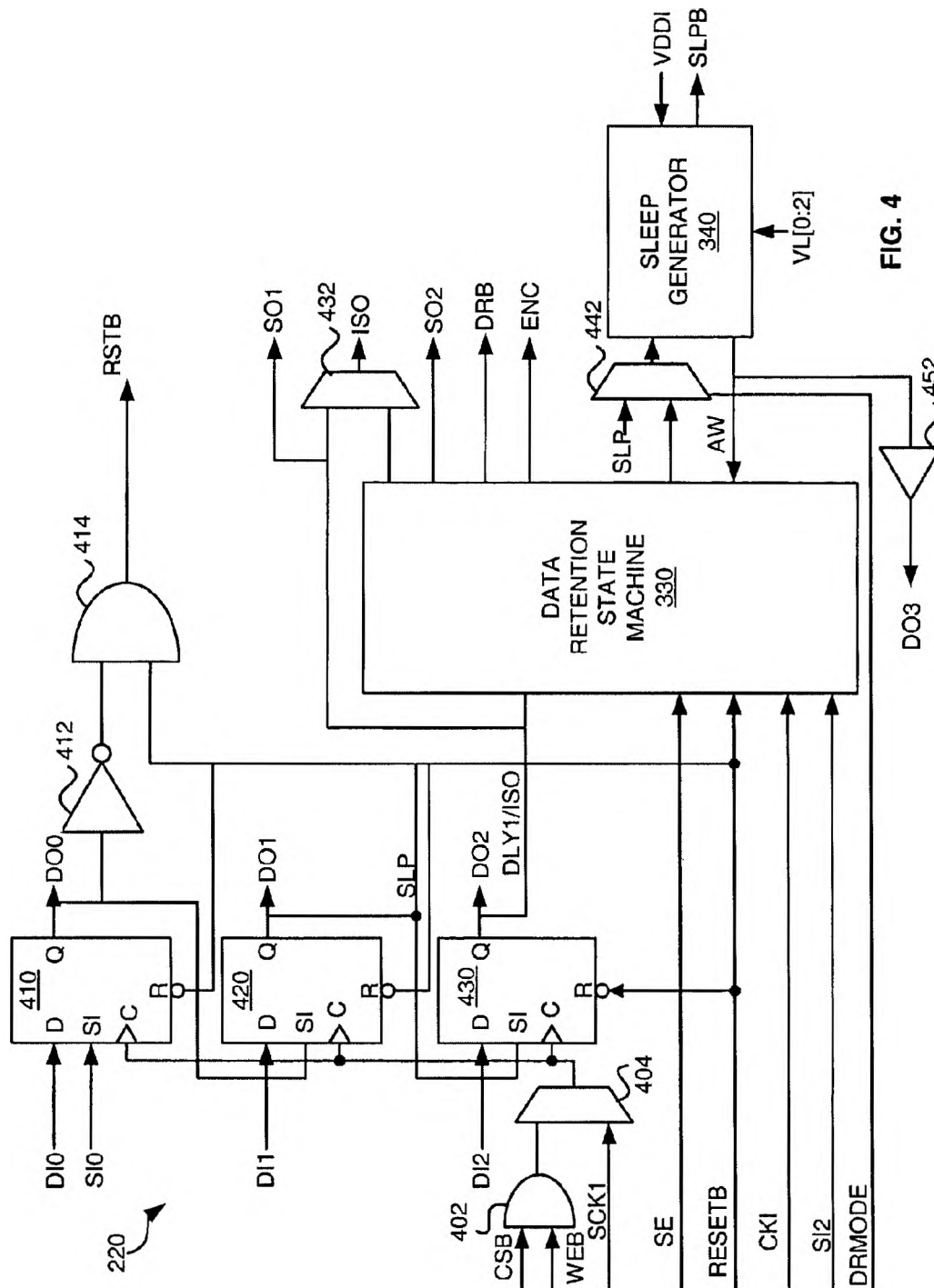
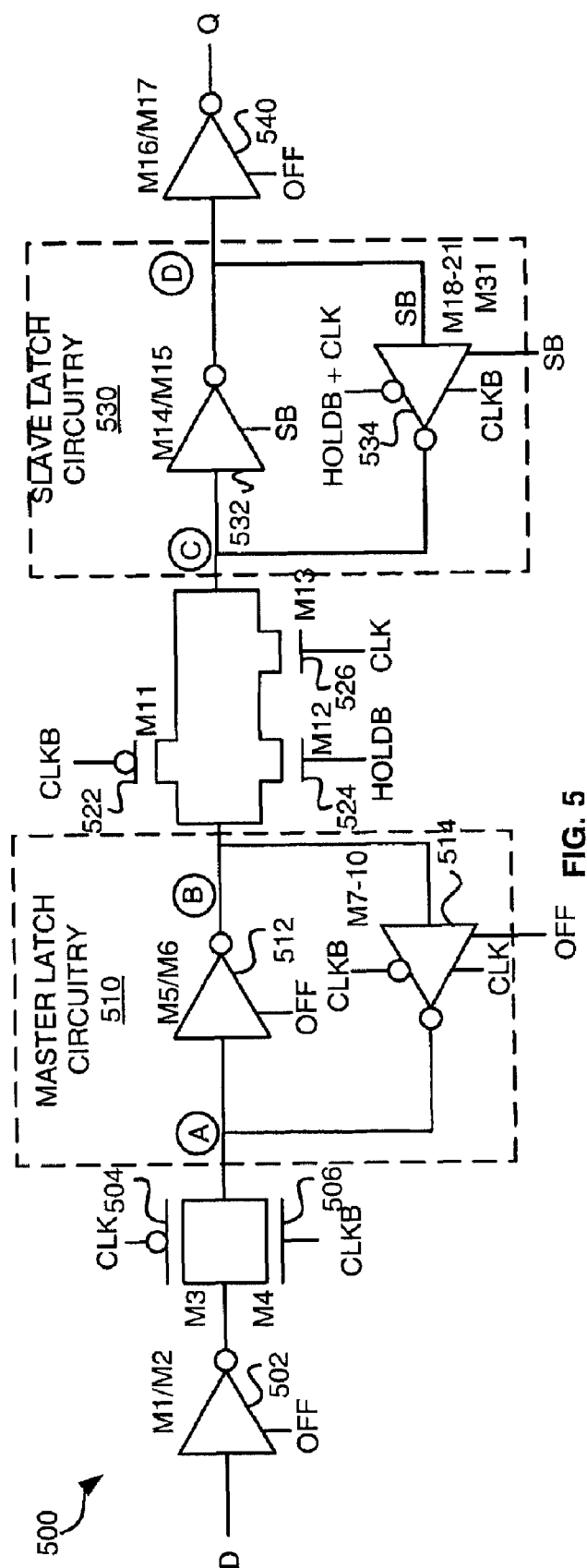


FIG. 4



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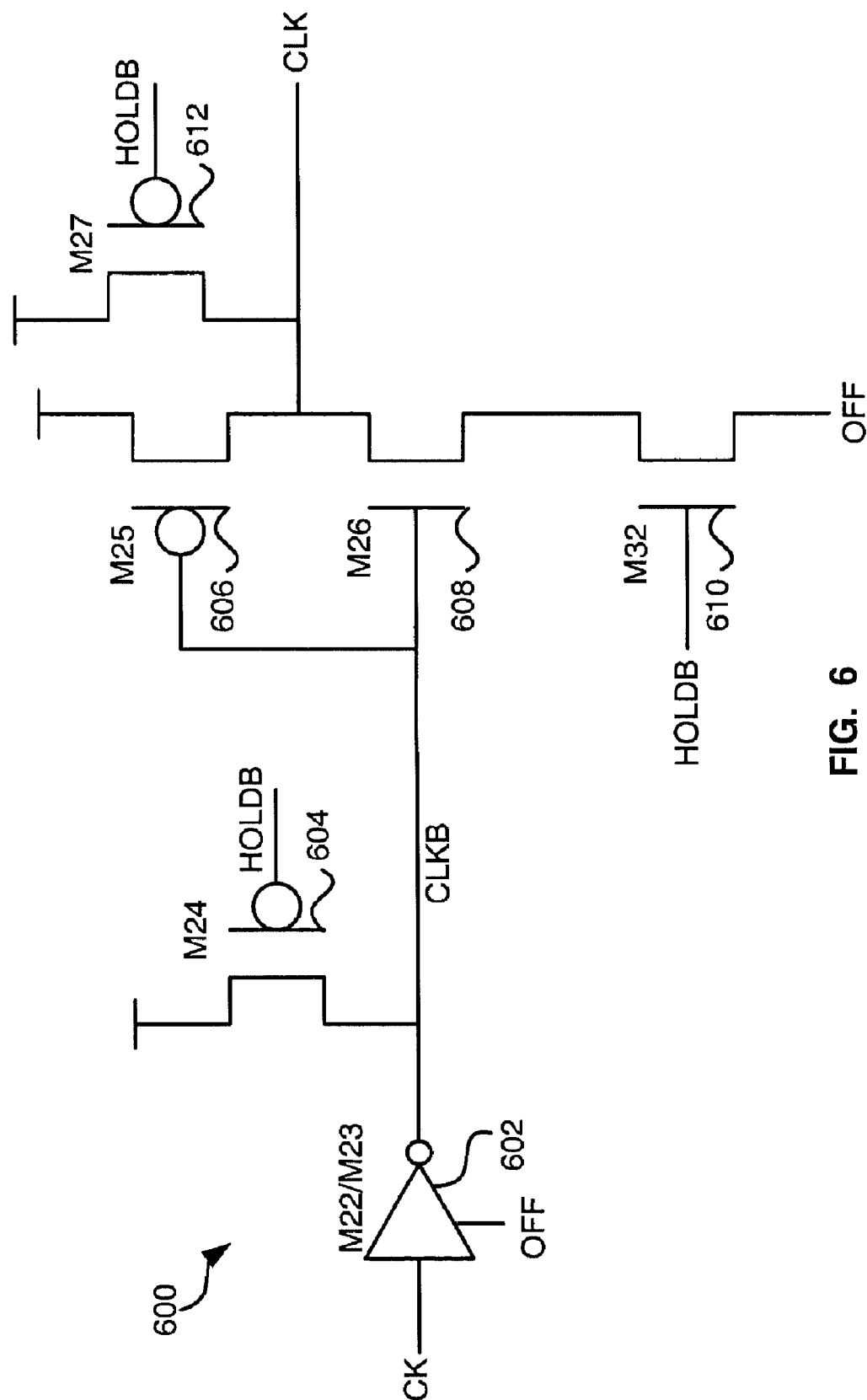


FIG. 6

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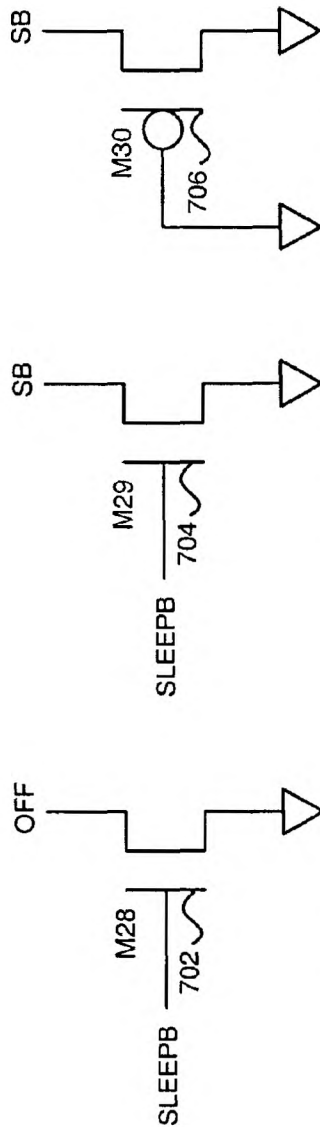


FIG. 7C

FIG. 7B

FIG. 7A

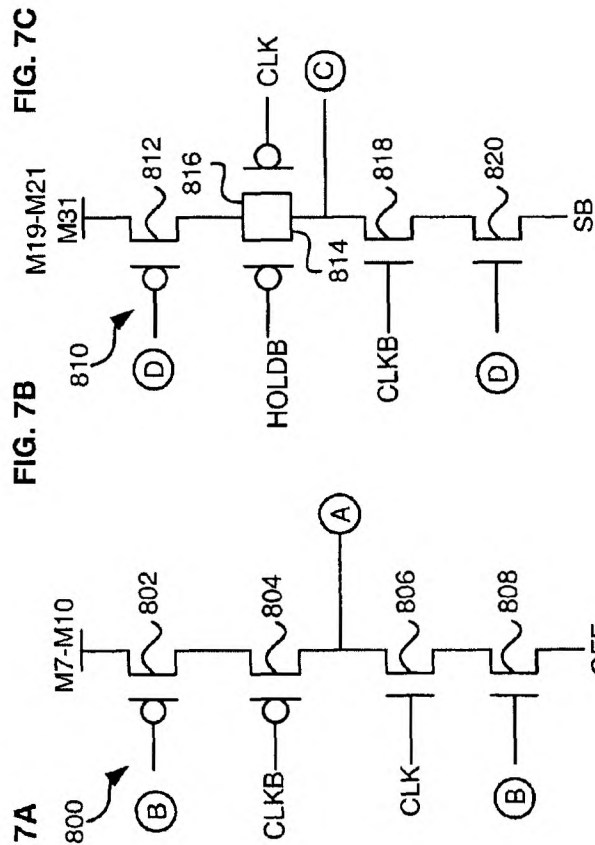


FIG. 8B

FIG. 8A

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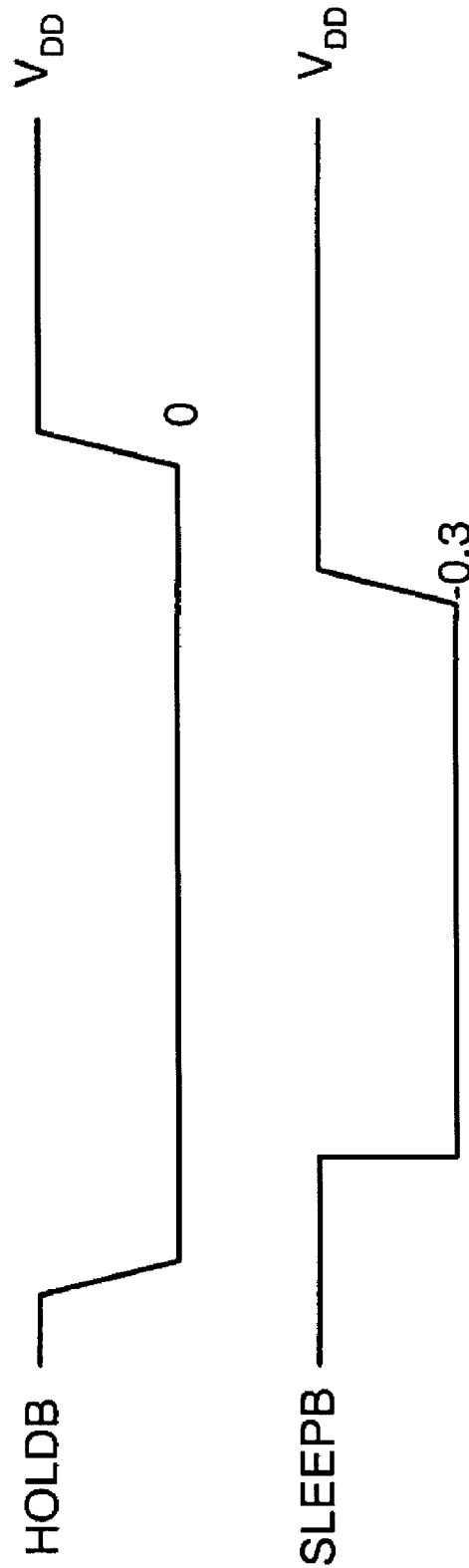


FIG. 9

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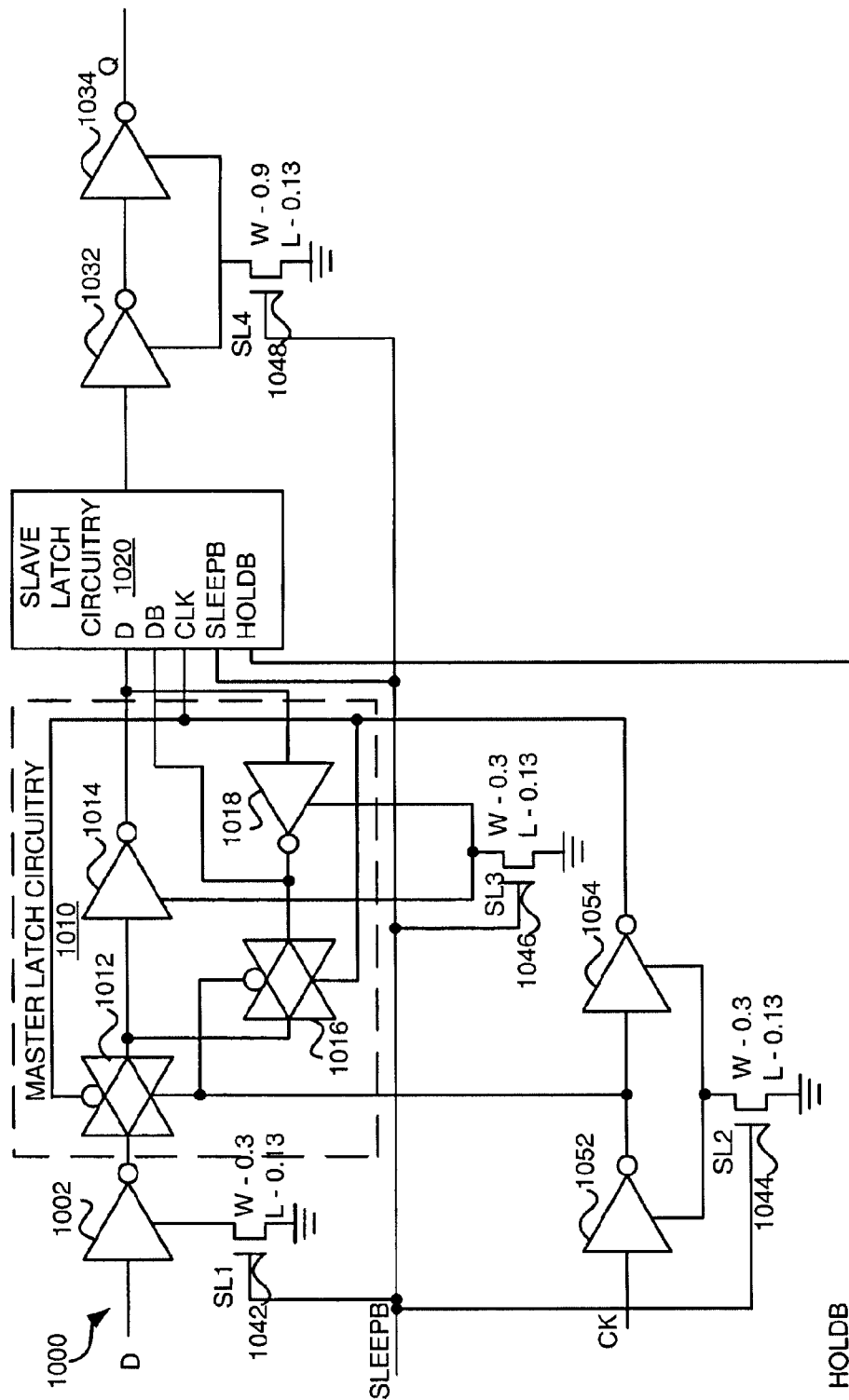


FIG. 10

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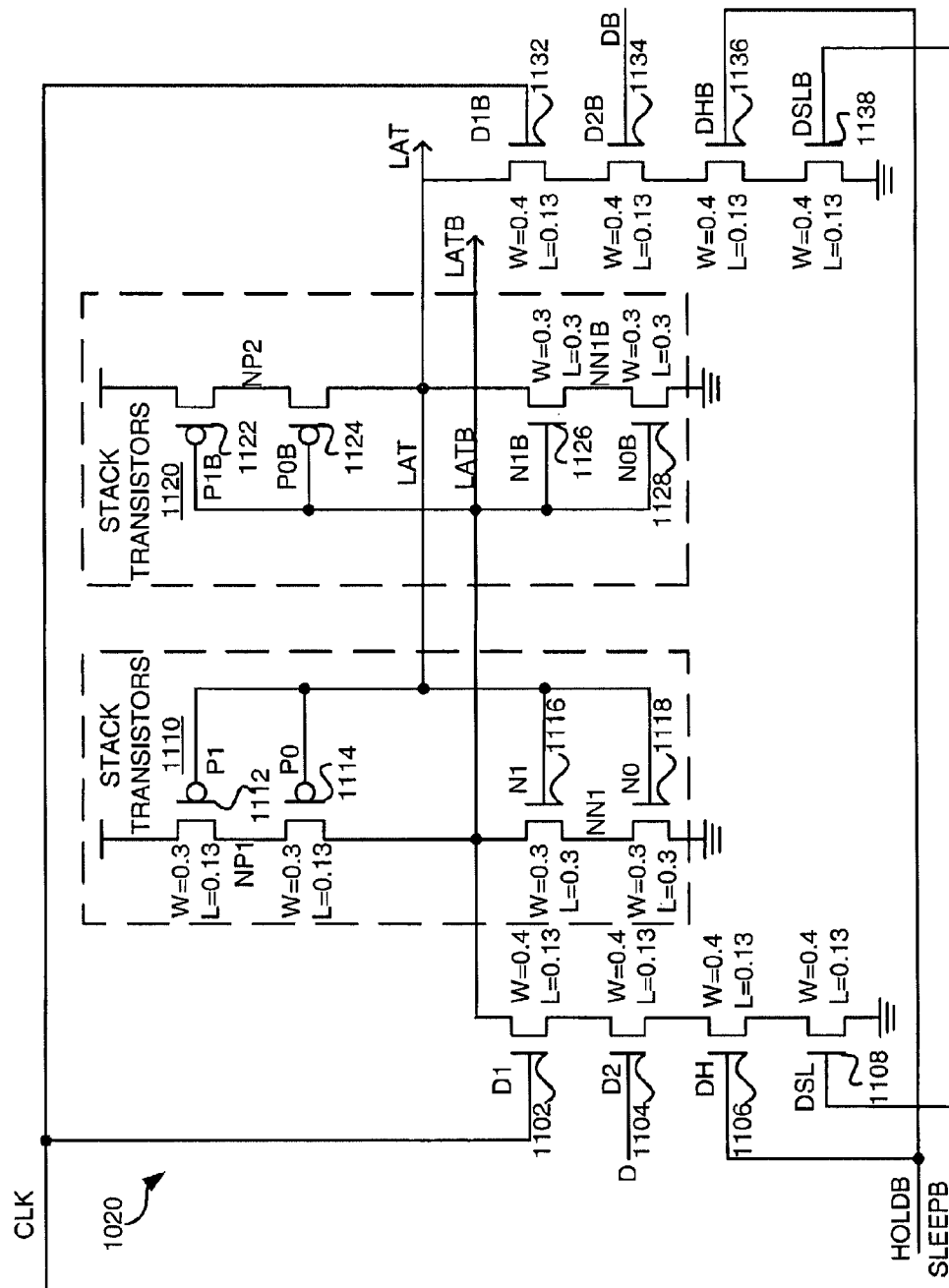


FIG. 11

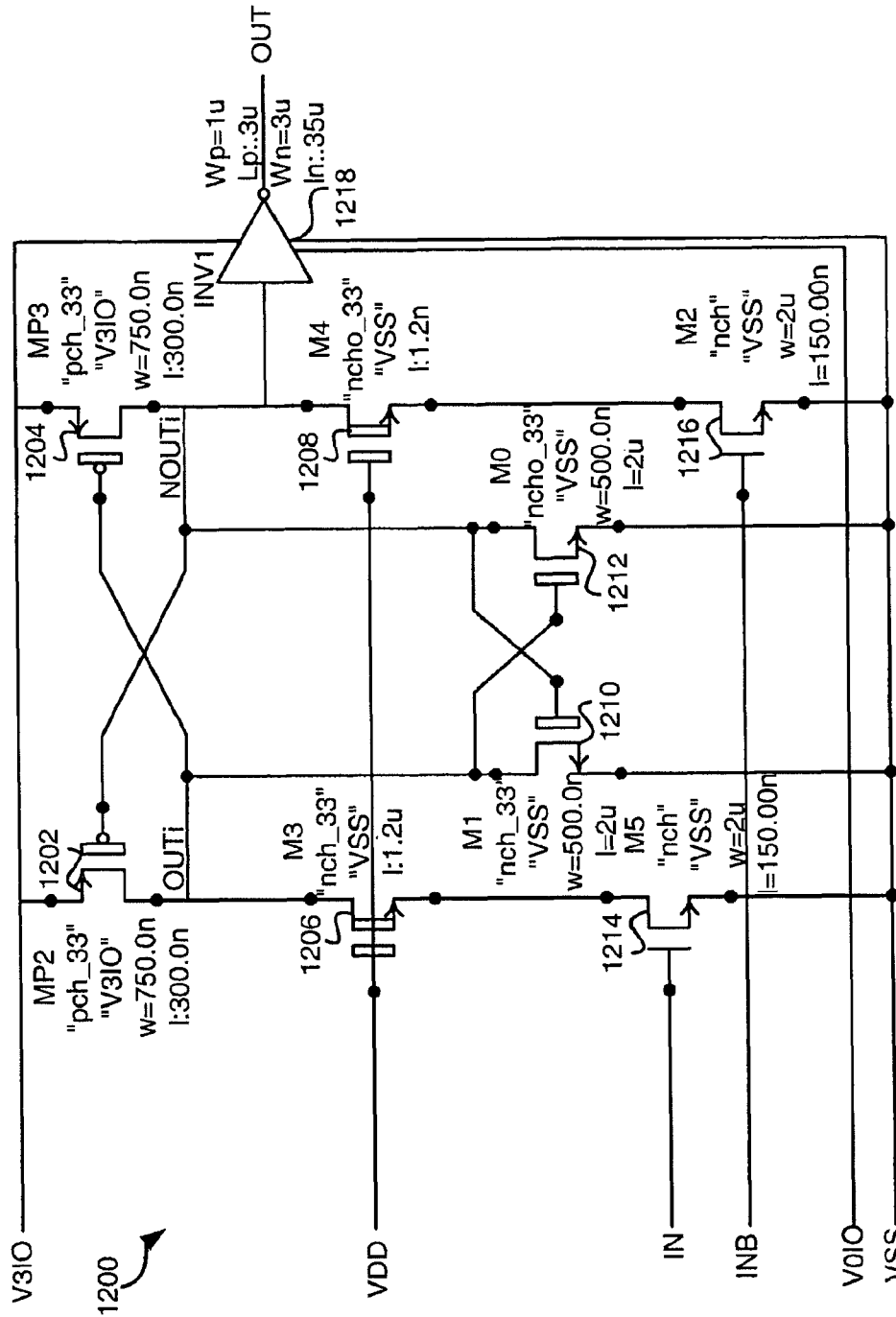


FIG. 12

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**LOW LEAKAGE AND DATA RETENTION
CIRCUITRY**

RELATED APPLICATIONS

This application is a continuation of U.S. application Ser. No. 12/542,352, filed Aug. 17, 2009, which is a continuation of U.S. application Ser. No. 12/284,311, filed Sep. 19, 2008 (now U.S. Pat. No. 7,592,837), which is a continuation of U.S. application Ser. No. 11/998,725, filed Nov. 30, 2007 (now U.S. Pat. No. 7,443,197), which is a continuation of U.S. application Ser. No. 11/732,181, filed Apr. 2, 2007 (now U.S. Pat. No. 7,348,804), which is a divisional and claims the priority benefit of U.S. application Ser. No. 11/041,687 filed Jan. 20, 2005 (now U.S. Pat. No. 7,227,383), which claims the priority benefit of U.S. Provisional Application No. 60/546,574, filed Feb. 19, 2004 and U.S. Provisional Application No. 60/586,565, filed Jul. 9, 2004.

The entire teachings of the above applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to integrated circuits, and more particularly to low leakage and data retention circuitry.

2. Description of the Related Art

Most integrated circuits have a design goal to reduce the overall power consumption. The total power consumed by an integrated circuit includes dynamic power consumption and standby leakage current consumption. The challenge in designing an integrated circuit is to reduce the dynamic power and leakage power, while maintaining performance and cost goals for the integrated circuit.

In complementary metal oxide semiconductors (CMOS), various types of leakage occur such as pn junction reverse-bias current, subthreshold leakage, oxide tunneling current, gate current due to hot-carrier injection, gate-induced drain leakage, and channel punch through current. When the threshold voltage for a CMOS transistor is reduced for higher performance, the leakage power is significant in the total power consumption of the CMOS circuit.

There are two approaches in reducing the leakage power for CMOS circuits. The first approach is a process level technique that controls the doping profile of the transistor. The other approach is a circuit level technique where voltages at the different device terminals such as the drain, source, gate, and body are controlled. Some circuit level techniques are discussed below.

One circuit level technique is stacking transistors, which is also called self-reverse bias. When more than one transistor in a stack of series-connected transistors is turned off, the subthreshold leakage current is reduced. One problem with the transistor stack is that only a three times reduction in leakage current is achieved. Another circuit level technique is a multiple threshold voltage design. Both high- and low-threshold transistors are on the same chip to deal with the leakage problem. The high-threshold transistors suppress the subthreshold leakage current. The low-threshold transistors are used to achieve higher performance. One problem with a multiple threshold design is that process complexity and costs are increased.

Another circuit level technique is a multiple body bias in which the body voltage is changed to modify the threshold voltage. If separate body biases are applied to different NMOS transistors, the transistor cannot share the same well,

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which requires triple well technologies. One problem is that well biasing consumes a lot of chip area and requires extra power supplies for each cell. This technique also increases process complexity and the leakage reduction is not optimal.

Another technique for reducing leakage is a sleep transistor. FIG. 1 depicts prior art circuitry including a sleep transistor. For NMOS sleep transistors, one or more NMOS transistors are added to logic gates in series with the cell transistors to VSS. The NMOS sleep transistors act as a switch to turn on and off the logic gate. In FIG. 1, the sleep transistor 130 is turned on (gate to VDD) during normal cell operation. When the cell is idle, the sleep transistor 130 is turned off (gate tied to VSS) to reduce the leakage current of the cell. Sleep transistors can also be PMOS transistors. One problem with sleep transistors is that if all logic has sleep transistors, the logic will lose their state information.

SUMMARY OF THE INVENTION

In an exemplary embodiment of the presently disclosed invention, a data retention circuit is provided. The exemplary circuit includes an input/output pad cell that itself includes level shifter circuitry, the level shifter circuitry having inputs and outputs. Output latching circuitry is also provided as a part of the data retention circuit. The output latching circuitry includes two transistors. The transistors are coupled to the outputs of the level shifter circuitry and retain a state of the level shifter circuitry based on the state of the inputs. A leakage optimization circuit is also included, the leakage optimization circuit is configured to simultaneously decrease leakage power in conjunction with the state retention of the output latching circuitry.

In another embodiment of the presently disclosed invention, a system for controlling power consumption within an integrated circuit is disclosed. The system includes a power island, the power island includes a first circuit. The first circuit of the power island is configured to receive an input signals and a hold signal. The circuit is further configured to process the input signals and retain data in a sleep state having low leakage. The first circuit is further configured to retain the data based on the hold signal. The system further includes a sleep transistor, which is coupled to the first circuit. The sleep transistor is configured to receive a negative voltage sleep signal and reduce power consumption of the first circuit in the sleep state. As a result, the first circuit has low leakage based on the sleep signal while simultaneously retaining the data.

BRIEF DESCRIPTION OF THE DRAWINGS

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The foregoing will be apparent from the following more particular description of example embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating embodiments of the present invention.

FIG. 1 is an illustration of circuitry including a sleep transistor in the prior art;

FIG. 2 is an illustration of an integrated circuit with a power supply in an exemplary implementation of the invention;

FIG. 2A is a block diagram of a leakage manager system for minimizing state leakage of a logic gate by application of a negative voltage to a sleep transistor.

FIG. 3 is an illustration of a power island manager with an isolation gate and a D flip-flop in an exemplary implementation of the invention;

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FIG. 4 is an illustration of a power island manager in an exemplary implementation of the invention;

FIG. 5 is an illustration of a D/Q portion of flip-flop circuitry in an exemplary implementation of the invention;

FIG. 6 is an illustration of a CK portion of flip-flop circuitry in an exemplary implementation of the invention;

FIG. 7A is an illustration of a sleep transistor for an OFF node in an exemplary implementation of the invention;

FIG. 7B is an illustration of a sleep transistor for an SB node in an exemplary implementation of the invention;

FIG. 7C is an illustration of a moderate impedance transistor for an SB node in an exemplary implementation of the invention;

FIG. 8A is an illustration of circuitry for a tristate inverter in the master latch in an exemplary implementation of the invention;

FIG. 8B is an illustration of circuitry for a tristate inverter in the slave latch in an exemplary implementation of the invention;

FIG. 9 is an illustration of a HOLDB and SLEEPB signals in an exemplary implementation of the invention;

FIG. 10 is an illustration of circuitry for low leakage and data retention in an exemplary implementation of the invention;

FIG. 11 is an illustration of slave latch circuitry in an exemplary implementation of the invention; and

FIG. 12 is an illustration of circuitry for a level shifter for an I/O pad in an exemplary implementation of the invention.

DETAILED DESCRIPTION OF THE INVENTION

A description of example embodiments of the invention follows.

As shown in the exemplary drawings wherein like reference numerals indicate like or corresponding elements among the figures, exemplary embodiments of a system and method according to the present invention are described below in detail. It is to be understood, however, that the present invention may be embodied in various forms. Therefore, specific details disclosed herein are not to be interpreted as limiting, but rather as a basis for the claims and as a representative basis for teaching one skilled in the art to employ the present invention in virtually any appropriately detailed system, structure, method, process or manner.

Power Island Manager—FIGS. 2-4

In some embodiments, an integrated circuit can be delineated into power islands. Power consumption can then be controlled within the power island. A power island manager provides control signals to the power island to control power consumption of the power island. In some embodiments, the low leakage, data retention circuitry is located within the power islands.

FIG. 2 depicts an illustration of an integrated circuit 200 with a power supply 280 in an exemplary implementation of the invention. The integrated circuit 200 includes a central processing unit (CPU) 210, a clock manager 212, power island managers 220, 222, and 224, a power supply manager 240, level shifter/isolation gates (LS/ISO) 250, 252, and 254, logic (power island 2) 260, memory (power island 0) 262, third party intellectual property (IP) (power island 1) 264, adaptive leakage controller (ALC) 270, and bus 280.

A power island is any section, delineation, partition, or division of an integrated circuit where power consumption is controlled within the section, delineation, partition, or division. In some embodiments, the power islands are delineated based on geographic factors of the integrated circuit. In some embodiments, the power islands are delineated based on

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functional IP units of the integrated circuit 200. In this example depicted in FIG. 2, power islands are delineated by memory 262, logic 260, and third party IP 264. Power islands are discussed in further detail in pending U.S. application Ser. No. 10/840,893 entitled “Managing Power on Integrated Circuits Using Power Islands” filed on May 7, 2004, which is hereby incorporated by reference.

The power island managers 220, 222, and 224 are any circuitry, device, or system configured to provide control signals to a power island to control power within the power island. The power island managers 220, 222, and 224 can dynamically change the power consumption of the power islands based on the needs and operation of the integrated circuit 200. The power island managers 220, 222, 224 may select a clock, change clock frequency, or modify the voltage within the power island to control the power consumption of the power island.

The ALC 270 provides control signals to compensate for process and temperature variation to provide the optimum voltage to be applied to sleep transistors in the power islands. The ALC 270 is described in further detail U.S. patent application Ser. No. 10/996,739 entitled “Systems and Methods for Minimizing Static Leakage of an Integrated Circuit” filed on Nov. 17, 2004.

FIG. 2A is a block diagram of a leakage manager system 290 for minimizing static leakage of a logic gate by application of a negative voltage to a sleep transistor in accordance with an example embodiment. The leakage manager system 290 comprises an adaptive leakage controller (ALC) 291, a negative voltage regulator 292, and a charge pump 294. The charge pump 294 generates a negative voltage 295 (SLPB). The ALC 291 determines whether to adjust the negative voltage 295. The ALC 291 generates a signal (depicted as CTRL) depending on the determination. The negative voltage regulator 292 adjusts the negative voltage 295 depending on the CTRL signal.

As described further herein, the negative voltage regulator 292 of one embodiment generates an enable (EN) signal to the charge pump 294 to enable the charge pump 294 to increase the magnitude of the negative voltage 295 (i.e., to make the negative voltage 295 more negative). If the EN signal is low, an alternating signal from an oscillator 293 to the charge pump 294 is disabled, preventing the charge pump 294 from increasing the magnitude of the negative voltage 295. Alternatively, if the EN signal is high, the alternating signal from the oscillator 293 is enabled so that the charge pump 294 will increase the magnitude of the negative voltage 295. Because the negative voltage regulator 292 toggles the EN signal on or off depending on whether the ALC 291 determines to adjust the negative voltage 295, the leakage manager system 290 maintains the negative voltage 295 at a particular negative voltage to minimize static leakage of the logic gate.

Under normal operation where the digital logic block is to operate, the sleep control receives a signal (sleep input, polarity unimportant here) to disable the charge pump and raise V_{sleep} voltage to V_{DD} .

Under idle operation, where the digital logic block is to sleep (change to a low leakage current state), the Charge Pump Control Logic (CPCL) sends a clock signal and an enable signal to the Negative Voltage Charge Pump (NVCP) to first rapidly drop the V_{sleep} signal to V_{SS} . Then the charge pump begins to push the V_{sleep} voltage below V_{SS} and continues to do so until it receives a pause signal from the CPCL. The Negative Bias Voltage Bias Regulator (NVBR) monitors the V_{sleep} voltage until a desirable reduction of the transistor current I_{off} has been achieved. At that point it sends a signal to the CPCL to initiate a Pause signal to the NVCP. As time

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passes the V_{sleep} voltage will slowly drift upwards toward V_{SS} and at a preset transistor I_{off} the NVBR sends a signal to the CPCL to restart the NVCP to restore the V_{sleep} negative voltage to achieve the desired I_{off} .

FIG. 3 depicts an illustration of the power island manager 220 with an isolation gate 350 and a D flip-flop 360 in an exemplary embodiment of the invention. The power island manager 220 includes a data retention state machine 330 and a sleep generator 340 that are coupled to each other.

The power island manager 220 is coupled to the isolation gate 350 by the ISO signal. The ISO signal is also coupled to other isolation gates. The data retention state machine 330 is coupled to DRB input of the D flip-flop 360 via the DRB signal. The data retention state machine 330 is also coupled to the AND gate 362 via the ENC signal. The clock island (CKI) signal is coupled to the data retention state machine 330 and the AND gate 362. The sleep generator 340 is coupled to the D flip-flop 360 and the AND gate 362 via the SLPB signal. The output of the AND gate 362 is coupled to the C input of the D flip-flop 360 via the CKA signal. The system reset signal is coupled to the RESETB input of the power island manager 220 and the RB input of the D flip-flop 360. The SLPB signal, the DRB signal, and the system reset signal are coupled to other data retention flip-flops.

FIG. 4 depicts an illustration of a power island manager 220 in an exemplary embodiment of the invention. The power island manager 220 includes an AND gate 402, a multiplexer (MUX) 404, a D flip-flop 410, an inverter 412, an AND gate 414, a D flip-flop 420, a D flip-flop 430, the data retention state machine 330, a MUX 432, a MUX 442, a sleep generator 340, and a buffer 452.

The DI0 pin is coupled to the D input of the D flip-flop 410. The SI0 pin is coupled to the SI input of the D flip-flop 410. The CSB and the WEB pins are coupled to the inputs of the AND gate 402. The output of the AND gate 402 and the SCK1 pin are coupled to the input of the MUX 404. The output of the MUX 404 is coupled to the C inputs of the D flip-flop 410, the D flip-flop 420, and the D flip-flop 430. The Q output of the D flip-flop 410 is coupled to the DO0 pin, which is coupled to the input of the inverter 412 and the SI input of the D flip-flop 420. The DI1 pin is coupled to the D input of the D flip-flop 420. The Q output of the D flip-flop 420 is coupled to the DO1 pin, which is coupled to the input of the AND gate 414 and the SI input of the D flip-flop 430. The output of the AND gate 414 is coupled to the RSTB pin. The DI2 pin is coupled to the D input of the D flip-flop 430. The Q output of the D flip-flop 430 is coupled to the DO2 pin, which is coupled to the DLY1/ISO pin. The DLY1/ISO pin is coupled to the SO1, the input of the MUX 432, and the data retention state machine 340.

The RESETB pin is coupled to the R input of the D flip-flop 430, the D flip-flop 420, and the D flip-flop 410. The SE pin, the RESETB pin, the CKI pin, and the SI2 pin are coupled to the data retention state machine 330. The data retention state machine 330 is coupled to the input of the MUX 432, the SO2 pin, the DRB pin, the ENC pin, and the input of the MUX 442. The output of the MUX 442, the VDDI pin, and the VL[0:2] are coupled to the sleep generator 340. The sleep generator 340 is coupled to the SLPB pin. The sleep generator 340 is coupled to the data retention state machine 330 via the AW pin and the input of the buffer 452. The output of the buffer 452 is coupled to the DO3 pin. The DRMODE pin is coupled to the MUX 442.

In operation, the power island manager 220 has a three bit register for controlling a power island for some embodiments. D [0], with input DI0 and output DO0, is an island reset for re-initializing a power island. This bit is combined with

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RESETB to form RSTB to re-initialize the power island whenever RESETB or the D [0] is active. D [1], with input DI1 and output DO1, is a sleep bit. When the D [1] bit is set to one, the power island goes into a low leakage state. D [2], with input DI2 and output DO2, is a DLY1/Isolate bit. When DRMODE is tied to low, the D [2] bit, when set to one, will add one clock cycle delay between DRB going active and SLPB going active. When DRMODE is tied high, the D [2] bit, when set to one, will activate isolation of the power island. D [3], such as DO3, is an awake bit. This D [3] bit goes high when SLPB is high. This can be used by software to determine when a power island is out of the sleep state.

The power island manager 220 has two operating modes: one that supports power islands with data retention flip-flops and one that does not. When the DRMODE pin is tied high, a power island is put to sleep by writing a one to D[1]. The data retention state machine 330 performs the timing. The isolate (ISO) signal goes active when the sleep bit is written to a one, and the enable clock (ENC) and the data retention (DRB) will go low after synchronization to the power island clock (CKI). One or two clock cycles later the sleep (SLPB) goes low. To come out of sleep mode, a zero is written to D[1]. In some embodiments, all clock buffers in the power islands can be put to sleep to further minimize leakage. Software can determine when the power island has come out of sleep by reading when DO3 is high.

The System Reset is typically applied once after initial system power up. In some embodiments, the System Reset goes to all data retention flip-flops. The System Reset signal and DI0 bar are combined in a logical AND (RSTB output) to provide initialization to non data retention flip-flops. To create a power island reset, D[0] is set to a one and then cleared to a zero by software.

When the DRMODE is tied low, the power island manager 220 can also provide the control signals for a power island without data retention flip-flops. The power island manager 220 may have a hardware driven method and a software driven method for interfacing to power islands without data retention flip-flops. The software sequence has the following sequence:

Write 04/turn on isolation
Write 06/turn on sleep, isolation on/come out of sleep
Write 05/turn sleep off, reset island, isolation on/wait for sleep to go high
Read/test for DO3=1; sleep is high
Write 00/turn isolation off, normal operation

The hardware driven method uses a clock to sequence the state machine. The only action software takes is to write the sleep bit (DI1) to a one to go into sleep and write a zero to the sleep bit to go out of sleep. Software can determine when the island has come out of sleep by reading when DO3 is high.

In some embodiments, the power island manager 220 contains two scan chains because some of the flip-flops are clocked on the positive and some on the negative. The scan chain enable pin switches the clock on scan chain 1 (SI1 is the input; SO1 is the output), the registers, to CKS1. Scan chain 2 (SI2 is the input; SO2 is the output) is connected to the data retention state machine 330 flip-flops that are clocked on the negative edge of CKI. A separate scan out is provided for each clock domain.

In some embodiments, the SLPB net uses p-type antenna diodes. Since the SLPB net may go to a negative voltage, an n-type antenna diode can cause excessive leakage to ground. The leakage can cause SLPB not to go negative and may not work properly. The CSB pin is a chip select pin. The WEB pin

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is the write enable pin. The VL [2:0] is the leakage control voltage value set by the ALC 270 (FIG. 2). The VDDI is the VDD from the power island.

Low Leakage, Data Retention Circuitry—FIGS. 5, 6, 7A-C, 8A-8B, and 9-12

FIGS. 5, 6, 7A-C, and 8A-8B disclose one embodiment for low leakage, data retention circuitry. In this embodiment, in sleep mode, the circuit parts of a flip-flop that do not require data retention are coupled to ground through a sleep transistor. The gate of the sleep transistor is coupled to a sleep signal that can be driven to a negative voltage such as $-0.3V$. Thus, the leakage in these circuit parts of the flip-flop is eliminated (reduced). When not in a sleep state, the sleep transistor has a gate value equal to or greater than the VDD supply, which effectively grounds the circuit.

The circuit parts that require data retention are coupled to ground through two transistors. One transistor acts effectively to ground the circuit above when not in sleep mode just as the sleep transistor described above. The other transistor is a PMOS device with the gate tied to ground, which provides medium impedance to ground. The voltage drop across this transistor acts to reduce the leakage by increasing the source bias of the NMOS transistors and simultaneously reduces the voltage across the circuit. In this embodiment, the data is retained in a sleep state and reduces the leakage by a factor of 22.

FIG. 5 depicts an illustration of a D/Q portion 500 of the flip-flop circuitry in an exemplary implementation of the invention. The D/Q portion 500 of the flip-flop circuitry includes an inverter 502, a M3 PMOS transistor 504, an M4 NMOS transistor 506, master latch circuitry 510, an M11 PMOS transistor 522, an M12 NMOS transistor 524, an M13 NMOS transistor 526, slave latch circuitry 530, and an inverter 540.

The D signal input is the input of the inverter 502, which includes transistors M1 and M2. The source of the inverter 502 is coupled to the node OFF, which is described below in FIG. 7A. The output of the inverter 502 is coupled to the M3 PMOS transistor 504 and the M4 NMOS transistor 506. The gate of the M3 PMOS transistor 504 is coupled to the CLK signal input. The gate of the M4 NMOS transistor 506 is coupled to the CLKB signal input.

The master latch circuitry 510 includes the inverter 512 and the inverter 514. The inverter 514 forms a feedback loop with the inverter 512, where the output of the inverter 512 is coupled to the input of the inverter 514 and the output of the inverter 514 is coupled to the input of the inverter 512. The inverter 512 corresponds to transistor M5 and M6. The inverter 514 corresponds to transistors M7-M10. The input of the inverter 512 is coupled to node A, which is described in FIG. 8A below. The source of the inverter 512 is also coupled to node OFF, which is described below in FIG. 7A. The output of the inverter 512 is coupled to node B, which is described below in FIG. 8A. The source of the inverter 514 is coupled to node OFF, which is described below in FIG. 7A. The PMOS gate of the inverter 514 is coupled to the CLKB signal input. The NMOS gate of the inverter 514 is coupled to the CLK signal input.

The M11 PMOS transistor 522 is in parallel to the M12 NMOS transistor 524 and the M13 NMOS transistor 526, which are in series. The gate of the M11 PMOS transistor 522 is coupled to the CLKB signal input. The gate of the M12 NMOS transistor 524 is coupled to the HOLDB signal input. The gate of the M13 NMOS transistor 526 is coupled to the CLK signal input.

The slave latch circuitry 530 includes the inverter 532 and the inverter 534. The inverter 534 forms a feedback loop with

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the inverter 532, where the output of the inverter 532 is coupled to the input of the inverter 534 and the output of the inverter 534 is coupled to the input of the inverter 532. The inverter 532 corresponds to transistor M14 and M15. The inverter 534 corresponds to transistors M18-21 and M31. The input of the inverter 532 is coupled to node C, which is described in FIG. 8B below. The source of the inverter 532 is also coupled to node SB, which is described below in FIGS. 7B-C. The output of the inverter 532 is coupled to node D, which is described below in FIG. 8B. The source of the inverter 534 is coupled to node SB, which is described below in FIGS. 7B-C. The PMOS gates of the inverter 534 are coupled to the HOLDB and CLK signal inputs. The NMOS gate of the inverter 534 is coupled to the CLKB signal input.

The output of the inverter 532 is coupled to the input of the inverter 540. The inverter 540 corresponds to transistors M16 and M17. The source of the inverter 540 is also coupled to node OFF, which is described below in FIG. 7A. The output of the inverter 540 is the Q signal output.

FIG. 6 depicts a CK portion 600 of the flip-flop circuitry in an exemplary implementation of the invention. The CK portion 600 of the flip-flop circuitry includes an inverter 602, an M24 PMOS transistor 604, an M25 PMOS transistor 606, an M26 NMOS transistor 608, an M32 NMOS transistor 610, and an M27 PMOS transistor 612.

The CK signal input is the input of the inverter 602, which includes transistors M22 and M23. The source of the inverter 602 is coupled to node OFF, which is described below in FIG. 7A. The output of the inverter 602 is coupled to the drain of the M24 PMOS transistor 604 and the node CLKB. The gate of the M24 PMOS transistor 604 is coupled to the HOLDB signal input. The output of the inverter 602 is also coupled to the M25 PMOS transistor 606 and the M26 NMOS transistor 608. The M25 PMOS transistor 606, the M26 NMOS transistor 608, and the M32 NMOS transistor 610 are coupled in series. The gate of the M32 NMOS transistor 610 is coupled to the HOLDB signal input.

The CLK signal output is coupled to the drain of the M25 PMOS transistor 606, the drain of the M26 NMOS transistor 608, and the drain of the M27 PMOS transistor 612. The gate of the M27 PMOS transistor 612 is coupled to the HOLDB signal input.

FIG. 7A depicts a sleep transistor 702 for the OFF node in an exemplary implementation of the invention. The sleep transistor 702 is an NMOS transistor that corresponds to transistor M28. The drain of the sleep transistor 702 is coupled to the OFF node. The gate of the sleep transistor 702 is coupled to the SLEEPB signal input. The source of the sleep transistor 702 is coupled to ground. In some embodiments, the OFF node can be separated into two or more nodes each having its own NMOS sleep transistor.

FIG. 7B depicts a sleep transistor 704 for the SB node in an exemplary implementation of the invention. The sleep transistor 704 is an NMOS transistor that corresponds to transistor M29. The drain of the sleep transistor 704 is coupled to the SB node. The gate of the sleep transistor 704 is coupled to the SLEEPB signal input. The source of the sleep transistor 704 is coupled to ground.

FIG. 7C depicts a sleep transistor 706 for the SB node in an exemplary implementation of the invention. The sleep transistor 706 is a PMOS transistor that corresponds to transistor M30. The source of the sleep transistor 706 is coupled to the SB node. The gate and drain of the sleep transistor 706 are coupled to ground.

FIG. 8A depicts circuitry 800 for the tristate inverter in the master latch in an exemplary implementation of the invention. The circuitry 800 for the master latch includes a PMOS

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transistor **802**, a PMOS transistor **804**, an NMOS transistor **806**, and an NMOS transistor **808** that are coupled together in series. The gates of the PMOS transistor **802** and the NMOS transistor **808** are coupled to the node B. The gate of the PMOS transistor **804** is coupled to the CLKB signal input. The gate of the NMOS transistor **806** is coupled to the CLK signal input. The drains of the PMOS transistor **804** and the NMOS transistor **806** are coupled to node A. The source of the NMOS transistor **808** is coupled to node OFF.

FIG. **8B** depicts circuitry **810** for the tristate inverter in the slave latch in an exemplary implementation of the invention. The circuitry **810** for the slave latch includes a PMOS transistor **812**, a PMOS transistor **814**, a PMOS transistor **816**, an NMOS transistor **818**, and an NMOS transistor **820**. The PMOS transistor **812** is coupled to the PMOS transistor **814** and the PMOS transistor **816** that are parallel to each other. The PMOS transistor **814** and the PMOS transistor **816** are coupled to the NMOS transistor **818**, which is also coupled to the NMOS transistor **820**.

The gates of the PMOS transistor **812** and the NMOS transistor **820** are coupled to the node D. The gate of the PMOS transistor **814** is coupled to the HOLDB signal input. The gate of the PMOS transistor **816** is coupled to the CLK signal input. The gate of the NMOS transistor **818** is coupled to the CLKB signal input. The drains of the PMOS transistor **814**, the PMOS transistor **816**, and the NMOS transistor **806** are coupled to node C. The source of the NMOS transistor **820** is coupled to node SB.

FIG. **9** depicts an illustration of the HOLDB and SLEEPB signals in an exemplary embodiment of the invention.

The operation begins with CK going to zero. This causes CLKB to be equal to VDD and CLK to be equal to zero, which isolates the slave latch circuitry **530** from the master latch circuitry **510**. The HOLDB signal goes to 0 to retain the state of the slave latch. The SLEEPB signal then goes to -0.3V. This shuts off transistor M28 in FIG. **7A**, which halts the leakage from all the circuits except in the slave latch circuitry **530**. When not in sleep mode, transistor M28 provides a low impedance path to ground.

The slave latch circuitry **530** is coupled to ground through the transistors M29 and M30, respectively depicted in FIGS. **7B** and **7C**. One purpose of transistor M29 is to provide a low impedance path to ground when not in sleep mode.

One purpose of transistor M30 is to provide a default moderate impedance path to ground when transistor M29 is off or in sleep mode. The leakage in the slave latch circuitry **530**, in going through transistor M30, causes node SB to rise. This provides a source bias to the slave NMOS transistors reducing the leakage through them and also reduces the voltage across the slave side to VDD-SB, which further reduces the leakage. Equilibrium is reached where the leakage cannot increase. Basically, the leakage is used to limit itself.

This embodiment uses the gated VDD solution because the voltage across the circuit is reduced to VDD-SB. This embodiment combines this gated VDD with the modulated back gate bias method because of the source bias SB but only for the NMOS transistors. This is accomplished without switching a lower VDD and driving a well. Thus, a simple process can be used. Also, this embodiment advantageously uses the moderate impedance transistor in a way that causes leakage to limit itself by reaching equilibrium.

FIGS. **10** and **11** disclose another embodiment for low leakage, data retention circuitry. In this embodiment, in a sleep state, the circuitries that do not require data retention are coupled to ground through a sleep transistor. The logic coupled to the transistors gated by the SLEEPB signal is shut off and draws minimal leakage. This process is accomplished

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by driving the SLEEPB signal below VSS by 0.3-0.4V. The HOLDB signal keeps the slave latch circuitry from changing state while the rest of the flip-flop comes out of the sleep state. The only part of the flip-flop still powered is the slave latch circuitry. The slave latch circuitry combines several techniques to minimize leakage.

FIG. **10** depicts circuitry **1000** for low leakage and data retention in an exemplary embodiment of the invention. The circuitry **1000** includes the inverter **1002**, the master latch circuitry **1010**, the slave latch circuitry **1020**, the inverter **1032**, the inverter **1034**, the sleep transistors **1042**, **1044**, **1046**, and **1048**, the inverter **1052**, and the inverter **1054**.

The D input is the input for the inverter **1002**. The master latch circuitry **1010** includes the transmission gate **1012**, the inverter **1014**, the transmission gate **1016**, and the inverter **1018**. The output of the inverter **1002** is coupled to the left contact of the transmission gate **1012**. The right contact of the transmission gate **1012** is coupled to the input of the inverter **1014** and the left contact of the transmission gate **1016**. The output of the inverter **1014** is coupled to the D input of the slave latch circuitry **1020** and the input of the inverter **1018**. The output of the inverter **1018** is coupled to the DB input of the slave latch circuitry **1020** and the right contact of the transmission gate **1016**.

The SLEEPB signal input is coupled to the gates for the SL1 sleep transistor **1042**, the SL2 sleep transistor **1044**, the SL3 sleep transistor **1046**, the SL4 sleep transistor **1048**, and the SLEEPB input of the slave latch circuitry **1020**. The SL1 sleep transistor **1042** is coupled to the inverter **1002** and ground. The SL2 sleep transistor **1044** is coupled to the inverter **1052**, the inverter **1054**, and ground. The SL3 sleep transistor **1046** is coupled to the inverter **1014**, the inverter **1018**, and ground. The SL4 sleep transistor **1048** is coupled to the inverter **1032**, the inverter **1034**, and ground. In some embodiments, the SL1 sleep transistor **1042**, the SL2 sleep transistor **1044**, the SL3 sleep transistor **1046**, and the SL4 sleep transistor **1048** can each be separated into two or more node each having its own NMOS sleep transistor.

The CK signal is the input of the inverter **1052**. The output of the inverter **1052** is coupled to the transmission gate **1012**, the transmission gate **1016**, and the input of the inverter **1054**. The output of the inverter **1054** is coupled to the transmission gate **1012**, the transmission gate **1016**, and the CLK input of the slave latch circuitry **1020**. The HOLDB signal input is coupled to the HOLDB input of the slave latch circuitry **1020**. The output of the slave latch circuitry **1020** is coupled to the input of the inverter **1032**. The output of the inverter **1032** is coupled to the input of the inverter **1034**. The output of the inverter **1034** is the Q signal.

FIG. **11** depicts slave latch circuitry **1020** in an exemplary embodiment of the invention. The slave latch circuitry **1020** includes D1 transistor **1102**, D2 transistor **1104**, DH transistor **1106**, DSL sleep transistor **1108**, stack transistors **1110**, stack transistors **1120**, D1B transistor **1132**, D2B transistor **1134**, DHB transistor **1136**, and sleep transistor **1138**.

The D1 transistor **1102**, the D2 transistor **1104**, the DH transistor **1106**, and the DSL sleep transistor **1108** are coupled to each other in series with the sleep transistor **1108** coupled to ground. The gate of the D1 transistor **1102** is coupled to the CLK signal input. The gate of the D2 transistor **1104** is coupled to the D signal input. The gate of the DH transistor **1106** is coupled to the HOLDB signal input. The gate of the sleep transistor **1108** is coupled to the SLEEPB signal input.

The stack transistors **1110** comprise P1 transistor **1112**, P0 transistor **1114**, N1 transistor **1116**, and N0 transistor **1118**. The P1 transistor **1112**, the P0 transistor **1114**, the N1 tran-

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sistor **1116**, and the **N0** transistor **1118** are coupled to each other in series with the **N0** transistor **1118** coupled to ground. The gates of the **P1** transistor **1112**, the **P0** transistor **1114**, the **N1** transistor **1116**, and the **N0** transistor **1118** are coupled to the **LAT** signal input. The drains of the **P0B** transistor **1124** and the **N1B** transistor **1126** are coupled to the **LAT** signal input.

The stack transistors **1120** comprise **P1B** transistor **1122**, **P0B** transistor **1124**, **N1B** transistor **1126**, and **N0B** transistor **1128**. The **P1B** transistor **1122**, the **P0B** transistor **1124**, the **N1B** transistor **1126**, and the **N0B** transistor **1128** are coupled to each other in series with the **N0B** transistor **1128** coupled to ground. The gates of the **P1B** transistor **1122**, the **P0B** transistor **1124**, the **N1B** transistor **1126**, and the **N0B** transistor **1128** are coupled to the **LATB** signal input. The drains of the **P0** transistor **1114** and the **N1** transistor **1116** are coupled to the **LATB** signal input.

In operation, the logic coupled to the transistors gated by the **SLEEPB** signal is shut off and draws minimal leakage. This process is accomplished by driving the **SLEEPB** signal below **VSS** by 0.3-0.4V. The **HOLDB** signal keeps the slave latch circuitry **1020** from changing state while the rest of the flip-flop comes out of the sleep state. The only part of the flip-flop still powered is the slave latch circuitry **1020**. The slave latch circuitry **1020** combines several techniques to minimize leakage. Transistors not necessary for state retention (stacks with **CLK**) have sleep transistors to shut off leakage (gated by the **SLEEPB** signal).

The 8 transistors in the stack transistors **1110** and **1120** use two techniques to reduce leakage. The first technique used is transistor stacking, which is also called self-reverse bias. The **N0** transistor **1118** and the **N1** transistor **1116** will have some small leakage even when the gate is at 0V. As a result, **VNN1** will be at a positive voltage. This causes **VGS(N1)** and **VBS(N1)** to be negative, and **VDS(N1)** to decrease. Consequently, the leakage current is reduced in **N0** transistor **1118** and the **N1** transistor **1116**. The same effect occurs on **N0B** transistor **1128**, **N1B** transistor **1126**, **P0** transistor **1114**, **P1** transistor **1112**, **P0B** transistor **1124**, and **P1B** transistor **1122**.

The second technique is called multiple threshold transistors. Increasing channel length of MOS transistors increases the threshold of the devices without any change in process complexity. The **N0** transistor **1118**, the **N1** transistor **1116**, the **N0B** transistor **1128**, and the **N1B** transistor **1126** have increased channel length, which raises **VTH** and reduces leakage current.

This embodiment reduces leakage by a factor of 25 over a current standard cell **D** flip-flop.

I/O Pad—FIG. 12

In some embodiments, a programmable general purpose input and output (I/O) padcell includes built in-level shifters and isolation that interface with the chip core logic. In these embodiments, a level shifter can be controlled to retain data.

FIG. 12 depicts circuitry **1200** for a level shifter for an I/O pad in an exemplary embodiment of the invention. The circuitry **1200** includes **MP2** transistor **1202**, **MP3** transistor **1204**, **M3** transistor **1206**, **M4** transistor **1208**, **M1** transistor **1210**, **M0** transistor **1212**, **M5** transistor **1214**, **M2** transistor **1216**, and an inverter **1218**.

The circuitry **1200** is for a latching level shifter. The **M3** transistor **1206** and the **M4** transistor **1208** are “native” cascode devices. The **M3** transistor **1206** and the **M4** transistor **1208** are also known as depletion-mode transistors. The **M3** transistor **1206** and the **M4** transistor **1208** are used to allow thin gate devices to be used in the input stage. This allows large voltage ratios between the **VDD** and the **V310**. The **M0** transistor **1212** and the **M1** transistor **1210** are output latching

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devices that allow the level shifter to retain the state when both **IN** and **INB** are 0. Thus, **IN** and **INB** control data retention.

In some embodiments, the gates of the **M3** transistor **1206** and the **M4** transistor **1208** are coupled to other transistors connected to the cascode voltage.

The following truth table is for circuitry **1200**.

IN	INB	OUT
0	0	Retain last state
0	1	0
1	0	1
1	1	Illegal

There will be setup time requirements for any signal compared to **SLPB**. If level shifters are used with an **SRAM** cell built into the output stage, the two inputs can be removed anytime after the output latch has flipped to a new state. Both 1.2V inputs to the level shifter cannot go to **VDD**. This can be prevented by including an inverter. If both the inverter and the level shifter have **SLPB** transistors, there is a potential timing race if **SLPB** goes to **VSS** with **VDD** high. In this case, the level shifters should be off before the output of the inverter drifts to **VDD**. In some embodiments, the **M5** transistor **1214** and the **M2** transistor **1216** can be configured to withstand greater voltages.

In some embodiments, the sources of the **M5** transistor **1214** and the **M2** transistor **1216** can be coupled to a common **SLEEPB** transistor **1240** to further reduce leakage. In one embodiment, the width of the **SLEEPB** transistor **1240** is 4 micrometers, and the length is 0.13 micrometers. The following truth table is for circuitry **1200** including this common **SLEEPB** transistor **1240**:

SLEEPB	IN	INB	OUT
1	0	0	Retain state (Data Retention)
1	0	1	0
1	1	0	1
1	1	1	Illegal
0	X	X	Retain State

In some embodiments, the **SLEEPB**=0 input state should be understood to include the **SLEEPB** voltage being below 0V (E.g. -0.35V generated by a leakage optimization circuit).

In this extension to FIG. 12 (and the above truth table), the two Data Retention states may be operated independently, sequentially or simultaneously. This is beneficial when the **SLEEPB** input is used to control/limit leakage power while the **IN/INB**=00 state is used for data retention. This is because the **SLEEPB** voltage comes from a charge pump and takes some time to transition from **Vdd** (=1) to the Data Retention mode.

The above description is illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

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While this invention has been particularly shown and described with references to example embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

What is claimed is:

1. An integrated circuit comprising:
 - a plurality of power islands having associated power consumptions, each of the power islands including circuitries and sleep transistors in coupled relation with the circuitries, and the sleep transistors being included within the integrated circuit to facilitate reduction of power consumed by the circuitries;
 - a power island manager configured to dynamically change the power consumptions based on needs and operation of the integrated circuit, the power island manager in communication with at least one of the power islands; and
 - an adaptive leakage controller configured to control change of a variable voltage to be applied to the sleep transistors, and the power island manager configured to generate the variable voltage based on a control signal received from the adaptive leakage controller.
2. The integrated circuit as claimed in claim 1 wherein the at least one of the power islands can be put to sleep and taken out of sleep at different times.
3. The integrated circuit as claimed in claim 2 wherein the power island manager includes a state machine to control when the at least one of the power islands is put to sleep and when the at least one of the power islands is taken out of sleep.
4. The integrated circuit as claimed in claim 1 wherein the power islands are delineated based on functional intellectual property units of the integrated circuit.
5. The integrated circuit as claimed in claim 1 wherein the power islands are delineated by memory, logic and third party intellectual property.
6. The integrated circuit as claimed in claim 1 wherein the variable voltage is an optimum voltage.
7. The integrated circuit as claimed in claim 6 wherein the optimum voltage is dependent upon both process variation and temperature variation.

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8. The integrated circuit as claimed in claim 6 wherein the optimum voltage is generated by a sleep generator within the power island manager.

9. The integrated circuit as claimed in claim 8 wherein the sleep generator comprises a charge pump.

10. The integrated circuit as claimed in claim 1 wherein the variable voltage is generated by a sleep generator within the power island manager.

11. The integrated circuit as claimed in claim 10 wherein the sleep generator comprises a charge pump.

12. The integrated circuit as claimed in claim 11 wherein the control signal is a digital signal.

13. The integrated circuit as claimed in claim 1 further comprising a central processing unit separate from and in communication with the power island manager.

14. The integrated circuit as claimed in claim 13 further comprising another power island manager, the central processing unit separate from and in communication with the another power island manager.

15. An integrated circuit comprising:

a plurality of power islands having associated power consumptions, and the power consumptions being dynamically changeable based on needs and operation of the integrated circuit, and each of the power islands including circuitries and sleep transistors in coupled relation with the circuitries, and the sleep transistors being included within the integrated circuit to facilitate reduction of power consumed by the circuitries;

a sleep generator including a charge pump to generate a variable voltage to be applied to the sleep transistors; and

an adaptive leakage controller configured to control change of the variable voltage by providing a digital control signal to the sleep generator.

16. The integrated circuit as claimed in claim 15 wherein the power islands are delineated based on functional intellectual property units of the integrated circuit.

17. The integrated circuit as claimed in claim 15 wherein the power islands are delineated by memory, logic and third party intellectual property.

18. The integrated circuit as claimed in claim 15 wherein the variable voltage is an optimum voltage.

19. The integrated circuit as claimed in claim 18 wherein the optimum voltage is dependent upon both process variation and temperature variation.

* * * * *

EXHIBIT E



US008854077B2

(12) **United States Patent**
Hoberman et al.

(10) **Patent No.:** **US 8,854,077 B2**

(45) **Date of Patent:** **Oct. 7, 2014**

(54) **LOW LEAKAGE AND DATA RETENTION CIRCUITRY**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 108 days.

(21) Appl. No.: **13/569,613**

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(60) Continuation of application No. 13/074,291, filed on Mar. 29, 2011, now Pat. No. 8,253,438, which is a continuation of application No. 12/542,352, filed on Aug. 17, 2009, now Pat. No. 7,940,081, which is a continuation of application No. 12/284,311, filed on Sep. 19, 2008, now Pat. No. 7,592,837, which is a continuation of application No. 11/998,725, filed on Nov. 30, 2007, now Pat. No. 7,443,197, which is a continuation of application No. 11/732,181, filed on Apr. 2, 2007, now Pat. No. 7,348,804, which is a division of application No. 11/041,687, filed on Jan. 20, 2005, now Pat. No. 7,227,383.

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H03K 19/17 (2006.01)

(52) **U.S. Cl.**
USPC 326/27; 326/38; 326/81

(58) **Field of Classification Search**
CPC H03K 19/00361; H03K 19/0016; H03K 17/16
USPC 326/21, 27, 37-41, 80-83
See application file for complete search history.

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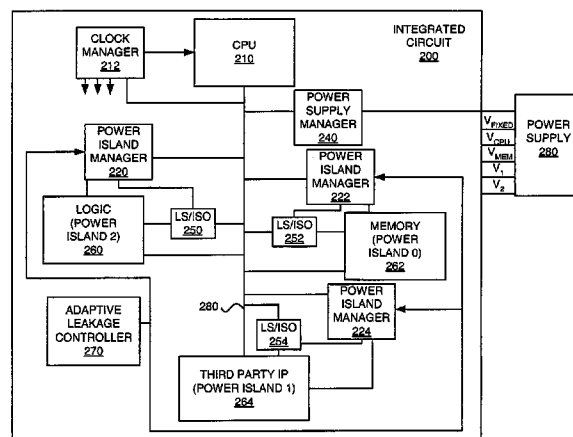
Primary Examiner — Don Le

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(57) **ABSTRACT**

An integrated circuit includes first circuitry and sleep transistor circuitry. The first circuitry receives input signals and processes the input signals. The first circuitry also retains data in a sleep state that has low leakage. The sleep transistor circuitry is coupled to the first circuitry and receives a sleep signal that has a negative voltage. The sleep circuitry reduces power consumption of the first circuitry in the sleep state to have low leakage based on the sleep signal while retaining the data in the first circuitry.

18 Claims, 12 Drawing Sheets



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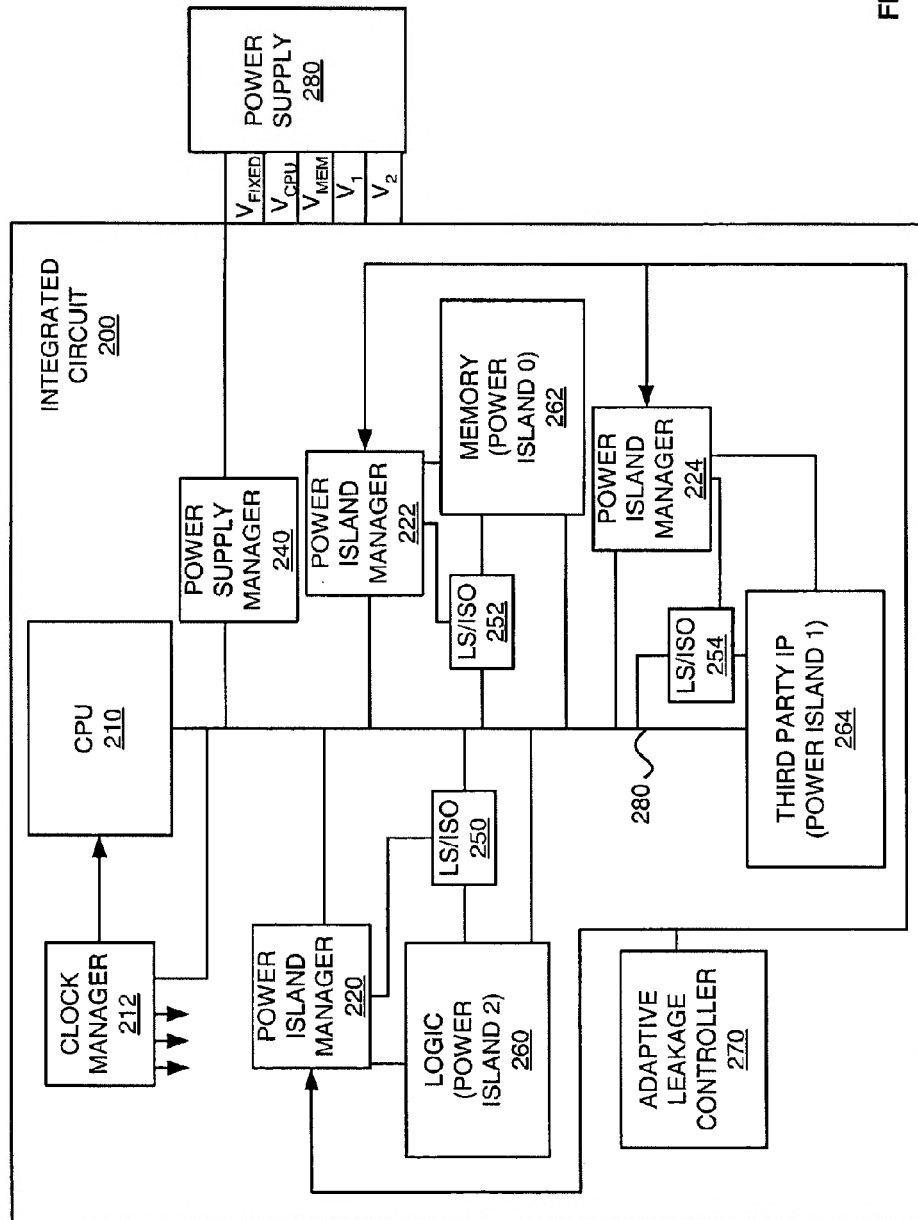


FIG. 2

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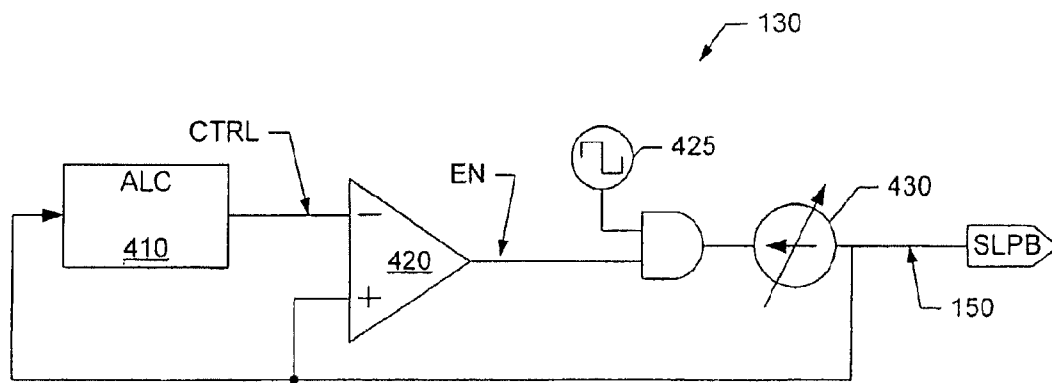


FIG. 2A

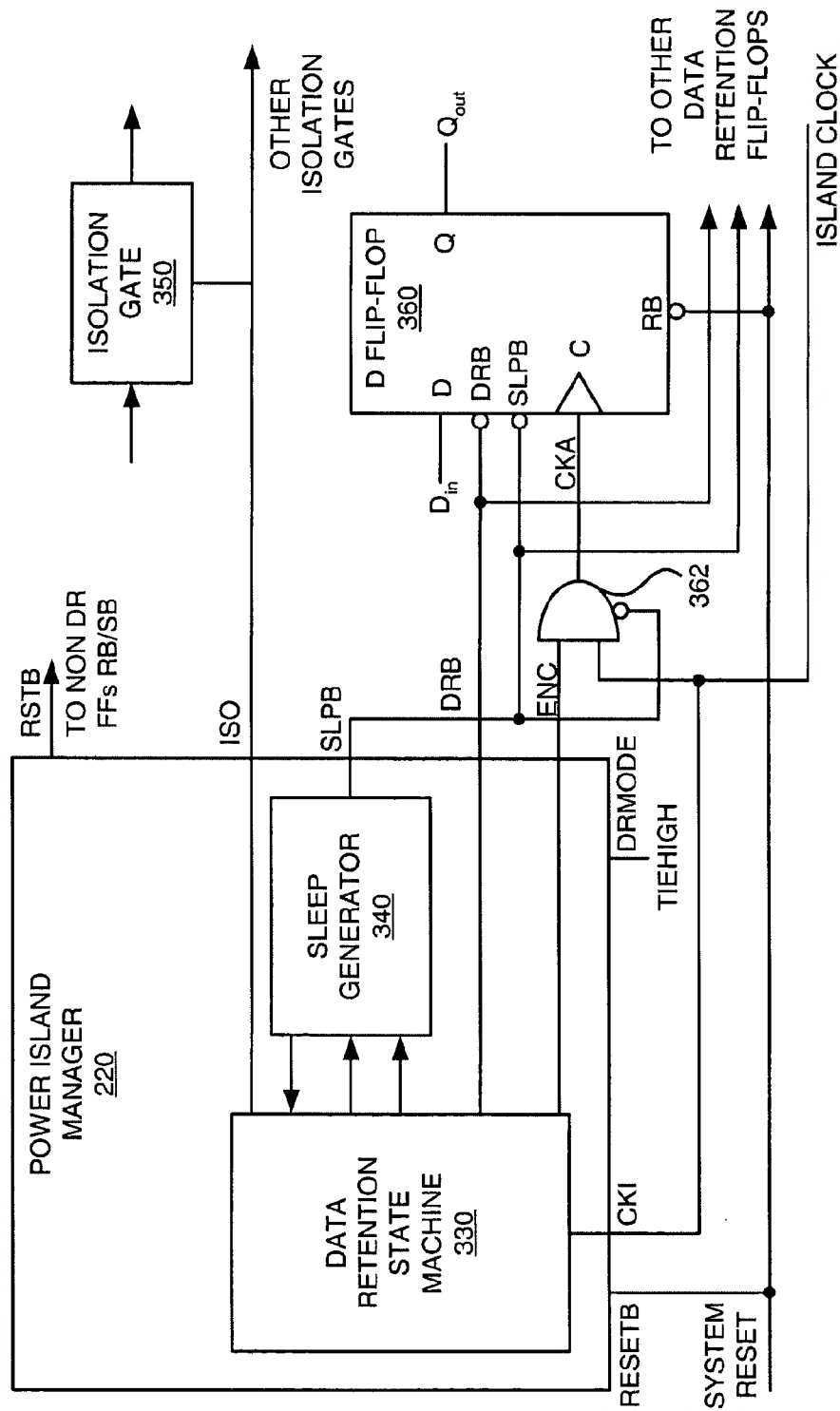


FIG. 3

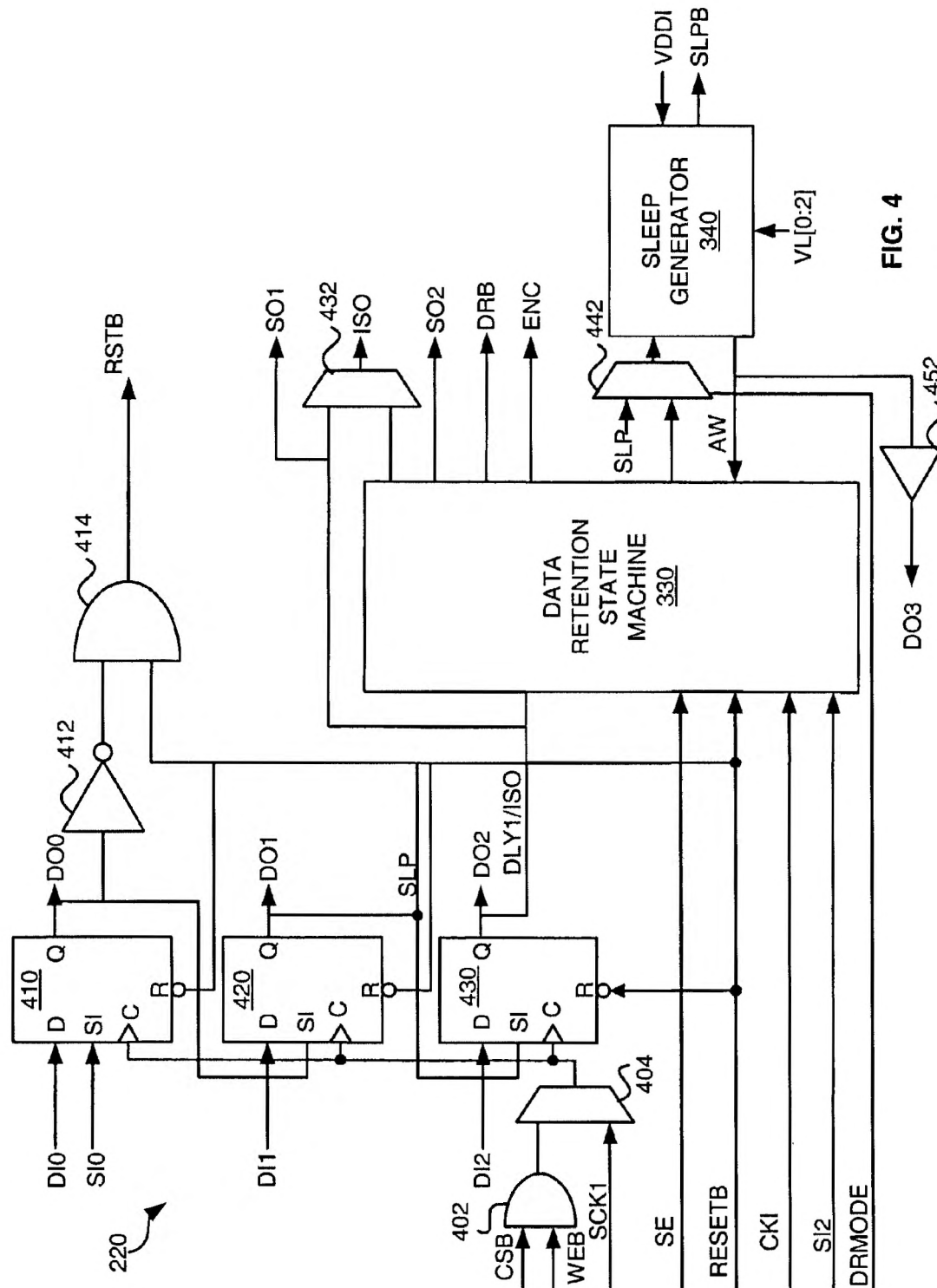


FIG. 4

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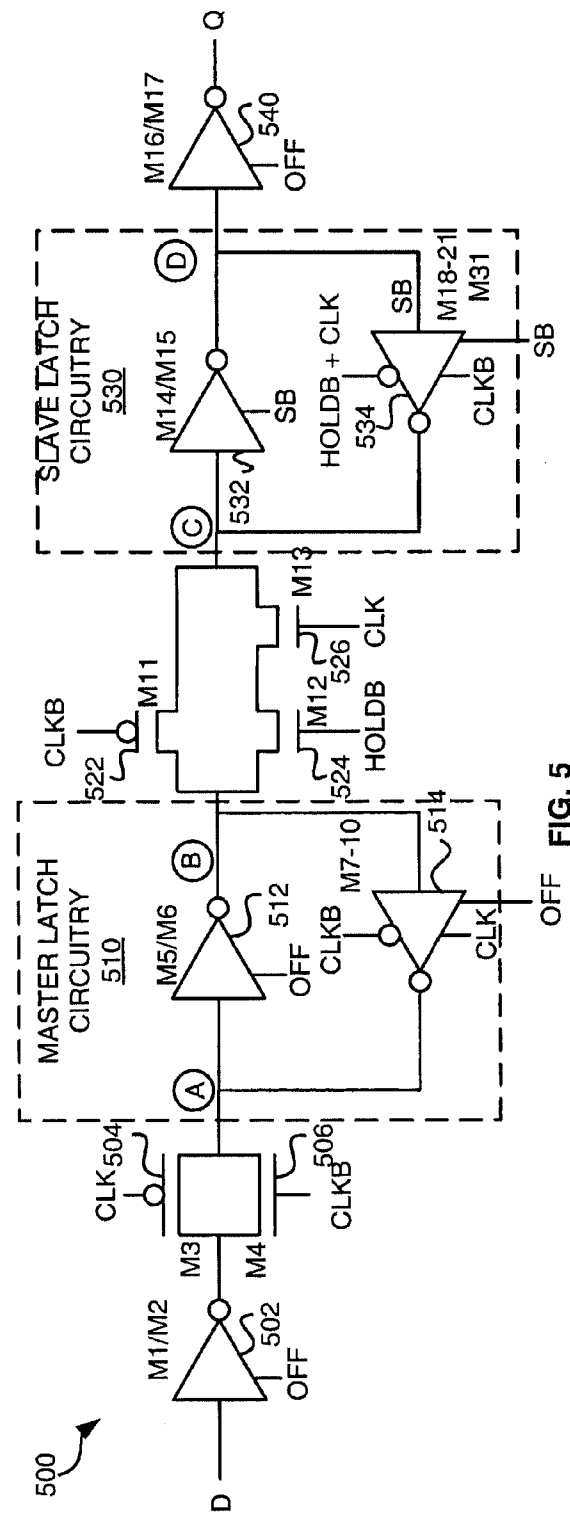


FIG. 5

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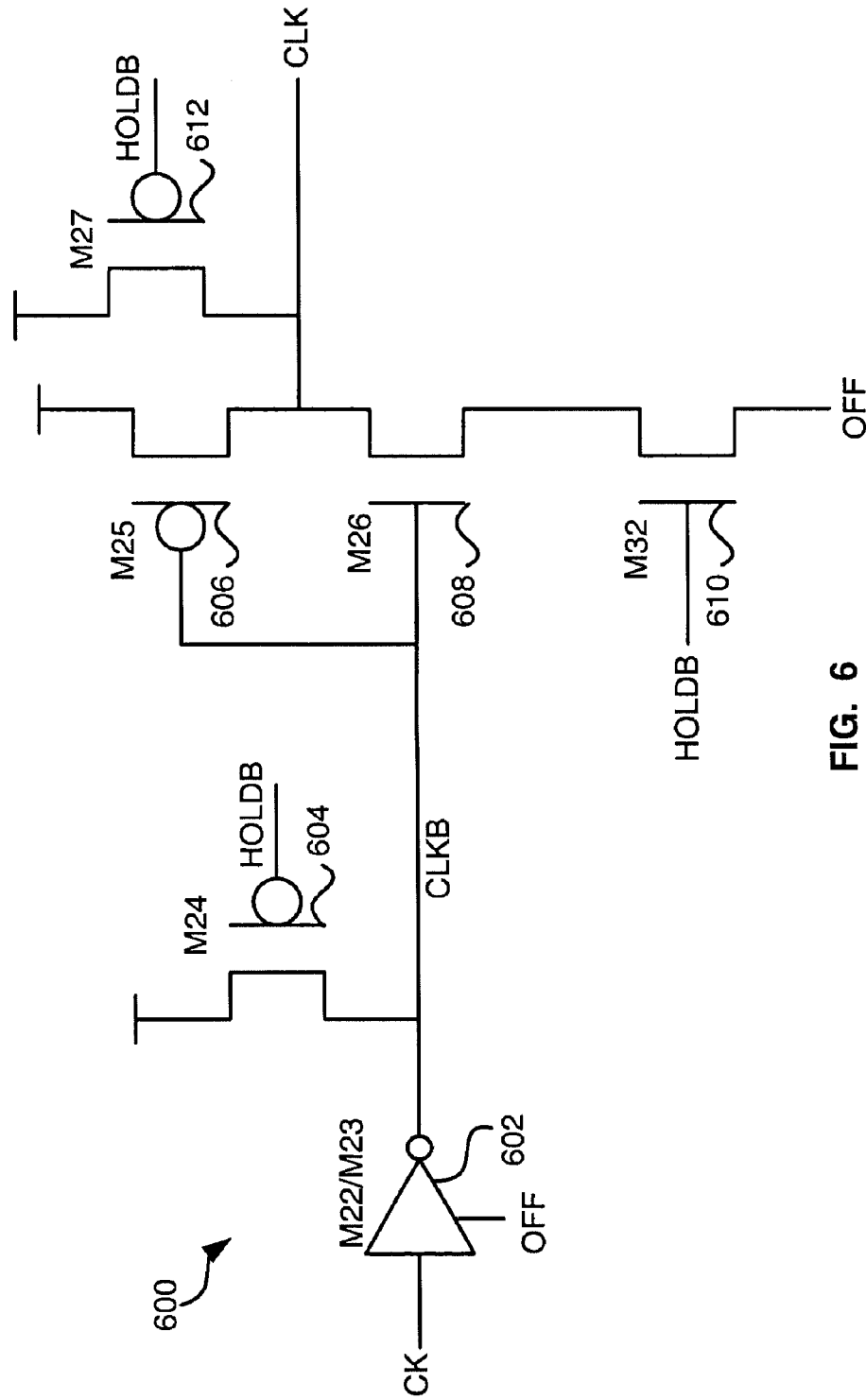


FIG. 6

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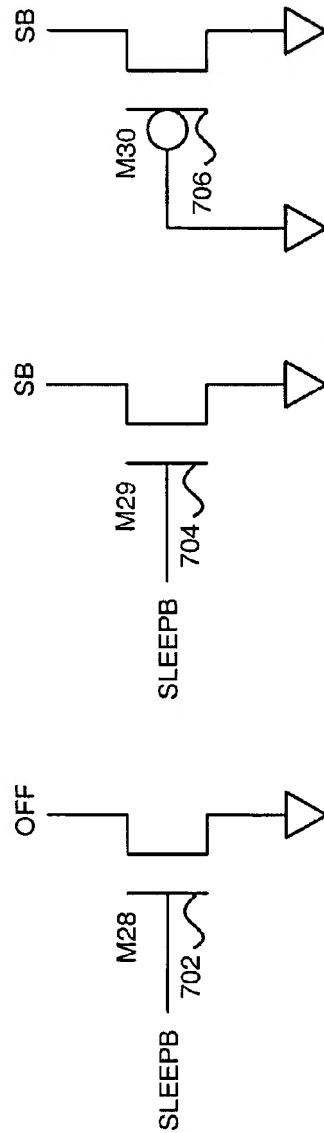


FIG. 7A

FIG. 7B

FIG. 7C

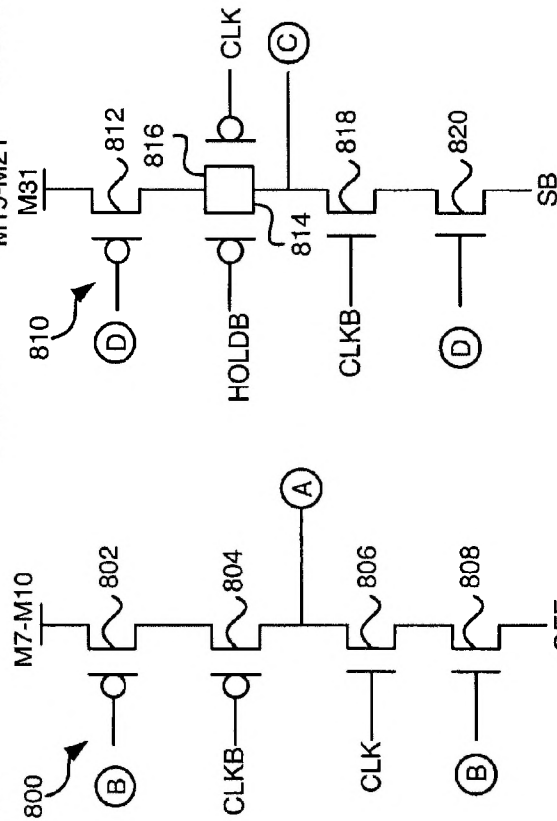


FIG. 8A

FIG. 8B

FIG. 8C

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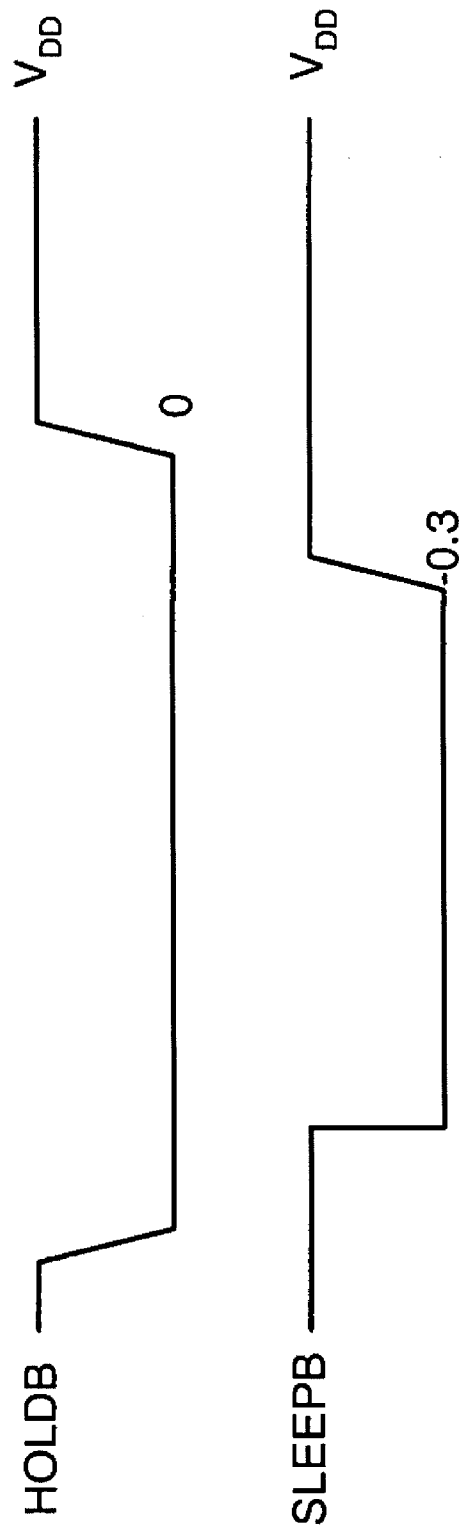


FIG. 9

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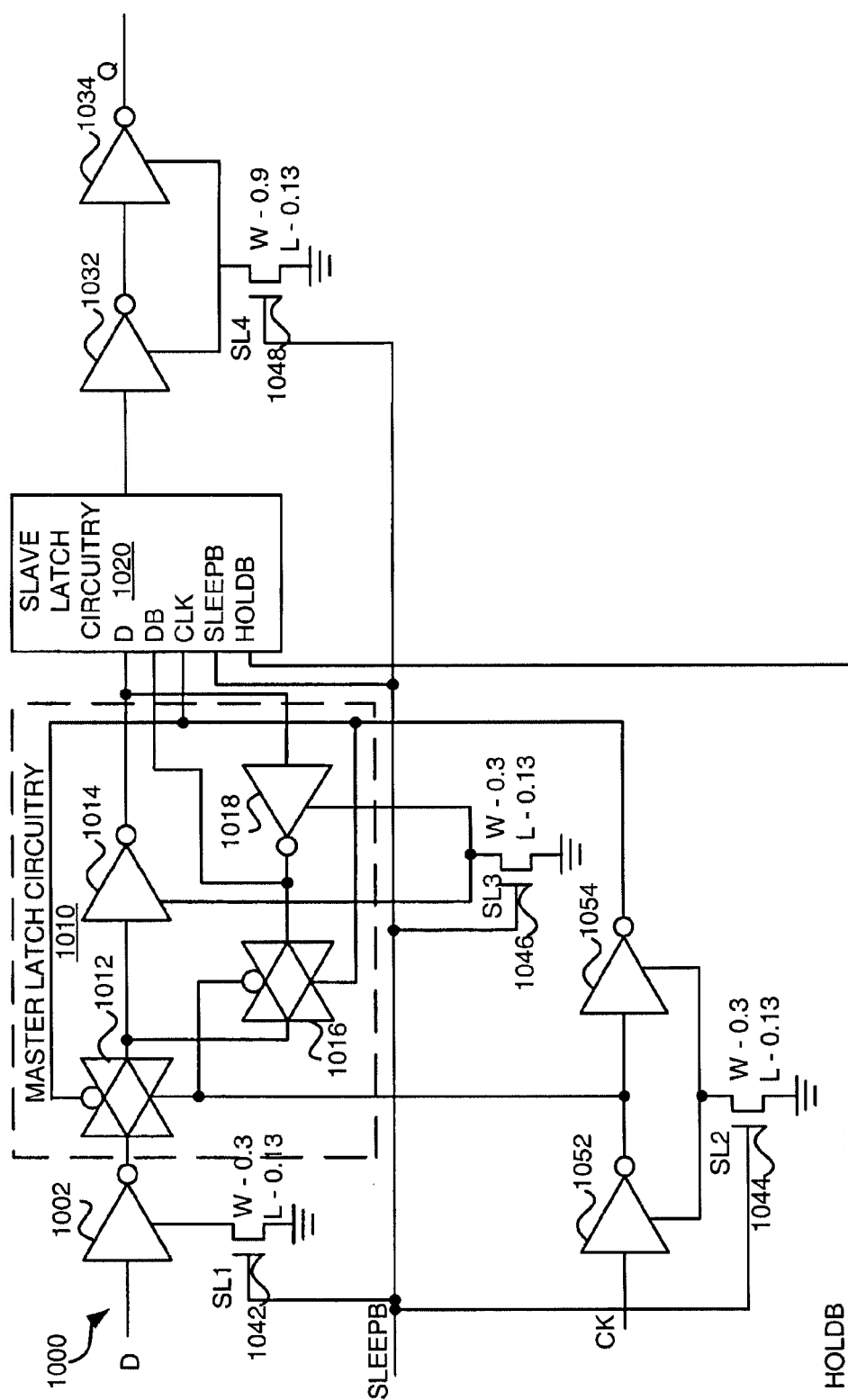


FIG. 10

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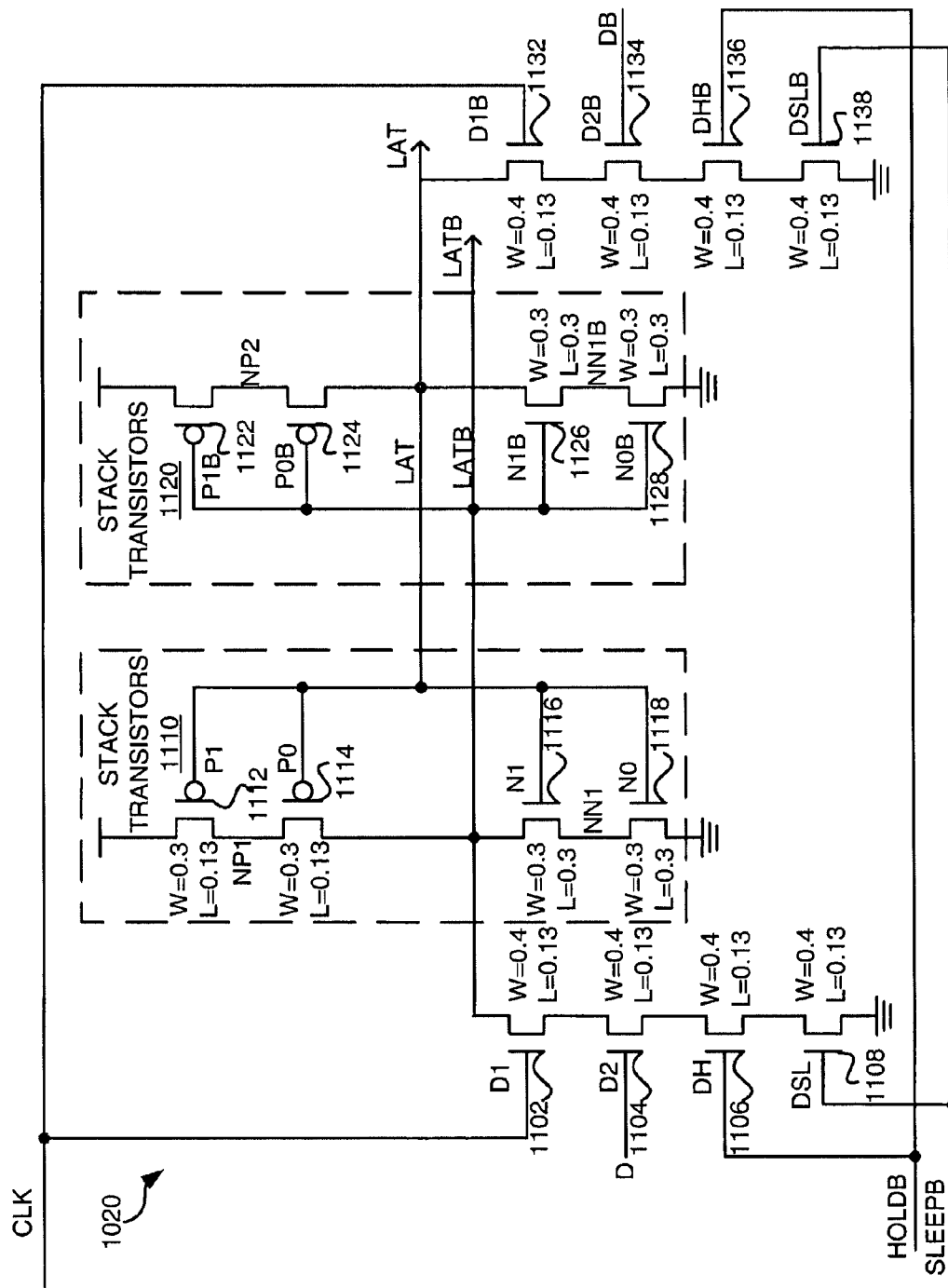


FIG. 11

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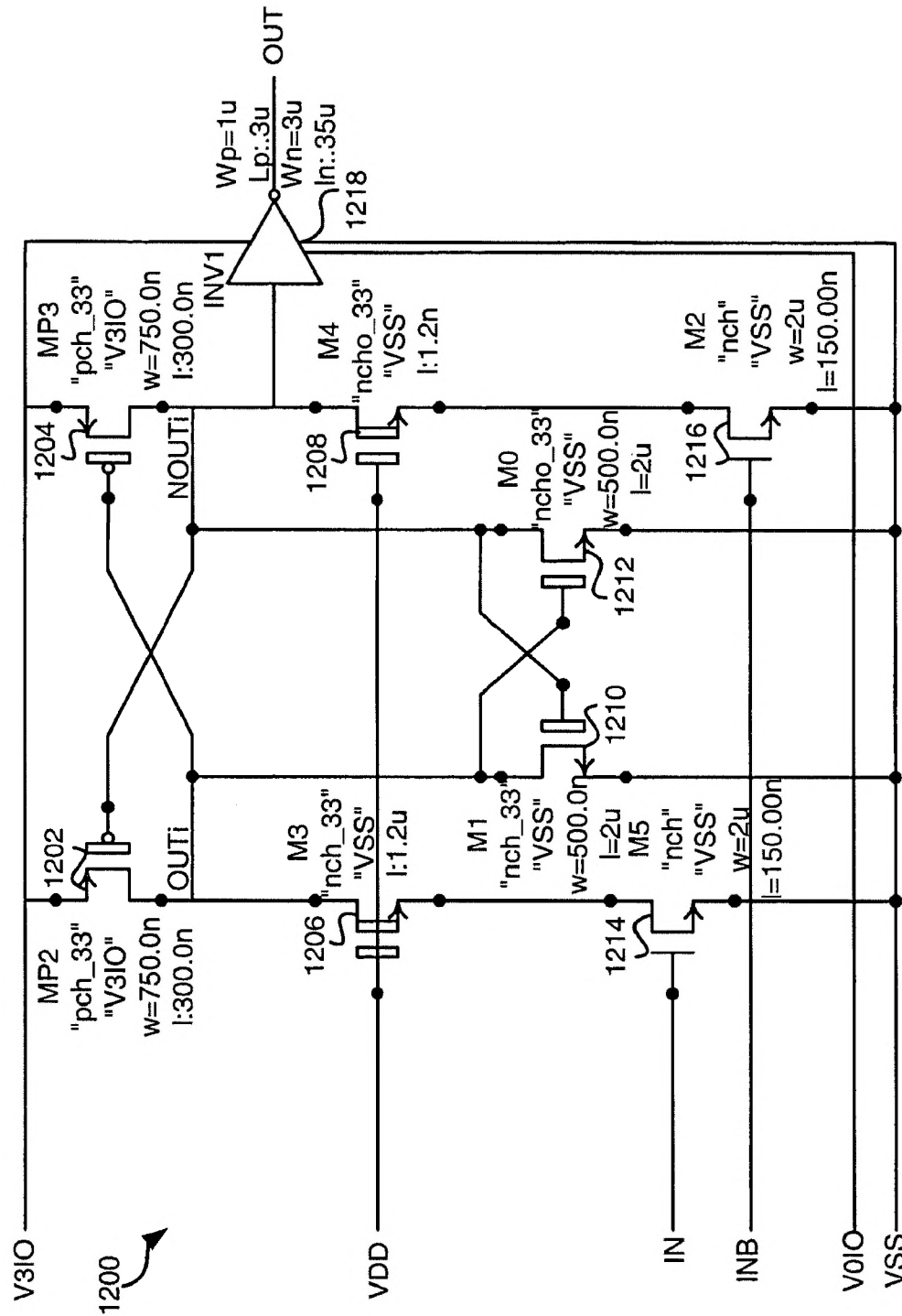


FIG. 12

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**LOW LEAKAGE AND DATA RETENTION
CIRCUITRY****RELATED APPLICATIONS**

This application is a continuation of U.S. application Ser. No. 13/074,291, filed Mar. 29, 2011 now U.S. Pat. No. 8,253,438, which is a continuation of U.S. application Ser. No. 12/542,352, filed Aug. 17, 2009 (now U.S. Pat. No. 7,940,081), which is a continuation of U.S. application Ser. No. 12/284,311, filed Sep. 19, 2008 (now U.S. Pat. No. 7,592,837), which is a continuation of U.S. application Ser. No. 11/998,725, filed Nov. 30, 2007 (now U.S. Pat. No. 7,443,197), which is a continuation of U.S. application Ser. No. 11/732,181, filed Apr. 2, 2007 (now U.S. Pat. No. 7,348,804), which is a divisional and claims the priority benefit of U.S. application Ser. No. 11/041,687 filed Jan. 20, 2005 (now U.S. Pat. No. 7,227,383), which claims the priority benefit of U.S. Provisional Application No. 60/546,574, filed Feb. 19, 2004 and U.S. Provisional Application No. 60/586,565, filed Jul. 9, 2004.

The entire teachings of the above applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION**1. Field of the Invention**

The present invention relates generally to integrated circuits, and more particularly to low leakage and data retention circuitry.

2. Description of the Related Art

Most integrated circuits have a design goal to reduce the overall power consumption. The total power consumed by an integrated circuit includes dynamic power consumption and standby leakage current consumption. The challenge in designing an integrated circuit is to reduce the dynamic power and leakage power, while maintaining performance and cost goals for the integrated circuit.

In complementary metal oxide semiconductors (CMOS), various types of leakage occur such as pn junction reverse-bias current, subthreshold leakage, oxide tunneling current, gate current due to hot-carrier injection, gate-induced drain leakage, and channel punch through current. When the threshold voltage for a CMOS transistor is reduced for higher performance, the leakage power is significant in the total power consumption of the CMOS circuit.

There are two approaches in reducing the leakage power for CMOS circuits. The first approach is a process level technique that controls the doping profile of the transistor. The other approach is a circuit level technique where voltages at the different device terminals such as the drain, source, gate, and body are controlled. Some circuit level techniques are discussed below.

One circuit level technique is stacking transistors, which is also called self-reverse bias. When more than one transistor in a stack of series-connected transistors is turned off, the subthreshold leakage current is reduced. One problem with the transistor stack is that only a three times reduction in leakage current is achieved. Another circuit level technique is a multiple threshold voltage design. Both high- and low-threshold transistors are on the same chip to deal with the leakage problem. The high-threshold transistors suppress the subthreshold leakage current. The low-threshold transistors are used to achieve higher performance. One problem with a multiple threshold design is that process complexity and costs are increased.

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Another circuit level technique is a multiple body bias in which the body voltage is changed to modify the threshold voltage. If separate body biases are applied to different NMOS transistors, the transistor cannot share the same well, which requires triple well technologies. One problem is that well biasing consumes a lot of chip area and requires extra power supplies for each cell. This technique also increases process complexity and the leakage reduction is not optimal.

Another technique for reducing leakage is a sleep transistor. FIG. 1 depicts prior art circuitry including a sleep transistor. For NMOS sleep transistors, one or more NMOS transistors are added to logic gates in series with the cell transistors to VSS. The NMOS sleep transistors act as a switch to turn on and off the logic gate. In FIG. 1, the sleep transistor **130** is turned on (gate to VDD) during normal cell operation. When the cell is idle, the sleep transistor **130** is turned off (gate tied to VSS) to reduce the leakage current of the cell. Sleep transistors can also be PMOS transistors. One problem with sleep transistors is that if all logic has sleep transistors, the logic will lose their state information.

SUMMARY OF THE INVENTION

In an exemplary embodiment of the presently disclosed invention, a data retention circuit is provided. The exemplary circuit includes an input/output pad cell that itself includes level shifter circuitry, the level shifter circuitry having inputs and outputs. Output latching circuitry is also provided as a part of the data retention circuit. The output latching circuitry includes two transistors. The transistors are coupled to the outputs of the level shifter circuitry and retain a state of the level shifter circuitry based on the state of the inputs. A leakage optimization circuit is also included, the leakage optimization circuit is configured to simultaneously decrease leakage power in conjunction with the state retention of the output latching circuitry.

In another embodiment of the presently disclosed invention, a system for controlling power consumption within an integrated circuit is disclosed. The system includes a power island, the power island includes a first circuit. The first circuit of the power island is configured to receive an input signals and a hold signal. The circuit is further configured to process the input signals and retain data in a sleep state having low leakage. The first circuit is further configured to retain the data based on the hold signal. The system further includes a sleep transistor, which is coupled to the first circuit. The sleep transistor is configured to receive a negative voltage sleep signal and reduce power consumption of the first circuit in the sleep state. As a result, the first circuit has low leakage based on the sleep signal while simultaneously retaining the data.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing will be apparent from the following more particular description of example embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating embodiments of the present invention.

FIG. 1 is an illustration of circuitry including a sleep transistor in the prior art;

FIG. 2 is an illustration of an integrated circuit with a power supply in an exemplary implementation of the invention;

FIG. 2A is a block diagram of a leakage manager system for minimizing state leakage of a logic gate by application of a negative voltage to a sleep transistor.

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FIG. 3 is an illustration of a power island manager with an isolation gate and a D flip-flop in an exemplary implementation of the invention;

FIG. 4 is an illustration of a power island manager in an exemplary implementation of the invention;

FIG. 5 is an illustration of a D/Q portion of flip-flop circuitry in an exemplary implementation of the invention;

FIG. 6 is an illustration of a CK portion of flip-flop circuitry in an exemplary implementation of the invention;

FIG. 7A is an illustration of a sleep transistor for an OFF node in an exemplary implementation of the invention;

FIG. 7B is an illustration of a sleep transistor for an SB node in an exemplary implementation of the invention;

FIG. 7C is an illustration of a moderate impedance transistor for an SB node in an exemplary implementation of the invention;

FIG. 8A is an illustration of circuitry for a tristate inverter in the master latch in an exemplary implementation of the invention;

FIG. 8B is an illustration of circuitry for a tristate inverter in the slave latch in an exemplary implementation of the invention;

FIG. 9 is an illustration of a HOLDB and SLEEPB signals in an exemplary implementation of the invention;

FIG. 10 is an illustration of circuitry for low leakage and data retention in an exemplary implementation of the invention;

FIG. 11 is an illustration of slave latch circuitry in an exemplary implementation of the invention; and

FIG. 12 is an illustration of circuitry for a level shifter for an I/O pad in an exemplary implementation of the invention.

DETAILED DESCRIPTION OF THE INVENTION

A description of example embodiments of the invention follows.

As shown in the exemplary drawings wherein like reference numerals indicate like or corresponding elements among the figures, exemplary embodiments of a system and method according to the present invention are described below in detail. It is to be understood, however, that the present invention may be embodied in various forms. Therefore, specific details disclosed herein are not to be interpreted as limiting, but rather as a basis for the claims and as a representative basis for teaching one skilled in the art to employ the present invention in virtually any appropriately detailed system, structure, method, process or manner.

Power Island Manager—FIGS. 2-4

In some embodiments, an integrated circuit can be delineated into power islands. Power consumption can then be controlled within the power island. A power island manager provides control signals to the power island to control power consumption of the power island. In some embodiments, the low leakage, data retention circuitry is located within the power islands.

FIG. 2 depicts an illustration of an integrated circuit 200 with a power supply 280 in an exemplary implementation of the invention. The integrated circuit 200 includes a central processing unit (CPU) 210, a clock manager 212, power island managers 220, 222, and 224, a power supply manager 240, level shifter/isolation gates (LS/ISO) 250, 252, and 254, logic (power island 2) 260, memory (power island 0) 262, third party intellectual property (IP) (power island 1) 264, adaptive leakage controller (ALC) 270, and bus 280.

A power island is any section, delineation, partition, or division of an integrated circuit where power consumption is controlled within the section, delineation, partition, or divi-

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sion. In some embodiments, the power islands are delineated based on geographic factors of the integrated circuit. In some embodiments, the power islands are delineated based on functional IP units of the integrated circuit 200. In this example depicted in FIG. 2, power islands are delineated by memory 262, logic 260, and third party IP 264. Power islands are discussed in further detail in pending U.S. application Ser. No. 10/840,893 entitled “Managing Power on Integrated Circuits Using Power Islands” filed on May 7, 2004, which is hereby incorporated by reference.

The power island managers 220, 222, and 224 are any circuitry, device, or system configured to provide control signals to a power island to control power within the power island. The power island managers 220, 222, and 224 can dynamically change the power consumption of the power islands based on the needs and operation of the integrated circuit 200. The power island managers 220, 222, 224 may select a clock, change clock frequency, or modify the voltage within the power island to control the power consumption of the power island.

The ALC 270 provides control signals to compensate for process and temperature variation to provide the optimum voltage to be applied to sleep transistors in the power islands. The ALC 270 is described in further detail U.S. patent application Ser. No. 10/996,739 entitled “Systems and Methods for Minimizing Static Leakage of an Integrated Circuit” filed on Nov. 17, 2004.

FIG. 2A is a block diagram of a leakage manager system 290 for minimizing static leakage of a logic gate by application of a negative voltage to a sleep transistor in accordance with an example embodiment. The leakage manager system 290 comprises an adaptive leakage controller (ALC) 291, a negative voltage regulator 292, and a charge pump 294. The charge pump 294 generates a negative voltage 295 (SLPB). The ALC 291 determines whether to adjust the negative voltage 295. The ALC 291 generates a signal (depicted as CTRL) depending on the determination. The negative voltage regulator 292 adjusts the negative voltage 295 depending on the CTRL signal.

As described further herein, the negative voltage regulator 292 of one embodiment generates an enable (EN) signal to the charge pump 294 to enable the charge pump 294 to increase the magnitude of the negative voltage 295 (i.e., to make the negative voltage 295 more negative). If the EN signal is low, an alternating signal from an oscillator 293 to the charge pump 294 is disabled, preventing the charge pump 294 from increasing the magnitude of the negative voltage 295. Alternatively, if the EN signal is high, the alternating signal from the oscillator 293 is enabled so that the charge pump 294 will increase the magnitude of the negative voltage 295. Because the negative voltage regulator 292 toggles the EN signal on or off depending on whether the ALC 291 determines to adjust the negative voltage 295, the leakage manager system 290 maintains the negative voltage 295 at a particular negative voltage to minimize static leakage of the logic gate.

Under normal operation where the digital logic block is to operate, the sleep control receives a signal (sleep input, polarity unimportant here) to disable the charge pump and raise V_{sleep} voltage to V_{DD} .

Under idle operation, where the digital logic block is to sleep (change to a low leakage current state), the Charge Pump Control Logic (CPCL) sends a clock signal and an enable signal to the Negative Voltage Charge Pump (NVCP) to first rapidly drop the V_{sleep} signal to V_{SS} . Then the charge pump begins to push the V_{sleep} voltage below V_{SS} and continues to do so until it receives a pause signal from the CPCL. The Negative Bias Voltage Bias Regulator (NVBR) monitors

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the V_{sleep} voltage until a desirable reduction of the transistor current I_{off} has been achieved. At that point it sends a signal to the CPCL to initiate a Pause signal to the NVCP. As time passes the V_{sleep} voltage will slowly drift upwards toward V_{SS} and at a preset transistor I_{off} the NVBR sends a signal to the CPCL to restart the NVCP to restore the V_{sleep} negative voltage to achieve the desired I_{off} .

FIG. 3 depicts an illustration of the power island manager 220 with an isolation gate 350 and a D flip-flop 360 in an exemplary embodiment of the invention. The power island manager 220 includes a data retention state machine 330 and a sleep generator 340 that are coupled to each other.

The power island manager 220 is coupled to the isolation gate 350 by the ISO signal. The ISO signal is also coupled to other isolation gates. The data retention state machine 330 is coupled to DRB input of the D flip-flop 360 via the DRB signal. The data retention state machine 330 is also coupled to the AND gate 362 via the ENC signal. The clock island (CKI) signal is coupled to the data retention state machine 330 and the AND gate 362. The sleep generator 340 is coupled to the D flip-flop 360 and the AND gate 362 via the SLPB signal. The output of the AND gate 362 is coupled to the C input of the D flip-flop 360 via the CKA signal. The system reset signal is coupled to the RESETB input of the power island manager 220 and the RB input of the D flip-flop 360. The SLPB signal, the DRB signal, and the system reset signal are coupled to other data retention flip-flops.

FIG. 4 depicts an illustration of a power island manager 220 in an exemplary embodiment of the invention. The power island manager 220 includes an AND gate 402, a multiplexer (MUX) 404, a D flip-flop 410, an inverter 412, an AND gate 414, a D flip-flop 420, a D flip-flop 430, the data retention state machine 330, a MUX 432, a MUX 442, a sleep generator 340, and a buffer 452.

The DI0 pin is coupled to the D input of the D flip-flop 410. The SI0 pin is coupled to the SI input of the D flip-flop 410. The CSB and the WEB pins are coupled to the inputs of the AND gate 402. The output of the AND gate 402 and the SCK1 pin are coupled to the input of the MUX 404. The output of the MUX 404 is coupled to the C inputs of the D flip-flop 410, the D flip-flop 420, and the D flip-flop 430. The Q output of the D flip-flop 410 is coupled to the DO0 pin, which is coupled to the input of the inverter 412 and the SI input of the D flip-flop 420. The DI1 pin is coupled to the D input of the D flip-flop 420. The Q output of the D flip-flop 420 is coupled to the DO1 pin, which is coupled to the input of the AND gate 414 and the SI input of the D flip-flop 430. The output of the AND gate 414 is coupled to the RSTB pin. The DI2 pin is coupled to the D input of the D flip-flop 430. The Q output of the D flip-flop 430 is coupled to the DO2 pin, which is coupled to the DLY1/ISO pin. The DLY1/ISO pin is coupled to the SO1, the input of the MUX 432, and the data retention state machine 330.

The RESETB pin is coupled to the R input of the D flip-flop 430, the D flip-flop 420, and the D flip-flop 410. The SE pin, the RESETB pin, the CKI pin, and the SI2 pin are coupled to the data retention state machine 330. The data retention state machine 330 is coupled to the input of the MUX 432, the SO2 pin, the DRB pin, the ENC pin, and the input of the MUX 442. The output of the MUX 442, the VDDI pin, and the VL[0:2] are coupled to the sleep generator 340. The sleep generator 340 is coupled to the SLPB pin. The sleep generator 340 is coupled to the data retention state machine 330 via the AW pin and the input of the buffer 452. The output of the buffer 452 is coupled to the DO3 pin. The DRMODE pin is coupled to the MUX 442.

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In operation, the power island manager 220 has a three bit register for controlling a power island for some embodiments. D [0], with input DI0 and output DO0, is an island reset for re-initializing a power island. This bit is combined with RESETB to form RSTB to re-initialize the power island whenever RESETB or the D [0] is active. D [1], with input DI1 and output DO1, is a sleep bit. When the D [1] bit is set to one, the power island goes into a low leakage state. D [2], with input DI2 and output DO2, is a DLY1/Isolate bit. When DRMODE is tied to low, the D [2] bit, when set to one, will add one clock cycle delay between DRB going active and SLPB going active. When DRMODE is tied high, the D [2] bit, when set to one, will activate isolation of the power island. D [3], such as DO3, is an awake bit. This D [3] bit goes high when SLPB is high. This can be used by software to determine when a power island is out of the sleep state.

The power island manager 220 has two operating modes: one that supports power islands with data retention flip-flops and one that does not. When the DRMODE pin is tied high, a power island is put to sleep by writing a one to D[1]. The data retention state machine 330 performs the timing. The isolate (ISO) signal goes active when the sleep bit is written to a one, and the enable clock (ENC) and the data retention (DRB) will go low after synchronization to the power island clock (CKI). One or two clock cycles later the sleep (SLPB) goes low. To come out of sleep mode, a zero is written to D[1]. In some embodiments, all clock buffers in the power islands can be put to sleep to further minimize leakage. Software can determine when the power island has come out of sleep by reading when DO3 is high.

The System Reset is typically applied once after initial system power up. In some embodiments, the System Reset goes to all data retention flip-flops. The System Reset signal and DI0 bar are combined in a logical AND (RSTB output) to provide initialization to non data retention flip-flops. To create a power island reset, D[0] is set to a one and then cleared to a zero by software.

When the DRMODE is tied low, the power island manager 220 can also provide the control signals for a power island without data retention flip-flops. The power island manager 220 may have a hardware driven method and a software driven method for interfacing to power islands without data retention flip-flops. The software sequence has the following sequence:

Write 04/turn on isolation
Write 06/turn on sleep, isolation on/come out of sleep
Write 05/turn sleep off, reset island, isolation on/wait for sleep to go high
Read/test for DO3=1; sleep is high
Write 00/turn isolation off, normal operation

The hardware driven method uses a clock to sequence the state machine. The only action software takes is to write the sleep bit (DI1) to a one to go into sleep and write a zero to the sleep bit to go out of sleep. Software can determine when the island has come out of sleep by reading when DO3 is high.

In some embodiments, the power island manager 220 contains two scan chains because some of the flip-flops are clocked on the positive and some on the negative. The scan chain enable pin switches the clock on scan chain 1 (SI1 is the input; SO1 is the output), the registers, to CKS1. Scan chain 2 (SI2 is the input; SO2 is the output) is connected to the data retention state machine 330 flip-flops that are clocked on the negative edge of CKI. A separate scan out is provided for each clock domain.

In some embodiments, the SLPB net uses p-type antenna diodes. Since the SLPB net may go to a negative voltage, an n-type antenna diode can cause excessive leakage to ground.

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The leakage can cause SLPB not to go negative and may not work properly. The CSB pin is a chip select pin. The WEB pin is the write enable pin. The VL [2:0] is the leakage control voltage value set by the ALC 270 (FIG. 2). The VDDI is the VDD from the power island.

Low Leakage, Data Retention Circuitry—FIGS. 5, 6, 7A-C, 8A-8B, and 9-12

FIGS. 5, 6, 7A-C, and 8A-8B disclose one embodiment for low leakage, data retention circuitry. In this embodiment, in sleep mode, the circuit parts of a flip-flop that do not require data retention are coupled to ground through a sleep transistor. The gate of the sleep transistor is coupled to a sleep signal that can be driven to a negative voltage such as $-0.3V$. Thus, the leakage in these circuit parts of the flip-flop is eliminated (reduced). When not in a sleep state, the sleep transistor has a gate value equal to or greater than the VDD supply, which effectively grounds the circuit.

The circuit parts that require data retention are coupled to ground through two transistors. One transistor acts effectively to ground the circuit above when not in sleep mode just as the sleep transistor described above. The other transistor is a PMOS device with the gate tied to ground, which provides medium impedance to ground. The voltage drop across this transistor acts to reduce the leakage by increasing the source bias of the NMOS transistors and simultaneously reduces the voltage across the circuit. In this embodiment, the data is retained in a sleep state and reduces the leakage by a factor of 22.

FIG. 5 depicts an illustration of a D/Q portion 500 of the flip-flop circuitry in an exemplary implementation of the invention. The D/Q portion 500 of the flip-flop circuitry includes an inverter 502, a M3 PMOS transistor 504, an M4 NMOS transistor 506, master latch circuitry 510, an M11 PMOS transistor 522, an M12 NMOS transistor 524, an M13 NMOS transistor 526, slave latch circuitry 530, and an inverter 540.

The D signal input is the input of the inverter 502, which includes transistors M1 and M2. The source of the inverter 502 is coupled to the node OFF, which is described below in FIG. 7A. The output of the inverter 502 is coupled to the M3 PMOS transistor 504 and the M4 NMOS transistor 506. The gate of the M3 PMOS transistor 504 is coupled to the CLK signal input. The gate of the M4 NMOS transistor 506 is coupled to the CLKB signal input.

The master latch circuitry 510 includes the inverter 512 and the inverter 514. The inverter 514 forms a feedback loop with the inverter 512, where the output of the inverter 512 is coupled to the input of the inverter 514 and the output of the inverter 514 is coupled to the input of the inverter 512. The inverter 512 corresponds to transistor M5 and M6. The inverter 514 corresponds to transistors M7-M10. The input of the inverter 512 is coupled to node A, which is described in FIG. 8A below. The source of the inverter 512 is also coupled to node OFF, which is described below in FIG. 7A. The output of the inverter 512 is coupled to node B, which is described below in FIG. 8A. The source of the inverter 514 is coupled to node OFF, which is described below in FIG. 7A. The PMOS gate of the inverter 514 is coupled to the CLKB signal input. The NMOS gate of the inverter 514 is coupled to the CLK signal input.

The M11 PMOS transistor 522 is in parallel to the M12 NMOS transistor 524 and the M13 NMOS transistor 526, which are in series. The gate of the M11 PMOS transistor 522 is coupled to the CLKB signal input. The gate of the M12 NMOS transistor 524 is coupled to the HOLDB signal input. The gate of the M13 NMOS transistor 526 is coupled to the CLK signal input.

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The slave latch circuitry 530 includes the inverter 532 and the inverter 534. The inverter 534 forms a feedback loop with the inverter 532, where the output of the inverter 532 is coupled to the input of the inverter 534 and the output of the inverter 534 is coupled to the input of the inverter 532. The inverter 532 corresponds to transistor M14 and M15. The inverter 534 corresponds to transistors M18-21 and M31. The input of the inverter 532 is coupled to node C, which is described in FIG. 8B below. The source of the inverter 532 is also coupled to node SB, which is described below in FIGS. 7B-C. The output of the inverter 532 is coupled to node D, which is described below in FIG. 8B. The source of the inverter 534 is coupled to node SB, which is described below in FIGS. 7B-C. The PMOS gates of the inverter 534 are coupled to the HOLDB and CLK signal inputs. The NMOS gate of the inverter 534 is coupled to the CLKB signal input.

The output of the inverter 532 is coupled to the input of the inverter 540. The inverter 540 corresponds to transistors M16 and M17. The source of the inverter 540 is also coupled to node OFF, which is described below in FIG. 7A. The output of the inverter 540 is the Q signal output.

FIG. 6 depicts a CK portion 600 of the flip-flop circuitry in an exemplary implementation of the invention. The CK portion 600 of the flip-flop circuitry includes an inverter 602, an M24 PMOS transistor 604, an M25 PMOS transistor 606, an M26 NMOS transistor 608, an M32 NMOS transistor 610, and an M27 PMOS transistor 612.

The CK signal input is the input of the inverter 602, which includes transistors M22 and M23. The source of the inverter 602 is coupled to node OFF, which is described below in FIG. 7A. The output of the inverter 602 is coupled to the drain of the M24 PMOS transistor 604 and the node CLKB. The gate of the M24 PMOS transistor 604 is coupled to the HOLDB signal input. The output of the inverter 602 is also coupled to the M25 PMOS transistor 606 and the M26 NMOS transistor 608. The M25 PMOS transistor 606, the M26 NMOS transistor 608, and the M32 NMOS transistor 610 are coupled in series. The gate of the M32 NMOS transistor 610 is coupled to the HOLDB signal input.

The CLK signal output is coupled to the drain of the M25 PMOS transistor 606, the drain of the M26 NMOS transistor 608, and the drain of the M27 PMOS transistor 612. The gate of the M27 PMOS transistor 612 is coupled to the HOLDB signal input.

FIG. 7A depicts a sleep transistor 702 for the OFF node in an exemplary implementation of the invention. The sleep transistor 702 is an NMOS transistor that corresponds to transistor M28. The drain of the sleep transistor 702 is coupled to the OFF node. The gate of the sleep transistor 702 is coupled to the SLEEPB signal input. The source of the sleep transistor 702 is coupled to ground. In some embodiments, the OFF node can be separated into two or more nodes each having its own NMOS sleep transistor.

FIG. 7B depicts a sleep transistor 704 for the SB node in an exemplary implementation of the invention. The sleep transistor 704 is an NMOS transistor that corresponds to transistor M29. The drain of the sleep transistor 704 is coupled to the SB node. The gate of the sleep transistor 704 is coupled to the SLEEPB signal input. The source of the sleep transistor 704 is coupled to ground.

FIG. 7C depicts a sleep transistor 706 for the SB node in an exemplary implementation of the invention. The sleep transistor 706 is a PMOS transistor that corresponds to transistor M30. The source of the sleep transistor 706 is coupled to the SB node. The gate and drain of the sleep transistor 706 are coupled to ground.

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FIG. 8A depicts circuitry 800 for the tristate inverter in the master latch in an exemplary implementation of the invention. The circuitry 800 for the master latch includes a PMOS transistor 802, a PMOS transistor 804, an NMOS transistor 806, and an NMOS transistor 808 that are coupled together in series. The gates of the PMOS transistor 802 and the NMOS transistor 808 are coupled to the node B. The gate of the PMOS transistor 804 is coupled to the CLKB signal input. The gate of the NMOS transistor 806 is coupled to the CLK signal input. The drains of the PMOS transistor 804 and the NMOS transistor 806 are coupled to node A. The source of the NMOS transistor 808 is coupled to node OFF.

FIG. 8B depicts circuitry 810 for the tristate inverter in the slave latch in an exemplary implementation of the invention. The circuitry 810 for the slave latch includes a PMOS transistor 812, a PMOS transistor 814, a PMOS transistor 816, an NMOS transistor 818, and an NMOS transistor 820. The PMOS transistor 812 is coupled to the PMOS transistor 814 and the PMOS transistor 816 that are parallel to each other. The PMOS transistor 814 and the PMOS transistor 816 are coupled to the NMOS transistor 818, which is also coupled to the NMOS transistor 820.

The gates of the PMOS transistor 812 and the NMOS transistor 820 are coupled to the node D. The gate of the PMOS transistor 814 is coupled to the HOLDB signal input. The gate of the PMOS transistor 816 is coupled to the CLK signal input. The gate of the NMOS transistor 818 is coupled to the CLKB signal input. The drains of the PMOS transistor 814, the PMOS transistor 816, and the NMOS transistor 806 are coupled to node C. The source of the NMOS transistor 820 is coupled to node SB.

FIG. 9 depicts an illustration of the HOLDB and SLEEPB signals in an exemplary embodiment of the invention.

The operation begins with CK going to zero. This causes CLKB to be equal to VDD and CLK to be equal to zero, which isolates the slave latch circuitry 530 from the master latch circuitry 510. The HOLDB signal goes to 0 to retain the state of the slave latch. The SLEEPB signal then goes to -0.3V. This shuts off transistor M28 in FIG. 7A, which halts the leakage from all the circuits except in the slave latch circuitry 530. When not in sleep mode, transistor M28 provides a low impedance path to ground.

The slave latch circuitry 530 is coupled to ground through the transistors M29 and M30, respectively depicted in FIGS. 7B and 7C. One purpose of transistor M29 is to provide a low impedance path to ground when not in sleep mode.

One purpose of transistor M30 is to provide a default moderate impedance path to ground when transistor M29 is off or in sleep mode. The leakage in the slave latch circuitry 530, in going through transistor M30, causes node SB to rise. This provides a source bias to the slave NMOS transistors reducing the leakage through them and also reduces the voltage across the slave side to VDD-SB, which further reduces the leakage. Equilibrium is reached where the leakage cannot increase. Basically, the leakage is used to limit itself.

This embodiment uses the gated VDD solution because the voltage across the circuit is reduced to VDD-SB. This embodiment combines this gated VDD with the modulated back gate bias method because of the source bias SB but only for the NMOS transistors. This is accomplished without switching a lower VDD and driving a well. Thus, a simple process can be used. Also, this embodiment advantageously uses the moderate impedance transistor in a way that causes leakage to limit itself by reaching equilibrium.

FIGS. 10 and 11 disclose another embodiment for low leakage, data retention circuitry. In this embodiment, in a sleep state, the circuitries that do not require data retention are

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coupled to ground through a sleep transistor. The logic coupled to the transistors gated by the SLEEPB signal is shut off and draws minimal leakage. This process is accomplished by driving the SLEEPB signal below VSS by 0.3-0.4V. The HOLDB signal keeps the slave latch circuitry from changing state while the rest of the flip-flop comes out of the sleep state. The only part of the flip-flop still powered is the slave latch circuitry. The slave latch circuitry combines several techniques to minimize leakage.

FIG. 10 depicts circuitry 1000 for low leakage and data retention in an exemplary embodiment of the invention. The circuitry 1000 includes the inverter 1002, the master latch circuitry 1010, the slave latch circuitry 1020, the inverter 1032, the inverter 1034, the sleep transistors 1042, 1044, 1046, and 1048, the inverter 1052, and the inverter 1054.

The D input is the input for the inverter 1002. The master latch circuitry 1010 includes the transmission gate 1012, the inverter 1014, the transmission gate 1016, and the inverter 1018. The output of the inverter 1002 is coupled to the left contact of the transmission gate 1012. The right contact of the transmission gate 1012 is coupled to the input of the inverter 1014 and the left contact of the transmission gate 1016. The output of the inverter 1014 is coupled to the D input of the slave latch circuitry 1020 and the input of the inverter 1018. The output of the inverter 1018 is coupled to the DB input of the slave latch circuitry 1020 and the right contact of the transmission gate 1016.

The SLEEPB signal input is coupled to the gates for the SL1 sleep transistor 1042, the SL2 sleep transistor 1044, the SL3 sleep transistor 1046, the SL4 sleep transistor 1048, and the SLEEPB input of the slave latch circuitry 1020. The SL1 sleep transistor 1042 is coupled to the inverter 1002 and ground. The SL2 sleep transistor 1044 is coupled to the inverter 1052, the inverter 1054, and ground. The SL3 sleep transistor 1046 is coupled to the inverter 1014, the inverter 1018, and ground. The SL4 sleep transistor 1048 is coupled to the inverter 1032, the inverter 1034, and ground. In some embodiments, the SL1 sleep transistor 1042, the SL2 sleep transistor 1044, the SL3 sleep transistor 1046, and the SL4 sleep transistor 1048 can each be separated into two or more node each having its own NMOS sleep transistor.

The CK signal is the input of the inverter 1052. The output of the inverter 1052 is coupled to the transmission gate 1012, the transmission gate 1016, and the input of the inverter 1054. The output of the inverter 1054 is coupled to the transmission gate 1012, the transmission gate 1016, and the CLK input of the slave latch circuitry 1020. The HOLDB signal input is coupled to the HOLDB input of the slave latch circuitry 1020. The output of the slave latch circuitry 1020 is coupled to the input of the inverter 1032. The output of the inverter 1032 is coupled to the input of the inverter 1034. The output of the inverter 1034 is the Q signal.

FIG. 11 depicts slave latch circuitry 1020 in an exemplary embodiment of the invention. The slave latch circuitry 1020 includes D1 transistor 1102, D2 transistor 1104, DH transistor 1106, DSL sleep transistor 1108, stack transistors 1110, stack transistors 1120, D1B transistor 1132, D2B transistor 1134, DHB transistor 1136, and sleep transistor 1138.

The D1 transistor 1102, the D2 transistor 1104, the DH transistor 1106, and the DSL sleep transistor 1108 are coupled to each other in series with the sleep transistor 1108 coupled to ground. The gate of the D1 transistor 1102 is coupled to the CLK signal input. The gate of the D2 transistor 1104 is coupled to the D input. The gate of the DH transistor 1106 is coupled to the HOLDB signal input. The gate of the sleep transistor 1108 is coupled to the SLEEPB signal input.

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The stack transistors **1110** comprise **P1** transistor **1112**, **P0** transistor **1114**, **N1** transistor **1116**, and **N0** transistor **1118**. The **P1** transistor **1112**, the **P0** transistor **1114**, the **N1** transistor **1116**, and the **N0** transistor **1118** are coupled to each other in series with the **N0** transistor **1118** coupled to ground. The gates of the **P1** transistor **1112**, the **P0** transistor **1114**, the **N1** transistor **1116**, and the **N0** transistor **1118** are coupled to the **LAT** signal input. The drains of the **P0B** transistor **1124** and the **N1B** transistor **1126** are coupled to the **LAT** signal input.

The stack transistors **1120** comprise **P1B** transistor **1122**, **P0B** transistor **1124**, **N1B** transistor **1126**, and **N0B** transistor **1128**. The **P1B** transistor **1122**, the **P0B** transistor **1124**, the **N1B** transistor **1126**, and the **N0B** transistor **1128** are coupled to each other in series with the **N0B** transistor **1128** coupled to ground. The gates of the **P1B** transistor **1122**, the **P0B** transistor **1124**, the **N1B** transistor **1126**, and the **N0B** transistor **1128** are coupled to the **LATB** signal input. The drains of the **P0** transistor **1114** and the **N1** transistor **1116** are coupled to the **LATB** signal input.

In operation, the logic coupled to the transistors gated by the **SLEEPB** signal is shut off and draws minimal leakage. This process is accomplished by driving the **SLEEPB** signal below **VSS** by 0.3-0.4V. The **HOLDB** signal keeps the slave latch circuitry **1020** from changing state while the rest of the flip-flop comes out of the sleep state. The only part of the flip-flop still powered is the slave latch circuitry **1020**. The slave latch circuitry **1020** combines several techniques to minimize leakage. Transistors not necessary for state retention (stacks with **CLK**) have sleep transistors to shut off leakage (gated by the **SLEEPB** signal).

The 8 transistors in the stack transistors **1110** and **1120** use two techniques to reduce leakage. The first technique used is transistor stacking, which is also called self-reverse bias. The **N0** transistor **1118** and the **N1** transistor **1116** will have some small leakage even when the gate is at 0V. As a result, **VNN1** will be at a positive voltage. This causes **VGS(N1)** and **VBS(N1)** to be negative, and **VDS(N1)** to decrease. Consequently, the leakage current is reduced in **N0** transistor **1118** and the **N1** transistor **1116**. The same effect occurs on **N0B** transistor **1128**, **N1B** transistor **1126**, **P0** transistor **1114**, **P1** transistor **1112**, **P0B** transistor **1124**, and **P1B** transistor **1122**.

The second technique is called multiple threshold transistors. Increasing channel length of MOS transistors increases the threshold of the devices without any change in process complexity. The **N0** transistor **1118**, the **N1** transistor **1116**, the **N0B** transistor **1128**, and the **N1B** transistor **1126** have increased channel length, which raises **VTH** and reduces leakage current.

This embodiment reduces leakage by a factor of 25 over a current standard cell **D** flip-flop.
I/O Pad—FIG. 12

In some embodiments, a programmable general purpose input and output (I/O) padcell includes built in-level shifters and isolation that interface with the chip core logic. In these embodiments, a level shifter can be controlled to retain data.

FIG. 12 depicts circuitry **1200** for a level shifter for an I/O pad in an exemplary embodiment of the invention. The circuitry **1200** includes **MP2** transistor **1202**, **MP3** transistor **1204**, **M3** transistor **1206**, **M4** transistor **1208**, **M1** transistor **1210**, **M0** transistor **1212**, **M5** transistor **1214**, **M2** transistor **1216**, and an inverter **1218**.

The circuitry **1200** is for a latching level shifter. The **M3** transistor **1206** and the **M4** transistor **1208** are “native” cascode devices. The **M3** transistor **1206** and the **M4** transistor **1208** are also known as depletion-mode transistors. The **M3** transistor **1206** and the **M4** transistor **1208** are used to allow

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thin gate devices to be used in the input stage. This allows large voltage ratios between the **VDD** and the **V310**. The **M0** transistor **1212** and the **M1** transistor **1210** are output latching devices that allow the level shifter to retain the state when both **IN** and **INB** are 0. Thus, **IN** and **INB** control data retention.

In some embodiments, the gates of the **M3** transistor **1206** and the **M4** transistor **1208** are coupled to other transistors connected to the cascode voltage.

The following truth table is for circuitry **1200**.

IN	INB	OUT
0	0	Retain last state
0	1	0
1	0	1
1	1	Illegal

There will be setup time requirements for any signal compared to **SLPB**. If level shifters are used with an **SRAM** cell built into the output stage, the two inputs can be removed anytime after the output latch has flipped to a new state. Both 1.2V inputs to the level shifter cannot go to **VDD**. This can be prevented by including an inverter. If both the inverter and the level shifter have **SLPB** transistors, there is a potential timing race if **SLPB** goes to **VSS** with **VDD** high. In this case, the level shifters should be off before the output of the inverter drifts to **VDD**. In some embodiments, the **M5** transistor **1214** and the **M2** transistor **1216** can be configured to withstand greater voltages.

In some embodiments, the sources of the **M5** transistor **1214** and the **M2** transistor **1216** can be coupled to a common **SLEEPB** transistor **1240** to further reduce leakage. In one embodiment, the width of the **SLEEPB** transistor **1240** is 4 micrometers, and the length is 0.13 micrometers. The following truth table is for circuitry **1200** including this common **SLEEPB** transistor **1240**:

SLEEPB	IN	INB	OUT
1	0	0	Retain state (Data Retention)
1	0	1	0
1	1	0	1
1	1	1	Illegal
0	X	X	Retain State

In some embodiments, the **SLEEPB=0** input state should be understood to include the **SLEEPB** voltage being below 0V (E.g. -0.35V generated by a leakage optimization circuit).

In this extension to FIG. 12 (and the above truth table), the two Data Retention states may be operated independently, sequentially or simultaneously. This is beneficial when the **SLEEPB** input is used to control/limit leakage power while the **IN/INB=00** state is used for data retention. This is because the **SLEEPB** voltage comes from a charge pump and takes some time to transition from **Vdd (=1)** to the Data Retention mode.

The above description is illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be

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determined with reference to the appended claims along with their full scope of equivalents.

While this invention has been particularly shown and described with references to example embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

What is claimed is:

1. A method carried out in an integrated circuit that includes an adaptive leakage controller, a power manager and a plurality of power islands, the method comprising:

receiving, at the power manager, a control signal from the adaptive leakage controller; and

employing the power manager to dynamically change power consumptions of the plurality of power islands, the employing the power manager to dynamically change power consumptions including: generating a variable voltage based on the control signal; and providing the variable voltage to at least one of low leakage sleep circuits of the integrated circuit.

2. The method as claimed in claim 1 further comprising putting to sleep and taking out of sleep, at different times, at least one of the power islands.

3. The method as claimed in claim 2 wherein the power manager employs a state machine to control the putting to sleep and the taking out of sleep.

4. The method as claimed in claim 1 wherein the variable voltage is an optimum voltage.

5. The method as claimed in claim 4 wherein the optimum voltage is dependent upon both process variation and temperature variation.

6. The method as claimed in claim 4 wherein the optimum voltage is generated by a sleep generator.

7. The method as claimed in claim 1 wherein the control signal is a digital signal.

8. The method as claimed in claim 1 wherein the at least one of the low leakage sleep circuits is connected in series to a source of a supply voltage and to a logic gate or storage cell of one of the power islands.

9. The method as claimed in claim 8 wherein the at least one of the low leakage sleep circuits modifies the supply voltage to the one of the power islands during a sleep mode.

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10. A method carried out in an integrated circuit that includes an adaptive leakage controller, a power manager, a plurality of power islands and a plurality of low leakage sleep circuits, the method comprising:

receiving, at the power manager, a control signal from the adaptive leakage controller; and

employing the power manager to dynamically change power consumptions of the plurality of power islands, the employing the power manager to dynamically change power consumptions including: generating a variable voltage based on the control signal; and providing the variable voltage to the plurality of low leakage sleep circuits,

wherein each of low leakage sleep circuits is associated with leakage reduction of a respective one of the plurality of power islands.

11. The method as claimed in claim 10 further comprising putting to sleep and taking out of sleep, at different times, at least one of the power islands.

12. The method as claimed in claim 11 wherein the power manager employs a state machine to control the putting to sleep and the taking out of sleep.

13. The method as claimed in claim 10 wherein the variable voltage is an optimum voltage.

14. The method as claimed in claim 13 wherein the optimum voltage is dependent upon both process variation and temperature variation.

15. The method as claimed in claim 13 wherein the optimum voltage is generated by a sleep generator.

16. The method as claimed in claim 10 wherein the control signal is a digital signal.

17. The method as claimed in claim 10 wherein at least one of the low leakage sleep circuits is connected in series to a source of a supply voltage and to a logic gate or storage cell of an associated one of the power islands.

18. The method as claimed in claim 17 wherein the at least one of the low leakage sleep circuits modifies the supply voltage to the associated one of the power islands during a sleep mode.

* * * * *

EXHIBIT F

(10) **Patent No.:** US 9,350,349 B2
(45) **Date of Patent:** *May 24, 2016

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Related U.S. Application Data

continuation of application No. 12/542,352, filed on Aug. 17, 2009, now Pat. No. 7,940,081, which is a continuation of application No. 12/284,311, filed on Sep. 19, 2008, now Pat. No. 7,592,837, which is a continuation of application No. 11/998,725, filed on Nov. 30, 2007, now Pat. No. 7,443,197, which is a continuation of application No. 11/732,181, filed on Apr. 2, 2007, now Pat. No. 7,348,804, which is a division of application No. 11/041,687, filed on Jan. 20, 2005, now Pat. No. 7,227,383.

- (60) Provisional application No. 60/586,565, filed on Jul. 9, 2004, provisional application No. 60/546,574, filed on Feb. 19, 2004.

(51) Int. Cl.

G11C 5/14 (2006.01)
H03K 3/356 (2006.01)
H03K 17/10 (2006.01)
H03K 19/00 (2006.01)
H03K 5/14 (2014.01)

(52) U.S. Cl.

CPC **H03K3/356113** (2013.01); **H03K 5/14** (2013.01); **H03K 17/102** (2013.01); **H03K 19/0016** (2013.01)

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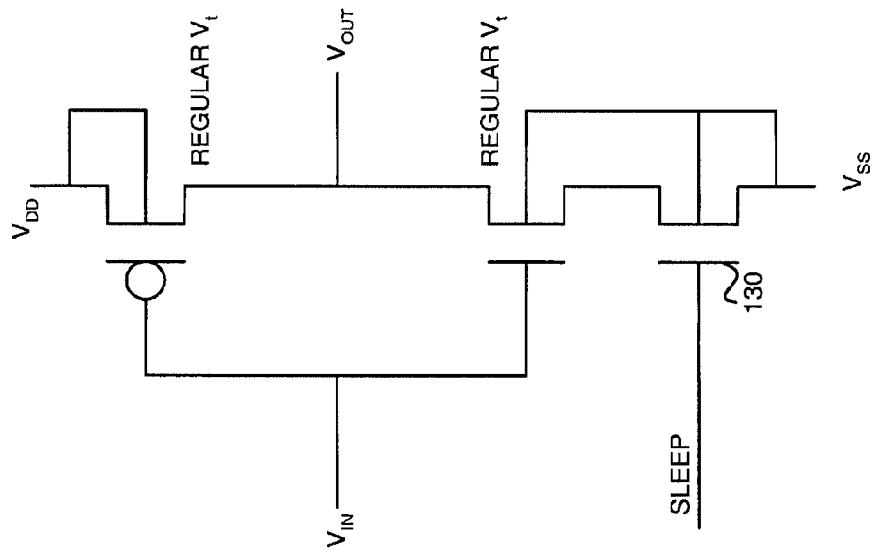


FIG. 1
PRIOR ART

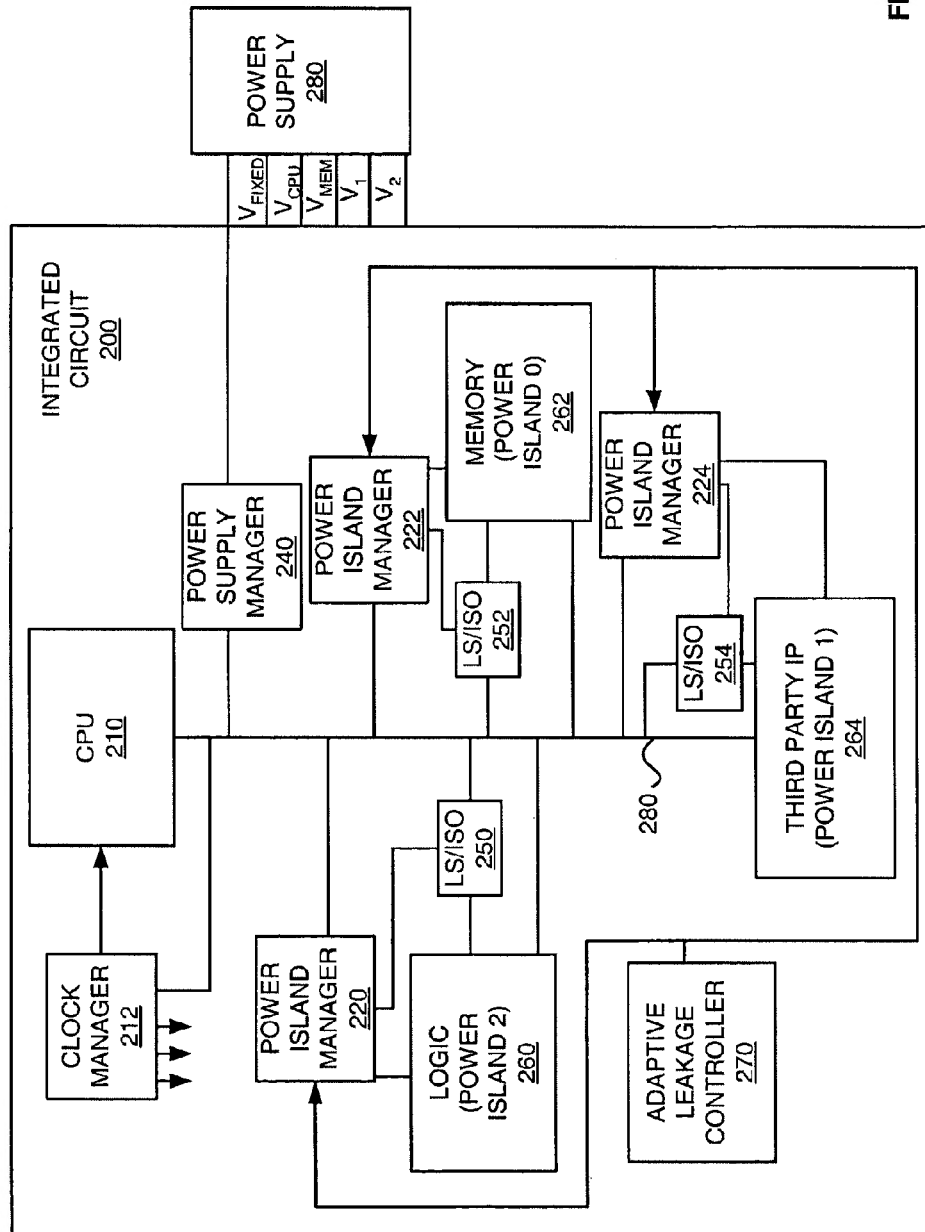


FIG. 2

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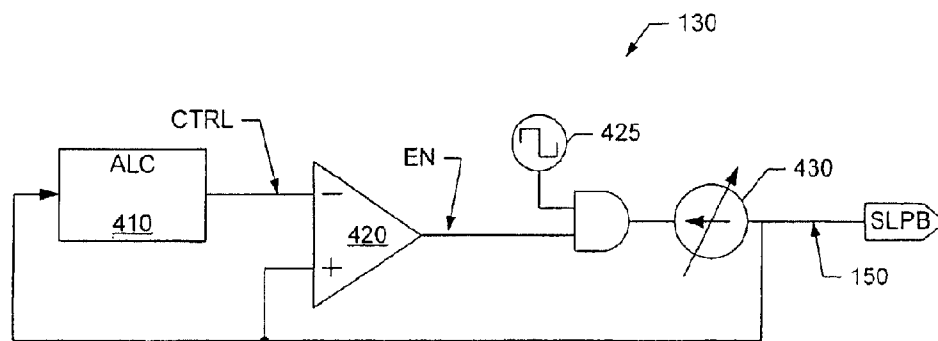


FIG. 2A

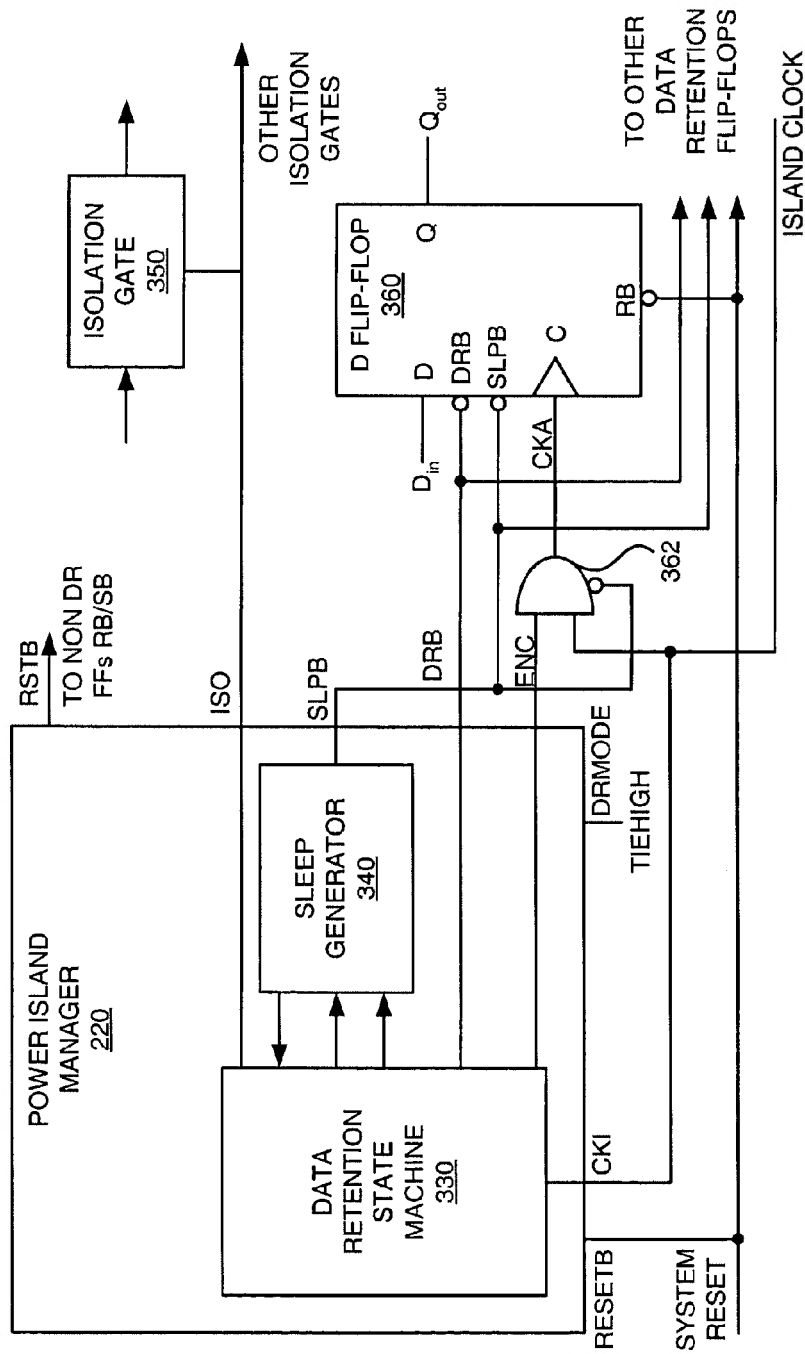


FIG. 3

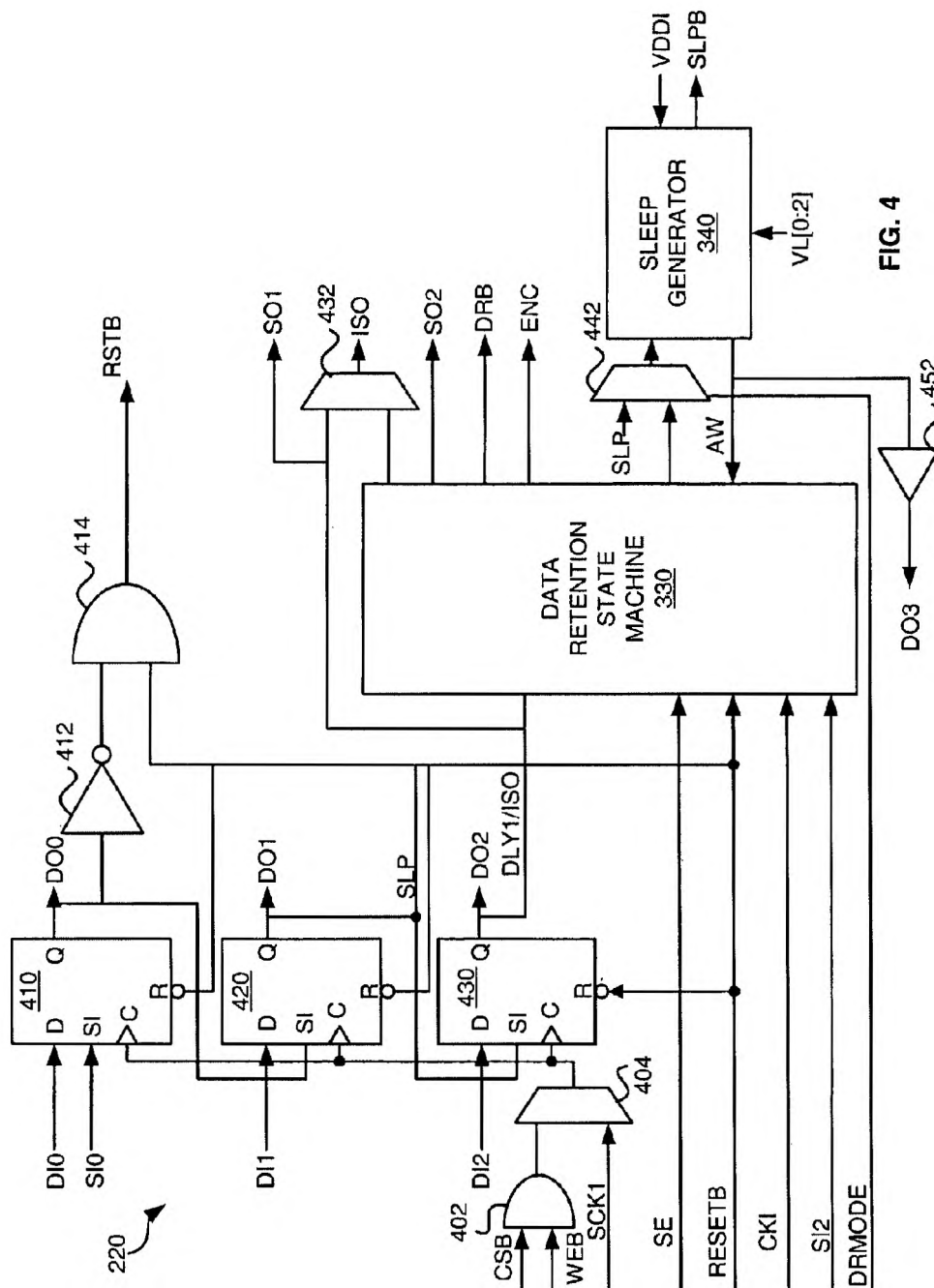
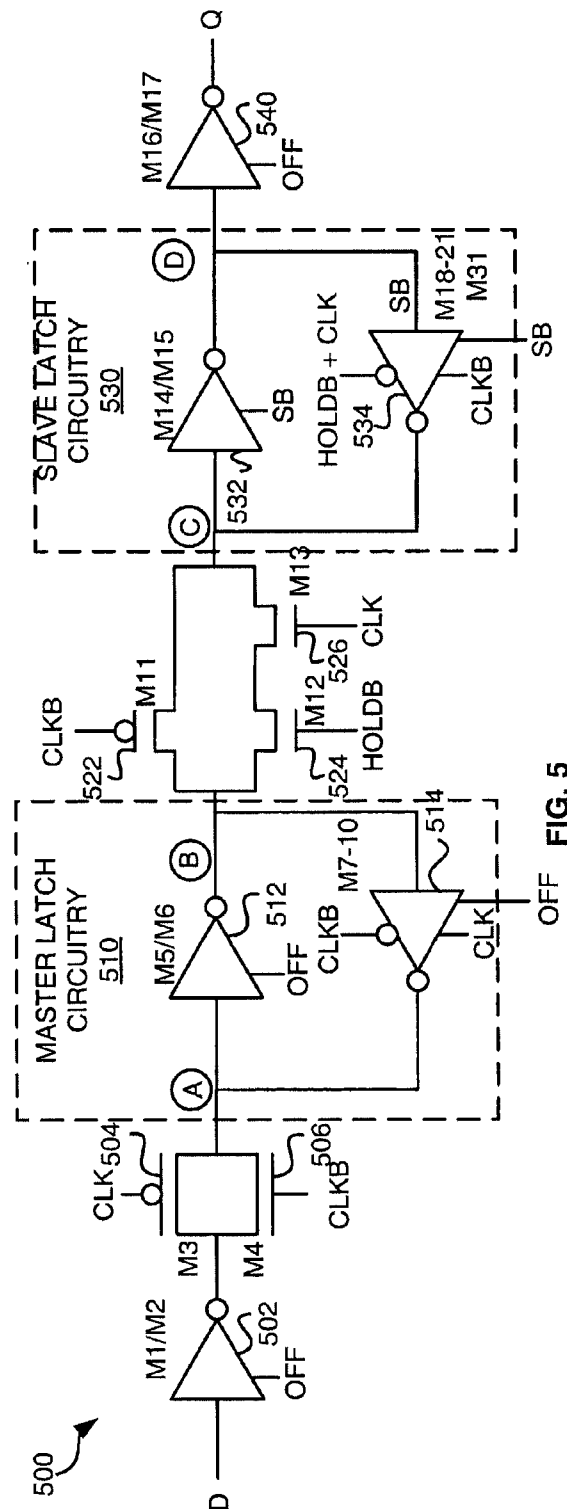


FIG. 4



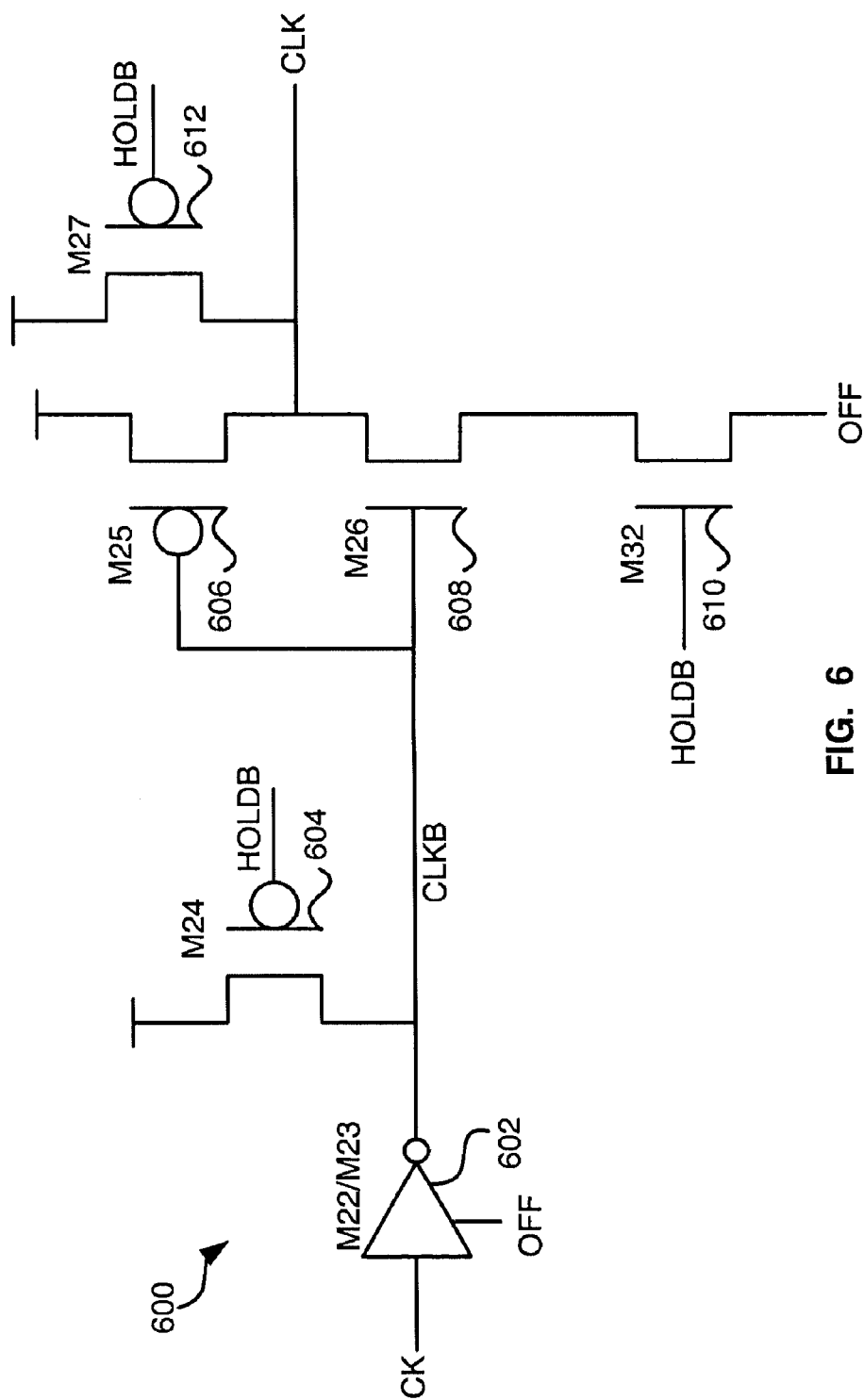


FIG. 6

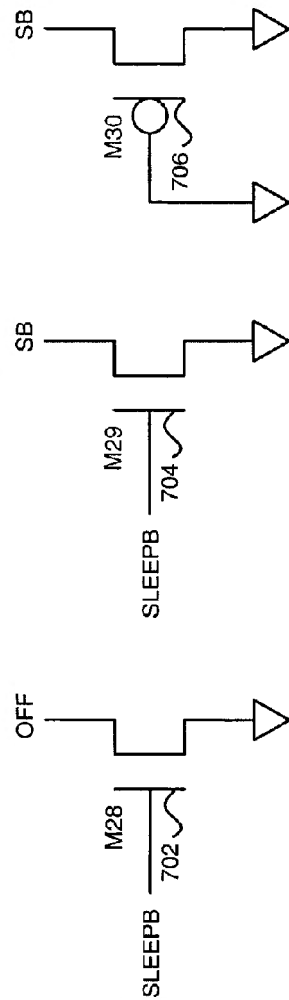


FIG. 7C

FIG. 7B

FIG. 7A

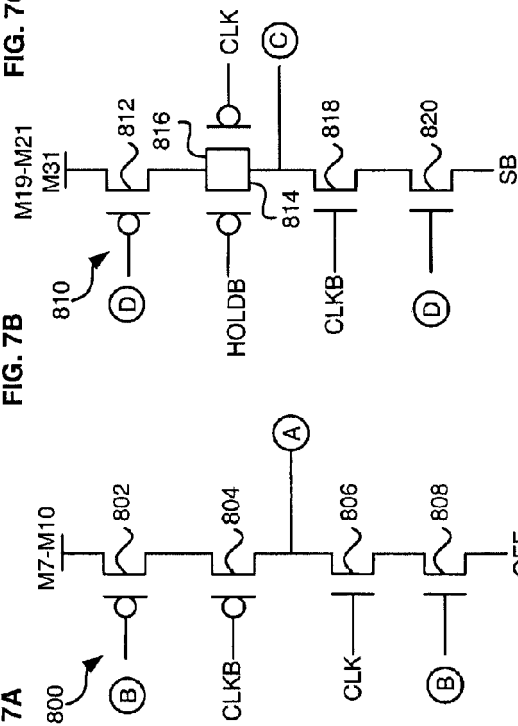


FIG. 8B

FIG. 8A

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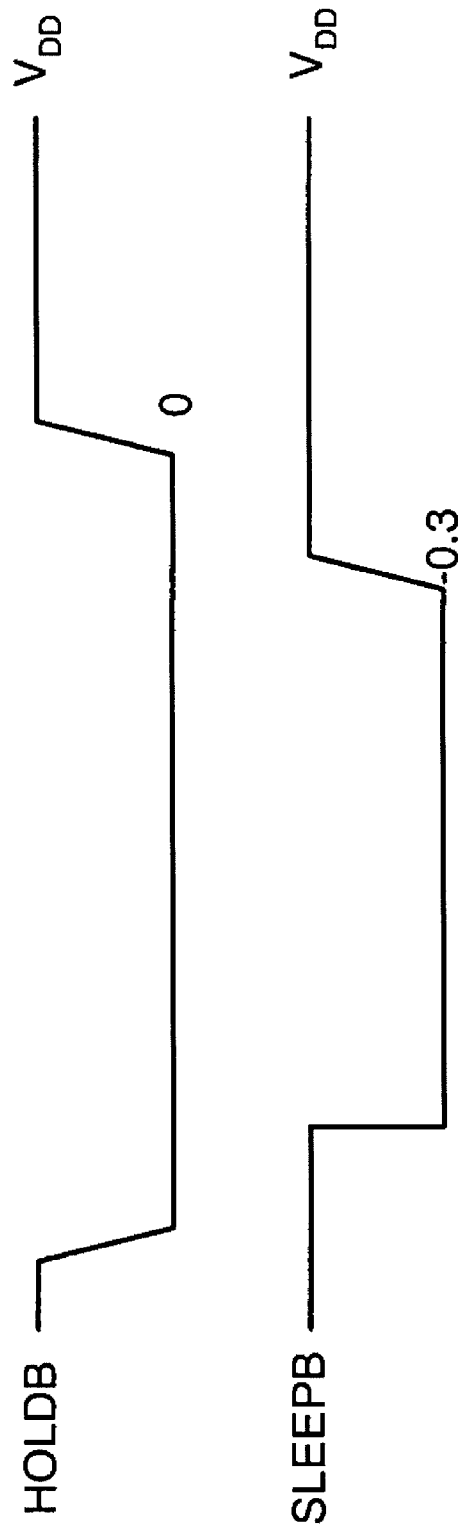
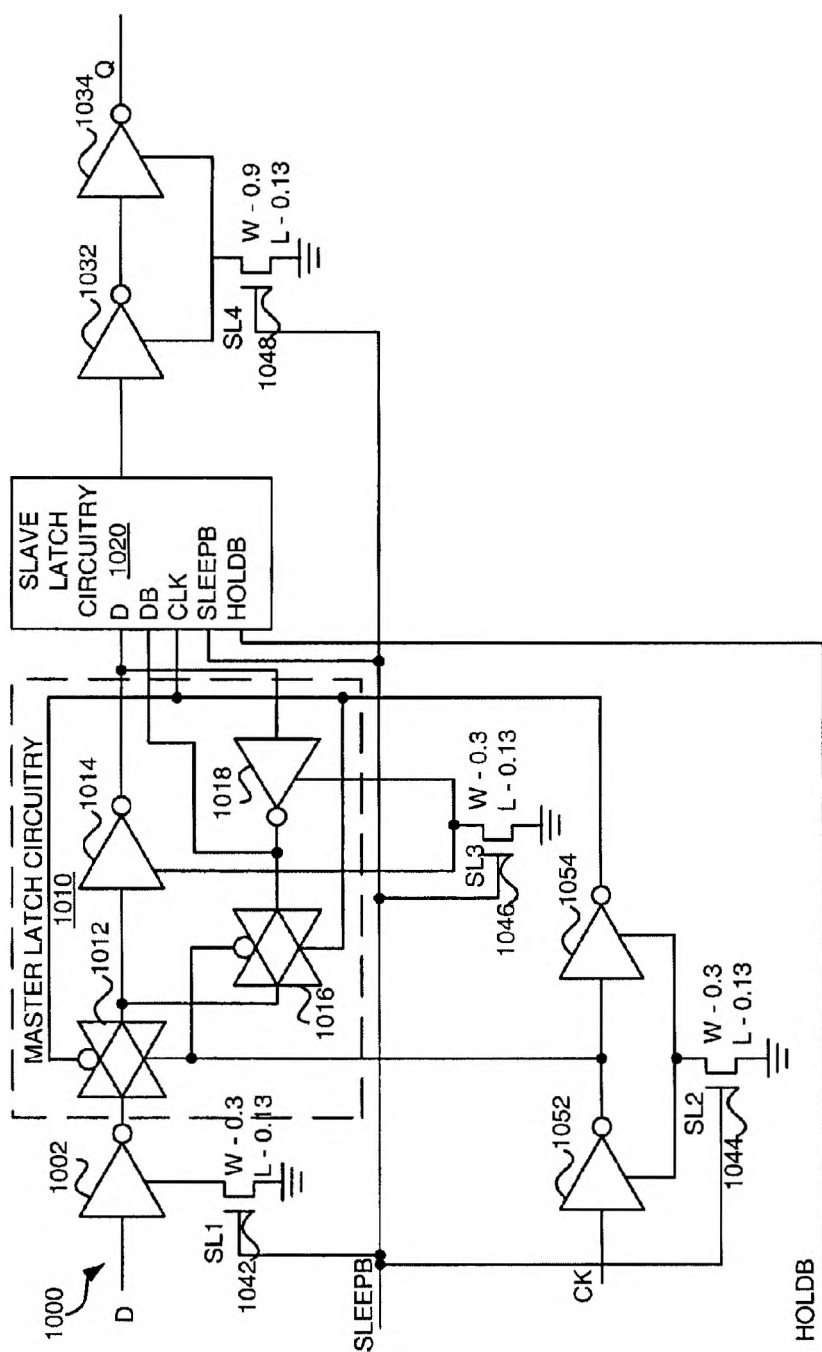


FIG. 9



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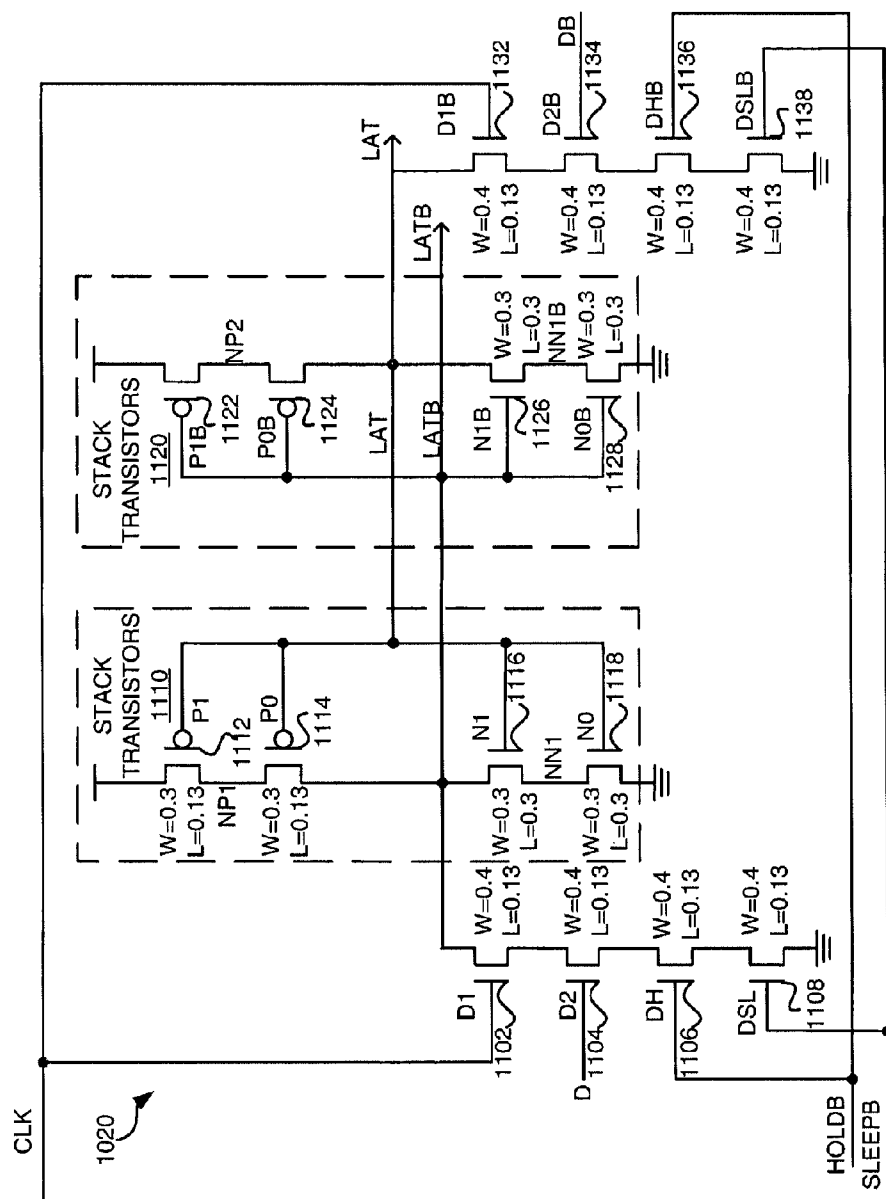


FIG. 11

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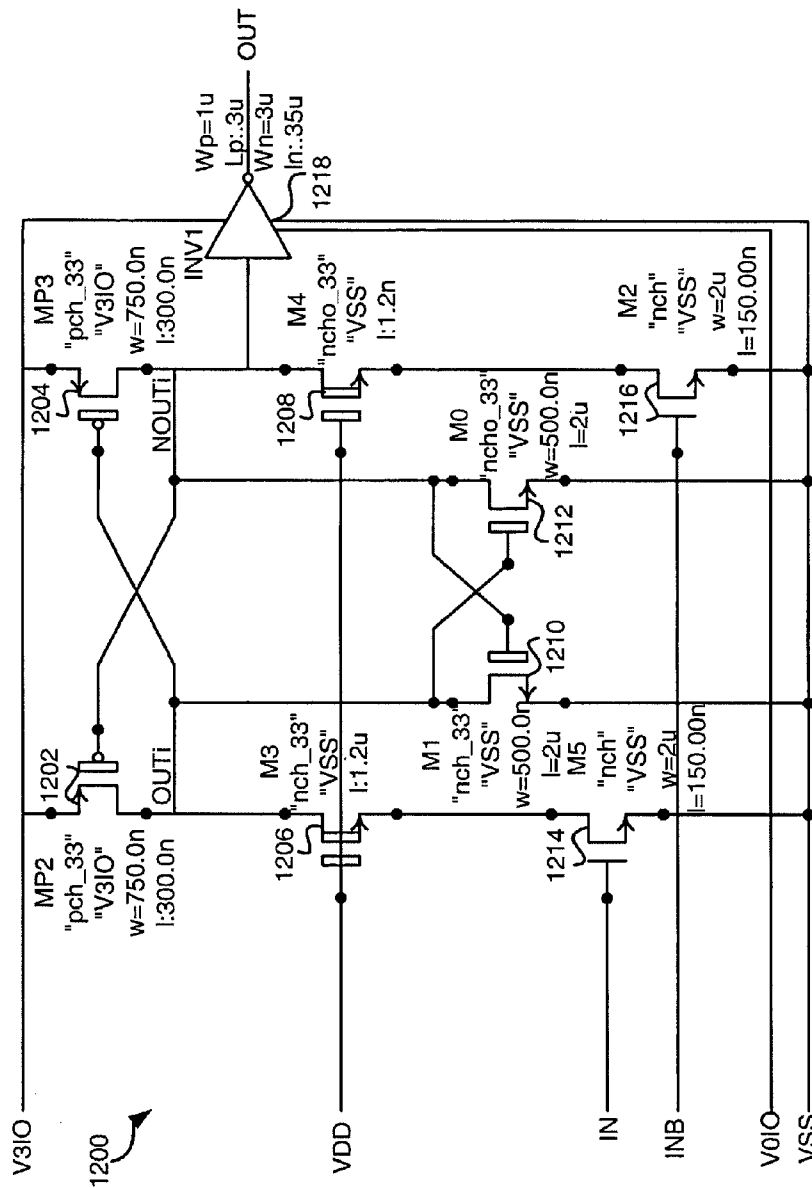


FIG. 12

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**LOW LEAKAGE AND DATA RETENTION
CIRCUITRY****CROSS-REFERENCE TO RELATED
APPLICATIONS**

This application is a continuation of U.S. application Ser. No. 13/569,613, filed Aug. 8, 2012, which is a continuation of U.S. application Ser. No. 13/074,291, filed Mar. 29, 2011 (now U.S. Pat. No. 8,253,438), which is a continuation of U.S. application Ser. No. 12/542,352, filed Aug. 17, 2009 (now U.S. Pat. No. 7,940,081), which is a continuation of U.S. application Ser. No. 12/284,311, filed Sep. 19, 2008 (now U.S. Pat. No. 7,592,837), which is a continuation of U.S. application Ser. No. 11/998,725, filed Nov. 30, 2007 (now U.S. Pat. No. 7,443,197), which is a continuation of U.S. application Ser. No. 11/732,181, filed Apr. 2, 2007 (now U.S. Pat. No. 7,348,804), which is a divisional and claims the priority benefit of U.S. application Ser. No. 11/041,687, filed Jan. 20, 2005 (now U.S. Pat. No. 7,227,383), which claims the priority benefit of U.S. Provisional Application No. 60/586,565, filed Jul. 9, 2004, and U.S. Provisional Application No. 60/546,574, filed Feb. 19, 2004.

The entire teachings of the above applications are incorporated herein by reference.

**STATEMENT REGARDING FEDERALLY
SPONSORED RESEARCH OR DEVELOPMENT**

Not applicable.

REFERENCE TO A MICROFICHE APPENDIX

Not applicable.

BACKGROUND OF THE INVENTION**1. Field of the Invention**

The present invention relates generally to integrated circuits, and more particularly to low leakage and data retention circuitry.

2. Description of the Related Art

Most integrated circuits have a design goal to reduce the overall power consumption. The total power consumed by an integrated circuit includes dynamic power consumption and standby leakage current consumption. The challenge in designing an integrated circuit is to reduce the dynamic power and leakage power, while maintaining performance and cost goals for the integrated circuit.

In complementary metal oxide semiconductors (CMOS), various types of leakage occur such as pn junction reverse-bias current, subthreshold leakage, oxide tunneling current, gate current due to hot-carrier injection, gate-induced drain leakage, and channel punch through current. When the threshold voltage for a CMOS transistor is reduced for higher performance, the leakage power is significant in the total power consumption of the CMOS circuit.

There are two approaches in reducing the leakage power for CMOS circuits. The first approach is a process level technique that controls the doping profile of the transistor. The other approach is a circuit level technique where voltages at the different device terminals such as the drain, source, gate, and body are controlled. Some circuit level techniques are discussed below.

One circuit level technique is stacking transistors, which is also called self-reverse bias. When more than one transistor in a stack of series-connected transistors is turned off, the sub-

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threshold leakage current is reduced. One problem with the transistor stack is that only a three times reduction in leakage current is achieved.

Another circuit level technique is a multiple threshold voltage design. Both high- and low-threshold transistors are on the same chip to deal with the leakage problem. The high-threshold transistors suppress the sub-threshold leakage current. The low-threshold transistors are used to achieve higher performance. One problem with a multiple threshold design is that process complexity and costs are increased.

Another circuit level technique is a multiple body bias in which the body voltage is changed to modify the threshold voltage. If separate body biases are applied to different NMOS transistors, the transistor cannot share the same well, which requires triple well technologies. One problem is that well biasing consumes a lot of chip area and requires extra power supplies for each cell. This technique also increases process complexity and the leakage reduction is not optimal.

Another technique for reducing leakage is a sleep transistor. FIG. 1 depicts prior art circuitry including a sleep transistor. For NMOS sleep transistors, one or more NMOS transistors are added to logic gates in series with the cell transistors to VSS. The NMOS sleep transistors act as a switch to turn on and off the logic gate. In FIG. 1, the sleep transistor **130** is turned on (gate to VDD) during normal cell operation. When the cell is idle, the sleep transistor **130** is turned off (gate tied to VSS) to reduce the leakage current of the cell. Sleep transistors can also be PMOS transistors. One problem with sleep transistors is that if all logic has sleep transistors, the logic will lose their state information.

SUMMARY OF THE INVENTION

In an exemplary embodiment of the presently disclosed invention, a data retention circuit is provided. The exemplary circuit includes an input/output pad cell that itself includes level shifter circuitry, the level shifter circuitry having inputs and outputs. Output latching circuitry is also provided as a part of the data retention circuit. The output latching circuitry includes two transistors. The transistors are coupled to the outputs of the level shifter circuitry and retain a state of the level shifter circuitry based on the state of the inputs. A leakage optimization circuit is also included, the leakage optimization circuit is configured to simultaneously decrease leakage power in conjunction with the state retention of the output latching circuitry.

In another embodiment of the presently disclosed invention, a system for controlling power consumption within an integrated circuit is disclosed. The system includes a power island, the power island includes a first circuit. The first circuit of the power island is configured to receive input signals and a hold signal. The circuit is further configured to process the input signals and retain data in a sleep state having low leakage. The first circuit is further configured to retain the data based on the hold signal. The system further includes a sleep transistor, which is coupled to the first circuit. The sleep transistor is configured to receive a negative voltage sleep signal and reduce power consumption of the first circuit in the sleep state. As a result, the first circuit has low leakage based on the sleep signal while simultaneously retaining the data.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing will be apparent from the following more particular description of example embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout

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the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating embodiments of the present invention.

FIG. 1 is an illustration of circuitry including a sleep transistor in the prior art;

FIG. 2 is an illustration of an integrated circuit with a power supply in an exemplary implementation of the invention;

FIG. 2A is a block diagram of a leakage manager system for minimizing state leakage of a logic gate by application of a negative voltage to a sleep transistor;

FIG. 3 is an illustration of a power island manager with an isolation gate and a D flip-flop in an exemplary implementation of the invention;

FIG. 4 is an illustration of a power island manager in an exemplary implementation of the invention;

FIG. 5 is an illustration of a D/Q portion of flip-flop circuitry in an exemplary implementation of the invention;

FIG. 6 is an illustration of a CK portion of flip-flop circuitry in an exemplary implementation of the invention;

FIG. 7A is an illustration of a sleep transistor for an OFF node in an exemplary implementation of the invention;

FIG. 7B is an illustration of a sleep transistor for an SB node in an exemplary implementation of the invention;

FIG. 7C is an illustration of a moderate impedance transistor for an SB node in an exemplary implementation of the invention;

FIG. 8A is an illustration of circuitry for a tristate inverter in the master latch in an exemplary implementation of the invention;

FIG. 8B is an illustration of circuitry for a tristate inverter in the slave latch in an exemplary implementation of the invention;

FIG. 9 is an illustration of HOLDB and SLEEPB signals in an exemplary implementation of the invention;

FIG. 10 is an illustration of circuitry for low leakage and data retention in an exemplary implementation of the invention;

FIG. 11 is an illustration of slave latch circuitry in an exemplary implementation of the invention; and

FIG. 12 is an illustration of circuitry for a level shifter for an I/O pad in an exemplary implementation of the invention.

DETAILED DESCRIPTION OF THE INVENTION

A description of example embodiments of the invention follows.

As shown in the exemplary drawings wherein like reference numerals indicate like or corresponding elements among the figures, exemplary embodiments of a system and method according to the present invention are described below in detail. It is to be understood, however, that the present invention may be embodied in various forms. Therefore, specific details disclosed herein are not to be interpreted as limiting, but rather as a basis for the claims and as a representative basis for teaching one skilled in the art to employ the present invention in virtually any appropriately detailed system, structure, method, process or manner.

Power Island Manager—FIGS. 2-4

In some embodiments, an integrated circuit can be delineated into power islands. Power consumption can then be controlled within the power island. A power island manager provides control signals to the power island to control power consumption of the power island. In some embodiments, the low leakage, data retention circuitry is located within the power islands.

FIG. 2 depicts an illustration of an integrated circuit 200 with a power supply 280 in an exemplary implementation of

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the invention. The integrated circuit 200 includes a central processing unit (CPU) 210, a clock manager 212, power island managers 220, 222, and 224, a power supply manager 240, level shifter/isolation gates (LS/ISO) 250, 252, and 254, logic (power island 2) 260, memory (power island 0) 262, third party intellectual property (IP) (power island 1) 264, adaptive leakage controller (ALC) 270, and bus 280.

A power island is any section, delineation, partition, or division of an integrated circuit where power consumption is controlled within the section, delineation, partition, or division. In some embodiments, the power islands are delineated based on geographic factors of the integrated circuit. In some embodiments, the power islands are delineated based on functional IP units of the integrated circuit 200. In this example depicted in FIG. 2, power islands are delineated by memory 262, logic 260, and third party IP 264. Power islands are discussed in further detail in pending U.S. patent application Ser. No. 10/840,893, entitled “Managing Power on Integrated Circuits Using Power Islands”, filed on May 7, 2004, which is hereby incorporated by reference.

The power island managers 220, 222, and 224 are any circuitry, device, or system configured to provide control signals to a power island to control power within the power island. The power island managers 220, 222, and 224 can dynamically change the power consumption of the power islands based on the needs and operation of the integrated circuit 200. The power island managers 220, 222, 224 may select a clock, change clock frequency, or modify the voltage within the power island to control the power consumption of the power island.

The ALC 270 provides control signals to compensate for process and temperature variation to provide the optimum voltage to be applied to sleep transistors in the power islands. The ALC 270 is described in further detail U.S. patent application Ser. No. 10/996,739, entitled “Systems and Methods for Minimizing Static Leakage of an Integrated Circuit”, filed on Nov. 17, 2004, which is incorporated herein for reference.

FIG. 2A is a block diagram of a leakage manager system 290 for minimizing static leakage of a logic gate by application of a negative voltage to a sleep transistor in accordance with an example embodiment. The leakage manager system 290 comprises an adaptive leakage controller (ALC) 291, a negative voltage regulator 292, and a charge pump 294. The charge pump 294 generates a negative voltage 295 (SLPB). The ALC 291 determines whether to adjust the negative voltage 295. The ALC 291 generates a signal (depicted as CTRL) depending on the determination. The negative voltage regulator 292 adjusts the negative voltage 295 depending on the CTRL signal.

As described further herein, the negative voltage regulator 292 of one embodiment generates an enable (EN) signal to the charge pump 294 to enable the charge pump 294 to increase the magnitude of the negative voltage 295 (i.e., to make the negative voltage 295 more negative). If the EN signal is low, an alternating signal from an oscillator 293 to the charge pump 294 is disabled, preventing the charge pump 294 from increasing the magnitude of the negative voltage 295. Alternatively, if the EN signal is high, the alternating signal from the oscillator 293 is enabled so that the charge pump 294 will increase the magnitude of the negative voltage 295. Because the negative voltage regulator 292 toggles the EN signal on or off depending on whether the ALC 291 determines to adjust the negative voltage 295, the leakage manager system 290 maintains the negative voltage 295 at a particular negative voltage to minimize static leakage of the logic gate.

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Under normal operation where the digital logic block is to operate, the sleep control receives a signal (sleep input, polarity unimportant here) to disable the charge pump and raise V_{sleep} voltage to V_{DD} .

Under idle operation, where the digital logic block is to sleep (change to a low leakage current state), the Charge Pump Control Logic (CPCL) sends a clock signal and an enable signal to the Negative Voltage Charge Pump (NVCP) to first rapidly drop the V_{sleep} signal to V_{SS} . Then the charge pump begins to push the V_{sleep} voltage below V_{SS} and continues to do so until it receives a pause signal from the CPCL. The Negative Bias Voltage Bias Regulator (NVBR) monitors the V_{sleep} voltage until a desirable reduction of the transistor current I_{off} has been achieved. At that point it sends a signal to the CPCL to initiate a Pause signal to the NVCP. As time passes the V_{sleep} voltage will slowly drift upwards toward V_{SS} and at a preset transistor I_{off} the NVBR sends a signal to the CPCL to restart the NVCP to restore the V_{sleep} negative voltage to achieve the desired I_{off} .

FIG. 3 depicts an illustration of the power island manager 220 with an isolation gate 350 and a D flip-flop 360 in an exemplary embodiment of the invention. The power island manager 220 includes a data retention state machine 330 and a sleep generator 340 that are coupled to each other.

The power island manager 220 is coupled to the isolation gate 350 by the ISO signal. The ISO signal is also coupled to other isolation gates. The data retention state machine 330 is coupled to DRB input of the D flip-flop 360 via the DRB signal. The data retention state machine 330 is also coupled to the AND gate 362 via the ENC signal. The clock island (CKI) signal is coupled to the data retention state machine 330 and the AND gate 362. The sleep generator 340 is coupled to the D flip-flop 360 and the AND gate 362 via the SLPB signal. The output of the AND gate 362 is coupled to the C input of the D flip-flop 360 via the CKA signal. The system reset signal is coupled to the RESETB input of the power island manager 220 and the RB input of the D flip-flop 360. The SLPB signal, the DRB signal, and the system reset signal are coupled to other data retention flip-flops.

FIG. 4 depicts an illustration of a power island manager 220 in an exemplary embodiment of the invention. The power island manager 220 includes an AND gate 402, a multiplexer (MUX) 404, a D flip-flop 410, an inverter 412, an AND gate 414, a D flip-flop 420, a D flip-flop 430, the data retention state machine 330, a MUX 432, a MUX 442, a sleep generator 340, and a buffer 452.

The DI0 pin is coupled to the D input of the D flip-flop 410. The SI0 pin is coupled to the SI input of the D flip-flop 410. The CSB and the WEB pins are coupled to the inputs of the AND gate 402. The output of the AND gate 402 and the SCK1 pin are coupled to the input of the MUX 404. The output of the MUX 404 is coupled to the C inputs of the D flip-flop 410, the D flip-flop 420, and the D flip-flop 430. The Q output of the D flip-flop 410 is coupled to the DO0 pin, which is coupled to the input of the inverter 412 and the SI input of the D flip-flop 420. The DI1 pin is coupled to the D input of the D flip-flop 420. The Q output of the D flip-flop 420 is coupled to the DO1 pin, which is coupled to the input of the AND gate 414 and the SI input of the D flip-flop 430. The output of the AND gate 414 is coupled to the RSTB pin. The DI2 pin is coupled to the D input of the D flip-flop 430. The Q output of the D flip-flop 430 is coupled to the DO2 pin, which is coupled to the DLY1/ISO pin. The DLY1/ISO pin is coupled to the SO1, the input of the MUX 432, and the data retention state machine 340.

The RESETB pin is coupled to the R input of the D flip-flop 430, the D flip-flop 420, and the D flip-flop 410. The SE pin,

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the RESETB pin, the CKI pin, and the SI2 pin are coupled to the data retention state machine 330. The data retention state machine 330 is coupled to the input of the MUX 432, the SO2 pin, the DRB pin, the ENC pin, and the input of the MUX 442. The output of the MUX 442, the VDDI pin, and the VL[0:2] are coupled to the sleep generator 340. The sleep generator 340 is coupled to the SLPB pin. The sleep generator 340 is coupled to the data retention state machine 330 via the AW pin and the input of the buffer 452. The output of the buffer 452 is coupled to the DO3 pin. The DRMODE pin is coupled to the MUX 442.

In operation, the power island manager 220 has a three bit register for controlling a power island for some embodiments. D [0], with input DI0 and output DO0, is an island reset for re-initializing a power island. This bit is combined with RESETB to form RSTB to re-initialize the power island whenever RESETB or the D [0] is active. D [1], with input DI1 and output DO1, is a sleep bit. When the D [1] bit is set to one, the power island goes into a low leakage state. D [2], with input DI2 and output DO2, is a DLY1/Isolate bit. When DRMODE is tied to low, the D [2] bit, when set to one, will add one clock cycle delay between DRB going active and SLPB going active. When DRMODE is tied high, the D [2] bit, when set to one, will activate isolation of the power island. D [3], such as DO3, is an awake bit. This D [3] bit goes high when SLPB is high. This can be used by software to determine when a power island is out of the sleep state.

The power island manager 220 has two operating modes: one that supports power islands with data retention flip-flops and one that does not. When the DRMODE pin is tied high, a power island is put to sleep by writing a one to D[1]. The data retention state machine 330 performs the timing. The isolate (ISO) signal goes active when the sleep bit is written to a one, and the enable clock (ENC) and the data retention (DRB) will go low after synchronization to the power island clock (CKI). One or two clock cycles later the sleep (SLPB) goes low. To come out of sleep mode, a zero is written to D[1]. In some embodiments, all clock buffers in the power islands can be put to sleep to further minimize leakage. Software can determine when the power island has come out of sleep by reading when DO3 is high.

The System Reset is typically applied once after initial system power up. In some embodiments, the System Reset goes to all data retention flip-flops. The System Reset signal and DI0 bar are combined in a logical AND (RSTB output) to provide initialization to non data retention flip-flops. To create a power island reset, D[0] is set to a one and then cleared to a zero by software.

When the DRMODE is tied low, the power island manager 220 can also provide the control signals for a power island without data retention flip-flops. The power island manager 220 may have a hardware driven method and a software driven method for interfacing to power islands without data retention flip-flops. The software sequence has the following sequence:

Write 04/turn on isolation
Write 06/turn on sleep, isolation on/come out of sleep
Write 05/turn sleep off, reset island, isolation on/wait for sleep to go high
Read/test for DO3=1; sleep is high
Write 00/turn isolation off, normal operation

The hardware driven method uses a clock to sequence the state machine. The only action software takes is to write the sleep bit (DI1) to a one to go into sleep and write a zero to the sleep bit to go out of sleep. Software can determine when the island has come out of sleep by reading when DO3 is high.

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In some embodiments, the power island manager **220** contains two scan chains because some of the flip-flops are clocked on the positive and some on the negative. The scan chain enable pin switches the clock on scan chain 1 (SI1 is the input; SO1 is the output), the registers, to CKS1. Scan chain 2 (SI2 is the input; SO2 is the output) is connected to the data retention state machine **330** flip-flops that are clocked on the negative edge of CKI. A separate scan out is provided for each clock domain.

In some embodiments, the SLPB net uses p-type antenna diodes. Since the SLPB net may go to a negative voltage, an n-type antenna diode can cause excessive leakage to ground. The leakage can cause SLPB not to go negative and may not work properly. The CSB pin is a chip select pin. The WEB pin is the write enable pin. The VL [2:0] is the leakage control voltage value equal to or greater than the VDD (FIG. 2). The VDDI is the VDD from the power island.

Low Leakage, Data Retention Circuitry—FIGS. 5, 6, 7A-C, 8A-8B, and 9-12

FIGS. 5, 6, 7A-C, and 8A-8B disclose one embodiment for low leakage, data retention circuitry. In this embodiment, in sleep mode, the circuit parts of a flip-flop that do not require data retention are coupled to ground through a sleep transistor. The gate of the sleep transistor is coupled to a sleep signal that can be driven to a negative voltage such as $-0.3V$. Thus, the leakage in these circuit parts of the flip-flop is eliminated (reduced). When not in a sleep state, the sleep transistor has a gate value equal to or greater than the VDD supply, which effectively grounds the circuit.

The circuit parts that require data retention are coupled to ground through two transistors. One transistor acts effectively to ground the circuit above when not in sleep mode just as the sleep transistor described above. The other transistor is a PMOS device with the gate tied to ground, which provides medium impedance to ground. The voltage drop across this transistor acts to reduce the leakage by increasing the source bias of the NMOS transistors and simultaneously reduces the voltage across the circuit. In this embodiment, the data is retained in a sleep state and reduces the leakage by a factor of 22.

FIG. 5 depicts an illustration of a D/Q portion **500** of the flip-flop circuitry in an exemplary implementation of the invention. The D/Q portion **500** of the flip-flop circuitry includes an inverter **502**, an M3 PMOS transistor **504**, an M4 NMOS transistor **506**, master latch circuitry **510**, an M11 PMOS transistor **522**, an M12 NMOS transistor **524**, an M13 NMOS transistor **526**, slave latch circuitry **530**, and an inverter **540**.

The D signal input is the input of the inverter **502**, which includes transistors M1 and M2. The source of the inverter **502** is coupled to the node OFF, which is described below in FIG. 7A. The output of the inverter **502** is coupled to the M3 PMOS transistor **504** and the M4 NMOS transistor **506**. The gate of the M3 PMOS transistor **504** is coupled to the CLK signal input. The gate of the M4 NMOS transistor **506** is coupled to the CLKB signal input.

The master latch circuitry **510** includes the inverter **512** and the inverter **514**. The inverter **514** forms a feedback loop with the inverter **512**, where the output of the inverter **512** is coupled to the input of the inverter **514** and the output of the inverter **514** is coupled to the input of the inverter **512**. The inverter **512** corresponds to transistor M5 and M6. The inverter **514** corresponds to transistors M7-M10. The input of the inverter **512** is coupled to node A, which is described in FIG. 8A below. The source of the inverter **512** is also coupled to node OFF, which is described below in FIG. 7A. The output of the inverter **512** is coupled to node B, which is described

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below in FIG. 8A. The source of the inverter **514** is coupled to node OFF, which is described below in FIG. 7A. The PMOS gate of the inverter **514** is coupled to the CLKB signal input. The NMOS gate of the inverter **514** is coupled to the CLK signal input.

The M11 PMOS transistor **522** is in parallel to the M12 NMOS transistor **524** and the M13 NMOS transistor **526**, which are in series. The gate of the M11 PMOS transistor **522** is coupled to the CLKB signal input. The gate of the M12 NMOS transistor **524** is coupled to the HOLDB signal input. The gate of the M13 NMOS transistor **526** is coupled to the CLK signal input.

The slave latch circuitry **530** includes the inverter **532** and the inverter **534**. The inverter **534** forms a feedback loop with the inverter **532**, where the output of the inverter **532** is coupled to the input of the inverter **534** and the output of the inverter **534** is coupled to the input of the inverter **532**. The inverter **532** corresponds to transistor M14 and M15. The inverter **534** corresponds to transistors M18-21 and M31. The input of the inverter **532** is coupled to node C, which is described in FIG. 8B below. The source of the inverter **532** is also coupled to node SB, which is described below in FIGS. 7B-C. The output of the inverter **532** is coupled to node D, which is described below in FIG. 8B. The source of the inverter **534** is coupled to node SB, which is described below in FIGS. 7B-C. The PMOS gates of the inverter **534** are coupled to the HOLDB and CLK signal inputs. The NMOS gate of the inverter **534** is coupled to the CLKB signal input.

The output of the inverter **532** is coupled to the input of the inverter **540**. The inverter **540** corresponds to transistors M16 and M17. The source of the inverter **540** is also coupled to node OFF, which is described below in FIG. 7A. The output of the inverter **540** is the Q signal output.

FIG. 6 depicts a CK portion **600** of the flip-flop circuitry in an exemplary implementation of the invention. The CK portion **600** of the flip-flop circuitry includes an inverter **602**, an M24 PMOS transistor **604**, an M25 PMOS transistor **606**, an M26 NMOS transistor **608**, an M32 NMOS transistor **610**, and an M27 PMOS transistor **612**.

The CK signal input is the input of the inverter **602**, which includes transistors M22 and M23. The source of the inverter **602** is coupled to node OFF, which is described below in FIG. 7A. The output of the inverter **602** is coupled to the drain of the M24 PMOS transistor **604** and the node CLKB. The gate of the M24 PMOS transistor **604** is coupled to the HOLDB signal input. The output of the inverter **602** is also coupled to the M25 PMOS transistor **606** and the M26 NMOS transistor **608**. The M25 PMOS transistor **606**, the M26 NMOS transistor **608**, and the M32 NMOS transistor **610** are coupled in series. The gate of the M32 NMOS transistor **610** is coupled to the HOLDB signal input.

The CLK signal output is coupled to the drain of the M25 PMOS transistor **606**, the drain of the M26 NMOS transistor **608**, and the drain of the M27 PMOS transistor **612**. The gate of the M27 PMOS transistor **612** is coupled to the HOLDB signal input.

FIG. 7A depicts a sleep transistor **702** for the OFF node in an exemplary implementation of the invention. The sleep transistor **702** is an NMOS transistor that corresponds to transistor M28. The drain of the sleep transistor **702** is coupled to the OFF node. The gate of the sleep transistor **702** is coupled to the SLEEPB signal input. The source of the sleep transistor **702** is coupled to ground. In some embodiments, the OFF node can be separated into two or more nodes each having its own NMOS sleep transistor.

FIG. 7B depicts a sleep transistor **704** for the SB node in an exemplary implementation of the invention. The sleep tran-

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sistor **704** is an NMOS transistor that corresponds to transistor **M29**. The drain of the sleep transistor **704** is coupled to the SB node. The gate of the sleep transistor **704** is coupled to the SLEEPB signal input. The source of the sleep transistor **704** is coupled to ground.

FIG. 7C depicts a sleep transistor **706** for the SB node in an exemplary implementation of the invention. The sleep transistor **706** is a PMOS transistor that corresponds to transistor **M30**. The source of the sleep transistor **706** is coupled to the SB node. The gate and drain of the sleep transistor **706** are coupled to ground.

FIG. 8A depicts circuitry **800** for the tristate inverter in the master latch in an exemplary implementation of the invention. The circuitry **800** for the master latch includes a PMOS transistor **802**, a PMOS transistor **804**, an NMOS transistor **806**, and an NMOS transistor **808** that are coupled together in series. The gates of the PMOS transistor **802** and the NMOS transistor **808** are coupled to the node B. The gate of the PMOS transistor **804** is coupled to the CLKB signal input. The gate of the NMOS transistor **806** is coupled to the CLK signal input. The drains of the PMOS transistor **804** and the NMOS transistor **806** are coupled to node A. The source of the NMOS transistor **808** is coupled to node OFF.

FIG. 8B depicts circuitry **810** for the tristate inverter in the slave latch in an exemplary implementation of the invention. The circuitry **810** for the slave latch includes a PMOS transistor **812**, a PMOS transistor **814**, a PMOS transistor **816**, an NMOS transistor **818**, and an NMOS transistor **820**. The PMOS transistor **812** is coupled to the PMOS transistor **814** and the PMOS transistor **816** that are parallel to each other. The PMOS transistor **814** and the PMOS transistor **816** are coupled to the NMOS transistor **818**, which is also coupled to the NMOS transistor **820**.

The gates of the PMOS transistor **812** and the NMOS transistor **820** are coupled to the node D. The gate of the PMOS transistor **814** is coupled to the HOLDB signal input. The gate of the PMOS transistor **816** is coupled to the CLK signal input. The gate of the NMOS transistor **818** is coupled to the CLKB signal input. The drains of the PMOS transistor **814**, the PMOS transistor **816**, and the NMOS transistor **806** are coupled to node C. The source of the NMOS transistor **820** is coupled to node SB.

FIG. 9 depicts an illustration of the HOLDB and SLEEPB signals in an exemplary embodiment of the invention.

The operation begins with CK going to zero. This causes CLKB to be equal to VDD and CLK to be equal to zero, which isolates the slave latch circuitry **530** from the master latch circuitry **510**. The HOLDB signal goes to 0 to retain the state of the slave latch. The SLEEPB signal then goes to -0.3V. This shuts off transistor **M28** in FIG. 7A, which halts the leakage from all the circuits except in the slave latch circuitry **530**. When not in sleep mode, transistor **M28** provides a low impedance path to ground.

The slave latch circuitry **530** is coupled to ground through the transistors **M29** and **M30**, respectively depicted in FIGS. 7B and 7C. One purpose of transistor **M29** is to provide a low impedance path to ground when not in sleep mode.

One purpose of transistor **M30** is to provide a default moderate impedance path to ground when transistor **M29** is off or in sleep mode. The leakage in the slave latch circuitry **530**, in going through transistor **M30**, causes node SB to rise. This provides a source bias to the slave NMOS transistors reducing the leakage through them and also reduces the voltage across the slave side to VDD-SB, which further reduces the leakage. Equilibrium is reached where the leakage cannot increase. Basically, the leakage is used to limit itself.

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This embodiment uses the gated VDD solution because the voltage across the circuit is reduced to VDD-SB. This embodiment combines this gated VDD with the modulated back gate bias method because of the source bias SB but only for the NMOS transistors. This is accomplished without switching a lower VDD and driving a well. Thus, a simple process can be used. Also, this embodiment advantageously uses the moderate impedance transistor in a way that causes leakage to limit itself by reaching equilibrium.

FIGS. 10 and 11 disclose another embodiment for low leakage, data retention circuitry. In this embodiment, in a sleep state, the circuitries that do not require data retention are coupled to ground through a sleep transistor. The logic coupled to the transistors gated by the SLEEPB signal is shut off and draws minimal leakage. This process is accomplished by driving the SLEEPB signal below VSS by 0.3-0.4V. The HOLDB signal keeps the slave latch circuitry from changing state while the rest of the flip-flop comes out of the sleep state. The only part of the flip-flop still powered is the slave latch circuitry. The slave latch circuitry combines several techniques to minimize leakage.

FIG. 10 depicts circuitry **1000** for low leakage and data retention in an exemplary embodiment of the invention. The circuitry **1000** includes the inverter **1002**, the master latch circuitry **1010**, the slave latch circuitry **1020**, the inverter **1032**, the inverter **1034**, the sleep transistors **1042**, **1044**, **1046**, and **1048**, the inverter **1052**, and the inverter **1054**.

The D input is the input for the inverter **1002**. The master latch circuitry **1010** includes the transmission gate **1012**, the inverter **1014**, the transmission gate **1016**, and the inverter **1018**. The output of the inverter **1002** is coupled to the left contact of the transmission gate **1012**. The right contact of the transmission gate **1012** is coupled to the input of the inverter **1014** and the left contact of the transmission gate **1016**. The output of the inverter **1014** is coupled to the D input of the slave latch circuitry **1020** and the input of the inverter **1018**. The output of the inverter **1018** is coupled to the DB input of the slave latch circuitry **1020** and the right contact of the transmission gate **1016**.

The SLEEPB signal input is coupled to the gates for the SL1 sleep transistor **1042**, the SL2 sleep transistor **1044**, the SL3 sleep transistor **1046**, the SL4 sleep transistor **1048**, and the SLEEPB input of the slave latch circuitry **1020**. The SL1 sleep transistor **1042** is coupled to the inverter **1002** and ground. The SL2 sleep transistor **1044** is coupled to the inverter **1052**, the inverter **1054**, and ground. The SL3 sleep transistor **1046** is coupled to the inverter **1014**, the inverter **1018**, and ground. The SL4 sleep transistor **1048** is coupled to the inverter **1032**, the inverter **1034**, and ground. In some embodiments, the SL1 sleep transistor **1042**, the SL2 sleep transistor **1044**, the SL3 sleep transistor **1046**, and the SL4 sleep transistor **1048** can each be separated into two or more nodes each having its own NMOS sleep transistor.

The CK signal is the input of the inverter **1052**. The output of the inverter **1052** is coupled to the transmission gate **1012**, the transmission gate **1016**, and the input of the inverter **1054**. The output of the inverter **1054** is coupled to the transmission gate **1012**, the transmission gate **1016**, and the CLK input of the slave latch circuitry **1020**. The HOLDB signal input is coupled to the HOLDB input of the slave latch circuitry **1020**. The output of the slave latch circuitry **1020** is coupled to the input of the inverter **1032**. The output of the inverter **1032** is coupled to the input of the inverter **1034**. The output of the inverter **1034** is the Q signal.

FIG. 11 depicts slave latch circuitry **1020** in an exemplary embodiment of the invention. The slave latch circuitry **1020** includes D1 transistor **1102**, D2 transistor **1104**, DH transis-

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tor **1106**, DSL sleep transistor **1108**, stack transistors **1110**, stack transistors **1120**, D1B transistor **1132**, D2B transistor **1134**, DHB transistor **1136**, and sleep transistor **1138**.

The D1 transistor **1102**, the D2 transistor **1104**, the DH transistor **1106**, and the DSL sleep transistor **1108** are coupled to each other in series with the sleep transistor **1108** coupled to ground. The gate of the D1 transistor **1102** is coupled to the CLK signal input. The gate of the D2 transistor **1104** is coupled to the D signal input. The gate of the DH transistor **1106** is coupled to the HOLDB signal input. The gate of the sleep transistor **1108** is coupled to the SLEEPB signal input.

The stack transistors **1110** comprise P1 transistor **1112**, P0 transistor **1114**, N1 transistor **1116**, and N0 transistor **1118**. The P1 transistor **1112**, the P0 transistor **1114**, the N1 transistor **1116**, and the N0 transistor **1118** are coupled to each other in series with the N0 transistor **1118** coupled to ground. The gates of the P1 transistor **1112**, the P0 transistor **1114**, the N1 transistor **1116**, and the N0 transistor **1118** are coupled to the LAT signal input. The drains of the P0B transistor **1124** and the N1B transistor **1126** are coupled to the LAT signal input.

The stack transistors **1120** comprise P1B transistor **1122**, P0B transistor **1124**, N1B transistor **1126**, and N0B transistor **1128**. The P1B transistor **1122**, the P0B transistor **1124**, the N1B transistor **1126**, and the N0B transistor **1128** are coupled to each other in series with the N0B transistor **1128** coupled to ground. The gates of the P1B transistor **1122**, the P0B transistor **1124**, the N1B transistor **1126**, and the N0B transistor **1128** are coupled to the LATB signal input. The drains of the P0 transistor **1114** and the N1 transistor **1116** are coupled to the LATB signal input.

In operation, the logic coupled to the transistors gated by the SLEEPB signal is shut off and draws minimal leakage. This process is accomplished by driving the SLEEPB signal below VSS by 0.3-0.4V. The HOLDB signal keeps the slave latch circuitry **1020** from changing state while the rest of the flip-flop comes out of the sleep state. The only part of the flip-flop still powered is the slave latch circuitry **1020**. The slave latch circuitry **1020** combines several techniques to minimize leakage. Transistors not necessary for state retention (stacks with CLK) have sleep transistors to shut off leakage (gated by the SLEEPB signal).

The 8 transistors in the stack transistors **1110** and **1120** use two techniques to reduce leakage. The first technique used is transistor stacking, which is also called self-reverse bias. The N0 transistor **1118** and the N1 transistor **1116** will have some small leakage even when the gate is at 0V. As a result, VNN1 will be at a positive voltage. This causes VGS(N1) and VBS(N1) to be negative, and VDS(N1) to decrease. Consequently, the leakage current is reduced in N0 transistor **1118** and the N1 transistor **1116**. The same effect occurs on N0B transistor **1128**, N1B transistor **1126**, P0 transistor **1114**, P1 transistor **1112**, P0B transistor **1124**, and P1B transistor **1122**.

The second technique is called multiple threshold transistors. Increasing channel length of MOS transistors increases the threshold of the devices without any change in process complexity. The N0 transistor **1118**, the N1 transistor **1116**, the N0B transistor **1128**, and the N1B transistor **1126** have increased channel length, which raises VTH and reduces leakage current.

This embodiment reduces leakage by a factor of 25 over a current standard cell D flip-flop.

I/O Pad—FIG. 12

In some embodiments, a programmable general purpose input and output (I/O) padcell includes built in-level shifters

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and isolation that interface with the chip core logic. In these embodiments, a level shifter can be controlled to retain data.

FIG. 12 depicts circuitry **1200** for a level shifter for an I/O pad in an exemplary embodiment of the invention. The circuitry **1200** includes MP2 transistor **1202**, MP3 transistor **1204**, M3 transistor **1206**, M4 transistor **1208**, M1 transistor **1210**, M0 transistor **1212**, M5 transistor **1214**, M2 transistor **1216**, and an inverter **1218**.

The circuitry **1200** is for a latching level shifter. The M3 transistor **1206** and the M4 transistor **1208** are “native” cascode devices. The M3 transistor **1206** and the M4 transistor **1208** are also known as depletion-mode transistors. The M3 transistor **1206** and the M4 transistor **1208** are used to allow thin gate devices to be used in the input stage. This allows large voltage ratios between the VDD and the V3IO. The M0 transistor **1212** and the M1 transistor **1210** are output latching devices that allow the level shifter to retain the state when both IN and INB are 0. Thus, IN and INB control data retention.

In some embodiments, the gates of the M3 transistor **1206** and the M4 transistor **1208** are coupled to other transistors connected to the cascode voltage.

The following truth table is for circuitry **1200**.

IN	INB	OUT
0	0	Retain last state
0	1	0
1	0	1
1	1	Illegal

There will be setup time requirements for any signal compared to SLPB. If level shifters are used with an SRAM cell built into the output stage, the two inputs can be removed anytime after the output latch has flipped to a new state. Both 1.2V inputs to the level shifter cannot go to VDD. This can be prevented by including an inverter. If both the inverter and the level shifter have SLPB transistors, there is a potential timing race if SLPB goes to VSS with VDD high. In this case, the level shifters should be off before the output of the inverter drifts to VDD. In some embodiments, the M5 transistor **1214** and the M2 transistor **1216** can be configured to withstand greater voltages.

In some embodiments, the sources of the M5 transistor **1214** and the M2 transistor **1216** can be coupled to a common SLEEPB transistor **1240** to further reduce leakage. In one embodiment, the width of the SLEEPB transistor **1240** is 4 micrometers, and the length is 0.13 micrometers. The following truth table is for circuitry **1200** including this common SLEEPB transistor **1240**:

SLEEPB	IN	INB	OUT
1	0	0	Retain state (Data Retention)
1	0	1	0
1	1	0	1
1	1	1	Illegal
0	X	X	Retain State

In some embodiments, the SLEEPB=0 input state should be understood to include the SLEEPB voltage being below 0V (E.g. -0.35V generated by a leakage optimization circuit).

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In this extension to FIG. 12 (and the above truth table), the two Data Retention states may be operated independently, sequentially or simultaneously. This is beneficial when the SLEEPB input is used to control/limit leakage power while the IN/INB=00 state is used for data retention. This is because the SLEEPB voltage comes from a charge pump and takes some time to transition from Vdd (=1) to the Data Retention mode.

The above description is illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

While this invention has been particularly shown and described with references to example embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

What is claimed is:

1. An integrated circuit comprising:

a plurality of power islands having associated power consumptions capable of being dynamically changed, each of the power islands including circuitries and sleep transistors in coupled relation with the circuitries; and a sleep generator in communication with at least one of the power islands to provide a variable voltage, and the sleep transistors being included within the integrated circuit to facilitate reduction of power consumed by the circuitries, and the sleep transistors being configured to receive the variable voltage that is:

- i) generated by the sleep generator based on a control signal receivable from an adaptive leakage controller; and
- ii) changed under control of the adaptive leakage controller.

2. The integrated circuit as claimed in claim 1 wherein the at least one of the power islands can be put to sleep and taken out of sleep at different times.

3. The integrated circuit as claimed in claim 2 wherein the sleep generator is within a power island manager that includes a state machine to control when the at least one of the power islands is put to sleep and when the at least one of the power islands is taken out of sleep.

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4. The integrated circuit as claimed in claim 1 wherein the power islands are delineated based on functional intellectual property units of the integrated circuit.

5. The integrated circuit as claimed in claim 1 wherein the power islands are delineated by memory, logic and third party intellectual property.

6. The integrated circuit as claimed in claim 1 wherein the variable voltage is an optimum voltage.

7. The integrated circuit as claimed in claim 6 wherein the optimum voltage is dependent upon both process variation and temperature variation.

8. The integrated circuit as claimed in claim 1 wherein the sleep generator comprises a charge pump.

9. The integrated circuit as claimed in claim 1 wherein the control signal is a digital signal.

10. A method carried out in an integrated circuit that includes an adaptive leakage controller and a plurality of power islands, each power island of the plurality of power islands including circuitries and sleep transistors in coupled relation with the circuitries, and the method comprising:

- generating a variable voltage based on a control signal received from the adaptive leakage controller;
- providing the variable voltage to at least one of the power islands;
- receiving the variable voltage at the sleep transistors to facilitate reduction of power consumed by the circuitries; and
- dynamically changing, under control of the adaptive leakage controller, the variable voltage.

11. The method as claimed in claim 10 further comprising putting to sleep and taking out of sleep, at different times, the at least one of the power islands.

12. The method as claimed in claim 11 wherein the putting to sleep and the taking out of sleep is controlled by a state machine.

13. The method as claimed in claim 10 wherein the variable voltage is an optimum voltage.

14. The method as claimed in claim 13 wherein the optimum voltage is dependent upon both process variation and temperature variation.

15. The method as claimed in claim 13 wherein the optimum voltage is generated by a charge pump.

16. The method as claimed in claim 10 wherein the control signal is a digital signal.

* * * * *

EXHIBIT G



US007224563B2

(12) **United States Patent**
Naffziger

(10) **Patent No.:** **US 7,224,563 B2**

(45) **Date of Patent:** **May 29, 2007**

(54) **METHOD AND DEVICE FOR CIRCUIT CONTROL**

(58) **Field of Classification Search** 361/115,
361/103, 90
See application file for complete search history.

(75) Inventor: **Samuel D. Naffziger**, Fort Collins, CO
(US)

(56) **References Cited**

(73) Assignee: **Hewlett-Packard Development Company, L.P.**, Houston, TX (US)

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 655 days.

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(21) Appl. No.: **10/651,360**

U.S. Appl. No. 60/480,056, Naffziger.

(22) Filed: **Aug. 29, 2003**

* cited by examiner

(65) **Prior Publication Data**

Primary Examiner—Stephen W. Jackson

US 2004/0257723 A1 Dec. 23, 2004

(57) **ABSTRACT**

Related U.S. Application Data

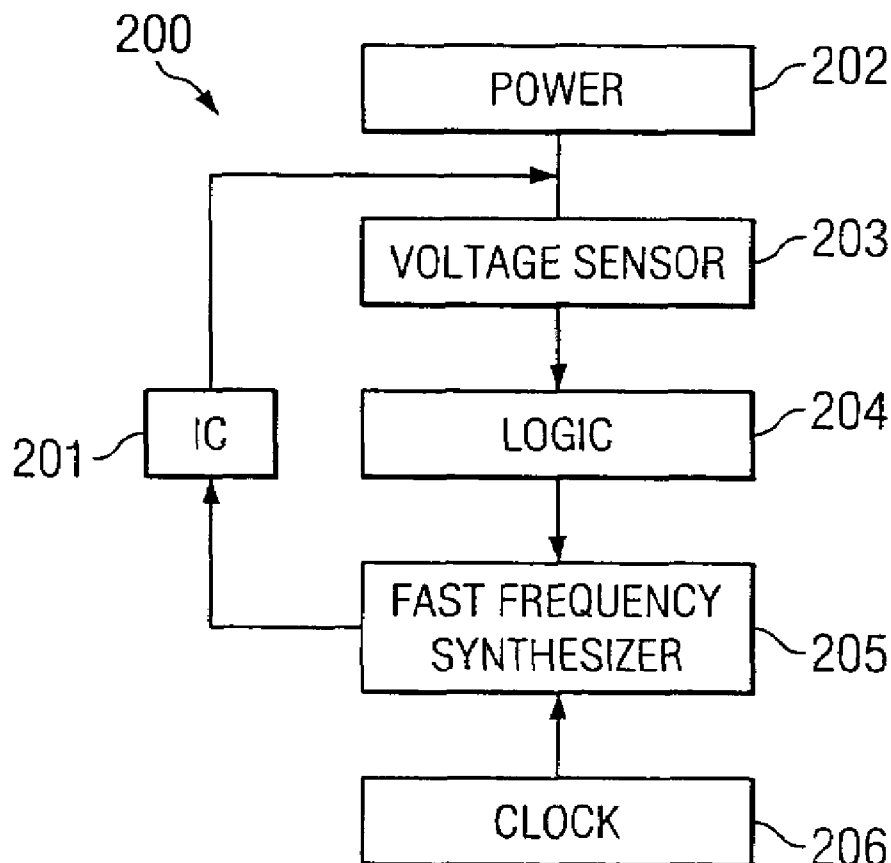
(60) Provisional application No. 60/480,056, filed on Jun. 20, 2003.

One disclosed embodiment of the invention is directed to circuit control that comprises sensing a delivered voltage to a portion of an integrated circuit, determining an appropriate frequency for the portion of the integrated circuit, and providing the appropriate frequency to the integrated circuit.

(51) **Int. Cl.**
H02H 7/00 (2006.01)

(52) **U.S. Cl.** 361/115; 361/90

35 Claims, 4 Drawing Sheets



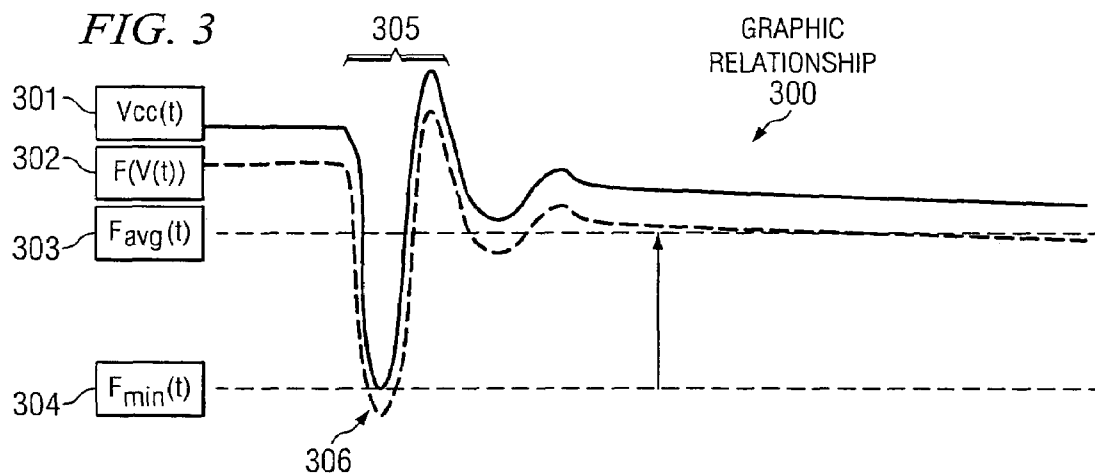
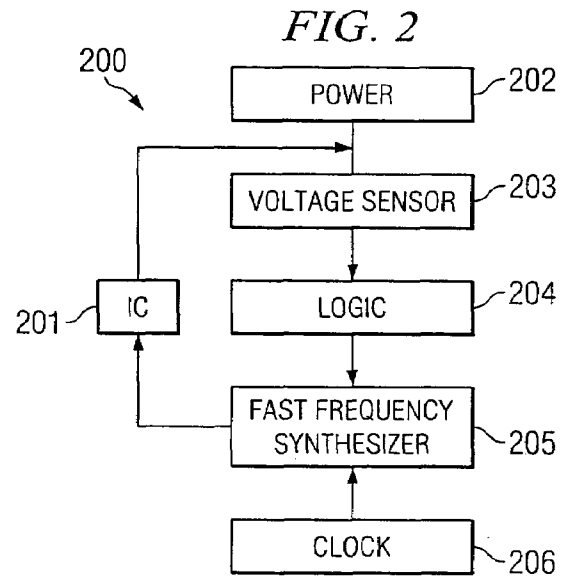
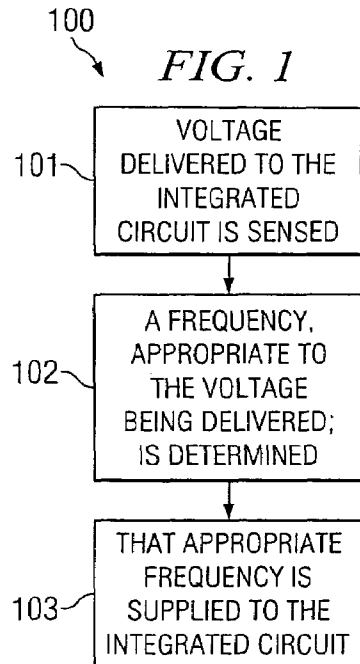


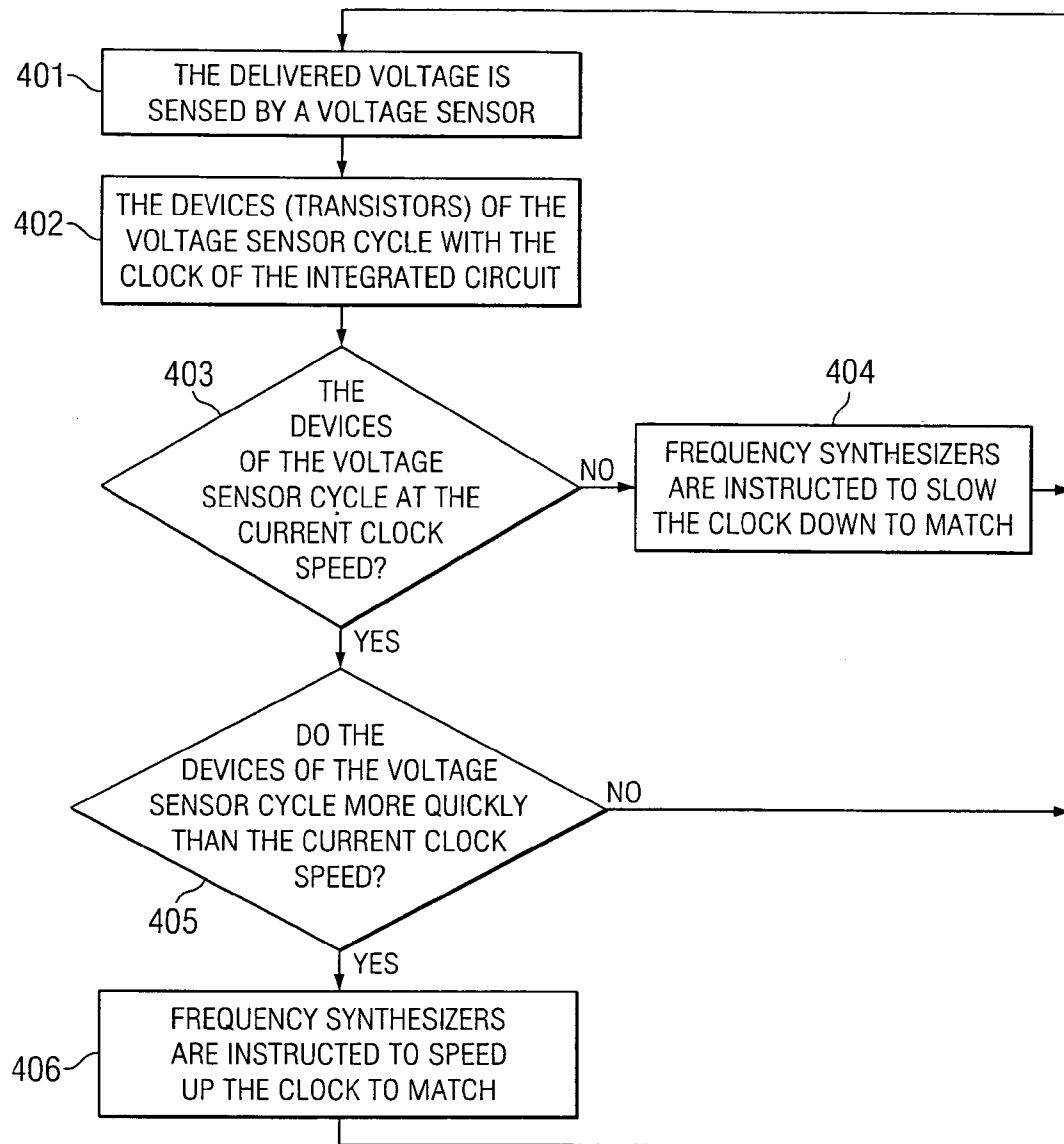
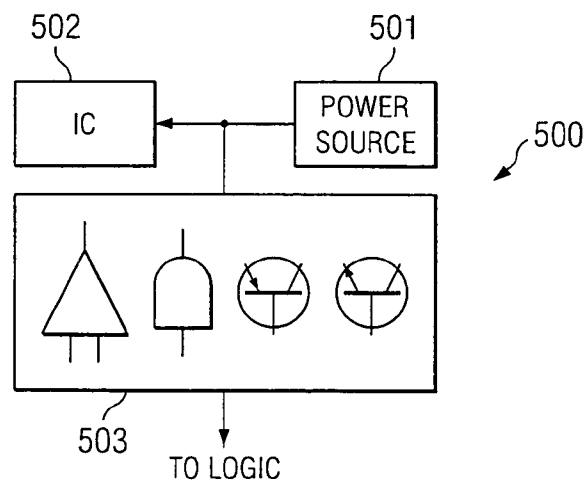
FIG. 4*FIG. 5*

FIG. 6

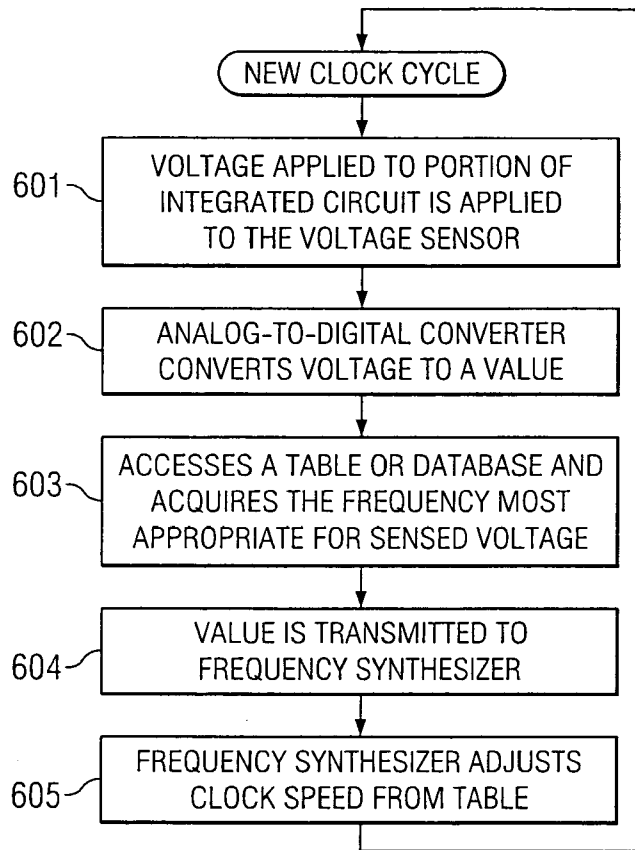
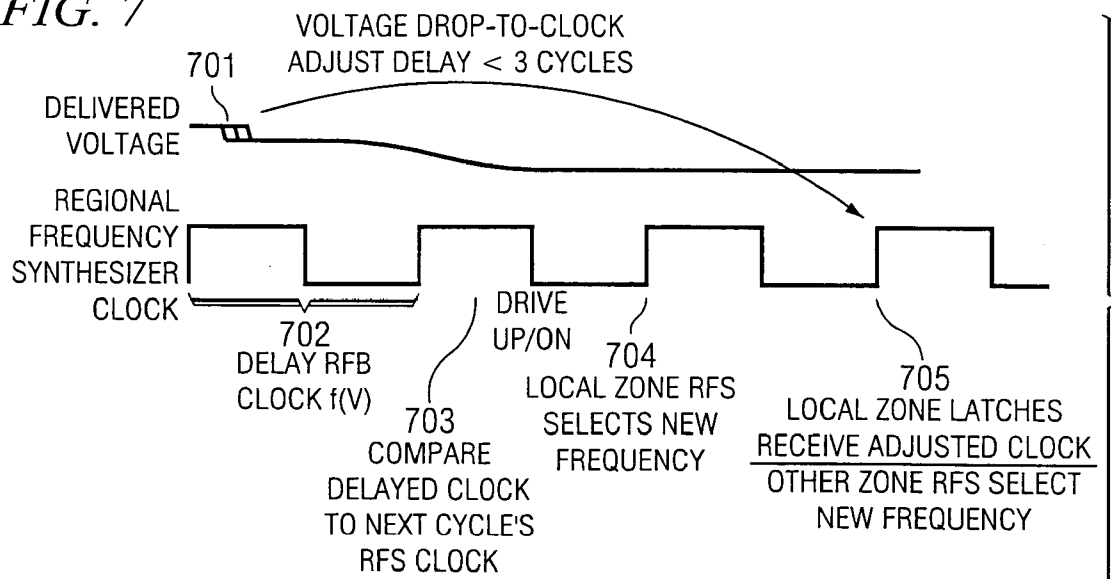


FIG. 7

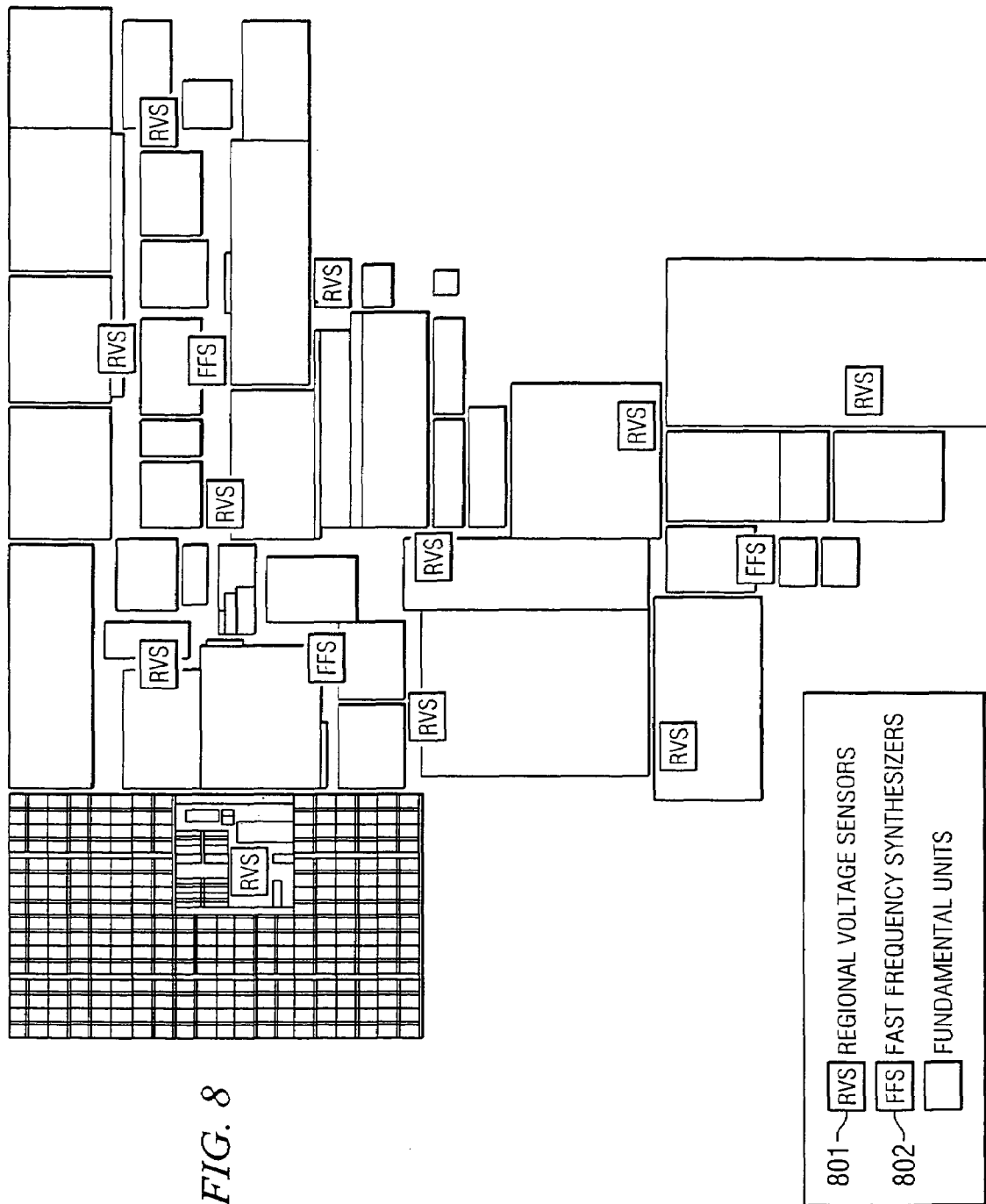


U.S. Patent

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METHOD AND DEVICE FOR CIRCUIT CONTROL

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to U.S. Provisional Patent Application No. 60/480,056, filed Jun. 20, 2003, entitled "A SYSTEM FOR RAPID ADAPTATION OF CLOCK FREQUENCY TO VOLTAGE TRANSIENTS."

BACKGROUND

Because of trends in process technology, scaling, and the frequency of operations for VLSI devices, power consumption has become a dominant issue in integrated circuit design. Managing power consumption is thus a high priority in the design objectives of these devices.

It is broadly recognized in the implementation of power management systems for VLSI devices that the most efficient means of power management is to simultaneously change 1) the voltage delivered to an integrated circuit, and 2) the frequency of that integrated circuit's operation. Because voltage is a primary determinant of switching speed for transistors of an integrated circuit, a designer will typically specify the maximum frequency at which a part can operate for a given voltage. Thus, for an example micro-processor, a power supply may generate a fixed voltage of 2 volts to a device and the device may be specified as operating at 2 GigaHertz (GHz). However, the design of the device has to be such that the voltage seen at the integrated circuit is never below the level that enables the full 2 GHz operation. If the voltage on the integrated circuit falls below that level, there could be a timing failure and some of the components would be unable to switch fast enough to make the 2 GHz cycle times.

But power supplies vary and electrical parasitics between the power supply and the actual transistors of an integrated circuit effect power transmission. Thus the voltage actually delivered to an integrated circuit is not a completely fixed value, but rather ripples and varies with time. On average these ripples may have a total magnitude of approximately + or -10% of the total voltage. If the intent is to deliver 2 volts to the integrated circuit, the actual delivered voltage may vary between 1.8 volts and 2.2 volts. Since the voltage in large part determines the switching speed of components, designers have to make sure that (in the current example) the device in use can still operate at 2 GHz even if the delivered voltage is 1.8 volts. This is a technique known as guardbanding. Without this guardbanding, the integrated circuit could fail when the voltage drops.

For power consumption, two relationships become important when the voltage varies. One is the relationship of the device speed to voltage; a relationship that is approximately linear. If the voltage applied to a transistor is lowered by 10%, the switching speed of that transistor is reduced by approximately 10%. A first order approximation can be shown as:

$$F \propto V \quad (1)$$

The second relationship is between power and frequency. Power (the total wattage dissipated by an integrated circuit) is equal to the switching capacitance of a device (a relatively fixed value for a given design, labeled C), multiplied by the voltage across the device squared (labeled V), and multiplied by the frequency at which the device is switching (plus a leakage term which may be disregarded here). This relationship is thus:

$$P = C \times V^2 \times F \quad (2)$$

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Using the previous example, if the capacitance on a component is switching once per cycle, then the capacitance is switching at a rate of 2 GHz, (or once every 500 picoseconds). Equation 2 show that a reduction in voltage would result in a square law reduction in power. For example, when voltage (V) drops 10%, becomes 0.9×V, the square law reduction causes the power (P) to be 0.9×0.9×P, or 0.81×P (a 19% reduction).

As equation 1 indicates, frequency is directly proportional to voltage. Thus when combined with equation 2, a reduction in frequency will lead to an additional voltage factor in power reduction. This results in power being reduced by approximately V³. Using the previous example, a 10% drop in V would result in a 0.9×0.9×0.9×P (0.72×P or 28%) reduction in power for a 10% reduction in voltage. This relationship is well known, and has been exploited for power management particularly in mobile devices such as laptops.

Many power-management solutions use software to minimize the excess computing power of microprocessors and other like devices. Based upon an expected load, the software determines how fast the processor must operate; for example, the software may note that a densely coded application may require more speed than a simple one. Once the software determines the speed required by the demand, it can reduce the speed to only that which is required. The result is a reduction in the power consumption for the device over time.

However, these methods lead to inefficiencies in voltage management. For example, these methods require that a software program predict the computing demands an integrated circuit may see and then change the voltage and frequency accordingly. This results in lag times associated with prediction inaccuracies. Further, the intention of these systems is to minimize the total energy consumed over time for the processor. Portable units, such as laptops, can then maximize the battery life with these algorithms. For a server type processor, minimizing total energy usage over a period of time is not the goal. Maximum computing power is the goal. Within a given power envelope, a server system should maximize the performance that is available on demand for a customer. Ideally, the full performance capability should be available at any time to a customer. Even in server systems, however, there are significant motivations for keeping the power down. For example, as a chip burns power it generates heat that is difficult to draw away from a small silicon die. Further, it is more expensive to run a large number of processors at higher power, and it is difficult to provide that power in tight spaces. Thus, for a server, a system that only tries to minimize power when the compute needs are high does not suffice; the compute needs are always high. Likewise, a system that simply provides maximum computing power is insufficient for most systems. Thus, there exists a need for a method that actively optimizes the power consumed while maintaining the system's ability to deliver the highest performance without having to rely on software predictions that are often inaccurate.

An additional shortcoming of currently available solutions is the time lag between the recognition that an opportunity to reduce power (or the recognition of the need to increase power due to high compute needs) and the operation that effects that change. After recognition, a command to vary voltage must be sent out to a voltage regulator which generates the voltage used by the processor. It then takes a number of microseconds (10s to 100s of microseconds, typically) for the voltage regulator to perform that task. It is not until that voltage transition is completed that the frequency can actually be raised on the processor itself,

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because a processor running at a frequency higher than the voltage supports can result in a timing failure. Thus, there is a time lag waiting for the voltage to slew before the frequency can be raised. Similarly, in order to lower the voltage (to reduce the power consumption) the frequency must be lowered first to avoid a timing failure caused by a voltage too low for a given frequency. A system that understood exactly how fast the integrated circuit could operate for a given voltage, combined with a system that could operate the chip at a frequency matched to that voltage, would result in a significant efficiency gains. Instead of anticipating a voltage reduction and lowering frequency in advance, such a system could lower voltage and frequency together. Such a system could also avoid the guardbanding necessary when a designer is required to anticipate the varying operating conditions of a device. If, using the above example, the voltage varies by + or -10%, a designer must ensure that the device will work at its quoted frequency if only 90% of the expected voltage is provided. Thus, there exists a need for a system that could set the frequency to an observed voltage and constantly vary the frequency to match the voltage actually delivered.

In order to further improve efficiencies, many power-management systems shut off parts of an integrated circuit that are not in use. For example, the floating point computation unit in a microprocessor is a high performance unit that is needed for technical code. For many applications (word processing, transaction processing, and other general integer applications) the floating point computation is unnecessary. A typical power-savings method might shut the clock down to the floating point unit so that it is not using power. But as units on an integrated circuit are powered up and down, the processor can experience large, sudden changes in power consumption. This poses a challenge to the power delivery system, because there is always some resistance and some inductance between the components and the power supply. Further, a sudden spike in power to dormant areas can result in a voltage drop to already powered sections that can cause operational and timing problems. Thus, there exists a need for a system that can adapt very rapidly to changes in voltage induced by sudden changes in power consumption.

SUMMARY

One disclosed embodiment of the invention is directed to circuit control that comprises sensing a delivered voltage to a portion of an integrated circuit, determining an appropriate frequency for the portion of the integrated circuit, and providing the appropriate frequency to the integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which

FIG. 1 is a flow chart of an embodiment of the present invention;

FIG. 2 is a circuit layout according to an embodiment of the present invention;

FIG. 3 is a graph illustrating some advantages of certain embodiments of the present invention;

FIG. 4 is a flow chart of an embodiment of the present invention;

FIG. 5 is a circuit layout according to an embodiment of the present invention;

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FIG. 6 is a flow chart of an embodiment of the present invention;

FIG. 7 is a chart of timing relationships; and

FIG. 8 is a circuit floor plan in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

Voltage sensors, such as those described in patent application Ser. No. 10/614,309, hereby incorporated by reference, can provide a means of detecting the voltage actually delivered to an integrated circuit. Often, the power consumption of different points on a integrated circuit will vary, resulting in a drop in voltage in one part of a integrated circuit that are not seen elsewhere. It may be advantageous to have a number of voltage sensors distributed across an entire die. Circuitry arranged to provide a determined frequency, such as a fast response frequency synthesizer as described in patent application Ser. No. 10/679,725, hereby incorporated by reference, can provide the ability to quickly adjust a clock frequency that drives a particular section of an integrated circuit. A frequency determining means is used to determine what frequency is appropriate for the integrated circuit (or a portion thereof) at the voltage delivered.

FIG. 1 depicts a flow chart 100 describing the basic stages of certain embodiments of the present invention. In stage 101, the voltage that is actually delivered to an integrated circuit is sensed. As described above, the voltage delivered by a power supply can vary over time. As the voltage varies, the frequency of the clock used to operate the integrated circuit may have to be changed in order to avoid timing failures. Stage 102 illustrates that the basic method determines an appropriate frequency to provide to the integrated circuit. Typically, this frequency is derived directly from the delivered voltage. Lastly, the basic method provides to the integrated circuit the frequency determined to by appropriate in stage 103.

FIG. 2 depicts an example component layout of one embodiment of the present invention. System 200 is capable of addressing all of the above described problems in the art for the management of integrated circuit 201. Power supply 202 supplies a voltage to system 200. As described above, this voltage is likely to vary. Voltage sensor 203 senses the voltage that is delivered to integrated circuit 201. In the depicted embodiment, voltage sensor 203 provides information regarding the delivered voltage to logic block 204. Logic block 204, in the depicted embodiment, determines the frequency that is appropriate for integrated circuit 201 and provides this information to frequency synthesizer 205. Frequency synthesizer 205 alters the system clock 206 signal to correspond with the determined appropriate frequency. Those of ordinary skill in the art will appreciate that system 200 is an example arrangement, and that the embodiments of the present invention are not limited to the arrangement depicted.

FIG. 3 illustrates some advantages of the above embodiments. Graphic relationship 300 show a comparison between the delivered voltage 301, the frequency 302 provided by an embodiment of the present invention, the average frequency 303 provided by an embodiment of the present invention, and the frequency 304 allowed by prior art methods.

As described above, the delivered voltage 301 will likely vary, as seen by voltage deviation 305. Prior art solutions required that the provided frequency 304 be low enough to still be viable even at the minimum voltage 306. Some embodiments of the present invention are able to continu-

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ously sense the delivered voltage **301** and provide a frequency **302** that tracks the delivered voltage **301**. Thus the average frequency **303**, provided by these embodiments of the present invention is significantly higher than the frequency **304** allowed by prior art solutions.

The embodiments of the present invention are not limited to one manner of voltage to frequency conversion. In one embodiment of the present invention, the voltage sensors measure the effect of the voltage on circuit speed. FIG. **4** is an example flow chart for an embodiment of this type. Method **400** illustrates, generally, how such an embodiment can use switching speed. The delivered voltage is sensed in stage **401**. In such an embodiment, the delivered voltage would then be applied **402** to test devices (such as transistors) that may be part of the voltage sensor. The voltage sensor then determines **403** if the test devices are able to cycle at the currently provided clock frequency. If not, the frequency synthesizer instructs **404** to slow the provided frequency in order to compensate. If the test devices can cycle at the currently provided frequency, the depicted method determines **405** if the test devices are capable of cycling at a rate faster than the provided frequency. If so, the frequency synthesizer is instructed **406** to raise the frequency accordingly. If not, the currently provided frequency is unchanged.

In one embodiment using this method, the voltage sensor contains a plurality of VLSI transistors that are implemented as gates. These transistors are specifically chosen to be of a length and propagation time delay that will represent the limits of the VLSI circuit on which the embodiment has been implemented. Thus, when the delay through the sensor transistors equals the cycle time of the instantaneous frequency on the integrated circuit, the integrated circuit is operating efficiently. If the voltage drops, the transistors in the voltage sensor will slow down (take longer to propagate than the cycle time). This indicates that the cycle time is too short and that frequency should be reduced in order to avoid a timing failure. Conversely, if the voltage rises, the propagation of the sensor transistors is faster than one clock cycle, and frequency can be safely increased.

FIG. **5** depicts an example voltage sensor that could be used with the above embodiments. Sensor **500** is connected to the power line supplying power from power source **501** to integrated circuit **502**. Test devices **503** comprise sensor **500**. These devices may be implemented as gates, simple transistors, or other components. Information regarding switching speed of these components is then transferred to a logic block.

Other embodiments of the present invention may use an analog to digital converter to actually measure the value of the delivered voltage. This measured number can then be used by indexing a table. FIG. **6** shows an example flow chart depicting a method that may be implemented by certain embodiments of the present invention. The delivered voltage is applied **601** to a voltage sensor. This voltage is converted **602** to a numeric value, by a analog-to-digital converter for example. Then the embodiment may access **603** a table or database that associates voltage values with appropriate frequencies, and transmit **604** the frequency associated with the delivered voltage to a frequency synthesizer. The synthesizer can then adjust **605** the clock frequency to match. For example, if the delivered voltage is measured as 1.4 volts, an embodiment could index a table that showed 1.4 volts could sustain 1.9 GHz. 1.9 GHz is then sent to the frequency synthesizer as the new frequency. During the next clock cycle, the process could repeat. If 1.42 volts is measured in the next cycle, the table could be

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indexed again, the appropriate frequency re-determined, and the new frequency (for example, 1.93 GHz) sent to the synthesizer.

Temperature effects can also cause devices to run faster or slower than the designer anticipated value. In a hot environment, devices tend to slow down. Embodiments such as those describe by FIG. **6** may require guardbanding to account for inaccuracies in a table or database brought about by temperature. However, embodiments such as those described by FIG. **4** can have transistors in the sensor to determine how fast an integrated circuit can run at a given voltage that experience the same physical conditions, such as temperature, the integrated circuit as a whole is experiencing. Because the detector transistors will slow as the temperature rises in the same manner as the devices in the integrated circuit, no additional correction is needed.

FIG. **7** is a timing diagram of the activities in the response loop. It shows a voltage drop **701** and how the regional voltage detectors slow down **702** in response to that drop **701**. It further shows where that slow down is detected **703**, how that information gets communicated back to the frequency synthesizer **704**, and how the frequency synthesizers change the frequency that is seen subsequently at the components of the integrated circuit **705**. Of course, the change in frequency is only useful when it is actually seen by the components on the integrated circuit that use the clock. With sudden changes in power consumption, steep voltage drops are seen. The faster the frequency changes in response to the voltage, the more efficient the system becomes. Ideally, frequency will remain very close to the maximum supported by the voltage. Some embodiments of the present invention incorporate voltage sensors that compare cycle time and synthesizers to supply the appropriate frequency. As a result, a system is provided where frequency follows along behind voltage, allowing the voltage to change freely based upon the power needs.

Many embodiments will find it advantageous to distribute multiple voltage sensors in several regions of an integrated circuit. Those of ordinary skill in the art will appreciate that the embodiments of the present invention are not limited to a single implementation of the arrangements depicted above. Some embodiments may have multiple voltage detectors, distributed as regional voltage detectors, as well as multiple frequency synthesizers. FIG. **8** shows where the regional voltage detectors are and where the frequency synthesizers are located in one embodiment. Regional voltage sensors **801** are distributed across VLSI (Very Large Scale Integration) integrated circuit **800**. These sensors **801** are able to sense the delivered voltage to a portion of VLS integrated circuit **800**, and by means of frequency synthesizers **802**, alter the frequency to different positions of the integrated circuit.

The frequency synthesizers **802** in some embodiments of the present invention can have the ability to "talk" to each other. If one frequency synthesizer **802** senses a voltage drop, i.e. the regional voltage detectors indicate a need to slow down, the frequency synthesizer associated with those detectors slow down immediately. This regional slow down can then be communicated to the other frequency synthesizer allowing them to follow. Remote ones, however, may slow down one or more cycles later. But because it takes a non-zero amount of time for voltage disturbances to propagate across the integrated circuit, the delay in slow down is inconsequential from an operational perspective. Thus, the clock frequency on a integrated circuit may not be universal, as it would be in a preemptive system, the frequency may have a time and location variance. Aspects of some embodi-

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ments may account for this. If one region of the integrated circuit sees a change in frequency that another region has not yet experienced, phase error may occur between the two. However, such errors are well known in the art of VLSI design, and one of ordinary skill in the art could easily adapt a specific VLSI design to compensate for such skew without undue experimentation.

Certain embodiments of the present invention utilize the concept of average frequency. As voltage is varying, these embodiments of the present invention push the frequency very close to maximum for the voltage. As a result, the frequency varies with respect to location and with respect to time. Thus, the performance of the integrated circuit (usually well correlated with operating frequency) is sustained at an average frequency substantially higher than the minimum frequency that is the maximum at which a prior art integrated circuit can safely operate. The difference between these two values and the benefit gained is illustrated in FIG. 3.

What is claimed is:

1. A method of circuit control, comprising:
sensing a delivered voltage to a portion of an integrated circuit;
determining an appropriate frequency for the portion of the integrated circuit; and
providing the appropriate frequency to said portion of said integrated circuit.
2. The method of claim 1 wherein said sensing, determining, and providing are continuously repeated during the integrated circuit's operation.
3. The method of claim 1 wherein the appropriate frequency is a maximum frequency possible for the portion of the integrated circuit at the delivered voltage.
4. The method of claim 1 further comprising:
applying the delivered voltage to constituent devices of a voltage sensor.
5. The method of claim 4 wherein the constituent devices are similar to devices comprising the portion of the integrated circuit.
6. The method of claim 4 further comprising:
further determining a switching speed of the constituent devices at the delivered voltage.
7. The method of claim 6 further comprising:
using the switching speed to determine the appropriate frequency.
8. The method of claim 4 further comprising:
exposing the voltage sensor and the portion of the integrated circuit to the same physical conditions.
9. The method of claim 8 wherein the physical conditions include temperature.
10. The method of claim 1 further comprising:
calculating a value for the delivered voltage.
11. The method of claim 10 further comprising:
using a tabulation of a set of values for the appropriate frequency associated with a set of values for the delivered voltage to determine the appropriate frequency.
12. A device for electronic circuit control comprising:
means for sensing a delivered voltage to one portion of an integrated circuit;
means for determining an appropriate frequency for the portion of the integrated circuit; and
means of providing the appropriate frequency to the portion of the integrated circuits, independent of frequencies provided to other portions of said integrated circuit.

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13. The device of claim 12 further comprising:
means for determining the maximum possible frequency for the portion of the integrated circuit at the delivered voltage.

14. The device of claim 12 wherein said sensing means further comprises:

means for testing a switching speed of at least one test device at the delivered voltage.

15. The device of claim 14 wherein the at least one test device is similar to a circuit device comprising the portion of the integrated circuit.

16. The device of claim 14 further comprising:
means for using the switching speed as the appropriate frequency.

17. The device of claim 14 wherein the at least one test device and the circuit device are exposed to similar physical conditions.

18. The device of claim 17 wherein the physical conditions include temperature.

19. The device of claim 12 further comprising:
means for calculating a value for the delivered voltage.

20. The device of claim 19 wherein said calculating means includes analog-to-digital converter.

21. The device of claim 19 further comprising:
means for associating the value of the delivered voltage with a value for the appropriate frequency.

22. The device of claim 21 wherein said associating means includes a tabulation of possible values for the delivered voltage associated with a set of values for the appropriate frequency.

23. A system for circuit control comprising:
at least one voltage sensor to sense a delivered voltage to a portion of an integrated circuit;
at least one logic block to determine an appropriate frequency from the delivered voltage for the portion of the integrated circuit; and
at least one circuitry arrangement to provide the appropriate frequency to the portion of the integrated circuit.

24. The system of claim 23 wherein the logic block determines as the appropriate frequency, the maximum frequency possible for the portion of the integrated circuit at the delivered voltage.

25. The system of claim 23 further comprising: at least one test device to which the delivered voltage is applied.

26. The system of claim 25 at least one test device logic block to determine a switching speed of the at least one test device at the applied voltage.

27. The system of claim 26 wherein the switching speed is used to determine the appropriate voltage.

28. The system of claim 25 wherein the at least one test device is similar to a device that comprises the portion of the integrated circuit.

29. The system of claim 25 wherein the at least one test device and the portion of the integrated circuit are exposed to similar physical conditions.

30. The system of claim 29 wherein the physical conditions include temperature.

31. The system of claim 23 further comprising:
a converter to convert the delivered voltage to a value.

32. The system of claim 31 wherein the converter is an analog-to-digital converter.

33. The system of claim 23 further comprising:
a table of possible values for the delivered voltage associated with possible values for the appropriate frequency.

34. The system of claim 33 wherein said table is a computer readable database.

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35. A system for circuit control comprising:
a plurality of voltage sensors arranged to sense a delivered
voltage to different
portions of an integrated circuit;
a plurality of logic blocks arranged to determine an appropriate frequency for each

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said portion from said delivered voltages; and
a plurality of circuitry arrangements to provide each said
portion its associated
appropriate frequency.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,224,563 B2
APPLICATION NO. : 10/651360
DATED : May 29, 2007
INVENTOR(S) : Samuel D. Naffziger

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 2, line 44, delete “bums” and insert -- burns --, therefor.

In column 7, line 65, in Claim 12, delete “circuits” and insert -- circuit --, therefor.

Signed and Sealed this

Twelfth Day of August, 2008

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a cursive "Dudas".

JON W. DUDAS
Director of the United States Patent and Trademark Office

Thursday, March 16, 2017



Mr. David Su
Vice President and General Counsel
MediaTek Inc.
No. 1, Dusing 1st Rd., Hsinchu Science Park,
Hsinchu, 30078
Taiwan

Dear Mr. Su,

I am writing to you with respect to the Microcomponent Patent Licensing Program of Conversant Intellectual Property Management Inc. ("CIPM"). As you may be aware, the license agreement between MOSAID Technologies Inc. (now Conversant Intellectual Property Management) and MediaTek Inc. expired on March 7, 2016. Please find attached a copy of the agreement. We'd like to begin discussions on renewing the agreement. Conversant's Microcomponent patent portfolio has grown over the years, both in size and importance.

Specifically, the following *exemplary* MediaTek product infringes at least Claim 42 of US Patent No. 7,111,179, Claims 16, 18, 20, 22 and 27 of US Patent No. 7,051,306, Claims 30, 31 and 38 of US Patent No. 7,996,811 and Claims 39 and 40 of US Patent No. 7,945,885, as well as their respective foreign counterparts:

- MediaTek MT6755 Multi-core processor.

Enclosed are exemplary claim charts corresponding to our assertion of patent infringement, as enumerated above.

We are willing to meet with MediaTek to discuss these issues and look forward to your prompt reply so we can arrange a meeting with you or your representatives, either in person or by telephone, as soon as possible.

For expediency's sake, please feel free to contact me by e-mail at misiag@conversantip.com.

Thank you in advance for your attention to this matter.

Best regards,

A handwritten signature in black ink, appearing to read "Richard Misiag". The signature is fluid and cursive, with a long horizontal stroke at the end.

Richard Misiag
Vice President, Licensing
Conversant Intellectual Property Management
T: 214-494-4841
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