

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent of:       Hoberman et al.  
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Title:                   POWER MANAGERS FOR AN INTEGRATED CIRCUIT

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT  
NO. 7,945,885 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

## TABLE OF CONTENTS

|      |                                                                |    |
|------|----------------------------------------------------------------|----|
| I.   | REQUIREMENTS FOR IPR .....                                     | 1  |
|      | A. Grounds for Standing .....                                  | 1  |
|      | B. Challenge and Relief Requested.....                         | 1  |
| II.  | THE '885 PATENT .....                                          | 2  |
|      | A. Brief Description .....                                     | 2  |
|      | B. Summary of the Prosecution History .....                    | 4  |
|      | C. Level of Ordinary Skill in the Art .....                    | 4  |
|      | D. Claim Construction.....                                     | 5  |
| III. | THE CHALLENGED CLAIMS ARE UNPATENTABLE.....                    | 6  |
|      | A. GROUND 1—Claims 1-64 are obvious over Nowka and Borkar..... | 6  |
|      | 1. Overview of Nowka .....                                     | 6  |
|      | 2. Overview of Borkar.....                                     | 10 |
|      | 3. The Nowka-Borkar Combination.....                           | 13 |
|      | 4. Claim 1 .....                                               | 18 |
|      | 5. Claim 2 .....                                               | 40 |
|      | 6. Claim 3 .....                                               | 42 |
|      | 7. Claim 4 .....                                               | 44 |
|      | 8. Claim 5 .....                                               | 45 |
|      | 9. Claim 6 .....                                               | 46 |
|      | 10.Claim 7 .....                                               | 46 |
|      | 11.Claim 8 .....                                               | 47 |
|      | 12.Claim 9 .....                                               | 48 |
|      | 13.Claim 10 .....                                              | 48 |
|      | 14.Claim 11 .....                                              | 48 |
|      | 15.Claim 12 .....                                              | 48 |
|      | 16.Claim 13 .....                                              | 50 |
|      | 17.Claim 14 .....                                              | 50 |
|      | 18.Claim 15 .....                                              | 50 |

|                   |    |
|-------------------|----|
| 19.Claim 16 ..... | 50 |
| 20.Claim 17 ..... | 51 |
| 21.Claim 18 ..... | 51 |
| 22.Claim 19 ..... | 51 |
| 23.Claim 20 ..... | 51 |
| 24.Claim 21 ..... | 51 |
| 25.Claim 22 ..... | 51 |
| 26.Claim 23 ..... | 51 |
| 27.Claim 24 ..... | 52 |
| 28.Claim 25 ..... | 52 |
| 29.Claim 26 ..... | 52 |
| 30.Claim 27 ..... | 52 |
| 31.Claim 28 ..... | 52 |
| 32.Claim 29 ..... | 52 |
| 33.Claim 30 ..... | 52 |
| 34.Claim 31 ..... | 52 |
| 35.Claim 32 ..... | 54 |
| 36.Claim 33 ..... | 54 |
| 37.Claim 34 ..... | 54 |
| 38.Claim 35 ..... | 54 |
| 39.Claim 36 ..... | 54 |
| 40.Claim 37 ..... | 54 |
| 41.Claim 38 ..... | 56 |
| 42.Claim 39 ..... | 56 |
| 43.Claim 40 ..... | 57 |
| 44.Claim 41 ..... | 57 |
| 45.Claim 42 ..... | 57 |
| 46.Claim 43 ..... | 57 |
| 47.Claim 44 ..... | 57 |
| 48.Claim 45 ..... | 57 |

|                                                                |    |
|----------------------------------------------------------------|----|
| 49.Claim 46 .....                                              | 57 |
| 50.Claim 47 .....                                              | 57 |
| 51.Claim 48 .....                                              | 57 |
| 52.Claim 49 .....                                              | 58 |
| 53.Claim 50 .....                                              | 58 |
| 54.Claim 51 .....                                              | 58 |
| 55.Claim 52 .....                                              | 58 |
| 56.Claim 53 .....                                              | 58 |
| 57.Claim 54 .....                                              | 58 |
| 58.Claim 55 .....                                              | 58 |
| 59.Claim 56 .....                                              | 59 |
| 60.Claim 57 .....                                              | 59 |
| 61.Claim 58 .....                                              | 59 |
| 62.Claim 59 .....                                              | 59 |
| 63.Claim 60 .....                                              | 59 |
| 64.Claim 61 .....                                              | 59 |
| 65.Claim 62 .....                                              | 59 |
| 66.Claim 63 .....                                              | 60 |
| 67.Claim 64 .....                                              | 60 |
| B. GROUND 2—Claims 1-64 are obvious over Nicol and Borkar..... | 60 |
| 1. Overview of Nicol.....                                      | 60 |
| 2. Overview of Borkar.....                                     | 61 |
| 3. Nicol-Borkar Combination.....                               | 61 |
| 4. Claim 1 .....                                               | 64 |
| 5. Claim 2 .....                                               | 80 |
| 6. Claim 3 .....                                               | 81 |
| 7. Claim 4 .....                                               | 82 |
| 8. Claim 5 .....                                               | 85 |
| 9. Claim 6 .....                                               | 85 |
| 10.Claim 7 .....                                               | 85 |

|                   |    |
|-------------------|----|
| 11.Claim 8 .....  | 86 |
| 12.Claim 9 .....  | 86 |
| 13.Claim 10 ..... | 87 |
| 14.Claim 11 ..... | 87 |
| 15.Claim 12 ..... | 87 |
| 16.Claim 13 ..... | 88 |
| 17.Claim 14 ..... | 88 |
| 18.Claim 15 ..... | 88 |
| 19.Claim 16 ..... | 88 |
| 20.Claim 17 ..... | 89 |
| 21.Claim 18 ..... | 89 |
| 22.Claim 19 ..... | 89 |
| 23.Claim 20 ..... | 89 |
| 24.Claim 21 ..... | 89 |
| 25.Claim 22 ..... | 89 |
| 26.Claim 23 ..... | 89 |
| 27.Claim 24 ..... | 90 |
| 28.Claim 25 ..... | 90 |
| 29.Claim 26 ..... | 90 |
| 30.Claim 27 ..... | 90 |
| 31.Claim 28 ..... | 90 |
| 32.Claim 29 ..... | 90 |
| 33.Claim 30 ..... | 90 |
| 34.Claim 31 ..... | 90 |
| 35.Claim 32 ..... | 91 |
| 36.Claim 33 ..... | 91 |
| 37.Claim 34 ..... | 91 |
| 38.Claim 35 ..... | 91 |
| 39.Claim 36 ..... | 91 |
| 40.Claim 37 ..... | 92 |

|                                                                                                                      |    |
|----------------------------------------------------------------------------------------------------------------------|----|
| 41.Claim 38 .....                                                                                                    | 94 |
| 42.Claim 39 .....                                                                                                    | 94 |
| 43.Claim 40 .....                                                                                                    | 95 |
| 44.Claim 41 .....                                                                                                    | 95 |
| 45.Claim 42 .....                                                                                                    | 95 |
| 46.Claim 43 .....                                                                                                    | 95 |
| 47.Claim 44 .....                                                                                                    | 95 |
| 48.Claim 45 .....                                                                                                    | 95 |
| 49.Claim 46 .....                                                                                                    | 95 |
| 50.Claim 47 .....                                                                                                    | 95 |
| 51.Claim 48 .....                                                                                                    | 95 |
| 52.Claim 49 .....                                                                                                    | 96 |
| 53.Claim 50 .....                                                                                                    | 96 |
| 54.Claim 51 .....                                                                                                    | 96 |
| 55.Claim 52 .....                                                                                                    | 96 |
| 56.Claim 53 .....                                                                                                    | 96 |
| 57.Claim 54 .....                                                                                                    | 96 |
| 58.Claim 55 .....                                                                                                    | 96 |
| 59.Claim 56 .....                                                                                                    | 97 |
| 60.Claim 57 .....                                                                                                    | 97 |
| 61.Claim 58 .....                                                                                                    | 97 |
| 62.Claim 59 .....                                                                                                    | 97 |
| 63.Claim 60 .....                                                                                                    | 97 |
| 64.Claim 61 .....                                                                                                    | 97 |
| 65.Claim 62 .....                                                                                                    | 97 |
| 66.Claim 63 .....                                                                                                    | 98 |
| 67.Claim 64 .....                                                                                                    | 98 |
| IV. THE BOARD SHOULD CONSIDER THE PETITION ON THE MERITS<br>AND NOT EXERCISE ITS DISCRETION TO DENY INSTITUTION .... | 98 |
| A. Discretionary denial under §325(d) is not warranted.....                                                          | 98 |
| B. Discretionary Denial under Section 314(a) Is Not Warranted.....                                                   | 99 |

|                                                                                              |     |
|----------------------------------------------------------------------------------------------|-----|
| C. The <i>Fintiv</i> Factors Weigh Against Exercising Discretion To Deny<br>Institution..... | 99  |
| V. CONCLUSION.....                                                                           | 100 |
| VI. PAYMENT OF FEES .....                                                                    | 100 |
| VII. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1).....                                      | 101 |
| A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1) .....                                 | 101 |
| B. Related Matters Under 37 C.F.R. § 42.8(b)(2).....                                         | 101 |
| C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3) .....                               | 102 |
| D. Service Information .....                                                                 | 102 |

## LIST OF EXHIBITS

- MTK-1001 U.S. Patent No. 7,945,885 to Hoberman et al. (“the ’885 patent”)
- MTK-1002 Excerpts from the Prosecution History of the ’885 patent
- MTK-1003 Declaration of Tajana Rosing, Ph.D.
- MTK-1004 “A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling” by Nowka, et al. (“Nowka”)
- MTK-1005 June Munford Declaration
- MTK-1006 U.S. Patent No. 6,484,265 to Borkar et al. (“Borkar”)
- MTK-1007 Advanced Configuration and Power Interface Specification 2.0
- MTK-1008 U.S. Patent No. 6,141,762 to Nicol, et al. (“Nicol”)
- MTK-1009 Complaint for Patent Infringement Against MediaTek, Inc. in *Mosaid Technologies Inc. v. MediaTek Inc., MediaTek USA, Inc.*, Case No. 2:23-cv-00129 (E.D. Tex. March 2023)
- MTK-1010 Affidavit of Service On MediaTek USA, Inc. in *Mosaid Technologies Inc. v. MediaTek Inc., MediaTek USA, Inc.*, Case No. 2:23-cv-00129 (March 30, 2023)
- MTK-1011 Claim Construction Order in *Mosaid Technologies Inc. v. Freescale Semiconductor, Inc.*, Case No. 6:11-cv-00173 (E.D. Tex. April 29, 2013)
- MTK-1012 Claim Construction Order in *Conversant Intellectual Property Management Inc., et al. v. Xilinx, Inc.*, Case No. 6:12-cv-00847 (E.D. Tex. January 9, 2015)
- MTK-1013 Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, Katherine K. Vidal (USPTO June 21, 2022)

MTK-1014 Stipulation

MTK-1015 U.S. Patent No. 8,086,884 to Naffziger et al. (“Naffziger”)

MTK-1016 “Variable Supply-Voltage Scheme for Low-Power High-Speed CMOS Digital Design” by Kuroda et al. (“Kuroda”)

MTK-1017 “Dynamic Power Management: Design Techniques and CAD Tools” by Benini & De Micheli (“Dynamic Power Management”)

MTK-1018 “A Survey of Design Techniques for System-Level Dynamic Power Management” by Benini, et al. (“Benini Survey”)

MTK-1019 “Managing Power and Performance for System-on-Chip Designs using Voltage Islands” by Lackey, et al. (“Lackey”)

MTK-1020 “Policy Optimization for Dynamic Power Management” by Benini et al., (“Benini Policy Optimization”)

MTK-1021 “Energy-Efficient Processor Design Using Multiple Clock Domains with Dynamic Voltage and Frequency Scaling” by Semeraro et al. (“Semeraro”)

## LISTING OF CHALLENGED CLAIMS

| Claim 1 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1[p]    | An integrated circuit comprising:                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 1[a]    | an integrated circuit chip;                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 1[b]    | a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;                                                                                                                                                                                                                                                                   |
| 1[c]    | one or more power consumption signals indicating one or more of the power consumptions;                                                                                                                                                                                                                                                                                                                                                                                                            |
| 1[d]    | a power management processor disposed on the integrated circuit chip and coupled to each of the power islands configured to monitor the one or more power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request. |
| Claim 2 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 2       | The integrated circuit as claimed in claim 1 wherein the power management software is embedded firmware in the integrated circuit.                                                                                                                                                                                                                                                                                                                                                                 |
| Claim 3 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 3       | The integrated circuit as claimed in claim 2 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.                                                                                                                                                                                                                                                   |
| Claim 4 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 4       | The integrated circuit as claimed in claim 2 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.                                                                                                                                                                                                                                                                                                                 |
| Claim 5 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 5       | The integrated circuit as claimed in claim 1 wherein each of the power consumptions is further controlled by stopping a clock.                                                                                                                                                                                                                                                                                                                                                                     |

| Claim 6  |                                                                                                                                                                                                                                                                                                                                                                                                                         |
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| 6        | The integrated circuit as claimed in claim 5 wherein stopping the clock comprises clock gating.                                                                                                                                                                                                                                                                                                                         |
| Claim 7  |                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 7        | The integrated circuit as claimed in claim 1 wherein the one or more power consumption signals include temperature or power dissipation measurement.                                                                                                                                                                                                                                                                    |
| Claim 8  |                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 8[p]     | An integrated circuit comprising:                                                                                                                                                                                                                                                                                                                                                                                       |
| 8[a]     | an integrated circuit chip;                                                                                                                                                                                                                                                                                                                                                                                             |
| 8[b]     | a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;                                                                                                                                                                                        |
| 8[c]     | one or more power consumption signals indicating one or more of the power consumptions;                                                                                                                                                                                                                                                                                                                                 |
| 8[d]     | a power manager disposed on the integrated circuit chip and coupled to each of the power islands configured to monitor the one or more power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request. |
| Claim 9  |                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 9        | The integrated circuit as claimed in claim 8 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.                                                                                                                                                                                                                    |
| Claim 10 |                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 10       | The integrated circuit as claimed in claim 9 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.                                                                                                                                                                        |

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| <b>Claim 11</b> |                                                                                                                                                                                                                                                                                                                                                                                        |
| 11              | The integrated circuit as claimed in claim 9 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.                                                                                                                                                                                                     |
| <b>Claim 12</b> |                                                                                                                                                                                                                                                                                                                                                                                        |
| 12              | The integrated circuit as claimed in claim 8 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.                                                                                                                                                                                                           |
| <b>Claim 13</b> |                                                                                                                                                                                                                                                                                                                                                                                        |
| 13              | The integrated circuit as claimed in claim 8 wherein each of the power consumptions is further controlled by stopping a clock.                                                                                                                                                                                                                                                         |
| <b>Claim 14</b> |                                                                                                                                                                                                                                                                                                                                                                                        |
| 14              | The integrated circuit as claimed in claim 13 wherein stopping the clock comprises clock gating.                                                                                                                                                                                                                                                                                       |
| <b>Claim 15</b> |                                                                                                                                                                                                                                                                                                                                                                                        |
| 15              | The integrated circuit as claimed in claim 8 wherein the one or more power consumption signals include temperature or power dissipation measurement.                                                                                                                                                                                                                                   |
| <b>Claim 16</b> |                                                                                                                                                                                                                                                                                                                                                                                        |
| 16[p]           | An integrated circuit comprising:                                                                                                                                                                                                                                                                                                                                                      |
| 16[a]           | an integrated circuit chip;                                                                                                                                                                                                                                                                                                                                                            |
| 16[b]           | a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;                                    |
| 16[c]           | a power management processor disposed on the integrated circuit chip and coupled to each of the power islands and configured to monitor the power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power |

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|                 | consumption in at least one of the power islands in response to a power consumption change request.                                                                                                                                                                |
| <b>Claim 17</b> |                                                                                                                                                                                                                                                                    |
| 17              | The integrated circuit as claimed in claim 16 wherein the power management software is embedded firmware in the integrated circuit.                                                                                                                                |
| <b>Claim 18</b> |                                                                                                                                                                                                                                                                    |
| 18              | The integrated circuit as claimed in claim 17 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.                  |
| <b>Claim 19</b> |                                                                                                                                                                                                                                                                    |
| 19              | The integrated circuit as claimed in claim 17 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.                                                                                |
| <b>Claim 20</b> |                                                                                                                                                                                                                                                                    |
| 20              | The integrated circuit as claimed in claim 16 wherein each of the power consumptions is further controlled by stopping a clock.                                                                                                                                    |
| <b>Claim 21</b> |                                                                                                                                                                                                                                                                    |
| 21              | The integrated circuit as claimed in claim 20 wherein stopping the clock comprises clock gating.                                                                                                                                                                   |
| <b>Claim 22</b> |                                                                                                                                                                                                                                                                    |
| 22              | The integrated circuit as claimed in claim 16 wherein each of the power consumption signals includes temperature or power dissipation measurement.                                                                                                                 |
| <b>Claim 23</b> |                                                                                                                                                                                                                                                                    |
| 23[p]           | The system of claim 22 wherein the first voltage comprises a source voltage.                                                                                                                                                                                       |
| 23[a]           | a integrated circuit chip;                                                                                                                                                                                                                                         |
| 23[b]           | a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power consumptions, each of the power consumptions being |

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|                 | independently controllable by changing a supply voltage and operating frequency;                                                                                                                                                                                                                                                                                                                            |
| 23[c]           | a power manager disposed on the integrated circuit chip coupled to each of the power islands and configured to monitor the power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request. |
| <b>Claim 24</b> |                                                                                                                                                                                                                                                                                                                                                                                                             |
| 24              | The integrated circuit as claimed in claim 23 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.                                                                                                                                                                                                       |
| <b>Claim 25</b> |                                                                                                                                                                                                                                                                                                                                                                                                             |
| 25              | The integrated circuit as claimed in claim 24 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.                                                                                                                                                           |
| <b>Claim 26</b> |                                                                                                                                                                                                                                                                                                                                                                                                             |
| 26              | The integrated circuit as claimed in claim 24 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.                                                                                                                                                                                                                         |
| <b>Claim 27</b> |                                                                                                                                                                                                                                                                                                                                                                                                             |
| 27              | The integrated circuit as claimed in claim 23 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.                                                                                                                                                                                                                               |
| <b>Claim 28</b> |                                                                                                                                                                                                                                                                                                                                                                                                             |
| 28              | The integrated circuit as claimed in claim 23 wherein each of the power consumptions is further controlled by stopping a clock.                                                                                                                                                                                                                                                                             |
| <b>Claim 29</b> |                                                                                                                                                                                                                                                                                                                                                                                                             |
| 29              | The integrated circuit as claimed in claim 28 wherein stopping the clock comprises clock gating.                                                                                                                                                                                                                                                                                                            |

| Claim 30 |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 30       | The integrated circuit as claimed in claim 23 wherein each of the power consumption signals includes temperature or power dissipation measurement.                                                                                                                                                                                                                                                                                                     |
| Claim 31 |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 31[p]    | The system of claim 16 further comprising a bus coupled to the power manager and the power islands.                                                                                                                                                                                                                                                                                                                                                    |
| 31[a]    | an integrated circuit;                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 31[b]    | a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;                                                                                                                                                                                                                                     |
| 31[c]    | one or more power consumption signals indicating one or more of the power consumptions;                                                                                                                                                                                                                                                                                                                                                                |
| 31[d]    | a power management processor coupled to each of the power islands configured to monitor the one or more power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request. |
| Claim 32 |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 32       | The system as claimed in claim 31 wherein the power management software is embedded firmware.                                                                                                                                                                                                                                                                                                                                                          |
| Claim 33 |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 33       | The system as claimed in claim 32 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.                                                                                                                                                                                                                  |
| Claim 34 |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 34       | The system circuit as claimed in claim 32 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.                                                                                                                                                                                                                                                                        |

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| <b>Claim 35</b> |                                                                                                                                                                                                                                                                                                                                                                             |
| 35              | The system as claimed in claim 31 wherein each of the power consumptions is further controlled by stopping a clock.                                                                                                                                                                                                                                                         |
| <b>Claim 36</b> |                                                                                                                                                                                                                                                                                                                                                                             |
| 36              | The system as claimed in claim 35 wherein stopping the clock comprises clock gating.                                                                                                                                                                                                                                                                                        |
| <b>Claim 37</b> |                                                                                                                                                                                                                                                                                                                                                                             |
| 37              | The system as claimed in claim 31 wherein the system is configured to have the supply voltage provided by an external regulator.                                                                                                                                                                                                                                            |
| <b>Claim 38</b> |                                                                                                                                                                                                                                                                                                                                                                             |
| 38              | The system as claimed in claim 31 wherein the one or more power consumption signals include temperature or power dissipation measurement.                                                                                                                                                                                                                                   |
| <b>Claim 39</b> |                                                                                                                                                                                                                                                                                                                                                                             |
| 39[p]           | The software product of claim 37 wherein the power islands are delineated based on functional circuitry of the integrated circuit.                                                                                                                                                                                                                                          |
| 39[a]           | an integrated circuit;                                                                                                                                                                                                                                                                                                                                                      |
| 39[b]           | a plurality of power islands of the integrated circuit having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;                                                                                                                                                          |
| 39[c]           | one or more power consumption signals indicating one or more of the power consumptions;                                                                                                                                                                                                                                                                                     |
| 39[d]           | a power manager coupled to each of the power islands configured to monitor the one or more power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request. |
| <b>Claim 40</b> |                                                                                                                                                                                                                                                                                                                                                                             |
| 40              | The system as claimed in claim 39 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.                                                                                                                                                                                   |

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| <b>Claim 41</b> |                                                                                                                                                                                                                                       |
| 41              | The system as claimed in claim 40 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors. |
| <b>Claim 42</b> |                                                                                                                                                                                                                                       |
| 42              | The system as claimed in claim 40 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.                                                               |
| <b>Claim 43</b> |                                                                                                                                                                                                                                       |
| 43              | The system as claimed in claim 39 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.                                                                     |
| <b>Claim 44</b> |                                                                                                                                                                                                                                       |
| 44              | The system as claimed in claim 39 wherein each of the power consumptions is further controlled by stopping a clock.                                                                                                                   |
| <b>Claim 45</b> |                                                                                                                                                                                                                                       |
| 45              | The system as claimed in claim 44 wherein stopping the clock comprises clock gating.                                                                                                                                                  |
| <b>Claim 46</b> |                                                                                                                                                                                                                                       |
| 46              | The system as claimed in claim 39 wherein the system is configured to have the supply voltage provided by an external regulator.                                                                                                      |
| <b>Claim 47</b> |                                                                                                                                                                                                                                       |
| 47              | The system as claimed in claim 39 wherein the one or more power consumption signals include temperature or power dissipation measurement.                                                                                             |
| <b>Claim 48</b> |                                                                                                                                                                                                                                       |
| 48[p]           | A system comprising:                                                                                                                                                                                                                  |
| 48[a]           | an integrated circuit;                                                                                                                                                                                                                |
| 48[b]           | a plurality of power islands of the integrated circuit having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power                                     |

|                 |                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                 | consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;                                                                                                                                                                                                                                                                                                        |
| 48[c]           | a power management processor coupled to each of the power islands configured to monitor the power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request. |
| <b>Claim 49</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 49              | The system as claimed in claim 48 wherein the power management software is embedded firmware.                                                                                                                                                                                                                                                                                                                                              |
| <b>Claim 50</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 50              | The system as claimed in claim 49 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.                                                                                                                                                                                                      |
| <b>Claim 51</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 51              | The system as claimed in claim 49 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.                                                                                                                                                                                                                                                                    |
| <b>Claim 52</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 52              | The system as claimed in claim 48 wherein each of the power consumptions is further controlled by stopping a clock.                                                                                                                                                                                                                                                                                                                        |
| <b>Claim 53</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 53              | The system as claimed in claim 52 wherein stopping the clock comprises clock gating.                                                                                                                                                                                                                                                                                                                                                       |
| <b>Claim 54</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 54              | The system as claimed in claim 48 wherein the system is configured to have the supply voltage provided by an external regulator.                                                                                                                                                                                                                                                                                                           |

| Claim 55 |                                                                                                                                                                                                                                                                                                                                                                 |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 55       | The system as claimed in claim 48 wherein each of the power consumption signals includes temperature or power dissipation measurement.                                                                                                                                                                                                                          |
| Claim 56 |                                                                                                                                                                                                                                                                                                                                                                 |
| 56[p]    | an integrated circuit;                                                                                                                                                                                                                                                                                                                                          |
| 56[a]    | a plurality of power islands of the integrated circuit having associated power consumptions, each of the power islands having a power consumption signal indicating a respective one of the power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency;                           |
| 56[b]    | a power manager coupled to each of the power islands configured to monitor the power consumption signals, the power manager being configured to individually control each of the power consumptions, and the power manager being configured to change power consumption in at least one of the power islands in response to a power consumption change request. |
| Claim 57 |                                                                                                                                                                                                                                                                                                                                                                 |
| 57       | The system as claimed in claim 56 wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions.                                                                                                                                                                       |
| Claim 58 |                                                                                                                                                                                                                                                                                                                                                                 |
| 58       | The system as claimed in claim 57 wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors.                                                                                                                           |
| Claim 59 |                                                                                                                                                                                                                                                                                                                                                                 |
| 59       | The system as claimed in claim 57 wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands.                                                                                                                                                                                         |
| Claim 60 |                                                                                                                                                                                                                                                                                                                                                                 |
| 60       | The system as claimed in claim 56 wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands.                                                                                                                                                                                               |

| Claim 61 |                                                                                                                                                    |
|----------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 61       | The system as claimed in claim 56 wherein each of the power consumptions is further controlled by stopping a clock.                                |
| Claim 62 |                                                                                                                                                    |
| 62       | The system as claimed in claim 61 wherein stopping the clock comprises clock gating.                                                               |
| Claim 63 |                                                                                                                                                    |
| 63       | The system as claimed in claim 56 wherein the system is configured to have the supply voltage provided by an external regulator.                   |
| Claim 64 |                                                                                                                                                    |
| 64       | The integrated circuit as claimed in claim 56 wherein each of the power consumption signals includes temperature or power dissipation measurement. |

MediaTek, Inc. (“Petitioner”) petitions for *Inter Partes* Review (“IPR”) of claims 1-64 (“Challenged Claims”) of U.S. Patent No. 7,945,885 (“the ’885 patent”).

## **I. REQUIREMENTS FOR IPR**

### **A. Grounds for Standing**

Petitioner certifies that the ’885 patent is available for IPR. Petitioner is not barred or estopped from requesting this review of the Challenged Claims. The present Petition is filed within one year of service of a complaint against Petitioner in *Mosaid Technologies Inc. v. MediaTek Inc., MediaTek USA, Inc.*, Case No. 2:23-cv-00129 (E.D. Tex. March 2023). MTK-1010.

### **B. Challenge and Relief Requested**

Petitioner requests IPR and cancellation of the Challenged Claims on the grounds below. Dr. Tajana Rosing provides complementary explanations in her Declaration (MTK-1003) cited throughout this petition.

| Ground | Claims | Basis | References       |
|--------|--------|-------|------------------|
| 1      | 1-64   | §103  | Nowka and Borkar |
| 2      | 1-64   | §103  | Nicol and Borkar |

Each reference pre-dates the ’885 patent’s earliest possible priority date (May 7, 2003; “Critical Date”) and qualifies as prior art.<sup>1</sup>

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<sup>1</sup> Petitioner does not concede that the ’885 patent is entitled to the Critical Date.

| Reference | Date                   | Prior Art Under |
|-----------|------------------------|-----------------|
| Nowka     | 11/2002 (published)    | §102(a)         |
| Nicol     | 10/31/2000 (published) | §102(b)         |
| Borkar    | 11/2002 (published)    | §102(e)         |

## II. THE '885 PATENT

### A. Brief Description

The '885 patent relates to managing power on an integrated circuit ("IC") using power islands. MTK-1001, Abstract, 1:23-25. The '885 patent explains that reducing power consumption in integrated circuits is a known design goal that is increasing in importance as ICs become more complex and power consuming. MTK-1001, 1:27-34, 2:9-18. One alleged problem in the existing art, according to the '885 patent, is "that power consumption is not efficiently utilized." MTK-1001, 1:66-67. "For example, the entire integrated circuit may operate at a maximum frequency just to support an application needing that maximum frequency, while other portions of the integrated circuit can operate at a lower frequency." MTK-1001, 1:67-2:4.

The '885 Patent explains that while "[s]ome prior integrated circuits have employed voltage islands or multiple clocks to lower power consumption," "the voltages in the power island and the frequencies of the multiple clocks are static;" "[t]he voltages and frequencies do not dynamically change based on the needs and operation of the integrated circuit." MTK-1001, 2:23-25.

The '885 patent proposes a method and apparatus for managing the power consumption of an integrated circuit (“IC”) using power islands whose power consumption is independently controlled. MTK-1001, Abstract, 2:29-32. A power island is “any section, delineation, partition, or division of the integrated circuit 110 where power consumption is controlled within the section, delineation, partition, or division.” MTK-1001, 3:56-59.

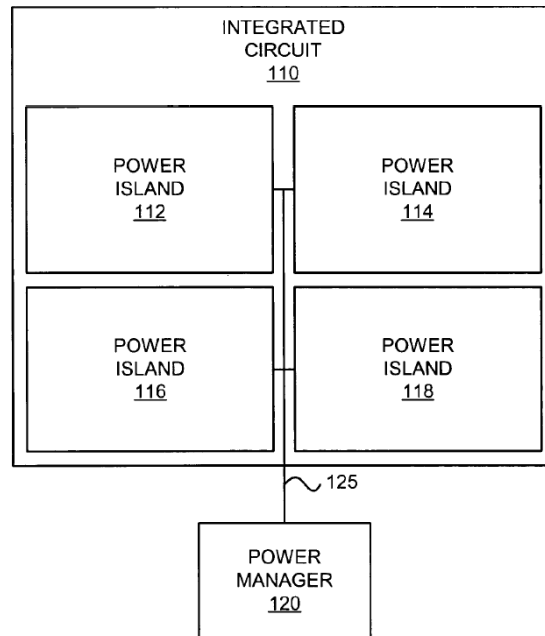


FIG. 1  
MTK-1001, Fig. 1.

The system has a “power manager” that determines a target power level for one of the power islands and then determines an action to change the power consumption for one of the islands to the target power level. MTK-1001, Abstract, 2:30-37. The action to change the power consumption can be selecting a clock

frequency or modifying a voltage for one of the power islands. MTK-1001, 4:51-58.

**B. Summary of the Prosecution History**

U.S. Application 12/176,645, which resulted in the '885 patent, was filed July 21, 2008. The '885 patent claims priority to provisional application 60/468,742, filed May 7, 2003. MTK-1001, 1. The Patent Office issued one non-final rejection during prosecution on nonstatutory double patenting grounds, in response to which the applicant filed terminal disclaimers on U.S. Patent Nos. 7,051,306 and 7,415,680. MTK-1002, 167, 189, 202. The Office never issued a rejection based on prior art grounds. While Nowka appears on the face of the '885 Patent, it was never the subject of a substantive rejection. Nowka, Nicol, and Borkar render the challenged claims obvious, as discussed below.

**C. Level of Ordinary Skill in the Art**

A person of ordinary skill in the art ("POSITA") would have had at least a bachelor of science degree in electrical engineering, computer engineering, computer science, or a related field, and at least two years of experience in the research, design, development, or testing of electronic circuits or components, or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa.

**D. Claim Construction**

Claim terms generally should be given their ordinary and customary meaning according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. § 42.100. For purposes of this proceeding only, Petitioner submits that no claim terms require a formal construction for purposes of addressing the Grounds in this Petition. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011). Petitioner notes for the Board that there have been prior litigations involving the '885 Patent, two of which had a claim construction order before voluntary dismissal, attached as MTK-1011 and MTK-1012. Petitioner submits that the Board does not need to address any of the prior constructions to resolve the patentability disputes before the PTAB, and that none of the constructions impact the invalidity analysis in this Petition.

Petitioner reserves the right to respond to any constructions offered/adopted by Patent Owner/Board. Furthermore, Petitioner does not concede that each challenged claim satisfies all statutory requirements and does not waive any arguments concerning grounds that can only be raised in district court.

### **III. THE CHALLENGED CLAIMS ARE UNPATENTABLE**

#### **A. GROUND 1—Claims 1-64 are obvious over Nowka and Borkar**

##### **1. Overview of Nowka**

Nowka is titled “A 32-bit PowerPC System-on-a-Chip With Support for Dynamic Voltage Scaling and Dynamic Frequency Scaling.” MTK-1004, Title. Nowka describes a PowerPC system-on-a-chip (“SOC”) processor that “makes use of dynamic voltage and frequency scaling to adapt to the dynamically changing performance demands and power consumption constraints of high-content, battery powered applications.” MTK-1004, Abstract; MTK-1003, ¶45. Nowka’s SOC consists of a high performance 32-bit processor core, also referred to as the “CPU core,” an integrated LCD display controller, I/O interfaces, a dedicated speech accelerator, an instruction decompression engine, a DES accelerator core, a low-voltage phase-locked-loop (PLL) core, a real-time-clock core, a clock power-management core, and a sleep-management core. MTK-1004, 1442. Some of these components are shown in the structural diagram in Figure 1 and die photograph in Figure 2.

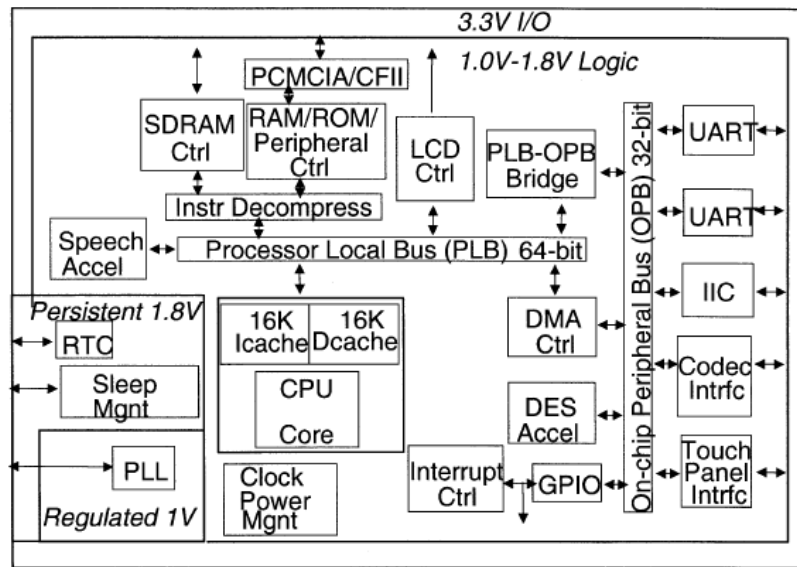
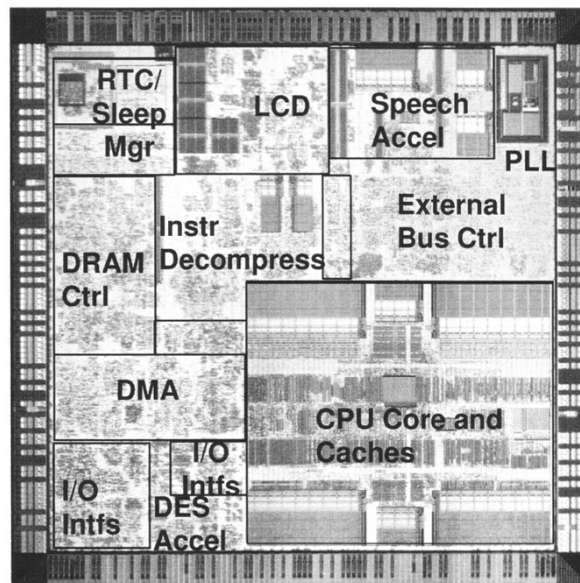


Fig. 1. PowerPC SOC structure.

MTK-1004, Fig. 1.



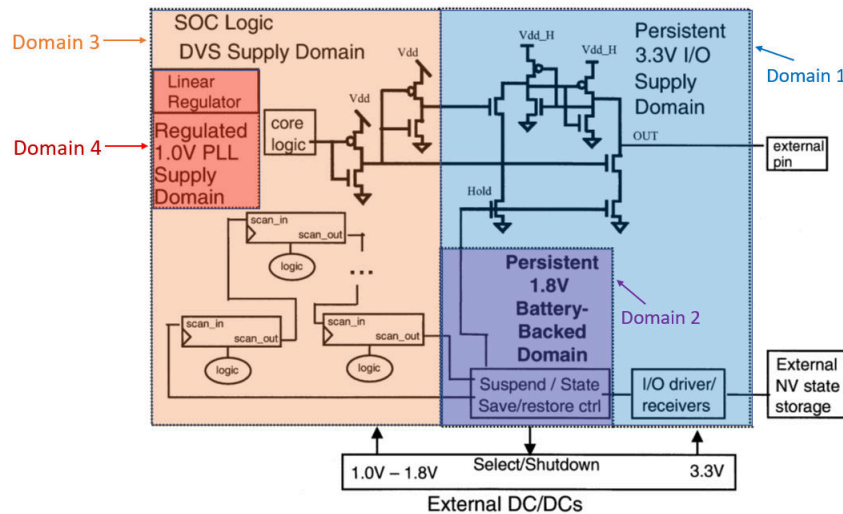
MTK-1004, Fig. 2.

Nowka explains that during “active computation,” the SOC’s “required performance tends to vary widely and quickly as a function of the workload” and that while peak performance demands high power consumption, periods of

inactivity allow for minimization of power consumption. MTK-1004, 1441. To “match the performance and power consumption of this device to the application,” “[c]apabilities to dynamically match the performance of the device with the demands of the applications are provided. This SOC additionally makes use of active power reduction techniques to dynamically match the power consumption techniques to dynamically match the power consumption with the requirements of the application. The active power consumption is reduced when resource demands are low through the use of dynamic voltage scaling, dynamic frequency scaling, unit and register level functional clock gating.” MTK-1004, 1442; MTK-1003, ¶46.

Nowka’s SOC “is divided into four distinct domains” to enable dynamic voltage and frequency scaling. These domains—two persistent voltage domains, one dynamically voltage-scaled and frequency-scaled logic domain, and one internally derived domain—are shown in annotated Figure 3 below. MTK-1004, 1442. The I/O drivers and receivers are in the persistent 3.3V domain (domain 1 below); the real-time clock and the logic controlling the voltage of the cores is in the persistent 1.8V domain (domain 2 below); the logic supply for the processor core, caches, SOC cores and accelerators in the 1-1.8V domain (domain 3 below); and the PLL is in the constant 1V domain (domain 4 below); MTK-1003, ¶47. The operating frequency of the variable voltage domain (domain 3) can also be altered

for additional active power reduction. MTK-1004, 1444 (“When the performance demands of the application decrease, the system software can lower the operating frequency.”).



MTK-1004, Fig. 3<sup>2</sup>

During operation, the logic supply is controlled by an “on-chip supervisor” that, under software control, “requests changes to the logic supply and requests shutdown of the logic supply during hibernation.” MTK-1004, 1442. The supply voltage to the logic can change between 1V and 1.8V and the frequency can be varied to reduce power consumption. MTK-1004, 1442, 1444. Nowka states that the “ability to change the output clock divider on-the-fly, without pausing the processor, allows the SOC to operate over an extremely broad range of

<sup>2</sup> All annotations to the figures have been added unless otherwise noted herein.

frequencies. This allows the power consumption to be determined by the system on a very fine time scale.” MTK-1004, 1446. Nowka’s SOC also uses clock gating and standby modes to reduce power consumption by the logic elements. MTK-1004, 1445-46.

## **2. Overview of Borkar**

Borkar is titled “Software control of transistor body bias in controlling chip parameters.” MTK-1006, Title. Borkar relates to controlling various circuit parameters, such as performance, power consumption, and temperature in integrated circuits. MTK-1006, 2:2-3; MTK-1003, ¶49. Borkar discusses controlling these parameters by changing the clock frequency, supply voltage, and threshold voltage (via body bias signals). MTK-1006, 2:49-54, Figs. 1-3, 5, 7, 9; MTK-1003, ¶50. Borkar discloses “domains,” also called “functional unit blocks,” which are groups of transistors on the chip that can be controlled independently of each other. MTK-1006, 9:48-59, 10:34-36. These domains are shown in Figures 5 and 7, which also show “voltage and frequency control circuitry” that controls power behavior of each domain via clock, body bias, and supply voltage. MTK-1006, 2:49-54, 11:41-67, Figs. 5, 7; MTK-1003, ¶51.

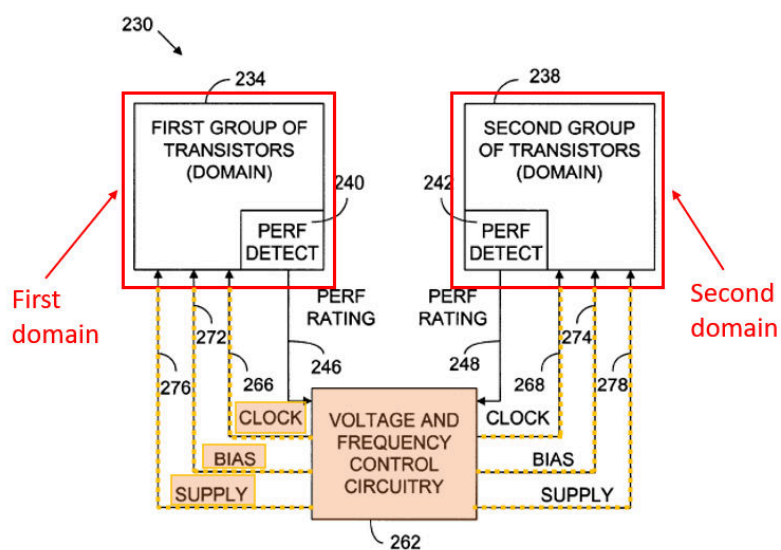


FIG. 5

MTK-1006, Fig. 5.

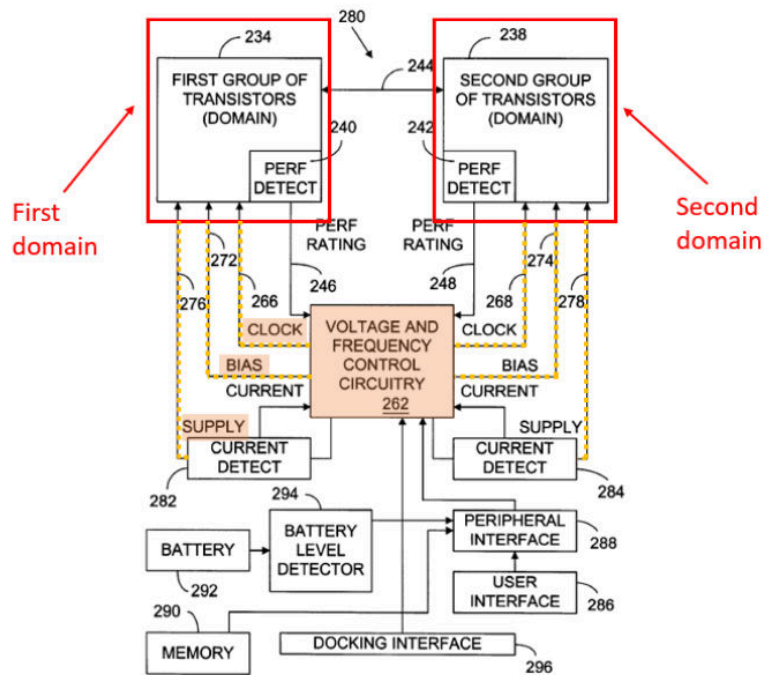


FIG. 7

MTK-1006, Fig. 7.

Further, Figure 7 of Borkar shows current detection circuitry, labeled 282 and 284, which detect the current being consumed and sends that information to the voltage and frequency control 262. MTK-1006, 13:22-25. The control circuitry then can determine the power consumption (which is current multiplied by supply voltage) and adjust the performance of the transistors accordingly. MTK-1006, 13:27-29; MTK-1003, ¶52.

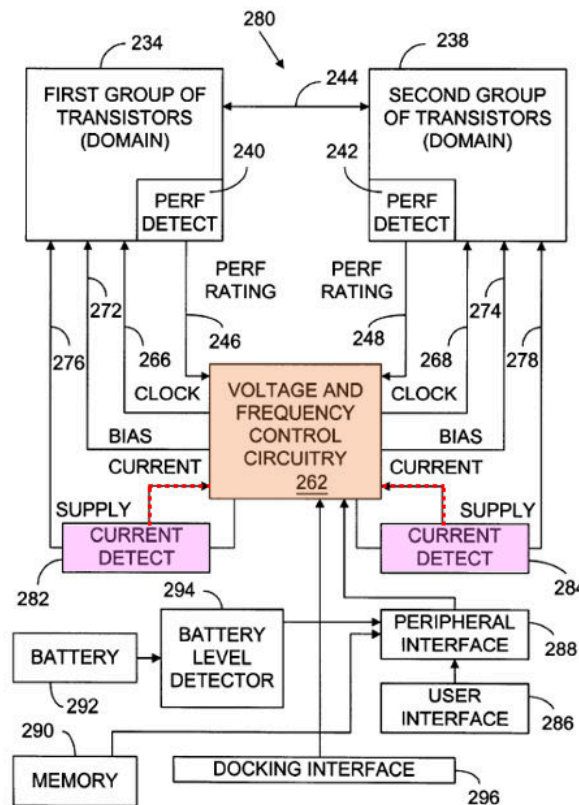


FIG. 7

MTK-1006, Fig. 7.

### 3. The Nowka-Borkar Combination

A POSITA would have been motivated to combine Nowka and Borkar for a number of reasons.

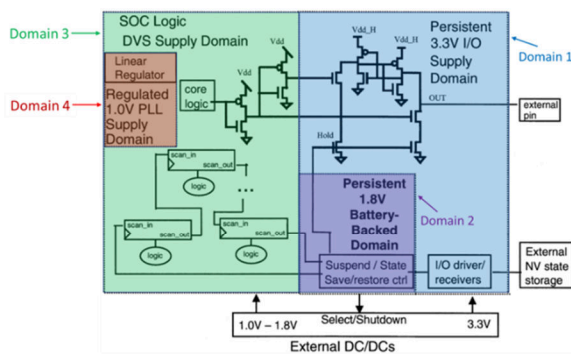
First, Nowka and Borkar are related to the same field: power management of integrated circuits on a chip. Nowka describes a “PowerPC system-on-a-chip processor which makes use of dynamic voltage scaling and on-the-fly frequency scaling to adapt to the dynamically changing performance demands and power consumption constraints of high-content, battery powered applications.” MTK-1004, Abstract. Similarly, Borkar “involves changing body bias signals ... clock

frequency signals and supply voltages to at least partially control a parameter. A parameter of the integrated circuit is a characteristic of the integrated circuit which can vary during performance including temperature, power consumption, and performance.” MTK-1006, 2:49-57; MTK-1003, ¶54.

Second, both Nowka and Borkar describe balancing performance and power consumption in an integrated circuit. For example, Nowka states that “[w]hile [devices’] peak performance demands tend to be significant, they are also highly power constrained.” MTK-1004, 1441. Similarly, Borkar states that “[t]he performance, power consumption, and temperature [of an integrated circuit] are typically related.” MTK-1006, 1:20-21. Borkar further states that “[t]he user may specify certain power conditions or a power versus performance tradeoff.” MTK-1006, 5:45-46. Therefore, both Nowka and Borkar address the need to balance performance and power consumption, and a POSITA considering Nowka’s solution would have naturally looked to Borkar for additional teachings. MTK-1003, ¶55.

Third, both Nowka and Borkar disclose operating distinct parts of the integrated circuit using different operating parameters, including the frequency and supply voltage. Nowka states that “the power distribution has been divided into four distinct domains as shown in Fig. 3.” MTK-1004, Fig. 3, 1442. Similarly, Borkar discloses that the “first and second groups of transistors may be different

function unit blocks (FUBS) on the same chip” and that “[b]ecause of transistor parameter variations, certain performance and/or power parameters of first domain 234 may be different than that of the second domain 238.” MTK-1006, 10:34-39. A side-by-side comparison of Nowka’s Fig. 3 and Borkar’s Fig. 5 shows distinct power domains. MTK-1003, ¶56.



MTK-1004, Fig. 3

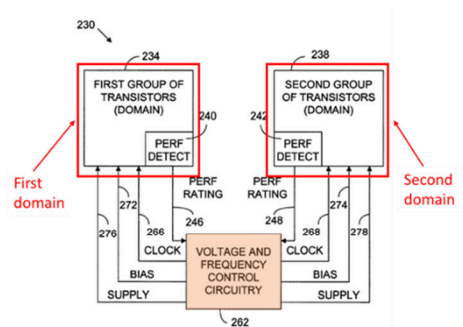


FIG. 5

MTK-1006, Fig. 5

Fourth, both Nowka and Borkar disclose controlling power consumption by changing the same quantities: supply voltage and operating frequency. Nowka states that “DVS systems adjust the supply voltage dynamically to meet the performance demands while minimizing power consumption” and that “[a]djustment to the output clock frequency can be done on-the-fly by modifying the output clock divider through a write to a control register.” MTK-1004, 1442, 1444. Similarly, Borkar discloses that “[t]he invention may also include changing clock frequency signals and supply voltage signals to at least partially control a parameter.” MTK-1006, 2:52-54. MTK-1003, ¶57.

Nowka, however, discloses a single variable power domain. A POSITA looking for more control over the SOC's power consumption would naturally look to Borkar's multiple domains, or FUBs, to effect this control. MTK-1006, 9:19-24 ("The invention...is not restricted to single chip, but rather control circuitry 114 and peripheral [] interface [] and voltage control circuitry 178 may also be used to control the settings for more than one chip (e.g., multiple processors)."); MTK-1003, ¶58. The logic domain of Nowka could be further divided into separate domains. This would be straightforward to accomplish because Nowka already has a variable power domain. For example, Nowka already discusses the physical effects and layout concerns for variable voltage domains in Section III.B, and a POSITA would have applied the same design principles to implement an additional variable domain. MTK-1004, 1443-1444; MTK-1003, ¶58.

An example of one way to implement multiple variable power domains in Nowka's SOC is shown in annotated Figure 1 below. Most of the components in Nowka's original logic domain, such as the cores, caches, and power management software are shown in a separate domain (orange) from the speech accelerator (green). Hence, the orange-colored domain constitutes one variable power island, and the green-colored domain, consisting of the speech accelerator, constitutes a second. MTK-1003, ¶59. "The speech accelerator performs the speech-labeling algorithm for acoustic modeling in speech recognition applications." MTK-1004,

1445. A POSITA would understand that this function would allow for independent operation of the speech accelerator because it does not need to operate at the same frequency as the processor cores. MTK-1003, ¶59. Because the speech accelerator only needs to operate at the capabilities of human hearing, its operating frequency and voltage can be scaled as needed. MTK-1003, ¶59. Further, a POSITA would understand that more control and precision for managing the power consumption in the speech accelerator are advantageous because “[t]he performance advantages of an accelerator can be extended to active power reductions if the additional performance allows both the core and the processor to be operated at a lower voltage and/or frequency.” MTK-1004, 1445; MTK-1003, ¶59.

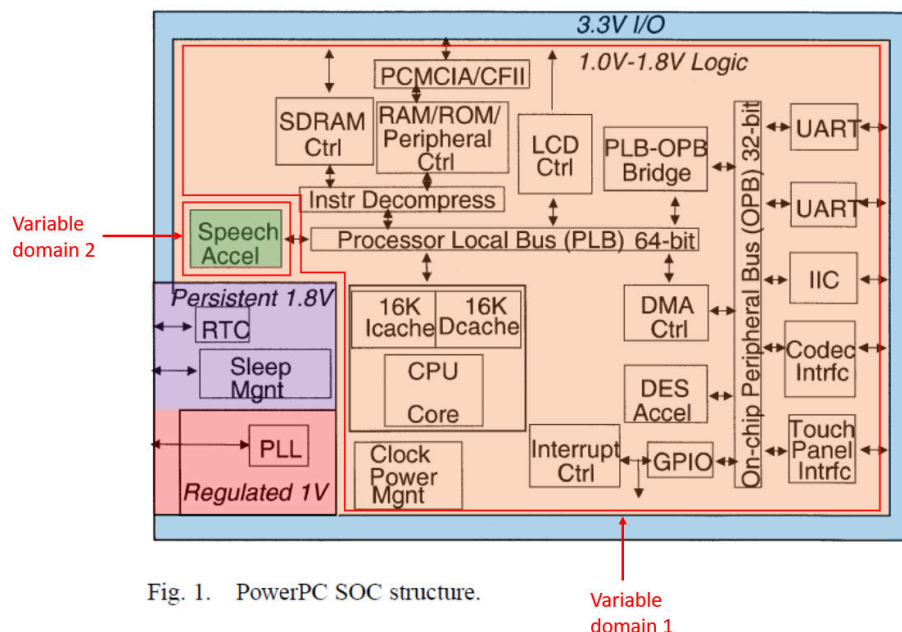


Fig. 1. PowerPC SOC structure.

MTK-1004, Figure 1.

Nowka also does not disclose monitoring power consumption signals. A

POSITA would have understood that monitoring power consumption level, as in Borkar, in the DVFS system of Nowka would provide an additional check on power consumption and would have been motivated to incorporate it. MTK-1003, ¶60. For example, Nowka teaches that “during peak activity the power consumption of the processor core is best kept at or below 500 mW.” MTK-1004, 1441; MTK-1003, ¶60.

And while Nowka does not explicitly disclose changing a threshold voltage to control the power consumption, Nowka explains that “[s]tatic power due to reverse-biased junction current, sub-threshold leakage, gate leakage and analog current sources can limit the operating lifetime of battery-powered systems. Decreasing the standby power of the IC increases shelf-life as well as overall energy efficiency.” MTK-1004, 1446. Thus, a POSITA would have been motivated to look to Borkar’s threshold voltage-tuning solution to alleviate static power in Nowka’s SOC. MTK-1003, ¶61.

**4. Claim 1**

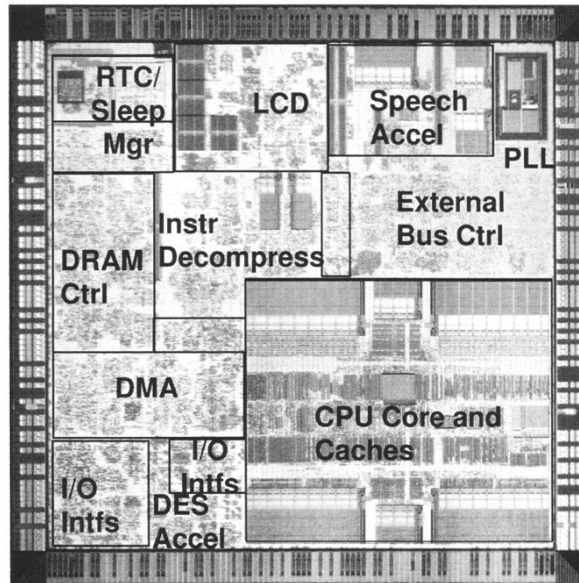
**(a) 1[p]**

To the extent the preamble is limiting,<sup>3</sup> in the Nowka-Borkar combination

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<sup>3</sup> Petitioner reserves the right to argue in counterpart litigation that the preamble is not limiting.

Nowka discloses an integrated circuit. For example, Nowka discloses a “PowerPC system-on-a-chip (SOC)” design that “consists of a higher performance 32-bit processor core.” MTK-1004, 1441, MTK-1003, ¶62. The ’885 patent defines an integrated circuit as “any electronic device that is instantiated into silicon and/or related manufacturing materials. One example of the integrated circuit 110 is a system-on-a-chip.” MTK-1001, 3:44-47. Fig. 2 shows a die photograph of Nowka’s SOC.



MTK-1004, Fig. 2.

Further, Borkar also discloses an integrated circuit. “The invention involves changing body bias signals applied to transistors in an integrated circuit in response to changing conditions to at least partially control a parameter of the integrated circuit.” MTK-1006, 2:49-52; MTK-1003, ¶63.

(b) 1[a]

In the Nowka-Borkar combination, Nowka discloses an integrated circuit chip. Nowka discloses a “PowerPC system-on-a-chip [SOC] processor,” which is an integrated circuit chip. MTK-1004, Abstract; MTK-1003, ¶¶64. Figure 1 shows the PowerPC SOC structure, and Figure 2 shows a die photograph of the SOC.

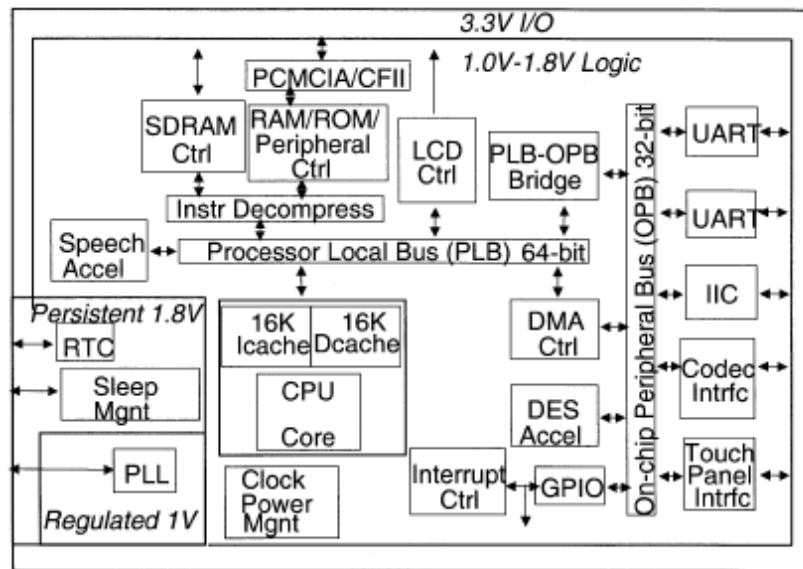
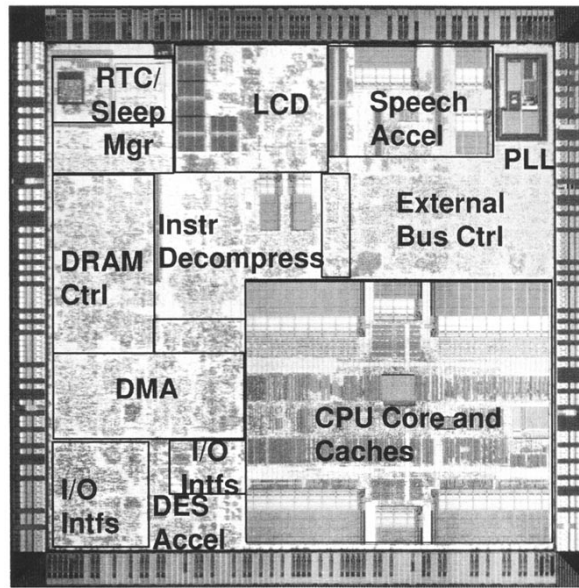


Fig. 1. PowerPC SOC structure.

MTK-1004, Fig. 1.



MTK-1004, Fig. 2.

Borkar also discloses an integrated circuit. MTK-1006, 2:49-60 (“The invention involves changing body bias signals applied to transistors in an *integrated circuit*...”), 4:5-9; MTK-1003, ¶65.

(c) 1[b]

The Nowka-Borkar combination renders obvious a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency. As discussed, Nowka discloses a power island (logic domain) with an associated power consumption that is independently controllable by changing a supply voltage and operating frequency. The logic domain is a power island because it is a “section, delineation, partition, or division” on the SOC where “power consumption is controlled within the section,

delineation, partition, or division.” MTK-1001, 3:56-59; MTK-1003, ¶67. Nowka discloses the power consumption of the logic domain being independently controllable by changing a supply voltage and operating frequency. “The active power consumption is reduced when resource demands are low through the use of dynamic voltage scaling, dynamic frequency scaling, unit and register level functional clock gating.” MTK-1004, 1442; MTK-1003, ¶67. For example, Nowka discloses changing the supply voltage of the logic domain while running Dhrystone2.1 benchmark (shown in Figure 5) and MPEG-4 decoding on the SOC (shown in Figure 6). MTK-1004, 1444; MTK-1003, ¶68.

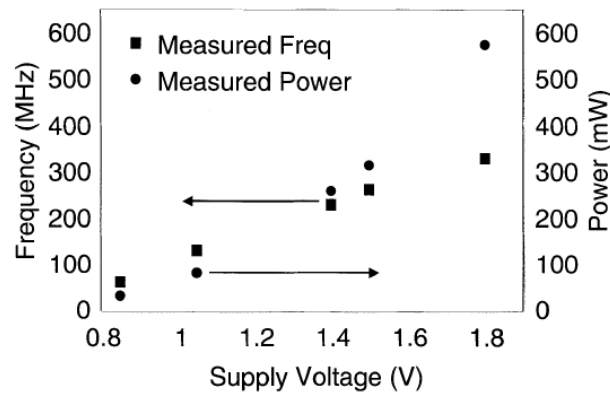


Fig. 5. Dhrystone2.1 voltage scaling measurements.

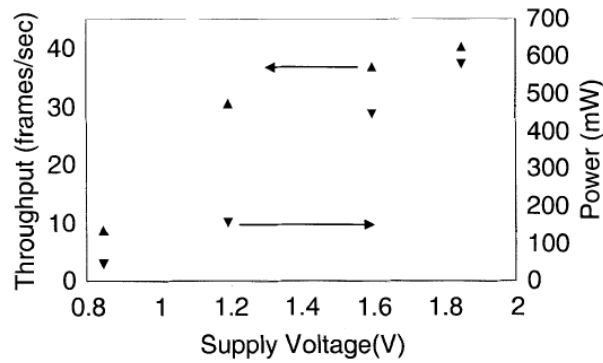


Fig. 6. MPEG-4 decode voltage scaling measurements.

MTK-1004, Figs. 5, 6.

As another example, Figure 8 shows the corresponding decrease and increase in power consumption in response to frequency and voltage changes to the logic domain. MTK-1004, 1444; MTK-1003, ¶69.

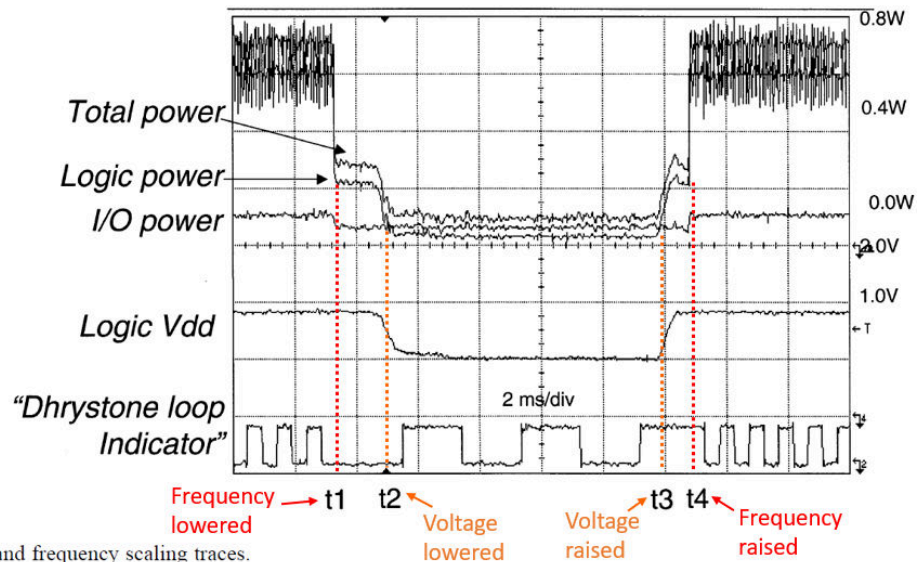


Fig. 8. Dynamic voltage and frequency scaling traces.

MTK-1004, Fig. 8.

Therefore, Nowka discloses the power consumption of a power island being independently controllable by changing a supply voltage and operating frequency. As discussed above in the Nowka-Borkar combination section, Nowka's implementation of a variable power domain could be expanded to multiple domains for greater control of power consumption. *Supra*, Section III.A.3. By implementing one or more extra variable-power domains in Nowka using Borkar, the ability in Nowka to change supply voltage and frequency of the logic domain would be expanded to the additional variable-power domain, for example the speech accelerator, providing greater granularity in power control and thus improved power savings. MTK-1003, ¶70. A POSITA would have understood that the speech accelerator function would allow for independent operation because it does not need to operate at the same frequency as the processor cores. MTK-

1004, 1445 (“The speech accelerator performs the speech-labeling algorithm for acoustic modeling in speech recognition applications.”). Because the speech accelerator only needs to operate at the capabilities of human hearing, its operating frequency and voltage can be scaled as needed. MTK-1003, ¶70. Further, a POSITA would have understood that more control and precision for managing the power consumption in the speech accelerator or other components, such as the DES accelerator, are advantageous because “[t]he performance advantages of an accelerator can be extended to active power reductions if the additional performance allows both the core and the processor to be operated at a lower voltage and/or frequency.” MTK-1004, 1445; MTK-1003, ¶70.

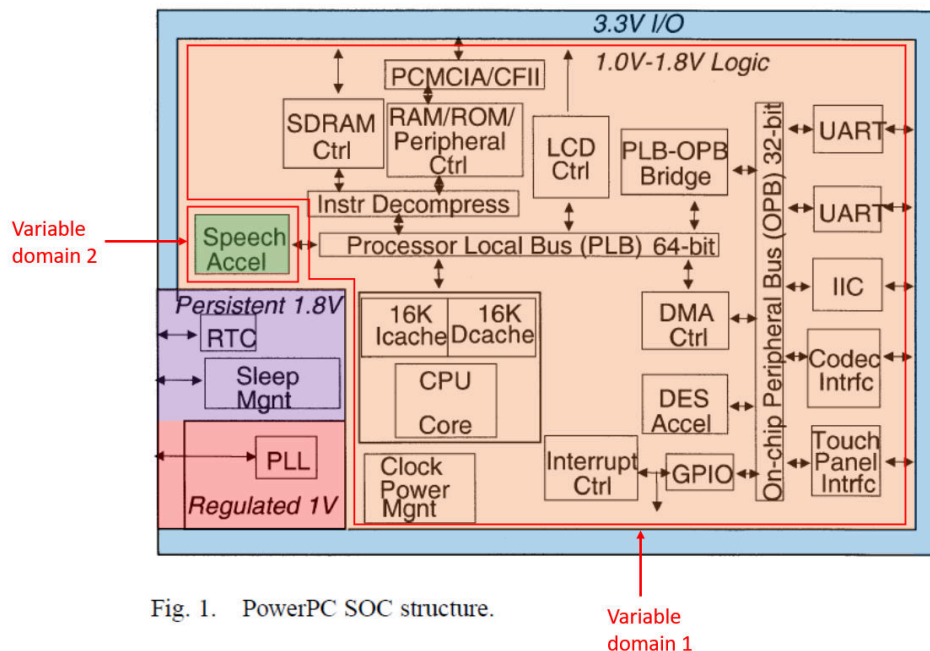


Fig. 1. PowerPC SOC structure.

MTK-1004, Fig. 1.

In this regard, Borkar similarly teaches varying power consumption via

frequency and voltage changes, but of *multiple* domains. For example, Borkar changes the body bias, supply voltage, and operating frequency applied to multiple domains. MTK-1006, 9:58-59, 10:30-11:39, Figs. 5, 7; MTK-1003, ¶71.

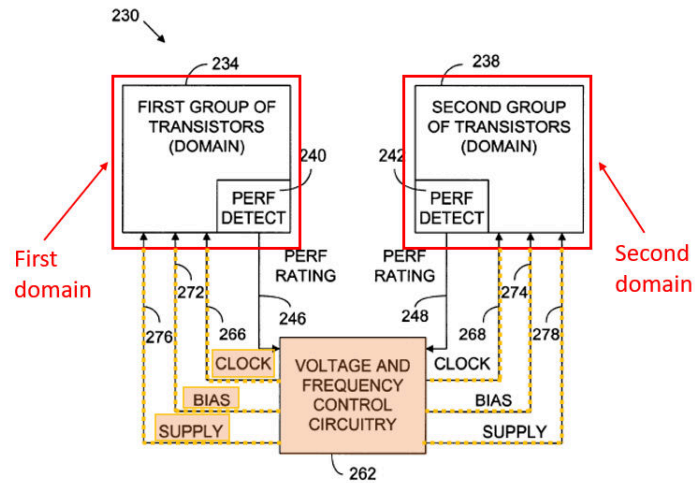


FIG. 5

MTK-1006, Fig. 5.

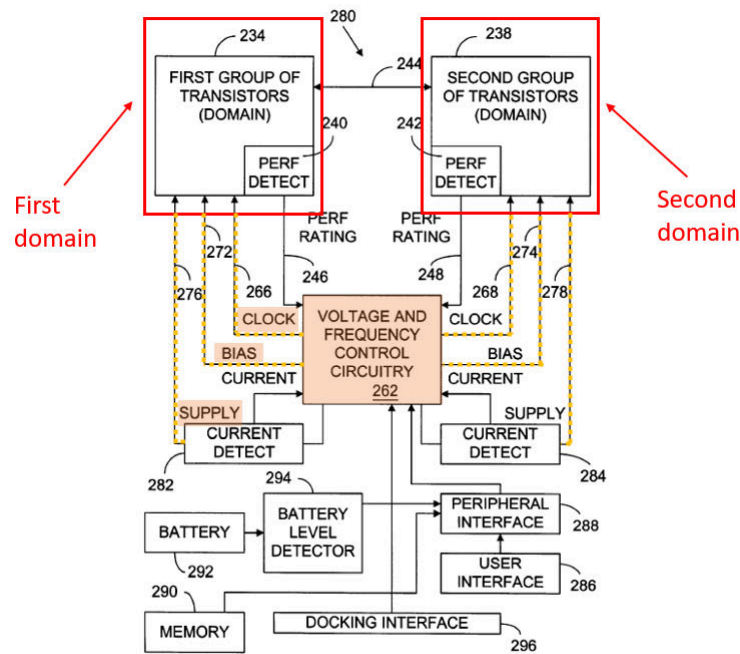


FIG. 7

MTK-1006, Fig. 7.

A POSITA would have been motivated to implement Borkar's multiple variable-domains in Nowka, for example by creating a second variable domain with the speech accelerator, for reasons discussed above. It would have been a straightforward implementation of the techniques disclosed in Nowka and Borkar (changing frequency and voltage in a power domain) applied to an analogous system (Nowka's SOC), with the modification of an additional variable power domain (Borkar). MTK-1003, ¶72.

**(d) 1[c]**

The Nowka-Borkar combination renders obvious one or more power consumption signals indicating one or more of the power consumptions. For example, Nowka discloses that “during peak activity the power consumption of the

processor core is best kept at or below 500 mW.” MTK-1004, 1441. A POSITA would have understood that Nowka recommends implementing a mechanism for maintaining power consumption at or below a threshold and would have naturally looked to a reference like Borkar which discloses such a mechanism. MTK-1003, ¶73. As explained further below, Borkar’s current signals are power consumption signals indicating power consumptions. *See* MTK-1006, 13:2-8.

Borkar discloses numerous embodiments (depicted in Figures 1-2, 4, 7) that explicitly show “current detection circuitry” which provide current signals to “voltage and frequency control circuitry.” Figure 1 of Borkar shows this current detection in an embodiment with a single processor, while Figure 7 shows current detection for multiple domains. MTK-1006, 4:58-60, 7:39-42, 13:8-11, Figs. 1-2, 4, 7 (Figs. 1, 7 shown below); MTK-1003, ¶74. Borkar’s control circuitry “*may consider the current signal (which when multiplied by the supply voltage indicates the active power consumption)* in deciding how to control the settings.” MTK-1006, 4:64-67. Borkar explains that “detect[ing] current being consumed” is a precise way of tracking power consumption levels. MTK-1006, 13:6-7; MTK-1003, ¶75. Further, “[t]he process of selecting the body bias, supply voltage, and/or clock settings in control circuitry 114 and 144 may be iterative process involving feedback from signals indicative of levels of the parameters (such as temperature and *current*) and others [*sic*] signals indicating preferences (such a

battery level signals and user selections).” MTK-1006, 6:48-53; MTK-1003, ¶74.

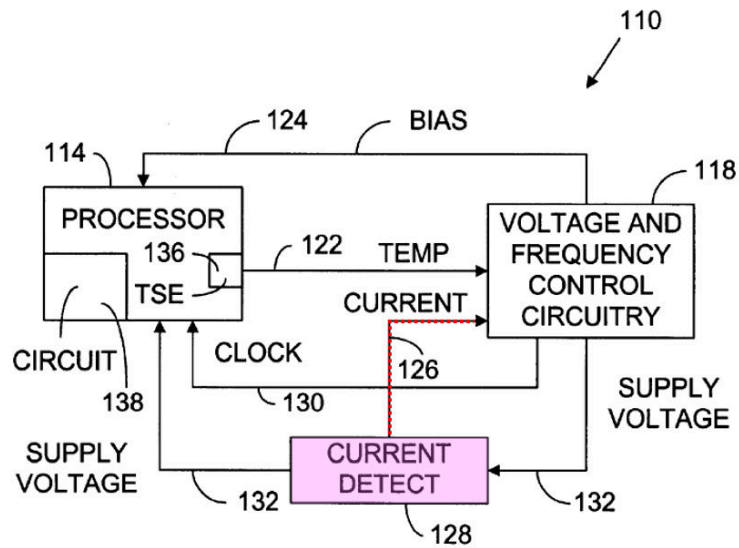


**FIG. 1**

MTK-1006, Fig. 1.

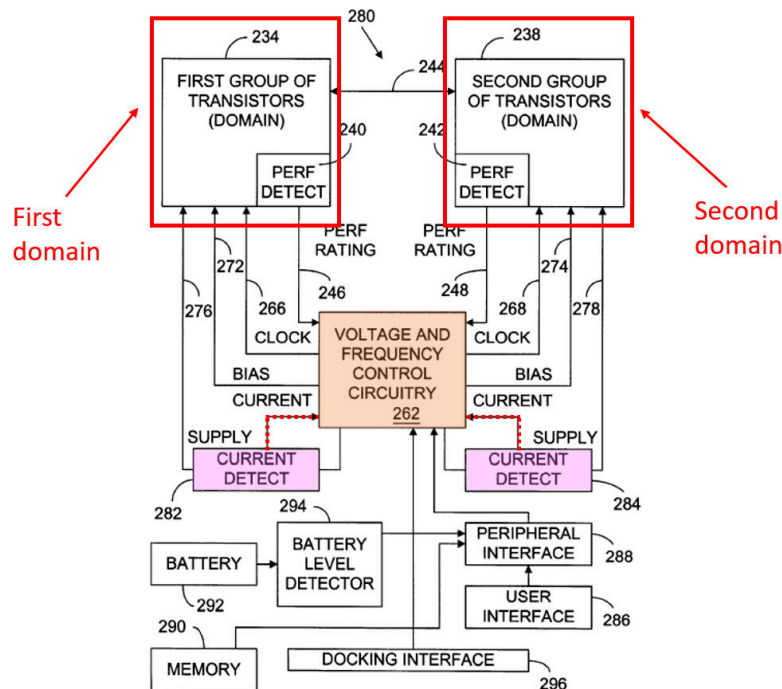


FIG. 7

MTK-1006, Fig. 7.

While the '885 patent does not define “power consumption signal,” it defines “power consumption level” as “any information, data, or statistic that indicate the power consumed in a power island...Some examples of power consumption levels are temperature and power.” MTK-1001, 6:49-50. A POSITA would understand that Borkar’s current information is a “power consumption signal” because the current information is used to calculate power consumption. MTK-1006, 13:6-7, 4:64-66 (“Control circuitry 118 may consider the current signal (which when multiplied by the supply voltage indicates the active power consumption) in deciding how to control the settings.”), 13:6-8 (“A more precise way [to not exceed power consumption levels] is to detect current being consumed.

The power can be determined from the current and supply voltage.”); MTK-1003, ¶75.

Borkar also discloses monitoring temperature signals, which the ’885 patent includes as an example of “power consumption level.” MTK-1001, 6:49-50.

Borkar’s Figure 1 (as well as Figures 2-4) depict a temperature sensitive element (TSE) on the processor which sends out a temperature signal to the voltage and frequency control circuitry or peripheral interface. MTK-1006, Figs. 1-4. Borkar explains that “control circuitry 118 monitors a temperature signal on conductor(s) 122. The temperature signals is related to the temperature of processor 136. A temperature sensitive element (TSE) 136, such as a diode, may be used in connection with a circuit to provide the temperature signal.” MTK-1006, 4:13-14; *see also* MTK-1006, 4:14-46, 6:48-53 (“The process of selecting the body bias, supply voltage, and/or clock settings in control circuitry 114 and 144 may be iterative process involving feedback from signals indicative of levels of the parameters (such as temperature and current) and others signals indicating preference (such a battery level signals and user selections).”), Figs. 1-4; MTK-1003, ¶¶76-77.

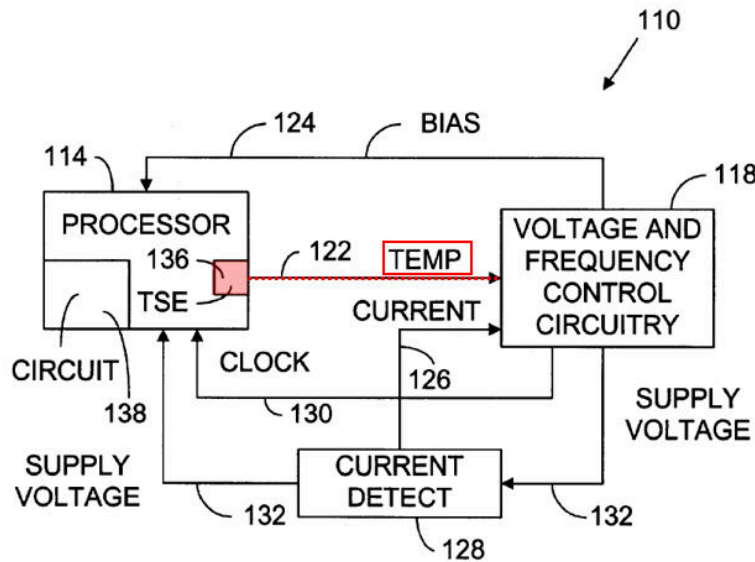


**FIG. 1**

MTK-1006, Fig. 1.

On “power consumption signals indicating one or more of the power consumptions,” Petitioner notes that in a prior litigation involving the ’885 patent, the court construed the term to have its plain meaning, but clarified that the power consumption signal is associated with a particular power island rather than multiple power islands or an entire chip. MTK-1012 at 36. For purposes of this Petition, Petitioner submits that there is no construction necessary because the plain and ordinary meaning suffices. MTK-1003, ¶78. However, the Nowka-Borkar combination also renders this element obvious under the prior court’s clarification because Borkar’s power consumption signals (current signals and temperature signals) are indicative of the state of the power island (processor or domain), not of multiple power islands or an entire chip. MTK-1003, ¶78.

**(e) 1[d]**

The Nowka-Borkar combination renders obvious a power management processor disposed on the integrated circuit chip and coupled to each of the power islands configured to monitor the one or more power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

Nowka discloses an “on-chip supervisor” that is connected to the power domains and which “requests changes to the logic supply and requests shutdown of the logic supply during hibernation.” MTK-1004, 1442. The supervisor, “in response to software commands and timeout and interrupt events, manages the clocks, internal state and external power supply to control the standby power.” MTK-1004, 1446; MTK-1003, ¶80. A POSITA would have understood that the “on-chip supervisor” is a power management processor because it changes power consumption in at least one power island (logic domain). MTK-1003, ¶81. For the same reason, Nowka’s on-chip supervisor is dedicated to execute power management software to control the power consumption, as such is the whole described purpose of the component.

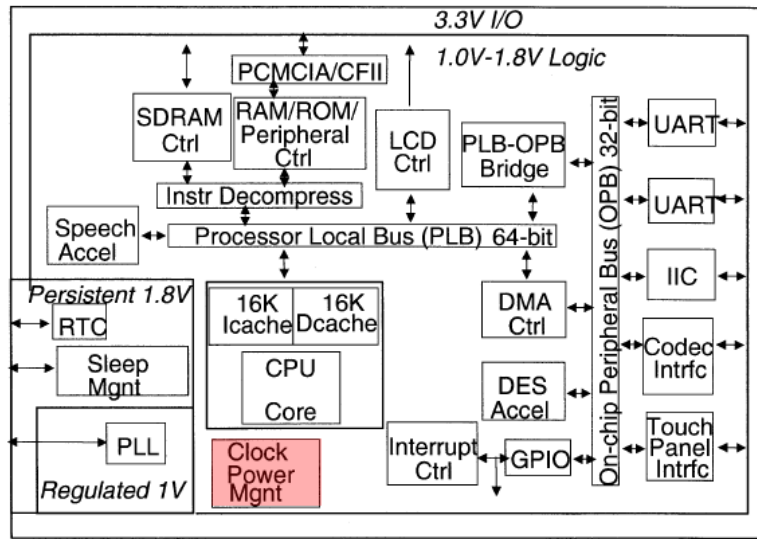


Fig. 1. PowerPC SOC structure.

MTK-1004, Fig. 1.

Furthermore, a POSITA would have understood and found obvious that the on-chip supervisor is coupled to the logic domain because such a connection is necessary for controlling the power behavior of the power islands as Nowka discloses. MTK-1003, ¶81. As modified by Borkar as explained in element 1[b], the Nowka-Borkar combination renders obvious controlling multiple variable domains, in which case the “on-chip supervisor” as modified by Borkar’s teachings (explained below) would be coupled to each of Nowka’s variable power domains. A POSITA would have been motivated to incorporate Borkar’s teachings regarding its power management processor, explained below, to modify Nowka and its “on-chip supervisor” in this way, for the same reasons explained in Section VIII.A.3 and element 1[b]. MTK-1003, ¶81.

Further, a POSITA would have understood that Borkar's "control circuitry" was a power management processor and/or could be incorporated into Nowka's "on-chip supervisor" to form the power management processor, as the two perform the similar function of controlling power consumption of the power islands. MTK-1004, 1446; MTK-1006, 4:3-5 ("Control circuitry 118 changes the body bias, supply voltage, and/or clock settings to at least partially to control one or more parameters of processor 114."), 4:20-33, 5:45-52 ("...For example, the user could specify that he or she wants the battery to last for 4 hours. Control circuitry 144 could then lower the supply voltage, lower the frequency of a clock of processor 114, and/or change the bias voltage of some or all transistors of processor 114. Control circuitry 144 may make additional changes as needed."); MTK-1003, ¶82. Borkar's control circuitry is also dedicated to execute the power management software because its whole described purpose is to manage the power of the processor or domains. MTK-1003, ¶82. Further, Borkar shows that its control circuitry is coupled to the power islands through conductors. MTK-1006, 11:22-27, 11:40-43, 11:55-58; MTK-1003, ¶82.

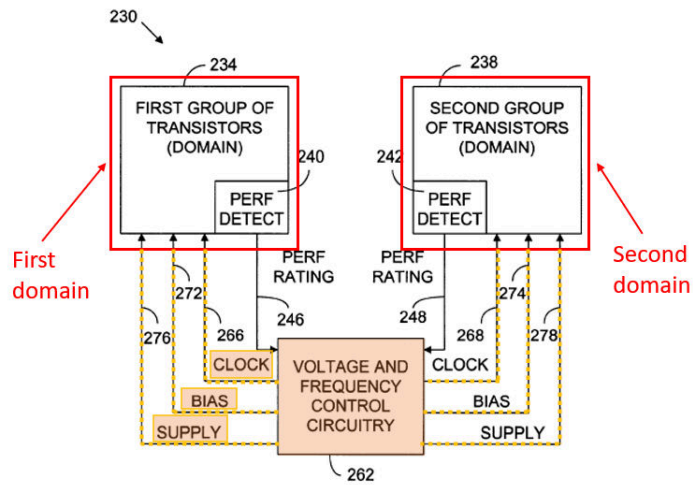


FIG. 5

MTK-1006, Fig. 5.

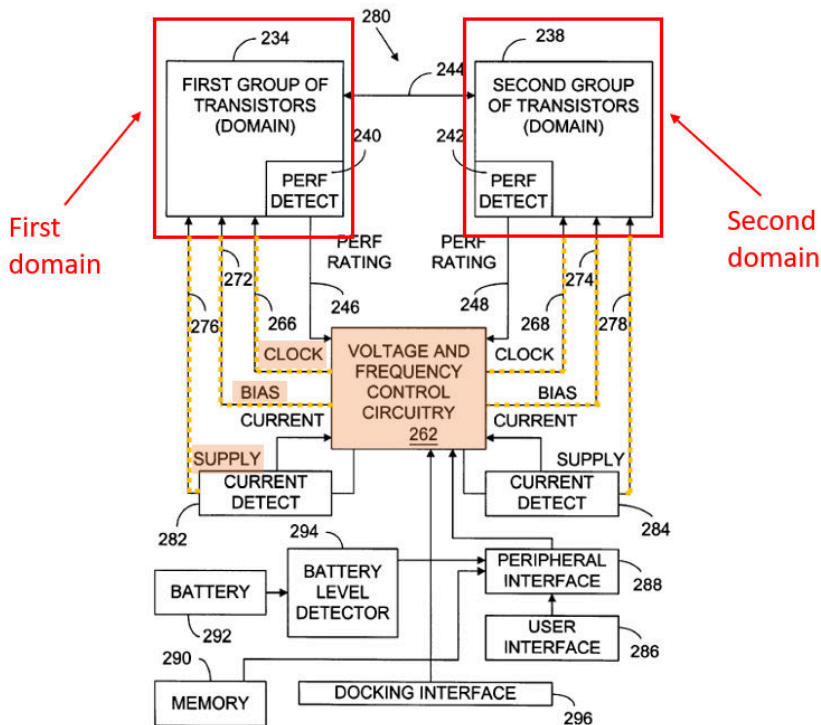


FIG. 7

MTK-1006, Fig. 7.

The Nowka-Borkar combination renders obvious that the power

management processor is configured to monitor one or more power consumption signals. As discussed for 1[c], Borkar discloses “current detection circuitry” which provide current signals to “voltage and frequency control circuitry.” MTK-1006, 4:58-60, 7:39-42, 13:8-11, Figs. 1-2, 4, 7. Borkar’s control circuitry “*may consider the current signal (which when multiplied by the supply voltage indicates the active power consumption)* in deciding how to control the settings.” MTK-1006, 4:64-67. Borkar also discloses monitoring temperature signals, as discussed for 1[c], incorporated herein. MTK-1006, 4:12-46, 6:48-53; MTK-1003, ¶83.

The Nowka-Borkar combination also renders obvious the power management processor being dedicated to execute power management software to individually control each of the power consumptions. A POSITA would have understood Nowka’s on-chip supervisor and Borkar’s control circuitry to be dedicated to execute the power management software because their whole described purpose is to manage the power of the power islands via executing power management software. MTK-1004, 1442 (“The on-chip supervisor controls the external DC/DC converter, which provides the logic supply.”), 1442 (“the supervisor requests changes to the logic supply and requests shutdown of the logic supply during hibernation.”), 1446 (“The on-chip clock and power supervisor, in response to software commands and timeout and interrupt events, manages the

clocks, internal state and external power supply to control the standby power.”); MTK-1006, 1:63-65 (“[T]he control circuitry controls the setting responsive to processor signal resulting for execution of software.”), 4:3-5 (“Control circuitry 118 changes the body bias, supply voltage, and/or clock settings to at least partially to control one or more parameters of processor 114.”), 4:20-33, 4:64-67, 5:20-24, 5:45-52, 5:59-64, 6:1-7, 6:12-13, 6:26-53, 11:22-35, 11:41-67, Figs. 1-5, 7; MTK-1003, ¶84. And as discussed for 1[b], incorporated herein, the Nowka-Borkar combination renders obvious individual control of power islands’ power consumptions.

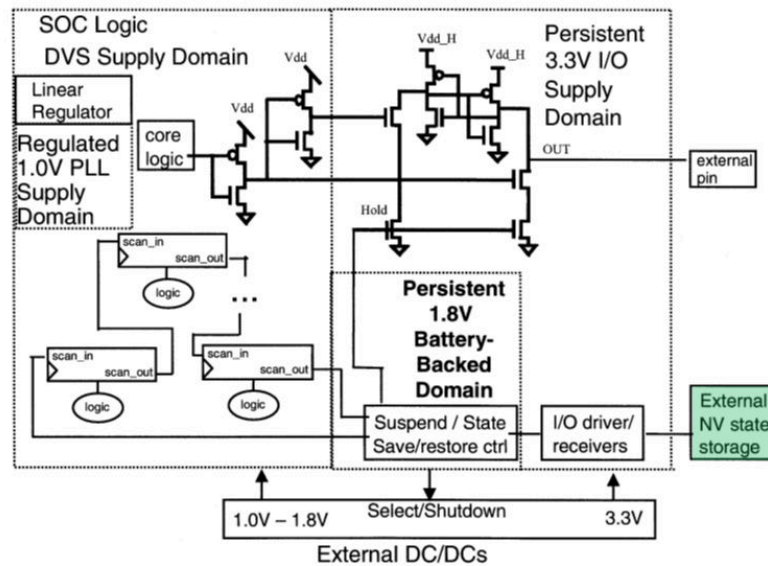
The Nowka-Borkar combination also renders obvious the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request. Nowka’s “on-chip supervisor” “requests changes to the logic supply and requests shutdown of the logic supply during hibernation.” MTK-1004, 1442. A POSITA would have understood that the “on-chip supervisor” changes power consumption in at least one power island (logic domain) is a power consumption change request. MTK-1003, ¶85. Further, POSITA would have found it obvious that the on-chip supervisor “requests changes to the logic supply” in response to a power consumption change request, and this is further supported by Nowka’s discussion that the “on-chip supervisor” operates “under software control” to change the logic

supply. MTK-1004, 1442; MTK-1003, ¶85. The supervisor, “in response to software commands and timeout and interrupt events, manages the clocks, internal state and external power supply to control the standby power.” MTK-1004, 1446; MTK-1003, ¶85. In addition, “under software control, both the voltage and the frequency of the processor can be modified, thereby allowing the performance demands of the application to be met while minimizing the dynamic power consumption.” MTK-1004, 1446; *see also* MTK-1004, 1442 (“Capabilities to dynamically match the performance of the device with the demands of the applications are provided.”). From these disclosures, a POSITA would have understood that Nowka’s on-chip supervisor executes the power consumption change in response to power consumption change requests from the “system software,” as the software must make the decisions to modify the power consumption level while “allowing the performance demands of the application to be met.” MTK-1004, 1446; MTK-1003, ¶85. Further, Borkar discloses changing power consumption in a power island in response to a power consumption change request. MTK-1006, 4:64-67 (“System 170 may operate the same as system 110 of FIG. 1 with respect to the body bias, supply voltage, and/or clock settings *in response to* changes in temperature and power consumption. System 200 may operate the same described above in connection with system 140 of FIG. 2 with respect to the body bias, supply voltage, and/or clock settings *in response input*

*signals* reflecting changes in temperature, power consumption, user settings, battery level signals, and docking station interface conditions.”), 13:28-30 (“These components can provides [*sic*] input signals that are considered by control circuitry 262 in deciding power constraints.”); MTK-1003, ¶86.

## **5. Claim 2**

The Nowka-Borkar combination renders obvious wherein the power management software is embedded firmware in the integrated circuit. A POSITA would have understood and found it obvious that Nowka’s “power management software” was embedded firmware because it likely resides in the non-volatile memory in accordance with design principles at the time. *See* MTK-1001, 4:62-5:2, Fig. 2; MTK-1007 at 5 (“Typically, [firmware] is the code that boots the machine [] and implements interfaces for sleep, wake, and some restart operations.”); MTK-1003, ¶87.



MTK-1004, Fig. 3.

This power management embedded firmware works with the “on-chip supervisor” and controls the hardware circuitry that changes parameters such as voltage and frequency of the PEs. MTK-1004, 1442 (“An on-chip supervisor controls the external DC/DC converter, which provides the logic supply. Under software control, the supervisor requests changes to the logic supply and requests shutdown of the logic supply during hibernation.”); MTK-1003, ¶88.

To the extent it is argued that Nowka’s “power management software” is not embedded firmware, a POSITA would have understood and found obvious that the power management software in Borkar was also embedded firmware because it is software that resides in the voltage and frequency control circuitry. MTK-1006, 7:61-65 (“However, in system 170 and 200, these the determination of the settings may occur by circuitry in peripheral interface 180 in response to software control

of operating system 176 and/or a program, rather than in hardware as in control circuitry 118 and 144.”), 4:3-5 (“Control circuitry 118 changes the body bias, supply voltage, and/or clock settings to at least partially to control one or more parameters of processor 114.”), 1:60-2:3, 4:64-67, 5:20-24, 5:47-52, 5:59-64, 6:1-7, 6:12-13, 6:31-43 (discussing control circuitry changing power settings), 6:63-7:4, 7:61-65, 8:1-46, 8:58-61 (discussing software controlling power), Figs. 1, 2, 5, 7; MTK-1003, ¶89. A POSITA would have been motivated to combine Nowka and Borkar for the reasons previously explained. *Supra*, Section III.A.3; MTK-1003, ¶89.

## 6. Claim 3

The Nowka-Borkar combination renders obvious wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors. For example, as discussed above for limitation 1[b], Nowka discloses a variable power domain that receives a supply voltage that varies from 1.0V to 1.8V. MTK-1004, 1442. Nowka also discloses “[t]he active power consumption is reduced when resources demands are low through the use of **dynamic voltage scaling**, dynamic frequency scaling, unit and register level functional clock gating.” MTK-1004, 1442. Dynamic voltage scaling constitutes selecting a non-zero supply voltage for the power domain. MTK-1003, ¶90. Borkar also discloses

that “control circuitry changes...supply voltage...to control one or more parameters of processor 114,” thereby also disclosing selecting a non-zero supply voltage. MTK-1006, 4:3-5; MTK-1003, ¶90.

Nowka further discloses stopping a clock to change the power consumption. Nowka discloses standby modes called “Freeze, Hibernation and Cryo modes.” MTK-1004, 1446. In Freeze mode, “*the system clock is stopped* and the logic supply is decreased to its minimum value of 1.0V.” MTK-1004, 1446; MTK-1003, ¶91. Similarly, in Cryo mode “the suspend controller *stops the clocks*, freezes the I/O drivers, scans the register state out through the IIC interface to nonvolatile storage, removes logic power and waits for a wakeup event.” MTK-1004, 1446; MTK-1003, ¶91.

In the combination, Borkar discloses changing power consumption by selecting a threshold voltage. “The leakage power consumption is higher with a smaller threshold voltage and lower with a higher threshold voltage. The active power consumption may also be effected by body bias.” MTK-1008, 3:52-56. “For example...body bias signals [may be] changed so that the *threshold voltage is raised*.” MTK-1006, 4:26-28; *see also* MTK-1006, 3:46-57, 4:28-32, 5:25-34, 5:55-64, 6:23-25, 6:31-40, 9:35-39, 12:39-42 (disclosing changing threshold voltage); MTK-1003, ¶92. A POSITA would have been motivated to combine Nowka and Borkar for the reasons previously explained. *Supra*, Section III.A.3;

MTK-1003, ¶92.

**7. Claim 4**

The Nowka-Borkar combination renders obvious wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands. Borkar discloses that some domains “may run off the same clock signal or otherwise need to run synchronously.” MTK-1006, 10:6-7. “Indeed, there can be reasons ...[that] groups of transistors that run off a different clock signal or that are asynchronous.” MTK-1006, 10:16-18. A POSITA would have understood and found it obvious that Borkar’s domains, or FUBs, can communicate synchronously or asynchronously. MTK-1006, 10:6-18; MTK-1003, ¶93. Therefore, a POSITA would have understood, and found it obvious, that a power island in the Nicol-Borkar combination is capable of communicating synchronously and asynchronously with a second power island. MTK-1003, ¶93.

On the terms “synchronously” and “asynchronously,” Petitioner notes that in a prior litigation involving a related patent, U.S. Patent No. 7,996,811, the court construed the term “synchronously” as “with coordination between components (i.e., power islands) before communication transmission begins,” “asynchronously” as “without coordination between components (i.e., power islands) before transmission begins.” MTK-1011 at 45. For purposes of this

Petition, Petitioner submits that there is no construction necessary because the plain and ordinary meaning suffices. MTK-1003, ¶94. However, the Nowka-Borkar combination also renders this element obvious under the prior court's construction because Borkar describes domains that communicate synchronously (with coordination between components before transmission begins) and asynchronously (without coordination between components before transmission begins). MTK-1003, ¶94.

## **8. Claim 5**

The Nowka-Borkar combination renders obvious wherein each of the power consumptions is further controlled by stopping a clock. For example, Nowka discloses that “in Freeze mode *the system clock is stopped.*” MTK-1004, 1446. In Cryo mode, “the suspend controller *stops the clocks*, freezes the I/O drivers,...removes logic power and waits for a wakeup event at which time it restores the supply, restores the state and restarts the clocks.” MTK-1004, 1446; MTK-1003, ¶95. From this teaching, and as explained above, in the modified version of Nowka containing two variable-power domains, it would have been obvious to a POSITA that the power consumption of both domains were further controlled by stopping a clock. MTK-1003, ¶95. Similarly, Borkar discloses a “clock signal producing circuitry” which “provides one or more clock signals,” which a POSITA would understand to enable stopping, or turning off, the clock

signal. MTK-1006, 13:61-63, Fig. 9; MTK-1003, ¶96.

## 9. Claim 6

The Nowka-Borkar combination renders obvious wherein stopping the clock comprises clock gating. For example, Nowka discloses “[t]he active power consumption is reduced when resources demands are low through the use of dynamic voltage scaling, dynamic frequency scaling, *unit and register level functional clock gating*.” MTK-1004, 1442; MTK-1003, ¶96. Further, Nowka discloses that “dynamic power is saved in this design by *gating off* inactive latches [12] and units. Approximately 80% of the processor registers and 50% of the SOC core registers are functionally *clock gated* when they are not accessed.” MTK-1004, 1445; MTK-1003, ¶97.

## 10. Claim 7

The Nowka-Borkar combination renders obvious wherein the one or more power consumption signals include temperature or power dissipation measurements. As discussed in 1[c], incorporated herein, Borka discloses power consumption signals including temperature measurements. *Supra* Ground 1, element 1[c]; MTK-1003, ¶98.

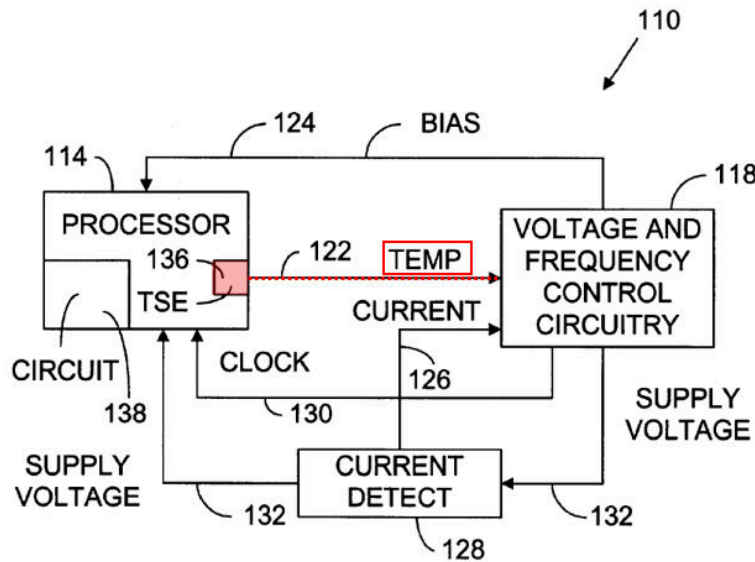


**FIG. 1**

MTK-1006, Fig. 1.

**11. Claim 8**

**(a) 8[p]**

*Supra* Ground 1, element 1[p]. MTK-1003, ¶99.

**(b) 8[a]**

*Supra* Ground 1, element 1[a]. MTK-1003, ¶100.

**(c) 8[b]**

*Supra* Ground 1, element 1[b]. MTK-1003, ¶101.

**(d) 8[c]**

*Supra* Ground 1, element 1[c]. MTK-1003, ¶102.

**(e) 8[d]**

*Supra* Ground 1, element 1[d]. MTK-1003, ¶103. For the same reasons explained regarding “power management processor” for 1[d], incorporated herein,

a POSITA would have understood the Nowka's "on-chip supervisor" combined with Borkar's "control circuitry" to be a "power manager."

**12. Claim 9**

The Nowka-Borkar combination renders obvious wherein the power manager comprises a processor configured to execute power management software to individually control each of the power consumptions. As discussed for 1[d], incorporated herein, a POSITA would have understood the Nowka-Borkar "power management processor" to be a processor configured to execute power management software to individually control each of the power consumptions. *Supra* Ground 1, element 1[d]. MTK-1003, ¶104.

**13. Claim 10**

*Supra* Ground 1, claims 3, 9. MTK-1003, ¶105.

**14. Claim 11**

*Supra* Ground 1, claims 4, 9. MTK-1003, ¶106.

**15. Claim 12**

The Nowka-Borkar combination renders obvious wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands. Nowka discloses an "on-chip supervisor" that "manages the clocks, internal state and external power supply to control the standby power." MTK-1004, 1446; MTK-1003, ¶107. Accordingly, the on-chip

supervisor acts as a “master” power manager during operation of Nowka’s integrated circuit because it oversees the power behavior of the entire SoC. MTK-1001, 5:48-49; MTK-1003, ¶107.

To the extent it is argued that Nowka’s on-chip supervisor is not a master manager, Borkar similarly discloses “control circuitry” that changes the body bias, supply voltage, and/or clock settings of the processor or multiple domains. MTK-1006, 4:3-5, 11:22-67; MTK-1003, ¶108. A POSITA would have understood Borkar’s control circuitry to be a “master” power manager because it controls the power behavior of multiple components on the chip. MTK-1003; ¶108. A POSITA would have understood that Borkar’s control circuitry would be integrated into Nowka’s on-chip supervisor to provide control of the SOC’s operating parameters. MTK-1003, ¶108.

Nowka discloses two examples of slave managers. First, the PLL (which controls the frequency) and the external DC/DC converters (which control the supply voltage) constitute a “slave manager” because they control the power of the logic domain. MTK-1004, 1442, 1444, MTK-1003, ¶109. Second, Nowka discloses “clock dividers controlled by register values” that “allow[s] the clocks to the cores to be modified dynamically and individually.” MTK-1004, 1445. Nowka further discloses that “the clocks to individual functional cores can also be frozen by the clock and power management software.” MTK-1004, 1445; MTK-

1003, ¶110. Accordingly, a POSITA would have understood the clock dividers and the relevant registers as a “slave power manager” because it changes power within the logic domain. MTK-1001, 6:11-12; MTK-1003, ¶110. Further, the control circuitry depicted in Borkar’s Figure 9 to controls the power behavior of each power domain or processor. MTK-1006, 4:3-5; MTK-1003, ¶111.

Accordingly, a POSITA would have understood that circuitry to be a slave power manager. MTK-1001, 6:11-12; MTK-1003, ¶111.

**16. Claim 13**

*Supra* Ground 1, claims 5, 8. MTK-1003, ¶112.

**17. Claim 14**

*Supra* Ground 1, claims 6, 13. MTK-1003, ¶113.

**18. Claim 15**

*Supra* Ground 1, claims 7, 8. MTK-1003, ¶114.

**19. Claim 16**

**(a) 16[p]**

*Supra* Ground 1, element 1[p]. MTK-1003, ¶115.

**(b) 16[a]**

*Supra* Ground 1, element 1[a]. MTK-1003, ¶116.

**(c) 16[b]**

*Supra* Ground 1, elements 1[b], 1[c]. MTK-1003, ¶117.

**(d) 16[c]**

*Supra* Ground 1, element 1[d]. MTK-1003, ¶118.

**20. Claim 17**

*Supra* Ground 1, claims 2, 16. MTK-1003, ¶119.

**21. Claim 18**

*Supra* Ground 1, claims 3, 17. MTK-1003, ¶120.

**22. Claim 19**

*Supra* Ground 1, claims 4, 17. MTK-1003, ¶121.

**23. Claim 20**

*Supra* Ground 1, claims 5, 16. MTK-1003, ¶122.

**24. Claim 21**

*Supra* Ground 1, claims 6, 20. MTK-1003, ¶123.

**25. Claim 22**

*Supra* Ground 1, claims 7, 16. MTK-1003, ¶124.

**26. Claim 23**

**(a) 23[p]**

*Supra* Ground 1, element 1[p]. MTK-1003, ¶125.

**(b) 23[a]**

*Supra* Ground 1, element 1[a]. MTK-1003, ¶126.

**(c) 23[b]**

*Supra* Ground 1, elements 1[b], 1[c]. MTK-1003, ¶127.

**(d) 23[c]**

*Supra* Ground 1, element 1[d]. MTK-1003, ¶128.

**27. Claim 24**

*Supra* Ground 1, claims 9, 23. MTK-1003, ¶129.

**28. Claim 25**

*Supra* Ground 1, claims 10, 24. MTK-1003, ¶130.

**29. Claim 26**

*Supra* Ground 1, claims 11, 24. MTK-1003, ¶131.

**30. Claim 27**

*Supra* Ground 1, claims 12, 23. MTK-1003, ¶132.

**31. Claim 28**

*Supra* Ground 1, claims 13, 23. MTK-1003, ¶133.

**32. Claim 29**

*Supra* Ground 1, claims 14, 28. MTK-1003, ¶134.

**33. Claim 30**

*Supra* Ground 1, claims 15, 23. MTK-1003, ¶135.

**34. Claim 31**

**(a) 31[p]**

*Supra* Ground 1, element 1[p]. The Nowka-Borkar combination further discloses a system. For example, Nowka discloses a “PowerPC system-on-a-chip (SOC)” design that “consists of a higher performance 32-bit processor core.”

MTK-1004, 1441. The '885 patent states that its “system 100 includes an integrated circuit 110 and a power manager 120. The integrated circuit 110 is any electronic device that is instantiated into silicon and/or related manufacturing materials. One example of the integrated circuit 110 is a system-on-a-chip.” MTK-1001, 3:43-47. Accordingly, a POSITA would have understood that Nowka’s SOC is a system. A POSITA would have also understood Borkar to disclose a system. MTK-1006, 1:59-60 (“In some embodiments, the invention includes a **system** having a processor and control circuitry.”), 2:13-36 (“FIG. 1 is a block diagram representation of a computer **system** according to some embodiments of the invention.... FIG. 5 is a block diagram representation of a **system**[.]”), 2:61-65, 4:60-64, 5:1-2. MTK-1003, ¶136.

**(b) 31[a]**

*Supra* Ground 1, element 1[a]. MTK-1003, ¶137.

**(c) 31[b]**

*Supra* Ground 1, element 1[b]. MTK-1003, ¶138.

**(d) 31[c]**

*Supra* Ground 1, element 1[c]. MTK-1003, ¶139.

**(e) 31[d]**

*Supra* Ground 1, element 1[d]. MTK-1003, ¶140.

**35. Claim 32**

*Supra* Ground 1, claims 2, 31. MTK-1003, ¶141.

**36. Claim 33**

*Supra* Ground 1, claims 3, 32. MTK-1003, ¶142.

**37. Claim 34**

*Supra* Ground 1, claims 4, 32. MTK-1003, ¶143.

**38. Claim 35**

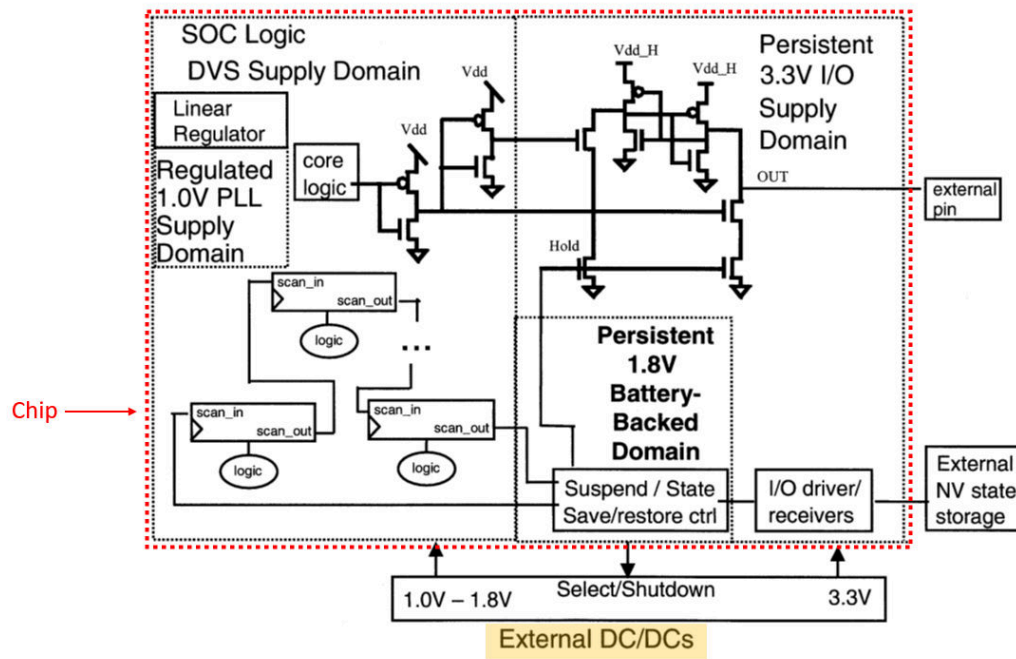
*Supra* Ground 1, claims 5, 31. MTK-1003, ¶144.

**39. Claim 36**

*Supra* Ground 1, claims 6, 35. MTK-1003, ¶145.

**40. Claim 37**

The Nowka-Borkar combination renders obvious wherein the system is configured to have the supply voltage provided by an external regulator. Nowka discloses an external “DC/DC converter, which controls the logic supply,” as shown in Figure 3. MTK-1004, 1442, Fig. 3. The DC/DC converter is external to the chip, and supplies multiple voltages to the SOC, including a 1.0-1.8V variable supply depending on the needs of the circuit, and a persistent 3.3V supplied to the I/O drivers and receivers. MTK-1004, 1442; MTK-1003, ¶146. Accordingly, a POSITA would have understood that Nowka is configured to have the supply voltage provided by an external regulator. MTK-1003, ¶¶146-147.



MTK-1004, Fig. 3.

Additionally, Borkar discloses an external regulator that provides the supply voltage. While Figure 3 depicts the “voltage control circuitry” inside of the chip, Borkar also discloses that “[v]oltage control circuitry 178 may be on the same chip (e.g., chip 186) as is processor 174 *or on a different chip.*” MTK-1006, 7:5-7. When the control circuitry is on a different chip than the processor, it would necessarily be external to the chip that contains the processor, thus making it an external regulator. MTK-1003, ¶148.

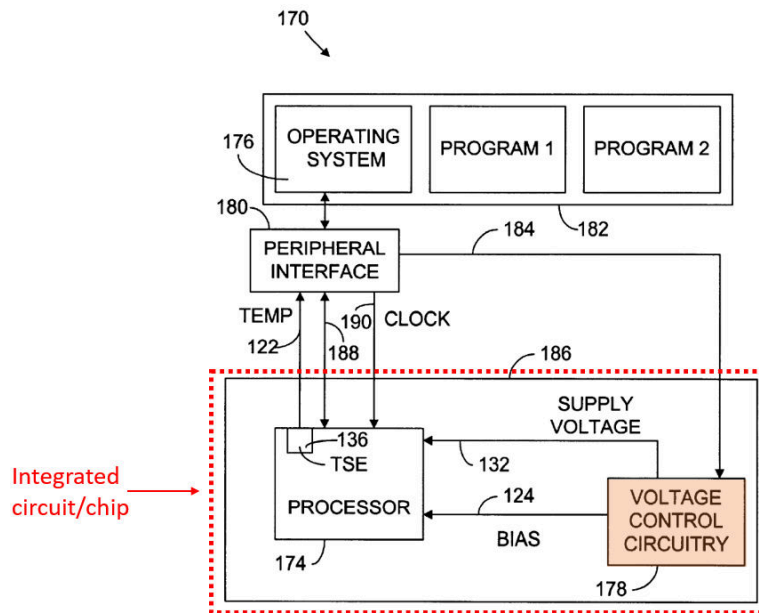


**FIG. 3**

MTK-1006, Fig. 3.

**41. Claim 38**

*Supra* Ground 1, claims 7, 31. MTK-1003, ¶149.

**42. Claim 39**

**(a) 39[p]**

*Supra* Ground 1, element 31[p]. MTK-1003, ¶150.

**(b) 39[a]**

*Supra* Ground 1, element 1[a]. MTK-1003, ¶151.

**(c) 39[b]**

*Supra* Ground 1, element 1[b]. MTK-1003, ¶152.

**(d) 39[c]**

*Supra* Ground 1, element 1[c]. MTK-1003, ¶153.

**(e) 39[d]**

*Supra* Ground 1, element 1[d]. MTK-1003, ¶154.

**43. Claim 40**

*Supra* Ground 1, claims 9, 39. MTK-1003, ¶155.

**44. Claim 41**

*Supra* Ground 1, claims 10, 40. MTK-1003, ¶156.

**45. Claim 42**

*Supra* Ground 1, claims 11, 40. MTK-1003, ¶157.

**46. Claim 43**

*Supra* Ground 1, claims 12, 39. MTK-1003, ¶158.

**47. Claim 44**

*Supra* Ground 1, claims 13, 39. MTK-1003, ¶159.

**48. Claim 45**

*Supra* Ground 1, claims 14, 44. MTK-1003, ¶160.

**49. Claim 46**

*Supra* Ground 1, claims 37, 39. MTK-1003, ¶161.

**50. Claim 47**

*Supra* Ground 1, claims 15, 39. MTK-1003, ¶162.

**51. Claim 48**

**(a) 48[p]**

*Supra* Ground 1, element 31[p]. MTK-1003, ¶163.

**(b) 48[a]**

*Supra* Ground 1, element 1[a]. MTK-1003, ¶164.

**(c) 48[b]**

*Supra* Ground 1, elements 1[b], 1[c]. MTK-1003, ¶165.

**(d) 48[c]**

*Supra* Ground 1, element 1[d]. MTK-1003, ¶166.

**52. Claim 49**

*Supra* Ground 1, claims 2, 48. MTK-1003, ¶167.

**53. Claim 50**

*Supra* Ground 1, claims 3, 49. MTK-1003, ¶168.

**54. Claim 51**

*Supra* Ground 1, claims 4, 49. MTK-1003, ¶169.

**55. Claim 52**

*Supra* Ground 1, claims 5, 48. MTK-1003, ¶170.

**56. Claim 53**

*Supra* Ground 1, claims 6, 52. MTK-1003, ¶171.

**57. Claim 54**

*Supra* Ground 1, claims 37, 48. MTK-1003, ¶172.

**58. Claim 55**

*Supra* Ground 1, claims 7, 48. MTK-1003, ¶173.

**59. Claim 56**

**(a) 56[p]**

*Supra* Ground 1, element 31[p]. MTK-1003, ¶174.

**(b) 56[a]**

*Supra* Ground 1, element 1[a]. MTK-1003, ¶175.

**(c) 56[b]**

*Supra* Ground 1, elements 1[b], 1[c]. MTK-1003, ¶176.

**(d) 56[c]**

*Supra* Ground 1, element 1[d]. MTK-1003, ¶177.

**60. Claim 57**

*Supra* Ground 1, claims 9, 56. MTK-1003, ¶178.

**61. Claim 58**

*Supra* Ground 1, claims 10, 57. MTK-1003, ¶179.

**62. Claim 59**

*Supra* Ground 1, claims 11, 57. MTK-1003, ¶180.

**63. Claim 60**

*Supra* Ground 1, claims 12, 56. MTK-1003, ¶181.

**64. Claim 61**

*Supra* Ground 1, claims 13, 56. MTK-1003, ¶182.

**65. Claim 62**

*Supra* Ground 1, claims 14, 61. MTK-1003, ¶183.

**66. Claim 63**

*Supra* Ground 1, claims 37, 56. MTK-1003, ¶184.

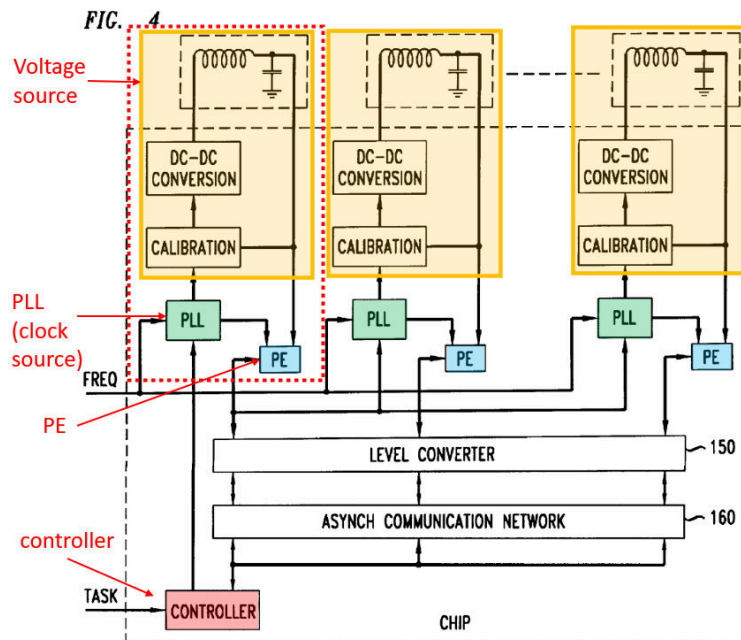
**67. Claim 64**

*Supra* Ground 1, claims 15, 56. MTK-1003, ¶185.

**B. GROUND 2—Claims 1-64 are obvious over Nicol and Borkar**

**1. Overview of Nicol**

Nicol discloses a dynamic load-balancing mechanism in a multiprocessor chip which divides tasks among multiple processors (or “processing elements,” “PEs”), and then adjusts the frequency and voltage of those processors to minimize power consumption. MTK-1008, Abstract; MTK-1003, ¶¶187-189. Nicol explains that there are “tasks that cannot be partitioned into concurrent evenly-loaded threads and, therefore, some PE within the multiprocessor would require a higher operating frequency and a higher operating voltage.” MTK-1008, 5:60-65; MTK-1003, ¶190. To address this limitation, Figure 4 shows each PE with its own associated clock source and voltage source to allow “the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.” MTK-1008, 5:66-6:3, Fig. 4; MTK-1003, ¶¶190-191.



MTK-1008, Fig. 4.

## 2. Overview of Borkar

*Supra* Ground 1, Overview of Borkar. MTK-1003, ¶192.

## 3. Nicol-Borkar Combination

A POSITA would have been motivated to modify Nicol's integrated circuit to incorporate the teachings of Borkar with reasonable expectation of success. Nicol and Borkar are in the same field of endeavor: power management on an integrated circuit. MTK-1008, 2:18-22 ("Improved performance of multi-processor chips is achieved by dynamically controlling the processing load of chips...as to minimize overall power consumption."); MTK-1006, 2:49-57 ("involves changing body bias signals ... clock frequency signals and supply voltages to at least partially control a parameter. A parameter of the integrated

circuit is a characteristic of the integrated circuit which can vary during performance including temperature, power consumption, and performance.”); MTK-1003, ¶194.

Further, Nicol and Borkar address the same known problem, the need to balance performance with power consumption in electronic systems. MTK-1008, 2:65-3:9 (discussing how power consumption and performance should match the load in order to save power); MTK-1006, 1:20-21 (“The performance, power consumption, and temperature [of an integrated circuit] are typically related.”), 5:45-46 (“The user may specify certain power conditions or a power versus performance tradeoff.”); MTK-1003, ¶195. Both Nicol and Borkar address that problem by the identified, predictable solution of using distinct units on an integrated circuit whose power can be independently controlled. MTK-1008, 5:66-6:2 (describing a plurality of processing elements (PEs) whose power can be independently controlled), Fig. 4 (depicting same); MTK-1006, 10:34-39 (“The first and second groups of transistors may be different function unit blocks (FUBS) on the same chip. Because of transistor parameter variations, certain performance and/or power parameters of first domain 234 may be different than that of the second domain 238.”); MTK-1003, ¶196. Both Nicol and Borkar also suggest the solution of dynamically controlling power parameters, such as frequency and voltage, of the units in response to changing needs and operations. MTK-1008,

4:64-66 (“The reduced load permits lowering the clock frequency to 100 MHz and lowering the supply voltage to 2.1V.”); MTK-1006, 5:25-29 (“In some embodiments, when the battery level signal is below a certain level, the supply voltage is lowered, the frequency of a processor clock is lowered, and/or the bias signals are changed to raise the threshold voltages of some or all of the transistors.”); MTK-1003, ¶196.

The similarities across Nicol and Borkar’s disclosures would have led a POSITA to incorporate Borkar’s teachings in Nicol’s dynamic power management. MTK-1003, ¶197. For example, Nicol discusses the need to adjust to temperature variations “to achieve high performance at varying operating temperatures and process corners.” MTK-1008, 1:41-44, 1:65-67. A POSITA would have understood that the discussion of temperature variation is closely related to the need to monitor power consumption because, as Borkar teaches, “performance, power consumption, and temperature are typically related.” MTK-1006, 1:19-20; MTK-1003, ¶197. A POSITA would have understood that Borkar’s power consumption monitoring mechanism would provide an additional check on the adverse effects of high power consumption (which causes high temperature) that Nicol discusses. MTK-1003, ¶197.

**4. Claim 1**

**(a) 1[p]**

To the extent the preamble is limiting, the Nicol-Borkar combination discloses an integrated circuit. Nicol discloses improving performance of multi-processor chips. MTK-1008, Abstract, 2:18-22. The “chip” refers to an integrated circuit, while “multi-processor” refers to multiple processors, or processing elements (PEs), on the integrated circuit. MTK-1008, 6:6-9 (“As shown in FIG. 4, all of the controllers are embodied in a single controller 200, which may be just another *processing element* of the *integrated circuit* that contains the other processing elements.”), cl. 5 (“The method of claim 1, wherein said steps are executed in a *multiprocessor integrated circuit*.”), Figs. 2, 4; MTK-1003, ¶198. Borkar also discloses managing power on an integrated circuit. MTK-1006, 2:49-60 (“The invention involves changing body bias signals applied to transistors *in an integrated circuit* in response to changing conditions to at least partially control a parameter of the *integrated circuit*....”), 4:5-9; MTK-1003, ¶199.

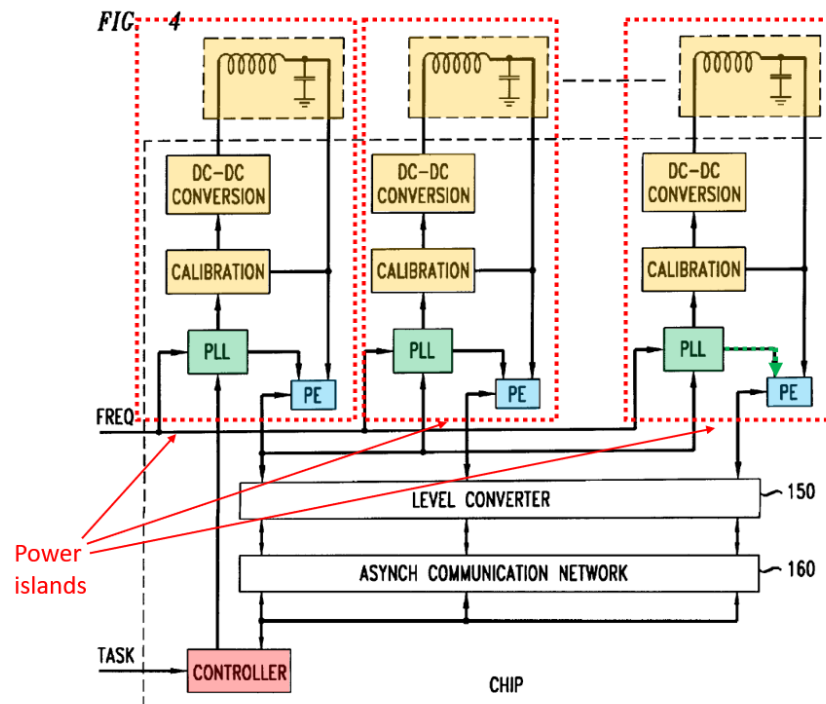
**(b) 1[a]**

The Nicol-Borkar combination discloses an integrated circuit chip. *See* MTK-1008, Abstract, 2:18-22 (“Improved performance of *multi-processor chips* is achieved by dynamically controlling the processing load of chips . . . .”), 6:6-9, Figs. 2, 4, cl. 5; MTK-1006, 2:49-60 (“The invention involves changing body bias

signals applied to transistors in an *integrated circuit*...”), 4:5-9; MTK-1003, ¶200.

**(c) 1[b]**

The Nicol-Borkar combination renders obvious a plurality of power islands disposed on the integrated circuit chip having associated power consumptions, each of the power consumptions being independently controllable by changing a supply voltage and operating frequency. The ’885 patent defines “power island” as “any section, delineation, partition, or division of the integrated circuit [] where power consumption is controlled within the section, delineation, partition, or division.” MTK-1001, 3:56-59. In the embodiment shown in Figure 4 of Nicol, “[a] separate power supply for each PE in a chip...[allows] the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.” MTK-1008, 5:66-6:2, Fig. 4. Thus, a POSITA would have understood and found obvious that Nicol’s plurality of processing elements is a plurality of power islands, each with a power consumption that is independently controllable by changing supply voltage and frequency. MTK-1003, ¶¶202-203.



MTK-1008, Fig. 4.

To the extent it is argued that Nicol does not explicitly disclose a plurality of power islands, Borkar also discloses and renders obvious a plurality of power islands, each with a power consumption independently controllable by changing a supply voltage and operating frequency. For example, Borkar discloses multiple “domains,” or groups of transistors, which have distinct power parameters. MTK-1006, 9:48-52, 9:58-59, 10:34-36. Body bias, supply voltage, and clock frequency of the each domain can be controlled individually. MTK-1006, 10:24-29.

Exemplary embodiments are shown in Figures 5 and 7. Accordingly, a POSITA would have understood and found obvious that Borkar's domains are a plurality of power islands, each with a power consumption that is independently controllable

by changing supply voltage and frequency. MTK-1003, ¶¶204-205.

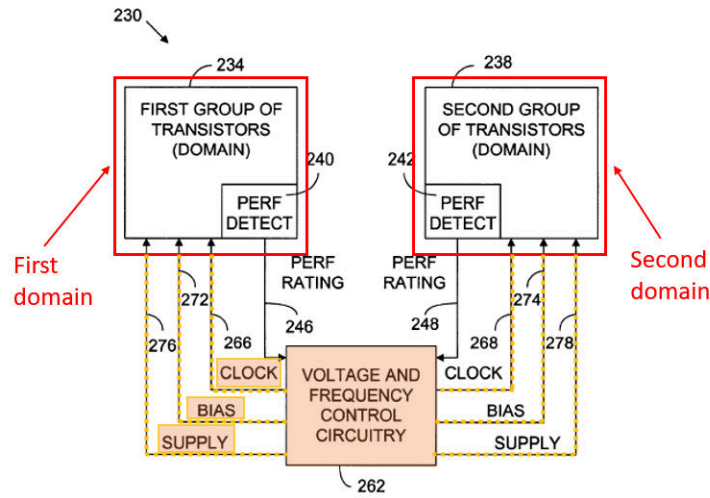


FIG. 5

MTK-1006, Fig. 5.

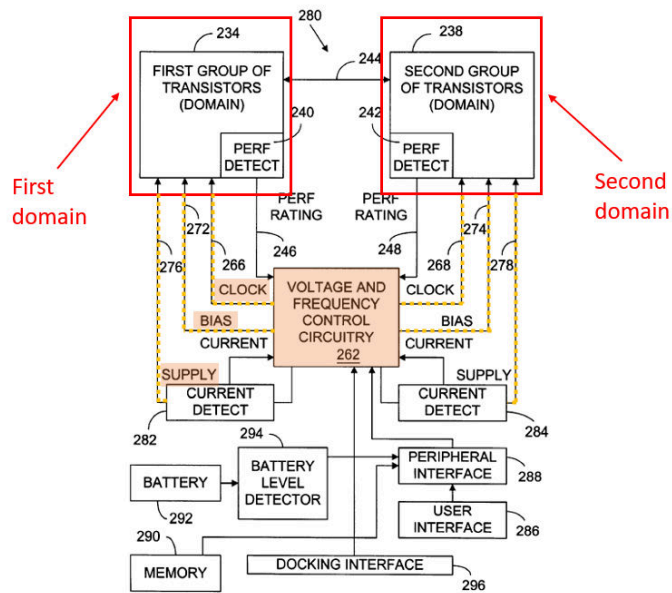


FIG. 7

MTK-1006, Fig. 7.

(d) 1[c]

In the combination, Borkar discloses one or more power consumption

signals indicating one or more of the power consumptions. Nicol discusses the need to adjust to temperature variations “to achieve high performance at varying operating temperatures and process corners.” MTK-1008, 1:41-44, 1:65-67. A POSITA would have been motivated to implement Borkar’s power consumption monitoring mechanism, which provides a check on the adverse effects of high power consumption (which causes high temperature) that Nicol discusses. MTK-1003, ¶207. Borkar discloses that its control circuitry “changes the body bias, supply voltage, and/or clock settings to at least partially to control one or more parameters of processor[.]” MTK-1006, 4:3-5. Control circuitry “may *consider the current signal (which when multiplied by the supply voltage indicates the active power consumption)* in deciding how to control the settings.” MTK-1006, 4:64-67. Borkar explains that “detect[ing] current being consumed” is a precise way of tracking power consumption levels. MTK-1006, 13:6-7; MTK-1003, ¶208. “The process of selecting the body bias, supply voltage, and/or clock settings in control circuitry 114 and 144 may be iterative process involving feedback from signals indicative of levels of the parameters (such as temperature and current) and others [*sic*] signals indicating preferences (such a battery level signals and user selections).” MTK-1006, 6:48-53; MTK-1003, ¶209. Figure 4 of Borkar shows this current detection in an embodiment with a single processor, while Figure 7 shows current detection for multiple domains. MTK-1006, 13:8-11; MTK-1003,

¶209.

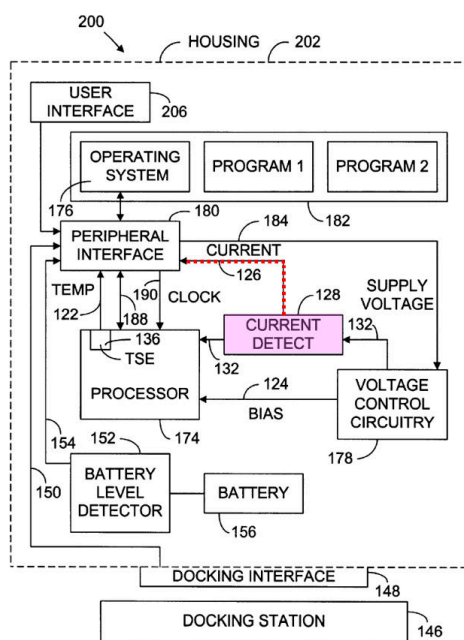


FIG. 4

MTK-1006, Fig. 4.

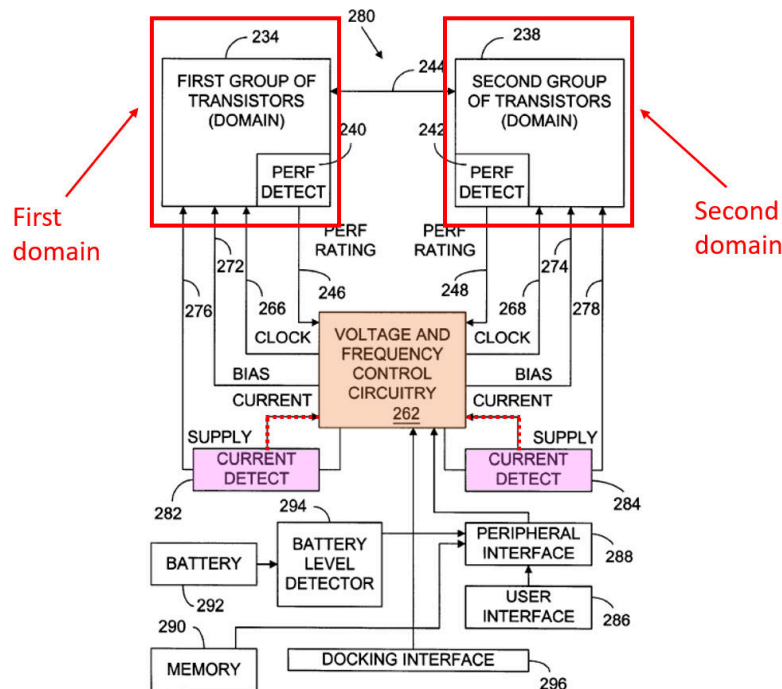


FIG. 7

MTK-1006, Fig. 7.

While the '885 patent does not define “power consumption signal,” it defines “power consumption level” as “any information, data, or statistic that indicate the power consumed in a power island...Some examples of power consumption levels are temperature and power.” MTK-1001, A POSITA would have understood that Borkar’s current information is a “power consumption signal” because the current information is used to calculate, and therefore indicates, power consumption. MTK-1006, 13:6-7, 4:64-66 (“Control circuitry 118 may consider the current signal (which when multiplied by the supply voltage indicates the active power consumption) in deciding how to control the settings.”); MTK-1003, ¶210.

Borkar also discloses monitoring temperature signals, which the '885 patent includes as an example of "power consumption level." MTK-1001, 6:49-50.

Borkar's Figure 1 (as well as Figures 2-4) depict a temperature sensitive element (TSE) on the processor which sends out a temperature signal to the voltage and frequency control circuitry or peripheral interface. MTK-1006, Figs. 1-4. Borkar explains that "control circuitry 118 monitors a temperature signal on conductor(s) 122. The temperature signals is related to the temperature of processor 136. A temperature sensitive element (TSE) 136, such as a diode, may be used in connection with a circuit to provide the temperature signal." MTK-1006, 4:13-14; *see also* MTK-1006, 4:14-46, 6:48-53 ("The process of selecting the body bias, supply voltage, and/or clock settings in control circuitry 114 and 144 may be iterative process involving feedback from signals indicative of levels of the parameters (such as temperature and current) and others signals indicating preference (such a battery level signals and user selections)."), Figs. 1-4; MTK-1003, ¶¶211-212.

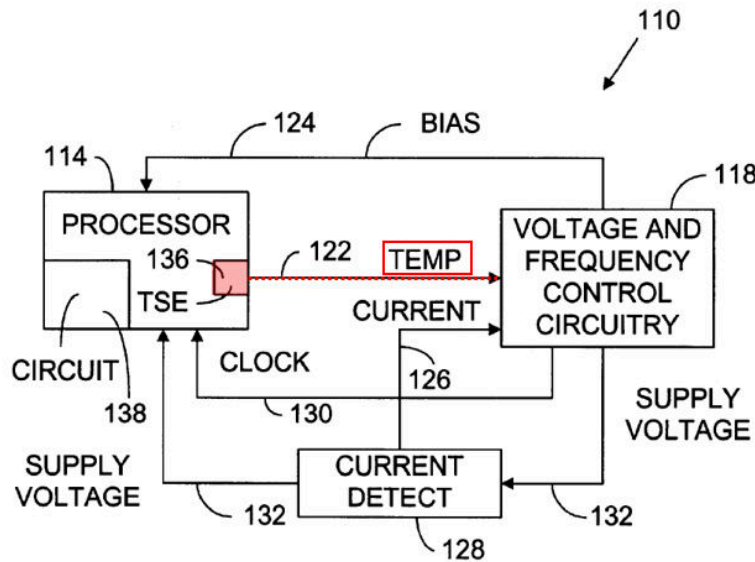


**FIG. 1**

MTK-1006, Fig. 1.

On “power consumption signals indicating one or more of the power consumptions,” Petitioner notes that in a prior litigation involving the ’885 patent, the court construed the term to have its plain meaning, but clarified that the power consumption signal is associated with a particular power island rather than multiple power islands or an entire chip. MTK-1012 at 36. For purposes of this Petition, Petitioner submits that there is no construction necessary because the plain and ordinary meaning suffices. MTK-1003, ¶213. However, the Nicol-Borkar combination also renders this element obvious under the prior court’s clarification because Borkar’s power consumption signals (current signals and temperature signals) are indicative of the state of the power island (processor or domain), not of multiple power islands or an entire chip. MTK-1003, ¶213.

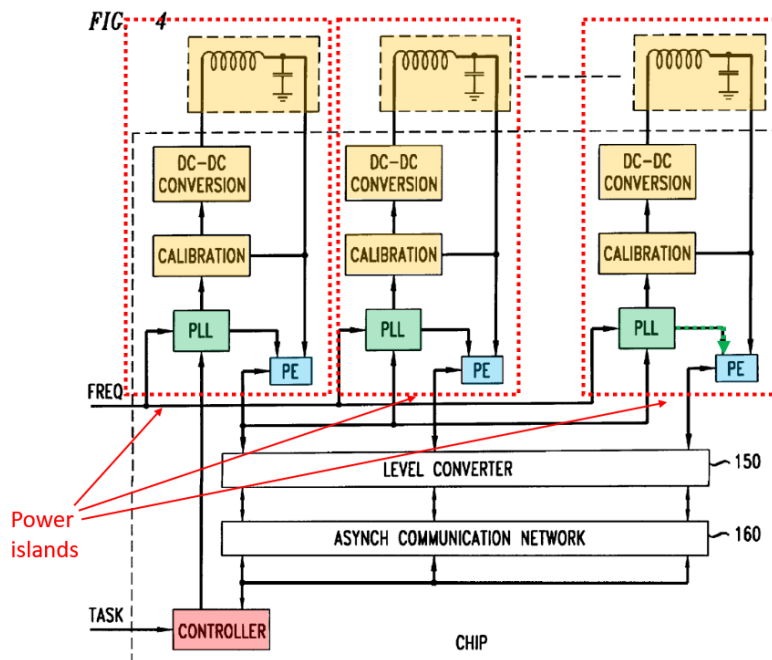
(e) 1[d]

The Nicol-Borkar combination renders obvious a power management processor disposed on the integrated circuit chip and coupled to each of the power islands configured to monitor the one or more power consumption signals, the power management processor being dedicated to execute power management software to individually control each of the power consumptions, and the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request.

First, a POSITA would have understood Nicol's "controller" PE (or "PE 200") to be a power management processor. The controller PE "allocates tasks to the other PEs" and "consider[s] the PE with the tasks that require the most time to carry out, and adjust[s] the clock frequency to insure that the most heavily loaded PE carries out its assigned tasks within the required completion time. Once the frequency is thus determined, a minimum supply voltage can be determined." MTK-1008, 2:53-54, 3:66-4:10; *see also* MTK-1008, 5:23-28, 6:6-13. Further, the name "processing element" implies that the controller PE is a processor. MTK-1008, 6:6-13 ("As shown in FIG. 4, all of the controllers are embodied in a single controller 200, which may be just another *processing element* of the integrated circuit that contains the other processing elements."). MTK-1003, ¶215.

Second, a POSITA would have understood that Borkar's "voltage and

frequency control circuitry” was a power management processor and/or would be integrated into Nicol’s “controller” PE, as the two perform the similar function of controlling power consumption of the power islands. MTK-1008, MTK-1008, 2:53-54, 3:66-4:10, 6:6-9; MTK-1006, 2:61-65; MTK-1003, ¶216. Further, a POSITA would have understood and found obvious that the Nicol-Borkar power management processor is coupled to each of the power islands because such a connection is necessary for controlling the power behavior of the power islands. Indeed, Nicol’s Figure 4 shows such coupling, as the controller is connected to each of the PEs to provide the task allocation, frequency and voltage control signals.



MTK-1008, Fig. 4.

Borkar’s Figures 5 and 7 also show such coupling of the power management

processor to the power islands through conductors. MTK-1006, 11:22-27, 11:40-43, 11:55-58; MTK-1003, ¶217.

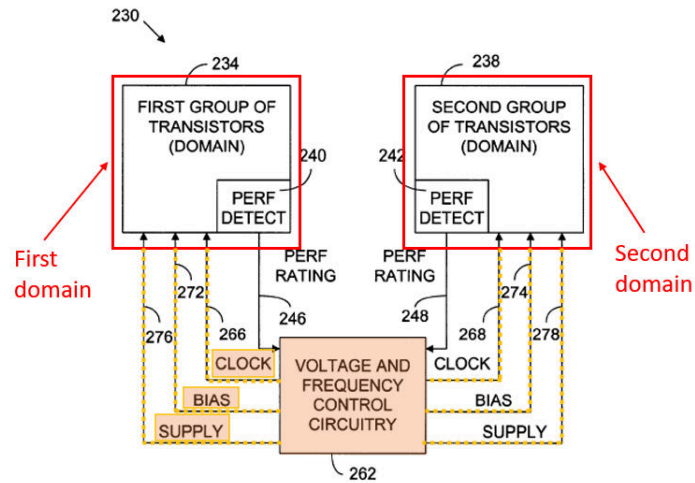


FIG. 5

MTK-1006, Fig. 5.

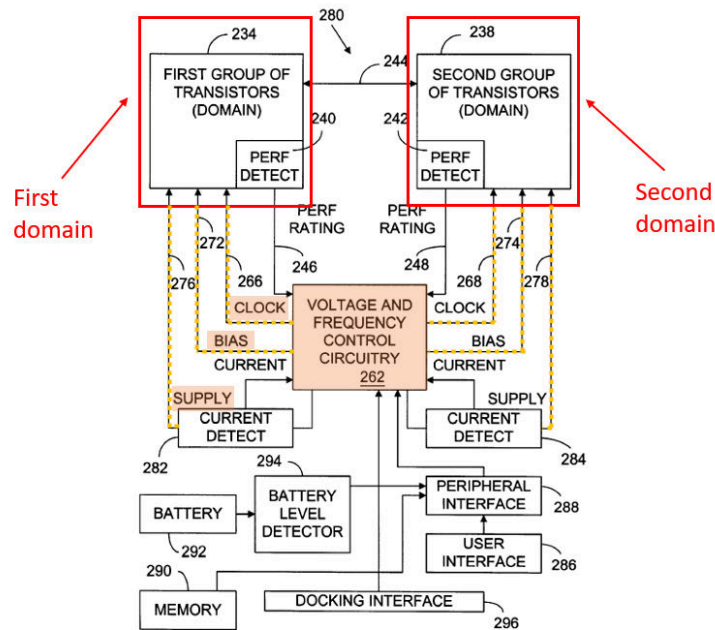


FIG. 7

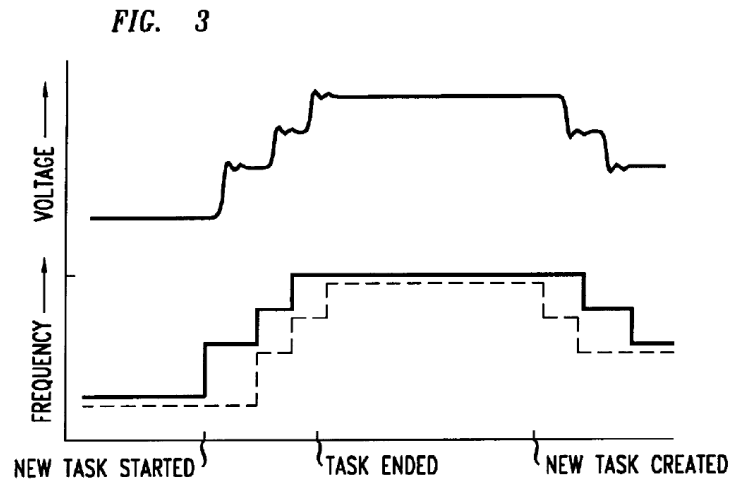
MTK-1006, Fig. 7.

The Nicol-Borkar combination renders obvious that the power management processor is configured to monitor one or more power consumption signals. As discussed for 1[c], incorporated herein, Borkar discloses “current detection circuitry” which provide current signals to “voltage and frequency control circuitry.” MTK-1006, 4:58-60, 7:39-42, 13:8-11, Figs. 1-2, 4, 7; MTK-1003, ¶218. Borkar’s control circuitry “*may consider the current signal (which when multiplied by the supply voltage indicates the active power consumption)* in deciding how to control the settings.” MTK-1006, 4:64-67. Borkar also discloses monitoring temperature signals, as discussed for 1[c], incorporated herein. MTK-1006, 4:12-46, 6:48-53; MTK-1003, ¶218.

The Nicol-Borkar combination also renders obvious the power management

processor being dedicated to execute power management software to individually control each of the power consumptions. A POSITA would have understood Nicol's controller PE and Borkar's control circuitry to be dedicated to execute the power management software because their whole described purpose is to manage the power of the power islands via executing power management software. MTK-1004, 1442 ("The on-chip supervisor controls the external DC/DC converter, which provides the logic supply."), 1442 ("the supervisor requests changes to the logic supply and requests shutdown of the logic supply during hibernation."), 1446 ("The on-chip clock and power supervisor, in response to software commands and timeout and interrupt events, manages the clocks, internal state and external power supply to control the standby power."), 1446 ("Under software control, both the voltage and the frequency of the processor can be modified, thereby allowing the performance demands of the application to be met while minimizing the dynamic power consumption."); MTK-1006, 1:63-65 ("[T]he control circuitry controls the setting responsive to processor signal resulting for execution of software."), 4:3-5 ("Control circuitry 118 changes the body bias, supply voltage, and/or clock settings to at least partially to control one or more parameters of processor 114."), 1:60-2:3, 4:20-33, 4:64-67, 5:20-24, 5:45-52, 5:59-64, 6:1-7, 6:12-13, 6:26-53, Figs. 1-5, 7; MTK-1003, ¶219. Further, as discussed for 1[b], the Nicol-Borkar combination renders obvious individual control of power islands' power consumptions.

The Nicol-Borkar combination renders obvious the power management processor being configured to change power consumption in at least one of the power islands in response to a power consumption change request. Nicol's operating system "independently program[s] the lowest operating frequency and corresponding lowest supply voltage for each PE." MTK-1008, 5:66-6:2. Nicol further describes the timing of changing frequency and voltage to the appropriate frequency and/or voltage to match the load when a task is being started and when the task has completed. MTK-1008, 4:54-66, 5:23-29, Fig. 3. A POSITA would have found obvious from this disclosure that there is a corresponding power consumption change request associated with each of the times that a new task starts, such that operating frequency and voltage must be stepped up, and when the task ends, such that frequency and voltage can be stepped down. MTK-1003, ¶¶220-221.



MTK-1008, Fig. 3.

Additionally, Borkar also renders this limitation obvious. Borkar's control circuitry also "changes the body bias, supply voltage, and/or clock settings to at least partially to [sic] control one or more parameters of processor 114," disclosing "power management processor being dedicated to execute power management software to individually control each of the power consumptions." MTK-1006, 4:3-5, 4:64-67 ("System 170 may operate the same as system 110 of FIG. 1 with respect to the body bias, supply voltage, and/or clock settings *in response to* changes in temperature and power consumption. System 200 may operate the same described above in connection with system 140 of FIG. 2 with respect to the body bias, supply voltage, and/or clock settings *in response input signals* reflecting changes in temperature, power consumption, user settings, battery level signals, and docking station interface conditions."), 11:25-67, 13:28-30 ("These components can provides [sic] input signals that are considered by control circuitry

262 in deciding power constraints.”); MTK-1003, ¶222. Therefore, it would have been obvious to a POSITA that the Nicol-Borkar power management processor changes power consumption in a power island in response to a power consumption change request.

## **5. Claim 2**

The Nicol-Borkar combination renders obvious wherein the power management software is embedded firmware in the integrated circuit. A POSITA would have understood and found it obvious that Nicol’s “operating system” was embedded firmware because it resides in the “controller” PE and controls the hardware circuitry that changes parameters such as voltage and frequency of the PEs. MTK-1008, 2:22-27 (“A controller in a multi-processor chip allocates tasks to the individual processors to equalize processing load among the chips, then the controller lowers the clock frequency...and finally reduces the supply voltage.”), 4:11-13 (“As indicated above, the operating system can reduce the supply voltage even further by tracking temperature and process variations.”), Fig. 4; MTK-1001, 4:62-5:2, Fig. 2; MTK-1003, ¶223.

To the extent it is argued that Nicol’s “operating system” is not embedded firmware, a POSITA would have understood and found it obvious that the power management software in Borkar was also firmware embedded in the voltage and frequency control circuitry. MTK-1006, 7:61-65 (“However, in system 170 and

200, these the determination of the settings may occur by circuitry in peripheral interface 180 in response to software control of operating system 176 and/or a program, rather than *in hardware as in control circuitry 118 and 144.*”), 4:3-5 (“Control circuitry 118 changes the body bias, supply voltage, and/or clock settings to at least partially to control one or more parameters of processor 114.”), 1:60-2:3, 4:64-67, 5:20-24, 5:47-52, 5:59-64, 6:1-7, 6:12-13, 6:31-43 (discussing control circuitry changing power settings), 7:61-65 (“[T]he determination of the settings may occur by circuitry in peripheral interface 180 in response to software control of operating system 176 and/or a program, rather than in hardware as in control circuitry 118 and 144.”), Figs. 1, 2, 5, 7; MTK-1003, ¶224. A POSITA would have been motivated to combine Nicol and Borkar for the reasons previously explained. *Supra*, Section III.B.3; MTK-1003, ¶224.

## **6. Claim 3**

The Nicol-Borkar combination renders obvious wherein one or more of the power consumptions is changed by selecting a non-zero supply voltage, stopping a clock and selecting one of plural threshold voltages of variable threshold transistors. Nicol discloses programming the “corresponding lowest supply voltage” for a PE based on the operating frequency. MTK-1008, 5:67-6:2; MTK-1003, ¶225. Nicol also discloses “gated clocking techniques to ‘shut down’ PEs that are not needed.” MTK-1008, 5:42-44; MTK-1003, ¶227. Nicol also discloses

existing techniques in the art “tuning the threshold voltages” to “ensure that the leakage current...does not become too large,” which would motivate a POSITA to implement tuning the threshold voltages, either in light of Nicol alone, or in view of Borkar. MTK-1008, 2:3-10; MTK-1003, ¶228.

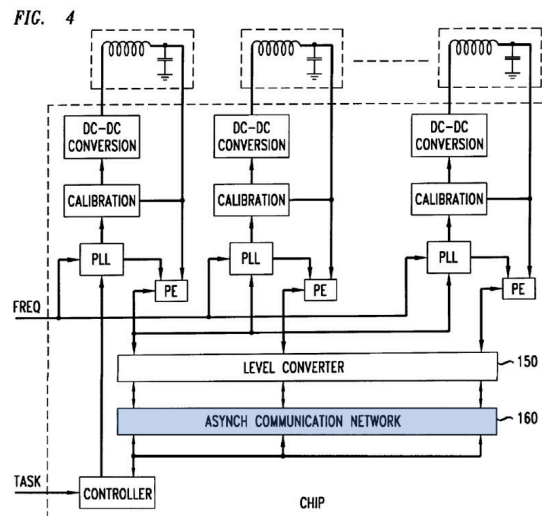
To the extent it is argued Nicol does not explicitly disclose selecting a threshold voltage to change power consumption, Borkar provides selecting a threshold voltage of variable threshold transistors. MTK-1006, 4:26-28 (“For example...body bias signals [may be] changed so that the threshold voltage is raised.”); *see also* MTK-1006, 3:46-57, 4:28-32, 5:25-34, 5:55-64, 6:23-25, 6:31-40, 9:35-39, 12:39-42; MTK-1003, ¶229.

Borkar also discloses that “control circuitry changes...supply voltage...to control one or more parameters of processor 114.” MTK-1006, 4:3-5; *see also* MTK-1006, 4:21-32, 5:25-6:7, 6:41-53, 11:20-21, 11:55-67, 12:39-45, 13:35-37, 13:57-60, Figs. 1, 2, 5, 7; MTK-1003, ¶226. A POSITA would have been motivated to combine Nicol and Borkar for the reasons previously explained. *Supra*, Section III.B.3; MTK-1003, ¶229.

## **7. Claim 4**

The Nicol-Borkar combination renders obvious wherein a first of the power islands is capable of communicating synchronously and asynchronously with a second of the power islands. Nicol discloses asynchronous communication

between its PEs, which can operate at different frequencies. MTK-1008, 6:14-21; MTK-1003, ¶230. “[E]ach PE within the FIG. 4 arrangement is connection [sic] to an arrangement comprising elements 150. Level converter 150 converts the variable voltage swings of the PEs to a fixed level swing, and network 160 resolves the issue of different clock domains.” See MTK-1008, 6:29-33, Fig. 4. A POSITA would have understood that the PEs are communicating asynchronously because they are operating at different frequencies and voltages, necessitating the level converter and asynchronous communication network. MTK-1003, ¶230.



MTK-1008, Fig. 4.

To the extent it is argued that Nicol does not render obvious this claim, Borkar discloses and renders obvious this claim. Borkar discloses that some domains “may run off the same clock signal or otherwise need to run synchronously.” MTK-1006, 10:6-7. A POSITA would have understood and found it obvious that Borkar’s domains, or FUBs, can communicate synchronously

or asynchronously. MTK-1006, 10:6-18 (discussing that domains may “run off the same clock or that have to run synchronously” or may “run off a different clock signal or that are asynchronous.”); MTK-1003, ¶231. Therefore, a POSITA would have understood, and found it obvious, that a power island in the Nicol-Borkar combination is capable of communicating synchronously and asynchronously with a second power island.

On the terms “synchronously” and “asynchronously,” Petitioner notes that in a prior litigation involving a related patent, U.S. Patent No. 7,996,811, the court construed the term “synchronously” as “with coordination between components (i.e., power islands) before communication transmission begins,” “asynchronously” as “without coordination between components (i.e., power islands) before transmission begins.” MTK-1011 at 45. For purposes of this Petition, Petitioner submits that there is no construction necessary because the plain and ordinary meaning suffices. MTK-1003, ¶232. However, the Nicol-Borkar combination also renders this element obvious under the prior court’s construction because both Nicol and Borkar describe domains that run off the same clock signal (with coordination between components before transmission begins) and run off differeng clock signals (without coordination between components before transmission begins). MTK-1003, ¶232.

**8. Claim 5**

The Nicol-Borkar combination renders obvious wherein each of the power consumptions is further controlled by stopping a clock. Nicol discloses “gated clocking techniques to ‘shut down’ PEs that are not needed.” MTK-1008, 5:42-44; MTK-1003, ¶233. Similarly, Borkar discloses a “clock signal producing circuitry” which “provides one or more clock signals,” which a POSITA would understand to enable stopping, or turning off, the clock signal. MTK-1006, 13:61-63, Fig. 9; MTK-1003, ¶234.

**9. Claim 6**

The Nicol-Borkar combination renders obvious wherein stopping the clock comprises clock gating. Nicol discloses “gated clocking techniques to ‘shut down’ PEs that are not needed.” MTK-1008, 5:42-44; MTK-1003, ¶235.

**10. Claim 7**

The Nicol-Borkar combination renders obvious wherein the one or more power consumption signals include temperature or power dissipation measurement. As discussed in 1[c], incorporated herein, the Nicol-Borkar combination discloses and renders obvious power consumption signals including temperature measurements. *Supra* Ground 1, element 1[c]; MTK-1003, ¶236.

**11. Claim 8**

**(a) 8[p]**

*Supra* Ground 2, 1[p]. MTK-1003, ¶237.

**(b) 8[a]**

*Supra* Ground 2, 1[a]. MTK-1003, ¶238.

**(c) 8[b]**

*Supra* Ground 2, 1[b]. MTK-1003, ¶239.

**(d) 8[c]**

*Supra* Ground 2, 1[c]. MTK-1003, ¶240.

**(e) 8[d]**

*Supra* Ground 2, 1[d]. MTK-1003, ¶241. For the same reasons explained regarding “power management processor” for 1[d], incorporated herein, a POSITA would have understood the Nicol’s controller PE combined with Borkar’s “control circuitry” to be a “power manager.”

**12. Claim 9**

The Nicol-Borkar combination discloses a processor configured to execute power management software to individually control each of the power consumptions. As discussed for 1[d], incorporated herein, a POSITA would have understood the Nicol-Borkar “power management processor” to be a processor configured to execute power management software to individually control each of the power consumptions. *Supra* Ground 1, element 1[d]. MTK-1003, ¶242.

**13. Claim 10**

*Supra* Ground 2, claims 3, 9. MTK-1003, ¶243.

**14. Claim 11**

*Supra* Ground 2, claims 4, 9. MTK-1003, ¶244.

**15. Claim 12**

The Nicol-Borkar combination renders obvious wherein the power manager comprises a master power manager and a slave power manager associated with each of the power islands. A POSITA would have understood the Nicol-Borkar system's "controller" PE to be the master power manager because it oversees the power behavior of the entire integrated circuit. MTK-1001, 5:48-49; MTK-1008, 2:53-56, 3:10-21, 3:66-4:10, 5:23-28, 6:6-13 (discussing "controller" or "PE 200" that assigns tasks among the PEs and calculates required frequency and/or voltage); MTK-1006, 4:3-5, 11:22-35 (discussing "control circuitry" changing variables such as frequency and voltage for processor or domains); MTK-1003, ¶245. A POSITA would have understood the PLL and voltage circuitry associated with each PE in Nicol, and the control circuitry depicted in Borkar's Figure 9, to be a slave power manager because this circuitry controls the power behavior of the individual power island (PE or domain) that it is associated with. MTK-1001, 6:11-12; MTK-1008, 2:50-53, 6:3-6; MTK-1006, 13:57-14:2; MTK-1003, ¶247.

Further, Borkar discloses "control circuitry" that changes the body bias,

supply voltage, and/or clock settings of the processor or multiple domains. MTK-1006, 4:3-5, 11:22-67; MTK-1003, ¶246. A POSITA would have understood Borkar's control circuitry to be a "master" power manager because it controls the power behavior of multiple components on the chip. MTK-1003; ¶246. Further, the control circuitry depicted in Borkar's Figure 9 to controls the power behavior of each power domain or processor. MTK-1006, 4:3-5; MTK-1003, ¶248. Accordingly, a POSITA would have understood that circuitry to be a slave power manager. MTK-1001, 6:11-12; MTK-1003, ¶248.

**16. Claim 13**

*Supra* Ground 2, claims 5, 8. MTK-1003, ¶249.

**17. Claim 14**

*Supra* Ground 2, claims 6, 13. MTK-1003, ¶250.

**18. Claim 15**

*Supra* Ground 2, claims 7, 8. MTK-1003, ¶251.

**19. Claim 16**

**(a) 16[p]**

*Supra* Ground 2, element 1[p]. MTK-1003, ¶252.

**(b) 16[a]**

*Supra* Ground 2, element 1[a]. MTK-1003, ¶253.

**(c) 16[b]**

*Supra* Ground 2, elements 1[b], 1[c]. MTK-1003, ¶254.

**(d) 16[c]**

*Supra* Ground 2, element 1[d]. MTK-1003, ¶255.

**20. Claim 17**

*Supra* Ground 2, claims 2, 16. MTK-1003, ¶256.

**21. Claim 18**

*Supra* Ground 2, claims 3, 17. MTK-1003, ¶257.

**22. Claim 19**

*Supra* Ground 2, claims 4, 17. MTK-1003, ¶258.

**23. Claim 20**

*Supra* Ground 2, claims 5, 16. MTK-1003, ¶259.

**24. Claim 21**

*Supra* Ground 2, claims 6, 20. MTK-1003, ¶260.

**25. Claim 22**

*Supra* Ground 2, claims 7, 16. MTK-1003, ¶261.

**26. Claim 23**

**(a) 23[p]**

*Supra* Ground 2, element 1[p]. MTK-1003, ¶262.

**(b) 23[a]**

*Supra* Ground 2, element 1[a]. MTK-1003, ¶263.

**(c) 23[b]**

*Supra* Ground 2, elements 1[b], 1[c]. MTK-1003, ¶264.

**(d) 23[c]**

*Supra* Ground 2, element 1[d]. MTK-1003, ¶265.

**27. Claim 24**

*Supra* Ground 2, claims 9, 23. MTK-1003, ¶266.

**28. Claim 25**

*Supra* Ground 2, claims 10, 24. MTK-1003, ¶267.

**29. Claim 26**

*Supra* Ground 2, claims 11, 24. MTK-1003, ¶268.

**30. Claim 27**

*Supra* Ground 2, claims 12, 23. MTK-1003, ¶269.

**31. Claim 28**

*Supra* Ground 2, claims 13, 23. MTK-1003, ¶270.

**32. Claim 29**

*Supra* Ground 2, claims 14, 28. MTK-1003, ¶271.

**33. Claim 30**

*Supra* Ground 2, claims 15, 23. MTK-1003, ¶272.

**34. Claim 31**

**(a) 31[p]**

*Supra* Ground 2, element 1[p]. MTK-1003, ¶273. The Nicol-Borkar combination provides a system. “[Fig. 3] shows the **system** operating at 70 MHz from a 1.8V supply when the load is increased in three steps to 140 MHz.” MTK-

1008, 4:58-60. A POSITA would have also understood Borkar to disclose a system. MTK-1006, 1:59-60 (“In some embodiments, the invention includes a *system* having a processor and control circuitry.”), 2:13-36; MTK-1003, ¶273.

**(b) 31[a]**

*Supra* Ground 2, element 1[a]. MTK-1003, ¶274.

**(c) 31[b]**

*Supra* Ground 2, element 1[b]. MTK-1003, ¶275.

**(d) 31[c]**

*Supra* Ground 2, element 1[c]. MTK-1003, ¶276.

**(e) 31[d]**

*Supra* Ground 2, element 1[d]. MTK-1003, ¶277.

**35. Claim 32**

*Supra* Ground 2, claims 2, 31. MTK-1003, ¶278.

**36. Claim 33**

*Supra* Ground 2, claims 3, 32. MTK-1003, ¶279.

**37. Claim 34**

*Supra* Ground 2, claims 4, 32. MTK-1003, ¶280.

**38. Claim 35**

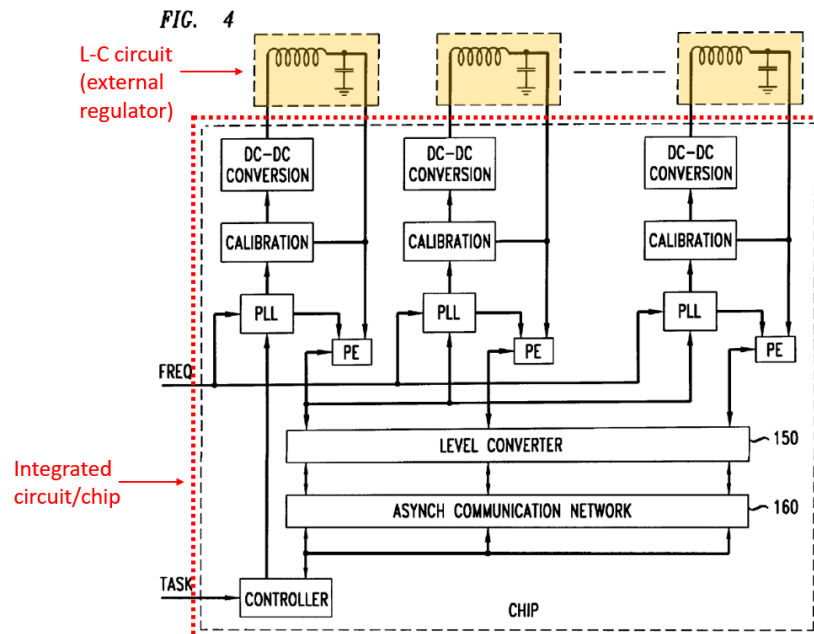
*Supra* Ground 2, claims 5, 31. MTK-1003, ¶281.

**39. Claim 36**

*Supra* Ground 2, claims 6, 35. MTK-1003, ¶282.

**40. Claim 37**

The Nicol-Borkar combination renders obvious wherein the system is configured to have the supply voltage provided by an external regulator. Nicol discloses that “there has been considerable interest in integrating much of the buck controller circuit onto the chip. The only off-chip components are the inductor [ ] and capacitor [ ] used in the buck converter.” MTK-1008, 1:56-60. Figure 4 illustrates such a divided buck controller circuit: the L-C circuit (inductor-capacitor) is external to the chip (delineated by the dotted line), while the calibration circuit and DC-DC conversion are internal to the chip. MTK-1008, 4:28-37, Fig. 4; MTK-1003, ¶283.



MTK-1008, Fig. 4.

A POSITA would have understood that Nicol's L-C circuit to be an

“external regulator” that provides the supply voltage. The plain meaning of the claim language requires that the regulator be “external” and provide the supply voltage, which the L-C circuit is and does. MTK-1008, 4:31-36 (“...to cause the combination of converter [] and L-C circuit [] to *create the supply voltage Vdd-local*, which is...applied to all of the PEs.”); MTK-1003, ¶284.

Additionally, Borkar discloses an external regulator that provides the supply voltage. While Figure 3 depicts the “voltage control circuitry” inside of the chip, Borkar also discloses that “Voltage control circuitry 178 may be on the same chip (e.g., chip 186) as is processor 174 *or on a different chip.*” MTK-1006, 7:5-7. When the control circuitry is on a different chip than the processor, it would necessarily be external to the chip that contains the processor, thus making it an external regulator. MTK-1003, ¶285.

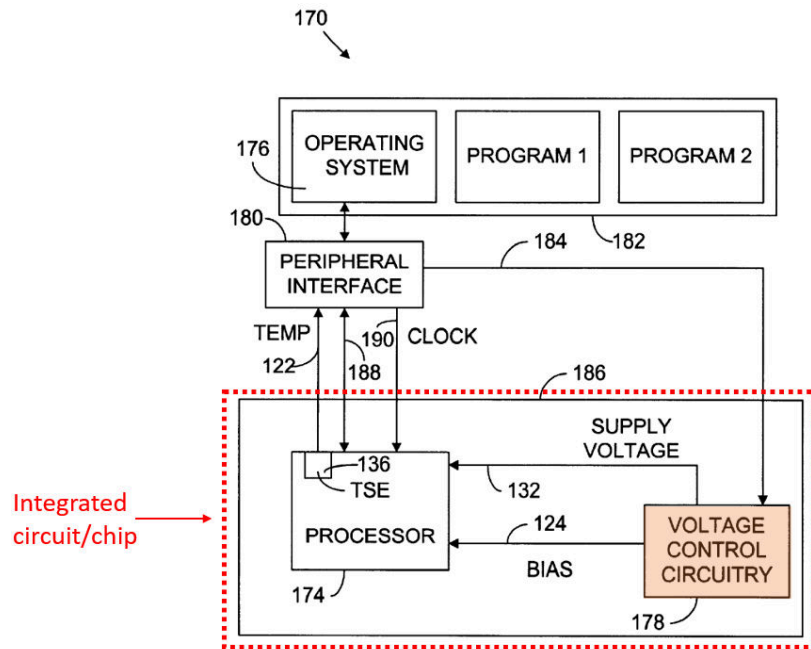


**FIG. 3**

MTK-1006, Fig. 3.

**41. Claim 38**

*Supra* Ground 2, claims 7, 31. MTK-1003, ¶286.

**42. Claim 39**

**(a) 39[p]**

*Supra* Ground 2, element 1[p]. MTK-1003, ¶287.

**(b) 39[a]**

*Supra* Ground 2, element 1[a]. MTK-1003, ¶288.

**(c) 39[b]**

*Supra* Ground 2, element 1[b]. MTK-1003, ¶289.

**(d) 39[c]**

*Supra* Ground 2, element 1[c]. MTK-1003, ¶290.

**(e) 39[d]**

*Supra* Ground 2, element 1[d]. MTK-1003, ¶291.

**43. Claim 40**

*Supra* Ground 2, claims 9, 39. MTK-1003, ¶292.

**44. Claim 41**

*Supra* Ground 2, claims 10, 40. MTK-1003, ¶293.

**45. Claim 42**

*Supra* Ground 2, claims 11, 40. MTK-1003, ¶294.

**46. Claim 43**

*Supra* Ground 2, claims 12, 39. MTK-1003, ¶295.

**47. Claim 44**

*Supra* Ground 2, claims 13, 39. MTK-1003, ¶296.

**48. Claim 45**

*Supra* Ground 2, claims 14, 44. MTK-1003, ¶297.

**49. Claim 46**

*Supra* Ground 2, claim 37, 39. MTK-1003, ¶298.

**50. Claim 47**

*Supra* Ground 2, claims 15, 39. MTK-1003, ¶299.

**51. Claim 48**

**(a) 48[p]**

*Supra* Ground 2, 31[p]. MTK-1003, ¶300.

**(b) 48[a]**

*Supra* Ground 2, 1[a]. MTK-1003, ¶301.

**(c) 48[b]**

*Supra* Ground 2, 1[b], 1[c]. MTK-1003, ¶302.

**(d) 48[c]**

*Supra* Ground 2, 1[d]. MTK-1003, ¶303.

**52. Claim 49**

*Supra* Ground 2, claims 2, 48. MTK-1003, ¶304.

**53. Claim 50**

*Supra* Ground 2, claims 3, 49. MTK-1003, ¶305.

**54. Claim 51**

*Supra* Ground 2, claims 4, 49. MTK-1003, ¶306.

**55. Claim 52**

*Supra* Ground 2, claims 5, 48. MTK-1003, ¶307.

**56. Claim 53**

*Supra* Ground 2, claims 6, 52. MTK-1003, ¶308.

**57. Claim 54**

*Supra* Ground 2, claims 37, 48. MTK-1003, ¶309.

**58. Claim 55**

*Supra* Ground 2, claims 7, 48. MTK-1003, ¶310.

**59. Claim 56**

**(a) 56[p]**

*Supra* Ground 2, 1[p]. MTK-1003, ¶311.

**(b) 56[a]**

*Supra* Ground 2, 1[a]. MTK-1003, ¶312.

**(c) 56[b]**

*Supra* Ground 2, 1[b], 1[c]. MTK-1003, ¶313.

**(d) 56[c]**

*Supra* Ground 2, 1[d]. MTK-1003, ¶314.

**60. Claim 57**

*Supra* Ground 2, claims 9, 56. MTK-1003, ¶315.

**61. Claim 58**

*Supra* Ground 2, claims 10, 57. MTK-1003, ¶316.

**62. Claim 59**

*Supra* Ground 2, claims 11, 57. MTK-1003, ¶317.

**63. Claim 60**

*Supra* Ground 2, claims 12, 56. MTK-1003, ¶318.

**64. Claim 61**

*Supra* Ground 2, claims 13, 56. MTK-1003, ¶319.

**65. Claim 62**

*Supra* Ground 2, claims 14, 61. MTK-1003, ¶320.

**66. Claim 63**

*Supra* Ground 1, claims 37, 56. MTK-1003, ¶321.

**67. Claim 64**

*Supra* Ground 2, claims 15, 56. MTK-1003, ¶322.

**IV. THE BOARD SHOULD CONSIDER THE PETITION ON THE MERITS AND NOT EXERCISE ITS DISCRETION TO DENY INSTITUTION**

**A. Discretionary denial under §325(d) is not warranted**

*Advanced Bionics* and the *Becton* factors strongly favor institution.

*Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential); *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential as to Section III.C.5, first paragraph).

***Advanced Bionics Part 1***— This Petition presents new prior art and arguments for which there is no indication in the file history that the Office ever previously considered in connection with the '885 patent. While Nowka (MTK-1004) appears on the face of the '885 patent, the Examiner never substantively addressed it during prosecution. MTK-1002, 199-203. Indeed, the Examiner never issued a rejection over any prior art reference. Furthermore, Nowka was never considered in combination with Borkar (MTK-1006), which was not before the Examiner during prosecution.

The '885 patent's prosecution did not involve negotiation between the applicant and the Examiner regarding the teachings of the prior art applied in the instant Petition, thus, exercise of the Board's discretion under § 325(d) is unwarranted. *See* IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential) (citing IPR2017-01586 Pap. 8 (PTAB Dec. 15, 2017) (precedential)).

**B. Discretionary Denial under Section 314(a) Is Not Warranted**

Given this is the first ever petition to be filed against the '885 Patent, the *General Plastic* factors do not apply. *General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357—01361, Paper 19 (PTAB Sept. 6, 2017) (precedential)

**C. The *Fintiv* Factors Weigh Against Exercising Discretion To Deny Institution**

The PTAB considers a set of non-exclusive factors (the *Fintiv* factors) in determining whether to institute an IPR proceeding where there is parallel district court litigation. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (designated precedential May 5, 2020). On June 21, 2022, Director Vidal issued “binding agency guidance” entitled “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation.” MTK-1013 (hereinafter the “Interim Guidance”). This Interim Guidance presents “several clarifications... to the PTAB’s... application of *Fintiv*

to discretionary institution where there is parallel litigation.” *Id.*, 2.

One clarification provided by the Interim Guidance specifies the effect of particular types of stipulations presented by petitioners on the Board’s application of the *Fintiv* framework. *Id.*, 3, 7-8. In particular, the Interim Guidance unequivocally states that “***the PTAB will not discretionarily deny institution*** of an IPR or PGR in view of parallel district court litigation where a petitioner stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition.” *Id.*, 7 (emphasis added) (citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020)). In the present case, Petitioner presents a stipulation not to pursue in the parallel district court proceeding the same grounds as in the present Petition or any grounds that could have reasonably been raised in the present Petition. *See* MTK-1014. Accordingly, based on the Interim Guidance, institution of the present Petition ***should not*** be discretionarily denied in view of the parallel district court proceeding. *See* MTK-1013, 7.

## V. CONCLUSION

As demonstrated herein, the Challenged Claims are unpatentable. Accordingly, Petitioner respectfully requests that the Board institute IPR.

## VI. PAYMENT OF FEES

Petitioner authorizes charge of fees to Deposit Account 06-1050.

**VII. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)**

**A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)**

MediaTek Inc. is the Petitioner and real party-in-interest. MediaTek USA Inc. is an additional real party-in-interest. No other parties had access to or control over the present Petition, and no other parties funded the present Petition.

**B. Related Matters Under 37 C.F.R. § 42.8(b)(2)**

Petitioner is not aware of any disclaimers or reexamination certificates regarding the '885 Patent. MOSAID—the alleged Patent Owner—filed a complaint asserting the '885 Patent against Petitioner on March 28, 2023 in the U.S. District Court for the Eastern District of Texas (Civil Action No. 2:23-CV-00129-JRG). The '885 Patent was asserted in four district court infringement actions (*Mosaid Technologies Inc. v. Freescale Semiconductor, Inc.*, Case. No. 6:11-cv-00173 (Apr. 8, 2011, E.D. Tex.); *MOSAID Technologies Inc. v. Xilinx, Inc.*, Case. No. 6:12-cv-00847 (Nov. 5, 2012, E.D. Tex.); *MOSAID Technologies Inc. v. ST-Ericsson, Inc.*, Case. No. 6:12-cv-00845 (Nov. 5, 2012, E.D. Tex.)); *Conversant Intellectual Property Management Inc. v. Samsung Electronics Co., Ltd., et al*, Case No. 2:15-cv-00281 (Feb. 26, 2015) (E.D. Tex.) and subject to one declaratory judgment action (*ARM Ltd. v. MOSAID Technologies, Inc.*, Case No. 3:11-cv-03869 (Aug. 5, 2011, N.D. Cal.), transferred to *ARM Ltd. v. MOSAID Technologies, Inc.*, Case No. 6:12-cv-00008 (Jan. 9, 2012, E.D. Tex), which were

all voluntarily dismissed based on settlement.

**C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)**

Petitioner provides the following designation of counsel.

| Lead Counsel                                                                                                                                                                                                                           | Backup counsel                                                                                                                                                                                                                                                                |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Timothy W. Riffe, Reg. No. 43,881<br>Fish & Richardson P.C.<br>60 South Sixth Street<br>Minneapolis, MN 55402<br>Tel: 202-783-5070<br>Fax: 877-769-7945<br>Email: <a href="mailto:IPR44508-0023IP5@fr.com">IPR44508-0023IP5@fr.com</a> | Joseph Colaianni, Reg. No. 39,948<br>Linhong Zhang, Reg. No. 64,749<br>Jared M. Hartzman, Reg. No. 70,255<br>60 South Sixth Street<br>Minneapolis, MN 55402<br>Tel: 202-783-5070<br>Fax: 877-769-7945<br><a href="mailto:IPR44508-0023IP5@fr.com">IPR44508-0023IP5@fr.com</a> |

**D. Service Information**

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at [IPR44508-0023IP5@fr.com](mailto:IPR44508-0023IP5@fr.com).

Respectfully submitted,

Dated: March 25, 2024

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(Control No. IPR2024-00719)

Attorneys for Petitioner

**CERTIFICATION UNDER 37 CFR § 42.24**

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,981 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: March 25, 2024

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**CERTIFICATE OF SERVICE**

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on March 25, 2024, a complete and entire copy of this Petition for *Inter partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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