



CMOS Digital Circuit Technology

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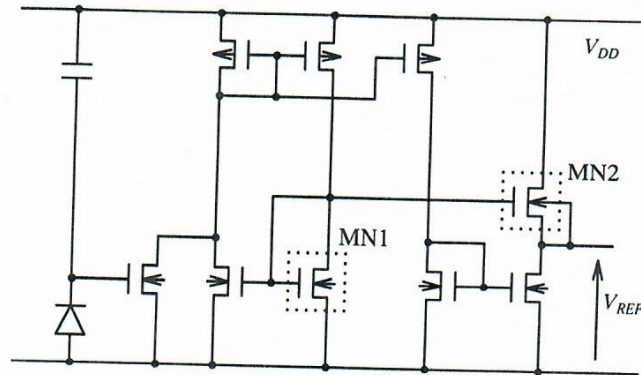


Figure 2.35 Band-gap reference voltage generator using gate work-function difference.

(E) Substrate Bias Generation

Sometimes it is advantageous to apply a negative bias to the P-type substrate, thereby reducing the parasitic capacitance of the diffused islands of NFETs and further preventing accidental forward biasing of the PN junctions [36]. A clocked circuit that generates DC voltage outside the range covered by the power supply is called a charge pump.

The circuit shown in Fig. 2.36(a) generates a negative voltage at the terminal SUB. All NFETs are on P-tubs that are connected to SUB. Q and $\bar{Q}$ are a pair of complementary clocks as shown in Fig. 2.36(b). When Q is high, node A is clamped to $+V_{TH}$ by a MOSFET in diode connection, MN1, whose source is grounded. When Q is low, node A is lower than V_{TH} by V_{DD} . At the same time node B is clamped to the voltage higher than the voltage of node A by V_{TH} , by a MOSFET in diode connection, MN2. This loading pulls the node A voltage above $-(V_{DD}-V_{TH})$. When clock Q becomes high again, the voltage of node B goes down by V_{DD} . At the same time, node C is clamped to the voltage of node B plus V_{TH} . When the voltage of node C, B, or A is lower than the substrate voltage, the MOS device MNC, MNB, or MNA, respectively, conducts, thereby pulling the substrate voltage down. With this mechanism a DC voltage lower than the ground potential is generated. This circuit is identical to the voltage doubler rectification circuit used in transformer-less vacuum tube radio [37].

The substrate voltage generator can be controlled by a feedback mechanism, to maintain the voltage within a narrow range. A technique to maintain the threshold voltage of a short-channel FET through negative feedback control exercised through

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