

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Barry A. Hoberman, *et al.*
U.S. Patent No.: 8,253,438 Attorney Docket No.: 44508-0023IP6
Issue Date: August 28, 2012
Appl. Serial No.: 13/074,291
Filing Date: March 29, 2011
Title: LOW LEAKAGE AND DATA RETENTION CIRCUITRY

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 8,253,438 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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LIST OF EXHIBITS

- MTK-1001 U.S. Patent No. 8,253,438 to Hoberman, *et al.* (“’438 Patent)
- MTK-1002 Excerpts from the Prosecution History of the ’438 Patent
- MTK-1003 Declaration of Dr. Paul Min, Ph.D.
- MTK-1004 U.S. Patent Publication No. 2003/0025130 to Takahashi, *et al.*
 (“Takahashi”)
- MTK-1005 U.S. Patent Publication No. 2003/0102904 to Mizuno, *et al.*
 (“Mizuno”)
- MTK-1006 U.S. Patent No. 7,091,766 to Ko, *et al.* (“Ko”)
- MTK-1007 U.S. Patent No. 5,440,520 to Schutz, *et al.* (“Schutz”)
- MTK-1008 Excerpts from Alan C. Dixon, *et al.*, *A Practical Approach to
Digital Electronics*, 2000
- MTK-1009 Excerpts from John D. Carpinelli, *Computer Systems
Organization and Architecture*, 2001
- MTK-1010 U.S. Patent No. 6,141,762 to Nicol, *et al.* (“Nicol”)
- MTK-1011 U.S. Patent No. 6,087,813 to Tobita (“Tobita”)
- MTK-1012 U.S. Patent No. 6,889,538 to Borkar (“Borkar”)
- MTK-1013 U.S. Patent No. 6,518,826 to Zhang (“Zhang”)
- MTK-1014 U.S. Patent No. 7,042,274 to Hazucha, *et al.* (“Hazucha”)
- MTK-1015 Excerpts from Modern Dictionary of Electronics, Seventh
Edition, 1999
- MTK-1016 Excerpts from Dictionary of Science and Technology, 2003
- MTK-1017 Excerpts from Adel S. Sedra, *et al.*, *Microelectronic Circuits*,
1998 (“Sedra”)
- MTK-1018 U.S. Patent No. 6,791,361 to Alon, *et al.* (“Alon”)
- MTK-1019 Complaint from MOSAID Technologies Inc. v. MediaTek, Inc.
et al., Case No. 2:23-CV-00129, ECF No. 1 (E.D. Tex. Mar. 28,
2023)

- MTK-1020 Affidavit of Service of Summons and Complaint on MediaTek USA, Inc. in MOSAID Technologies Inc. v. MediaTek, Inc. *et al.*, Case No. 2:23-CV-00129, ECF. No. 9 (E.D. Tex. Mar. 30, 2023)
- MTK-1021 MOSAID Technologies Inc.’s Disclosure of Asserted Claims and Infringement Contentions in Case No. 2:23-CV-00129, Dated July 6, 2023
- MTK-1022 Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, Katherine K. Vidal (USPTO June 21, 2022)
- MTK-1023 Petitioner’s *Sotera* Stipulation
- MTK-1024 Declaration of June A. Munford
- MTK-1025 U.S. Patent No. 6,556,071 to Notani, *et al.* (“Notani”)
- MTK-1026 Excerpts from Mitchell et al., *The Ultimate Competitive Advantage, Secrets of Continually Developing a More Profitable Business Model*, 2003
- MTK-1027 Excerpts from Wolf, *Modern VLSI Design, System-on-Chip Design*, Third Edition, 2002
- MTK-1028 Dickson, *On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique*, IEEE Journal of Solid-State Circuits, 1976
- MTK-1029 Excerpts from Shoji, *CMOS Digital Circuit Technology*, 1988
- MTK-1030 Excerpts from Brown, *Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices*, 1998
- MTK-1031 Palumbo, et al., *Charge-Pump Circuits: Power-Consumption Optimization*, IEEE Transactions on Circuits and Systems - I: Fundamental Theory and Applications, 2002
- MTK-1032 Claim Construction Order in *Mosaid Technologies Inc. v. Freescale Semiconductor, Inc.*, Case No. 6:11-cv-00173 (E.D. Tex. April 29, 2013)

MTK-1033 Claim Construction Order in *Conversant Intellectual Property Management Inc., et al. v. Xilinx, Inc.*, Case No. 6:12-cv-00847 (E.D. Tex. January 9, 2015)

LISTING OF CHALLENGED CLAIMS

Claim 1	
1[p]	An integrated circuit comprising:
1[a]	a plurality of power islands having associated power consumptions, each of the power islands including circuitries and sleep transistors in coupled relation with the circuitries, and the sleep transistors being included within the integrated circuit to facilitate reduction of power consumed by the circuitries;
1[b]	a power island manager configured to dynamically change the power consumptions based on needs and operation of the integrated circuit, the power island manager in communication with at least one of the power islands; and
1[c]	an adaptive leakage controller configured to control change of a variable voltage to be applied to the sleep transistors, and the power island manager configured to generate the variable voltage based on a control signal received from the adaptive leakage controller
Claim 2	
2	The integrated circuit as claimed in claim 1 wherein the at least one of the power islands can be put to sleep and taken out of sleep at different times.
Claim 3	
3	The integrated circuit as claimed in claim 2 wherein the power island manager includes a state machine to control when the at least one of the power islands is put to sleep and when the at least one of the power islands is taken out of sleep.
Claim 4	
4	The integrated circuit as claimed in claim 1 wherein the power islands are delineated based on functional intellectual property units of the integrated circuit.
Claim 5	
5	The integrated circuit as claimed in claim 1 wherein the power islands are delineated by memory, logic and third party intellectual property.

Claim 6	
6	The integrated circuit as claimed in claim 1 wherein the variable voltage is an optimum voltage.
Claim 7	
7	The integrated circuit as claimed in claim 6 wherein the optimum voltage is dependent upon both process variation and temperature variation.
Claim 8	
8	The integrated circuit as claimed in claim 6 wherein the optimum voltage is generated by a sleep generator within the power island manager.
Claim 9	
9	The integrated circuit as claimed in claim 8 wherein the sleep generator comprises a charge pump.
Claim 10	
10	The integrated circuit as claimed in claim 1 wherein the variable voltage is generated by a sleep generator within the power island manager.
Claim 11	
11	The integrated circuit as claimed in claim 10 wherein the sleep generator comprises a charge pump.
Claim 12	
12	The integrated circuit as claimed in claim 11 wherein the control signal is a digital signal.
Claim 13	
13	The integrated circuit as claimed in claim 1 further comprising a central processing unit separate from and in communication with the power island manager.
Claim 14	
14	The integrated circuit as claimed in claim 13 further comprising another power island manager, the central processing unit separate from and in communication with the another power island manager.
Claim 15	
15[p]	An integrated circuit comprising:

15[a]	a plurality of power islands having associated power consumptions, and the power consumptions being dynamically changeable based on needs and operation of the integrated circuit, and each of the power islands including circuitries and sleep transistors in coupled relation with the circuitries, and the sleep transistors being included within the integrated circuit to facilitate reduction of power consumed by the circuitries;
15[b]	a sleep generator including a charge pump to generate a variable voltage to be applied to the sleep transistors; and
15[c]	an adaptive leakage controller configured to control change of the variable voltage by providing a digital control signal to the sleep generator.
Claim 16	
16	The integrated circuit as claimed in claim 15 wherein the power islands are delineated based on functional intellectual property units of the integrated circuit
Claim 17	
17	The integrated circuit as claimed in claim 15 wherein the power islands are delineated by memory, logic and third party intellectual property.
Claim 18	
18	The integrated circuit as claimed in claim 15 wherein the variable voltage is an optimum voltage.
Claim 19	
19	The integrated circuit as claimed in claim 18 wherein the optimum voltage is dependent upon both process variation and temperature variation.

MediaTek Inc. (“Petitioner” or “MediaTek”) petitions for *Inter Partes* Review (“IPR”) of claims 1-19 (“Challenged Claims”) of U.S. Patent No. 8,253,438 (“’438 Patent”).

I. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the ’438 Patent is available for IPR and Petitioner is not barred or estopped from requesting review of the Challenged Claims. The Petition is filed within one year of service of a complaint against Petitioner in *Mosaid Technologies Inc. v. MediaTek Inc., MediaTek USA, Inc.*, Case No. 2:23-cv-00129 (E.D. Tex. March 2023). *See* MTK-1019; MTK-1020.

B. Challenge and Relief Requested

Petitioner requests IPR of the Challenged Claims on the grounds below. Dr. Paul Min provides supporting explanations in his declaration (MTK-1003) cited throughout this petition.

Ground	Claims	Pre-AIA §103 Basis
1A	1-19	Takahashi (MTK-1004)
1B	7, 19	Takahashi in view of Schutz (MTK-1007)
1C	9, 15	Takahashi in view of Notani (MTK-1025)
2A	1-19	Mizuno (MTK-1005)
2B	9, 15	Mizuno in view of Notani (MTK-1025)

Each reference pre-dates the '438 Patent's earliest possible priority date (February 19, 2004; "Critical Date") and qualifies as prior art.¹

Reference	Date	Prior Art Under
Takahashi	February 6, 2003 (published)	§102(b)
Mizuno	June 6, 2003 (published)	§102(a)/(e)
Schutz	August 8, 1995 (issued)	§102(b)
Notani	March 18, 2002 (filed)	§102(a)/(e)

II. THE '438 PATENT

A. Brief Description

The '438 Patent relates to reducing power in integrated circuits. MTK-1001, Title, 1:25-35; MTK-1003, ¶74. An integrated circuit's total power consumption includes the power consumed while it is active and while it is inactive (idle). MTK-1001, 1:30-32; MTK-1003, ¶75. The idle power consumption is due to leakage current—the current flowing through the integrated circuit even while it is not performing its designed function. MTK-1001, 1:36-43; MTK-1003, ¶75.

¹ In co-pending litigation between Patent Owner MOSAID Technologies Inc. ("Patent Owner" or "MOSAID") and Petitioner, MOSAID asserts that the Challenged Claims are entitled to an invention date at least as early as December 11, 2003. MTK-1021, 8. Petitioner does not concede the '438 Patent is entitled to claim priority to the Critical Date or any earlier date.

The '438 Patent acknowledges that methods of reducing leakage current were well-known. MTK-1001, 1:44-2:17; MTK-1003, ¶76. One solution is to include a sleep transistor in series between the circuit and a supply voltage (*e.g.*, VDD or VSS) as a switch to turn the circuit on and off. MTK-1001, 2:5-17; MTK-1003, ¶76.

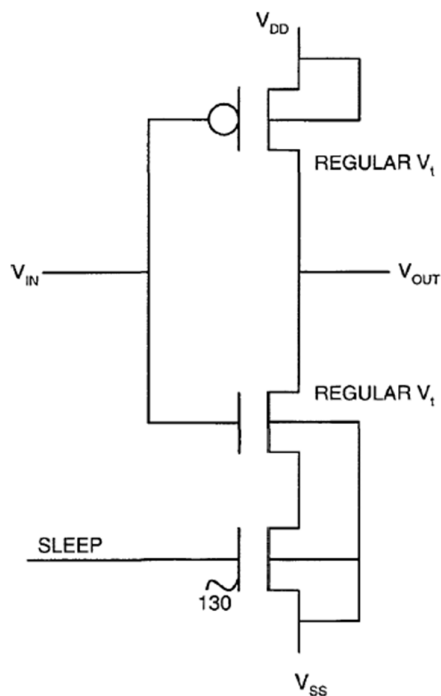
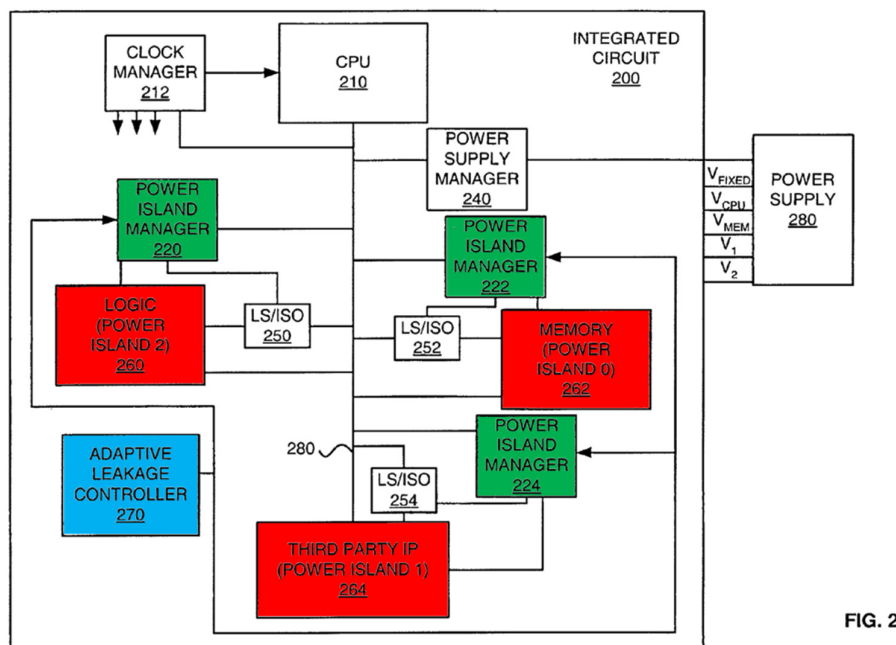


FIG. 1
PRIOR ART

MTK-1001, FIG. 1.

Another common solution is to divide the circuits in an integrated circuit into distinct power islands whose power consumptions can be controlled independently. MTK-1001, 3:46-52, 3:62-4:7; MTK-1003, ¶77.

The '438 Patent discloses a technique for allegedly reducing power consumption using sleep transistors and power islands with other functional blocks. MTK-1001, 3:46-4:24; MTK-1003, ¶¶78.²



MTK-1001, FIG. 2³

The power islands (red) in the integrated circuit have associated low leakage circuitry such as sleep transistors. MTK-1001, 3:46-52, 3:62-4:7; MTK-1003, ¶¶79-80. Each power island is connected to a power island manager (green) that provides control signals to the power island to control its power

² The '438 Patent discloses additional techniques for retaining data while circuitry is in a low-power “sleep” state. Because the Challenged Claims are not directed to such features, Petitioner does not discuss those.

³ Annotations and color added unless otherwise noted.

consumption. MTK-1001, 3:46-52, 4:8-17. The technique also uses an adaptive leakage controller (blue) that provides control signals to the power island managers. *Id.*, 4:18-36; MTK-1003, ¶81. The voltages applied to the power islands are optimized to reduce leakage currents while the power islands are in sleep mode, thereby reducing overall power consumption. MTK-1001, 4:18-5:4; MTK-1003, ¶¶81-82.

B. Summary of the Prosecution History

U.S. Patent Application No. 13/074,291 resulted in the '438 Patent and was filed on March 29, 2011, with a series of priority claims from a priority filing date of February 19, 2004. MTK-1002, 70-72. Following a preliminary amendment adding new claims, the claims were allowed without rejection on April 26, 2012. *Id.*, 79-83, 113-121; MTK-1003, ¶83.

C. Level of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSITA”) would have had at least a bachelor of science degree in electrical engineering, computer engineering, computer science, or a related field, and at least two years of experience in the research, design, development, or testing of electronic circuits or components, or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa. MTK-1003, ¶24.

D. Claim Construction

Claim terms generally should be given their ordinary and customary meaning. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R.

§42.100. For purposes of this proceeding only, Petitioner submits that no claim terms require a formal construction to address the Grounds in this Petition.

Wellman, Inc. v. Eastman Chem. Co., 642 F.3d 1355, 1361 (Fed. Cir. 2011).

Petitioner reserves the right to respond to any constructions offered/adopted by the Patent Owner or Board. Petitioner does not concede that each challenged claim satisfies all statutory requirements and does not waive any arguments concerning grounds that can only be raised in district court.

III. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. GROUND 1A—CLAIMS 1-19 ARE OBVIOUS OVER TAKAHASHI

1. Overview of Takahashi

Takahashi discloses systems and methods for “suppressing the leakage current in an integrated circuit.” MTK-1004, Title; MTK-1003, ¶¶87-88.

Takahashi describes “a first embodiment of a semiconductor integrated circuit” in Figures 1-5. MTK-1004, [0047]-[0053]; MTK-1003, ¶89. “[D]evice 200” includes a “logic circuit 10 having a CMOS structure, switching circuit 20 for supplying an operating current to logic circuit 10, voltage regulator 40 capable of supplying variable and multiple voltages, and control circuit 30 for controlling voltage regulator 40.” MTK-1004, [0048].

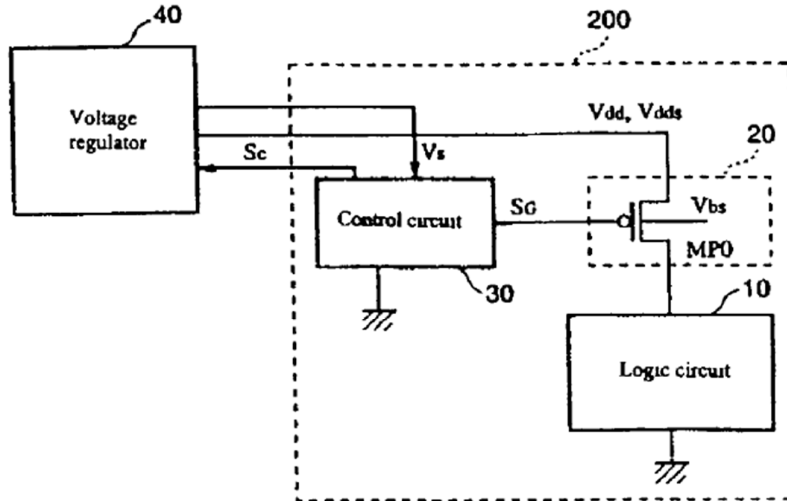


FIG. 1

MTK-1004, FIG. 1

“Switching circuit 20 supplies an operating current to logic circuit 10 during operation and suppresses the leakage current of the low threshold voltage transistor of logic circuit 10 during standby.” MTK-1004, [0052]. “Control signal S_G of different levels is applied to the gate of transistor MP0 during operation and during standby” such that “[t]ransistor MP0 is turned on or off according to the level of said control signal S_G .” MTK-1004, [0053]. MTK-1003, ¶90. “[D]ifferent levels are applied during operation and during standby, respectively, for the source voltage at the source of transistor MP0.” MTK-1004, [0053]; MTK-1003, ¶91. “[S]ource voltages V_{dd} and V_{dds} ” are set to a “nominal operating voltage” while logic circuit 10 is active and to a lower voltage while in “standby (Sleep mode).” MTK-1004, [0053]-[0054], [0110]; MTK-1003, ¶91. Lowering “source voltages” during standby places “transistor MP0” into a “super

cut-off status” that reduces leakage current and therefore power consumption during standby. *Id.*

A related embodiment shown in Figures 11-17 adds a “fusing circuit 202” to “device 200” that is programmed with “control data DAT.” MTK-1004, [0045], [0097]-[0117]; MTK-1003, ¶92. The control data DAT is “based on the process requirements of device 200 during operation (Active mode) and during standby (Sleep mode)” such that “voltage regulator 100 generates source voltages V_{dd1} , V_{dd2} , and V_{dd3} using optimum values ... according to control data DAT and control signal S_C indicating the operating status of device 200.” MTK-1004, [0110], [0117]; MTK-1003, ¶92. By changing the source voltages based on the “process requirements” of the transistors in device 200, “the effect of variations in the production process can be reduced.” MTK-1004, [0117]; MTK-1003, ¶93. The components and operation of “device 200” in the embodiment of Figures 11-17 otherwise remains the same as in the embodiment of Figures 1-5. MTK-1003, ¶93-95.

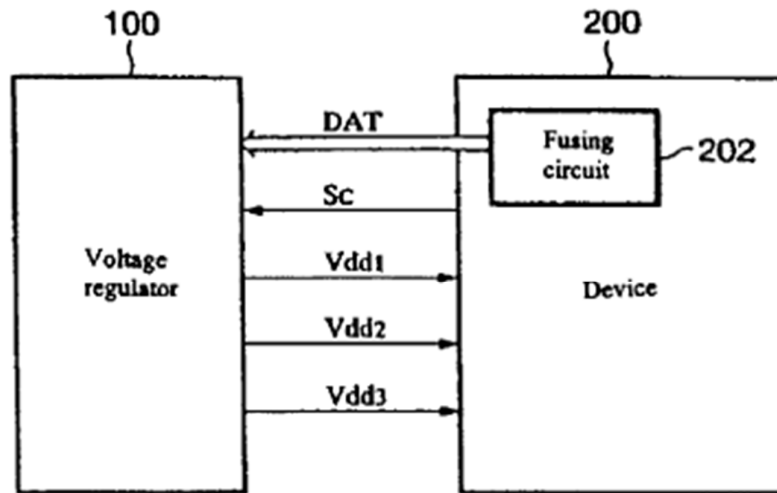


FIG. 11

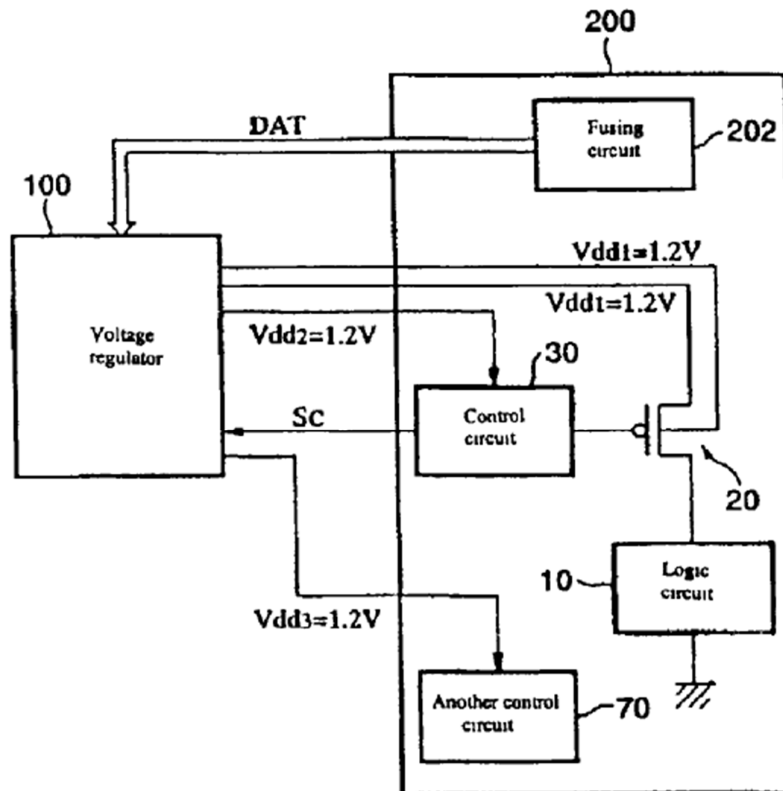


FIG. 16

MTK-1004, FIGS. 11, 16

2. Claim 1

(a) Element 1[p]

To the extent the preamble is limiting, Takahashi discloses methods carried out in a “semiconductor integrated circuit,” such as those depicted in the embodiments of Figures 1-5 and 10-17. MTK-1004, Abstract, [0001], [0047], [0097]; MTK-1003, ¶¶96-98.

(b) Element 1[a]

Takahashi discloses a plurality of power islands having associated power consumptions, each of the power islands including circuitries and sleep transistors in coupled relation with the circuitries. MTK-1003, ¶¶99-101.

The '438 patent describes a power island as any “section, delineation, partition, or division of an integrated circuit where power consumption is controlled within the section, delineation, partition, or division.” MTK-1001, 3:62-65. A POSITA would have understood and found obvious that Takahashi discloses multiple such power islands, each of which includes sleep transistors coupled with circuitries.⁴ MTK-1003, ¶¶102.

⁴ Petitioner submits that “sleep transistor” does not need to be construed for the purpose of this petition. The '438 patent describes that “sleep transistors act as a switch to turn on and off the logic gate” and are configured to “reduce power consumption” of a circuit “in the sleep state” that results in the “circuit hav[ing]

First, a POSITA would have understood and found obvious that Takahashi's logic circuit 10 (*i.e.*, circuitries) and "switching circuit 20" (*i.e.*, sleep transistors), depicted in at least Figures 1, 4-10, and 16-17, comprise a power island. *Id.* Takahashi's integrated circuit includes "logic circuit 10 having a CMOS structure" that "is a functional circuit for performing a logic operation." MTK-1004, [0045], [0048], [0078]. "[L]ogic circuit 10" can be "a CMOS inverter," "an AND circuit, a NAND circuit, or an OR circuit," or "may consist of other kinds of logic circuits." *Id.*, [0050]. "[L]ogic circuit 10" has an associated power consumption controlled by the "switching circuit 20" that "supplies an operating current to logic circuit 10 during operation and suppresses the leakage current of the ... logic circuit 10 during standby." *Id.*, [0052]; MTK-1003, ¶101-103.

low leakage based on the sleep signal." MTK-1001, 2:5-17; 2:42-47. The petition's references' disclosures, in light of a POSITA's knowledge, are consistent with the '438 patent's descriptions and render this limitation obvious as described herein. *See* MTK-1003, ¶¶99-115, 130-148, 295-321, 332-346.

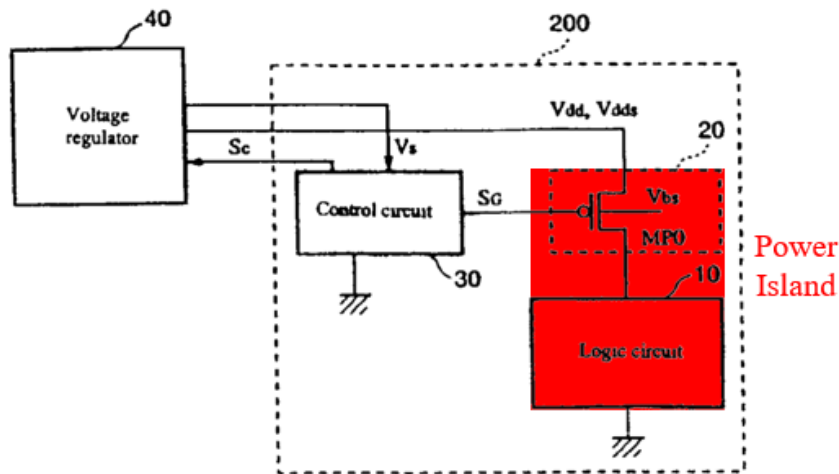


FIG. 1

MTK-1004, FIG. 1

Second, a POSITA would have understood and found obvious that Takahashi's "control circuit 70" (*i.e.*, circuitries) included in "device 200" of Figures 11-17 for "Wake up logic," would be coupled with a "switching circuit 20" (*i.e.*, sleep transistors) and thus comprise another power island. MTK-1004, [0110]-[0116], FIGS. 14-17; MTK-1001, 3:62-65; MTK-1003, ¶¶103-104. "[C]ontrol circuit 70" has an associated power consumption controlled by "source voltage V_{dd3} " that varies based on whether it is in an operational or standby state. *Id.*

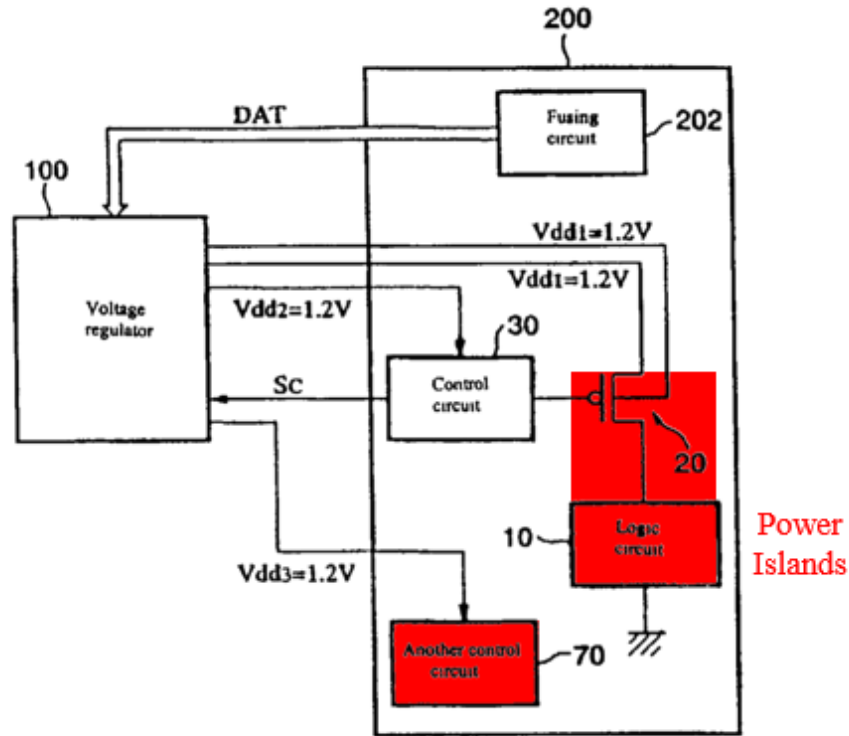


FIG. 16

MTK-1004, FIG 16

A POSITA would have found it obvious to include another “switching circuit 20” (*i.e.*, sleep transistors) to further reduce power consumption of “Wake up logic” in “control circuit 70” during standby to achieve the same power savings described for Figure 10, as discussed below. MTK-1003, ¶¶103-104.

Third, a POSITA would have found it obvious for Takahashi’s integrated circuit, such as those depicted in Figures 1-5 and 11-17, to include multiple additional power islands. MTK-1003, ¶¶105-106. Figure 10 depicts a related embodiment in which the integrated circuit includes a “logic circuit 230” and includes “[m]emories 210, 220, 270, and 280, ... microprocessor core 240, DSP

core 250, and peripheral circuit 260.” MTK-1004, [0089]. Each of these functional circuits 210-280 (*i.e.*, circuitries), along with their respective “pMOS transistors 310, 320, ... , and 380” (*i.e.*, sleep transistors), comprises a power island. *Id.*, [0045], [0090]; MTK-1003, ¶¶106-107.

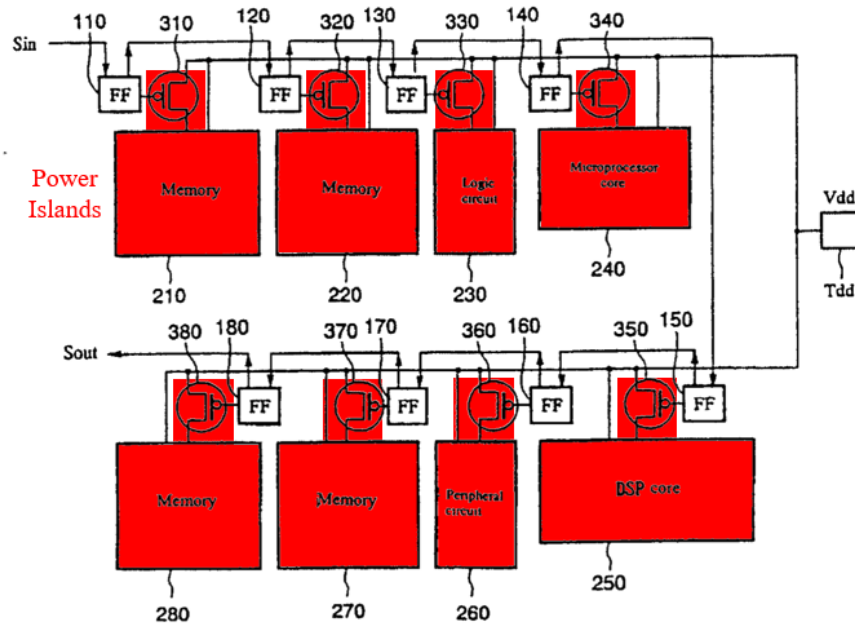


FIG. 10

MTK-1004, FIG 10

A POSITA would have found it obvious to incorporate multiple power islands as shown in Figure 10 into the embodiments of Figures 1-5 and 11-17 to provide additional functionality (*e.g.*, memory), and to control their individual power consumption. MTK-1003, ¶108. A POSITA would have understood that a device can include more than one “logic circuit” and been motivated to provide a “switching circuit” (*i.e.*, sleep transistor) for each to suppress leakage current

and obtain the same power savings described for Figure 10. MTK-1003, ¶¶108-110.

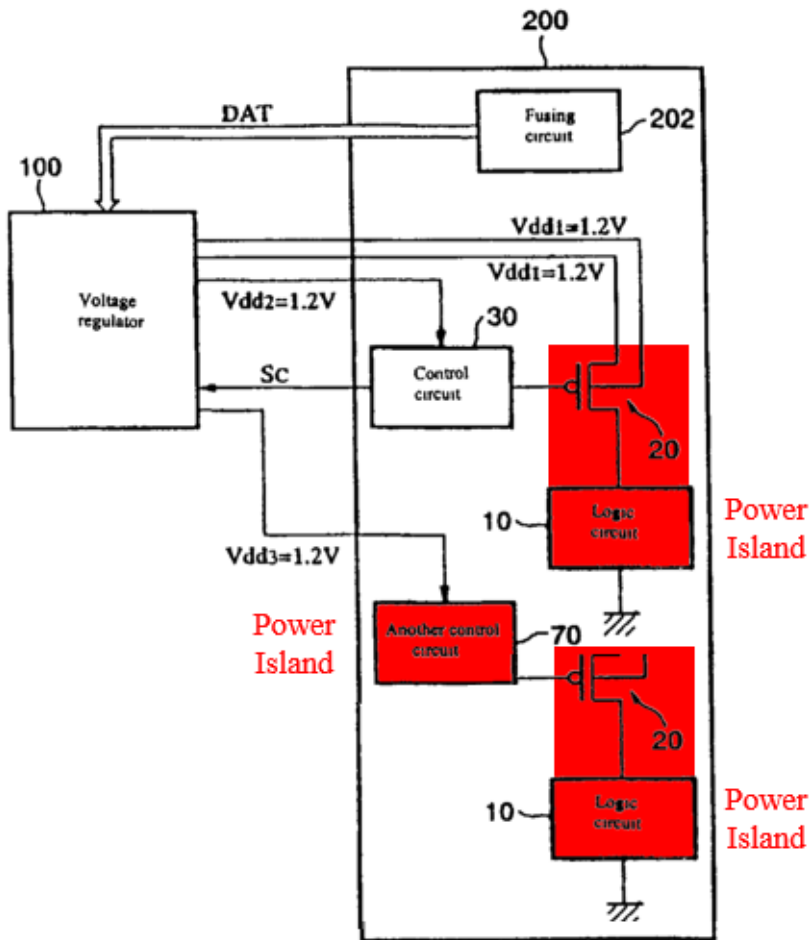


FIG. 16

EX-1004, FIG. 16 (as modified)

Thus, a POSITA would have readily understood and found obvious that Takahashi's "device 200" includes a plurality of power islands, including one or more "logic circuit[s] 10," "control circuit 70," and/or circuits 210-280 from Figure 10, along with their respective sleep transistors ("switching circuits"),

whose power consumptions are capable of being dynamically changed. MTK-1003, ¶¶109-112.

Lastly, a POSITA would have understood that each of Takahashi's "switching circuit 20" in Takahashi is included in the integrated circuit to facilitate reduction of power consumed by the circuitries. Takahashi explains that "switching circuit 20 ... suppresses the leakage current of the ... logic circuit 10 during standby." MTK-1004, [0052]; *see also id.*, [0054]-[0059], [0062], [0116], [0118]. In the related embodiment of Figure 10, Takahashi discloses that each of "pMOS transistors 310, 320, ..., and 380" of the "switching circuit" can be turned off so that the "occurrence of a leakage current in the [respective] functional circuit can be suppressed." *Id.*, [0090]; *see also id.* [0092]. Thus, a POSITA would have understood and found obvious that each "switching circuit 20" in Takahashi's integrated circuit reduces "power consumption due to leakage current" for the respective "logic circuit 10" or other circuitry. MTK-1004, [0062]; MTK-1003, ¶¶113-115; *see also* MTK-1004, [0003], [0010], [0085].

Petitioner notes that "power island" has been construed in prior litigations involving a patent describing similar subject matter, U.S. Patent No. 7,051,306. *See* MTK-1003, ¶114n.1; MTK-1032 43-44; MTK-1033 28-29. For purposes of this Petition, no construction is necessary because plain and ordinary meaning suffices. And while the prior constructions involved a different patent and different claims and are not binding on this proceeding, Takahashi's disclosures,

in light of a POSITA's knowledge, also render these terms obvious under the prior constructions. See MTK-1003, MTK-1003, ¶114n.1.

(c) Element 1[b]

Takahashi's integrated circuits also include a power island manager in communication with at least one of the power islands. MTK-1003, ¶116. Takahashi includes a "voltage regulator" that "controls the level of voltage to be supplied to device 200." MTK-1004, [0098]. A POSITA would have understood and found obvious that Takahashi's "voltage regulator" is a power island manager because it controls power within the power islands, *e.g.*, of "logic circuit 10" and "control circuit 70" included in the power islands. MTK-1003, ¶117; MTK-1001, 4:8-11. As shown below, "voltage regulator" is in communication with each of the power islands.

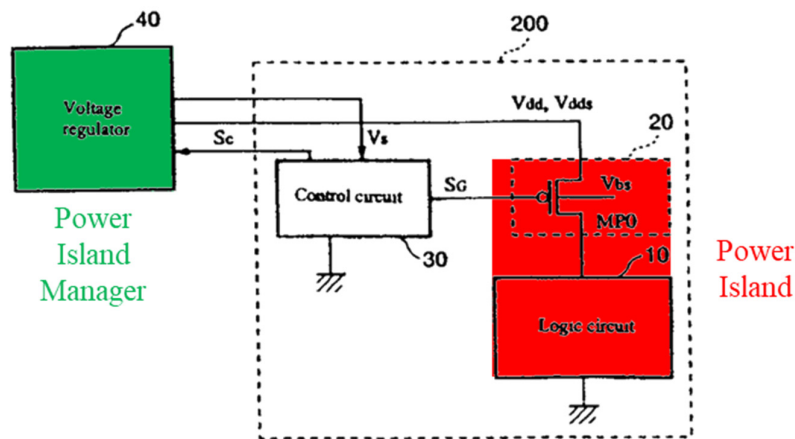


FIG. 1

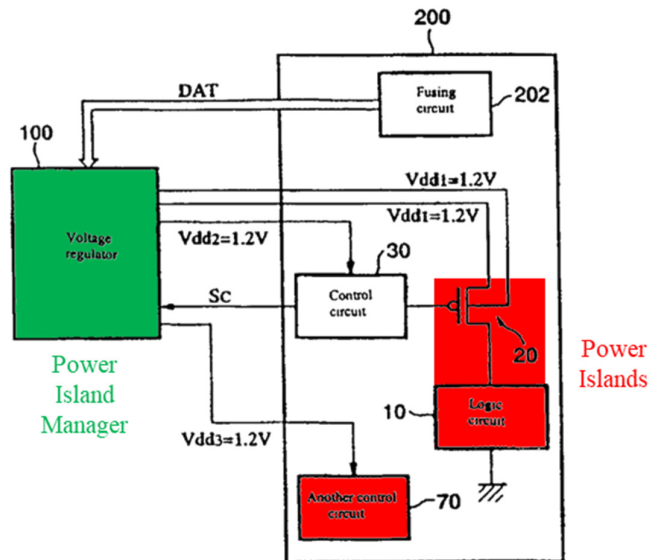


FIG. 16

MTK-1004, FIGS. 1, 16.

Takahashi's "voltage regulator" is configured to dynamically change the power consumptions of the power islands based on the needs and operation of the integrated circuit. MTK-1003, ¶¶117-129. When "device 200" is in "Active mode," the "voltage regulator" provides an "operating voltage" to the power islands' circuitries, including "logic circuit 10" and "control circuit 70," via their sleep transistors (*e.g.*, "switching circuit 20"). *Id.*, [0110]-[0117], FIGS. 14-17. During "Sleep mode," the "voltage regulator" lowers the voltage signals to place the power islands' circuitries, including "logic circuit 10" and "control circuit 70," into a low-power standby status (*i.e.*, dynamically changes their power consumption). *Id.* Thus, as in the '438 patent, Takahashi's "voltage regulator" "control[s] power within [each] power island" by "modify[ing] the voltage within the power island" based on whether the power island needs to be operational

(“Active Mode”) or can be placed into standby (“Sleep Mode”). MTK-1001, 4:11-14; MTK-1003, ¶¶117-129.

Active Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	1.2V	1.2V	1.20V	Weak
Fuse prog-1	0	0	1	1.15V	1.15V	1.15V	NTPW,NWPT
Fuse prog-2	0	1	0	1.05V	1.05V	1.05V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.95V	0.95V	0.95V	NSPT,NTPS
Fuse prog-4	1	0	0	0.85V	0.85V	0.85V	Strong

FIG. 14

Sleep Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

MTK-1004, FIGS. 14-15

(d) Element 1[c]

Takahashi’s integrated circuit includes a “control circuit 30” that discloses and renders obvious an adaptive leakage controller.⁵ MTK-1003, ¶¶130-133.

⁵ Petitioner submits that “adaptive leakage controller” does not need to be construed for the purpose of this petition. The ’438 patent describes, and a POSITA would understand consistent with that disclosure, that the “adaptive

“[C]ontrol circuit 30 ... generates control signal S_C as the operating status of device 200 changes and outputs it into voltage regulator 100.” MTK-1004, [0116]-[0117]. Based on “control signal S_C ,” the “voltage regulator” (*i.e.*, power island manager) generates variable “source voltages V_{dd1} , V_{dd2} , and V_{dd3} using optimum values under the respective preset conditions according to control data DAT and control signal S_C indicating the operating status of device 200, and outputs them into device 200.” MTK-1004, [0116]-[0117]. As shown below, “voltage regulator” (*i.e.*, power island manager) generates the variable “source voltage V_{dd} ” or “ V_{dd1} ” based on “control signal S_C ” (*i.e.*, control signal) and applies it to “switching circuit 20” (*i.e.*, sleep transistor).

leakage controller” is purposed to adapt an amount of leakage current by providing “optimum voltages to be applied to sleep transistors in the power islands.” MTK-1001, 4:21-27 (citing U.S. patent application Ser. No. 10/996,739 as describing it in detail). The petition’s references’ disclosures, in light of a POSITA’s knowledge, are consistent with the ’438 patent’s descriptions and render this limitation obvious as described herein. *See* MTK-1003 ¶¶130-148.

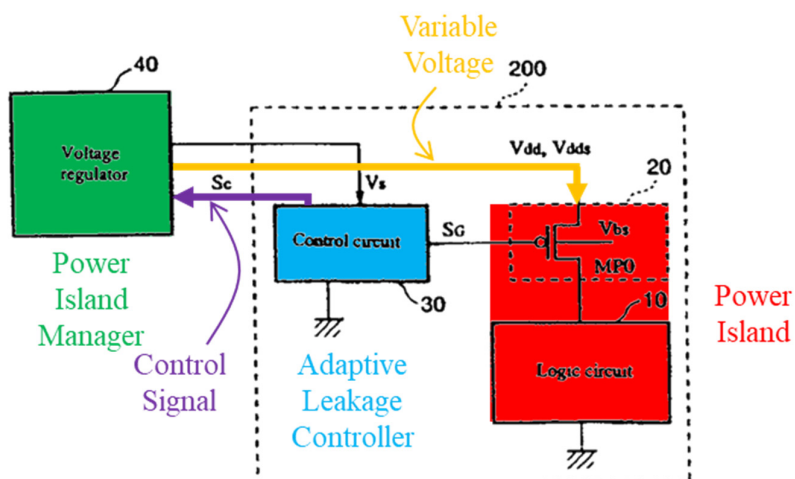


FIG. 1

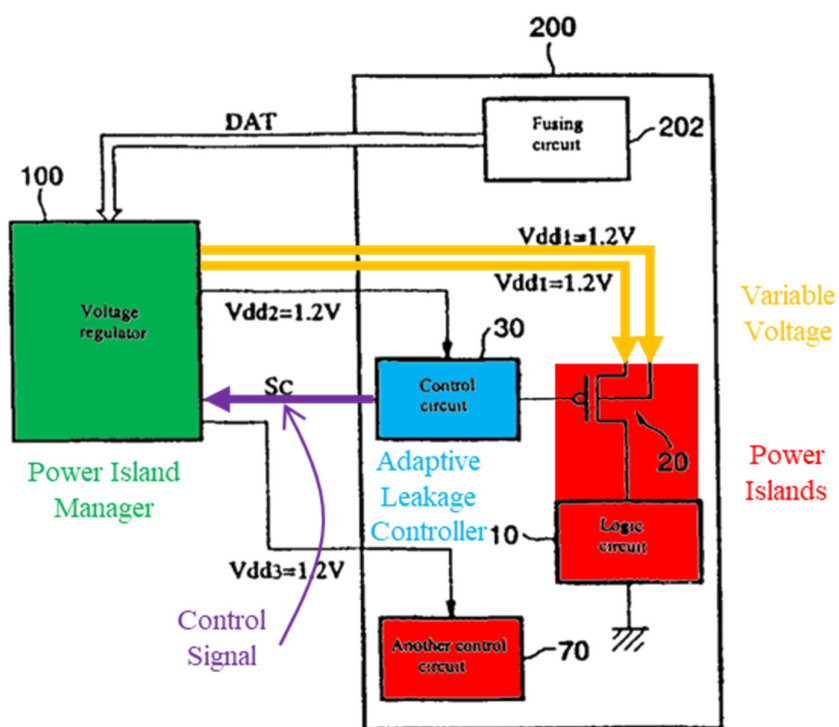


FIG. 16

MTK-1004, FIGS. 1, 16

The value of “source voltage” varies depending on whether the “control signal Sc” from the adaptive leakage controller (control circuit 30) indicates “device 200” is in active (Figure 16) or standby (Figure 17) mode.

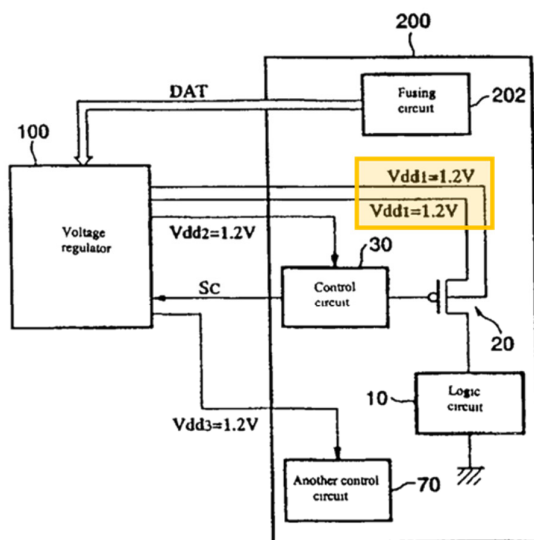


FIG. 16

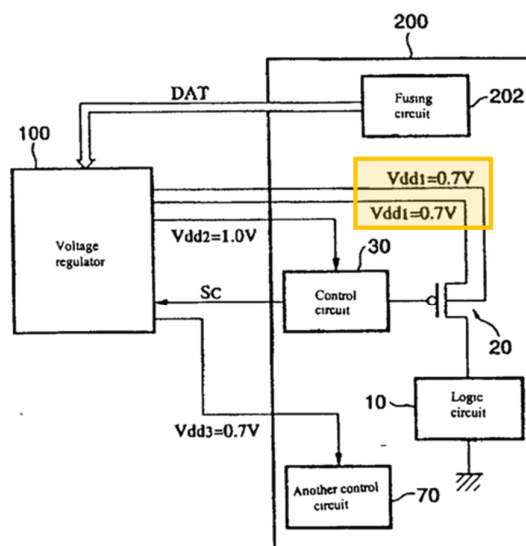


FIG. 17

By optimizing the source voltages in this way, “the switching circuit can be turned on during operation to supply driving current to the logic circuit, and ... can be turned off to suppress the occurrence of leakage current in low threshold voltage transistors in the logic circuit” during standby. *Id.*, [0117]-[0118] (“switching circuit” is put into a “super cut-off status” by applying “a voltage equal to or higher than the source voltage ... to the gate of the pMOS transistor” and “a bulk bias voltage with the same level as that of the source voltage or a higher level ... to the channel region of the transistor in order to suppress the current to the switching transistor during standby”); MTK-1003, ¶¶134-135. Thus, a POSITA would have understood and found obvious that

Takahashi's "control circuit 30" is an adaptive leakage controller configured to provide control signals for optimizing and causing the voltage regulator to vary the voltages applied to "switching circuit 20" ("sleep transistor") and power islands of "device 200." MTK-1001, 4:21-23; MTK-1003, ¶¶135-148.⁶

3. Claim 2

As discussed at element 1[c], Takahashi's "logic circuit 10" and "control circuit 70" are put into "standby (Sleep mode)" or "operation (Active mode)" at different times to reduce power consumption when not being used. MTK-1004, [0110]; MTK-1003, ¶¶149-151. Takahashi explains that "[t]ransistor MP0 [of switching circuit 20] is turned on or off" to supply "a driving current ... to logic circuit 10" or "cut off" the driving current such that "leakage current at logic

⁶ To the extent the claimed "adaptive leakage controller" must provide control signals to compensate for process and temperature variation to provide an optimum voltage to sleep transistors, Takahashi renders obvious those features. Takahashi discloses a "fusing circuit 202" that provides "control data DAT" indicating the "effect of variations in the production process" on the "driving capability" of the transistors in "device 200." MTK-1004, [0117]; MTK-1003, ¶¶138-147. As explained at Claim 7, it would have been obvious to a POSITA for the "control circuit 30" to provide "control data DAT" that accounts for "variations in the production process" as well as for temperature variation. *Id.*

circuit 10 is suppressed.” *Id.*, [0052]-[0053]; *see also id.*, [0098], [0112]-[0116] (addressing Figures 11-17). Takahashi discloses providing “control circuit 70” with a varying “source voltage V_{dd3} ” to place “Wake up logic” into a standby or operational state at different times. MTK-1004, [0098]-[0100], [0110]-[0117].

If required by Claim 2,⁷ a POSITA also would have found it obvious to selectively put “logic circuit 10” or “control circuit 70” power islands into standby or operational states at different times from other power islands, as done in Takahashi’s Figure 10 embodiment. MTK-1004, [0087]-[0095] (“[I]n the semiconductor integrated circuit shown in FIG. 10, supply of driving current to the respective functional circuits can be controlled individually by controlling the on/off status of the respective transistors constituting the switching circuit.”); MTK-1003, ¶¶151-155. A POSITA would have been motivated to do so because selectively placing individual power islands into “standby (Sleep mode)” or “operation (Active mode)” would reduce power consumption of “device 200.” *Id.* A POSITA would have understood that powering down unused power islands even while other power islands in “device 200” are operational would reduce the overall power consumption of “device 200.” *Id.* A POSITA would have known

⁷ Petitioner does not concede that the plain meaning of Claim 2 requires putting at least one power island to sleep and taking it out of sleep at different times *from other power islands*. MTK-1003, ¶152n.3.

how to implement such a feature, as shown in Figure 10 of Takahashi, in the integrated circuits of Figures 1-5 and 11-17. *Id.*

4. Claim 3

Takahashi discloses that “voltage regulator 100” (*i.e.*, power island manager) uses the inputs “control data DAT” and “control signal Sc” to determine optimum “source voltages” for putting power islands into standby and operational states. MTK-1004, [0098]-[0117]; MTK-1003, ¶¶156-160.

The “control data DAT” is set “according to the driving capabilities of the pMOS transistor and the nMOS transistor constituting device 200.” MTK-1004, [0100]. For example, Figure 13 shows that the “levels of source voltage V_{dd} ” vary between 1.2V and 0.85V depending on the driving strength of the pMOS and nMOS transistors. MTK-1004, [0107]-[0108].

P-MOS	NWPS Vdd=1.05V	NTPS Vdd=0.95V	Strong Vdd=0.85V	Strong corner
	NWPT Vdd=1.15V	Typical Vdd=1.05V	NSPT Vdd=0.95V	
	Weak Vdd=1.2V	NTPW Vdd=1.15V	NSPW Vdd=1.05V	
Weak corner		N-MOS		

FIG. 13

MTK-1004, FIG. 13

In Figures 14-15, “[v]oltage regulator 100 generates different levels of source voltages during operation and during standby according to said control data DAT and status control signal S_c ” to put the power islands into standby and operational states. MTK-1004, [0110]-[0111].

<u>Active</u> Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	1.2V	1.2V	1.20V	Weak
Fuse prog-1	0	0	1	1.15V	1.15V	1.15V	NTPW,NWPT
Fuse prog-2	0	1	0	1.05V	1.05V	1.05V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.95V	0.95V	0.95V	NSPT,NTPS
Fuse prog-4	1	0	0	0.85V	0.85V	0.85V	Strong

FIG. 14

<u>Sleep</u> Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

MTK-1004, FIGS. 14-15

A POSITA would have therefore understood and found obvious that Takahashi’s “voltage regulator” (*i.e.*, power island manager) includes a state machine with the output states shown in Figures 14-15 that controls when the power islands are put to sleep (*i.e.*, standby) and out of sleep (*i.e.*, operational) based on “control data DAT” and “control signal S_c ” inputs. MTK-1003, ¶¶160-167; MTK-1001, 6:19-21; MTK-1008 (defining “state machine” as a “circuit

containing several different states reachable from each other, with state changes happening synchronously”); MTK-1009; *see also* MTK-1006, 2:63-3:6, 7:20-50, 9:42-63, FIG. 4.

5. Claim 4

A POSITA would have understood and found it obvious that Takahashi’s power islands are delineated based on functional intellectual property (“IP”) units of the integrated circuit. MTK-1003, ¶¶168-172. According to the ’438 patent, examples of “functional IP units of the integrated circuit” include “memory 262,” “logic 260,” and “third party IP 264.” MTK-1001, 3:66-4:3 (*“the power islands are delineated based on functional IP units of the integrated circuit 200. In this example depicted in FIG. 2, power islands are delineated by memory 262, logic 260, and third party IP 264.”*); *see also id.*, 3:53-61(“integrated circuit 200 includes ... intellectual property (IP) (power island 1) 264.”), FIG. 2.

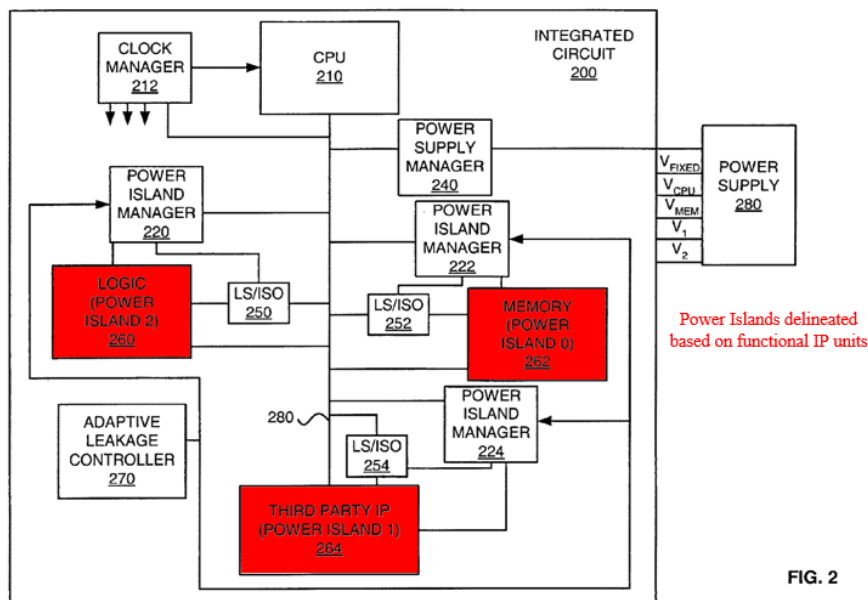


FIG. 2

MTK-1001, FIG. 2

A POSITA therefore would have readily understood that an “IP unit” refers to a predefined and reusable integrated circuit component, *e.g.*, a logic unit, memory cell, or functional block, that is the intellectual property of one party. MTK-1026 (“intellectual property cores” are “predefined,” and “are programming files that ... perform a specific standard function”); MTK-1027 (“An IP block is a pre-designed component that can be used in a larger design.”); MTK-1003, ¶¶169-172.

A POSITA would also have understood and found it obvious that Takahashi’s power islands, like the ’438 patent’s, include logic circuits (*e.g.*, logic circuit 10), control circuits (*e.g.*, “control circuit 70”), and memories (*e.g.*, “memory 210,” “memory 220,” “memory 270,” and “memory 280”) that are predefined and verified functional integrated circuit modules, and thus would be functional IP units of the integrated circuit. MTK-1004, [0017]-[0024], [0045], [0048], [0050], [0078], [0087], [0089]-[0095], [0099], claims 1, 4, 7-8, and FIGS. 1-2, 4, 8, 10, 16; MTK-1003, ¶¶172-181.

6. Claim 5

Takahashi discloses and renders obvious that its power islands are delineated by memory, logic, and third-party IP, *e.g.*, a functional block that is the IP of one party. MTK-1003, ¶¶182-186. For example, Takahashi discloses that its “logic circuit 10” can be “a CMOS inverter,” “an AND circuit, a NAND

circuit, or an OR circuit,” or “may consist of other kinds of logic circuits.”

MTK-1004, [0050]. Takahashi’s Figure 10 depicts power islands including “logic circuit 230,” “[m]emories 210, 220, 270, and 280” and third party IP units such as “microprocessor core” 240, “peripheral circuit” 260, and “DSP core” 250. *Id.*, [0089], FIG. 10; MTK-1003, ¶¶182-186.

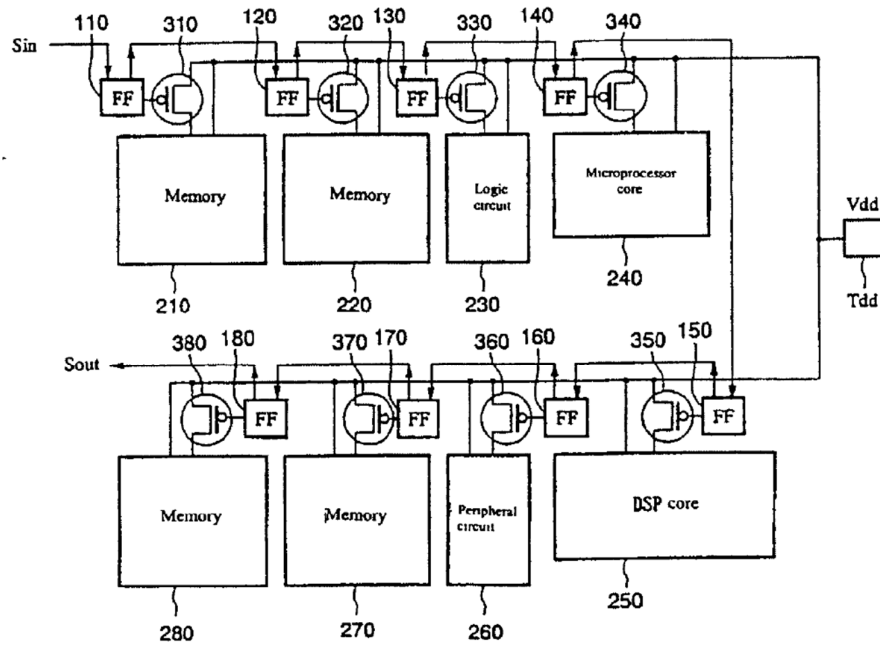


FIG. 10

MTK-1004, FIG. 10

7. Claim 6

Takahashi discloses that the variable “source voltage” provided by the “voltage regulator” is set to “optimum values under the respective present conditions according to control data DAT and control signal SC indicating the operating status of device 200.” MTK-1004, [0117]; *see also id.*, [0099]-[0100], [0107], [0109]-[0111], [0123], FIGS. 13-15. By optimizing the variable “source

voltage,” “the effect of variations in the production process can be reduced” and the “occurrence of leakage current is suppressed.” *Id.*, Abstract, [0109], [0116]-[0118], [0123]; MTK-1003, ¶¶187-191.

8. Claim 7

As discussed at Claim 6, Takahashi discloses that the “source voltage” is optimized based on process variation so that “the effect of variations in the production process can be reduced.” MTK-1004, [0117]; *see also* Claims 1[c], 4; MTK-1004, [0099]-[0100], [0107], [0109]-[0111], [0123], FIGS. 13-17.

It was also well-known at the time of the '438 Patent that transistor performance is dependent both on process variation and temperature variation. MTK-1003, ¶¶193-196; *see also, e.g.*, MTK-1010, 1:37-2:14 (“[I]t is known that varying supply voltage to a chip can improve performance by eliminating unexpected variability in the supply voltage, and by accounting for process and operating temperature variations.”); MTK-1011, 12:18-21; MTK-1012, 2:34-43, FIG. 2; MTK-1013, 1:19-30; MTK-1014, 4:14-23. Thus, it would have been obvious to a POSITA to optimize the “source voltage” based on temperature and process variation to further improve performance of the pMOS and nMOS transistors in “switching circuit 20” and “logic circuit 10” and reduce power consumption due “leakage current” in “device 200.” MTK-1004, Abstract; MTK-1003, ¶¶195-197.

A POSITA would have been readily capable of implementing such a change with a reasonable expectation of success. MTK-1003, ¶¶195-197. For example, a POSITA would have known how to incorporate a temperature sensor in Takahashi's integrated circuit such that the "voltage regulator" would optimize the "source voltage" output based on temperature and process variation indicated by "control data DAT" and "status control signal S_C." MTK-1004, [0098]-[0117], FIGS. 11-17; MTK-1003, ¶¶195-197.

9. Claim 8

Takahashi's "voltage regulator" (*i.e.*, power island manager) provides an optimum "source voltage" to "switching circuit 20" during "standby (Sleep mode)." MTK-1004, [0110], FIGS. 15, 17; MTK-1003, ¶¶198-202; *see* Claim 4.

Sleep Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

MTK-1004, FIG. 15

As explained at Claim 6, Takahashi's "[v]oltage regulator 100 generates different levels of source voltages ... during standby" so that "switching circuit 20 is in the super cut-off status during standby, and the occurrence of leakage current at logic circuit 10 is suppressed." MTK-1004, [0111], [0116]. Thus, a

POSITA would have understood and found obvious that “voltage regulator 100” generates an optimum variable voltage for “device 200” during “standby (Sleep mode)” using a sleep generator. MTK-1003, ¶¶201-204; *see* MTK-1001, 5:8-67, FIGS. 3-4.

10. Claim 9

A POSITA would have understood and found it obvious for Takahashi’s sleep generator within its “voltage regulator” to comprise a charge pump. MTK-1003, ¶¶205-207. As discussed with respect to element 1[c] and claims 6 and 8 above, Takahashi discloses a “voltage regulator” (including a sleep generator) that “controls the level of voltage to be supplied to device 200.” MTK-1004, [0098].

A POSITA would have also understood that *how* Takahashi’s sleep generator generates the optimum voltage is merely a design choice selected from among a finite number of well-known solutions. MTK-1003, ¶¶207-208. One such method for generating a regulated voltage is using a charge pump, which was a well-known solution for efficiently controlling integrated circuits and could be implemented using routine electrical and computer engineering principles. *Id.* *See also*, MTK-1028, MTK-1029, MTK-1030, MTK-1031. Charge pumps were a known solution for providing variable voltages from a power supply at least as of 1976, and the basic structure of a charge pump would have been well-known to a POSITA and obvious to implement. *Id.* Thus, it would have been obvious to

a POSITA for Takahashi's sleep generator to comprise a charge pump for generating its variable voltage. *See Uber Techs., Inc. v. X One, Inc.*, 957 F.3d 1334, 1341 (Fed. Cir. 2020) (claims unpatentable where there were "a finite number of known, predictable solutions at the time of the invention" such that a POSITA "would have faced a simple design choice"). A POSITA would have been able to include a charge pump in Takahashi's sleep generator to achieve predictable results without undue experimentation due to the well-known application and the design of charge pumps in integrated circuits for various applications. MTK-1003, ¶¶207-208.

11. Claim 10

Supra 1[b]-1[c] and Claims 6, 8. MTK-1003, ¶209.

12. Claim 11

Supra 1[b]-1[c] and Claims 6, 8, 10. MTK-1003, ¶210.

13. Claim 12

As explained at element 1[c], Takahashi's "control signal S_C " is binary, indicating either an operational or standby status of "device 200." MTK-1004, Abstract, [0098], [0111], [0116]-[0117]; MTK-1003, ¶¶211-17. Similarly, in other embodiments at Figures 6-9, similar "control signals S_{C1} and S_{C2} " are provided to "voltage switching circuit 50" that is "provided in place of the voltage regulator." MTK-1004, [0065]. "[C]ontrol signals S_{C1} and S_{C2} " take one of two values—either "the level of source voltage V_{ddN} " or "ground potential GND." MTK-1004, [0069]-[0074]. A POSITA would have understood that the

binary “control signals S_{C1} and S_{C2} ” are digital signals, and that “control signal S_C ” that likewise takes one of two values also is digital. MTK-1015 (defining “digital signal” as “[a]n electrical signal with two states”); MTK-1016; MTK-1003, ¶¶213-215.

“[C]ontrol data DAT” is a digital signal with a specific “number of bits.” MTK-1004, [0098], [0101], [0104], [0109]-[0111], FIGS. 14-15. A POSITA would have found it obvious to use digital signals for both the “control data DAT” and “control signal S_C ” such that the “voltage regulator” selects the “source voltage” levels based solely on digital inputs rather than a mix of digital and analog inputs. MTK-1003, ¶¶213-215.

All electrical signals are either digital or analog. MTK-1003, ¶215. It would have been obvious to a POSITA for “control signal S_C ” to be digital as one of only two options. *See Uber Techs.*, 957 F.3d at 1341.

14. Claim 13

Takahashi discloses and renders obvious a central processing unit (CPU) that is separate from and in communication with the “voltage regulator” (*i.e.*, power island manager). For example, Figure 10 of Takahashi discloses a “Microprocessor core” 240 that is a CPU that receives (*i.e.*, is in communication with) a “source voltage V_{dd} .” MTK-1004, [0089], FIG. 10. As discussed above at element 1[a], it would have been obvious to include multiple power islands in Takahashi’s other embodiments as well, such that Takahashi’s “voltage

regulator” that provides the “source voltage V_{dd} ” in the embodiments of Figures 1-5 and 11-17 would also provide the “source voltage V_{dd} ” for “Microprocessor core.” MTK-1003, ¶¶218-221.

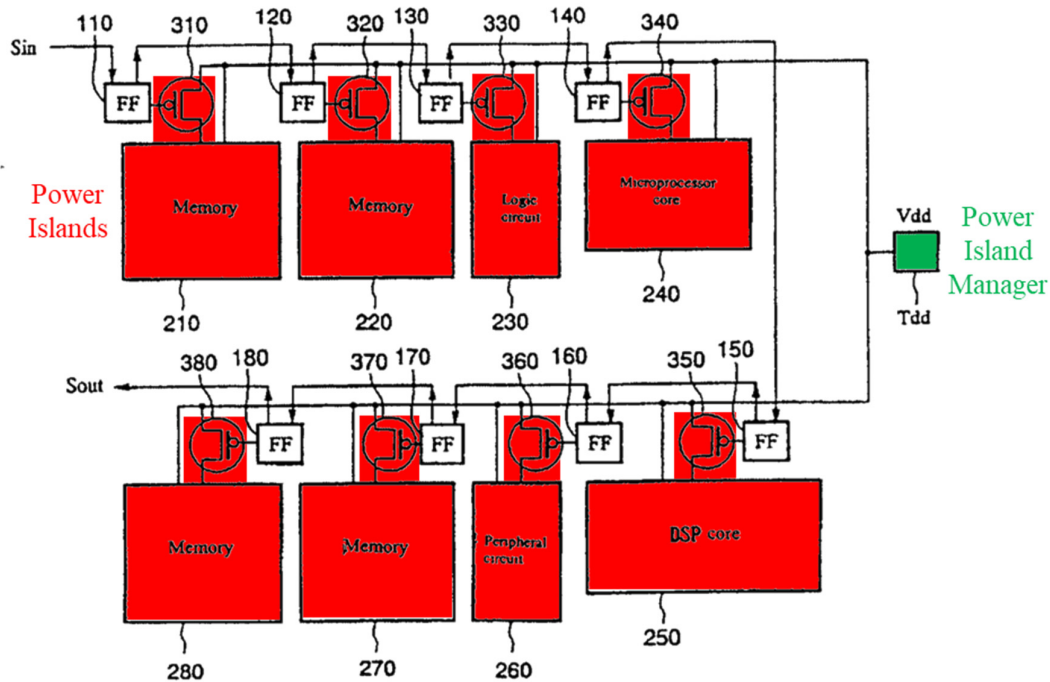


FIG. 10

MTK-1004, FIG. 10

15. Claim 14

A POSITA would have found it obvious for Takahashi’s integrated circuit to include an additional “voltage regulator” (*i.e.*, power island manager) in communication with the CPU. MTK-1003, ¶¶222-226. As explained at element 1[a], it would have been obvious for Takahashi’s “device 200” to include multiple power islands. A POSITA would have understood that certain power islands have substantially different voltage and/or current requirements that

require separate “voltage regulators,” *e.g.*, between a “logic circuit” and a “memory.” *See* MTK-1004, [0089], FIG. 10; MTK-1003, ¶¶224-225. A POSITA would have therefore found it obvious that, where the CPU (*e.g.*, “Microprocessor core”) controls the operation of both of those power islands, that the CPU must communicate with separate “voltage regulators” to place those power islands into “operational” or “standby” states. MTK-1003, ¶¶224-225. For example, in the embodiments of Figures 11-17, a CPU may communicate with “voltage regulator 100” via “control circuit 30” to control “logic circuit 10” and communicate with a separate “voltage regulator” via “another control circuit 70” to control a memory or other functional block. MTK-1003, ¶¶224-225.

16. Claim 15

(a) Element 15[p]

Supra 1[p]. MTK-1003, ¶227.

(b) Element 15[a]

Supra 1[a] and 1[b]. MTK-1003, ¶228.

(c) Element 15[b]

Supra 1[c] and Claims 8-11. MTK-1003, ¶229.

(d) Element 15[c]

Supra 1[c], Claim 10 and Claim 12. MTK-1003, ¶230.

17. Claim 16

Supra Claim 4 and 15[p]-15[c]. MTK-1003, ¶231.

18. Claim 17

Supra Claim 5 and 15[p]-15[c]. MTK-1003, ¶232.

19. Claim 18

Supra Claim 6 and 15[p]-15[c]. MTK-1003, ¶233.

20. Claim 19

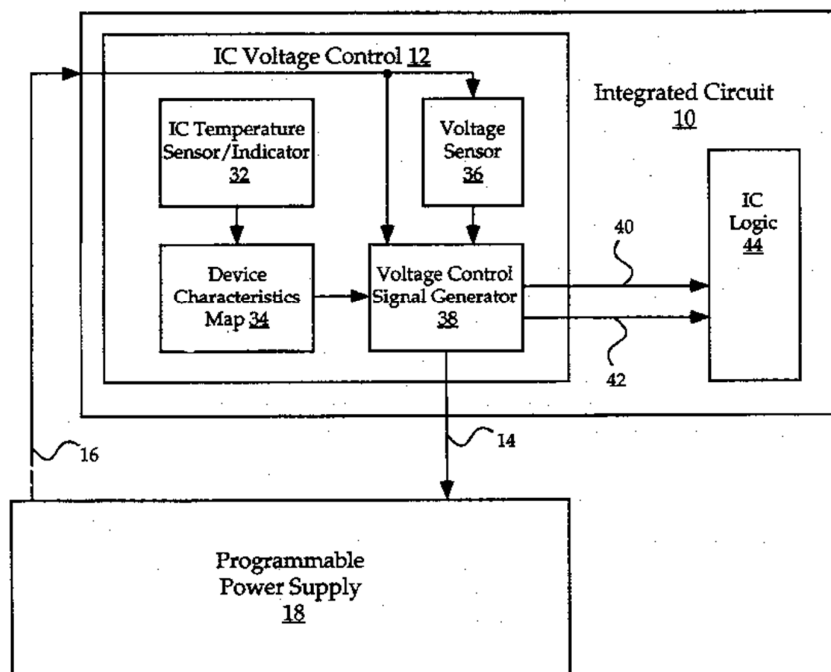
Supra Claim 7, 15[p]-15[c] and Claim 18. MTK-1003, ¶234.

**B. GROUND 1B—CLAIMS 7 AND 19 ARE OBVIOUS OVER
TAKAHASHI IN VIEW OF SCHUTZ**

1. Overview of Schutz

Schutz relates to controlling an integrated circuit's supply voltage "to optimize performance and reduce power consumption." MTK-1007, 1:7-36; MTK-1003, ¶¶236-240. Specifically, Schutz discloses an "integrated circuit device 10 [that] selects the supply voltage 16 based on a plurality of predetermined operational voltages and the temperature of integrated circuit device 10." *Id.*, Abstract, 6:31-35.

Figure 2



MTK-1007, FIG. 2

As shown in Figure 2, “IC voltage control circuit 12 includes an IC temperature sensor circuit 32, a device characteristics map 34, a voltage sensor circuit 36, and a voltage control signal generator 38.” *Id.*, 6:37-41. “The device characteristics map 34 stores predetermined operational characteristics of integrated circuit device 10,” which may be determined as part of the manufacturing and testing of the device. *Id.*, 6:64-66, 7:1-5, 7:24-37. Based on a temperature detected by “IC temperature sensor 32, device characteristics map 34 provides the corresponding operational voltage value to the voltage control signal generator 38,” which controls “programmable power supply 18” to provide the selected voltage for integrated circuit device 10. *Id.*, 7:38-45. Thus, Schutz’s

“integrated circuit device 10” ensures a reliable operation speed for the device and reduces power consumption regardless of manufacturing variations and temperature changes. *Id.*, 1:13-2:45; MTK-1003, ¶240.

2. Takahashi-Schutz Combination

A POSITA would have been motivated to modify Takahashi’s integrated circuit to incorporate the teachings of Schutz with a reasonable expectation of success. MTK-1003, ¶¶241-255. Both Takahashi and Schutz are directed to optimizing power to integrated circuits, including to reduce power consumption. MTK-1004, [0001] (“The present invention pertains to a semiconductor integrated circuit ... by which power consumption can be reduced by suppressing leakage current.”), *see also* [0002], [0017]; MTK-1007, Title, Abstract, 1:7-10 (“The present invention relates generally to supplying electrical power to circuits.”), *see also* 1:13-2:45. The ’438 Patent relates to this same field of endeavor. *See* MTK-1001, Abstract, 1:24-35; 2:34-47; MTK-1003, ¶242.

Takahashi and Schutz both address the problem of providing optimum voltages to an integrated circuit and do so in similar ways. MTK-1003, ¶¶243-248. Takahashi discloses adjusting “source voltages” “according to the driving capabilities of the transistors” in the circuit. MTK-1004, [0099]-[0100]. Likewise, Schutz adjusts the “supply voltage 16” to “optimize the high speed or high frequency performance” of the device depending on the device’s

“manufacturing process,” “intended use,” and “performance characteristics.”

MTK-1007, 5:14-18, 7:5-8.

Both Takahashi and Schutz perform device testing to determine the characteristics of the device. MTK-1004, [0099]-[0100], [0109]; MTK-1007, 5:14-27, 7:24-37. Takahashi and Schutz then program non-volatile memory in the devices based on the testing results and use this programming to optimize the supply voltages to the integrated circuits. MTK-1004, [0098]-[0117], FIGS. 14-17; MTK-1007, 4:55-5:34, 6:64-7:45, 8:12-28, FIG. 3. Specifically, Takahashi’s “voltage regulator 100” receives “control data DAT” stored in “fusing circuit 202”, and “generates source voltages V_{dd1} , V_{dd2} , and V_{dd3} using optimum values ... according to control data DAT and control signal SC indicating the operating status of device 200.” MTK-1004, [0098], [0117]. Similarly, Schutz’s “IC voltage control circuit 12” “selects one of the predetermined operational voltages stored in the device” that is the “optimized operational voltage for the measured device temperature,” after which the selected “supply voltage is generated by the programmable power supply.” MTK-1007, 8:11-28. Thus, both references reduce “the effect of variations in the production process” by powering their devices using “optimum source voltages.” MTK-1004, [0117]; MTK-1007, 7:5-37 (“predetermined operational voltages may be chosen to optimize the high speed or high frequency performance” for a “given temperature” and “particular device”), 8:12-19.

Figure 2

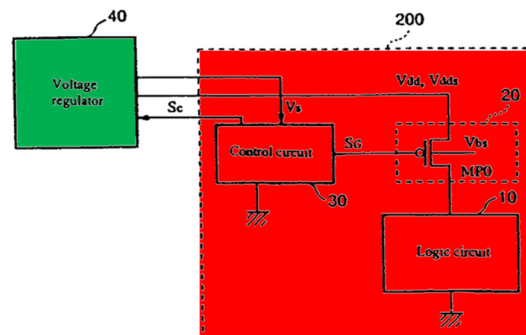
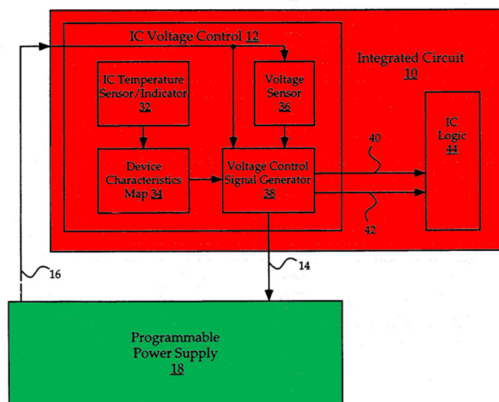


FIG. 1

MTK-1007, FIG. 2 (left); MTK-1004, FIG. 1 (right)

The similarities between Takahashi and Schutz would have led a POSITA to implement Schutz's teachings in Takahashi's integrated circuit to further improve Takahashi's ability to optimize the voltages in "device 200." MTK-1003, ¶¶245-248.⁸ Takahashi already programs "control data DAT" into "fusing circuit 202" to account for "variations during the production process." MTK-1004, [0099]; MTK-1003, ¶249. As explained at Claim 5 of Ground 1A, a POSITA would have understood that other factors including temperature impact the optimum voltages to provide "device 200." MTK-1003, ¶250. Thus, while Takahashi's "source voltages" are optimized for process variation, those voltages may not be the most optimal voltages for the "device 200." MTK-1004, [0117].

⁸ As explained at Ground 1A, Takahashi alone renders obvious the features of Claim 7. If Takahashi fails to render obvious those features, Takahashi in combination with Schutz renders obvious Claim 7.

A POSITA therefore would have understood and been motivated to further optimize the voltages generated by “voltage regulator 100” to account for temperature variations. MTK-1003, ¶¶251-255.

Schutz provides such a system for optimizing the voltages provided to an “integrated circuit device” to account for temperature variations. MTK-1007, Abstract; MTK-1003, ¶¶251-252. Specifically, Schutz discloses that its “integrated circuit device may include a temperature sensor to allow selection of the predetermined operational voltage according to device temperature to avoid speed-limiting voltage and temperature combinations.” MTK-1007, Abstract; *see also id.*, 8:13-19 (“optimized operational voltage” may be based on “measured device temperature” or “other factors including ... manufacturing characteristics or the intended application of the device”). Schutz’s “IC temperature sensor 32 senses the temperature of the device 10 and indicates that temperature to the device characteristics map 34.” MTK-1007, 6:50-52. “In response ... device characteristics map 34 provides the corresponding predetermined operational voltage value to the voltage control signal generator 38.” *Id.*, 7:38-42. “[V]oltage control signal generator 38” then controls “programmable voltage generator 18” to generate the optimal “supply voltage 16” for “integrated circuit device 10.” *Id.*, 4:14-18, 8:20-28.

Because Takahashi and Schutz provide a similar solution to a similar problem within the same field of endeavor, a POSITA would have naturally

looked at, and been motivated to combine, the two references to optimize the “source voltages” in Takahashi’s system. Specifically, a POSITA would have been motivated to employ Schutz’s “IC temperature sensor” to optimize “source voltages” from “voltage regulator 100” based on both process variation and temperature variation. MTK-1003, ¶253.

A POSITA would have readily implemented Schutz’s temperature sensor to further optimize the voltages provided “device 200” with predictable results. MTK-1003, ¶254. Temperature sensors were well known in the art, and a POSITA would have needed only routine electrical and computer engineering principles to add a temperature sensor to Takahashi’s “device 200.” A POSITA would have known how to modify Takahashi’s “voltage regulator 100” to consider temperature in addition to the “control data DAT and status control signal Sc” when selecting the optimum values for the “source voltages” provided to “device 200.” MTK-1004, [0111]; MTK-1003, ¶254.

TABLE 2

predetermined operational voltage	programmed value
+5.0	000
−5.0	001
12.0	010
3.3	011
2.5	100
1.8	101
1.5	110
1.2	111

TABLE 3

0–20° C.	3.0 V	40–50° C.	3.3 V
10–20° C.	3.1 V	50–60° C.	3.4 V
20–30° C.	3.2 V	60–70° C.	3.5 V
30–40° C.	3.2 V	70–80° C.	3.6 V

Active Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	1.2V	1.2V	1.20V	Weak
Fuse prog-1	0	0	1	1.15V	1.15V	1.15V	NTPW,NWPT
Fuse prog-2	0	1	0	1.05V	1.05V	1.05V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.95V	0.95V	0.95V	NSPT,NTPS
Fuse prog-4	1	0	0	0.85V	0.85V	0.85V	Strong

FIG. 14

Sleep Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

MTK-1007, Tables 2-3 (left); MTK-1004, FIGS. 14-15 (right)

Such a combination would predictably optimize the voltages provided to the “device 200” to further account for temperature variations, thereby improving the performance and power consumption of Takahashi’s “device 200.” MTK-1003, ¶¶254-255.

3. Claim 7

The Takahashi-Schutz combination renders obvious Claim 7. MTK-1003, ¶256. Schutz discloses an “IC voltage control circuit 12” that selects an optimum operational voltage “based on the temperature of the device” and “device characteristics.” MTK-1007, 6:64-7:37; MTK-1003, ¶¶257-258. An “IC temperature sensor 32” detects the temperature of the integrated circuit device and an “optimized operational voltage” for the device is selected based on the measured temperature and a “device characteristics map 34.” MTK-1007, 6:50-7:37, 8:12-18; MTK-1003, ¶258.

From Schutz’s teachings, a POSITA would have found it obvious for Takahashi’s “voltage regulator” to generate an optimum voltage that is dependent upon both process variation and temperature variation. For instance, it would have been obvious for “voltage regulator 100” to receive a temperature signal from a temperature sensor like Schutz’s “IC temperature sensor 32,” and to generate optimum “source voltages” based on the temperature signal in addition to “status control signal Sc” and “control data DAT” that accounts for process

variations. MTK-1004, [0098], [0111], [0117], FIGS. 13-17; MTK-1003, ¶¶259-260.

A POSITA would have had a reasonable expectation of success in combining Schutz and Takahashi, because the combination would represent a simple integration of Schutz’s “IC temperature sensor 32” into Takahashi’s system for generating optimum source voltages for “device 200.” MTK-1003, ¶¶261-62. Employing Schutz’s “IC temperature sensor 32” would have required routine electrical or computer engineering knowledge and was a task well within the skill of a POSITA. *Id.* Incorporating Schutz’s temperature sensing to account for temperature variation in addition to the “effect of variations in the production process” would provide additional improvements in performance and power consumption for “device 200.” *Id.*

4. Claim 19

Supra Claim 7. MTK-1003, ¶263.

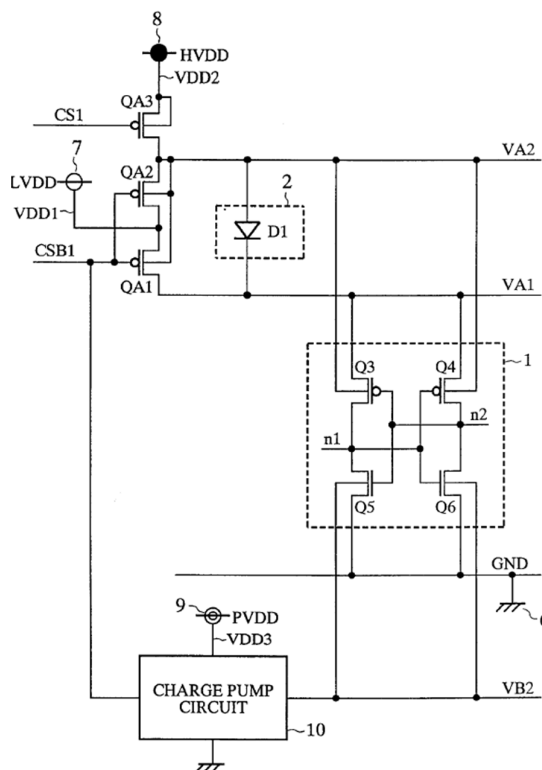
C. GROUND 1C—CLAIMS 9 AND 15 ARE OBVIOUS OVER TAKAHASHI IN VIEW OF NOTANI

1. Overview of Notani

Notani relates to “a semiconductor integrated circuit capable of reducing a power consumption by controlling supply of power for an internal circuit in accordance with an active state and a sleep state of the internal circuit.” MTK-1025, 1:6-9. MTK-1003, ¶¶264-267. According to Notani, Figure 1 “is a circuit

diagram for illustrating a semiconductor integrated circuit according to an embodiment 1 of this invention.” MTK-1025, 4:38-40.

FIG.1



MTK-1025, FIG. 1

“The charge pump circuit 10 is supplied with the voltages on the power supply lines VDD3 and GND, and drives the substrate power supply line VB2 in response to the control signal CSB1.” *Id.* at 5:7-10. “The control signals CS1 and CSB1 are produced by a control circuit (not depicted) of the semiconductor integrated circuit, and are complementary signals which are representative of whether the internal circuit 1 is at the active state or the sleep state.” *Id.* at 5:65-6:2. “When the internal circuit 1 is at the active state, the control signals CS1 and

CB1 have H level and L level, respectively. When the internal circuit 1 is at the sleep state, the control signals CS1 and CB1 have L level and H level, respectively.” *Id.* at 6:2-6.

2. Takahashi-Notani Combination

A POSITA would have been motivated to modify Takahashi’s integrated circuit to incorporate the teachings of Notani with a reasonable expectation of success. MTK-1003, ¶¶268- Both Takahashi and Notani are directed to optimizing power to integrated circuits, including to reduce power consumption. MTK-1004, [0001], [0002], [0017]; MTK-1025, Title, 1:6-9 (“semiconductor integrated circuit capable of reducing power consumption by controlling supply of power for an internal circuit in accordance with an active state and a sleep state of the internal circuit”). The ’438 Patent relates to this same field of endeavor. *See* MTK-1001, Abstract, 1:25-35; 2:33-46; MTK-1003, ¶268.

Takahashi and Notani also address the same known power consumption problem in the same way. MTK-1003, ¶269. As discussed above, both Takahashi and Notani reduce overall power consumption by placing circuit blocks into a low-power standby (i.e., sleep) mode when not in operation. *See, e.g.,* MTK-1004, [0017], [0052]-[0053], [0094]-[0095]; MTK-1025, Abstract, 1:6-9, 2:31-34, 2:64-3:10, 5:65-6:19, 8:5-24, 8:44-56; MTK-1003, ¶269. Takahashi does so using a “voltage regulator” that “controls the level of voltage to be supplied to device 200,” where the voltage is received by the power islands’

sleep transistors to facilitate reduction of power consumed by the power islands' circuitries. MTK-1004, [0098], FIGS. 1 and 16; MTK-1003, ¶269. Notani does so using a "voltage generating circuit" that comprises a "charge pump" and outputs a "ground voltage on an active state" and a "voltage which is lower than the ground voltage, on the sleep state." MTK-1025, Abstract, 3:11-20, 4:38-47, 5:7-10, FIGS. 1 and 5.

Similarities across Takahashi's and Notani's teachings would have led a POSITA to employ Notani's charge pump within Takahashi's "voltage regulator" to improve Takahashi's ability to reduce power consumption, including that resulting from leakage currents. MTK-1003, ¶270.⁹ For example, Takahashi discloses that "[v]oltage regulator 100 controls the levels of source voltages V_{dd1} , V_{dd2} , and V_{dd3} supplied to device 200 using predetermined optimum values according to control signal S_C indicating control data DAT and the operating condition of the device." MTK-1004, [0109]-[0117], Figures 14-17.

As discussed for Ground 1A, a POSITA would have understood that **how** Takahashi's voltage regulator generates source voltages V_{dd1} , V_{dd2} , and V_{dd3} is

⁹ As explained at Ground 1A, Takahashi by itself discloses and renders obvious a sleep generator comprising a charge pump. MTK-1003, ¶270n.7. If Takahashi fails to render obvious this feature, Takahashi in combination with Notani does so.

merely a design choice with a finite number of well-known solutions. MTK-1003, ¶¶271, 64-73. One such method for generating a regulated voltage is using a charge pump. *Id.* A POSITA would have understood that by utilizing Notani's charge pump circuit, "a known circuit," MTK-1025, 7:12-13, "it is possible to reduce the leakage current," *id.*, 9:28-37. MTK-1003, ¶¶271, 64-73.

Because Takahashi and Notani provide a similar solution to a similar problem within the same field of endeavor, a POSITA would have naturally looked at and been motivated to combine them to reduce leakage current and power consumption in Takahashi's system. Specifically, a POSITA would have been motivated to employ Notani's "charge pump" with Takahashi's "voltage regulator" to power down circuits within Takahashi's "device 200" when not in use. MTK-1003, ¶¶272-273.

A POSITA would have understood that employing Notani's charge pump in Takahashi's "voltage regulator" to control the power to individual circuits would have been readily implemented by a POSITA with predictable results. MTK-1003, ¶¶272-273. The use of charge pumps was a well-known solution for efficiently controlling an integrated circuit, and a POSITA would have needed only routine electrical and computer engineering principles to implement a charge pump with Takahashi's "voltage regulator." MTK-1003, ¶273. Such a combination would predictably reduce the overall power consumption of "device

200” by reducing the power consumption of inactive circuits even while “device 200” remains operational. *Id.*

3. Claim 9

The Takahashi-Notani combination renders obvious Claim 9. MTK-1003, ¶¶274-275. Notani discloses a “voltage generating circuit” that comprises a “charge pump” and outputs a “ground voltage on an active state” and a “voltage which is lower than the ground voltage, on the sleep state.” MTK-1025, Abstract, 3:11-20, 4:38-47, 5:7-10, 9:66-10:6, 10:49-54; FIGS. 1 and 5. “The charge pump circuit 10 is supplied with the voltages on the power supply lines VDD3 and GND, and drives the substrate power supply line VB2 in response to the *control signal CSB1*.” *Id.* at 5:7-10.

From Notani’s teachings, a POSITA would have found it obvious for Takahashi’s “voltage regulator” to generate an optimum voltage in response to a control signal, i.e., “*control signal S_C*,” using a charge pump, which was a “known circuit,” MTK-1025, 7:12-13, at the time of the alleged invention. MTK-1003, ¶276. A POSITA would have had a reasonable expectation of success in combining Notani and Takahashi, because the combination would represent a simple integration of Notani’s “charge pump” into Takahashi’s “voltage regulator” for generating optimum source voltages for “device 200.” MTK-1003, ¶¶276-277. Employing Notani’s “charge pump” would have required merely routine electrical or computer engineering knowledge and was a

task well within the skill of a POSITA. *Id.* Incorporating Notani’s charge pump would provide additional improvements in performance and power consumption for “device 200.” *Id.*

4. Claim 15

Supra Claim 9; Ground 1A, Claims 1, 8, 12. MTK-1003, ¶¶278-281.

D. GROUND 2A—CLAIMS 1-19 ARE OBVIOUS OVER MIZUNO

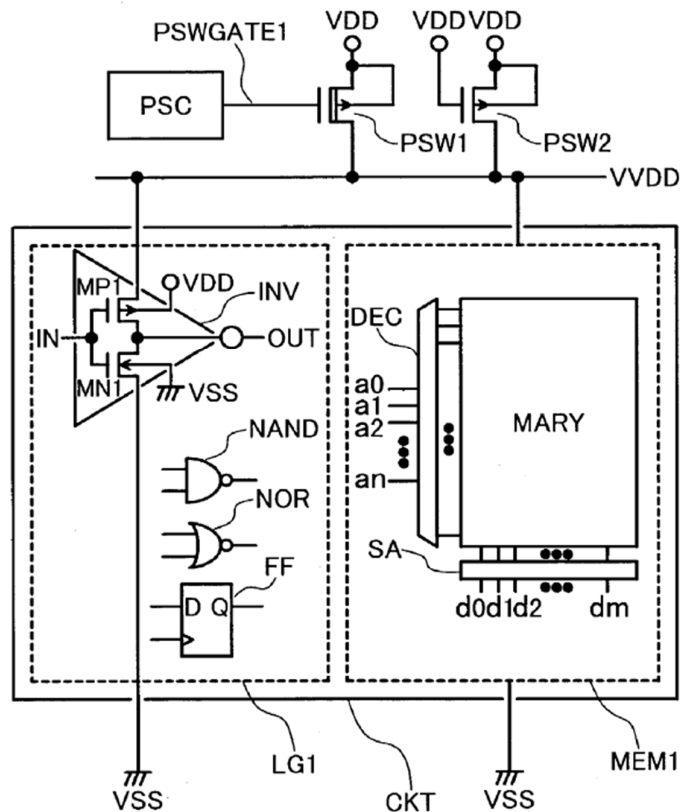
1. Overview of Mizuno

Mizuno relates to “a semiconductor integrated circuit device with excellent high speed and low power operation characteristics.” MTK-1005, [0001]; MTK-1003, ¶¶283-284. Mizuno’s integrated circuit device contains a “leakage current control circuit” that is coupled to a “circuit block CKT.” MTK-1005, Abstract, [0008]-[0009], [0053]. The “leakage current control circuit” is provided to “reduc[e] the different types of leakage current ...while the circuit block is in standby state,” while still “allow[ing] high speed circuit block operation while the circuit block is in the operation state.” MTK-1005, Abstract, [0008]-[0009].

Figures 1-30 depict one embodiment of Mizuno’s integrated circuit device. MTK-1005, [0052]-[0107]; MTK-1003, ¶¶285-286. In this embodiment, “power switch controller PSC controls the on and off operation of the power switch PSW1 connected between the power supply VDD and the virtual power line VVDD” and “also controls the current flow in the power supply VDD and the virtual power line VVDD.” MTK-1005, [0054]; MTK-1003, ¶¶285-286. The

“power supplied to the circuit block during operation is mainly supplied from the power switch [PSW1]; and the currently supplied to the circuit block during standby operation is mainly supplied to the current source PSW2.” MTK-1005, [0054]; MTK-1003, ¶¶285-286.

FIG.1

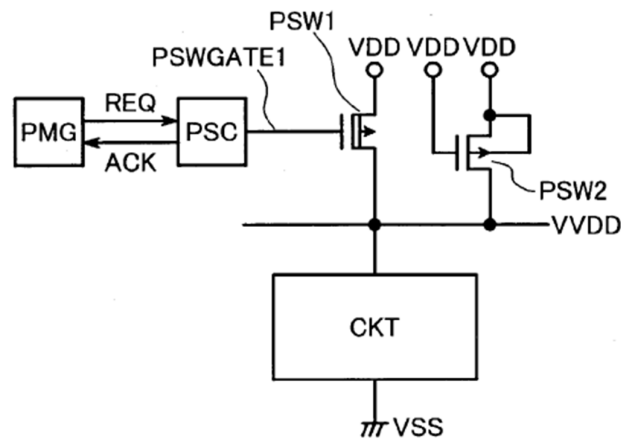


MTK-1005, FIG. 1

A “power controlling circuit PMG” shown in Figure 22 communicates with “power switch controller PSC by means of the request line REQ and response line ACK [to control] the on/off operation of the power switch PSW1

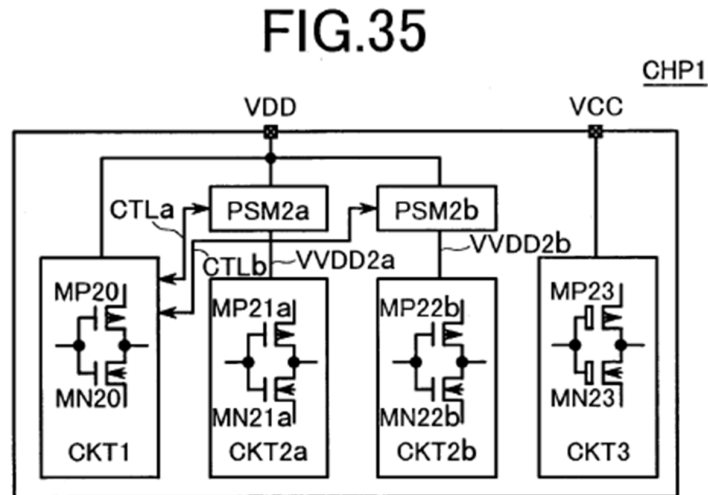
and [control] the state of the circuit block.” MTK-1005, [0093]; MTK-1003, ¶¶286-288.

FIG.22



MTK-1005, FIG. 22

In a related embodiment depicted in Figures 35-40, an integrated circuit chip includes multiple circuit blocks whose power is provided either directly or via “leakage reduction circuits.” MTK-1005, [0120]-[0134]; MTK-1003, ¶¶289-290. Mizuno explains that “the various adaptations and specific examples disclosed for the first embodiment are also applicable to the leakage current reduction circuit of the third embodiment.” MTK-1005, [0130]. By controlling the leakage currents through individual circuit blocks using “multiple leakage control circuits [PSM2a, PSM2b] as in FIG. 35 ... the leakage current of the overall chip can be efficiently reduced.” MTK-1005, [0122]; MTK-1003, ¶¶289-290.



MTK-1005, FIG. 35

2. Claim 1

(a) Element 1[p]

To the extent the preamble is limiting, Mizuno discloses methods carried out in “a semiconductor integrated circuit device with excellent high speed and low power operation characteristics.” MTK-1005, Title, [0001]; MTK-1003, ¶¶291-293.

(b) Element 1[a]

Mizuno discloses a plurality of power islands having associated power consumptions, each of the power islands including circuitries and sleep transistors in coupled relation with the circuitries. MTK-1003, ¶¶294.

The '438 patent describes a power island. *See* Ground 1A, element 1[a]. MTK-1001, 3:62-65. A POSITA would have understood and found obvious that Mizuno discloses multiple such power islands, each of which includes sleep transistors and circuitries coupled with one another. MTK-1003, ¶¶295.

First, Mizuno discloses a “first embodiment,” in Figures 1-30. *See* MTK-1005, [0052]-[0107]. A POSITA would have understood and found obvious that, within this “first embodiment,” Mizuno’s “circuit block CKT,” depicted in Figures 1 and 22 below and which may include a “logic circuit LG1” and/or a “memory MEM1,” MTK-1005, [0053], coupled to a power switch PSW1, comprises a power island. MTK-1003, ¶296.

FIG.1

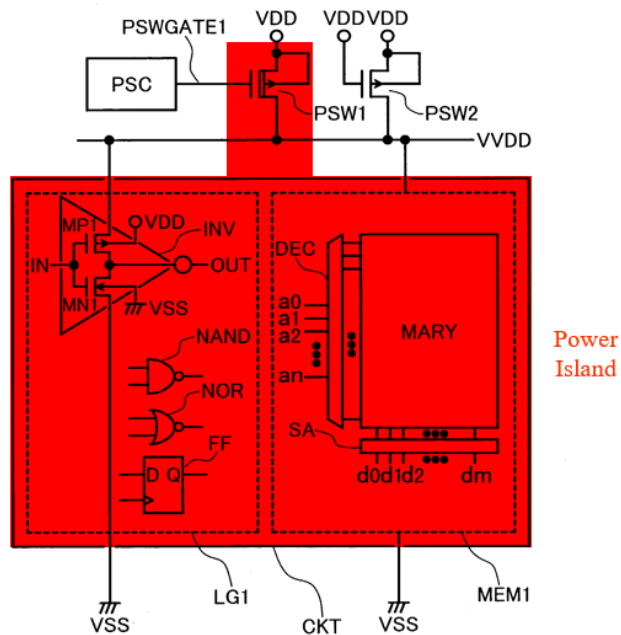
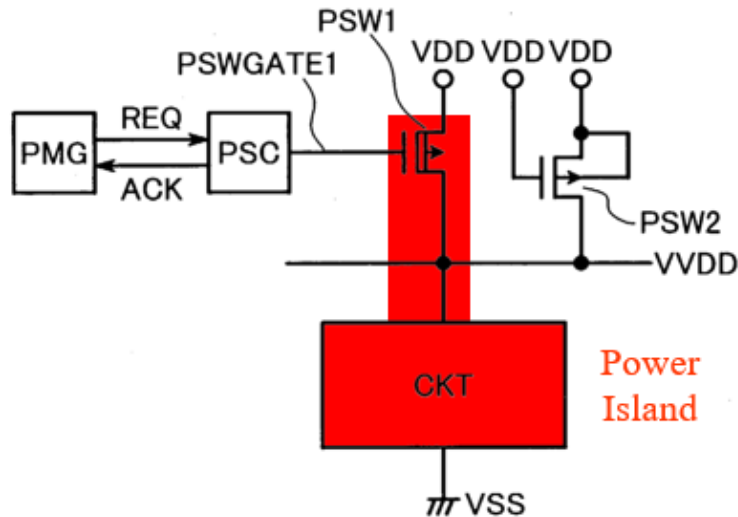


FIG.22



MTK-1005, FIGS. 1 and 22

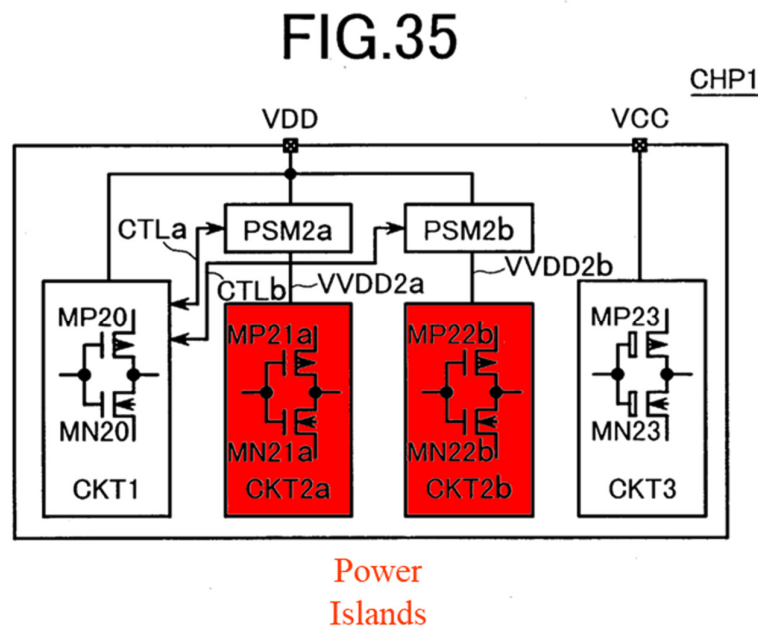
Mizuno's integrated circuit includes a "circuit block CKT as shown for example in FIG. 1 contain[ing] a logic circuit LG1 ... and a memory MEM1,"¹⁰ and a "power switch PSW1." MTK-1005, [0053]. A POSITA would have understood and found it obvious that Mizuno's "circuit block CKT," comprising a "logic circuit LG1" and/or "memory MEM1," when coupled with power switch PSW1, is a power island because power consumption is controlled within it. *Id.*, [0054]; MTK-1003, ¶297; MTK-1001, 3:62-65.

¹⁰ Mizuno discloses that "circuit block CKT may ... be comprised only of a logic circuit LG1 or a memory MEM1," and need not include both. MTK-1005, [0053].

A POSITA would have understood that Mizuno's "circuit block CKT" is a "circuitry," and that Mizuno's "power switch PSW1" is a "sleep transistor." MTK-1003, ¶298. Mizuno's "PSW1" "utilize[s] PMOS transistors," MTK-1005, [0089], and during an "operating state," "power is supplied to the circuit block CKT by way of the power switch PSW1 so that the virtual power line VVDD reaches VDD potential and the circuit block CKT is operable." *Id.*, [0055]. Conversely, during "standby," the "power switch PSW1 turns off" and "voltage (or voltage potential) of virtual power line VVDD gradually discharges ... to ground VSS." *Id.*, [0054]-[0055]. "As the voltage of the virtual power line VVDD becomes lower ... [t]he leakage current flowing to circuit block CKT ... also gradually becomes a smaller value," thereby reducing the power consumption of the circuit block CKT during standby. *Id.*; MTK-1003, ¶298.

In standby, leakage current through "power switch PSW1" is substantially less than that through "current source PSW2" (i.e., " $I_{\text{off}}(\text{PSW1}) \ll I_{\text{off}}(\text{PSW2})$ ") such that "current source PSW2 functions as a leak current limiter circuit for circuit block CKT." MTK-1005, [0055]-[0057], [0085], [0093], [0122]; MTK-1003, ¶299. Thus, a POSITA would have understood and found obvious that Mizuno's "power switch PSW1" and "current source PSW2" are sleep transistors that reduce leakage in the integrated circuit during standby to facilitate reduction of power consumed by the circuitries in "CKT1." MTK-1003, ¶¶300-306; MTK-1001, Abstract, 2:5-17, 2:42-47, 4:18-5:4, 7:10-15.

Second, a POSITA would have understood and/or found it obvious that Mizuno discloses an embodiment having a plurality of power islands. MTK-1003, ¶¶307-310. Specifically, Mizuno discloses a related “third embodiment” in FIGS. 35-40, of an integrated circuit having multiple “circuit blocks” that are power islands.

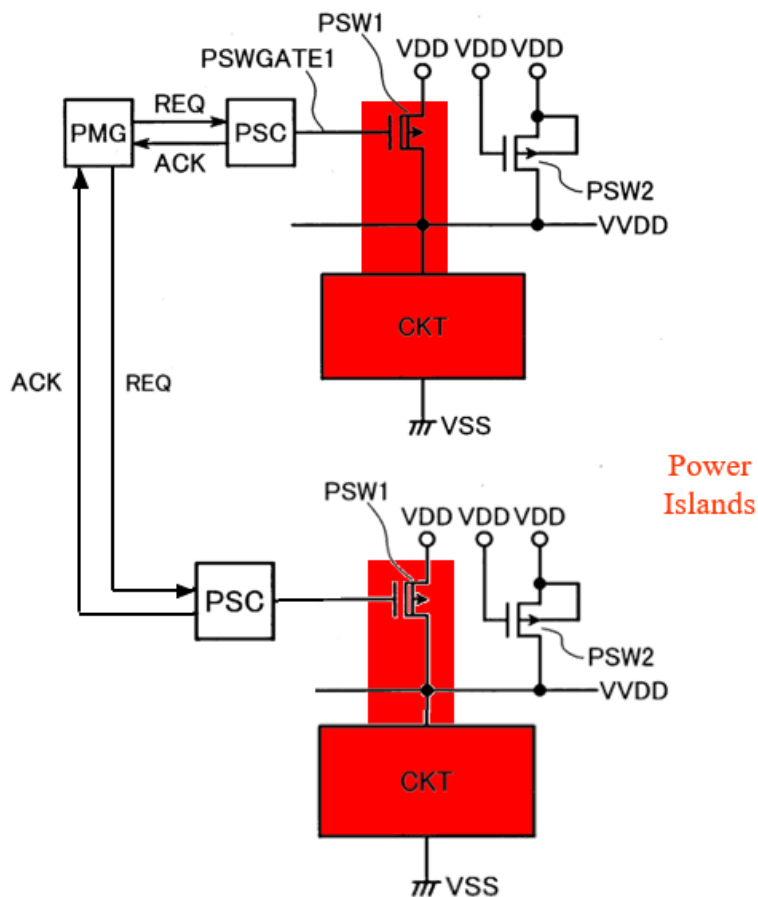


MTK-1005, FIG. 35

In the embodiment of FIGS. 35-40, “leakage reduction circuits PSM2a and PSM2b,” which are similar to the leakage reduction circuits in the embodiment of FIGS. 1-30, control/dynamically change power within the circuit blocks CKT2a and CKT2b, respectively. MTK-1003, ¶¶311-15; MTK-1005, [0121]-[0133]. Thus, a POSITA would have understood and found obvious that Mizuno’s integrated circuit in FIGS. 35-40 includes multiple power islands. MTK-1003, ¶315.

Finally, it would have been obvious to a POSITA to include multiple power islands in Mizuno's "first embodiment" (FIGS. 1-30), as shown below, based at least on Mizuno's disclosures with respect to its related "third embodiment" (FIGS. 35-40). MTK-1003, ¶¶316-317.

FIG.22



MTK-1005, FIG. 22 (as modified)¹¹

Indeed, a POSITA would have understood that the various adaptations and examples disclosed for the embodiments depicted in FIGS. 1-30 and 35-40, respectively, are applicable to one another. *Id.*; *see also, e.g.*, MTK-1005, [0130] (“[T]he various adaptations and specific examples disclosed for the first embodiment are also applicable ... the third embodiment”). A POSITA would have been motivated to include multiple leakage current reduction circuits and power islands in its “first embodiment” because, according to Mizuno, “[b]y establishing multiple leakage control circuits as in FIG. 35, and controlling the leakage current of circuits grouped in multiple circuits integrated onto the chip, the leakage current of the overall chip can be efficiently reduced.” MTK-1005, [0122]; MTK-1003, ¶317.

A POSITA would have had a reasonable expectation of success in including multiple power islands within Mizuno’s “first embodiment” depicted in FIGS. 1-30, because the combination would represent a simple integration of additional circuit blocks into Mizuno’s system for controlling the putting to sleep

¹¹ A POSITA would have understood that the “PMG” in FIG. 22 corresponds to the “CKT1” circuit in FIG. 35, and that FIG. 35’s “CTLa, CTLb [] leakage control lines” are “equivalent to the request line REQ and response line ACK of FIG. 22.” MTK-1005, [0121]; MTK-1003, ¶316n.9.

and taking out of sleep of Mizuno's power islands. MTK-1003, ¶318. Including multiple power islands in Mizuno's "first embodiment," as was already done in Mizuno's related "third embodiment," would have required merely routine electrical or computer programming knowledge and was a task well within the skill of a POSITA. *Id.*

As noted above with respect to Ground 1A, "power island" has been construed in prior litigations involving a patent describing similar subject matter, U.S. Patent No. 7,051,306. *See* MTK-1003, ¶320n.12; MTK-1032 43-44, 44-46; MTK-1033 28-29, 29-34. For purposes of this Petition, Petitioner submits that no construction is necessary because plain and ordinary meaning suffices. And while the prior constructions involved a different patent and different claims and are not binding on this proceeding, Mizuno's disclosures, in light of a POSITA's knowledge, also render this term obvious under the prior constructions. *See* MTK-1003, ¶320n.10.

(c) Element 1[b]

Mizuno's integrated circuit also includes a power island manager in communication with at least one of the power islands. MTK1003, ¶321-325. Mizuno includes a "power switch controller PSC" that "controls the on and off operation of the power switch PSW1 connected between the power supply VDD and the virtual power line VVDD" that powers "circuit block CKT." MTK-1005, [0054], [0093]. During operation, the "PSC" turns on "power switch PSW 1" so

that “the current supplied to the circuit block ... is mainly supplied from power switch [PSW1].” *Id.* During standby, the “PSC” turns off “power switch PSW1” and “the current supplied to the circuit block ... is mainly supplied [by] the current source PSW2.” *Id.* “[T]he size of the respective leakage currents ... during standby in the circuit block are determined by the current source PSW 2” and “is smaller than the leakage current flowing in the circuit block CKT during operation.” MTK-1005, [0059].

FIG.1

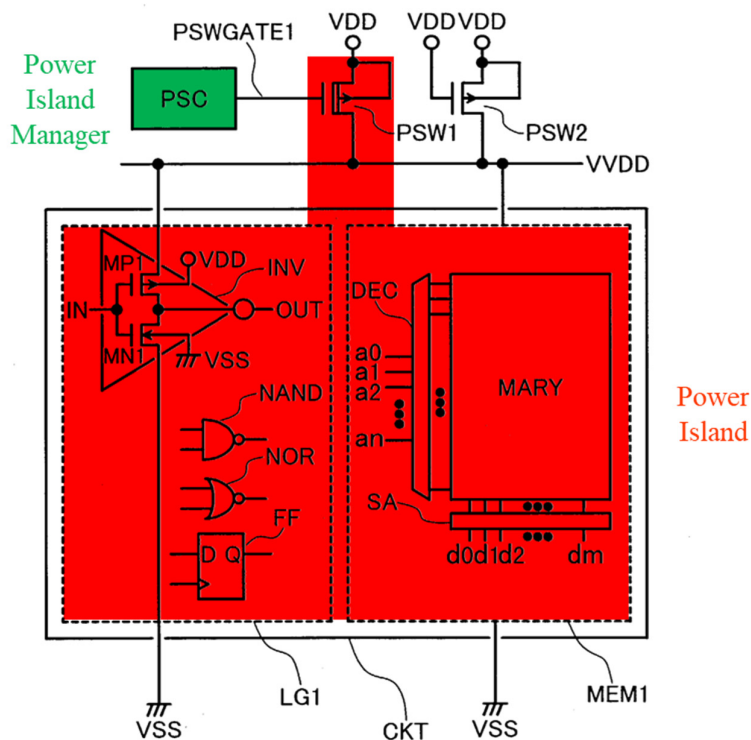
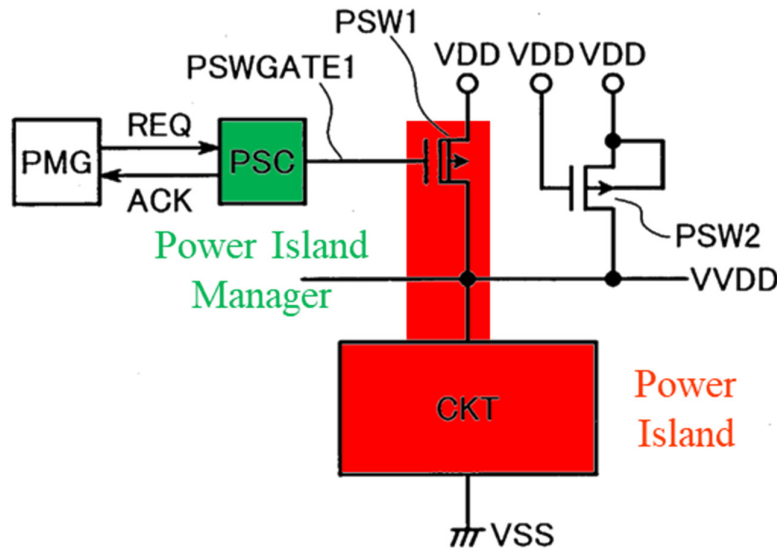
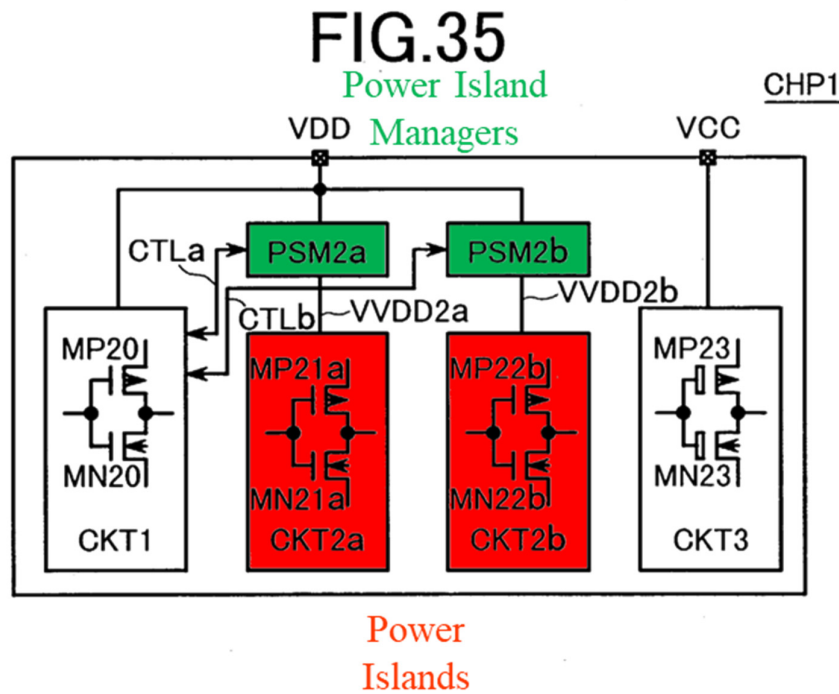


FIG.22



MTK-1005, FIGS. 1, 22

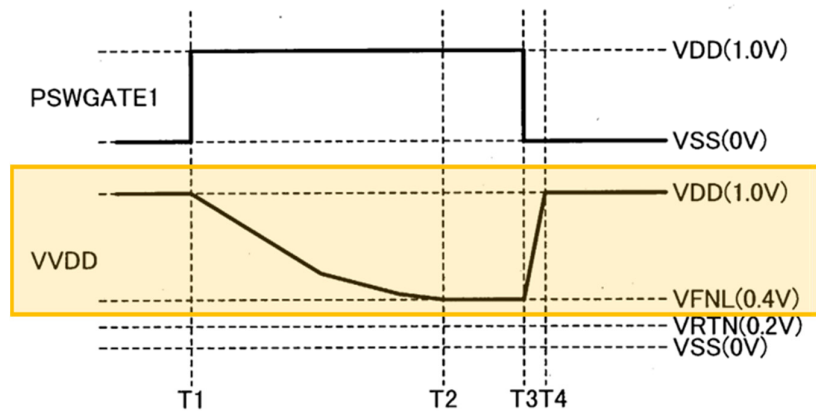
A POSITA would have understood and found obvious that Mizuno's "power switch controller PSC" is a power manager because it controls power within "circuit block CKT" by "modify[ing] the voltage within the power island." See MTK-1001, 4:8-11; MTK-1003, ¶¶322-325. Similarly, in the embodiment of Figures 35-40, "leakage reduction circuits PSM2a and PSM2b" include power managers that control power within the circuit blocks CKT2a and CKT2b, respectively. MTK-1003, ¶326; MTK-1005, [0121]-[0133].



MTK-1005, FIG. 35

Thus, Mizuno's "PSC" is configured to dynamically change the power consumptions of the power islands based on the needs and operation of the integrated circuit. MTK-1003, ¶¶326-328. Depending on whether the integrated circuit requires "CKT1" to be operational, the "PSC" "controls the on and off operation of the power switch PSW1 connected between the power supply VDD and the virtual power line VVDD" that powers "circuit block CKT." MTK-1005, [0054], [0093]. As shown in Figure 2 of Mizuno, based on the "PSC" turning the "power switch PSW1" on or off based on the output "PSWGATE1," "virtual power line VVDD" powering "CKT1" changes so that "circuit block CKT is operable (in operating state)" or in standby. *Id.*, [0055].

FIG.2

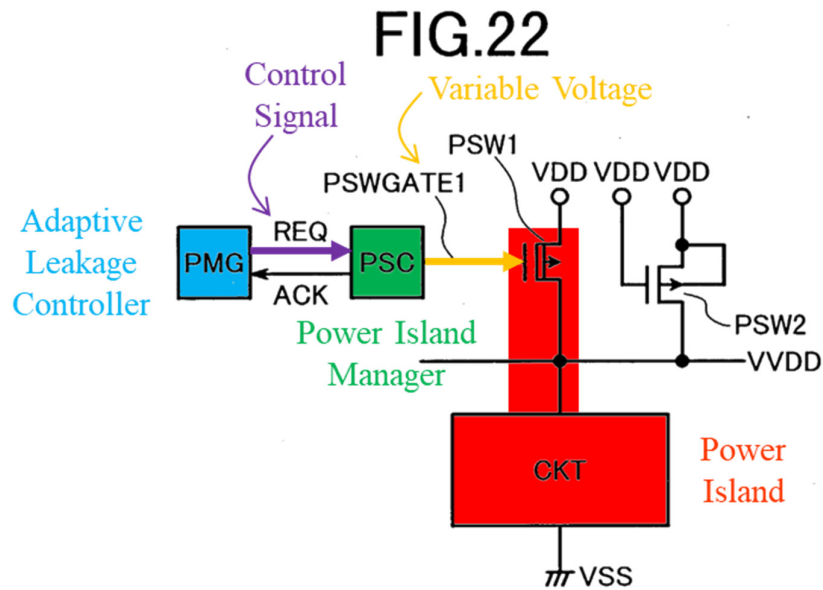


MTK-1003, FIG. 2

Thus, as in the '438 patent, Mizuno's "power switch controller PSC" "control[s] power within [each] power island by "modify[ing] the voltage within the power island" based on whether the power island needs to be operational or can be placed into standby. MTK-1001, 4:11-14, MTK-1003, ¶329-330.

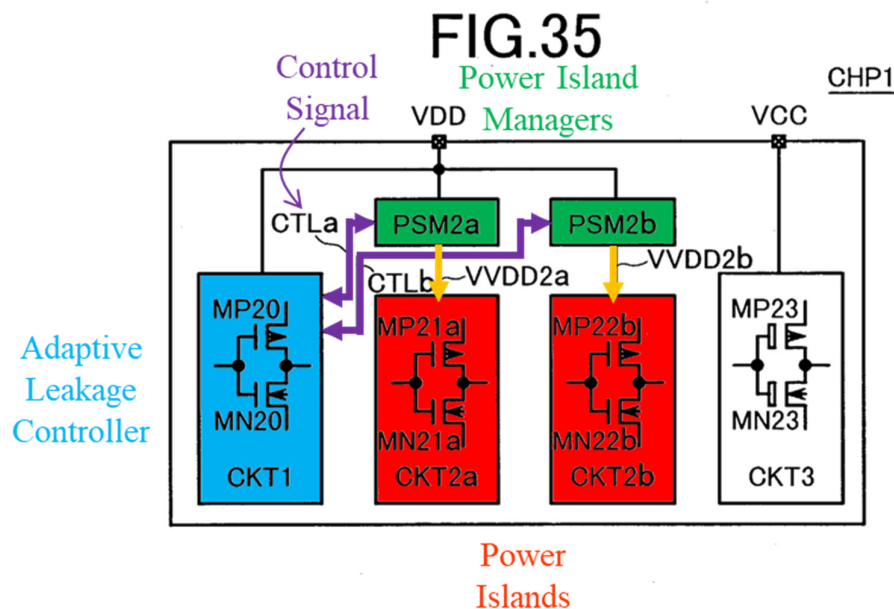
(d) Element 1[c]

Mizuno's integrated circuit includes a "power controlling circuit PMG" that discloses and renders obvious an adaptive leakage controller. MTK-1003, ¶¶331-333. "[P]ower controller circuit PMG ... reduces power consumption in the chip overall" by controlling the "PSC by means of the request line REQ and response line ACK." MTK-1005, [0093]. Based on "REQ" and "ACK" control signals, "power switch controller PSC" (*i.e.*, power island manager) generates variable voltage "PSWGATE1" to turn "power switch PSW1" on or off. *See id.*, [0055].



MTK-1005, FIG. 22

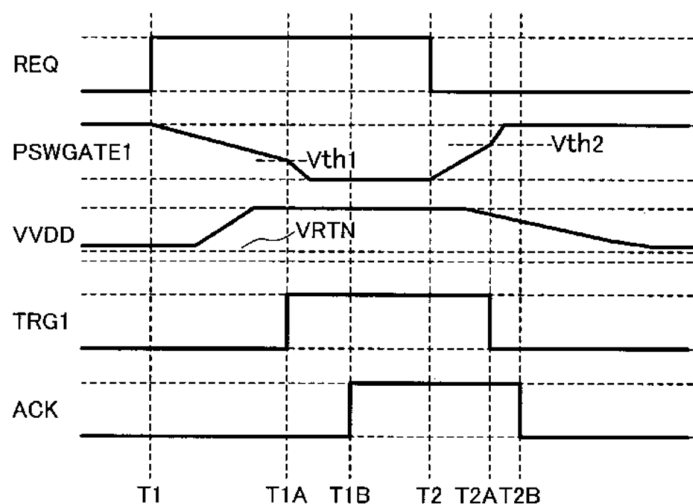
Similarly, in the embodiment of Figures 35-40, “circuit block CKT1” has “circuits to control the leakage reduction circuits PSM2a and PSM2b” over “CTLa, CTLb ... leakage control lines” that are “equivalent to the request line REQ and response line ACK of FIG. 22.” *Id.*, [0121]; MTK-1003, ¶¶334-336.



MTK-1005, FIG. 35

“[S]etting the request line REQ to high level turns on the power switch PSW1” to provide the “circuit block CKT” with an operating voltage VDD through “power switch PSW1.” *Id.*, [0093]. “Conversely, when the request line REQ is set to low level, the power switch PSW1 turns off” and the “circuit block CKT” receives a lower voltage through “current source PSW2 [that] functions as a leak current limiter circuit.” *Id.*, [0057], [0093]; MTK-1003, ¶¶334-336. As shown in Figure 24, for instance, when Mizuno’s “power controlling circuit PMG” sets “REQ” from high to low, voltage “VVDD” to “circuit block CKT” decreases from VDD to VRTN and leakage current “Ioff(CKT)” through “circuit block CKT” also reduces. MTK-1005, [0096]-[0098]; MTK-1003, ¶335; *see also* MTK-1005, [0055]-[0056], [0065]-[0066], FIG. 5.

FIG.24



MTK-1005, FIG. 24

Thus, a POSITA would understand and find obvious that Mizuno’s “power controlling circuit PMG” (“circuit block CKT1” in Figures 35-40) is an adaptive leakage controller configured to control change of a variable voltage “PSWGATE1” applied to “power switch PSW1” (*i.e.*, sleep transistor) by providing control signals to the “PSC” (*i.e.*, power island manager). MTK-1003, ¶336. In turn, the power to “circuit block CKT” is optimized to reduce power consumption due to leakage currents during standby and to place “circuit block CKT” into operating mode when in use. MTK-1001, 4:21-23, MTK-1003, ¶¶336.¹²

3. Claim 2

¹² To the extent the claimed “adaptive leakage controller” must provide control signals to compensate for process and temperature variation to provide an optimum voltage to sleep transistors, Mizuno discloses and renders obvious those features. Mizuno discloses that the voltages provided to the “power switch PSW1” such as VREF and VDD2a in Figures 35-40 are optimized based on the operating status and “variations (non-uniformities) in chip manufacture or information on environmental fluctuations.” MTK-1005, [0126]-[0128]; MTK-1003, ¶¶337-345. A POSITA would understand and find obvious that such information would be provided via the signal CTLa. *Id.*

As discussed at element 1[c], Mizuno’s “circuit block CKT” is put into standby and taken out of standby at different times to reduce power consumption when “circuit block CKT” is not being used. MTK-1005, [0087], [0093]; MTK-1003, ¶¶346-347.¹³ Specifically, the “PSC” puts “circuit block CKT”—including “logic circuit LG1” and “memory MEM1”—into standby or operational modes at different times by controlling “the on and off operation of the power switch PSW1” and “current flow in the power supply VDD and the virtual power line VVDD.” MTK-1005, [0054]; MTK-1003, ¶¶347.

To the extent required by Claim 2, Mizuno also discloses and renders obvious that power islands can be placed into standby and operational states at different times from other power islands. MTK-1003, ¶¶350-351. As discussed at element 1[a], the embodiment of Figures 35-40 includes multiple “leakage

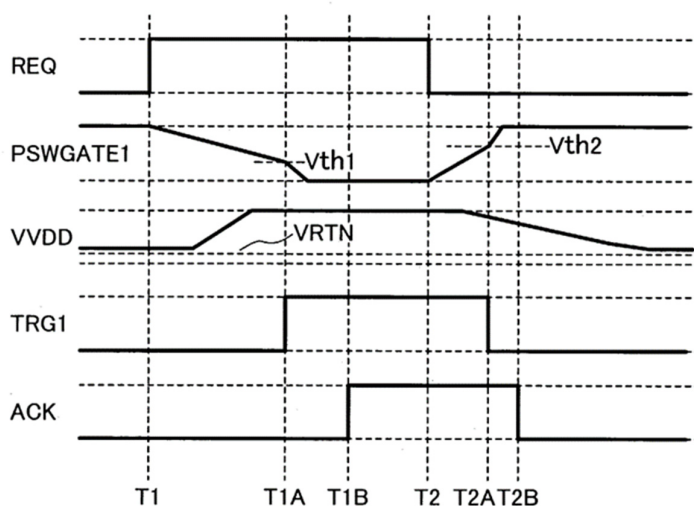
¹³ Mizuno discloses both a “standby (idle)” state that maintains “information within the information retention circuits within the circuit block,” as well as a “deep stand-by state” in which “information in the information retention circuit within the circuit block will be lost.” MTK-1005, [0005], [0087]. The benefit of the “deep stand-by state” is that power to the “circuit block CKT” can be reduced even further to achieve “lower power consumption than in stand-by state with data retention.” *Id.*, [0087]. A POSITA would have understood that both types of standby states are “sleep” states. MTK-1003, ¶¶348-349.

reduction circuits PSM2a and PSM2b” that control “the leakage current of circuits grouped in multiple circuits integrated onto the chip.” MTK-1005, [0121]-[0122]; MTK-1003, ¶¶350-351. Mizuno explains that “leakage reduction circuits PSM2a and PSM2b” are controlled by “CTLa, CTLb ... leakage control lines of the leakage reduction circuit” that are “equivalent to the request line REQ and response line ACK of FIG. 22.” MTK-1005, [0122]. Thus, one of “[c]ircuit blocks CKT2a and CKT2b” can be placed into standby or operational mode at a different time from another using the control lines “CTLa, CTLb.” MTK-1005, [0093], [0121]; MTK-1003, ¶¶350-351.

4. Claim 3

A POSITA would have understood and found obvious that Mizuno’s “PSC” power manager includes a state machine with distinct output states to control putting a power island into standby (“sleep”) and operational (“out of sleep”) states. MTK-1003, ¶¶352-353, 358-65; *see* MTK-1001, 6:16-18; MTK-1008; MTK-1009; *see also* MTK-1006, 2:63-3:6, 7:20-50, 9:42-63, FIG. 4.

In Figures 23-24, when “REQ reaches high level” to initiate a “shift[] from standby to the operation state” (time T1), the “PSC” enters a first state in which “gate signal PSWGATE1 is driven to high impedance by C1 by way of the C1DRV control circuit.” MTK-1005, [0096]; MTK-1003, ¶¶354-355.



Once “PSWGATE1” reaches a “level (Vth1) at time T1A,” the “PSC” enters a second state in which “PSWGATE1 is ... driven to a low impedance by C2 by way of the C2DRV control circuit” and “TRG1 is driven to high level by the timer TIM1.” *Id.* Finally, at time T1B, the “PSC” enters a third state in which “ACK is driven to high level” and “virtual power line VVDD may be fully

charged up to ... VDD.” *Id.* Mizuno describes a similar state machine process for the “shift[] from the operation state to standby state.” MTK-1005, [0097]-[0101], MTK-1003, ¶¶356-357, 363-365.¹⁴

5. Claim 4

A POSITA would have understood and found it obvious that Mizuno’s power islands are delineated based on functional IP units of the integrated circuit. MTK-1003, ¶366. As discussed for element 1[a], a POSITA would have understood and found obvious that Mizuno’s power island, depicted in Figures 1 and 22, includes a “*logic circuit LG1*” and/or a “*memory MEM1*,” MTK-1005, [0053], which together comprise the power island’s “circuit block CKT.” MTK-1005, FIGS. 1 and 22; MTK-1003, ¶367.

As discussed with respect to claim 4 of Ground 1A, *supra*, a POSITA would have understood that an “IP unit” refers to a predefined and reusable integrated circuit component, *e.g.*, a logic unit, memory cell, or functional block, that is the IP of one party. MTK-1026; MTK-1027; MTK-1003, ¶368. Thus, a POSITA would have understood and found it obvious that Mizuno’s power islands, like the ’438 patent’s power islands, include logic circuits (*e.g.*, “logic

¹⁴ A POSITA would have understood that the examples of the “PSC” at Figures 25-30 likewise include a state machine to control transitions between standby and operational states. MTK-1005, [0102]-[0107]; MTK-1003, ¶363.

circuit LG1”) and memories (*e.g.*, “memory MEM1”) that are predefined and verified functional integrated circuit modules, and thus would be functional IP units of the integrated circuit. MTK-1005, [0053], [0065]-[0068], [0070]-[0072], [0075], [0077], [0100], [0110]-[0118], [0121], [0133], FIGS. 1-30, 31, 35-37, 39, claims 1-2, 5, 10, 16-18; MTK-1003, ¶¶369-370.

6. Claim 5

Mizuno discloses and renders obvious that its power islands are delineated by memory, logic, and third-party IP, *e.g.*, a functional block that is the IP of one party. MTK-1003, ¶¶371-375. Mizuno discloses that its “circuit block CKT” can include “**logic circuit** LG1 or a **memory** MEM1.” MTK-1005, [0053], FIG. 1. Mizuno similarly explains that “circuit block” can include third-party IP, such as a “an inverter INV, a NAND circuit NAND, a NOR circuit NOR and a flip-flop circuit FF,” a “word decoder DEC and sensing amplifier SA, etc.” *Id.*; *see also id.* at [0121] (describing circuit blocks CKT1, CKT2a, CKT2b, and CKT3), [0126], [0133]; FIGS. 35-40. A POSITA would have understood that such circuits may be their own third-party IP power islands or part of “logic circuit LG1” and/or “memory MEM1.” *Id.*; MTK-1003, ¶¶374-375.

7. Claim 6

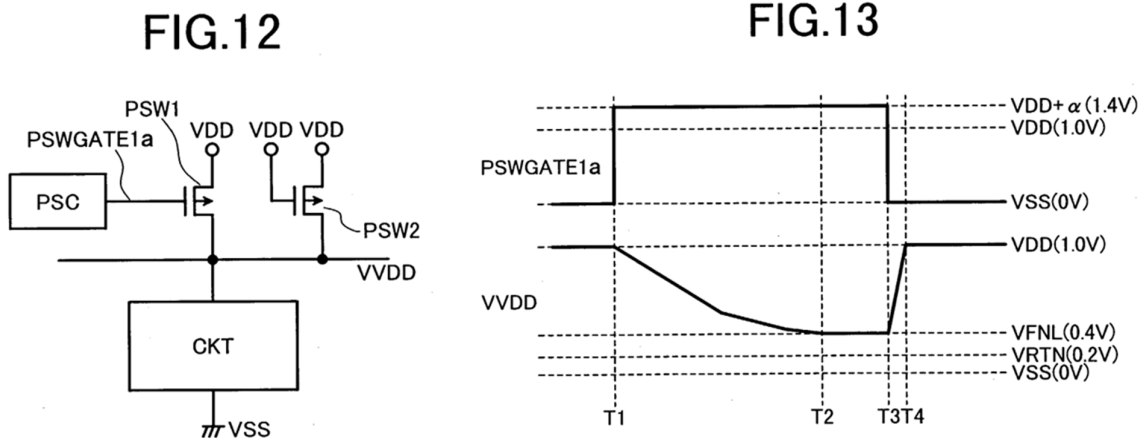
Variable voltage “PSWGATE” is set such that when “gate signal PSWGATE1 of power switch PSW1 is driven to low level by the power switch controller PSC ... the power switch PSW1 turns on,” and when “PSWGATE1 of power switch PSW1 is driven to high level by the power switch controller PSC

... the power switch PSW1 turns off.” MTK-1005, [0055]. The levels of “PSWGATE” are, therefore, optimized to be above or below the threshold voltage of the “power switch PSW1” transistor to turn the switch on or off. MTK-1005, [0058] (“the MOS transistor threshold voltage V_{th} is the gate voltage when the MOS transistor drain current ... starts to flow”), FIGS. 3, 41; MTK-1003, ¶¶376-378.

The threshold voltage of “power switch PSW1” depends on the structure and process used. MTK-1005, [0090]; MTK-1003, ¶¶379-380. To balance “tradeoffs” between “on-resistance per surface area of power switch PSW1 during operation” and “gate tunneling leakage current” during standby, Mizuno proposes a structure with “a thick gate dielectric film for the MOS transistors comprising the power switch PSW1 compared to the MOS transistors comprising the circuit block CKT.” *Id.* Then, “PSWGATE1” is set to an optimum voltage that is sufficiently above or below the threshold voltage of “power switch PSW1” such that “on-resistance during operation can ... be reduced and a power switch with a sufficiently small leakage current during standby can be obtained.” *Id.*; *see also id.*, [0125]-[0126].

During standby, the current in “circuit block CKT” is dominated by “current source PSW2,” such that “ $I_{off}(PSW1) \ll I_{off}(PSW2)$.” MTK-1005, [0057], [0079]. “The condition $I_{off}(PSW1) \ll I(PSW2)$ can be satisfied by selecting device parameters for the power switch PSW1 and the current source

PSW2” and “overdriv[ing] the power switch PSW1 gate signal up to VDD+a during standby” as shown in Figures 12-13. MTK-1005, [0079].



MTK-1005, FIGS. 12-13

By setting “PSWGATE” to the optimum level “VDD+a,” a “reverse bias voltage is ... applied across the source-drain of power switch PSW1 and the Ioff(PSW1) becomes small.” *Id.* Thus, a POSITA would have understood and found obvious that variable voltage “PSWGATE” is an optimum voltage. MTK-1003, ¶¶381-383.

8. Claim 7

As discussed at Claim 6, Mizuno optimizes variable “PSWGATE1” based on variations in the process used for the transistor in “power switch PSW1.” MTK-1003, ¶¶384-385.

As discussed at Claim 7 of Ground 1A, it was well-known that transistor performance is dependent upon process and temperature variations, and Mizuno discloses optimizing voltages to account for such variations. *See, e.g.*, MTK-

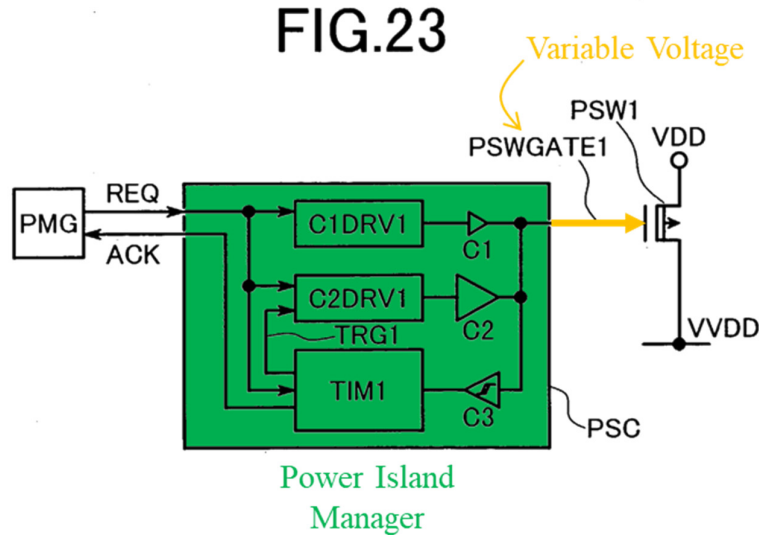
1005, [0064], [0076]-[0077] (adjusting “the substrate bias voltage value applied to the MOS transistor substrate ... according to the process, temperature and power supply voltage”), [0080]-[0081], [0086] (adjusting “output voltage VFNL ... according to the power supply VDD voltage, temperature and process conditions, etc.”), [0126] (“[t]he virtual power line VVDD2a or VVDD2b voltages can also be changed based on the information on variations (non-uniformities) in chip manufacture or information on environmental fluctuations”), [0128]; MTK-1003, ¶¶387-388.

A POSITA therefore would have found it obvious to optimize “PSWGATE1” and other voltages generated by the “PSC” and provided to “power switch PSW1” based on process and temperature variations. MTK-1005, [0090]-[0091] (describing structure for “PSW1” and “PSW2” in which “leakage current flow in the circuit block during standby due to process variations can also be reduced”); MTK-1003, ¶¶389-391.

9. Claim 8

Mizuno’s “PSC” (*i.e.*, power island manager) generates an optimum voltage “PSWGATE1” to turn “power switch PSW1” off during a standby mode. MTK-1003, ¶¶392-394. As shown in Figure 23, during standby “gate signal PSWGATE1” is “first of all driven to high impedance by C1, by way of the C1DRV control circuit for C1.” MTK-1005, [0098]. Then, after “potential detector C3 detects that the gate signal PSWGATE1 was driven to a level V_{th2} ,”

the “PSWGATE1 is ... driven to a low impedance by C2 by way of the C2DRV control circuit for C2.” *Id.*; see also *id.*, [0095], [0103]-[0106].



MTK-1005, FIG. 23

In the related embodiment of Figures 35-40, Mizuno discloses that voltage VVDD2a provided to “power switch PSW1” is generated by “power switch PSW1s.” MTK-1005, FIGS. 27-30, 38; MTK-1003, ¶¶395.

Thus, a POSITA would have understood and found obvious that Mizuno’s “PSC” (*i.e.*, power island manager) includes a sleep generator for generating the optimum voltage provided to the sleep transistor during standby. MTK-1003, ¶¶396-398.

10. Claim 9

A POSITA would have understood and found it obvious for Mizuno’s sleep generator (located within its “PSC” power island manager) to comprise a charge pump. MTK-1003, ¶399. For instance, as already discussed with respect

to element 1[b] and claim 8 above, Mizuno discloses a “PSC” including a sleep generator which controls power within “circuit block CKT” by modifying the voltage within the power island. *See* MTK-1003, ¶400; MTK-1005, [0054], [0093], FIGS. 1 and 22. A POSITA would have understood and found it obvious that Mizuno’s sleep generator generates a regulated voltage that is received by the power islands’ sleep transistors to facilitate reduction of power consumed by the power islands’ circuitries. MTK-1003, ¶400.

A POSITA would have also understood that **how** Mizuno’s sleep generator generates a regulated voltage is merely a design choice with a finite number of well-known solutions. MTK-1003, ¶¶401-402, 64-73; *see also*, Ground 1A, Claim 9, MTK-1028, MTK-1029, MTK-1030, MTK-1031. One such method for generating a regulated voltage is using a charge pump. *Id.* Thus, it would have been obvious to a POSITA to have Mizuno’s sleep generator comprise a charge pump for generating its variable voltages. *See Uber Techs.*, 957 F.3d at 1341. A POSITA would have been able to include a charge pump in Mizuno’s sleep generator to achieve predictable results without any undue experimentation. MTK-1003, ¶¶401-402.

11. Claim 10

Supra 1[b]-1[c] and Claims 6, 8. MTK-1003, ¶403.

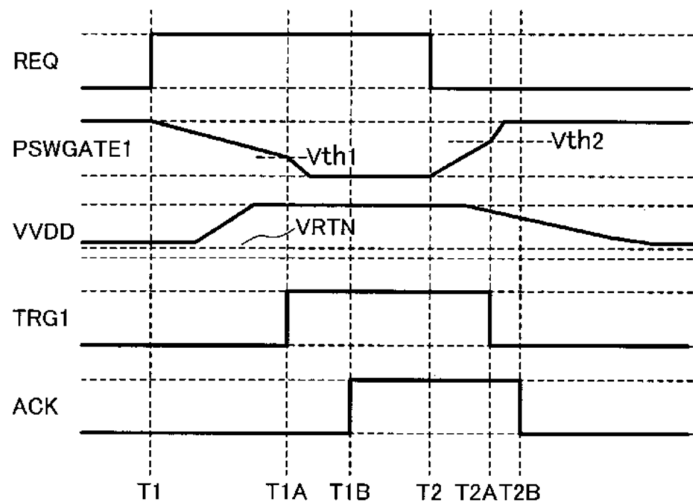
12. Claim 11

Supra 1[b]-1[c] and Claims 6, 8, 10. MTK-1003, ¶404.

13. Claim 12

Mizuno discloses that control signal “REQ” is a digital control signal that takes one of two levels, as shown in Figure 24. MTK-1005, [0093], FIGS. 24, 26, 28, 30; MTK-1003, ¶¶405-407.

FIG.24



MTK-1005, FIG. 24

Specifically, setting “REQ” to the “high level turns on the power switch PSW1 and controls the circuit block CKT in the operation state.” *Id.*

“Conversely, when the request line REQ is set to low level, the power switch PSW1 turns off and the circuit block is controlled to the standby state.” *Id.*

Thus, a POSITA would have understood that “REQ” (and “equivalent” signals “CTL_a, CTL_b”) is a digital control signal, and otherwise would have found it

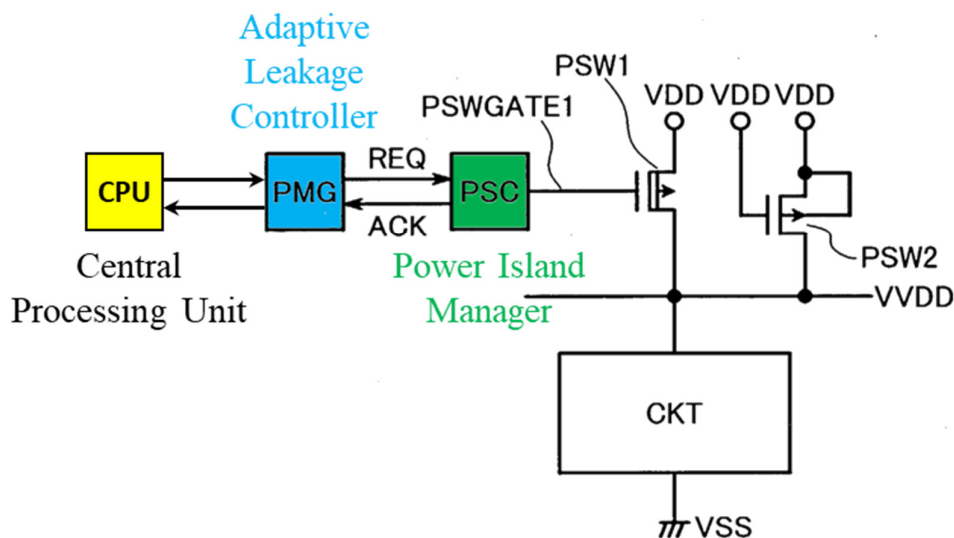
obvious to use a digital signal for “request line REQ.” MTK-1003, ¶¶408-410; MTK-1015; MTK-1016.¹⁵

14. Claim 13

A POSITA would have found it obvious for Mizuno’s integrated circuit to include a central processing unit (CPU) separate from and in communication with the “PSC” (*i.e.*, power island manager). MTK-1003, ¶¶411-415. Mizuno discloses that “power controlling circuit PMG [of Figure 22] that reduces power consumption in the chip overall” is the “external section of the power switch controller.” MTK-1005, [0093]. A POSITA would have understood and found obvious that the power controlling circuit PMG” receives instructions from a CPU, from which it then controls the “PSC” via “REQ” and “ACK” control lines. *Id.*; MTK-1003, ¶¶412-414. Thus, the CPU is separate from and in communication with the “PSC” via “power controlling circuit PMG.” *Id.*

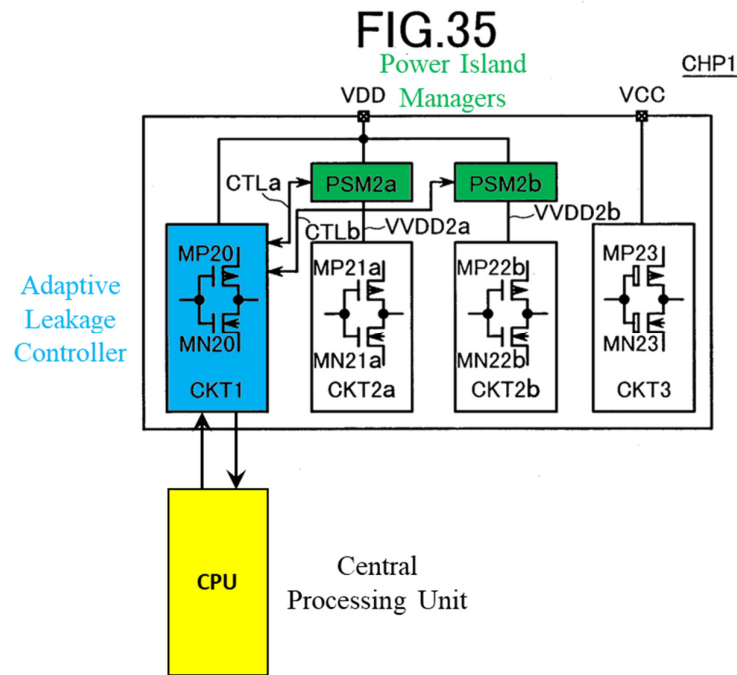
¹⁵ As explained at Claim 12 of Ground 1A, all electrical signals are either digital or analog, such that it also would have been obvious to a POSITA to use a digital signal for “REQ” as one of a finite set of two available options.

FIG.22



MTK-1005, FIG. 22 (as modified)

In the embodiment of Figures 35-40, these operations are performed by “circuit block CKT1,” which uses “CTLa, CTLb ... leakage control lines ... equivalent to the request line REQ and response line ACK of FIG. 22” to control “leakage reduction circuits PSM2a and PSM2b.” MTK-1005, [0121]; MTK-1003, ¶¶414-415.

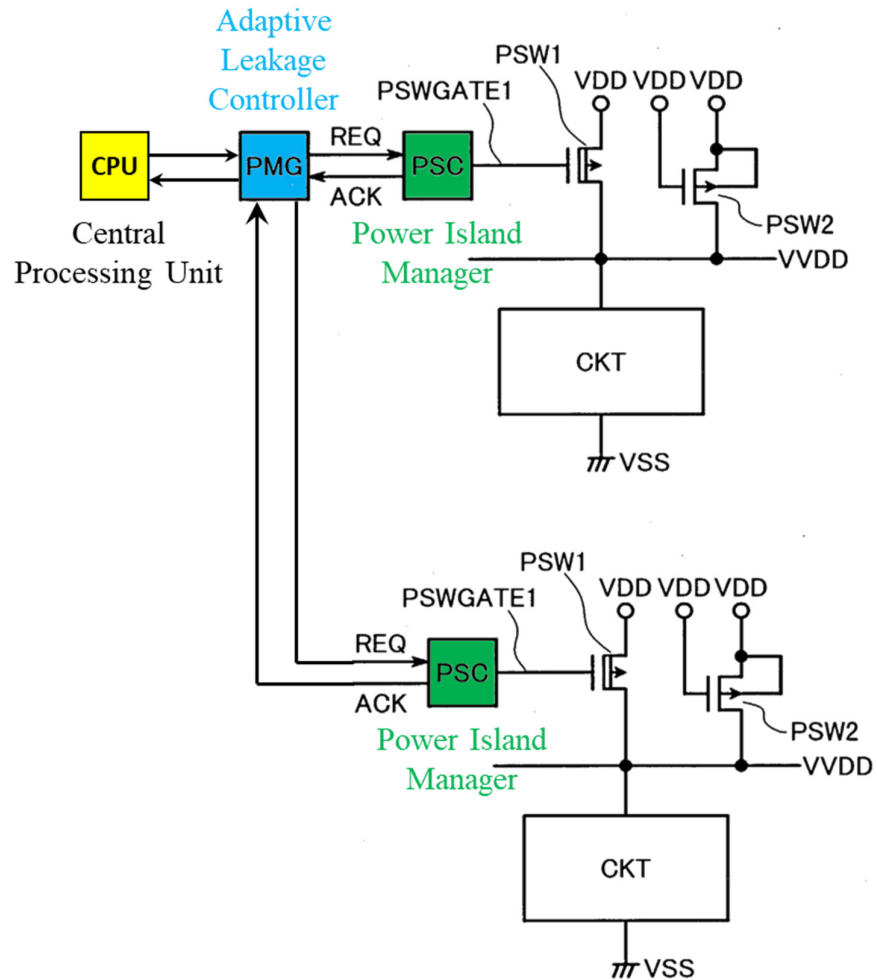


MTK-1003, FIG. 35 (as modified)

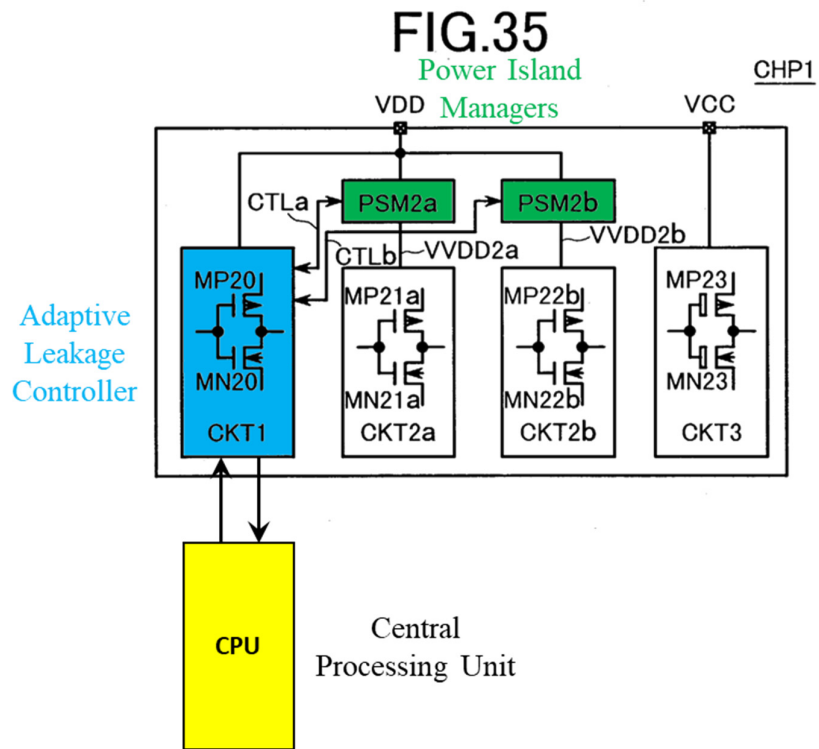
15. Claim 14

Mizuno renders obvious another power island manager separate from and in communication with the CPU. MTK-1003, ¶¶416. As discussed at Claim 13 above, a POSITA would have understood and found obvious that “power controlling circuit PMG” in Figures 1-30 and “circuit block CKT1” in Figures 35-40 receives external communications from a CPU, which it then uses to control the power island managers via the “REQ” and “ACK” control lines (“CTLa, CTLa” in Figures 35-40). MTK-1003, ¶417. Where there are multiple power islands as shown below, the CPU communicates with the separate power island managers for those power islands via the same “power controlling circuit PMG” or “circuit block CKT1.” MTK-1003, ¶¶417-419.

FIG.22



MTK-1005, FIG. 22 (as modified)



MTK-1005, FIG. 35 (as modified)

16. Claim 15

(a) Element 15[p]

Supra 1[p]. MTK-1003, ¶420.

(b) Element 15[a]

Supra 1[a] and 1[b]. MTK-1003, ¶421.

(c) Element 15[b]

Supra 1[c] and Claims 8-11. MTK-1003, ¶422.

(d) Element 15[c]

Supra 1[c], Claim 10 and Claim 12. MTK-1003, ¶423.

17. Claim 16

Supra Claim 4 and 1[p]-1[c]. MTK-1003, ¶424.

18. Claim 17

Supra Claim 5 and 1[p]-1[c]. MTK-1003, ¶425.

19. Claim 18

Supra Claim 6 and 1[p]-1[c]. MTK-1003, ¶426.

20. Claim 19

Supra Claim 7, 1[p]-1[c] and Claim 18. MTK-1003, ¶427.

**E. GROUND 2B—CLAIMS 9 AND 15 ARE OBVIOUS OVER
MIZUNO IN VIEW OF NOTANI**

1. Mizuno-Notani Combination

A POSITA would have been motivated to modify Mizuno’s integrated circuit to incorporate the teachings of Notani with a reasonable expectation of success. MTK-1003, ¶428. Both Mizuno and Notani are directed to reducing power consumption in integrated circuits, including power consumption due to leakage currents during standby. MTK-1005, Abstract, [0009], [0087]-[0088], [0093], [0130]; MTK-1025, Title, 1:6-9. The ’438 Patent relates to this same field of endeavor. *See* MTK-1001, Abstract, 1:25-35; 2:35-47; MTK-1003, ¶428.

Both are directed to retaining data in an integrated circuit during low-power standby states. MTK-1005, [0007], [0009], [0053], [0065]-[0066], [0087]-[0088] (“The present invention is characterized in that power consumption due to leakage current in the circuit block during the standby state can be greatly reduced while still maintaining (keeping) the information within the information retention circuits within the circuit block.”), [0099]; MTK-1025,

Abstract (“As a result, it is possible to reduce a leakage current withholding data in the internal circuit on the sleep state”), 2:31-34 (“It is an object of this invention to provide a semiconductor integrated circuit capable of reducing a leakage current with holding data in an internal circuit on a sleep state, even if a supply voltage to be used on the sleep state is lowered.”). The ’438 Patent is directed to these same fields of endeavor. *See* MTK-1001, Title (“Low Leakage and Data Retention Circuitry”), Abstract, 1:25-35; 2:21-47, 3:46-52; MTK-1003, ¶429.

Mizuno and Notani also address the same known power consumption problem in the same way. MTK-1003, ¶430. Both Mizuno and Notani reduce overall power consumption by placing circuit blocks into a low-power standby (i.e., sleep) mode when not in operation. *See, e.g.*, MTK-1005, [0054]-[0055], [0093], [0121]-[0122]; MTK-1025, Abstract, 1:6-9, 2:31-34, 2:64-3:10, 5:65-6:19, 8:5-24, 8:44-56; MTK-1003, ¶430. Mizuno uses a “PSC” which controls power within Mizuno’s “circuit block CKT” by modifying the voltage within the power island. *See* MTK-1005, [0054], [0093], FIGS. 1 and 22. Notani uses a “voltage generating circuit” that comprises a “charge pump” and outputs a “ground voltage on an active state” and a “voltage which is lower than the ground voltage, on the sleep state.” MTK-1025, Abstract, 3:11-20, 4:38-47, 5:7-10, FIGS. 1 and 5.

The similarities across Mizuno's and Notani's teachings would have led a POSITA to employ Notani's charge pump within Mizuno's "PSC" to improve Mizuno's ability to reduce power consumption, including that resulting from leakage currents. MTK-1003, ¶¶431-432.¹⁶ As discussed for Ground 2A, a POSITA would have understood that *how* Mizuno's "PSC" generates a regulated voltage is merely a design choice with a finite number of well-known solutions. *Id.* One such method for generating a regulated voltage is using a charge pump. MTK-1003, ¶¶431-432, 64-73. A POSITA would have understood that by utilizing Notani's charge pump circuit, "a known circuit," MTK-1025, 7:12-13, "it is possible to reduce the leakage current," *id.*, 9:28-37. MTK-1003, MTK-1003, ¶¶431-432.

Because Mizuno and Notani provide a similar solution to a similar problem within the same field of endeavor, a POSITA would have naturally looked at, and been motivated to combine, the references to reduce the leakage current, and thus power consumption, in Mizuno's system. Specifically, a POSITA would have been motivated to employ Notani's "charge pump" with Mizuno's "PSC" to

¹⁶ As explained at Ground 2A, Mizuno by itself discloses and renders obvious a sleep generator comprising a charge pump. MTK-1003, ¶431n.13. If Mizuno fails to independently render obvious this feature, Mizuno in combination with Notani renders that limitation obvious.

power-down circuits within Mizuno's integrated circuit when not in use. MTK-1003, ¶¶431-432.

A POSITA would have understood that employing Notani's charge pump in Mizuno's "PSC" to control the power to individual circuits would have been readily implemented by a POSITA with predictable results. MTK-1003, ¶¶432-433. The use of charge pumps was a well-known solution for efficiently controlling an integrated circuit, and a POSITA would have needed only routine electrical and computer engineering principles to implement a charge pump with Mizuno's "PSC." MTK-1003, ¶¶432-433. Such a combination would predictably reduce the overall power consumption of the device by reducing the power consumption of inactive circuits even while the device remains operational. MTK-1003, ¶¶432-433.

2. Claim 9

The Mizuno-Notani combination renders obvious Claim 9. *Surpa* Ground 1C, Claim 8. MTK-1003, MTK-1003, ¶434.

From Notani's teachings, a POSITA would have found it obvious for Mizuno's "power switch controller PSC" to generate an optimum voltage in response to a control signal, i.e., "REQ," using a charge pump, which was a "known circuit," MTK-1024, 7:12-13, in existence at the time of the alleged invention. MTK-1003, ¶¶435-436. A POSITA would have had a reasonable expectation of success in combining Notani and Mizuno, because the

combination would represent a simple integration of Notani’s “charge pump” into Mizuno’s “PSC” for generating optimum source voltages for the integrated circuit. MTK-1003, ¶¶435-436. Employing Notani’s “charge pump” would have required merely routine electrical or computer engineering knowledge and was a task well within the skill of a POSITA. *Id.* Incorporating Notani’s charge pump would provide additional improvements in performance and power consumption for the circuit. *Id.*

3. Claim 15

Supra Claim 9; Ground 2A, Claims 1, 6, 8. MTK-1003, ¶¶437-440.

IV. THE BOARD SHOULD CONSIDER THE PETITION ON THE MERITS

A. Discretionary Denial under Section 325(d) Is Unwarranted

Advanced Bionics and the *Becton* factors strongly favor institution.

Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential); *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential as to §III.C.5, first paragraph).

Advanced Bionics Part 1—The examiner never issued a rejection over prior art during prosecution. *See generally* MTK-1002. The references relied upon here were not cited by the examiner and are not listed on the face of the ’438 Patent. *See generally* MTK-1001, MTK-1002. Thus, there is no indication that the examiner substantively considered any references, and therefore, the

Petition's art and arguments cannot be said to be the same as, or substantially similar to, those previously presented for the '438 Patent. *Id.* Accordingly, neither condition of the first prong of the *Advanced Bionics* framework is met.

Becton factors [a], [b], and [d] counsel in favor of institution. None of Takahashi, Mizuno, Ko, Schutz, or Notani were addressed during prosecution ([a]), nor are they cumulative of other art relied on or considered by the examiner ([b]). *Id.* There are also no overlapping arguments ([d]) between the prosecution record and the Grounds above. Thus, *Becton* factors [a], [b], and [d] favor Petitioner.

Advanced Bionics Part 2—The Board need not reach the second prong to resolve against discretionary denial under §325(d), since the first prong is not satisfied. *See Oticon Med. AB et. al. v. Cochlear Ltd.*, IPR2019-00975, Paper 15 at 20 (PTAB Oct. 16, 2019) (precedential) (no denial because “new, noncumulative prior art asserted in the Petition”). Nonetheless, each of *Becton* factors [c], [e], and [f] favors Petitioner. None of Takahashi, Mizuno, Ko, Schutz, or Notani was cited during prosecution, and thus did not form the basis of any rejection ([c]). As for factors [e] and [f], by not considering Takahashi, Mizuno, Ko, Schutz, Notani, or combinations thereof, the Office erred in its evaluation of the prior art, warranting reconsideration. *Advanced Bionics*, Paper 6, 10. The Grounds above demonstrate why consideration is warranted.

B. Discretionary Denial under Section 314(a) Is Not Warranted

In *General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357—01361, Paper 19 at 9-10 (PTAB Sept. 6, 2017) (precedential), the Board identified seven factors for discretionary denials under §314(a). Given this is the first ever petition to be filed against the '438 Patent, the *General Plastics* factors do not apply. See *Acronis, Inc. v. Realtime Data LLC*, IPR2018-00706, Paper 11, 15-16 (Oct. 1, 2018).

C. The *Fintiv* Factors Weigh Against Denial

In *Apple Inc. v. Fintiv, Inc.*, the Board enumerated six factors to determine whether a petition should be discretionarily denied under §314(a). IPR2020-00019, Paper 11 at 2-3 (Mar. 20, 2020) (precedential) (“*Fintiv*”). In June 2022, the USPTO issued updated discretionary guidance in view of the *Fintiv* factors and expressly noted that ***the PTAB will not discretionarily deny institution if Petitioner presents a Sotera stipulation.*** MTK-1022. Petitioner eliminated any risk of duplicated effort by presenting a *Sotera* stipulation. MTK-1023; *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (Dec. 1, 2020). For at least this reason, the Board should not discretionarily deny this Petition.

V. CONCLUSION

As demonstrated herein, the Challenged Claims are unpatentable. Accordingly, Petitioner respectfully requests that the Board institute IPR.

VI. PAYMENT OF FEES

Petitioner authorizes charge of fees to Deposit Account 06-1050.

VII. MANDATORY NOTICES UNDER 37 C.F.R. §42.8(A)(1)

A. Real Party-in-Interest under 37 C.F.R. §42.8(b)(1)

MediaTek Inc. is the Petitioner and real party-in-interest. MediaTek USA Inc. is an additional real party-in-interest. No other parties had access to or control over the present Petition, and no other parties funded the present Petition.

B. Related Matters under 37 C.F.R. §42.8(b)(2)

MOSAID—the alleged Patent Owner—filed a complaint asserting the '438 Patent against Petitioner on March 28, 2023, in the U.S. District Court for the Eastern District of Texas (Case No. 2:23-CV-00129).

C. Lead and Back-Up Counsel under 37 C.F.R. §42.7(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR44508-0023IP6@fr.com.

Respectfully submitted,

Dated: March 22, 2024

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CERTIFICATION UNDER 37 C.F.R. § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,885 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: March 22, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) et seq. and 42.105(b), the undersigned certifies that on March 22, 2024, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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