

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MEDIATEK, INC.,
Petitioner,

v.

MOSAID TECHNOLOGIES INC,
Patent Owner.

Case IPR2024-00720
Patent 8,253,438

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

	Page
I. INTRODUCTION.....	1
II. PETITIONER’S GROUNDS FAIL.....	2
A. “Power Islands” In The ’438 Patent.....	2
B. Petitioner Fails To Demonstrate That Any Grounds Render Obvious Power Consumptions That Are Dynamically Changeable “Based On Needs And Operation Of The Integrated Circuit” (All Claims, All Grounds).	5
1. The Petition Should Be Denied For Failing To Address The Construction Of “Based On Needs And Operation Of The Integrated Circuit.”.....	6
2. The Board Should Apply The Agreed-Upon Construction Of “Based On Needs And Operation Of The Integrated Circuit.”	7
3. Petitioner Does Not Show That Any Ground Teaches The Agreed-Upon Construction.	9
4. Even If The Board Does Not Construe The Term, Petitioner Fails To Show How The Prior Art Teaches Power Consumptions Changeable “Based On Needs And Operation Of The Integrated Circuit.”	10
C. Petitioner Fails To Demonstrate That Any Grounds Disclose Or Render Obvious “A Plurality Of Power Islands” (All Claims, All Grounds).....	14
1. The Petition Should Be Denied For Failing To Address The Construction of “Power Island.”	17
2. Petitioner’s Takahashi Grounds Fail (All Claims, Grounds 1A, 1B, 1C).	18

a.	Petitioner Fails To Show That Takahashi Discloses Or Renders Obvious “A Plurality Of Power Islands” (All Claims, Grounds 1A, 1B, 1C).	18
i.	Petitioner Admits That Takahashi’s Figure 1 Does Not Disclose “A Plurality Of Power Islands.”	27
ii.	Petitioner Does Not Show That Takahashi’s Figure 16 Discloses “A Plurality Of Power Islands.”	28
iii.	Petitioner Does Not Show That Takahashi’s Figure 10 Discloses Or Teaches “A Plurality Of Power Islands.”	38
b.	Petitioner’s Arguments That Takahashi Renders Obvious “A Plurality Of Power Islands” Are Conclusory.....	48
i.	Petitioner Does Not Distinguish Alleged Teachings Of Takahashi From Express Disclosures In Takahashi.	49
ii.	Petitioner Offers Only Conclusory Statements, Not Evidence, About The Motivation To Combine Takahashi’s Distinct Disclosures In The Way Proposed By Petitioner.....	52
3.	Petitioner’s Mizuno Grounds Fail (All Claims, Grounds 2A, 2B).....	57
a.	Petitioner Fails To Show That Mizuno Discloses “A Plurality Of Power Islands” (All Claims, Grounds 2A, 2B).	58
i.	Petitioner Does Not Show That Mizuno Discloses “A Plurality Of Power Islands” In Its “Figures 1-30.”	59
ii.	Petitioner Does Not Show That Mizuno Discloses “A Plurality Of Power Islands” In Its “Figures 35-40.”	60

b.	Petitioner’s Arguments That Mizuno Renders Obvious “A Plurality Of Power Islands” Are Conclusory (All Claims, Grounds 2A, 2B).	62
4.	Petitioner’s Multiple-Reference Grounds Incorporate The Flaws Of Petitioner’s Single-Reference Grounds (Grounds 1B, 1C, 2B, Claims 7, 9, 15, 19).....	65
III.	CONCLUSION	68

TABLE OF AUTHORITIES

	Page(s)
COURT DECISIONS	
<i>ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.</i> , 694 F.3d 1312 (Fed. Cir. 2012)	53
<i>Arendi S.A.R.L. v. Apple, Inc.</i> , 832 F.3d 1355 (Fed. Cir. 2016)	64
<i>Bd. of Regents of the Univ. of Tex. Sys. v. BENQ Am. Corp.</i> , 533 F.3d 1362 (Fed. Cir. 2008)	12
<i>Becton Dickinson & Co. v. Tyco Healthcare Grp., LP</i> , 616 F.3d 1249 (Fed. Cir. 2010)	12
<i>Belden Inc. v. Berk-Tek LLC</i> , 805 F.3d 1064 (Fed. Cir. 2015)	57
<i>DSS Tech. Mgmt. v. Apple Inc.</i> , 885 F.3d 1367 (Fed. Cir. 2018)	64
<i>Graham v. John Deere Co.</i> , 383 U.S. 1 (1966).....	49
<i>In re Kotzab</i> , 217 F.3d 1365 (Fed. Cir. 2000)	52
<i>In re Magnum Oil Tools Int'l, Ltd.</i> , 829 F.3d 1364 (Fed. Cir. 2016)	17
<i>Intelligent Bio-Systems, Inc. v. Illumina Cambridge, Ltd.</i> , 821 F.3d 1359 (Fed. Cir. 2016)	9
<i>KSR Int'l Co. v. Teleflex Inc.</i> , 550 U.S. 398 (2007).....	49

<i>PAR Pharm., Inc. v. TWi Pharms., Inc.</i> , 773 F.3d 1186 (Fed. Cir. 2014)	62
<i>Polaris Indus., Inc. v. Arctic Cat, Inc.</i> , 882 F.3d 1056 (Fed. Cir. 2018)	53
<i>Southwire Co. v. Cerro Wire LLC</i> , 870 F.3d 1306 (Fed. Cir. 2017)	62
<i>Texas Instruments, Inc. v. ITC</i> , 988 F.2d 1165 (Fed. Cir. 1993)	13
<i>Trintec Indus., Inc. v. Top-U.S.A. Corp.</i> , 295 F.3d 1292 (Fed. Cir. 2002)	61

AGENCY DECISIONS

<i>10x Genomics, Inc. v. President and Fellows of Harvard College</i> , IPR2023-01299, Paper 15 (Mar. 7, 2024)	7
<i>Apple Inc. v. One-E-Way, Inc.</i> , IPR2021-00284, Paper 7 (Jun. 11, 2021)	10
<i>Matterport, Inc. v. Appliance Computing III, Inc.</i> , IPR2021-00939, Paper 15 (Nov. 23, 2021)	52
<i>Orthopediatrics Corp. v. K2M, Inc.</i> , IPR2018-01546, Paper 10 (Feb. 14, 2019)	6
<i>PayPal, Inc. v. IOENGINE, LLC</i> , IPR2019-00906, Paper 16 (Oct. 29, 2019)	54
<i>Samsung Austin Semiconductor, LLC v. Red Rock Analytics, LLC</i> , IPR2018-00556, Paper 18 (Aug. 20, 2018)	54
<i>TCT Mobile (US) Inc., v. Semiconductor Energy Lab. Co., Ltd.</i> , IPR2022-00440, Paper 13 (Aug. 3, 2022)	10
<i>Valeo N. Am., Inc. v. Magna Elecs., Inc.</i> , IPR2014-01206, Paper 13 (Dec. 23, 2014)	52

Xerox Corp. v. Bytemark, Inc.,
IPR2022-00624, Paper 9 (Aug. 24, 2022)
(precedential) 17

STATUTES

35 U.S.C. § 103 [pre-AIA].....49

REGULATIONS

37 C. .R. § 42.6(a)(3) 23, 25
37 C.F.R. § 42.104(b)(3).....6, 7
37 C.F.R. § 42.104(b)(4).....6, 7
37 C.F.R. § 42.65(a).....17
37 C.F.R. § 42.100(b) 8

RULES, RULEMAKING, AND OTHER AGENCY AUTHORITIES

83 Fed. Reg. 51,340 (Oct. 11, 2018).....8
Consolidated Trial Practice Guide
Patent Trial And Appeal Board 8

EXHIBIT LIST	
2001-2003	Reserved
2004	<i>MOSAID Techs. Inc. v. MediaTek, Inc.</i> , 2:23-cv-00129, Joint Claim Construction And Prehearing Statement (May 9, 2024) [JCCS]
2005	U.S. Patent No. 7,051,306 ['306]
2006	U.S. Patent No. 8,854,077 ['077]

I. INTRODUCTION

The Petition should be denied because Petitioner fails to demonstrate that it would prevail as to at least one challenged claim. Petitioner does not address two key issues at the core of its challenge. First, all challenged claims recite integrated circuits with components whose power consumptions are changeable “based on needs and operation of the integrated circuit” of which they are a part. Petitioner never meaningfully addresses this limitation, and thus does not show that it is taught in the cited art. Petitioner does not even mention the construction of this limitation, adopted by two courts and agreed to in parallel litigation by both parties to this IPR, much less attempt to demonstrate that the construction is satisfied.

Second, all challenged claims recite integrated circuits comprising a “plurality of power islands,” *i.e.*, more than one power island. Petitioner fails to explain how a “plurality of power islands” is taught in the cited art. Petitioner alludes to obviousness, but fails to offer anything more than conclusory statements in this vein.

Further undermining Petitioner’s position is its unexplained inconsistency concerning the meaning of the term “power island.” While taking the position that “power island” requires no construction in this proceeding, Petitioner recognizes that interpretation of “power island” might affect the analysis by constantly pairing what are essentially anticipation arguments with perfunctory statements of obviousness. Because Petitioner does not identify any construction of “power island” that it is

applying to the cited art, the distinctions (if any) between these arguments are unclear. Meanwhile, in co-pending district court litigation, Petitioner is proposing a construction that its primary references, Takahashi and Mizuno, do not satisfy. Petitioner does not analyze Takahashi or Mizuno under its construction here, asserting only that these references’ “disclosures, in light of a POSITA’s knowledge, also render these terms obvious” under the construction. *See Pet.*, 16-17, 61.

To be clear, none of this is about disputed facts or about the interpretation of evidence cited by the Petitioner. The Petition does not address “based on needs and operation of the integrated circuit,” and makes statements about “power islands” that are not supported by more than attorney fiat. The Petition should be denied.

II. PETITIONER’S GROUNDS FAIL.

A. “Power Islands” In The ’438 Patent.

The ’438 patent’s specification describes systems for reducing power consumption in integrated circuits (“ICs”) while maintaining performance. Crucial to the systems the ’438 patent is the idea of “power islands”—delineations of an IC into subdivisions “where power consumption is controlled within” the subdivision. Ex. 1001 [’438] 3:62-65.

The ’438 patent describes exemplary designs where such islands include “logic,” “memory,” and “third party IP.” Ex. 1001 [’438] 4:1-4. In some examples, power management involves “control signals” provided by an “adaptive leakage

controller.” See, e.g., Ex. 1001 [’438] Fig. 2 (see “Adaptive Leakage Controller 270”), 4:1-24. Each claim correspondingly recites a system comprising a “plurality of power islands” that involves, *inter alia*, an “adaptive leakage controller” and a “control signal.” *Id.*, cls. 1-19. In exemplary Figure 2, such islands are separately controlled by “power island managers”:

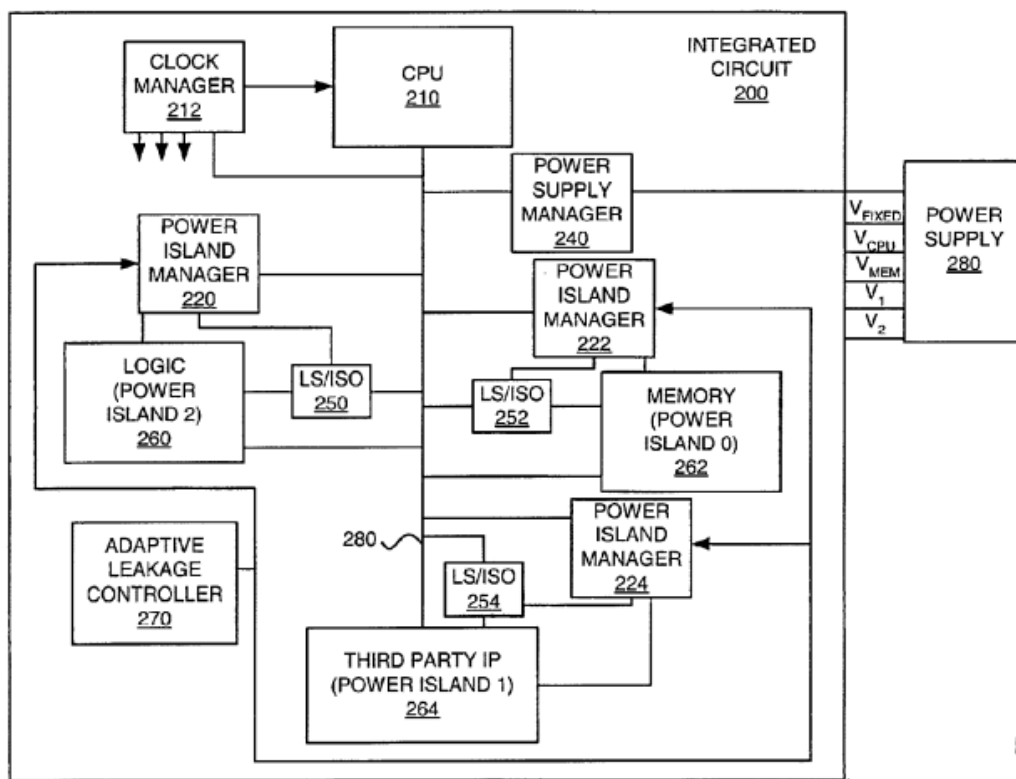


FIG. 2

Id., Fig. 2. Here, “power island managers” 220, 222, and 224 separately manage power consumption within the power islands 260, 262, and 264. *Id.*, 4:1-17. Many claims in the ’438 patent claims correspondingly recite a “power island manager.” *Id.*, cls. 1-14.

The crucial point is that “power islands” are not merely delineations of

integrated circuits, but delineations with separately controllable power. If one considers only whether there are functionally divided blocks of circuits, one may very well have “islands.” But what makes a “**power** island” is the adjective “power”—a power island must be configured as to have power control independent of other components, as discussed in detail below. When evaluating any disclosure, the adjective “power” in “power island” means that merely having a functional block of circuitry is not enough: one must ask whether and how the block has independent power control.

This is where the Petition falls apart. Petitioner can credibly argue that Takahashi or Mizuno disclose distinguishable functional blocks of circuitry; Petitioner does not show that these blocks have separately controlled power. Petitioner invites the Board to ignore the crucial point: a “power island” is a **power** island, not merely a functional island. Petitioner focuses instead upon hypothetical claims where “power” is removed from every recitation of “power island.” This is erroneous.

Similarly, although all claims recite changing power consumption in power islands “based on needs and operation of the integrated circuit,” Petitioner simply ignores this language.

The references leave Petitioner no choice, of course, as neither Takahashi nor Mizuno teach pluralities of “power islands,” let alone power islands with power

consumptions changeable “based on needs and operation of the integrated circuit.”

But Petitioner’s plight is no substitute for a proper validity analysis.

In refusing to analyze purported “power islands” and “based on needs and operation of the integrated circuit” under any claim construction, *see* Section II.C, Section II.B, and in refusing to acknowledge where or how the references might not disclose “a plurality of power islands,” Sections II.C.2.b and II.C.3.b, Petitioner’s analysis presents something of a moving target. Details of how Petitioner’s analysis fails to show that Takahashi or Mizuno fail to render the challenged claims obvious (alone or in combination) are nevertheless addressed below.

B. Petitioner Fails To Demonstrate That Any Grounds Render Obvious Power Consumptions That Are Dynamically Changeable “Based On Needs And Operation Of The Integrated Circuit” (All Claims, All Grounds).

Each challenged claim requires power islands whose power consumptions are changeable “based on needs and operation of the integrated circuit.” While the ’438 patent has not yet been subject to claim construction, several of the same terms in the claims of the ’438 patent were subject to claim construction for the ’306 patent, which is incorporated by reference in the ’438. One of these terms, “[b]ased on needs and operation of the integrated circuit” has been construed by two prior district courts as “based on *future operational needs* and *current operating status* of the integrated circuit.” Ex. 1032 [Freescale-Order] 48; Ex. 1033 [Xilinx-Order] 9. Both

Petitioner and Patent Owner agree that it should be construed this way in the co-pending litigation. Ex. 2004 [JCCS] 2. The Board should apply this agreed-upon construction here. See Section II.B.2.

Fatally, although Petitioner cites the orders that provide this construction (in connection with the term “power island,” see, e.g., Pet., 16, 61), and although Petitioner proposes this construction in the co-pending litigation, the Petition does not address this construction (Section II.B.1)—or otherwise show how it is disclosed in or obvious over the cited art (Section II.B.3). Even if the Board were to disregard this construction, Petitioner still fails to show that the limitation is met. See Section II.B.4.

1. The Petition Should Be Denied For Failing To Address The Construction Of “Based On Needs And Operation Of The Integrated Circuit.”

Petitioner had the burden to construe the claims and demonstrate that the construed claims are satisfied. See 37 C.F.R. §§ 42.104(b)(3)-(4). Its failure to carry that burden is sufficient reason to deny institution. In *Orthopediatrics Corp. v. K2M, Inc.*, IPR2018-01546, Paper 10 (Feb. 14, 2019), for instance, the Board denied institution where the petitioner argued contradictory claim constructions between an IPR and the district court, and the district court had accepted petitioner’s construction. *Id.*, 11-12 (“it is incumbent upon Petitioner to address substantively the District Court’s claim construction of a limitation when construction of that

limitation is likely to be a focal point of the *inter partes* review proceeding.”); *see also 10x Genomics, Inc. v. President and Fellows of Harvard College*, IPR2023-01299, Paper 15, 13 (Mar. 7, 2024) (“our rules require that Petitioner substantively address any claim terms in dispute. ... Thus, we find the Petition is deficient on its face under 37 C.F.R. § 42.104(b)(3), as merely stating ‘no construction [is] necessary’—while knowing the construction is actually disputed under § 112(f)—is not sufficient for purposes of institution.”).

Where “based on needs and operation of the integrated circuit” has been construed by two different district courts, and the parties agree that this construction should be applied in co-pending litigation, it was incumbent upon Petitioner to say more than that “[f]or purposes of this proceeding only, Petitioner submits that no claim terms require a formal construction to address the Grounds in this Petition.” Pet., 6. Under these circumstances, Petitioner has failed to comply with 37 C.F.R. §§ 42.104(b)(3)-(4) and that failure should prove sufficient to deny institution.

2. The Board Should Apply The Agreed-Upon Construction Of “Based On Needs And Operation Of The Integrated Circuit.”

Again, two different district courts have construed “based on needs and operation of the integrated circuit” to mean “based on future operational needs and current operating status of the integrated circuit.” Ex. 1032 [Freescale-Construction] 48; Ex. 1033 [Xilinx-Construction] 9. These prior cases involved the ’306 patent,

which is incorporated by reference in the '438 patent. Ex. 1032 [Freescale-Construction] 1 (construing U.S. 7,051,306); Ex. 2005 ['306] (issued from Application 10/840,893); Ex. 1001 ['438] 4:3-7 (incorporating Application 10/840,893). In the co-pending litigation, Petitioner and Patent Owner agree that the same construction should apply to the '438 patent. Ex. 2004 [JCCS] 2. The Board should apply this construction here.

For starters, a construction agreed to by two district courts and both parties appearing before the Board should presumptively apply in this proceeding, which utilizes the same claim construction standard. 37 C.F.R. § 42.100(b).

The Board's rules also provide that "[a]ny prior claim construction determination concerning a term of the claim in a civil action . . . that is timely made of record in the *inter partes* review proceeding will be considered." 37 C.F.R. § 42.100(b). The Board must also give "appropriate weight" to district court claim constructions. CTPG (Nov. 2019 Update), 46-47; Changes to the Claim Construction Standard, 83 Fed. Reg. 51,340, 51,354 (Oct. 11, 2018).

The Board's use of the agreed-upon construction is particularly appropriate in view of the Office's motivation for aligning its claim construction standard with that used by district courts: to "avoid[] . . . potential . . . inconsistencies between PTAB and federal court proceedings" and promote greater certainty over claim scope. *See, e.g.*, 83 Fed. Reg. at 51,343. Adopting a construction used by two prior district

courts and agreed to by both parties to this IPR in co-pending litigation harmonizes the Board's practice with that of the district courts, as intended.

Petitioner provides no account of why the Board should not construe the term, or apply a different construction. Petitioner merely "submits that no claim terms require a formal construction to address the Grounds in this Petition." Pet., 5-6. This vague reference to "claim terms" does not even acknowledge that "based on needs and operation of the integrated circuit" has been previously construed and proposed for construction in co-pending litigation. As we now explain, Petitioner does not show that this limitation is taught in the cited art.

3. Petitioner Does Not Show That Any Ground Teaches The Agreed-Upon Construction.

Petitioner does not even purport to analyze its grounds based on any claim construction, let alone the agreed construction of "based on needs and operation of the integrated circuit." Neither Petitioner's brief nor its expert declaration even mention it—anywhere. *See generally* Pet.; Ex. 1003 [Min-Decl.].

This abject failure of proof requires denial of institution. *See, e.g., Intelligent Bio-Systems, Inc. v. Illumina Cambridge, Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) ("the expedited nature of IPRs bring with it an obligation for petitioners to make their case in their petition to institute"). The Board routinely denies institution where an agreed-upon construction is not met. *See, e.g., Apple Inc. v. One-E-Way, Inc.*,

IPR2021-00284, Paper 7, 14 (Jun. 11, 2021) (“On this record, Petitioner does not show sufficiently that Ham teaches [limitation] under the claim construction agreed to by the parties and adopted for purposes of this Decision.”); *TCT Mobile (US) Inc., v. Semiconductor Energy Lab. Co., Ltd.*, IPR2022-00440, Paper 13, 14-15 (Aug. 3, 2022) (denying institution when agreed-upon construction was not met). Institution should similarly be denied here.

4. Even If The Board Does Not Construe The Term, Petitioner Fails To Show How The Prior Art Teaches Power Consumptions Changeable “Based On Needs And Operation Of The Integrated Circuit.”

Although the Board should adopt the prior, agreed construction, even if it were ignored, Petitioner still fails to demonstrate a reasonable likelihood of prevailing. Petitioner addresses “based on needs and operation of the integrated circuit” twice: in one paragraph arguing that Takahashi teaches a power island manager configured to dynamically change power consumptions “based on needs and operation of the integrated circuit” in claim 1, and in one paragraph arguing that Mizuno teaches the same limitation.

Regarding Takahashi, Petitioner states in full:

Takahashi’s “voltage regulator” is configured to dynamically change the power consumptions of the power islands based on the needs and operation of the integrated circuit. When “device 200” is in “Active mode,” the “voltage regulator” provides an “operating voltage” to the

power islands' circuitries, including "logic circuit 10" and "control circuit 70," via their sleep transistors (e.g., "switching circuit 20"). During "Sleep mode," the "voltage regulator" lowers the voltage signals to place the power islands' circuitries, including "logic circuit 10" and "control circuit 70," into a low-power standby status (i.e., dynamically changes their power consumption). Thus, as in the '438 patent, Takahashi's "voltage regulator" "control[s] power within [each] power island" by "modify[ing] the voltage within the power island" based on whether the power island needs to be operational ("Active Mode") or can be placed into standby ("Sleep Mode").

Pet., 18-19 (citations omitted). Regarding Mizuno, Petitioner states, again in full:

Thus, Mizuno's "PSC" is configured to dynamically change the power consumptions of the power islands based on the needs and operation of the integrated circuit. Depending on whether the integrated circuit requires "CKT1" to be operational, the "PSC" "controls the on and off operation of the power switch PSW1 connected between the power supply VDD and the virtual power line VVDD" that powers "circuit block CKT." As shown in Figure 2 of Mizuno, based on the "PSC" turning the "power switch PSW1" on or off based on the output "PSWGATE1," "virtual power line VVDD" powering "CKT1" changes so that "circuit block CKT is operable (in operating state)' or in standby. Thus, as in the '438 patent, Mizuno's "power switch controller PSC" "control[s] power within [each] power island" by "modify[ing] the voltage within the power island" based on whether the power island needs to be operational or can be placed into standby.

Pet., 64-65 (citations omitted).

Such “analysis” does little more than pair assertions about the references with claim language, or phrases introduced by Petitioner that sound similar to claim language. Both analyses conclude, for example, with a statement that power is controlled “based on whether the power island needs to be operational” or can be “placed into standby.” Pet. 19, 65. As Petitioner sees it, whenever a circuit has two states that differ in power consumption, any change from one to the other constitutes dynamically changing power consumption “based on needs and operation of the integrated circuit.” This argument should be rejected.

First, Petitioner’s interpretation ignores the express language of the claim, which recites changing power consumption not based on whether a power island “needs to be operational” (as Petitioner has phrased it), but separately recites changing power consumption based on **both** the “needs” **and** “operation” of the integrated circuit of which the power island is a part. Petitioner’s analysis does not distinguish between these distinct elements. Different terms presumptively have different meanings, *see Bd. of Regents of the Univ. of Tex. Sys. v. BENQ Am. Corp.*, 533 F.3d 1362, 1371 (Fed. Cir. 2008), yet Petitioner does not explain why it would be appropriate in this case not to “giv[e] effect to all terms in the claim.” *See, e.g., Becton Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1257 (Fed. Cir. 2010). Indeed, Petitioner’s analysis effectively reads “based on needs and

operation of the integrated circuit” entirely out of the claim—again, without any argument why this is appropriate. *See Texas Instruments, Inc. v. ITC*, 988 F.2d 1165, 1171 (Fed. Cir. 1993) (finding that an express limitation cannot be read out of a claim).

Second, Petitioner does not identify any **basis** on which power consumption is changed in the cited art. Petitioner does not, for example, identify circumstances under which Takahashi changes the device identified by Petitioner from “operational” to “standby”; Petitioner merely quotes from Takahashi’s description of power consumption in both states. So too with Mizuno, where Petitioner only vaguely asserts that a change of state may occur “[d]epending on whether the integrated circuit requires ‘CKT1’ to be operational.” Pet. 64. By not identifying any basis on which “the integrated circuit” of Mizuno “requires” a component to be operational, Petitioner offers no evidence that Mizuno shows the limitation. In effect, Petitioner offers circular reasoning: a change is “based on needs and operation of [an] integrated circuit” whenever it is implemented by an integrated circuit. Petitioner’s cursory analysis of this limitation should be compared with the pages used by Petitioner in attempting to address it in a co-pending IPR. *See, e.g.*, IPR2024-00598, Paper 2, 10-15 (arguing that a primary reference disclosed determining a power level “based on needs and operation of the integrated circuit”), 41-42 (arguing that a secondary reference disclosed this limitation), 54-59 (arguing

that another primary reference disclosed this limitation).

Petitioner does not show that the cited art teaches dynamically changing power consumption in power islands “based on needs and operation of the integrated circuit,” and all of Petitioner’s grounds therefore fail.

C. Petitioner Fails To Demonstrate That Any Grounds Disclose Or Render Obvious “A Plurality Of Power Islands” (All Claims, All Grounds).

Each of the claims recites a system comprising “a plurality of power islands.” The term “power island” requires construction and has also already been construed by two different district courts:

<i>Freescale</i> District Court Construction	<i>Xilinx</i> District Court Construction
a section of an integrated circuit where power consumption is controlled by independently varying its operating voltage and its frequency of operation	a section of an integrated circuit where power consumption is controlled by independently varying its operating voltage or its frequency of operation (or both)
Ex. 1032, 44; Ex. 2004 [JCCS] 3	Ex. 1033, 29; Ex. 2004 [JCCS] 3

In the co-pending litigation, the parties agree that “power island” requires construction, and that the proper construction is one of the above: Patent Owner proposes the *Freescale* construction, and Petitioner proposes the *Xilinx* construction. Ex. 2004 [JCCS] 3. The constructions have one difference. The *Freescale* construction requires control by “independently varying” both the “operating

voltage **and** ... frequency of operation,” while the *Xilinx* construction requires power consumption controlled by “independently varying” either the “operating voltage **or** ... frequency of operation (or both).”

As context for these proposals, the '438 specification states that “[a] power island is any section, delineation, partition, or division of an integrated circuit where power consumption is controlled within the section, delineation, partition, or division,” Ex. 1001 ['438] 3:62-65, and includes examples of how power consumption is “controlled within” a power island. *See, e.g., id.*, 4:8-17 (power controlled “within [a] power island” by “select[ing] a clock, chang[ing] clock frequency, or modify[ing] the voltage within the power island to control the power consumption of the power island.”). The parties’ dispute could be regarded as centering on which district court construction, in the context of the entire intrinsic record, more appropriately reflects how power consumption is “controlled within” a section of an integrated circuit.

While the parties disagree about **which** construction to use, they agree that a “power island” is a section of an integrated circuit where power consumption is controlled by “independently varying” one or more power characteristics, including at least one of an “operating voltage” or a “frequency of operation.” In short, the parties agree that “power island” is indeed a “**power**” island—a section with independently controllable power. Here, however, Petitioner contends that “no

claim terms require a formal construction.” Pet., 6. Petitioner fails to explain the inconsistent position it takes here that no construction is necessary.

Petitioner tries to downplay the *Xilinx* and *Freescale* constructions, stating that “power island” has been “construed in prior litigations involving **a patent describing similar subject matter.**” Pet., 16. Petitioner neglects to mention that this patent was incorporated by reference into the ’438 patent when introducing “power islands,” Ex. 1001 [’438] 4:3-7, and mirrors various descriptions of “power islands” in the ’306 patent. *Compare* Ex. 1001 [’438] 3:62-4:1 *with* Ex. 2005 [’306] 3:51-59.¹ Given this relationship, it is no surprise that in the co-pending litigation, the parties agree that “power island” means the same thing in both the ’438 patent and the ’306 patent. Ex. 2004 [Joint-Claim-Construction-Statement] 3.

Again, Petitioner has little choice, because Petitioner cannot—and does not attempt to—argue that the cited art teaches “a plurality of power islands” by comparing the art to either party’s (*i.e.*, either district court’s) construction. Petitioner instead pays only the most conclusory possible lip service. Petitioner

¹ Petitioner is familiar with the ’306 patent. Like the ’438 patent, it is presently at issue in the parallel litigation, *see, e.g.*, Ex. 2004 [Joint-Claim-Construction--Statement] 1, and the subject of co-pending IPR proceedings. *See* IPR2024-00598.

states, for example, that “Takahashi’s disclosures, in light of a POSITA’s knowledge, also render these terms obvious under the prior constructions.” Pet., 16-17. Petitioner’s expert does not elaborate upon “Takahashi’s disclosures,” “the prior constructions,” or any alleged significance of one to the other, but simply repeats this assertion. Ex. 1003 [Min-Decl.] ¶ 114, n.1. Petitioner’s “analysis” of Mizuno simply replaces “Takahashi” in this assertion with “Mizuno.” Pet., 61.

Such conclusory statements are entitled to little weight. *See, e.g.*, 37 C.F.R. § 42.65(a); *see also Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9, 15-17 (Aug. 24, 2022) (precedential) (denying institution when expert declaration “adds little to the conclusory assertion for which it is offered to support”). “To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016). Nor would any of the alleged “pluralit[ies] of power islands” identified by Petitioner qualify under either construction. See Sections II.C.2, II.C.3.

1. The Petition Should Be Denied For Failing To Address The Construction of “Power Island.”

“Power island” is a term that both parties agree requires construction and, indeed, has been previously construed by two different district courts in mostly

similar terms. Both parties advance one of these constructions in district court and, aside from the distinction identified above, agree on the balance of the construction. But Petitioner does not make any real attempt to argue that either construction is satisfied—nor does Petitioner make any real attempt to argue why “power island,” only in this IPR, does not require construction. Petitioner had the burden to construe the claims and demonstrate that the construed claims are satisfied, and for exactly the same reasons discussed in Section II.B.1 with “based on needs and operation of the integrated circuit,” the Petition should be denied for failing to address the construction of “power island.”

2. Petitioner’s Takahashi Grounds Fail (All Claims, Grounds 1A, 1B, 1C).

Petitioner argues that various embodiments of Takahashi disclose “a plurality of power islands,” but never addresses the gaps between Takahashi and “power islands” in the sense of the ’438 patent. Instead, Petitioner points to structures that Takahashi expressly discloses are **not** “power islands,” then additionally and vaguely proposes a combination of distinct systems in Takahashi in which the details of power control are left to the Board’s imagination. Petitioner does not show that the cited materials teach a “a plurality of power islands.”

a. *Petitioner Fails To Show That Takahashi Discloses Or Renders Obvious “A Plurality Of Power Islands” (All Claims, Grounds 1A, 1B, 1C).*

Each of the challenged claims recites a system comprising a “plurality of power islands,” *i.e.*, more than one “power island.” The Petition correspondingly attempts to identify several purported “power islands” in Takahashi. But Takahashi itself never mentions “power islands,” and Petitioner fails to demonstrate that Takahashi discloses or teaches this limitation.

Takahashi discusses “semiconductor integrated circuit[s] wherein the circuit area can be minimized, and defects can be detected reliably during a standby status while maintaining the reliability of a gate oxide film.” Ex. 1004 [Takahashi] (Abstract).

Takahashi describes systems that consume power in one of two states: an “operation” state (also called an “active” state), and a “standby” state (also called a “sleep” state). *See, e.g., id.*, Abstract (referring to circuit in “an operating status” and “a standby status”), [0017] (“Summary of invention” describing “the present invention” as having a “voltage supply circuit” that “supplies ... [a] first source voltage while the aforementioned functional circuit is in a standby status, and ... [a] second source voltage while the aforementioned functional circuit is operating.”), [0029]-[0030] (describing Figures 4 and 5 as depicting an embodiment “during operation” and “during standby,” respectively), Figs. 4-5, [0031]-[0032] (describing Figures 6 and 7 similarly, for another embodiment), [0033]-[0034] (describing Figures 8 and 9 similarly, for another embodiment), Figs. 8-9, [0041]-[0042]

(describing Figures 16 and 17 as “showing the source voltages generated by the voltage regulator . . . during operation” and “during standby,” respectively), [0110] (describing Figures 14 and 15 as respectively depicting “voltage levels of source voltages” “during” “operation (Active mode)” and “standby (Sleep mode)”), Figs. 14-15.

Petitioner confirms that Takahashi’s systems consume power in two states, “operating” and “standby.” *See, e.g.*, Pet., 7 (describing Takahashi’s Figure 1 via a disclosure in which a “switching circuit . . . supplies an operating current” to a component “during operation” and “suppresses [] leakage current” “during standby”) (quoting Ex. 1004 [Takahashi] [0052]); *see also id.* (quoting Takahashi to the effect that “[D]ifferent levels [of a source voltage] are applied during operation and during standby, respectively”) (quoting Ex. 1004 [Takahashi] [0053]).

In some embodiments of Takahashi, the voltages supplied during “operation” and “sleep” are determined by fuses set after an assessment of the transistors used to fabricate the device. *See, e.g.*, Ex. 1004 [Takahashi] [0098]-[0099], [0109] (“After the production process for device 200 is completed, it is measured using a test circuit in order to extrapolate the driving capabilities of the pMOS transistor and the NMOS transistor constituting device 200 according to the result of the measurement, so that the condition of device 200 . . . can be determined. . . . [F]using circuit 202 can be programmed to set the respective fuses to desired conditions according to the

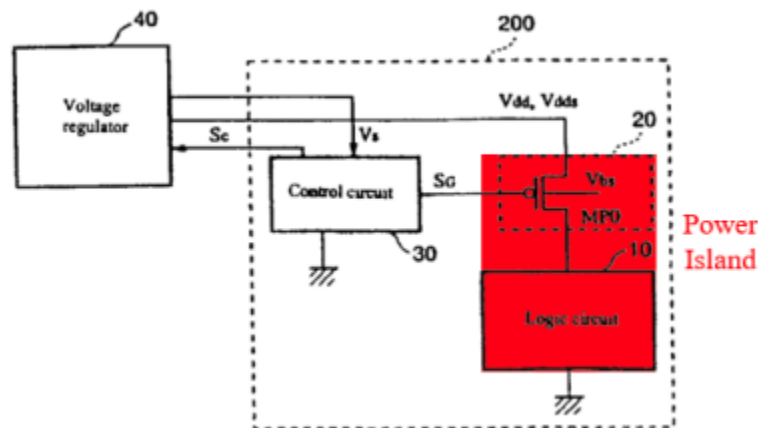
condition of device 200”). In any such embodiment—however any fuses have been set—each component is supplied with one fixed voltage during the “operation” state of the device, and one fixed voltage during the “standby” state of the device. *Id.*, [0109] (“control data DAT in accordance with the condition of device 200 are output by fusing circuit 202”), [0111] (“Voltage regulator 100 generates different levels of source voltages during operation and during standby according to said control data DAT ...”), [0110] (describing Figures 14 and 15 as “show[ing] the voltage levels of source voltages ... generated by voltage regulator 100 according ... control data DAT set based on the process requirements of device 200 during operation (Active mode) and during standby (Sleep mode)”). Again, Petitioner confirms this aspect of Takahashi. *See, e.g.*, Pet. 8 (stating that “The control data DAT [in Takahashi’s Figures 11-17] is ‘based on the process requirements of device 200 during operation (Active mode) and during standby (Sleep mode),’” but that “[t]he ... operation of ‘device 200’ in the embodiment of Figures 11-17 otherwise remains the same as in the embodiment of Figures 1-5”) (quoting Ex. 1004 [Takahashi] [0110])).

In addition to describing devices that can be placed in an “operation” or “standby” state, Takahashi’s Figure 10 separately discloses aspects of a “measuring circuit.” *See, e.g.*, Ex. 1004 [Takahashi] [0087] (“FIG. 10 shows an example of a circuit capable of performing I_{ddq} measurement”), Fig. 10. Takahashi states that its measuring circuit could be used to detect “manufacturing defects.” *See, e.g., id.*,

[0015] (stating that the prior art has “no effective I_{ddq} testing method for detecting manufacturing defects for the aforementioned technologies”), [0095] (“ I_{ddq} of a specific functional circuit can be measured by designing the test pattern input to the scan-pass circuit [of Figure 10] appropriately”).

Petitioner finds alleged “power islands” in three separate embodiments in Takahashi, depicted in its Figures 1, 16 and 10 (discussed by Petitioner in that order).

Petitioner first contends that a POSITA “would have understood and found obvious” that a “logic circuit 10” in Takahashi’s Figure 1 is a power island, providing the following annotation:

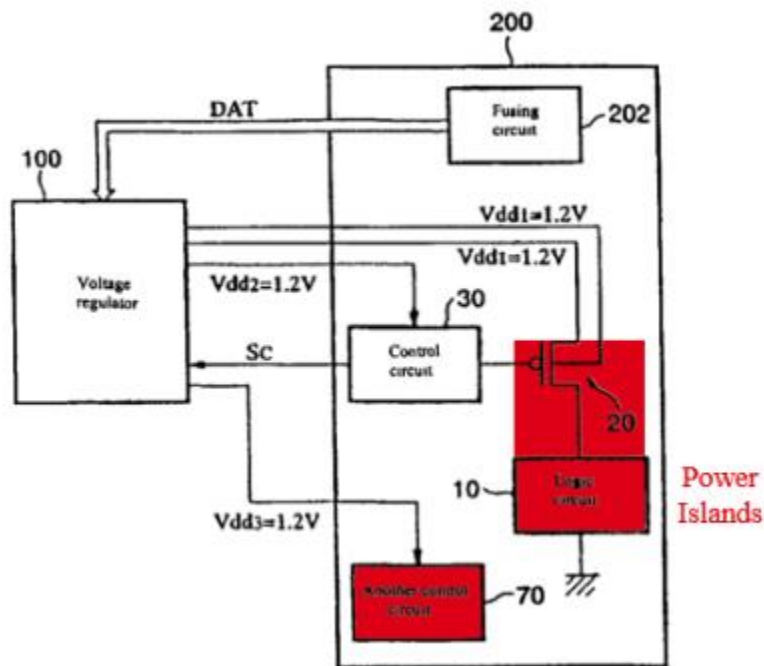


Pet., 11-12. Petitioner contends that “power consumption” within the “logic circuit 10” is “controlled by the ‘switching circuit 20’ that ‘supplies an operating current to logic circuit 10 during operation and suppresses the leakage current of the ... logic circuit 10 during standby.’” *Id.*, 11 (quoting Ex. 1004 [Takahashi] [0052]). This statement is accompanied by a citation to an expert declaration which states that

“when the ‘switching circuit 20’ is on, the ‘logic circuit 10’ receives a voltage V_{dd} to place the ‘logic circuit 10’ into operational mode, and when off, the ‘logic circuit 10’ receives a lower voltage that places the ‘logic circuit 10’ into a low-power standby state.” Ex. 1003 [Min-Decl.] ¶ 102.²

Petitioner then contends that “another control circuit 70” in Takahashi’s Figure 16 is a power island, providing the following annotated version of that figure:

² Petitioner’s annotation of Takahashi’s Figure 1 differs from its expert’s annotation in that Petitioner includes the “switching circuit 20” within a red rectangle that contains “logic circuit 10,” Pet. 12, while Petitioner’s expert does not. Ex. 1003 [Min-Decl.] ¶ 101. Similarly, where Petitioner states that “Takahashi’s logic circuit 10 ... and ‘switching circuit 20’ ... comprise a power island,” Pet., 11, Petitioner’s expert states that “Takahashi’s ‘logic circuit 10’ is a power island,” Ex. 1003 [Min-Decl.] ¶ 101, *i.e.*, not including “switching circuit 20.” Petitioner does not discuss this discrepancy. The Board should consider “power islands” as alleged in the Petition only. See 37 C.F.R. § 42.6(a)(3) (prohibiting incorporation by reference of arguments from one document into another).



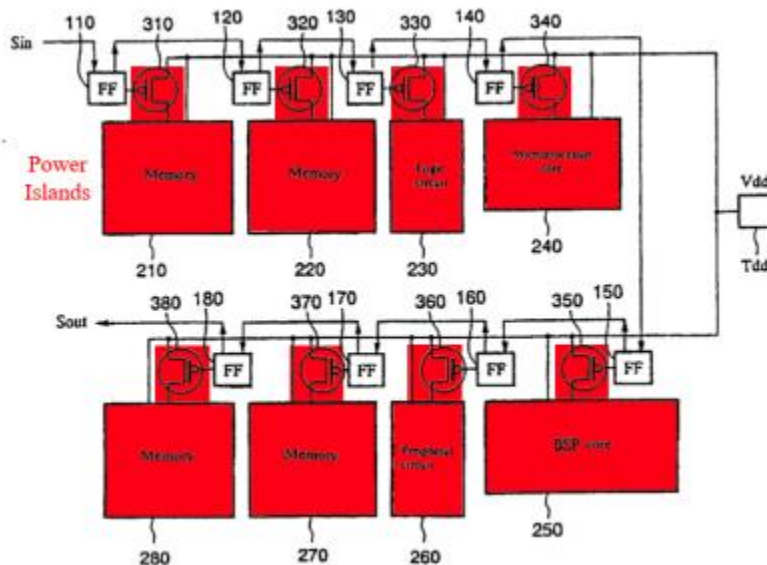
Pet., 12-13. Petitioner argues that “power consumption [within another control circuit 70]” is “controlled by” the separate “source voltage V_{dd3} ’ that varies based on whether it is in an operational or standby state.” *Id.*, 12 (citing Ex. 1004 [Takahashi] [0110]-[0116] & FIGS. 14-17). This statement is accompanied by citation to an expert declaration which states that in Takahashi’s Figure 16, “source voltage V_{dd3} ’ varies between 1.2V and 0.7V based on whether the ‘Wake up logic’ is in an operational or standby state.” Ex. 1003 [Min-Decl.] ¶ 104.³

³ As with Takahashi’s Figure 1, *see supra* note 2, Petitioner and Petitioner’s expert differ in how they identify alleged “power islands” in Figure 16: Petitioner

Petitioner then contends that a “POSITA would have found it obvious for Takahashi’s integrated circuit, such as those depicted in Figures 1-5 and 11-17, to include multiple additional power islands.” Pet., 13. The alleged source of inspiration for these “additional power islands” is Takahashi’s measuring circuit Figure 10—each of whose circuits 210-280 “along with their respective ‘pMOS transistors 310, 320, ... , and 380’ (i.e., sleep transistors)” is alleged by Petitioner, without explanation, to “comprise[] a power island.” *Id.*, 14. Significantly, Petitioner does not identify how the power consumptions of the circuits 210-280 are allegedly controlled, and thus fails to show any plurality of “power islands” in Figure 10. Material not cited by Petitioner should not be considered. *See* 37 C.F.R. § 42.6(a)(3) (prohibiting incorporation by reference of arguments from one document into another). Petitioner’s expert states that each circuit 210-280 along with its respective pMOS transistor 310-380 is a “power island” because “power consumption within each of the functional circuits 210-280 in Figure 10 is controlled by the ‘switching circuit ... with pMOS transistors 310, 320, ... , and 380’” in the

includes Figure 16’s “switching circuit 20” in an alleged “power island” that contains “logic circuit 10,” Pet., 13, while Petitioner’s expert does not. Ex. 1003 [Min-Decl.] ¶¶ 103-104.

circuits 210-280. Ex. 1003 [Min-Decl.] ¶ 107 (citing Ex. 1004 [Takahashi] [0090]).



Ex. 1004 [Takahashi] Fig. 10 (as annotated by Petitioner, Pet., 14).⁴ But Petitioner’s expert does not identify any component responsible for changing the states of the transistors 310-380 in Takahashi’s Figure 10, whether in Takahashi’s Figure 10, or anywhere else. See Section II.C.2.a.iii.

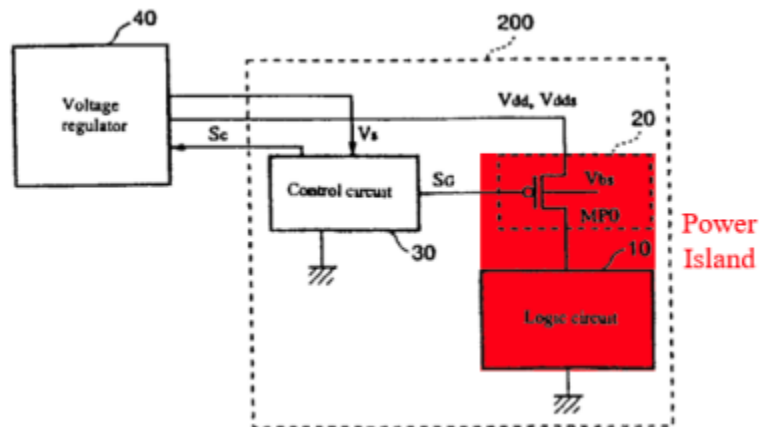
As a threshold matter, none of these three systems—Takahashi’s Figure 1, Takahashi’s Figure 16, or Takahashi’s Figure 10—discloses “a plurality of power

⁴ Once again, see *supra* note 2 and 3, Petitioner and Petitioner’s expert analyze this figure differently: Petitioner includes transistors 310-380 with the blocks 210-280 in its alleged “power islands”, Pet., 14, while Petitioner’s expert does not. Ex. 1003 [Min-Decl.] ¶ 106.

islands,” as required by all challenged claims. Petitioner’s arguments that systems comprising “a plurality of power islands” are nevertheless obvious in view of these disparate disclosures are conclusory.

i. Petitioner Admits That Takahashi’s Figure 1 Does Not Disclose “A Plurality Of Power Islands.”

Petitioner admits that Takahashi’s Figure 1 does not disclose a “plurality of power islands.” Petitioner’s annotation of Takahashi’s Figure 1 identifies only a block consisting of the “logic circuit 10” and “switching circuit 20” as a power island, Pet., 11—implicitly admitting that at most, Takahashi’s Figure 1 discloses at most a single power island, not “a plurality of power islands”:



Pet., 12 (Fig. 1 of Takahashi, as annotated by Petitioner).

Petitioner confirms this reading of Figure 1 when it elsewhere states in conclusory terms that “a POSITA would have found it obvious for Takahashi’s integrated circuit, such as those depicted in Figures 1-5 and 11-17, to include

multiple additional power islands.” Pet., 13 (citing Ex. 1003 [Min-Decl.] ¶¶ 105-106, stating the same conclusion).⁵ Although Petitioner does not elaborate upon the relevance of including “multiple additional” power islands in Figure 1, Petitioner is implicitly attempting to address the fact that Takahashi’s Figure 1 does **not** include “multiple” power islands to begin with—*i.e.*, that Figure 1 does not disclose “a plurality of power islands.”

ii. Petitioner Does Not Show That Takahashi’s Figure 16 Discloses “A Plurality Of Power Islands.”

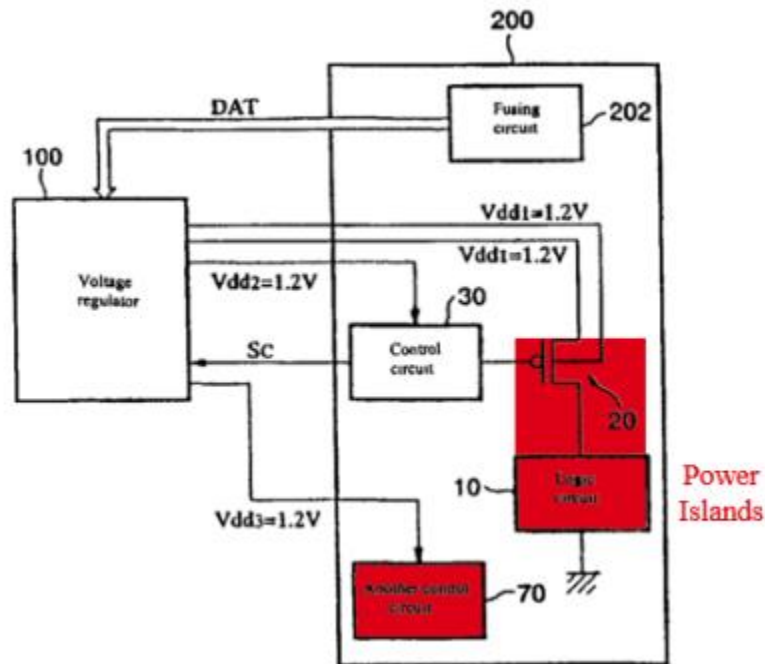
Petitioner argues that Takahashi’s Figure 16 teaches a plurality of power islands in its disclosure of a “logic circuit 10” and its “switching circuit 20” (one purported power island), and in its “another control circuit 70” (a second power island, or at least a part of a second allegedly obvious power island). See Pet., 13. It is not clear whether Petitioner takes the position that “another control circuit 70” in Takahashi’s Figure 16 is by itself a second “power island” (as suggested by Petitioner’s annotation of Figure 16, Pet., 13), or whether Petitioner argues only that it would be obvious for “another control circuit 70” to be **part of** a second “power island” in a modification that added circuitry not present in Figure 16 (as suggested

⁵ Petitioner’s alleged motivation to make this modification, see Pet., 14-15, is discussed further in Section II.C.2(b) below.

by Petitioner’s argument that a POSITA “would have found it obvious to include another ‘switching circuit 20’ . . . to further reduce power consumption . . . in ‘control circuit 70,’” Pet. 13).⁶ Either way, Petitioner’s analysis is again flawed, because Petitioner simply asserts that these components are power islands without engaging with the essential characteristics of a “power island.” As discussed above, in the co-pending litigation, the parties’ proposed constructions of “power island” agree that a power island is a section of an integrated circuit where power consumption is controlled by independently varying at least one of its operating voltage and its frequency of operation. *See* Section II.C. Petitioner does not even attempt to argue that this is the case, *see id.*, and this is not the case.

Petitioner’s annotated version of Figure 16 is again reproduced below:

⁶ This ambiguity is compounded by the discrepancy between Petitioner’s and Petitioner’s expert’s readings of Figure 16. *See supra* note 3.



Pet., 13 (Figure 16 as annotated by Petitioner, showing “logic circuit 10” and “another control circuit 70” as parts of alleged power islands within “device 200”); *see also id.*, 12 (citing Ex. 1004 [Takahashi] [0110]). Both of Petitioner’s alleged “power islands” are part of a single component (Figure 16’s “device 200”) that Takahashi discloses as having two alternative states: “operation” (or “active”) and “standby” (or “sleep”), as discussed above.

For good reason, Petitioner does not argue, let alone demonstrate, that the blocks it annotates in red are “power islands” under the *Freescale* or *Xilinx* district court constructions proffered by Patent Owner and Petitioner, respectively, in the co-pending district court litigation. *See* Section II.C.1. Under those constructions,

a “power island” is “a section of an integrated circuit where power consumption is controlled by ***independently varying*** its operating voltage and its frequency of operation” or “***independently varying*** its operating voltage or its frequency of operation (or both).” *See id.* Petitioner does not even attempt to identify evidence that power consumption in either block is “controlled by ***independently varying*** its operating voltage [and/or] its frequency of operation [or both].”

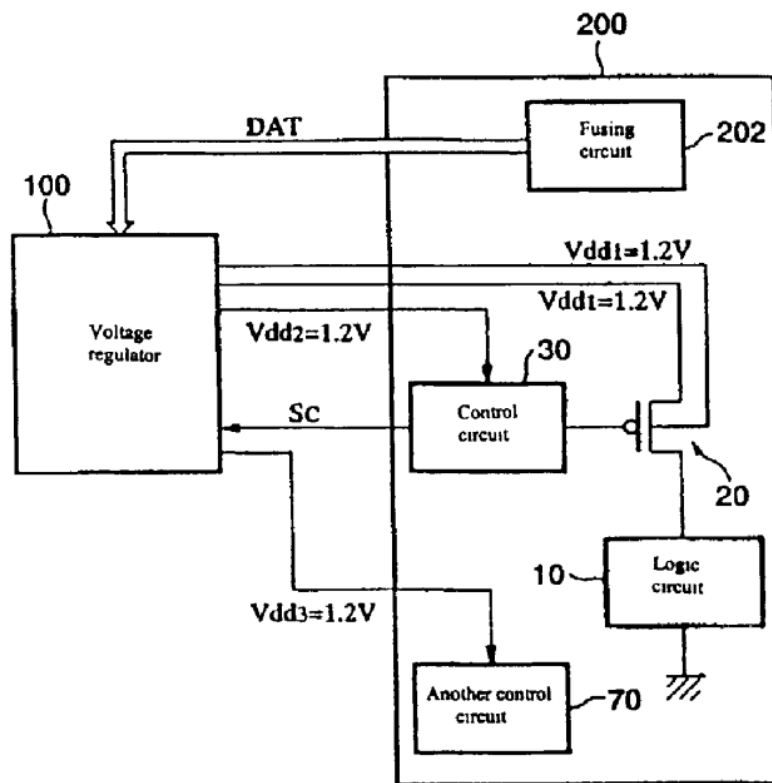
To the contrary, Takahashi discloses that the voltages supplied to “logic circuit 10” and “another circuit 70” in Figure 16 are not independently varying, but regulated together. The “logic circuit 10” and “another circuit 70” are parts of a single “device 200.” *See* Ex. 1004 [Takahashi] Fig. 16. Takahashi discloses that the “logic circuit 10” and “another circuit 70” receive one voltage when the “device 200” is in its “operation” state, and another voltage when the “device 200” is in its “standby” state. *See, e.g., id.*, [0112] & Fig. 16 (labeling the voltages supplied to “logic circuit 10” and “another circuit 70” in Figure 16 as “ V_{dd1} ” and “ V_{dd3} ,” respectively), [0110] (referring to “voltage levels of source voltages V_{dd1} ... and V_{dd3} ” within “device 200 during operation (Active mode) and during standby (Sleep

mode)”)”; [0111] (stating that “Voltage regulator 100 [in Figure 16] generates different levels of source voltages during operation and during standby”). Petitioner acknowledges that the voltages supplied to “logic circuit 10” and “control circuit 70” are regulated **together** (and are not independently varying) when arguing that “in ‘Active mode,’ the ‘voltage regulator’ provides an ‘operating voltage’ to the ... circuitries, including ‘logic circuit 10’ **and** ‘control circuit 70,’” while “[d]uring ‘Sleep mode,’ the ‘voltage regulator’ lowers the voltage signals to place the ... circuitries, including “logic circuit 10” **and** ‘control circuit 70,’ into a low-power standby status.” Pet., 18.

Indeed, Takahashi not only discloses that the voltages supplied to “logic circuit 10” and “control circuit 70” in its Figure 16 are not regulated independently, Takahashi discloses that the voltages supplied to these components are **exactly the same** in either state of the “device 200.”

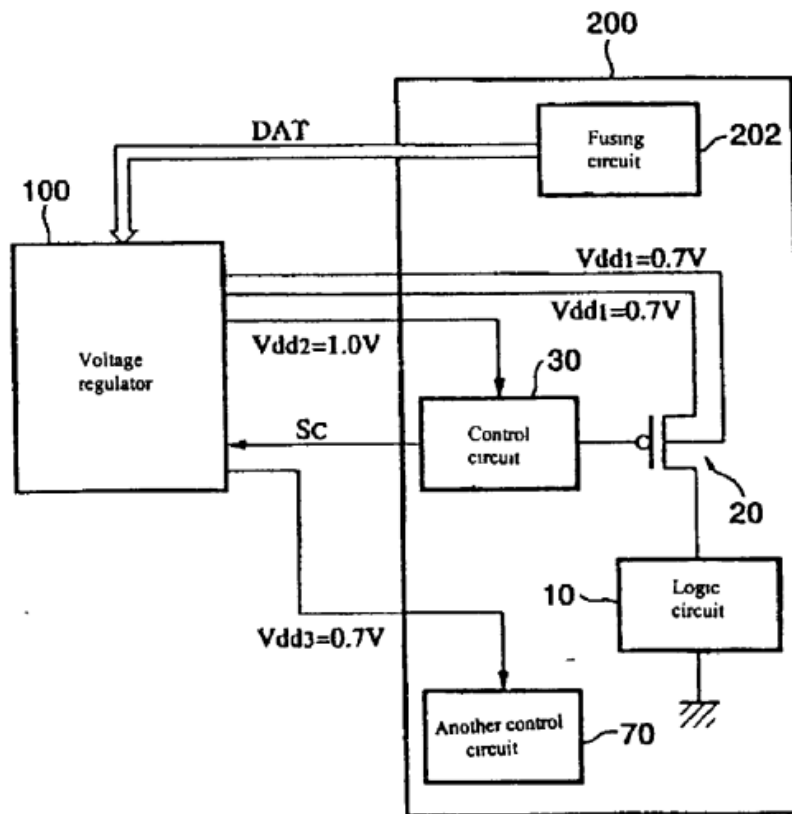
⁷ Although many of Takahashi’s Figures 11-17 do not individually disclose every feature of Takahashi’s Figure 16, Petitioner invites the Board to read these figures as though they describe the Figure 16 embodiment, *see, e.g.*, Pet., 8 (referring to an embodiment “shown in Figures 11-17”), and for purposes of the Board’s institution decision, Patent Owner assumes that they do so.

Figure 16 expressly provides that the same 1.2V is supplied to “logic circuit 10” (as “ V_{dd1} ”) and to “another control circuit 70” (as “ V_{dd3} ”) during the “operation” state of the “device 200”:



Ex. 1004 [Takahashi] Fig. 16, [0112] (“FIG. 16 is a circuit diagram showing source voltages V_{dd1} , V_{dd2} , and V_{dd3} generated by voltage regulator 100 during **operation**”).

Figure 17 similarly expressly provides that the same 0.7V is supplied to “logic circuit 10” (as “ V_{dd1} ”) and to “another control circuit 70” (as “ V_{dd3} ”) in the “standby” state of the “device 200”:



Ex. 1004 [Takahashi] [0114] (“FIG. 17 is a circuit diagram showing source voltages V_{dd1} , V_{dd2} , and V_{dd3} generated by voltage regulator 100 during *standby*”).

As mentioned above, see Section II.C.1.a, Takahashi discloses variations of its Figure 16 in which the “fusing circuit 202” is configured differently. Takahashi’s Figure 16 depicts a system where the transistors comprising the “device 200” were “weak,” and the values of the voltages V_{dd1} , V_{dd2} , and V_{dd3} correspondingly set to voltages deemed appropriate by the designer for “weak” transistors. See, e.g., Ex. 1004 [Takahashi] [0117] (“process requirements of device 200 are decided through inspections, the fuses in fusing circuit 202 are disconnected accordingly through

programming, and control data DAT in accordance with the process requirements of device 200 is output into voltage regulator 100”); [0113] (Figure 16 is labeled “assuming, for example, that the transistors constituting device 200 are in the ‘Weak’ section under the process requirements”); [0099] (“when the driving capabilities of the transistors are weak, the levels of the source voltages supplied to device 200 are set high.”). When “fusing circuit 202” is configured differently (because the transistors comprising the “device 200” are classified as something other than “weak”), Takahashi discloses that the voltages V_{dd1} and V_{dd3} supplied to the “logic circuit 10” and “another control circuit 70” may be set to other values than those depicted in Figure 16. *See, e.g., id.*, [0117]. Even in these alternate configurations, however, Takahashi discloses that the voltages supplied to the “logic circuit 10” and “another control circuit 70” are ***the same***—not independently varying—in either state of the “device 200.”

Petitioner’s annotations of Takahashi’s Figures 14 and 15 confirm this by disclosing that whether the transistors of a device are classified as “weak,” “strong,” or other possibilities, the voltage “ V_{dd1} ” supplied to the “logic circuit 10” is the same as the voltage “ V_{dd3} ” supplied to “another circuit 70” in both states of the device:

Active Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	1.2V	1.2V	1.20V	Weak
Fuse prog-1	0	0	1	1.15V	1.15V	1.15V	NTPW,NWPT
Fuse prog-2	0	1	0	1.05V	1.05V	1.05V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.95V	0.95V	0.95V	NSPT,NTPS
Fuse prog-4	1	0	0	0.85V	0.85V	0.85V	Strong

FIG. 14

Sleep Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

Pet., 19 (Petitioner's annotation of Ex. 1004 [Takahashi] FIGS. 14 & 15, depicting "V_{dd1}" and "V_{dd3}" as the same in each "Process requirement"). (Here the "operation" state of "device 200" is labeled as "Active mode" and the "standby" state of "device 200" is labeled as "Sleep mode." Ex. 1004 [Takahashi] [0110]-[0111].)

In sum: Petitioner's analysis of Figure 16 cites embodiments where the voltages supplied to the "logic circuit 10" and "another control circuit 70" are **the same** during **every** state of the "device 200" of which they are a part. Petitioner nowhere analyzes any frequencies of operation of these components. Petitioner therefore makes no showing that Takahashi's Figure 16 discloses "a plurality of power islands" in its "logic circuit 10" or "another circuit control 70" under either

party's proposed district court construction of "power island." See Section II.B.

Even if the Board did not adopt either prior district court construction, an interpretation of "power island" would at a minimum have to be consistent with the '438 patent disclosure that "[a] power island is any section, delineation, partition, or division of an integrated circuit where power consumption is **controlled within** the section ..." Ex. 1001 ['438] 3:62-65. One would not regard power consumption as "controlled within" a section of circuitry when power consumption of that section is **only** variable in ways that affect power consumption in **other** circuitry. Yet this is Petitioner's argument.

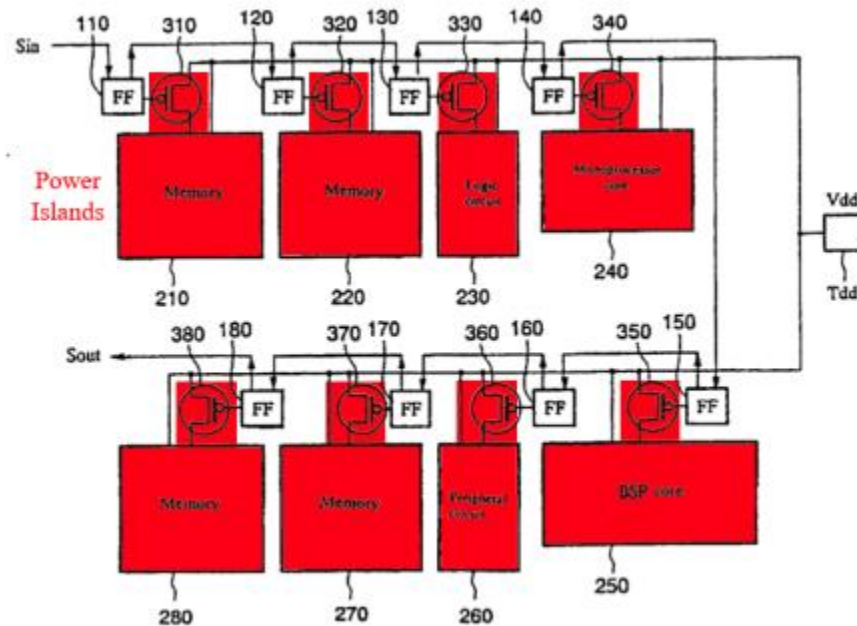
Petitioner states, for example, that "power consumption" within another control circuit 70 is "controlled by" the separate "source voltage V_{dd3} " that varies based on whether it is in an operational or standby state." Pet., 12 (citing Ex. 1004 [Takahashi] [0110]-[0116] & FIGS. 14-17). Here, the word "it" in Petitioner's "whether it is in an operational or standby state" can only be understood consistently with Takahashi as a reference to the "device 200" of which "another control circuit 70" is a part. Takahashi nowhere discloses, for example, "another control circuit 70" being provided with the " V_{dd3} " of 1.2 V associated with "operation" in Figure 16, Ex. 1004 [Takahashi] [0041], at the same time that "logic circuit 10" is provided with the " V_{dd1} " of 0.7 V associated with "standby" in Figure 17. Ex. 1004 [Takahashi] [0042]. To the contrary, Takahashi states that its Figure 16 describes

the “source voltages V_{dd1} , V_{dd2} , **and** V_{dd3} generated by voltage regulator 100 **during operation**,” while its Figure 17 describes “source voltages V_{dd1} , V_{dd2} , **and** V_{dd3} generated by voltage regulator 100 **during standby**.” Ex. 1004 [Takahashi] [0112], [0114].

Petitioner’s argument, then, is that “another control circuit 70” in Takahashi’s Figure 16 is a “power island” because the entire device 200 can be in an “operation” or “standby” state. Far from showing that power consumption is controlled **within** “another control circuit 70” in Figure 16, however, this shows that power consumption is **not** controlled within “another control circuit 70” in Figure 16, but at most within a larger circuit—contrary to the specification’s teachings about “power islands.” For at least these reasons, Petitioner has not shown that Takahashi’s Figure 16 discloses “a plurality of power islands.”

iii. Petitioner Does Not Show That Takahashi’s Figure 10 Discloses Or Teaches “A Plurality Of Power Islands.”

Petitioner also alleges that Takahashi’s Figure 10 discloses “power islands.” Pet., 13-16. Petitioner’s annotation of this figure is reproduced below. Petitioner contends that “[e]ach of these functional circuits 210-280 ... along with their respective ‘pMOS transistors 310, 320, ..., and 380’ ... comprises a power island.”



Pet., 14 (Petitioner's annotation).

As an initial matter, Petitioner, quite rightly, does not argue that Takahashi's Figure 10 discloses a system for practicing the entirety of any challenged claim. Petitioner does not, for example, identify any "control signal" or "adaptive leakage controller" in Figure 10, nor does Petitioner contend that Figure 10 (or its corresponding disclosure) teaches "dynamically chang[ing] power consumptions" or changing or generating a "variable voltage to be applied to ... sleep transistors." *Cf.* Ex. 1001 ['438] cls. 1-19. Petitioner cannot make such arguments because Petitioner does not identify anything in Figure 10 that modifies the states of the pMOS transistors 310-380, let alone modifies these states such that the power consumption in any functional circuit 210-280 is controlled by independently

varying its operating voltage or frequency of operation.

In more detail, Takahashi describes its Figure 10 as directed towards an “ I_{ddq} Measuring circuit” capable of “performing I_{ddq} measurement,” *i.e.*, testing for manufacturing defects. Ex. 1004 [Takahashi] [0085]-[0087] (“FIG. 10 shows an example of a circuit capable of performing I_{ddq} measurement.”); [0015] (“In addition, there is no effective I_{ddq} testing method for detecting manufacturing defects for the aforementioned technologies.”). The disclosure accompanying Takahashi’s Figure 10 correspondingly focuses on the setup of I_{ddq} measurement, and not on the use of any circuit that includes Figure 10’s “functional circuits.” *Id.*, [0091]; [0094] (“power consumption of the respective functional circuits ... can be measured using the measuring circuit of the present example by designing a test pattern to be input into the scan-pass circuit appropriately.”); [0095] (“by controlling the on/off status of the respective transistors ... I_{ddq} of a specific functional circuit can be measured”).

Takahashi discloses that the components 210-280 in Figure 10 are “functional circuits to be operated using source voltage V_{dd} .” *Id.*, [0089]. During I_{ddq} measurement, the “scan-pass circuit” of Figure 10 “is configured with flip-flops 110, 120, ... , and 180” via “[t]est data S_{in} input” that “is transferred to the output side one after another by said scan-pass circuit.” *Id.*, [0088]. The “pMOS transistors 310, 320, ... , and 380 ... are turned on/off according to the data held in respective flip-flops 110, 120, ... , and 180 in order to supply a driving current to a prescribed

functional circuit when in the on status.” *Id.* [0090].

Takahashi offers the following example of the transistors being “turned on/off according to the data held in respective flip-flops 110, 120, ... , and 180”:

For example, ***when the test pattern is designed appropriately***, data [logic] 0 is stored into flipflop 130, and data [logic] 1 is stored into all the other flip-flops. Under said condition, transistor 330 is on, and the other transistors are all off. Thus, driving current is supplied to logic circuit 230, and logic circuit 230 becomes operational. On the other hand, because no driving current is supplied to any functional circuits other than logic circuit 230, these functional circuits are all in the standby status.

Ex. 1004 [Takahashi] [0092]. Significantly, Takahashi does not say that any ***component of Figure 10*** provides the “test pattern,” or that any component of Figure 10 is otherwise responsible for controlling the on/off status of the transistors 310-380. Similarly, the disclosures cited by Petitioner, *see generally* Pet., 14, 16 (citing Ex. 1004 [Takahashi] [0089]-[0090], [0092]) show only that during I_{ddq} measurement, the states of transistors 310-380 and the operational/standby states of the corresponding functional circuits correspond with one another, following the “test pattern” input—that is, a transistor is on (and its corresponding functional circuit operational) during the measurement, or off (and its functional circuit in standby) during the measurement, according to data supplied by a “test pattern” from

a source not depicted in Figure 10. See, e.g., Ex. 1003 [Takahashi] [0092].

Takahashi is silent on what specifies or generates any given “test pattern.”

Instead, Takahashi contains repeated disclosures, not cited by Petitioner, suggesting that Takahashi’s Figure 10 does not provide any control of the states of the transistors 310-380. Quoting selectively, for example, Petitioner states:

Takahashi discloses that each of “pMOS transistors 310, 320, ..., and 380” of the “switching circuit” can be turned off so that the “occurrence of a leakage current in the [respective] functional circuit can be suppressed.”

Pet., 16 (quoting Ex.1004 [0090]). Petitioner omits what little Takahashi says about **how** its transistors are turned on/off: the sentence cited by Petitioner states that

[t]hese transistors are turned on/off **according to the data held in respective flip-flops 110, 120, ..., and 180** in order to supply a driving current to a prescribed functional circuit when in the on status.

Ex. 1004 [Takahashi] [0090]. And Takahashi is silent on what supplies “the data held in respective flip-flops 110, 120, ... , 180,” stating only that that the “on/off status of [the] respective transistors 310, 320, ... , and 380 [in Figure 10] **can be** controlled individually **by designing a pattern ... of test data input** into the scan-pass circuit **appropriately.**” *Id.*, [0091]; see also *id.*, [0092] (discussing how components of the logic circuits in Figure 10 may behave “when the test pattern is **designed appropriately**”), [0094] (stating “power consumption of the respective

functional circuits during the operation can be measured using the measuring circuit of the present example by *designing a test pattern* to be input into the scan-pass circuit *appropriately*.”).

Petitioner does not address these disclosures in Takahashi, let alone address any differences that might exist between any mechanism used to set the “on/off status” of the “transistors 310, 320, ... , and 380” via the “test data input into the scan-pass circuit” of Figure 10, Ex. 1004 [Takahashi] [0091], and the mechanism that Petitioner discusses in connection with the “power islands” alleged to exist in Figures 1 and 16—namely, the “voltage regulator” of those figures. *See, e.g.*, Pet. 17-18 (stating that Takahashi’s “‘voltage regulator’ ... controls power within the power island[s]”). Takahashi’s Figure 10 does not, for example, depict any “voltage regulator.”

In any event, under either party’s proposed district court construction, a “power island” is a portion of an integrated circuit “where power consumption *is controlled* by independently varying” at least one power characteristic of that portion—its “operating voltage,” its “frequency of operation,” or both. *See* Section II.B. As Takahashi is silent on how the states of transistors 310-380 in its Figure 10 are set—stating only that they are determinable by designing a test pattern “appropriately”—Petitioner’s cited disclosures do not show that the functional circuits 210-280 are “power islands” in Figure 10. Here, Petitioner makes a basic

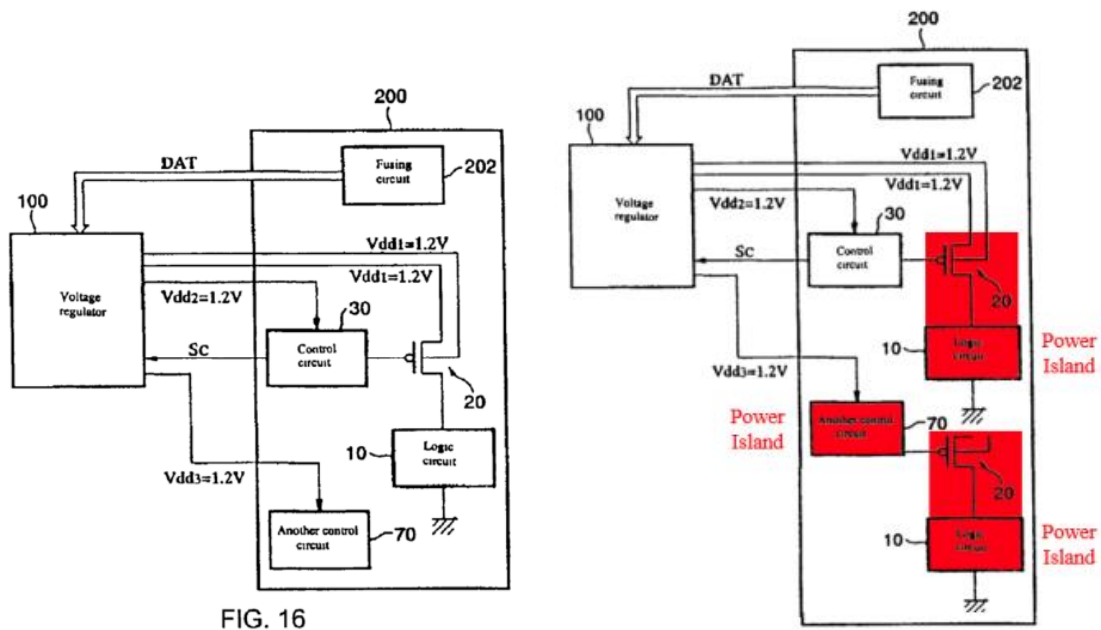
error: confusing a disclosure of components that **could be** power islands in an “appropriately” designed system with components that **are** power islands because of how a system is actually configured to control them.

Even if the Board did not adopt the construction proposed by either party in the co-pending litigation, “power island” should be interpreted consistently with the ’438 patent’s disclosure that “[a] power island is any section, delineation, partition, or division of an integrated circuit where power consumption is **controlled** within the section, delineation, partition, or division.” Ex. 1001 [’438] 3:62-65. Again, because Takahashi does not disclose how the states of transistors 310-380 in its Figure 10 are set (except to say that they can be determined by designing a test pattern “appropriately”), Petitioner has not shown that the power consumptions of the functional circuits 210-280 are controlled in Figure 10 consistent with this disclosure.

Petitioner implicitly acknowledges that Takahashi’s Figure 10 might not disclose “a plurality of power islands” in its proposed obviousness combination, in which Petitioner proposes that Figure 10 teaches inclusion of “multiple additional power islands” in Takashi’s Figure 16. See Pet., 13-15. (Petitioner has not offered any non-conclusory basis for a motivation to combine these disclosures, as discussed elsewhere. See Section II.C.2.b.) In this proposal, Petitioner does not rely on Takahashi’s Figure 10 for any control of alleged “power islands” in its proposed

combination. Petitioner's failure to use Takahashi's Figure 10 for this purpose makes sense because, as explained above, Takahashi's Figure 10 does not itself disclose "a plurality of power islands." Petitioner does not show how the proposed combination discloses "a plurality of power islands" either.

In more detail, citing Takahashi's Figure 10, Petitioner states that "[a] POSITA would have found it obvious to incorporate multiple power islands as shown in Figure 10 into the embodiments of Figures 1-5 and 11-17." *Id.*, 14. Petitioner argues that a POSITA "would have understood that" Takahashi's Figure 16 embodiment, for example, could "include more than one 'logic circuit' and been motivated to provide a 'switching circuit' ... for each to suppress leakage current and obtain the same power savings described for Figure 10." *Id.*, 14-15. Petitioner includes a modified version of Takahashi's Figure 16, which is reproduced to the right of Takahashi's actual Figure 16 below.



Ex. 1004 [Takahashi] Fig. 16; Pet., 15 (Fig. 16 as modified by Petitioner).

Although Petitioner styles its modification of Figure 16 as “incorporat[ing] multiple power islands as shown in Figure 10 into the embodim[en]t[] of” Figure 16, Pet., 14, the mechanism of controlling power within the alleged “power islands” in this modification is not from Figure 10. In the modified figure, Petitioner proposes that a POSITA “would have understood that a device can include more than one ‘logic circuit’ and been motivated to provide a ‘switching circuit’ for each,” and implies (by what it does not modify in Figure 16) that the circuit would somehow employ the voltage regulator of Figure 16. Pet., 14-15. Petitioner proposes, in other words, that components *already present* in Figure 16 be *uplicated* (as to “include more than one ‘logic circuit’ and ... a ‘switching circuit’ ... for each,” *id.*, 14), and that control of the resulting system somehow be implemented by some form of the

“voltage regulator 100” ***already present*** in Figure 16. No mention is made of any “flip-flops” configured with “test data” from an input S_{in} to a “scan-pass circuit,” as identified by Petitioner’s expert (but not Petitioner) in connection with alleging that Takahashi’s disclosed “power islands” in the functional circuits 210-280 of Figure 10. *See* Ex. 1003 [Min-Decl.] ¶ 107. Presumably, Petitioner’s combination does not draw from Figure 10 for this purpose because Petitioner seeks a combination that would embody the challenged claims. *See, e.g.,* Pet., 21 (annotating Takahashi’s Figure 16 with labels indicative of claim limitations other than “power island”). If control in Petitioner’s modified Figure 16 required unspecified “test data” from an unidentified source (as it does in Figure 10), perhaps even Petitioner would presumably admit that the system did not embody the challenged claims, just as Petitioner does not argue that Figure 10 embodies any challenged claims.

Petitioner’s proposal that power consumption in the purported “power islands” in its modification of Figure 16 could be controlled by a modified version of the voltage regulator in Figure 16 fares no better. As explained above, the components in un-modified Figure 16 are not “power islands” because Takahashi expressly discloses that their supply voltages are regulated together—according to the state of the “device 200” of which they are a part. *See* Section II.C.2(a)(ii). In proposing that “[a] POSITA would have understood that a device [as in Figure 16] can include more than one ‘logic circuit’ and been motivated to provide a ‘switching

circuit’ ... for each,” Pet., 14, Petitioner proposes adding more components to Takahashi’s Figure 16 without explaining how the voltage regulator in the modification would be configured to provide independently varying voltages. In not addressing this issue, Petitioner’s “analysis” of its modified Figure 16 simply takes for granted that Takahashi’s Figure 16 already discloses a “plurality of power islands”—which it does not. See Section II.C.2(a)(ii).

For at least these reasons, Petitioner does not show that Takahashi’s Figure 10 discloses or renders obvious “a plurality of power islands.”

b. *Petitioner’s Arguments That Takahashi Renders Obvious
“A Plurality Of Power Islands” Are Conclusory.*

Although Petitioner’s Grounds 1A, 1B, and 1C are styled as single-reference obviousness grounds, Petitioner never acknowledges—not even in the alternative, or for purposes of argument only—exactly **how** the disclosures it cites might fail to anticipate the challenged claims. One is left wondering whether Petitioner is arguing obviousness at all (*i.e.*, whether Petitioner is actually arguing that the cited embodiments of Takahashi necessarily practice the challenged claims), whether Petitioner’s argument is that a cited system could obviously have been configured to practice the challenged claims even if it would not necessarily do so, or whether Petitioner is drawing upon the alleged understanding of the POSITA to modify or combine disclosures in Takahashi. Because of this lack of specificity, it is no

surprise that Petitioner’s arguments are conclusory and fail.

i. Petitioner Does Not Distinguish Alleged
Teachings Of Takahashi From Express Disclosures
In Takahashi.

Separately from arguing that Takahashi discloses “a plurality of power islands,” the Petition states in the alternative that Takahashi renders this limitation obvious. But the only arguments offered specifically for purposes of Petitioner’s obviousness arguments are conclusory. The Petition’s failure to articulate a substantive obviousness argument is a consequence of its failure to expressly identify—even in an alternative, or for the purposes of argument—exactly where Takahashi might fail to disclose a “plurality of power islands.” Petitioner’s refusal to expressly acknowledge where the cited disclosures might **not** disclose the claimed invention is contrary to the law of obviousness, which requires identification of “the differences between the subject matter sought to be patented and the prior art” 35 U.S.C. § 103 [pre-AIA], *see also, e.g., KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966)).

As one example, the Petition states that a POSITA “would have understood **and found obvious** that Takahashi’s logic circuit 10 ... and ‘switching circuit 20’ ... depicted in at least Figures 1, 4-10, and 16-17, comprise a power island,” Pet., 11, but only discusses express disclosures of Takahashi in connection with “logic circuit 10” and “switching circuit 20,” and does not separately argue obviousness. *See id.*

As another example, the Petition states in connection with its discussion of Takahashi's Figures 1-5 and 11-17 that a POSITA "would have found it obvious for Takahashi's integrated circuit ... to include multiple additional power islands." Pet., 13. Implicitly, this statement is an acknowledgement that Takahashi's Figures 1-5 and 11-17 might **not** disclose a "plurality of power islands." The argument that follows, however, depends upon the assumption that Takahashi's Figure 10 **already** discloses "a plurality of power islands," see, e.g., *id.*, 13-15 (arguing that "[a] POSITA would have found it obvious to incorporate **multiple power islands as shown in Figure 10** into the embodiments of Figures 1-5 and 11-17"), which it does not. See Section II.C.2(a)(iii). The Petition, that is, never expressly makes clear how the claimed systems could be obvious in view of Takahashi, unless a system comprising "a plurality of power islands" were already assumed to be disclosed by Takahashi.

Indeed, in many places, Petitioner's arguments refer not to a specific embodiment of Takahashi, or to Petitioner's proposed modification of the Figure 16 embodiment of Takahashi, but to "Takahashi's integrated circuit"—making it difficult to determine what Petitioner is even arguing renders the challenged claims obvious. The following chart illustrates Petitioner's scattershot approach in the context of claim 1.

Claim 1 element as labeled by Petitioner ⁸	Embodiments in Petitioner’s argument
1[a]	Figure 1 (<i>e.g.</i> , Pet., 12) Figure 16 (<i>e.g.</i> , Pet., 13) Figure 10 (<i>e.g.</i> , Pet., 14, 16) Modification of Figure 16 to “include additional power islands” as allegedly taught by Figure 10 (<i>e.g.</i> , Pet., 15)
1[b]	Figure 1 (<i>e.g.</i> , Pet., 17) Figure 16 (<i>e.g.</i> , Pet., 18)
1[c]	Figures 1 and 16 (<i>e.g.</i> , Pet., 21-22)

As this chart indicates, it is possible to read Petitioner as arguing that claim 1 is separately rendered obvious by Takahashi’s Figure 1 alone and by Takahashi’s Figure 16 alone, but the Petition never expressly states either one of these contentions—or identifies why these embodiments of Takahashi might render claim 1 obvious even if they do not anticipate it. Petitioner’s “obviousness” arguments

⁸ The labels “1[a],” “1[b],” and “1[c]” refer to Petitioner’s partition of claim 1 into elements. Pet., vii.

should be rejected for this lack of specificity. *See, e.g., Valeo N. Am., Inc. v. Magna Elecs., Inc.*, IPR2014-01206, Paper 13, 15 (Dec. 23, 2014) (denying institution and noting that “Petitioner’s obviousness analysis is incomplete in that it: fails to state explicitly the differences between the [prior art] and the claimed subject matter, does not explain persuasively the relevance of the evidence, and presents conclusory assertions regarding how the references are combined.”); *Matterport, Inc. v. Appliance Computing III, Inc.*, IPR2021-00939, Paper 15, 16-17 (Nov. 23, 2021) (denying institution because “Petitioner does not identify differences between [cited art] and element 1.2 or how Petitioner proposes to combine or modify the asserted prior art to meet element 1.2.”).

ii. Petitioner Offers Only Conclusory Statements, Not Evidence, About The Motivation To Combine Takahashi’s Distinct Disclosures In The Way Proposed By Petitioner.

Even when arguing obviousness based upon a single reference, a motivation must exist for combining features of different embodiments or otherwise modifying the teachings of a reference. *See, e.g., In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000). In determining whether there is a motivation to combine, there must be “particular” findings of a reason the ordinary artisan, with no knowledge of the claimed invention, “would have selected these components for combination in the manner claimed.” *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1069 n.4

(Fed. Cir. 2018).

The Petition asserts that a POSITA would have been motivated to modify Takahashi's Figures 1 and Figure 16 "to incorporate multiple additional power islands" "to provide additional functionality (*e.g.*, memory)" and to "control their individual power consumption," Pet., 14, and to "obtain the same power savings described for Figure 10." *Id.*, 15. These arguments are legally insufficient and unsupported by evidence.

First, a generically stated desire to improve something is insufficient, without more, to show that a POSITA would have combined features in a particular way. In *ActiveVideo Networks, Inc. v. Verizon Commc 'ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012), for example, the challenger's expert testified that "[t]he motivation to combine would be because you wanted to build something better. You wanted a system that was more efficient, cheaper, or you wanted a system that had more features, makes it more attractive to your customers," and the Federal Circuit rejected this testimony as insufficient, as a matter of law, to support a finding of obviousness. Citing *ActiveVideo* and similar cases, the Board has found testimony that a proposed modification would provide "increased utility" and could be obtained with "minimal modifications" to be "generic," failing "to provide necessary factual support" for a motivation to combine, and "akin to stating in a conclusory fashion that the combination 'would have been obvious.'" *See, e.g., Samsung Austin*

Semiconductor, LLC v. Red Rock Analytics, LLC, IPR2018-00556, Paper 18, 21 (Aug. 20, 2018). To prove obviousness, a challenger must make “clear how Petitioner relies upon its alleged motivations to combine as support for its contention that the claimed invention would have been obvious,” by “connect[ing] the alleged rationale to combine the prior art with the specific limitations of the claims and claim mapping.” *PayPal, Inc. v. IOENGINE, LLC*, IPR2019-00906, Paper 16, 22 (Oct. 29, 2019).

Petitioner does not substantively address what would motivate a POSITA to “incorporate multiple additional power islands” into Figures 1-5 or Figures 11-17, beyond a rote statement that such a modification would “provide additional functionality (e.g., memory), and to control their individual power consumption.” Pet., 14. Petitioner’s expert merely repeats similar statements. See Ex. 1003 [Min-Dec.] ¶ 108. Aside from generally suggesting that Takahashi’s devices might be improved by increasing their capabilities, Petitioner does not address *why*, in view of Takahashi or any other knowledge of the POSITA, a POSITA would specifically choose to add “additional functionality (e.g. memory)” to embodiments that Takahashi did not already have memory, or why, if Figures 1-5 and 11-17 did not already disclose “a plurality of power islands,” it would be desirable for a POSITA to adopt Takahashi’s Figures 1-5 or 11-17 (which do *not* disclose pluralities of power islands, see Sections II.C.2(a)(i), II.C.2(a)(ii)) as a model to “control ...

individual power consumption” of multiple power islands in a modified circuit. Pet., 14.

Petitioner’s “power savings” rationale for combining alleged teachings of Takahashi’s Figure 10 with Takahashi’s Figure 16, *see, e.g.*, Pet., 13, fares no better. As a threshold matter, while Petitioner states in one place that “[a] POSITA would have found it obvious to include another ‘switching circuit 20’ ... to further reduce power consumption of ‘Wake up logic’ in ‘control circuit 70’ during standby to achieve the same power savings described for Figure 10, as discussed below,” Pet., 13, and in another place that “[a] POSITA would have understood that a device can include more than one ‘logic circuit’ and been motivated to provide a ‘switching circuit’ (i.e., sleep transistor) for each to suppress leakage current and obtain the same power savings described for Figure 10,” Pet., 14-15, Petitioner never discusses what the alleged “same power savings described for Figure 10” actually are—and Petitioner’s expert does not elaborate. *See id.*, 13 (citing Ex. 1003 [Min-Decl.] ¶ 103-104), Ex. 1003 [Min-Decl.] ¶ 103-104(not mentioning any “power savings” relating to Figure 10, even implicitly); *see also* Pet., 15 (citing Ex. 1003 [Min-Decl.] ¶ 108-110), Ex. 1003 [Min-Decl.] ¶ 108-110 (stating, without elaboration or citations, that “[a] POSITA would have understood and been motivated to control power consumption within these additional power islands using the mechanism shown in the embodiments of Figures 1-5, 10, and 11-17 to reduce the overall power

consumption of the device”).

To the extent that such remarks are intended to refer to Takahashi’s statement that elements of its Figure 10 may help to reduce “leakage current,” *see, e.g.*, Pet. 16; *see also* Ex. 1004 [Takahashi] [0090]; *see also id.*, [0085] (discussing “leakage” in connection with Takahashi’s Figure 9), Petitioner does not argue how these alleged benefits of Figure 10 would necessarily be realized in Petitioner’s proposed combination—which modifies Figure 16 in a way that does not employ the scan-pass circuit or “test data S_{in} input” of Takahashi’s Figure 10. *See* Section II.C.2(a)(iii).

Similarly, Petitioner’s proposed rationale for modifying Figure 16 has no clear relation to what Takahashi says about its Figure 10. Takahashi does not disclose that its Figure 10 is generally useful in achieving power savings in integrated circuits. Takahashi states that its Figure 10 is “an example of a circuit capable of performing I_{ddq} measurement,” where the on/off states of transistors 310-380 are set before measurement to allow for “power consumption due to leakage current at each functional circuit” to be “measured” “during standby.” Ex. 1004 [Takahashi] [0087], [0094]. Takahashi does not disclose how an implementation of Figure 10 might consume power when its components are **not** in “standby” status, or how any power savings associated with reduced leakage current would compare with the power **requirements** of any circuitry required provide control of Figure 10 (*e.g.*, via

control over the “test data” input). As already noted, *see* Section II.C.2(a)(iii), Petitioner does not identify any control in Takahashi’s Figure 10. Similarly, Petitioner does not address whether Figure 1 and Figure 16 might save power by **not** having circuitry capable of independently varying power consumptions of the components identified by Petitioner, or otherwise assess the impact on power consumption of its unspecified modifications to the voltage regulators in those figures.

A proper obviousness analysis “concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015). Petitioner’s arguments, which amount to simply asserting that a POSITA would have found it advantageous to satisfy the claims, do not show that the challenged claims are obvious.

3. Petitioner’s Mizuno Grounds Fail (All Claims, Grounds 2A, 2B).

Petitioner’s arguments regarding Mizuno share the same faults as Petitioner’s arguments involving Takahashi. Broadly speaking, Petitioner invites the Board to infer that any component disclosed as capable of being placed in operating or standby states must be a “power island” in any integrated circuit of which it is a part. These arguments fail to engage with any construction of “power island,” *see* Section

II.B, and should be rejected.

- a. *Petitioner Fails To Show That Mizuno Discloses “A Plurality Of Power Islands” (All Claims, Grounds 2A, 2B).*

Mizuno is concerned with aspects of preventing “leakage,” or current flow that occurs when a circuit is not in use. *See, e.g.,* Ex. 1005 [Mizuno] [0009] (describing “[t]he present invention” of Mizuno as “capable of reducing the different types of leakage current ... while [a] circuit block is in standby state”). The Petition purports to identify several “power islands” in Mizuno:

First, Petitioner contends that “‘circuit block CKT,’ depicted in Figures 1 and 22 ... and which may include a ‘logic circuit LG1’ and/or a ‘memory MEM1,’ coupled to a power switch PSW1, comprises a power island,” Pet., 55 (quoting Ex. 1005 [Mizuno] [0053]) (citations omitted), allegedly “because power consumption is controlled within it.” Pet., 56. The Petition elaborates that Mizuno discloses that the “circuit block CKT” of which the Logic circuit LG1 and Memory MEM1 are both a part is capable of being toggled between an “operating state” and a “standby” state, via operation of a “power switch PSW1” which affects the power consumed by “circuit block CKT.” *Id.*, 57.

Second, Petitioner contends that circuit blocks CKT2a and CKT2b of Figures 35-40 are power islands, allegedly because “‘leakage reduction circuits PSM2a and PSM2b,’ which are similar to the leakage reduction circuits in the embodiment of

FIGS. 1-30, control/dynamically change power within the circuit blocks CKT2a and CKT2b, respectively.” Pet., 58 (quoting Ex. 1005 [Mizuno] [0121]).

As with Petitioner’s arguments regarding Takahashi, these arguments fail to demonstrate that Mizuno discloses “a plurality of power islands” in the sense of the ’438 patent. The evidence cited by Petitioner does not speak to either of the constructions proposed by the parties in the co-pending district court litigation, *see* Section II.B, or even address the specification’s statement that “a power island is [a] section ... of an integrated circuit where power consumption is controlled ***within the section***”

i. Petitioner Does Not Show That Mizuno Discloses “A Plurality Of Power Islands” In Its “Figures 1-30.”

The Petition does not even argue that Mizuno’s “first embodiment,” which Petitioner regards as depicted in both of Mizuno’s Figures 1 and 22, *see, e.g.*, Pet. 55 (stating that “Mizuno discloses a ‘first embodiment,’ in Figures 1-30”), discloses “a plurality of power islands,” arguing only that because “power consumption is controlled within” the “circuit block CKT” of Mizuno’s Figure 1 or Figure 22, the “circuit block CKT” of Mizuno’s Figure 1 is a “power island.” Pet., 56. In only identifying one purported “power island” in Mizuno’s Figures 1 and 22, Petitioner here acknowledges that Mizuno’s Figures 1 and 22 do ***not*** disclose a system with “a plurality of power islands.”

Petitioner confirms that Mizuno’s Figures 1 and 22 do not disclose “a plurality of power islands” when it argues that “it would have been obvious to a POSITA to **include** multiple power islands in Mizuno’s ‘first embodiment’ (FIGS. 1-30),” as supposedly taught by another embodiment in Mizuno. Pet., 59.

ii. Petitioner Does Not Show That Mizuno Discloses
“A Plurality Of Power Islands” In Its “Figures 35-40.”

The first “plurality of power islands” argued by Petitioner to be disclosed in Mizuno is the circuit blocks CKT2a and CKT2b of Mizuno’s Figures 35-40,⁹ which are alleged to be power islands because “leakage reduction circuits PSM2a and PSM2b,” which Petitioner says “are similar to the leakage reduction circuits in the embodiment of FIGS. 1-30,” are said to “control/dynamically change power within the circuit blocks CKT2a and CKT2b, respectively.” Pet., 58. The Petition does not elaborate upon **how** power to CKT2a and CKT2b is “controlled” or “dynamically

⁹ Although not all of Mizuno’s Figures 35-40 depict both the “CKT2a” and “CKT2b” of Mizuno’s Figure 35, the Petition treats these figures as though they describe a single embodiment, *see, e.g.*, Pet., 58 (referring to “the embodiment of FIGS. 35-40”), which Patent Owner will assume for purposes of preliminary response.

changed” by the leakage reduction circuits PSM2a and PSM2b; the Petition only says that this occurs, and concludes from this assertion that CKT2a and CKT2b are each power islands.

The Petition does not, for example, offer further explanation of how power consumption of, *e.g.*, CKT2a is specifically “controlled within” CKT2a by leakage reduction circuit PSM2a (Ex. 1001 [’438] 3:62-65), let alone demonstrate that power consumption within CKT2a is controllable by ***independently varying*** the operating voltage of CKT2a and/or the frequency of operation of CKT2a, as either of the parties’ proposed constructions in the district court would require. *See* Section II.B.

Petitioner’s implicit argument may be that a disclosure of separately labeled “leakage reduction circuits” amounts to a teaching of the independent control of these “leakage reduction circuits,” or perhaps more broadly that a disclosure of distinct switches to these circuits renders some mechanism of independent control of power consumption within those circuits obvious. *See generally* Pet., 57-58. But this is not an argument that Petitioner bothers to make; instead, Petitioner’s argument is one of inherency.

To establish inherency, Petitioner must demonstrate that the requisite control (and thus a “plurality of power islands”) is “necessarily present, not merely probably or possibly present, in the prior art.” *Trintec Indus., Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 1295 (Fed. Cir. 2002) (cleaned up); *see also* *PAR Pharm., Inc. v. TWi*

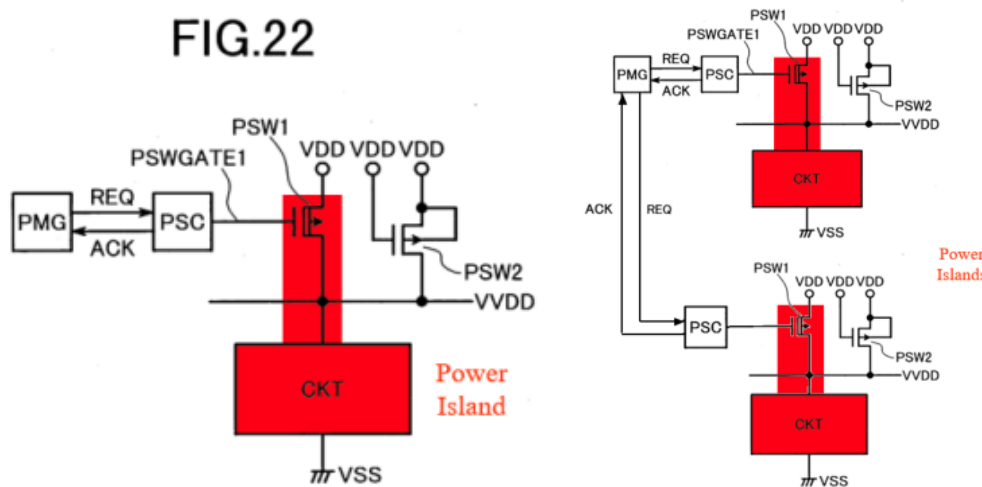
Pharms., Inc., 773 F.3d 1186, 1195–96 (Fed. Cir. 2014) (“A party must [] meet a high standard in order to rely on inherency to establish the existence of a claim limitation in the prior art in an obviousness analysis—the limitation at issue necessarily must be present, or the natural result of the combination of elements explicitly disclosed by the prior art.”); *Southwire Co. v. Cerro Wire LLC*, 870 F.3d 1306, 1310–11 (Fed. Cir. 2017) (similar). Petitioner, who does even attempt to address the relevant standard, does not satisfy this high burden.

b. *Petitioner’s Arguments That Mizuno Renders Obvious
“A Plurality Of Power Islands” Are Conclusory (All
Claims, Grounds 2A, 2B).*

Separately from arguing that Mizuno discloses “a plurality of power islands,” the Petition states in the alternative that Mizuno renders this limitation obvious. In each case, however, the support offered for this alternative assertion is conclusory.

Petitioner argues that “it would have been obvious to a POSITA to include multiple power islands in Mizuno’s ‘first embodiment’ (FIGS. 1-30),” as allegedly depicted in a proposed modification of Mizuno’s Figure 22. Pet., 59. Mizuno’s Figure 22 and Petitioner’s proposed modification are depicted side by side below.

FIG.22



Pet. 56 (Mizuno’s Figure 22, as annotated by Petitioner); Pet. 59 (Mizuno’s Figure 22, as modified and annotated by Petitioner). Quoting Mizuno, Petitioner states that “[b]y establishing multiple leakage control circuits as in FIG. 35, and controlling the leakage current of circuits grouped in multiple circuits integrated onto the chip, the leakage current of the overall chip can be efficiently reduced.” Pet., 60 (quoting Ex. 1005 [Mizuno] [0122]).

Petitioner’s remark does not elaborate upon *how* “the integrated circuit of Figures 1-30” would be modified so that power consumption was “individually controlled” within these multiple circuit blocks, let alone how such a modification of the “first embodiment”—which, to be clear, Petitioner’s expert has characterized only in terms of claim limitations that such a modification would render obvious—would subsequently satisfy or render obvious the remaining limitations of the challenged claims. After modifying Mizuno’s Figure 22 for purposes of locating “a

plurality of power islands” in the resulting system, for example, Petitioner’s analysis never discusses how power consumption would be managed in this modified system (let alone managed by a system that satisfies the rest of any challenged claim). As a single example, separately from reciting a “plurality of power islands,” independent claim 1 recites a “power island manager” configured to “dynamically change the power consumptions” of the plurality of power islands—yet Petitioner does not identify a single “power island manager” configured to dynamically change the power consumptions alleged to exist in its modified Figure 22.

If Petitioner’s expert is implicitly appealing to common sense—that is, to a vague notion that wherever a reference discloses a single circuit block in a specific context, a POSITA would understand a teaching of a similar circuit that operates “individually controlled” copies of that circuit block—the Petition does not even attempt to address the relevant standard. *See Arendi S.A.R.L. v. Apple, Inc.*, 832 F.3d 1355, 1362–63 (Fed. Cir. 2016) (when there is a “missing limitation” an obviousness argument, the inquiry into “a reasoned basis for resort to common sense must be searching”); *DSS Tech. Mgmt. v. Apple Inc.*, 885 F.3d 1367, 1374 (Fed. Cir. 2018) (“common sense” can be used to supply a missing limitation “**only** when ‘the limitation in question [is] unusually simple and the technology particularly straightforward.’”). Petitioner does not, for example, even argue (let alone identify evidence) that the individual control at issue in managing a plurality of “power

islands” in the sense of the challenged claims is “unusually simple” or “particularly straightforward.”

Petitioner’s obviousness analysis of “power islands” as allegedly taught by Mizuno’s Figure 35 embodiment is similarly conclusory. Although the Petition states that a POSITA “would have understood **and found obvious** that Mizuno’s integrated circuit [in Figure 35] includes multiple power islands,” Pet., 58, the Petition does not contain any argument or evidence specific to obviousness—*i.e.*, why the Figure 35 embodiment, Mizuno’s discussion of this embodiment, or any knowledge of the POSITA would render obvious a “plurality of power islands” in some modification of Mizuno’s Figure 35, if Mizuno’s Figure 35 did not already literally disclose this limitation (which it does not, *see* Section II.C.3(a)).

4. Petitioner’s Multiple-Reference Grounds Incorporate The Flaws Of Petitioner’s Single-Reference Grounds (Grounds 1B, 1C, 2B, Claims 7, 9, 15, 19).

Petitioner’s multiple-reference obviousness grounds, which are largely directed to dependent claims, incorporate Petitioner’s single-reference obviousness arguments as to independent claims—particularly independent claim 1—without supplementation. In particular, these grounds do not offer any additional evidence or argument that Takahashi or Mizuno teach “a plurality of power islands” in the sense of the ’438 patent, and do not explain how the grounds would otherwise nevertheless teach “a plurality of power islands” in Petitioner’s proposed

combinations. For this reason, the Board does not need to address these grounds in its institution decision.

Petitioner's Ground 1B, for example, challenges claims 7 and 19, which depend from independent claims 1 and 15, respectively, and which additionally recite "wherein [a] variable voltage is an optimum voltage" and "wherein the optimum voltage is dependent upon both process variation and temperature variation," as supposedly obvious in view of Takahashi and a secondary reference Schutz. After a brief discussion of Schutz, Pet., 38-39, the Petition includes a section in which Petitioner argues that a POSITA would have been motivated to combine Takahashi and Schutz, Pet., 39-44, and proposes that "[s]pecifically, a POSITA would have been motivated to employ Schutz's 'IC temperature sensor' to optimize 'source voltages' from 'voltage regulator 100' based on both process variation and temperature variation." Pet., 43. Neither this discussion nor Petitioner's subsequent analysis (Petitioner's entire challenge to claim 19 is three words "supra claim 7," Pet., 45) make any argument relating any alleged teachings of Schutz to "power islands" in any system, or revisit the question of why Takahashi teaches "a plurality of power islands."

Petitioner's Ground 1B thus appears to take for granted the central premise of Petitioner's Ground 1A—the obviousness of claim 1 in view of Takahashi alone. Petitioner's Ground 1B therefore fails for at least the reasons identified above in

connection with Ground 1A.

It is the same with Petitioner's Ground 1C, which argues that claims 9 and 15 are obvious in view of a combination of Takahashi and the secondary reference Notani. Claim 9 depends from claim 1 and additionally recites (among other things, and including via dependence on claim 8) an "optimum voltage," wherein the optimum voltage "is generated by a sleep generator within the power island manager," and "wherein the sleep generator comprises a charge pump." Claim 15 is an independent claim that recites (again, among other things) "a sleep generator including a charge pump." After a two-paragraph overview of Notani, Pet., 45-47, Petitioner's Ground 1C analysis includes a section in which Petitioner argues that a POSITA would have been motivated to combine Takahashi and Notani, Pet., 47-50, and proposes that a POSITA would have been "led . . . to employ Notani's charge pump within Takahashi's 'voltage regulator'" Pet., 48. This discussion repeatedly refers back to Petitioner's analysis in Ground 1A of obviousness in view of Takahashi alone. *See, e.g.*, Pet., 48-49; *see also* Pet. 48 n.9. Petitioner's analysis of claim 9 does not include any analysis of limitations already present in claim 1, and Petitioner's analysis of claim 15 is the single sentence "Supra Claim 9; Ground 1A, Claims 1, 8, 12." Pet., 51. In particular, Petitioner's Ground 1C does not (for example) identify "power islands" in Notani, or make argument relating any alleged teachings of Notani to "power islands" in any system. Like Petitioner's Ground 1B,

Petitioner's Ground 1C thus fails to address—let alone cure—the defects of Petitioner's Ground 1A, and fails for at least the reasons identified in connection with Ground 1A.

It is the same with the Petition's Ground 2B, which argues that claims 9 and 15 are obvious in view of Mizuno and Notani. Petitioner's arguments regarding Mizuno and Notani do not expressly address limitations already present in claim 1—except by reference to the single-reference obviousness Ground 2A. *See, e.g.,* Pet., 87, 87 n.16, 89. Thus again, for at least the same reasons that Petitioner's Ground 2A fails, so must Petitioner's Ground 2B.

III. CONCLUSION

For each of the foregoing reasons, the Board should not institute trial.

Respectfully submitted,

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Dated: July 11, 2024

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), counsel for Patent Owner certifies that this document complies with the type-volume limitation of 37 C.F.R. § 42.24(b). According to Microsoft Office Word's word count, this document contains approximately 13,905 words, including any statement of material facts to be admitted or denied in support, and excluding the table of contents, table of authorities, mandatory notices under § 42.8, exhibit list, certificate of service or word count, or appendix of exhibits or claim listing.

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that, pursuant to 37 C.F.R. § 42.6(e) and with the agreement of counsel for Petitioner, true and correct copies of the following documents were served by electronic service on the date below:

PATENT OWNER'S PRELIMINARY RESPONSE

EXHIBITS 2004-2006

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