

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MEDIATEK, INC.,
Petitioner,

v.

MOSAID TECHNOLOGIES INC,
Patent Owner.

Case IPR2024-00721
Patent 9,350,349

PATENT OWNER'S PRELIMINARY RESPONSE

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2005	U.S. Patent No. 7,051,306 ['306]
2006	U.S. Patent No. 8,854,077 ['077]

I. INTRODUCTION

The Petition should be denied because Petitioner fails to demonstrate that it would prevail as to at least one challenged claim. Critically, Petitioner does not address a key interpretive issue at the core of its challenge. The '349 patent is directed towards, and all of the challenged claims recite, systems or methods involving a “plurality of power islands,” *i.e.*, more than one power island. Petitioner’s grounds are based on Takahashi and Mizuno, but Petitioner fails to explain how a “plurality of power islands” is obvious based on either one of them. Nor does Petitioner acknowledge how Takahashi or Mizuno might fail to disclose a “plurality of power islands,” preventing Petitioner from being able to provide anything approaching a bona fide obviousness analysis. Rather, Petitioner offers conclusory statements that the limitation is taught in the art. But obviousness may not be shown through conclusory statements.

Further undermining Petitioner’s position is its unexplained inconsistency concerning the meaning of the term “power island.” While taking the position that “power island” requires no construction in this proceeding, Petitioner expressly acknowledges that interpretation of “power island” might affect the analysis—by constantly pairing what are essentially anticipation arguments with perfunctory statements of obviousness. Because Petitioner does not identify any construction(s) of “power island” that it is applying to the cited art, the distinction (if any) between

these arguments is unclear. Meanwhile, in co-pending district court litigation, Petitioner is proposing a construction that Takahashi and Mizuno do not satisfy. Petitioner does not even analyze Takahashi or Mizuno under that construction in this proceeding; Petitioner simply says, in single sentences, that these references’ “disclosures, in light of a POSITA’s knowledge, also render this term obvious” under that construction. *See* Pet., 16-17 (Takahashi), *see also id.*, 61-62 (Mizuno).

To be clear, none of this is about disputed facts or about the interpretation of evidence cited by the Petitioner. It is about the Petition making statements about “power islands” that do not address relevant aspects of the intrinsic record, or the construction of “power island” proposed by Petitioner in the parallel litigation, and are not supported by more than attorney fiat. The Petition should be denied.

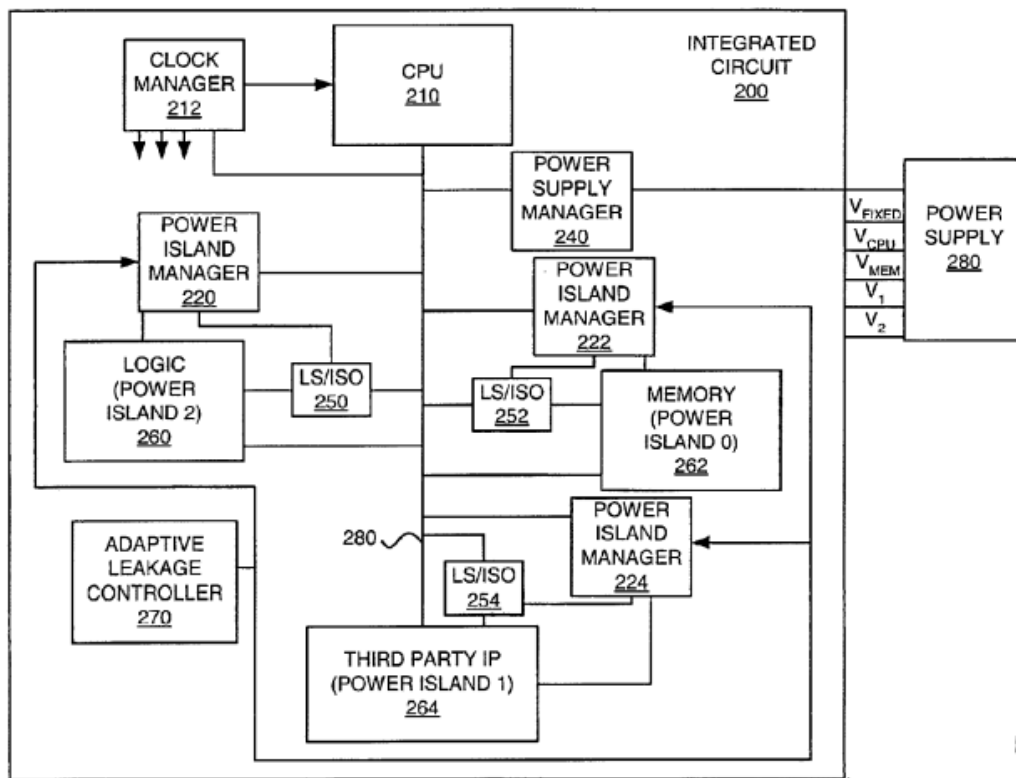
II. PETITIONER’S GROUNDS FAIL.

A. “Power Islands” In The ’349 Patent.

The ’349 specification describes systems for reducing power consumption in integrated circuits while maintaining performance. Crucial to the systems claimed in the ’349 patent is the idea of “power islands,” or delineations of an integrated circuit into subdivisions “where power consumption is controlled within” the subdivisions. Ex. 1001 [’349] 4:8-11.

The ’349 patent correspondingly describes exemplary designs where such islands include “logic,” “memory,” and “third party intellectual property (IP).” Ex.

1001 ['349] 4:1-7. These islands are separately controlled by “power island managers” and adjusted “dynamically ... based on the needs and operation of the integrated circuit” of which they are a part by “select[ing] a clock, chang[ing] clock frequency, or modify[ing] the voltage within the power island to control the power consumption of the power island.” *Id.*, 4:25-31. An exemplary configuration of such a design is depicted in the '349 patent's Figure 2:



Id., Fig. 2. Here, “power island managers” 220, 222, and 224 of Figure 2 are configured to separately manage power consumption within their respective power islands 260 (“logic (power island 2)”), 262 (“memory (power island 0)”), and 264 (“third party intellectual property (IP) (power island 1)”). See, e.g., *id.*, 4:1-17.

In some instances, the '349 patent's specification discusses power management involving the use of "control signals" provided by an "adaptive leakage controller." *See, e.g.*, Ex. 1001 ['349] FIG. 2 (*see* "Adaptive Leakage Controller 270"), *see also id.*, 4:22-31. All claims of the '349 patent correspondingly recite systems or methods involving not only a "plurality of power islands" but, *inter alia*, an "adaptive leakage controller" and a "control signal." *Id.*, cls. 1-16.

The crucial point for present purposes is that "power islands" are not merely delineations of an integrated circuit, but delineation with separately controllable power. If one considers only if there exist functionally divided blocks of circuits, one may very well have "islands." But what makes a "**power** island" is the adjective "power"—an island must be configured so as to have power control independent of other components as discussed in detail below. Thus, when judging the prior art's disclosures, the adjective "power" in "power island" means that merely having functional blocks of circuitry is not enough—the question is whether and how those blocks have independent power control.

This point is where the Petition falls apart in addressing the prior art. Petitioner can perhaps credibly argue that Takahashi or Mizuno disclose various distinct functional blocks of circuitry, but not that these blocks are shown to have separately controllable power. Petitioner invites the Board to ignore the crucial point of a "power island"—that it is a **power** island and not merely a functional island.

Petitioner is thus not engaging with the actual claim terms at all, instead focusing upon hypothetical claims where “power” is struck out from the phrase “power island” everywhere it appears. This is basic error. The references leave Petitioner no choice, of course, as neither Takahashi nor Mizuno disclose or suggest “power islands.” But a Petitioner’s plight is no substitution for applying the legal requirements of validity analysis.

In refusing to analyze the purported “power islands” of these references under any claim construction, *see* Section II.B, and in refusing to acknowledge where or how the references might not disclose “a plurality of power islands,” Sections II.C.2 and II.D.2, Petitioner’s analysis presents something of a moving target. Details of how the variously cited teachings of Takahashi and Mizuno nevertheless fail to render the challenged claims obvious are addressed in Sections II.C and II.D. Petitioner has not shown cited references do not teach or render obvious any system or method in “a plurality of power islands.”

B. Petitioner Fails To Demonstrate That Any Of Its Grounds Disclose Or Render Obvious “A Plurality Of Power Islands” (All Claims, All Grounds).

Each of the challenged claims recites “a plurality of power islands.” While the ’349 patent has not yet been subject to claim construction, several of the same terms in the claims of the ’349 patent were subject to claim construction for the ’306 patent, which is incorporated by reference in the ’349 patent, Ex. 1001 [’349] 4:17-

21. One of these terms, “power island,” requires construction and, indeed, has already been construed by two different district courts in litigations involving Freescale and Xilinx. *See generally* Ex. 1032 [Freescale-Order] 44; Ex. 1033 [Xilinx-Order] 29. The constructions are as follows:

<i>Freescale</i> District Court Construction	<i>Xilinx</i> District Court Construction
a section of an integrated circuit where power consumption is controlled by independently varying its operating voltage and its frequency of operation Ex. 1032, 44; Ex. 2004 [JCCS] 3	a section of an integrated circuit where power consumption is controlled by independently varying its operating voltage or its frequency of operation (or both) Ex. 1033, 29; Ex. 2004 [JCCS] 3

What is more, in the co-pending district court litigation between Patent Owner and Petitioner, the parties have proposed that there is a need for construction of the term “power island,” and that the proper construction is one of those previously decided by district courts. There, Patent Owner has proposed the *Freescale* construction, and Petitioner has proposed the *Xilinx* construction.¹ Ex. 2004

¹ The two prior district court constructions have one difference. The *Freescale* district court construction (Ex. 1032, 44) requires power consumption to be controlled by “independently varying” both “its operating voltage **and** its

[JCCS] 3.

To provide context for these proposals, the '349 specification states that “[a] power island is any section, delineation, partition, or division of an integrated circuit where power consumption is controlled within the section, delineation, partition, or division.” Ex. 1001 ['349] 4:8-11. The '349 specification includes additional disclosures of how power consumption is “controlled within” a power island, *see id.*, 4:28-31 (power controlled “within [a] power island” by “select[ing] a clock, chang[ing] clock frequency, or modify[ing] the voltage within the power island to control the power consumption of the power island.”), and the parties’ dispute could be regarded as centering on over which of the above interpretations—in view of not just these disclosures, but the rest of the intrinsic record²—is a more appropriate

frequency of operation.” The *Xilinx* district court construction (Ex. 1033, 29) is broader and requires that power consumption be controlled by “independently varying” either “its operating voltage **or** its frequency of operation (or both).”

² In the co-pending district court litigation, both parties have identified this and other disclosures as relevant to the construction of “power island” in the '349 patent. *See* Ex. 2004 [JCCS], Ex. A, 2 (PDF page 8) (Patent Owner citing, *inter alia*, Ex. 1001 ['349] 3:59-4:32) & Ex. B, 2 (PDF page 11) (Petitioner citing, *inter*

interpretation of what it means for power consumption to be “controlled within” a section of an integrated circuit.

But while the parties disagree about *which* district court construction to use, they agree that a “power island” in the sense of the ’349 patent is a section of an integrated circuit where power consumption is controlled by “independently varying” one or more power characteristics, including at least one of an “operating voltage” or a “frequency of operation.” In short, all parties agree that “power island” is indeed a “**power**” island—a section (or delineation) with independently controllable power.

Petitioner here contends, however, that “power island” requires no construction. Pet., 5-6 (“For purposes of this proceeding only, Petitioner submits that no claim terms require a formal construction for addressing the Grounds in this Petition.”) Petitioner does not explain why “power island” does not “require” construction here, but it is apparent. Petitioner’s hopes turn upon ignoring the failure

alia, Ex. 2006 [U.S. Patent No. 8,854,077] 3:65-4:20). The ’349 patent is a continuation of U.S. Patent No. 8,854,077, *see* Ex. 1001 [’349] Cover Page, and the disclosure cited by Petitioner in the ’077 patent is identical to Ex. 1001 [’349] at 4:8-31.

of the prior art to disclose multiple “power islands”—power-controllable sections of integrated circuits. What better way to avoid confronting this failure than to conceal it by avoiding any engagement with the claim term?

Admittedly, Petitioner does not conceal the existence of the *Xilinx* and *Freescale* constructions. But Petitioner seeks to avoid discussing them in substance, stating that the term “power island” has been “construed in prior litigations involving ***a patent describing similar subject matter.***” Pet., 15. Petitioner neglects to mention that this patent, U.S. Patent No. 7,051,306, “the ’306 patent,” is far more than just a patent “describing similar subject matter.” The ’349 patent expressly incorporates the ’306 patent by reference when introducing “power islands.” Ex. 1001 [’349] 4:17-21. The ’349 patent directly copies various descriptions of “power islands” from the ’306 patent. *Compare* Ex. 1001 [’349] 4:8-16 *with* Ex. 2005 [’306] 3:51-59.³ Given this relationship, it is no surprise that in the co-pending litigation, the parties agree that “power island” means the same thing in both the ’349 patent and the ’306 patent. Ex. 2004 [JCCS] 3. Petitioner’s characterization of the ’306 patent

³ Petitioner is familiar with the ’306 patent. Like the ’349 patent, it is presently at issue in the parallel litigation, *see, e.g.*, Ex. 2004 [JCCS] 1, and the subject of co-pending IPR proceedings. *See* IPR2024-00598 (challenging the ’306 patent).

as merely “a patent describing similar subject matter” in this proceeding is a gross understatement, and an obvious attempt to minimize the importance of the concept of “power island.”

Again, Petitioner has little choice because Petitioner cannot—and does not even attempt to—argue that the cited art teaches “a plurality of power islands” by comparing the art to either party’s (or either district court’s) construction. Petitioner instead pays only the most conclusory possible lip service. Petitioner states, for example, that “Takahashi’s disclosures, in light of a POSITA’s knowledge, also render this term obvious under the prior constructions.” Pet., 16. Petitioner’s expert does not elaborate upon “Takahashi’s disclosures,” or “the prior constructions,” or any alleged significance of one to the other, but simply repeats this assertion. Ex. 1003 [Min-Decl.] ¶ 101, n.1. Petitioner’s “analysis” of the Mizuno reference in terms of the district court construction (and Petitioner’s expert’s “analysis”) does not even make a conclusory statement about Mizuno’s disclosures, stating only that “Petitioner submits that no construction is necessary for the reasons discussed above for Ground 1A,” Pet., 66—that is, for the reasons discussed in connection with Takahashi alone—while in the declaration cited by Petitioner, *id.* (citing Ex. 1003 [Min-Decl.] ¶ 281 n.9), Petitioner’s expert states that “***Takahashi’s*** disclosures, in light of a POSITA’s knowledge, also render this term obvious under the prior constructions,” Ex. 1003 [Min-Decl.] ¶ 281 n.9, where presumably “Mizuno’s

disclosures” was intended.

Such conclusory statements are entitled to little weight. *See, e.g.*, 37 C.F.R. § 42.65(a); *see also Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9, 15-17 (August 24, 2022) (precedential) (denying institution when expert declaration “adds little to the conclusory assertion for which it is offered to support”). Fundamentally, obviousness may not be proven by Petitioner’s and its expert’s conclusory statements. *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.”). Nor would any of the alleged “power islands” identified by Petitioner qualify under either construction, as explained below. *See* Sections II.C (Takahashi), II.D (Mizuno).

This is more than sufficient reason to deny institution. “Power island” is a term that both parties agree requires construction and, indeed, has been previously construed by two different district courts in mostly similar terms. Both parties, moreover, advance one of these constructions in district court and, aside from the distinction identified above, both parties agree on the balance of the construction. Petitioner, however, does not make any real attempt to argue that either of these constructions is satisfied under any of its grounds nor does it make any real attempt to argue why “power island,” only in this IPR, does not require construction.

Petitioner had the burden to construe the claim and demonstrate that the construed claims are satisfied. *See* 37 C.F.R. §§ 42.104(b)(3)-(4) . Its failure to carry that burden is sufficient reason to deny institution. In *Orthopediatrics Corp. v. K2M, Inc.*, IPR2018-01546, Paper 10 (Feb. 14, 2019), for instance, the Board denied institution where the petitioner took contradictory claim constructions between the IPR and the district court and the district court had accepted petitioner's construction. *Id.*, 11-12. As the Board explained:

Because of the unique circumstances of this proceeding, where Petitioner advocated for a different claim construction in the related district court litigation, we determine that construction of the claim term in dispute is necessary for the resolution of issues before us. Lacking such claim construction, the Petition fails to comply with 37 C.F.R. § 42.104(b)(3).

... Keeping in mind that Petitioner has the burden to show a reasonable likelihood of prevailing in showing that at least one claim is unpatentable, it is incumbent upon Petitioner to address substantively the District Court's claim construction of a limitation when construction of that limitation is likely to be a focal point of the inter partes review proceeding. By failing to reconcile its proffered claim construction here with its very different construction proffered in District Court—which the District Court agreed with—Petitioner fails to satisfy this burden.

Id.; *see also* *10x Genomics, Inc. v. President and Fellows of Harvard College*,

IPR2023-01299, Paper 15, 13 (Mar. 7, 2024) (“Because Petitioner has the burden to show a reasonable likelihood of prevailing in its assertion that at least one claim is unpatentable, our rules require that Petitioner substantively address any claim terms in dispute. ... Thus, we find the Petition is deficient on its face under 37 C.F.R. § 42.104(b)(3), as merely stating ‘no construction [is] necessary’—while knowing the construction is actually disputed under § 112(f)—is not sufficient for purposes of institution.”).

Consequently, where “power islands” has been construed by two different district courts and the parties agree the term requires construction (each advocating for one of those constructions), it was incumbent upon Petitioner to say more than that “[f]or purposes of this proceeding only, Petitioner submits that no claim terms require a formal construction for purposes of addressing the Grounds in this Petition.” Pet., 5-6.

This is particularly so given that the district court and the Board apply precisely the same claim construction standard. Notably, the Office made clear, in the preamble of the rulemaking associated with the switch from a “broadest reasonable interpretation” standard to a *Phillips*-style claim construction standard, the Office’s official “agree[ment] with “[s]everal comments [which] acknowledged that harmonizing the claim construction standards **would prevent parties from taking inconsistent positions** ...” *Changes to the Claim Construction Standard for*

Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340, 51350 (Oct. 11, 2018); *id.* (““With a uniform application of the *Phillips* standard, patent challengers ... ***will instead be required to choose a single claim construction that best captures the true meaning of the patent claim* ...””).**

At the very least, Petitioner needed to explain why a twice construed, currently disputed term required “no formal construction.” Under these circumstances, Petitioner has failed to comply with 37 C.F.R. §§ 42.104(b)(3)-(4) and that failure should prove sufficient to deny institution.

C. Petitioner’s Takahashi Grounds Fail (All Claims, Grounds 1A, 1B, 1C).

One of Petitioner’s two primary references is Takahashi, a published patent application. Petitioner argues that various embodiments of Takahashi disclose “a plurality of power islands,” but never addresses the gaps between the disclosures of Takahashi and “power islands” in the sense of the ’349 patent. Instead, Petitioner points to structures that Takahashi expressly discloses are ***not*** “power islands,” then additionally proposes a vague combination of distinct systems in Takahashi, in which the details of how power is controlled are simply left to the Board’s imagination. Petitioner does not show that the cited material teaches a “a plurality of power islands.”

1. Petitioner Fails To Show That Takahashi Discloses Or Renders Obvious “A Plurality Of Power Islands” (All Claims, Grounds 1A, 1B, 1C).

Each of the challenged claims, again, recites a system comprising a “plurality of power islands,” *i.e.*, more than one “power island.” The Petition correspondingly attempts to identify several purported “power islands” in Takahashi. Takahashi itself, however, never mentions “power islands,” and Petitioner fails to demonstrate that anything that it identifies in Takahashi discloses or teaches a “plurality of power islands”—whether within any structure actually disclosed in Takahashi, or in Petitioner’s vaguely proposed combination of structures in Takahashi.

Takahashi discusses “semiconductor integrated circuit[s] wherein the circuit area can be minimized, and defects can be detected reliably during a standby status while maintaining the reliability of a gate oxide film.” Ex. 1004 [Takahashi] (Abstract).

Takahashi describes its systems as consuming power in one of two states: an “operation” state (sometimes also referred to as an “active” state), and a “standby” state (sometimes also referred to as a “sleep” state). *See, e.g., id.*, Abstract (referring to a circuit in “an operating status” and “a standby status”), [0017] (paragraph beginning “Summary of invention” describing “the present invention” as having a “voltage supply circuit” that “supplies ... [a] first source voltage while the aforementioned functional circuit is in a standby status, and ... [a] second source

voltage while the aforementioned functional circuit is operating.”), [0029]-[0030] (describing Figures 4 and 5 as depicting an embodiment “during operation” and “during standby,” respectively), Figs. 4-5, [0031]-[0032] (describing Figures 6 and 7 similarly for another embodiment), [0033]-[0034] (describing Figures 8 and 9 similarly for another embodiment), Figs. 8-9, [0041]-[0042] (describing Figures 16 and 17 as “showing the source voltages generated by the voltage regulator . . . during operation” and “during standby,” respectively), [0110] (describing Figures 14 and 15 as respectively depicting “voltage levels of source voltages” “during” “operation (Active mode)” and “standby (Sleep mode)”)), Figs. 14-15.

Petitioner’s own reading of Takahashi confirms that the systems described in Takahashi consume power in two states, “operating” and “standby.” *See, e.g.*, Pet., 7 (describing Takahashi’s Figure 1 via a disclosure in which a “switching circuit . . . supplies an operating current” to a component “during operation” and “suppresses [] leakage current” “during standby”) (quoting Ex. 1004 [Takahashi] [0052]); *see also id.* (quoting Takahashi to the effect that “[D]ifferent levels [of a source voltage] are applied during operation and during standby, respectively”) (quoting Ex. 1004 [Takahashi] [0053]).

In some embodiments of Takahashi, the voltages supplied to components during “operation” and “sleep” states are set by fuses after an assessment of the condition of the transistors that were used to fabricate the device. *See, e.g.*, Ex. 1004

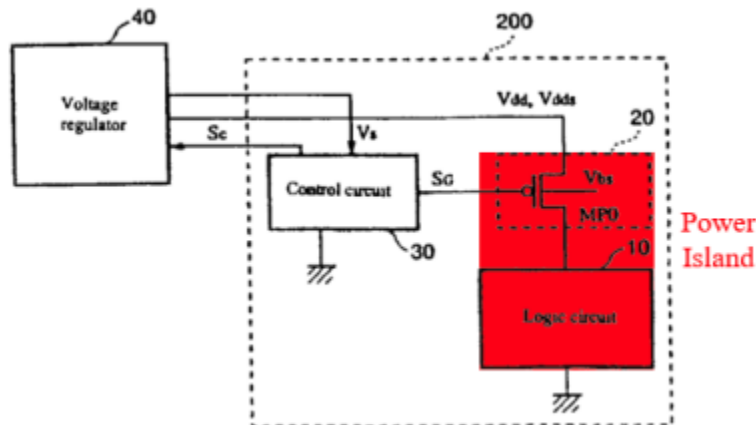
[Takahashi] [0098]-[0099], [0109] (“After the production process for device 200 is completed, it is measured using a test circuit in order to extrapolate the driving capabilities of the pMOS transistor and the NMOS transistor constituting device 200 according to the result of the measurement, so that the condition of device 200 ... can be determined. ... [F]using circuit 202 can be programmed to set the respective fuses to desired conditions according to the condition of device 200”). But within such embodiments—however any fuses have been set—each component is supplied with one fixed voltage during the “operation” state of the device, and one fixed voltage during the “standby” state of the device. *Id.*, [0109] (“control data DAT in accordance with the condition of device 200 are output by fusing circuit 202”), [0111] (“Voltage regulator 100 generates different levels of source voltages during operation and during standby according to said control data DAT ...”), [0110] (describing Figures 14 and 15 as “show[ing] the voltage levels of source voltages ... generated by voltage regulator 100 according ... control data DAT set based on the process requirements of device 200 during operation (Active mode) and during standby (Sleep mode)”). Again, this aspect of Takahashi is confirmed by Petitioner’s own reading of Takahashi. *See, e.g.,* Pet., 8 (stating that “The control data DAT [in Takahashi’s Figures 11-17] is ‘based on the process requirements of device 200 during operation (Active mode) and during standby (Sleep mode),’” but that “[t]he operation of ‘device 200’ in the embodiment of Figures 11-17 otherwise

remains the same as in the embodiment of Figures 1-5”) (quoting Ex. 1004 [Takahashi] [0110]).

In addition to describing “devices” whose components can be placed in an “operation” or “standby” state, Takahashi’s Figure 10 separately discloses aspects of the design of a “measuring circuit.” *See, e.g.*, Ex. 1004 [Takahashi] [0087] (“FIG. 10 shows an example of a circuit capable of performing I_{ddq} measurement”), Fig. 10. Takahashi states that its measuring circuit can be used to detect “manufacturing defects.” *See, e.g., id.*, [0015] (stating that in the prior art, “is no effective I_{ddq} testing method for detecting manufacturing defects for the aforementioned technologies”), [0095] (stating that with a design as in Figure 10 could be used in “ I_{ddq} of a specific functional circuit can be measured by designing” its inputs “appropriately”).

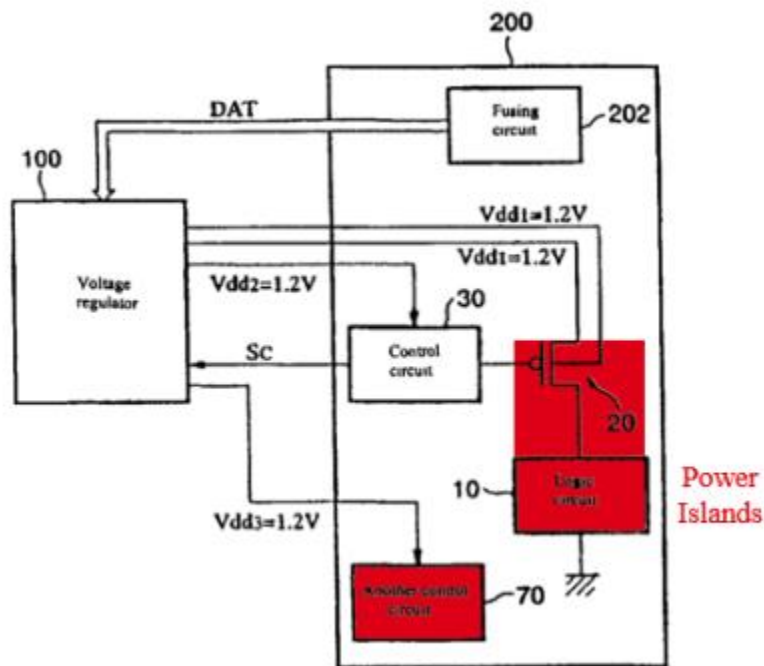
Petitioner finds alleged “power islands” in three separate embodiments in Takahashi, depicted in its Figures 1, 16 and 10 (discussed by Petitioner in that order).

Petitioner first contends that a POSITA “would have understood and found obvious” that a “logic circuit 10” in Takahashi’s Figure 1 is a power island, providing the following annotation:



Pet., 11. Petitioner contends that “power consumption within the ‘logic circuit 10’ is controlled ... by the ‘switching circuit 20’ ... that ‘supplies an operating current to logic circuit 10 during operation and suppresses the leakage current of the ... logic circuit 10 during standby.’” *Id.* (quoting Ex. 1004 [Takahashi] [0052]). This statement is accompanied by a citation to an expert declaration which states that “when the ‘switching circuit 20’ is on, the ‘logic circuit 10’ receives a voltage V_{dd} to place the ‘logic circuit 10’ into operational mode, and when off, the ‘logic circuit 10’ receives a lower voltage that places the ‘logic circuit 10’ into a low-power standby state.” Ex. 1003 [Min-Decl.] ¶ 103.

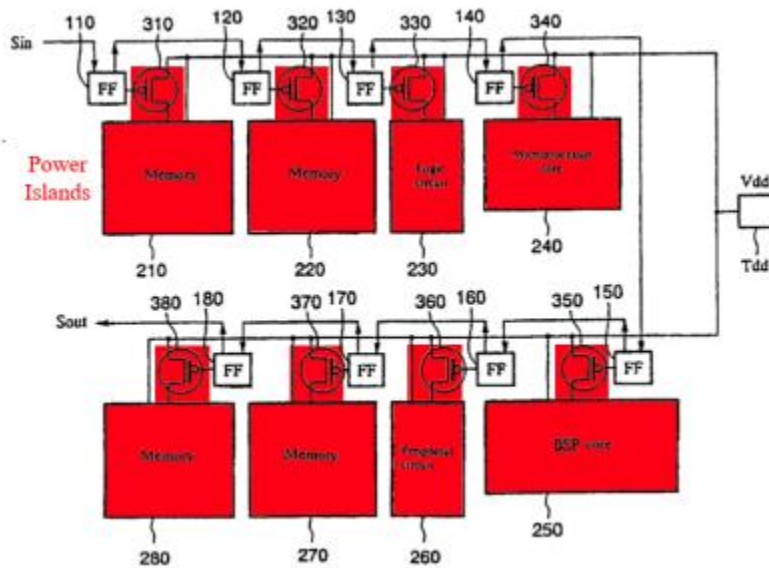
Petitioner then contends that “another control circuit 70” in Takahashi’s Figure 16 is part of a power island, providing the following annotated version of that figure:



Pet., 12-13. Petitioner argues that “power consumption within ‘control circuit 70’ is controlled ... by ‘source voltage V_{dd3} ’ that varies based on whether it is in an operational or standby state.” *Id.*, 12 (citing Ex. 1004 [Takahashi] [0110]-[0116] & FIGS. 14-17). This statement is accompanied by a citation to an expert declaration which states that in Takahashi’s Figure 16, “‘source voltage V_{dd3} ’ varies between 1.2V and 0.7V based on whether the ‘Wake up logic’ is in an operational or standby state.” Ex. 1003 [Min-Decl.] ¶ 105.

Petitioner then contends that a “POSITA also would have found it obvious for Takahashi’s integrated circuit, such as the ones depicted in Figures 1-5 and 11-17, to include multiple additional power islands.” Pet., 13. The alleged source of inspiration for these “additional power islands” is Takahashi’s measuring circuit

Figure 10—each of whose circuits 210-280 “along with their respective ‘pMOS transistors 310, 320, ... , and 380’ (i.e., switching circuits / sleep transistors)” is alleged by Petitioner to “comprise[] a power island” because “they are sections of the integrated circuit where power consumption is controlled within the section”—a recitation that simply echoes language from the ’349 patent. *Id.*; see also Ex. 1001 [’349] 4:8-12. Aside from making this recitation, Petitioner does not specify how the power consumptions of the circuits 210-280 are allegedly controlled, and thus fails to show any plurality of “power islands” in Figure 10. In material not cited by Petitioner, *but see* 37 C.F.R. § 42.6(a)(3) (prohibiting incorporation by reference of arguments from one document into another). Petitioner’s expert states that each circuit 210-280 along with its respective pMOS transistor 310-380 is a “power island” because “power consumption within each of the functional circuits 210-280 in Figure 10 is controlled by the ‘switching circuit ... with pMOS transistors 310, 320, ... , and 380’” in the circuits 210-280. Ex. 1003 [Min-Decl.] ¶ 108 (citing Ex. 1004 [Takahashi] [0090]).



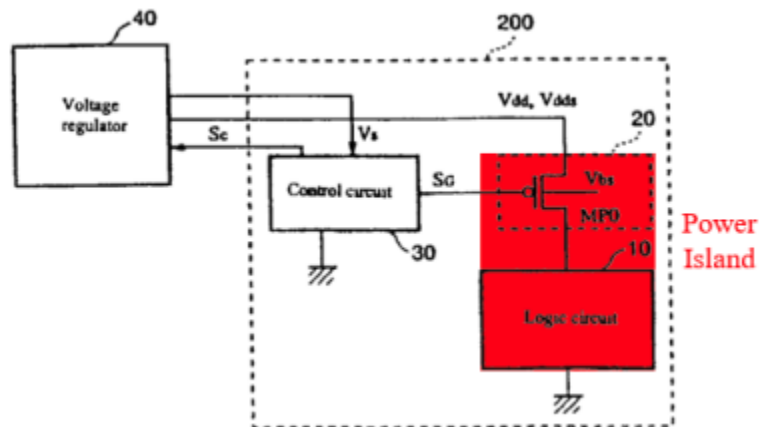
Ex. 1004 [Takahashi] Fig. 10 (as annotated by Petitioner, Pet., 14). But Petitioner's expert does not identify any component responsible for setting or changing the states of the transistors 310-380 in Takahashi's Figure 10, whether in Takahashi's Figure 10, or anywhere else. See Section II.C.1(c).

As a threshold matter, none of these three systems—Takahashi's Figure 1, Takahashi's Figure 16, or Takahashi's Figure 10—discloses “a plurality of power islands,” as required by all challenged claims. Petitioner's arguments that systems comprising “a plurality of power islands” could nevertheless be rendered obvious by these disparate disclosures are conclusory.

a. *Petitioner Admits That Takahashi's Figure 1 Does Not Disclose “A Plurality Of Power Islands.”*

Petitioner admits that Takahashi's Figure 1 does not disclose a “plurality of power islands.” Petitioner's annotation of Takahashi's Figure 1 identifies only a

block consisting of the “logic circuit 10” and “switching circuit 20” as a power island, Pet., 11, admits that at most, Takahashi’s Figure 1 discloses at most a single power island—not “a plurality of power islands.”



Pet., 11 (Fig. 1 of Takahashi, as annotated by Petitioner).

Petitioner confirms this reading of Figure 1 when it elsewhere states, in conclusory terms, that “a POSITA also would have found it obvious for Takahashi’s integrated circuit, such as the ones depicted in Figures 1-5 and 11-17, to include multiple additional power islands.” Pet., 13 (citing Ex. 1003 [Min-Decl.] ¶ 106, which states the same conclusion).⁴ Although Petitioner does not elaborate upon the relevance of including “multiple additional” power islands in Takahashi’s Figure 1,

⁴ Petitioner’s alleged motivation to make this modification, see Pet., 13-15, is discussed further in Section II.C.2(b) below.

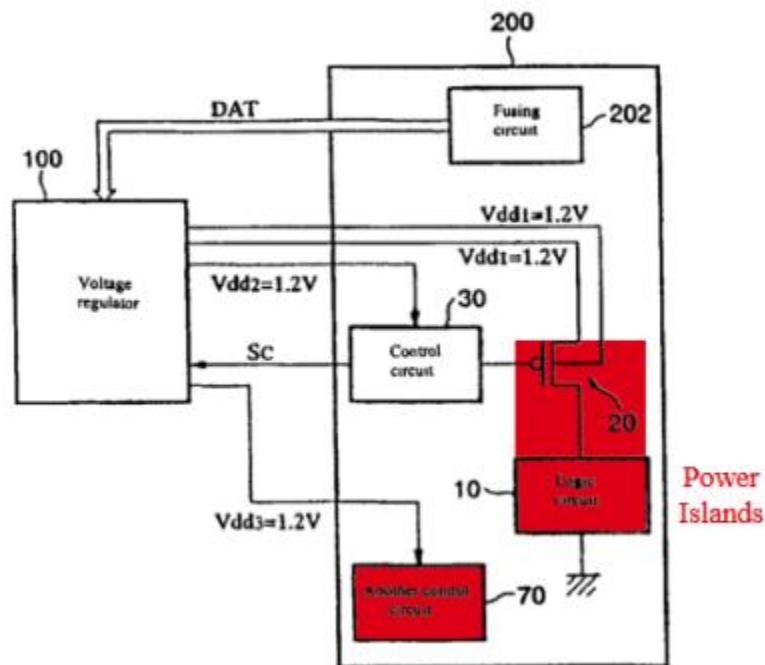
implicitly, Petitioner is attempting to address the fact that Takahashi's Figure 1 does **not** include "multiple ... power islands" to begin with—*i.e.*, that Takahashi's Figure 1 does not disclose "a plurality of power islands," as required by all challenged claims.

b. *Petitioner Does Not Show That Takahashi's Figure 16 Discloses "A Plurality Of Power Islands."*

Petitioner argues that Takahashi's Figure 16 teaches a plurality of power islands in its disclosure of a "logic circuit 10" and its "switching circuit 20" (one purported power island), and in its "another control circuit 70" (a second power island, or at least a part of a second allegedly obvious power island). See Pet., 12-13. It is not clear whether Petitioner takes the position that "another control circuit 70" as disclosed in Takahashi is by itself a second "power island" (as suggested by Petitioner's annotation of Figure 16, Pet., 12), or whether Petitioner argues only that it would be obvious for "another control circuit 70" to be made **part of** a second "power island" in a modification of Figure 16 that added circuitry not already present in Figure 16 (as suggested by Petitioner's argument that a POSITA "would have found it obvious to include another 'switching circuit 20' ... to further reduce power consumption ... in 'control circuit 70,'" Pet., 13). Either way, Petitioner's analysis is again flawed, because Petitioner simply asserts that these components are power islands without engaging with the essential characteristics of a "power island." As

discussed above, in the co-pending litigation, the parties propose constructions of the term “power island” which agree on the premise that a power island is a section of an integrated circuit where power consumption is controlled by independently varying at least one of its operating voltage and its frequency of operation. See Section II.B. Petitioner does not even attempt to argue that this is the case, *see id.*, and this is not the case.

Petitioner’s annotated version of Figure 16 is again reproduced below:



Pet., 12 (Figure 16 as annotated by Petitioner, showing “logic circuit 10” and “another control circuit 70” as parts of alleged power islands within “device 200”); *see also id.* (citing Ex. 1004 [Takahashi] [0110]). Both of Petitioner’s alleged

“power islands” are part of a single component (Figure 16’s “device 200”) that Takahashi discloses as having two alternative states: “operation” (or “active”) and “standby” (or “sleep”), as discussed above.

For good reason, Petitioner does not argue (let alone demonstrate) that the blocks it annotates in red in Takahashi’s Figure 16 are “power islands” under either the *Freescall* or *Xilinx* district court constructions, proffered by Patent Owner and Petitioner, respectively, in the co-pending district court litigation. See Section II.B. Under those constructions, a “power island” is “a section of an integrated circuit where power consumption is controlled by ***independently varying*** its operating voltage and its frequency of operation” or “***independently varying*** its operating voltage or its frequency of operation (or both).” See *id.* Petitioner does not even attempt to identify evidence that power consumption in either block is “controlled by ***independently varying*** its operating voltage [and/or] its frequency of operation [or both].”

To the contrary, Takahashi expressly discloses that the voltages supplied to “logic circuit 10” and “another circuit 70” in Figure 16 are ***not*** independently varying; they are regulated together. Both the “logic circuit 10” and “another circuit 70” are part of a single “device 200,” see Ex. 1004 [Takahashi] Fig. 16, and Takahashi discloses that the “logic circuit 10” and “another circuit 70” each receive one voltage when the entire “device 200” is in its “operation” state, and another

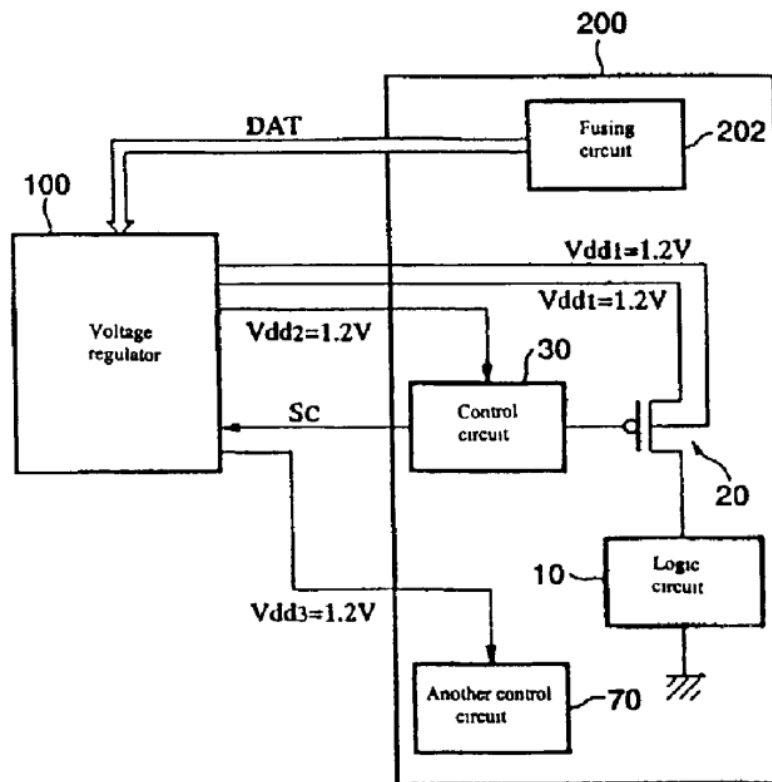
voltage when the entire “device 200” is in its “standby” state. *See, e.g., id.*, [0112] & Fig. 16 (labeling the voltages supplied to “logic circuit 10” and “another circuit 70” in Figure 16 as “ V_{dd1} ” and “ V_{dd3} ,” respectively), [0110] (referring to “voltage levels of source voltages V_{dd1} ... and V_{dd3} ” within “device 200 during operation (Active mode) and during standby (Sleep mode)”)⁵; [0111] (stating that “Voltage regulator 100 [in Figure 16] generates different levels of source voltages during operation and during standby”). Petitioner expressly acknowledges that the voltages supplied to “logic circuit 10” and “control circuit 70” are regulated **together** (and not independently varying) when Petitioner argues that “[i]n ‘Active mode,’ the ‘voltage regulator’ ... provides an ‘operating voltage’ to the ... circuitries, including ‘logic circuit 10’ **and** ‘control circuit 70,’” while “[d]uring ‘Sleep mode,’ the ‘voltage regulator’ ... lowers (i.e., varies) the voltage signals to place the ... circuitries, including ‘logic circuit 10’ **and** ‘control circuit 70,’ into a low-power standby

⁵ Although many of Takahashi’s Figures 11-17 do not individually disclose every feature of Takahashi’s Figure 16, the Petition invites the Board to read these figures as though they describe the Figure 16 embodiment, *see, e.g., Pet.*, 8 (referring to an embodiment “shown in Figures 11-17”), and for purposes of the Board’s institution decision, Patent Owner assumes that they do so.

status.” Pet., 18.

Not only does Takahashi disclose that the voltages supplied to “logic circuit 10” and “control circuit 70” in its Figure 16 are regulated together, Takahashi expressly discloses that the voltages supplied to “logic circuit 10” and “control circuit 70” in Figure 16 are *exactly the same* in either state of the “device 200.”

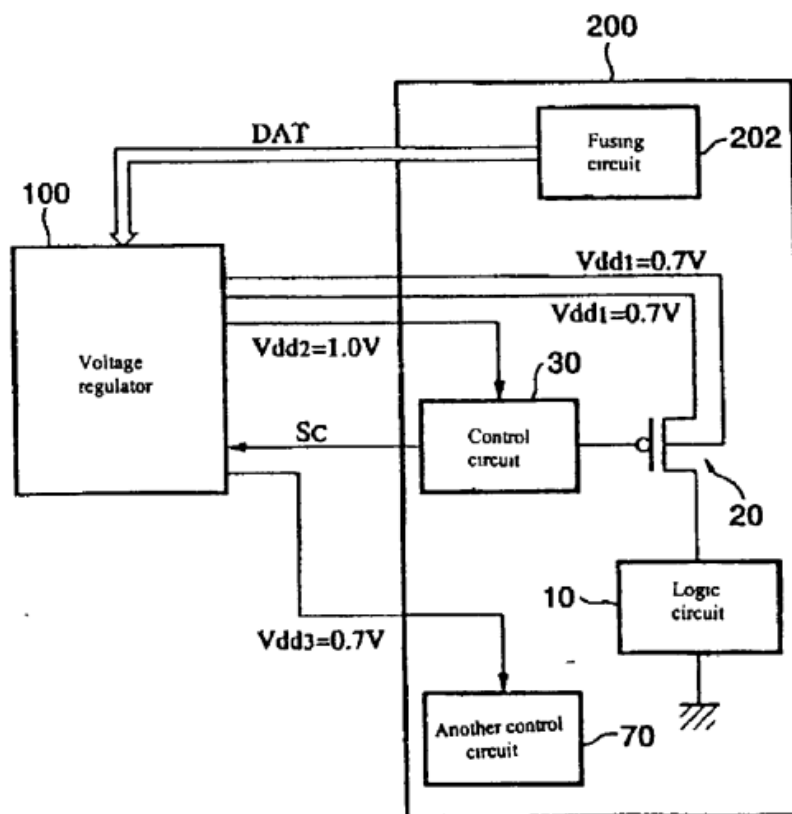
Figure 16 expressly provides that the same 1.2V is supplied to “logic circuit 10” (as “ V_{dd1} ”) and to “another control circuit 70” (as “ V_{dd3} ”) during the “operation” state of the “device 200”:



Ex. 1004 [Takahashi] Fig. 16, [0112] (“FIG. 16 is a circuit diagram showing source voltages V_{dd1} , V_{dd2} , and V_{dd3} generated by voltage regulator 100 during *operation*

and the destinations to which the respective source voltages are supplied.”).

Figure 17 similarly expressly provides that the same 0.7V is supplied to “logic circuit 10” (as “ V_{dd1} ”) and to “another control circuit 70” (as “ V_{dd3} ”) in the “standby” state of the “device 200”:



Ex. 1004 [Takahashi] [0114] (“FIG. 17 is a circuit diagram showing source voltages V_{dd1} , V_{dd2} , and V_{dd3} generated by voltage regulator 100 during *standby* and the destinations to which the respective source voltages are supplied.”).

As briefly discussed above, see Section II.C.1.a, Takahashi also discloses

variations of its Figure 16 in which the “fusing circuit 202” configured differently. Takahashi’s Figure 16 corresponds to a system where the transistors comprising the “device 200” were classified as “weak,” and the values of the voltages V_{dd1} , V_{dd2} , and V_{dd3} correspondingly set to voltages deemed appropriate by the designer for such transistors. *See, e.g.*, Ex. 1004 [Takahashi] [0117] (“process requirements of device 200 are decided through inspections, the fuses in fusing circuit 202 are disconnected accordingly through programming, and control data DAT in accordance with the process requirements of device 200 is output into voltage regulator 100”); [0113] (Figure 16 is labeled “assuming, for example, that the transistors constituting device 200 are in the ‘Weak’ section under the process requirements”); [0099] (“when the driving capabilities of the transistors are weak, the levels of the source voltages supplied to device 200 are set high.”). Takahashi states that when “fusing circuit 202” is configured differently (*i.e.*, because the transistors comprising the “device 200” are classified as something other than “weak”), the voltages V_{dd1} and V_{dd3} supplied to the “logic circuit 10” and “another control circuit 70” may be set to values **other** than the values depicted in Figure 16. *See, e.g., id.*, [0117]. Even in these alternate configurations, however, Takahashi expressly discloses that the voltages supplied to the “logic circuit 10” and “another control circuit 70” are **the same** in both states of the “device 200”—in particular, these voltages are not independently variable in any embodiment.

Petitioner's annotation of Takahashi's Figures 14 and 15 confirms this by disclosing that whether the transistors in the circuit were classified as "weak," "strong," or as other possibilities, the voltage " V_{dd1} " supplied to the "logic circuit 10" is the same as the voltage " V_{dd3} " supplied to "another circuit 70" in both states of operation of the resulting circuit:

Active Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	1.2V	1.2V	1.20V	Weak
Fuse prog-1	0	0	1	1.15V	1.15V	1.15V	NTPW,NWPT
Fuse prog-2	0	1	0	1.05V	1.05V	1.05V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.95V	0.95V	0.95V	NSPT,NTPS
Fuse prog-4	1	0	0	0.85V	0.85V	0.85V	Strong

FIG. 14

Sleep Mode	Bit 2	Bit 1	Bit 0	Vdd1 SW Tr Source (TVDD)	Vdd2 SW Tr Gate	Vdd3 Wake up logic	Process requirement
Fuse prog-0	0	0	0	0.7V	1.0V	0.7V	Weak
Fuse prog-1	0	0	1	0.7V	1.0V	0.7V	NTPW,NWPT
Fuse prog-2	0	1	0	0.7V	1.0V	0.7V	TYPC,NSPW,NWPS
Fuse prog-3	0	1	1	0.7V	1.0V	0.7V	NSPT,NTPS
Fuse prog-4	1	0	0	0.7V	1.0V	0.7V	Strong

FIG. 15

Pet., 18 (Petitioner's annotation of Ex. 1004 [Takahashi] FIGS. 14 & 15, depicting " V_{dd1} " and " V_{dd3} " as the same in each "Process requirement"). (Here, the "operation" state of "device 200" is labeled "Active mode" and the "standby" state of "device 200" is labeled "Sleep mode." Ex. 1004 [Takahashi] [0110]-[0111].)

In sum: Petitioner's analysis of Figure 16 only cites embodiments where the

voltages supplied to the “logic circuit 10” and “another control circuit 70” are exactly the same during all states of operation of the “device 200” of which they are a part. (Petitioner does not analyze any frequencies of operation of these components.) Correspondingly, Petitioner makes no showing that Takahashi’s Figure 16 discloses “a plurality of power islands” in its “logic circuit 10” or “another circuit control 70” under either party’s proposed district court construction of “power island.” See Section II.B.

Even if the Board did not adopt either prior district court construction, any interpretation of “power island” would (at a minimum) have to be consistent with the ’349 patent’s disclosure that “[a] power island is any section, delineation, partition, or division of an integrated circuit where power consumption is **controlled within** the section ...” Ex. 1001 [’349] 4:8-12. One would not regard power consumption as “controlled within” a section of circuitry in a design where power consumption of the section is **only** variable in ways that affect the power consumption of other circuitry. Yet this is what Petitioner is essentially arguing.

Petitioner states, for example, that “power consumption within ‘control circuit 70’ is controlled ... by ‘source voltage V_{dd3} ’ that varies based on whether it is in an operational or standby state.” Pet., 12 (citing Ex. 1004 [Takahashi] [0110]-[0116] & FIGS. 14-17). Here, the word “it” in Petitioner’s “whether it is in an operational or standby state” can only be understood consistently with Takahashi if “it” refers

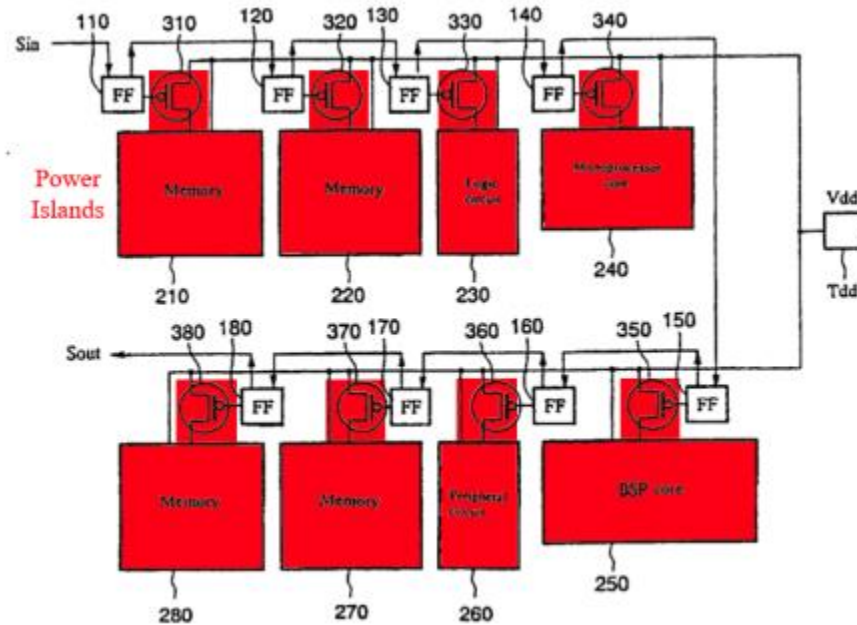
to the “device 200” of which “another control circuit 70” is a part. Takahashi **nowhere** discloses, for example, that “another control circuit 70” is provided the “ V_{dd3} ” of 1.2 V from Figure 16 (associated with “operation,” Ex. 1004 [Takahashi] [0041]) at the same time that “logic circuit 10” is provided the “ V_{dd1} ” of 0.7 V labeled from Figure 17 (associated with “standby,” Ex. 1004 [Takahashi] [0042]). Directly to the contrary, Takahashi states its Figure 16 describes the “source voltages V_{dd1} , V_{dd2} , **and** V_{dd3} generated by voltage regulator 100 during operation,” while its Figure 17 alone describes “source voltages V_{dd1} , V_{dd2} , **and** V_{dd3} generated by voltage regulator 100 during standby.” Ex. 1004 [Takahashi] [0112], [0114].

Petitioner’s argument, then, is that “another control circuit 70” in Takahashi’s Figure 16 is a “power island” because the entire **device 200** can be in an “operation” or “standby” state. This is not a showing that power consumption is **controlled within** “another control circuit 70” in Figure 16, but a showing that power consumption in “another control circuit 70” is **not** controlled within “another control circuit 70” in Figure 16, such that power consumption in “another control circuit 70” in Figure 16 is inconsistent with the specification’s discussion of how power consumption is controlled in “power islands.”

For at least these reasons, Petitioner does not show that Takahashi’s Figure 16 discloses “a plurality of power islands.”

c. *Petitioner Does Not Show That Takahashi's Figure 10 Discloses Or Teaches "A Plurality Of Power Islands."*

In identifying purported disclosures of “power islands,” Petitioner also briefly discusses Takahashi’s Figure 10. Pet., 13-15. Petitioner’s annotation of Takahashi’s Figure 10 is reproduced below. Petitioner contends that “[e]ach of these functional circuits 210-280 ... along with their respective ‘pMOS transistors 310, 320, ..., and 380’ ... comprises a power island.” Pet., 13.



Id., 14 (Petitioner’s annotation).

As an initial matter, Petitioner, quite rightly, does not argue that Takahashi’s Figure 10 discloses a system for practicing the entirety of any challenged claim. Petitioner does not, for example, identify any “control signal” or “adaptive leakage controller” in Figure 10. Petitioner cannot make such arguments because Petitioner

does not identify anything in Figure 10 that modifies the states of the pMOS transistors 310-380, let alone modifies these states such that the power consumption in any functional circuit 210-280 is then controlled by independently varying its operating voltage or frequency of operation.

In more detail, Takahashi describes its Figure 10 as directed towards an “ I_{ddq} Measuring circuit” capable of “performing I_{ddq} measurement,” *i.e.*, testing for manufacturing defects. Ex. 1004 [Takahashi] [0085]-[0087] (“FIG. 10 shows an example of a circuit capable of performing I_{ddq} measurement.”); [0015] (“In addition, there is no effective I_{ddq} testing method for detecting manufacturing defects for the aforementioned technologies.”). The disclosure accompanying Takahashi’s Figure 10 correspondingly focuses on the setup of I_{ddq} measurement, and not on the functionality of any circuit that includes Figure 10’s “functional circuits.” *Id.*, [0091]; [0094] (“power consumption of the respective functional circuits ... can be measured using the measuring circuit of the present example by designing a test pattern to be input into the scan-pass circuit appropriately.”); [0095] (“by controlling the on/off status of the respective transistors ... I_{ddq} of a specific functional circuit can be measured ...”).

Takahashi discloses that the components 210-280 in Figure 10 are “functional circuits to be operated using source voltage V_{dd} .” *Id.*, [0089]. During I_{ddq} measurement, the “scan-pass circuit” of Figure 10 “is configured with flip-flops 110,

120, ... , and 180” via “[t]est data S_{in} input” that “is transferred to the output side one after another by said scan-pass circuit.” *Id.*, [0088]. The “pMOS transistors 310, 320, ... , and 380 ... are turned on/off according to the data held in respective flip-flops 110, 120, ... , and 180 in order to supply a driving current to a prescribed functional circuit when in the on status.” *Id.* [0090].

Takahashi offers the following example of the transistors being “turned on/off according to the data held in respective flip-flops 110, 120, ... , and 180”:

For example, *when the test pattern is designed appropriately*, data [logic] 0 is stored into flipflop 130, and data [logic] 1 is stored into all the other flip-flops. Under said condition, transistor 330 is on, and the other transistors are all off. Thus, driving current is supplied to logic circuit 230, and logic circuit 230 becomes operational. On the other hand, because no driving current is supplied to any functional circuits other than logic circuit 230, these functional circuits are all in the standby status.

Ex. 1004 [Takahashi] [0092]. Significantly, Takahashi does not say that any ***component of Figure 10*** provides the “test pattern” in this example, or that any component of Figure 10 would otherwise be responsible for controlling the on/off status of the transistors 310-380 in this example. Similarly, the disclosures cited by Petitioner, *see generally* Pet., 13 (citing Ex. 1003 [Takahashi] [0090]), indicate only that during I_{ddq} measurement, the states of transistors 310-380 and the

operational/standby states of the corresponding functional circuits correspond with one another, and follow a “test pattern” input—that is, a transistor is on (and its corresponding functional circuit operational) during the measurement, or off (and its corresponding functional circuit in standby) during the measurement, according to data supplied by a “test pattern” from a source not depicted in Figure 10. *See, e.g.*, Ex. 1003 [Takahashi] [0092]. Takahashi is entirely silent on what might specify or generate any given “test pattern” input to its Figure 10.

Indeed, Takahashi contains repeated express disclosures, not cited by Petitioner, suggesting that Takahashi’s Figure 10 is not itself designed to control the states of the transistors 310-380. Quoting selectively from Takahashi, for example, Petitioner states:

“These [sleep] transistors are turned on/off ... to supply a driving current to a prescribed functional circuit when in the on status” and suppress the “occurrence of a leakage current” during standby, thereby reducing power consumption due to leakage.

Pet., 23 (quoting Ex.1004 [Takahashi] [0090] (Petitioner’s ellipsis)). Petitioner omits what little Takahashi says about **how** its transistors are turned on/off: in more detail, the sentence partially quoted by Petitioner states:

[t]hese transistors are turned on/off ***according to the data held in respective flip-flops 110, 120, ..., and 180*** in order to supply a driving current to a prescribed functional circuit when in the on status.

Ex. 1004 [Takahashi] [0090]. And Takahashi is entirely silent on what supplies “the data held in respective flip-flops 110, 120, ... , 180,” stating only that that the “on/off status of [the] respective transistors 310, 320, ... , and 380 [in Figure 10] **can be** controlled individually **by designing a pattern ... of test data input** into the scan-pass circuit **appropriately.**” *Id.*, [0091]; *see also id.*, [0092] (discussing how components of the logic circuits depicted in Figure 10 may behave “when the test pattern is **designed appropriately**”), [0094] (stating “power consumption of the respective functional circuits during the operation can be measured using the measuring circuit of the present example by **designing a test pattern** to be input into the scan-pass circuit **appropriately.**”).

Petitioner does not address these disclosures in Takahashi, let alone address any differences that might exist between whatever mechanism that might be used to set the “on/off status” of the “transistors 310, 320, ... , and 380” via the “test data input into the scan-pass circuit” of Figure 10, Ex. 1004 [Takahashi] [0091], and the control mechanism that Petitioner discusses in connection with the “power islands” alleged to exist in Figures 1 and 16—namely, the “voltage regulator” depicted in those figures (but **not** depicted in Figure 10). *See, e.g.*, Pet. 17-18 (stating that “the outputs of the ‘voltage regulator’” in Takahashi “control[] power within the power island[s]”).

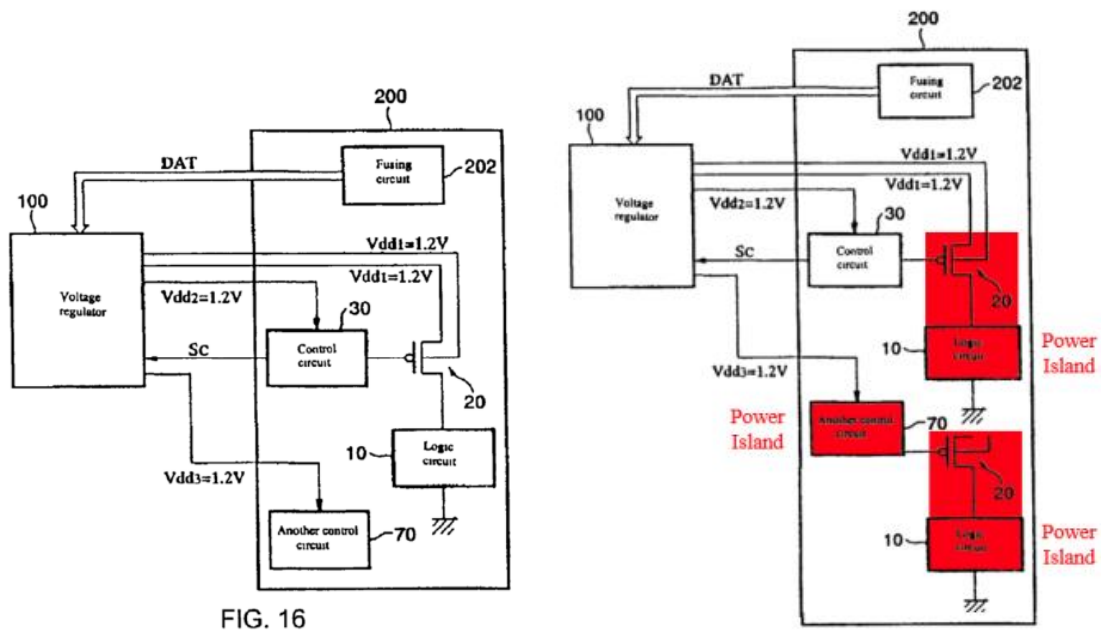
In any event, under either party’s proposed district court construction, a

“power island” is a portion of an integrated circuit “where power consumption **is controlled** by independently varying” at least one power characteristic of that portion—its “operating voltage,” its “frequency of operation,” or both. See Section II.B. As Takahashi is silent on how the states of transistors 310-380 in its Figure 10 are actually set—stating only that they could be determined by designing a test pattern “appropriately”—the evidence cited by Petitioner does not show that the functional circuits 210-280 are “power islands” in Figure 10. Indeed, here Petitioner is making a basic error: confusing a disclosure of components that **could be** “power islands” **in an appropriately designed system** with components that **are** “power islands” in a given system, because of how the system is configured to control them.

Even if the Board did not adopt the construction proposed by either party in the co-pending litigation, a “power island” in the sense of ’349 patent should be interpreted consistently with the ’349 patent’s disclosure that “[a] power island is any section, delineation, partition, or division of an integrated circuit where power consumption is **controlled** within the section, delineation, partition, or division.” Ex. 1001 [’349] 4:8-12. Again, because Takahashi does not disclose how the states of transistors 310-380 in its Figure 10 are set (except to say that they can be determined by designing a test pattern “appropriately”), Petitioner has not shown that the power consumptions of the functional circuits 210-280 are controlled in Figure 10 consistent with this disclosure in the specification.

Petitioner implicitly acknowledges that Takahashi's Figure 10 might not disclose "a plurality of power islands" in its proposed obviousness combination, in which Petitioner proposes that Figure 10 teaches the inclusion of "multiple additional power islands" in Takashi's Figure 16. *See* Pet., 13-15. (Petitioner has not offered any non-conclusory basis for a motivation to combine these disclosures, as discussed elsewhere. *See* Section II.C.2.b.) In this proposal, Petitioner makes no use of Takahashi's Figure 10 for any alleged control of the "power islands" in its proposed combination. Petitioner's failure to use Takahashi's Figure 10 for this purpose makes sense because, as explained above, Takahashi's Figure 10 does not itself disclose "a plurality of power islands." And Petitioner does not show how the proposed combination discloses "a plurality of power islands," either.

In more detail, citing Takahashi's Figure 10, Petitioner states that "a POSITA also would have found it obvious for Takahashi's integrated circuit, such as the ones depicted in Figures 1-5 and 11-17, to include multiple additional power islands." *Id.*, 13. Petitioner argues that a POSITA "would have further understood that" Takahashi's Figure 16 embodiment, for example, "can include more than one 'logic circuit' and been motivated to provide a 'switching circuit' ... for each to obtain the same power savings described for Figure 10." *Id.*, 14-15. Petitioner accompanies this argument with a modified version of Takahashi's Figure 16, which is reproduced to the right of Takahashi's actual Figure 16 below.



Ex. 1004 [Takahashi] Fig. 16; Pet., 15 (Fig. 16 as modified by Petitioner).

Although Petitioner styles its modification of Figure 16 as “incorporat[ing] power islands like these [in Figure 10] into the embodiments of Figures 1-5 and 11-17,” Pet., 14, the mechanism of controlling power within the alleged “power islands” in Petitioner’s combination is not taken from Figure 10 at all. In the above modified figure, Petitioner proposes that a POSITA would have “understood that a device can include more than one ‘logic circuit’ and been motivated to provide a ‘switching circuit’ ... for each,” and implies (by depicting the “voltage regulator” of Figure 16 in unmodified form in the modified figure) that the resulting circuit would somehow employ the voltage regulator of Figure 16. Pet., 14-15. Petitioner proposes, in other words, that components *already present* in Figure 16 be duplicated (as to “include more than one ‘logic circuit’ and ... a ‘switching circuit’ ... for each,” *id.*, 14), and

that control of the resulting system somehow be implemented by a modified form of the “voltage regulator 100” ***already present*** in Figure 16. No mention is made here of any “flip-flops” configured with “test data” from an input S_{in} to a “scan-pass circuit,” as identified by Petitioner’s expert (but not Petitioner) in connection with alleging that Takahashi’s Figure 10 disclosed “power islands” in its functional circuits 210-280. *See* Ex. 1003 [Min-Decl.] ¶¶ 107-108. Presumably, Petitioner is not drawing from the actual structure of Figure 10 in its combination because it is attempting to argue that its combination embodies the challenged claims. *See, e.g.,* Pet., 17 (annotating Takahashi’s Figure 16 with labels indicative of claim limitations other than “power island”). If control of the components of Petitioner’s combination were dependent upon unspecified “test data” from an unidentified source (as is the case in Figure 10), then even Petitioner would presumably have to admit that this combination did not embody any of the challenged claims, as Petitioner appears to concede that Figure 10 does not embody any challenged claim.

Petitioner’s actual proposal—that power consumption in the purported “power islands” in its proposed modification of Figure 16 could be controlled by a modified version of the voltage regulator in Figure 16—fares no better. As explained above, the components alleged by Petitioner to be “power islands” in Figure 16 are not “power islands” because Takahashi expressly discloses that their supply voltages are regulated together—according to the state of the “device 200”

of which they are a part. See Section II.C.1.b. In proposing that “[a] POSITA would have further understood that a device [as in Figure 16] can include more than one ‘logic circuit’ and been motivated to provide a ‘switching circuit’ ... for each,” Pet., 14, Petitioner proposes adding more components to Takahashi’s Figure 16, without explaining how the voltage regulator in the modified Figure 16 would be configured to provide independently varying voltages to these components. In not addressing this issue, Petitioner’s “analysis” of its modified Figure 16 simply takes for granted that Takahashi’s Figure 16 already discloses a “plurality of power islands”—which it does not. See Section II.C.1.b.

For at least these reasons, Petitioner does not show that Takahashi’s Figure 10 discloses or renders obvious “a plurality of power islands.”

2. Petitioner’s Arguments That Takahashi Renders Obvious “A Plurality Of Power Islands” Are Conclusory.

Although Petitioner’s Grounds 1A, 1B, and 1C are styled as single-reference obviousness grounds, Petitioner never expressly acknowledges—not even in the alternative, or for purposes of argument only—exactly **how** the disclosures it cites might fail to anticipate the challenged claims. One is left wondering whether Petitioner is arguing obviousness at all (*i.e.*, whether Petitioner is actually arguing that the cited embodiments of Takahashi necessarily practice the challenged claims), whether Petitioner’s argument is that a cited embodiment could obviously have been

configured to practice the challenged claims even if it would not necessarily do so, or whether Petitioner is drawing upon an alleged understanding of the POSITA to modify or combine disclosures in Takahashi to arrive the claimed invention. Because of this lack of specificity, it is no surprise that Petitioner’s arguments are conclusory and fail.

a. *Petitioner Does Not Distinguish Alleged Teachings Of Takahashi From Express Disclosures In Takahashi.*

Separately from arguing that Takahashi discloses “a plurality of power islands,” the Petition states in the alternative that Takahashi renders this limitation obvious. But the only arguments offered specifically for purposes of Petitioner’s obviousness arguments are conclusory. The Petition’s failure to articulate a substantive obviousness argument is a consequence of its failure to expressly identify—even in an alternative, or for the purposes of argument—exactly where Takahashi might fail to disclose a “plurality of power islands.” Petitioner’s refusal to expressly acknowledge where the cited disclosures might **not** disclose the claimed invention is contrary to the law of obviousness, which requires identification of “the differences between the subject matter sought to be patented and the prior art” 35 U.S.C. § 103 [pre-AIA], *see also, e.g., KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 399 (2007) (citing *Graham v. John Deere Co.*, 383 U. S. 1, 17-18 (1966)).

As one example, the Petition states that “a POSITA would have understood

and found obvious that Takahashi’s logic circuit 10 ... and ‘switching circuit 20’ ... depicted in at least Figures 1, 4-10, 16-17, comprise a power island,” Pet., 11, but only discusses the alleged express disclosures of Takahashi in connection with “logic circuit 10” and “switching circuit 20,” and does not separately argue obviousness. *See id.*

As another example, the Petition states in connection with its discussion of Takahashi’s Figures 1-5 and 11-17 embodiments that a POSITA “would have found it obvious for Takahashi’s integrated circuit ... to include multiple additional power islands.” Pet., 13. Implicitly, this statement is an acknowledgement that Takahashi’s Figures 1-5 and 11-17 might **not** disclose a “plurality of power islands,” as required by all challenged claims. The argument that follows, however, depends upon the assumption that Takahashi’s Figure 10 already discloses “a plurality of power islands,” *see, e.g., id.*, 14 (arguing that “[a] POSITA would have found it obvious to incorporate power islands **like these** [in Figure 10] into the embodiments of Figures 1-5 and 11-17”), which it does not. *See* Section II.C.1(c). The Petition, that is, never expressly makes clear how the claimed systems involving “a plurality of power islands” could be obvious in view of Takahashi, unless a system comprising “a plurality of power islands” were already expressly disclosed in Takahashi.

Indeed, in many places, Petitioner’s arguments refer not to a specific

embodiment of Takahashi, or to Petitioner’s proposed modification of the Figure 16 embodiment of Takahashi, but only to “Takahashi’s integrated circuit”—making it difficult to determine what Petitioner is even arguing to render the challenged claims obvious. As an example of this difficulty, the following chart illustrates Petitioner’s scattershot approach in the context of claim 1.

Claim 1 element as labeled by Petitioner ⁶	Embodiments in Petitioner’s argument
1[a]	Figure 1 (<i>e.g.</i> , Pet., 11) Figure 16 (<i>e.g.</i> , Pet., 12) Figure 10 (<i>e.g.</i> , Pet., 14)
1[b]	Figure 1 (<i>e.g.</i> , Pet., 17, 19) Figure 16 (<i>e.g.</i> , Pet., 17, 20)
1[c]	Figure 1 (<i>e.g.</i> , Pet., 22) Figure 10 (<i>e.g.</i> , Pet., 23) Figure 16 (<i>e.g.</i> , Pet., 23-24) Modification of Figure 16 to “include additional power

⁶ The labels “1[a],” “1[b],” and “1[c]” refer to Petitioner’s partition of claim 1 into elements. Pet., vii.

Claim 1 element as labeled by Petitioner ⁶	Embodiments in Petitioner's argument
	islands” as allegedly taught by Figure 10 (<i>e.g.</i> , Pet., 24)
1[d]	Figure 1 (<i>e.g.</i> , Pet., 25) Figure 16 (<i>e.g.</i> , Pet. 26)
1[e]	Figure 1 (<i>e.g.</i> , Pet., 29) Figure 16 (<i>e.g.</i> , Pet. 30)

As this chart indicates, it is possible to read Petitioner as arguing that claim 1 is separately and independently rendered obvious by Takahashi's Figure 1 alone and by Takahashi's Figure 16 alone, but the Petition never expressly states either of these contentions—or identifies why these embodiments of Takahashi might render claim 1 obvious even if they do not anticipate it.⁷ Petitioner's “obviousness” arguments

⁷ Although Petitioner does not appear to take the position that Takahashi's Figure 10 discloses a system that embodies any of the claims (without modification), for example, *see* Pet., 13-15, 22-23 (discussing Figure 10 without mapping it to claim language); Section II.C.1(c), the Petition can be read as taking the position that Takahashi's unmodified Figures 1 and 16 do each embody at least challenged independent claim 1.

should be rejected for this lack of specificity. *See, e.g., Valeo N. Am., Inc. v. Magna Elecs., Inc.*, IPR2014-01206, Paper 13, 15 (Dec. 23, 2014) (denying institution and noting that “Petitioner’s obviousness analysis is incomplete in that it: fails to state explicitly the differences between the [prior art] and the claimed subject matter, does not explain persuasively the relevance of the evidence, and presents conclusory assertions regarding how the references are combined.”); *Matterport, Inc. v. Appliance Computing III, Inc.*, IPR2021-00939, Paper 15, 16–17 (Nov. 23, 2021) (denying institution because “Petitioner does not identify differences between [cited art] and element 1.2 or how Petitioner proposes to combine or modify the asserted prior art to meet element 1.2.”).

b. *Petitioner Offers Only Conclusory Statements, Not Evidence, About The Motivation To Combine Takahashi’s Distinct Disclosures In The Way Proposed By Petitioner.*

Even when arguing obviousness based upon a single reference, a motivation must exist for combining features of different embodiments or otherwise modifying the teachings of a reference. *See, e.g., In re Kotzab*, 217 F.3d 1365, 1370 (Fed. Cir. 2000). In determining whether there is a motivation to combine, there must be “particular findings” of a reason the ordinary artisan, with no knowledge of the claimed invention, “would have selected these components for combination in the manner claimed.” *Polaris Indus., Inc. v. Arctic Cat, Inc.*, 882 F.3d 1056, 1069 n.4

(Fed. Cir. 2018).

The Petition asserts that a POSITA would have been motivated to modify Takahashi's Figures 1 and Figure 16 "to incorporate power islands like these [alleged to exist in Figure 10]" "to provide additional functionality (e.g., memory), and to control their power consumption," Pet., 14, and to "obtain the same power savings described for Figure 10." *Id.* These arguments are legally insufficient and unsupported by evidence.

First, a generically stated desire to improve something is insufficient, without more, to show that a POSITA would have combined features in a particular way. In *ActiveVideo Networks, Inc. v. Verizon Commc 'ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012), for example, the challenger's expert testified that "[t]he motivation to combine would be because you wanted to build something better. You wanted a system that was more efficient, cheaper, or you wanted a system that had more features, makes it more attractive to your customers," and the Federal Circuit rejected this testimony as insufficient, as a matter of law, to support a finding of obviousness. Citing *ActiveVideo* and similar cases, the Board has found testimony that a proposed modification would provide "increased utility" and could be obtained with "minimal modifications" to be "generic," failing "to provide necessary factual support" for a motivation to combine, and "akin to stating in a conclusory fashion that the combination 'would have been obvious.'" *See, e.g., Samsung Austin*

Semiconductor, LLC v. Red Rock Analytics, LLC, IPR2018-00556, Paper 18, 21 (Aug. 20, 2018). To prove obviousness, a challenger must make “clear how Petitioner relies upon its alleged motivations to combine as support for its contention that the claimed invention would have been obvious,” by “connect[ing] the alleged rationale to combine the prior art with the specific limitations of the claims and claim mapping.” *PayPal, Inc. v. IOENGINE, LLC*, IPR2019-00906, Paper 16, 22 (Oct. 29, 2019).

Petitioner does not substantively address what would motivate a POSITA to “incorporate power islands like these” into Figures 1-5 or Figures 11-17, beyond a rote statement that such a modification would “provide additional functionality (e.g., memory), and to control their power consumption.” Pet., 14. Petitioner’s expert merely repeats similar statements. See Ex. 1003 [Min-Decl.] ¶ 109. Aside from generally suggesting that Takahashi’s devices might be improved by increasing their capabilities, Petitioner does not address *why*, in view of Takahashi or any other knowledge of the POSITA, a POSITA specifically choose to add “additional functionality (e.g. memory)” to embodiments that Takahashi did not already have memory, or why, if Figures 1-5 and 11-17 did not already disclose “a plurality of power islands,” it would be desirable for a POSITA to use Takahashi’s Figures 1-5 or 11-17 (which do *not* disclose pluralities of power islands, see Sections II.C.1(a), II.C.1(b)) as a model to “control ... power consumption” in a modified circuit that

did (allegedly) have “a plurality of power islands.” Pet., 14.

Petitioner’s alternative “power savings” rationale for combining alleged teachings of Takahashi’s Figure 10 with Takahashi’s Figure 16, *see, e.g.*, Pet., 14, fares no better. As a threshold matter, while Petitioner states in one place that “[a] POSITA would have found it obvious to include another ‘switching circuit’ ... to further reduce power consumption of the ‘Wake up logic’ in ‘control circuit 70’ during standby and achieve the same power savings described for Figure 10 (discussed below)” Pet., 13, and in another place that “[a] POSITA would have further understood that a device can include more than one ‘logic circuit’ and been motivated to provide a ‘switching circuit’ (i.e., sleep transistor) for each to obtain the same power savings described for Figure 10,” Pet., 14, Petitioner does not discuss what the alleged “same power savings described for Figure 10” actually are—and Petitioner’s expert does not elaborate. *See id.*, 13 (citing Ex. 1003 [Min-Decl.] ¶ 111), Ex. 1003 [Min-Decl.] ¶ 111 (referring only to “the same power savings described for Figure 10, as discussed below”); *see also* Pet., 14 (citing Ex. 1003 [Min-Decl.] ¶ 112), Ex. 1003 [Min-Decl.] ¶ 112 (simply repeating Petitioner’s statement about “the same power savings described for Figure 10”).

To the extent that these remarks are intended to refer to Takahashi’s statement that elements of its Figure 10 may help to reduce “leakage current” (and power consumption due to leakage current), *see, e.g.*, Pet., 23; *see also* Ex. 1004

[Takahashi] [0090]; *see also id.*, [0085] (discussing “leakage” in connection with Takahashi’s Figure 9), Petitioner does not argue how these alleged benefits of Figure 10 would necessarily be realized in Petitioner’s proposed combination—which modifies Figure 16 in a way that is not shown to employ the “flip-flops” used in the system of Petitioner’s Figure 10, or the “test data S_{in} input” described by Takahashi in connection with setting the “flip-flops” in Figure 10. *See* Section II.C.1(c).

Similarly, Petitioner’s proposed rationale for modifying Figure 16 has no clear relation to what Takahashi says about its own Figure 10. Takahashi does not disclose that its Figure 10 is useful in achieving general power savings in an integrated circuit. Takahashi states that its Figure 10 is “an example of a circuit capable of performing I_{ddq} measurement,” where the transistors 310-380 on/off states are set before measurement to allow for “power consumption due to leakage current at each functional circuit” to be “measured” “during standby.” Ex. 1004 [Takahashi] [0087], [0094]. Takahashi does not disclose how an implementation of its Figure 10 might affect power consumption when components are **not** in a “standby” status, or how any supposed power savings associated with reduced leakage compare with the power **requirements** of circuitry required to change or otherwise control the “test data” input to Figure 10. (As already noted, *see* Section II.C.1(c), Petitioner does not identify any such control circuitry in Takahashi’s Figure 10 itself.) Similarly, Petitioner does not address whether Figure 1 and Figure 16 may potentially realize

power **savings** by **not** having circuitry capable of independently varying the power consumptions of the components identified by Petitioner, or otherwise assess the impact of making unspecified modifications to the voltage regulators in those figures.

A proper obviousness analysis “concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015). Petitioner’s arguments, which amount to simply asserting that a POSITA would have found it advantageous to satisfy the claims, do not address this, and do not show that the challenged claims are obvious.

D. Petitioner’s Mizuno Grounds Fail (All Claims, Grounds 2A, 2B).

Petitioner’s arguments regarding the Mizuno reference share the same faults as Petitioner’s arguments involving Takahashi. Broadly speaking, Petitioner invites the Board to infer that any component that is disclosed as capable of being placed in operating or standby states must be a “power island” in any integrated circuit of which it is a part. These arguments, which fail to engage with any construction of “power island,” *see* Section II.B, should be rejected.

1. Petitioner Fails To Show That Mizuno Discloses “A Plurality Of Power Islands” (All Claims, Grounds 2A, 2B).

Mizuno is concerned with aspects of preventing “leakage,” or current flow within a circuit that occurs when the circuit is not in use. *See, e.g.*, Ex. 1005 [Mizuno] [0009] (describing “the present invention” of Mizuno as “capable of reducing the different types of leakage current ... while [a] circuit block is in standby state”). The Petition purports to identify several “power islands” in Mizuno:

First, Petitioner contends that “‘circuit block CKT,’ depicted in Figures 1 and 22 ... and which may include a ‘logic circuit LG1’ and/or a ‘memory MEM1,’ coupled to a power switch PSW1, comprises a power island,” Pet., 60 (quoting Ex. 1005 [Mizuno] [0053]) (citations omitted), allegedly “because power consumption is controlled within it.” Pet., 61-62. The Petition elaborates that Mizuno discloses that the “circuit block CKT” of which the Logic circuit LG1 and Memory MEM1 are both a part is capable of being toggled between an “operating state” and a “standby” state, via operation of a “power switch PSW1” which affects the power consumed by “circuit block CKT.” *Id.*

Second, Petitioner contends that circuit blocks CKT2a and CKT2b of Figures 35-40 are power islands, allegedly because “‘leakage reduction circuits PSM2a and PSM2b,’ which are similar to the leakage reduction circuits in the embodiment of FIGS. 1-30, control/dynamically change power within the circuit blocks CKT2a and

CKT2b, respectively.” Pet., 63-64 (quoting Ex. 1005 [Mizuno] [0121]).

As with Petitioner’s arguments regarding Takahashi, these arguments fail to demonstrate that Mizuno discloses “a plurality of power islands” in the sense of the ’349 patent. The evidence cited by Petitioner does not speak to either of the constructions proposed by the parties in the co-pending district court litigation, *see* Section II.B, or even address the specification’s statement that “a power island is [a] section ... of an integrated circuit where power consumption is controlled ***within the section***”

a. *Petitioner Does Not Show That Mizuno Discloses “A Plurality Of Power Islands” In Its “Figures 1-30.”*

The Petition does not even argue that Mizuno’s “first embodiment,” which Petitioner regards as depicted in both of Mizuno’s Figures 1 and 22, *see, e.g.*, Pet. 60 (stating that “Mizuno discloses a ‘first embodiment,’ in Figures 1-30”), discloses “a plurality of power islands,” arguing only that because “power consumption is controlled within it and is capable of being dynamically changed,” the “circuit block CKT” of Mizuno’s Figure 1 or Figure 22, the “circuit block CKT” of Mizuno’s Figure 1 is a “power island.” Pet., 61-62. In only identifying one purported “power island” in Mizuno’s Figures 1 and 22, Petitioner here implicitly acknowledges that Mizuno’s Figures 1 and 22 do ***not*** disclose a system with “a plurality of power islands.”

Petitioner confirms that Mizuno's Figures 1 and 22 do not disclose "a plurality of power islands" when it later argues that "it would have been obvious to a POSITA to **include** multiple power islands in Mizuno's 'first embodiment' (depicted in FIGS. 1-30)," as supposedly taught by another embodiment in Mizuno. Pet., 64.

b. *Petitioner Does Not Show That Mizuno Discloses "A Plurality Of Power Islands" In Its "Figures 35-40."*

The first "plurality of power islands" argued by Petitioner to be disclosed in Mizuno is the circuit blocks CKT2a and CKT2b of Mizuno's Figures 35-40,⁸ which are alleged to be power islands because "leakage reduction circuits PSM2a and PSM2b," which Petitioner says "are similar to the leakage reduction circuits in the embodiment of FIGS. 1-30," are said to "control/dynamically change power within the circuit blocks CKT2a and CKT2b, respectively." Pet., 63. The Petition does not elaborate upon **how** power to CKT2a and CKT2b is "controlled" or "dynamically changed" by the leakage reduction circuits PSM2a and PSM2b; the Petition only

⁸ Although not all of Mizuno's Figures 35-40 depict both the "CKT2a" and "CKT2b" of, *e.g.*, Mizuno's Figure 35, the Petition treats these figures together, as though they describe a single embodiment, *see, e.g.*, Pet., 63 (referring to "a related 'third embodiment' in FIGS. 35-40"), which Patent Owner will assume to be correct for the purpose of this preliminary response.

says that this occurs, and concludes from this assertion that CKT2a and CKT2b are each power islands.

The Petition does not, for example, offer further explanation of how power consumption of, *e.g.*, CKT2a is specifically “controlled within” CKT2a by leakage reduction circuit PSM2a (Ex. 1001 [’349] 4:8-12), let alone demonstrate that power consumption within CKT2a is controllable by ***independently varying*** the operating voltage of CKT2a and/or the frequency of operation of CKT2a, as either of the parties’ proposed constructions in the district court would require. *See* Section II.B.

Petitioner’s implicit argument may be that a disclosure of separately labeled “leakage reduction circuits” amounts to a teaching of the independent control of these “leakage reduction circuits,” or perhaps more broadly that a disclosure of distinct switches to these circuits renders some mechanism of independent control of power consumption within those circuits obvious. *See generally* Pet., 63-65. But this is not an argument that Petitioner bothers to make; instead, Petitioner’s argument is one of inherency.

To establish inherency, Petitioner must demonstrate that the requisite control (and thus a “plurality of power islands”) is “necessarily present, not merely probably or possibly present, in the prior art.” *Trintec Indus., Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 1295 (Fed. Cir. 2002) (cleaned up); *see also* *PAR Pharm. v. TWi Pharms., Inc.*, 773 F.3d 1186, 1195–96 (Fed. Cir. 2014) (“A party must [] meet a high standard

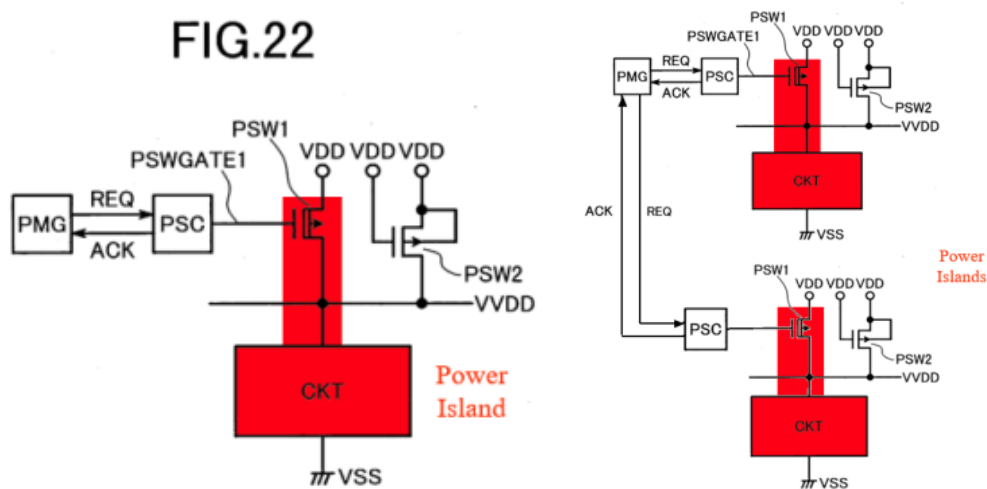
in order to rely on inherency to establish the existence of a claim limitation in the prior art in an obviousness analysis—the limitation at issue necessarily must be present, or the natural result of the combination of elements explicitly disclosed by the prior art.”); *Southwire Co. v. Cerro Wire LLC*, 870 F.3d 1306, 1310–11 (Fed. Cir. 2017) (similar). Petitioner, who does even attempt to address the relevant standard, does not and cannot satisfy this high burden.

2. Petitioner’s Arguments That Mizuno Renders Obvious “A Plurality Of Power Islands” Are Conclusory (All Claims, Grounds 2A, 2B).

Separately from arguing that Mizuno discloses “a plurality of power islands,” the Petition states in the alternative that Mizuno renders this limitation obvious. In each case, however, the support offered for this alternative assertion is conclusory.

Petitioner argues that “it would have been obvious to a POSITA to include multiple power islands in Mizuno’s ‘first embodiment’ (depicted in FIGS. 1-30),” Pet. 64, as allegedly depicted in a proposed modification of Mizuno’s Figure 22. Mizuno’s Figure 22 and Petitioner’s proposed modification are depicted side by side below.

FIG.22



Pet., 61 (Mizuno’s Figure 22, as annotated by Petitioner); 64 (Mizuno’s Figure 22, as modified and annotated by Petitioner). Quoting Mizuno, Petitioner states that “[b]y establishing multiple leakage control circuits as in FIG. 35, and controlling the leakage current of circuits grouped in multiple circuits integrated onto the chip, the leakage current of the overall chip can be efficiently reduced.” *Id.*, 65 (quoting Ex. 1005 [Mizuno] [0122]).

This remark, however, does not elaborate upon **how** the integrated circuit of Figures 1-30 would be modified so that power consumption was “individually controlled” within these multiple circuit blocks, let alone how such a modification of the “first embodiment”—which, to be clear, Petitioner’s expert has characterized only in terms of claim limitations that such a modification would render obvious—would subsequently satisfy or render obvious the remaining limitations of the challenged claims. After modifying Mizuno’s Figure 22 for purposes of locating “a

plurality of power islands” in the resulting system, for example, Petitioner’s analysis never discusses how power consumption would be managed in this modified system (let alone managed by a system that satisfies the rest of any challenged claim).

If Petitioner’s expert is implicitly appealing to common sense—that is, to a vague notion that wherever a reference discloses a single circuit block in a specific context, a POSITA would understand a teaching of a similar circuit that operates “individually controlled” copies of that circuit block—the Petition does not even attempt to address the relevant standard. *See Arendi S.A.R.L. v. Apple, Inc.*, 832 F.3d 1355, 1362–63 (Fed. Cir. 2016) (when there is a “missing limitation” an obviousness argument, the inquiry into “a reasoned basis for resort to common sense must be searching”); *DSS Tech. Mgmt. v. Apple Inc.*, 885 F.3d 1367, 1374 (Fed. Cir. 2018) (“common sense” can be used to supply a missing limitation “**only** when ‘the limitation in question [is] unusually simple and the technology particularly straightforward.’”). Petitioner does not, for example, even argue (let alone identify evidence) that the individual control at issue in managing a plurality of “power islands” in the sense of the challenged claims is “unusually simple” or “particularly straightforward.”

Petitioner’s obviousness analysis of “power islands” as allegedly taught by Mizuno’s Figure 35 embodiment is similarly conclusory. Although the Petition states that a POSITA “would have understood **and found obvious** that Mizuno’s

integrated circuit [in Figure 35] includes multiple power islands,” Pet., 64, the Petition does not contain any argument or evidence specific to obviousness—*i.e.*, why the Figure 35 embodiment, Mizuno’s discussion of this embodiment, or any knowledge of the POSITA would render obvious a “plurality of power islands” in some modification of Mizuno’s Figure 35, if Mizuno’s Figure 35 did not already literally disclose this limitation (which it does not, *see* Section II.D.1.b).

E. Petitioner’s Multiple-Reference Grounds Incorporate The Flaws Of Petitioner’s Single-Reference Grounds (Grounds 1B, 1C, 2B, Claims 7, 8, 14, 15).

Petitioner’s multiple-reference obviousness grounds, which are largely directed to dependent claims, incorporate Petitioner’s single-reference obviousness arguments as to independent claims—particularly independent claim 1—without supplementation. In particular, these grounds do not offer any additional evidence or argument that Takahashi or Mizuno teach “a plurality of power islands” in the sense of the ’349 patent, and do not explain how the grounds would otherwise nevertheless teach “a plurality of power islands” in Petitioner’s proposed combinations. For this reason, the Board does not need to address these grounds in its institution decision.

As one example, Petitioner’s Ground 1B challenges the validity of claims 7 and 14, which depend from independent claims 1 and 10, respectively, and which both additionally recite “wherein [a] variable voltage is an optimum voltage” and

“wherein the optimum voltage is dependent upon both process variation and temperature variation,” as supposedly obvious in view of a combination of Takahashi and a secondary reference Schutz. After a brief discussion of Schutz, Pet., 43-44, the Petition includes a section entitled “Takahashi-Schutz combination,” in which Petitioner argues that a POSITA would have been motivated to combine Takahashi and Schutz, Pet., 44-49, and proposes that “[s]pecifically, a POSITA would have been motivated to employ Schutz’s ‘IC temperature sensor’ to further optimize the ‘source voltages’ from ‘voltage regulator 100’ based on both process variation and temperature variation.” *Id.*, 48. This discussion does not expressly address any analysis of independent claims 1 or 10, except in the assertion that “a POSITA would have understood that other factors including temperature also impact the optimum voltages to provide the ‘device 200’”—an assertion said to be “[a]s explained at Claim 7 of Ground 1A,” *id.*, 47—and in a footnote that states, in its entirety, “[a]s explained at Ground 1A, Takahashi alone renders obvious the features of Claims 7 and 14. However, to the extent that Takahashi fails to independently render obvious those features, Takahashi in combination with Schutz renders obvious optimizing a voltage based on process and temperature variations as recited by Claims 7 and 14.” *Id.*, 46 n.7. The section of Petitioner’s Ground 1B that is specific to claim 7 similarly does not revisit any analysis of claim 1, focusing almost entirely on the role of Schutz in allegedly rendering obvious the “temperature

variation” aspect of claim 7, *see, e.g., id.*, 49-50, while Petitioner’s entire challenge to claim 14 is three words “supra claim 7.” *Id.*, 50-51. Petitioner’s Ground 1B does not, for example, identify any “power islands” in Schutz, or make argument relating any alleged teachings of Schutz to “power islands” in any system.

Petitioner’s Ground 1B thus appears to take for granted the central premise of Petitioner’s Ground 1A—that is, the obviousness of claim 1 in view of Takahashi alone. In particular, none of the arguments advanced in Petitioner’s Ground 1B explain why the proposed combination of Takahashi and Schutz would disclose or render obvious “a plurality of power islands” if Takahashi were not already assumed to do this, and Petitioner’s Ground 1B therefore fails for at least the reasons identified above in connection with Ground 1A.

It is the same with Petitioner’s Ground 1C, which argues that claims 8 and 15 are obvious in view of a combination of Takahashi and the secondary reference Notani. Claim 8 depends from claim 1 and additionally recites “wherein [a] sleep generator comprises a charge pump.” Claim 15 is an independent claim that recites (again, among other things) an optimum voltage “wherein the optimum voltage is generated by a charge pump.” After a two-paragraph overview of Notani, Pet., 51-52, Petitioner’s Ground 1C analysis includes a section entitled “Takahashi-Notani combination,” in which Petitioner argues that a POSITA would have been motivated to combine Takahashi and Notani, *id.*, 52-55, and proposes that a POSITA would

have been “led ... to employ Notani’s charge pump within Takahashi’s ‘voltage regulator’ ...” *Id.*, 53. This discussion expressly refers to Petitioner’s analysis in Ground 1A of obviousness in view of Takahashi alone, *see, e.g., id.*, 53-54; *see also* 53 n.8, focusing instead upon how the “voltage regulator” in Takahashi could additionally and allegedly use a “charge pump” disclosed in Notani. *Id.* Petitioner’s analysis of claim 8 does not include any analysis of limitations already present in claim 1, and Petitioner’s analysis of claim 15 is the single sentence “Supra Claim 8; Ground 1A, Claim 6.” *Id.*, 56. In particular, Petitioner’s Ground 1C does not (for example) identify any “power islands” in Notani, or make argument relating any alleged teachings of Notani to “power islands” in any system. Like Petitioner’s Ground 1B, Petitioner’s Ground 1C thus fails to address—let alone cure—the defects of Petitioner’s Ground 1A regarding Takahashi and “a plurality of power islands.” Petitioner’s Ground 1C thus fails for at least the reasons identified above in connection with Ground 1A.

It is the same with the Petition’s Ground 2B, which argues that claims 8 and 15 are obvious in view of Mizuno and Notani. Like Petitioner’s arguments involving the combination of Takahashi and Notani, Petitioner’s arguments regarding Mizuno and Notani do not expressly address limitations already present in claim 1—except by reference to a single-reference obviousness ground (here Ground 2A instead of Ground 1A), *see, e.g., Pet.*, 94, 94 n.15. So again, for at least the same reasons that

Petitioner's Ground 2A fails, so must Petitioner's Ground 2B.

III. CONCLUSION

For each of the foregoing reasons, the Board should not institute trial.

Respectfully submitted,

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Dated: July 11, 2024

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), counsel for Patent Owner certifies that this document complies with the type-volume limitation of 37 C.F.R. § 42.24(b). According to Microsoft Office Word's word count, this document contains approximately 13,347 words, including any statement of material facts to be admitted or denied in support, and excluding the table of contents, table of authorities, mandatory notices under § 42.8, exhibit list, certificate of service or word count, or appendix of exhibits or claim listing.

Respectfully submitted,

LOWENSTEIN & WEATHERWAX LLP

Dated: July 11, 2024

By: /s/ Granville Kaufman

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CERTIFICATE OF SERVICE

I hereby certify that, pursuant to 37 C.F.R. § 42.6(e) and with the agreement of counsel for Petitioner, true and correct copies of **PATENT OWNER'S PRELIMINARY RESPONSE** and **EXHIBITS 2004-2006** are being served electronically on July 11, 2024, to the persons below:

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