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(12) **United States Patent**
Hoberman et al.

(10) **Patent No.: US 8,854,077 B2**
(45) **Date of Patent: Oct. 7, 2014**

(54) **LOW LEAKAGE AND DATA RETENTION CIRCUITRY**

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(73) Assignee: **Conversant Intellectual Property Management Inc.**, Ottawa, Ontario (CA)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 108 days.

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Related U.S. Application Data

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(51) **Int. Cl.**
H03K 19/17 (2006.01)

(52) **U.S. Cl.**
USPC **326/27**; 326/38; 326/81

(58) **Field of Classification Search**
CPC H03K 19/00361; H03K 19/0016; H03K 17/16
USPC 326/21, 27, 37–41, 80–83
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,781,481 A 7/1998 Iwakiri
5,973,552 A 10/1999 Allan

(Continued)

FOREIGN PATENT DOCUMENTS

DE 198 11 353 C1 7/1999
EP 1 331 736 A1 7/2003

(Continued)

OTHER PUBLICATIONS

Tschanz, James W., et al.,"Dynamic Sleep Transistor and Body Bias for Active Leakage Power Control of Microprocessors", IEEE Journal of Solid-State Circuits, vol. 38, No. 11, Nov. 2003, pp. 1838-1845.

(Continued)

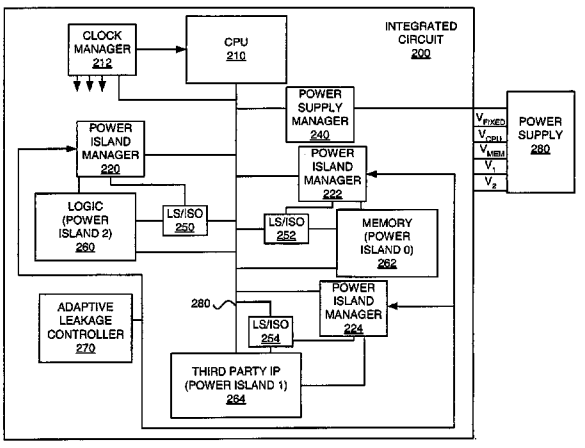
Primary Examiner — Don Le

(74) *Attorney, Agent, or Firm* — Conley Rose, P.C.; J. Robert Brown, Jr.

(57) **ABSTRACT**

An integrated circuit includes first circuitry and sleep transistor circuitry. The first circuitry receives input signals and processes the input signals. The first circuitry also retains data in a sleep state that has low leakage. The sleep transistor circuitry is coupled to the first circuitry and receives a sleep signal that has a negative voltage. The sleep circuitry reduces power consumption of the first circuitry in the sleep state to have low leakage based on the sleep signal while retaining the data in the first circuitry.

18 Claims, 12 Drawing Sheets



(56) **References Cited**

U.S. PATENT DOCUMENTS

6,046,627	A	4/2000	Itoh et al.	
6,144,251	A	11/2000	Ogawa	
6,208,170	B1	3/2001	Iwaki et al.	
6,208,171	B1	3/2001	Kumagai et al.	
6,242,948	B1	6/2001	Makino	
6,246,265	B1	6/2001	Ogawa	
6,288,591	B1	9/2001	Riccio	
6,307,233	B1	10/2001	Awaka et al.	
6,329,874	B1	12/2001	Yc et al.	
6,337,583	B1	1/2002	Ooishi et al.	
6,384,639	B1	5/2002	Chen et al.	
6,414,534	B1	7/2002	Wang et al.	
6,437,623	B1	8/2002	Hsu et al.	
6,437,627	B1	8/2002	Tran et al.	
6,456,110	B1	9/2002	Elamanchili et al.	
6,522,171	B2	2/2003	Hanson et al.	
6,535,433	B2	3/2003	Ooishi	
6,552,601	B1	4/2003	Burr	
6,586,963	B2	7/2003	Choi et al.	
6,598,148	B1	7/2003	Moore et al.	
6,621,306	B2	9/2003	Ooishi et al.	
6,624,687	B1	9/2003	Burr	
6,631,502	B2	10/2003	Buffet et al.	
6,646,492	B2	11/2003	Park et al.	
6,838,901	B2	1/2005	Sakata et al.	
6,864,718	B2	3/2005	Yu	
6,998,895	B2	2/2006	Uvieghara	
7,051,306	B2	5/2006	Hoberman et al.	
7,227,383	B2	6/2007	Hoberman et al.	
7,348,804	B2	3/2008	Hoberman et al.	
7,391,250	B1	6/2008	Chuang	
7,397,721	B2	7/2008	Lee	
7,415,680	B2	8/2008	Hoberman et al.	
7,443,197	B2	10/2008	Hoberman et al.	
7,592,837	B2	9/2009	Hoberman et al.	
7,940,081	B2	5/2011	Hoberman et al.	
7,945,885	B2	5/2011	Hoberman et al.	
8,253,438	B2	8/2012	Hoberman et al.	
2002/0089352	A1	7/2002	Hanson et al.	
2003/0067322	A1	4/2003	Stan et al.	
2003/0103368	A1	6/2003	Arimoto et al.	
2004/0039954	A1	2/2004	White et al.	
2004/0268278	A1	12/2004	Hoberman et al.	
2006/0006929	A1	1/2006	Caplan et al.	
2006/0095807	A1	5/2006	Grochowski et al.	
2007/0176642	A1	8/2007	Kursun et al.	
2008/0180157	A1	7/2008	Choi et al.	
2009/0152948	A1	6/2009	Hoberman et al.	
2010/0031073	A1 *	2/2010	Yeh et al.	713/324
2010/0066439	A1 *	3/2010	Caplan et al.	327/535
2013/0173077	A1 *	7/2013	Ye et al.	700/295

FOREIGN PATENT DOCUMENTS

JP	07105174	A	4/1995
JP	09-261013		10/1997
JP	10-261946		9/1998
JP	11-214962		8/1999
JP	2000-003237		1/2000
JP	2000-013215		1/2000
JP	2001284530	A	10/2001
JP	2002-507852		3/2002
JP	2003-510941		3/2003
WO	9948208	A1	9/1999
WO	WO 01/24364		4/2001

OTHER PUBLICATIONS

Chen, G., et al., "Adaptive Garbage Collection for Battery-Operated Environments," Proceedings of USENIX JVM02 Symposium, Aug. 2002.

Chen, G., et al., "Energy Savings Through Compression in Embedded JavaEnvironments," Proceedings of the CODES'02, Jun. 2002.

Das, K., et al., "Ultra Low-Leakage Power Strategies for Sub-1 V VLSI: Novel Circuit Styles and Design Methodologies for Partially Depleted Silicon-On-Insulator (PD-SOI) CMOS Technology," 16th International Conference on VLSI Design, 2003, pp. 291-296.

De Micheli, G., et al., "System-Level Power Optimization: Techniques and Tools," Date 2000.

Degalahal, V., et al., "Analyzing Soft Errors in Leakage Optimized SRAM Design," Proceedings of 16th International Conference on VLSI Design, Jan. 2003, New Delhi, India.

Delaluz, V., "DRAM Energy Management Using Software and Hardware Directed Power Mode Control," Proceedings of the 7th International Symposium on High Performance Computer Architecture, Jan. 20-24, 2001, Monterrey, Mexico.

Delaluz, V., et al., "Automatic Data Migration for Reducting Energy Consumption in Multi-Bank Memory Systems," DAC 2002, Jun. 10-14, 2002, New Orleans, LA, USA.

Delaluz, V., et al., "Hardware and Software Techniques for Controlling DRAM Power Modes," IEEE Transaction on Computers, Nov. 2001, vol. 50.

Delaluz, V., et al., "Scheduler-Based DRAM Energy Management," DAC 2002, Jun. 10-14, 2002, New Orleans, LA, USA, ACM.

Duarte, D., et al., "A Complete Phase-Locked Loop Power Consumption Model," Proceedings of the 2002 Design, Automation and Test in Europe Conference and Exhibition (DATE'02), 2002, IEEE.

Duarte, D., et al., "Evaluating Run-Time Techniques for Leakage Power Reduction," Proceedings of the 15th International Conference on VLSI Design (VLSID'02) 2002, IEEE.

Duarte, D., et al., "Impact of Scaling on the Effectiveness of Dynamic Power Reduction Schemes," Proceedings of the 20th International Conference on Computer Design (ICCD), Sep. 16-18, 2002, Freiberg, Germany.

Duarte, D., et al., "Impact of Technology Scaling and Packaging on Dynamic Voltage Scaling Techniques," Proceedings of the 15th Annual IEEE International ASIC/SOC Conference, Sep. 25-28, 2002, Rochester, NY.

Duarte, D., et al., "Impact Technology Scaling in the Clock System Power," Proceedings of the IEEE Computer Society Annual Symposium on VLSI, Apr. 25-26, 2002, Pittsburgh, PA.

Filseth, E., "Tally Power into Cost of 'Free' Silicon," EETimes, Jan. 11, 1999, located at http://www.eetimes.com/story/speakout/OEG19990111S028.

Flynn, J., et al., "Power Management in Complex SoC Design," Synopsys, Apr. 2004, located at http://www.synopsys.com/sps.

Frenkil, J., "A Multi-Level Approach to Low-Power IC Design," IEEE Spectrum, Feb. 1998, Vo. 35, No. 2.

Grunwald, D., et al., "Kool Chips Workshop," MICRO33, Dec. 10, 2000, Monterey, CA.

Gupta, R., et al., "Low Power Wireless Networked System Design," HotChips, Aug. 18, 2002, Stanford, CA.

Halter, J., et al., "A Gate-Level Leakage Power Reduction Method for Ultra-Low-Power CMOS Circuits," IEEE Customs Integrated Circuits Conference, 1997, pp. 475-478.

Hezavei, J., et al., "Input Sensitive High-Level Power Analysis," Proceedings of the 2001 IEEE Workshop on Signal Processing Systems (SiPS), Sep. 2001, pp. 149-156.

Horiguchi, M., et al., "Switched-Source-Impedance CMOS Circuit for Low Standby Subthreshold Current Giga-Scale LSI's," IEEE Journal of Solid-State Circuits, vol. 28, No. 11, Nov. 1993, pp. 1131-1135.

Hu, J.S., et al., "Using Dynamic Branch Behavior for Power-Efficient Instruction Fetch," Proc. of IEEECS Annual Symposium on VLSI (ISVLSI 2003), Feb. 20-21, 2003, Tampa, FL.

Inukai, T., et al., "Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration," Custom Integrated Circuits Conference, 2000.CICC.Proceedings of the IEEE 2000, pp. 409-412.

Kao, J., et al., "Dual-Threshold Voltage Techniques for Low-Power Digital Circuits," IEEE Journal of Solid-State Circuits, vol. 35, No. 7, Jul. 2000, pp. 1009-1018.

Kawaguchi, H., et al., "A CMOS Scheme for 0.5V Supply Voltage with Pico-Ampere Standby Current," Solid-State Circuits Conference 1998. Digest of Technical Papers. 45th ISSCC 1998 IEEE International, Feb. 5-7, 1998, pp. 192-193.

(56) **References Cited**

OTHER PUBLICATIONS

Kawaguchi, H., et al., "A Super Cut-Off CMOS (SCCMOS) Scheme for 0.5 V Supply Voltage with Picoampere Stand-By Current," IEEE Journal of Solid-State Circuits, vol. 35, No. 10, Oct. 2000, pp. 1498-1501.

Kim, S., et al., "Energy Efficient Instruction Cache Using Page-Based Placement," Proceedings of the International Conference on Compilers, Architectures and Synthesis for Embedded Systems, CASES'01, Nov. 1-17, 2001, Atlanta, GA, USA.

Kim, S., et al., "Partitioned Instruction Cache Architecture for Energy Efficiency," ACM Transactions on Computational Logic, Jul. 2002, pp. 1-23, vol. V, No. N.

Kim, S., et al., "Power-aware Partitioned Cache Architectures," Proceedings of ACM/IEEE International Symposium on Low Power Electronics and Design, 2001, ILSPED'01, Aug. 6-7, 2001, Huntington Beach, CA.

Kim, S., et al., "Predictive Precharging for Bitline Leakage Energy Reduction," Proceedings of 15th Annual IEEE International ASIC/SOC Conference, Sep. 25-28, 2002, Rochester, NY.

Lackey, D., et al., "Managing Power and Performance for System-on-Chip Designs using Voltage Islands," Computer Aided Design, 2002, ICCAD 2002.IEEE/ACM International Conference on Nov. 10-14, 2002, pp. 195-202.

Li L., et al., "Managing Leakage Energy in Cache Hierarchies," Journal of Instruction-Level Parallelism, 2003, pp. 1-24, vol. 5.

Li, L., et al., "Leakage Energy Management in Cache Hierarchies," 11th International Conference on Parallel Architectures and Compilation Techniques (PACT'02), Sep. 2002.

"Managing Power in Ultra Deep Submicron ASIC/IC Design," May 2002, Synopsys, Inc.

Manne, S., et al., "Kool Chips Tutorial," 32nd Annual International Symposium on Microarchitecture, Nov. 15, 1999, Haifa, Israel.

Matsuya, et al., "0.5 μm Low-Voltage-Supply Full-Custom LSI Design Technology," *NTT R&D*, vol. 43, No. 3, pp. 29-38 (1994).

Mutoh, S., et al., "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS," IEEE Journal of Solid-State Circuits, vol. 30, No. 8, Aug. 1995, pp. 847-854.

Nose, K., et al., "VTH-Hopping Scheme to Reduce Subthreshold Leakage for Low-Power Processors," IEEE Journal of Solid-State Circuits, vol. 37, No. 3, Mar. 2002, pp. 413-415.

Pangrle, B., "Low Power Design: A Holistic Approach in an Era of New Semiconductor Technologies," San Diego Telecom Council Semiconductor SIG, Nov. 14, 2002.

Rabaey, J., "Design Aids for Low Power: Part II Architecture and System Levels," 1997.

Ramanarayanan, R., et al., "Characterizing Dynamic and Leakage Power Behavior in Flip Flops," Proceedings of the 15th Annual IEEE International ASIC/SOC Conference, Sep. 2002.

Roy, K., et al., "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits," Proceedings of the IEEE, Feb. 2000, pp. 305-327, vol. 91, No. 2, IEEE.

Supplementary European Search Report for Application No. PCT/US2005/001938, dated Apr. 22, 2009.

Tsai, Y-F, et al., "Implication of Technology Scaling on Leakage Reduction Techniques," DAC 2003, Jun. 2-6, 2003, ACM, Anaheim, CA, USA.

Zhang, W., "Exploiting VLIW Schedule Slacks for Dynamic and Leakage Energy Reduction," Proceedings of the 34th Annual International Symposium on Microarchitecture (MICRO'01), Dec. 2001.

Zhang, W., et al., "Compiler Support for Reducing Leakage Energy Consumption," Proceedings of the 6th Design Automation and Test in Europe Conference (Date-03), Mar. 2003, Munich, Germany.

Zhang, Z., et al., "Active Leakage Control with Sleep Transistors and Body Bias," www.eecs.berkeley.edu/~zyzhang/ee241/final.pdf.

Japanese Rejection Decision; Application No. 2011-217253; Oct. 22, 2013; 3 pages.

* cited by examiner

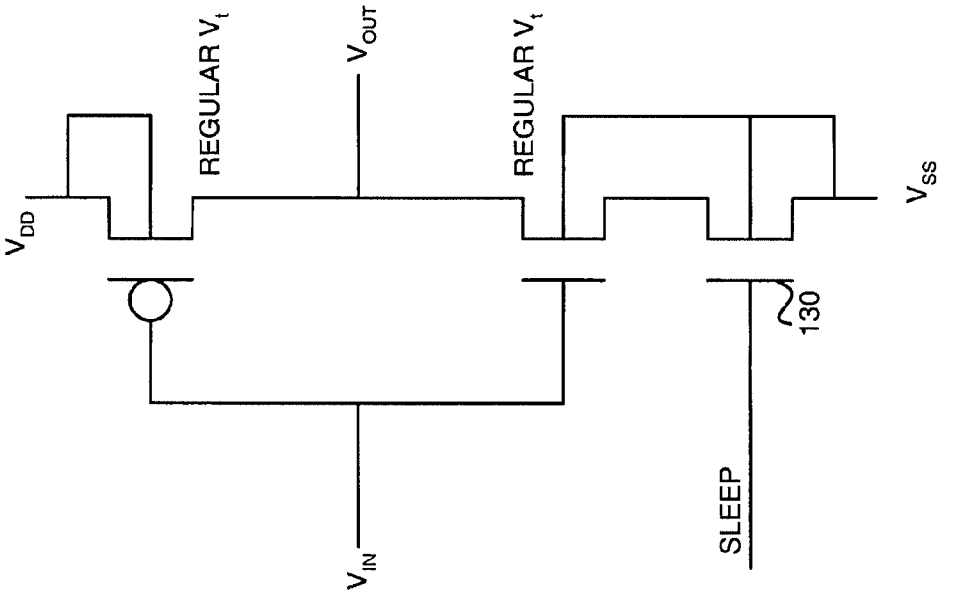


FIG. 1
PRIOR ART

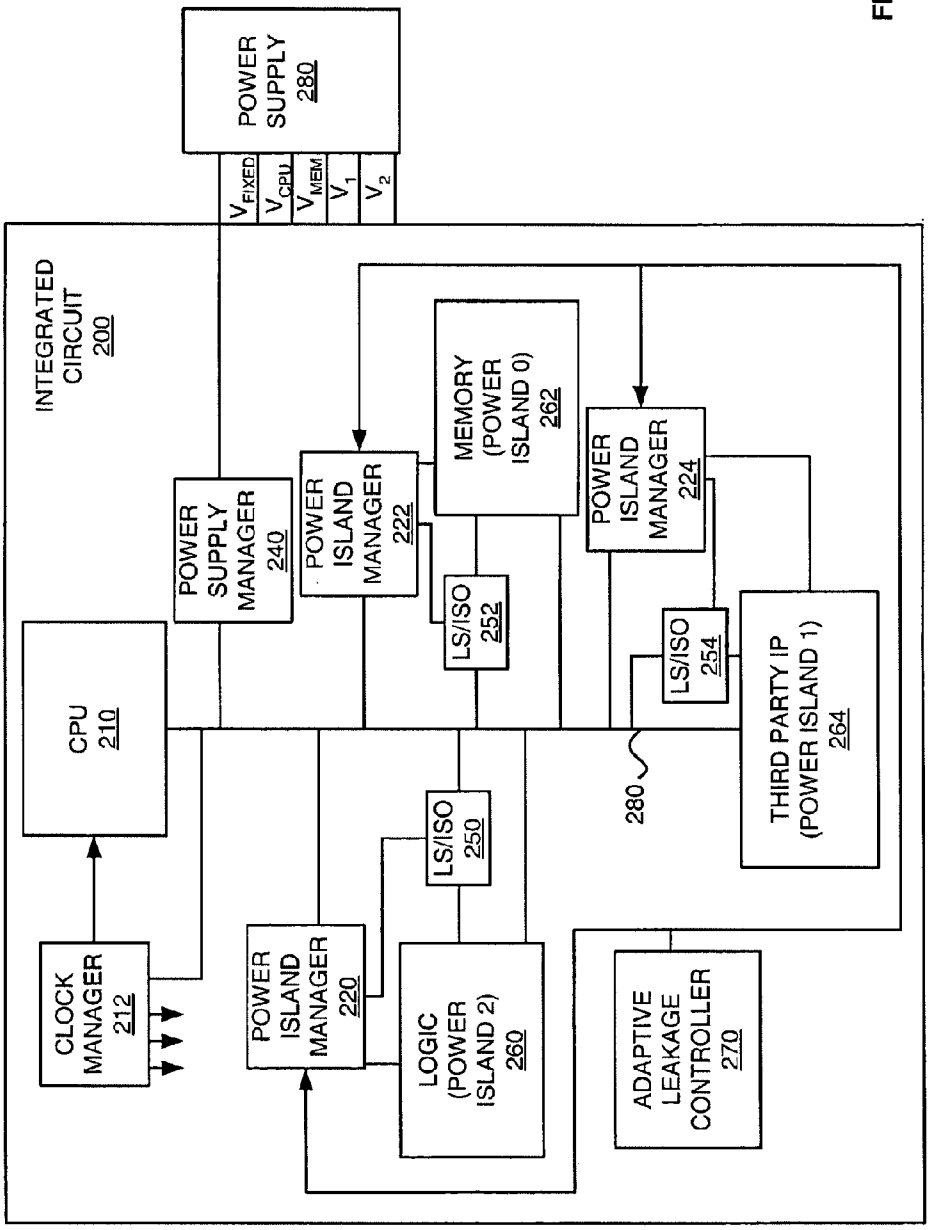

POWER SUPPLY 280
V_{FIXED}
V_{CPU}
V_{MEM}
V_1
V_2
INTEGRATED CIRCUIT 200
MEMORY (POWER ISLAND 0) 262
POWER SUPPLY MANAGER 240
POWER ISLAND MANAGER 222
POWER ISLAND MANAGER 224
LS/ISO 252
LS/ISO 254
CPU 210
THIRD PARTY IP (POWER ISLAND 1) 264
280
LS/ISO 250
CLOCK MANAGER 212
POWER ISLAND MANAGER 220
LOGIC (POWER ISLAND 2) 260
ADAPTIVE LEAKAGE CONTROLLER 270

FIG. 2

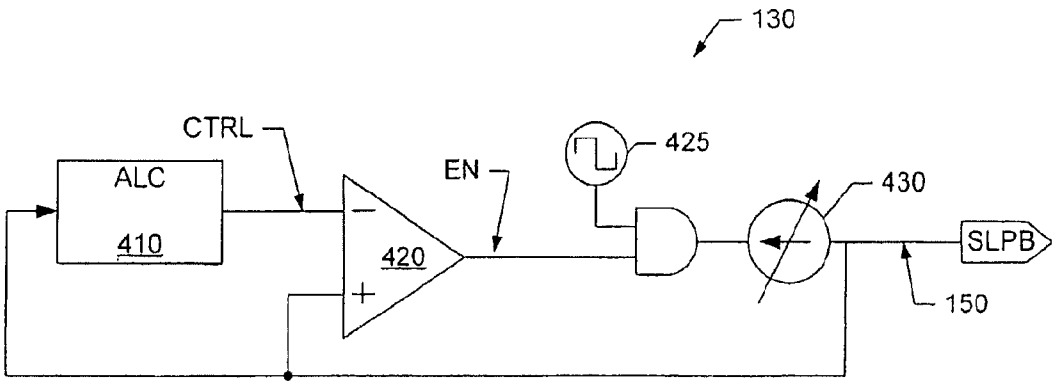


FIG. 2A

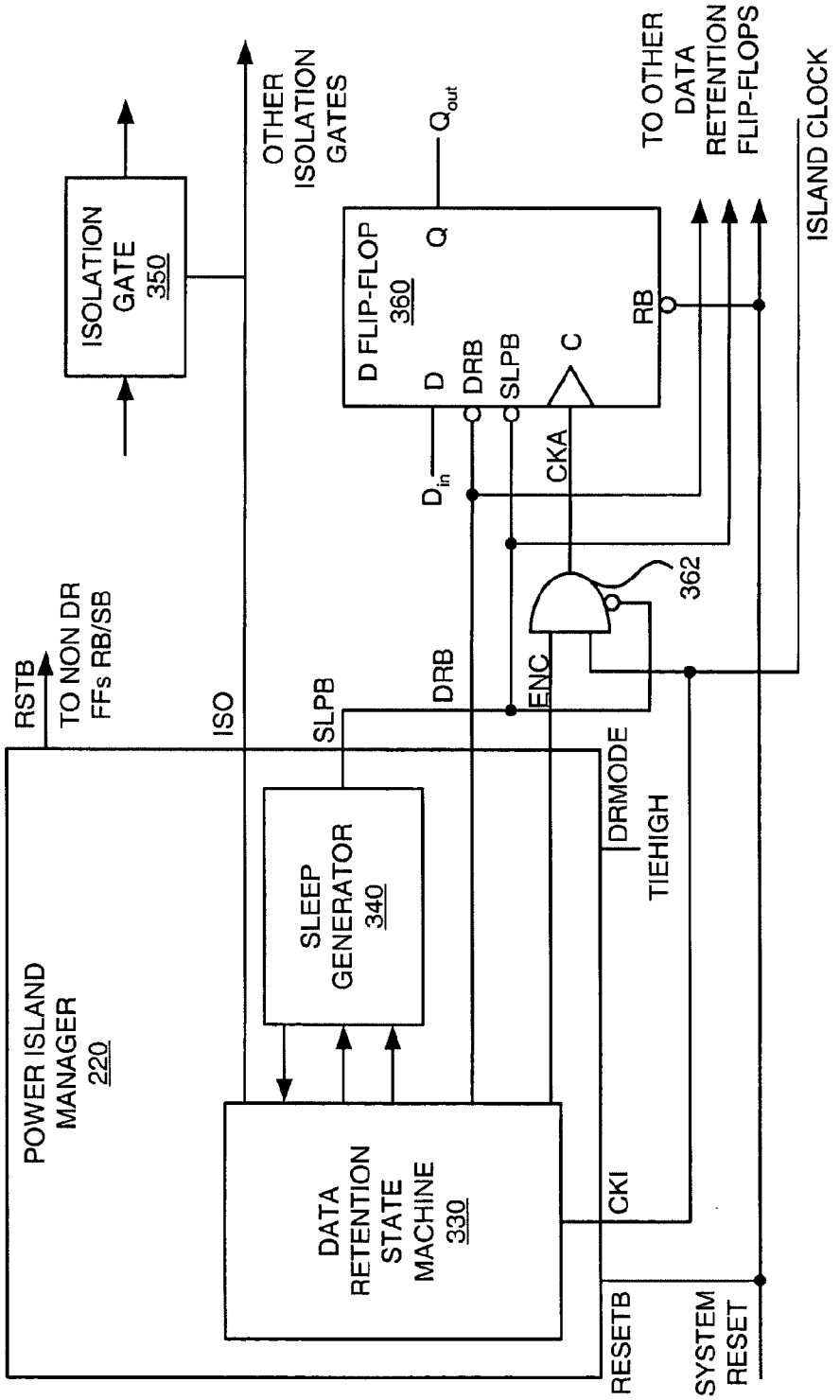

ISOLATION GATE 350
OTHER ISOLATION GATES
Q_{out}
TO OTHER DATA RETENTION FLIP-FLOPS
ISLAND CLOCK
D FLIP-FLOP 360
Q
D
DRB
SLPB
C
RB
D_{in}
CKA
362
RSTB
TO NON DR FFs RB/SB
ISO
SLPB
DRB
ENC
DRMODE
TIEHIGH
POWER ISLAND MANAGER 220
SLEEP GENERATOR 340
DATA RETENTION STATE MACHINE 330
CKI
RESETB
SYSTEM RESET

FIG. 3

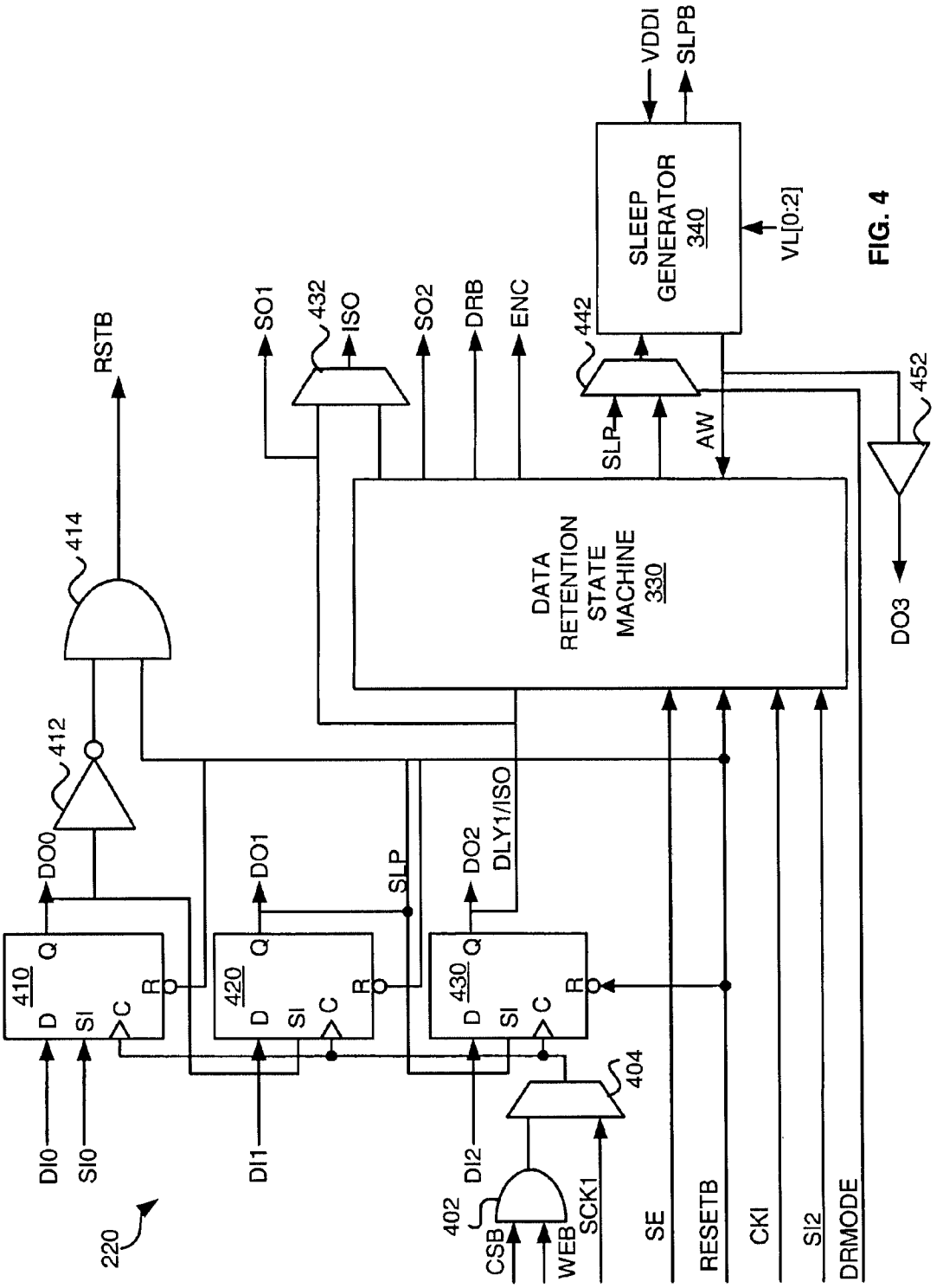

VDDI
SLPB
SLEEP GENERATOR 340
VL[0:2]
442
452
SO1
432
ISO
SO2
DRB
ENC
RSTB
SLP
AW
DATA RETENTION STATE MACHINE 330
DO3
414
412
DO0
DO1
SLP
DO2
DLY1/ISO
410
420
430
Q
D
SI
C
R
404
DI0
SI0
DI1
DI2
402
CSB
WEB
SCK1
SE
RESETB
CKI
SI2
DRMODE
220

FIG. 4

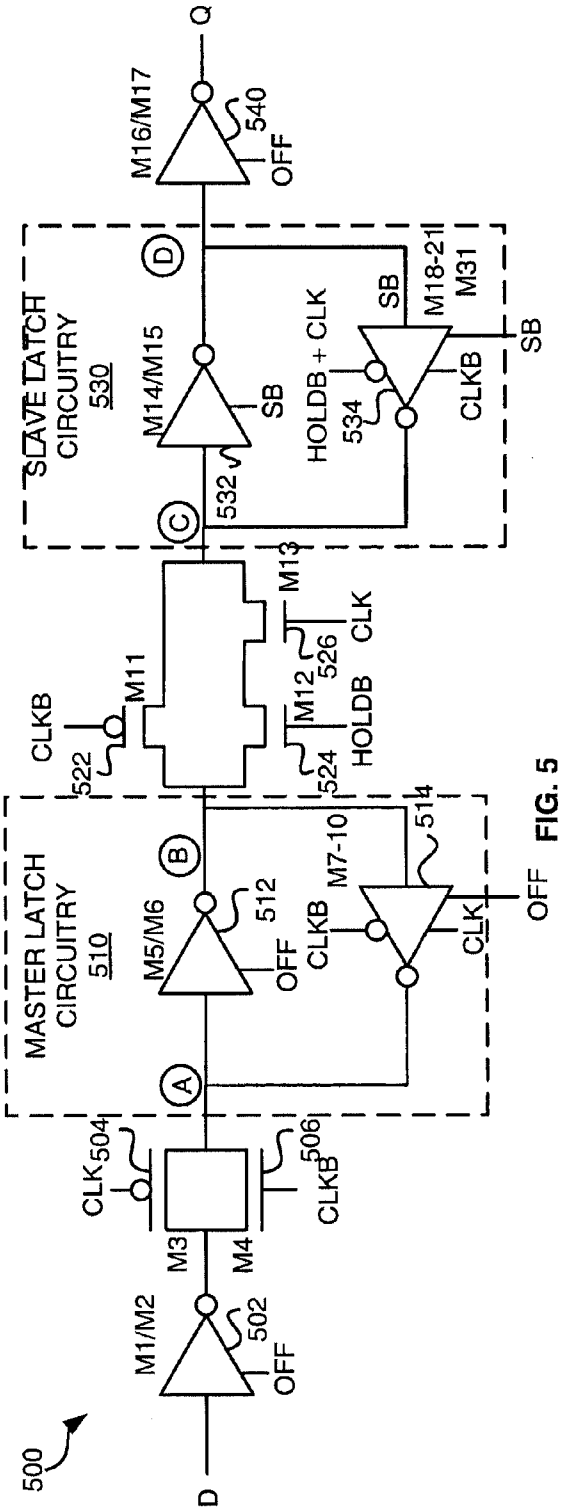

Q
M16/M17
540
OFF
SLAVE LATCH CIRCUITRY 530
D
M14/M15
SB
HOLDB + CLK
534
M18-21
M31
SB
CLKB
532
C
M13
CLK
526
M12
HOLDB
524
CLKB
522
M11
MASTER LATCH CIRCUITRY 510
B
M5/M6
512
OFF
CLKB
M7-10
514
CLK
OFF
A
CLK
504
CLKB
506
M3
M4
M1/M2
502
OFF
500
D

FIG. 5

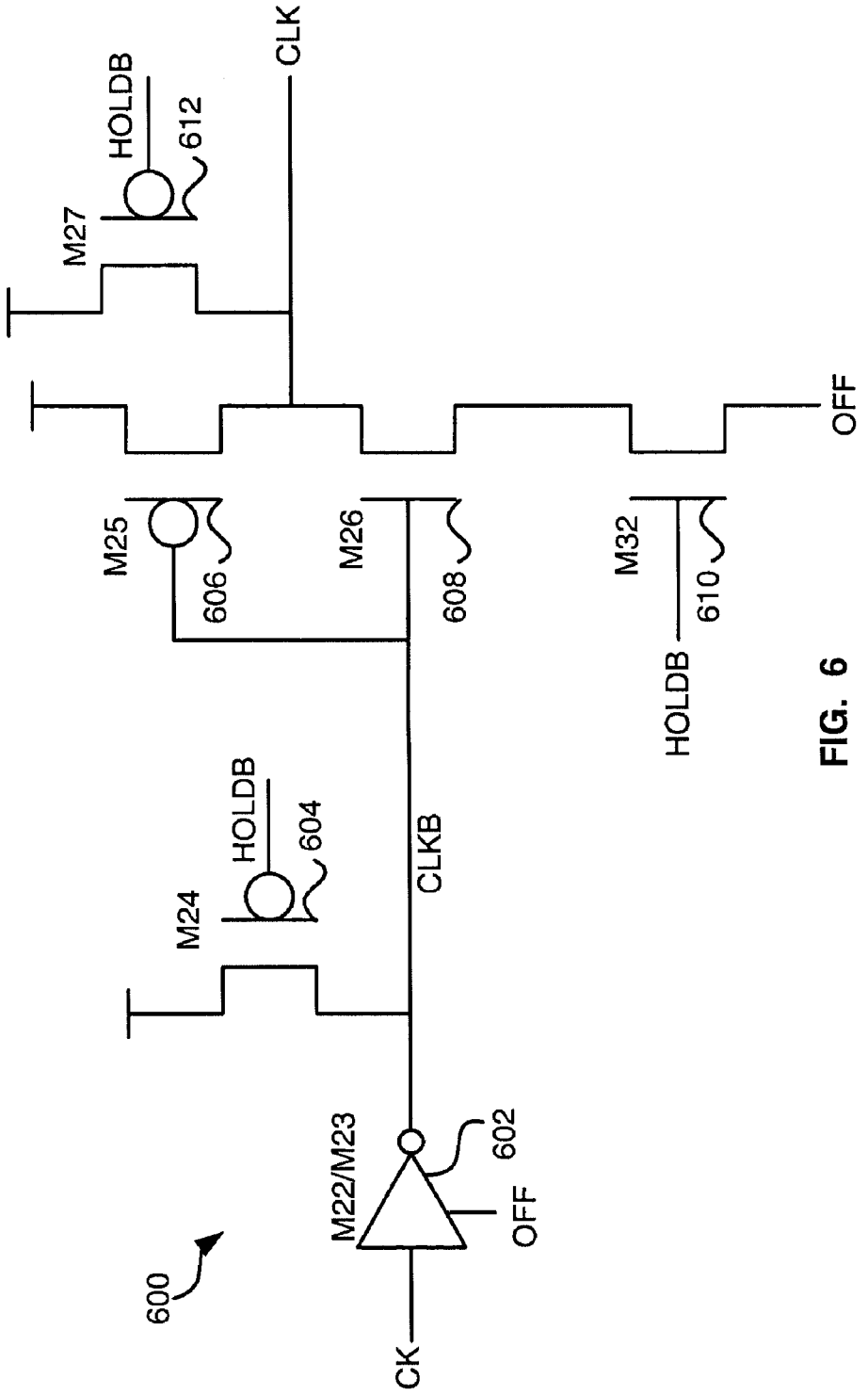

CLK
HOLDB
612
M27
OFF
M25
606
M26
608
M32
610
HOLDB
HOLDB
604
M24
CLKB
M22/M23
602
OFF
600
CK

FIG. 6

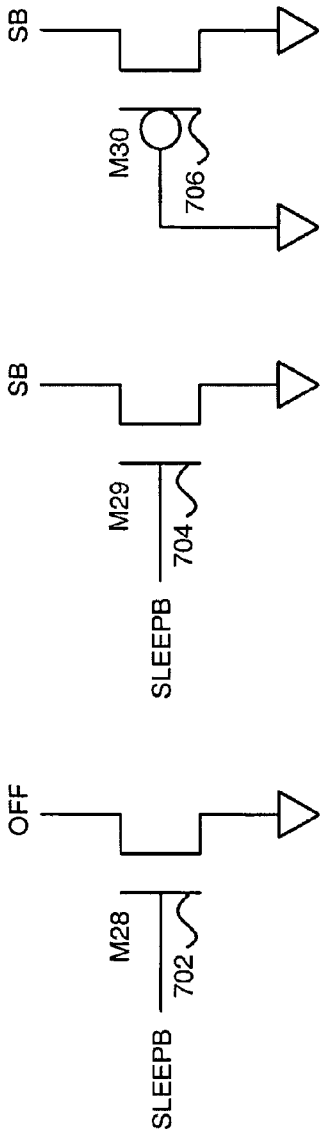


FIG. 7A

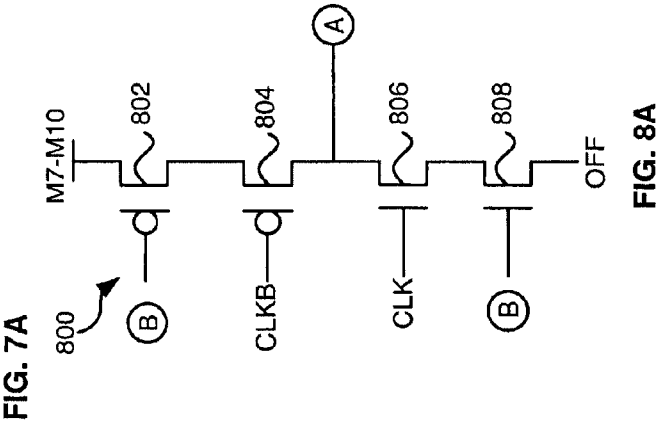


FIG. 7B

FIG. 7C

FIG. 8A

FIG. 8B

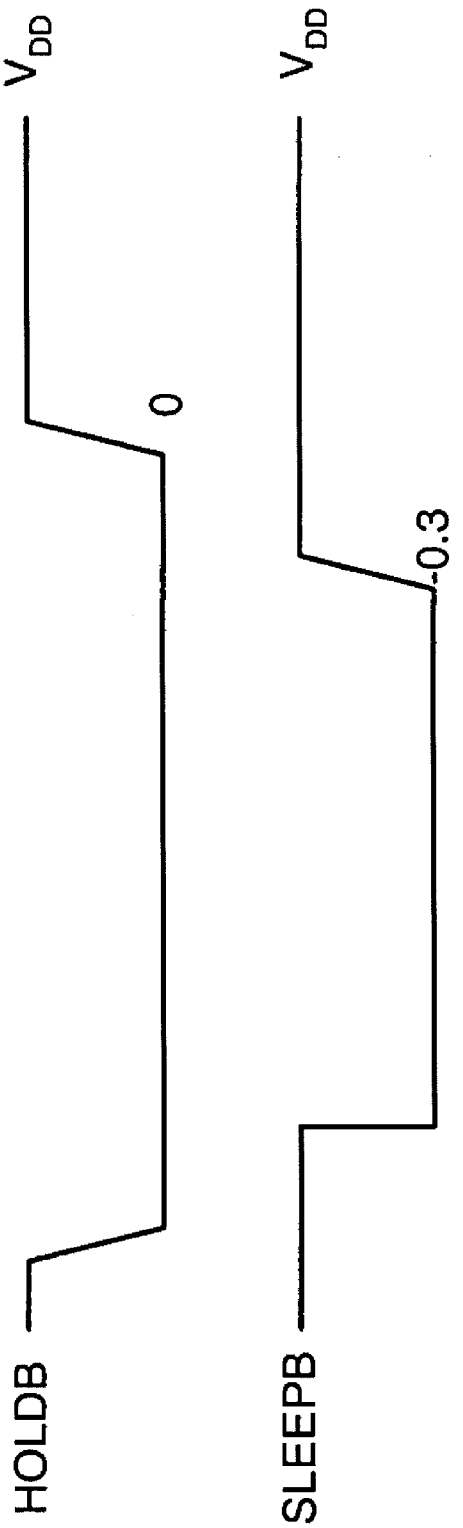


FIG. 9

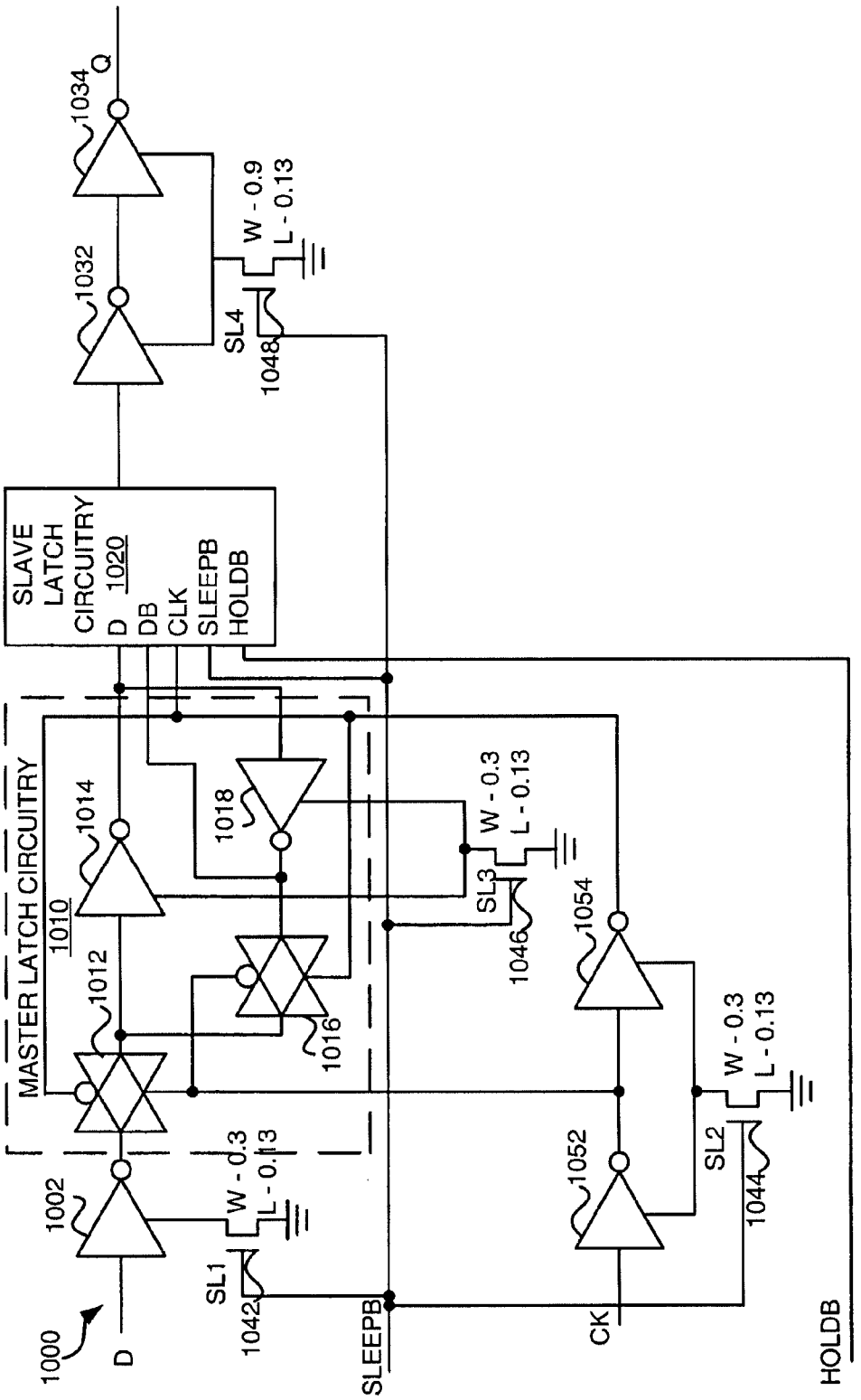

1034
Q
1032
W - 0.9
L - 0.13
SL4
1048
SLAVE LATCH CIRCUITRY
D 1020
DB
CLK
SLEEPB
HOLDB
MASTER LATCH CIRCUITRY
1010
1014
1018
W - 0.3
L - 0.13
SL3
1046
1054
1012
1016
1002
W - 0.3
L - 0.13
1052
SL2
1044
SL1
1042
1000
D
SLEEPB
CK
HOLDB

FIG. 10

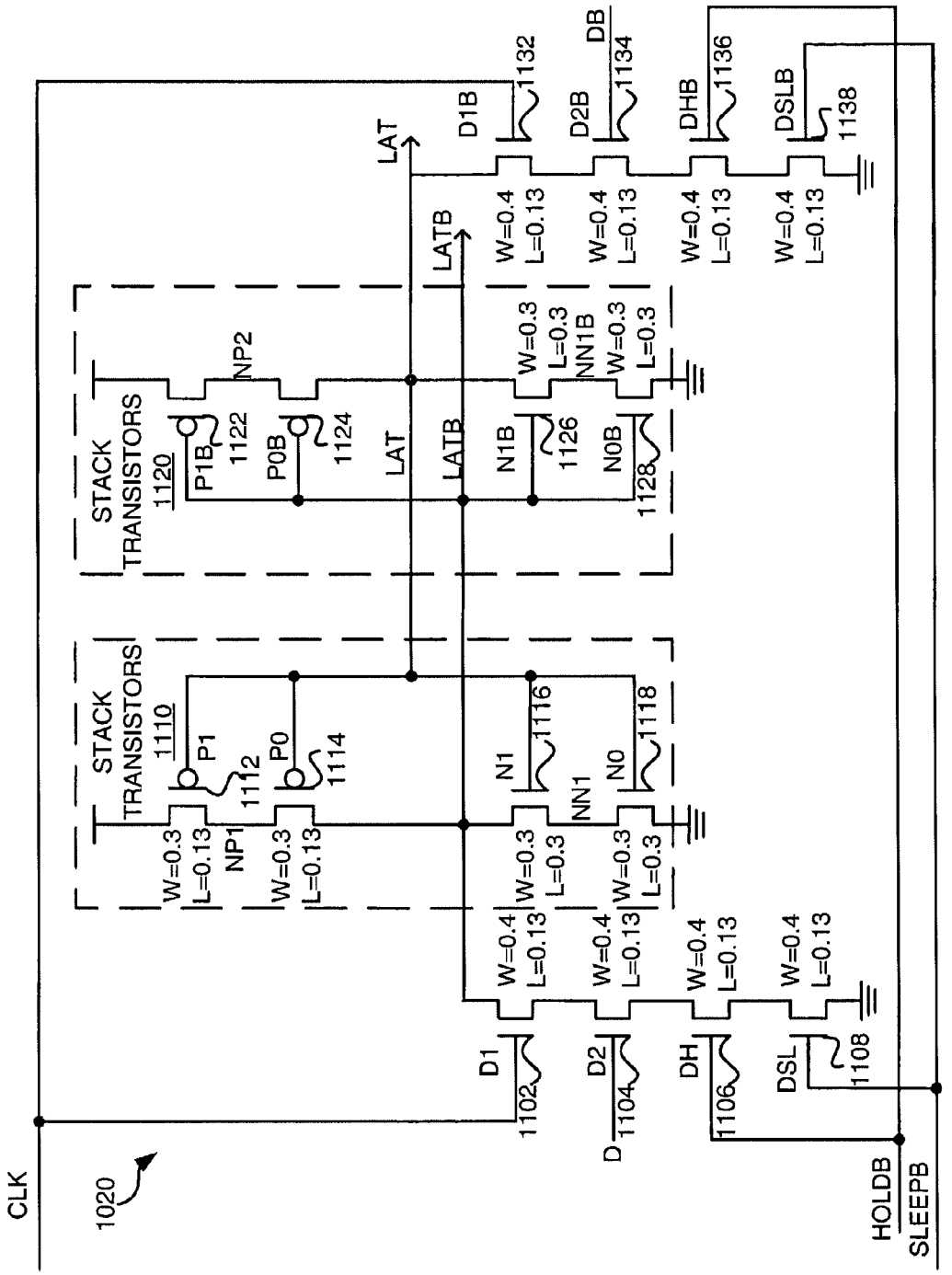

CLK
1020
D1
1102
D2
1104
D
DH
1106
DSL
1108
HOLDB
SLEEPB
STACK TRANSISTORS 1110
P1
1112
P0
1114
N1
1116
N0
1118
NN1
NP1
W=0.3 L=0.13
W=0.3 L=0.3
W=0.4 L=0.13
STACK TRANSISTORS 1120
P1B
1122
P0B
1124
N1B
1126
N0B
1128
NN1B
NP2
LAT
LATB
D1B
1132
D2B
DB
1134
DHB
1136
DSLB
1138

FIG. 11

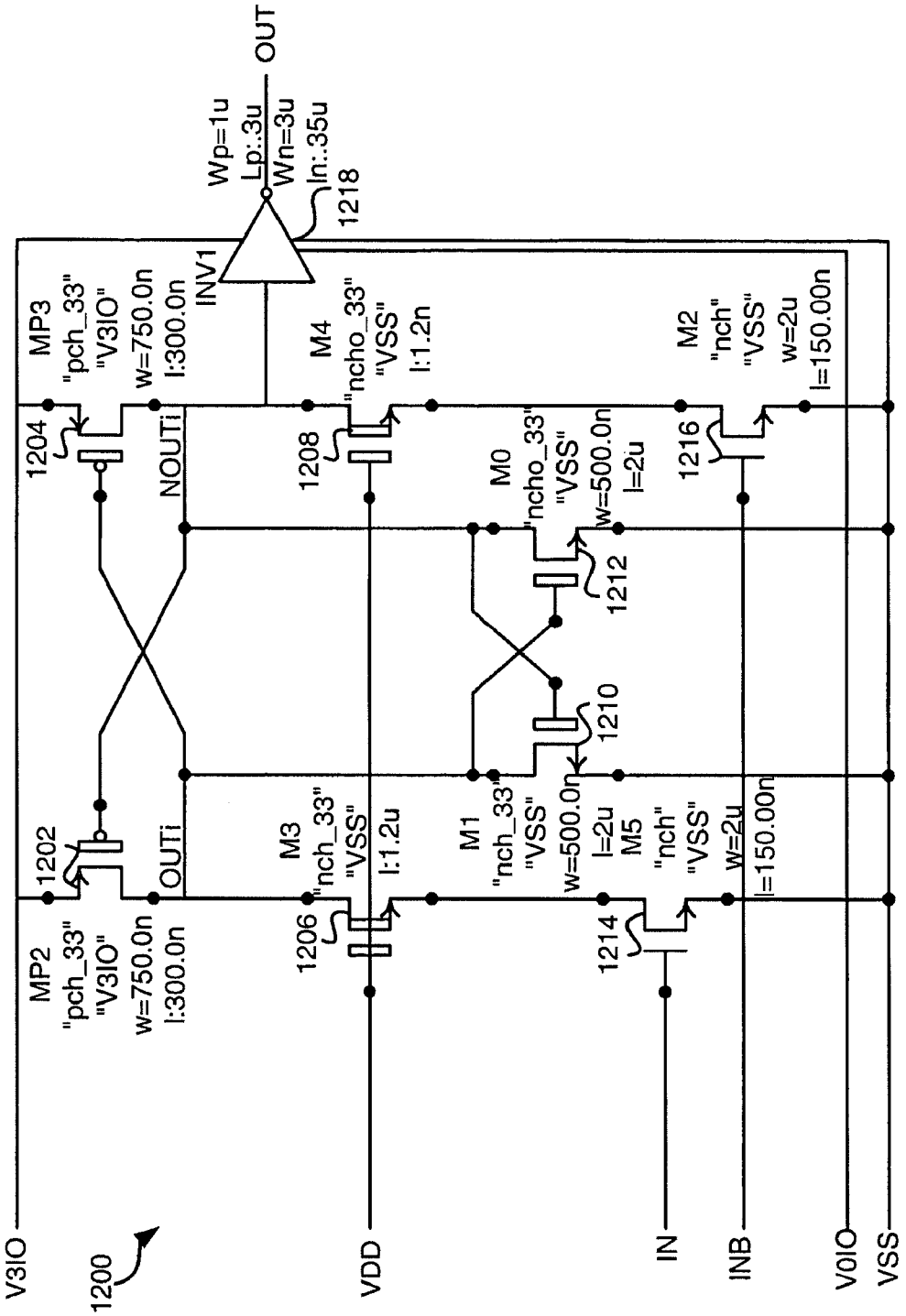

OUT
Wp=1u
Lp:.3u
Wn=3u
ln:.35u
1218
INV1
MP3
"pch_33"
"V3IO"
w=750.0n
l:300.0n
M4
"ncho_33"
"VSS"
l:1.2n
M2
"nch"
"VSS"
w=2u
l=150.00n
1204
NOUTi
1208
M0
"ncho_33"
"VSS"
w=500.0n
l=2u
1216
1212
1210
1202
OUTi
M3
"nch_33"
"VSS"
l:1.2u
M1
"nch_33"
"VSS"
w=500.0n
l=2u
M5
"nch"
"VSS"
w=2u
l=150.00n
MP2
"pch_33"
"V3IO"
w=750.0n
l:300.0n
1206
1214
V3IO
1200
VDD
IN
INB
V0IO
VSS

FIG. 12

LOW LEAKAGE AND DATA RETENTION CIRCUITRY

RELATED APPLICATIONS

This application is a continuation of U.S. application Ser. No. 13/074,291, filed Mar. 29, 2011 now U.S. Pat. No. 8,253,438, which is a continuation of U.S. application Ser. No. 12/542,352, filed Aug. 17, 2009 (now U.S. Pat. No. 7,940,081), which is a continuation of U.S. application Ser. No. 12/284,311, filed Sep. 19, 2008 (now U.S. Pat. No. 7,592,837), which is a continuation of U.S. application Ser. No. 11/998,725, filed Nov. 30, 2007 (now U.S. Pat. No. 7,443,197), which is a continuation of U.S. application Ser. No. 11/732,181, filed Apr. 2, 2007 (now U.S. Pat. No. 7,348,804), which is a divisional and claims the priority benefit of U.S. application Ser. No. 11/041,687 filed Jan. 20, 2005 (now U.S. Pat. No. 7,227,383), which claims the priority benefit of U.S. Provisional Application No. 60/546,574, filed Feb. 19, 2004 and U.S. Provisional Application No. 60/586,565, filed Jul. 9, 2004.

The entire teachings of the above applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to integrated circuits, and more particularly to low leakage and data retention circuitry.

2. Description of the Related Art

Most integrated circuits have a design goal to reduce the overall power consumption. The total power consumed by an integrated circuit includes dynamic power consumption and standby leakage current consumption. The challenge in designing an integrated circuit is to reduce the dynamic power and leakage power, while maintaining performance and cost goals for the integrated circuit.

In complementary metal oxide semiconductors (CMOS), various types of leakage occur such as pn junction reverse-bias current, subthreshold leakage, oxide tunneling current, gate current due to hot-carrier injection, gate-induced drain leakage, and channel punch through current. When the threshold voltage for a CMOS transistor is reduced for higher performance, the leakage power is significant in the total power consumption of the CMOS circuit.

There are two approaches in reducing the leakage power for CMOS circuits. The first approach is a process level technique that controls the doping profile of the transistor. The other approach is a circuit level technique where voltages at the different device terminals such as the drain, source, gate, and body are controlled. Some circuit level techniques are discussed below.

One circuit level technique is stacking transistors, which is also called self-reverse bias. When more than one transistor in a stack of series-connected transistors is turned off, the subthreshold leakage current is reduced. One problem with the transistor stack is that only a three times reduction in leakage current is achieved. Another circuit level technique is a multiple threshold voltage design. Both high- and low-threshold transistors are on the same chip to deal with the leakage problem. The high-threshold transistors suppress the subthreshold leakage current. The low-threshold transistors are used to achieve higher performance. One problem with a multiple threshold design is that process complexity and costs are increased.

Another circuit level technique is a multiple body bias in which the body voltage is changed to modify the threshold voltage. If separate body biases are applied to different NMOS transistors, the transistor cannot share the same well, which requires triple well technologies. One problem is that well biasing consumes a lot of chip area and requires extra power supplies for each cell. This technique also increases process complexity and the leakage reduction is not optimal.

Another technique for reducing leakage is a sleep transistor. FIG. **1** depicts prior art circuitry including a sleep transistor. For NMOS sleep transistors, one or more NMOS transistors are added to logic gates in series with the cell transistors to VSS. The NMOS sleep transistors act as a switch to turn on and off the logic gate. In FIG. **1**, the sleep transistor **130** is turned on (gate to VDD) during normal cell operation. When the cell is idle, the sleep transistor **130** is turned off (gate tied to VSS) to reduce the leakage current of the cell. Sleep transistors can also be PMOS transistors. One problem with sleep transistors is that if all logic has sleep transistors, the logic will lose their state information.

SUMMARY OF THE INVENTION

In an exemplary embodiment of the presently disclosed invention, a data retention circuit is provided. The exemplary circuit includes an input/output pad cell that itself includes level shifter circuitry, the level shifter circuitry having inputs and outputs. Output latching circuitry is also provided as a part of the data retention circuit. The output latching circuitry includes two transistors. The transistors are coupled to the outputs of the level shifter circuitry and retain a state of the level shifter circuitry based on the state of the inputs. A leakage optimization circuit is also included, the leakage optimization circuit is configured to simultaneously decrease leakage power in conjunction with the state retention of the output latching circuitry.

In another embodiment of the presently disclosed invention, a system for controlling power consumption within an integrated circuit is disclosed. The system includes a power island, the power island includes a first circuit. The first circuit of the power island is configured to receive an input signals and a hold signal. The circuit is further configured to process the input signals and retain data in a sleep state having low leakage. The first circuit is further configured to retain the data based on the hold signal. The system further includes a sleep transistor, which is coupled to the first circuit. The sleep transistor is configured to receive a negative voltage sleep signal and reduce power consumption of the first circuit in the sleep state. As a result, the first circuit has low leakage based on the sleep signal while simultaneously retaining the data.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing will be apparent from the following more particular description of example embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating embodiments of the present invention.

FIG. **1** is an illustration of circuitry including a sleep transistor in the prior art;

FIG. **2** is an illustration of an integrated circuit with a power supply in an exemplary implementation of the invention;

FIG. **2**A is a block diagram of a leakage manager system for minimizing state leakage of a logic gate by application of a negative voltage to a sleep transistor.

FIG. **3** is an illustration of a power island manager with an isolation gate and a D flip-flop in an exemplary implementation of the invention;

FIG. **4** is an illustration of a power island manager in an exemplary implementation of the invention;

FIG. **5** is an illustration of a D/Q portion of flip-flop circuitry in an exemplary implementation of the invention;

FIG. **6** is an illustration of a CK portion of flip-flop circuitry in an exemplary implementation of the invention;

FIG. **7**A is an illustration of a sleep transistor for an OFF node in an exemplary implementation of the invention;

FIG. **7**B is an illustration of a sleep transistor for an SB node in an exemplary implementation of the invention;

FIG. **7**C is an illustration of a moderate impedance transistor for an SB node in an exemplary implementation of the invention;

FIG. **8**A is an illustration of circuitry for a tristate inverter in the master latch in an exemplary implementation of the invention;

FIG. **8**B is an illustration of circuitry for a tristate inverter in the slave latch in an exemplary implementation of the invention;

FIG. **9** is an illustration of a HOLDB and SLEEPB signals in an exemplary implementation of the invention;

FIG. **10** is an illustration of circuitry for low leakage and data retention in an exemplary implementation of the invention;

FIG. **11** is an illustration of slave latch circuitry in an exemplary implementation of the invention; and

FIG. **12** is an illustration of circuitry for a level shifter for an I/O pad in an exemplary implementation of the invention.

DETAILED DESCRIPTION OF THE INVENTION

A description of example embodiments of the invention follows.

As shown in the exemplary drawings wherein like reference numerals indicate like or corresponding elements among the figures, exemplary embodiments of a system and method according to the present invention are described below in detail. It is to be understood, however, that the present invention may be embodied in various forms. Therefore, specific details disclosed herein are not to be interpreted as limiting, but rather as a basis for the claims and as a representative basis for teaching one skilled in the art to employ the present invention in virtually any appropriately detailed system, structure, method, process or manner.

Power Island Manager—FIGS. **2-4**

In some embodiments, an integrated circuit can be delineated into power islands. Power consumption can then be controlled within the power island. A power island manager provides control signals to the power island to control power consumption of the power island. In some embodiments, the low leakage, data retention circuitry is located within the power islands.

FIG. **2** depicts an illustration of an integrated circuit **200** with a power supply **280** in an exemplary implementation of the invention. The integrated circuit **200** includes a central processing unit (CPU) **210**, a clock manager **212**, power island managers **220**, **222**, and **224**, a power supply manager **240**, level shifter/isolation gates (LS/ISO) **250**, **252**, and **254**, logic (power island **2**) **260**, memory (power island **0**) **262**, third party intellectual property (IP) (power island **1**) **264**, adaptive leakage controller (ALC) **270**, and bus **280**.

A power island is any section, delineation, partition, or division of an integrated circuit where power consumption is controlled within the section, delineation, partition, or division. In some embodiments, the power islands are delineated based on geographic factors of the integrated circuit. In some embodiments, the power islands are delineated based on functional IP units of the integrated circuit **200**. In this example depicted in FIG. **2**, power islands are delineated by memory **262**, logic **260**, and third party IP **264**. Power islands are discussed in further detail in pending U.S. application Ser. No. 10/840,893 entitled "Managing Power on Integrated Circuits Using Power Islands" filed on May 7, 2004, which is hereby incorporated by reference.

The power island managers **220**, **222**, and **224** are any circuitry, device, or system configured to provide control signals to a power island to control power within the power island. The power island managers **220**, **222**, and **224** can dynamically change the power consumption of the power islands based on the needs and operation of the integrated circuit **200**. The power island managers **220**, **222**, **224** may select a clock, change clock frequency, or modify the voltage within the power island to control the power consumption of the power island.

The ALC **270** provides control signals to compensate for process and temperature variation to provide the optimum voltage to be applied to sleep transistors in the power islands. The ALC **270** is described in further detail U.S. patent application Ser. No. 10/996,739 entitled "Systems and Methods for Minimizing Static Leakage of an Integrated Circuit" filed on Nov. 17, 2004.

FIG. **2**A is a block diagram of a leakage manager system **290** for minimizing static leakage of a logic gate by application of a negative voltage to a sleep transistor in accordance with an example embodiment. The leakage manager system **290** comprises an adaptive leakage controller (ALC) **291**, a negative voltage regulator **292**, and a charge pump **294**. The charge pump **294** generates a negative voltage **295** (SLPB). The ALC **291** determines whether to adjust the negative voltage **295**. The ALC **291** generates a signal (depicted as CTRL) depending on the determination. The negative voltage regulator **292** adjusts the negative voltage **295** depending on the CTRL signal.

As described further herein, the negative voltage regulator **292** of one embodiment generates an enable (EN) signal to the charge pump **294** to enable the charge pump **294** to increase the magnitude of the negative voltage **295** (i.e., to make the negative voltage **295** more negative). If the EN signal is low, an alternating signal from an oscillator **293** to the charge pump **294** is disabled, preventing the charge pump **294** from increasing the magnitude of the negative voltage **295**. Alternatively, if the EN signal is high, the alternating signal from the oscillator **293** is enabled so that the charge pump **294** will increase the magnitude of the negative voltage **295**. Because the negative voltage regulator **292** toggles the EN signal on or off depending on whether the ALC **291** determines to adjust the negative voltage **295**, the leakage manager system **290** maintains the negative voltage **295** at a particular negative voltage to minimize static leakage of the logic gate.

Under normal operation where the digital logic block is to operate, the sleep control receives a signal (sleep input, polarity unimportant here) to disable the charge pump and raise V_{sleep} voltage to V_{DD}.

Under idle operation, where the digital logic block is to sleep (change to a low leakage current state), the Charge Pump Control Logic (CPCL) sends a clock signal and an enable signal to the Negative Voltage Charge Pump (NVCP) to first rapidly drop the V_{sleep} signal to V_{SS}. Then the charge pump begins to push the V_{sleep} voltage below V_{SS} and continues to do so until it receives a pause signal from the CPCL. The Negative Bias Voltage Bias Regulator (NVBR) monitors

the V_{sleep} voltage until a desirable reduction of the transistor current I_{off} has been achieved. At that point it sends a signal to the CPCL to initiate a Pause signal to the NVCP. As time passes the Vsleep voltage will slowly drift upwards toward V_{SS} and at a preset transistor I_{off} the NVBR sends a signal to the CPCL to restart the NVCP to restore the V_{sleep} negative voltage to achieve the desired I_{off}.

FIG. **3** depicts an illustration of the power island manager **220** with an isolation gate **350** and a D flip-flop **360** in an exemplary embodiment of the invention. The power island manager **220** includes a data retention state machine **330** and a sleep generator **340** that are coupled to each other.

The power island manager **220** is coupled to the isolation gate **350** by the ISO signal. The ISO signal is also coupled to other isolation gates. The data retention state machine **330** is coupled to DRB input of the D flip-flop **360** via the DRB signal. The data retention state machine **330** is also coupled to the AND gate **362** via the ENC signal. The clock island (CKI) signal is coupled to the data retention state machine **330** and the AND gate **362**. The sleep generator **340** is coupled to the D flip-flop **360** and the AND gate **362** via the SLPB signal. The output of the AND gate **362** is coupled to the C input of the D flip-flop **360** via the CKA signal. The system reset signal is coupled to the RESETB input of the power island manager **220** and the RB input of the D flip-flop **360**. The SLPB signal, the DRB signal, and the system reset signal are coupled to other data retention flip-flops.

FIG. **4** depicts an illustration of a power island manager **220** in an exemplary embodiment of the invention. The power island manager **220** includes an AND gate **402**, a multiplexer (MUX) **404**, a D flip-flop **410**, an inverter **412**, an AND gate **414**, a D flip-flop **420**, a D flip-flop **430**, the data retention state machine **330**, a MUX **432**, a MUX **442**, a sleep generator **340**, and a buffer **452**.

The DI**0** pin is coupled to the D input of the D flip-flop **410**. The SI**0** pin is coupled to the S**1** input of the D flip-flop **410**. The CSB and the WEB pins are coupled to the inputs of the AND gate **402**. The output of the AND gate **402** and the SCK**1** pin are coupled to the input of the MUX **404**. The output of the MUX **404** is coupled to the C inputs of the D flip-flop **410**, the D flip-flop **420**, and the D flip-flop **430**. The Q output of the D flip-flop **410** is coupled to the DO**0** pin, which is coupled to the input of the inverter **412** and the SI input of the D flip-flop **420**. The DI**1** pin is coupled to the D input of the D flip-flop **420**. The Q output of the D flip-flop **420** is coupled to the DO**1** pin, which is coupled to the input of the AND gate **414** and the SI input of the D flip-flop **430**. The output of the AND gate **414** is coupled to the RSTB pin. The DI**2** pin is coupled to the D input of the D flip-flop **430**. The Q output of the D flip-flop **430** is coupled to the DO**2** pin, which is coupled to the DLY**1**/ISO pin. The DLY**1**/ISO pin is coupled to the SO**1**, the input of the MUX **432**, and the data retention state machine **340**.

The RESETB pin is coupled to the R input of the D flip-flop **430**, the D flip-flop **420**, and the D flip-flop **410**. The SE pin, the RESETB pin, the CKI pin, and the SI**2** pin are coupled to the data retention state machine **330**. The data retention state machine **330** is coupled to the input of the MUX **432**, the SO**2** pin, the DRB pin, the ENC pin, and the input of the MUX **442**. The output of the MUX **442**, the VDDI pin, and the VL[0:2] are coupled to the sleep generator **340**. The sleep generator **340** is coupled to the SLPB pin. The sleep generator **340** is coupled to the data retention state machine **330** via the AW pin and the input of the buffer **452**. The output of the buffer **452** is coupled to the DO**3** pin. The DRMODE pin is coupled to the MUX **442**.

In operation, the power island manager **220** has a three bit register for controlling a power island for some embodiments. D [**0**], with input DI**0** and output DO**0**, is an island reset for re-initializing a power island. This bit is combined with RESETB to form RSTB to re-initialize the power island whenever RESETB or the D [**0**] is active. D [**1**], with input DI**1** and output DO**1**, is a sleep bit. When the D [**1**] bit is set to one, the power island goes into a low leakage state. D [**2**], with input DI**2** and output DO**2**, is a DLY**1**/Isolate bit. When DRMODE is tied to low, the D [**2**] bit, when set to one, will add one clock cycle delay between DRB going active and SLPB going active. When DRMODE is tied high, the D [**2**] bit, when set to one, will activate isolation of the power island. D [**3**], such as DO**3**, is an awake bit. This D [**3**] bit goes high when SLPB is high. This can be used by software to determine when a power island is out of the sleep state.

The power island manager **220** has two operating modes: one that supports power islands with data retention flip-flops and one that does not. When the DRMODE pin is tied high, a power island is put to sleep by writing a one to D[**1**]. The data retention state machine **330** performs the timing. The isolate (ISO) signal goes active when the sleep bit is written to a one, and the enable clock (ENC) and the data retention (DRB) will go low after synchronization to the power island clock (CKI). One or two clock cycles later the sleep (SLPB) goes low. To come out of sleep mode, a zero is written to D[**1**]. In some embodiments, all clock buffers in the power islands can be put to sleep to further minimize leakage. Software can determine when the power island has come out of sleep by reading when DO**3** is high.

The System Reset is typically applied once after initial system power up. In some embodiments, the System Reset goes to all data retention flip-flops. The System Reset signal and DI**0** bar are combined in a logical AND (RSTB output) to provide initialization to non data retention flip-flops. To create a power island reset, D[**0**] is set to a one and then cleared to a zero by software.

When the DRMODE is tied low, the power island manager **220** can also provide the control signals for a power island without data retention flip-flops. The power island manager **220** may have a hardware driven method and a software driven method for interfacing to power islands without data retention flip-flops. The software sequence has the following sequence:

Write 04/turn on isolation
Write 06/turn on sleep, isolation on/come out of sleep
Write 05/turn sleep off, reset island, isolation on/wait for sleep to go high
Read/test for DO3=1; sleep is high
Write 00/turn isolation off, normal operation

The hardware driven method uses a clock to sequence the state machine. The only action software takes is to write the sleep bit (DI**1**) to a one to go into sleep and write a zero to the sleep bit to go out of sleep. Software can determine when the island has come out of sleep by reading when DO**3** is high.

In some embodiments, the power island manager **220** contains two scan chains because some of the flip-flops are clocked on the positive and some on the negative. The scan chain enable pin switches the clock on scan chain **1** (SI**1** is the input; SO**1** is the output), the registers, to CKS**1**. Scan chain **2** (SI**2** is the input; SO**2** is the output) is connected to the data retention state machine **330** flip-flops that are clocked on the negative edge of CKI. A separate scan out is provided for each clock domain.

In some embodiments, the SLPB net uses p-type antenna diodes. Since the SLPB net may go to a negative voltage, an n-type antenna diode can cause excessive leakage to ground.

The leakage can cause SLPB not to go negative and may not work properly. The CSB pin is a chip select pin. The WEB pin is the write enable pin. The VL [2:0] is the leakage control voltage value set by the ALC **270** (FIG. **2**). The VDDI is the VDD from the power island.

Low Leakage, Data Retention Circuitry—FIGS. **5**, **6**, **7**A-C, **8**A-**8**B, and **9**-**12**

FIGS. **5**, **6**, **7**A-C, and **8**A-**8**B disclose one embodiment for low leakage, data retention circuitry. In this embodiment, in sleep mode, the circuit parts of a flip-flop that do not require data retention are coupled to ground through a sleep transistor. The gate of the sleep transistor is coupled to a sleep signal that can be driven to a negative voltage such as −0.3V. Thus, the leakage in these circuit parts of the flip-flop is eliminated (reduced). When not in a sleep state, the sleep transistor has a gate value equal to or greater than the VDD supply, which effectively grounds the circuit.

The circuit parts that require data retention are coupled to ground through two transistors. One transistor acts effectively to ground the circuit above when not in sleep mode just as the sleep transistor described above. The other transistor is a PMOS device with the gate tied to ground, which provides medium impedance to ground. The voltage drop across this transistor acts to reduce the leakage by increasing the source bias of the NMOS transistors and simultaneously reduces the voltage across the circuit. In this embodiment, the data is retained in a sleep state and reduces the leakage by a factor of 22.

FIG. **5** depicts an illustration of a D/Q portion **500** of the flip-flop circuitry in an exemplary implementation of the invention. The D/Q portion **500** of the flip-flop circuitry includes an inverter **502**, a M**3** PMOS transistor **504**, an M**4** NMOS transistor **506**, master latch circuitry **510**, an M**11** PMOS transistor **522**, an M**12** NMOS transistor **524**, an M**13** NMOS transistor **526**, slave latch circuitry **530**, and an inverter **540**.

The D signal input is the input of the inverter **502**, which includes transistors M**1** and M**2**. The source of the inverter **502** is coupled to the node OFF, which is described below in FIG. **7**A. The output of the inverter **502** is coupled to the M**3** PMOS transistor **504** and the M**4** NMOS transistor **506**. The gate of the M**3** PMOS transistor **504** is coupled to the CLK signal input. The gate of the M**4** NMOS transistor **506** is coupled to the CLKB signal input.

The master latch circuitry **510** includes the inverter **512** and the inverter **514**. The inverter **514** forms a feedback loop with the inverter **512**, where the output of the inverter **512** is coupled to the input of the inverter **514** and the output of the inverter **514** is coupled to the input of the inverter **512**. The inverter **512** corresponds to transistor M**5** and M**6**. The inverter **514** corresponds to transistors M**7**-M**10**. The input of the inverter **512** is coupled to node A, which is described in FIG. **8**A below. The source of the inverter **512** is also coupled to node OFF, which is described below in FIG. **7**A. The output of the inverter **512** is coupled to node B, which is described below in FIG. **8**A. The source of the inverter **514** is coupled to node OFF, which is described below in FIG. **7**A. The PMOS gate of the inverter **514** is coupled to the CLKB signal input. The NMOS gate of the inverter **514** is coupled to the CLK signal input.

The M**11** PMOS transistor **522** is in parallel to the M**12** NMOS transistor **524** and the M**13** NMOS transistor **526**, which are in series. The gate of the M**11** PMOS transistor **522** is coupled to the CLKB signal input. The gate of the M**12** NMOS transistor **524** is coupled to the HOLDB signal input. The gate of the M**13** NMOS transistor **526** is coupled to the CLK signal input.

The slave latch circuitry **530** includes the inverter **532** and the inverter **534**. The inverter **534** forms a feedback loop with the inverter **532**, where the output of the inverter **532** is coupled to the input of the inverter **534** and the output of the inverter **534** is coupled to the input of the inverter **532**. The inverter **532** corresponds to transistor M**14** and M**15**. The inverter **534** corresponds to transistors M**18**-**21** and M**31**. The input of the inverter **532** is coupled to node C, which is described in FIG. **8**B below. The source of the inverter **532** is also coupled to node SB, which is described below in FIGS. **7**B-C. The output of the inverter **532** is coupled to node D, which is described below in FIG. **8**B. The source of the inverter **534** is coupled to node SB, which is described below in FIGS. **7**B-C. The PMOS gates of the inverter **534** are coupled to the HOLDB and CLK signal inputs. The NMOS gate of the inverter **534** is coupled to the CLKB signal input.

The output of the inverter **532** is coupled to the input of the inverter **540**. The inverter **540** corresponds to transistors M**16** and M**17**. The source of the inverter **540** is also coupled to node OFF, which is described below in FIG. **7**A. The output of the inverter **540** is the Q signal output.

FIG. **6** depicts a CK portion **600** of the flip-flop circuitry in an exemplary implementation of the invention. The CK portion **600** of the flip-flop circuitry includes an inverter **602**, an M**24** PMOS transistor **604**, an M**25** PMOS transistor **606**, an M**26** NMOS transistor **608**, an M**32** NMOS transistor **610**, and an M**27** PMOS transistor **612**.

The CK signal input is the input of the inverter **602**, which includes transistors M**22** and M**23**. The source of the inverter **602** is coupled to node OFF, which is described below in FIG. **7**A. The output of the inverter **602** is coupled to the drain of the M**24** PMOS transistor **604** and the node CLKB. The gate of the M**24** PMOS transistor **604** is coupled to the HOLDB signal input. The output of the inverter **602** is also coupled to the M**25** PMOS transistor **606** and the M**26** NMOS transistor **608**. The M**25** PMOS transistor **606**, the M**26** NMOS transistor **608**, and the M**32** NMOS transistor **610** are coupled in series. The gate of the M**32** NMOS transistor **610** is coupled to the HOLDB signal input.

The CLK signal output is coupled to the drain of the M**25** PMOS transistor **606**, the drain of the M**26** NMOS transistor **608**, and the drain of the M**27** PMOS transistor **612**. The gate of the M**27** PMOS transistor **612** is coupled to the HOLDB signal input.

FIG. **7**A depicts a sleep transistor **702** for the OFF node in an exemplary implementation of the invention. The sleep transistor **702** is an NMOS transistor that corresponds to transistor M**28**. The drain of the sleep transistor **702** is coupled to the OFF node. The gate of the sleep transistor **702** is coupled to the SLEEPB signal input. The source of the sleep transistor **702** is coupled to ground. In some embodiments, the OFF node can be separated into two or more nodes each having its own NMOS sleep transistor.

FIG. **7**B depicts a sleep transistor **704** for the SB node in an exemplary implementation of the invention. The sleep transistor **704** is an NMOS transistor that corresponds to transistor M**29**. The drain of the sleep transistor **704** is coupled to the SB node. The gate of the sleep transistor **704** is coupled to the SLEEPB signal input. The source of the sleep transistor **704** is coupled to ground.

FIG. **7**C depicts a sleep transistor **706** for the SB node in an exemplary implementation of the invention. The sleep transistor **706** is a PMOS transistor that corresponds to transistor M**30**. The source of the sleep transistor **706** is coupled to the SB node. The gate and drain of the sleep transistor **706** are coupled to ground.

FIG. **8**A depicts circuitry **800** for the tristate inverter in the master latch in an exemplary implementation of the invention. The circuitry **800** for the master latch includes a PMOS transistor **802**, a PMOS transistor **804**, an NMOS transistor **806**, and an NMOS transistor **808** that are coupled together in series. The gates of the PMOS transistor **802** and the NMOS transistor **808** are coupled to the node B. The gate of the PMOS transistor **804** is coupled to the CLKB signal input. The gate of the NMOS transistor **806** is coupled to the CLK signal input. The drains of the PMOS transistor **804** and the NMOS transistor **806** are coupled to node A. The source of the NMOS transistor **808** is coupled to node OFF.

FIG. **8**B depicts circuitry **810** for the tristate inverter in the slave latch in an exemplary implementation of the invention. The circuitry **810** for the slave latch includes a PMOS transistor **812**, a PMOS transistor **814**, a PMOS transistor **816**, an NMOS transistor **818**, and an NMOS transistor **820**. The PMOS transistor **812** is coupled to the PMOS transistor **814** and the PMOS transistor **816** that are parallel to each other. The PMOS transistor **814** and the PMOS transistor **816** are coupled to the NMOS transistor **818**, which is also coupled to the NMOS transistor **820**.

The gates of the PMOS transistor **812** and the NMOS transistor **820** are coupled to the node D. The gate of the PMOS transistor **814** is coupled to the HOLDB signal input. The gate of the PMOS transistor **816** is coupled to the CLK signal input. The gate of the NMOS transistor **818** is coupled to the CLKB signal input. The drains of the PMOS transistor **814**, the PMOS transistor **816**, and the NMOS transistor **806** are coupled to node C. The source of the NMOS transistor **820** is coupled to node SB.

FIG. **9** depicts an illustration of the HOLDB and SLEEPB signals in an exemplary embodiment of the invention.

The operation begins with CK going to zero. This causes CLKB to be equal to VDD and CLK to be equal to zero, which isolates the slave latch circuitry **530** from the master latch circuitry **510**. The HOLDB signal goes to 0 to retain the state of the slave latch. The SLEEPB signal then goes to −0.3V. This shuts off transistor M**28** in FIG. **7**A, which halts the leakage from all the circuits except in the slave latch circuitry **530**. When not in sleep mode, transistor M**28** provides a low impedance path to ground.

The slave latch circuitry **530** is coupled to ground through the transistors M**29** and M**30**, respectively depicted in FIGS. **7**B and **7**C. One purpose of transistor M**29** is to provide a low impedance path to ground when not in sleep mode.

One purpose of transistor M**30** is to provide a default moderate impedance path to ground when transistor M**29** is off or in sleep mode. The leakage in the slave latch circuitry **530**, in going through transistor M**30**, causes node SB to rise. This provides a source bias to the slave NMOS transistors reducing the leakage through them and also reduces the voltage across the slave side to VDD-SB, which further reduces the leakage. Equilibrium is reached where the leakage cannot increase. Basically, the leakage is used to limit itself.

This embodiment uses the gated VDD solution because the voltage across the circuit is reduced to VDD-SB. This embodiment combines this gated VDD with the modulated back gate bias method because of the source bias SB but only for the NMOS transistors. This is accomplished without switching a lower VDD and driving a well. Thus, a simple process can be used. Also, this embodiment advantageously uses the moderate impedance transistor in a way that causes leakage to limit itself by reaching equilibrium.

FIGS. **10** and **11** disclose another embodiment for low leakage, data retention circuitry. In this embodiment, in a sleep state, the circuitries that do not require data retention are coupled to ground through a sleep transistor. The logic coupled to the transistors gated by the SLEEPB signal is shut off and draws minimal leakage. This process is accomplished by driving the SLEEPB signal below VSS by 0.3-0.4V. The HOLDB signal keeps the slave latch circuitry from changing state while the rest of the flip-flop comes out of the sleep state. The only part of the flip-flop still powered is the slave latch circuitry. The slave latch circuitry combines several techniques to minimize leakage.

FIG. **10** depicts circuitry **1000** for low leakage and data retention in an exemplary embodiment of the invention. The circuitry **1000** includes the inverter **1002**, the master latch circuitry **1010**, the slave latch circuitry **1020**, the inverter **1032**, the inverter **1034**, the sleep transistors **1042**, **1044**, **1046**, and **1048**, the inverter **1052**, and the inverter **1054**.

The D input is the input for the inverter **1002**. The master latch circuitry **1010** includes the transmission gate **1012**, the inverter **1014**, the transmission gate **1016**, and the inverter **1018**. The output of the inverter **1002** is coupled to the left contact of the transmission gate **1012**. The right contact of the transmission gate **1012** is coupled to the input of the inverter **1014** and the left contact of the transmission gate **1016**. The output of the inverter **1014** is coupled to the D input of the slave latch circuitry **1020** and the input of the inverter **1018**. The output of the inverter **1018** is coupled to the DB input of the slave latch circuitry **1020** and the right contact of the transmission gate **1016**.

The SLEEPB signal input is coupled to the gates for the SL**1** sleep transistor **1042**, the SL**2** sleep transistor **1044**, the SL**3** sleep transistor **1046**, the SL**4** sleep transistor **1048**, and the SLEEPB input of the slave latch circuitry **1020**. The SL**1** sleep transistor **1042** is coupled to the inverter **1002** and ground. The SL**2** sleep transistor **1044** is coupled to the inverter **1052**, the inverter **1054**, and ground. The SL**3** sleep transistor **1046** is coupled to the inverter **1014**, the inverter **1018**, and ground. The SL**4** sleep transistor **1048** is coupled to the inverter **1032**, the inverter **1034**, and ground. In some embodiments, the SL**1** sleep transistor **1042**, the SL**2** sleep transistor **1044**, the SL**3** sleep transistor **1046**, and the SL**4** sleep transistor **1048** can each be separated into two or more node each having its own NMOS sleep transistor.

The CK signal is the input of the inverter **1052**. The output of the inverter **1052** is coupled to the transmission gate **1012**, the transmission gate **1016**, and the input of the inverter **1054**. The output of the inverter **1054** is coupled to the transmission gate **1012**, the transmission gate **1016**, and the CLK input of the slave latch circuitry **1020**. The HOLDB signal input is coupled to the HOLDB input of the slave latch circuitry **1020**. The output of the slave latch circuitry **1020** is coupled to the input of the inverter **1032**. The output of the inverter **1032** is coupled to the input of the inverter **1034**. The output of the inverter **1034** is the Q signal.

FIG. **11** depicts slave latch circuitry **1020** in an exemplary embodiment of the invention. The slave latch circuitry **1020** includes D**1** transistor **1102**, D**2** transistor **1104**, DH transistor **1106**, DSL sleep transistor **1108**, stack transistors **1110**, stack transistors **1120**, D**1**B transistor **1132**, D**2**B transistor **1134**, DHB transistor **1136**, and sleep transistor **1138**.

The D**1** transistor **1102**, the D**2** transistor **1104**, the DH transistor **1106**, and the DSL sleep transistor **1108** are coupled to each other in series with the sleep transistor **1108** coupled to ground. The gate of the D**1** transistor **1102** is coupled to the CLK signal input. The gate of the D**2** transistor **1104** is coupled to the D signal input. The gate of the DH transistor **1106** is coupled to the HOLDB signal input. The gate of the sleep transistor **1108** is coupled to the SLEEPB signal input.

The stack transistors **1110** comprise P**1** transistor **1112**, P**0** transistor **1114**, N**1** transistor **1116**, and N**0** transistor **1118**. The P**1** transistor **1112**, the P**0** transistor **1114**, the N**1** transistor **1116**, and the N**0** transistor **1118** are coupled to each other in series with the N**0** transistor **1118** coupled to ground. The gates of the P**1** transistor **1112**, the P**0** transistor **1114**, the N**1** transistor **1116**, and the N**0** transistor **1118** are coupled to the LAT signal input. The drains of the P**0**B transistor **1124** and the N**1**B transistor **1126** are coupled to the LAT signal input.

The stack transistors **1120** comprise P**1**B transistor **1122**, P**0**B transistor **1124**, N**1**B transistor **1126**, and N**0**B transistor **1128**. The P**1**B transistor **1122**, the P**0**B transistor **1124**, the N**1**B transistor **1126**, and the N**0**B transistor **1128** are coupled to each other in series with the N**0**B transistor **1128** coupled to ground. The gates of the P**1**B transistor **1122**, the P**0**B transistor **1124**, the N**1**B transistor **1126**, and the N**0**B transistor **1128** are coupled to the LATB signal input. The drains of the P**0** transistor **1114** and the N**1** transistor **1116** are coupled to the LATB signal input.

In operation, the logic coupled to the transistors gated by the SLEEPB signal is shut off and draws minimal leakage. This process is accomplished by driving the SLEEPB signal below VSS by 0.3-0.4V. The HOLDB signal keeps the slave latch circuitry **1020** from changing state while the rest of the flip-flop comes out of the sleep state. The only part of the flip-flop still powered is the slave latch circuitry **1020**. The slave latch circuitry **1020** combines several techniques to minimize leakage. Transistors not necessary for state retention (stacks with CLK) have sleep transistors to shut off leakage (gated by the SLEEPB signal).

The 8 transistors in the stack transistors **1110** and **1120** use two techniques to reduce leakage. The first technique used is transistor stacking, which is also called self-reverse bias. The N**0** transistor **1118** and the N**1** transistor **1116** will have some small leakage even when the gate is at 0V. As a result, VNN**1** will be at a positive voltage. This causes VGS(N**1**) and VBS (N**1**) to be negative, and VDS(N**1**) to decrease. Consequently, the leakage current is reduced in N**0** transistor **1118** and the N**1** transistor **1116**. The same effect occurs on N**0**B transistor **1128**, N**1**B transistor **1126**, P**0** transistor **1114**, P**1** transistor **1112**, P**0**B transistor **1124**, and P**1**B transistor **1122**.

The second technique is called multiple threshold transistors. Increasing channel length of MOS transistors increases the threshold of the devices without any change in process complexity. The N**0** transistor **1118**, the N**1** transistor **1116**, the N**0**B transistor **1128**, and the N**1**B transistor **1126** have increased channel length, which raises VTH and reduces leakage current.

This embodiment reduces leakage by a factor of 25 over a current standard cell D flip-flop.

I/O Pad—FIG. **12**

In some embodiments, a programmable general purpose input and output (I/O) padcell includes built in-level shifters and isolation that interface with the chip core logic. In these embodiments, a level shifter can be controlled to retain data.

FIG. **12** depicts circuitry **1200** for a level shifter for an I/O pad in an exemplary embodiment of the invention. The circuitry **1200** includes MP**2** transistor **1202**, MP**3** transistor **1204**, M**3** transistor **1206**, M**4** transistor **1208**, M**1** transistor **1210**, M**0** transistor **1212**, M**5** transistor **1214**, M**2** transistor **1216**, and an inverter **1218**.

The circuitry **1200** is for a latching level shifter. The M**3** transistor **1206** and the M**4** transistor **1208** are "native" cascode devices. The M**3** transistor **1206** and the M**4** transistor **1208** are also known as depletion-mode transistors. The M**3** transistor **1206** and the M**4** transistor **1208** are used to allow thin gate devices to be used in the input stage. This allows large voltage ratios between the VDD and the V**3**I**0**. The M**0** transistor **1212** and the M**1** transistor **1210** are output latching devices that allow the level shifter to retain the state when both IN and INB are 0. Thus, IN and INB control data retention.

In some embodiments, the gates of the M**3** transistor **1206** and the M**4** transistor **1208** are coupled to other transistors connected to the cascode voltage.

The following truth table is for circuitry **1200**.

IN	INB	OUT
0	0	Retain last state
0	1	0
1	0	1
1	1	Illegal

There will be setup time requirements for any signal compared to SLPB. If level shifters are used with an SRAM cell built into the output stage, the two inputs can be removed anytime after the output latch has flipped to a new state. Both 1.2V inputs to the level shifter cannot go to VDD. This can be prevented by including an inverter. If both the inverter and the level shifter have SLPB transistors, there is a potential timing race if SLPB goes to VSS with VDD high. In this case, the level shifters should be off before the output of the inverter drifts to VDD. In some embodiments, the M**5** transistor **1214** and the M**2** transistor **1216** can be configured to withstand greater voltages.

In some embodiments, the sources of the M**5** transistor **1214** and the M**2** transistor **1216** can be coupled to a common SLEEPB transistor **1240** to further reduce leakage. In one embodiment, the width of the SLEEPB transistor **1240** is 4 micrometers, and the length is 0.13 micrometers. The following truth table is for circuitry **1200** including this common SLEEPB transistor **1240**:

SLEEPB	IN	INB	OUT
1	0	0	Retain state (Data Retention)
1	0	1	0
1	1	0	1
1	1	1	Illegal
0	X	X	Retain State

In some embodiments, the SLEEPB=0 input state should be understood to include the SLEEPB voltage being below 0V (E.g. −0.35V generated by a leakage optimization circuit).

In this extension to FIG. **12** (and the above truth table), the two Data Retention states may be operated independently, sequentially or simultaneously. This is beneficial when the SLEEPB input is used to control/limit leakage power while the IN/INB=00 state is used for data retention. This is because the SLEEPB voltage comes from a charge pump and takes some time to transition from Vdd (=1) to the Data Retention mode.

The above description is illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be

determined with reference to the appended claims along with their full scope of equivalents.

While this invention has been particularly shown and described with references to example embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the scope of the invention encompassed by the appended claims.

What is claimed is:

1. A method carried out in an integrated circuit that includes an adaptive leakage controller, a power manager and a plurality of power islands, the method comprising:

receiving, at the power manager, a control signal from the adaptive leakage controller; and

employing the power manager to dynamically change power consumptions of the plurality of power islands, the employing the power manager to dynamically change power consumptions including: generating a variable voltage based on the control signal; and providing the variable voltage to at least one of low leakage sleep circuits of the integrated circuit.

2. The method as claimed in claim **1** further comprising putting to sleep and taking out of sleep, at different times, at least one of the power islands.

3. The method as claimed in claim **2** wherein the power manager employs a state machine to control the putting to sleep and the taking out of sleep.

4. The method as claimed in claim **1** wherein the variable voltage is an optimum voltage.

5. The method as claimed in claim **4** wherein the optimum voltage is dependent upon both process variation and temperature variation.

6. The method as claimed in claim **4** wherein the optimum voltage is generated by a sleep generator.

7. The method as claimed in claim **1** wherein the control signal is a digital signal.

8. The method as claimed in claim **1** wherein the at least one of the low leakage sleep circuits is connected in series to a source of a supply voltage and to a logic gate or storage cell of one of the power islands.

9. The method as claimed in claim **8** wherein the at least one of the low leakage sleep circuits modifies the supply voltage to the one of the power islands during a sleep mode.

10. A method carried out in an integrated circuit that includes an adaptive leakage controller, a power manager, a plurality of power islands and a plurality of low leakage sleep circuits, the method comprising:

receiving, at the power manager, a control signal from the adaptive leakage controller; and

employing the power manager to dynamically change power consumptions of the plurality of power islands, the employing the power manager to dynamically change power consumptions including: generating a variable voltage based on the control signal; and providing the variable voltage to the plurality of low leakage sleep circuits,

wherein each of low leakage sleep circuits is associated with leakage reduction of a respective one of the plurality of power islands.

11. The method as claimed in claim **10** further comprising putting to sleep and taking out of sleep, at different times, at least one of the power islands.

12. The method as claimed in claim **11** wherein the power manager employs a state machine to control the putting to sleep and the taking out of sleep.

13. The method as claimed in claim **10** wherein the variable voltage is an optimum voltage.

14. The method as claimed in claim **13** wherein the optimum voltage is dependent upon both process variation and temperature variation.

15. The method as claimed in claim **13** wherein the optimum voltage is generated by a sleep generator.

16. The method as claimed in claim **10** wherein the control signal is a digital signal.

17. The method as claimed in claim **10** wherein at least one of the low leakage sleep circuits is connected in series to a source of a supply voltage and to a logic gate or storage cell of an associated one of the power islands.

18. The method as claimed in claim **17** wherein the at least one of the low leakage sleep circuits modifies the supply voltage to the associated one of the power islands during a sleep mode.

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