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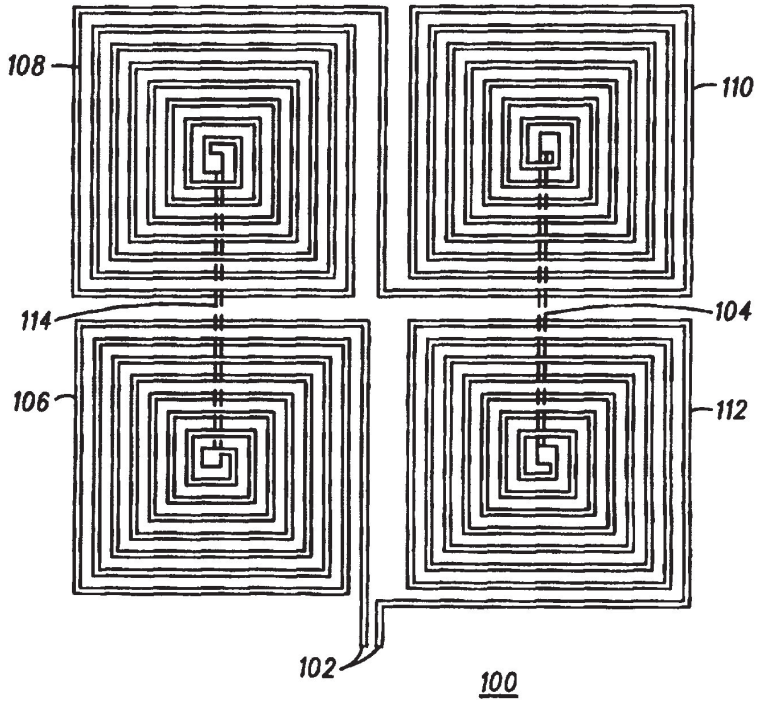
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(54) Title: LOW RADIATION PLANAR INDUCTOR/TRANSFORMER AND METHOD

(57) Abstract

The present invention provides a planar magnetic field inductor/transformer (100, 200, 300, 400, 500, 600, 700, 800, 900, 1000, 1700, 1800) and method (1900, 2000) that has a plurality of at least three planar loops/spiral conductor coils (106, 108, 110, 112) which are arranged one after another in a simple/compound loop fashion. The loops (106, 108, 110, 112) carry a current produced by a signal source, and the plurality of planar adjacent loops/spiral conductor coils (106, 108, 110, 112) are arranged to maximize cancellation of a moment of the plurality of loops/spiral conductor coils (106, 108, 110, 112) over a predetermined range.



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LOW RADIATION PLANAR INDUCTOR/TRANSFORMER AND METHOD

Field of the Invention

The present invention relates generally to induction and, more particularly, to substantially planar inductors.

Background of the Invention

To obtain a coupled inductor or transformer, the windings are typically on a spool around a loop of magnetic material. The winding may include either a wire of conducting material or may be a part of a printed circuit board. In this configuration the inductor/transformer requires additional volume and cost. Other structures in the prior art include printed circuit boards with embedded magnetic material which require additional steps in their manufacture. Planar inductors that are unshielded by magnetic material tend to radiate a magnetic field producing EMI (electromagnetic interference) that interferes with adjacent circuitry.

Thus, there is a need for a method and planar inductor/transformer that maximizes cancellation of a moment of the plurality of loops/spiral conductor coils over a predetermined range. Thus, the planar inductor/transformer

may be oriented to allow placement of EMI-sensitive circuitry in the predetermined range.

Brief Description of the Drawings

FIG. 1 is a diagrammatic representation of a 4-loop single layer planar inductor in accordance with the present invention.

FIG. 2 is a diagrammatic representation of a 4-loop, two layer planar inductor in accordance with the present invention.

FIGs. 3-5 are schematic representations of 4-loop, 6-loop, and 8-loop planar inductors/transformers in accordance with the present invention.

FIG. 6 is a schematic representation of the magnetic field of a 6-loop inductor/transformer in accordance with the present invention.

FIG. 7 is a diagrammatic representation of a side view of one embodiment of a planar inductor/transformer having a bulk ferrite above and below the planar structure in accordance with the present invention.

FIG. 8 is a diagrammatic representation of a side view of another embodiment of a planar inductor/transformer including a shield above and below the planar structure for enhancing cancellation of the magnetic field in accordance with the present invention.

FIG. 9 is a diagrammatic representation of another embodiment of a planar inductor/transformer including multiple auxiliary conducting structures adjacent to the planar structure for enhancing cancellation of the magnetic field in accordance with the present invention.

FIG. 10 is a diagrammatic representation of a side view of an embodiment of a transformer including a primary winding on one surface and a secondary winding on an opposite surface in accordance with the present invention.

FIG. 11 represents a radiation field pattern for a single spiral as is known in the art.

FIG. 12 represents a radiation field pattern for a figure 8 shape as is known in the art.

FIG. 13 represents a radiation field pattern for the structure shown in FIG. 1.

FIG. 14 represents a radiation field pattern for the structure shown in FIG. 9.

FIG 15 reresents a radiation field pattern for the structures shown in FIGs. 4 and 6.

FIG 16 reresents a radiation field pattern for the structure shown in FIG. 18.

FIG. 17 is a schematic representation of another embodiment of a double spiral, with one spiral inside another spiral, of a planar inductor in accordance with the present invention.

FIG. 18 is a diagrammatic representation of an asymmetricly placed 4-loop single layer planar inductor in accordance with the present invention.

FIG. 19 is a flow chart of one embodiment of steps of one embodiment of a method in accordance with the present invention.

FIG. 20 is a flow chart of one embodiment of steps of another embodiment of a method in accordance with the present invention.

FIGs. 21-22 are graphical representations of results of simulations of the coupled magnetic field of a circular loop, a 4-loop inductor, a 6-loop inductor and an 8-loop inductor in correspondence with FIGs. 3-5.

FIG. 23 is a graphical representation of the inductance of a 4-loop spiral inductor implementation of the present invention and a simple circular spiral occupying the same area on a two-layer printed circuit board.

FIG. 24 is a graphical representation of the resistance of a 4-loop spiral inductor implementation of the present invention and a simple circular spiral occupying the same area on a two-layer printed circuit board.

FIG. 25 is a graphical representation of the quality factor (Q) of a 4-loop spiral inductor implementation of the present invention and a simple circular spiral occupying the same area on a two-layer printed circuit board.

FIG. 26 is a diagrammatic representation of a spiral inductor that is placed concentrically above a non-interacting multiloop inductor structure such that the coupled magnetic field is substantially zero in accordance with the present invention.

FIG. 27 is a diagrammatic representation of a printed circuit board inductor with a topology that includes at least four consecutively coupled conducting loops/spirals on a polygonal lattice wherein the conducting loops/spirals are scaled from the topology to provide a zero net moment in accordance with the present invention.

Detailed Description of a Preferred Embodiment

The present invention provides a method and planar inductor/transformer that maximizes cancellation of a moment of the plurality of loops/spiral conductor coils over a predetermined range such that interference with external and adjacent circuitry is minimized. The invention is particularly useful for switched power converters and inductors in RF transmitters which have a size constraint.

Presently planar inductors are not a part of choice in the above applications due to interference. The present invention reduces interference by at least an order of magnitude in comparison with the prior art, thus making the present invention more suitable for use in power converters and RF transmitters.

The present invention provides a planar magnetic field inductor/transformer that has a plurality of at least three planar adjacent loops/spiral conductor coils arranged one after another in a simple/compound loop fashion. The planar adjacent loops/spiral conductor coils carry a current produced by a signal source, and the plurality of planar adjacent loops/spiral conductor coils are arranged to maximize cancellation of a moment of the plurality of loops/spiral conductor coils over a predetermined range. Typically, an electrical connection to an internal end of a loop/spiral is made through an electriclly conducting via that passes through a substrate. For example, a spiral may be achieved by providing space from a substrate surface by a plurality of spaced apart electrically conductive posts having a staggered arrangement between adjacent windings of the spiral. As is known in the art, a transformer generally includes at least two windings disposed on top of each other in a semiconductor substrate and separated by an electrically insulating film.

The inductor/transformer may include a multi-layer structure that further includes one of: A) at least another planar magnetic field inductor/transformer arranged with the planar magnetic field inductors/transformers one above the other; and B) at least another planar magnetic field inductor/transformer arranged with the planar magnetic field inductors/transformers one above the other and a bulk

ferromagnetic layer having a thickness of greater than 100μm wherein the ferromagnetic layer/layers is located in one of the following locations: B1) above the planar magnetic field inductor(s)/transformer(s); B2) below the planar magnetic field inductor(s)/transformer(s); B3)above and below the planar magnetic field inductor(s)/transformer(s).

The spiral inductor is typically embodied by disposing an electrical conductor in a first spiral on a first surface of a substrate, wherein the spiral includes an external end disposed outside the spiral as a first terminal and an internal end disposed within the spiral as a second terminal.

The planar adjacent loops/spiral conductor coils are typically arranged having alternating opposite current flow or. alternatively, set/sets of planar adjacent loops/spiral conductor coils that have current flows having phases that cancel.

The planar magnetic field inductor/transformer may be selected to further include a conducting structure/structures for enhancing cancellation of a extraneous magnetic field/fields, wherein the conducting structure/structures is/are located above, below, adjacent to, or above and below the planar magnetic field inductor/transformer.

The at least three planar adjacent loops/spiral conductor coils may have a same predetermined structure, i.e., size and shape, to provide maximum cancellation of a moment over a 360° range or alternatively, may have dissimilar structures to provide maximum cancellation of the moment over a range less than 360°.

For example, to design an inductor with a predetermined inductance and quality factor (Q) wherein the substantially planar inductor has four spiral loops distributed over one or many layers, the following approximate equations are utilized:

$$L = \frac{(4 * \mu * n * p * d)}{\pi} * (\log(3.2 * n)) + (\mu * d)(1.2 (n * p)^2$$

$$Q = \frac{\log(3.2 * n)}{\pi} + (0.3 * m * n * p)$$

where n is the number of turns in the spiral, p is the number of layers, m is the width of the conductor (e.g., a trace) in terms of the skin depth of the conductor. The thickness of the conductor is assumed to be substantially equal to the skin depth of the conductor. Skin depth is the depth to which there is substantial current flow on a conductor surface;

and

$$L = \frac{(4 * \mu * n * p * d)}{\pi} * (\log(3.2 * n)) + (\mu * d)(1.2 (n * p)^2$$

where d is a lateral dimension of an individual loop and μ is the magnetic permeability.

Typically, the gap between the conductors is equal to the conductor thickness. The effect of the printed circuit board material is generally negligible. The current density in the conductor is approximately constant.

In an experimental implementation, a multilayer inductor was constructed with the following properties: d=2 cm and n=7:

For p=1: Theoretical L= 2.15 μH and Experimental L=2.05 μH;

For p=2: Theoretical L= 7.3 μH and Experimental L=7.5 μH;

For p=1: Theoretical Q = 22 and Experimental Q =17;

For p=1: Theoretical Q = 43 and Experimental Q = 35.

FIG. 1, numeral 100, is a diagrammatic representation of a 2N-loop, N a predetermined integer, single layer planar inductor, where 2N is selected to be 4, in accordance with the present invention. The planar magnetic field inductor/transformer typically includes an even number (2N) of planar adjacent loops/spiral conductor coils arranged one after another in a simple closed loop. The 4 planar adjacent loops/spiral conductor coils (106, 108, 110, 112) carry a current produced by a signal source. The even number of planar adjacent loops/spiral conductor coils are arranged to provide total cancellation of a magnetic field on N axes and to maximize overall cancellation of the magnetic field. The planar magnetic field inductor/transformer may be further

implemented as described above. The current flows counterclockwise in two diagonally located coils (106, 110) and clockwise in the other two diagonally located coils (108, 112). The inductor has two terminals (102) and has two crossovers (104, 114) that connect the centers of each of the two pairs of spirals.

FIG. 2, numeral 200, shows a diagrammatic representation of a 4-loop, two layer planar inductor that, for example, may be implemented on a two-layer printed circuit board. The inductor has two terminals (210) and has 4 vias (202, 204, 206, 208) which couple the top layer (212) and bottom layer (214) located at the centers of the spirals. In FIG. 2 the magnetic fields of the two layers are coupled, and the total inductance is larger than the sum of the individual inductances of the two layers.

Alternatively, two layers may utilized to construct two non-interacting inductors disposed concentrically (FIG. 26, numeral 2600). In the implementation shown in FIG. 26, a spiral inductor (2604) is placed concentrically above a non-interacting multiloop/spiral inductor structure (2602) wherein two sets of loops/spirals are coupled by vias (2606, 2608) such that the coupled magnetic field is substantially zero.

FIGs. 3-5, numerals 300, 400, and 500, are schematic representations of 4-loop, 6-loop, and 8-loop planar inductors/transformers in accordance with the present invention. In FIG. 3 two alternate loops (302, 306) have current flowing clockwise, and the other two alternate loops (304, 308) have current flowing counterclockwise.

In FIG. 4, numeral 400, three alternate loops (402, 406, 410) have current flowing clockwise, and the other three alternate loops (404, 408, 412) have current flowing counterclockwise. In FIG. 5, numeral 500, four alternate loops (502, 506, 510, 514) have current flowing clockwise, and the other four alternate loops (504, 508, 512, 516) have current flowing counterclockwise.

FIG. 6, numeral 600, is a schematic representation of the magnetic field of a 6-loop inductor/transformer in accordance with the present invention, wherein the inductor/transformer is located on a board, e.g., a printed circuit board (602). There are 6 current loops, 3 alternate loops (604, 608, 612) have current flowing clockwise and the other 3 loops (606, 610, 614) have current flowing counterclockwise. Thus there is a magnetic field that wraps above from alternate loops (606, 610 and 614) and below the board from the other alternate loops (604, 618, and 612).

FIG. 7, numeral 700, is a diagrammatic representation of a side view of one embodiment of a planar inductor/transformer having a bulk ferrite above (706) and below (708) the planar conducting structure in accordance with the present invention, typically located on a printed circuit board (PCB, 710). The 2-layer (702, 704) implementation of the set of loops/spirals of the present invention are located one layer above the other, with the board (710) between them. The bulk ferrite (706, 708) covers the planar conducting structure (i.e., the loops/spirals) and provides an efficient magnetic path and increases the inductance of the planar inductor/transformer.

FIG. 8, numeral 800, is a diagrammatic representation of a side view of another embodiment of a planar inductor/transformer including a shield (806) above and below the planar structure for enhancing cancellation of the magnetic field in accordance with the present invention. The set of loops/spirals (804) of the present invention are located within the board (802) between them and may, where selected, include multiple layers of loops/spirals.

FIG. 9, numeral 900, is a diagrammatic representation of another embodiment of a planar inductor/transformer including multiple auxiliary conducting structures (902, 904, 906, 908) adjacent to the planar structure (910) for enhancing

cancellation of the magnetic field in accordance with the present invention. The multiple auxiliary structures (902, 904, 906, 908) are located symmetrically and concentrically with respect to the planar structure (910) where maximum cancellation of a moment over a 360° range is desired.

Where cancellation of the moment over a range less than 360° is desired, dissimilar structures (where a structure includes size and/or shape) may be used for the loops/spirals. The multiple auxiliary structures may also be asymmetrical.

FIG. 10, numeral 1000, is a diagrammatic representation of a side view of an embodiment of a transformer including a primary winding (1004) on one surface and a secondary winding (1006) on an opposite surfaces of a printed circuit board (PCB, 1002) in accordance with the present invention.

Radiation fields shown in FIGs. 11-16 represent radiation field patterns, i.e., polar field patterns, measured in the plane of the structure. FIG. 11, numeral 1100, represents a radiation field pattern for a single spiral (1102) as is known in the art. FIG. 12, numeral 1200, represents a radiation field pattern for a figure 8 shape (1202) as is known in the art.

FIG. 13, numeral 1300, represents a radiation field pattern for the structure shown in FIG. 1. The overall

magnitude of the field (1302) obtained using the present invention is reduced by a factor of at least 10 in a far field when compared with the magnitude of the field (1202) obtained from the structures of the prior art. Thus, the far field is completely cancelled, and the near field is nearly cancelled.

FIG. 14, numeral 1400, represents a radiation field pattern for the structure shown in FIG. 9. The overall magnitude of the field (1402) obtained using the present invention exhibits an enhancement in near field cancellation over the field obtained in FIG. 13.

FIG 15, numeral 1500, represents a radiation field pattern for the structures shown in FIGs. 4 and 6. The overall magnitude of the field (1502) obtained using the present invention exhibits greater cancellation in the near field than the field obtained in FIG. 13.

FIG 16, numeral 1600, represents a radiation field pattern for the structure shown in FIG. 18. The magnitude of the radiation field (1602) obtained using the present invention has been minimized along one axis of the plane. This reduced field in a preferred direction allows the use of the present invention adjacent to sensitive circuitry.

FIG. 17, numeral 1700, is a schematic representation of another embodiment of a double spiral, with one spiral (Inner spiral, 1708) inside another spiral (Outer Spiral, 1706), of a planar inductor in accordance with the present invention. A crossover (1704) is utilized to make one of the two terminal connections (Inductor Terminals,1702). The moment due to the inner spiral is equal and opposite to the moment due to the outer spiral. In the far field the total moment is cancelled in all directions.

FIG. 18, numeral 1800, is a diagrammatic representation of a 4-loop single layer planar inductor in accordance with the present invention. The 4 planar adjacent loops/spiral conductor coils (1806, 1808, 1810, 1812) carry a current produced by a signal source. The planar adjacent loops/spiral conductor coils are arranged to form a rhombus to provide total cancellation of a magnetic field on the perpendicular bisectors of the sides of the rhombus, enhanced cancellation of the magnetic field along the short diagonal and reduced cancellation of the magnetic field along the long diagonal. Current flows as described for FIG. 1. The planar magnetic field inductor/transformer may be further implemented as described above. The inductor has two terminals (1802) and has two crossovers (1804, 1814) that connect the centers of each of the two pairs of spirals.

FIG. 19, numeral 1900, is a flow chart of one embodiment of steps of a method in accordance with the present invention. The method maximizes cancellation of a magnetic field over a predetermined range for the plurality of loops/spiral conductor coils arranged to form an inductor/transformer. The method includes the steps of: A) placing (1902) a plurality of at least three planar adjacent similar/dissimilar structured loops/spiral conductor coils interconnected electrically, one after another in a simple/compound loop fashion; and B) injecting (1904) a current produced by a signal source, into the plurality of planar adjacent loops/spiral conductor coils are arranged to maximize cancellation of the magnetic field of the plurality of loops/spiral conductor coils over the predetermined range. The inductor/transformer may be implemented as further described above.

Where selected, as shown in FIG. 20, numeral 2000, the method may maximize cancellation of a total moment of the plurality of loops/spiral conductor coils arranged to form an inductor/transformer, comprising the steps of: A) placing (2002) a plurality of at least three planar adjacent same structure loops/spiral conductor coils interconnected electrically, one after another in a simple/compound loop fashion; B) injecting (2004) a current produced by a signal source, into the plurality of planar adjacent loops/spiral

conductor coils are arranged to maximize cancellation of a total moment of the plurality of loops/spiral conductor coils.

The coupled magnetic field in the plane of the multiloop structure has been computed (FIGs. 21-22) for a 4-loop, 6-loop and 8-loop implementation (see FIGs. 3, 4, 5). The horizontal axis represents distance from the center of the multiloop structure relative to the lateral dimension of the structure. The vertical axis represents a measure of the mutual inductance with a test loop. The coupled magnetic field of the multiloop structure is plotted as a function of distance from the center and compared to the magnetic field for a simple circular loop which has the same inductance. The coupling depends on the direction. A best (FIG. 21-perpendicular to a side of a polygon) and a worst (FIG. 22-along a diagonal of a polygon) case coupling are shown.

In the worst case (2200), the coupling is reduced by 20dB for a 4-loop (2204) structure at a distance of 2 inductor lengths away, as compared to a simple loop (2202). The reduction in coupling for a 6-loop (2206) structure and 8-loop (2208) structure at the same distance is 30dB and 40dB respectively. The reduction in coupling is more than 60dB for a 4-loop structure at 10 inductor lengths away. The 6-loop and 8-loop structure show even smaller coupling at this distance.

FIG. 23, numeral 2300, is a graphical representation of the inductance of a 4-loop spiral inductor implementation of the present invention and a simple circular spiral occupying the same area on a two-layer printed circuit board.

In the best case (2100), the coupling is reduced by at least 80dB for the 4-loop (2104), 6-loop (2106) and 8-loop (2108) structures at 2 inductor lengths away and beyond compared to coupling for a simple circular loop (2102).

FIG. 23, numeral 2300, is a graphical representation of the inductance of a 4-loop spiral inductor (2304) implementation of the present invention and a simple circular spiral (2302) occupying the same area on a two-layer printed circuit board.

FIG. 24, numeral 2400, is a graphical representation of the resistance of a 4-loop spiral inductor (2404) implementation of the present invention and a simple circular spiral (2402) occupying the same area on a two-layer printed circuit board.

FIG. 25, numeral 2500, is a graphical representation of the quality factor (Q) of a 4-loop spiral inductor (2504) implementation of the present invention and a simple circular

spiral (2502) occupying the same area on a two-layer printed circuit board.

For the 4-loop spiral, inductance is reduced and the resistance is increased compared to the simple spiral. However the highest Q obtained is comparable and acceptable for most applications. Higher Q is obtainable by increasing the number of turns in each of the spirals.

The inductance, series resistance and Q of a PCB implementation of the 4-loop planar spiral has been analyzed. The inductance and Q available in a certain area on a PCB with a given resolution has been characterized.

The maximum inductance for a given planar area and a trace width is obtained from a simple spiral. The inductance and quality factor (Q) of a 4-loop spiral is compared to a simple spiral, both made out of the same PCB process.

In one embodiment, shown in FIGs. 27 and 28, numerals 2700 and 2800, the printed circuit board inductor may have a topology that includes at least three consecutively coupled conducting loops/spirals (2702, 2704, 2706; 2802, 2804, 2806) that also form a central conducting loop/spiral (2708; 2808), wherein the conducting loop/spirals are arranged on a polygonal lattice on/in a printed circuit board and an overall

configuration of the conducting loops/spirals is scaled from the topology to provide a zero net moment of the printed circuit board inductor. Where selected, the shapes of each of the conducting loops/spirals may be polygonal.

In one embodiment, the printed circuit board may be multi-layered, and predetermined portions of the conducting loops/spirals may be implemented on different levels (layer 1-2710; layer 2-2712) of the multi-layer printed circuit board and connected by vias to form the printed circuit board inductor.

FIG. 29, numeral 2900, is a schematic representation of positive (2902) and negative (2904) moments with respect to the embodiment of the present invention shown in FIGs. 27 and 28.

In addition, a non-interacting concentric inductor may be arranged in extreme proximity above/below the printed circuit board inductor.

Typically, the printed circuit board inductor has a polygonal shape, and the size and orientation of the printed circuit board inductor is determined by magneto-static analysis. Where the printed circuit board is multi-layered, predetermined portions of the non-interacting concentric

inductor may be implemented on different levels of the multi-layered printed circuit board, The portions of the non-interacting concentric inductor are typically connected by vias to form the complete non-interacting concentric inductor.

As used herein the word "spiral" indicates a winding conducting structure (e.g., a wire, a trace) in a clockwise or counterclockwise direction. A "spiral" thus includes rectangular, polygonal, oval, elliptical, circular as well as other irregular generally spirally shapes.

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

I claim:

1. A planar magnetic field inductor/transformer comprising a plurality of at least three planar adjacent loops/spiral conductor coils coupled serially and arranged one after another in a simple/compound loop fashion, carrying a current produced by a signal source, wherein the plurality of planar adjacent loops/spiral conductor coils are arranged to maximize cancellation of a moment of the plurality of loops/spiral conductor coils over a predetermined range.

2. A planar magnetic field inductor/transformer comprising an even number, 2N, of planar adjacent loops/spiral conductor coils arranged one after another in a simple closed loop, carrying a current produced by a signal source, wherein the even number of planar adjacent loops/spiral conductor coils are arranged to provide total cancellation of a magnetic field on N axes and to maximize overall cancellation of the magnetic field.

3. A method for maximizing cancellation of a total moment of the plurality of loops/spiral conductor coils arranged to form an inductor/transformer, comprising the steps of:

A) placing a plurality of at least three planar adjacent same structure loops/spiral conductor coils interconnected electrically, one after another in a simple/compound loop fashion;

B) injecting a current produced by a signal source, into the plurality of planar adjacent loops/spiral conductor coils are arranged to maximize cancellation of a total moment of the plurality of loops/spiral conductor coils.

4. A method for maximizing cancellation of a magnetic field over a predetermined range for the plurality of loops/spiral conductor coils arranged to form an inductor/transformer, comprising the steps of:

A) placing a plurality of at least three planar adjacent dissimilar structured loops/spiral conductor coils interconnected electrically, one after another in a simple/compound loop fashion;

B) injecting a current produced by a signal source, into the plurality of planar adjacent loops/spiral conductor coils are arranged to maximize cancellation of the magnetic field of the plurality of loops/spiral conductor coils over the predetermined range.

5. A printed circuit board inductor having a topology comprising:

A) a first conducting loop/spiral;

B) a second conducting loop/spiral coupled to the first conducting loop/spiral;

C) a third conducting loop/spiral coupled to the second conducting loop/spiral, and, where selected, further conducting loops/spirals consecutively coupled; and

D) a central conducting loop/spiral formed by the at least first, second and third conducting loops/spirals,

wherein the conducting loop/spirals are arranged on a polygonal lattice on/in a printed circuit board and an overall configuration of the conducting loops/spirals is scaled from the topology to provide a zero net moment of the printed circuit board inductor.

6. The printed circuit board inductor of claim 5 wherein the shapes of each of the conducting loops/spirals are polygonal.

7. The printed circuit board inductor of claim 5 wherein the printed circuit board is multi-layered and predetermined portions of the conducting loops/spirals are implemented on different levels of the multi-layered printed circuit board and are connected by vias to form the printed circuit board inductor.

8. The printed circuit board inductor of claim 5 further including a non-interacting concentric inductor arranged in extreme proximity above/below the printed circuit board inductor.

9. The printed circuit board inductor of claim 8 wherein the printed circuit board inductor has a polygonal shape and a size and orientation of the printed circuit board inductor is determined by magneto-static analysis.

10. The printed circuit board inductor of claim 8 wherein the printed circuit board is multi-layered and predetermined portions of the non-interacting concentric inductor are implemented on different levels of the multi-layer printed circuit board and are connected by vias to form the non-interacting concentric inductor.

FIG. 1

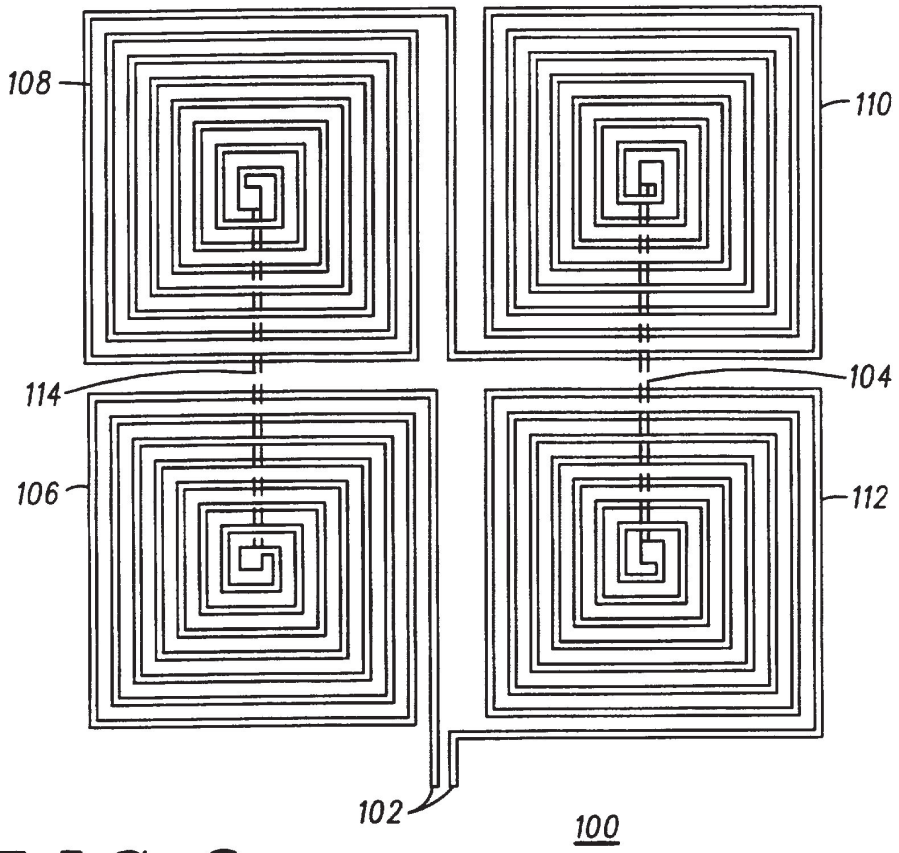


FIG. 3

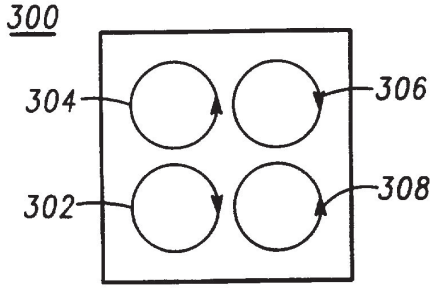


FIG. 4

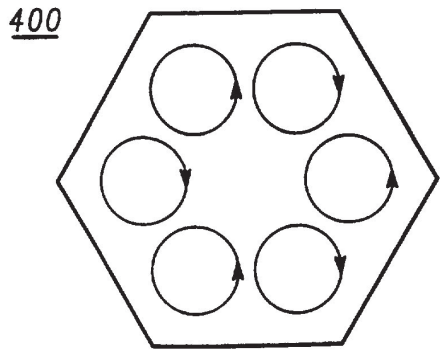
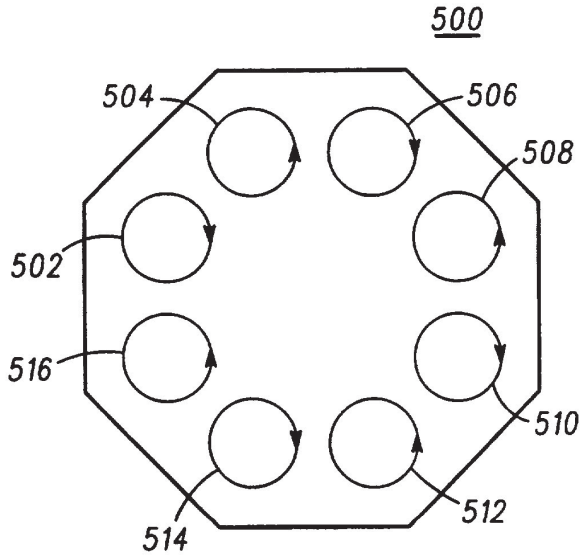


FIG. 5



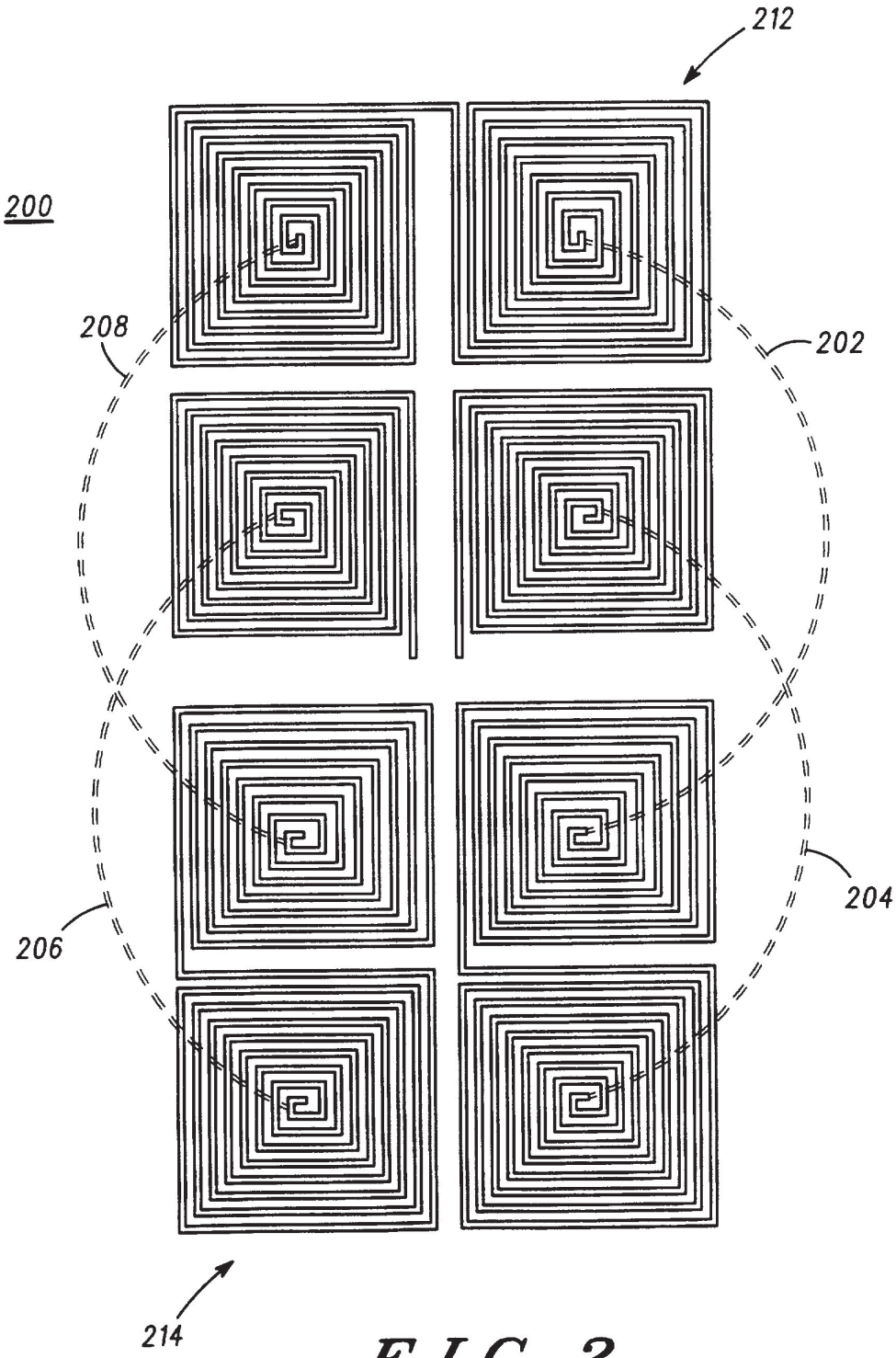


FIG. 2

FIG. 6

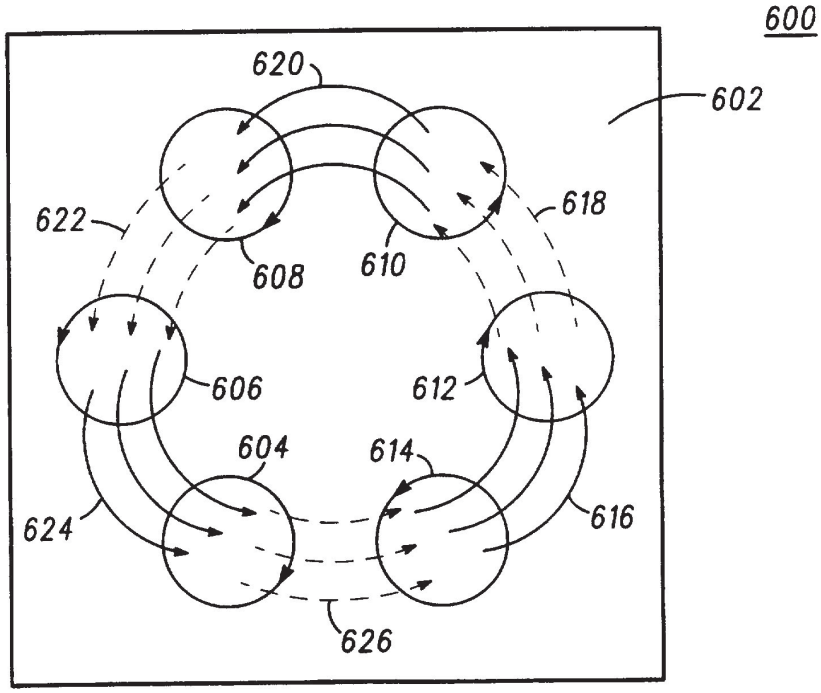


FIG. 7

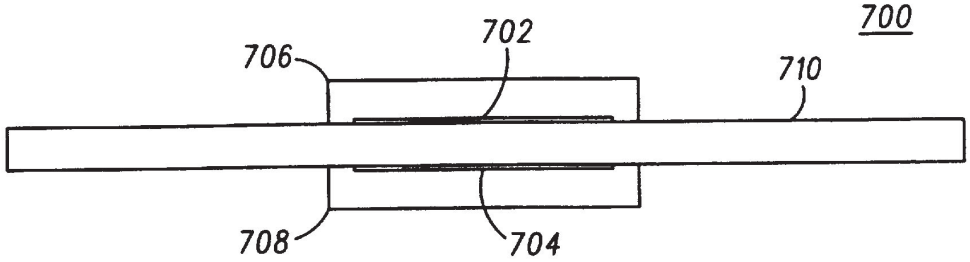


FIG. 8

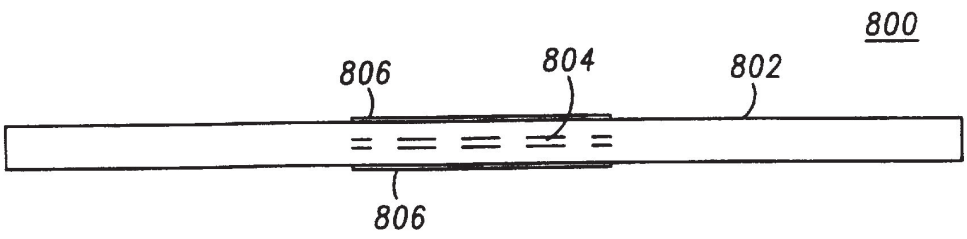


FIG. 9

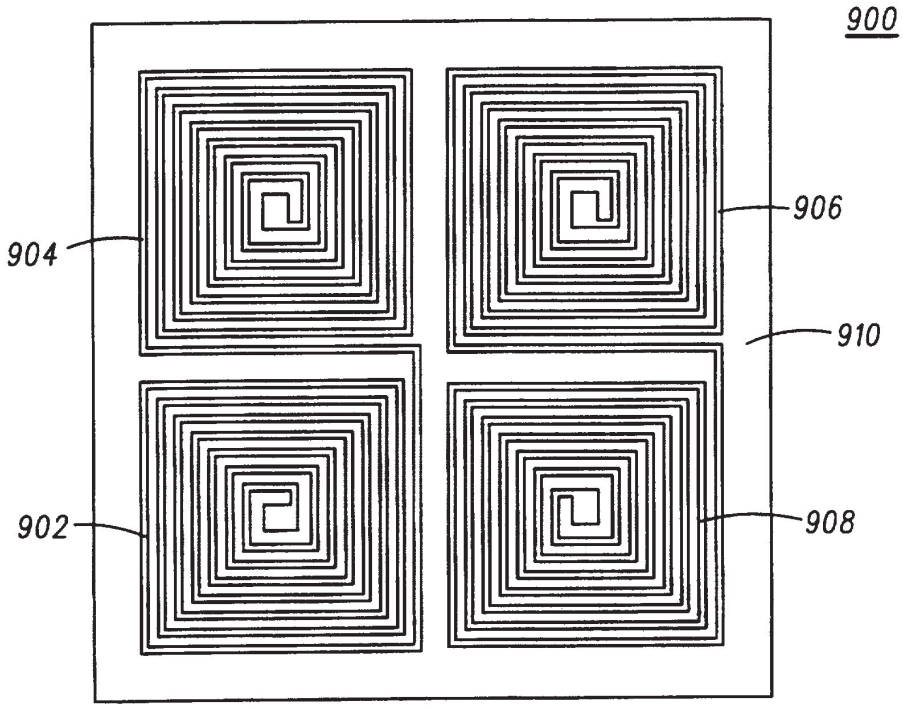
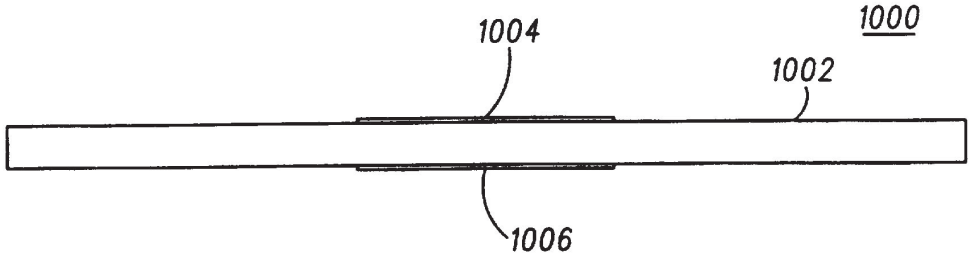


FIG. 10



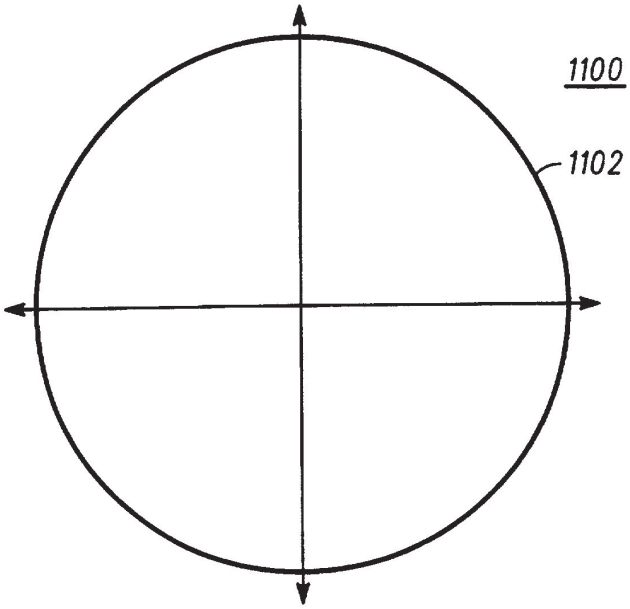


FIG.11

FIG.12

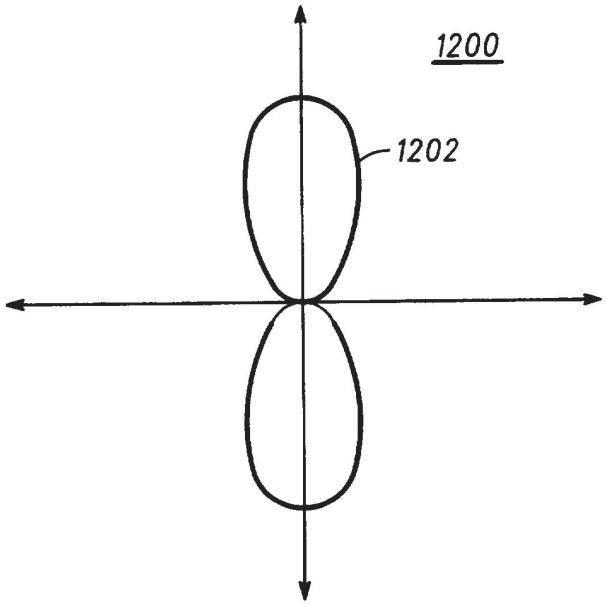


FIG.13

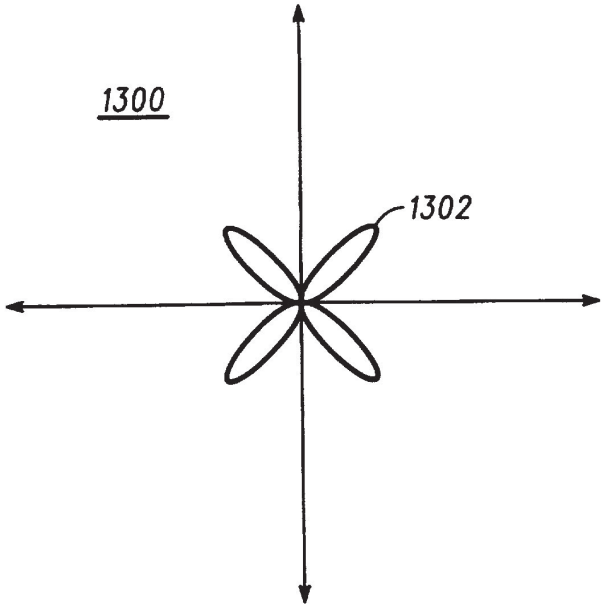


FIG.14

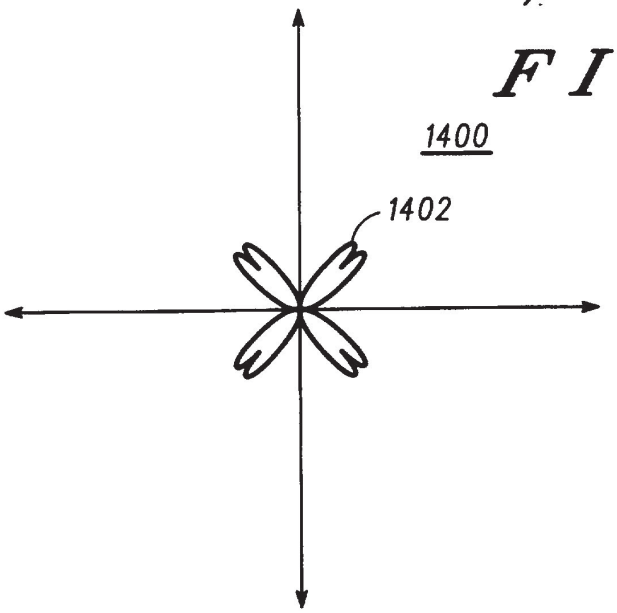


FIG.15

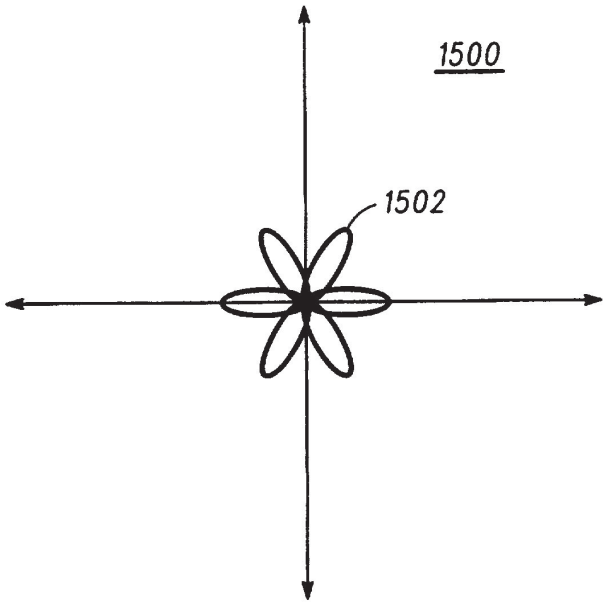
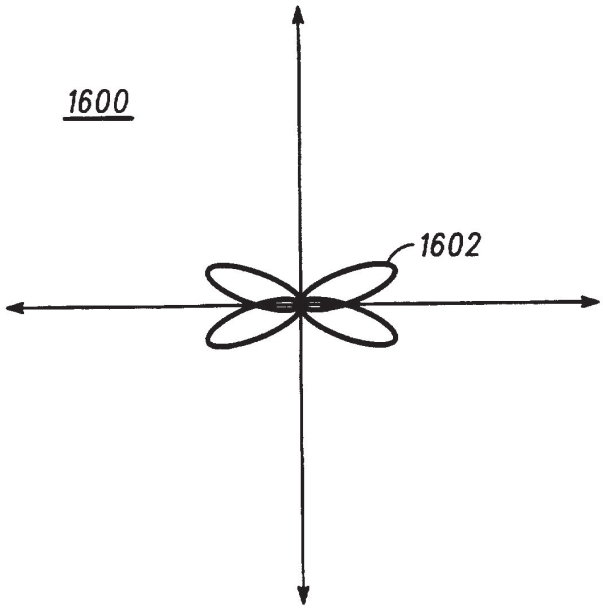


FIG.16



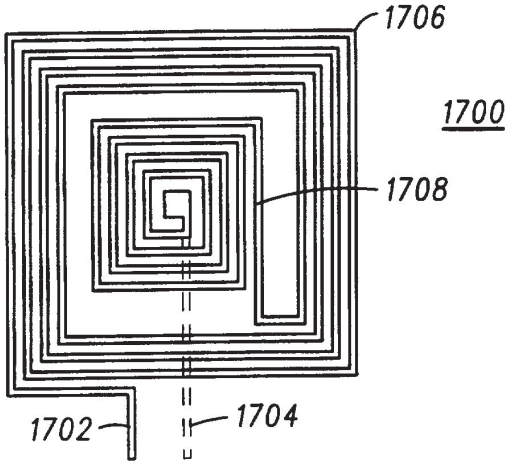


FIG.17

FIG.18

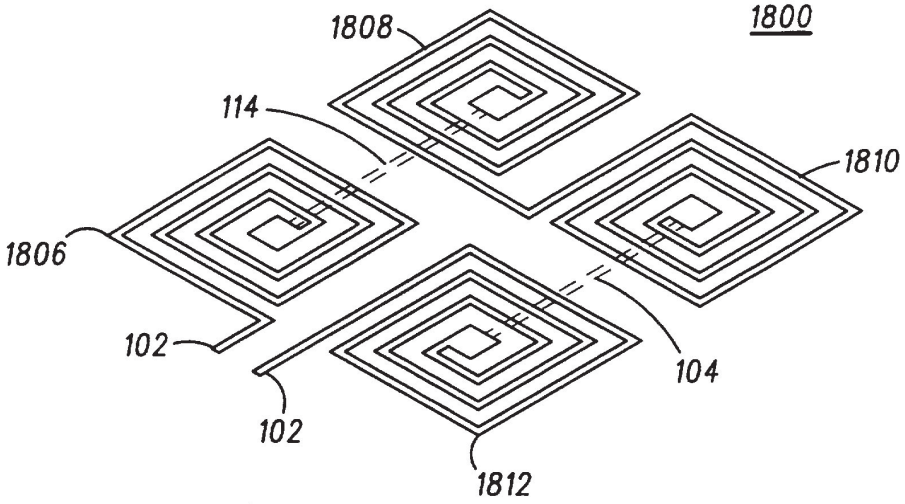


FIG.19

1900

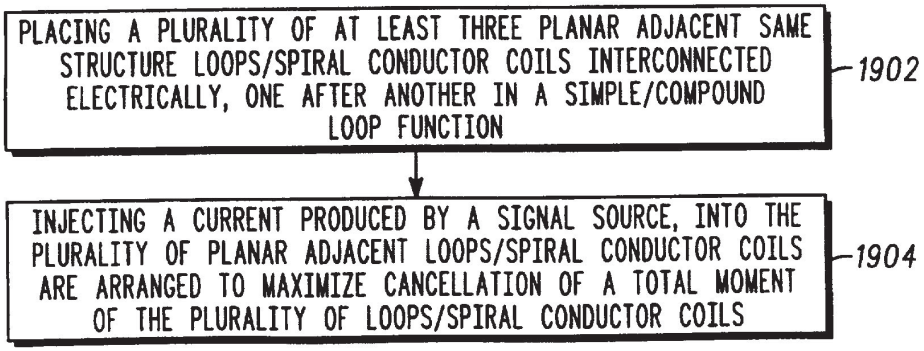


FIG. 20

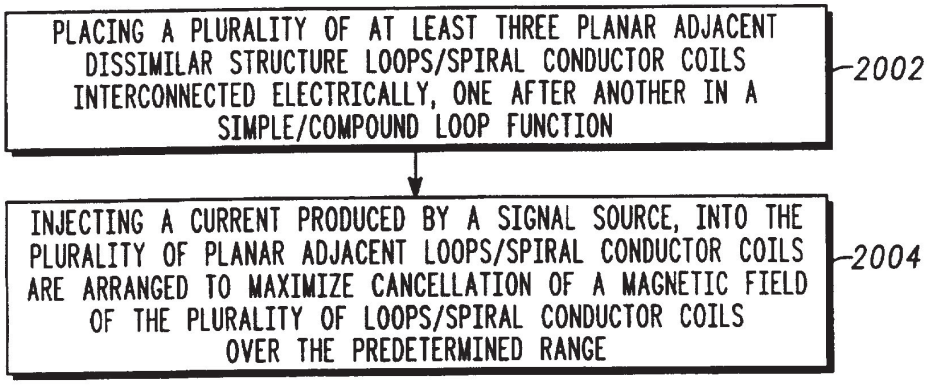

2000
PLACING A PLURALITY OF AT LEAST THREE PLANAR ADJACENT DISSIMILAR STRUCTURE LOOPS/SPIRAL CONDUCTOR COILS INTERCONNECTED ELECTRICALLY, ONE AFTER ANOTHER IN A SIMPLE/COMPOUND LOOP FUNCTION
2002
INJECTING A CURRENT PRODUCED BY A SIGNAL SOURCE, INTO THE PLURALITY OF PLANAR ADJACENT LOOPS/SPIRAL CONDUCTOR COILS ARE ARRANGED TO MAXIMIZE CANCELLATION OF A MAGNETIC FIELD OF THE PLURALITY OF LOOPS/SPIRAL CONDUCTOR COILS OVER THE PREDETERMINED RANGE
2004

FIG. 21

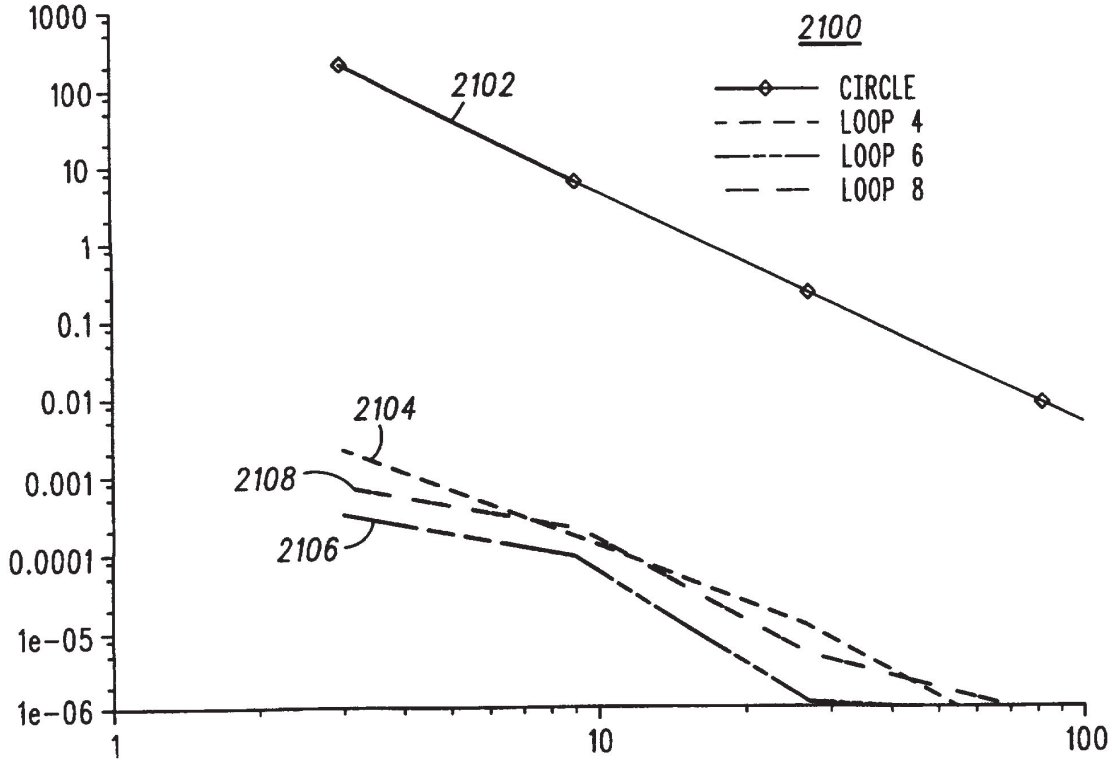

2100
1000
100
10
1
0.1
0.01
0.001
0.0001
1e-05
1e-06
1
10
100
2102
2104
2106
2108
CIRCLE
LOOP 4
LOOP 6
LOOP 8

FIG. 22

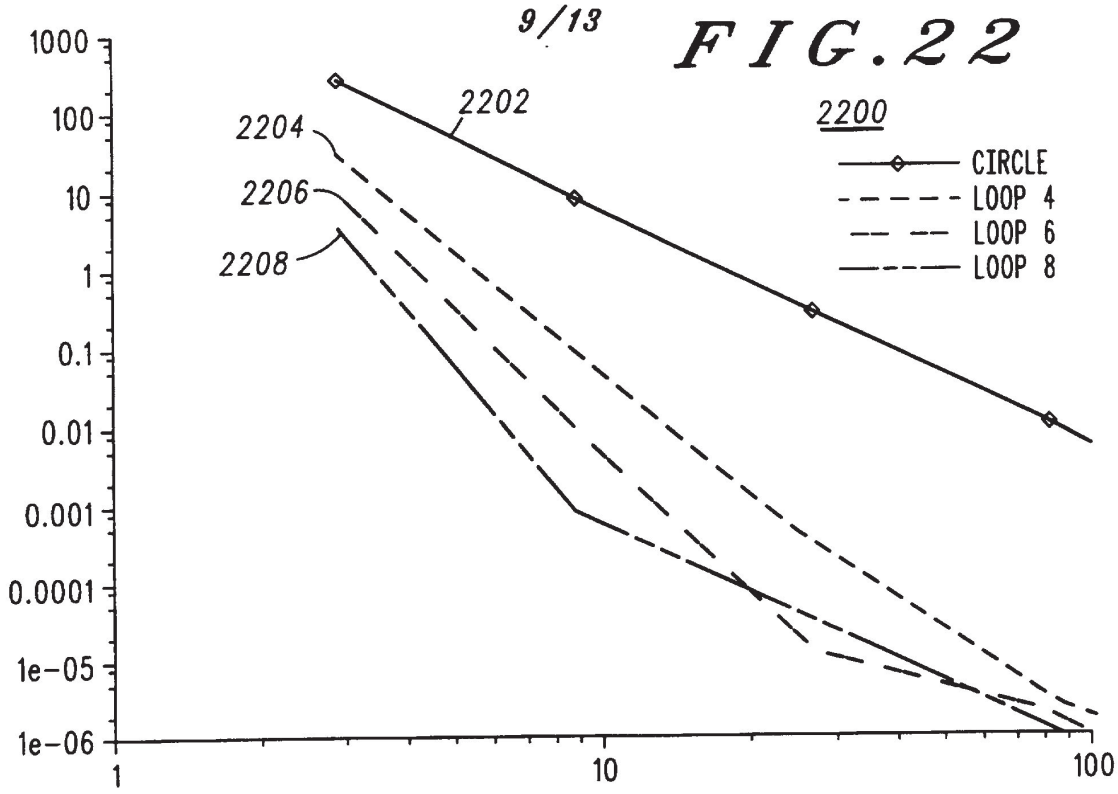

1000
100
10
1
0.1
0.01
0.001
0.0001
1e-05
1e-06
1
10
100
2200
2202
2204
2206
2208
CIRCLE
LOOP 4
LOOP 6
LOOP 8

FIG. 23

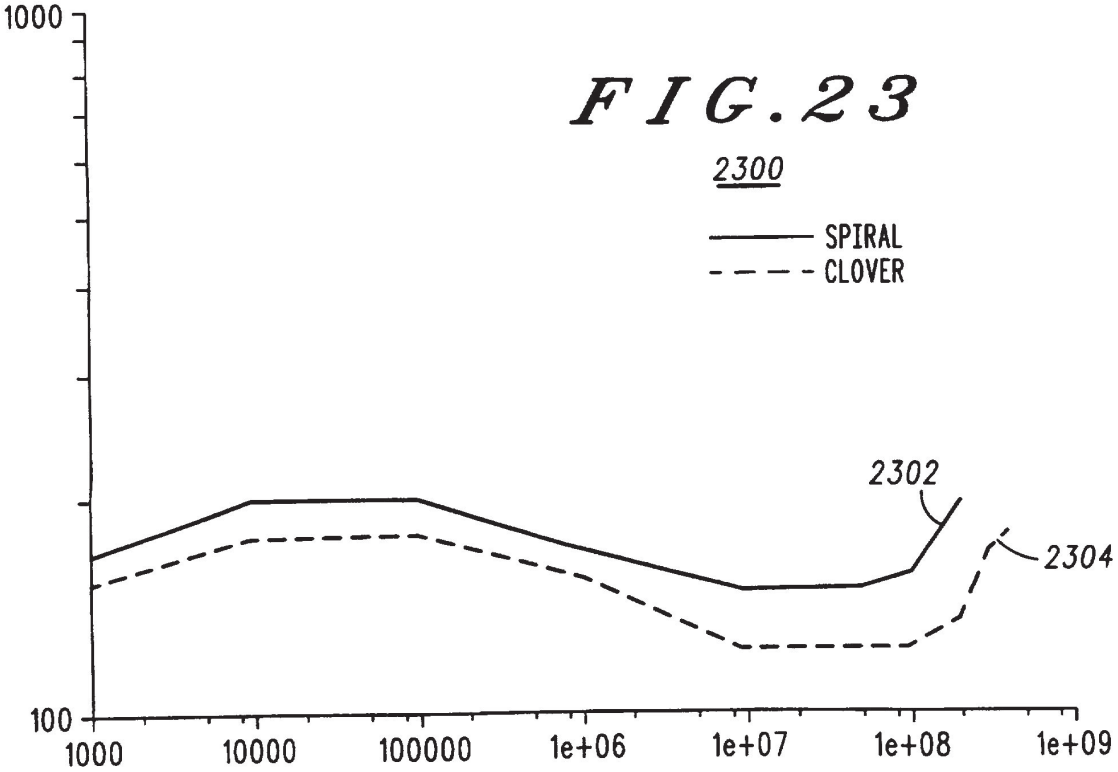

1000
100
1000
10000
100000
1e+06
1e+07
1e+08
1e+09
2300
SPIRAL
CLOVER
2302
2304

FIG. 24

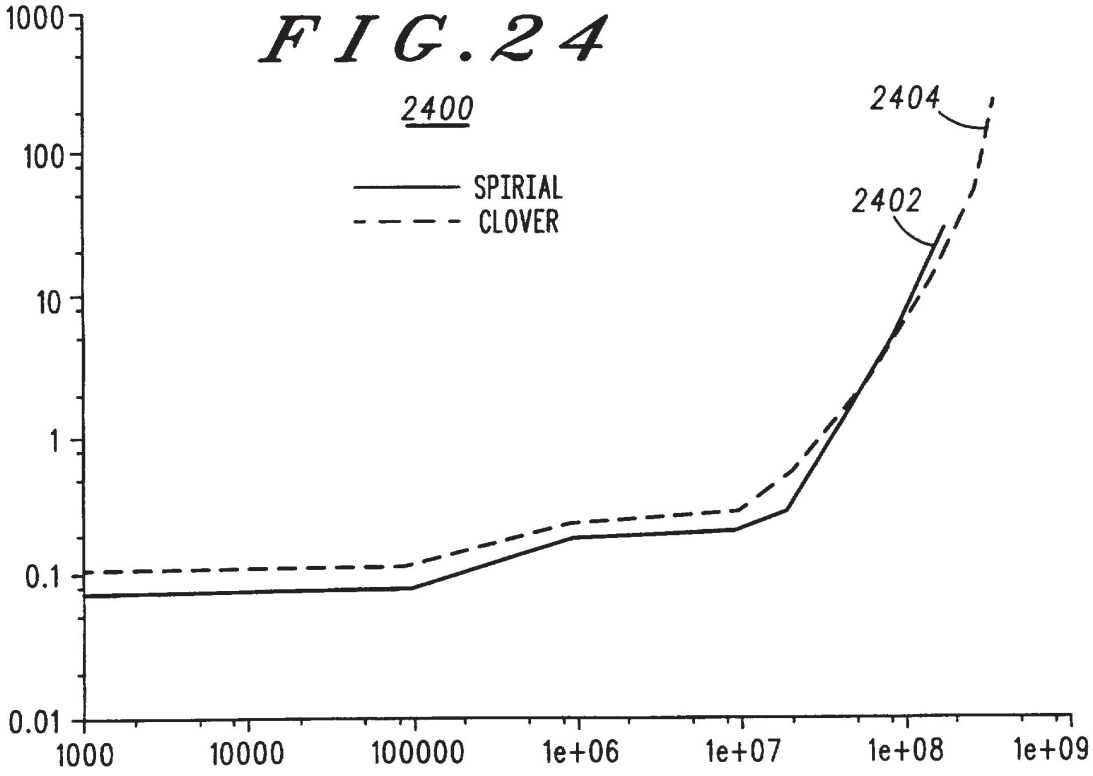
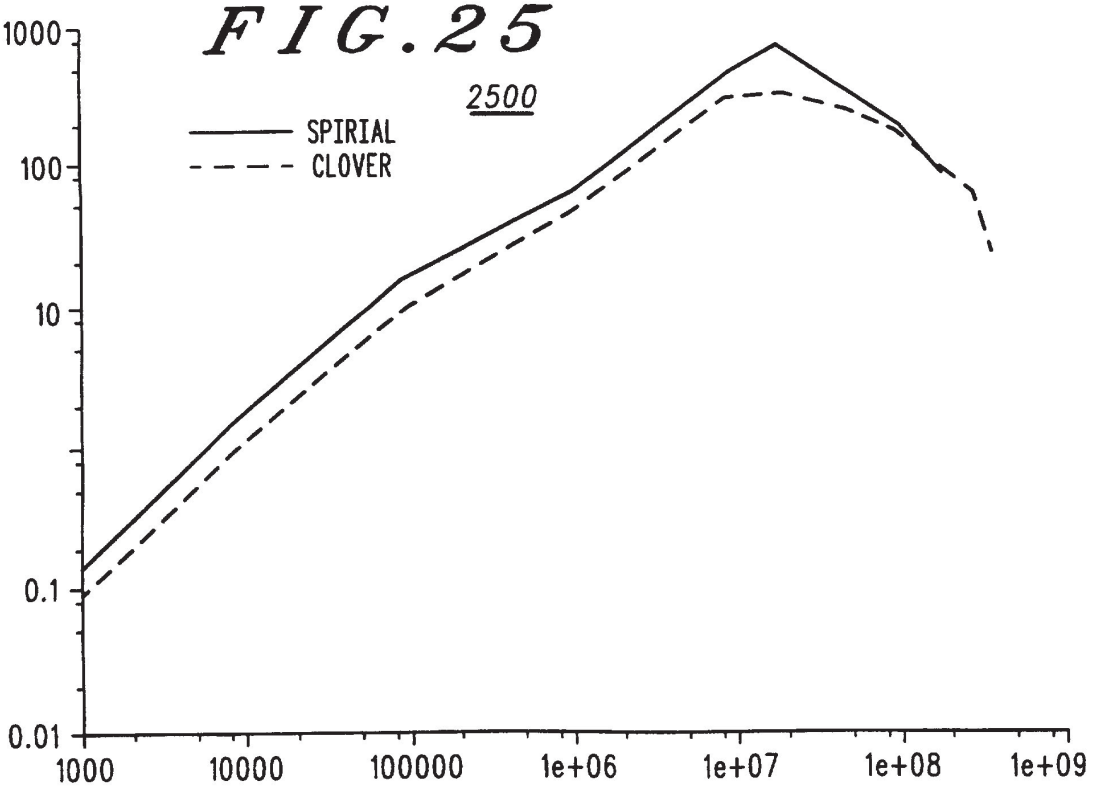

2400
SPIRIAL
CLOVER
2404
2402
1000
100
10
1
0.1
0.01
1000
10000
100000
1e+06
1e+07
1e+08
1e+09

FIG. 25


2500
SPIRIAL
CLOVER
1000
100
10
0.1
0.01
1000
10000
100000
1e+06
1e+07
1e+08
1e+09

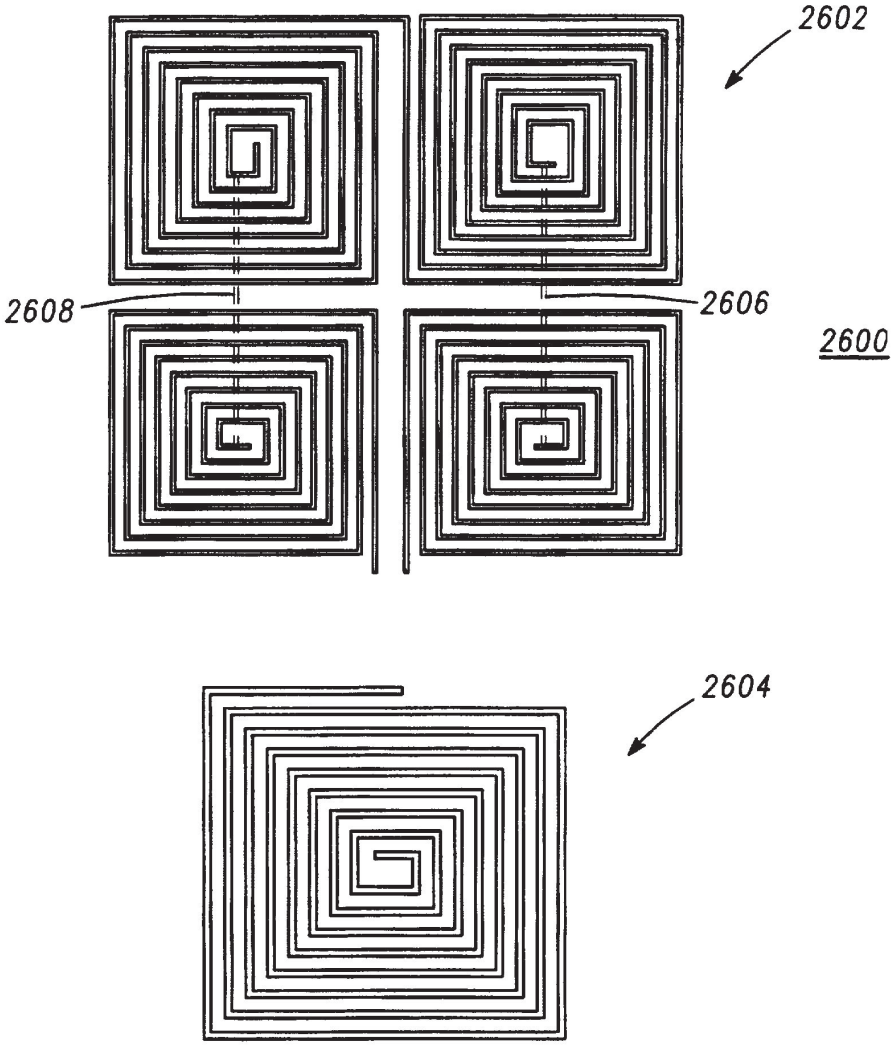


FIG. 26

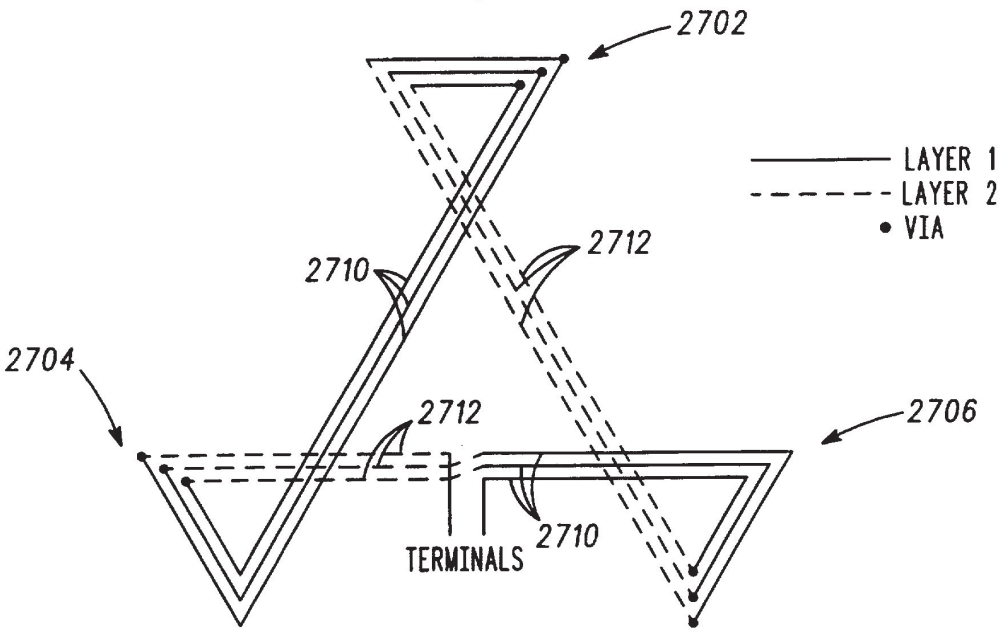

2702
LAYER 1
LAYER 2
• VIA
2712
2710
2704
2712
2706
2710
TERMINALS
2700

FIG. 27

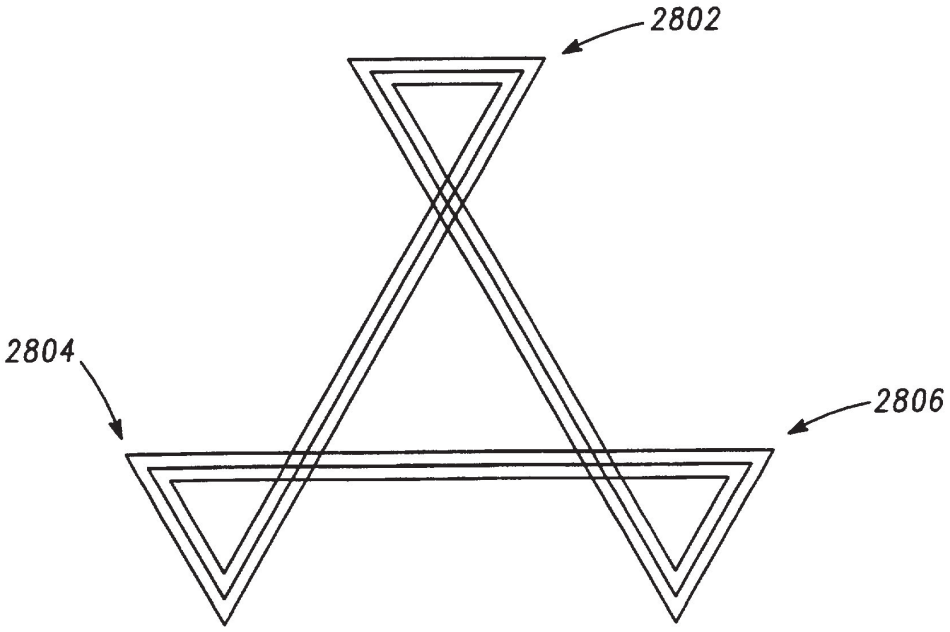

2802
2804
2806
2800

FIG. 28

FIG.29

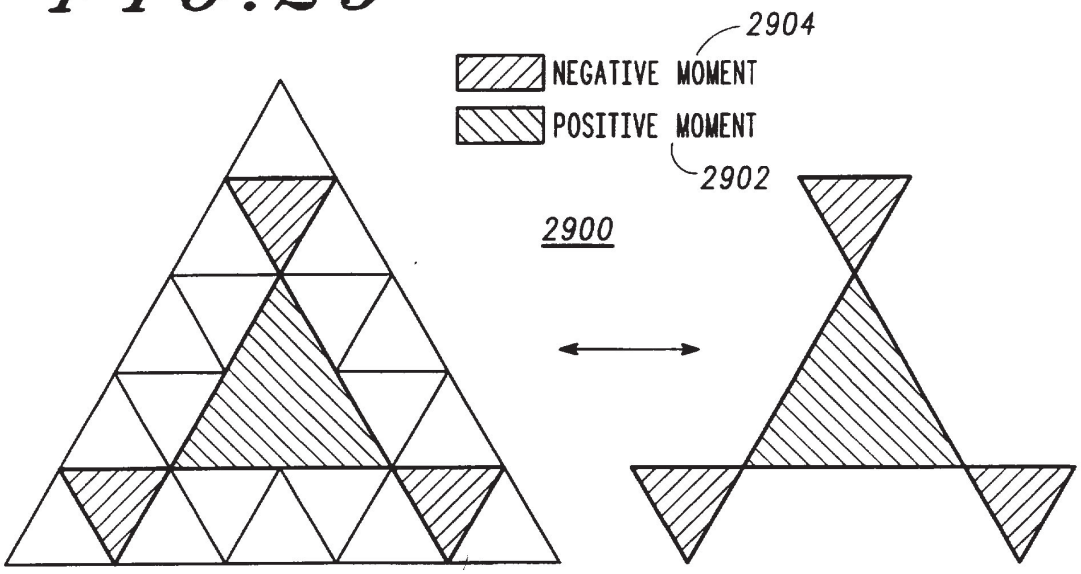
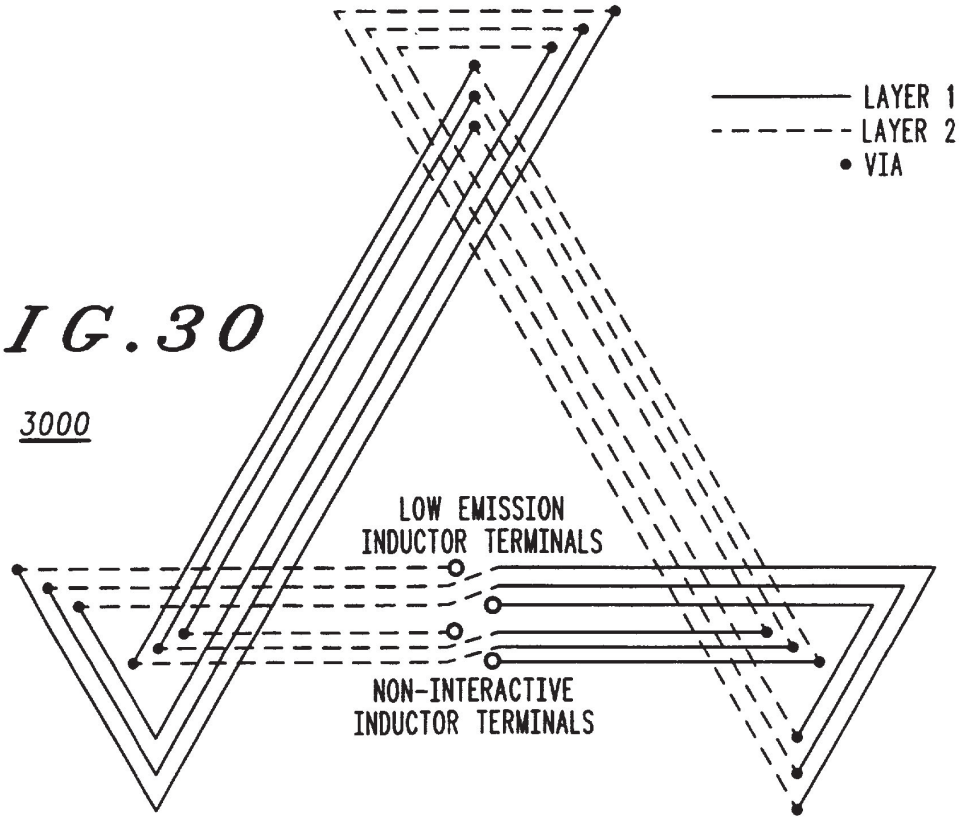

2904
NEGATIVE MOMENT
POSITIVE MOMENT
2902
2900

FIG.30


LAYER 1
LAYER 2
VIA
3000
LOW EMISSION
INDUCTOR TERMINALS
NON-INTERACTIVE
INDUCTOR TERMINALS

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/11900

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H01F 27/28, 27/30
US CL :336/171,180,200,223,232
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 336/171,180,200,223,232,83,206,212 H01F 15/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,572,179 A [ITO et al] 05 May 1995, col.3, lines 20-46; col. 5, lines 64-69.	1-6
---		-----
Y	see col. 5, lines 64-69	9
Y	US 4,959,631 A [HASEGAWA et al] 25 September 1990 (25/09/90), col. 1, lines 19-23; col. 4, lines 14-20.	6-7, 10
Y	US 5,583,474 A[MIZOGUCHI et al] 10 December 1996 (10/12/96), col. 10, lines 46-60; col. 11, lines 4-10.	6-7, 10
Y	JP 3-82106 A [KANEKO] 08 APRIL 1991 (08/04/91), see the abstract and constitution.	9

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
28 AUGUST 1997	27 OCT 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer ANH MAI Telephone No. (703) 308-2800

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/11900

B. FIELDS SEARCHED
Electronic data bases consulted (Name of data base and where practicable terms used):

APS, search terms: spiral inductor, polygonal, topology, magnetostatic
IPC, search terms: spiral inductor, polygonal, topology, magnetostatic

INTEL-1007
U.S. Patent 7,151,430