

# A Single-Chip 900-MHz Spread-Spectrum Wireless Transceiver in 1- $\mu$ m CMOS—Part I: Architecture and Transmitter Design

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**Abstract**—A single-chip transceiver for frequency-hopped code division multiple access (CDMA) in the 900 MHz industrial, scientific and medical (ISM) band is implemented in 1- $\mu$ m CMOS. It combines a digital frequency synthesizer, a double quadrature upconverter, an integrated oscillator, and a power amplifier with variable output. Data modulates a carrier hopping at 20 kHz with quaternary frequency-shift keying (4-FSK). At an output power level of +3 dBm, the harmonics and spurious tones lie at  $-52$  dBc or below. When active, the transmitter drains 100 mA from 3 V.

## I. INTRODUCTION

THERE is much interest today in the single-chip wireless transceiver which consumes a small amount of power, needs no off-chip components, supports voice and data traffic over short ranges by transmitting a modest power, implements power control, and is resilient to interferers. For many semiconductor companies this transceiver is particularly important if it is fabricated in the CMOS technology they use for their other IC products. This companion set of two papers reports on the design and performance of the first such integrated CMOS transceiver, developed for spread-spectrum code division multiple access (CDMA) operation in the 902–928 MHz industrial, scientific, and medical (ISM) frequency band.

Over the years, radio communication across any significant distance was strictly regulated by issue of a license to transmit on precisely defined frequencies, with upper limits prescribed on the bandwidth of the transmitted signal and on its power level. With the advent of cellular and cordless telephones, the need for broad interoperability specifies, in addition, a modulation format and channel-access protocols. The Federal Communications Commission (FCC) has also opened up three frequency bands for unlicensed use in ISM applications. Instead of assigning fixed frequencies to certain users by license, multiple users gain access to these bands by spreading the transmitted spectrum according to uncorrelated pseudonoise (PN) codes [1]. The FCC rules (Part 15.249) permit spreading either by direct-sequence modulation or by frequency hopping

of the carrier, as long as the user spreads the signal by at least a certain amount. For instance, in the case of frequency hopping, the user must cover 50 distinct frequency slots before the hopping sequence repeats. The maximum transmitted power is limited to 1 W, and the out-of-ISM band emission must be 50 dB lower than the in-band transmitted power. There is free choice of modulation scheme.

The ISM band gives great flexibility in the design of wireless equipment. From the researcher's perspective, it is now possible to explore the multidimensional design space comprising modulation scheme, spreading method, transceiver architecture, and circuit building blocks, with the goal of finding the most compact transceiver, or one that consumes the least power at a given performance. This approach underlies the transceiver development described here. The goal is to develop a wireless device operating in microcells at a data rate of up to 160 kb/s, implemented entirely in the MOSIS 1- $\mu$ m CMOS technology available at the inception of this project.

The next section summarizes the transceiver operation and some of the important architectural choices. Following that, the transistor-level circuit design of the key building blocks in the transmitter portion is described, and then the section on experimental results presents and discusses the collective performance of the entire transmitter portion of the transceiver. The companion paper covers the receiver architecture and broader issues of single-chip integration.

## II. TRANSCIEVER ARCHITECTURE

The transceiver (Fig. 1) implements a customized *frequency-hopped spread-spectrum* (FH-SS) radio system [2]. Any spread-spectrum communication provides an inherent immunity to multipath fading, but with frequency hopping the front-end signal processing takes place at the *hopping rate*, which is much lower than the *chip rate* required in direct-sequence SS [1] to spread the spectrum over a wide bandwidth. Thus, if a compact agile frequency synthesizer is available, a frequency-hopped transceiver potentially offers the lower power implementation.

With FH-SS, there is also wider choice of modulation. The modest data rate in this system may be conveyed by frequency-shift keying (FSK) the carrier. Among the various types of multilevel FSK, quaternary FSK (4-FSK) uses bandwidth most

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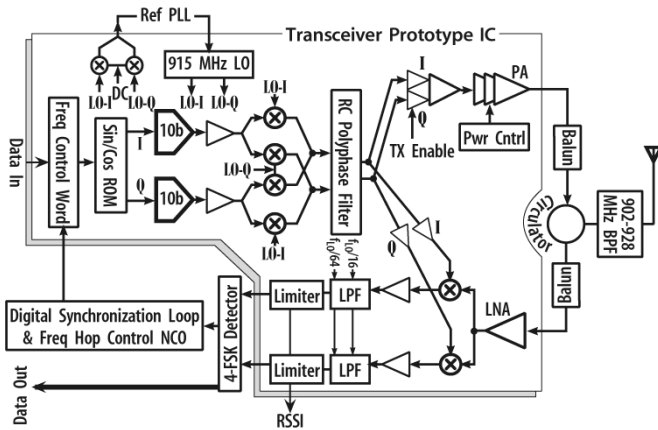


Fig. 1. Transceiver block diagram.

efficiently at low levels of error probability [3], [4]. It maps a pair of binary data bits to one of four equally spaced offsets of the carrier frequency ( $f_c$ ), that is  $f_c \pm \Delta f$  and  $f_c \pm 3\Delta f$ , or as here,  $f_c \pm 2\Delta f$ . 4-FSK symbols are at half the base data rate. A noncoherent receiver detects data by sensing the outputs of four bandpass filters centered at the offset frequencies. This is much simpler than a receiver for direct-sequence SS communication systems, whose operation at least requires phase recovery, and whose front-end clocks at some high chip rate. On the other hand, a direct-conversion, or zero-IF, architecture is well suited to receive FSK [5] and is recognized as the best candidate for monolithic integration.

The transceiver's block diagram is first described at the top level. Subsequent sections cover each block in greater detail. Finally, the overall performance of the transmitter in the integrated transceiver is reported.

Fig. 1 shows a baseband *direct-digital frequency synthesizer* (DDFS) used as an agile frequency synthesizer and data modulator. The DDFS creates digital samples of a baseband sinusoidal waveform by addressing a sine ROM at a frequency set by a 24-b control word. Two 10-b D/A converters (DAC's) map the 10-b words at the DDFS outputs into discrete analog samples. The quadrature outputs synthesize a complex FH-SS (in the sense of magnitude and phase) at baseband. A *fixed-frequency oscillator* upconverts these outputs to the ISM band in a single-sideband mixer. With the oscillator frequency at the center of the ISM band, 915 MHz, either the upper or the lower sideband may be selected. The DDFS/DAC output frequency then need only span 0 to 13 MHz to cover the ISM range of  $915 \pm 13$  MHz. The circuits are designed flexibly so that if for practical reasons the oscillator frequency must be lowered, the DDFS/DAC output frequency may be raised by  $2\times$  to maintain the transmitted frequencies within the ISM band.

After upconversion, a power amplifier (PA) drives the antenna with the modulated hopped carrier. The maximum PA output is 20 mW into  $50 \Omega$  (+13 dBm), sufficient for operation in microcells with 100 m diameter, or for communication over 1 km over an unobstructed line-of-sight link. A key feature is that a 5-b digital word controls the output power over a 30 dB range, to a minimum value of 20  $\mu$ W. Accurate power control

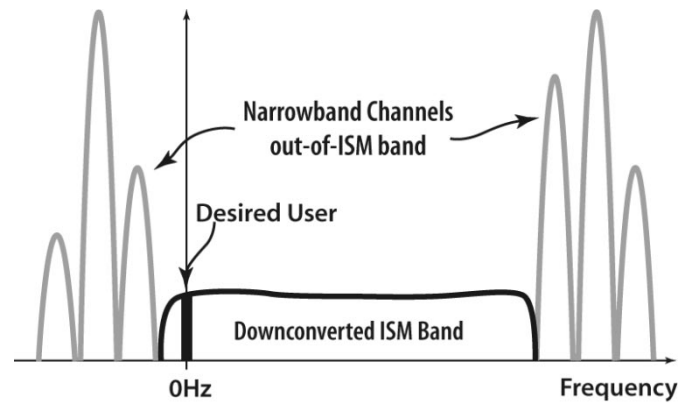


Fig. 2. Downconverted ISM-band frequency-hopped spectrum in a direct-conversion receiver and the large narrowband signals that surround it.

by the basestation over this dynamic range is necessary to achieve the potential user capacity of an FH-CDMA system [6].

An off-chip passive dielectric resonator filter between the PA and antenna suppresses out-of-band signals at the transmitter output. These out-of-band signals may be generated within the transmitter, for instance the images around the clock frequency of the discrete-time waveforms. Internally, the dielectric filter comprises three coupled resonators tailored to a passband spanning 902–928 MHz, a 50-MHz-wide transition band, and an eventual stopband loss of 40 dB (see Fig. 32 for the filter response over a limited frequency range). The passband insertion loss is about 1.5 dB.

Users of a CDMA wireless systems all transmit and receive in the same frequency band and distinguish themselves by a unique spreading code. The receiver is tuned to the 902–928 MHz band and the same dielectric filter used reciprocally acts as the RF preselect filter. The received FH-FSK is concurrently *despread and downconverted* to zero-IF in the receiver front end. The DDFS-based agile frequency synthesizer, after upconversion but without modulation, is used as the local oscillator (LO) in the downconversion mixers (Fig. 1). A baseband circuit [7] synchronizes the LO to the spreading code, that is, the hopping pattern, of the user of interest, by always downconverting that user's carrier frequency to dc and downconverting *all other* users of the ISM band as well, but to frequencies positioned away from dc (Fig. 2). The receiver discriminates positive FSK offsets ( $+\Delta f$  and  $+2\Delta f$ ) from negative offsets ( $-\Delta f$  and  $-2\Delta f$ ) in quadrature downconversion paths [5]. A *low-pass channel-select filter* in each path passes only the selected user's received signal and suppresses neighboring users.

As in most FM receivers, a simple *limiting amplifier* boosts the received signal to binary levels whose zero crossings contain the modulation. No linear automatic gain control (AGC) is necessary. A digital detector correlates the limited signals in the quadrature channels with the four expected frequency offsets, makes a decision based on the strongest correlation over each symbol, and maps the result to a pair of data bits [7], [8]. The correlation detector also creates early-late data words for a digital phase-locked loop (PLL)

to align the LO hopping pattern and the symbol timing clock in the detector [7], [9].

The transmitter and receiver operate in time-division duplex. As they share the same prefilter, in principle the PA output may be connected to the low-noise amplifier (LNA) input, and a common matching network may transform the shared node impedance to the antenna impedance [10]. However, no one network could be found to match the shorted-together PA and LNA ports to  $50\ \Omega$  in both transmit and receive modes. Instead, separate matching networks are used at each port, and a passive circulator combines the matched outputs into the antenna. The circulator introduces a loss of about 1 dB, which degrades the receiver noise figure. Alternatively, a low-loss RF switch could be used.

### III. CIRCUIT DESIGN

#### A. Direct Digital Frequency Synthesizer

Direct digital frequency synthesis is the best way to create rapidly hopping frequencies. The DDS table-lookup process is feedforward and memoryless, where the programmable ramp rate of an accumulator sets the instantaneous output frequency. Therefore, the output waveform changes with continuous phase from one frequency to any other in one clock cycle. By contrast, the limited loop bandwidth of a PLL-based frequency synthesizer prolongs the settling time. PLL's are usually narrowband to lower spurious tones caused by reference feedthrough, and they require large-modulus dividers to finely resolve frequency resolution. This further lowers bandwidth [11]. To meet FCC regulations on the 900-MHz ISM band, this transceiver hops in a pseudorandom pattern across 54 different frequencies uniformly covering the band (Fig. 3), requiring a frequency resolution of 482 kHz in the synthesizer. For frequency diversity, the system combines *block interleaving* of the data with hopping the carrier once every four transmitted symbols, that is at 20 khops/s. The two requirements of agility and frequency resolution will conflict in a PLL, but resolve in the DDS.

DDFS-based frequency synthesizers are often thought to dissipate a large power. The ROM must use a large internal wordlength to synthesize spectrally pure sinewaves, and therefore its power dissipation is large, particularly at high clock rates. The DDS is usually clocked at 5 to  $6\times$  the highest synthesized frequency, to relax the analog filter which conventionally follows it to remove the image tones around the clock. The DAC after the DDS must operate at the same clock rate and resolve 10 b or more to achieve the required spectral purity in wireless systems. Most importantly, dynamic distortion in the DAC creates spurious tones, and low distortion at high clock rates is often obtained at the price of a disproportionate rise in power dissipation. The challenge, then, is how to implement a DDS and DAC synthesizing frequencies of tens of megahertz with spurious tones below, say  $-55\ \text{dBc}$ , at a power dissipation acceptable for a battery-operated device.

Various techniques to compress the size of the sine ROM in a DDS [12], [13] have been used in CMOS DDS IC's which

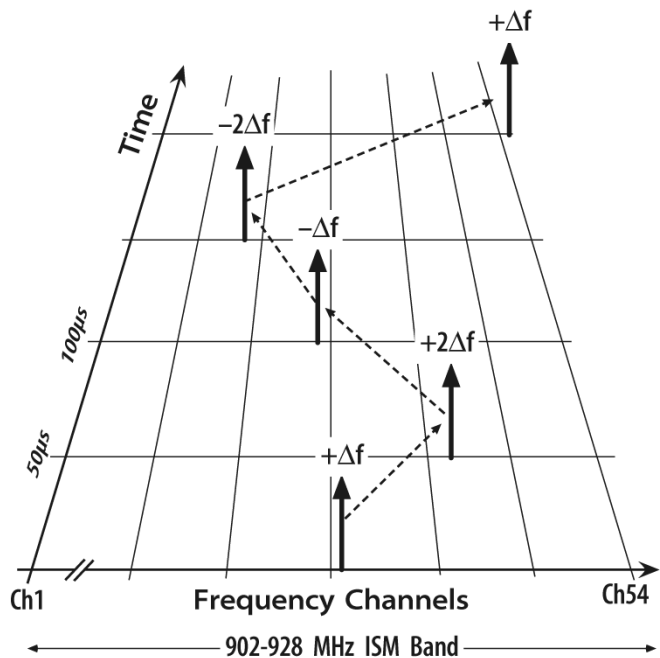


Fig. 3. Illustrating this transceiver's frequency hopping pattern in the ISM band and 4-FSK modulation on the carrier.

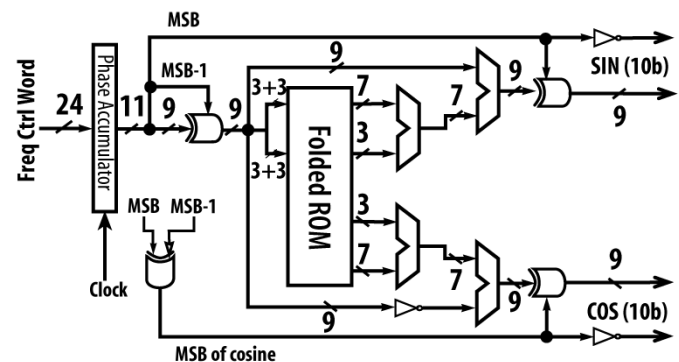


Fig. 4. Block diagram of direct digital frequency synthesizer (DDFS).

produce digital sinewaves with very high spectral purity [14]. Low power dissipation was not necessarily a goal in those implementations; however, it is here [15]. The DDS (Fig. 4) is implemented with scalable digital cells, whose size is the smallest required to clock at 100 MHz from a 3-V supply. The internal wordlengths guarantee that the spectral impurities of any synthesized sinewave lie below  $-72.6\ \text{dB}$ . In practice, dynamic nonlinearities from the DAC will create much larger spurious tones in the synthesized analog waveform.

The ROM used here is  $32\times$  smaller than a straightforward design containing all the coefficients of one full cycle of a sinewave. This small size arises from four simplifications. First, a full sinewave is reconstructed by addressing stored coefficients for only a quarter of a cycle of a sinewave. Second, by phase shifting its input address, one ROM is made to yield both sine and cosine outputs. Third, the ROM stores the difference between magnitude and phase of sinewave samples, which lowers the stored wordlength by 2 b. And fourth, one large table in the ROM is replaced by a coarse table and a

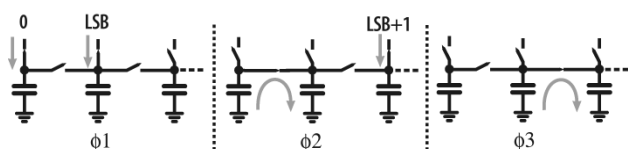


Fig. 5. Principle of quasi-passive binary-weighted DAC showing charge-transfer across the three clock phases.

second fine interpolation table. When clocked at 80 MHz, this DDFS dissipates 54 mW from 3 V.

### B. D/A Converter

DAC's operating at clock rates of hundreds of megahertz normally use current steering. Although this is originally a bipolar circuit technique exploiting the differential pair as a fast current switch, it has also been used at video rates in CMOS. With proper division between binary and segmented current sources, these DAC's display static integral linearity approaching 12 b without trimming, but "glitches," or code-dependent transients, in current switching causes their performance to degrade at high clock rates. Glitches in the discrete-time steps when the DAC synthesizes a sinewave create spurious tones (spurs) in its frequency spectrum. Often the glitch size depends nonlinearly on the codes, producing nonharmonic spurs. The spurs lying close to the sinewave frequency cannot be filtered.

This transceiver uses a glitch-free high-speed CMOS DAC. The DAC samples-and-holds each discrete-time output for two-thirds of the clock period while the next output is being calculated; it then resets to zero over the remaining one-third of the clock period. The core of the DAC works on the principle of charge bisection in an array of equal-valued capacitors connected by FET switches [16] (Fig. 5). This is a circuit-level implementation of a charge-transfer device, and as in a charge-coupled device (CCD), proper operation requires a clock with three nonoverlapping phases to ensure unidirectional charge flow from least significant bit (LSB) to most significant bit (MSB). Starting from an initial capacitor charged low at the start of every clock cycle, capacitors are precharged to either a low ( $V_{LO}$ ) or a high ( $V_{HI}$ ) reference voltage depending on the bit value. Then, the charge is bisected by redistribution with the capacitor to the right. After propagating through  $N$  stages, the charge is equal to the reference value  $C(V_{HI} - V_{LO})$  binary-weighted by  $N$  bits, with a superimposed fixed offset charge  $CV_{LO}$ . This offset is unimportant in a differential implementation.

The operation of this D/A converter is pipelined to yield a new conversion every clock cycle [16]. The least-significant 3-b nibble of the current DAC input word is applied to the first three DAC stages, which interact in a sequence set by the three phases of the clock; the next 3-b nibble, delayed by one clock cycle, is applied to the next three stages; the next 3-b nibble is delayed by two clocks, and so on (Fig. 6).

A 10-b DAC is implemented by 11 equal unit capacitors in cascade. There are various possible sources of inaccuracy in this DAC. First is mismatch in the unit capacitors. The capacitor available in the MOSIS 1- $\mu\text{m}$  CMOS technology

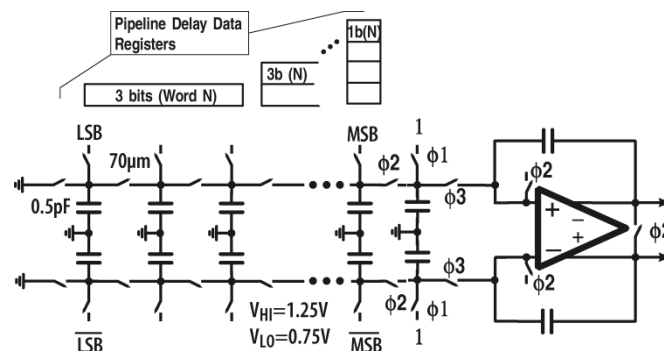


Fig. 6. Differential DAC circuit, showing output charge-to-voltage buffer and input registers necessary for pipelined operation.

is formed by the polysilicon gate over a heavily-doped  $n^+$  region. Data on the matching of these capacitors is obtained from an experimental study of MOSFET matching [17], which shows that the variance in FET current at a given bias depends inversely on polysilicon gate area which is a pessimistic measure of mismatch in FET gate capacitance. Data on capacitor matching was published later [18]. From both sources it is found that to achieve a standard deviation of 0.1% as required for 10-b overall DAC linearity, the capacitor plate area must be at least  $400 \mu\text{m}^2$ , which in this structure yields a capacitance of 0.5 pF. Strictly speaking, only the last two MSB stages in this nonsegmented DAC must match to this accuracy, while the matching in each preceding stage may be progressively relaxed by  $2\times$  without appreciable effect. To simplify automatic layout generation, the actual DAC uses the same capacitor in each charge redistribution cell.

There are three other potential sources of DAC inaccuracy, namely: voltage-dependent *junction capacitance* of the FET switches between each DAC capacitor; *charge-injection* through the FET switches on to the DAC capacitors; and *interwire capacitance* shunting DAC capacitors and the intercell switches. When two capacitors, initially with unequal charges, are connected in parallel, the charge bisects exactly if the capacitors are matched and the total charge is conserved over the transient. This is all that is necessary for DAC operation (Fig. 5). If two matched capacitors are voltage-dependent, the final *voltage* may not be the mean of the initial voltages on the two capacitors, but *charge* is. So voltage-dependence is of no consequence; only the junction capacitors must match well.

The FET's inject either a fixed or a signal-dependent stray charge into the DAC capacitors. As the gate voltage rises at turn-on, it initially displaces charge into the substrate through the depletion region under the gate. When the FET enters inversion, the changing gate voltage modulates the inversion layer, now displacing charge into the source or drain terminal (in the case of an NFET switch, into whichever terminal is at the lower potential). During  $\phi_1$ , the capacitor precharges to a fixed voltage, and at the end of this phase as the FET turns off, it injects a *fixed* stray charge through the gate overlap capacitance on to the DAC capacitor. This alters the reference voltage on the capacitor, causing gain error in the DAC but no nonlinearity. However, at the rising edge of  $\phi_2$  and  $\phi_3$ , the FET switch enters inversion at a gate voltage depending on

the smaller of the voltages stored on the capacitors attached to either side. Over the remaining excursion of the gate voltage, the FET injects a signal-dependent charge onto the capacitors. At the conclusion of these two phases, the FET extracts most of this injected charge, but now as the two capacitor voltages are equal, the FET shuts off at a higher gate voltage than before, leaving behind a small, signal-dependent charge. Simulations show that this effect introduces spurs below  $-70$  dBc on a synthesized sinewave. Complementary switches cancel, to the first order, clock feedthrough due to the NFET and PFET.

The stray wiring capacitance shunting the DAC capacitors is not troublesome as long as each DAC stage is identical. Somewhat unexpectedly, the stray capacitance shunting the *intercell switches* gives rise to the greatest dynamic nonlinearity. Charge redistributing between a pair of cells during  $\phi_2$  leaks through this stray capacitance into the adjacent cell capacitor, contaminating the sample during  $\phi_3$ . Due to the pipelined operation, the difference between voltages in adjacent cells grows as the synthesized sinewave frequency rises, causing a larger error charge to leak through this stray capacitance between stages. This intercell stray capacitance is lowered to a few femtofarads by spacing apart each DAC cell, which accounts for the large physical size of the DAC. Owing to this improved layout, the spurious levels in the synthesized sinewave spectra here (Fig. 7) are much lower than reported in an earlier version [19]. At low synthesized frequencies, various harmonics appear all lying at  $-62$  dBc or lower, while at high synthesized frequencies, the largest spurious tone rises to  $-57$  dBc. It is difficult to distinguish between aliased harmonics and anharmonic spurious tones in this spectrum. The measured noise floor of the synthesized spectrum is about 1 dB above the theoretical quantization noise level.

A quasi-differential DAC is implemented with two identical pipelines, which take as their inputs a digital codeword and its complement. A switched-capacitor (SC) integrator converts the differential output charge at the last stage into a voltage (Fig. 6). Unlike the capacitors in the core, linear conversion of charge-to-voltage requires use of an *integrator capacitor* in this buffer with a very small voltage-coefficient. The voltage coefficient of the single-poly linear capacitor is specified as 0.12%/V, which means that over the 0.5-V full-scale excursion of the DAC output it introduces a 0.06% nonlinearity. This is acceptably small for a 10-b DAC. The SC integrator operates with two of the three clock phases used in the DAC: at  $\phi_2$  the differential input and output are shorted to a common-mode bias voltage of 1.5 V, discharging the integration capacitor; then at  $\phi_3$  charge is transferred to the integrator from an additional stage following the main DAC, and the capacitor holds the charge over  $\phi_1$ . This extra stage at the DAC output is precharged to 2 V and shifts the 1-V common-mode level in the DAC core to 1.5 V at the op amp input. In doing so, it halves the voltage swing owing to charge redistribution. As a result, the differential sinewave at the DAC buffer output is 0.5 V full-scale, reset to zero over 33% of each clock cycle. The rms value of the fundamental frequency in this resetting waveform is 3.5 dB lower than of a continuous sinewave with the same amplitude.

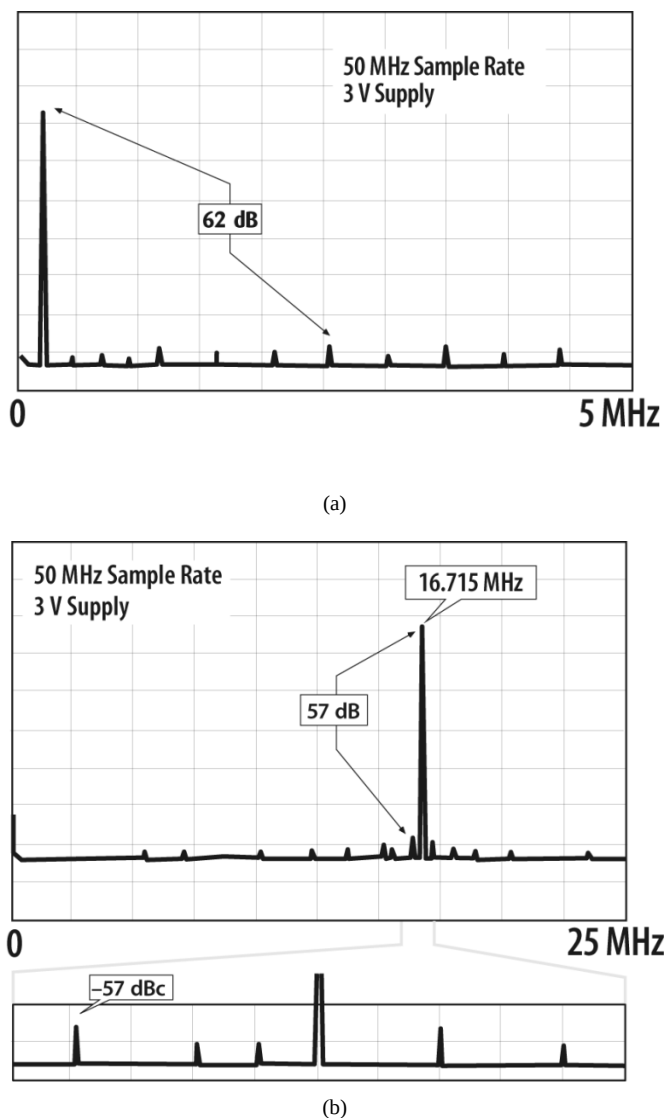


Fig. 7. Measured spectra of sinewaves synthesized by standalone DDS/DAC: (a) synthesized 200 kHz and (b) synthesized 16 MHz, with details of close-in spurious tones.

The DAC core may be clocked to beyond 100 MHz, and the clock frequency is eventually limited only by the RC time constant of the FET switch resistance, DAC capacitor, and FET capacitances. However, the op amp-based SC buffer cannot clock faster than 100 MHz. The op amp is a single-stage, gain-booster cascode differential pair. Minimum-size reset switches are used at the input to lower the capacitive load. The signal swing at the input terminals of the op amp is restricted to 1.2–1.8 V to keep the input FET's out of the triode region, otherwise the transient response of the op amp will slow down considerably.

In precharging to the reference voltage, each DAC cell capacitor  $C$  samples wideband noise of  $\sqrt{(kT/C)}$  Vrms induced by the FET switch resistance. After redistribution, this noise charge bisects but adds to a second uncorrelated noise sample of  $1/2\sqrt{(kT/1/2C)}$  induced by the series switch which shorts together two adjacent capacitors. The final noise captured in each DAC stage is  $\sqrt{(kT/C)} = 0.09$  mVrms, when  $C = 0.5$  pF. At the last stage, the signal is halved again,

and because of an additional switching operation the noise rises slightly. The total rms noise at this node is still well below the single-ended LSB voltage of 0.25 mV.

The three-phase nonoverlapping clocks are synthesized on-chip from a single externally supplied square wave. One possible way to do so is to tap these phases from a three-stage ring oscillator locked to an 80-MHz reference, but the ring oscillator usually introduces an unacceptably large jitter. Instead, a three-stage ring counter divides a low-jitter 240-MHz sinewave input, and NAND gates at its outputs create three nonoverlapped phases. Each phase also needs a well-aligned complementary clock, which is derived by inverting a clock phase and balancing the inverter delay with ratioed delay stages [20].

### C. Upconversion Mixers

The passive *four-FET commutating switch* (Fig. 8) is used as a double-balanced upconversion mixer. Balanced quadrature signals from the RF oscillator upconvert the baseband outputs of the quadrature DDS/DAC frequency synthesizer in two four-FET switch mixers, whose outputs are tied together to select a single sideband. Each switch mixer connects the baseband signal to the balanced output either as is, or inverted. The double-balanced configuration cancels the strong second-order nonlinearity of the FET I-V triode characteristic, but third-order nonlinearity will remain. There are two other possible sources of nonlinearity in this mixer. First, with inadequate gate voltage swing, that is  $V_G < V_s(\text{max}) + V_t$ , the mixer NFET's are in saturation and clip the output waveform. This clipping will not appear if the gate voltage swing is large enough. However,  $V_G$  must still swing sufficiently low to turn OFF the FET's at the lowest  $V_s$ . Second, the finite slope of the gate voltage waveform gives rise to a dynamic nonlinearity. The FET turns ON when  $V_G = V_s + V_t$ , which means that by modulating the instant of turn-on and therefore the *commutation pulsewidth* (Fig. 9), the input signal creates a third-order distortion. This form of distortion appears in FET sample-and-hold switches and the resulting signal-to-distortion ratio (SDR) is empirically modeled as [21]

$$\text{SDR} = 20 \log \left( \frac{V_G}{V_{in} f_{in} t_F} \right) - 4 \text{ dB} \quad (1)$$

where  $f_{in}$  is the input signal frequency and  $V_G/t_F$  is the slope of the gate voltage. As this distortion arises from time modulation, it will appear even if the FET I-V characteristics are perfectly linear. At an input frequency of 10 MHz and a gate voltage falling by 3 V in 0.5 ns, HSPICE predicts a mixer IIP3 of +16 dBV amplitude (Fig. 9). With a DAC output amplitude of 0.5 V (−6 dBV) the third harmonic appears 43 dB below the fundamental tone.

When two signals are in quadrature at the fundamental frequency, their third harmonics are in *antiquadrature*. Therefore, an image-reject mixer configured to select the *upper* sideband of the *fundamental baseband* frequency will select the *lower* sideband of the third harmonic, as is explained in greater detail in (2) and (3). After upconversion, a low synthesized frequency and its third harmonic will both lie in

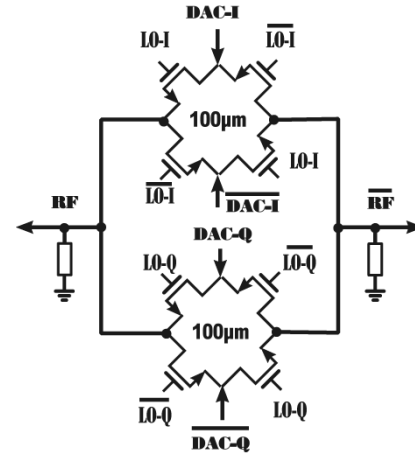


Fig. 8. Four-FET switch upconversion mixer as used in this transmitter, here shown in quadrature image-reject configuration.

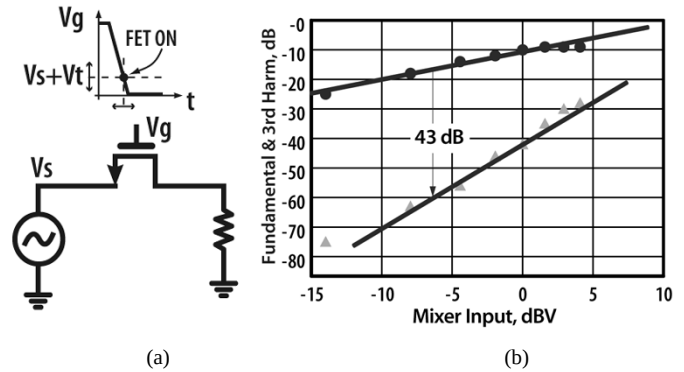


Fig. 9. (a) The large baseband signals modulate the switching instant of the mixer, resulting in (b) third-order distortion, shown as a function of the input signal level.

the ISM band. This form of distortion, too, is lowered by applying a larger LO drive,  $V_G$ , to the mixer.

In a simple embodiment of the quadrature upconverter (Fig. 8), the signals in the *I* and *Q* channels of the single-sideband mixer are summed in current mode by shorting together the outputs (drain terminals) of the two upconversion FET's. However, when the quadrature phases of the gate voltage overlap in time, they create a conduction path between the inputs (source terminals) of the two mixers (Fig. 10). During this overlap time, the mixer switches connect the output of the SC buffer op amp (Fig. 6) in one DAC to the buffer output of the other DAC. This may overload the mixer output and cause serious distortion. To sustain the overload without clipping, either the bias current in the op amp should be raised, or it must be followed by a second linear buffer designed specifically to absorb this load. The second option is more power efficient. Accordingly, a differential pair degenerated with a polysilicon resistor and loaded with another resistor (Fig. 11) follows the op amp. This buffer distorts the 0.5-V amplitude sinewave by less than −60 dB, and its loaded voltage gain is 0.75 (that is, −2.5 dB).

The DAC output spectrum comprises the fundamental frequency  $f_1$  and images of the fundamental frequency around the clock frequency  $f_{clk} \pm f_1$ . Harmonics at the DAC output,

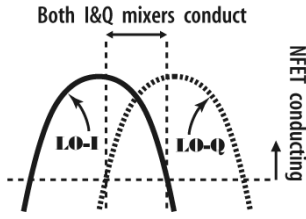


Fig. 10. Both mixers in image-reject topology conduct during the overlapping portion of the quadrature LO waveforms. Thus, one mixer input loads the other.

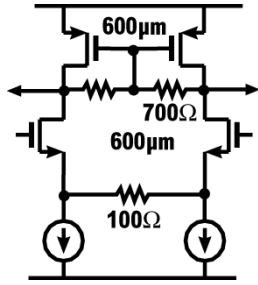


Fig. 11. Baseband buffer following DAC, required to drive mixer and subsequent circuits.

which tend to be much lower than the images, are neglected for the purpose of this discussion. The frequency spectrum of any sampled-and-held waveform is subject to a  $\sin x/x$  envelope. Here, because the sample is held over a 67% duty cycle, the first null lies at  $(3/2)f_{\text{clk}}$  (Fig. 12). Both the synthesized baseband sinewave and its images are upconverted. As the mixer FET's are driven into commutation, in the time-domain the baseband sampled-data waveform is multiplied by a square wave which alternates between  $+1$  and  $-1$  at the frequency of the RF oscillator. In the frequency domain, this is the convolution of the DAC output spectrum with the spectrum of a square wave. The square wave consists of the fundamental frequency  $f_{\text{RF}}$  and odd harmonics  $3f_{\text{RF}}$ ,  $5f_{\text{RF}}$ ,  $\dots$ , with relative amplitudes of  $1/3^{\text{rd}}$ ,  $1/5^{\text{th}}$ ,  $\dots$ .

The upconverting waveforms in the two commutating mixers are square waves delayed by a quarter-period ( $1/4f_{\text{RF}}$ ), whose frequency spectra are, respectively

$$V_{\text{LO-I}} = \sin \omega_{\text{RF}} t + \frac{1}{3} \sin 3\omega_{\text{RF}} t + \dots \quad (2)$$

$$\begin{aligned} V_{\text{LO-Q}} &= \sin \omega_{\text{RF}} \left( t + \frac{\pi}{2\omega_{\text{RF}}} \right) \\ &+ \frac{1}{3} \sin 3\omega_{\text{RF}} \left( t + \frac{\pi}{2\omega_{\text{RF}}} \right) + \dots \\ &= \cos \omega_{\text{RF}} t - \frac{1}{3} \cos 3\omega_{\text{RF}} t + \dots \end{aligned} \quad (3)$$

The baseband spectrum is therefore upconverted by quadrature phases to the fundamental of the RF, and by *anti*-quadrature phases to the third harmonic of the RF. As a result of the sign difference, a mixer arrangement designed to select the *upper* sideband at the fundamental RF,  $f_{\text{RF}} + f_1$ , will select the *lower* sideband at the third harmonic of the RF,  $3f_{\text{RF}} - f_1$ .

To achieve a high conversion efficiency with the constant-envelope FSK modulation, the input level is large enough to force the PA to operate in the clipping region. Third-order

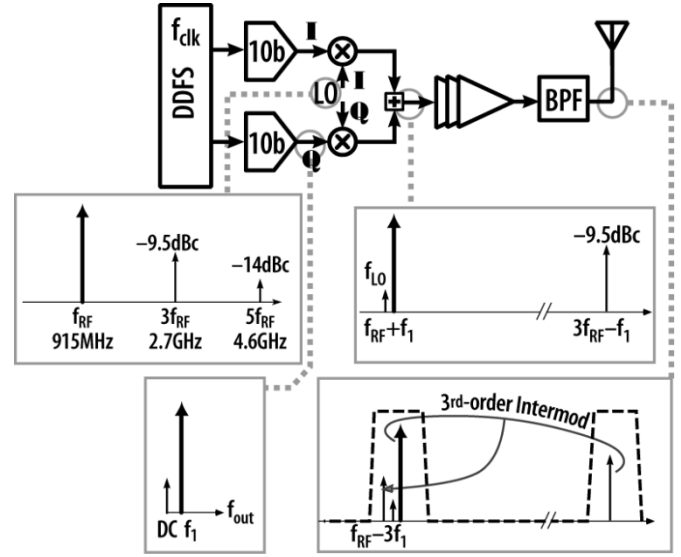


Fig. 12. Frequency spectra at various key points in the transmitter: commutating mixer LO, baseband signal with dc offset, output of upconversion mixer after sideband selection, and in-band intermodulation product created in nonlinear power amplifier.

intermodulation distortion among the various input frequencies will create new frequencies at the PA output, such as  $(3f_{\text{RF}} - f_1) - 2(f_{\text{RF}} + f_1) = f_{\text{RF}} - 3f_1$ . Although this intermod lies at the same frequency as the upconverted third harmonic of the DDPS baseband output, its amplitude may be much larger, and this results in an unacceptably large spurious emission in the ISM band. Therefore, frequencies upconverted by the third harmonic of the RF must not be allowed to enter the nonlinear PA.

Linear mixers, which preserve the sinusoidal waveforms of the baseband and LO signals during analog multiplication, ideally generate only sum and difference frequencies at the output but no harmonics. RF-CMOS linear mixers have been proposed [22] as a way to overcome upconversion to harmonics. However, to preserve waveshape, a linear mixer must use a small LO drive, and this in turn means that the baseband input experiences a large conversion loss to the RF output. It is not easy to make up this loss at the mixer's upconverted output, because subsequent amplification is at RF.

The four-FET switch upconversion mixer used in this transceiver achieves, in practice, a conversion gain very close to the theoretical value of  $2/\pi$  [23], the maximum possible in a mixer core. However, as a consequence of switching, the baseband signal is now upconverted around the third harmonic of the RF oscillator frequency ( $\sim 2.7$  GHz). This undesired upconversion must be removed prior to the nonlinear PA. A simple solution is to filter out all frequencies lying around 2.7 GHz. However, an on-chip *LC* low-pass using low-*Q* spiral inductors is not sufficiently selective to pass 928 MHz yet adequately attenuate 2.7 GHz. Also, it was found on an earlier prototype of a single-chip transmitter where such a filter is used [24] that the inductors consume a very large chip area. As described in the following section, an alternative, very compact "phasing" method may selectively null the undesired harmonic upconversion.

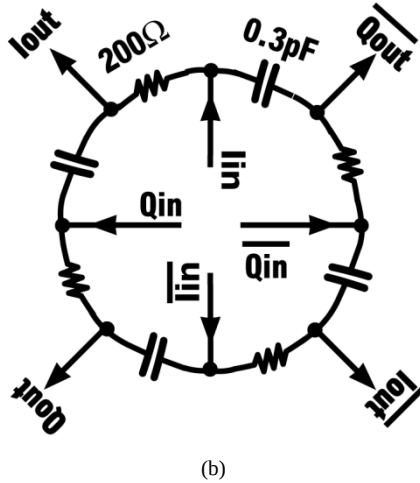
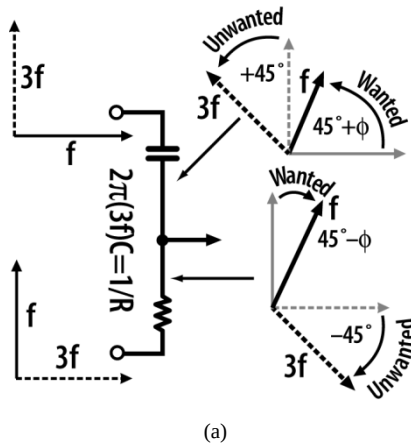


Fig. 13. (a) Principle of RC polyphase filter, showing how it nulls one input sequence, but passes the other. (b) Balanced implementation of polyphase filter.

#### D. Filtering Major Spectral Impurities

The polyphase filter selectively passes or nulls quadrature inputs depending on their *sequence* [25]. When the in-phase component *leads* the quadrature component by  $90^\circ$ , it is said to comprise one sequence, whereas when it *lags* by  $90^\circ$  it comprises the other sequence. An RC–CR network retards or advances the phase of its inputs at a frequency  $1/(2\pi RC)$  by  $+45^\circ$  or  $-45^\circ$ , respectively, so depending on which one of the two possible input sequences is applied, the outputs will either reinforce or null (Fig. 13). The full analog polyphase filter consists of a circular symmetric RC network, which is subject to balanced quadrature inputs, and produces balanced quadrature outputs. This discriminating property of the polyphase filter is used here in a new way, to null upconversion around the third harmonic while passing upconversion around the fundamental.

First, a single-sideband mixer arrangement must be devised to upconvert a baseband signal into one sequence at the fundamental RF and into the opposite sequence at the third harmonic. A standard image-reject mixer, consisting of two mixers driven by quadrature phases each of the baseband and RF signals, yields only a *single phase* of the upconverted signal. To create an upconverted output in *quadrature phases*,

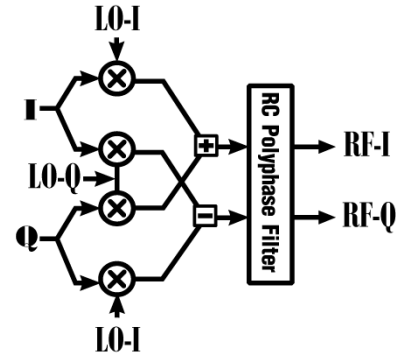


Fig. 14. Double-quadrature upconversion mixer produces the two opposite sequences in quadrature required at the input to the polyphase filter.

this is extended with four mixers to a full-matrix trigonometric product (Fig. 14), which has been called the double-quadrature mixer [26], [27]. The following trigonometric relations define the pairwise summed outputs:

$$\begin{aligned} & \cos \omega_1 t \cdot \left( \cos \omega_{RF} t - \frac{1}{3} \cos 3\omega_{RF} t + \dots \right) \\ & - \sin \omega_1 t \cdot \left( \sin \omega_{RF} t + \frac{1}{3} \sin 3\omega_{RF} t + \dots \right) \\ & = \frac{1}{2} \left( \cos(\omega_{RF} + \omega_1)t - \frac{1}{3} \cos(3\omega_{RF} - \omega_1)t + \dots \right) \quad (4) \end{aligned}$$

$$\begin{aligned} & \cos \omega_1 t \cdot \left( \sin \omega_{RF} t + \frac{1}{3} \sin 3\omega_{RF} t + \dots \right) \\ & + \sin \omega_1 t \cdot \left( \cos \omega_{RF} t - \frac{1}{3} \cos 3\omega_{RF} t + \dots \right) \\ & = \frac{1}{2} \left( \sin(\omega_{RF} + \omega_1)t + \frac{1}{3} \sin(3\omega_{RF} - \omega_1)t + \dots \right). \quad (5) \end{aligned}$$

The output consists of the upper sideband of the tone  $\omega_1$  upconverted around the fundamental  $\omega_{RF}$ , and the lower sideband of the tone upconverted around  $3\omega_{RF}$ . Furthermore, they are in opposite sequences because the two outputs at  $\omega_{RF} - \omega_1$  are in quadrature while at  $3\omega_{RF} - \omega_1$  they are in *anti-quadrature* [(4) and (5)].  $R \times C$  in the filter is set to  $1/(2\pi \times 2.7 \text{ GHz})$ . The 2.7-GHz currents entering the two inputs to the filter are, respectively, rotated anti-phase at the output and *null*. Whereas the 900-MHz current traversing this filter is advanced in phase through the capacitor by an angle  $45^\circ + \phi$  while it is retarded by the same  $45^\circ - \phi$  through the resistor (Fig. 13). Here,  $\phi = \arctan(0.9/2.7) = 26.5^\circ$ . The rotated signals reinforce in phase at the output, so the filter *passes* the input sequence at 900 MHz. In effect, the double-quadrature upconversion combined with the polyphase filter acts as a sharply tuned notch filter for third harmonic upconversion. The small  $R$  and  $C$  required make the filter physically compact.

The values of the integrated  $R$  and  $C$  in the polyphase filter are subject to process variations. Simulations show that in spite of a deviation in the RC time constant of as large as  $\pm 20\%$ , the polyphase filter suppresses the unwanted upconversion by more than 17 dB.

It has been suggested [27] that following a double quadrature upconversion mixer, a polyphase filter tuned to the LO

frequency can also further suppress the unwanted sideband at 900 MHz, which appears at the output due to gain mismatch in the mixers and errors in quadrature phase at the LO. Analysis shows that this is not feasible, because with random gain and phase errors the residual unwanted sideband acquires, with equal likelihood, either the *same* sequence as the wanted sideband or the *opposite* sequence. As the polyphase *only* suppresses the opposite sequence [25], on average it cannot improve the ratio of the wanted to the unwanted sideband in an upconversion mixer.

There are two other sources of unwanted frequencies which will appear in the transmitter output: the upconverted images of the synthesized frequency around the DDFS/DAC clock, and the upconverted dc offset at the DAC buffer. Each is now considered individually. At a sampling frequency of  $\omega_{\text{clk}}$ , the baseband frequency spectrum of a sampled-and-held waveform which resets for one-third of the clock cycle is (Fig. 15)

$$F(j\omega) = \frac{\sin\left(\pi \frac{\omega}{\frac{\pi}{2}\omega_{\text{clk}}}\right)}{\pi \frac{\omega}{\frac{\pi}{2}\omega_{\text{clk}}}} [\delta(\omega - \omega_1) - \delta(\omega - \omega_{\text{clk}} + \omega_1) + \delta(\omega - \omega_{\text{clk}} - \omega_1) + \dots] \quad (6)$$

where the coefficient on the right-hand side is the  $\sin x/x$  envelope, and the three terms are the baseband synthesized frequency and its upper and lower images around the clock. Depending on its sign, each term upconverts in the double-quadrature mixer into either an upper or a lower sideband. The output spectrum comprises frequencies  $\omega_{\text{RF}} + \omega_1$ ,  $\omega_{\text{RF}} + \omega_1 \pm \omega_{\text{clk}}$ ,  $\dots$  or, in the case of a lower selected sideband,  $\omega_{\text{RF}} - \omega_1$ ,  $\omega_{\text{RF}} - \omega_1 \pm \omega_{\text{clk}}$ ,  $\dots$  (Fig. 12). On passing through the nonlinear power amplifier, this ensemble of frequencies suffers intermodulation distortion. However, third-order intermodulation between the main tone and one upconverted image creates a signal at the *other* upconverted image. For example, one such intermodulation product lies at

$$2 \times (\omega_{\text{RF}} + \omega_1) - (\omega_{\text{RF}} + \omega_1 - \omega_{\text{clk}}) = \omega_{\text{RF}} + \omega_1 + \omega_{\text{clk}}. \quad (7)$$

In fact, all the third-order intermods in this case coincide with members of the original frequency ensemble. Therefore, intermodulation does not create any new frequencies, but merely redistributes energy between the original ensemble of frequencies. For a modulation with constant amplitude, such as the 4-FSK used here, amplitude rebalancing between frequencies is a benign effect.

The images around the DDFS/DAC clock (Fig. 15) must also be suppressed. However, when  $\omega_{\text{clk}} > 80$  MHz, these images will upconvert out of the ISM band, where they will experience the 40-dB stopband loss of the *off-chip* RF filter (Fig. 15). The attenuated images lie below the permissible out-of-ISM band limits on radiation set by the FCC. This eliminates the need for an image-reject filter after the DAC, which would otherwise be quite power-hungry because it must pass the DAC output with very low distortion. In effect, the highly linear, passive RF preselect filter at the transmitter output fulfills this role without draining any bias current.

Another important spectral impurity arises from dc offset at the DAC's output buffers, which upconverts as a spurious tone

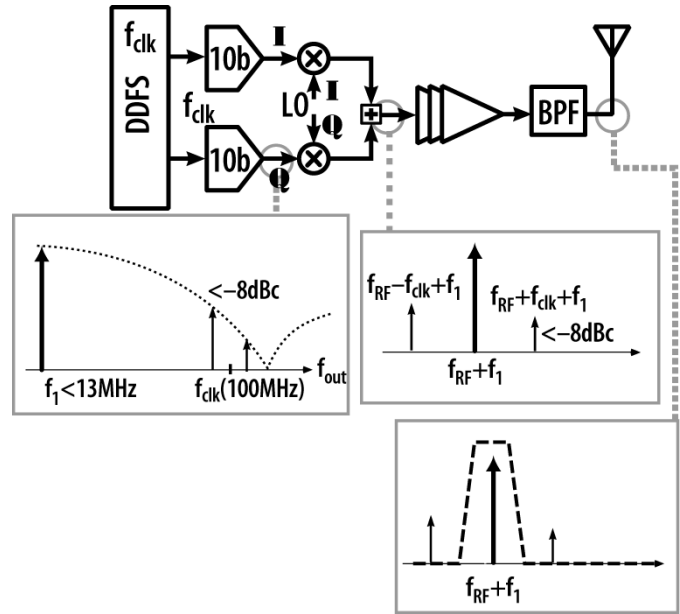


Fig. 15. Upconverted spectrum of DDFS/DAC images. With a sufficiently high clock rate, the upconverted images lie in the stopband of the RF filter. This eliminates a baseband image-reject filter after the DAC.

at the RF oscillator frequency. More precisely, offsets  $V_{O1}$  and  $V_{O2}$  at the two DAC output buffers upconvert into quadrature phases, add as vectors, and pass through the polyphase filter just as does the desired baseband tone synthesized by the DDFS. The amplitude of the main synthesized sinewave at  $\omega_{\text{RF}} + \omega_1$  is equal to the DAC full-scale voltage  $V_{\text{FS}}$ , and the relative strength of the spurious tone at  $\omega_{\text{RF}}$  is  $\sqrt{(V_{O1}^2 + V_{O2}^2)} : V_{\text{FS}}$ .

The SC integrator at the DAC output (Fig. 6) is not autozeroed, so its equivalent input offset voltage appears at the output multiplied by the gain,  $2\times$ . To this adds the offset of the following open-loop buffer. The analog switch mixer FET's do not contribute offset. Monte Carlo simulations on SPICE using MOSFET matching data [17] suggest a cumulative offset of 16 mV rms in the baseband section prior to the mixer. The upconverted dc offset produces a spur potentially much larger than the spurs in the DDFS/DAC output. For example, with  $V_{\text{FS}} = 0.5$  V and  $V_{O1} \approx V_{O2} \approx 10$  mV, the spurious tone at the mixer outputs is  $-31$  dBc relative to the desired tone using the above equation. This spurious tone remains stationary as the carrier frequency hops across the ISM band, and unlike the modulated waveform it does not spread out in frequency. A steady emission of this magnitude at 915 MHz will violate FCC rules. To circumvent this problem, the RF oscillator frequency is lowered *below the ISM band*, to a frequency where the RF filter at the transmitter output attenuates it by at least 10 dB. To compensate, the DDFS must now synthesize higher frequencies, and only its upper sideband is used, which lies in the ISM band after upconversion. In the final implementation, the RF oscillator is tuned to roughly 890 MHz, while the DDFS/DAC clocks at 100 MHz to synthesize frequencies of up to 38 MHz ( $=928 - 890$ ). The closest image now lies at  $890 + 100 - 38 = 952$  MHz and suffers a loss of about 30 dB in the RF filter. Owing to the  $\sin x/x$  rolloff of the

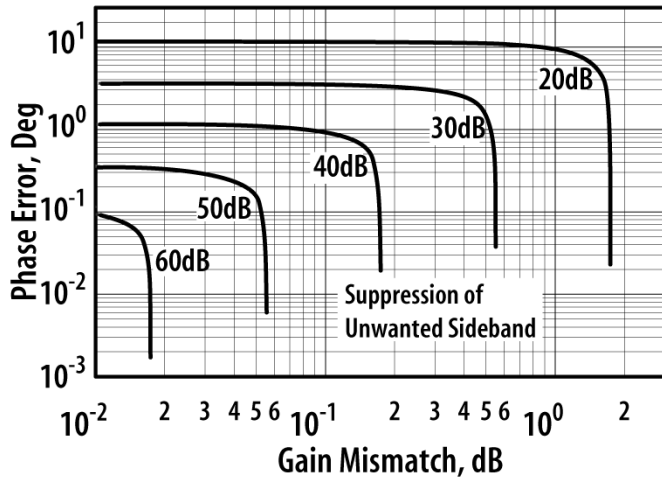


Fig. 16. Curves of equal unwanted sideband suppression in an image-reject mixer, as functions of gain mismatch in the mixers and phase error in quadrature LO signals.

sampled-and-held DAC output, the image is lower by another 8 dB compared to the main tone. At the transmitter output, therefore, the closest image is lower by 38 dB compared to the desired tone. When the synthesized frequency lies at the lower end of the ISM band, 902 MHz, the image is farthest and lowered by another 12 dB because of greater attenuation in the RF filter and the  $\sin x/x$  response. As the carrier frequency hops, on average the image will lie 44 dB below the main tone. It may be further lowered either by using an RF filter with a sharper transition band, or by raising the DAC clock frequency.

#### E. RF Quadrature Oscillator

Errors in the quadrature phases of the baseband signals and the upconversion frequency, and gain mismatch in the two channels, limit suppression of the unwanted sideband in a quadrature upconverter (Fig. 16). The DDFS produces perfect quadrature by definition, although skew in the clocks to the two channels of the DDFS/DAC must be kept to a minimum. For example, a skew of 73 ps between the clocks to the  $I$  and  $Q$  DAC's appears as a  $1^\circ$  phase error between 38 MHz synthesized sine and cosine waveforms. The clock lines are therefore laid out with great care.

A greater phase error usually arises in the RF oscillator. Most oscillators produce a single-phase output, some as a balanced signal. Normally an external passive RC-CR phase-shift network converts this into quadrature phases [5]. An integrated RC-CR network will suffer from process spread on the RC time constant, resulting in amplitude imbalance between the quadrature outputs. Furthermore, the typical RC phase-shift network will load the RF oscillator. A buffer after the oscillator to relieve this loading will be power hungry and may also attenuate the oscillation amplitude. These various conflicts resolve in an oscillator which inherently produces balanced outputs in accurate quadrature and directly drives the switching upconversion mixers. This type of oscillator is used here.

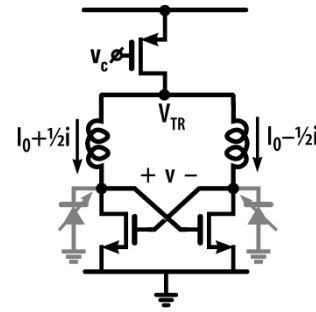


Fig. 17. Core of on-chip LC voltage-controlled oscillator.

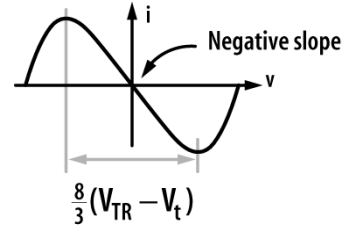


Fig. 18. Illustrating differential negative resistance region produced by FET pair, and the amplitude of oscillation this implies.

The oscillator core comprises a cross-coupled pair of common-source FET's with inductor loads (Fig. 17). The NFET pair presents a differential negative resistance to the two on-chip inductor loads, which are selected to resonate at the desired frequency with the capacitance at the NFET gate and the drain junction. The voltage-dependent junction capacitance is used to fine-tune the oscillation frequency, as follows. The other terminals of the inductors tie to a common point, and then to the supply through a PFET biased in the triode region. As the PFET resistance varies with its gate voltage, it changes the dc voltage drop across the PFET, and through the inductors the bias voltage  $V_{TR}$  appearing on the NFET drains. A fractional frequency tuning range of about 7% is expected over a PFET  $V_{GS}$  ranging from 1 to 2 V.

When both NFET's are in the saturation region, the  $I$ - $V$  characteristic produces a differential negative resistance (Fig. 18); when one FET turns OFF or enters the triode region, the differential resistance becomes positive. To guarantee startup, the oscillator is designed with a surplus of negative dissipation. The oscillation amplitude grows at power-up and stabilizes when the *energy gained* by the tuned circuit as the oscillation swings through the negative resistance balances *energy lost* in the positive resistance region. It follows that the oscillation amplitude must be at least as large as the negative resistance region, which spans a differential voltage of  $4(V_{TR} - V_t)$  and is easily several volts. This large amplitude improves the "carrier-to-noise" ratio in the oscillator core, thus lowering phase noise [28]. A large oscillation amplitude is important to counteract the low  $Q$  tuned circuit: in this implementation, the spiral inductor  $Q$  is between three to four. It also improves the conversion gain when driving the mixers.

Various oscillators with quadrature outputs have been published over the years. One of the first was a cross-coupled two-vacuum tube oscillator with mutual inductance [29]. More

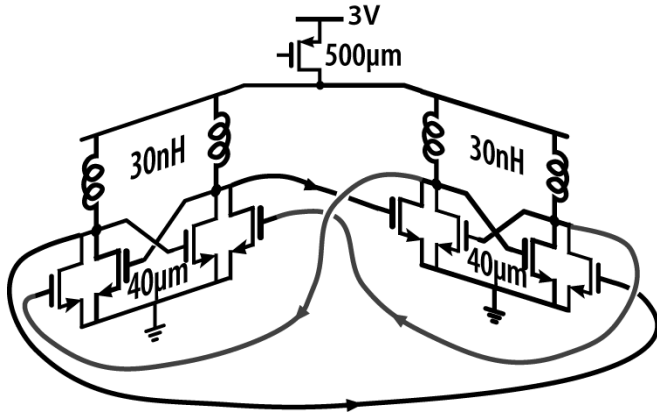


Fig. 19. Quadrature oscillator comprises a pair of cross-coupled LC oscillators synchronized in frequency.

recently, balanced quadrature outputs are obtained from two cross-coupled relaxation oscillators [30]. Another oscillator consists of two LC biquad filters in feedback [31]. Four-stage ring oscillators also produce quadrature at taps two stages apart [32], [33]. However, it is difficult (although apparently not impossible [34]) to obtain the requisite low phase noise in CMOS ring oscillators.

This transceiver uses an LC quadrature oscillator. It comprises two unit oscillators as described above, labeled A and B, and additional coupling FET's inserted in parallel with the oscillator core. The balanced output of Oscillator A is *direct-coupled* to the coupling FET's in Oscillator B, and the output of Oscillator B is *cross-coupled* into Oscillator A (Fig. 19). The two oscillators synchronize to exactly the same frequency but are forced into quadrature phases by the coupling topology. The following symmetry argument explains how, owing only to the topology, the circuit oscillates in quadrature.

Suppose phasors  $\vec{v}_A$  and  $\vec{v}_B$ , respectively, are the steady-state outputs of Oscillators A and B, with reference polarities as shown (Fig. 20). Then the phasor current into the tuned load of Oscillator A is  $g_m(\vec{v}_A + \vec{v}_B)$ , but it is  $g_m(-\vec{v}_A + \vec{v}_B)$  into the load of Oscillator B, where  $g_m$  is the differential average large-signal transconductance of the FET's. Arguing purely by symmetry, if the respective components in the two circuits are identical then the two oscillations must also be identical in frequency *and* in amplitude. Therefore, the impedance of the two LC tuned circuits is equal, and the phasor currents driving them are also *equal in magnitude*. This is only possible if  $\vec{v}_A$  and  $\vec{v}_B$  are in quadrature<sup>1</sup> (Fig. 20), which proves the circuit principle.

$\vec{v}_B$  may lead  $\vec{v}_A$  by  $90^\circ$ , or lag it; in either case the conditions for quadrature oscillation are met. To resolve this ambiguity, the asymmetrical frequency dependence of the tuned circuit impedance is invoked. First consider the steady-state relation between resonator current and voltage. In Oscillator A, for instance, the voltage across the resonator is  $\vec{v}_A$ , while the current supplied by the FET is  $g_m(\vec{v}_A + \vec{v}_B)$ . As  $\vec{v}_A$  and  $\vec{v}_B$  are equal and at right angles, the steady-state tuned

<sup>1</sup> Suppose  $v_B = r$ , a real number, and  $v_A = re^{j\theta}$ . Then  $|v_A + v_B| = |-v_A + v_B|$  implies that  $|1 + e^{j\theta}| = |1 - e^{j\theta}|$ , which requires  $\cos \theta = 0$ , that is  $\theta = \pm 90^\circ$ .

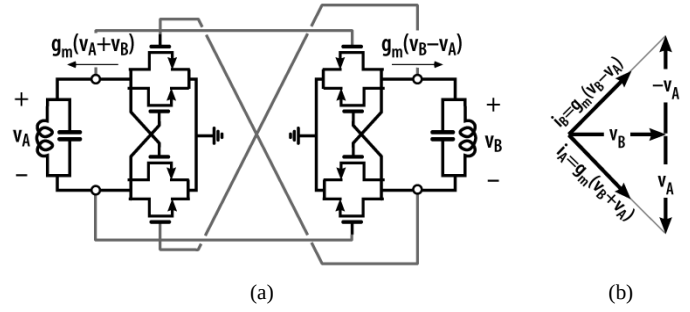


Fig. 20. (a) Quadrature oscillator redrawn, emphasizing its symmetry and showing the resonator currents; and (b) the relative phases of the voltages across the resonators required for symmetric operation.

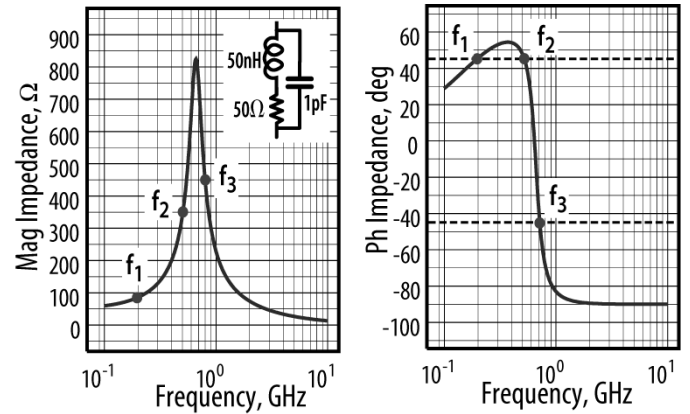


Fig. 21. Magnitude and phase of a realistic resonator's impedance, showing three possible oscillation frequencies. The oscillator selects the highest frequency because the feedback loop gain is largest here.

circuit impedance is  $1/(\sqrt{2}g_m)$  and its phase is either  $+45^\circ$  or  $-45^\circ$  (Fig. 20). In an LC resonator with series loss in the inductor, these phases appear at three different frequencies,  $f_1$ ,  $f_2$ , and  $f_3$  (Fig. 21). However, among them only  $f_3$  is stable, because at this frequency the impedance is largest, and thus the feedback factor in the oscillator is strongest. At  $f_3$  the phase of the resonator's impedance is  $-45^\circ$ , which means that  $\vec{v}_B$  must lead  $\vec{v}_A$  by  $90^\circ$ , as is shown in Fig. 20. Note also that the oscillation frequency is *higher* than the resonance of the tuned circuit, which is an advantage when building an RF circuit operating close to the capabilities of an IC technology. The standard theory of phase noise [28] must be modified for this oscillator, and this will be the subject of another publication.

Measurements on a standalone prototype of this oscillator have been reported previously [35]. The accuracy of quadrature cannot be measured on an oscilloscope, because a  $1^\circ$  phase error at 900 MHz, for instance, corresponds to a differential delay of 3 ps between the *I* and *Q* outputs, which is very difficult to resolve on a linear time axis. Instead, by using the oscillator in a single-sideband upconversion experiment, the quadrature error is deduced from measurements on the logarithmic amplitude display of a spectrum analyzer. The standalone oscillator's outputs drive the gates of two four-FET mixers on the same chip; balanced quadrature outputs from a 10-MHz sinewave generator drive the sources of the FET's; and the drains are shorted together into two 50- $\Omega$  loads to select one sideband of the upconverted output [35]. The

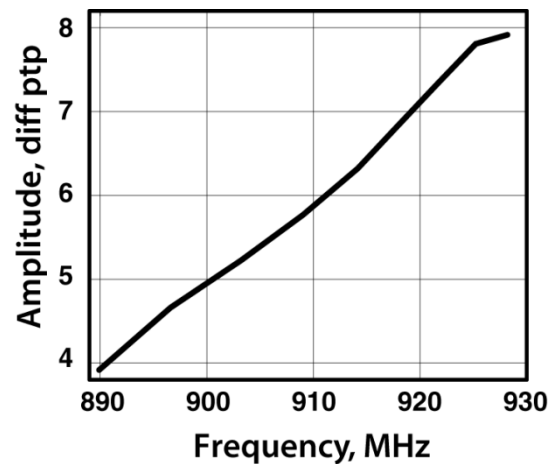
unwanted sideband is found to be 45 dB below the wanted sideband, which implies a quadrature accuracy of better than  $1^\circ$  and a gain matching of better than 0.1 dB (Fig. 16). The oscillation amplitude is indirectly measured by biasing the FET mixers as common-source stages and de-embedding their simulated gain at the oscillation frequency. The measured close-in phase-noise (Fig. 22) shows a slope of 28 dB/decade up to an offset frequency of 200 kHz, attributed to upconverted flicker noise originating in the oscillator NFET's, and thereafter the slope falls to 20 dB/decade. Over the 18% fractional tuning range of this oscillator, the single-sideband phase-noise at a 100-kHz offset frequency remains almost constant at  $-102$  dBc/Hz.

In the transceiver also, the oscillator outputs *directly* drive the gates of the upconversion mixer FET's. The mixer gate capacitance loads the tuned circuit in the oscillator. As the large amplitude oscillation output applied at the gate sweeps the mixer FET's from inversion, through depletion, into accumulation, and the large DDFS/DAC signal at the FET source varies its bias, the changing capacitance of each mixer FET will modulate the oscillator's resonant frequency to create spurious tones in the form of FM sidebands. However, this double-balanced mixer loads a balanced oscillator, and it is found that the increasing capacitance which loads one side of the quadrature oscillator counteracts the decreasing capacitance loading the other side. SPICE simulations show that the average capacitance presented by the balanced mixers to the inductor loads varies very little over the cycle (Fig. 23), so that the oscillator keeps to the average resonant frequency. FM sidebands produced by the very small fluctuations in average capacitance lie below  $-60$  dBc. It should be noted that if the *common-mode* value of the baseband inputs to the mixers shifts, then the mixer FET's will be biased differently, and *all* mixers will present a different capacitance to the inductor load. This will shift the oscillation frequency. The modulation coefficient from the common-mode input to the oscillation frequency in this circuit is 2.5 MHz/V. This is low enough that any common-mode noise is not expected to contribute significant phase noise.

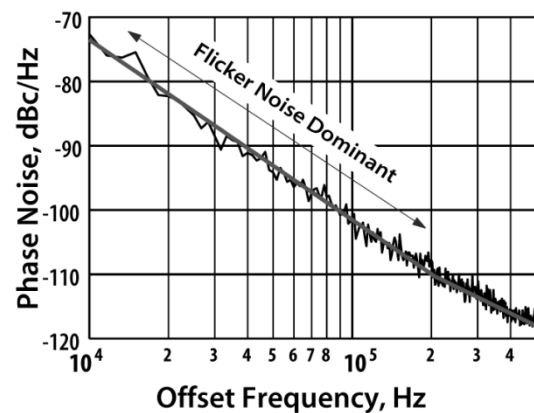
The 30-nH spiral inductors in the oscillator are implemented in Metal 2, which has the lower sheet resistance, and Metal 1 brings out the inner end of the spiral. The substrate under the inductor is etched away after fabrication, leaving the inductor encased in  $\text{SiO}_2$  above a cavity [23], [36]. This eliminates the capacitance to substrate of this large inductor and also all losses due to displacement currents or eddy currents in the substrate. The only remaining loss is in the resistance of the windings. The inductor turns wind outwards from a large hole in the middle. Any turns in the middle would contribute mostly loss but little inductance [23].

#### F. Power Amplifier

The PA must deliver up to 20 mW into a  $50\text{-}\Omega$  load, controllable by a digital word to a level as low as  $20\text{ }\mu\text{W}$ . The PA is also a balanced circuit, whose two antiphase outputs combine in an off-chip balun into the single-ended  $50\text{-}\Omega$  antenna load. The impedance at all ports of the balun is  $50\text{ }\Omega$ .



(a)



(b)

Fig. 22. Measurements on standalone oscillator prototype: (a) amplitude of oscillation versus frequency tuning range and (b) typical phase noise across tuning range.

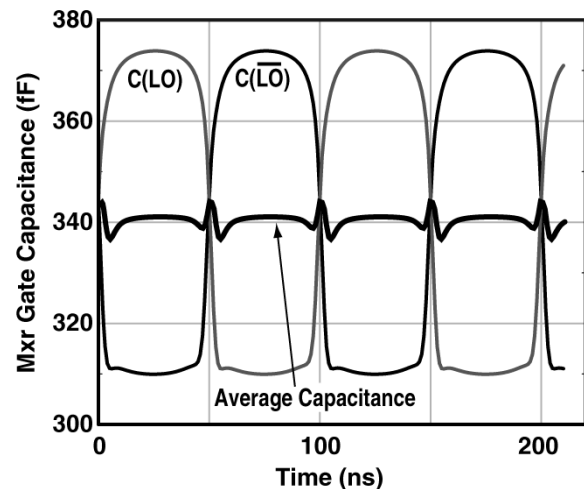


Fig. 23. Simulated variation in small-signal gate capacitance of each FET in one upconversion mixer caused by the large baseband signal. Average capacitance varies by very little.

Thus, each half of the balanced PA delivers a peak output of 10 mW, which corresponds to a peak-to-peak swing of 2 V. To deliver a higher output power into  $50\text{ }\Omega$  from a 3-V supply, the load must be transformed with high-quality discrete  $L$ 's and  $C$ 's into a small resistance [37].

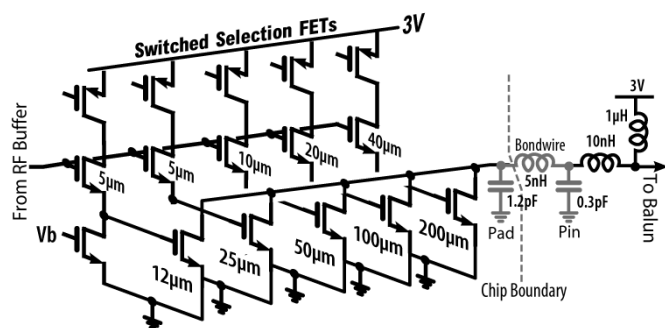


Fig. 24. Power amplifier circuit (one half of quasi-differential circuit is shown here). NFET's in the binary-weighted array are digitally selected by PFET's. Output currents combine in matching network, which absorbs package inductor and capacitors.

A phase-continuous frequency-hopped sinewave modulated by 4-FSK defines a constant envelope waveform. This may be amplified in a high-efficiency but nonlinear Class-AB circuit to generate the antenna current (Fig. 24). The PA is constructed as follows. An NFET is chosen to give the specified large-signal transconductance at the *fundamental frequency* of 900 MHz. This FET is 400- $\mu\text{m}$  wide and 1- $\mu\text{m}$  long. The upconverted voltage at the mixer output is driven into this FET through an inductor-loaded common-source stage, buffered by an NFET source follower to level-shift down the amplified signal. This combination is referred to as the *driver* circuit for the PA. The MOSFET PA has a large junction capacitance  $C_{DB}$  to substrate at the output. At a specified radio frequency, this capacitance limits the power the FET can deliver to a 50- $\Omega$  load: as the FET width is scaled up for larger transconductance,  $C_{DB}$  grows proportionally, until its low-pass response with the fixed load resistor drops below 900 MHz. The design rules of the CMOS technology set the ratio of FET  $g_m$  to  $C_{DB}$ . To estimate the effect of  $C_{DB}$ , note that  $C_{DB} \approx C_{GS}$ , from which it follows that  $g_m \approx \omega_T C_{DB}$ , where  $\omega_T$  is the radian unity current-gain frequency.

Next, this output FET is split into an array of binary-weighted FET's in parallel, whose total width is the same as the original. The respective source followers in the driver circuit are split too in the same way. The gates of the array of source followers are tied together, and the drains of the output FET's are tied together to drive the off-chip load. PMOS switches in series with the drain of each source follower activate individual elements of this array by digital control. Only the activated FET's in the output array contribute currents to the antenna, and the sum of these currents is weighted by the digital word applied to the PFET switches. A five-stage circuit yields an output range of  $(2^5 - 1):1$  in current, or 30 dB in power delivered to the load. In this way, power control is built into the core of this circuit.

The circuit responds rapidly to updates in the power control word. As the transmitter turns ON and OFF, a sequence of power control words to optimally shape the attack and decay envelopes of the PA output can lower frequency splatter.

Each side of the quasi-differential PA connects to the off-chip transmission line through a pad and a bondwire. An ordinary CMOS metal pad over the substrate encounters a

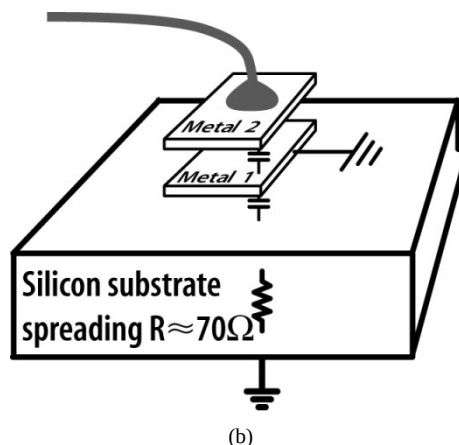
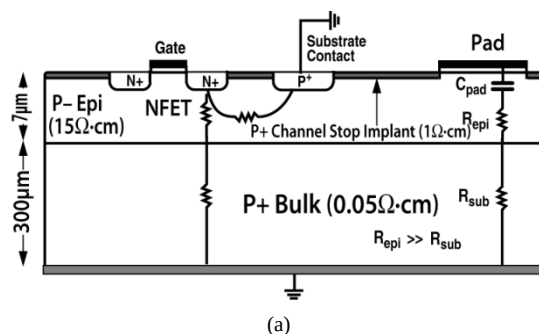


Fig. 25. Sources of RF loss in the CMOS substrate. (a) Model of the substrate showing various parasitic elements of concern. (b) Special shielded RF pad used at PA outputs and LNA inputs.

significant loss at RF because the signal couples capacitively through the oxide into the substrate spreading resistance (Fig. 25). Under a pad  $110 \times 110 \mu\text{m}$  in size, the spreading resistance is about 70  $\Omega$ , and at 900 MHz this dominates the pad impedance to ground. This means that almost half the power intended for the antenna load will be wasted into the substrate, a 3-dB loss in power gain. To prevent this, a special structure called the "RF pad" [23] is used (Fig. 25). It consists of the smallest practicable square of Metal-2 to which a wirebond may attach,  $60 \times 60 \mu\text{m}$  in size, and a common Metal-1 grounded shield placed under two adjacent RF pads carrying balanced signals. The shield connects to off-chip ground via three bondwires to lower the series inductance. This very effectively shields the signals from loss in the substrate spreading resistance. The pad now appears like a lossless capacitor to ground.

A simple matching network transforms the PA output to nearly 50  $\Omega$  (Fig. 24). The network absorbs the pad capacitance, bondwire inductance, and capacitance at the package pins, and requires an external chip inductor of 10 nH. An external RF choke connected to the 3-V supply carries the bias current for the output FET array. The drain voltage of the PA FET's swings above the power supply.

Measurements on a standalone PA prototype [38] with six stages verify that the output power sweeps over the designed range as the digital control word changes from 000001 to 111111 (Fig. 26). The driver's output voltage swing is unaffected by the digital word and is chosen so that all ON FET's in the output array operate at their 1-dB

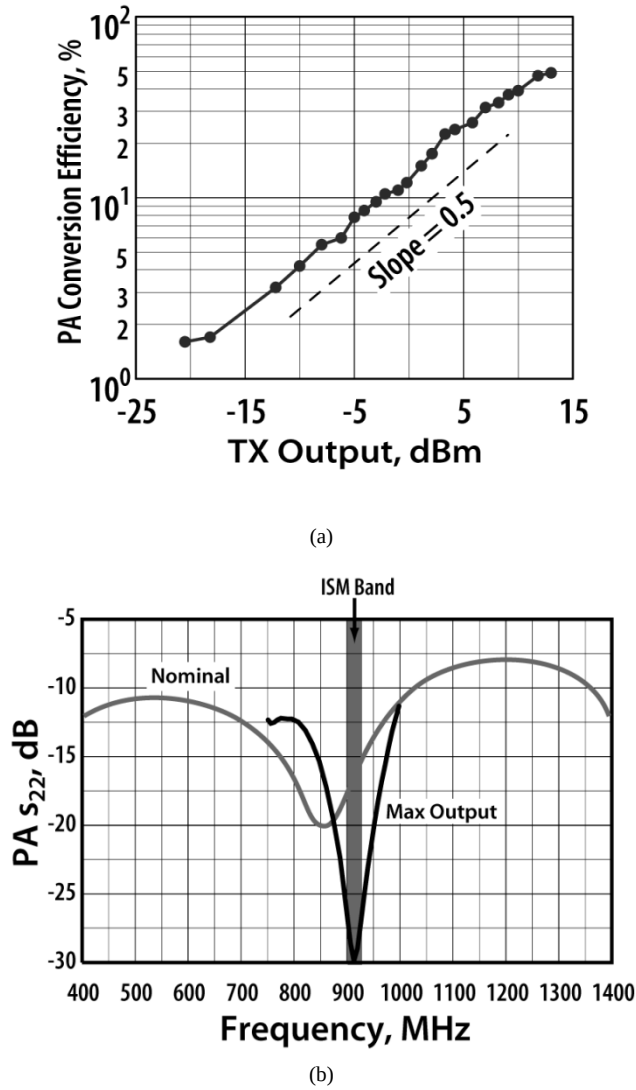


Fig. 26. (a) Measured PA efficiency across full output range. The efficiency conforms to theoretical expectations. (b) Measured output  $s_{22}$  at middle and maximum output power levels.

compression point. This is the optimum condition to amplify a constant-envelope signal with high efficiency. A larger drive into strong saturation will produce higher sidelobes in the output spectrum, which will interfere with adjacent channels; a smaller drive will not sufficiently use the FET's available range.

It is straightforward to predict the dependence of this PA's power conversion efficiency on output power. Efficiency is defined here as the ratio of the RF power delivered to the load to the dc power drawn from the 3-V supply by the PA core, that is, by the output FET array and the corresponding array of source followers. As the preamplifier drives the FET array with the same voltage amplitude under all conditions, the current taken from the supply is proportional to the effective width  $W_{\text{eff}}$  of the array transistors that are activated by the control word. The output FET's are nearly perfect transconductors and deliver a power to the load  $I^2 R$  which is proportional to  $W_{\text{eff}}^2$ . Thus, the efficiency is directly proportional to  $W_{\text{eff}}$ , in other words to the square-root of output power. This trend is clearly

apparent in a logarithmic efficiency plot (Fig. 26). A higher output power at greater efficiency may be obtained by adding progressively larger FET's to the array, until the increased capacitance limits the pole frequency with the 50- $\Omega$  load, or the voltage swing on the load exceeds limits set by the 3-V power supply. The measured power-conversion efficiency at maximum output of +13 dBm is about 50%.

The question arises as to whether a change in the digital word, and thus the output power, also causes the PA output impedance to vary. If the output impedance changes greatly, the match to the 50- $\Omega$  load impedance will worsen at some settings, and this may lower power-conversion efficiency and possibly cause instability. In this context, the large drain junction capacitance of the MOSFET is an unexpected asset because it is attached to the FET output irrespective of whether or not the FET is ON. The shorted-together drain junctions of the FET array present a *constant* capacitance whose susceptance at 900 MHz dominates the  $g_{\text{DS}}$  and governs the PA output admittance.

The measured  $s_{22}$  of the standalone prototype at 900 MHz is -15 dB at mid power levels, and falls to -30 dB at maximum power (Fig. 26). This might appear like a large change in decibels, but it corresponds to a change in the output reflection coefficient from a small value, 0.18, to a yet smaller value, 0.03. This variation is due to the relatively minor change in output impedance contributed by  $r_{\text{DS}}$  as FET's in the array turn ON. This range of  $s_{22}$  is satisfactory as far as efficient power transfer to the load is concerned, and furthermore, the impedance matching holds across a wide bandwidth. This means improved stability. The stability factor [39]  $K$  is 1.4 at 100 MHz, rising to 29 at 2 GHz. A value of  $K$  greater than one guarantees unconditional stability under any load.

#### IV. ISSUES OF MONOLITHIC INTEGRATION

The various building blocks described above are integrated onto a common substrate shared with the receiver. This section describes some of the challenges in buffering the various baseband and RF building blocks and their physical layout.

For convenience, an off-chip PLL is used to lock the RF oscillator to a 10-MHz crystal. An RF output buffer is now required to drive an off-chip prescaler. Another set of FET switch mixers is used for this purpose. The oscillator upconverts a dc input to its own frequency in this mixer, which then drives external 50- $\Omega$  loads; alternatively, one can think of the mixer FET's with dc bias as differential common-source amplifiers. After frequency division and comparison with the 10-MHz reference, the PLL filter output sets the frequency of the on-chip VCO.

The DAC must drive the junction and gate capacitance of the FET switches in the upconversion mixers and also the current into the RC polyphase filter. One possible way to drive this load is to scale up the op amp at the DAC output, but this results in an unacceptably large current drain. Instead, the 50-MHz open-loop buffers described previously (Fig. 11) are scaled to drive this load. It should be noted that these baseband buffers must supply 900-MHz currents into the polyphase filter through the mixers.

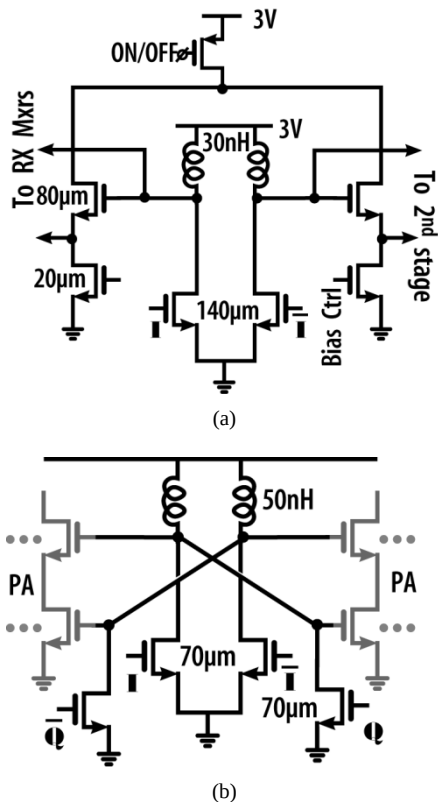


Fig. 27. RF buffers following polyphase filter. (a) First buffer separately amplifies  $I$  and  $Q$  channels and drives receive mixers as well as second buffer in transmitter. (b) Second buffer finally combines  $I$  and  $Q$  channels to select single sideband and drives PA.

Following the upconversion mixers and the RC polyphase filter, other buffers are required to drive the power amplifier and the receiver's downconversion mixers. As the modulated signal after the mixers lies in the 915-MHz band, these buffers must be RF circuits (Fig. 27). The first buffer consists of two common-source stages with inductor loads, which directly distribute the upconverted frequency-hopped sinewave to the receiver mixers. Then through additional source followers they also drive the PA in the transmitter. When the transceiver duplexes from transmit to receive mode, the supply to these source followers is switched off with a series PMOSFET, which isolates the frequency synthesizer from the PA. The buffers equally load the four output nodes of the polyphase filter and thereby preserve quadrature accuracy. Note that the two quadrature paths are so far entirely separate in the transmitter. They now combine in a second-stage buffer, consisting of a differential differencing amplifier with inductor loads, and here one sideband is finally selected (Fig. 27). By inverting the polarity of the  $Q$  digital output, the DDFS controls whether this is the upper or lower sideband. This second-stage buffer is the driver stage to the array of FET's in the PA.

When the transmitter turns off, ideally the PA output should fall to zero. All the PFET's in the PA (Fig. 24) are turned OFF in receive mode to better isolate the PA output. Thus, while the DDFS/DAC supplies a frequency-hopped LO to the receive mixers, it encounters two stages of isolation to the PA output: the OFF power supply switch in the first buffer and

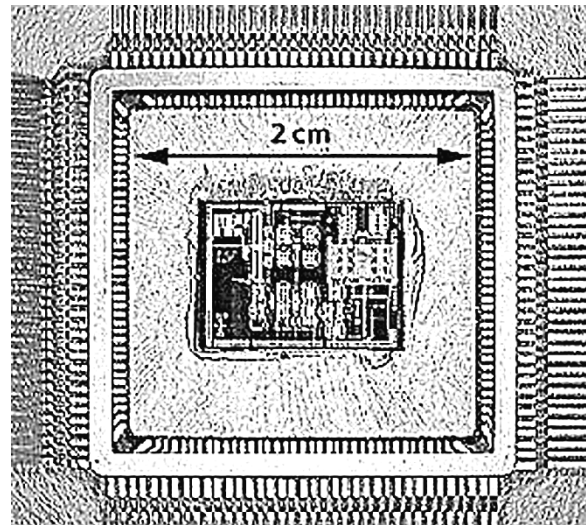


Fig. 28. Photo of chip mounted in TQFP.

the OFF power-control switches in the PA core. As described below, a satisfactory isolation is achieved in practice. There are no series RF switches in the transceiver; all the switching is on the supply currents and bias lines.

## V. EXPERIMENTAL RESULTS

The transceiver chip is mounted in a standard 148-pin ceramic thin quad flat pack (TQFP), designed for use with large digital IC's. Ground bondwires are attached to the grounded metallized paddle in the cavity, while signal and supply bondwires span an average length of about 5 mm from the chip boundary to the traces on the package (Fig. 28). All analog circuits are balanced, and bondwire inductance is of no concern for those circuits operating at a constant current. For differential circuits which do not operate at constant current, only the second harmonic flows through the bondwire inductance to produce a common-mode fluctuation, which the next balanced stage rejects. The bondwire inductance at the RF signal pads in the receiver and the transmitter is absorbed into the respective matching networks.

The transmitter output spectrum is first measured with the DDFS synthesizing a single tone (Fig. 29). There is no RF filter in this measurement. When the DAC operates at the designed full-scale voltage of 1 V<sub>ptp</sub>, the largest spurious tone in the output spectrum is at  $-60$  dBc, consistent with the results obtained from the DAC alone (Fig. 7) [19]. However, dc offset in the DAC output buffers produces a relatively large LO leakage at  $-30$  dBc. The magnitude of the dc offset voltage may be deduced from the spectrum. The desired sideband of the upconverted tone adds in phase at the output of the quadrature mixer, but the upconverted offsets add in quadrature. Therefore, as this is a typical LO leakage across several samples, it may be deduced that

$$\frac{\sqrt{2}\sigma(V_{os})}{V_{FS}} = 10^{\frac{30}{20}} = 10^{-1.5} \Rightarrow \sigma(V_{os}) = 22 \text{ mV}.$$

Recall from Section III-D that Monte Carlo simulations predict a sigma of 16 mV. One way to lower the relative spurious

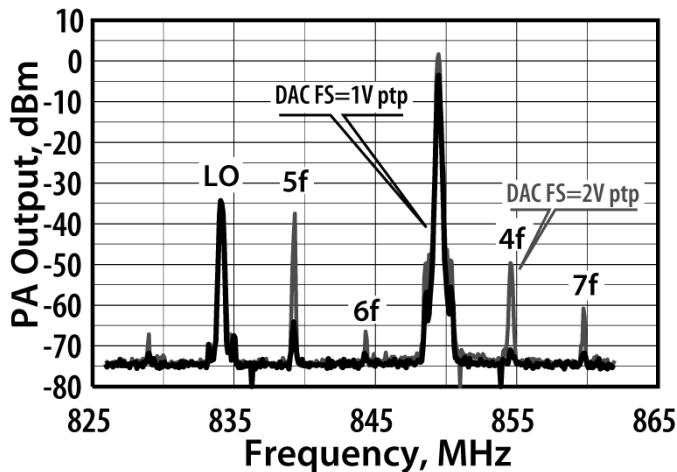


Fig. 29. Measured transmitter output with a single tone, at two different DAC reference voltages. Harmonics and LO leakage are shown. The DAC is designed for a 1 Vptp full-scale.

tone at the LO frequency is to raise the full-scale voltage of the DAC, which increases the sinewave amplitude without affecting the offsets. When doubled to 2 V, the LO leakage is indeed measured to be 6 dB lower. However, the various other harmonics rise substantially (Fig. 29). For instance, the fifth harmonic now grows to almost the same level as the LO leakage. This measurement verifies what may well have been expected in advance, that when the DAC is overdriven, its spurious-free dynamic range rapidly deteriorates. Fig. 30 shows how the various high-order harmonics in a sampled-data waveform and its images will appear in the Nyquist band.

The synthesized waveform with the DAC full-scale set to 2 V is advantageous for the transmitter because it doubles the drive to the PA and leads to a higher transmitted output power. Also, the in-band spurious tones at  $-40$  dBc are tolerable in the transmitted output spectrum. However, this spurious-laden waveform is unacceptable as the dehopping receiver LO, because every large spur may downconvert some nearby channel onto the desired channel. In fact, in the worst case when the channel hops to the edge of the ISM band, some spur may downconvert a very strong narrowband non-ISM-band channel, such as paging transmissions situated at 949 MHz (Fig. 2). This means that the demands on spectral purity in the hopping transmitted signal are vastly different than in the dehopping receiver LO. The solution finally adopted as a compromise in this transceiver is described later.

Upconverted thermal noise in the DAC buffer sets the noise floor at the PA output. The simulated buffer output noise is  $18$  nV/ $\sqrt{\text{Hz}}$ . With the PA set at maximum output level, the subsequent stages amplify this noise by 10 dB to produce a noise floor of  $-132$  dBm/Hz in the  $50\text{-}\Omega$  load. The measured noise floor is  $-134$  dBm/Hz (Fig. 29).

A dither function enabled by a control bit is built into the DDFS. The effect of an LSB dither on the DDFS output on the output spectrum was experimentally investigated. On the whole this is not beneficial (Fig. 31), because dither is found to create many more spurious tones without measurably lowering their average level.

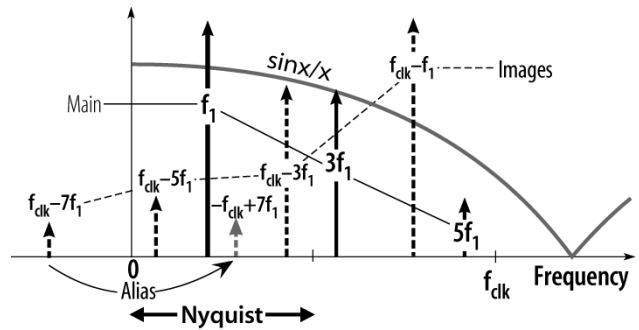


Fig. 30. Illustrating how harmonics and image frequencies appear at the baseband DAC output. These are upconverted in the transmitter, and depending on their phases, are selected as upper or lower sidebands.

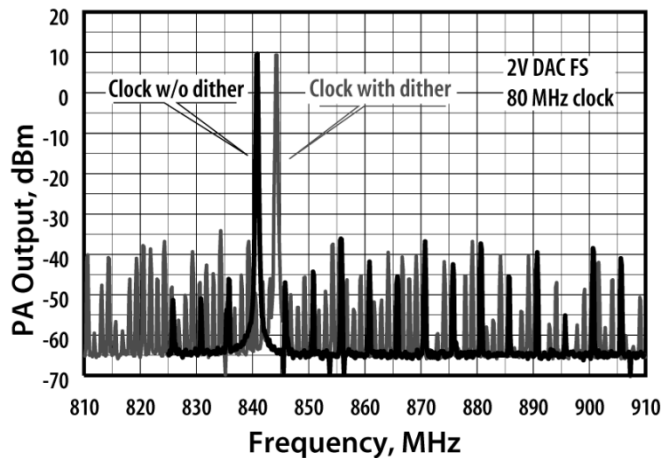


Fig. 31. Measured transmitter output with a single-tone, with and without dithering on the LSB output of the DDFS.

The most important evaluation of the transmitter is with frequency hopping enabled, when it operates as in the intended use. These measurements are now discussed. The DDFS is hopped at a 20-kHz rate to produce a spread-spectrum covering the upper half of the ISM band, 912 to 922 MHz (Fig. 32). The first set of measurements is with the DAC full-scale set to 2 V. Although this is twice as high as the rated full-scale voltage of the DAC, it is found that the specified peak RF output power of 13 dBm cannot be achieved otherwise. This implies that during design, the gain in the transmitter following the DAC was incorrectly overestimated by 6 dB. There is no RF filter between the transmitter and the spectrum analyzer during this measurement. The image-reject mixer suppresses the unwanted sideband by 42 dB, and the various other spurious tones lie at or below this level. When the DAC full-scale is lowered to its designed value of 1 V, the peak output power falls by 6 dB, but with the exception of the LO leakage, the various spurious tones fall by 20 dB! In other words, the spectral purity improves dramatically. The harmonic levels and spurious tones are consistent with measurements on the individual building blocks. Setting aside for a moment the matter of LO leakage, we may conclude that this frequency-hopped transmitter is capable of delivering a signal-to-spurious ratio of about 53 dB at a lower than rated output power. To produce the rated output power with the same spectral purity, the transmitter

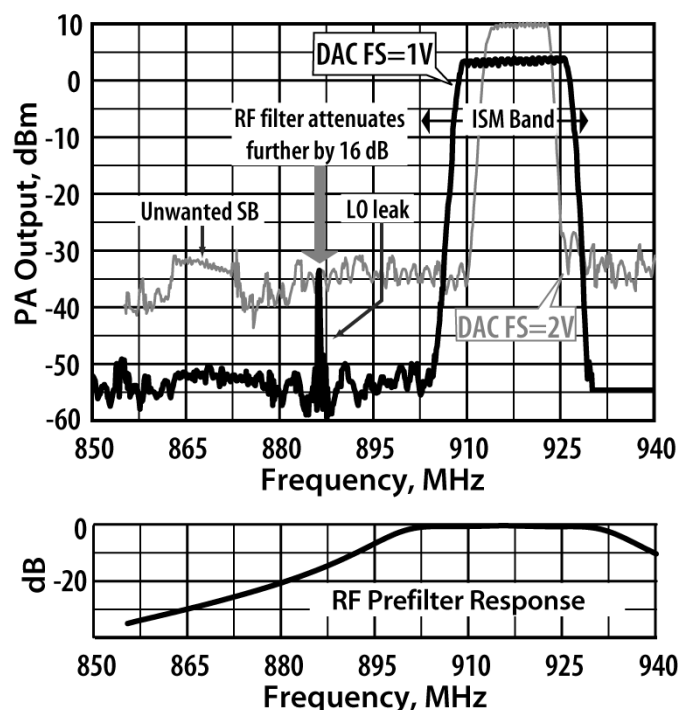


Fig. 32. Measured transmitter output spectrum with frequency-hopped spread-spectrum. Output spectra are compared at two DAC full-scale voltages. Shown below is the measured frequency response of the RF transmitter filter, which will shape the transmitter output.

needs another 6 dB of gain, perhaps distributed between the baseband and the RF sections. For instance, another stage might be added to the power amplifier array (Fig. 24) to raise the output power by 6 dB. It should be noted that most integrated transmitters supply an RF output power of only 0 dBm, which then drives an external power amp module. By comparison, it is much more exacting to develop the required +13 dBm (20 $\times$  more power) on this transmitter IC.

Let us now turn to the issue of LO leakage in the transmitter output spectrum. Although the signal hops in frequency, the LO leakage is static. Even with the DAC full-scale set to 1 V, LO leakage concentrates at a single frequency with a level of  $-40$  dBc. This is unacceptably high. However, if the RF oscillator is tuned to a frequency *below* the ISM band (the reader may have noticed that in the measurements presented here, it is tuned to 887 MHz, 15 MHz below the ISM band), and the DDFS/DAC is clocked faster to synthesize *higher* frequency sinewaves (in this case, higher by 15 MHz), then the LO leakage will fall in the transition band of the RF filter at the transmitter output and be attenuated. The RF filter used in this transceiver attenuates signals 15 MHz into the transition band by 16 dB (Fig. 32). This pushes down the radiated LO leakage to  $-56$  dBc and satisfies FCC requirements.

Another way to lower LO leakage is to suppress the dc offsets appearing at the mixer inputs. It is not practical to do so with series on-chip coupling capacitors, because, first, this requires a very large capacitor, and second, the signal would suffer an unacceptable voltage division between this capacitor and its bottom-plate parasitic to ground. A more practical solution is to use a dc nulling loop outside the signal

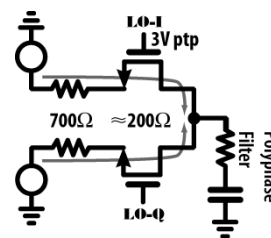


Fig. 33. The gain in quadrature mixer channels is well-matched because of the large and well-matched source resistors, and as a result of the large LO signal applied at the gates of the FET's.

path, which samples the dc component at the mixer input with an offset-compensated amplifier and corrects it at the DAC output. If the RF oscillator is positioned outside the ISM band, the DDFS/DAC must produce a baseband spread-spectrum which is dc-free. The loop removing offsets will therefore not remove valuable signal spectrum.

It is also remarkable that the image-rejection mixer suppresses the unwanted sideband by 55 dB (Fig. 32). As discussed earlier, the RC polyphase filter cannot suppress the effect of random errors in gain between the *I* and *Q* mixer channels or departures from quadrature phases of the LO. With reference to Fig. 16, this implies that in this mixer the phase error from quadrature is  $0.2^\circ$  or less, and the gain mismatch between the mixer channels is 0.03 dB (0.3%) or less. The phase accuracy may be attributed to the oscillator used here (Fig. 19), which inherently yields very precise quadrature phases, insensitive to small imbalances in the four *LC* resonant circuits. To understand how gain matching is achieved, consider a simplified circuit diagram of the image-suppression mixer (Fig. 33). In the absence of phase errors, if the amplitudes of the two currents are exactly equal, the image will be completely suppressed. The baseband signals are produced by two differential pairs whose transconductances are well-matched by the polysilicon degeneration resistors (Fig. 11). These buffers present an output resistance of  $700\ \Omega$ , also set by well-matched polysilicon resistor loads. By dominating the mixer FET ON resistance of about  $200\ \Omega$ , these resistors mask any mismatch in the FET resistance. This mismatch mainly arises from fluctuations in average inversion layer mobility in the two FET's; the effect of threshold voltage mismatch is not felt as seriously because of the large LO drive at the mixer FET gates.

Yet another practical concern in a transmitter is frequency pulling. This arises from inevitable interactions between the large PA output and the LO, for instance because of finite reverse isolation in the upconversion mixers, or through stray coupling on the transceiver board between the PA output pins and the LO's external resonator (Fig. 34). It is particularly of concern in time-division duplexed (TDD) systems, where rapid duplexing at the frame rate can throw the local oscillator out of the PLL lock range. This parasitic effect is measured in this transmitter by switching the PA output from minimum to maximum and then noting the steady-state shift in frequency of the *unlocked* RF oscillator. The free-running frequency is pulled by only 200 kHz, or 220 parts-per-million. The PLL locking the oscillator can easily correct this. In fact, as the

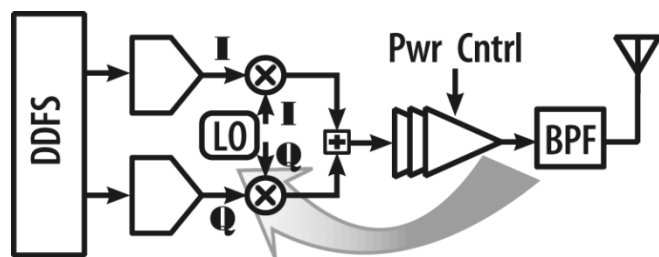


Fig. 34. Parasitic coupling from the PA to the transmitter LO causes frequency pulling when the transmitter turns on and off.

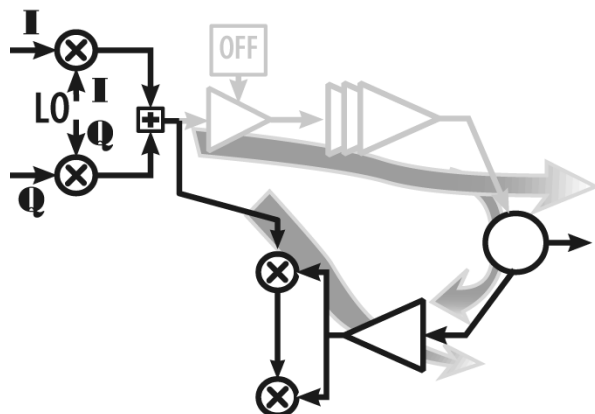


Fig. 35. Various paths through which the synthesizer output couples into the receiver front-end.

transceiver uses only a fixed-frequency oscillator, the PLL bandwidth is designed to suppress frequency pulling and the close-in phase noise. This small frequency pulling is mainly a result of the fully differential transceiver design, which rejects most parasitic interactions as common-mode. It is also due to the fully integrated LO which, aside from the heavily filtered control voltage line from the external PLL, does not interact with any external components which are liable to pick up stray signals on the transceiver board.

The signal leaking through the shut-off transmitter, while the transceiver is in receive mode, is also measured (Fig. 35). This tests the degree to which turning OFF the PA buffer and the power amplifier FET's isolates the frequency synthesizer output from leaking into the antenna. The main concern here is that if this residual emission from the PA couples into the LNA input via parasitic paths in the IC substrate, or through the capacitance between the PA output and LNA input pins on the IC package, it may overwhelm the weak signal of interest being received at the antenna. Also of concern is the practical matter that when it is in OFF mode, a transmitter must not emit a signal.

The measured transmit output power level drops by 65 dB from its maximum value when the PA and its buffer are turned OFF. During receive mode, therefore, the transmitter emits a low-level signal on the order of  $-50$  dBm into the antenna. The next question is: how much of this unwanted emission couples into the receiver input? To ascertain this, the signal appearing at the antenna side of the receiver balun, with the antenna disconnected, is measured on a spectrum analyzer. A

very weak signal of  $-92$  dBm is found here, whose spectrum is identical to the LO port drive at the receive mixers. Most likely this couples into the LNA by reverse leakage through the receive mixers. However, direct coupling through the leaky transmitter cannot be ruled out, nor coupling through the substrate. In any event, this signal will enter the LNA and always self-downconvert to dc, because it is at exactly the same instantaneous frequency as the de hopping LO applied to the mixer. Now, as described in the companion paper [40], the receiver is designed to tolerate a large dc offset, so this parasitic coupling into the receiver input does not compromise its dynamic range.

## VI. DISCUSSION

A transceiver architecture is described for frequency-hopped communications which exploits the mixed analog-digital capabilities of CMOS in various important ways. The hopping frequency is synthesized at baseband in a digital circuit. A glitch-free DAC, which exploits the sample-and-hold properties of CMOS, converts this into an analog waveform. An LO, which need only produce a fixed frequency with low phase noise, upconverts the hopped waveform to the 902–928 MHz ISM band. The FET's insulating gate allows a large amplitude of oscillation, which is key to lowering close-in phase noise. The power amplifier exploits digital switch selection for power control, and again the FET insulating gate is important in achieving good efficiency. These various instances illustrate a comprehensive CMOS-oriented design approach to wireless transmitter design.

Another important feature of this fully integrated architecture is that all analog signals are *balanced*, and as far as possible they are maintained in *quadrature phases*, which is made use of to cancel several unwanted frequencies. We conjecture that this approach also significantly lowers parasitic effects such as frequency pulling, which handicap the practical use of wireless transceivers.

The following paper in this issue [40] describes details of the physical packaging of the transceiver IC, power consumption of the various blocks, and other aspects of integrating the transmitter with the receiver on a common substrate.

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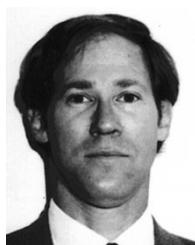
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