

TP 3.3: A Single-Chip CMOS Transceiver for DCS-1800 Wireless Communications

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This CMOS transceiver chip for the DCS-1800 wireless communication system is realized in a 0.25 μ m CMOS process [1]. The realization of a CMOS transceiver that complies with the specifications of a high-quality digital-wireless system requires overall integration of architecture, building block and transistor-level design. A highly-integrated architecture minimizes the number of high-frequency external nodes, as these are difficult to drive with CMOS circuits. Up- and downconversion topologies allow at the same time mixing and a high-quality on-chip single-ended to differential conversion. Extra buffers between building blocks optimize overall circuit performance.

Figure 1 shows a schematic of the architecture of the DCS-1800 transceiver. The transmitter and receiver are realized on the same die in combination with a synthesizer. A single synthesizer serves both receiver and transmitter. For testing, only the VCO is implemented in this chip version. The full synthesizer is described in Reference 2. The selected architecture is a direct upconversion transmitter, combined with a low-IF receiver [3]. Both allow for a single-stage conversion, without requiring high-frequency filtering between stages. The low-IF receiver uses 100kHz IF. It has the same high degree of integration as a zero-IF receiver, however, without the disadvantage of the highly sensitive baseband operation typical for the zero-IF receiver. To meet the DCS-1800 specifications, the low-IF architecture must have 35dB mirror signal suppression (i.e., quadrature accuracy), 5dB total noise figure, high-frequency input linearity of -4dBm IP3 and oscillator phase noise < -122dBc/Hz at 600kHz from the carrier. Direct upconversion topology gives the same degree of integration. Its disadvantage is sensitivity to parasitic modulation of the oscillator through coupling with the high-power antenna signal that is located at the same frequency. To reduce this parasitic coupling significantly a fully-integrated VCO with on-chip inductor is used [4]. In this way, there is no external high-frequency node that can easily pick up the transmitted antenna signal.

The VCO drives its differential signal in a three-stage polyphase filter for quadrature generation (Figure 2). Two source followers are used as buffers between the VCO output and the polyphase filter. The outputs of the polyphase filter drive the LO inputs of both the up- and downconverter, these are nMOS gates and nMOS drains respectively. Separate buffers are used so the capacitive load of the upconverter does not load the resistive input of the downconverter. The upconverter uses an nMOS resistor-loaded cascode stage, the downconverter uses a pMOS current-source-loaded cascode stage.

The upconversion mixer is based on an intrinsic linear mixer circuit that converts a quadrature baseband signal and a local oscillator signal into a modulated high-frequency current via four nMOS transistors modulated in their linear region [5]. 2GHz broadband operation is achieved by using an output buffer with an active-coil load (transistor M6) instead of a true inductive load (Figure 3). An important aspect of the circuit is the additional large on-chip capacitor at the baseband input node. In this way

the RF-modulated signal linearity and amplitude are not degraded by the output impedance of the baseband signal source nor by the bonding wire impedance or matching. Special attention is given the matching between the I and Q paths in order to ensure a high mirror signal suppression.

Figure 4 shows a schematic of the downconversion path. The LNA circuit topology consists of a single-stage resistor loaded cascode amplifier with a low-Q voltage boosting input section based on the resonator formed with the bondwire inductor. The passive input section provides an extra 3dB of amplification. The input transistor M1 uses a VGS-VT of 250mV, sufficient to obtain the required linearity of -4dBm input IP3. The downconversion mixers, also shown in Figure 4, use 2 nMOS transistors modulated in the linear region. The classic cross-coupling with 4 transistors is not used, with the advantage that the downconversion mixers can at the same time act as high-quality single-ended to differential converters for the RF signal. Because only two mixing transistors are used, an active coil circuit must be used in the input buffers so they are able to suppress the low frequency signal generated due to the dependence of gds on VDS.

Figure 5 shows a micrograph of the DCS-1800 transceiver realized in standard 0.25 μ m CMOS. The die is 8.6mm². Total power is 192mW from a 2.0V power supply, and 240 mW from a 2.5 V power supply. This latter is subdivided as follows: downconversion path, 75mW; upconversion, 50mW; oscillator, 15mW; and quadrature generator (buffers included), 100mW.

For the VCO measured phase noise is -123.6dBc/Hz at 600kHz from the carrier. All measurements are in the DCS-1800 band with 2.0V power supply. Figure 6 shows the output spectrum of the upconverter modulated with a 1MHz single-sideband signal. The measured local-oscillator-to-carrier suppression is 33dB and the measured mirror-signal suppression is >38dB, equivalent to a 0.7° phase error.

Figure 7 shows results of linearity measurements of the downconverter-LNA combination. The measured input IP3 is -3.0dBm. With a 2.0V power supply the measured noise figure for the total receiver is 12.5dB. With a 2.5V power supply, measured noise figure is 4.9dB, within the DCS-1800 specification. Conversion gain at 1.88GHz is 32.5dB. Low-frequency bandwidth is 500kHz and the phase accuracy measured on the low-frequency downconverted I and Q signals is 0.6°.

References:

- [1] Sevenhans, J., et al., "An Analog Radio front-end Chip Set for a 1.9GHz Mobile Radio Telephony Application," ISSCC Digest of Technical Papers, pp.44-45, Feb., 1994.
- [2] Craninckx, J., M. Steyaert, "A Fully Integrated CMOS DCS-1800 Frequency Synthesizer," ISSCC Digest of Technical Papers, Feb., 1998
- [3] Crols, J., M. Steyaert, *CMOS Wireless Transceiver Design*, Boston: Kluwer Academic Publishers, 1997.
- [4] Craninckx, J., M. Steyaert, H. Miyakama, "A Fully Integrated Spiral-LC CMOS VCO Set with Prescaler for GSM and DCS-1800 Systems," Proc. CICC, pp.403-406, May, 1997.
- [5] Borremans, M., M. Steyaert, "A 2V, Low Power, Single-Ended 1GHz CMOS Direct Upconversion Mixer," Proc. CICC, pp.517-520, May, 1997.

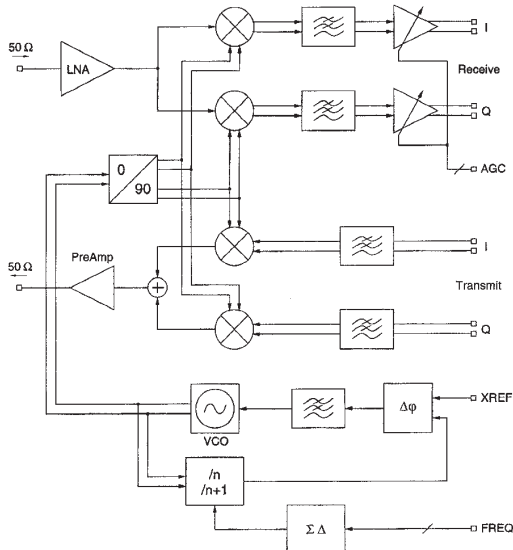


Figure 1: Block schematic of low-IF receiver/direct upconversion architecture.

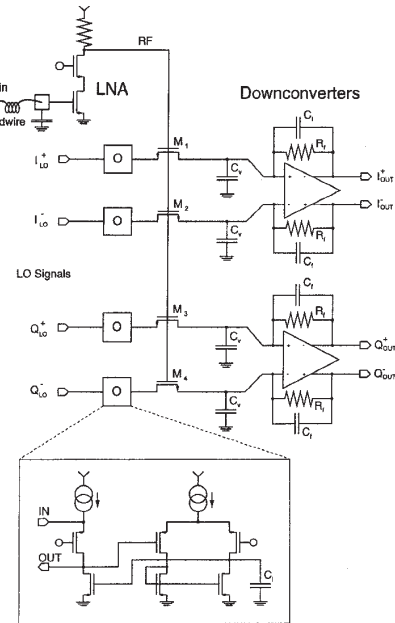


Figure 4: Low-noise amplifier and downconverter.
Figure 5: See page 411.

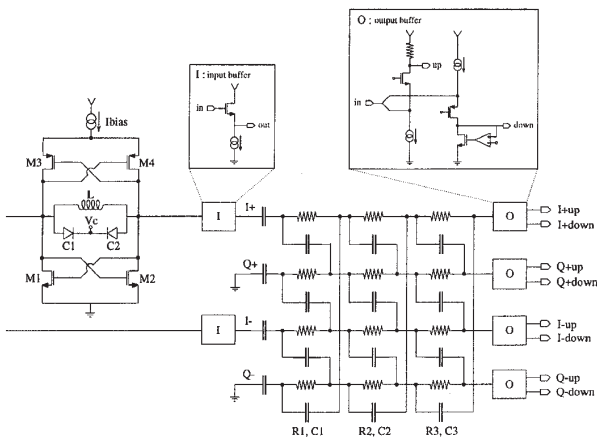


Figure 2: Generation of quadrature oscillator signal.

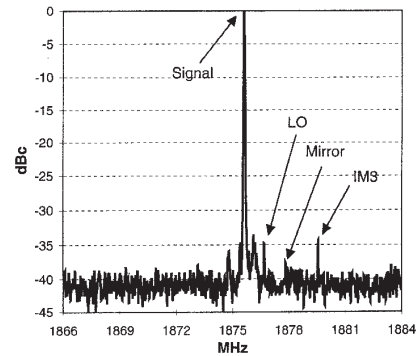


Figure 6: Measured output spectrum of full transmitter.

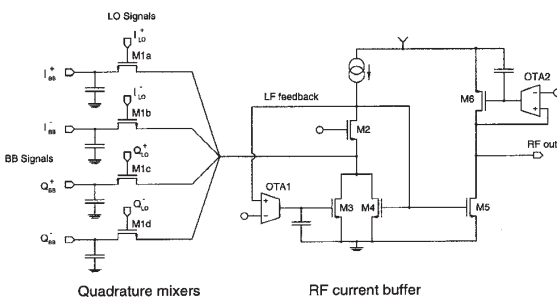


Figure 3: Linear upconversion quadrature mixers and output current buffer.

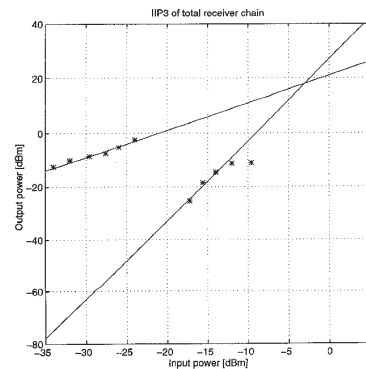


Figure 7: Receiver IP3 measurement results.