A CMOS Frequency Synthesizer with an Injection-Locked Frequency Divider for a 5-GHz Wireless LAN Receiver

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***Abstract*—A fully integrated 5-GHz phase-locked loop (PLL) based frequency synthesizer is designed in a 0.24 μm CMOS technology. The power consumption of the synthesizer is significantly reduced by using a tracking injection-locked frequency divider (ILFD) as the first frequency divider in the PLL feedback loop. On-chip spiral inductors with patterned ground shields are also optimized to reduce the VCO and ILFD power consumption and to maximize the locking range of the ILFD. The synthesizer consumes 25 mW of power of which only 3.8 mW is consumed by the VCO and the ILFD combined. The PLL has a bandwidth of 280 kHz and a phase noise of −101 dBc/Hz at 1 MHz offset frequency. The spurious sidebands at the center of adjacent channels are less than −54 dBc.**

***Index Terms*—CMOS RF circuits, frequency synthesizers, injection-locked frequency dividers, wireless LAN.**

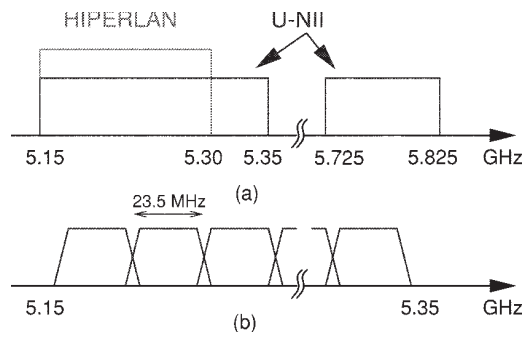

Fig. 1. (a) U-NII and HIPERLAN frequency bands and (b) channel allocation in our U-NII band WLAN system.

I. Introduction

THE DEMAND for wireless local area network (WLAN) systems which can support data rates in excess of 20 Mb/s with very low cost and low power consumption is rapidly increasing. The newly released unlicensed national information infrastructure (U-NII) frequency band in the United States is primarily intended for wideband WLAN and provides 300 MHz of spectrum at 5 GHz [Fig. 1(a)]. The lower 200 MHz of this band (5.15–5.35 GHz) overlaps the European high-performance radio LAN (HIPERLAN) frequency band. The upper 100 MHz of the spectrum which overlaps the industrial, scientific, and medical (ISM) band is not used in our system. To stay compatible with HIPERLAN the lower 200 MHz of the spectrum is divided into eight channels which are 23.5 MHz wide [Fig. 1(b)]. The minimum signal level at the receiver is −70 dBm while the maximum strength of the received signal is −20 dBm. The large dynamic range and wide channel bandwidths set very stringing requirements for the synthesizer phase noise and spurious sideband levels.

In this paper we describe the design of a fully integrated integer-N frequency synthesizer as a local oscillator (LO) for a U-NII band WLAN receiver. The front end of the receiver is described in [9].

Section II describes some of the synthesizer design challenges and reviews previously existing solutions. In Section III we present our proposed architecture of the frequency synthesizer which takes advantage of an injection-locked frequency divider (ILFD) to reduce the overall power consumption. Section IV-A is dedicated to the design of the VCO and demonstrates how on-chip spiral inductors can be optimized to reduce the VCO power consumption and to improve the phase noise performance at the same time. Section IV-B describes the design issues of ILFD's as well as the optimization of on-chip spiral inductors for wide-locking-range and low-power ILFD's. The pulse swallow frequency divider, charge pump, and loop filter are the subjects of Sections IV-C, IV-D, and IV-E, respectively. The measurement results are presented in Section V and conclusions are made in Section VI.

II. Frequency Synthesizers

Frequency synthesizers are an essential part of wireless receivers and often consume a large percentage (20–30%) of the total power (Table I). A typical PLL-based frequency synthesizer comprises both high and low frequency blocks. The high frequency blocks, mainly the VCO and first stage of the frequency dividers, are the main power consuming blocks, especially in a CMOS implementation. Therefore, BiCMOS technology has often been chosen over CMOS, where the VCO and the prescaler are designed with bipolar transistors and the low frequency blocks are CMOS [1]. Off-chip VCO's and dividers have also been used as an alternative [4]. However, because of the increased cost neither of these two solutions is suitable for many applications, and a fully integrated CMOS solution is favorable. A dividerless frequency synthesizer [11] which eliminates power–hungry frequency dividers is one solution for such low-power and fully integrated systems. In this technique an

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TABLE I
POWER CONSUMPTION OF FULLY INTEGRATED WIRELESS RECEIVERS

Reference	Receiver power	PLL power
[10]	115mW	36mW
[13],[2]	225mW	51mW

aperture phase detector is used to compare the phase of the reference signal and the VCO output at every rising edge of the reference signal for only a time window which is a small fraction of the reference period. Thus no frequency divider is required in this PLL. The idea of a dividerless frequency synthesizer, although suitable for systems such as a GPS receiver where only one LO signal is required, is not readily applied to wireless systems which require multiple LO frequencies with a small frequency separation.

III. PROPOSED SYNTHESIZER ARCHITECTURE

Our proposed architecture (Fig. 2) is an integer-N frequency synthesizer with an initial low power divide-by-two in the PLL feedback loop. The prescaler follows the fixed frequency divider and operates at half the output frequency, thus, its power consumption is reduced significantly. Furthermore, the first divider is an injection-locked frequency divider [6], [7] which takes advantage of the narrowband nature of the system and trades off bandwidth for power via the use of resonators. To further reduce the power consumption, optimization techniques are used to design the on-chip spiral inductors of the VCO and ILFD.

Because of the fixed initial divide-by-two in the loop the reference frequency in our system is half of the LO spacing and is 11 MHz. Consequently, the loop bandwidth is reduced to maintain the loop stability. This bandwidth reduction helps to filter harmonics of the reference signal, mainly the second harmonic, which generate spurs in the middle of the adjacent channels. The drawbacks of a reduced loop bandwidth are an increased settling time and a higher in-band VCO phase noise. The higher in-band VCO phase noise is not a limiting factor as the in-band noise is dominated by the upconverted noise of the reference signal. The slower settling time is only a problem in very fast frequency-hopped systems.

The synthesized LO frequency in our system is 16/17 of the received carrier frequency. This choice of LO frequency not only eases the issue of image rejection in the receiver [9], but also facilitates the generation of the second LO, which is 1/16 of the first LO, with the same synthesizer.

IV. SYNTHESIZER BUILDING BLOCKS

A. Voltage-Controlled Oscillator

Fig. 3 shows the schematic of the VCO. Two cross-coupled transistors M1 and M2 generate the negative impedance required to cancel the losses of the RLC tank. On-chip spiral inductors with patterned ground shields [15] are used in this design. The two main requirements for the VCO are low phase noise and low power consumption. If the inductors were the main source of noise, maximizing their quality factor would improve the phase noise significantly. However, in multi-GHz VCO's with short channel transistors, inductors are not the

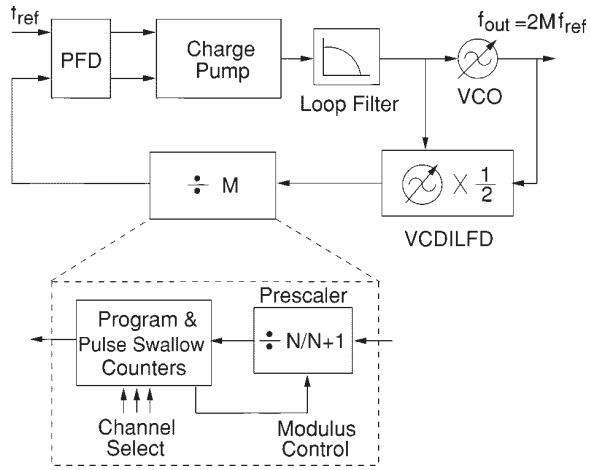

Fig. 2. Frequency synthesizer block diagram.

main source of noise and a better design strategy is to maximize the effective parallel impedance of the RLC tank at resonance. This choice increases the oscillation amplitude for a given power consumption and hence reduces the phase noise caused by the noise injection from the active devices. Since inductors are the main source of loss in the tank, the LQ product should be maximized to maximize the effective parallel impedance of the tank at resonance, where L is the inductance and Q is the quality factor of the spiral inductors. It is important to realize that maximizing Q alone does not necessarily maximize the LQ product, and it is the latter that matters here.

To design the spiral inductors, we use the same inductor model reported in [14]. The inductance is first approximated with a monomial expression as in [3]. Optimization is used next to find the inductor with the maximum LQ product. The inductors in this design are 2.26 nH each with an estimated quality factor of 5.8 at 5 GHz. It is worth mentioning that at 5 GHz, the magnetic loss in the highly doped substrate of the epi process reduces the inductor quality factor significantly. Approximate calculations show that substrate inductive loss is proportional to the cube of the inductor's outer diameter. Therefore, a multilayer stacked inductor which has a smaller area compared to a single-layer inductor with the same inductance may achieve a larger quality factor. We should mention that in our design, inductors are laid out using only the top-most metal layer.

The varactors in Fig. 3 are accumulation-mode MOS capacitors [5], [12]. The quality factor of these varactors can be substantially degraded by gate resistance if they are not laid out properly. In our design each varactor is laid out with 14 fingers which are 3 μm wide and 0.5 μm long. The quality factor of this varactor at 5 GHz is estimated to exceed 60. The losses of the *RLC* tank are thus dominated by the inductors, as expected.

B. Injection-Locked Frequency Divider

Fig. 4 shows the schematic of the voltage–controlled ILFD used in the frequency synthesizer. The incident signal (the VCO output) is injected into the gate of M3 and is delivered with a subunity voltage gain to Vx, the common source connection of M1 and M2. Transistor M4 is used to provide a symmetric

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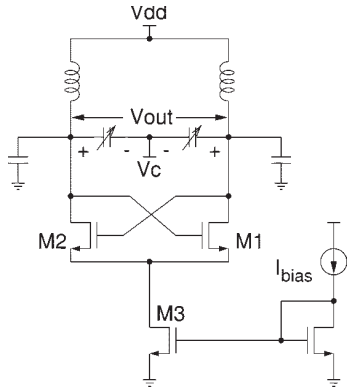

Fig. 3. Schematic of the VCO.

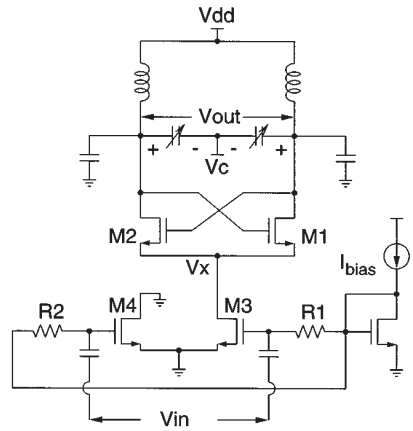

Fig. 4. Schematic of the differential ILFD.

load for the VCO. The output signal is fed back to the gates of M1 and M2 and is summed with the incident signal across the gates and sources of M1 and M2. The nonlinearity of M1 and M2 generates intermodulation products which allow sustained oscillation at a fraction of the input frequency [6]. As shown in [6] in the special case of a divide-by-two and a third-order nonlinearity, the phase-limited locking range of an LC ILFD can be expressed as

$$\left|\frac{\Delta\omega}{\omega_r}\right| < \left|\frac{H_0 a_2 V_i}{2Q}\right| \tag{1}$$

where

ω_r free–running oscillation frequency;
$\Delta\omega$ frequency offset from ω_r;
V_i incident amplitude;
H_0 impedance of the RLC tank at resonance;
Q quality factor of the RLC tank;
a_2 second-order coefficient of the nonlinearity.

As (1) suggests, a larger incident amplitude as well as a larger H_0/Q result in a larger achievable $\Delta\omega$ which we refer to as the *locking range*. In an LC oscillator $(H_0/Q) = \omega L$, so the largest practical inductance should be used to maximize the locking range.

A larger quadratic nonlinearity (a_2) also increases the locking range. So a circuit architecture with a large second-order nonlinearity is favorable for a divide-by-two ILFD and in fact the circuit in Fig. 4 has such a characteristic. The common source connection node of the differential pair moves at twice the frequency of the output signal even in the absence of the incident signal. So this circuit has a natural tendency for divide-by-two operation when the incident signal is effectively injected into node Vx.

To further extend the locking range, the ILFD is designed such that the resonant frequency of its output tank tracks the input frequency. Accumulation mode MOS varactors are used to tune the ILFD and its control voltage is tied to the VCO control voltage (Fig. 2). The locking range of the ILFD therefore does not limit the tuning range of the PLL beyond what is determined by the VCO.

As in the VCO design, on-chip spiral inductors with patterned ground shields are used in the ILFD, but with a different optimization objective. As mentioned earlier the largest practical inductance L maximizes the locking range. However, reduction of power consumption demands maximization of the LQ product. The inductor has its largest value when the total capacitance that resonates with it is minimized. To reduce its parasitic bottom plate capacitance the inductor should be laid out with narrow topmost metal lines. However, the large series resistance of narrow metal strips degrades the inductor quality factor and reduces the LQ product significantly. Therefore, both L and the LQ product may not be maximized simultaneously for an on-chip spiral inductor resonating with a fixed capacitance. Optimization is thus used to design for the maximum inductance such that the LQ product is large enough to satisfy the specified power budget. The inductors resulting from this trade-off are 9.5 nH each with an estimated quality factor of 4.2 at the divider output frequency (2.5 GHz).

C. Pulse Swallow Frequency Divider

The pulse swallow frequency divider ($\div$M) consists of a $\div 22/23$ prescaler followed by a program and pulse swallow counter. Only one CMOS logic ripple counter is used for both program and pulse swallow counters. The program counter generates one output pulse for every ten input pulses. The output of the pulse swallow counter is controlled by three channel select bits. The overall division ratio is 220–227. At the beginning of the cycle the prescaler divides by 23. As soon as the first three bits of the ripple counter match the channel select bits, the prescaler begins to divide by 22. The next cycle starts after the ripple counter counts to ten.

The prescaler consists of three dual-modulus divide-by-2/3 and one divide-by-2 frequency divider made of source-coupled logic (SCL) flip-flops and gates (Fig. 5). The modulus control (MC) input selects between divide-by-22 and divide-by-23. Except for the second dual modulus all other dividers including the CMOS counters are triggered by the falling edges of their input clocks, allowing a delay of as much as half the period of the input of each divider. With this arrangement we guarantee overlap between O_2, O_3, and O_4 (Fig. 5) and prevent a race condition.

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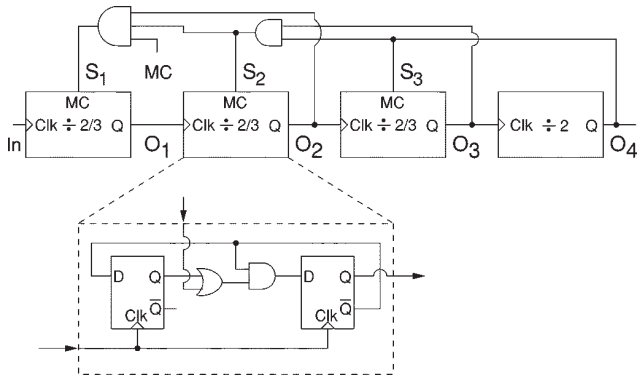

Fig. 5. Block diagram of the prescaler.

D. Charge Pump

Fig. 6 shows the circuit diagram of the charge pump and loop filter. The charge pump has a differential architecture. However, only a single output node, O_p, drives the loop filter. To prevent the node O_n from drifting to the rails when neither of the up and down signals (U and D) is active, the unity gain buffer shown in Fig. 6 is placed between the two output nodes. This buffer keeps the two output nodes at the same potential and thus reduces the charge pump offset. The power of the spurious sidebands in the synthesized output signal is thereby reduced. In this charge pump the current sources are always on and the PMOS and NMOS switches are used to steer the current from one branch of the charge pump to the other.

E. Loop Filter

Resistor R_1 and capacitor C_1 in the loop filter (Fig. 6) generate a pole at the origin and a zero at $1/(R_1C_1)$. Capacitor C_2 and the combination of R_3 and C_3 are used to add extra poles at frequencies higher than the PLL bandwidth to reduce reference feedthrough and decrease the spurious sidebands at harmonics of the reference frequency. The thermal noise of R_1 and R_3, although filtered by the loop, directly modulates the VCO control voltage and can cause substantial phase noise in the VCO if the resistors are not sized properly. The capacitors and resistors of the loop filter should be properly chosen to perform the required filtering function and maintain the stability of the loop without introducing too much noise. Fig. 7 shows a linearized phased-locked loop model. In a third-order loop, the loop filter contains only R_1, C_1, and C_2 and its impedance can be written as

$$Z(s) = \left(\frac{b}{b+1}\right)\frac{\tau s+1}{sC_1(\frac{\tau s}{b+1}+1)} \tag{2}$$

where $\tau = R_1C_1$ and $b = C_1/C_2$. The open loop transfer function of the third-order PLL is

$$\frac{\varphi_o}{\varphi_i} = \frac{K_{\text{vco}}I_p}{2\pi}\left(\frac{b}{b+1}\right)\frac{\tau s+1}{s^2C_1(\frac{\tau s}{b+1}+1)} \tag{3}$$

where K_{vco} is the VCO gain constant and I_p is the charge pump current. The phase margin of the loop is

$$PM = \tan^{-1}(\tau\omega_c) - \tan^{-1}\left(\frac{\tau\omega_c}{b+1}\right) \tag{4}$$

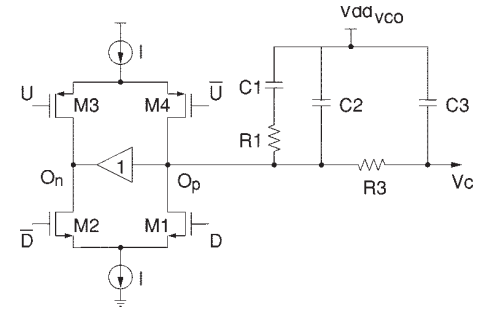

Fig. 6. Simplified schematic of the charge pump and loop filter.

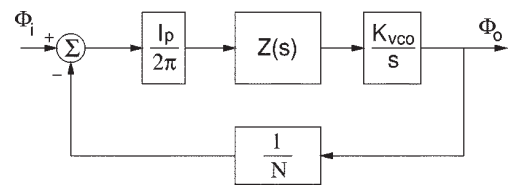

Fig. 7. Linearized PLL model.

where ω_c is the crossover frequency. By differentiating (4) with respect to ω_c it can be shown that the maximum phase margin is achieved at

$$\omega_c = \sqrt{b+1}/\tau \tag{5}$$

and the maximum phase margin is

$$PM_{\max} = \tan^{-1}(\sqrt{b+1}) - \tan^{-1}\left(\frac{\sqrt{b+1}}{b+1}\right). \tag{6}$$

Notice that the maximum phase margin is only a function of b (ratio of C_1 and C_2) and for b less than 1 the phase margin is less than 20° which makes the loop practically unstable.

To complete our loop analysis we force $\omega_c = \sqrt{b+1}/\tau$ to be the crossover frequency of the loop and get

$$\frac{K_{\text{vco}}I_p}{2\pi N}\left(\frac{b}{b+1}\right) = \frac{C_1}{\tau^2}\sqrt{b+1}. \tag{7}$$

Now we can define a loop filter design recipe as follows.

1) Find K_{vco} from the VCO simulation.
2) Choose a desired phase margin and find b from (6).
3) Choose the loop bandwidth and find τ from (5).
4) Select C_1 and I_p such that they satisfy (7).
5) Calculate the noise contribution of R_1. If the calculated noise is negligible the design is complete, otherwise go back to step four and increase C_1.

The same loop analysis can be repeated for a fourth-order loop. In this case the phase margin is

$$PM = \tan^{-1}(\tau\omega_c) - \tan^{-1}\left(\frac{A(\tau\omega_c)}{1-B(\tau\omega_c)^2}\right) \tag{8}$$

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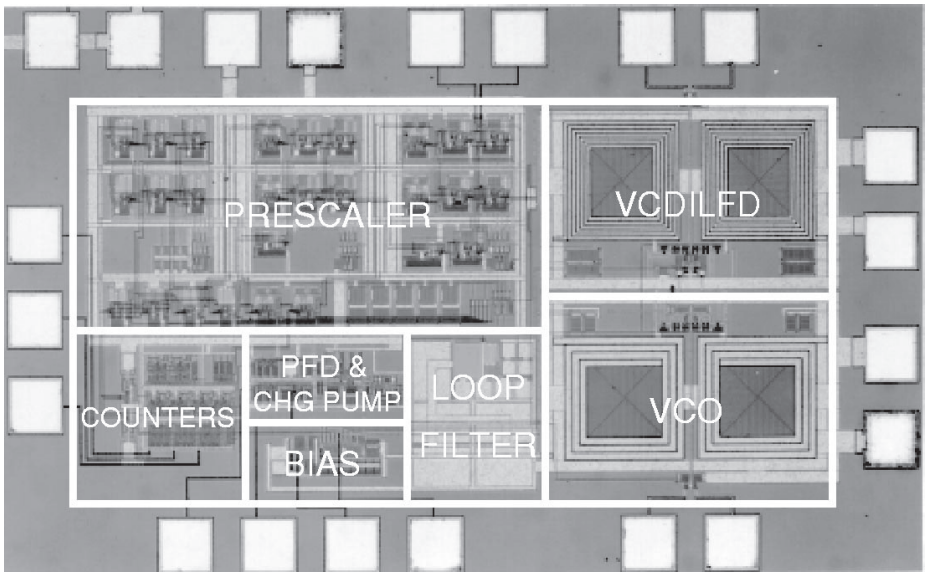

Fig. 8. Die micrograph.

where

$$A = \frac{\frac{C_2}{C_1} + \frac{C_3}{C_1} + \frac{\tau_2}{\tau}\left(1 + \frac{C_2}{C_1}\right)}{1 + \frac{C_2}{C_1} + \frac{C_3}{C_1}}$$

$$B = \frac{\frac{C_2}{C_1}\frac{\tau_2}{\tau}}{1 + \frac{C_2}{C_1} + \frac{C_3}{C_1}}$$

and $\tau_2 = R_3 C_3$. The crossover frequency for the maximum phase margin is shown in (9), at the bottom of the page.

Finally for ω_c to be the crossover frequency it should satisfy (10), shown at the bottom of the page.

As in the third-order loop the maximum phase margin is not a function of the absolute values of the R's and C's and is only a function of their ratios (C_2/C_1, C_3/C_1, and R_3/R_1). The loop filter design recipe for the fourth-order loop is modified as follows.

1) Find K_{vco} from the VCO simulation.
2) Choose a desired phase margin and find C_2/C_1, C_3/C_1, and τ_2/τ from (8) and (9).
3) Choose the loop bandwidth and find τ from (9).
4) Select C_1 and Ip such that they satisfy (10).
5) Calculate the noise contribution of R_1 and R_2.If their noise contribution is negligible the design is complete, otherwise go back to step four and increase C_1.

Notice that in a fourth-order loop there are two degrees of freedom in choosing C_2/C_1, C_3/C_1, and τ_2/τ to achieve a desired phase margin. Therefore, the suppression of the spurious sidebands can be improved without reducing the phase margin or the loop bandwidth.

In our system the maximum VCO gain constant is 500 MHz/V. With this VCO gain, and loop filter values of $R_1 = 47$ kΩ, $C_1 = 30$ pF, $C_2 = 3.3$ pF, $R_3 = 8$ kΩ, $C_3 = 2$ pF, and $I_p = 50$ μA, the crossover frequency is about 280 kHz with a 46° phase margin. The calculated contribution to VCO phase noise at 10 MHz offset frequency is -137 dBc/Hz, which is negligible compared to the intrinsic noise of the VCO.

V. Measurement Results

The frequency synthesizer is designed in a 0.24-μm CMOS technology. Fig. 8 shows the die micrograph of the synthesizer with an area of 1 mm $\times$1.6 mm, including pads.

$$\omega_c = \frac{1}{\tau}\sqrt{\frac{1}{2}\left(\frac{2B + AB + A - A^2}{B(B-A)} + \sqrt{\left(\frac{2B + AB + A - A^2}{B(B-A)}\right)^2 - \frac{4(1-A)}{B(B-A)}}\right)}. \tag{9}$$

$$\frac{I_p}{2\pi}\frac{K_{\text{vco}}}{N}\sqrt{\frac{1 + (\tau\omega_c)^2}{(A\tau\omega_c)^2 + (1 - B(\tau\omega_c)^2)^2}} = C_1\left(1 + \frac{C_2}{C_1} + \frac{C_3}{C_1}\right)\omega_c^2. \tag{10}$$

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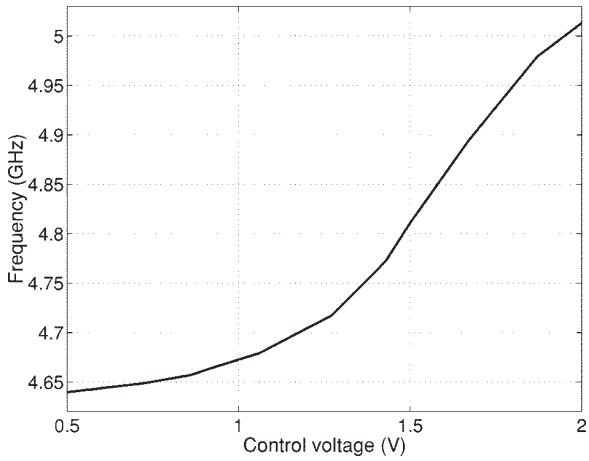

Fig. 9. VCO tuning range.

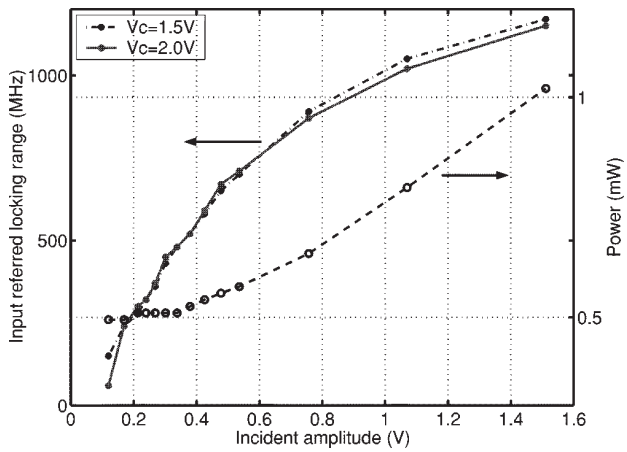

Fig. 10. ILFD locking range and power consumption as a function of incident amplitude.

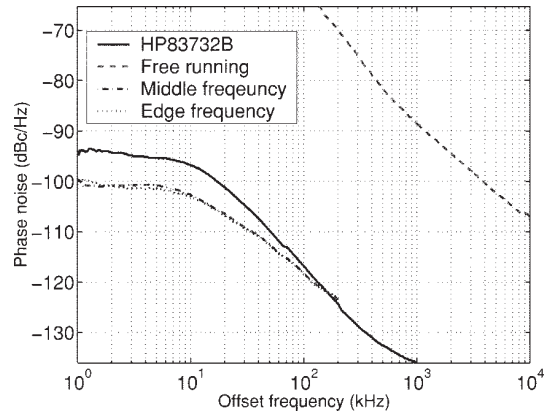

Fig. 11. ILFD phase noise measurements.

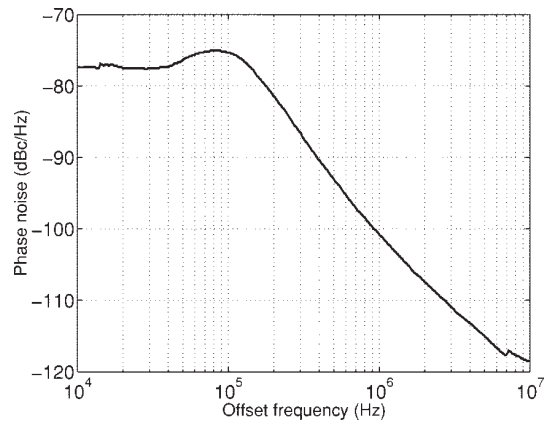

Fig. 12. Phase noise of the synthesizer output signal.

TABLE II
ILFD PERFORMANCE SUMMARY

Output frequency tuning	110MHz ≈ 5%
Input locking range	600MHz ≈ 12% @ 0.55mW
	1000MHz ≈ 20% @ 0.8mW
Technology	0.24μm CMOS
Die area	0.186mm^2
Flip–flop based divider (for comparison)	
0.24μm CMOS	5mW @ 5GHz
0.1μm CMOS [8]	2.6mW @ 5GHz

The analog blocks (VCO, ILFD, and prescaler) are supplied by 1.5 V while the digital portions of the synthesizer are supplied by 2 V. The reason for this choice of supplies is to achieve a larger tuning range for the VCO. The accumulation mode MOS capacitors in this technology have a flatband voltage (V_{FB}) around zero volts. Thus to get the full range of capacitor variation the control voltage should exceed the VCO supply to produce a net negative voltage across the varactors in Fig. 3. To eliminate a need for multiple supplies the VCO can be biased with a PMOS current source, and by connecting the sources of M1 and M2 to ground. More than 500 MHz (10% of the center frequency) of VCO tuning range is achieved for a 1.5-V control voltage variation (Fig. 9).

The free-running oscillation frequency of the ILFD changes more than 110 MHz (≈5% of the center frequency) for a 1.5-V control voltage variation.

Fig. 10 shows the locking range of the ILFD as a function of the incident amplitude for two different control voltages. As expected, changing the control voltage only changes the operation frequencies and not the locking range. The ILFD's average power consumption is also shown on the same figure. Increasing the incident amplitude increases the locking range and the average power consumption. The average power at 1-V incident amplitude is less than 0.8 mW while the locking range exceeds 1000 MHz (≈20% of the center frequency).

The ILFD phase noise measurement results are shown in Fig. 11. The solid line shows the phase noise of the HP83732B signal generator used as the incident signal. The dashed line is the phase noise of the free–running ILFD. The two other curves are the phase noise of the ILFD when locked to two different incident frequencies. The curve marked as *middle frequency* is measured when the incident frequency is in the middle of the locking range and the *edge frequency* curve is measured at the lower edge of the locking range. At low offset frequencies the output of the frequency divider follows the phase noise of the incident signal and is 6 dB lower due to the divide-by-two operation. However, at larger offset frequencies the added noise from the divider itself, the external amplifier, and measurement tools reduces the 6 dB difference between the incident and

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TABLE III
MEASURED SYNTHESIZER PERFORMANCE

Synthesizer performance	
Synthesized frequencies	4.840–4.994GHz
Reference frequency	11MHz
LO spacing	22MHz
Number of channels	8
Spur @ f_{ref}	≤ -45dBc
Spur @ $2 \times f_{ref}$	≤ -54dBc
Phase noise	-101dBc/Hz @ 1MHz
Loop bandwidth	280kHz
Power dissipation	
VCO	3.0mW
ILFD	0.8mW
Prescaler	19mW
Total	25mW
Supply voltage	1.5V (analog)
	2.0V (digital)
Implementation	
Die area	1.6mm^2
Technology	0.24μm CMOS

output phase noise. The ILFD phase noise measurements for offset frequencies higher than 200 kHz are not accurate due to the dominance of noise from the external amplifier.

The spurious tones at 11-MHz offset frequency from the center frequency are more than 45 dB below the carrier. The spurs at the 22-MHz offset frequency are at -54 dBc. Since the LO spacing is twice the reference frequency, the spurs at 11-MHz offset frequency fall at the edge of each channel and are less critical than the 22-MHz spurs which are located at the center of adjacent channels. With the -54 dBc spurs at 22 MHz offset frequency, an undesired adjacent channel may be 44 dB stronger than the desired channel for a minimum 10 dB signal-to-interference ratio.

Phase noise measurements of the complete synthesizer output signal are shown in Fig. 12. The phase noise at small offset frequencies is mainly determined by the phase noise of the reference signal. The phase noise measured at offset frequencies beyond the PLL bandwidth is the inherent VCO phase noise. The phase noise at 1-MHz offset frequency is measured to be -101 dBc/Hz. The phase noise at 22 MHz offset frequency is extrapolated to be -127.5 dBc/Hz. Therefore the signal in the adjacent channel can be 43 dB stronger than that of the desired channel for a 10 dB signal–to–interference ratio.

VI. CONCLUSION

In this work we demonstrate the design of a fully integrated, 5-GHz CMOS frequency synthesizer designed for a U-NII band WLAN system. The tracking injection-locked frequency divider used as the first divider in the PLL feedback loop reduces the power consumption considerably without limiting the performance of the PLL. Table II summarizes the performance of the ILFD. The power consumption of two flip-flop based frequency dividers at 5 GHz are also listed for comparison purposes. In a 0.24-μm CMOS technology a simulated SCL flip-flop based frequency divider loaded with the same capacitance as in the ILFD consumes almost an order of magnitude more power than the ILFD with a 600-MHz locking range. The measurement results of a fast flip-flop based divider in an advanced 0.1-μm CMOS technology show a power consumption of 2.6 mW at 5 GHz [8] which is more than four times the power of the ILFD with a 600 MHz locking range.

Table III summarizes the performance of the synthesizer. The spurious sidebands at offset frequencies of twice the reference signal are more than 54 dB below the carrier. The spurs are mainly due to charge injection from the U and D signals to the loop, and can be reduced significantly by using a cascode structure for transistors M1–M4 (Fig. 6). Better matching between the up and down current sources also improves the sideband spurs. Of the 25-mW total power consumption, less than 3.8 mW is consumed by the VCO and ILFD combined. This low power consumption is achieved by the optimized design of the spiral inductors in the VCO and ILFD. The prescaler operates at 2.5 GHz and consumes 19 mW, of which about 40% is consumed in the first 2/3 dual modulus divider. Therefore the ILFD, which takes advantage of narrowband resonators, consumes an order of magnitude less power than the first 2/3 dual modulus divider, while operating at twice the frequency.

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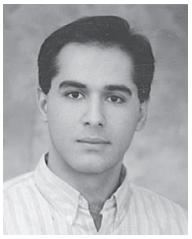

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