

Advanced Silicon IC Interconnect Technology and Design: Present Trends and RF Wireless Implications

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Abstract—Back-end-of-the-line (BEOL) trends in silicon integrated circuits (IC's) include fully planarized interconnect structures with six levels of nonlocal wiring, copper metallization for improved resistance and electromigration, dual damascene patterning for improved line definition and lower BEOL manufacturing cost, and low dielectric constant interlevel dielectrics for reduced line and coupling capacitance. Advanced IC design complexity is being alleviated by the use of intellectual property (IP) cores or macrocells, particularly for advanced application-specific IC's and system-on-a-chip (SOC) implementations. Virtual Design Environment software, developed for distributed design of advanced printed circuit board, will expand to the chip level as SOC designs incorporate IP cores and involve increasingly complex interconnect wiring design. These trends are summarized and synergistic front-end developments discussed and implications for RF wireless technologies are presented. A timetable for such technology and design trends is projected based upon the 1997 National Technology Roadmap for Semiconductors.

Index Terms—Interconnect technology, Virtual Design Environment; wireless technology projections.

I. INTRODUCTION

WIRELESS communications technology that is highly leveraged to, and compatible with, mainstream silicon (Si) complimentary metal-oxide-semiconductor (CMOS) integrated circuits (IC's) will have a significant cost advantage compared to competing technologies and continue to benefit from accelerated technology performance enhancements driven by logic and high-volume application-specific IC's (ASIC's). In the past decade, significant developments have taken place in Si IC back-end-of-the-line (BEOL) technology that have been/are being/will soon be incorporated into mainstream IC products. These developments enhance monolithically integrated Si radio-frequency (RF) circuits, enable on-chip embedded wireless communications, and enhance prospects for system-on-a-chip (SOC) implementations.

The BEOL technology advances are mainly fourfold, including the following:

- 1) chemical-mechanical planarization (CMP), which enables five-eight levels of on-chip metallization with high manufacturing yield;

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- 2) copper metallization for lines and vias to replace aluminum lines and tungsten (W) vias for improved electrical resistance and electromigration capability;
- 3) dual damascene (DD) patterning to replace metal reactive ion etching (RIE) and dielectric gap fill to provide improved line definition and lower BEOL manufacturing cost;
- 4) low dielectric constant (low- k) interlevel dielectrics (ILD's) to replace SiO₂ for lower line and coupling capacitance.

CMP has been well established in IC manufacturing in the past five years, although the fundamental principles of this most rapidly growing IC unit process are not well established. Copper metallization and DD patterning are being introduced at this time in IC products and will clearly be fully incorporated in microprocessors, ASIC's and high-performance SOC's in the next five years. Low- k ILD's, with CMP, copper metallization, and DD patterning, are still in the research and advanced development stage; incorporation in initial products is anticipated in a few years with dominant incorporation in advanced microprocessors, ASIC's and SOC's in the next decade.

An unrelated development, but very synergistic for embedded RF wireless technologies, is occurring in ASIC design with fabrication in Si foundries. The increased IC manufacturing capabilities driven by continued decrease in MFS, increase in Si wafer diameter, and increase in chip size continue to overwhelm developments in design tools; clearly an IC design crises exists. An industry response, built upon the success of conventional gate arrays and standard cell designs, has been design reuse of fully functional proprietary macrocells or intellectual property (IP) cores. Examples of such cores are embedded microprocessors, digital signal processors (DSP's), cache memory, and embedded controllers. In present leading-edge IC design, floor planning of major building blocks is a critical initial step, whether the design is full-custom or involves design reuse with IP cores. Such IP core-based designs are expected to be common in the future.

Recently, Virtual Design Environment (VDE) software has been developed for distributed design of complex printed circuit boards (PCB's). A key to the VDE software is the producibility module, which evaluates alternative implementations using a vendor database. While IC design, both digitally based and RF analog-based, has been performance and/or manufacturing-cost driven, the anticipated trends toward de-

sign reuse of IP cores with an interconnection-dominated (both cost and performance) IC leads to the need for similar VDE software, modified to incorporate interconnect performance models. This paper summarizes Si BEOL trends, namely CMP, copper metallization, DD patterning, and low- k ILD's, briefly summarizes important (but more widely followed by the RF community) synergistic front-end developments (reduced MFS driven by lithography, SiGe device technology that is compatible with Si CMOS, and high- k materials for both storage capacitors and metal-oxide-semiconductor (MOS) gates), and presents a design reuse trend perspective that is considered an important enabler for embedded wireless capability and full SOC implementations. This paper concludes with a timetable for these interconnect technology and design trends based upon the 1997 National Technology Roadmap for Semiconductors (NTRS).

II. SILICON IC BEOL TECHNOLOGY TRENDS

The four main BEOL innovation that affect interconnect-limited Si IC's are: 1) CMP; 2) copper metallization; 3) DD patterning; and 4) low- k ILD's. All are the result of intense research and development efforts to reduce the impact of on-chip interconnection on both electrical performance and yield/manufacturing cost as the IC minimum feature size (MFS) has reduced from 750 to 180 nm in the past decade, with 100-nm technology a current research priority. Even with full implementation of these four innovations within the next decade, on-chip interconnection will remain a dominant issue in high-performance microprocessors, ASIC's, and SOC's [1, ch. on Interconnects].

Global planarization using CMP was the first of these innovations, developed by IBM and used in IC products first by IBM, Intel, and Micron in the early 1990's; currently all major IC manufacturers use CMP for microprocessors and ASIC's, where four-six levels of metallization are required to achieve minimum chip area [2], [3]. The planarization provided by CMP allows an almost unlimited stacking of metallization level in IC's, constrained only by real-estate requirements for conducting vias for interlevel interconnection (and to the Si devices) and by yield considerations (particularly with the current technology approach of sputtered Al lines or trenches with chemical vapor deposited (CVD) W vias). CMP has been the most rapidly growing IC unit process in the past five years, with approximately a 30% compound annual growth rate (CAGR) for equipment and consumables (mainly slurries and pads).

Copper metallization has been actively pursued in many research laboratories for over a decade, as improved electrical conductivity and electromigration capability can be achieved [4]–[7]. The IBM announcement in September 1997 that copper will be used in the next generation of advanced IC chips (with such chips presently going into products) has intensified such efforts at major IC companies. The IBM six-level copper interconnect capability (with oxide ILD's and W local interconnects) has superior electrical performance (clock speed in comparably designed reduced instruction set computer (RISC) processors and improved electromigration

capability) and is claimed to result in a higher yield, lower cost manufacturing process. The latter feature, if demonstrated by other manufacturers, will result in widespread implementation of copper metallization even where the performance advantages are not needed (similar to the increasing use of CMP in Si IC manufacturing plants with only three levels of metallization).

With copper metallization and oxide ILD's, diffusion barriers (and adhesion promoters) are necessary to prevent copper penetration into SiO₂; copper is known to diffuse rapidly under the high electric-field strengths within the ILD's (~ 1 MV/cm) and to decrease minority-carrier lifetime appreciably in Si. TaN, Ta, and TiN are currently the liners of choice, deposited along with a seed layer of Cu by either physical vapor deposition (PVD), i.e., sputtering, or by CVD. Following the PVD or CVD deposition of liner and seed, Cu is electroplated to the final dimensions. On-chip electroplating has not been previously used in Si IC manufacturing, but research and development efforts leveraged to prior developments in first-level packaging have indicated very promising results [8], [9]. The equipment and consumable suppliers have expanded earlier development programs and additional companies are introducing first-generation equipment in preparation of the next expansion of IC manufacturing facilities (similar to the CMP expansion in the mid 1990's).

Incorporation of copper for IC metallization requires a new patterning strategy. In conventional IC's, patterning is achieved by RIE of aluminum lines, followed by deposition of an ILD, patterning of the ILD for vias, CVD of W (or, in less demanding applications, PVD of aluminum), and CMP of W to result in a planarized dielectric surface with W-vias. After PVD of Al for the next interconnect level, the process is repeated. Unfortunately (in the opinion of many), RIE of copper has not been possible without elevated processing temperature, which requires a hard mask and increasing process complexity. As a result, the process described for the W vias has been incorporated for both lines and vias, which is a damascene (or inlaid metal) process.

For further reduction in process complexity, the DD process has been developed in which both lines and vias are formed in the same process (requires two lithography steps, but one copper-deposition and one CMP step). While the damascene process is another BEOL IC manufacturing process change, development of a high-yield DD process provides reduced manufacturing cost and improved line width control, particularly with the different interconnect dimensions incorporated for six or more metallization levels. In fact, DD patterning, has such inherent advantages that various groups committed to aluminum metallization are investigating Al-DD patterning with Al vias deposited by either CVD or by PVD followed by a high-temperature high-pressure "Al-flow" process.

Various DD patterning strategies have been investigated, four well-developed alternatives for oxide ILD's with two additional processes developed for low- k ILD's using clustered hard masks [10]–[12]. The alternatives, summarized in Fig. 1, involve tradeoffs in various unit process steps, particularly lithography and ILD etch. While all have relative advantages, the via-first deep etch and buried hard mask have some key

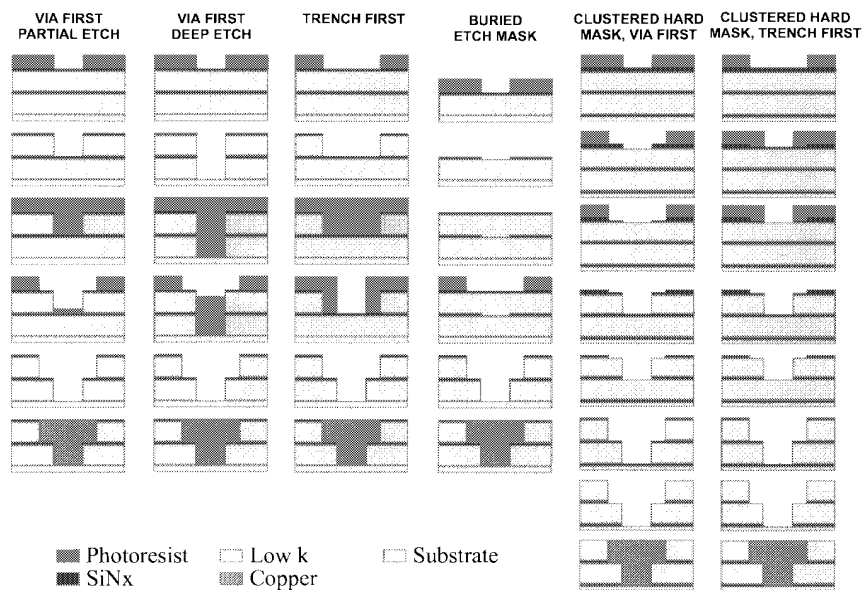


Fig. 1. DD patterning strategies for copper/low- k dielectrics. The first four are conventional approaches developed for oxide dielectrics, while the two clustered hard mask techniques have been recently proposed with polymer dielectrics (after [12]).

advantages among the four traditional techniques and the use of clustered hard masks (or some modification) considered to be advantageous with polymer ILD's [12].

Since DD patterning is being introduced with copper metalization, the timetable for full implementation is similar. While Al DD is being pursued, the required use of relatively high temperatures and/or other unique processing is not considered desirable, except in niche applications (at least by this author). The requirements for a nonoxide ILD (i.e., low- k) are significantly different if used for RIE-patterned metal where gap fill is important or if used in DD patterning where CMP process ability is critical. The use of low- k materials with RIE-patterned Al clearly has advantages in some applications. The apparent process requirements of Al DD will prevent the use of many low- k material alternatives.

The fourth BEOL innovation is the use of low- k materials for ILD's to reduce propagation delays and reduce electrostatic coupling between lines (adjacent lines on the same interconnect level and parallel lines on adjacent levels in close proximity). While the performance advantages of low- k are greater than for Cu in many designs and less process changes are involved in incorporating low- k materials, the incorporation of low- k will mostly follow manufacturing introduction of copper. One reason is the large number of choices of low- k material [13]–[15] and the desire to have a material which can be used for at least three generations of technology; a second reason is the difference in process requirements for the ILD with RIE-patterned metal and DD patterning. With copper clearly going into products, with fairly well accepted Cu performance advantages, and with increasingly accepted Cu with DD manufacturing cost advantages, the industry is driving harder toward low- k with Cu as a near-term development issue (e.g., the SEMATECH Cu-low k development effort initiated in 1997). Due to the number of low- k alternatives and the need to establish a manufacturing base with Cu and DD,

the incorporation of low- k ILD's will not be introduced in manufacturing for another few years, with widespread use with Cu in products in about five years.

III. SYNERGISTIC Si IC FRONT-END TECHNOLOGY DEVELOPMENTS

While the BEOL developments described in Section II have great performance leverage for RF wireless products, continued advancements in front-end-of-the-line (FEOL) technologies for Si IC's need to be considered. These FEOL advancements include continued reduction in MFS, continued growth of maximum chip area, development of CMOS-compatible SiGe heterojunction bipolar transistor (HBT) technology, and high- k dielectrics for MOS field-effect transistor (MOSFET) gates and dynamic random-access memory (DRAM) storage capacitors.

The continued decrease in lower cost per electronic function for three decades has been driven by continued reduction in MFS and the more modest growth of maximum chip area (combined to allow batch processing of increasing complex IC's with an increasing number of transistors). Continued developments in lithography and pattern transfer have resulted in optical stepper lithography achieving 250-nm MFS in widespread manufacturing today, with 180-nm MFS in advanced plants and with 130-nm MFS IC's being shipped in small quantities. Clearly, the Si IC industry will make optical lithography work to the 130-nm technology node, although the choice at 100 nm and below is unclear. While the transition from 200-mm-diameter wafers to 300 mm has been delayed by the short-term reduction in demand, larger chips will clearly be possible with the transition to 300-mm wafers that will commence during the next increase in IC product demand. More on-chip capability will permit increasingly complex SOC implementations and offer increased leverage for process-compatible RF wireless implementations.

The incorporation of SiGe HBT technology into high-volume CMOS IC manufacturing has been demonstrated by IBM [16]–[18]. While heteroepitaxial layer growth and additional processing steps are required, manufacturing in a state-of-the-art 200-mm-diameter CMOS-compatible IC line has been demonstrated and is ongoing. The performance advantages of these HBT's compared to digital CMOS-compatible MOSFET's is significant and can result in lower cost RF wireless building blocks. The possibility of monolithically integrable IP cores of high-performance digital CMOS with high-frequency analog circuits with SiGe HBT's is extremely attractive in performance, cost, and time-to-market.

Innovative high- k thin-film dielectrics are being developed for scaled-MOSFET gates and for DRAM storage capacitors [19], [20]. While these ferroelectric materials (e.g., titanates) require high deposition temperatures (FEOL compatible only), deposition at lower BEOL-compatible temperatures can provide a dielectric constant (~ 30), which can be useful in RF filtering applications and on-chip power decoupling. The loss tangent of these polycrystalline films are reasonably low (<0.005) through 40 GHz.

IV. Si IC DESIGN REUSE TRENDS AND VDE SOFTWARE

Si IC fabrication innovations as described in Sections II and III have advanced at a faster rate than enhancements in design tools for more than a decade, resulting in a design and verification crises for leading-edge Si IC's [21], [22]. The largest delay in bringing new IC's to market has been, and will continue to be for the foreseeable future, the design and verification process, particularly for mixed-signal designs, SOC implementations and densely packed ASIC's. Design reuse of complex macrocells (also called IP cores) is a growing response to the design and verification process, in which previously developed and proven sub-chip designs are reused in new IC's. This concept extends the well-developed use of in-house design libraries, but the extension to interconnect-limited designs using complex macrocells as building blocks is a significant extension both for the IC designer and, with widespread implementation, the industry as well.

Since commercial IC foundries have reduced the technological capability gap enjoyed by vertically integrated industrial leaders, all IC designers have access to near state-of-the-art facilities (within one to two generations). Licensing of fully verified complex macrocells can reduce the time-to-market appreciably, as well as reducing new-product risk. Such IP cores can be either "hard" (fully verified in Si for a given foundry implementation and less transferable) or "soft" (verified at the logic design stage); for mixed-signal and RF wireless applications, hard IP cores are required. The advantage of such a design approach will, in the opinion of this author, lead to more common fabrication design rules with leading-edge IC foundries and offset the strong IC designer mind set of designing from scratch. The time-to-market advantage of using hard IP cores will become overwhelming unless an unexpected breakthrough in design and verification tools is forthcoming.

In the anticipated design and manufacturing environment, software tools to accommodate the projected paradigm are

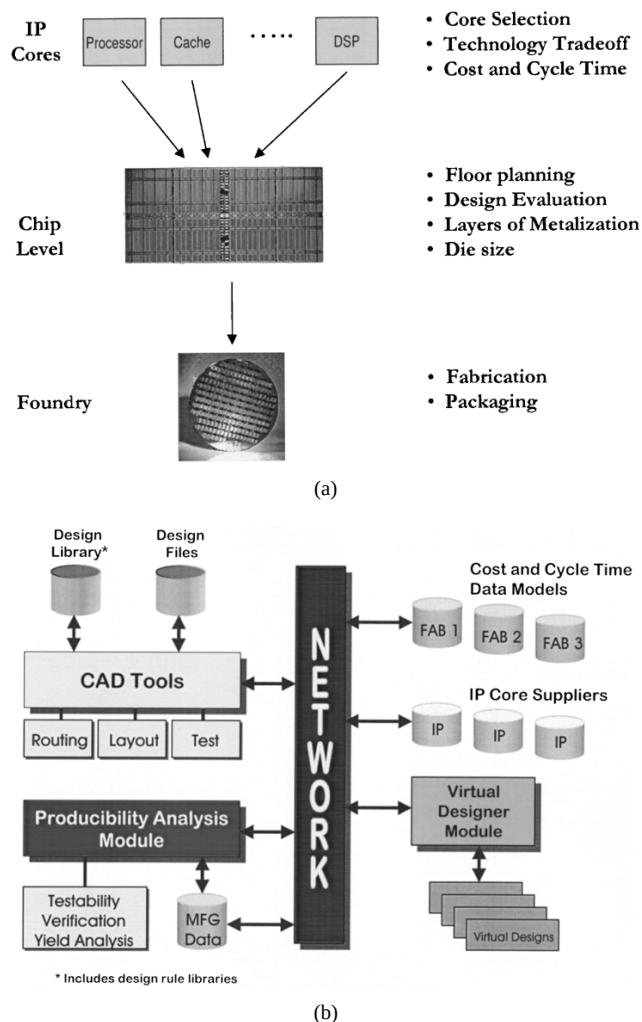


Fig. 2. VDE envisioned for IP core-based IC design and manufacturing. The approach is modeled after a technique developed for PCB design and manufacturing as described in [23] and [24]. (a) VDE-based design and manufacturing process. (b) Highlights of IP core-based design and manufacturing process.

needed. This anticipated IC design environment is similar to the PCB design environment, where selection of IP cores is analogous to selection of packaged IC's and where chip design becomes analogous to PCB design. For example, an ASIC design will increasingly focus on interconnection, personalized "glue" circuits, and some specialized high-value-added circuits with appreciable reuse of a prior-verified basic building blocks. A key component in such a software tool set is the VDE as developed for PCB design [23], [24].

The VDE envisioned is depicted in Fig. 2(a) and extends an ASIC design company with in-house design libraries and computer-aided design (CAD) tools coupled to alternative Si IC fabrication foundries; the full IP core-based design and manufacturing process is shown in Fig. 2(b). A key aspect of the VDE is the producibility analysis module (PAM), which incorporates verification software, yield analysis programs and foundry manufacturing data to evaluate alternative designs at the behavioral synthesis level, the logic verification level and the physical verification level. Verification at both the logic and physical levels are particularly challenging for mixed-

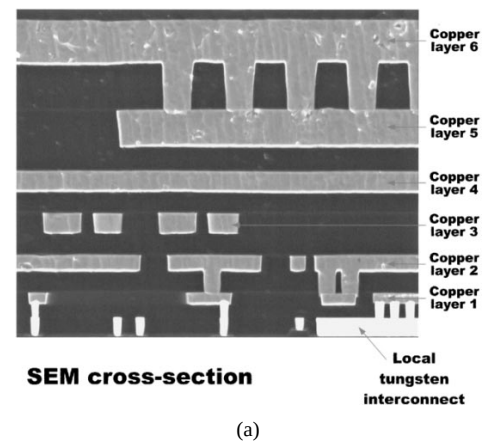
signal and SOC implementations in general and for complex embedded RF wireless circuits in particular. With a well-developed PAM, proposed designs can be “tuned” to properly account for differences in foundry capabilities or “generalized” to account for additional nontechnical issues such as cost or cycle time; cycle time is considered to be critical in opening new markets.

Knowledge-based models characterizing cost and cycle time are needed for each IC foundry and IP core supplier, with properly specified databases. Once developed, intelligent software agents (ISA’s) could access the models over the network and activate calculation of key parameters. These results would be returned to each feasible IC foundry and IP core supplier by the ISA to the virtual designer module (VDM) for use in evaluation and in guiding design improvement. The VDM incorporates an evolutionary programming technology to search for improved designs for the emulated IC using an genetic algorithm approach. The resultant set of viable virtual designs can then be considered. While this process is under active development for PCB designs, the PAM must be fully developed in a form suitable for IC’s; the verification tool set is particularly critical for interconnect-limited designs in general and for RF wireless interconnect-limited designs in particular.

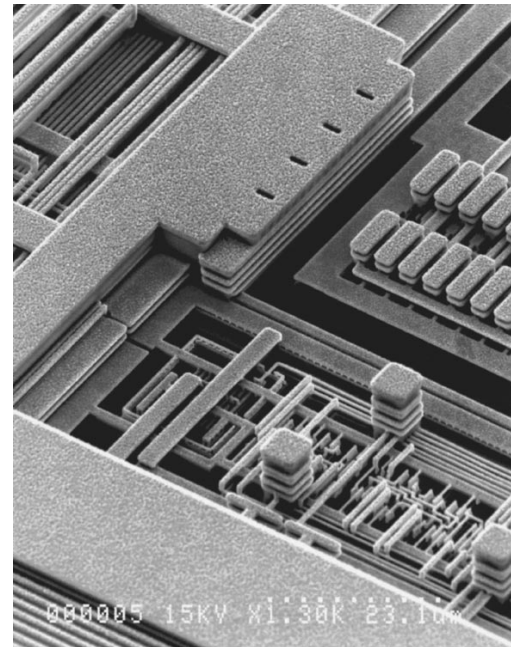
V. RF WIRELESS TECHNOLOGY IMPLICATIONS

The underlying assumption in relating these Si IC technology and design trends to RF wireless technologies is that Si CMOS-compatible IC’s will continue to penetrate RF wireless applications wherever CMOS-compatible performance is adequate. The rapid enhancements in Si IC technology, such as described earlier, and the decreasing cost per electronic function are overriding factors. The BEOL and FEOL technology advancements combined with trends in design reuse of macrocells and IP cores are sufficient enablers in mixed-signal ASIC’s and SOC implementations for RF wireless applications that CMOS-compatible Si IC implementations will penetrate at an increasing rate, augmented mostly by copper metallization with low- k ILD’s, SiGe high-frequency HBT’s, RF-compatible IP cores, and improvements in interconnect-limited design tools needed for high-clock-rate logic IC’s.

Consider the six-level copper interconnect structure (with one level of local W interconnect and W vias for device contact) patterned with single-level damascene patterning at the first copper level ($M1$ level) and DD patterning for $M2$ – $M6$, as depicted in Fig. 3. The “inverse scaling” at the upper levels is typical and easily achieved with DD patterning. While the typical digital IC process generally is constrained to copper thickness $\sim 1.5 \mu\text{m}$ for $M5$ and $M6$, thicker lines are feasible. Planar inductors with upper level wiring will have higher Q than lower level conventional wiring due to the higher conductivity of Cu (compared to Al), the thicker upper level metal lines, and the reduced coupling to the Si. Torroidal-like inductors using multiple layers of interconnect are also feasible. While the IBM technology depicted using conventional SiO_2 as the ILD throughout, the eventual incorporation of low- k materials will reduced



(a)



(b)

Fig. 3. Six-level damascene patterned interconnect structure as reported by IBM (from IBM web page). Note that the local interconnect level and vias to the device contacts are tungsten, the first copper level ($M1$) is single-damascene patterned and levels $M2$ – $M6$ are DD patterned. (a) Focused ion beam–scanning electron microscopy (FIB–SEM) cross section. (b) Three-dimensional perspective after etching of oxide dielectric.

parasitic electrostatic coupling and improve RF inductor performance further (increased self-resonant frequency). Higher Q inductors are significant performance enhancers in many monolithic RF circuits [25]–[29].

The development of SiGe devices with high f_t and f_{max} in a CMOS-compatible process is an additional significant advance for low-cost high-performance RF wireless technology. While the required heteroepitaxy technology and HBT devices will probably not be used in mainstream logic and microprocessor circuits in the foreseeable future (i.e., as long as CMOS scaling remains economically viable), the implications in telecommunication applications in general and in RF wireless applications specifically are significant. Clearly, this technology is fully compatible with SOC implementations with an array of RF wireless circuits using SiGe HBT’s [30], [31].

Design reuse trends which have occurred with the growing crises in Si IC design and verification will enable further embedded RF wireless implementations and mixed-signal SOC's. Either Si MOSFET or SiGe HBT devices can be incorporated into fully functional RF circuits and macrocells in a format compatible with Si IC foundry implementations. Amplifiers, mixers, RF switches, and transceivers can be developed as IP cores, similar to in-house design libraries. While designers may relish the opportunity to initiate a design with bare Si (or GaAs or even InP), the business case for interconnect-constrained design using macrocells and IP cores will become increasingly compelling.

The design tools needed in such a paradigm will focus on routing and interconnect-based simulation. The limits to increasing integration will shift from MFS to interconnect-related issues of delay, clock skew, and coupling (electrostatic and electromagnetic). Design tools incorporating electromagnetic coupling and interference will be required in signal routing design tools [32]–[34]. The RF/microwave engineer expertise will be needed even in logic circuits with high clock rates.

VI. NTRS-BASED TIMETABLE PROJECTIONS

The Semiconductor Industry Association (SIA) has been coordinating industry-wide projections of semiconductor technology and classifying issues to guide research and development programs. On-chip interconnect and design and test are two of the paramount issues, which have led to the newly announced Focus Center Research Programs (FCRP's) sponsored by the Semiconductor Research Corporation (SRC). These recognized critical areas clearly impact the RF wireless technology area. In this section, we project a timetable for some of these developments based upon the SIA NTRS [1], [22, ch. on Design and Test].

A. Interconnect

The Interconnect section of the roadmap indicates the following five difficult challenges before 2006 with MFS of 100 nm and above:

- 1) chip reliability issues with copper, damascene patterning, and low- k ILD's;
- 2) process integration issues with Cu/low- k and Al/low- k , particularly low cost, high yield, and acceptable reliability;
- 3) barriers that solve integrations issues with Cu/low- k ;
- 4) dimensional control of feature sizes and film thickness to control interconnect electrical impact (and the required metrology);
- 5) low- k materials with the electrical, mechanical, and thermal requirements for high-performance IC's.

While the results reported over the last year indicate that there are no show stoppers for DD-patterned copper interconnects with oxide ILD's at the 130-nm technology node, the low- k ILD alternatives to date have various deficiencies. This author believes that low- k selection will continue to be the only gating item in this part of the roadmap, with

viable alternatives having dielectric constants ~ 2.6 becoming available in the near future; introduction of low- k with Cu will be delayed by a combination of the need to gather manufacturing experience with copper and DD patterning and the semiconductor industry desire for a dielectric constant ~ 2.0 .

The five difficult challenges delineated for beyond 2006, with MFS below 100 nm include the following:

- 1) dimensional control issues, including metrology, *in situ* process control, and CAD techniques;
- 2) aspect ratios for metal fill and ILD etch, particularly with DD patterning;
- 3) barriers which need to be thin to fully utilize Cu and low- k ILDs;
- 4) FEOL-benign processes, that is BEOL process which do not damage scaled devices (e.g., soft etch and clean);
- 5) solutions after Cu/low- k , which are unspecified and uncertain.

This author considers metrology and barriers to be the major issues in Cu/low- k interconnect structures at MFS < 100 nm. Interconnect solutions beyond Cu/low- k are beyond the scope of this paper, but those indicated in the NTRS are intra-chip compatible optical interconnects and high-temperature (400 K) superconductors.

In summary, the NTRS limiters to Cu/low- k of most significance in the context of RF wireless technology for the foreseeable future are low- k ILD materials compatible with DD patterned copper and barriers for Cu that can be scaled to < 100 nm MFS. Recent work indicates that certain polymer low- k ILD's might not need conventional liners with Cu, although additional research is clearly needed [35].

B. Design and Test

In the design and test period, the five key challenges before 2006 include the following:

- 1) design environment and standards, design data models, and access supporting incremental processing;
- 2) more accurate interconnect and power models for synthesis/system-level design;
- 3) constraint-dominated interconnect synthesis as gigascale designs become dominated by interconnect;
- 4) verification becoming the dominant effort in design, including timing verification, system-level verification, and core-based designs;
- 5) elimination of negative yield impact due to tester limits.

Clearly, the role of interconnect-limited design is recognized as an Si IC design issue, even without RF implementations, which require additional interconnect modeling.

The five difficult challenges after 2006 that were highlighted in the design and test period are as follows:

- 1) dramatically improved design productivity to deal with increasing complexity, particularly design and test times;
- 2) power management at all levels;
- 3) architectural and other design methods to overcome fatal interconnect performance problems, i.e., nothing viable currently on the horizon after Cu/low- k ;

- 4) signal integrity and IC reliability, including various issues of noise, interconnect, and reliability;
- 5) automated synthesis/layout of analog/mixed signal designs.

The concern with design productivity and design cycle time are clearly indicated with CAGR of design productivity aimed for 41% in 2006 compared to 21% in 1997 and the design cycle time (currently measured in months) reduced by 45% in 2006. Design reuse for SOC's is anticipated to increase from 40% presently to 70% in 2006.

RF Wireless Perspective

The NTRS roadmap indicates rapid progress toward incorporating high-performance RF wireless circuits in Si IC's for SOC's is almost assured. The potential show stoppers and/or gating items controlling RF wireless implications are as follows.

- 1) Low- k ILD selection; while dielectric constants ~ 2.6 have a significant payoff in RF applications, the semiconductor industry push for $k \sim 2.0$ may inhibit going to an intermediate material for only one or two generations (unless the technology is scalable as with zerogels or some polymers); liners will only be an issue at <100 nm MFS.
- 2) Acceptance of and second-source availability for SiGe HBT technology compatible with Si CMOS; while IBM has clearly demonstrated the capabilities, alternative foundries need to be developed which requires a significant product base.
- 3) Acceptance of hard IP cores that can be licensed from design houses or foundries and be widely accessible; this difference in designer mind set will become a business necessity if a design and verification breakthrough does not occur.

Based upon the NTRS and the perspective/judgment of this author, the use of hard IP-core macrocells for RF wireless applications will appear in DD-patterned Si IC's with copper metallization in products from vertically integrated companies (e.g., IBM and Motorola) in the next two to three years. Widespread usage of this technology will occur within five years. The use of low- k ILD's with $k \sim 2.6$ may be driven by a growing RF wireless industry, with the low- k restricted to a few levels where RF circuit performance and interconnection are performance drivers. The dominance of SiGe HBT's in RF applications will be established by the wireless market; at a sufficient market size with device performance dominance, Si MOSFET's will be replaced. This timetable is more difficult to predict, at least by this author.

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