

Interconnect Technology and Design Implications for Future ASIC and System-on-a-Chip (SOC) Implementations

Ronald J. Gutmann, Kevin Chan and Robert J. Graves
Electronics Agile Manufacturing Research Institute
Center for Integrated Electronics and Electronic Manufacturing
Rensselaer Polytechnic Institute, Troy, NY, USA

Abstract – Back-end-of-the-line (BEOL) interconnect technology is undergoing a rapid transformation as a result of the projected impact on IC performance at decreasing minimum feature sizes. As a result, design complexity is becoming the gating item in leading edge IC products, leading to increasing design reuse of IC functional building blocks (i.e. macrocells and intellectual property (IP) cores), particularly for advanced application specific ICs (ASICs) and system-on-a-chip (SOC) implementations. Virtual Design Environment (VDE) software developed for complex printed circuit boards will expand to the chip level as SOC implementations (and advanced ASICs) incorporate increasing use of IP cores and increasingly complex wiring designs. IC manufacturing operations will become increasingly involved in providing and licensing IP cores in support of this evolving design methodology.

Index terms: IC interconnect technology, IP cores, virtual design environment, agile manufacturing

INTRODUCTION

In the past decade, significant developments have taken place in IC back-end-of-the-line (BEOL) technology which have been/are being/will soon be incorporated in mainstream products. These technology advances are mainly four-fold: chemical-mechanical planarization (CMP) that enables 6-8 levels of on-chip metallization with high manufacturing yield, copper metallization for lines and vias for improved electrical resistivity and electromigration capability, dual Damascene (DD) patterning for improved line definition and lower BEOL manufacturing cost, and low dielectric constant (low-k) interlevel dielectrics (ILDs) for lower line and coupling capacitance. CMP has become well established in IC manufacturing in the last 4-8 years, although the fundamental principles of this most rapidly growing IC unit process are not well established. Copper metallization and DD patterning are being introduced at this time in IC products and will clearly be fully

incorporated in leading edge microprocessors, ASICs and SOC in the next few years. Low-k ILDs, with CMP, copper metallization and DD patterning, are still in the research and development stage; incorporation in some products will occur in the next few years, with dominant incorporation in IC manufacturing over the next decade. While front-end-of-the-line (FEOL) developments like silicon-on-insulator (SOI), CMOS-compatible silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) and high-k dielectrics for memory cells and power decoupling are also enhancing IC technology capabilities, FEOL impacts are greatest on IP core capabilities and IC real estate requirements; the IC interconnect technology performance limitation and complexity remains (and is enhanced as FEOL capabilities improve).

Virtual Design Environment (VDE) software has been developed for rapid-time-to-market (i.e. agile) implementation of complex printed circuit boards (PCBs). One key to the VDE software is the producibility module, which evaluates alternative implementations using databases on vendor capabilities and design rules for layout and routing. The trends toward increasing reuse of previously designed and verified IP cores or macrocells in new ASICs and SOC implementations establishes a parallel between leading-edge PCB design and IC design in this new environment. Lower cost and rapid time-to-market products will result from more design reuse and long-distance IC interconnect routing that is not performance limiting.

This paper summarizes IC BEOL technology trends, presents a VDE design environment envisioned for IP-core based ASICs and SOC implementations, and discusses the implications of this new interconnect technology and design environment on IC manufacturing needs.

IC BEOL Technology Trends

The four main BEOL innovations affecting interconnect-limited Si ICs are CMP, copper metallization, DD patterning and low-k ILDs. All are the

result of intense research and development efforts to reduce the impact of on-chip interconnection on both electrical performance and yield/manufacturing cost as the IC minimum feature size (MFS) has reduced from 750 nm to 180 nm in the past decade, with 100 nm technology and below a current research priority. Even with full implementation of these four innovations within the next decade, on-chip interconnection will remain a dominant issue in high-performance microprocessors, ASICs and SOCs [1].

Global planarization using CMP was the first of these innovations, developed by IBM and used in IC products first by IBM, Intel and Micron in the early '90s; presently all major IC manufacturers use CMP for microprocessors and ASICs, where 6 to 8 levels of metallization are required to achieve minimum chip area [2-3]. The planarization provided by CMP allows an almost unlimited stacking of metallization level in ICs, constrained only by via real estate requirements (for interlevel interconnection) and by yield considerations.

Copper metallization has been actively pursued in many research laboratories for over a decade, as improved electrical conductivity and electromigration capability can be achieved [4-7]. The IBM announcement in September 1997 that copper will be used in IC manufacturing has intensified such efforts at major IC companies. The IBM six-level copper interconnect capability (with oxide ILDs and tungsten local interconnects) has superior electrical performance (clock speed in comparably designed processors and improved electromigration capability) and is claimed to result in a higher-yield, lower-cost manufacturing process. The latter feature, if demonstrated by other manufacturers, will result in widespread implementation of copper metallization even where the performance advantages are not needed (similar to the increasing use of CMP in Si IC manufacturing).

With copper metallization and oxide ILDs, diffusion barriers (and adhesion promoters) are necessary to prevent copper penetration into SiO_2 ; copper is known to diffuse rapidly under the high electric field strengths within the ILDs ($\sim 1\text{MV/cm}$) and to decrease minority-carrier lifetime appreciably in Si. TaN, Ta and TiN are presently the liners of choice, deposited along with a seed layer of Cu by physical vapor deposition (PVD), ie. sputtering. Following PVD of liner and seed, Cu is electroplated to the final dimensions. On-chip electroplating has not been previously used in Si IC manufacturing, but research and development efforts leveraged to prior developments in first-level packaging have indicated very promising results [8-9].

Incorporation of copper for IC metallization requires a new patterning strategy. In conventional ICs, patterning is achieved by reactive ion etching (RIE) of aluminum lines, followed by deposition of an ILD, patterning of the ILD for vias, CVD of tungsten (or in less demanding applications PVD of aluminum), and CMP of W to result in a planarized dielectric surface with W-vias. Unfortunately (in the opinion of many), RIE of copper has not been possible without elevated processing temperature which requires a hard mask and increasing process complexity. As a result, the process described for the tungsten vias has been incorporated for both lines and vias, that is a DD (or inlaid metal) patterning in which both lines and vias are formed in the same process (requires two lithography steps but one copper-deposition and one CMP step).

While the Damascene process is another BEOL IC manufacturing process change, development of a high-yield DD process provides reduced manufacturing cost and improved line width control, particularly with the different interconnect dimensions incorporated for 6 to 8 (or more) metallization levels. In fact, DD patterning has such inherent advantages that various groups committed to aluminum metallization are investigating Al-DD patterning.

The fourth BEOL innovation is the use of low-k materials for ILDs to reduce propagation delays and reduce electrostatic coupling between lines. While the performance advantages of low-k are greater than for Cu for many ICs and less process changes are involved in incorporating low-k materials, the incorporation of low-k will mostly follow manufacturing introduction of copper. One reason is the large number of choices of low-k material [10-12] and the desire to have a material which can be used for a few generations of technology; a second reason is the difference in process requirements for the ILD with RIE-patterned metal and DD patterning. Copper is going into manufacturing as a result of the well accepted Cu performance advantages and the increasingly accepted Cu with DD manufacturing cost advantages; the industry is driving harder toward low-k with Cu as a near-term development issue (e.g. the SEMATECH Cu-low k development effort). Because of the number of low-k alternatives and the need to establish a manufacturing base with Cu and DD patterning, low-k ILDs will not be introduced in manufacturing for another few years, with widespread use in products in about five years.

A more complete discussion of these issues relative to the RF wireless industry is described elsewhere [13].

Silicon IC fabrication innovations have advanced at a faster rate than enhancements in design tools for more than a decade, resulting in a design and verification crises for leading-edge Si ICs [14-15]. The largest delay in bringing new ICs to market will continue to be the design and verification process, particularly for mixed-signal designs, densely packed ASICs and SOC implementations. Design reuse of complex macrocells or IP cores is a growing response to the design and verification bottleneck, in which previously developed and proven sub-chip designs are reused in new ICs. This concept extends the well-developed use of in-house design libraries, but the extension to interconnect-limited designs using IP cores as building blocks is a significant enhancement both for the IC designer and the industry infrastructure.

Since commercial IC foundries have reduced the technological capability gap enjoyed by vertically-integrated industrial leaders, all IC designers have access to near state-of-the-art facilities (within one to two generations). Licensing of fully-verified complex macrocells can reduce the time-to-market appreciably as well as reducing new-product risk. Such IP cores can be either "hard" (fully verified in Si for a given foundry implementation and less transferable) or "soft" (verified at the behavior synthesis levels); wide implementation will occur if hard IP cores can be widely utilized. The advantage of such a design approach will lead to more common fabrication design rules at leading-edge IC foundries and offset the strong IC designer mind set of full custom design. The time-to-market advantage of using hard IP cores will become overwhelming unless an unexpected breakthrough in design and verification tools is forthcoming.

In the anticipated design and manufacturing environment, enabling software tools to accommodate the projected paradigm are needed. This anticipated IC design environment is similar to the PCB design environment, where selection of IP cores is analogous to selection of packaged ICs and where chip design becomes analogous to PCB design. For example, an ASIC design using IP cores will focus on interconnection personalized "glue" circuits. A key component is a VDE-like software tool set as developed for PCB design [16-17].

The VDE envisioned is depicted in Figure 1A and extends the model of an ASIC design company with in-house design libraries and CAD tools coupled to alternative Si IC fabrication foundries; the full IP core-based design and manufacturing process is shown in

Figure 1B. One key aspect of the VDE is the producibility analysis module (PAM) which incorporates verification software, yield analysis programs and foundry manufacturing data to evaluate alternative designs at the behavioral synthesis level, the logic verification level and the physical verification level. Verification at both the logic and physical levels are particularly challenging for ASICs and SOC implementations. With a well-developed PAM, proposed designs can be "tuned" to properly account for differences in foundry capabilities or "generalized" to account for additional non-technical issues such as cost or cycle time; cycle time is considered to be critical in opening new markets.

Knowledge-based models characterizing cost and cycle time are needed for each IC foundry and IP core supplier, with properly specified databases as parallels to those developed for the VDE at the PCB design level. Once developed, intelligent software agents (ISAs) could access the models over the network and activate calculation of key parameters. These results would be returned to each feasible IC foundry and IP core supplier by the ISA to the Virtual Designer Module (VDM) for use in evolutionary algorithms for evaluation and guiding design improvement. The resultant set of viable virtual designs can then be considered toward reducing the overall design cycle. While this process is under active development for PCB designs, the PAM must be fully developed in a form suitable for ICs; the verification tool set is particularly critical for interconnect-limited designs, particularly in mixed signal ICs. The analogy between the design and manufacturing process for ICs and PCBs is depicted in Figure 2.

IC Manufacturing Implications

The IP-core/design reuse trend underway in the IC industry will evolve at an accelerated pace as a result of the BEOL technology innovations presented. VDE-like software will enable the necessary distributed design capability with alternative manufacturing site selection based upon capabilities and availability. In this section the impact of such a design methodology on the IC manufacturing environment will be projected.

Fortunately, many of the technical requirements needed in IC manufacturing are already being incorporated to achieve high quality products with higher manufacturing yield, reduction in cycle time and enhanced interactions with customers and suppliers. Computer network-based manufacturing support systems are the underlying technology base needed to support quick time-to-market innovative products based upon

IP-core/design reuse technology. These platforms will need to support VDE-like software, but the requirements appear straightforward.

One area of particular need is to reconfigure hard IP core designs for different IC manufacturing capabilities. While such a requirement appears imposing today, the rapid establishment of near-leading edge stand-alone foundries plus the foundry activities introduced by vertically integrated companies will ease the technological barriers. If the design bottleneck for future ICs continues as anticipated, the industry evolution envisioned will strongly favor those that provide the necessary infrastructure first. This trend is already occurring, and we believe that many IC manufacturing facilities will move aggressively in this direction in the next decade. While standardization will become an issue, establishment of a limited number of alternative VDE platforms is a viable option to standardization.

ACKNOWLEDGMENTS

The EAMRI at Rensselaer was established in April of 1994 (DMI9320955) under sponsorship of the National Science Foundation and the Advanced Research Projects Agency as one of three AMRI's designated to provide a focus for Agile Manufacturing research in key US industries. The interconnect technology research has been supported by the New York SEMATECH Center of Excellence and the Center for Advanced Interconnect Science and Technology by the Semiconductor Research Corporation (SRC).

REFERENCES

- [1] Semiconductor Industry Association, *National Technology Roadmap for Semiconductors*, 1997, chapter on Interconnects.
- [2] J.E. Steigerwald, S.P. Murarka and R.J. Gutmann, *Chemical-Mechanical Planarization of Microelectronic Materials*, Wiley Interscience, 1997.
- [3] Chemical-Mechanical Planarization for ULSI Multilevel Interconnection (CMP-MIC), first four annual conference digests, 1996-99.
- [4] D. Edelstein, et al., "Full Copper Wiring in a Sub-0.25 Micron CMOS ULSI Technology", International Electron Devices Meeting, 1997, pp. 773-776.
- [5] C.K. Hu and J.M.E. Harper, "Copper Interconnects and Reliability", *Materials Chemistry and Physics*, Vol. 52, 1998, pp. 5-16.
- [6] S.P. Murarka and R.J. Gutmann, special issue on Copper Metallization for Future VLSI, *Materials Chemistry and Physics*, Vol. 41, 1995, pp. 159-228.
- [7] T.A. Alford, J. Li, J.W. Mayer and S-Q Wang, special issue of Copper-Based Metallization and Interconnects, *Thin Solid Films*, Vol. 262, 1995, pp. 1-242.
- [8] P.C. Andricacos, C. Uzoh, J.O. Dukovic, J. Horkans and H. Deligianni, "Damascene Copper Electroplating for Chip Interconnections", *IBM Journal*, Vol. 42, 1998, pp. 557-574.
- [9] P.C. Andricacos, "Electroplated Copper Wiring on IC Chips", *Interface*, Vol. 7, 1998, pp. 23-35.
- [10] W.W. Lee and P.S. Ho, "Low-Dielectric Constant Materials for ULSI Interlayer Dielectric Applications", *MRS Bulletin*, Vol. 22, 1997, pp. 19-23.
- [11] R.J. Gutmann et al., "Low Dielectric Constant Polymers for On-Chip Interlevel Dielectrics with Copper Metallization", *Materials Research Society Proceedings*, Vol. 381, 1995, pp. 177-195.
- [12] Dielectrics for ULSI Multilevel Interconnection (DUMIC), first four conference proceedings, 1995-98.
- [13] R.J. Gutmann, "Advanced Silicon IC Interconnect Technology and Design: Present Trends and RF Wireless Implications," *IEEE Transactions on Microwave Theory and Techniques*, MTT-47, 1999, to be published.
- [14] P. Jain, J. Turley, V. Agarwal, F. Bond and P. Varhol, *Key Technology and Design Issues*, a series of five articles in *Computer Design*, October 1998, pp. 40-74.
- [15] Semiconductor Industry Association, *National Technology Roadmap for Semiconductors*, 1997, chapter on Design and Test.
- [16] R. Subbu, A.C. Sanderson, C. Hocaoglu and R.J. Graves, "Distributed Virtual Design Environment using Intelligent Agent Architecture", *Proceedings of the Industrial Engineering Research Conference*, May, 1998.
- [17] R. Subbu, C. Hocaoglu, and A.C. Sanderson, "A Virtual Design Environment using Evolutionary Agents", *Proceedings of the International Conference on Robotics and Automation*, May 1998.