

**UNITED STATES INTERNATIONAL TRADE COMMISSION  
WASHINGTON, D.C.  
Before the Honorable MaryJoan McNamara  
Administrative Law Judge**

**In the Matter of**

**CERTAIN MOBILE PHONES, TABLET  
COMPUTERS, SMART WATCHES,  
SMART SPEAKERS, AND DIGITAL  
MEDIA PLAYERS, AND PRODUCTS  
CONTAINING SAME**

**Inv. No. 337-TA-1300**

**DECLARATION OF PAUL R. PRUCNAL, PH.D. IN SUPPORT OF  
COMPLAINANTS' CLAIM CONSTRUCTION BRIEF**

I, Paul R. Prucnal, declare under penalty of perjury as follows:

1. I have been retained as an expert in this investigation by counsel for Complainant Ericsson Inc. ("Ericsson") to provide my opinions in connection with U.S. Patent Nos. 7,151,430 (the "'430 Patent"), 9,509,273 (the "'273 Patent") and 9,853,62100 (the "'621 Patent").
2. I understand that the technical field relevant to the '430 patent is inductors implemented within a semiconductor chip, and the technical field for the '273 and '621 patents is a transformer filter arrangement that can be integrated into a radio receiver or transmitter circuit.
3. I am being compensated at a rate of \$675 per hour for the time I spend on this matter. I do not have any financial or other interest in either party in this investigation or this proceeding itself, nor or in any other proceeding involving the '770 patent or the '400 patent, or any related patents.
4. Unless otherwise noted, the statements made herein are based on my personal knowledge, experience, and education. If called to testify about this declaration, I could and would do so competently and truthfully.

## **I. BACKGROUND AND QUALIFICATIONS**

5. I believe I am qualified to serve as a technical expert in this proceeding based upon my educational and work experience. A copy of my current *curriculum vitae* is provided as Exhibit A to this declaration. In preparing my analysis I have looked over all of intrinsic and extrinsic evidence cited in Complainants' Markman Brief and cited herein, including the '430, '273, and '621 patents and file histories.

6. I am currently a professor of Electrical and Computer Engineering at Princeton University in the School of Engineering and Applied Science.

7. I received my undergraduate education at Bowdoin College, where I graduated summa cum laude in 1974 with an A.B. in Mathematics and Physics. I then graduated from Columbia University in 1976 with a M.S. in Electrical Engineering. I went on to receive an M.Phil. from Columbia in 1978 in Electrical Engineering and a Ph.D. from Columbia in 1979 in Electrical Engineering.

8. Upon receiving my Ph.D. in 1979, I joined Columbia University as an Assistant Professor of Electrical Engineering and in 1984 I was promoted to Associate Professor.

9. In 1988, I joined the faculty of Princeton University as an Associate Professor of Electrical Engineering. My responsibilities there included teaching and research. During that time, I also was the founding director of the New Jersey Advanced Technology Center for Photonics and Optoelectronic Materials. My responsibilities there included leading a \$10 million research program involving approximately thirty faculty members.

10. In 1990, I was promoted to the position of full Professor of Electrical Engineering at Princeton University. My teaching responsibilities have included courses in electronic circuits, signal processing, photonics, and communications. My broad research interests at Princeton have included wireless communications, fiber-optic communications networks, computer interconnects, and network security. I also direct the Lightwave Communications Research Laboratory at Princeton University, through which much of my present research is conducted.

11. While at Princeton University, I received several awards and recognitions, including: (a) becoming a Fellow of the Institute for Electrical and Electronics Engineers (IEEE); (b) becoming a Fellow of the Optical Society of America (OSA); (c) receiving the Rudolf Kingslake Medal and Prize from the Society of Photo-Optical Instrumentation Engineers (SPIE) for the most noteworthy original paper in Optical Engineering; (d) receiving the Gold Medal Award from the Faculty of Mathematics, Physics, and Informatics at the Comenius University for leadership in the field of Optics; (e) receiving the Princeton University Graduate Mentoring Award; (f) receiving numerous Engineering Council Teaching Awards; (g) receiving the Walter Curtis Johnson Prize for Excellence in Teaching; (h) receiving the Princeton School of Engineering and Applied Science Distinguished Teacher Award; (i) receiving the 2015 President's Award for Distinguished Teaching at Princeton; (j) being elected to the National Academy of Inventors (2018). My election to the National Academy of Inventors cited my work on advanced wireless interference-cancellation technology.

12. I am the author of two books, "Optical Code Division Multiple Access: Fundamentals and Applications" (2005), and "Neuromorphic Photonics" (2018), and co-author

or contributor to approximately 33 additional book chapters, as well as over 300 peer-reviewed publications in peer-reviewed journals, and 365 conference proceedings.

13. In addition to the activities, education, and professional experience listed above, I have been involved in numerous research projects that contribute to my expertise relating to this report. My responsibilities in these projects have included, among other things, interference cancellation techniques for radio-frequency communications, simultaneous transmit-and-receive techniques for cellular radios, anti-jamming systems for radio communications and spread spectrum communications. Specifics on a few of these research projects are provided below.

14. In 1982, I worked for Optical Information Systems, Inc. on a project that involved transceiver design for fiber optic communications. My responsibilities included the design of transmitters and receivers for high-speed communication.

15. From 1983-1984, I worked for GTE Labs on a project that involved performance analysis of fiber optic communication systems. My responsibilities included the investigation of high performance modulation formats for communications.

16. From 1985-1986, I worked for AT&T Bell Laboratories on a project that involved research on multiple access techniques. My responsibilities included investigating time-division multiplexing for fiber optic networks.

17. In 1987-1988, I worked for IBM on a project that involved research on multiple access techniques for local area networks.

18. From 1987-1989, I worked for Dove Electronics on a project that involved research on communication switching technology and architectures. My responsibilities included the design and analysis of packet switching architectures.

19. From 1992-1995, I worked for Siemens Corporate Research on a project that involved research on switching technology. My responsibilities included the investigation of technologies for high speed multiplexing and switching networks.

20. From 1996 - present I have worked for the Institute for Defense Analyses on projects related to national security involving communications and computing.

21. From 1998-2000, I worked on a project for Ultrafast Optical Systems performing testing and measurement on optoelectronic transceivers.

22. From 1999-2000, I worked for SAIC on a project that involved research on communication network architectures. My responsibilities included the investigation of novel switching and multiplexing techniques for high-speed communication networks.

23. From 1999-2002, I worked for Multi Link Technologies, Inc. on a project that involved communication transceiver design.

24. From 2000-2002, I worked for Ultra-Fast Optical Systems on a project that involved research and development on regenerators for communication systems.

25. From 2000 - present, I have been a member of the advisory board on network technology for Alphion, Inc.

26. From 2003-2006, I worked for Kailight Inc. on a project that involved research and development on switching technology. My responsibilities included the design and testing of digital repeater for communication networks.

27. From 2006-2008, I led a DARPA funded project developing an add drop multiplexer for self-healing ring networks.

28. From 2004-2011, I worked for NEC Laboratories on a project that involved research on physical layer security in communication networks. My responsibilities included the design and analysis of techniques for steganography and data encryption.

29. I am also a named inventor on at least 27 issued U.S. patents, and at least 5 additional U.S. patent applications.

30. I have extensive experience in the electrical engineering field throughout my career. In particular, during the past 10 years I have taught several undergraduate and graduate courses at Princeton on communications, such as "Photonics and Lightwave Communications," which covers optical and radio-frequency analog and digital communications systems; "Electronic Circuit Design," which covers circuits, including their design and implementation; and "An Introduction to Engineering," which covers general electrical engineering principles. I am also involved with independent research projects involving senior thesis work in a variety of electrical engineering disciplines.

31. My research has been supported by research contracts and grants from the National Science Foundation (NSF), the U.S. Army Communication Electronics Command, the Defense Advanced Research Projects Agency (DARPA), the U.S. Navy, the National Security Agency, and L3 Telemetry East.

32. I have extensive experience consulting for the communications industry, including AT&T Bell Laboratories, NEC Labs, the Institute for Defense Analyses, and Alphion, Inc.

33. I have been a technical advisor to several startup companies in the telecommunications industry. Based on my patents, Kalight Photonics developed communication repeaters, before being acquired by a publicly traded company.

Another company, in conjunction with L3 Telemetry East, developed an anti-jamming system for the Army that helps defend against IEDs. This work is also based on my patents.

# **1. Claim Construction**

34. I understand that claim terms are to be construed from the perspective of a person of ordinary skill in the art (“POSITA”) as measured at the time of the invention.

35. I understand that in construing claim terms, a word or term should be given its plain and ordinary meaning unless it appears that the inventors were using the word or term to mean something else. In making this determination, of paramount importance are the claims, the patent specification, and the prosecution history. Additionally, the specification and prosecution history must be consulted to confirm whether the patentee had acted as a lexicographer (i.e., had provided special meaning to any disputed terms), or had intentionally disclaimed, disavowed, or surrendered any claim scope.

36. I understand that the most important evidence to consider in construing the claims is the “intrinsic” evidence, which I understand to include the claim language, the patent specification, and the prosecution history.

37. I understand that one must consider that a POSITA would have read a claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification. For this reason, the words of the claim must be interpreted in view of the entire specification. The specification is the primary basis for construing the claims and provides a safeguard that correct constructions closely align with the specification.

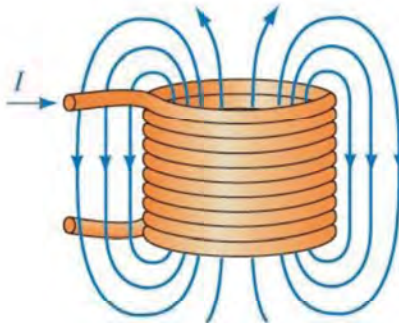
## 2. Indefiniteness

38. I understand that sometimes a claim term may be invalid for indefiniteness. A claim is indefinite only if, when read in light of the specification delineating the patent, and the prosecution history, it fails to inform, with reasonable certainty, a POSITA about the scope of the invention. It is my understanding that this standard mandates only clarity but does not require absolute precision, which is unattainable.

## II. TECHNICAL BACKGROUND

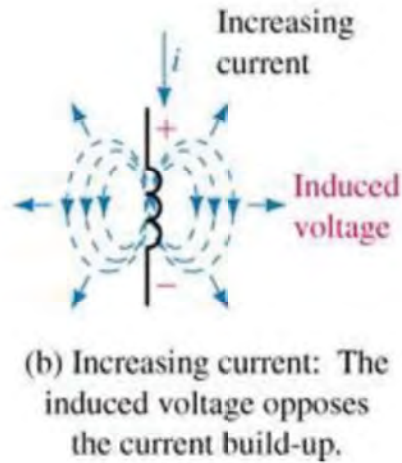
### Inductors and Oscillators

39. The '430 patent relates to an “inductor” design and relates to voltage-controlled “oscillators.” JXM-0001 at 1:19-22; 1:59-61. An inductor is a common electrical component, often consisting of coils or loops of conductive material, that take advantages of the properties of electromagnetic fields when an electric current passing through the inductor. Inductors are sometimes referred to as “coils” and the symbol for an inductor in an electrical circuit is the letter L. An exemplary inductor is shown below that has an electric current  $I$  flowing through its conductive coils:

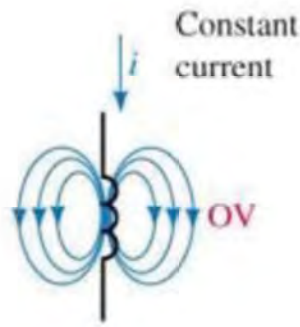


40. In the next few paragraphs I will explain how an inductor works. Magnetic fields are produced by moving electric charges. When an electrical current  $I$  flows through its

conductive coils, a magnetic field is present around those conductors. Creating this magnetic field takes work, and the inductor stores it as energy. Because work is also required to change this magnetic field, the inductor tends to oppose any further change in the current  $I$  and an opposing voltage  $V$  is induced across the inductor. Changing the stored magnetic field more quickly requires an even greater amount of work, so higher frequency signals, which change the current at a faster rate, induce an even larger opposing voltage across the inductor.



41. By contrast, if a constant direct current (DC) is applied to the inductor coils, the current passes through the inductor without opposition. As shown below, no voltage (0 Volts) is induced across the inductor when the current is steady and the magnetic field is unchanged.



(a) Steady current: Induced voltage is zero.

42. As indicated in the Background of the '430 patent, inductors can be used to make voltage-controlled oscillators. An oscillator is a circuit that is capable of producing waveforms. A voltage-controlled-oscillator or VCO is an oscillator which produces waveforms that can have a variable frequency.

43. The Background of the '430 patent refers to creating single-chip WCDMA (3G) transceivers. The Background further indicates these WCDMA transceivers require "two RF VCO's to be running on the chip at the same time." JXM-0001 at 1:26-33. In WCDMA systems, signals are transmitted and received in several different frequency bands, including signals at frequencies of 850 MHz and 1900 MHz.

44. In voltage-controlled oscillators, inductors are used to create a "resonator" circuit that produces waveforms at the desired RF frequency. Inductors, in combination with capacitors (a different type of circuit component that stores energy in the form of an electric field and opposes changes in voltage), can form a frequency-selective resonant circuit that allows a desired frequency to pass. In a resonant circuit, the stored energy is transferred back and forth between the inductor and a capacitor at a preferred frequency, called the "resonant frequency," which is

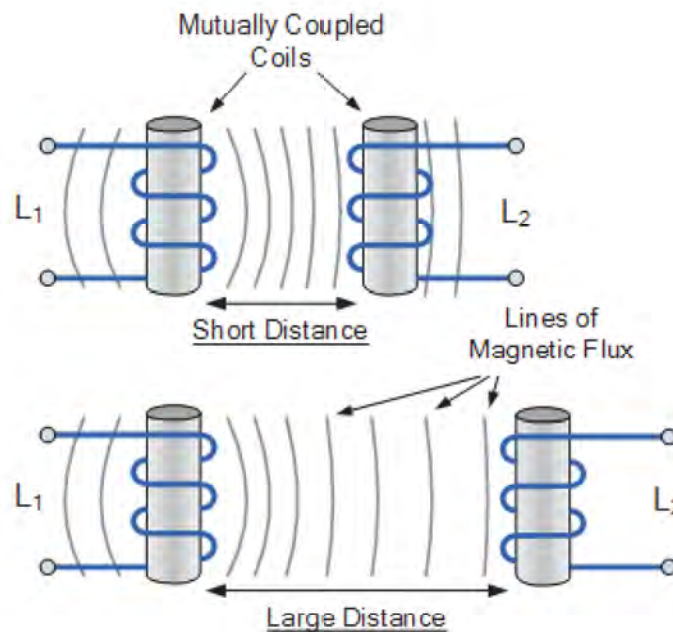
determined by the circuit component values. This circuit is commonly referred to as an oscillator and can generate high frequency waveforms for use in RF VCOs.

### **Mutual Inductance and Coils/Inductors**

45. The '430 patent indicates in the Background section that an arrangement of two RF voltage-controlled oscillators on a single chip may produce undesired interaction between the two oscillators, which “may result in spurious receiver responses and unwanted frequencies in the transmit spectrum.” This undesired interaction is caused by “mutual coupling mechanisms,” and the primary mechanism is usually electromagnetic (EM) coupling between the large inductor structures in the voltage-controlled oscillators.

46. Mutual inductance is the interaction of the magnetic field of one coil with another coil. Current flowing through one conductive coil produces a magnetic field that may generate (“induce”) a voltage in another coil that is situated in the same field. Mutual inductance is the phenomenon used to operate electric transformers and motors. But mutual inductance is a bad thing when the magnetic field generated by one coil interferes with the operation of another coil by electromagnetic induction.

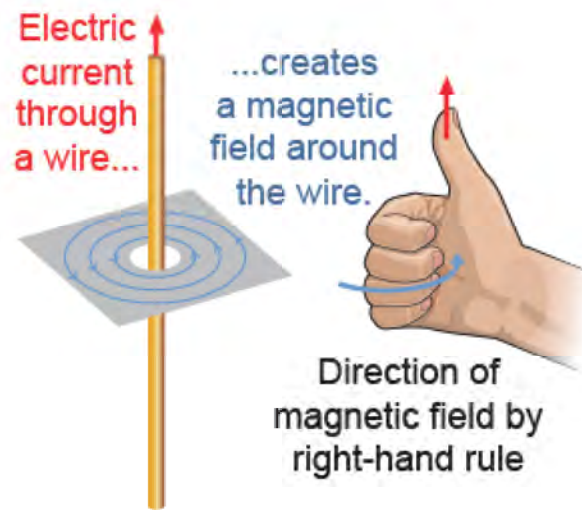
47. As shown below, the amount of mutual electromagnetic coupling between inductor L1 and L2 increases when inductor L2 is positioned closer to inductor L1. Inductor L1 generates a magnetic field because current is flowing through its coils, and this magnetic field can induce a voltage in the coils of inductor L2.



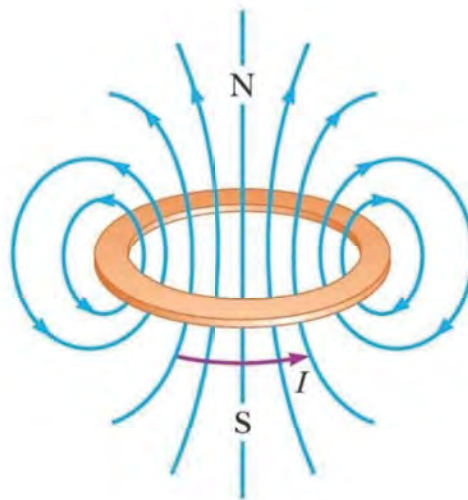
48. In the '430 patent, data is provided concerning the coupling coefficient  $k$  between two inductors. Coupling coefficient  $k$  is the amount of inductive coupling that exists between two coils. The amount of coupling is dependent on such parameters as the inductance values and relative spacing of the two coils.

#### **Electromagnetic Fields and Conductive Loops/Coils**

49. The magnetic field generated by current flowing through a straight conductor curls around the conductor in a ring. There is a relationship between the direction of current through a conductive coil and the direction of the magnetic field generated by that current. This is known as the "right hand rule." As shown below, by pointing your right thumb in the direction of the current in the wire and curling your fingers, your fingers will be curled in the same direction as the magnetic field generated by the current in the conductor.

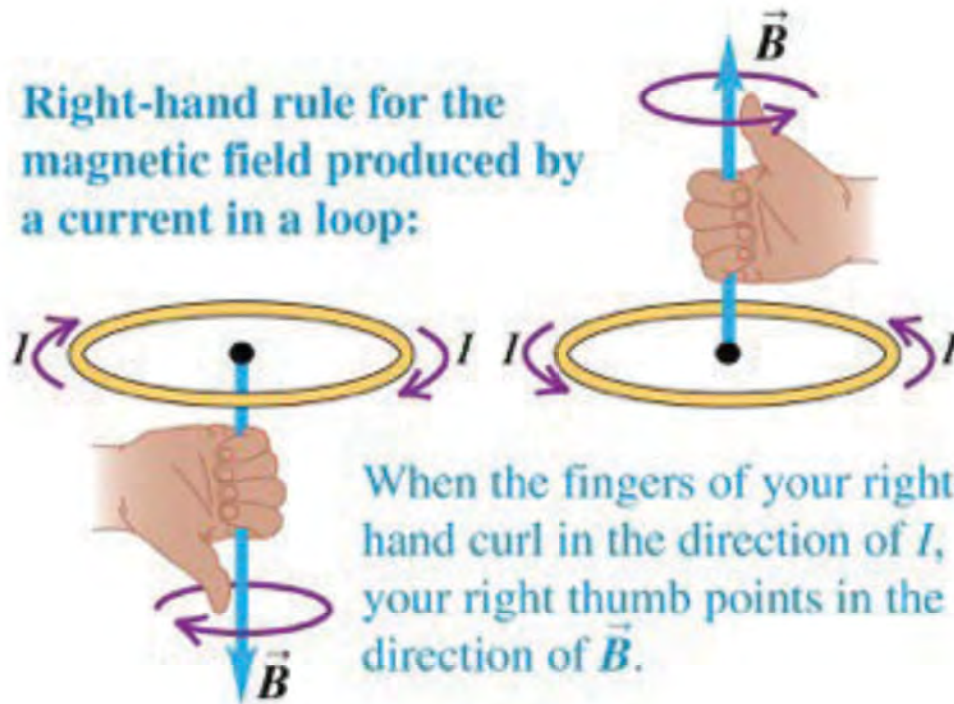


50. The inductors discussed in the '430 patent are in the shape of coils or loops. The same “right hand rule” can be used to determine the direction of the magnetic field generated by current flowing around each of these conductive coils or loops. Here, current flowing counter-clockwise around a circular coil generates a magnetic field with a direction pointing up:



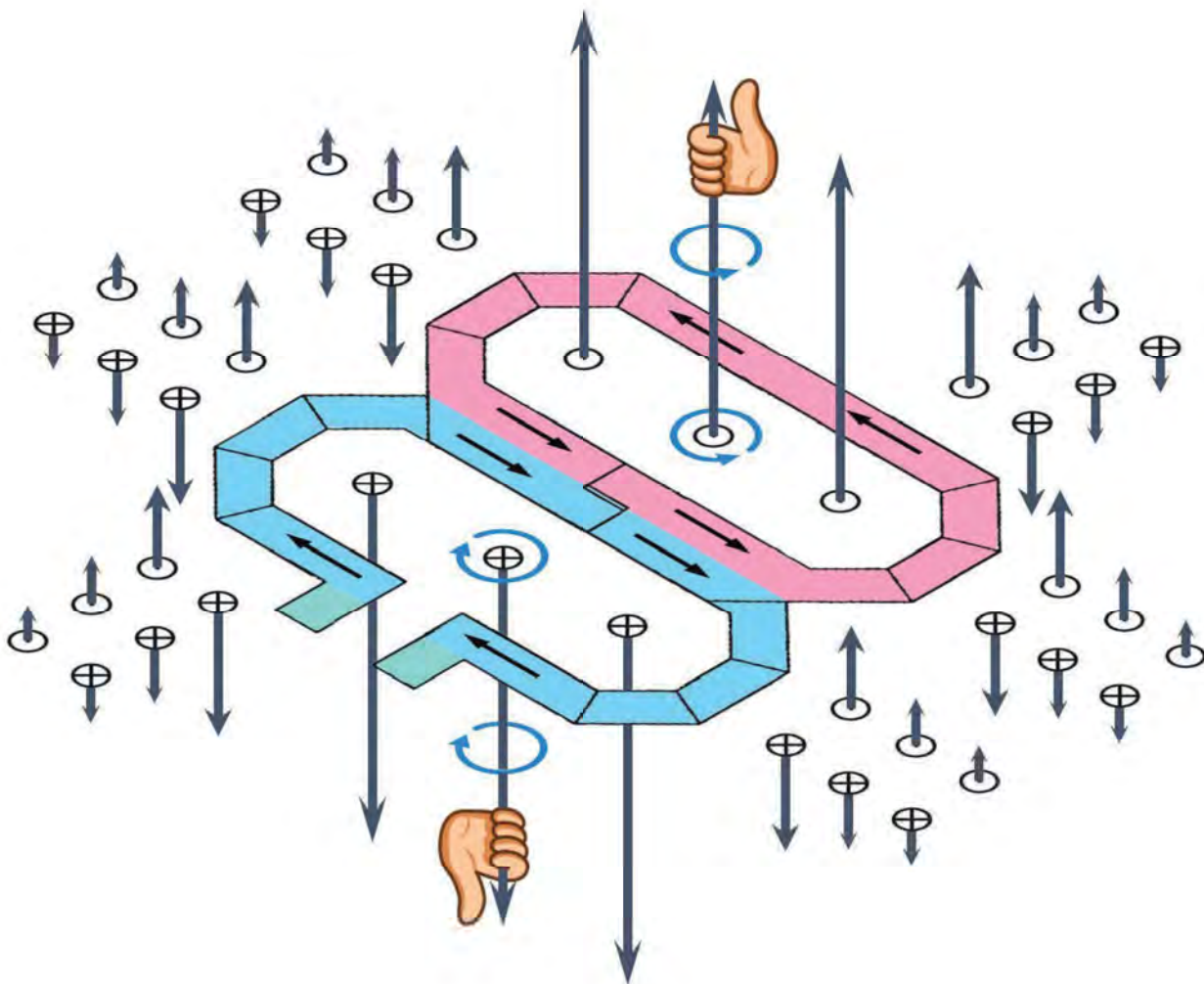
51. The magnetic field generated by this circular loop is strongest in the center and in locations near the coil. The magnetic field strength increase (depends directly on) the amount of current passing through the loop and decreases (depends inversely) on the distance from the loop.

52. When there are multiple coils on a chip, the resulting magnetic field at a particular location is the combination of the magnetic field contributions from each of these coils. In the example below, the loop on the left has current that flows in a counter-clockwise direction while the loop on the right has current that flows in a clockwise direction. The direction of the magnetic fields generated by each of these two loops will be approximately equal and opposite:



53. The '430 patent reduces mutual electromagnetic coupling between different inductors on a chip by forming an inductor of two (or four) symmetrical loops. As shown in Figure 2 of the '430 patent, the inductor is 8-shaped and formed of two loops. The top loop

(shown in red below) has current that flows in a counter-clockwise direction while the bottom loop (shown in blue below) has current that flows in a clockwise direction. The direction of the magnetic fields generated by each of these two loops will be approximately equal and opposite. When the magnetic field components from each loop are added together, they tend to cancel each other out at locations away from the inductor, as shown below:



### III. THE '430 PATENT

54. The '430 patent application was filed on August 16, 2004. The '430 patent is titled "Method of and Inductor Layout for Reduced VCO Coupling," and issued on December

19, 2006, to inventor Thomas Mattsson. The '430 patent has 3 independent claims and 18 dependent claims.

### **1. LEVEL OF ORDINARY SKILL IN THE ART**

55. A person of ordinary skill in the art (“POSITA”) relative to the '430 patent would have a bachelor’s degree in electrical engineering, computer science, computer engineering, or a similar discipline, and either a master’s degree in one of these fields of study or a minimum of two years of experience working in the wireless communications industry.

### **2. Preambles of claim 1 and 11: “An inductor layout having reduced mutual electromagnetic coupling, comprising” (claim 1)**

| <b>Ericsson’s Construction</b> | <b>Apple’s Construction</b> |
|--------------------------------|-----------------------------|
| 1. Limiting                    | 1. Not limiting             |

56. I agree with Ericsson that the preamble of claim 1 is limiting. I have been informed that a preamble is limiting if it “recites essential structure or steps” and “it is ‘necessary to give life, meaning, and vitality’ to the claim.” Here, a POSITA would understand that the preamble sets forth the essential feature of the invention, i.e., an “inductor layout” or “inductor design” that performs the function of “reducing EM coupling” or “mutual EM coupling” between the inductors. JXM-0001 at 1:59-66, 3:4-13.

### **3. A method of reducing mutual electromagnetic coupling between a first inductor and a second inductor on a semiconductor die, comprising (claim 11):**

| <b>Ericsson’s Construction</b> | <b>Apple’s Construction</b> |
|--------------------------------|-----------------------------|
| 11. Limiting                   | 11. Not limiting            |

57. A POSITA would have also understood the preamble of claim 11 to be limiting for a multitude of reasons for the same reason as indicated with respect to claim 1. But also because of the preamble’s requirement that the two inductors be “on a semiconductor die” is

necessary to understand the subject matter and is a fundamental characteristic of the fabrication method recited in the claim. Whenever the specification refers to this method, it also indicates it is implemented on a *single semiconductor chip*, and the Summary of the Invention makes this clear: “An inductor design for reducing mutual EM coupling between VCO resonators and a method of implementing the same on a single semiconductor chip.” JXM-0001 at 1:59-61.

58. This is clearly set forth in other parts of the specification:

In general, in another aspect, *a method* of reducing mutual electromagnetic coupling between *two inductors on a semiconductor die* comprises the step of *forming a first inductor on the semiconductor die* having a shape that is substantially symmetrical about a first predefined axis, the shape causing the first inductor to have a reduced far field, at least in some directions. *The method* further comprises the step of *forming a second inductor on the semiconductor die* at a predetermined distance from the first inductor, wherein a mutual electromagnetic coupling between the first inductor and the second inductor is reduced as a result of the first inductor having a reduced far field.

JXM-0001 at 2:13-24 (emphasis added).

Recent advances in wireless communication technology have allowed an entire RF transceiver to be implemented *on a single semiconductor die or chip*. However, integrating a complete RF transceiver *on a single chip* presents a number of challenges. For example, in wideband code division multiple access (WCDMA) transceivers, *a single-chip solution* requires two RF VCOs to be running on the chip at the same time.

JXM-0001 at 1:26-33 (emphasis added)

59. A person of ordinary skill would also understand that the preamble limitation to a “semiconductor die” would help inform them of other limitations in the body of the claim relating to physical dimensions. For instance, Claim 11 further requires that the “far field” of the first inductor be reduced, that the second inductor be positioned “at a predetermined distance from the first inductor,” and that current be supplied using “two closely spaced loops.” Therefore, the preamble requirement that both inductors be on the same semiconductor die aids in understanding the meaning and boundaries of these other limitations. Two inductors that are

on the same chip must be formed and positioned and supplied with current in a way that results in a reduced electromagnetic field and minimizes magnetic field contributions.

60. Additionally<sup>1</sup>, the language used in the other patent claims informs a person of ordinary skill that the fabrication method of claim 11 is limited to forming both inductors on a semiconductor die. The '430 patent includes ten apparatus claims directed at a two-inductor layout and nine method claims directed at forming two inductors on a die. JXM-0001 at claims 1-19. Dependent method claims 12-19 have similar limitations to dependent apparatus claims 2-10, with the exception of dependent apparatus claim 2. With respect to dependent claim 2, it recites: "The inductor layout according to claim 1, wherein said first inductor and said second inductor are *formed on a single semiconductor die*." JXM-0001 at claim 2 (emphasis added). A person of ordinary skill would understand that with respect to independent claim 11, there is no dependent method claim that corresponds to claim 2 because independent method claim 11 (unlike independent apparatus claim 1) has a preamble that already states the first inductor and second inductor are "on a semiconductor die." Therefore, a person of ordinary skill would conclude that the "semiconductor die" language in the preamble of method claim 11 is intended to be limiting and that the method claims require forming both inductors on a semiconductor die.

#### 4. "two closely spaced terminals"

| Ericsson's Construction       | Apple's Construction                         |
|-------------------------------|----------------------------------------------|
| This term does not need to be | "two terminals spaced as close to each other |

<sup>1</sup> The prosecution history shows a preliminary amendment made prior to any substantive examination replaced independent apparatus claim 1 and independent method claim 11 with new claims 25 and 26, which eventually issued as patent claims 1 and 11. The stated purpose of amending these claims was "to place them in better form" and to add the "two closely spaced terminals" limitation. JXM-0007.23—JXM-0007.24; JXM-0007.101, JXM-0007.105—JXM-0007.107. The change in form for the method claim provided antecedent basis for "a first inductor" and "a second inductor" in the preamble, and was accompanied by removal of "said semiconductor die" from the body of the claim because the "semiconductor die" limitation in the preamble was now associated with the first inductor and the second inductor.

|                                                                                                                                                                                                                                                           |                                                      |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|
| <p>construed.</p> <p>Plain and ordinary meaning applies, which is “two terminals in proximity to each other (such that the electromagnetic field at a certain distance from the first inductor (where the second inductor is positioned) is reduced)”</p> | <p>as possible”</p> <p>Alternatively: Indefinite</p> |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|

61. I understand Apple proposes that “two closely spaced terminals” should be construed as “two terminals spaced as close to each other as possible,” or in the alternative that the term is indefinite. I disagree with both proposals. I agree with Ericsson that this term does not need to be construed, and that here, the plain and ordinary meaning would be “two terminals *in proximity to each other* (such that the electromagnetic field at a certain distance from the first inductor (where the second inductor is positioned) is reduced).”

62. A POSITA would understand that in the context of the ’430 patent, “two closely spaced terminals” simply means “in close proximity” to one another and not “as close to each other as possible.” The language Apple applies comes from the specification at 4:28-42, but is just one example of terminals being in close enough proximity to each other such that the electromagnetic field at a certain distance from the first inductor (where the second inductor is positioned) is reduced. In other words, a POSITA would understand that the terminals need to be “in close proximity,” which includes being as close to each other as possible, but the claim language does not require them to be that close. Placing the terminals as close to each other as possible is merely *one example* of a design choice for terminal placement. The two terminals simply need to be “near” (i.e., proximate) each other.

63. Furthermore, as explained in ’430 Patent, when there are multiple conductive coils on a chip, the resulting magnetic field at a particular location is the combination of the

magnetic field contributions from each of these conductors. And if current is flowing in opposite directions in two different conductors, the magnetic fields from the conductors will also be in opposite directions and tend to cancel each other out at locations away from those two conductors.

64. These features of conductors and electromagnetism inform a person of ordinary skill that the “closely spaced” limitations in the claims are related to the functional limitations. Magnetic field contributions from these two terminals are minimized and mutual electromagnetic coupling between the two inductors is reduced as long as the spacing between the terminals is close enough that magnetic field contributions from each of the two terminals tend to cancel each other out in the vicinity of the second inductor.

65. A POSITA would understand that the specification does not ascribe a hard rule as to the spacing of the two terminals but simply requires that they be in close proximity (e.g., Fig. 2) versus the prior art (e.g., Fig. 1) as shown below. The spacing is for the purpose of reducing the electromagnetic field at the second inductor, originating from the first inductor. The specification makes this goal clear. *See, e.g., 1:66-2:2* (“In addition, two such inductors ***may be placed near each other*** and oriented in a way so that the induced current in the second inductor due to the ***magnetic field originating from first inductor is significantly reduced.***”) (emphasis added). A POSITA would understand that “near each other” simply means in close proximity to achieve the goal of reducing the electromagnetic field where the second inductor is positioned.

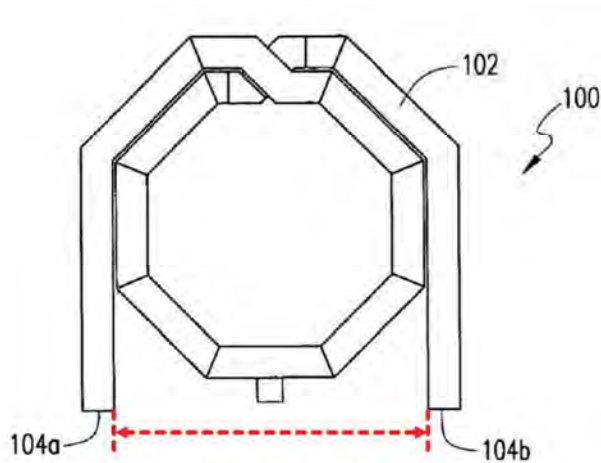


**FIG. 1**  
(PRIOR ART)

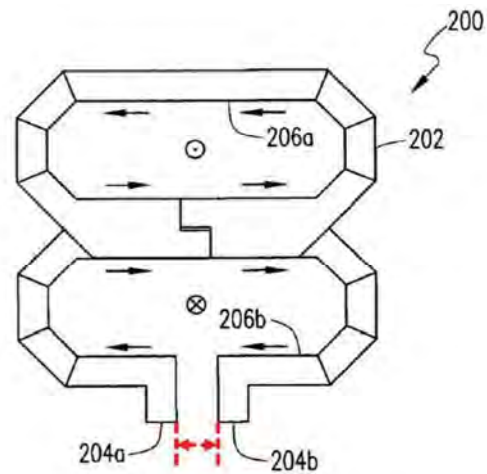


**FIG. 2**

'430 patent at Figs. 1 and 2 (emphasis added).

66. Nothing in the claim language, Fig. 2, the prosecution history, or cited art indicates the disputed claim limitations can only be met if the terminals are “as close to each other as possible.” Instead, the prosecution history and cited art indicate the two terminals for supplying electrical current to inductors in the prior art appear to be as far apart as possible, as shown below:

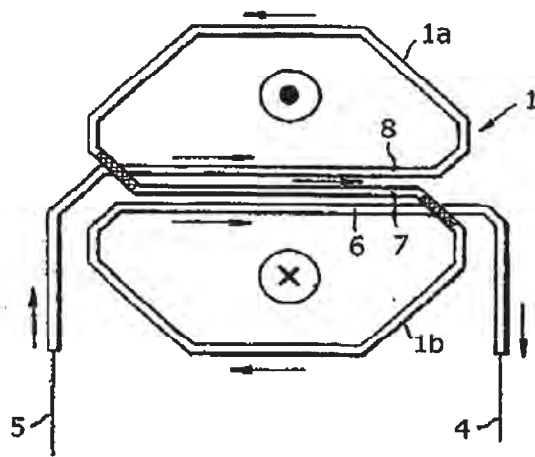


FIG.2

JXM-0007.115; *see also, id.* at JXM-0007.110, JXM-0007.249.

67. Additionally, the embodiment of an 8-shaped inductor 902 shown in Figure 9 of the '430 patent has two terminals for supplying current that are closely spaced but are not "as close together to each other as possible." These terminals are separated from each other along the vertical axis, and the specification further indicates that the layout for the other parts is symmetrical about that axis with "wires routed on top of each other so that they will not create an additional loop."

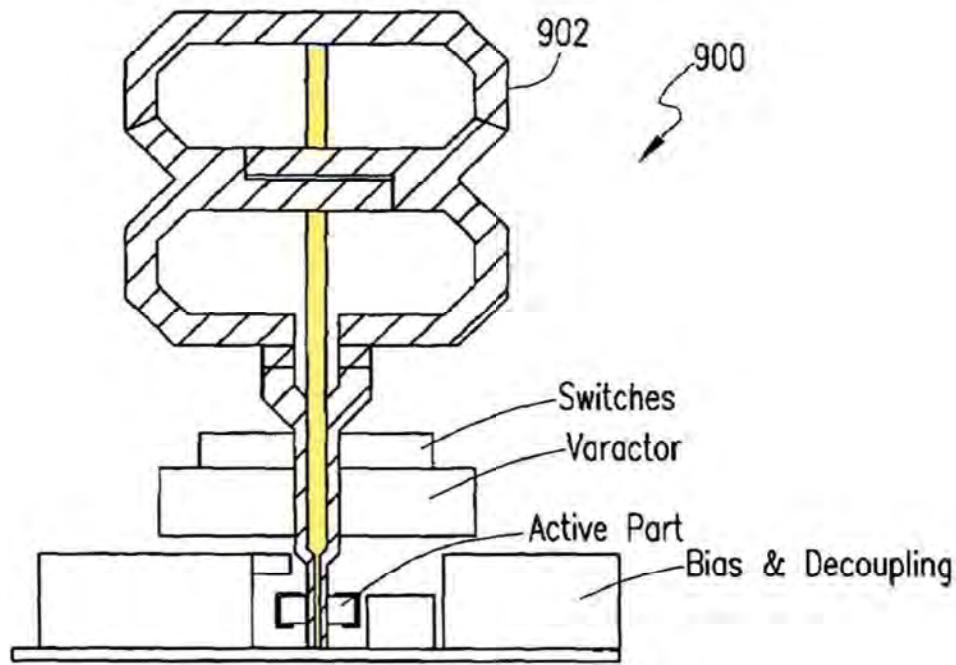


**FIG. 9**

JXM-0001 at 8:37-46, Figure 9.

68. Furthermore, the specification does not indicate these claim limitations are met only if the terminals are “as close to each other as possible.” It is clear that “closely spaced” just means two terminals *in proximity to each other* (such that the electromagnetic field at a certain distance from the first inductor (where the second inductor is positioned) is reduced). The specification refers to inductor 200 as an example, and states: For example, positioning the two terminals 204a and 204b as close to each other as possible helps make the field contributions from the two parts of the inductor 200 identical.” The narrower “as close to each other as possible,” is clearly not required to achieve the claimed function of “*minimizing* magnetic field contributions from the terminals.” Instead, the specification indicates this option is an *example*

that would help make field contributions from the two parts of inductor 200 *identical*, which the claim language defining the terminals and inductors does not require. JXM-0001 at 4:28-32; claims 1 and 11.

69. The specification expressly indicates that variations in spacing and size are possible, and that the layout will depend on considerations that are well-known to persons of ordinary skill. After the one phrase in the specification relied on by Apple for its proposed construction, the specification states:

*In theory, it should be possible to modify the geometry of the inductor (e.g., make the upper loop slightly larger) to compensate for this effect. The symmetry of the inductor 200 with respect to a center vertical axis is also important for minimizing the generation of common-mode signal components.*

*Other considerations may include basic layout parameters, such as the width and height of the inductor coil 202 together with the width and spacing of the surrounding metal wires. These parameters, however, are mainly determined by requirements on inductance, Q-factor, chip area, and process layout rules and have only minor influence on mutual coupling characteristics as long as symmetry of the inductor coil is maintained.*

JXM-0001 at 4:28-32 (emphasis added); claims 1 and 11.

70. In the context of the '430 patent and chip design generally, Apple's proposed construction does not make sense. A POSITA would understand that there are many considerations in play when spacing chip components, and a blanket requirement that the two terminals be spaced as close together as possible would impede on all of those competing considerations.

71. For instance, as discussed in Design of Analog CMOS Integrated Circuit (2<sup>nd</sup> Ed.), an extensive set of design rules can be used, including the layout of ground lines which can shield sensitive signals:

The extensive sets of design rules enforced by mainstream CMOS processes aim to maximize the yield of digital ICs while allowing moderately aggressive circuit design. Analog systems, on the other hand, demand many more layout precautions so as to minimize effects such as crosstalk, mismatches, noise, etc.

...

Second, sensitive signals can be “shielded” in the layout. Depicted in Fig. 19.42(a), one approach places ground lines on the two sides of the signal, forcing most of the electric field lines emanating from the “noise” lines to terminate on ground rather than on the signal. Note that this method proves more effective than simply allowing more space between the signal and the noisy lines [19.42(b)]. The shielding, however, is obtained at the cost of more complex wiring and greater capacitance between the signals and ground.

CXM-0013, e.g., at CXM-0013.5-7, CXM-0013.24-26.

72. This and other authoritative texts on the design of analog circuits have identified relevant layout considerations and informed skilled artisans that “additional” spacing may be prudent between two terminals to address problems with noise, capacitance, and the complexity of the wiring. As an example, capacitive crosstalk between the interconnect lines on a chip was a problem that engineers had to address. Figure 19.42 and the accompanying section on Analog Layout Techniques indicate signal lines may have to be shielded from each other by putting additional ground lines between them or by allowing more space to reduce coupling.

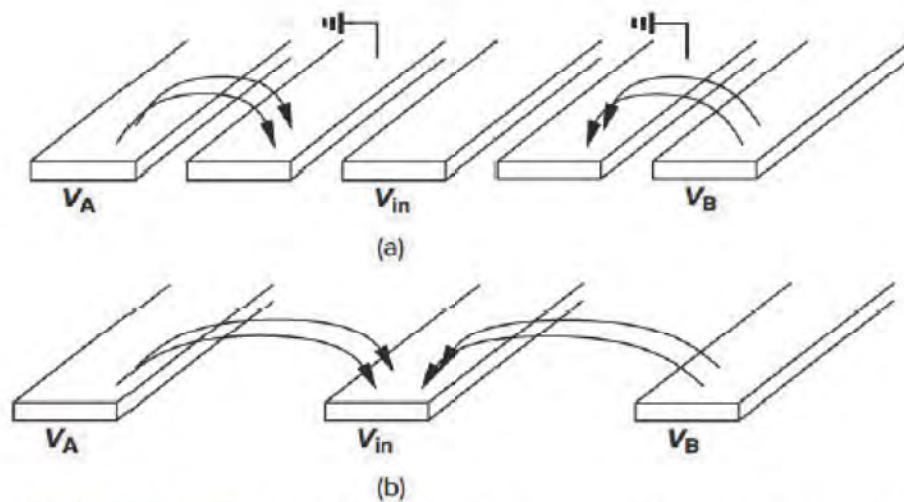


**Figure 19.42** (a) Shielding sensitive signals by additional ground lines; (b) greater spacing between lines to reduce coupling.

*See id.*

73. In general the spacing of the terminals would be determined by fabrication tolerances. In this instance, that would mean the minimum dimensions such that fabrication variations in the conductor width would not cause the conductors to actually touch and/or the terminals to short. For example, as discussed in Razavi below.

#### 19.1.1 Design Rules

While the width and length of each transistor are determined by circuit design, most of the other dimensions in a layout are dictated by “design rules,” i.e., a set of rules that guarantees proper transistor and interconnect fabrication despite various tolerances in each step of processing. Most design rules can be categorized under one of the four groups described here.

**Minimum Width** The widths (and lengths) of the geometries defined on a mask must exceed a minimum value imposed by both lithography and the processing capabilities of the technology. For example, if a polysilicon rectangle is excessively narrow, then, owing to fabrication tolerances, it may simply break or at least suffer from a large local resistance (Fig. 19.2). In general, the thicker a layer, the greater its minimum allowable width, indicating that as technologies scale, the thickness must be decreased proportionally. Figure 19.3 depicts examples of minimum widths in a 40-nm technology. Note that the thickness of the layers is not under the control of the layout designer.



**Figure 19.2** Excessive width variation in a narrow poly line.

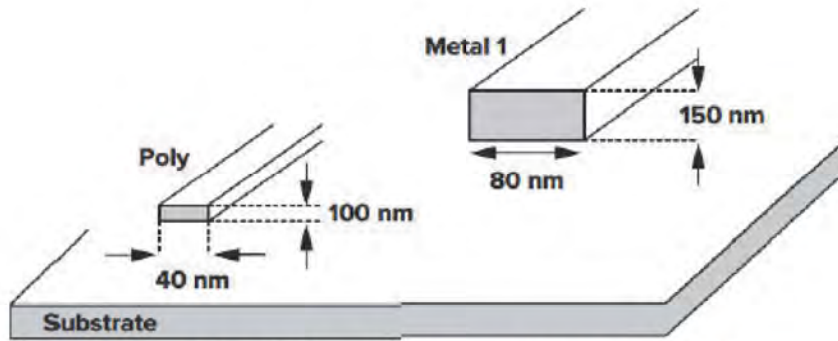


**Figure 19.3** Widths and thicknesses of poly and metal lines.

**Minimum Spacing** The geometries built on the same mask or, in some cases, different masks must be separated by a minimum spacing. For example, as shown in Fig. 19.4(a), if two polysilicon lines are placed too close to each other, they may be shorted. As another example, consider the case shown in Fig. 19.4(b), where a polysilicon line runs close to the S/D area of a transistor. A minimum spacing is required here to ensure that the implant surrounding the transistor does not overlap with the poly line.

*See id.*

74. Having an absolute rule as to the spacing (as Apple proposes) would not make sense and impede the ability of designers to meet specific case-by-case fabrication tolerances. For instance, two excessively close poly lines can cause a short. A POSITA would want to design the chip such that the conductor width would not cause the conductors to actually touch (as shown in Fig. 19.4 below).

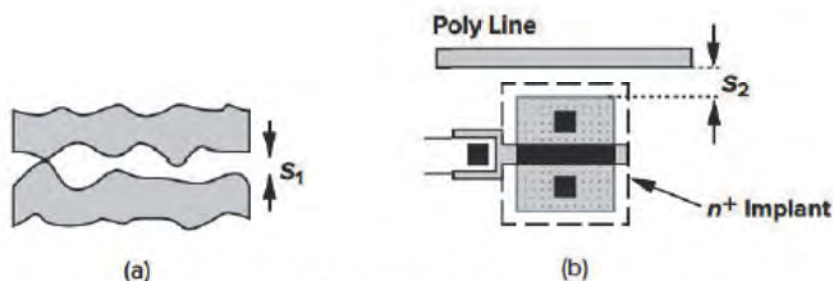


**Figure 19.4** (a) Short between two excessively close poly lines; (b) minimum spacing between active and poly.

*See id.*

75. Indeed, modern CMOS technologies typically involve hundreds of layout design rules including rules about spacing. But Apple's construction that terminals be spaced as close to each other as possible is not one that I am aware of. The below figure outlines some exemplary design rules.

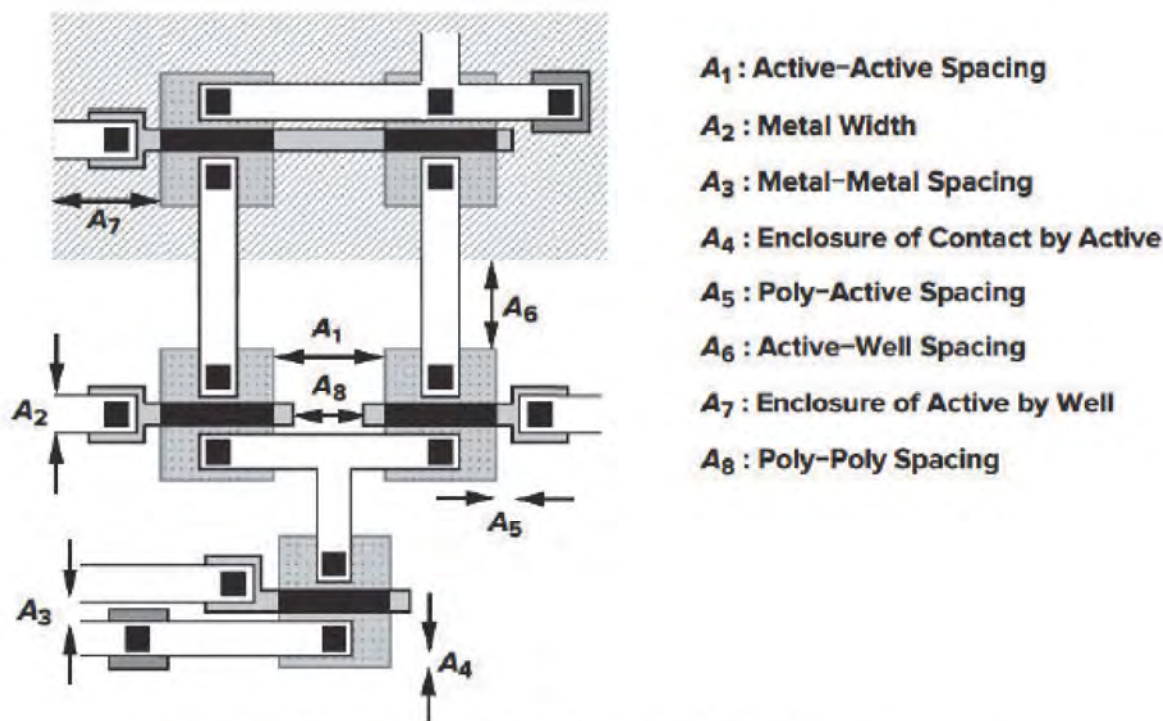


**Figure 19.7** Layout of a differential pair with PMOS current-source loads.

*See id.*

76. By contrast, Ericsson’s construction for “closely spaced,” is supported by the claim language, prosecution history, cited references, drawings, specification, and relevant extrinsic evidence, which provided persons of ordinary skill with enough information to understand what this term means. The purpose of the “closely spaced” limitation is related to functional limitations for minimizing magnetic field contributions and reducing mutual electromagnetic coupling. Therefore, spacing between two terminals supplying electric current to the first inductor is close enough when their magnetic field contributions tend to cancel each other out in the vicinity of the second inductor.

77. Because a POSITA would recognize that the spacing of the terminals would be determined by fabrication tolerances and other design considerations, instead of by one example cited in the specification. Therefore, I agree with Ericsson’s proposed construction and disagree with Apple’s proposed constructions.

**5. “a first inductor having a reduced far field”/”forming the first inductor to reduce a far field”**

| <b>Ericsson’s Construction</b>                                                                                                       | <b>Apple’s Construction</b> |
|--------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|
| “(reduced/reduce the) electromagnetic field at a certain distance from the first inductor (where the second inductor is positioned)” | Indefinite                  |

**“reduced electromagnetic field”**

| <b>Ericsson’s Construction</b>                                                                                                                                                                                                              | <b>Apple’s Construction</b> |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|
| <p>This term does not need to be construed.</p> <p>Plain and ordinary meaning applies, which is “the electromagnetic field emanating from the first inductor is reduced (at a certain distance from the first inductor where the second</p> | Indefinite                  |

78. As discussed prior, the claims include a first inductor and a second inductor (in the inductor layout or on a semiconductor die), and the first inductor is described as having “a reduced far field” or as being formed to “reduce a far field.” A person of ordinary skill would understand that the term “far field” requires construction because it does not have an ordinary and accustomed meaning in the specific field of the ’430 patent, which relates to VCOs used in RF transceivers and to an improved inductor design in a VCO. JXM-0001 at 1:17-22.

79. I have studied the prosecution history and amendments therein. As a result of a preliminary amendment, instead of having independent claim 1 recite a “reduced *electromagnetic field at a certain distance from said first inductor*” and independent claim 11 recite the first inductor has a “reduced *far field*,” patent claims 1 and 11 both recite the first inductor has a reduced “**far field**.” The claim language used in the original application shows that “far field” has the same meaning as “the electromagnetic field at a certain distance from the first inductor.” I understand this to mean that the purpose of this form change was to have patent claims 1 and 11 use exactly the same language to define the first inductor, instead of having claim 11 recite “far field” while claim 1 used an alternative phrase that has exactly the same meaning.

80. Furthermore, the Summary of the Invention confirms that the term “far field” is synonymous with “electromagnetic field at a certain distance from the first inductor” (where the second inductor is positioned. According to one paragraph in the Summary:

In general, in another aspect, a method of reducing mutual electromagnetic coupling between two inductors on a semiconductor die comprises the step of forming a first inductor on the semiconductor die having a shape that is substantially symmetrical about a first predefined axis, the shape causing the first inductor to *have a reduced far field*, at least in some directions.

JXM-0001 at 2:13-19 (emphasis added).

81. In the next paragraph in the Summary, the term “far field” is replaced with the definition set forth in the Description, corresponding to Ericsson’s proposed construction:

In general, in another aspect, an inductor layout having reduced mutual electromagnetic coupling comprises a first inductor having a shape that is substantially symmetrical about a first predefined axis, the shape causing the first inductor to *have a reduced electromagnetic field at a certain distance from the first inductor*, at least in some directions.

JXM-0001 at 2:25-30 (emphasis added).

82. The Summary also indicates the “certain distance” at which the electromagnetic field from the first inductor is reduced is at a second inductor located on the same chip. JXM-0001 at 1:66–2:2: “two such inductors *may be placed near each other* and oriented in a way so that the induced current in the second inductor due to the magnetic field originating from first inductor is significantly reduced.” JXM-0001 at 1:66–2:2. In the examples provided in the specification, the distance between the first and second inductors varies between 0.50 mm and 2.00 mm. *See* Figures 6 and 12; the patent specification further indicates the electromagnetic field and the far field is reduced “at a certain distance” from the first inductor and that unwanted mutual coupling between the pair of inductors is very low as a result. JXM-0001 at 4:14–21:

As a result, the *EM field* components *emanating at a certain distance* from the two substantially symmetrical loops 206a and 206b also have opposite directions and tend to counteract each other. . . . Consequently, the inductor 200 has been found to have a significantly *reduced far field at a certain distance from the inductor* coil 202.

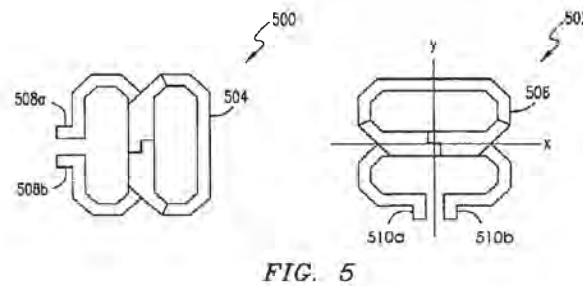
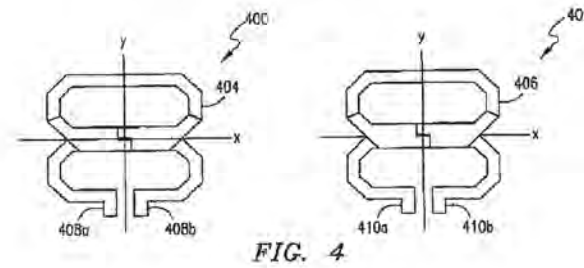
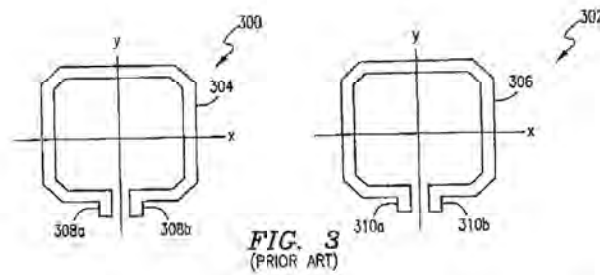
JXM-0001 at 4:14–21 (emphasis added).

83. Furthermore, the examples and metrics in the written description of the ’430 patent that provide guidance concerning a first inductor having a “reduced far field” and a “reduced electromagnetic field” at a certain distance from the first inductor (where the second inductor is positioned) include: the layouts of four different embodiments of the invention with two inductors in Figures 4, 5, 7, and 11; data showing the amounts of attenuation and

electromagnetic coupling between two inductors with different coil shapes, orientations, and offsets in Table 1, Table 2, and Table 3; and plots showing the drop in voltage gain between the ports of the first and second inductors for different coil shapes (as the distance between the first and second inductor is varied between 0.50 mm and 2.00 mm) in Figures 6 and 12.

84. Additionally, the patent expressly describes how a person of ordinary skill can determine the effectiveness of the reduced electromagnetic field from a first inductor in reducing mutual electromagnetic coupling with a second inductor at a certain distance from the first inductor. More specifically, data and plots were provided using several commercially available tools, such as the Momentum 2D EM Simulator from Agilent Technologies and FastHenry from the Computational Prototyping Group, and the patentee even provided a plot in Figure 8 that compares the results obtained using different tools. JXM-0001 at Fig. 8, 5:40-6:51, 7:64-8:27. These tools identified in the specification were well-known in 2004 and allowed persons of ordinary skill to independently calculate the electromagnetic fields from and electromagnetic coupling between two inductors for any of the disclosed embodiments. *See, e.g.*, CXM-0018; CXM-0021; CXM-0019; CXM-0020.

85. As an example, the patent uses the Momentum EM Simulator to show that the reduced far field from an 8-shaped first inductor greatly reduces mutual electromagnetic coupling with an 8-shaped second inductor located 1.00 mm away. A comparison is made of inductor layouts with two 8-shaped inductors in the orientations shown in Figures 4 or 5 to a prior art layout with two O-shaped inductors (shown in Figure 3):



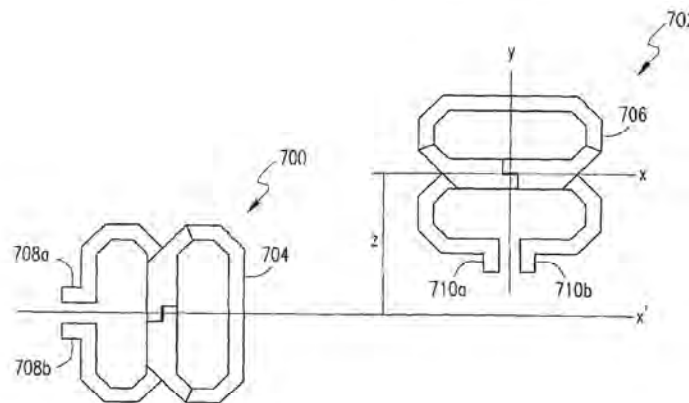
86. Data is provided in Table 1 showing the coupling coefficient “K” and amount of attenuation “Att” in decibels that results when using the inductor layouts in the embodiments of Figures 4 or 5 compared to the “reference” prior art layout of Figure 3. This data indicates replacing O-shaped inductors with the claimed 8-shaped inductors reduces the amount of mutual electromagnetic coupling by at least 30 decibels:

TABLE 1

| Inductor 1 | Inductor 2  | L1 [nH] | Q1    | Gvdd [dB] | Att [dB]  | K        |
|------------|-------------|---------|-------|-----------|-----------|----------|
| O-shape    | O-shape     | 0.841   | 16.93 | -54.0     | reference | 0.002077 |
| 8-shape    | O-shape     | 1.216   | 15.20 | -75.6     | 21.6      | 0.000173 |
| 8-shape_90 | O-shape     | 1.218   | 15.63 | -74.9     | 20.9      | 0.000187 |
| 8-shape    | 8-shape     | 1.216   | 15.84 | -86.5     | 32.5      | 0.000049 |
| 8-shape_90 | 8-shape     | 1.216   | 15.19 | -89.7     | 35.7      | 0.000034 |
| 8-shape_90 | 8-shape_-90 | 1.217   | 15.69 | -92.8     | 38.8      | 0.000024 |

As can be seen, making one of the inductors 8-shaped was shown to reduce the mutual coupling by up to 20 dB. Making both of them 8-shaped was shown to improve the isolation by up to 30 dB. Making both connectors 8-shaped and rotating them by 90 degrees in opposite directions was shown to improve the isolation nearly 40 dB.

87. Furthermore, the Momentum EM Simulator is used to show how the reduced far field from an 8-shaped first inductor reduces the mutual electromagnetic coupling with an 8-shaped second inductor located 1.00 mm away that is also offset on the vertical axis by a varying amount. A comparison is made of inductor layouts with two 8-shaped inductors that are offset, as shown in the Figure 7 embodiment below, to the prior art layout with two O-shaped inductors:



JXM-0001 at Figure 7.

88. Data shown in Table 2 depicting the coupling coefficient  $K$  and amount of attenuation  $A_{tt}$  in decibels that results when the claimed 8-shaped inductors are used with different offset spacing:

TABLE 2

| Offset<br>[mm] | L1 [nH] | Q1    | Gvdd [dB] | Att [dB] | Deg [dB]  | k estim  |
|----------------|---------|-------|-----------|----------|-----------|----------|
| 0.0            | 1.216   | 15.19 | -89.7     | 35.7     | reference | 0.000034 |
| 0.1            | 1.216   | 15.19 | -85.3     | 31.3     | 4.4       | 0.000057 |
| 0.2            | 1.216   | 15.19 | -82.5     | 28.5     | 7.2       | 0.000078 |
| 0.3            | 1.216   | 15.19 | -81.0     | 27.0     | 8.7       | 0.000093 |
| 0.5            | 1.216   | 15.19 | -81.8     | 27.8     | 7.9       | 0.000085 |
| 0.7            | 1.216   | 15.19 | -85.8     | 31.8     | 3.9       | 0.000053 |
| 1.0            | 1.216   | 15.19 | -103.4    | 49.4     | -13.7     | 0.000007 |

JXM-0001 at 7:52-63.

89. This data again indicates that replacing the prior art inductors with the claimed 8-shaped inductors reduces mutual electromagnetic coupling by about 30 decibels, as described in the specification:

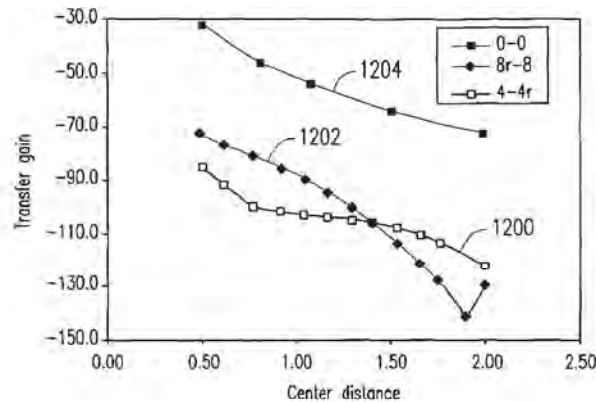
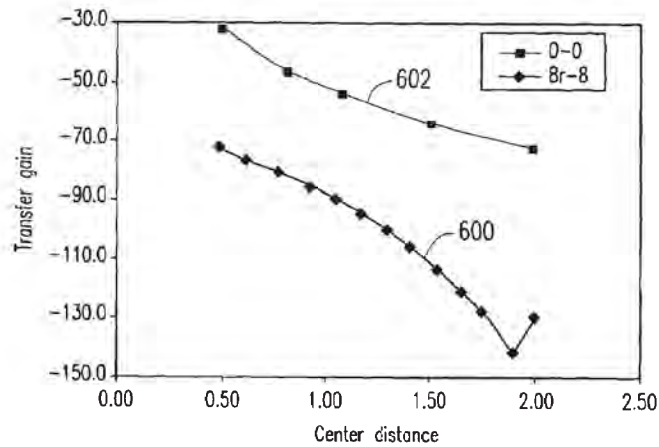
With this arrangement, some degradation of the inductor isolation was observed, but even at a 1 mm offset, which corresponds to an orientation of 45 degrees, an improvement of about 30 dB in mutual coupling reduction is achieved for the 8-shaped inductor.

JXM-0001 at 7:46-51.

90. Additional examples show replacing prior art inductors with four-leaf-clover-shaped inductors also greatly reduces mutual electromagnetic coupling because these claimed inductors having a reduced electromagnetic field at a certain distance from the inductor. *See* JXM-0001 at 3:19-27. One inductor layout of a pair of four-leaf-clover-shaped inductors is shown in Figure 11, and the data in Table 3 indicates use of four-leaf-clover-shaped inductors reduces mutual electromagnetic coupling by about 40 decibels. *See* JXM-0001 at 9:26-37 (Table 3).

91. The examples in the '430 patent include specific parameters for coil size, geometry, orientation, spacing, offset, inductance value (L1), and RF frequency that provide sufficient guidelines to enable a person of ordinary skill to determine the scope of the claims. In

Figures 6 and 12 below, the FastHenry tool was used to show the drop in voltage gain between the ports of the first and second inductors as the distance between the first and second inductor is varied between 0.50 mm and 2.00 mm:



92. As shown above, the pair of 8-shaped inductors (plots 600 and 1202) have between 30 and 40 dB more isolation than the pair of prior art O-shaped inductors (plots 602 and 1204) over these same distances, while the pair of four-leaf-clover-shaped inductors (plot 1200) provides 10 dB more of isolation than the 8-shaped inductors for distances below 1.00 mm. *See* JXM-0001 at 7:25-33; 9:13-17.

93. Furthermore, after the filing of the '430 patent application in 2004, other researchers published papers directed to the benefits of using inductors with shapes and

orientations that reduce mutual electromagnetic coupling between inductors located on the same semiconductor die. There is a 2009 paper entitled, "Reduction of Inductive Crosstalk Using Quadrupole Inductors," that refers to 8-shaped inductors as "quadrupole inductors." See CXM-0011.2 and Fig. 2. The Abstract states, "Interference due to inductor crosstalk is a growing concern in modern RFICs where inductors are placed in close proximity. A quadrupole inductor is explored as a method to reduce inductive crosstalk." CXM-0011.1.

One inductor, designated as the aggressor inductor, is driven with a 4-stage differential ring oscillator and a buffer which generates a signal of known frequency. Another inductor, designated as the victim inductor, is used as a component in a voltage-controlled oscillator (VCO). Therefore, the signal from the aggressor inductor propagates and couples into the victim inductor and becomes a form of interference in the VCO.

CXM-0011.4.

94. In this paper, the authors use the term "very far" to refer to points where the distance to the inductor is much larger than the inductor radius. The 8-shaped inductors in this paper are used in similar ways and for similar reasons as the 8-shaped inductors in the '430 patent:

The quadrupole has a very desirable characteristic: at points equidistant to the two loops, or at points very far away, two equal but opposite magnetic fields are seen, which will cancel one another. Hence, by orienting the quadrupole inductor properly, the magnetic coupling can be significantly reduced.

CXM-0011.2.

95. The distance between the "first" aggressor inductor (having electromagnetic fields that cause interference) and the "second" victim inductor, which are on the same chip, is less than 1.00 mm, as shown below:

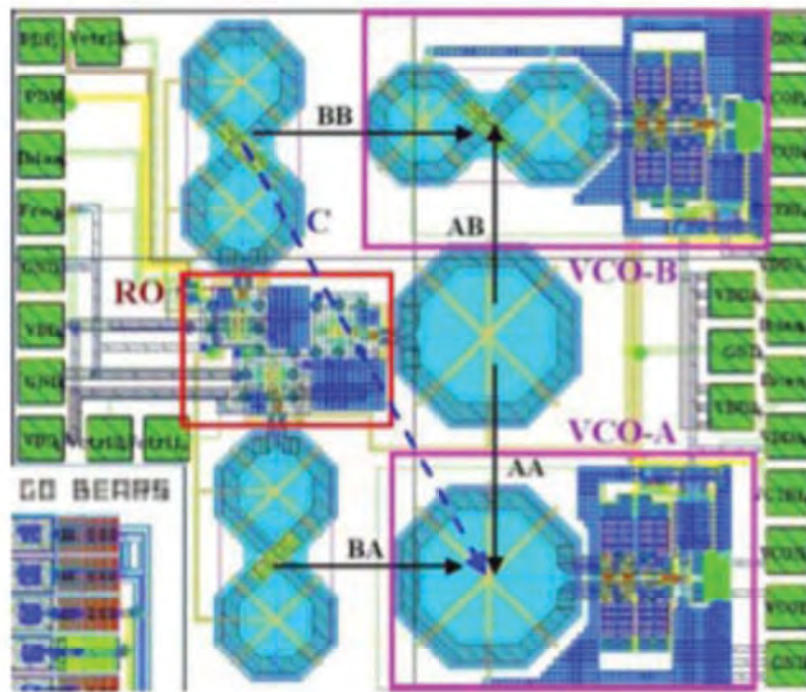


Fig. 6. Chip layout with ring oscillator (RO) and VCO sections labeled. Four permutations of aggressors and victims (AA, AB, BA, BB) are labeled. Case C (dashed line) is for a separation of 830  $\mu\text{m}$  and an angle of 28°.

CXM-0011.4.

96. Additionally, a 2008 paper entitled, “Twisted Inductors for Low Coupling Mixed-Signal and RF Applications,” shows 8-shaped inductors and four-leaf-clover-shaped inductors in Figure 1, which are referred to as 2-lobed and 4-lobed twisted inductors. See CXM-0014.1 and Fig. 1. This paper describes the problems encountered when using conventional inductors: “Fundamentally, parasitic coupling originates in conventional spiral inductors because the magnetic field is not localized; it extends far beyond the perimeter of the inductor causing parasitic currents to be induced in nearby inductors.” CXM-0014.1. Figures 2 and 5 of the paper are similar to Figures 6 and 12 in the '430 patent in showing the reduced coupling and voltage gain between the first and second inductors with various geometries as the distance between them is varied (separation is no greater than 200 microns in paper):

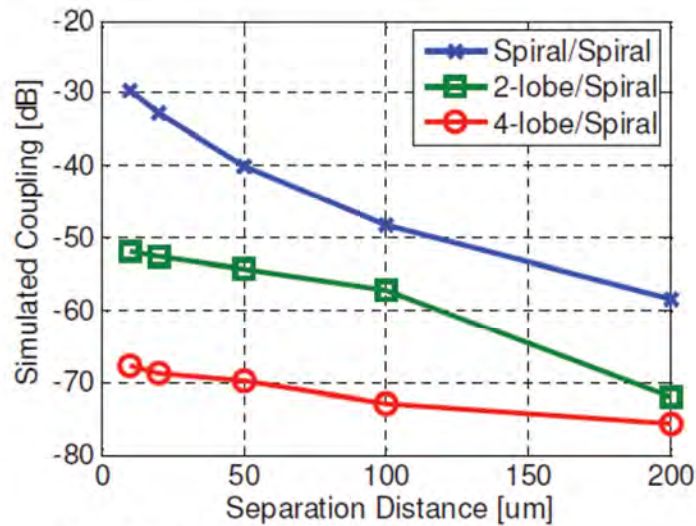


Figure 2: Simulation results of the magnetic coupling versus separation distance at 5GHz between the spiral/spiral, 2-lobe/spiral and 4-lobe/spiral pairs.

CXM-0014.2.

97. Moreover, the 2008 paper expressly compares data with and cites to the '430 patent, stating: "Simulation results of similar structures developed independently also confirm our measured results." See CXM-0014.3, CXM-0014.4.

98. These 2009 and 2008 papers are relevant because they are in the same technical field and address the same problems as the '430 patent. The Field of the Invention for the '430 patent concerns "voltage-controlled oscillators (VCO) of the type used in radio frequency (RF) transceivers and, in particular, to an improved inductor design in a VCO," while the Background of the Invention refers to the problems with existing techniques for "reducing the mutual EM coupling between the VCOs due to the inductors." JXM-0001 at 1:19-22, 1:41-42.

99. In contrast, any extrinsic evidence (including potential testimony by an Apple technical expert) concerning the use of the term "far field" by antenna designers is irrelevant to construction of the disputed terms in the '430 patent. To begin with, the Dictionary of IEEE Standards Terms, which lists the phrase "far-field region," indicates this phrase is used in the

field of land-mobile communications transmitters to describe the “region of the field of an *antenna*.” JXM-0006.3. The function and purpose of an antenna is to convert electrical signals into electromagnetic waves in order to send radio transmissions. The inductors described in the ’430 patent are not antennas and the word “antenna” does not appear in the ’430 patent. That is because the point of the inductor designs and VCO resonator circuits described in the ’430 patent is “reducing mutual EM coupling between VCO resonators.” JXM-0001 at 1:59-61.

100. Any definitions used by antenna designers for “far field” would lead to absurd results if applied to the inductors and circuits described in the ’430 patent. Consequently, these antenna definitions would be rejected by persons of ordinary skill. The ’430 patent specification indicates the invention relates to the voltage-controlled oscillators used in RF transceivers, and in particular to WCDMA (3G) transceivers. JXM-0001 at 1:18-33. There are a number of different frequencies used in WCDMA systems, such as bands centered at 850 MHz. The wavelength of an 850 MHz radio signal is *3.53 meters*, which is much larger than any chip or device.

101. The “far field” of an antenna transmitting at 850 MHz, which is a required frequency for WCDMA transceivers, is at least 0.35 meters long. Whatever definition Apple uses for an antenna’s “far field,” that definition would cause this Court to interpret the ’430 patent claims as directed at electromagnetic fields that are about 35 centimeters away from the first inductor. Apple’s antenna interpretation would be completely irrational to a person of ordinary skill because the ’430 patent specification provides examples showing reductions in voltage gain and mutual coupling between inductors that are one millimeter apart, which makes Apple’s alternate definitions off by a factor of 350.

102. As a general rule of thumb, the far-field region can be loosely defined as being sufficiently far from the antenna such that the radiating field behaves like a uniform plane wave.

103. If the antenna length  $D$  is less than  $\lambda/2$ , where  $\lambda$  is the wavelength, then the far-field region starts at  $2\lambda$ . But such a short antenna would not be efficient as a transmitter.

104. By contrast, transmitters require longer antennas with lengths  $D=\lambda/2$  or greater, and in that case the far-field starts approximately at the Fraunhofer distance  $2D^2/\lambda$  and must be at least as long one wavelength and longer than the antenna. Using this relation, if the transmitter antenna has length  $D=\lambda/2$  or longer, then the Fraunhofer distance is at least  $2D^2/\lambda = \lambda/2$ , so the far field distance is at least one wavelength. For example, if a transmitter is operating at a frequency of 850MHz (with wavelength  $\lambda=c/850\text{MHz}=35.29\text{cm}$ ), then the far-field distance is approximately 35cm.

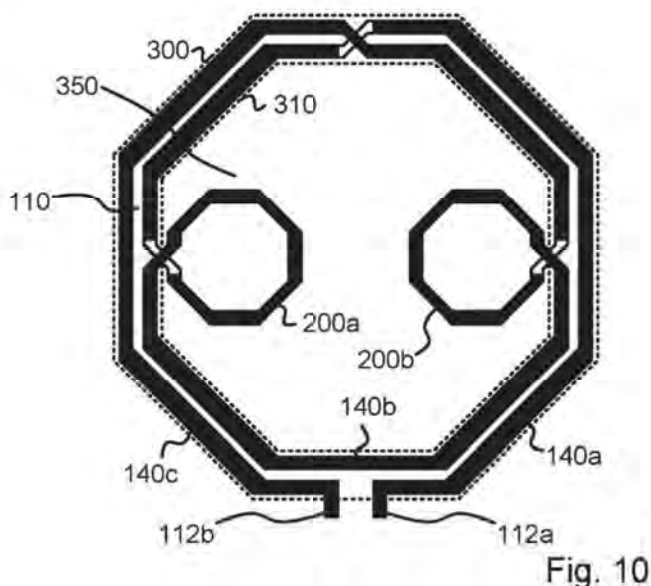
#### **IV. THE '273 AND '621 PATENTS**

105. The '273 patent issued from Application No. 14/233,497, filed as Application No. PCT/SE2012/050729 on June 28, 2012. The '273 patent is titled "Transformer Filter Arrangement," and issued on November 29, 2016, to inventors Stefan Andersson, Fenghao Mu, and Johan Wernehag. The '621 patent is also titled "Transformer Filter Arrangement," and issued on December 26, 2017, to inventors Stefan Andersson, Fenghao Mu, and Johan Wernehag. The '621 patent issued from Application No. 15/044,466, filed on February 16, 2016, which is a continuation of Application No. 14/233,497.

106. The Field of the Invention is described as relating to "a transformer filter arrangement, which may be integrated in an integrated circuit, for example a transformer filter arrangement for use in a radio receiver circuit or a radio transmitter circuit." JXM-0002 at 1:5- 9. The invention, as stated in the Summary of the Invention, is: "[t]he transformer filter

arrangement comprises a transformer having a first winding and a second winding formed by conducting layers of one of a chip and printed circuit board. Winding loops of both the first and the second windings, when considered in a plane of one of the chip and printed circuit board, enclose an area of the one of the chip and printed circuit board. The transformer filter arrangement comprises at least one reactive sub circuit, each comprising at least one inductor. The first winding of the transformer is divided into a plurality of winding segments. At least a first one of the at least one reactive sub circuit being connected in series with the winding segments of the first winding between two such winding segments, and having at least one of the at least one inductor, possibly each inductor of the at least the first one of the at least one reactive sub circuit, located inside said area. The planar transformer and the at least one reactive sub circuit are tuned such that the transformer filter arrangement is configured to pass signals at a fundamental frequency and to suppress signals at least at one interfering frequency.” JXM-0002 at 1:47-67.

An example of the structure of one of the two windings required by the asserted claims is shown in Figure 10 below:



107. In this example structure, the winding (labeled as first winding 110) includes an outer border 300 and an inner border 310 formed by tracing. The inner border 310 of this winding 110 encloses an area 350. This area is valuable space to be used on an integrated circuit chip or a PCB. As such, in this example, two reactive subcircuits 200a and 200b are formed in this enclosed area 350. In this structure the two reactive subcircuits 200a and 200b are inductors formed in series with the tracings of the winding 110.

**1. LEVEL OF ORDINARY SKILL IN THE ART**

108. A POSITA relative to the '273 patent and the '621 patent would have a bachelor's degree in electrical engineering, computer science, computer engineering, or a similar discipline, and either a master's degree in one of these fields of study or a minimum of two years of experience working in the wireless communications industry.

**2. “winding loops of both the first and the second windings, when considered in a plane of the first winding and the second winding of the transformer, enclose an area” (claims 1, 7, 12, and 13 of '273 patent and claims 1 and 18 of '621 patent)**

| Ericsson’s Construction                                                                                                                                             | Apple’s Construction                                                                                                                                                                                                                                    |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Plain and ordinary meaning applies, which is “an area of the chip or PCB is contained within winding loops of both the first and second winding of the transformer” | “winding loops of the first winding when considered in a first plane of the first winding enclose an area, and winding loops of a second winding when considered in a second plane of the second winding, enclose the same area when viewed from above” |

109. The specification establishes specific nomenclature and characteristics of planar transformers in the context of on-chip transformers.

The balun arrangement 30 considered in embodiments of the present invention is of the type comprising a planar transformer with a primary and a secondary winding that are electromagnetically coupled to each other. Here, a planar transformer can be considered to be implemented by interleaved or stacked topology on a chip or printed circuit board, where the

windings in interleaved topology are placed in the same conducting layer with vias interconnecting the winding parts to close the winding loops, and the windings in the stacked topology are placed in adjacent conducting layers covering substantially the same chip or substrate area.

JXM-0002 at 5:36-46.

110. Most notably, the balun arrangements discussed in the patent specification were implemented in at least two ways. The balun or transformer may be implemented on a chip or printed circuit board as an interleaved topology or as a stacked topology. Each winding of the transformer is considered to be within the same “plane” of the planar transformer although, as will be shown, a stacked topology exhibits a plane that includes more than one metal layer.

111. Looking first at a *stacked* arrangement, a person of ordinary skill would find that the plain and ordinary meaning of the disputed claim language covers what is described in the specification and shown in Figures 9 and 10:

FIG. 9 illustrates the layout of the second winding 120 according to this example embodiment. The second winding is formed by conducting layers of a chip or printed circuit board, as will be further demonstrated below. The second winding is located between an outer border 300 and an inner border 310, which is inside the outer border 300, wherein the inner border 310 defines an area 350. That is, the winding loops of the second winding 120, considered in a plane of the chip or printed circuit board, encloses the area 350.

JXM-0002 at 8:43-51.

112. Thus, the claimed first winding (referred to as a second winding in the specification) may be realized in a first metal layer in a plane of a chip or PCB and enclose a specific area that is inside these windings (*e.g.*, area “350” as denoted in FIG. 9). Moreover, the claimed second winding (referred to as a first winding in the specification) may be realized in a second metal layer of the same plane (which includes both of these metal layers) of a chip or

PCB and enclose a specific area that is inside these windings (*e.g.*, area “350” as denoted in FIG.

10), which appears to match the enclosed area that was referenced in FIG. 9:

FIG. 10 illustrates the layout of the first winding 110 together with two inductors 200*a* and 200*b* of reactive sub circuits. For example, the layout examples in FIGS. 9-10 may correspond to the schematic circuit diagram of the transformer filter arrangement 30 shown in FIG. 4 having two reactive sub circuits 130*a-b* implemented as the reactive sub circuit 130 in FIG. 5. In that case, the inductor 200*a* belongs to the reactive sub circuit 130*a* and corresponds to the inductor 200 of FIG. 5. Similarly, the inductor 200*b* belongs to the reactive sub circuit 130*b* and corresponds to the inductor 200 of FIG. 5. The winding segments 140*a-c* are indicated in FIG. 10 as well. The terminals 112*a-b* of the first winding 110 are indicated at the bottom of FIG. 10. The first winding is formed by conducting layers of a chip or printed circuit board. As can be seen in FIG. 10, also the first winding is located between the same outer border 300 and the same inner border 310 as the second winding 120. That is, also the winding loops of the first winding 110, considered in a plane of the chip or printed circuit board, encloses the area 350.

JXM-0002 at 8:60-9:12.

113. The specification refers to the enclosed areas in Figures 9 and 10 using the same reference numeral 350, indicating that the claimed plane must include both the first and the second windings, which provide the borders that enclose area 350. This interpretation is supported by the specification:

As illustrated in FIG. 10, the inductors 200*a* and 200*b* of the reactive sub circuits 130*a-b* can be located inside the inner border 310, *i.e.* in the area 350, thereby saving valuable circuit area; the combination of the planar transformer 100 together with the inductors 200*a* and 200*b* of the reactive sub circuits 130*a-b* occupies the same circuit area as a “normal” planar transformer (*i.e.* a planar transformer where both windings are laid out as in FIG. 9), and no additional circuit area outside the outer border 300 is consumed by the inductors 200*a* and 200*b* of the reactive sub circuits 130*a-b*.

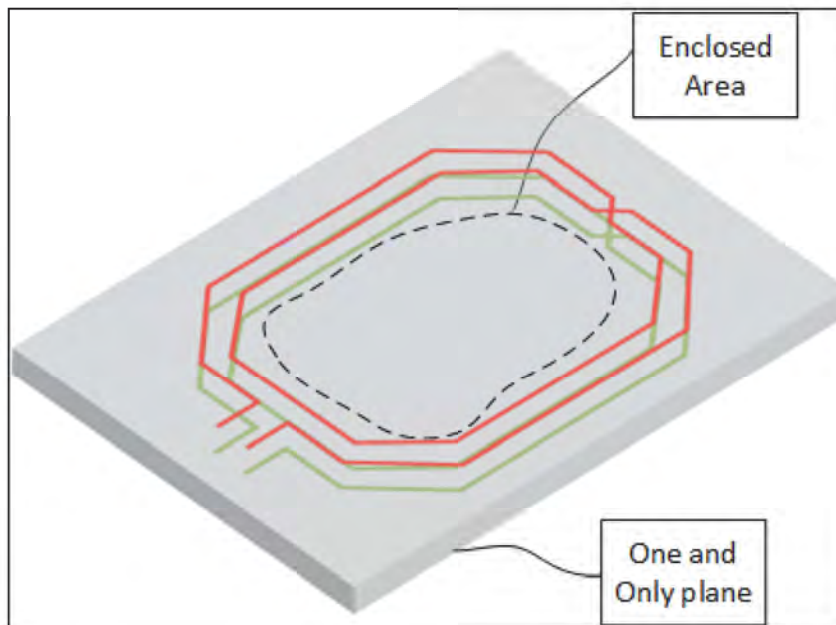
JXM-0002 at 9:39-49.

114. In this *stacked* topology, the tracings of the first winding in a first metal layer of the plane and the second windings in a second metal layer of the plane may be substantially (although not entirely) “mirror images” of each other. But these two windings are disposed in two different metal layers on a substrate. And the reason why these overlapping windings must be in two different layers is to maintain electrical isolation from each other and realize the electrical functionality of a planar transformer.

115. Thus, when the “plane” for the overall chip or PCB is considered, there is an “area” (as denoted by reference numeral 350) that is “enclosed” by both windings in a stacked topology that consists of the *intersection* of the first metal layer space enclosed by the first winding and the second metal layer space enclosed by the second winding. As will be shown below, a similar “area” is “enclosed” by the *intersection* of the spaces enclosed by the first winding and by the second winding in an interleaved topology. Moreover, an “area” is “enclosed” by the *intersection* of the spaces enclosed by both windings in a “shifted” stacked topology, which is not explicitly described in the patent specification but was known in 2011 to persons of ordinary skill and described in contemporaneous literature.

116. Under Apple’s construction, the claims only cover a *stacked* topology, and only one in which there is a *perfect overlap* of the innermost border of the two stacked windings. In order to limit the scope of the claims in this manner and rule out disclosed embodiments, Apple’s construction rewrites the disputed term by adding limitations that appear nowhere in the claim language or in the patent specification, and which are inconsistent with the ordinary meaning of the phrase “enclose an area.” In particular, Apple’s proposed construction inserted requirements for “a second plane” and that the two winding loops “enclose *the same* area *when viewed from above*.”

117. Apple’s construction conjures up and asks the Court to delineate a new, *second* plane that the specification does not recognize. As shown below in a pictorial representation of the combination of the two sets of windings disclosed in FIGs. 9 and 10, the two metal layers of the stacked embodiment are on either side of a substrate (not shown) and are within the one and only plane (shown as having a nominal thickness). Apple’s construction is inconsistent with the claims and written description by requiring a person of ordinary skill to imagine “a second plane” with which to determine whether the two planes enclose “the same area when viewed from above.” This rewriting of the claim to split one plane into two is fiction that is unsupported by anything in the specification.



118. A person of ordinary skill would understand that the claimed “area” that is “enclosed” by the two sets of windings is the chip space that is inside the innermost border of the first and second windings of the claimed transformer—valuable chip space that can be used for the placement of additional circuitry, such as the inductors 200a, 200b, and 340 of Figures 10 and 13. As shown above, this area is in a plane thick enough to encompass the layers of the first

and second windings in a stacked topology. It is the area that is an intersection of the chip (or PCB) space enclosed by the first winding and the chip (or PCB) space enclosed by the second winding.

119. Apple's construction deliberately changes the ordinary meaning of the words to preclude any interleaved topology, even though the patent specification expressly indicates that "embodiments of the present invention" can be implemented by interleaved or stacked topology." CXM-0002 at 5:36-46. It is accomplished by Apple's creation of a "second" plane and addition of a limitation requiring that the "same" area instead of "an area" is within both sets of windings.

120. Apple's construction would exclude what are expressly described as "embodiments of the present invention." In particular, the planar transformer can be achieved using an interleaved structure:

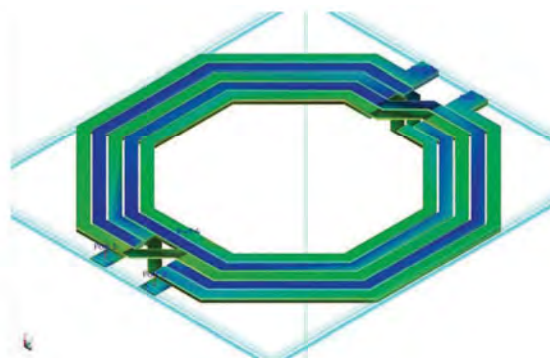
Here, a planar transformer can be considered to be implemented by *interleaved* or stacked topology on a chip or printed circuit board, where the windings in interleaved topology are placed in the same conducting layer with vias interconnecting the winding parts to close the winding loops, and the windings in the stacked topology are placed in adjacent conducting layers covering substantially the same chip or substrate area.

CXM-0002 at 5:36-46 (emphasis added).

121. And by requiring "a second plane" for considering the second winding, Apple's construction is incoherent to a person of ordinary skill because both the first and second windings in an interleaved structure are on the same metal layer. A second plane different from the first plane has no meaning or context for this interleaved structure for a planar transformer.

122. The fact that Apple's construction is at odds with the views of a person of ordinary skill at the time of the invention is confirmed by relevant, contemporaneous documentary evidence written by persons in the same technical field. According to persons or

ordinary skill in 2011, “[an] interleaved structure is a planar structure which mainly makes use of lateral magnetic coupling. ... Figure 2.11 shows the layout of an interleaved balun with a turns ratio of 2:3 with center tap at half of the physical length of secondary winding.” CXM-0023.21–CXM-0021.22. As shown in this referenced figure, the tracings of the first winding and second winding can be located in the same metal layer (except for connecting tracings that dip into adjacent metal layers to electrically couple the tracings while maintaining electrical isolation between the windings). The transformer windings correspond to the green tracings (first winding) and the blue tracing (the second winding) in FIG. 2.11 of CXM-0023.21–CXM-0021.22.



123. Apple’s construction also rules out this interleaved structure by forcing the area enclosed by the first winding and the area enclosed by the second winding to be “the same area.” This would force the innermost transformer winding of the green trace and the innermost transformer winding of the blue trace to occupy exactly the same physical space in order to enclose “the same area when viewed from above.” If the blue tracings and green tracings in the same metal layer were to occupy the same space, the result would be shorting and a direct physical connection between the first and second windings, thereby preventing the transformer from functioning as a transformer.

124. Further, this same contemporaneous documentary shows that Apple's construction would exclude a preferred way that was then known for implementing the stacked topology for a planar transformer:

Figure 2.12 shows a stacked balun with a turn ratio of 2:2. The two windings in the stacked balun belong to different layers. Including the layers to accommodate the crossings, a stacked balun is normally implemented using four metal layers.

CXM-0023.22–CXM-0023.23.

125. Apple's construction would rule out this stacked structure by forcing all the windings on four metal layers to enclose "the same area when viewed from above," notwithstanding the consideration by Apple of a second plane. If the windings are in more than two different planes and if the crossings do not overlap, how can each winding enclose *the same* area when considered in only a first and second plane?

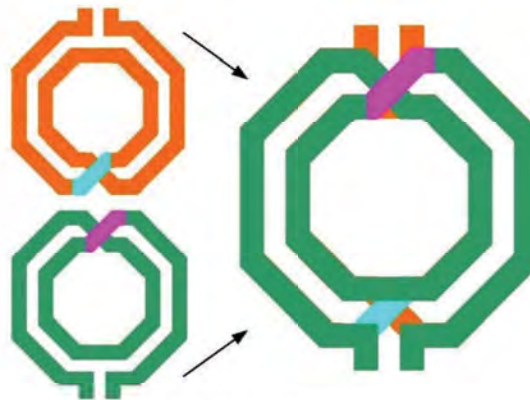


Figure 2.12 A stacked 2:2 balun

126. Further yet, this same contemporaneous evidence indicates persons of ordinary skill also implemented the stacked topology in another way that runs afoul of Apple's construction. Persons of ordinary skill in 2011 would shift the alignment of windings on different

metal layers. As a result, there would be places where the tracings on different layers, when viewed from above, would not overlap, as shown in FIG. 2.18 on page 29:

The optimization on spacing is a fine-adjustment process to find the best performance in terms of insertion loss and amplitude and phase imbalance. For a stacked balun, increasing the spacing between adjacent conductors improves the amplitude and phase imbalance only a little as vertical coupling is dominant. For an interleaved structure, normally the minimum allowed spacing defined in the design rules of the process will be tried at first. Then a couple of simulations should be run with adjusted spacing until a satisfying performance is achieved.

CXM-0023.22-CXM-0023.23.

127. This is another instance where Apple's contrived construction rules out actual implementations of stacked topology for planar transformers, which is one of the preferred embodiments of the invention.

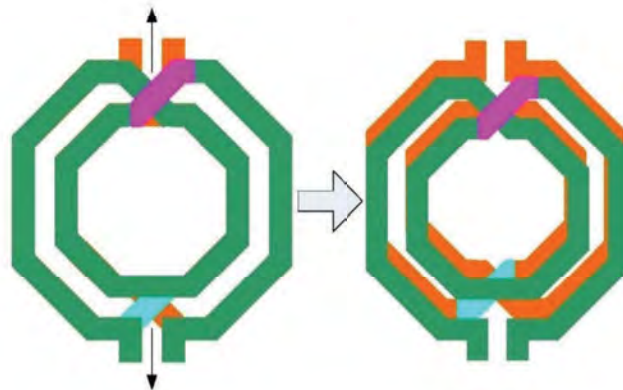


Figure 2.18 A shifted stacked balun

128. All of the structures shown and described above, which have first and second windings arranged to form a transformer, are examples of planar transformers. That is, the transformer windings are realized in a plane instead of as a coil. The use of the word “planar” by persons of ordinary skill, including the ’430 inventors, to describe each of these known implementations confirms that each of these structures should fall within the scope of the disputed claim language, which refers to chip or PCB area “when considered in a plane of the first winding and the second winding.”

129. The cited prior art also supports Ericsson’s consideration of the term “plane” as covering a space that includes windings on different metal layers in a chip or PCB. U.S. Pub. 2009/0195324, cited by the Examiner during prosecution, teaches that a “plane” may include *multiple layers* in a CMOS chip. In particular, “[t]he substrate 66 defines a *circuit plane* where etching, deposition, or other techniques are used to form the circuit transformer circuit 24 *in one or more layers*.” U.S. Pub. 2009/0195324 at [0022].

130. In summary, persons of ordinary skill in 2011-12 understood that the windings of a planar transformer on a chip or PCB would not be an exact mirror of each other, whether implemented on the same or different metal layers. Skilled artisans would have identified “an area” that is “enclosed” by the first and second windings as an area that is within the innermost boundaries of the first and second windings when considered together. This area within the innermost winding provides available space for a reactive subcircuit, such as the inductors shown in Figures 10 and 13. This construction of the disputed term is consistent with its ordinary meaning and provides all the functionality of a planar transformer while achieving the stated goal in the Summary of providing a transformer filter arrangement “suitable for integrated circuit integration.”

**3. “interfering frequency” (claims 1, 7, 12, and 13 of ‘273 patent and claims 1 and 18 of ‘621 patent)**

| <b>Ericsson’s Construction</b>                                                                                                                                                                                 | <b>Apple’s Construction</b>                       |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|
| Plain and ordinary meaning applies, which is “frequency, such as an odd-order harmonic of the fundamental frequency that results in unwanted signal content within the bandwidth of the wanted signal content” | “odd-order harmonic of the fundamental frequency” |

131. It is my opinion that the ordinary meaning proposed by Ericsson is supported by the specification:

The planar transformer 100 and the one or more reactive sub circuits 130 a-b are tuned such that the transformer filter arrangement 30 is configured to pass signals at a fundamental frequency and to suppress signals at one or more interfering frequencies. Thereby, the desired filtering action may be accomplished. . . .

For example, in a radio receiver circuit, so called harmonic down conversion, *i.e.* that unwanted signal content is down converted by harmonics of a local oscillator (LO) signal into the same band as wanted signal content is down converted to by the fundamental tone of the LO signal, and thereby interferes with said wanted signal content, may pose a problem. The one or more interfering frequencies, for which the transformer filter arrangement 30 is configured to suppress signals, may therefore be or include one or more harmonics of said fundamental frequency, for which the transformer filter arrangement 30 is adapted to pass signals. Thereby, the problems with harmonic down conversion may be reduced.

CXM-0002 6:49-53, 6:64-7:9.

132. That is, the reactive subcircuit (which is disposed in an area enclosed by the planar transformer) is a filter that suppresses all (interfering) frequencies outside of a passband centered around a fundamental frequency. These suppressed frequencies may be harmonics, odd-order harmonics, or any other unwanted signal that is outside the wanted signal centered at the fundamental frequency.

133. The specification indicates the inventors contemplated various filtering arrangements to suppress many forms of unwanted signals:

The reactive sub circuit 130 of FIG. 6 may be used to accomplish a band pass characteristic of the transformer filter arrangement 30. The series connection of the inductor 210 and the capacitor 215 may be tuned to resonate at the fundamental frequency, thereby providing a pass band around the fundamental frequency, where signals at frequencies inside this pass band are allowed to pass,

whereas signals at frequencies outside this pass band are suppressed.

CXM-0002 at 8:4-11.

134. That suppression may be accomplished in different ways:

In some embodiments, the transformer filter arrangement may have a notch-filter characteristic with notches at the one or more harmonic frequencies.”

CXM-0002 at 7:9-11.

135. The inventors differentiated this concept in dependent claim 11.

“The transformer filter arrangement of claim 8, wherein the transformer filter arrangement has a notch-filter characteristic with notches at the at least one harmonic frequency.

CXM-0002 at claim 11.

136. The specification also identifies unwanted signals of particular relevance:

In case the down conversion mixer used operates on differential signals (*e.g.* with reference to FIG. 2, if the down conversion mixer is included in the differential processing circuitry 40), it is normally of particular relevance to suppress signals at odd order harmonics of the fundamental frequency, since these, in contrast to signals at the even order harmonics of the fundamental frequency, are not inherently suppressed by the use of differential signal processing. Therefore, in some embodiments, said one or more harmonics of the fundamental frequency may be or include one or more odd order harmonics.

CXM-0002 at 7:11-22.

137. The specification even identifies what may be the most harmful of these harmonic unwanted signals:

Normally, of the odd order harmonics, the third harmonic (for which the frequency is three times the fundamental frequency) may be the most harmful one. For example, the third harmonic of an LO signal is normally the one of the odd order harmonics that has the highest amplitude (consider *e.g.* a square-wave LO signal). Therefore, in some embodiments, the one or more odd order

harmonics included in said one or more harmonics of the fundamental frequency may be or include the third harmonic.

CXM-0002 at 7:22-30.

138. Most significantly, the patent specifically claims the filtering out of particular harmonics, including the odd order harmonic, in dependent claims. Dependent claim 9 recites: The transformer filter arrangement of claim 8, wherein the at least one harmonic includes at least one odd order harmonic.” Dependent claim 10 recites: “The transformer filter arrangement of claim 9, wherein the at least one odd order harmonic includes a third harmonic.” CXM-0002 at claims 9 and 10.

139. The specification provides a comparison with a circuit found in cited prior art, i.e., U.S. Patent Publication 2009/0195324:

The circuit in US 2009/0195324 A1 comprises a balun transformer, which has a series connection of a capacitor and an inductor connected between a center tap of the balanced-side winding of the balun transformer and ground. Notably, the capacitor and inductor are located outside the balun transformer, thereby taking up additional circuit area. In contrast thereto, in embodiments of the present invention, inductors of reactive sub circuits are located inside the inner border 310 of the transformer windings 110, 120, whereby valuable circuit area is saved. In US 2009/0195324 A1, the capacitor and inductor are set to resonate at a resonance frequency equal to a second harmonic frequency. Further analysis of the circuit in US 2009/0195324 A1 reveals that, what this circuit actually does is to suppress common-mode variations at said resonance frequency, but does not perform any “actual” filtering, i.e. it does not remove or suppress any content of the differential signal at the resonance frequency; a balanced input signal, with a frequency equal to said resonance frequency, input on the balanced-side winding of the balun transformer in the circuit of US 2009/0195324 A1 would pass through that circuit unaffected, i.e. in the same way as if said capacitor and inductor had not been present.

CXM-0002 at 11:56–12:12.

140. And the specification even indicates that different characteristics can be combined in embodiments of the invention: “[E]mbodiments of the present invention, which performs actual filtering, are capable of suppressing such odd-order distortion appearing as differential

signals. It can be noted that, in fact, embodiments of the present invention may be combined with the circuit disclosed in U.S. 2009/0195324 A1 to achieve both filtering and common-mode stabilization.” CXM-0002 at 12:31-34.

141. In my opinion, Apple’s construction should be rejected because it rewrites the claim language and does so by importing the limitations of dependent claim 9 into the independent claims.

I declare under penalty of perjury that the foregoing is true and correct to the best of my knowledge and belief insofar as it states facts and that it contains my honest opinions on the matters upon which I have been asked to give them.

Executed on June 22, 2022 in Princeton, NJ.

  
Paul R. Prucnal

**PAUL R. PRUCNAL**

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**Education:**

Ph.D. 1979 Columbia University  
M.Phil. 1978 Columbia University  
M.S. 1976 Columbia University, Electrical Engineering  
A.B. 1974 Bowdoin College, *summa cum laude*

**Experience:**

1990-Current Princeton University, Professor  
1992 Visiting Professor, University of Parma (Sabbatical)  
1991 Visiting Professor, RCAST, University of Tokyo (Sabbatical)  
1989-1991 New Jersey Advanced Technology Center for Photonics and  
Optoelectronic Materials, Founding Director  
1988-1990 Princeton University, Associate Professor  
1984-1988 Columbia University, Associate Professor  
1979-1984 Columbia University, Assistant Professor

**Consulting:**

- Phillips Laboratories (1979-1981)
- Optical Information Systems, Inc (1982)
- GTE Labs (1983-1984)
- AT&T Bell Laboratories (1985-1986)
- IBM (1987-1988)
- Dove Electronics (1987-1989)
- Siemens Corporate Research (1992-1995)
- Center for Computing Sciences (1996-Present)
- Sun Microsystems (1998-2001)
- SAIC (1999-2000)
- Multi Link Technologies, Inc. (1999-2002)
- Alphion, Inc. (2000-Present)
- Ultra Fast Optical Systems (2000-2002)
- Kailight Inc. (2003-2006)
- NEC Laboratories (2004-2011, 2020-present)
- Princeton Optronics (2005-2006)
- Access Optical Networks (2010-2018)
- Bascom Hunter Technologies (2010-present)
- Luminous Computing (2019-present)

**Current Research Activities (experimental and theoretical):**

Optical networks, photonic switching, optical signal processing, RF photonics,  
optical interconnects, silicon photonics, neuromorphic photonics.

## **Honors:**

### **Invited Plenary Speaker**

- 9th International Conference on Computer Communications, Tel Aviv, October 1988
- Topical Meeting on Photonic Switching, Salt Lake City, March 1989
- Congreso de Informatica y Telecomunicaciones, Berisso, Argentina, April 1989
- IEEE Communications Society Local Chapter Talks, 1989
- IEEE International Conference on Communications, Atlanta, April 1990
- LEOS Annual Meeting, Boston, November 5, 1990
- IEEE Computer Communications Workshop, October 1992
- IEEE Optical Fiber Communications Conference, February 1993
- OSA Optical Computing Topical Meeting, March 1993
- IEEEOSA Topical Meeting on Photonic Switching, March 1993
- IEEE LEOS Conference, November 1993
- Rank Prize Symposium, April 1994
- Workshop on Massively Parallel Processing using Optical Interconnects, April 1994
- Keynote Address, Viva a Ciencia, Symposium commemorating the 25th Anniversary of Submarine Cables in Portugal, October 1994
- IEEE Optical Fiber Communication Conference, February 1995
- European Fiber Optic Communication & Networking Conference, June 1995
- IEEE LEOS Conference, October 1995
- IEEE LEOS Conference, October 1996
- IEEE Computer Society, May 1996
- ECOC, September 1997
- IEEE LEOS, November 1997
- Sarnoff Symposium, March, 1998
- Rank Prize Symposium, April 1998
- ECOC, September 1998
- XI<sup>th</sup> Slovak/Czech/Polish Optical Conference on Wave and Quantum Aspects of Contemporary Optics, September 1998
- American Physical Society Annual Meeting, invited tutorial, March 2000
- American Physical Society Annual Meeting, Minneapolis, MN, March 2000
- CLEO/PR-2001, Makahuri Messe, Chiba, Japan, June 2001
- OSA Topical Meeting-Integrated Photonics Research, Vancouver, Canada, July 2002
- WOCC 2002, Newark, NJ, April 2002
- Photonics Prague 2002, Prague, Czech Republic, May 2002
- Europe-U.S.-Japan Symposium on Ultrafast Photonic Technology, Chiba, Japan, July 2003
- ECS'03 Bratislava, Slovakia, September 2003
- IEEE Photonics in Switching Topical Meeting, Versailles France, September, 2003

- "From Smoke Signals to All-Optical Communications," Given at University of Žilina, Žilina, Slovakia, October 24, 2005
- "RF Photonics," DSA, Holmdel, NJ, February 22, 2005
- "Reconfigurable universal transceivers," U.S. Army Communications Electronics Command, Fort Monmouth, NJ, March 11, 2005
- "All-optical signal processing; "Progress and applications," Distinguished speaker seminar series, University of Arizona, Tucson, AZ, April 15, 2005
- "Reconfigurable, asynchronous, incoherent optical CDMA networks, " O-CDMA PI Review, Key West, FL, May 2, 2005
- "All-optical signal processing; Progress and applications," Center for Communications Research, Princeton, NJ, May 18, 2005
- Plenary Lecture, "All-optical signal processing: Progress and applications," Ninth Canadian Workshop on Information Theory, McGill University, Montreal, June 6, 2005
- "Flexible access techniques for fiber-to-the-home," O-CDMA systems Workshop, Key West, FL, May 3-4, 2005
- "Advanced technology for next-generation networks," NJ Legislative Caucus on Science and Technology: Shaping New Jersey's Telecommunication Future, Princeton, May 20, 2005
- "All-optical signal processing: Progress and applications," Center for Computing Sciences, Bowie, MD, June 30, 2005.
- "Advanced optical signal processing techniques for communications and computing," NEC, Tamagawa Labs, Tokyo, August 24, 2005
- "All-optical signal processing: Challenges and applications," Tokyo University, August 25, 2005
- "All-optical signal processing: Challenges and applications," Chinese University of Hong Kong, August 26, 2005
- "All-optical signal processing: Challenges and applications," Tsinghua University, Beijing, August 31, 2005
- "All-optical signal processing: Challenges and applications," The Cooper Union, New York City, December 13, 2005
- Keynote Speaker at PRISM/NJCST Summit, May 20, 2005
- "Design of an avionics platform for Lockheed-Martin based on incoherent optical CDMA," Sarnoff Symposium, Princeton, NJ, March 27-28, 2006
- "How optics has changed data communications," 15<sup>th</sup> Czech-Slovak-Polish Optical Conference on Wave and Quantum Aspects of Contemporary Optics. Liberec, Czech Republic, September 11-15, 2006
- "The roll of optics in optical communications," 15<sup>th</sup> Czech-Slovak-Polish Optical Conference on Wave and Quantum Aspects of Contemporary Optics. Liberec, Czech Republic, September 11-15, 2006
- "OCDMA-an alternative for optical communications?" Optical Communications, OK 2005, Prague, Czech Republic, September 20-21, 2005
- "Is optical CDMA viable technique for broadband networks?," Photonics Prague 2005, Prague, Czech Republic, June 8-11, 2005
- "Reconfigurable asynchronous incoherent OCDMA", PI annual meeting, Chicago, IL August 2006

- Workshop on Optical and Wireless Communications Technologies & “*Princeton testbed for optical and wireless communications*”, PRISM – University-Industry Research Symposium, Princeton University, February 3, 2006
- Seminar of “*Effective Teaching Methods*”, McGraw Center, Princeton University, March 15, 2006
- “*All-Optical Signal Processing: Challenges and Applications*”, Universita Komenskeho, Bratislava, May 31, 2006
- All-Optical Signal Processing: Technologies for Network Applications, Polytechnic University, New York, NY, November 30, 2006
- All-Optical Signal Processing: Technologies for Network Applications, Globecom Access '06 Business Forum, San Francisco, November 29, 2006
- Concordia University, Montreal, Canada, 5<sup>th</sup> Workshop on Optimization of Optical Networks, May 8, 2008
- Princeton, NJ Workshop on Modeling and Analysis of Computer and Communication Networks, May 9, 2008
- Santa Fe, NM 2008 Workshop on Interconnections within High Speed Digital Systems. May 18-21, 2008
- Lockheed Martin, Cherry Hill, NJ Seminar presentation and research presentation. July 11, 2008
- St. Thomas, US Virgin Islands ICCCN 2008 August 3, 2008
- Baltimore, MD MIRTHER Summer Workshop, August 5, 2008
- College Park, MD Research seminar at Laboratory for Physical Sciences. October 1, 2008
- “Truly-Asynchronous, Scalable and Survivable Optical CDMA Networks with Heterogeneous QoS,” at the 2009 IEEE Lasers and Electro-Optics Society Summer Topical Meeting (LEOS), Newport Beach, CA, USA, July 20-22, 2009
- “Physical layer network security based on optical processing using compact passive devices,” OECC 2009, Hong Kong, July 2009.
- Invited panel member, “Quality of Service Performance and Switching Implementation in Optical Networks,” at AH-ICI2009, November 2009.
- “Undergraduate Studies and Research in Electrical Engineering at Princeton,” at The Lincoln School, Kathmandu, Nepal, November 2009.
- “Physical Layer Security in Data Networks using Optical Signal Processing,” 2009 ACP, Shanghai, China, November 2009.
- “*Photonic Neurons for Terahertz Pulse Processing*,” 9th International Conference on Optical Communications and Networks (ICOON 2010), Nanjing, China, October 24-27, 2010.
- “*Ultrafast optical processing and information security*,” L3 Communications Telemetry East, Bristol, PA, February 23, 2011.
- “*Ultrafast optical processing and information security*,” IEEE World Wide Security and Mobility Conference (WWSMC 2011), Princeton, NJ, July 27, 2011.
- “*Fiber optic networks technology tutorial*,” Center for Communication Research, La Jolla, CA, August 9, 2011.

- *"Lightwave neuromorphic signal processing,"* University of Delaware, Newark, DE, October 25, 2011.
- School of Engineering and Applied Science, Leadership Council Speaker, April 5, 2012.
- *"Using technology to protect our information infrastructure,"* The Lotus Club, April 27, 2012.
- *"Photonic Neuromorphic Signal Processing and Computing,"* 2012 International Workshop on Information Physics and Computing in Nano-scale Photonics and Materials (IPCN), Orleans, France, September 7, 2012
- *"Photonic neuromorphic spike processor for ultrafast and low energy cognitive computing,"* Bell Labs/Alcatel-Lucent Green ICT Summit, Murray Hill, NJ, USA, January 2013
- *"Photonic neuromorphic spike processing for ultrafast cognitive computing,"* IEEE North Jersey Section Computer Chapter and Signal Processing Chapter, Teaneck, NJ, USA, September 2013
- *"Integrated photonic spike processing,"* Sandia Labs Beyond Moore Device Physics Workshop, Albuquerque, NM, USA, January 2014
- *"Photonic spike processing,"* Neuro-Inspired Computational Elements Workshop, Albuquerque, NM, USA, February 2014
- *"Lightwave neuromorphic processing,"* AFCEA C4I Technology Review Days, Utica, NY, USA, June 2014
- European Conference Optical Communication (ECOC), Rome, Italy, September, 2018
- European Conference Optical Communication (ECOC), Brussels, Belgium, December 6, 2020
- *"Photonics for Neuromorphic Computing,"* 2021 IEEE Photonics Conference (IPC, formerly the IEEE LEOS Annual Meeting), Vancouver, Canada (October, 2021). Virtual.
- *"Silicon Neuromorphic Photonics,"* 26<sup>th</sup> OptoElectronics and Communications Conference (OECC) 2021, Hong Kong, (July, 2021). Virtual.

#### **Professional Societies:**

- Fellow of the IEEE (January, 1992)
- Fellow of the OSA (February, 1997)
- Fellow of the National Academy of Inventors (December, 2017)

#### **Academic Societies and Awards:**

- Phi Beta Kappa (Alpha of Maine Chapter, 1973)
- Citation for Outstanding Achievement, School of Engineering and Applied Science, Columbia University 1976)
- Eta Kappa Nu (Gamma Lambda Chapter, 1978)
- Sigma Xi (Kappa Chapter, 1979)
- Rudolf Kingslake Medal and Prize, SPIE, for the most noteworthy original paper in Optical Engineering, 1990
- Gold Medal Award from the Faculty of Mathematics, Physics and Informatics at the Comenius University, for leadership in the field of Optics 2006

- Princeton University Graduate Mentoring Award 2006
- E-Council Excellence in Teaching for ELE 203 Fall 2006
- E-Council Excellence in Teaching for ELE 454 Spring 2008
- Walter Curtis Johnson Prize for Teaching Excellence June 2009
- School of Engineering and Applied Science Distinguished Teacher Award, June 1, 2009
- Awards for undergraduate research in my lab:
  - Bryan Bosworth '09 received the Peter Mark Prize from the EE Department at Class Day, June 2009, for the "best undergraduate research" in the area of electronic materials and devices.
  - John Chang '10, J. Rich Steers Award from the New York City Post of the Society of American Military Engineers, December 2009
- Honored by Shirley Tilghman at the event "Celebrate Princeton Invention"
- CNSA selected by the National Security Agency as a "Center of Excellence in Research in Information Assurance." The award was presented in June at the NSA by Howard Schmidt, Obama's Cybersecurity Coordinator. This honor has just been highlighted in the news on the Princeton University webpage. <http://www.princeton.edu/main/news/archive/S29/01/99S63/index.xml?section=topstories>
- Awards for research in my lab:
  - John Chang, Graduate advisee, J. Rich Steers Award, February 5, 2010
  - Bhavin Shastri, PostDoc, IEEE Photonics Society 2011 Fellowship
  - Vinayak Venkataraman '11, recipient of 2011 John Ogden Bigelow Jr. Prize in Electrical Engineering
  - Mary Catherine Wen '11, recipient of 2011 Newport Research Undergraduate Award for Excellence in Photonics
- "Princeton named cyber security hub by National Security Agency," News at Princeton, November 22, 2010 and SEAS website, December 6, 2010
- "Fiber-optic photonic neurons to be developed in collaboration between Princeton University and Lockheed Martin," Laser Focus World Magazine, July 20, 2011
- "Photonic neuron may compute a billion times faster than brain circuits," Princeton University website, News at Princeton, July 18, 2011
- "For students, blazing fast lab work," Princeton Alumni Weekly Magazine, September 14, 2011, Vol. 112, No. 1
- 2012 Honoree, The Lotos Club, New York City
- Lifetime Achievement Award for Excellence in Teaching, awarded by the Princeton Engineering Council 2015
- The President's Award for Distinguished Teaching 2015
- Featured on November 18, 2016 in the MIT Technology Review, in an article titled "Silicon photonic neural network unveiled."  
Ref: [arxiv.org/abs/1611.02272](https://arxiv.org/abs/1611.02272): Neuromorphic Silicon Photonics
- Awards for research in my lab:
  - Lamia Ateshian: 2018 Optical Engineering Award, Princeton

- Alexander Tait: 2017 IEEE Photonics Society Graduate Student Fellowship
- Matthew Chang: 2016 CLEO pitch panel winner
- Alexander Tait: 2016 SEAS award for excellence
- Alexander Tait: 2016 IEEE Summer Topical Meeting Series Best Student Poster Award (first place).
- Mitchell Nahmias: 2015 IEEE Summer Topical Meeting Series Best Student Poster Award (first place).
- National Academy of Inventors (NAI) Fellow, December 2017.

#### Patents:

|     | Patent Number   | Issue Date | Title                                                                                                                            |
|-----|-----------------|------------|----------------------------------------------------------------------------------------------------------------------------------|
| 1.  | US 4,744,623    | 05/17/1988 | Integrated fiber optic coupler for VHSIC/VLSI interconnects                                                                      |
| 2.  | US 4,791,407    | 12/13/1988 | Alternate mark/space inversion line code                                                                                         |
| 3.  | US 4,887,879    | 12/19/1989 | Fiber optic tap                                                                                                                  |
| 4.  | US 5,060,305    | 10/22/1991 | Self clocked, self routed photonic switch                                                                                        |
| 5.  | US 5,073,980    | 12/17/1991 | Photonic Switch employing Shared data Transmission Facility                                                                      |
| 6.  | US 5,493,433    | 02/20/1996 | Terahertz Optical Asymmetric Demultiplexer                                                                                       |
| 7.  | US 5,825,519    | 10/20/1998 | Optical Mach-Zehnder Time Division Demultiplexer                                                                                 |
| 8.  | US 5,828,474    | 10/27/1998 | Optical Apparatus for Transmitting Data of an Electrical Signal                                                                  |
| 9.  | US 5,841,560    | 11/24/1998 | System for Optical Pulse Train Compression and Packet Generation                                                                 |
| 10. | US 5,917,979    | 06/29/1999 | Asymmetric Optical Loop Mirror Exhibiting Threshold Discrimination for Separation of Input Pulses of Differing Magnitudes        |
| 11. | US 6,265,999    | 07/24/2001 | High Speed Serial-to-Parallel Analog-to-Digital Conversion                                                                       |
| 12. | US 6,433,715 B2 | 08/13/2002 | High-Speed Serial-To-Parallel and Analog-to Digital Conversion                                                                   |
| 13. | US 6,448,913    | 09/10/2002 | Toad Based Optical Data Format Converter                                                                                         |
| 14. | US 6,535,662    | 03/18/2003 | TOAD Having Enhanced Extinction Ratio of the Switching Window                                                                    |
| 15. | US 7,035,550    | 04/25/2006 | All Optical 3R Regeneration using the Sagnac and Mach-Zehnder Versions of the Terahertz Optical Asymmetric Interferometer (TOAD) |
| 16. | US 7,068,894    | 06/27/2006 | An All-Optical Wavelength Converter Based on Sagnac Interferometer with an SOA at Asymmetric Position                            |
| 17. | US 8,315,489    | 11/20/2012 | Optical Sensor Array (AON)                                                                                                       |
| 18. | US 8,456,730    | 06/04/2013 | Directly modulated spatial light modulator (AON)                                                                                 |
| 19. | Israel 173226   | 03/01/2014 | All-Optical Wavelength Converter based on Sagnac Interferometer with an SOA at Asymmetric Position                               |
| 20. | US 8,682,170    | 03/25/2014 | System and Method for Broadband RF Interference Cancellation                                                                     |

|     |                        |            |                                                                                                    |
|-----|------------------------|------------|----------------------------------------------------------------------------------------------------|
| 21. | US 8,693,810           | 04/08/2014 | Optical Counter-Phase System and Method of RF Interference Cancellation                            |
| 22. | US 8,749,874           | 06/10/2014 | Optical Integration System and Method                                                              |
| 23. | US 8,917,960 B2        | 12/23/2014 | Optical Switch Using a Michelson Interferometer                                                    |
| 24. | US 9,344,125           | 05/17/2016 | Remote Interference Cancellation for Communications Systems (Bascom Hunter)                        |
| 25. | US 9,444,502           | 09/13/2016 | Interference Cancellation System for Cancelling Interference in the Optical Domain (Bascom Hunter) |
| 26. | US 9,571,205           | 02/14/2017 | Systems Approach to Interference Cancellation                                                      |
| 27. | US 9,838,125 B2        | 12/05/2017 | Multibeam Radio Frequency Photonic Beamformer Using a Multi-Signal Slow Light Time Delay Unit      |
| 28. | US 10,009,135          | 06/26/2018 | System and Method for Photonic Processing                                                          |
| 29. | Filed<br>US 62/664,386 | 4/30/2018  | Design of High Channel Count Two-Pole Photonic Microring Weight Banks                              |
| 30. | Filed<br>US 62/663,057 | 4/26/2018  | Excitable Laser Processor in a III-V Photonic Integrated Circuit Platform                          |
| 31. | Filed<br>US 62/647,393 | 3/23/2018  | Photonic Tensor Machine                                                                            |
| 32. | Filed<br>US 62/669,097 | 5/9/2018   | Photonic Circuit Total Laboratory Automation, Data Management and Virtualization                   |
| 33. | Filed<br>US 62/667,058 | 5/4/2018   | Method for Linear Analog Photonic Processing Using Mode Filters                                    |
| 34. | Filed<br>US 62/719,516 | 8/17/2018  | Feedback Control for Microring Weight Banks                                                        |
| 35. | Filed<br>US 62/690,393 | 6/27/2018  | Optically Accelerated FPGA                                                                         |
| 36. | Filed<br>US 62/690,425 | 6/27/2018  | Nonlinear Remodulation Unit with Electronic Amplification                                          |
| 37. | Filed<br>US 62/949,912 | 12/18/2019 | Organic Light-Emitting Diode Neuron                                                                |
| 38. | US 10,670,860          | 06/02/2020 | Design of High Channel Count Two-Pole Photonic Microring Weight Banks                              |
| 39. | Filed<br>US 63/045,660 | 06/29/2020 | Integrated Neuromorphic Computing System                                                           |
| 40. | Filed<br>US 63/045,720 | 06/29/2020 | Thin Film Neuromorphic Computing System                                                            |
| 41. | Filed<br>US 17/125,287 | 12/17/2020 | Light-Emitting Diode Neuron                                                                        |
| 42. | Filed<br>US 17/360,155 | 06/28/2021 | Integrated Neuromorphic Computing System                                                           |
| 43. | Filed<br>US 63/237,223 | 08/26/2021 | Real-time RF fingerprinting using continuous-time recurrent neural network algorithm on FPGA       |
| 44. | US 11,187,963          | 11/30/2021 | System and method for programmable nonlinear silicon photonic circuit                              |

**Patents: Invention Disclosures (2021):**

1. S. Bilodeau, T. Ferreira de Lima, E. A. Doris, M. Hack, P. R. Prucnal. "Stacked reconfigurable optical cavities for smart sensing pixels."
2. S. Bilodeau, T. Ferreira de Lima, E. A. Doris, M. Hack, P. R. Prucnal. "Transmission-mode interferometric modulator filter bank."
3. S. Bilodeau, T. Ferreira de Lima, E. A. Doris, M. Hack, P. R. Prucnal. "Compact, scalable thin film neuromorphic photonic system."
4. S. Bilodeau, T. Ferreira de Lima, E. A. Doris, M. Hack, P. R. Prucnal. "Thin film resonance cavity enhanced photodetector bank."
5. S. Bilodeau, T. Ferreira de Lima, E. A. Doris, M. Hack, P. R. Prucnal. "Thin-film absorption modulator filter bank."
6. E. A. Doris, S. Bilodeau, T. Ferreira de Lima, M. Hack, P. R. Prucnal. "Interleaved Time-Division-Multiplexing and Wavelength-Division-Multiplexing for Optically-Interconnected Neuromorphic Computing Platforms."
7. S. Bilodeau, T. Ferreira de Lima, E. A. Doris, M. Hack, P. R. Prucnal. "Photochemical optical cavity photonic memristor."
8. S. Bilodeau, T. Ferreira de Lima, E. A. Doris, M. Hack, P. R. Prucnal. "Thin-film optical memory actuation of emissive microcavity."

**Professional Activities:****Associate Editor:**

- IEEE Transaction on Communications, Area Editor, 1996 – present
- Proceedings of the IEEE, Review Editor, 1982-1985
- IEEE Circuits and Devices Magazine, 1988-1991
- IEEE Transactions on Communications, 1988-1996
- IEEE Lightwave Communications Magazine, 1989-1991
- Applied Optics, 1989-1994
- IEEE Networks Magazine, Special Issue on "Optical Multi-access Networks," 3, No. 2, March 1989 (Guest editor)
- Photonics Technology Letters, 1990-1991
- Photonic Network Communications, Kluwer Academic Publishers, Nowell, MA (Prof. Harmen R. van As, Vienna University of Technology, Editor), Editorial Advisory Board, 1996-
- Optical Fiber Technology, (Dr. Emmanuel Desurvire, Alcatel, Editor), Editorial Advisory Board, 1998-
- Journal of Lightwave Technology, Special Issue on "Photonic Packet Switching Technologies, Techniques and Systems", vol. 16, no. 12, December 1998, Guest Editor
- IEEE Journal of Selected Topics in Quantum Electronics, Primary Guest Editor, 2018

### **Program Committees:**

- IEEE/OSA Conference on Optical Fiber Communication, 1988
- IEEE/OSA Topical Meeting on Photonic Switching, 1989
- IEEE/OSA Conference on Lasers and Electro-optics, Subcommittee on Lightwave Communications, 1989
- IEEE/OSA Conference on Lasers and Electro-optics, Subcommittee on Optical Switching, Logic and Storage Systems, 1991
- IEEE/OSA Topical Meeting on Photonic Switching, 1991
- IEEE Princeton Section, Sarnoff Symposium, 1991
- OSA Regional Engineering Workshop, October 1991
- IEEE/OSA Topical Meeting on Optical Computing, 1993
- IEEE/OSA Topical Meeting on Photonics in Switching, 1993
- SPIE Conference on Multigigabit fiber communication systems, 1993
- IEEE (Princeton Section) Sarnoff Symposium, 1994
- IEEE/OSA Topical Meeting on Integrated Photonics Research, 1994
- IEEE Workshop on Massively Parallel Processing using Optical Interconnections, 1994
- ECOC'94, Photonics in Switching Joint Sessions, 1994
- ECOC'94, Florence, Italy, September 1994
- IEEE/OSA Integrated Photonics Research Topical Meeting, 1994
- IEEE/OSA MPPOI, 1995
- IEEE Princeton Central NJ Sarnoff Symposium, 1995
- IEEE/OSA Conference on Lasers and Electro optics, Subcommittee on Optical Switching, Logic and Storage Systems, 1995
- IEEE/OSA Topical Meeting on Photonic Switching, 1995
- IEEE/OSA Conference on Lasers and Electro optics, Subcommittee on Optical Switching, Logic and Storage Systems, 1996
- IEEE/OSA MPPOI, 1996
- IEEE/OSA MPPOI, 1998
- IEEE/OSA Conference on Optical Fiber Communication, 2000
- International Program Committee, IASTED international Conference on Communication, Internet and Information Technology, St. Thomas, USVI November 2006
- Organizer of upcoming PRISM/Complex Materials Center Workshop on "Optical and Wireless Communications"
- Optical Fiber Communications 2009
- 2010 IEEE Optical Fiber Communication and National Fiber Optic Engineers Conference (OFC/NFOEC), San Diego, CA, USA, March 21-25, 2010.
- Summer Topical Meeting on Terabit Optical Ethernet, Hilton Montreal Bonaventure, Montreal, Quebec, Canada, 18-20 July 2011.
- Second Asian Himalayan International Conference on the Internet and Next Generation of Mobile, Wireless and Optical Communication Networks, 2011.

- International Program Committee, International Conference on Communication, Internet, and Information Technology (CIIT 2012).
- Advisory and program committee on Information Physics and Computing in Nanoscale Photonics and Materials Workshop in 2012 Unconventional Computation and Natural Computation Conference
- Technical committee for ICSPCS 2016 (2016 10th International Conference on Signal Processing and Communication Systems - ICSPCS)
- 2019 IEEE Summer Topical, Committee, Fort Lauderdale, Florida, 8-10 July, 2019

**Conference or Subcommittee Chair:**

- IEEE Summer Topical Meeting on Optical Multiple Access Networks, July 1990, Technical Co-chair
- IEEE/OSA Conference on Lasers and Electrooptics, Technical Subcommittee on Optical Switching, Logic and Storage Systems, 1992
- IEEE/OSA Conference on Lasers and Electrooptics, Technical Subcommittee on Optical Switching, Logic and Storage Systems, 1993
- IEEE Globecom'93, Session 51 on "Optical communication network systems"
- SPIE Conference on High-Speed Optical Switching, Devices, Networks and Systems, Los Angeles, January 1994
- IEEE/OSA Photonics in Switching Topical Meeting, Sendai, Japan, North American Conference Chair, April 1996
- OSA Photonics in Switching Topical Meeting, Stockholm, Sweden, Conference Program Chair, March 1997
- OSA Photonics in Switching Topical Meeting, Santa Barbara, Conference General Chair, July 1999. Organizer and General Chair, "O-CDMA Systems Workshop" Key West, FL May 3-4, 2005
- CLEO/Europe-EQEC, Co-organizer of Joint Symposium, Munich, Germany, 23-27, June 2019
- European Conference Optical Communication (ECOC), Brussels, Belgium, Workshop Organizer and Co-Chair, "Pathway to bringing photonics into high-performance computing: from materials to applications," December 2020.

**Conference Session Presider:**

- 1996 Conference on Information Sciences and Systems, Session FP-2 "Optical Networks"
- The 3rd International Conference on Massively Parallel Processing "Using Optical Interconnects, Session III, "WDM in MPP Systems"
- Conference on Information Sciences and Systems, Session on "Optical Communications," Princeton, March 1988, 1994
- IEEE Workshop on Computer Communications, "Optical Networks and Photonic Switching," Harriman, September 1988

- IEEE/OSA Topical Meeting on Photonic Switching, Session on "Packet Switching," Salt Lake City, March 1989
- IEEE Communication Theory Workshop, Session on "Optical communication," Hawk's Cay, April 1989
- IEEE/OSA Conference on Lasers and Electro-optics, Session on "Optical multi-access techniques for multiuser communication systems," 1989
- International Workshop on Digital Communications, Session on "Optical multiaccess networks," Tirrenia, Italy, September 1989
- IEEE/OSA Topical Meeting on Photonic Switching, Session on Logic and Control, Salt Lake City, UT, March 1991
- OSA Annual Meeting, Session on "Integrated and Guided-Wave Optics," Boston, MA, November 1990
- IEEE Princeton Section Sarnoff Symposium, Session on Optoelectronic Systems Applications, 1991
- LEOS Summer Topic Meeting on Optical Multiple Access Networks, Session on "Packet Switching," 1992
- Conference on Information Sciences and Systems, Session TA-1 on "Optical Communications," Princeton, March 1994
- IEEE Workshop on Massively Parallel Processing using Optical Interconnections, Session III, 1994
- Sarnoff Symposium, Session on "Novel optical systems," April, 1995
- 32<sup>nd</sup> Annual Conference on Information Sciences and Systems, Session Chair, March, 1998

#### **Boards, Committees, Review Panels:**

- Columbia Radiation Laboratory, 1979-1988
- Columbia Bioengineering Institute, 1979-1988
- NSF Review Panel on Optical Communications, March 1987
- 9th International Conference on Computer Communications, Plenary Session, Tel Aviv, (October, 1988)
- Executive Board, NSF Engineering Research Center in Telecommunications, 1985-1988
- NSF Review Panel, "Research Experiences for Undergraduates Program," January 9-10, 1989
- Board of Directors, Edwin H. Armstrong Foundation, 1982-
- LEOS Steering Committee, Optical Switching and Processing, 1990-1995
- President's Committee on U.S.-Japan Joint Opto-Electronics Fabrication Project 1981
- NSF Panel on Optical Networks, January 1993
- IEEE LEOS Standing Technical Committee on Optical Communications, 1994
- External Review Panel, Fiber Optic Signal Processing for EWRadar Applications Naval Research Lab 6 Basic Research Program, Washington, DC. December 8, 1995
- IEEE LEOS Standing Technical Committee on "Optical interconnects and processing systems," 1995-1996

- POEM Executive Committee, 1991-
- Scientific Advisory Board, Epitaxial Lab Inc., Stony Brook, NY; Jie Piao, Pres., 1995-
- Scientific Advisory Board, Institute for Defense Analysis, Center for Computing Sciences, 1996-
- Editorial Board, "Photonic Network Communications Journal, Kluwer Academic Publishers, 1996-
- IEEE MPPOL'96 Panelist, "Intrasystem optical interconnects: performance, cost, functionality."
- Research Group for Optical Soliton Communications (ROSC, Japan), Foreign member ,1997-
- Executive Council, University League Nursery School 1995-1998 (Treasurer)
- Trustee, University League Nursery School, 1998-
- Board of Directors (President), Glen Homeowners Association, 1995
- Technical Advisory Boards: Alphion, Kailight Photonics, and Access Optical Networks, Inc.
- Princeton University Office of Intellectual Property – Member of Committee on Intellectual Property Rights, 2011
- Princeton University Phi Beta Kappa Selection Committee, 2012
- School of Engineering and Applied Science: Helen Shipley Hunt fund selection committee, 2012
- Princeton University Schmidt Fund Selection Committee, 2011-2012
- Chair of Princeton University Schmidt fund selection committee, 2012-2013
- Princeton University McGraw Center Writing Executive Committee, 2012
- Princeton University Committee of Seven, 2013
- Princeton University Dean of the Faculty's Committee on Online Education, 2012-2013
- Princeton Writing Program's Executive Committee, 7/1/2012 - 7/1/2016
- Princeton University Committee on Undergraduate Admission and Financial Aid, 2013-2016
- Natural Sciences and Engineering Research Council of Canada – Reviewer 2016
- Bascom Hunter Technologies, Board of Directors
- Access Optical Networks, Advisor, 2018-present
- Luminous Computing, Advisor, 2019-present
- Princeton University Writing Program Executive Committee, 2021
- Princeton University Committee on Intellectual Property and Technology Licensing, 2021
- Princeton University Phi Beta Kappa Committee, 2021
- Princeton University School of Engineering and Applied Sciences Director of the PRISM Center for Network Science and Applications, 2021
- Princeton University School of Engineering and Applied Sciences Andlinger Center, Associated Faculty Member (May, 2021)

- Princeton ECE Faculty representative to IEEE Student Chapter, 2021
- Princeton ECE Graduate Committee, 2021
- Princeton ECE OPT Faculty Coordinator
- Princeton ECE Sophomore Advisor, 2021

**Professional Societies:**

- IEEE (Student '75, Member '78, Senior Member '90, Fellow '92)
- Optical Society of America, Fellow 1997; SPIE
- National Academy of Inventors, Fellow, 2017

**Vice Chairman:**

- Princeton LEOS Chapter, 1990-1991

**Papers in conference proceedings based on peer review:**

1. Prucnal, P.R. (1980), "A new generalized performance measure for single-threshold optical communication systems," in Opt. Comm. Sys., Proceeding of the NSF Grantee-User Meeting on Optical Communication Systems, pp. 27-33.
2. Prucnal, P.R. (1981), "Detection and estimation in signal-dependent noise," in Opt. Comm. Sys., Proceeding of the NSF Grantee-User Meeting on Optical Communication Systems, pp. 103-108.
3. Prucnal, P.R. (1982), "Wideband FSK optical communications experiment," in Opt. Comm. Sys., Proceeding of the NSF Grantee-User Meeting on Optical Communication Systems, pp. 58-61.
4. Prucnal, P.R. and Fan, T.R. (1983), "Frequency-shift-key modulation for fiber-optic communication," in Opt. Comm. Sys., Proceeding of the NSF Grantee-User Meeting on Optical Communication Systems, pp. 79-86.
5. Prucnal, P.R., Santoro, M.A. and Lockwood, T. (1985), "Spread spectrum local area network using optical processing," Proceeding International Tirrenia Workshop on Digital Commun., 5.2.
6. Prucnal, P.R., Fossum, E.R. and Osgood, R.M. (1986), "Integrated fiber optic coupler for VLSI interconnects," Proceeding Soc. Photoopt. Inst. Eng., 625, pp. 154-158.
7. Prucnal, P.R. (1986), "VLSI fiber optic LAN," Proceeding Int. Opt. Comp. Conference, 700, pp. 230-238.
8. Prucnal, P.R. (1986), "All-optical ultra-fast networks," SPIE Proceeding Fiber Telecomm. and Comp. Net., 715, pp. 42-47.
9. Prucnal, P.R. (1986), "VLSI optical interconnection networks," SPIE Proceeding Integ. And Pack. Of Optoelec. Dev., 703, pp. 106-115.
10. Prucnal, P.R. (1986), "Spread spectrum fiber-optic LANs," Proceeding FOCLAN 86, pp. 101-108.
11. Aide, R.W., Harstead, E.E., Cacouris, T., Fossum, E.R., Prucnal, P.R., and Osgood, R.M. (1986), "Direct connection of optical fibers to integrated circuits," Proceeding Internat. Elect. Packaging Soc.
12. Prucnal, P.R., Blumenthal, D., Perrier, P.A. (1987), "Self-routing optical switch with optical processing," Topical Meeting on Photonic Switching, Tech. Digest Series, 13, (Optical Society of America, Washington, DC), pp. 42-44.

13. Prucnal, P.R. (1987), "All-optical micro-area networks," Proceeding International Work. On High-Speed Opt. Processes and Opto-elect. Dev. Based on Compound Semicond. E5.
14. Prucnal, P.R. (1987), "All-optical integrated circuit micro-area network," Proceeding 95th Amer. Soc. Eng. Educ. Annual Conference, p. 85.
15. Blumenthal, D.J., Prucnal, P.R., Thylen, L. and Granestrand, P. (1988), "Self-routing of 12.5 Gbps data through an 8x8 lithium niobate optical cross bar matrix with gigahertz switching speed," Opt. Fiber Communic. Conference, Tech. Digest, 1, (Optical Society of America, Washington, DC), p. 183.
16. Harstead, E.H., Elby, S.D. and Prucnal, P.R. (1988), "Low-loss high-impedance integrated fiber-optic tap," Opt. Fiber Communic. Conference, Tech. Digest, 1, (Optical Society of America, Washington, DC), p. 161.
17. Perrier, P.A. and Prucnal, P.R. (1988), "Optical self-routing of 12.5 Gbps time-division-multiplexed data," Conference on Lasers and Electroopt. Tech. Digest Series, 7 (Optical Society of America, Washington, DC), pp. 74-75.
18. Prucnal, P.R. (1988), "Ultra fast fiber-optic networks using all-optical processing," IEEE International Conference on Communications, Conference Record, #3, (IEEE Press, NJ), pp. 1485-1489.
19. Prucnal, P.R. (1988), "Self-routing photonic switch with optical processing," Proceeding Franco-American Workshop on New Research Directions in Integrated Networks, p. 23.
20. Elby, S.E. and Prucnal, P.R. (1988), "Fiber-optic interconnect devices for VLSI micro-area networks," Proceeding Soc. Photoopt. Inst. Eng., (SPIE, Bellingham, WA), 994, pp. 77-91.
21. Prucnal, P.R. and Perrier, P.A. (1988), "Demonstration of a high-dimensionality local area network photonic switch," Proceeding 14th European Conference on Opt.Communic., 292, #1 (IEE, London), pp. 264-267.
22. Prucnal, P.R. and Perrier, P.A. (1988), "Optical self-routing in a self-clocked photonic switch using pulse-interval encoding," Proceeding 14th European Conference on Opt. Communic., 292, #1 (IEE, London), pp. 259-263.
23. Perrier, P.A. and Prucnal, P.R. (1988), "Demonstration of high-dimensionality optical local area network switch," Optical Society of America, Tech. Digest Series, #11, (Optical Society of America, Washington, DC), p. 79.
24. Perrier, P.A. and Prucnal, P.R. (1988), "Self-synchronizing pulse-interval technique for optical routing control in a photonic switch," Optical Society of America, Tech. Digest Series, 11, (Optical Society of America, Washington, DC), p. 51.
25. Prucnal, P.R. and Perrier, P.A. (1988), "A new direction in photonic switching," Proceeding 9th International Conference on Comp. Communic., (North Holland, NY), pp. 149-154.
26. Maguire, G.Q. and Prucnal, P.R. (1989), "High-density optical storage using optical delay lines," Proceeding Soc. Photoopt. Inst. Eng. Conference on Medical Imaging, in press.
27. Perrier, P.A., Prucnal, P.R. and Chbat, M.W. (1989), "Demonstration of a self-clocked optical time-slot interchanger," Topical Meeting on Photonic

- Switching, Tech. Digest Series, (Optical Society of America, Washington, DC), FC3, pp. 139-141.
28. Prucnal, P.R. (1989), "A new direction in photonic switching, Topical Meeting on Photonic Switching, Tech. Digest Series, (Optical Society of America, Washington, DC), p. 7.
  29. Prucnal, P.R., Perrier, P.A., and Chbat, M.W. (1989), "Self-clocked optical time-division switch," Proceeding Conference Lasers and Electro-opt., 11, (Optical Society of America, Washington, DC), p. FG3, pp.398-399.
  30. Cho, H. and Prucnal, P.R. (1989), "Parameter optimization of GaAsAlGaA multiple-quantum-well electro absorption modulators," Proceeding Conference Lasers and Electro-opt., 11, (Optical Society of America, Washington, DC), p. TuJ38.
  31. Prucnal, P.R. and Perrier, P.A. (1989), "Optical interconnect switch," Proceeding Soc. Photoopt. Inst. Eng. 1178, (SPIE, Bellingham, WA), 162-170.
  32. Kwong, W.C., Prucnal, P.R. and Perrier, P.A. (1989), "Synchronous versus asynchronous CDMA for fiber-optic LANs using optical signal processing," Proceeding Globecom, 28, pp. 1012-1016.
  33. Prucnal, P.R. and Perrier, P.A. (1989), "Demonstration of a high-dimensionality space-division photonic switch," Proceeding Electrochem. Soc.
  34. Goel, K.K., Perrier, P.A., Prucnal, P.R., Milbrodt, M.A., Desurvire, E. (1989), "Optical self-routing through a tree-structured space-division photonic switch using pulse-interval binary encoding," Optical Society of America Tech. Digest Series, 12 (Optical Society of America, Washington, DC), p. 48.
  35. Prucnal, P.R., Perrier, P.A. and Kwong, W.C. (1989), "Synchronous CDMA for fiber-optic LANs using optical signal processing," Proceeding Inter. Conference on Integrated Opt. and Opt. Fiber Communic., poster.
  36. Prucnal, P.R. (1989), "An optical interconnect switch," Proceeding Materials Res. Soc., 354.
  37. Prucnal, P.R. (1990), "Passive shared-media systems," Proceeding IEEE International Conference on Communications, pp. 1135-1139.
  38. Kwong, W.C. and Prucnal, P.R. (1990), "Continuous phase FSK direct detection FDMA lightwave network with laser phase noise immunity," Proceedings of 1990 CISS, Princeton University, Princeton, NJ, 883-888.
  39. Perrier, P.A., Chbat, M.W. and Prucnal, P.R. (1990), "Optical clock recovery for high-speed optical networks," in Digest of LEOS Summer Topical on Optical Multiple Access Networks (IEEE, New York, NY), paper OMF12, pp. 73-74.
  40. Kwong, W.C. and Prucnal, P.R. (1990), "Theory on multichannel CPFSK lightwave networks with laser phase noise immunity," Technical Digest on Optical Multiple Access Networks, LEOS, Summer Topical Meeting '90, IEEE 90TH0306-1, Library of Congress 90-82546, pp. 66-67.
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