

UNITED STATES PROVISIONAL APPLICATION

For

EFFICIENT RECEIVER PROCESS PIPELINING

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EFFICIENT RECEIVER PROCESS PIPELINING

BACKGROUND

Various embodiments generally may relate to the field of wireless communications.

DETAILED DESCRIPTION

The following detailed description refers to the accompanying drawings. The same reference numbers may be used in different drawings to identify the same or similar elements. In the following description, for purposes of explanation and not limitation, specific details are set forth such as particular structures, architectures, interfaces, techniques, etc. in order to provide a thorough understanding of the various aspects of various embodiments. However, it will be apparent to those skilled in the art having the benefit of the present disclosure that the various aspects of the various embodiments may be practiced in other examples that depart from these specific details. In certain instances, descriptions of well-known devices, circuits, and methods are omitted so as not to obscure the description of the various embodiments with unnecessary detail.

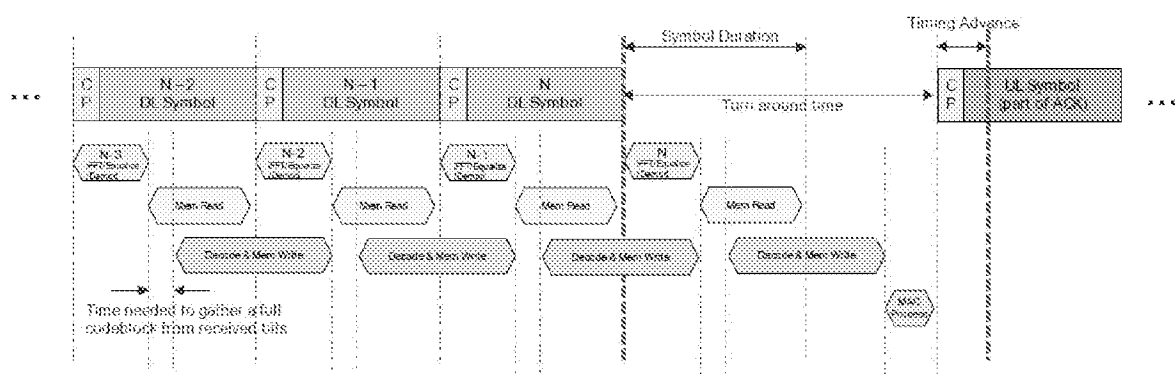
Various embodiments may enable encoded information to be segmented into multiple codeblocks and map a group of codeblocks to be aligned with Orthogonal Frequency Division Multiplexing (OFDM) symbol boundaries such that efficient receiver processing utilizing processing pipelining can be implemented.

In various embodiments, codeblocks may be grouped within a transport block, and a OFDM symbol boundaries may be aligned for each group of codeblocks.

By grouping the codeblocks, the receiver can efficiently process the received information. Furthermore, addition of cyclic redundancy check (CRC) per group of codeblocks allow the receiver to report back acknowledgement with more fidelity.

After data signal is received, the device typically has certain amount of time to perform demodulation and decoding to verify the correctness of the received bits and send acknowledgement (ACK) of the correctly received bits. The time between end of data signal and transmission of acknowledgement is the turnaround time.

Improving turnaround time (i.e. reducing) between received data channel and uplink ACK feedback is desired. It is a complex trade-off between chip area penalty versus additional required processing time (i.e. turnaround time). Turnaround time will typically include Inverse Fast Fourier Transform (IFFT), phase/amplitude compensation, Equalization, [Interleaving], channel code decoding (e.g. LDPC decoding), Media Access Control (MAC) layer processing, and/or transmit preparation. For a given hardware design, receiver may be able to process higher data rates per slot with larger turnaround time. Basically a trade-off between processing time vs. supported rate. Of course, supported memory size and memory access interface design will also impact processing time, which makes the trade-off complicated.



Note: Many functionality & functional blocks are omitted/simplified in the above diagram

Figure 1

Figure 1 is an example of pipelined processing of received data signal and transmission of ACK. Assuming total of N OFDM symbols for data, the receiver can start the processing of # $N-3$ symbol after complete reception of # $N-3$ symbol. The receiver performs inverse FFT, equalization, demodulation, and de-interleaving (if needed). The decoder reads the demodulated received bits for decoding process. Transmit information is usually segmented into codeblocks, where each codeblock is decoded separately. Therefore, the decoder has to read enough bits (or log-likelihood ratios (LLRs)) of a codeblock for it to start decoding process.

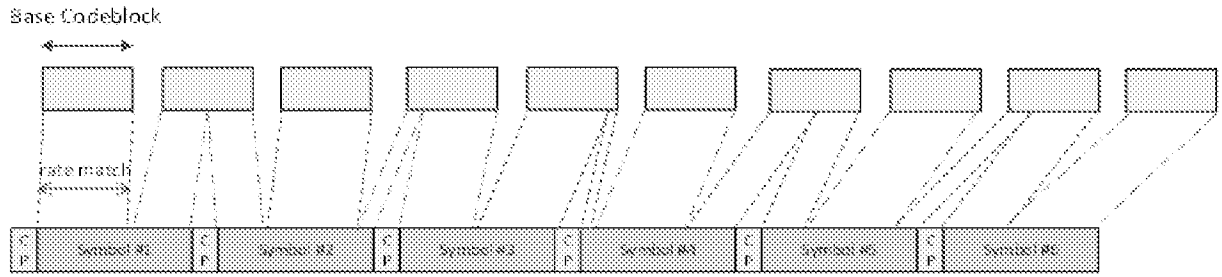


Figure 2

At the transmitter information bit sequence is segmented into sub-blocks. Each sub-block is encoded (e.g. Low-Density Parity Check (LDPC)) and turned into base coded sub-block. Base coded sub-block is the encoded information bits of a segmented information bits that is not rate matched. It may correspond to a mother code rate of the encoder (e.g. LDPC). After rate matching a base coded sub-block, rate-matched base coded sub-blocks are obtained and these are mapped to available resources in the assigned OFDM symbols. An example is shown in Figure 2.

The problem is that size of the rate-matched coded sub-block and the allocated resource elements of a OFDM symbol is not typically identical, and therefore it can lead to non-integer numbers of codeblock mapping per OFDM symbol.

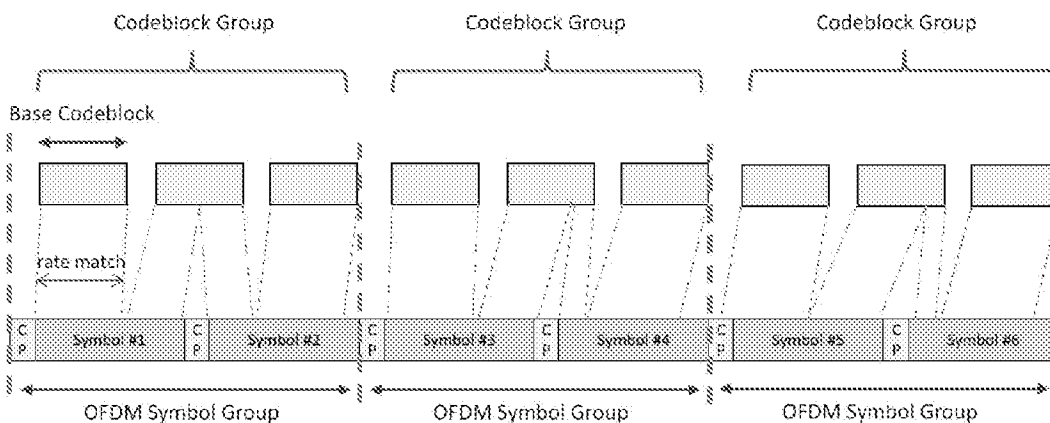


Figure 3

In various embodiments, N codeblocks, called codeblock group, may be aligned to M OFDM symbols, called OFDM symbol group. An example is shown in Figure 3. In one example, N and M can be 1. This results in single codeblock mapped to a single OFDM symbol. An integer number of codeblock mapping to a group of OFDM symbols, allows efficient pipelined process at the receiver. Furthermore, each group of codeblocks can be associated with an acknowledgement bit. This results in multiple acknowledgement bits per transport block when the transport block have multiple group of codeblocks. It may be also possible to have different number of codeblocks in the codeblock group and/or different code block size per code block group and/or each code block in each code block group may have distinct size. For example, a transport block may have three code block groups CBG0, CBG1, CBG2, wherein code blocks CB0,CB1 are in CBG1, CB2,CB3,CB4,CB5,CB6 are in CBG1, and CB7-CB13 are in CBG2.

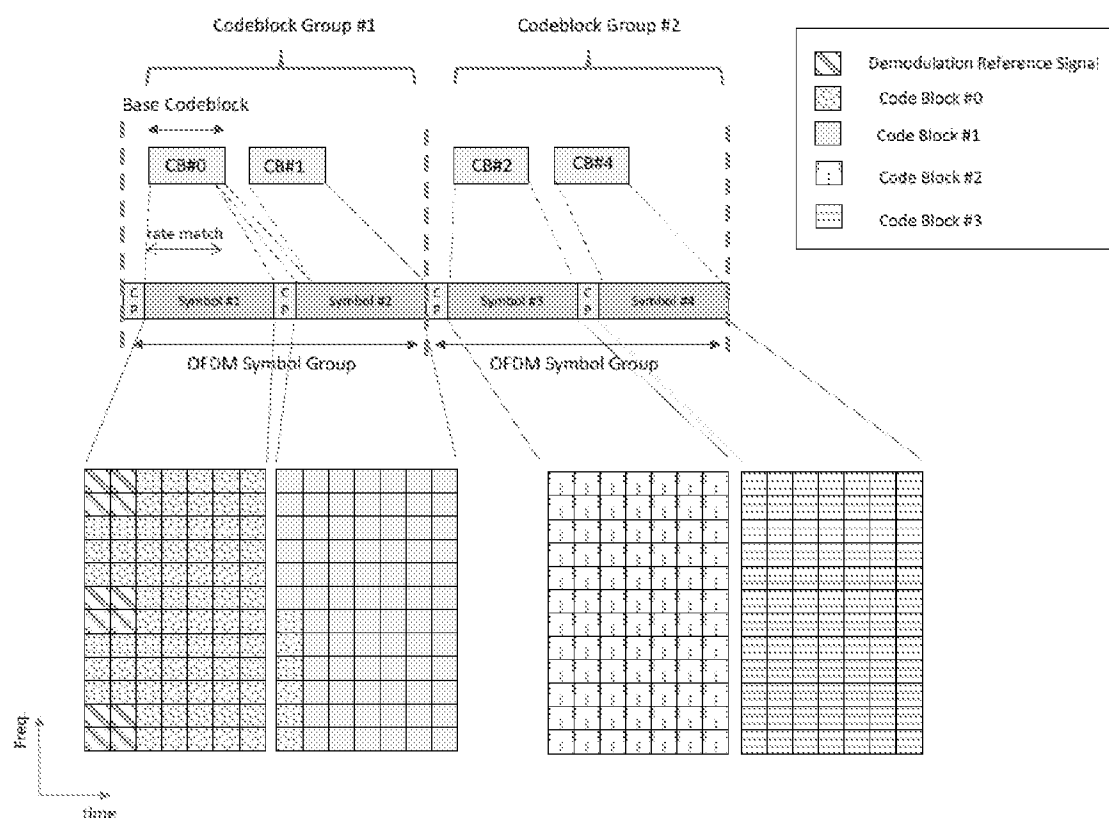


Figure 4

Each OFDM symbol of the allocated data transmission, may have different number of available resource elements (REs) for data transmission. If the codeblock group is rate matched to always fit into M OFDM symbols, different codeblock groups may end up with different code-

rates. This may result in different link performance. An example of different OFDM symbols containing different number of allocated REs is shown in Figure 4. In the example, the second codeblock group is sent over more REs compared with the first codeblock group.

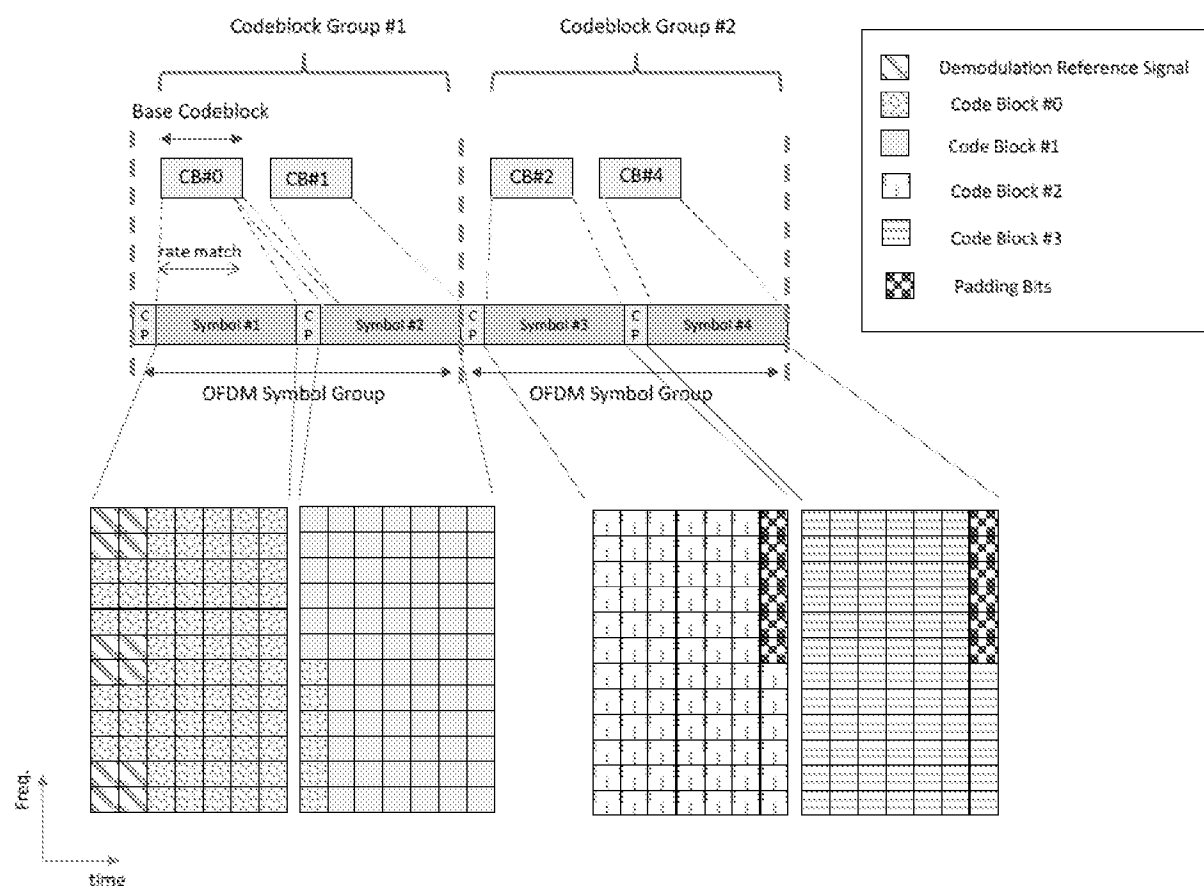


Figure 5

To avoid variable code rate within the transport block, bit padding can be used such that each codeblock groups have similar effective code-rates. The bit padding can be done prior to the encoding, where known bit sequences (or bit sequences that could be computed from received and decoded bits prior to padding) are used for padding. Alternatively, bit padding can be done after encoding and rate matching. The padded bits can be inserted in front or at the end of each codeblock or inserted in the front of end of the codeblock group. An example of padding is shown in Figure 5. Another option is to use repetition instead of padding. Within a code block group, there may be further segmentation to align code blocks to the OFDM symbol boundaries as well.

An alternative technique to avoid variable code rate within the transport block includes performing non-equal size information payload segmentation. For example, if the first codeblock group has smaller REs compared with the second codeblock group, the information bits that are segmented to the first codeblock group may be smaller than the second codeblock group. For e.g. if codeblock group 1 (CBG1) has 1 CB and 960 REs, and CBG2 has 2 CBs and 1000 REs/CB, and transmission is performed using modulation coding scheme (MCS) of $\frac{1}{2}$ code rate and Quadrature Phase Shift Keying (QPSK) modulation, and transport block size (TBS) is 2960 bits, codeblock segmentation of the transport block can be 960 for the first CB1, 1000 for CB2 and CB3. The segmentation can will use the modulation order and code rate to determine the segmentation size for each segment.

The determination of the codeblock group size and the OFDM symbol group size can be determined by the receiver capability and signaled by control signals. Configurable code block segmentation may also be used, wherein the code block segmentation applied on a particular transmission (for a transport block or a service) or a link (e.g. downlink/uplink) can be explicitly configured e.g. by a network entity such as a base station. Thus, the configurable segmentation enables allows segmentation to support a fast pipelined operation in case of low-latency/fast turn-around, while it can also support an operation where balanced performance (across all code blocks) is targeted with a somewhat relaxed processing requirement.

The number of code block groups may be configured via higher layer or physical layer signaling. In some embodiments, the number of code block groups may be associated with the configuration of a slot duration and a number of subslots associated with a single slot duration.

Because acknowledgements can be generated for each codeblock group, it may be possible for the transmitter to omit the transmission of a codeblock group and transmit data signals for another receiver that requires much more urgent data delivery. It also allows a transmitter to omit retransmission of a code block group that is already successfully received by the receiver.

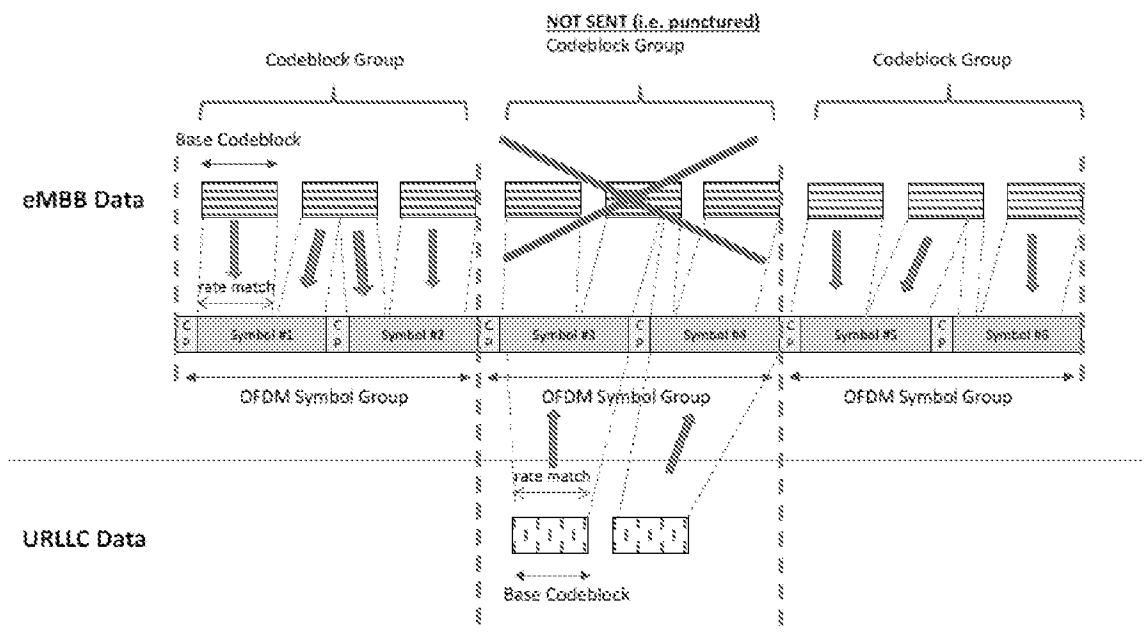


Figure 6

The omission of such codeblock group can be signaled by the transmitter. One example of the signaling is done in the padding bits of the codeblock group prior to the codeblock group omission. An example is shown in Figure 6.

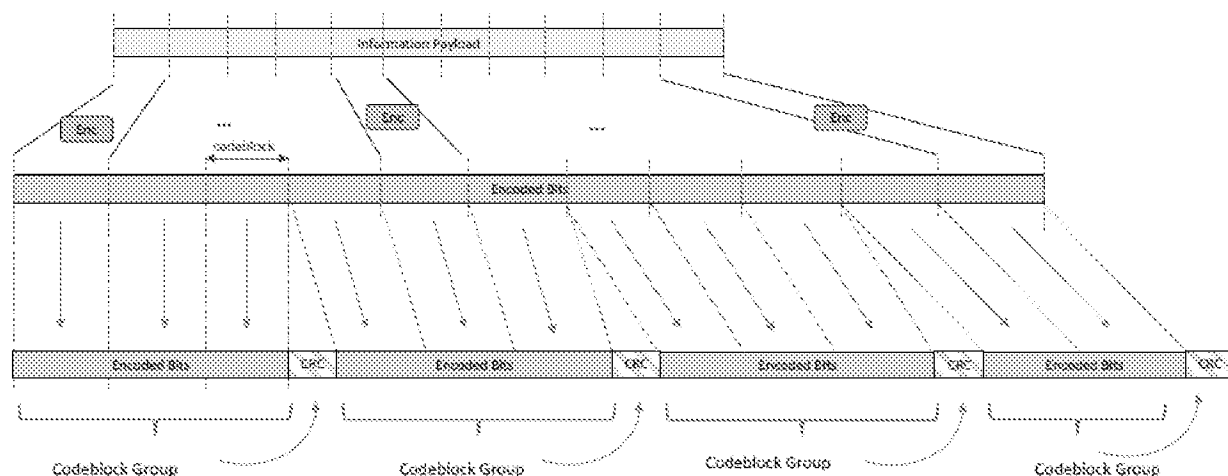
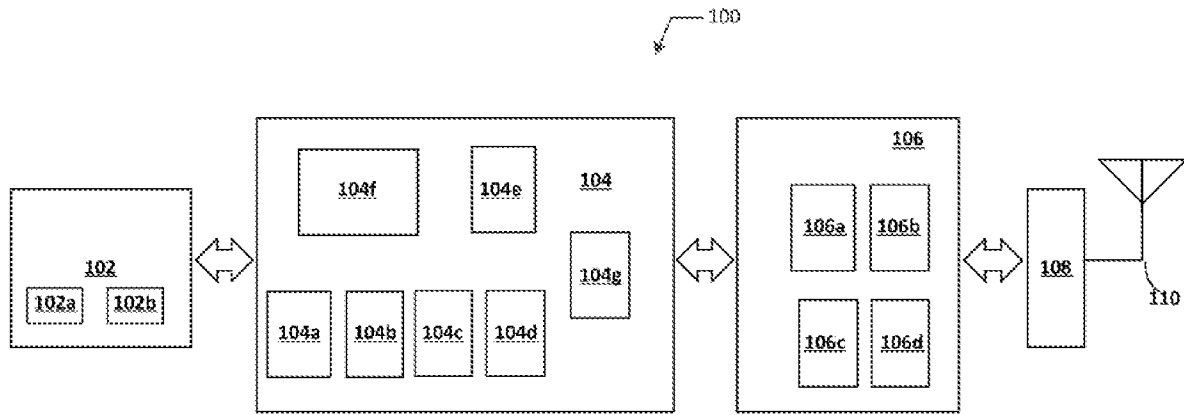


Figure 7

Alternatively, the omission of the codeblock group by the receiver can be done by checking the CRC of the information bits of the codeblock group. The transmitter computes the CRC of each codeblock group and appends the CRC bits to the end of the bits corresponding to the codeblock group prior to encoding. An example of this is shown in Figure 7.

**Figure X-1**

As used herein, the term "circuitry" may refer to, be part of, or include an Application Specific Integrated Circuit (ASIC), an electronic circuit, a processor (shared, dedicated, or group), and/or memory (shared, dedicated, or group) that execute one or more software or firmware programs, a combinational logic circuit, and/or other suitable hardware components that provide the described functionality. In some embodiments, the circuitry may be implemented in, or functions associated with the circuitry may be implemented by, one or more software or firmware modules. In some embodiments, circuitry may include logic, at least partially operable in hardware.

Embodiments described herein may be implemented into a system using any suitably configured hardware and/or software. Figure X-1 illustrates, for one embodiment, example components of an electronic device 100. In embodiments, the electronic device 100 may be, implement, be incorporated into, or otherwise be a part of a user equipment (UE), an evolved NodeB (eNB), or some other device. In some embodiments, the electronic device 100 may include application circuitry 102, baseband circuitry 104, Radio Frequency (RF) circuitry 106, front-end module (FEM) circuitry 108 and one or more antennas 110, coupled together at least as shown. In embodiments where the electronic device 100 is implemented in or by an eNB, the electronic device 100 may also include network interface circuitry (not shown) for

communicating over a wired interface (for example, an X2 interface, an S1 interface, and the like).

The application circuitry 102 may include one or more application processors. For example, the application circuitry 102 may include circuitry such as, but not limited to, one or more single-core or multi-core processors 102a. The processor(s) 102a may include any combination of general-purpose processors and dedicated processors (e.g., graphics processors, application processors, etc.). The processors 102a may be coupled with and/or may include computer-readable media 102b (also referred to as “CRM 102b”, “memory 102b”, “storage 102b”, or “memory/storage 102b”) and may be configured to execute instructions stored in the CRM 102b to enable various applications and/or operating systems to run on the system.

The baseband circuitry 104 may include circuitry such as, but not limited to, one or more single-core or multi-core processors. The baseband circuitry 104 may include one or more baseband processors and/or control logic to process baseband signals received from a receive signal path of the RF circuitry 106 and to generate baseband signals for a transmit signal path of the RF circuitry 106. Baseband circuitry 104 may interface with the application circuitry 102 for generation and processing of the baseband signals and for controlling operations of the RF circuitry 106. For example, in some embodiments, the baseband circuitry 104 may include a second generation (2G) baseband processor 104a, third generation (3G) baseband processor 104b, fourth generation (4G) baseband processor 104c, and/or other baseband processor(s) 104d for other existing generations, generations in development or to be developed in the future (e.g., fifth generation (5G), 6G, etc.). The baseband circuitry 104 (e.g., one or more of baseband processors 104a-d) may handle various radio control functions that enable communication with one or more radio networks via the RF circuitry 106. The radio control functions may include, but are not limited to, signal modulation/demodulation, encoding/decoding, radio frequency shifting, and the like. In some embodiments, modulation/demodulation circuitry of the baseband circuitry 104 may include Fast-Fourier Transform (FFT), precoding, and/or constellation mapping/demapping functionality. In some embodiments, encoding/decoding circuitry of the baseband circuitry 104 may include convolution, tail-biting convolution, turbo, Viterbi, and/or Low Density Parity Check (LDPC) encoder/decoder functionality. Embodiments of modulation/demodulation and encoder/decoder functionality are not limited to these examples and may include other suitable functionality in other embodiments.

In some embodiments, the baseband circuitry 104 may include elements of a protocol stack such as, for example, elements of an evolved universal terrestrial radio access network (E-UTRAN) protocol including, for example, physical (PHY), media access control (MAC), radio link control (RLC), packet data convergence protocol (PDCP), and/or radio resource control (RRC) elements. A central processing unit (CPU) 104e of the baseband circuitry 104 may be configured to run elements of the protocol stack for signaling of the PHY, MAC, RLC, PDCP and/or RRC layers. In some embodiments, the baseband circuitry may include one or more audio digital signal processor(s) (DSP) 104f. The audio DSP(s) 104f may include elements for compression/decompression and echo cancellation and may include other suitable processing elements in other embodiments. The baseband circuitry 104 may further include computer-readable media 104g (also referred to as “CRM 104g”, “memory 104g”, “storage 104g”, or “CRM 104g”). The CRM 104g may be used to load and store data and/or instructions for operations performed by the processors of the baseband circuitry 104. CRM 104g for one embodiment may include any combination of suitable volatile memory and/or non-volatile memory. The CRM 104g may include any combination of various levels of memory/storage including, but not limited to, read-only memory (ROM) having embedded software instructions (e.g., firmware), random access memory (e.g., dynamic random access memory (DRAM)), cache, buffers, etc.). The CRM 104g may be shared among the various processors or dedicated to particular processors. Components of the baseband circuitry 104 may be suitably combined in a single chip, a single chipset, or disposed on a same circuit board in some embodiments. In some embodiments, some or all of the constituent components of the baseband circuitry 104 and the application circuitry 102 may be implemented together, such as, for example, on a system on a chip (SOC).

In some embodiments, the baseband circuitry 104 may provide for communication compatible with one or more radio technologies. For example, in some embodiments, the baseband circuitry 104 may support communication with an E-UTRAN and/or other wireless metropolitan area networks (WMAN), a wireless local area network (WLAN), a wireless personal area network (WPAN). Embodiments in which the baseband circuitry 104 is configured to support radio communications of more than one wireless protocol may be referred to as multi-mode baseband circuitry.

RF circuitry 106 may enable communication with wireless networks using modulated electromagnetic radiation through a non-solid medium. In various embodiments, the RF circuitry 106 may include switches, filters, amplifiers, etc., to facilitate the communication with the wireless network. RF circuitry 106 may include a receive signal path that may include circuitry to down-convert RF signals received from the FEM circuitry 108 and provide baseband signals to the baseband circuitry 104. RF circuitry 106 may also include a transmit signal path that may include circuitry to up-convert baseband signals provided by the baseband circuitry 104 and provide RF output signals to the FEM circuitry 108 for transmission.

In some embodiments, the RF circuitry 106 may include a receive signal path and a transmit signal path. The receive signal path of the RF circuitry 106 may include mixer circuitry 106a, amplifier circuitry 106b and filter circuitry 106c. The transmit signal path of the RF circuitry 106 may include filter circuitry 106c and mixer circuitry 106a. RF circuitry 106 may also include synthesizer circuitry 106d for synthesizing a frequency for use by the mixer circuitry 106a of the receive signal path and the transmit signal path. In some embodiments, the mixer circuitry 106a of the receive signal path may be configured to down-convert RF signals received from the FEM circuitry 108 based on the synthesized frequency provided by synthesizer circuitry 106d. The amplifier circuitry 106b may be configured to amplify the down-converted signals and the filter circuitry 106c may be a low-pass filter (LPF) or band-pass filter (BPF) configured to remove unwanted signals from the down-converted signals to generate output baseband signals. Output baseband signals may be provided to the baseband circuitry 104 for further processing. In some embodiments, the output baseband signals may be zero-frequency baseband signals, although this is not a requirement. In some embodiments, mixer circuitry 106a of the receive signal path may comprise passive mixers, although the scope of the embodiments is not limited in this respect.

In some embodiments, the mixer circuitry 106a of the transmit signal path may be configured to up-convert input baseband signals based on the synthesized frequency provided by the synthesizer circuitry 106d to generate RF output signals for the FEM circuitry 108. The baseband signals may be provided by the baseband circuitry 104 and may be filtered by filter circuitry 106c. The filter circuitry 106c may include a low-pass filter (LPF), although the scope of the embodiments is not limited in this respect.

In some embodiments, the mixer circuitry 106a of the receive signal path and the mixer circuitry 106a of the transmit signal path may include two or more mixers and may be arranged for quadrature downconversion and/or upconversion, respectively. In some embodiments, the mixer circuitry 106a of the receive signal path and the mixer circuitry 106a of the transmit signal path may include two or more mixers and may be arranged for image rejection (e.g., Hartley image rejection). In some embodiments, the mixer circuitry 106a of the receive signal path and the mixer circuitry 106a of the transmit signal path may be arranged for direct downconversion and/or direct upconversion, respectively. In some embodiments, the mixer circuitry 106a of the receive signal path and the mixer circuitry 106a of the transmit signal path may be configured for super-heterodyne operation.

In some embodiments, the output baseband signals and the input baseband signals may be analog baseband signals, although the scope of the embodiments is not limited in this respect. In some alternate embodiments, the output baseband signals and the input baseband signals may be digital baseband signals. In these alternate embodiments, the RF circuitry 106 may include analog-to-digital converter (ADC) and digital-to-analog converter (DAC) circuitry and the baseband circuitry 104 may include a digital baseband interface to communicate with the RF circuitry 106.

In some dual-mode embodiments, a separate radio IC circuitry may be provided for processing signals for each spectrum, although the scope of the embodiments is not limited in this respect.

In some embodiments, the synthesizer circuitry 106d may be a fractional-N synthesizer or a fractional $N/N+1$ synthesizer, although the scope of the embodiments is not limited in this respect, as other types of frequency synthesizers may be suitable. For example, synthesizer circuitry 106d may be a delta-sigma synthesizer, a frequency multiplier, or a synthesizer comprising a phase-locked loop with a frequency divider. The synthesizer circuitry 106d may be configured to synthesize an output frequency for use by the mixer circuitry 106a of the RF circuitry 106 based on a frequency input and a divider control input. In some embodiments, the synthesizer circuitry 106d may be a fractional $N/N+1$ synthesizer.

In some embodiments, frequency input may be provided by a voltage controlled oscillator (VCO), although that is not a requirement. Divider control input may be provided by either the baseband circuitry 104 or the application circuitry 102 depending on the desired output

frequency. In some embodiments, a divider control input (e.g., N) may be determined from a look-up table based on a channel indicated by the application circuitry 102.

Synthesizer circuitry 106d of the RF circuitry 106 may include a divider, a delay-locked loop (DLL), a multiplexer and a phase accumulator. In some embodiments, the divider may be a dual modulus divider (DMD) and the phase accumulator may be a digital phase accumulator (DPA). In some embodiments, the DMD may be configured to divide the input signal by either N or $N+1$ (e.g., based on a carry out) to provide a fractional division ratio. In some example embodiments, the DLL may include a set of cascaded, tunable, delay elements, a phase detector, a charge pump and a D-type flip-flop. In these embodiments, the delay elements may be configured to break a VCO period up into N_d equal packets of phase, where N_d is the number of delay elements in the delay line. In this way, the DLL provides negative feedback to help ensure that the total delay through the delay line is one VCO cycle.

In some embodiments, synthesizer circuitry 106d may be configured to generate a carrier frequency as the output frequency, while in other embodiments, the output frequency may be a multiple of the carrier frequency (e.g., twice the carrier frequency, four times the carrier frequency) and used in conjunction with quadrature generator and divider circuitry to generate multiple signals at the carrier frequency with multiple different phases with respect to each other. In some embodiments, the output frequency may be a LO frequency (f_{LO}). In some embodiments, the RF circuitry 106 may include an IQ/polar converter.

FEM circuitry 108 may include a receive signal path that may include circuitry configured to operate on RF signals received from one or more antennas 110, amplify the received signals and provide the amplified versions of the received signals to the RF circuitry 106 for further processing. FEM circuitry 108 may also include a transmit signal path that may include circuitry configured to amplify signals for transmission provided by the RF circuitry 106 for transmission by one or more of the one or more antennas 110. In some embodiments, the FEM circuitry 108 may include a TX/RX switch to switch between transmit mode and receive mode operation. The FEM circuitry 108 may include a receive signal path and a transmit signal path. The receive signal path of the FEM circuitry may include a low-noise amplifier (LNA) to amplify received RF signals and provide the amplified received RF signals as an output (e.g., to the RF circuitry 106). The transmit signal path of the FEM circuitry 108 may include a power amplifier (PA) to amplify input RF signals (e.g., provided by RF circuitry 106), and one or more

filters to generate RF signals for subsequent transmission (e.g., by one or more of the one or more antennas 110).

In some embodiments, the electronic device 100 may include additional elements such as, for example, a display, a camera, one or more sensors, and/or interface circuitry (for example, input/output (I/O) interfaces or buses) (not shown). In embodiments where the electronic device is implemented in or by an eNB, the electronic device 100 may include network interface circuitry. The network interface circuitry may be one or more computer hardware components that connect electronic device 100 to one or more network elements, such as one or more servers within a core network or one or more other eNBs via a wired connection. To this end, the network interface circuitry may include one or more dedicated processors and/or field programmable gate arrays (FPGAs) to communicate using one or more network communications protocols such as X2 application protocol (AP), S1 AP, Stream Control Transmission Protocol (SCTP), Ethernet, Point-to-Point (PPP), Fiber Distributed Data Interface (FDDI), and/or any other suitable network communications protocols.

In embodiments, the device of Figure X-1 may include circuitry to identify a plurality of collections of codeblocks and to generate an association between collections of the plurality of collections of codeblocks to respective OFDM symbols.

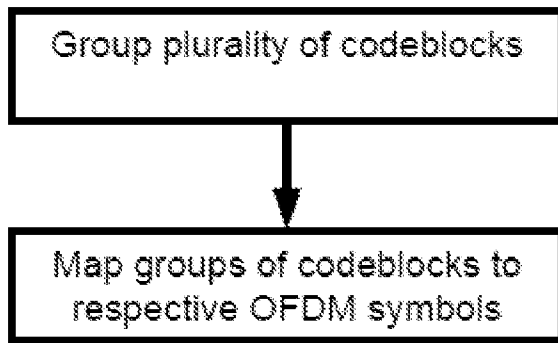


FIGURE X-2

X-2

In some embodiments, the electronic device of Figure X-1 may be configured to perform one or more processes, techniques, and/or methods as described herein, or portions thereof. One such process is depicted in Figure X-2. For example, the process may include grouping or causing to group a plurality of codeblocks and mapping one or more groups of codeblock to respective OFDM symbols.

EXAMPLES

Example 1 may include an apparatus including:

means for grouping or causing to group a plurality of codeblocks; and

means for mapping one or more groups of codeblock to respective OFDM symbols.

Example 2 may include the apparatus of example 1 and/or some other example herein, and may further include:

means for segmenting or causing to segment a data transport block into one or more segments; and

means for encoding or causing to encode segments of the one or more segments into a codeblock.

Example 3 may include the apparatus of any of examples 1 or 2 and/or some other example herein, and may further include means for computing or causing to compute a cyclic redundancy checksum for each group of codeblocks.

Example 4 may include the apparatus of one of example 3 and/or some other example herein, and may further include means for appending or causing to append the cyclic redundancy checksum to the group of codeblocks.

Example 5 may include the apparatus of any of examples 1-4 and/or some other example herein, and wherein means for mapping or causing to map include means for rate matching or causing to rate match a group of codeblocks to a plurality of OFDM symbols.

Example 6 may include the apparatus of any of examples 1-5 and/or some other example herein, and may further include means for normalizing or causing to normalize the effective code rate of each group of codeblocks belonging to a same data transport block.

Example 7 may include the apparatus of example 6, and wherein means for normalizing or causing to normalize includes means for appending or causing to append a group of codeblocks with padding bits or modulated.

Example 8 may include the apparatus of any of examples 1-8 and/or some other example herein, wherein information is segmented and wherein the apparatus includes means for determining or causing to determine one or more segment sizes for codeblocks based at least in part on one or more of: a determination of available resource elements for each codeblock group, code-rate of a transmission; and/or modulation order of the transmission.

Example 9 may include the apparatus of example 8 and/or some other example herein, wherein means for determining or causing to determine a segment size of a codeblock includes means for determining or causing to determine the segment size according to an approximately linear relationship with the available resource elements for the codeblock group.

Example 10 may include the apparatus of any of examples 1-9 and/or some other example herein, wherein the apparatus is a user equipment (UE), or a portion thereof.

Example 11 may include the apparatus of any of examples 1-9 and/or some other example herein, wherein the apparatus is an evolved nodeB (eNB), or a portion thereof.

Example 12 may include a system and method of segmentation of data transport block, encoding each segment into a codeblock, grouping plurality of codeblocks, and mapping group of codeblock to a plurality of OFDM symbols.

Example 13 may include the system and method of example 12 and/or some other example herein, wherein cyclic redundancy checksum is computed for the said group of codeblocks and appended to the group of codeblocks.

Example 14 may include the system and method of example 12 and/or some other example herein, wherein a group of codeblocks is rate matched to a plurality of OFDM symbols.

Example 15 may include the system and method of example 12 and/or some other example herein, wherein a group of codeblocks is appended with padding bits or modulated symbols to normalize the effective code rate of each group of codeblocks belonging to the same data transport block to be similar.

Example 16 may include the system and method of example 12 and/or some other example herein, wherein information is segmented and each segment size is determined by available resource elements for each codeblock group and code-rate and modulation order of the transmission.

Example 17 may include the system and method of example 16 and/or some other example herein, wherein the segment size of a codeblock and the available resource elements for the said codeblock have approximately linear relationship.

Example 18 may include a method including:

grouping or causing to group a plurality of codeblocks; and
mapping one or more groups of codeblock to respective OFDM symbols.

Example 19 may include the method of example 18 and/or some other example herein, and may further include:

segmenting or causing to segment a data transport block into one or more segments; and
encoding or causing to encode segments of the one or more segments into a codeblock;

Example 20 may include the method of any of examples 18 or 19 and/or some other example herein, and further including computing or causing to compute a cyclic redundancy checksum for each codeblock of the group of codeblocks.

Example 21 may include the method of one of example 20 and/or some other example herein, and further including appending or causing to append the cyclic redundancy checksum to the group of codeblocks.

Example 22 may include the method of any of examples 18-21 and/or some other example herein, and wherein mapping or causing to map includes rate matching or causing to rate match a group of codeblocks to a plurality of OFDM symbols.

Example 23 may include the method of any of examples 18-22 and/or some other example herein, and further including normalizing or causing to normalize the effective code rate of each group of codeblocks belonging to a same data transport block.

Example 24 may include the method of example 23, and wherein normalizing or causing to normalize includes appending or causing to append a group of codeblocks with padding bits or modulated.

Example 25 may include the method of any of examples 18-24 and/or some other example herein, wherein information is segmented and wherein the method includes determining

or causing to determine one or more segment sizes for codeblocks based at least in part on one or more of: a determination of available resource elements for each codeblock group, code-rate of a transmission; and/or modulation order of the transmission.

Example 26 may include the method of example 25 and/or some other example herein, wherein determining or causing to determine a segment size of a codeblock includes determining or causing to determine the segment size according to an approximately linear relationship with the available resource elements for the codeblock group.

Example 27 may include the method of any of examples 18-26 and/or some other example herein, wherein the method is performed by a user equipment (UE), or a portion thereof.

Example 28 may include the method of any of examples 18-26 and/or some other example herein, wherein the method is performed by an evolved nodeB (eNB), or a portion thereof.

Example 29 may include an apparatus including circuitry to:
identify a plurality of collections of codeblocks; and
generate an association between collections of the plurality of collections of codeblocks to respective OFDM symbols.

Example 30 may include the apparatus of example 29 and/or some other example herein, and may further include circuitry to:
segment a data transport block into one or more segments; and
encode segments of the one or more segments into a codeblock;

Example 31 may include the apparatus of any of examples 29 or 30 and/or some other example herein, and may further include circuitry to compute a cyclic redundancy checksum for a collection of codeblocks.

Example 32 may include the apparatus of one of example 31 and/or some other example herein, and may further include circuitry to appending or causing to append the cyclic redundancy checksum to the collection of codeblocks.

Example 33 may include the apparatus of any of examples 29-32 and/or some other example herein, and wherein circuitry to map includes circuitry to rate match a collection of codeblocks to a plurality of OFDM symbols.

Example 34 may include the apparatus of any of examples 29-33 and/or some other example herein, and may further include circuitry to normalize the effective code rate of each collection of codeblocks belonging to a same data transport block.

Example 35 may include the apparatus of example 34, and wherein circuitry to normalize includes circuitry to append a group of codeblocks with padding bits or modulated.

Example 36 may include the apparatus of any of examples 29-35 and/or some other example herein, wherein information is segmented and wherein the apparatus includes circuitry to determine one or more segment sizes for codeblocks based at least in part on one or more of: a determination of available resource elements for each codeblock group, code-rate of a transmission; and/or modulation order of the transmission.

Example 37 may include the apparatus of example 36 and/or some other example herein, wherein circuitry to determine a segment size of a codeblock includes circuitry to determine the segment size according to an approximately linear relationship with the available resource elements for the codeblock group.

Example 38 may include the apparatus of any of examples 29-37 and/or some other example herein, wherein the apparatus is a user equipment (UE), or a portion thereof.

Example 39 may include the apparatus of any of examples 29-37 and/or some other example herein, wherein the apparatus is an evolved nodeB (eNB), or a portion thereof.

Example 40 may include an apparatus comprising means to perform one or more elements of a method described in or related to any of examples 1-39, or any other method or process described herein.

Example 41 may include one or more non-transitory computer-readable media comprising instructions to cause an electronic device, upon execution of the instructions by one or more processors of the electronic device, to perform one or more elements of a method described in or related to any of examples 1-39, or any other method or process described herein.

Example 42 may include an apparatus comprising logic, modules, and/or circuitry to perform one or more elements of a method described in or related to any of examples 1-39, or any other method or process described herein.

Example 43 may include a method, technique, or process as described in or related to any of examples 1-39, or portions or parts thereof.

Example 44 may include an apparatus comprising: one or more processors and one or more computer readable media comprising instructions that, when executed by the one or more processors, cause the one or more processors to perform the method, techniques, or process as described in or related to any of examples 1-39, or portions thereof.

Example 45 may include a method of communicating in a wireless network as shown and described herein.

Example 46 may include a system for providing wireless communication as shown and described herein.

Example 47 may include a device for providing wireless communication as shown and described herein.

The foregoing description of one or more implementations provides illustration and description, but is not intended to be exhaustive or to limit the scope of embodiments to the precise form disclosed. Modifications and variations are possible in light of the above teachings or may be acquired from practice of various embodiments.