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This is to certify that the Annexure attached hereto is a copy of the undermentioned Patent Application submitted to the State Intellectual Property Office of the People's Republic of China:

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Claims

What is claimed is:

1. A method for processing information in a communication system, comprising:
acquiring an input sequence, the input sequence having a length of B;
obtaining C code blocks based on the input sequence and the maximum code block length Z
in a set of code block lengths, wherein each of the code blocks includes an input bit segment of
the input sequence, and at least one of the C code blocks includes a cyclic redundancy check
(CRC) code bit segment with a length of L or a padding bit segment; wherein

B, Z and C are integers greater than 0, and L is an integer greater than or equal to 0 and less
than Z.

2. The method as defined in claim 1, characterized in that:

if $B > Z$, then $C = \lceil B/(Z-L) \rceil$, and at least one of the C code blocks includes a segment with
a length of K_3 , wherein the segment includes an input bit segment and a CRC bit segment, and
 $K_3 = \lceil (B+C \cdot L)/C \rceil$.

3. The method as defined in claim 2, characterized in that: the code block including a
segment with a length of K_3 further comprises a padding bit segment with a length of F_3 , where
 $F_3 = I_3 - K_3$, I_3 being the smallest code block length in the set of code block lengths that is greater
than or equal to K_3 .

4. The method as defined in claim 2 or 3, characterized in that: at least one of the C code
blocks includes a segment with a length of K_4 , where $K_4 = \lfloor (B+C \cdot L)/C \rfloor$, and the number of
code blocks including a segment with a length of K_4 is $C_4 = C \cdot K_3 - (B+C \cdot L)$, the number of code
blocks including a segment with a length of K_3 is $C_3 = C - C_4$.

5. The method as defined in claim 4, characterized in that: the code block including a
segment with a length of K_4 further comprises a padding bit segment with a length of F_4 , where

$F_4 = I_4 - K_4$, I_4 being the smallest code block length in the set of code block lengths that is greater than or equal to K_4 .

6. The method as defined in any one of claims 1 to 5, characterized in that: if $L > 0$, each of the code blocks includes a CRC bit segment, and the CRC bit segment is a check bit segment generated for the input bit segment in each of the code blocks, or the CRC bit segment is a check bit segment generated for the input bit segment and padding bit segment in each of the code blocks.

7. The method as defined in claim 1, characterized in that: $C = \lceil B/Z \rceil$, and the C code blocks include at least one code block whose input bit segment has a length of K_5 , where $K_5 = \lceil B/C \rceil$.

8. The method as defined in claim 7, characterized in that: the code block including an input bit segment with a length of K_5 further comprises a padding bit segment with a length of F_5 , where $F_5 = I_5 - K_5$, I_5 being the smallest code block length in the set of code block lengths that is greater than or equal to K_5 .

9. The method as defined in claim 7 or 8, characterized in that: the C code blocks include at least one code block whose input bit segment has a length of K_6 , where $K_6 = \lfloor B/C \rfloor$, and the number of code blocks including an input bit segment with a length of K_6 is $C_6 = C \cdot K_5 - B$, the number of code blocks including an input bit segment with a length of K_5 is $C_5 = C - C_6$.

10. The method as defined in claim 9, characterized in that: the code block including an input bit segment with a length of K_6 further comprises a padding bit segment with a length of F_6 , where $F_6 = I_6 - K_6$, I_6 being the smallest code block length in the set of code block lengths that is greater than or equal to K_6 .

11. The method as defined in claim 1, characterized in that: the number of code blocks in the C code blocks including a CRC bit segment is G, where G is an integer greater than 0 and less than or equal to C.

12. The method as defined in claim 11, characterized in that:

the C code blocks respectively belong to G code block groups, and the number of code blocks in each of the code block groups including CRC bit segments is 1;

each of the CRC bit segments is a check bit segment generated for an input bit segment in at least one code block of a code block group, or each of the CRC bit segments is a check bit segment generated for an input bit segment and padding bit segment in at least one code block of a code block group.

13. The method as defined in claim 12, characterized in that: $G = \lceil B/(M \cdot Z - L) \rceil$, $C = \lceil (B + G \cdot L)/Z \rceil$, G is an integer greater than 0 and less than or equal to C, M is an integer greater than 0, and $\lceil C/G \rceil \leq M$.

14. The method as defined in claim 12, characterized in that:

$G = \min(\lceil B/(Z - L) \rceil, G_{\max})$, $G_{\max} > 0$, $G_{\max}$ is the maximum supported number of code block groups;

if $G < G_{\max}$, then $C = G$; or if $G = G_{\max}$, then $C = \lceil (B + G \cdot L)/Z \rceil$.

15. The method as defined in any one of claims 11 to 14, characterized in that: the G code block groups include at least one code block group having C_9 code blocks, where $C_9 = \lceil C/G \rceil$.

16. The method as defined in claim 15, characterized in that: the G code block groups include at least one code block group having C_{10} code blocks, where $C_{10} = \lfloor C/G \rfloor$, the number of code block groups having C_{10} code blocks is $G_2 = G \cdot C_9 - C$, and the number of code block groups having C_9 code blocks is $G_1 = G - G_2$.

17. A communication device, the communication device comprising:

an acquiring unit configured to acquire an input sequence;

a processing unit configured to obtain C code blocks based on the input sequence and the maximum code block length Z in a set of code block lengths, wherein each of the code blocks

includes an input bit segment of the input sequence, and at least one of the code blocks includes a cyclic redundancy check (CRC) code bit segment with a length of L or a padding bit segment; wherein

B, Z and C are integers greater than 0, and L is an integer greater than or equal to 0 and less than Z.

18. The communication device as defined in claim 17, characterized in that:

if $B > Z$, then $C = \lceil B/(Z-L) \rceil$, and at least one of the C code blocks includes a segment with a length of K_3 , wherein the segment includes an input bit segment and a CRC bit segment, and $K_3 = \lceil (B+C \cdot L)/C \rceil$.

19. The communication device as defined in claim 18, characterized in that: the code block including a segment with a length of K_3 further comprises a padding bit segment with a length of F_3 , where $F_3 = I_3 - K_3$, I_3 being the smallest code block length in the set of code block lengths that is greater than or equal to K_3 .

20. The communication device as defined in claim 18 or 19, characterized in that: at least one of the C code blocks includes a segment with a length of K_4 , where $K_4 = \lfloor (B+C \cdot L)/C \rfloor$, and the number of code blocks including a segment with a length of K_4 is $C_4 = C \cdot K_3 - (B+C \cdot L)$, the number of code blocks including a segment with a length of K_3 is $C_3 = C - C_4$.

21. The communication device as defined in claim 20, characterized in that: the code block including a segment with a length of K_4 further comprises a padding bit segment with a length of F_4 , where $F_4 = I_4 - K_4$, I_4 being the smallest code block length in the set of code block lengths that is greater than or equal to K_4 .

22. The communication device as defined in any one of claims 17 to 21, characterized in that: if $L > 0$, each of the code blocks includes a CRC bit segment, and the CRC bit segment is a check bit segment generated for the input bit segment in each of the code blocks, or the CRC bit segment is a check bit segment generated for the input bit segment and padding bit segment in each of the code blocks.

23. The communication device as defined in claim 17, characterized in that: $C = \lceil B/Z \rceil$, and the C code blocks include at least one code block whose input bit segment has a length of K_5 , where $K_5 = \lceil B/C \rceil$.

24. The communication device as defined in claim 23, characterized in that: the code block including an input bit segment with a length of K_5 further comprises a padding bit segment with a length of F_5 , where $F_5 = I_5 - K_5$, I_5 being the smallest code block length in the set of code block lengths that is greater than or equal to K_5 .

25. The communication device as defined in claim 23 or 24, characterized in that: the C code blocks include at least one code block whose input bit segment has a length of K_6 , where $K_6 = \lfloor B/C \rfloor$, and the number of code blocks including an input bit segment with a length of K_6 is $C_6 = C \cdot K_5 - B$, the number of code blocks including an input bit segment with a length of K_5 is $C_5 = C - C_6$.

26. The communication device as defined in claim 25, characterized in that: the code block including an input bit segment with a length of K_6 further comprises a padding bit segment with a length of F_6 , where $F_6 = I_6 - K_6$, I_6 being the smallest code block length in the set of code block lengths that is greater than or equal to K_6 .

27. The communication device as defined in claim 17, characterized in that: the number of code blocks in the C code blocks including a CRC bit segment is G, where G is an integer greater than 0 and less than or equal to C.

28. The communication device as defined in claim 27, characterized in that:
the C code blocks respectively belong to G code block groups, and the number of code blocks in each of the code block groups including CRC bit segments is 1;
each of the CRC bit segments is a check bit segment generated for an input bit segment in at least one code block of a code block group, or each of the CRC bit segments is a check bit segment generated for an input bit segment and padding bit segment in at least one code block of

a code block group.

29. The communication device as defined in claim 28, characterized in that:
 $G = \lceil B/(M \cdot Z - L) \rceil$, $C = \lceil (B + G \cdot L)/Z \rceil$, G is an integer greater than 0 and less than or equal to C ,
 M is an integer greater than 0, and $\lceil C/G \rceil \leq M$.

30. The communication device as defined in claim 28, characterized in that:

$G = \min\{\lceil B/(Z - L) \rceil, G_{\max}\}$, $G_{\max} > 0$, $G_{\max}$ is the maximum supported number of code block groups;

if $G < G_{\max}$, then $C = G$; or if $G = G_{\max}$, then $C = \lceil (B + G \cdot L)/Z \rceil$.

31. The communication device as defined in any one of claim 27 to 30, characterized in that:
the G code block groups include at least one code block group having C_9 code blocks, where
 $C_9 = \lceil C/G \rceil$.

32. The communication device as defined in claim 31, characterized in that: the G code block groups include at least one code block group having C_{10} code blocks, where $C_{10} = \lfloor C/G \rfloor$,
the number of code block groups having C_{10} code blocks is $G_2 = G \cdot C_9 - C$, and the number of code block groups having C_9 code blocks is $G_1 = G - G_2$.

Description

Information Processing Method and Device, and Communication System

TECHNICAL FIELD

Embodiments of the present invention relates to the field of communications and, more particularly, to a method, device and communication system for information processing.

BACKGROUND

In a communication system, control information or data information is usually transmitted between communication devices (for example, base stations or terminals) in the form of information sequences. Due to the complexity and variety of the wireless propagation environment, the transmitted information sequences are susceptible to interference and errors. In order to reliably transmit an information sequence, the transmitting end device performs CRC check, segmentation and check, channel coding, rate matching and interleaving on the information sequence, and maps the interleaved coded bits into modulation symbols and sends them to the receiving end device. After receiving the modulation symbol, the receiving-end communication device recovers the information sequence by deinterleaving, de-rate matching, decoding, concatenation and CRC check. These processes can reduce transmission errors and improve the reliability of data transmission.

In the fifth generation mobile communication system, it has been considered to introduce a new channel coding method to improve performance, for example, a low density parity check (LDPC) code, a polarization code and the like. LDPC code is a kind of linear block coding with sparse parity check matrix, which has the characteristics of structural flexibility and low decoding complexity. Because it uses a partially parallel iterative decoding algorithm, it has a higher throughput than the traditional Turbo code. An LDPC code commonly used in communication systems has special structural features, and its base matrix has $m \times n$ elements. If z is used as an extension factor, the check matrix H can be obtained as $(m \times z) \times (n \times z)$ - the matrix of z , that is, having $m \times n$ block matrices, with each block being a $z \times z$ all-zero matrix or unit

matrix obtained by cyclic shift. The extension factor z is generally determined according to the code block size supported by the system and the size of the information data.

After using different channel coding methods, the communication system has different coding and decoding capabilities. How to deal with the information sequence to meet the needs of channel coding, so as to better improve the performance of the system code, has become a problem to be solved.

SUMMARY OF THE INVENTION

In view of the above, the embodiments of the present invention provide a method, a device and a communication system for processing information, and the code blocks output after processing the input sequence can be adapted to the requirements of channel coding.

In a first aspect, a method of information processing in a communication system is provided, comprising:

acquiring an input sequence, the input sequence having a length of B ;

obtaining C code blocks based on the input sequence and the maximum code block length Z in a set of code block lengths, wherein each of the code blocks includes an input bit segment of the input sequence, and at least one of the C code blocks includes a cyclic redundancy check (CRC) code bit segment with a length of L or a padding bit segment; wherein B , Z and C are integers greater than 0, and L is an integer greater than or equal to 0 and less than Z .

Since the maximum code block length in the set of code block lengths has been taken into consideration in the obtainment of the code block by processing the input sequence, the requirements of the code block length inputted for channel coding can be met, and the number of code blocks can also be reduced.

In a possible embodiment of the above aspect, if $B > Z$ and each code block includes a CRC bit segment with a length of L , then $C = \lceil B/(Z-L) \rceil$, where $\lceil \cdot \rceil$ indicates rounding up the value to an integer. At least one of the C code blocks includes a segment with a length of K_3 , wherein the segment includes an input bit segment and a CRC bit segment, and $K_3 = \lceil (B+C \cdot L)/C \rceil$.

Alternatively, the code block including a segment with a length of K_3 further comprises a padding bit segment with a length of F_3 , where $F_3=I_3-K_3$, I_3 being the smallest code block length in the set of code block lengths that is greater than or equal to K_3 .

In another possible embodiment of the above aspect, at least one of the C code blocks includes a segment with a length of K_4 , where $K_4=\lfloor (B+C\cdot L)/C \rfloor$, and the number of code blocks including a segment with a length of K_4 is $C_4=C\cdot K_3-(B+C\cdot L)$, the number of code blocks including a segment with a length of K_3 is $C_3=C-C_4$.

Alternatively, the code block including a segment with a length of K_4 further comprises a padding bit segment with a length of F_4 , where $F_4=I_4-K_4$, I_4 being the smallest code block length in the set of code block lengths that is greater than or equal to K_4 .

In the above embodiments, in each of the code blocks obtained by processing the input sequence, the code block lengths of any two code blocks are equal, or are two adjacent code block lengths in the set of code block lengths, and the valid information bits in any two code blocks differ by at most 1 bit, so that the code rate of each code block is uniform. Using these code blocks as input for encoding or decoding can avoid system performance fluctuations.

In another possible embodiment of the above aspect, if $B\leq Z$, then $C=1$, the CRC bit segment in the code block has a length of $L=0$, that is, the CRC bit segment is not included; if the code block length I_0 in the set of code block lengths is greater than or equal to the minimum code block length of B , the padding bit segment in the code block has a length of I_0-B .

In another possible embodiment of the above aspect, if the channel coding mode has self-checking capability, the CRC bit segment may not be added, that is, $L=0$. At this time, $C=\lceil B/Z \rceil$, and the C code blocks include at least one code block whose input bit segment has a length of K_5 , where $K_5=\lceil B/C \rceil$.

Alternatively, the code block including an input bit segment with a length of K_5 further comprises a padding bit segment with a length of F_5 , where $F_5=I_5-K_5$, I_5 being the smallest code block length in the set of code block lengths that is greater than or equal to K_5 .

In another possible embodiment of the above aspect, the C code blocks further include at least one code block whose input bit segment has a length of K_6 , where $K_6=\lfloor B/C \rfloor$, and the

number of code blocks including an input bit segment with a length of K_6 is $C_6=C \cdot K_5-B$, the number of code blocks including an input bit segment with a length of K_5 is $C_5=C-C_6$.

In the above embodiment, the CRC bit segment is not included in each code block obtained by processing the input sequence, which can save the overhead of the system's CRC.

In another possible embodiment of the above aspect, if $L>0$, each of the code blocks includes a CRC bit segment, and the CRC bit segment is a check bit segment generated for the input bit segment in each of the code blocks, or the CRC bit segment is a check bit segment generated for the input bit segment and padding bit segment in each of the code blocks.

A second aspect provides a method for information processing in a communication system, the method comprising:

acquiring an input sequence, the input sequence having a length of B ;

determining the number of code block groups G and the number of code blocks in each code block group based on one of the maximum number of code block groups $G_{\max}$ or the maximum number of code blocks in each code block group M , the input sequence and the maximum code block length Z ;

obtaining C code blocks based on the input sequence, the number of code block groups G and the number of code blocks in each code block group.

In a possible embodiment of the first aspect or the second aspect, the number of code blocks in the C code blocks including a CRC bit segment is G , where G is an integer greater than 0 and less than or equal to C .

In another possible embodiment of the first aspect or the second aspect, the C code blocks respectively belong to G code block groups, and the number of code blocks in each of the code block groups including CRC bit segments is 1; each of the CRC bit segments is a check bit segment generated for an input bit segment in at least one code block of a code block group, or each of the CRC bit segments is a check bit segment generated for an input bit segment and padding bit segment in at least one code block of a code block group.

Since a plurality of code blocks obtained after processing the input sequence are added with CRC bit segments according to the code block group, the system's CRC overhead can be saved, and the performance of ACK feedback is better when provided on a code block group basis, and system efficiency is improved.

In another possible embodiment of the above aspect, $G = \lceil B/(M \cdot Z - L) \rceil$ or $G = \min\{\lceil B/(Z - L) \rceil, G_{\max}\}$, where M is an integer greater than 0, and $\lceil C/G \rceil \leq M$, $G_{\max} > 0$, $G_{\max}$ is the maximum supported number of code block groups;

$$C = \lceil (B + G \cdot L) / Z \rceil .$$

In another possible embodiment of the above aspect, the G code block groups include at least one code block group having C_9 code blocks, where $C_9 = \lceil C/G \rceil$.

Alternatively, the G code block groups include at least one code block group having C_{10} code blocks, where $C_{10} = \lfloor C/G \rfloor$, the number of code block groups having C_{10} code blocks is $G_2 = G \cdot C_9 - C$, and the number of code block groups having C_9 code blocks is $G_1 = G - G_2$.

In the above embodiment, the numbers of code blocks in any two code block groups differ by at most 1, such that the block error rate (BLER) and the missed-detection performance of each code block group tend to be consistent.

A third aspect provides a method for information processing in a communication system, the method comprising:

acquiring C code blocks based on the length of the output sequence and the maximum code block length Z in the set of code block lengths;

obtaining an output sequence based on the C code blocks, wherein each code block includes an output bit segment in the output sequence, and at least one code block includes a cyclic redundancy check (CRC) code bit segment with a length of L or a padding bit segment; wherein B , Z and C are integers greater than 0, and L is an integer greater than or equal to 0 and less than Z .

A fourth aspect provides a communication device, the communication device comprising:

an acquiring unit configured to acquire an input sequence;

a processing unit configured to obtain C code blocks based on the input sequence and the maximum code block length Z in a set of code block lengths, wherein each of the code blocks includes an input bit segment of the input sequence, and at least one of the code blocks includes a cyclic redundancy check (CRC) code bit segment with a length of L or a padding bit segment; wherein B , Z and C are integers greater than 0, and L is an integer greater than or equal to 0 and less than Z .

The communication device may be configured to perform the method performed by the transmitting end device as described above, with specific reference to the description of the above aspects.

In one possible design, the communication device presented by the present application may include a module or unit configured to perform actions corresponding to those of the transmitting end device in the above method design. The module or unit may be software, hardware, or software and hardware.

A fifth aspect provides a communication device, the communication device comprising:

an acquiring unit configured to acquire C code blocks based on the length of the output sequence and the maximum code block length Z in the set of code block lengths;

a processing unit configured to obtain an output sequence based on the C code blocks acquired by the acquiring unit; wherein each code block includes an output bit segment in the output sequence, and at least one code block includes a cyclic redundancy check (CRC) code bit segment with a length of L or a padding bit segment; wherein B , Z and C are integers greater than 0, and L is an integer greater than or equal to 0 and less than Z .

The communication device may be configured to perform the method performed by the receiving end device as described above, with specific reference to the description of the above aspects.

In one possible design, the communication device presented by the present application may include a module or unit configured to perform actions corresponding to those of the receiving end device in the above method design. The module or unit may be software, hardware, or software and hardware.

In a sixth aspect, an embodiment of the present invention provides a communication system, the system including the communication device described above.

In yet another aspect, an embodiment of the present invention provides a computer storage medium including a program designed to perform the above aspects.

In the method, device and communication system of the embodiment of the present invention, the code block outputted after the processing of the input sequence can meet the requirements of code block length sets in different channel coding modes, and the difference in

code rate between various code blocks is balanced. By using these code blocks for encoding or decoding, the processing performance of communication system can be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a structural schematic view illustrating a communication system provided by an embodiment of the present invention.

Figure 2 is a flow diagram illustrating an information processing method provided by another embodiment of the present invention.

Figure 3 is a structural schematic view illustrating a code block provided by another embodiment of the present invention.

Figure 4 is a structural schematic view illustrating a code block provided by another embodiment of the present invention.

Figure 5 is a schematic view illustrating an information processing method provided by another embodiment of the present invention.

Figure 6 is a schematic view illustrating an information processing method provided by another embodiment of the present invention.

Figure 7 is a schematic view illustrating an information processing method provided by another embodiment of the present invention.

Figure 8 is a schematic view illustrating an information processing method provided by another embodiment of the present invention.

Figure 9 is a flow diagram illustrating an information processing method provided by another embodiment of the present invention.

Figure 10 is a flow diagram illustrating an information processing method provided by another embodiment of the present invention.

Figure 11 is a structural schematic view illustrating a communication device provided by another embodiment of the present invention.

Figure 12 is a structural schematic view illustrating a receiving end device provided by another embodiment of the present invention.

DETAILED DESCRIPTION

The technical solutions in the embodiments of the present invention will be clearly and comprehensively described in conjunction with the accompanying drawings. It is understood that the embodiments described are only a part of the embodiments of the present invention, and not all of the embodiments. Any embodiments obtained by those skilled in the art based on the embodiments of the present invention without creative efforts are within the scope of protection of the present invention.

As shown in Figure 1, communication system 100 comprises a communication device 10 and a communication device 11, and control information or data information is received and transmitted between the communication device 10 and the communication device 11 as an information sequence. The communication device 10 functions as a transmitting end device, and transmits an information sequence on the basis of a transmission block (TB), and a transmission block CRC bit is added to each transmission block. A transmission block added with a transmission block CRC functions as an input sequence. If the length of the input sequence is less than the maximum code block length Z , padding bits may be added based on the code block length in the set of code block lengths, and then enter the encoder for channel coding. If the length of the input sequence exceeds the maximum code block length Z , the input sequence is divided into a number of input bit segments, and each code block (CB) entering the encoder includes one of the input bit segments, CRC check bit segments may be added to some or all of the code blocks to improve the error detection performance of the code blocks. Padding bits may also be added to some or all of the code blocks so that the block length of each code block satisfies the legal code block length requirements defined for the set of code block lengths. The communication device 10 performs channel coding on each code block separately, for example, coding using LDPC code to obtain a corresponding encoded code block. Each of the encoded code blocks includes a plurality of pre-coding information bits and check bits generated by the code - which are collectively referred to as coded bits.

The encoded code block is interleaved by the sub-block and stored in the circular buffer of the communication device 10. The communication device 10 selects a segment of coded bit from the circular buffer, that is, a coded bit segment is interleaved and mapped into a modulation symbol for transmission. When the communication device 10 retransmits, another coded bit segment is selected and sent from the circular buffer. If the data in the circular buffer is transmitted once, the data is returned to the front end of the circular buffer to re-encode the bit.

As the receiving end device, the communication device 11 demodulates the received modulation symbols, and after deinterleaving, stores the soft values of the received encoded bit segments in corresponding positions in the soft buffer. If a retransmission occurs, the communication device 11 combines the soft values of the coded bit segments retransmitted each time and stores them in the soft buffer, where combination as used herein indicates that if the coded bits received in two occasions are in the same position, the soft values of the coded bits received in two occasions are combined. The communication device 11 decodes all soft values in the soft buffer to obtain a code block of the information sequence. Since the communication device 11 can acquire the transmission block size, the number of code blocks in which a transmission block is divided and the length of each code block can be determined, and the communication device 11 can obtain the output bit segment in each code block. If the code block includes the CRC bit segment, the communication device 11 can also use the CRC bit segment to verify the output bit segment or the output bit segment and the padding bit segment in the code block. The communication device 11 combines the various output bit segments into an output sequence, that is, a transmission block, and further sifts and combines the transmission block to finally obtain an information sequence. It can be seen that the communication device 11 performs the inverse of the information processing method of the communication device 10.

It should be noted that, in various embodiments of the present invention, for example, the communication device 10 may be a network device in a communication system, such as a base station, etc, and the corresponding communication device 11 may be a terminal. The communication device 10 may also be a terminal in a communication system, and accordingly, the communication device 11 may be a network device in a communication system, such as a base station or the like.

For ease of understanding, some of the nouns involved in this application are described below.

In the present application, the terms “network” and “system” are often used interchangeably, but the meaning can be understood by those skilled in the art. A terminal is a device having a communication function, and may include a handheld device having a wireless communication function, an in-vehicle device, a wearable device, a computing device, or other processing device connected to a wireless modem. Terminals can be called different names in different networks, such as: user equipment, mobile stations, subscriber units, stations, cellular phones, personal digital assistants, wireless modems, wireless communication devices, handheld devices, laptops, cordless phones, wireless local loop station, etc. For convenience of description, this application is simply referred to as a terminal. A base station (BS), also referred to as a base station device, is a device deployed in a radio access network to provide wireless communication functions. The name of a base station may be different in different wireless access systems, for example, in a Universal Mobile Telecommunications System (UMTS) network, a base station is called a Node B (NodeB), and known as an evolved Node B (eNB or eNodeB) in an LTE network, and base stations in the 5th generation network may also use other names. The invention is not limited to this.

Figure 2 is a flow diagram illustrating an information processing method used in a communication system provided by an embodiment of the present invention, the method may be used in a transmitting end device, and comprises the following steps:

201: acquiring an input sequence.

In various embodiments of the invention, the input sequence may be a transmission block or a transmission block to which a transmission block CRC is added. Here, the transmission block is used to transmit control information or data information. The transmission block acquired by the transmitting end device or the transmission block to which the transmission block CRC is added may be used as an input sequence for code block segmentation.

The length of the input sequence is B , that is, the input sequence is composed of B bits, and can be generally expressed as $b_0, b_1, \dots, b_{B-1}$, and B is an integer greater than zero.

202: obtaining C code blocks based on the input sequence acquired in step 201 and the maximum code block length Z in a set of code block lengths, wherein each of the code blocks includes an input bit segment of the input sequence, and at least one code block includes a cyclic redundancy check (CRC) code bit segment with a length of L or a padding bit segment.

Wherein Z and C are integers greater than 0, and L is an integer greater than or equal to 0 and less than Z .

Usually, a set of code block lengths is defined in the system, including one or more legal code block lengths, where the maximum code block length is Z . With different channel coding methods, the set of code block lengths may be different. Taking LDPC coding as an example of channel coding, if the size of the LDPC base matrix is 34×50 , where the number of columns corresponding to the information bits is 16, the extension factor z is $\{8, 10, 12, 14, 16, 20, 24, 28, 32, 40, 48, 56, 64, 80, 96, 112, 128, 160, 192, 224, 256, 320, 384\}$, the code block length in the set of code block lengths is $16 \times z$, and the maximum code block length Z is $16 \times 384 = 6144$ bits. It should be noted that the description is merely illustrative and not limiting.

Each code block obtained by the transmitting end device performing code block segmentation on the input sequence is its output sequence, and each code block can be represented as $C_{r0}, C_{r1}, C_{r2}, C_{r3}, \dots, C_{r(K_r-1)}$, where r is the code block number, $0 \leq r < C$, and K_r is the code block length of the r th code block, that is, the number of bits in the r th code block.

In a possible embodiment, the input sequence is divided into C input bit segments based on the maximum code block length Z , and among the C code blocks, the code block i includes the input bit segment i , and the code block j includes the input bit segment j , and so on, where $0 \leq i, j < C$.

In addition to the input bit segment, a code block may optionally further include at least one of a CRC bit segment with a length of L and a padding bit segment.

After adopting the new channel coding mode, for example, LDPC coding, which has better self-checking capability, and the method of adding the CRC bit segment is also flexible, and a CRC bit segment with the length of L can be added to each input bit segment. A CRC bit segment with the length of L may be added to a plurality of input bit segments together, and a CRC bit segment may not be added to the input bit segment, in which case $L=0$.

Correspondingly, for the C code blocks, the number of code blocks including the CRC bit segment may be C, that is, each code block includes a CRC bit segment; the number of code blocks including the CRC bit segment may also be G, where G is an integer greater than 0, and less than or equal to C, that is, one of the plurality of code blocks includes a CRC bit segment; the number of code blocks including the CRC bit segment may also be 0, that is, each code block does not include the CRC bit segment, or $L=0$.

For convenience of description, in various embodiments of the present invention, a bit segment composed of an input bit segment and a CRC bit segment in a code block is sometimes referred to as a segment, that is, a segment includes an input bit segment and a CRC bit segment. If the difference between the block length K in the set of code block lengths and the length of the segment in a code block is not 0, and K is a minimum code block length greater than or equal to the segment length, the code block further includes a padding bit segment and the length of the padding bit segment is the difference between the legal block length K and the segment length. The padding bit segment is composed of one or more bits whose value is <NULL>. In some systems, the bit with the value <NULL> is also set to "0".

If the code block includes a padding bit segment, the CRC bit segment may be a check bit segment generated for the segment, or may be a check bit segment generated for the input bit segment. For example, the CRC bit segment may be generated by inputting a bit segment check in the code block, and the padding bit segment is then added. For another example, a padding bit segment may be added to the code block, then a CRC bit segment is generated for the input bit segment and the padding bit segment check in the code block, and the CRC bit segment is added to the code block. The positions of the input bit segment, the padding bit segment and the CRC bit segment in the code block are not limited here. As shown in Figure 3 (code block 1), the CRC bit segment can be placed in the last segment of the code block, and as shown in Figure 4 (code block 2), the padding bit segment can be placed in front of the input bit segment of the code block. It should be noted that this embodiment is merely exemplary, and the present invention is not limited thereto.

In the information processing method provided by the embodiment of the present invention, since the maximum code block length in the set of code block lengths has been taken into consideration in the obtainment of the code block by processing the input sequence, the

requirements of the code block length inputted for channel coding can be met, and the number of code blocks can also be reduced.

Due to the C code blocks generated from the input sequence, the length of each code block needs to be a code block length in the set of code block lengths. The lengths of the various code blocks in the set of code block lengths are arranged in ascending or descending order according to the size. In order to make the code rate of each code block uniform, among the generated C code blocks, the lengths of any two code blocks are equal, or the lengths of any two code blocks are two adjacent code block lengths in the set of code block lengths. Code block segmentation can be achieved in a variety of ways.

Figure 5 is a schematic view illustrating an information processing method provided by another embodiment of the present invention. In this way, the padding bit segments are concentrated in one code block, which is suitable for the case where two adjacent code block lengths in the set of code block lengths have a small interval. As shown in Figure 5:

If $B > Z$, each code block includes a CRC bit segment with the length of L , then $C = \lceil B/(Z-L) \rceil$, where $\lceil \cdot \rceil$ indicates rounding up the value to an integer, and C code blocks include C_1 code blocks with a code block length of K_1 and C_2 code blocks with a code block length of K_2 , where K_1 is a minimum code block length in the set of code block lengths that satisfies $C \cdot K_1 \geq (B + C \cdot L)$, and K_2 is a maximum code block length in the set of code block lengths that is smaller than K_1 , and $C_2 = \lfloor \frac{C \cdot K_1 - (B + C \cdot L)}{K_1 - K_2} \rfloor$, $C_1 = C - C_2$, where $\lfloor \cdot \rfloor$ indicates rounding down the value to an integer. One of the code blocks having a code block length of K_2 includes a padding bit segment with a length of $F = C_1 \cdot K_1 + C_2 \cdot K_2 - (B + C \cdot L)$.

It can be seen from Figure 5 that the input sequence with a length of B is divided into C input bit segments based on the determined number of code blocks and the code block length, wherein the length of one input bit segment is $K_2 - L - F$, the length of $C_2 - 1$ input bit segments is $K_2 - L$, and the length of C_1 input bit segments is $K_1 - L$. The number of code blocks with a length of K_2 is C_2 , the number of code blocks with a length of K_1 is C_1 , the length of input bit segment in the code blocks with a code block length of K_2 and including a padding bit segment is $K_2 - L - F$, the length of input bit segment in the code blocks with a code block length of K_2 and without padding bit segment is $K_2 - L$, the length of input bit segment in the code blocks with a code block

length of K_1 is K_1-L . It should be noted that the position of the padding bit segment shown in the figure is merely exemplary, and is not limited to being in the first code block, nor is it limited to being at the beginning position of the code block, and may be located after the CRC bit segment in the code block.

Taking the set of LDPC code block lengths exemplified in the foregoing embodiment as an example, where $B=32000$ bits, $Z=6144$ bits, $L=24$ bits, the number of blocks divided into is $C=\lceil B/(Z-L) \rceil =6$, the length of each code block after addition of the CRC bit segment is $B+C\cdot L=32144$ bits, the minimum code block length K_1 in the set of code block lengths satisfying $C\cdot K_1 \geq (B+C\cdot L)$ is 6144 bits, and the maximum code block length K_2 smaller than K_1 in the set of code block lengths is 5120 bits. Then, among the six code blocks, the number of code blocks whose code block length is $K_1=6144$ bits is two, and the number of code blocks whose code block length is $K_2=5120$ bits is four, one code block whose code block length is K_2 and further includes a padding bit segment with a length of 624 bits, for example, a padding bit segment with a length of 624 bits may be included in the first code block whose code block length is K_2 . It should be noted that the description herein is merely illustrative and not limiting.

Alternatively, in this way, if the length of the input sequence $B \leq Z$, then $C=1$, the length of the CRC bit segment in the code block is $L=0$, that is, the CRC bit segment is not included, if the code block length I_0 in the set of code block lengths is a minimum code block length greater than or equal to B , the length of the padding bit length in the code block is I_0-B .

Figure 6 is a schematic view illustrating an information processing method provided by another embodiment of the present invention. As shown in Figure 6:

If $B > Z$, each code block includes a CRC bit segment with a length of L , then $C=\lceil B/(Z-L) \rceil$, where $\lceil \cdot \rceil$ indicates rounding up the value to an integer. The total length of the input sequence and the various CRC bit segments is $(B+C\cdot L)$. As described in the foregoing embodiment, the segment includes an input bit segment and a CRC bit segment, and after evenly dividing the block, there is at least one code block with segments having a length of K_3 , where $K_3=\lceil (B+C\cdot L)/C \rceil$, that is, at least one of the C code blocks includes a segment with a length of K_3 .

Further, the code block with segments having a length of K_3 further includes a padding bit segment with a length of F_3 , where $F_3 = I_3 - K_3$, I_3 being a minimum code block length in the set of code block lengths that is greater than or equal to K_3 . If F_3 is 0, there is no padding bit segment in the code block with segments having a length of K_3 .

Further, at least one of the C code blocks includes a segment with a length of K_4 , where $K_4 = \lfloor (B + C \cdot L) / C \rfloor$, among the C code blocks, the number of code blocks including segments with a length of K_4 is $C_4 = C \cdot K_3 - (B + C \cdot L)$, the number of code blocks including segments with a length of K_3 is $C_3 = C - C_4$.

If $(B + C \cdot L) \% C = 0$, % is a modulo operation, then $K_4 = K_3$, each code block in the C code blocks includes a segment with a length of K_3 , that is, the number of code blocks with segments having a length of K_3 is C .

Further, the code block with segments having a length of K_4 further includes a padding bit segment with a length of F_4 , where $F_4 = I_4 - K_4$, I_4 being a minimum code block length in the set of code block lengths that is greater than or equal to K_4 . If F_4 is 0, there is no padding bit segment in the code block with segments having a length of K_4 .

It can be seen from Figure 6 that the input sequence with a length of B is divided into C input bit segments based on the determined number of code blocks and the code block length, wherein the length of C_4 input bit segments is $K_4 - L$, and the length of C_3 input bit segments is $K_3 - L$. The number of code blocks with a segment length of K_4 and a code block length of I_4 is C_4 , the number of code blocks with a segment length of K_3 and a code block length of I_3 is C_3 , the length of input bit segment in the code block with a segment length of K_4 is $K_4 - L$, and the length of input bit segment in the code block with a segment length of K_3 is $K_3 - L$. The padding bit segments are evenly distributed in the various code blocks. It should be noted that the position of the padding bit segment shown in the figure is merely exemplary, and is not limited to being at the middle position of the code block, and may be located before the input bit segment in the code block or located after the CRC bit segment in the code block.

Still taking the set of LDPC code block lengths as an example, where $B = 32000$ bits, $Z = 6144$ bits, $L = 24$ bits, $Z = 16 \cdot 384 = 6144$ bits, the number of blocks divided into is $C = \lceil B / (Z - L) \rceil = 6$, the length of each code block after addition of the CRC bit segment is $B + C \cdot L = 32144$ bits; after

evenly dividing the block, $K_3=5358$ bits, $K_4=5357$ bits. After segmentation, two code blocks with a segment length of 5358 bits and four code blocks with a segment length of 5357 bits are obtained, the minimum code block length I_3 greater than or equal to K_3 is 6144 bits. The extension factor z of the LDPC matrix used for encoding the code block channel of the segment length K_3 is greater than or equal to the minimum value 384 of $\lceil K_3/16 \rceil$, the minimum code block length I_4 greater than or equal to K_4 is 6144 bits. The extension factor z of the LDPC matrix used for encoding the code block channel of the segment length K_4 is greater than or equal to the minimum value of $\lceil K_4/16 \rceil$, 384. Correspondingly, the length of the padding bit segment in the code block with a segment length of 5358 bits is 786 bits, and the length of the padding bit segment in the code block with a segment length of 5357 bits is 787 bits.

Taking the set of LDPC code block lengths as another example, where $B=25604$ bits, $L=24$ bits, $Z=16*384=6144$ bits, the number of blocks divided into is $C=\lceil B/(Z-L) \rceil=5$, the length of each code block after addition of the CRC bit segment is $B+C*L=25604$ bits; after evenly dividing the block, $K_3=5121$ bits, $K_4=5120$ bits. After segmentation, four code blocks with a segment length of 5121 bits and four code blocks with a segment length of 5120 bits are obtained, the minimum code block length I_3 greater than or equal to K_3 is 6144 bits. The extension factor z of the LDPC matrix used for encoding the code block channel of the segment length K_3 is greater than or equal to the minimum value 384 of $\lceil K_3/16 \rceil$, the minimum code block length I_4 greater than or equal to K_4 is 5120 bits. The extension factor z of the LDPC matrix used for encoding the code block channel of the segment length K_4 is greater than or equal to the minimum value of $\lceil K_4/16 \rceil$, 320. Correspondingly, the length of the padding bit segment in the code block with a segment length of 5358 bits is 1023 bits, and the length of the padding bit segment in the code block with a segment length of 5357 bits is 0 bit.

It should be noted that the description is merely illustrative and not limiting.

Alternatively, in this way, if the length of the input sequence $B \leq Z$, then $C=1$, the length of the CRC bit segment in the code block is $L=0$, that is, the CRC bit segment is not included, if the code block length I_0 in the set of code block lengths is a minimum code block length greater than or equal to B , the length of the padding bit length in the code block is I_0-B .

The input bits and CRC bits included in the code block are also commonly referred to as valid information bits, and the number of valid information bits is a numerator for calculating the code block code rate. For a long interval between adjacent code blocks in a set of code block lengths, if a large number of padding bits appear in one code block, and there are no padding bits in other code blocks, the number of valid information bits in different code blocks may be significantly different. The length of the sequence output after encoding and rate matching of each code block is usually equal or equivalent, that is, the denominators of the calculated code block code rate are substantially equal, which results in a large difference in code rates between the code blocks, and these code blocks may cause the overall performance to deteriorate when the system is encoded or decoded. In the foregoing manner, in each of the code blocks obtained by processing the input sequence, the code block lengths of any two code blocks are equal or are two adjacent code blocks in the set of code block lengths; and in any two code blocks, the valid information bits differ by at most 1 bit, and the padding bit segments are evenly distributed in each code block, so that the code rate of the code blocks is uniform. Using these code blocks as input for encoding or decoding can avoid system performance fluctuations.

Figure 7 is a schematic view illustrating an information processing method provided by another embodiment of the present invention. In this method, no CRC bit segment is added to each code block, that is, $L=0$. As shown in Figure 7:

The number of code blocks $C = \lceil B/Z \rceil$, C code blocks include at least one code block with an input bit segment length of K_5 , where $K_5 = \lceil B/C \rceil$.

Further, the code block with the input bit segment length K_5 further includes a padding bit segment with a length of F_5 , where $F_5 = I_5 - K_5$, I_5 being a minimum code block length in the set of code block lengths that is greater than or equal to K_5 .

Further, the C code blocks further include at least one code block whose input bit segment length is K_6 , where $K_6 = \lfloor B/C \rfloor$, the number of code blocks whose input bit segment length is K_6 in the C code blocks is $C_6 = C \cdot K_5 - B$, and the number of code blocks whose input bit segment length is K_5 is $C_5 = C - C_6$.

If $B\%C=0$, % is a modulo operation, then $K_6=K_5$, each code block in the C code blocks includes an input bit segment with a length of K_5 , that is, the number of code blocks whose input bit segment length is K_5 is C.

Further, the code block with the input bit segment length K_6 further includes a padding bit segment with a length of F_6 , where $F_6=I_6-K_6$, I_6 being a minimum code block length in the set of code block lengths that is greater than or equal to K_6 .

It can be seen from Figure 7 that the input sequence with a length of B is divided into C input bit segments based on the determined number of code blocks and the code block length, wherein the length of C_6 input bit segments is K_6 , and the length of C_5 input bit segments is K_5 . The length of the input bit segment is K_6 , the number of code blocks with a code block length of I_6 is C_6 , and the number of code blocks with an input bit segment length of K_5 and a code block length of I_5 is C_5 . The padding bit segments are evenly distributed in the various code blocks. It should be noted that the position of the padding bit segment shown in the figure is merely exemplary, and is not limited to being at the last position of the code block, and may be located before the input bit segment in the code block or located after the input bit segment in the code block.

Still taking the set of LDPC code block lengths as an example, where $B=32000$ bits, $Z=16*384=6144$ bits, the number of blocks divided into is $C=\lceil B/Z \rceil =6$; after evenly dividing the block, $K_5=5334$ bits, $K_6=5333$ bits, the number of code blocks with an input bit segment length of K_5 is 4, the number of code blocks with an input bit segment length of K_6 is 2, and $I_5=I_6=6144$ bits. Accordingly, the length of the padding bit segment in the code block with an input bit segment length of K_5 is 810 bits, and the length of the padding bit segment in the code block with an input bit segment length of K_6 is 811 bits. It should be noted that the description herein is merely illustrative and not limiting.

If the information coding has a good self-checking capability, the CRC bit segment is not included in each code block obtained after processing the input sequence, and this can save the overhead of the system's CRC.

Figure 8 is a schematic view illustrating an information processing method provided by another embodiment of the present invention. The method can be used to add a CRC bit segment to a plurality of input bit segments. In this case, the number of code blocks in the C

code blocks that includes the CRC bit segment is G , where G is an integer greater than 0 and less than or equal to C . As shown in Figure 8:

The C code blocks respectively belong to the G code block groups, and the number of code blocks in each of the code block groups including CRC bit segments is 1. For any one code block group, the CRC bit segment may be a check bit segment generated for an input bit segment of at least one code block in the code block group, and may also be a check bit segment generated for an input bit segment and padding bit segment of one code block in the code block group. For example, it may be a check bit segment generated only for an input bit segment in a code block including a CRC bit segment, or may be a check bit segment generated for an input bit segment of all code blocks in a code block group, or may be a check bit segment generated only for an input bit segment and a padding bit segment in a code block including a CRC bit segment, and may also be a check generated for an input bit segment and a padding bit segment of all code blocks in a code block group. It should be noted that the embodiments of the present invention are not limited thereto.

Since a plurality of code blocks obtained after processing the input sequence are added with CRC bit segments according to the code block group, the system's CRC overhead can be saved, and the performance of ACK feedback is better when provided on a code block group basis, and system efficiency is improved.

A possible embodiment is that the input sequence is divided into C input bit segments, the C input bit segments are divided into G groups, and the code blocks including the corresponding input bit segments are a code block group, that is, the C code blocks belong to G code block groups respectively.

Another possible embodiment is to divide the input sequence into G bit groups, further divide each bit group, and obtain C input bit segments, with code blocks including input bit segments in a bit group being a code block group, and thus C code blocks belong to G code block groups respectively.

In an embodiment of the present invention, the number of code block groups G may be determined according to the maximum number of code blocks M included in one code block

group. For example, $G = \lceil B/(M \cdot Z - 1) \rceil$, $C = \lceil (B + G \cdot L)/Z \rceil$, G is an integer greater than 0 and less than or equal to C , M is an integer greater than 0, and $\lceil C/G \rceil \leq M$.

Taking $B=92000$, $Z=6144$, $L=24$ and $M=4$ as an example, a first grouping can be obtained, where $G=4$, $C=15$, that is, 4 code block groups with 15 code blocks can be obtained according to the input sequence.

In still another embodiment of the present invention, the number of code block groups G may be determined according to the maximum number of code block groups $G_{\max}$. For example, $G = \min(\lceil B/(Z - L) \rceil, G_{\max})$, $G_{\max} > 0$; if $G < G_{\max}$, then $C = G$; if $G = G_{\max}$, then $C = \lceil (B + G \cdot L)/Z \rceil$.

Taking $B=92000$, $Z=6144$, $L=24$ and $G_{\max}=4$ as an example, a second grouping can be obtained, where $G=4$, $C=15$, that is, 4 code block groups with 15 code blocks can be obtained according to the input sequence.

Based on the foregoing embodiment, in order to make the number of code blocks in each code block group uniform, the G code block groups include at least one code block group having a code block number of C_9 , where $C_9 = \lceil C/G \rceil$; the G code block groups further include at least one code block group whose code block number is C_{10} , where $C_{10} = \lceil C/G \rceil$, the number of code block groups in which the number of code blocks is C_{10} is $G_2 = G \cdot C_9 - C$, and the number of code block groups in which the number of code blocks is C_9 is $G_1 = G - G_2$.

Taking the first grouping or the second grouping in the foregoing example as an example, where $C_9=4$, $C_{10}=3$, the number of code blocks in three code block groups is 4, and the number of code blocks in one code block group is 3. The 15 code blocks are divided into 4 code block groups with the code block groups each containing 3, 4, 4, and 4 code blocks, respectively.

The method of the foregoing embodiment can make the number of code blocks in any two code block groups after the grouping differ by at most one, so that the block error rate (BLER) and the missed-detection performance of each code block group tend to be consistent.

In still another embodiment of the present invention, in order to make the input bit segment and the CRC bit segment length in each code block group uniform, the G code block groups include at least one code block group having a code block number C_9 , where $C_9 = \lceil P_1/Z \rceil$ and

$P_1 = \lceil (B+G \cdot L)/G \rceil$; the G code block groups further includes at least one code block group having a code block number of C_{10} , where $C_{10} = \lceil P_2/Z \rceil$ and $P_2 = \lceil (B+G \cdot L)/G \rceil$, the number of code block groups whose code block number is C_{10} is $G_4 = G \cdot P_1 - (B+G \cdot L)$, and the number of code block groups whose code block number is C_9 is $G_3 = G - G_4$, wherein the number of code block groups G can be determined according to the maximum number of code blocks M included in one code block group, for example, $G = \lceil B/(MZ-L) \rceil$. The number of code block groups G can be determined according to the maximum number of code block groups $G_{\max}$, for example, $G = \min\{ \lceil B/(Z-L) \rceil , G_{\max} \}$.

Taking $B=92000$, $Z=6144$, $L=24$ and $M=4$ as an example, $G=4$, $P_1=P_2=23024$, $C_9=C_{10}=4$, and the number of code blocks in each code block group is 4, with a total of 16 code blocks.

In the method of the foregoing embodiment, the lengths of the valid information bits included in the various code block groups after the grouping may be different by at most one.

It can be seen from Figure 8 that the input sequence with a length of B is divided into C input bit segments based on the determined number of code blocks, the number of code block groups and the code block length, and C code blocks belong to G code block groups. Each of the code block groups includes a CRC bit segment with a length of L, wherein each code block group of the G_2 code block groups includes C_{10} code blocks, and each of the G_1 code block groups includes C_9 code blocks.

It should be noted that the description is merely illustrative and not limiting.

Alternatively, in this way, if the input sequence length $B \leq M \cdot Z$, then $G=1$, the length of the CRC bit segment in the C code blocks is $L=0$, that is, the CRC bit segment is not included in each code block. The code block segmentation can be seen in Figure 7, and will not be described here.

Figure 9 is a flow diagram illustrating a method for processing summary information of a communication system according to another embodiment of the present invention, which may be used in a transmitting end device, where the method comprises:

901: acquiring an input sequence, the input sequence having a length of B;

902: determining the number of code block groups G and the number of code blocks in each code block group based on one of the maximum number of code block groups $G_{\max}$ or the maximum number of code blocks in each code block group M , the input sequence and the maximum code block length Z ;

Wherein, G code block groups are obtained according to the maximum code block group number $G_{\max}$, the input sequence and the maximum code block length Z , or G code block groups are obtained according to the maximum code block group M , the input sequence and the maximum code block length Z per code block group. For the determination of the number of code blocks in each code block group, reference may be made to the respective segmentation modes described in Figure 8 above, and details are not described herein again.

Step 903: obtaining C code blocks based on the input sequence, the number of code block groups G and the number of code blocks in each code block group.

The number of code blocks C can be obtained according to the number of code block groups G and the number of code blocks in each code block group. The input sequence is divided to obtain C input bit segments, each code block includes one of the input bit segments. The number of code blocks to which the CRC bit segment is added in each code block group is 1. For any one code block group, the CRC bit segment may be a check bit segment generated for the input bit segment in at least one code block in the code block group. The check bit segment may also be a check bit segment generated for the input bit segment and the padding bit segment in at least one code block in the code block group.

In order to ensure uniformity of the code blocks, the lengths of the G CRC bit segments $(B+G \cdot L)$ may be added based on the input sequence to determine the length of each code block, and division is performed according to the length of each code block.

For convenience of description, in the embodiment of the present invention, bits other than the padding bit segment included in each code block are referred to as hybrid segments, and it can be seen that the hybrid segment includes an input bit segment or an input bit segment and a CRC bit segment. In a code block group, the hybrid segment in only one code block is an input bit segment and a CRC bit segment, and the hybrid segments in other code blocks are input bit segments.

At least one of the C code blocks includes a hybrid segment with a length of K_7 , where $K_7 = \lceil (B+G \cdot L)/C \rceil$.

Further, the code block with the hybrid segment having a length of K_7 further includes a padding bit segment with a length of F_7 , where $F_7 = I_7 - K_7$, I_7 being a minimum code block length in the set of code block lengths that is greater than or equal to K_7 .

Further, at least one of the C code blocks includes a hybrid segment with a length of K_8 , where $K_8 = \lfloor (B+G \cdot L)/C \rfloor$, and among the C code blocks, the number of code blocks including hybrid segments with a length of K_8 is $C_8 = C \cdot K_7 - (B+G \cdot L)$, and the number of code blocks including hybrid segments with a length of K_7 is $C_7 = C - C_8$.

If $(B+G \cdot L) \% C = 0$, % is modulo operation, then $K_8 = K_7$, each code block in the C code blocks includes an input bit segment with a length of K_7 or a hybrid segment with a length of K_7 , that is, the number of code blocks whose mixed segment length is K_7 is C.

Further, the code block with the hybrid segment length K_8 further includes a padding bit segment with a length of F_8 , where $F_8 = I_8 - K_8$, I_8 being a minimum code block length in the set of code block lengths that is greater than or equal to K_8 .

Taking $B=92000$, $M=4$, $Z=6144$ and $L=24$ as an example, the number of code block groups at this time is $G = \lceil B/(M \cdot Z - L) \rceil$, $G=4$, the number of code blocks is $C = \lceil (B+G \cdot L)/Z \rceil$, $C=15$. The 15 code blocks are divided into 4 code block groups with the code block groups each containing 3, 4, 4, and 4 code blocks, respectively. After evenly dividing the block, $K_7=6140$ bits, $K_8=6139$ bits, the number of code blocks having a hybrid segment length of K_7 is 11, and the number of code blocks having a hybrid segment length of K_8 is 4. In the code block with a hybrid segment length of K_7 , the length of the padding segment is 4 bits, and in the code block with a hybrid segment length of K_8 , the length of the padding segment is 5 bits. For example, the hybrid segment length in the 11 code blocks of the 0-2nd group may be 6140 bits, and that in the 4 code blocks of the third group is 6139 bits. Table 1 shows the lengths of input bit segments, CRC bit segments and padding bit segments in various code blocks with this manner of segmentation. Of course, the hybrid segment length in the 0-3rd code block may be 6139 bits, and the hybrid segment length in the 4-14th code block is 6140.

Table 1: Examples of Code Block Segmentation

Group No.	Code Block No.	Input Bit Segment Length (bits)	CRC Bit Segment Length (bits)	Padding Bit Segment Length (bits)
0	0	6140	0	4
	1	6140	0	4
	2	6116	24	4
1	3	6140	0	4
	4	6140	0	4
	5	6140	0	4
	6	6116	24	4
2	7	6140	0	4
	8	6140	0	4
	9	6140	0	4
	10	6116	24	4
3	11	6139	0	5
	12	6139	0	5
	13	6139	0	5
	14	6115	24	5

It should be noted that the above are convenient examples and the invention is not limited thereto.

Adding CRC according to the code block group can save the overhead of CRC check and further improve system performance. If the system adopts hybrid automatic repeat-request (HARQ) and implements grouped feedback on positive/negative (ACK/NACK) information, then adding CRC according to the code block group can save feedback signaling overhead and improve system transmission efficiency.

Based on the information processing method of the foregoing embodiments, the communication device 10 can also separately encode the C code blocks to obtain the encoded code blocks. The communication device 10 can encode each code block according to the channel coding and coding method used by the system, that is, each output sequence C_{r0} , C_{r1} , C_{r2} , C_{r3} , ..., $C_{r(K-1)}$ in step 202 is used as an input sequence of the encoder, for example, using LDPC coding, or Polar coding. This is not a limitation here. After encoding the code block, the communication device 10 transmits the encoded code block to the receiving end.

Figure 10 is a flow diagram illustrating an information processing method provided by another embodiment of the present invention, where the method is applicable to a receiving end device. As shown in Figure 10, the method comprises:

1001: acquiring C code blocks based on the length of the output sequence and the maximum code block length Z in the set of code block lengths;

In various embodiments of the invention, the output sequence may be a transmission block or a transmission block to which a transmission block CRC is added. Here, the transmission block may be obtained by dividing the information sequence into blocks according to the transmission block size, for transmitting control information or data information. The transmission block obtained by the receiving end device according to the received code block or the transmission block added with the transmission block CRC may be used as an output sequence of the code block segmentation. Since the processes of the transmitting end device and the receiving end device are reciprocal, for the transmitting end device, the output sequence of the code block segmentation of the receiving end device is equivalent to the input sequence of the code block segmentation of the transmitting end device.

The communication device 11 can obtain the received transmission block size (TB size), that is, the length of the output sequence, and the maximum code block length Z in the set of code block lengths, so that the number of code blocks C of the output sequence can be determined.

The communication device 11 receives the C coded code blocks transmitted by the communication device 10 and decodes them with a decoder to obtain C code blocks.

1002: obtaining an output sequence based on the C code blocks acquired in step 1002.

Wherein each code block includes an output bit segment in the output sequence, and at least one code block includes a cyclic redundancy check (CRC) bit segment with a length of L , or a padding bit segment; wherein, B , Z , and C are all integers greater than 0, L is an integer greater than or equal to 0 and less than Z .

In addition to determining the number of code blocks in step 1001, the communication device 11 can also determine the length of each code block, the length of the output bit segment in the code block, the length L of the CRC bit segment, and the length of the padding bit segment. For details, refer to the example of code block segmentation in each embodiment shown in Figures 5-8, in which how to determine the number of code blocks, the code block length, and the length L of the CRC bit segment, and the padding bit length is described. The

communication device 11 acquires the output bit segments from the respective code blocks and then combines them to obtain an output sequence.

In addition to the output bit segment, the code block includes a CRC bit segment with a length of L . If the CRC bit segment is a check bit segment generated for the output bit segment in the code block, the communication device 11 verifies the output bit segment in the code block based on the CRC bit segment, and if the check passes, the code block is determined. The verified output bit segment can be used to further merge with other output bit segments that pass the check. If the CRC bit segment is the check bit segment generated for the output bit segment and the padding bit segment in the code block, the communication device 11 checks the output bit segment and the padding bit segment in the code block based on the CRC bit segment. If the check passes, it determines that the output bit segment and the padding bit segment in the code block are correct, and the communication device 11 further merges the output bit segment with other output bit segments passed by the check. If the CRC bit segment is a check bit segment generated by the output bit segments of the plurality of code blocks, the communication device 11 checks the output bit segments in these code blocks, and if the check passes, the communication device 11 combines these output bit segments with other correct output bit segments. If the CRC bit segment is a check bit segment generated by the output bit segment and padding bit segments in the plurality of code blocks, the communication device 11 checks the output bit segment and the padding bit segment in the code blocks based on the CRC bit segment, and if the check passes, the communication device 11 merges these output bit segments with other verified output bit segments.

The method performed by the communication device 11 is the inverse process of the communication device 10. For the number of code blocks, the length, the padding segment length and the addition of the CRC bit segment, reference may be made to the code block segmentation example described in the foregoing Figures 5-8. The only difference is that the output bit segment of the output sequence indicated by the communication device 11 corresponds to the input bit segment of the input sequence indicated by the communication device 10. Since the methods and effects of information processing have been described in the foregoing embodiments, they are not described here again.

Figure 11 is a structural schematic view illustrating a communication device provided by another embodiment of the present invention. The communication device is applicable to the communication system shown in Figure 1. The communication device 10 can include an acquiring unit 101 and a processing unit 102, wherein:

The acquiring unit 101 is configured to acquire an input sequence, and the processing unit 102 is configured to obtain C code blocks based on the input sequence and the maximum code block length Z in the set of code block lengths, where each code block includes an input bit segment in the input sequence, at least one of the code blocks includes a cyclic redundancy check (CRC) bit segment with a length of L , or a padding bit segment; wherein, B , Z and C are integers greater than 0, L is an integer greater than or equal to 0, and less than Z . For embodiments that can be used to implement the foregoing method, reference may be made to the foregoing embodiments of method, and details of which are not described here again.

The communication device 10 may further include an encoding unit 103, which may also be referred to as an encoder or an encoding circuit or the like, and is mainly used to encode the various code blocks output by the processing unit 102, for example, the C code blocks in the above embodiment perform LDPC encoding separately.

The communication device 10 may also include a transceiving unit 104, which may also be referred to as a transceiver, transceiver, or transceiver circuit or the like. The transceiving unit 104 is mainly used for transmitting and receiving radio frequency signals, for example, for transmitting the encoded code block encoded by the encoding unit 103 to the communication device 11.

The communication device 10 may also include other units, e.g. a unit for generating a transmission block CRC, a rate matching unit, an interleaving unit, a modulating unit, etc, which may be used to implement the respective partial functions of the communication device 10 of Figure 1, respectively.

It should be noted that the communication device 10 may include one or more memories and processors for implementing various functions of the communication device 10 of Figure 1. The memory and processor can be set individually for each unit. It is also possible that multiple units share the same memory and processor.

Figure 12 is a block diagram illustrating the construction of a communication device which can be applied to the communication system shown in Figure 1. The communication device 11 may include an acquiring unit 111 and a processing unit 112, where:

The acquiring unit 111 is configured to obtain C code blocks based on the length of the output sequence and the maximum code block length Z in the set of code block lengths;

The processing unit 112 is configured to obtain an output sequence based on the C code blocks acquired by the acquiring unit 111, wherein each code block includes an output bit segment in the output sequence, and at least one code block includes a cyclic redundancy check (CRC) with a length of L, or a padding bit segment; wherein B, Z and C are integers greater than 0, and L is an integer greater than or equal to 0 and less than Z.

The acquiring unit 111 and the processing unit 112 can be used to implement the method in the foregoing method embodiments. For details, refer to the description in the foregoing method embodiments, and the details of which are not described here again.

The communication device 11 may further include a decoding unit 113, which may also be referred to as a decoder or a decoding circuit or the like, and is mainly used for decoding the various encoded code blocks received by the transceiving unit 114.

The communication device 11 may also include a transceiving unit 114, which may also be referred to as a transceiver, transceiver, or transceiver circuit or the like. The transceiving unit 114 is mainly used for transmitting and receiving radio frequency signals, for example, for receiving the encoded code blocks in the foregoing method embodiments transmitted by the communication device 10.

The communication device 11 may also include other units, e.g. a unit for transmission block CRC check, a de-rate matching unit, a de-interleaving unit, a demodulation unit, etc, which may be used to implement respective portions of the communication device 11 as shown in Figure 1.

It should be noted that the communication device 11 may include one or more memories and processors for implementing various functions of the communication device 11 as in Figure 1. The memory and processor can be set individually for each unit. It is also possible that multiple units share the same memory and processor.

It is also understood by those skilled in the art that the various illustrative logical blocks and steps listed in the embodiments of the present invention can be implemented by electronic hardware, computer software, or a combination of both. Whether such functionality is implemented by hardware or software depends on the design requirements of the particular application and the overall system. Persons skilled in the art can implement the described functions using various methods for each specific application, but such implementation should not be construed as being beyond the scope of the embodiments of the present invention.

The various illustrative logic units and circuits described in the embodiments of the present invention may be implemented by a general purpose processor, a digital signal processor, an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any designed combination of the above to implement or operate the functions described. A general purpose processor may be a microprocessor, which may alternatively be any conventional processor, controller, microcontroller, or state machine. The processor may also be implemented by a combination of computing devices, such as a digital signal processor and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a digital signal processor core, or any other similar configuration.

The steps of the method or algorithm described in the embodiments of the present invention may be directly embedded in hardware, a software unit executed by a processor, or a combination of the two. The software unit can be stored in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, removable disk, CD-ROM, or any other form of storage medium in the art. Illustratively, the storage medium can be coupled to the processor such that the processor can read information from the storage medium and can write information to the storage medium. Alternatively, the storage medium can also be integrated into the processor. The processor and the storage medium may be disposed in an ASIC, and the ASIC may be disposed in a UE. Alternatively, the processor and the storage medium may also be located in different components in a UE.

From the description of the above embodiments, those skilled in the art can clearly understand that the present invention can be implemented with hardware, firmware, or a combination thereof. When implemented with software, the functions described above may be

stored in or transmitted as one or more instructions or codes on a computer readable medium. Computer readable media includes both computer storage media and communication media, including any medium that facilitates transfer of a computer program from one location to another. A storage medium may be any available media that can be accessed by a computer. By way of example but without limitation, computer readable media may comprise RAM, ROM, EEPROM, CD-ROM or other optical disk storage, disk storage media or other magnetic storage device, or can be used for carrying or storing desired program codes in the form of an instruction or data structure, and any other medium that can be accessed by the computer. Also, any connection may suitably be a computer readable medium. For example, if the software is transmitted from a website, server, or other remote source using coaxial cable, optical fiber and cable, twisted pair, digital subscriber line (DSL), or wireless technologies such as infrared, radio, and microwave, then the coaxial cable, optical fiber and cable, twisted pair, DSL, or wireless technologies such as infrared, wireless, and microwave are included in the fixing of the associated medium. As used in the present invention, a disk and a disc include a compact disc (CD), a laser disc, a compact disc, a digital versatile disc (DVD), a floppy disk, and a Blu-ray disc, wherein the disc is usually magnetically copied, and the disc uses laser to optically replicate data. Combinations of the above should also be included within the scope of the computer readable media.

In summary, the foregoing merely illustrates preferred embodiments of the technical solution of the present invention, and is not intended to limit the scope of the present invention. Any modifications, equivalent substitutions, improvements, etc made within the spirit and scope of the present invention are intended to be included within the scope of protection of the present invention.

Drawings

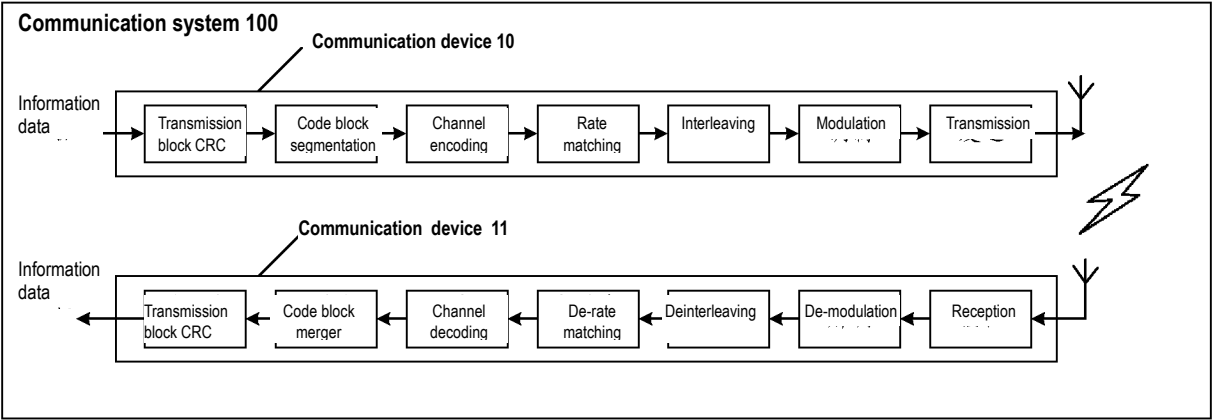


Figure 1

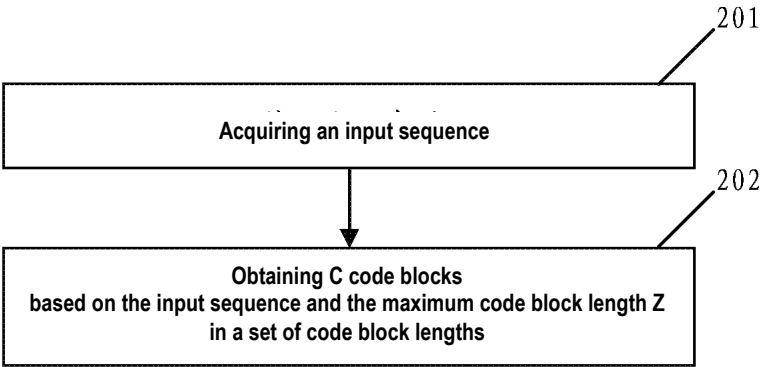


Figure 2

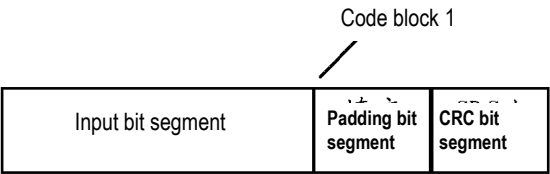


Figure 3

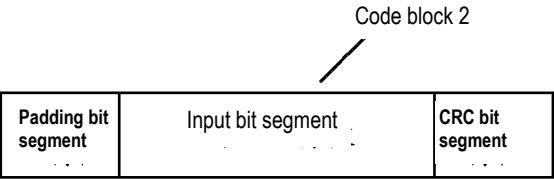


Figure 4

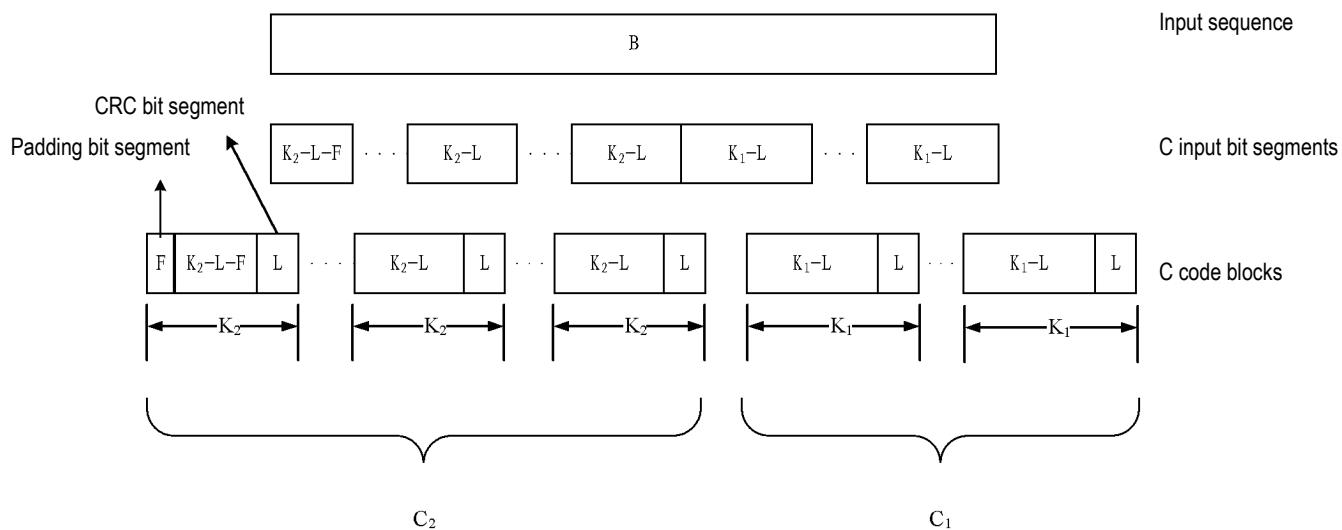


Figure 5

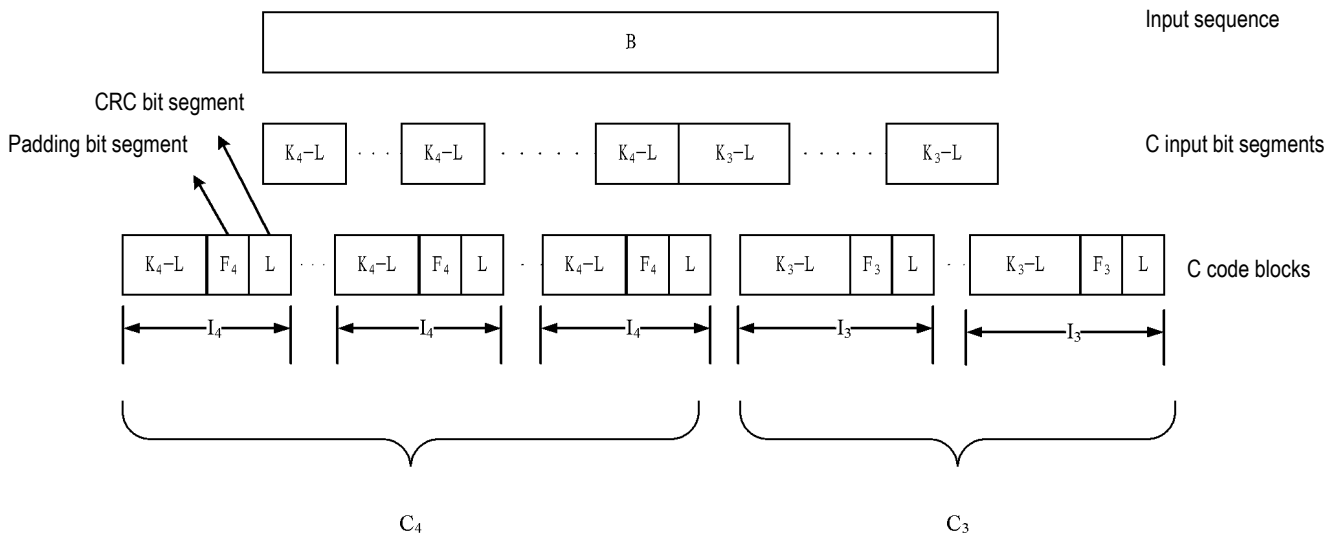


Figure 6

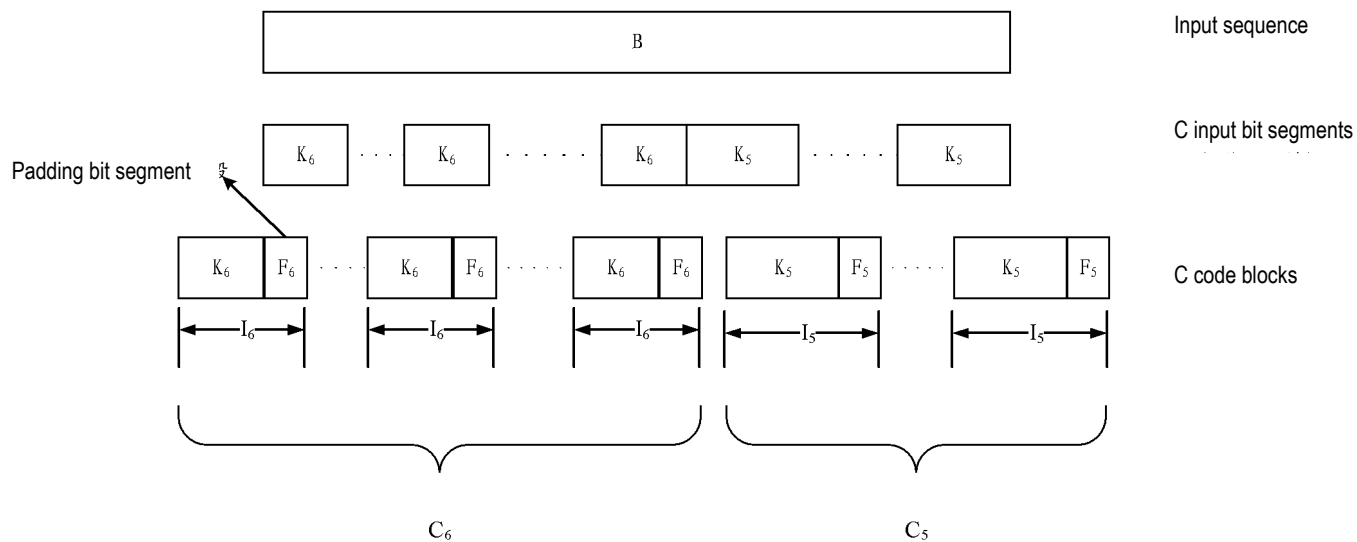


Figure 7

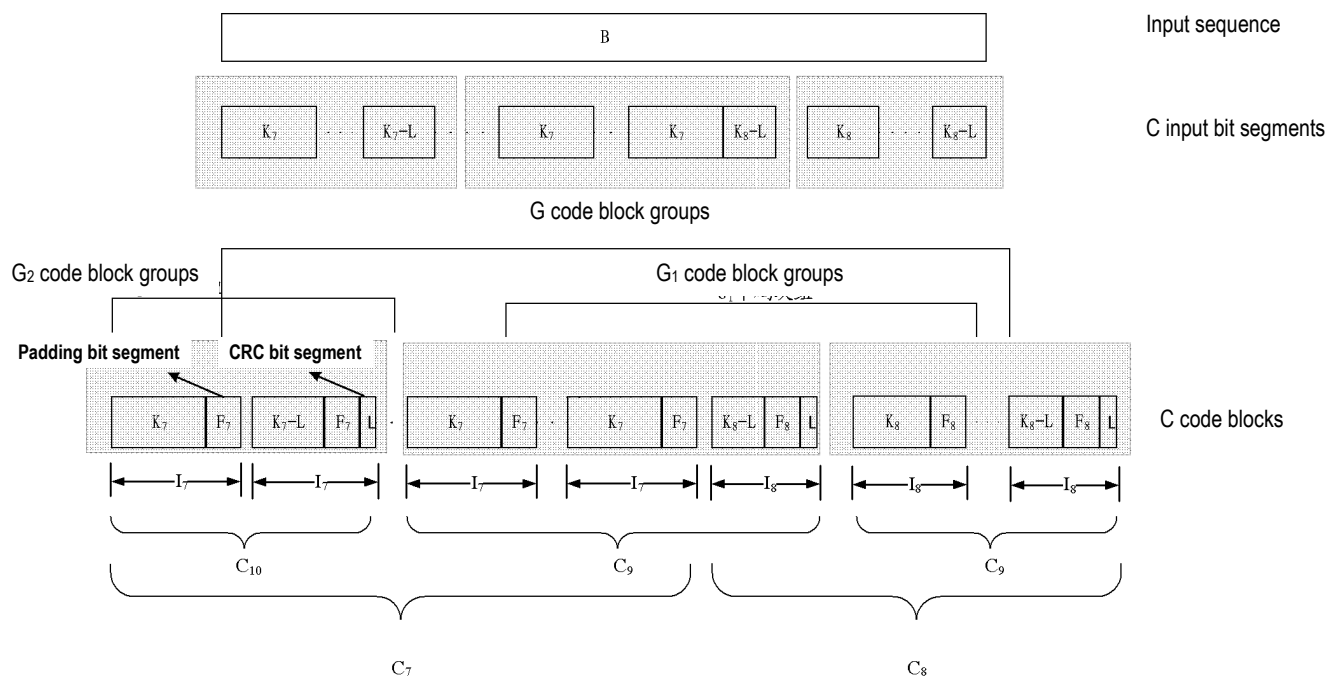


Figure 8

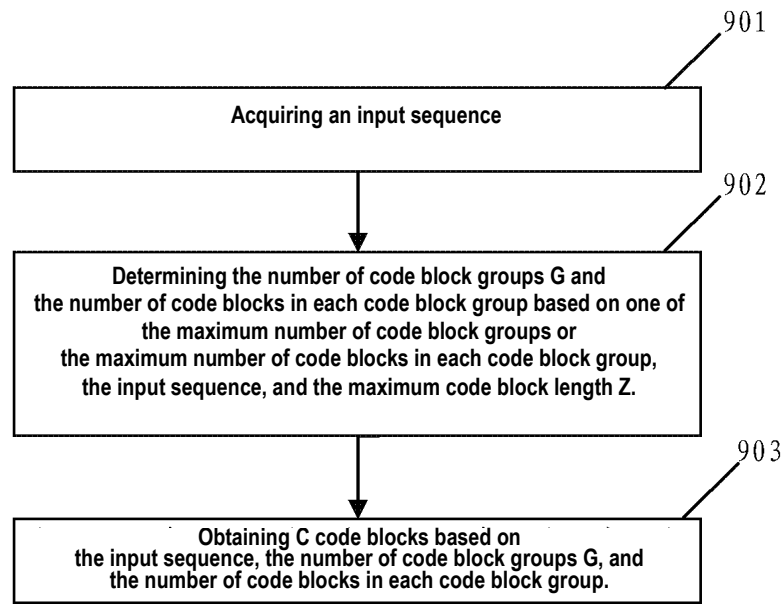


Figure 9

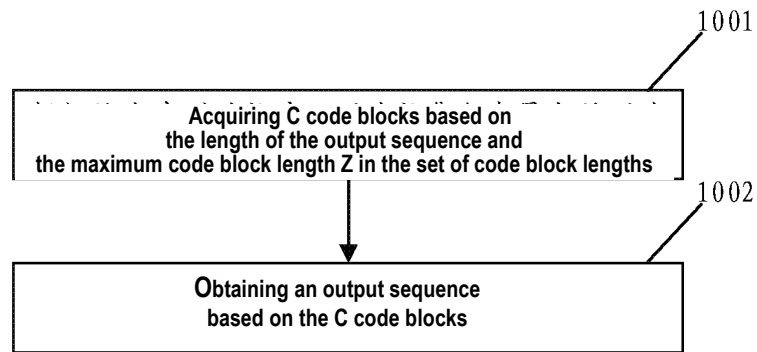


Figure 10

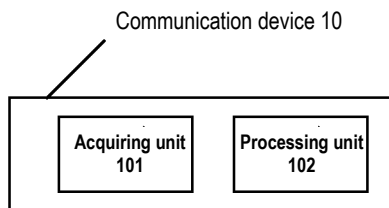


Figure 11

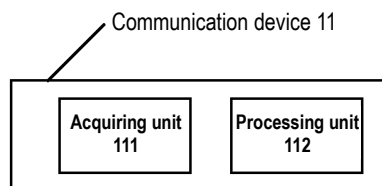


Figure 12



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Date: February 22, 2024

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