

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.

Petitioner,

v.

LIONRA TECHNOLOGIES LIMITED,

Patent Owner.

Case IPR2024-00734
U.S. Patent 7,632,518

PATENT OWNER’S RESPONSE TO THE PETITION

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TABLE OF PATENT OWNER'S EXHIBITS

Exhibit No.	Description
2001	Declaration of Dr. Eric Cole in support of Patent Owner's Response
2002	CV of Dr. Eric Cole, DPS

I. Introduction

Patent Owner respectfully requests that the Board find all of Petitioner's challenges to the claims of U.S. Patent No. 7,632, 518 ("the '518 patent") without merit. Petitioner's obviousness challenges rely on multiple references that a Person of Ordinary Skill in the Art (POSITA) would not have combined in the absence of impermissible hindsight and improperly seek to conflate multiple incompatible prior art elements in an effort to satisfy a single claim limitation.

II. Background

The '518 Patent is entitled "Dynamic Access Control Lists" and was filed on April 8, 2004. *See* Ex. 1001. Robert Faulk, the inventor of the '518 Patent, recognized that existing network security techniques, specifically access control lists used in Layer 3 routers to restrict access based on IP addresses, were inadequate and there was a need for enhanced and dynamic access control lists. Ex. 2002, ¶ 47.

Then and now, computers or hosts in an Ethernet local area network (LAN) are attached to the network and each host is uniquely identified by a physical address which is designated a media access control (MAC) address in an Ethernet network. The MAC address of each host is typically hardwired into an Ethernet network interface card in the host. The network interface card in each host transmits and receives Ethernet packets to communicate with the other hosts in the network. Each

Ethernet packet includes an address segment including the MAC address of the host to receive the packet (destination MAC address) along with the MAC address of the host sending the packet (source MAC address), and further includes a data segment, as will be understood by those skilled in the art. Ex. 2002, ¶ 44, Ex. 1001, 1:5-24.

The MAC address of each host is utilized by Ethernet switches in the network to receive and forward Ethernet packets between hosts. More specifically, a switch receives an Ethernet packet from a source host, examines the destination MAC address portion of the packet to determine where to forward the packet, and forwards the packet to the host corresponding to the destination MAC address. *Id.*

In many situations, an Ethernet network must communicate with hosts outside the network and in different types of networks. For example, a user of a host in an Ethernet network may want to access various Web sites and Web pages contained on the Internet. To communicate with other types of networks, the host utilizes the Internet Protocol (IP) which allows hosts in many different types of networks to communicate with each other through IP packets. Within the Ethernet network, each host must be assigned an IP address by a network administrator for the purpose of communicating with computers outside the network via the Internet Protocol. Ex. 2002, ¶ 45, Ex. 1001, 1:25-35.

Devices known as routers operated to forward IP packets from one network to another utilizing the IP addresses contained in the IP packets being communicated. A router typically included an access control list (ACL) to restrict or define the hosts with which a given host is allowed to communicate. Access control lists were and are utilized as a tool for network security to define or control the hosts and other objects, such as files and directories, with which a given host can communicate. For example, IP packets from a particular IP network or a particular Web site may be restricted from being received by hosts in the Ethernet network. In this situation, the access control list on the router would contain a field indicating that packets from the IP address corresponding to this Web site are to be denied, meaning that any such packets received by the router will not be forward to the intended host in the Ethernet network. IP packets include source and destination IP addresses, with the source IP address corresponding to the IP address of the host that sent the packet and the destination IP address corresponding to the host that is to receive the packet. Ex. 2002, ¶ 46, Ex. 1001, 1:36-57.

The inventor of the '518 Patent recognized that there was a need for access control lists that allows access of hosts in a computer network such as an Ethernet network to be restricted or controlled based upon user names, MAC addresses, domain names, and DNS names instead of merely IP address information. Ex. 2002,

¶ 47, Ex. 1001, *Id.*, 3:12-16. Mr. Faulk addressed that need with the enhanced and dynamic access control lists disclosed and claimed in the '518 Patent. The '518 Patent discloses and claims both methods and apparatus corresponding to his inventions.

The '518 Patent discloses an Ethernet switch according to an embodiment of the claimed inventions using a functional block diagram in Figure 3 of the '518 Patent. Ex. 1001, 4:42-44.

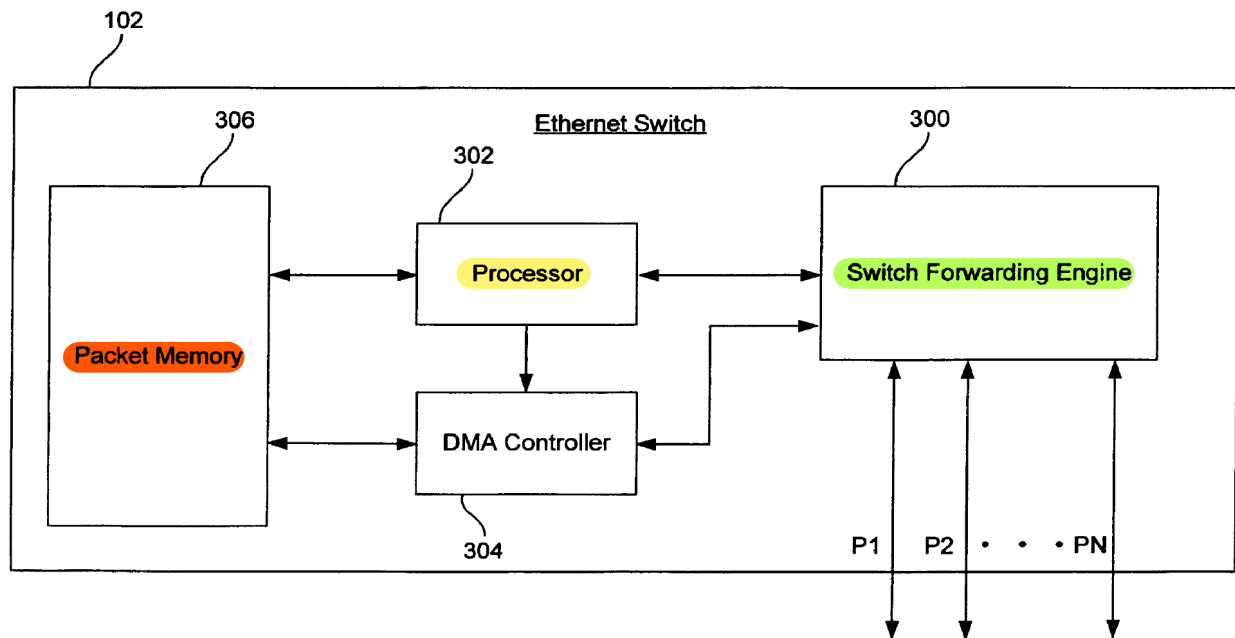


FIG. 3

Ex. 1001, Fig. 3 (annotated). The red Packet Memory 306 corresponds to the “memory circuit” in claims 15 and 19, the yellow Processor 302 corresponds to the

claimed “processor,” and the green Switch Forwarding Engine 300 corresponds to the claimed “forwarding circuit.”

In the embodiment corresponding to challenged apparatus claims 15 and 19, the switch 102 includes a direct memory access (DMA) controller 304 that transfers the packets selected by the switch forwarding engine 300 to a packet memory 306. The selected packets are stored in the packet memory 306 for processing by the processor 302. Also stored in the packet memory 306 is the enhanced access control list 108 along with required programming instructions for execution by the processor to control the overall operation of the switch 102. To store a selected packet from the switch forwarding engine 300, the processor 302 programs required registers in the DMA controller 304.

The switch forwarding engine 300 then supplies the packet to the DMA controller 304 which, in turn, stores the packet in the packet memory 306. The processor 302 accesses the stored packets in the packet memory 306 along with the stored enhanced access control list 108 to generate the dynamic access control list 104. Ex. 2002, ¶ 48.

III. Person of Ordinary Skill in the Art

A person of ordinary skill in the art in the field of the '518 Patent would have been a person with a Bachelor's degree in computer science, computer engineering,

electrical engineering or equivalent and at least two years of experience in computer networking and network system security. Additional education in the field could be substituted for industry experience, and vice versa.

IV. The Challenged Claims of the '518 Patent are Not Unpatentable.

The Petition challenges the validity of the claims of the '518 Patent on two grounds, both of which are limited to obviousness. Petition at 9. Ground 1 is directed to the challenged method claims (1 and 3) and ground 2 is directed to the challenged apparatus claims (15, 17, and 19-21). *Id.*

For the limitations of claims 1 and 3, the Petition and Petitioner's declarant, Dr. Crovella, rely on three references. The first reference is U.S. Patent No. 6,651,096 to Gai et al. (Ex. 1006, "Gai") and is entitled "Method and Apparatus for Organizing, Storing and Evaluating Access Control Lists." The second reference is U.S. Patent No. 8,751,647 to Yip et al. (Ex.1013, "Yip") and is entitled "Method and Apparatus for Network Login Authorization." The third reference is U.S. Patent No. 7,523,485 to Kwan (Ex.1007, "Kwan") and is entitled "System and Method for Source IP Anti-Spoofing Security." *Id.*

For the limitations of claims 15, 17, and 19-21, the Petition and Petitioner's declarant, Dr. Crovella, rely on these three references and a fourth reference, U.S. Patent No, 7,003,597 to Georgiou et al. (Ex. 1008, "Georgiou").

As discussed below, ground 1 fails because a POSITA would not have been motivated to combine Gai, Yip and Kwan to achieve the claimed invention. *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”); *Virtek Vision Int'l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 888 (Fed. Cir. 2024) Ground 2 fails for the same reasons as ground 1 and also because Petitioner's proposed combination of four (or five) incompatible memory devices or circuits does not correspond to or meet the limitation of the claimed memory circuit.

A. Ground 1 does not establish that challenged claims 1 and 3 are rendered obvious by Gai in view of Yip and Kwan.

As noted above, Petitioner asserts that independent claim 1 and dependent claim 3 would have been obvious to a POSITA over three references – Gai, Yip and Kwan. Petition, 9-22.

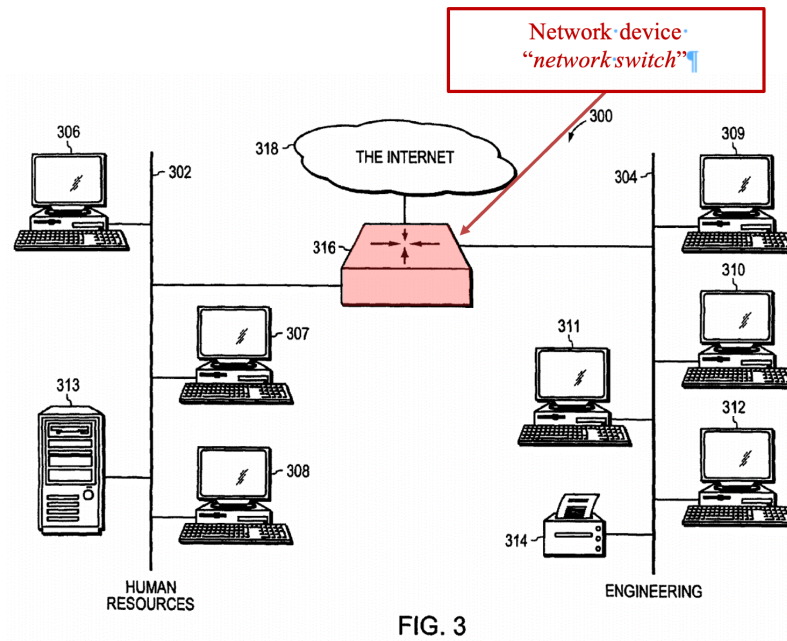
A POSITA would have considered these references in the context of the layers of the Open Systems Interconnection (OSI) Reference Model and especially Layer 2, the data link layer, Layer 3, the network layer, and Layer 4, the transport layer. Ex. 2001, ¶ 51. And, as discussed below, a POSITA would not have been motivated to combine these references.

1. Gai is directed to a Layer 3 device and was intended to achieve higher switching speeds.

The first reference Petitioner relies on is U.S. Patent No. 6,651,096 to Gai et al. and is entitled “Method and Apparatus for Organizing, Storing and Evaluating Access Control Lists.”

The purported invention in Gai “relates to a method and apparatus for efficiently organizing, storing and evaluating access control lists (ACLs) for use by an *intermediate network device* of a computer network.” Ex. 1006, Abstract (emphasis added). A POSITA would have understood that Gai is directed to and discloses a Layer 3 intermediate device that communicates with the Internet. Ex. 2001, ¶ 52.

Gai discloses that “[p]referably, *intermediate network device 316 is a layer 3 intermediate device and thus operates up to the network layer of the communication protocol stack implemented within the network 300*. For example, device 316 preferably includes an Internet Protocol (IP) software layer. Device 316 may also implement network services such as route processing, path determination and path switching functions.” Ex. 1006, 5:23-29 (emphasis added).



Ex.1006, Fig. 3 (annotated).

Petition, 33.

Although Gai discusses Layer 2 devices, a POSITA would have understood that Gai's disclosure was directed to Layer 3 switching devices. Ex. 2001, ¶ 53. Gai teaches that "intermediate devices, commonly referred to as routers, may operate at higher communication layers, such as layer 3, which in TCP/IP networks corresponds to the Internet Protocol (IP) layer. IP message packets include a corresponding header which contains an IP source address and an IP destination address. Routers or layer 3 switches may re-assemble or convert received data frames from one LAN standard (e.g., Ethernet) to another (e.g. Token Ring). Thus, layer 3 devices are often used to interconnect dissimilar subnetworks. Some layer 3

intermediate network devices may also examine the transport layer headers of received messages to identify the corresponding TCP or UDP port numbers being utilized by the corresponding network entities. Such extended-capability devices are often referred to as Layer 4, Layer 5, Layer 6, Layer 7 switches or Network Appliances.” Ex. 1006, 2:9-24.

As taught by Gai, “[t]he term layer 3 intermediate device as used [in Gai] are intended broadly to cover any intermediate device operating primarily at the internetwork layer, including, without limitation, routers as defined by Request for Comments (RFC) 1812 from the Internet Engineering Task Force (IETF), intermediate devices that are only partially compliant with RFC 1812, intermediate devices that provide additional functionality, such as Virtual Local Area Network (VLAN) support, IEEE 802.1Q support and/or IEEE 802.1D support, etc.” *Id.*, 5:35-44.

Gai’s boilerplate recitation of possible applicability to “switches and/or layer 2 intermediate devices” would have been considered by a POSITA in the context of Gai’s detailed disclosure of a Layer 3 device and its assertion that it could “operate with other, possibly far more complex, network topologies.” *Id.*, 5:44-59. A POSITA would not have considered a Layer 2 device to be a more complex network topology. *See also* Ex. 1006, 62-65 (“A suitable platform for intermediate network

device 316 are the Catalyst 8500® series of switch routers and/or the Catalyst® 6000 family of multi layer switches both from Cisco Systems, Inc.”). Ex. 2001, ¶ 54.

A POSITA would also have understood that the Access Control Lists discussed in Gai were directed to Layer 3 switching. *See, e.g.*, Ex. 1006, 16:63-17:25 (discussing, e.g., Source and Destination Port Identification, Internet Protocol Source and Destination Address Fields). Ex. 2001, ¶ 55.

A POSITA would also have considered the teachings of Gai in the context of Gai's stated goals. Gai's primary goal is to achieve higher switching speeds. As Gai teaches, “[t]here is no need for the forwarding entity 404 to evaluate multiple ACLs for each message. In addition, the evaluation of the single, unified ACL is performed by the TCAM *at much higher speeds*. Accordingly, forwarding entity 404 can *process messages much more quickly than the prior art devices*. In addition, ACL evaluation through the TCAM 410 preferably takes place in hardware rather than software. That is, forwarding entity 404 may include one or more Application Specific Integrated Circuits (ASICs) for extracting and supplying the relevant information to TCAM 410, unlike the prior art devices in which ACL evaluation is performed by one or more software modules or libraries. *The present invention is thus able to achieve much higher switching speeds than the prior art devices. Indeed, the forwarding entity 404 of the present invention is effectively able to*

process network messages at rates of multi-Gigabits per second.” Ex. 1006, 17:51-67. Ex. 2001, ¶ 56.

2. Yip is directed to a Layer 3 device that blocks ports.

The second reference Petitioner relies on is U.S. Patent No. 8,751,647 to Yip et al. and is entitled “Method and Apparatus for Network Login Authorization.”

Yip is directed to completely blocking access to a port until a lengthy authorization process is completed. Yip teaches “control[ing] the admission of a user to a network by preventing a port through which the user connects to the network from forwarding data packets until the user is authorized. A network login controller operates in conjunction with a user interface to receive a user identification data from the port user. The network login controller further operates in conjunction with an authorization server to authenticate the user by sending a user authentication request containing the user identification data to the authentication server. The network login controller grants or denies permission to the user to access the network based on the user authentication response from the authentication server. If permission is granted, then the network login controller unblocks the port through which the user is connected to place it in packet-forwarding mode.” Ex. 1013, Abstract. Ex. 2001, ¶ 58.

Yip teaches assigning temporary IP addresses, which is inconsistent with Gai's Access Control Lists. Ex. 2001, ¶ 59. In Yip, "prior to obtaining the user identification data 121, the end station/host computer H11 211 needs at least a temporary IP address to gain access to the network login controller 110 and associated user interface 120 on packet-forwarding device 200." Ex. 1013, 7:66-8:3. In Yip, "[s]ometimes, the end station/host computer needs to obtain a temporary IP address from the packet-forwarding device 200 before network login authorization 100 can take place, such as in the case of a campus environment where a roaming user will not always be using the same port for authentication. In one embodiment, assigning a temporary IP address to end station/host computer H11 211 is handled by an IP address server 130." *Id.*, 8:8-16. Yip further teaches that "[i]n one embodiment, at processing block 405 of FIG. 5, the user connects to a port of a packet-forwarding device 200 and, if necessary, obtains a temporary IP address from an IP address server 130 accessible to device 200. In one embodiment, the IP address server 130 is a DHCP server that may reside on the network 300, or in the packet switching device 200 itself. A temporary IP address is required in the campus environment where a typical user is a roaming user that may connect to the network from any number of ports that are available at various locations on the campus." *Id.*, 9:21-30.

Yip only discusses using a MAC address in alternate embodiments. Ex. 2001, ¶ 60. “In an alternate embodiment, a static layer-2 address, such as the user's end station MAC address may be adequate for purposes of obtaining access to the network login controller 110 and user interface 120 on packet-forwarding device 200.” Ex. 1013, 6:23-28 (emphasis added). “In some cases the end station/host computer, e.g. H11 211, uses its MAC address, ...” *Id.*, 8:3-4. However, Yip does not explain when or why or how a MAC address would be used, and a POSITA would not consider Yip's bare assertion that a MAC address could be used, without more, as teaching the use of MAC addresses. Ex. 2001, ¶ 60.

3. A POSITA Would Not Have Been Motivated to Combine Gai and Yip.

As discussed above, Yip teaches blocking a specific port. A POSITA would not look to Yip's teaching of blocking a port until a lengthy authentication process had been completed in connection with Gai's teaching of high-speed network switching. Blocking one or more ports for an indeterminate time would be antithetical to Gai's goal of higher switching speeds and faster processing of messages. Ex. 2001, ¶ 61.

The Petitioner argues that text-based Access Control Lists that included MAC addresses of devices authorized to access the network would have been obvious to a POSITA based on the combination of Gai and Yip. *Id.*, ¶¶ 62-63. However, as

explained by Dr. Cole, a POSITA would not have been motivated to combine Gai and Yip. *Id.*, ¶ 64.

At the time of the invention, April 2004, network systems were often viewed as and divided into multiple layers throughout the industry. MAC addresses, which were typically used only for granular hardware level device management within a local area network (LAN) were usually hosted in the data link layer of the network, while ACLs were hosted in the Network and transport layers. Crossing these layers would lead to inefficiencies and increase network complexity, leading to potential new vulnerabilities and higher costs for implementation. *Id.*, ¶ 64.

The Petitioner does not address the inherent incompatibility and complexity a combination of Yip and Gai would introduce into a network and does not explain how a combination would be done in an effective manner other than his assertions that a combination would in theory work together at the time. The separation of the layers went against general industry understanding at the time, and presented more problems than the end result could justify. *Id.*, ¶ 64.

The proposed combination of Gai and Yip would not have been viewed as a feasible option from the perspective of a network professional in April 2004 and would have been avoided as a potential performance killer and costly endeavor for any company that attempted to implement it. A POSITA would not think to combine

ACLs and MAC addresses due to their inherent separation within network layers causing complexity and performance issues when theoretically combined. *Id.*, ¶ 64.

4. Kwan is directed to a Layer 2 device.

The third reference Petitioner relies on is U.S. Patent No. 7,523,485 to Kwan and is entitled “System and Method for Source IP Anti-Spoofing Security.”

A POSITA would understand that Kwan's teachings are directed to the subnet or Layer 2 level. Ex. 2001, ¶ 66 “One approach to improving defenses against Source IP Spoofing is to attack the problem at the subnet or Layer 2 level.” Ex. 1007, 3:21-23.

Kwan discloses a Layer 2 device. Ex. 2001, ¶ 67. “FIG. 2 shows a view of an embodiment of a network device 200 of the present invention. This network device provides layer 2 switching functions.” Ex. 1007, 3:42-45. “The network device 200 contains a processing device which operates to analyze data, packets received on a port to identify the MAC address of the host sending the data packet. Each data packet can include at least the MAC address of the device sending the data packet (source MAC address) and the MAC address of the device to which the data packet is to be sent to (destination MAC address).” *Id.*, 3:59-64.

Although Kwan recognizes that “each host on the subnet can also have an IP address,” *id.*, 3:67, a POSITA would understand that Kwan's teachings are directed

to a subnet with limited connectivity. Ex. 2001, ¶ 68. A POSITA would understand this because Kwan contemplates limiting each port to a single host, Ex. 1007, 6:30-31 (“If there is more than one host device allowed per port, ...”) and teaches limiting the number of IP addresses associated with each port. Ex. 2001, ¶ 68. “Additional MAC address and IP address pairs will continue to be learned until the maximum number of MAC and IP Addresses is reached.” Ex. 1007, 6:36-38. *See also Id.*, 6:60-7:5.

Kwan’s discloses and teaches using a lengthy and time-consuming process for learning the correct IP address. Ex. 2001, ¶ 69. “[A] tiered, or delayed, approach is required to successfully detect the source IP address. This approach could allow for first identifying the MAC address and then waiting for an appropriate amount of time to learn the correct IP address.” Ex. 1007, 6:5-8. Kwan also teaches that “[i]t is also advantageous to confirm that the learned IP address is correct by performing a reverse IP check.” *Id.*, 6:25-27.

5. A POSITA Would Not Have Been Motivated to Combine Gai and Kwan.

A POSITA would not be motivated to combine Kwan’s teachings of a subnetwork Layer 2 device with Gai’s teachings of a Layer 3 intermediate device because a POSITA would recognize that what works for Layer 2 switching generally

does not apply to Layer 3 switching. A POSITA would also recognize that limiting the number of hosts that can connect to a single port or requiring a lengthy process for learning the correct IP address as taught by Kwan would be contrary to Gai's stated goal of achieving higher switching speeds. Ex. 2001, ¶ 70.

Petitioner's assertion that it would have been obvious to a POSITA to implement Gai's administrator text-based ACLs to include MAC addresses as well as seed IP addresses and learn IP addresses is wrong, as is Petitioner's assertion that a POSITA would have been motivated to combine Gai and Kwan's teachings. Ex. 2001, ¶ 72.

As an initial matter, and as discussed above in the context of Gai and Yip, it would not have been obvious to a POSITA nor viewed as feasible to combine the functionality of ACLs and MAC addresses, which is a requirement necessary for a combination of Gai and Kwan to function as proposed by Petitioner. *Id.*, ¶ 72.

In addition, adding dynamic IP learning functionality to ACLs including MAC addresses would introduce new vulnerabilities into the network, such as IP spoofing the MAC address into applying incorrect security controls. *Id.*, ¶ 73. Petitioner's argument that this combination of technology provides additional security by "reducing false learning" and "combating source IP spoofing," ignores the conceptual hurdle that adding to the number of network components relying on an

updated dynamic IP address could result in more reliance on faulty information. *Id.*, ¶ 73.

In April 2004, a network security POSITA would have viewed a combination of IP address properties and MAC addresses in text-based ACLs as far too complex and vulnerable to integrate into a network with the certainty needed for network security. *Id.*, ¶ 73.

6. A POSITA Would Not Have Been Motivated to Combine Gai, Yip and Kwan to Meet the Enhanced and Dynamic Access Control List Limitations of Claims 1 and 3.

As discussed above, a POSITA would not have been motivated to combine the Gai, Yip and Kwan references to satisfy the enhanced access control list limitations and the dynamic access control list limitations of claim 1 of the '518 Patent. Patent Owner has presented compelling evidence that a skilled artisan would have been discouraged from pursuing a combination of Gai and Yip, or Gai and Kwan, or Gai, Yip and Kwan.

Where, as here, a Patent Owner presents strong evidence that there would not have been a motivation to combine the asserted references, it is proper for the Board to consider Patent Owner's evidence and find that Petitioner has failed to meet its burden of showing unpatentability. *See Lab'y Corp. of Am. Holdings v. Ravgen, Inc.*, Nos. 2023-1342, 2023-1345, 2025 U.S. App. LEXIS 171, at *10 (Fed. Cir. Jan. 6,

2025) (*citing Arctic Cat Inc. v. Bombardier Recreational Prods. Inc.*, 876 F.3d 1350, 1363 (Fed. Cir. 2017) (affirming PTAB decision that Petitioner failed to establish a motivation to combine the asserted obviousness references).

And, because a dependent claim cannot be obvious if the independent claim from which it depends is not obvious, Petitioner has not established that dependent claim 3 is unpatentable. *See, e.g., Comaper Corp. v. Antec, Inc.*, 596 F.3d 1343 (Fed. Cir. 2010). If an independent claim is nonobvious, then the dependent claim is also nonobvious. *In re Fine*, 837 F.2d 1071, 1076 (Fed. Cir. 1988) (“A claim that depends from a non-obvious independent claim is non-obvious because it contains all the limitations of the independent claim, plus a further limitation.”). The Board does not need to consider “arguments that certain dependent claim limitations would have been obvious where the base claim has not been proven invalid.” *SynQor, Inc. v. Artesyn Techs., Inc.*, 709 F.3d 1365, 1375 (Fed. Cir. 2013). *See also Zimmer Surgical, Inc. v Stryker Corp.*, 365 F.Supp. 3d 466, 487-488 (D. Del. 2019) (“As a dependent claim contains at least one more limitation than the independent claim upon which it depends, it cannot be invalid under § 102 . . . if the independent claim upon which it depends is not anticipated.”) (*citing CA, Inc. v. Simple.com, Inc.*, 780 F. Supp. 2d 196, 260 (E.D.N.Y. 2009), *Duhn Oil Tool, Inc. v. Cooper Cameron Corp.*, 2012 U.S. Dist. LEXIS 24088, 2012 WL 604138 (E.D. Cal. Feb. 23, 2012)).

B. Ground 2 does not establish that challenged claims 15, 17, and 19-21 are rendered obvious by Gai in view of Yip and Kwan and Georgiou.

For the limitations of claims 15, 17, and 19-21 of the '518 Patent, Petitioner and Petitioner's declarant, Dr. Crovella, rely on the Gai Patent (as modified per Yip and Kwan) and U.S. Patent No, 7,003,597 to Georgiou et al. ("Georgiou"). *See* Petition at 9, 43-85; Ex. 1003, ¶¶ 133-257.

1. It would not have been obvious to a POSITA to combine the teachings of Gai and Georgiou to meet the dynamic access control list limitations of claims 15, 17, and 19-21.

Independent claim 15 recites limitations to a dynamic access control list, specifically [15.1.5] subject to access restrictions contained in a dynamic access control list; [15.2.4] [the memory circuit...operable to store]...a dynamic access control list; [15.3.3] [the processor...] operable to process the specific packets stored in the memory circuit using the enhanced access control list to generate the dynamic access control list and; [15.3.4] [the processor...operable to...] store the dynamic access control list in the memory circuit.

The Petition and Dr. Crovella assert that these "dynamic access control list" limitations would have been obvious to a POSITA who would have been motivated to combine Gai, Yip and Kwan. *See* Petition at 63-65, 69, 73-76; Ex. 1003, ¶¶ 180-187, 201-204, 214-221.

Independent claim 19 recites limitations to a dynamic access control list, specifically [19.1.6] subject to access restrictions contained in a dynamic access control list; [19.2.4] [the memory circuit...operable to store]...a dynamic access control list; [19.3.3] operable to process the specific packets stored in the memory circuit using the enhanced access control list to generate the dynamic access control list and [19.3.4] [the processor... operable to...] store the dynamic access control list in the memory circuit.

The Petition and Dr. Crovella assert that these “dynamic access control list” limitations would have been obvious to a POSITA who would have been motivated to combine Gai, Yip and Kwan. *See* Petition at 80-81; Ex. 1003, ¶¶ 236, 240, 243-244.

For the reasons stated above with respect to challenged claim 1, Petitioner has failed to meet its burden to establish that a POSITA would have been motivated to combine the Gai, Yip, Kwan and Georgiou references to satisfy the dynamic access control list limitations of independent claims 15 and 19 of the Challenged Patent.

Claims 17, 20 and 21 are dependent claims that incorporate the limitations of the independent claims, including the dynamic access control list limitations, and Petitioner failed to meet its burden of establishing that a POSITA would have been motivated to combine the Gai, Yip, Kwan and Georgiou references to satisfy the

dynamic access control list limitations incorporated by reference in dependent claims 17, 20 and 21 for the same reasons stated above with respect to challenged claim 1.

2. It would not have been obvious to a POSITA to combine the teachings of Gai, Yip, Kwan, and Georgiou to meet the memory circuit limitation of claims 15, 17, and 19-21.

Independent claim 15 recites limitations to a memory circuit, specifically [15.2.1] a memory circuit coupled to the forwarding circuit; [15.2.2] the memory circuit operable to store packets; [15.2.3] [the memory circuit...operable to store]...an enhanced access control list; [15.2.4] [the memory circuit...operable to store]...a dynamic access control list; [15.3.1] a processor coupled to the forwarding circuit and to the memory circuit; [15.3.3] [the processor...] operable to process the specific packets stored in the memory circuit using the enhanced access control list to generate the dynamic access control list; and [15.3.4] [the processor...operable to...] store the dynamic access control list in the memory circuit.

The Petition and Dr. Crovella assert that the claimed “memory circuit” limitation of claim 15 is disclosed by the non-volatile random access memory (NVRAM) 408, dynamic memory 409, TCAM 410 and memory 411 in Gai as modified by Yip, Kwan, and Georgiou. *See* Petition at 65-71, 73-76; Ex. 1003, ¶¶ 188-208, 214-221.

Independent claim 19 recites limitations to a memory circuit, specifically [19.2.1] a memory circuit coupled to the forwarding circuit; [19.2.2] the memory circuit operable to store packets; [19.2.3] [the memory circuit...operable to store]...an enhanced access control list; [19.2.4] [the memory circuit...operable to store]...a dynamic access control list; [19.3.1] a processor coupled to the forwarding circuit and to the memory circuit; [19.3.3] [the processor...] operable to process the specific packets stored in the memory circuit using the enhanced access control list to generate the dynamic access control list; and [19.3.4] [the processor...operable to...] store the dynamic access control list in the memory circuit.

The Petition and Dr. Crovella assert that the claimed “memory circuit” limitation of claim 19 is also disclosed by the non-volatile random access memory (NVRAM) 408, dynamic memory 409, TCAM 410 and memory 411 in Gai as modified by Yip, Kwan, and Georgiou. *See* Petition at 80-81; Ex. 1003, ¶¶ 237-240, 241, 243-244.

Petitioner argues that it would have been obvious to combine the teachings of Gai and Georgiou. Petitioner's declarant, Dr. Crovella, highlights a technological limitation in Gai where the process of forwarding a significant number of packets for processing in the CPU would create processing delays as the packet flow outpaces the processing capabilities. Dr. Crovella offers Georgiou as a solution to

this issue, based on Georgiou's purported teaching of a process of storing packets temporarily in dynamic memory until the CPU is freed up based on Georgiou's statements regarding "receiv[ing] and temporarily stor[ing] the incoming packets in a memory ... until subsequent processing can access and retrieve the packets, as appropriate, for action on the packet contents." Ex. 1003, ¶¶ 138-139. Dr. Crovella states that this combination would "make more efficient use of Gai's network bandwidth." *Id.*, ¶ 141.

Petitioner and Dr. Crovella are wrong. A POSITA considering a hypothetical combination of Georgiou and Gai as described would instantly note that the reliance on dynamic memory to store packets would bottleneck the system greatly within a relatively fast time frame as packets fill up the dynamic memory and slow down the stream of data to a crawl during filtering processes. Temporary storage in dynamic memory would lead to further network inefficiencies as the flow of packets would still outpace processing capabilities, meaning that there would be a net increase in the overall number of packets over time, regardless of how many packets can be redirected to dynamic memory. Ex. 2001, ¶ 83.

Further, implementing this process would be extremely costly and inefficient, as well as conceptually incompatible with the typical methods of switch hardware to forward packets at the highest sustainable rate as designed. A POSITA would thus

view a combination of switch hardware storing packets and storing packets in the CPU as an unrealistic and impractical goal to implement in the network. *Id.*

A POSITA would have recognized that storing Internet Protocol (IP) packets in memory as allegedly taught by Georgiou would be incompatible with Gai's goal of higher switching speeds and faster processing of messages. *Id.*, ¶ 94.

A POSITA would have considered Gai's teaching that, "[t]here is no need for the forwarding entity 404 to evaluate multiple ACLs for each message. In addition, the evaluation of the single, unified ACL is performed by the TCAM ***at much higher speeds***. Accordingly, forwarding entity 404 can ***process messages much more quickly than the prior art devices***. In addition, ACL evaluation through the TCAM 410 preferably takes place in hardware rather than software. That is, forwarding entity 404 may include one or more Application Specific Integrated Circuits (ASICs) for extracting and supplying the relevant information to TCAM 410, unlike the prior art devices in which ACL evaluation is performed by one or more software modules or libraries. ***The present invention is thus able to achieve much higher switching speeds than the prior art devices. Indeed, the forwarding entity 404 of the present invention is effectively able to process network messages at rates of multi-Gigabits per second.***" Ex. 1006, 17:51-67.

A POSITA would also have considered Gai's teaching that "the processing and forwarding of packets by the network device is substantially improved" because "[w]ith a single, unified ACL defined per interface per direction and stored in a CAM-type memory, the intermediate network device is able to rapidly evaluate network messages. In particular, upon receipt of a packet at a first interface, a forwarding entity at the intermediate network device tests the packet against the single, unified ACL stored in the corresponding portion of the CAM. When a match is obtained, the corresponding decision is returned to the forwarding entity, which then takes the appropriate action (e.g., forward, discard, log and forward, transfer to CPU for additional processing, etc.) Since the intermediate network device only evaluates a single, unified ACL stored in the CAM, rather than multiple ACLs stored in RAM, a decision can be rapidly obtained." *Id.*, 4:26-42.

However, Georgiou has a diametrically opposite approach. Ex. 2001, ¶ 96. In Georgiou, "after reception of a packet from the network interface, the packet is typically temporarily stored in an inbound buffer in the network interface from where it is then transferred to memory to await subsequent processing." Ex. 1013, 3:18-22.

A POSITA would not have been motivated to combine Gai and Georgiou's teachings because any modification to Gai in accordance with Georgiou's teachings

would have **slowed** Gai's processing and been directly contrary to Gai's goal of faster processing, as well as adding increased complexity (e.g., a DMA circuit). Ex. 2001, ¶ 97.

A POSITA would not have been motivated to combine Gai, Yip, Kwan and Georgiou because of the inherent separation of MAC addresses and ACL lists, the introduction of massive performance issues, and increased vulnerability within a system that would be too complex, costly, and incompatible for a realistic integration. *Id.*, ¶ 84.

3. The Non-Volatile Random Access Memory (NVRAM) 408, Dynamic Memory 409, and TCAM 410 Disclosed in Gai Do Not Meet the Limitation of a “Memory Circuit Coupled to the Forwarding Circuit” recited in claims 15 and 19.

The Petition and Dr. Crovella identify four separate circuits in Gai as corresponding to “a memory circuit” in independent claims 15 and 19 of the Challenged Patent. *See* Petition at 65-71, 73-76; 80-81; Ex. 1003, ¶¶ 188-208, 214-221, 237-240, 241, 243-244.

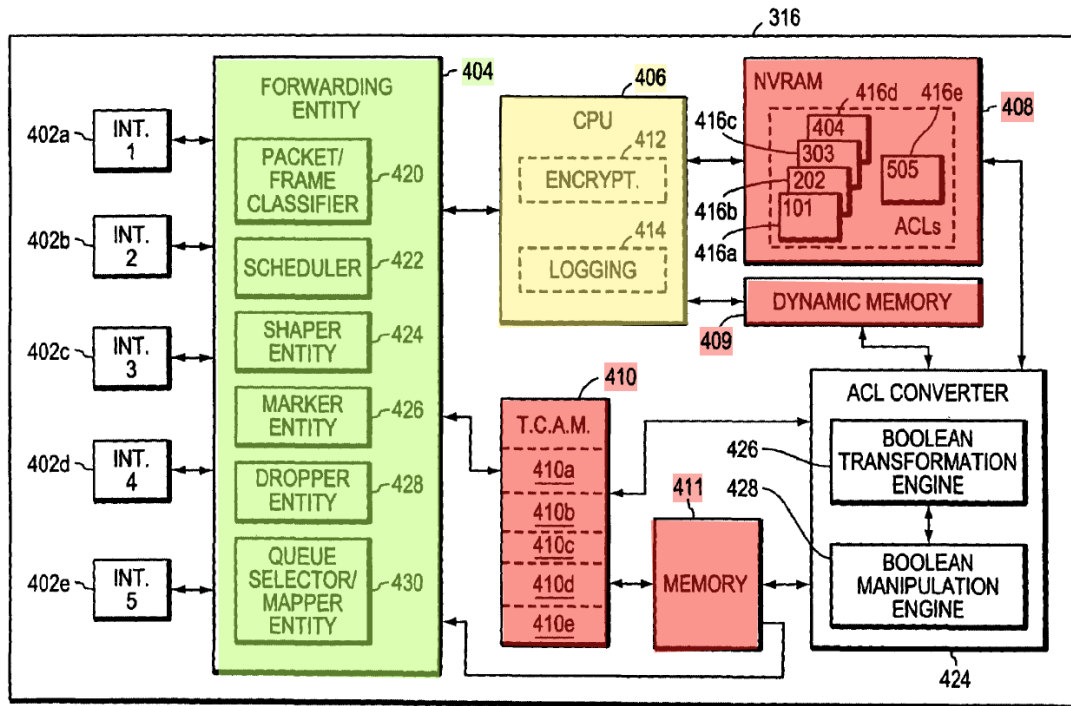


FIG. 4

Ex. 1006, Fig. 4 (annotated with yellow processor, green forwarding circuit and red memory circuit(s)).

Gai discloses that, “[d]evice 316 further includes at least one forwarding entity 404, a central processing unit (CPU) 406, non-volatile random access **memory** (NVRAM) 408, dynamic **memory** 409 and at least one content addressable or associative **memory** 410. The associative memory 410 is preferably a ternary content addressable memory (TCAM), and its cells (not shown) may be associated with or assigned one of three values, such as “0”, “1” or “don't care”. Associated

with and coupled to the TCAM 410 is another memory device 411, such as a dynamic random access **memory**.” Ex. 1006, 5:66-6:9 (emphasis added).

A POSITA would *not* have understood that four different memory circuits (or devices) correspond to a single memory circuit as recited in claims 15 and 19 of the Challenged Patent. A POSITA would have recognized that the different types of memory in Gai – non-volatile RAM, dynamic memory, and content addressable memory – could not be combined into a single memory circuit operable to store packets, enhanced control lists, and dynamic control lists. Ex. 2001, ¶ 92.

A POSITA would also have understood that Gai's four different memory circuits (or devices), along with a fifth memory circuit or device to store packets, would not correspond to a single memory circuit as recited in claims 15 and 19 of the Challenged Patent as Petitioner and Dr. Crovella suggest. *Id.*, ¶ 93.

A POSITA would have recognized that Gai teaches that the processor is coupled to NVRAM 208 and dynamic memory 409. *Id.*, ¶ 98. “CPU 406, ..., is coupled to NVRAM 408, which may contain one or more text-based access control lists (ACLs) 416*a*-416*e*, such as ACLs 101, 202, 303, 404 and 505, and also to dynamic memory 409.” Ex. 1006, 6:13-18.

A POSITA would have recognized that NVRAM 408 and dynamic memory 409 are not “a memory circuit ... operable to store packets and operable to store ...

a dynamic access control list” as claimed. A POSITA would understand that transient packets would not be stored in non-volatile RAM (NVRAM). Ex. 2001, ¶ 98.

A POSITA would also have recognized that Gai teaches that “[t]he forwarding entity 404 is also coupled to the CPU 406, the TCAM 410, which may be apportioned into segments 410*a-e* whereby each segment 410*a-e* corresponds to a particular interface 402*a-e*, and memory 411.” Ex. 1006, 6:23-28. A POSITA would have recognized that TCAM 410 and memory 411 are not “a memory circuit ... operable to store packets and operable to store an enhanced access control list” as claimed. A POSITA would understand that transient packets would not be stored in ternary content addressable memory (TCAM). Ex. 2001, ¶ 99.

A POSITA would have further recognized that Gai's teachings include “an access control list (ACL) converter 424 [that] is operatively coupled to NVRAM 408 for accessing the text-based ACLs 416*a-e*, dynamic memory 409 for processing the ACLs 416*a-e*, and to TCAM 410 and its associated memory 411 for storing modified versions of the ACLs 416*a-e* ...” Ex. 1006, 6:36-41. A POSITA would have recognized that an ACL converter does not correspond to either the claimed processor or forwarding circuit as identified by the Petition and Dr. Crovella, and

would therefore not couple the memory to either the processor or the forwarding circuit. Ex. 2001, ¶ 100.

A POSITA would have also recognized that Gai does not disclose or teach a memory circuit operable to store packets. In Gai, “[t]he message [packet] 100 is captured and provided to the forwarding entity 404.” Ex. 1006, 16: 67-17:1. In Gai, “the forwarding entity 404 is basically configured to forward or switch network messages among the various interfaces 402*a-e* of device 316.” *Id.*, 6:27-31. Ex. 2001, ¶ 101.

Even if a POSITA would have considered adding an additional DMA circuit operable to store packets, as suggested by a combination of Gai and Georgiou as proposed by the Petition and Dr. Crovella, which a POSITA would not have done for at least the reasons stated above, that resulting quintet of circuits would not have corresponded to “a memory circuit” as claimed in claims 15 and 19 of the ’518 Patent. Ex. 2001, ¶ 101.

Accordingly, the non-volatile random access memory (NVRAM) 408, dynamic memory 409, TCAM 410, and memory 411 in Gai do not teach, suggest, or disclose the “memory circuit” limitations of claims 15 and 19 of the ’518 Patent. *Id.*, ¶ 102. Furthermore, a POSITA would have understood from the combined

teachings of Gai and Georgiou that Gai and Georgiou teach, suggest or disclose the “memory circuit” limitations of claims 15 and 19 of the '518 Patent. *Id.*, ¶ 103.

Claims 17, 20 and 21 are dependent claims that incorporate the limitations of the independent claims, including the memory circuit limitations. For the reasons stated above with respect to challenged claims 15 and 19, neither the combined teachings of Gai and Georgiou or the non-volatile random access memory (NVRAM) 408, dynamic memory 409 and TCAM 410 in Gai disclose, teach or suggest the “memory circuit” limitations incorporated by reference in dependent claims 17, 20 and 21. *Id.*, ¶ 104. And, as discussed above, a dependent claim cannot be obvious if the independent claim from which it depends is not obvious. Therefore, Petitioner has not established that dependent claims 17, 20 and 21 are unpatentable.

V. Conclusion

Petitioner has failed to meet its burden of establishing that the Challenged Claims are unpatentable and the Petition should be denied for all claims.

Respectfully submitted,

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CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

The undersigned hereby certifies that the word count in this Patent Owner's Response is 6,960, as counted by the word-processing program Microsoft Word that was used to generate this Patent Owner's Response, where such word count excludes the table of contents, table of authorities, mandatory notices, certificate of service, appendix of exhibits, claim listing, and this certificate of word count. This Patent Owner Response is in compliance with the 14,000-word limit set forth in 37 C.F.R. § 42.24(b)(1).

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above document was served on January 22, 2025, by filing this document through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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