

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.

Petitioner,

v.

LIONRA TECHNOLOGIES LIMITED,

Patent Owner.

Case IPR2024-00734
U.S. Patent 7,632,518

PATENT OWNER'S SUR-REPLY

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Patent Trial and Appeal Board
U.S. Patent and Trademark Office
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TABLE OF PATENT OWNER'S EXHIBITS

Exhibit No.	Description
2001	Declaration of Dr. Eric Cole in support of Patent Owner's Response
2002	CV of Dr. Eric Cole, DPS

I. Introduction

Patent Owner respectfully requests that the Board find all of Petitioner's challenges to the claims of U.S. Patent No. 7,632, 518 ("the '518 Patent") without merit and reject the flawed arguments made in Petitioner's Reply to Patent Owner's Response ("Reply," Paper 13). With respect to Ground 1, this Board should disregard Petitioner's contentions that are premised on an unauthenticated publication that is apparently dated 2018, more than one decade after the April 8, 2004 filing date of the '518 patent and the April 20, 1999 filing date of U.S. Patent No. 6,651,096 ("Gai"). As discussed below, when all of the teachings of each reference are considered, it is apparent that the prior art references are directed at different layers of the OSI 7-layer reference model and a POSITA would not have been motivated to combine Layer 3 devices (e.g., Gai) with Layer 2 devices (e.g., Kwan). With respect to Ground 2, the question of whether "a" is treated as singular or plural depends heavily on the context of its use. *Tivo, Inc. v. Echostar Communications Corp.*, 516 F.3d 1290, 1303 (Fed. Cir. 2008). As discussed below, the claims and written description make clear that the singular meaning applies to "a memory circuit" in the '518 Patent.

Accordingly, for the reasons set forth below and in Paper 9, Patent Owner's Response, the Board should find that none of the challenged claims are unpatentable.

II. Ground 1: Claims 1 and 3 are Not Obvious over Gai, Yip, and Kwan.

Ground 1 fails because a POSITA would not have been motivated to combine U.S. Patent No. 6,651,096 to Gai et al. (Ex. 1006, “Gai”), U.S. Patent No. 8,751,647 to Yip et al. (Ex.1013, “Yip”), and U.S. Patent No. 7,523,485 to Kwan (Ex.1007, “Kwan”) to achieve the claimed inventions. *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”); *Virtek Vision Int'l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 888 (Fed. Cir. 2024).

As explained in the Response, a POSITA would have considered these references in the context of the layers of the Open Systems Interconnection (OSI) Reference Model and especially Layer 2, the data link layer, Layer 3, the network layer, and Layer 4, the transport layer. Paper 9, 7 (citing Ex. 2001, ¶ 51). “Various types of products are available for performing switching-related functions at various levels of the OSI model. Hubs or repeaters operate at layer one, and essentially copy and ‘broadcast’ incoming data to a plurality of spokes of the hub. Layer two switching-related devices are typically referred to as multiport bridges, and are capable of bridging two separate networks. Bridges can build a table of forwarding rules based upon which MAC (media access controller) addresses exist on which

ports of the bridge, and pass packets which are destined for an address which is located on an opposite side of the bridge. Bridges typically utilize what is known as the 'spanning tree' algorithm to eliminate potential data loops; a data loop is a situation wherein a packet endlessly loops in a network looking for a particular address. The spanning tree algorithm defines a protocol for preventing data loops. Layer three switches, sometimes referred to as routers, can forward packets based upon the destination network address. Layer three switches are capable of learning addresses and maintaining tables thereof which correspond to port mappings. Processing speed for layer three switches can be improved by utilizing specialized high performance hardware, and off loading the host CPU so that instruction decisions do not delay packet forwarding." Ex. 1010, U.S. Patent Publication No. 2001/0012294A1, [0006].

A. Gai is directed to a Layer 3 device and was intended to achieve higher switching speeds.

Petitioner's arguments that Gai is applicable to Layer 2 devices (Paper 13, Reply, 6-11) are not well-founded. Both Patent Owner and Dr. Cole addressed Gai's unexplained single-sentence assertion that Gai's invention may be utilized at layer 2. *See* Paper 9, Response, 10-11, Ex. 2001, Cole Decl., ¶54. Dr. Cole's agreement that Gai states what Gai states does not make Gai's teachings applicable to Layer 2

devices to a POSITA in 2004. *See* Paper 13, Reply, 6-7. Petitioner does not address Patent Owner's arguments (Paper 9, Response, 8-11) that Gai explicitly states that Gai's disclosure is directed to Layer 3 (or higher devices). *See* Paper 13, Reply, 9-10.

Petitioner's improper reliance on what appears to be an excerpt from a 2018 publication should be rejected by this Board. *See, e.g.,* Paper 13, Reply, 9-11; Ex. 1021, 2nd Crovella Decl., ¶¶ 8-10. As an initial matter, Exhibit 1022 is contrary to the Trial Practice Guide. "Petitioner may not submit new evidence or argument in reply that it could have presented earlier, e.g. to make out a prima facie case of unpatentability." *Patent Trial and Appeal Board Consolidated Trial Practice Guide* (November 2019), 73.

Moreover, Exhibit 1022 is objectionable for at least the following reasons. The exhibit, which is apparently dated 2018, is not relevant to any ground upon which trial was instituted under FRE 401 and 402. The exhibit's probative value to any ground upon which trial was instituted is substantially outweighed by the danger of unfair prejudice, confusing the issues, undue delay, wasting time, or needlessly cumulative evidence under FRE 403. The entirety of the exhibit is inadmissible hearsay to the extent it is offered for the truth of the matter asserted under FRE 802. Petitioner has not produced evidence sufficient to support a finding that the exhibit

is what Petitioner claims it is under FRE 901. The exhibit is, on its face, incomplete evidence under FRE 106.

At its core, Ex. 1022 is inadmissible hearsay from 2018 that Petitioner alleges describes a product from 1999 – the Cisco Catalyst 6000. There is nothing in Ex. 1022 to indicate that it is discussing the Cisco Catalyst 6000 in 1999. It appears more likely that Ex. 1022 does not, as it seems improbable that Cisco did not enhance and modify the Catalyst 6000 products over approximately 20 years. It should also be noted that Gai does not assert that Gai's disclosure was ever implemented in a Cisco Catalyst 6000. Gai, at most, asserts that “[a] suitable platform for intermediate network device 316 are the Catalyst 8500® series of switch routers and/or the Catalyst® 6000 family of multi layer switches both from Cisco Systems, Inc.” Ex. 1006, 6:62-65. Moreover, a POSITA would have understood that the term “multilayer switch” was used to refer to Layer-3 switches. “Layer-3 switches operate at the layer 3 of the OSI model and are based on routing technologies. They establish logical connections between ports based on network addresses. Use these for connecting different networks into an internetwork. Layer-3 switches are sometimes called routing switches or multilayer switches.”¹

¹ <https://www.cs.umd.edu/~meesh/cmssc411/website/proj01/pub/nine.html>

Gai, does, however, explicitly assert that “[p]referably, intermediate network device 316 is a layer 3 intermediate device...” *Id.*, 5:23-24. Accordingly, a POSITA considering the entire disclosure of Gai would understand that Gai’s teachings are directed to layer 3 devices.

B. Yip is directed to a Layer 3 device that does not teach using a MAC address in an ACL.

Yip is directed to completely blocking access to a port until a lengthy authorization process is completed. Yip teaches “control[ing] the admission of a user to a network by preventing a port through which the user connects to the network from forwarding data packets until the user is authorized. A network login controller operates in conjunction with a user interface to receive a user identification data from the port user. The network login controller further operates in conjunction with an authorization server to authenticate the user by sending a user authentication request containing the user identification data to the authentication server. The network login controller grants or denies permission to the user to access the network based on the user authentication response from the authentication server. If permission is granted, then the network login controller unblocks the port through which the user is connected to place it in packet-forwarding mode.” Ex. 1013, Abstract. Ex. 2001, ¶ 58.

Yip is not directed to access control lists and Yip's discussion of ACLs (or access lists) is in the background of the invention section of the patent specification. *See* Ex. 1013, 2:33-58. Yip does not disclose an ACL with a MAC address and Dr. Crovella is simply wrong when he asserts that "Yip's disclosure of an ACL including a MAC address means that the ACL is utilized at Layer 2." Paper 13, Reply, 12 (citing Ex. 1022, Crovella Decl.).

Yip teaches that "[o]ther prior art network security techniques have been implemented at a connection point (i.e. at the LAN switch level) to prevent intruder and hacker attacks. For example, algorithms and techniques have been designed and implemented in LAN switches to prohibit cyber-attacks, such as access control lists (ACLs), ..." Ex. 1013, 2:33-38. Yip also teaches that "access lists were developed to combat cyber-attacks on the LAN switch by providing an administrator-controlled list of Internet Protocol (IP) addresses or media access control (MAC) addresses that were authorized to access the network." *Id.*, 2:43-47 (emphasis added). Yip further notes that "[w]hen the targeted device is behind a firewall, an access list protects against such attacks by explicitly restricting inbound access to the device to **a select few IP addresses**." *Id.*, 2:52-55 (emphasis added).

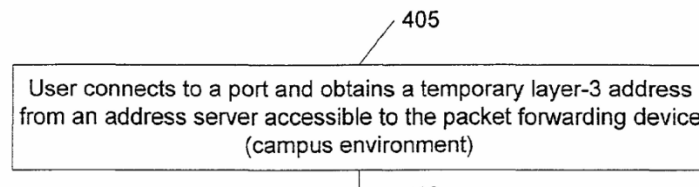
In fact, Yip teaches away from using MAC addresses, which are machine or hardware based. "A major drawback to access lists, DoS, and SYN attack

protections is that **access to the network is machine- or hardware-based** instead of user-based. Therefore, an unauthorized user who has access to an authorized machine can still gain access to the network, completely bypassing the intended security protection.” *Id.*, 2:56-61 (emphasis added).

Yip’s discussions of MAC addresses in alternate embodiments do not include using a MAC address in an access list. Yip simply teaches that “in an alternate embodiment, a static layer-2 address, such as the user's end station MAC address may be adequate for purposes of obtaining access to the network login controller 110 and user interface 120 on packet-forwarding device 200.” *Id.*, 6:23-28 (emphasis added). Yip teaches that a MAC address may be used as part of Yip’s process for obtaining a temporary IP address. “[P]rior to obtaining the user identification data 121, the end station/host computer H11 211 needs at least a temporary IP address to gain access to the network login controller 110 and associated user interface 120 on packet-forwarding device 200. In some cases the end station/host computer, e.g. H11 211, uses its MAC address, while in other cases the end station/host computer uses a previously obtained IP address, such as in the case of an Internet service provider environment where the user uses the same port and VLAN for authentication each time.” *Id.*, 7:66-8:8. Yip’s teaching that a MAC address may be used as part of the process of obtaining a temporary IP address taught

in, for example, block 405 of Yip's Figure 5, does not equate to using a MAC address in an access control list and a POSITA, especially in light of Yip's derogation of hardware-based access control, would not have considered that part of Yip's teachings.

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Ex. 1013, Fig. 5.

Accordingly, a POSITA considering the entire disclosure of Yip would understand that Yip's teachings are directed to layer 3 devices and incompatible with Layer-2 devices such as Kwan.

C. A POSITA would not have been motivated to combine Gai and Yip and Kwan to achieve the claimed invention.

Petitioner's reliance on "non-benefit-based rationales" (Paper 13, Reply, 12) is misplaced. As the Federal Circuit has noted, "obviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention." *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (emphasis added). "KSR did not do away with the requirement that there must exist a motivation to

combine various prior art references in order for a skilled artisan to make the claimed invention.” *Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 887 (Fed. Cir. 2024). The assertion that two elements were disclosed in the prior art and therefore known satisfies the motivation to combine analysis is an error as a matter of law. *Id.*, *Virtek Vision* at 888. “It does not suffice to simply be known. A reason for combining must exist.” *Id.*

Petitioner’s assertion that the Board should disregard all of what Yip teaches (Paper 13, Reply, 13) should be disregarded. “Even a single reference can include both types of statements [suggesting a combination and critiquing or otherwise discouraging the same], and [the Federal Circuit] have held that it is error to fail to consider the entirety of the art.” *Arctic Cat Inc. v. Bombardier Recreational Products Inc.*, 876 F.3d 1350, 1360 (Fed. Cir. 2017). *See also Chemours Co. FC, LLC v. Daikin Indus.*, 4 F.4th 1370 (Fed. Cir. 2021) (reversing Board decision where the motivation to combine analysis did not take into account express disclosure teaching away from the proposed combination).

For the reasons set forth above, Petitioner’s additional arguments regarding the Cisco Catalyst 6000 (Paper 13, Reply, 14-15) are misplaced and, in any event, the Cisco Catalyst 6000 is neither a patent nor a printed publication and is not part of the prior art appropriately considered in an Inter Partes Review. 35 U.S.C. §

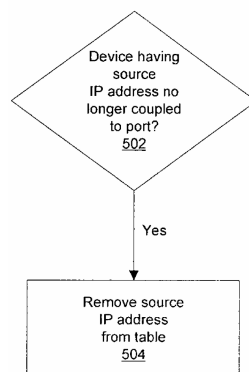
311(b) (“A petitioner in an inter partes review may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications.”).

In the Reply, Petitioner misapprehends or misrepresents Patent Owner's arguments regarding the combination of the Gai and Kwan references. A POSITA would consider all of Kwan's teachings, whether they support Petitioner's arguments or not. Petitioner does not dispute that Kwan teaches a lengthy and time-consuming process for learning the correct IP address. Ex. 2001, Cole Decl., ¶ 69. “[A] tiered, or delayed, approach is required to successfully detect the source IP address. This approach could allow for first identifying the MAC address and then waiting for an appropriate amount of time to learn the correct IP address.” Ex. 1007, Kwan, 6:5-8. Kwan also teaches that “[i]t is also advantageous to confirm that the learned IP address is correct by performing a reverse IP check.” *Id.*, 6:25-27. Petitioner instead asserts that this is not relevant to switching speeds of an already learned IP address. Paper 13, Reply, 18. However, Kwan teaches limiting the number of IP addresses associated with each port. *See* Ex. 2001, Cole Decl., ¶ 68. “Additional MAC address and IP address pairs will continue to be learned until the maximum number of MAC and IP Addresses is reached.” Ex. 1007, Kwan, 6:36-38. *See also Id.*, 6:60-7:5.

Petitioner does not address the fact that limiting the number of IP addresses for each port as Kwan teaches means that there would be a limited number of already learned IP addresses.

Moreover, Kwan also teaches dropping host devices with learned IP addresses, further limiting the number of IP addresses that have to be learned in the lengthy process Kwan teaches. “[T]he port security processor 242 will periodically poll ports for the learned IP addresses which are stored in the table to ensure that the host devices with the learned source IP addresses are still coupled to the port. (See FIG. 5 step 502). If it is determined that a host device having the learned source IP address is no longer coupled to a port then source IP address for the host that is no longer present can be removed from the table so as to allow a new source IP address to have access on the port. (See FIG. 5, step 504).” Ex. 1007, Kwan, 5:9-17.

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Ex. 1007, Kwan, Fig. 5. When all of the teachings of Kwan are considered along with all of the teachings of Gai, it is apparent that Kwan's teachings are incompatible with Gai's teachings and would, in fact, result in slower overall switching speeds.

For the reasons set forth above and in Paper 9, Response, because, *inter alia*, Gai and Yip are directed to Layer-3 devices and Kwan is directed to Layer-2 devices, a POSITA would not have been motivated to combine these references in order to achieve the claimed invention. Petitioner's arguments are improperly premised on cherry-picking portions of the prior art and disregarding those portions that teach away from their proposed combination of references.

III. Ground 2: Claims 15, 17, and 19-21 are Not Obvious over Gai, Kwan and Georgiou.

Petitioner essentially presents two counter-arguments to Patent Owner's contentions that the combination of Gai, Kwan and U.S. Patent No, 7,003,597 to Georgiou et al. (Ex. 1008, "Georgiou") would not achieve the claimed invention. Petitioner first argues that a POSITA would have ignored Georgiou's explicit teaching that "after reception of a packet from the network interface, the packet is typically temporarily stored in an inbound buffer in the network interface from where it is then transferred to memory to await subsequent processing." Ex. 1013, Georgiou, 3:18-22. *See* Paper 9, Reply, 22. Petitioner instead argues that only a few packets would be stored. *Id.* Petitioner cites to three portions of Gai in support of

this argument – Ex. 1006 1:22-27, 5:51-67, and 17:44-48. But the cited portions of Gai do not provide support for Petitioner's argument. The first citation is to a discussion of a typical network in the prior art. *See* Ex. 1006, Gai, 1:22-27. The second citation is to IEEE standards and a partial listing of the components preferably included in an intermediate network device. *See Id.*, 5:51-67. The third citation is to a listing of other possible actions that may be provided to the forwarding entity. *See Id.*, 17:44-48. Petitioner does not show where or how inbound packets would be temporarily stored in Petitioner's proposed combination. Petitioner also does not dispute that Gai does not disclose or teach a memory circuit operable to store memory packets. *See* Paper 9, Reply, 26.

Petitioner's second argument is that the claims are not limited to the recited elements. Specifically, Petitioner argues that “a memory circuit coupled to the forwarding circuit, the memory circuit operable to store packets and operable to store an enhanced access control list and a dynamic access control list;” as recited in claims 15 and 19 encompasses multiple memory circuits. *See* Paper 9, Reply, 22-26.

The question of whether “a” is treated as singular or plural in a patent claim limitation depends heavily on the context of its use. *See Norian Corp. v. Stryker Corp.*, 432 F.3d 1356, 1359 (Fed. Cir. 2005). The general rule that “a” or “an” in a

patent claim carries the meaning of “one or more” does not apply when the context clearly evidences that the usage is limited to the singular. *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1344 (Fed. Cir. 2008).

Where, as here, the claims and the written description make clear that the singular meaning applies, the claims should be interpreted accordingly. *See, e.g., Tivo, Inc. v. Echostar Communications Corp.*, 516 F.3d 1290, 1303 (Fed. Cir. 2008).

The '518 Patent specification discloses an Ethernet switch according to an embodiment of the claimed inventions using a functional block diagram in Figure 3 of the '518 Patent. Ex. 1001, 4:42-44.

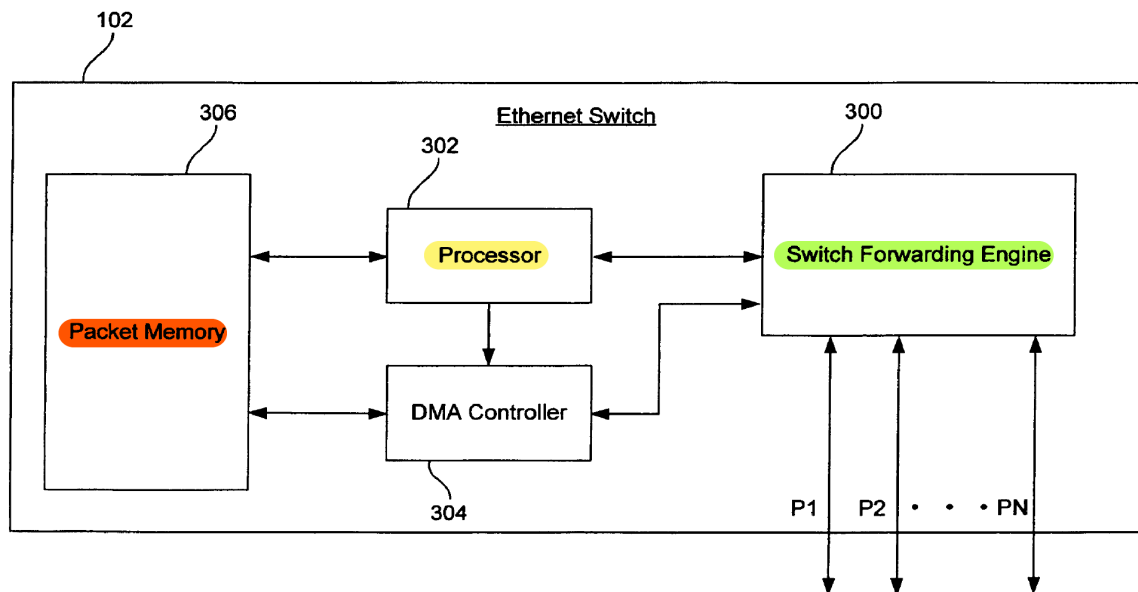


FIG. 3

Ex. 1001, Fig. 3 (annotated). The red Packet Memory 306 corresponds to the “memory circuit” in claims 15 and 19, the yellow Processor 302 corresponds to the

claimed “processor,” and the green Switch Forwarding Engine 300 corresponds to the claimed “forwarding circuit.”

“The switch 102 further includes a direct memory access (DMA) controller 304 that transfers the packets selected by the switch forwarding engine 300 to a packet memory 306. The selected packets are stored in the packet memory 306 for processing by the processor 302. Also stored in either the packet memory 306 or memory in the processor 302 is the enhanced access control list 108 (FIG. 2) along with required programming instructions for execution by the processor to control the overall operation of the switch 102. To store a selected packet from the switch forwarding engine 300, the processor 302 programs required registers in the DMA controller 304. The switch forwarding engine 300 then supplies the packet to the DMA controller 304 which, in turn, stores the packet in the packet memory 306. The processor 302 accesses the stored packets in the packet memory 306 along with the stored enhanced access control list 108 (FIG. 2) to generate the dynamic access control list 104 (FIG. 2).” Ex. 1001, 9:28-44. The dynamic access control list is stored in the memory circuit by the claimed processor “operable to process the specific packets stored in the memory circuit using the enhanced access control list to generate the dynamic access control list and store the dynamic access control list in the memory circuit, ...” Ex. 1001, 12:11-14, 44-47.

The written description in the '518 Patent is directed to a single memory circuit. As are the limitations of independent claims 15 and 19 which clearly recite a memory circuit coupled to a forwarding circuit and a processor wherein the packets and the enhanced and dynamic control lists are explicitly recited as being stored in the memory circuit.

The Federal Circuit teaches that the prosecution history is also relevant to this analysis in *Harari v. Lee*, 656 F.3d 1331, 1341 (Fed. Cir. 2011) (“[W]e [the Court of Appeals] read the limitation in light of the claim and specification to discern its meaning. *Insituform Techs., Inc. v. Cat Contracting, Inc.*, 99 F.3d 1098, 1105-06 (Fed. Cir. 1996) (analyzing the ‘claims, specification and file history’ to determine that ‘a vacuum cup’ means one and only one vacuum cup). When the claim language and specification indicate that ‘a’ means one and only one, it is appropriate to construe it as such even in the context of an open-ended ‘comprising’ claim.”).

The memory circuit limitation was emphasized during the prosecution of the '518 Patent. The applicant distinguished the cited prior art by, *inter alia*, arguing that “Droms does not disclose or suggest a memory circuit in a network switching circuit that is operable to store an enhanced access control list and a dynamic access control list. Droms also does not disclose or suggest a processor in a network switching circuit that processes specific packets stored in the memory circuit using

the enhanced access control list to generate the dynamic access control list.” Ex. 1002, Prosecution History, 102, 104. The applicant reiterated the argument later in the prosecution, arguing that “Droms also does not disclose or suggest a memory circuit in a network switching circuit that stores an enhance access control list and a dynamic access control list.” *Id.*, 140, 142.

Accordingly, the specification, claims, and prosecution history all show that “a” memory circuit should be construed as a single memory circuit in the challenged claims of the ’518 Patent. To do otherwise would invite legal error. *See, e.g., Wonderland Nursery Goods Co., Ltd. v. Baby Trend, Inc.*, 727 F. App’x 1017 (Fed. Cir. 2018) (reversing the PTAB after applying the proper claim construction using a singular “a” for claim interpretation).

Petitioner does not dispute that Petitioner points to 4 separate circuits in Gai for some of “a memory circuit” in independent claims 15 and 19 of the ’518 Patent.

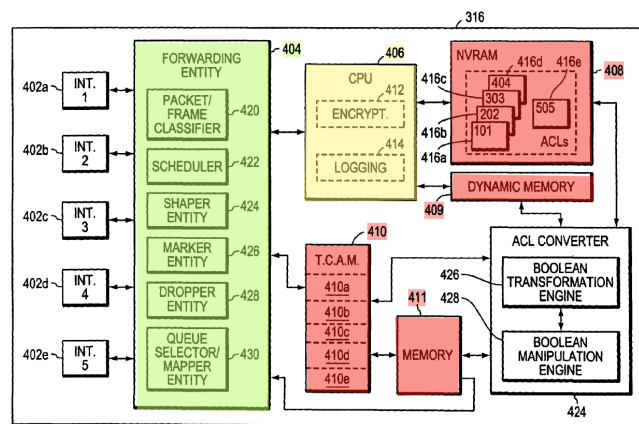


FIG. 4

Ex. 1006, Fig. 4 (annotated with yellow processor, green forwarding circuit and red memory circuit(s)). Petitioner also does not dispute that Gai does not a memory circuit operable to store packets.

A POSITA would have recognized that the different types of memory in Gai – non-volatile RAM, dynamic memory, and content addressable memory – could not be combined into a single memory circuit operable to store packets, enhanced control lists, and dynamic control lists. A POSITA would also have understood that Gai's four different memory circuits (or devices), along with a fifth memory circuit or device to store packets, would not correspond to a single memory circuit as recited in claims 15 and 19 of the Challenged Patent as Petitioner urges.

Accordingly, the non-volatile random access memory (NVRAM) 408, dynamic memory 409, TCAM 410, and memory 411 in Gai do not teach, suggest, or disclose the “memory circuit” limitations of claims 15 and 19 of the '518 Patent. Furthermore, a POSITA would have understood from the combined teachings of Gai and Georgiou that Gai and Georgiou do not teach, suggest or disclose the “memory circuit” limitations of claims 15 and 19 of the '518 Patent.

IV. Conclusion

Petitioner has failed to meet its burden of establishing that the Challenged Claims are unpatentable and the Petition should be denied for all claims.

Respectfully submitted,

Dated: June 11, 2025

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CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

The undersigned hereby certifies that the word count in this Patent Owner's Sur-Reply is 4,149, as counted by the word-processing program Microsoft Word that was used to generate this Patent Owner Sur-Reply, where such word count excludes the table of contents, table of authorities, mandatory notices, certificate of service, appendix of exhibits, claim listing, and this certificate of word count. This Patent Owner Sur-Reply is in compliance with the 5,600-word limit set forth in 37 C.F.R. § 42.24(c)(4).

Date: June 11, 2025

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

The undersigned hereby certifies that the above document was served on June 11, 2025, by filing this document through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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