

Cisco Systems, Inc.,
v.
Lionra Technologies Limited

IPR2024-00734, U.S. Patent No. 7,623,518

Patent Owner's Demonstrative Exhibits

July 14, 2025

Ex. 2003

'518 Patent, Claim 1

- [1.0] A method of developing an access control list, comprising:
 - [1.1] a developing an enhanced access control list including data related to at least one of user names, DNS names, Windows domain names, and physical addresses;
 - [1.2.1] converting, in a network switch, at least one of;
 - [1.2.2] user names into corresponding IP and physical addresses according to data in the enhanced access control list, wherein converting user names into corresponding IP and physical addresses according to data in the enhanced access control list includes: detecting login packets being communicated over the network; determining a MAC address from the login packets; detecting server message block login packets being communicated over the network; determining an IP address from the server message block login packets; and developing records in the access control list using the obtained IP address for the respective user name;
 - [1.2.3] DNS names into corresponding IP addresses according to data in the enhanced access control list; and,
 - [1.2.4] physical addresses into IP addresses according to data in the enhanced access control list; and;
 - [1.3] developing, in the network switch, the access control list from each of the operations of converting.

'518 Patent, Claim 1; Ex. 1001, 10:12-37

'518 Patent, Claim 15

[15.0] A network switching circuit, comprising:

[15.1.1] a forwarding circuit operable to detect specific received packets and

[15.1.2] to provide the specific packets on a processor port, and

[15.1.3] further operable to receive packets on one of a plurality of ports including the processor port

[15.1.4] and to forward each received packet to a port corresponding to a destination address contained in the packet

[15.1.5] subject to access restrictions contained in a dynamic access control list;

[15.2.1] a memory circuit coupled to the forwarding circuit,

[15.2.2] the memory circuit operable to store packets and

[15.2.3] the memory circuit ... operable to store an enhanced access control list and

[15.2.4] the memory circuit ... operable to store ... a dynamic access control list; and

[[15.3.1] a processor coupled to the forwarding circuit and the memory circuit,

[15.3.2] the processor operable to define the specific packets detected by the forwarding circuit and

[15.3.3] the processor...operable to process the specific packets stored in the memory circuit using the enhanced access control list to generate the dynamic access control list and

[15.3.4] the processor ... operable ... to store the dynamic access control list in the memory circuit, and

[15.3.5] the processor...further to provide the specific packet to the processor port of the forwarding circuit after processing the packets.

'518 Patent, Claim 15; Ex. 1001, 11:57-12:17

'518 Patent, Claim 19

- [19.0] A computer network, comprising:
 - [19.1.1] a network switch including,
 - [19.1.2] a forwarding circuit operable to detect specific received packets and
 - [19.1.3] to provide the specific packets on a processor port, and
 - [19.1.4] further operable receive packets on one of a plurality of ports including the processor port and
 - [19.1.5] to forward each received packet to a port corresponding to a destination address contained in the packet
 - [19.1.6] subject to access restrictions contained in a dynamic access control list;
 - [19.2.1] a memory circuit coupled to the forwarding circuit,
 - [19.2.2] the memory circuit operable to store packets and
 - [19.2.3] the memory circuit ... operable to store an enhanced access control list and
 - [19.2.4] the memory circuit ... operable to store ... a dynamic access control list; and
 - [19.3.1] a processor coupled to the forwarding circuit and to the memory circuit,
 - [19.3.2] the processor operable to define the specific packets detected by the forwarding circuit and
 - [19.3.3] operable to process the specific packets stored in the memory circuit using the enhanced access control list to generate the dynamic access control list and
 - [19.3.4] the processor ... operable ... to store the dynamic access control list in the memory circuit, and
 - [19.3.5] the processor...further to provide the specific patent to the processor port of the forwarding circuit after processing the packets; and
- [19.4] a plurality of hosts, each host coupled to a respective port of the network switch.

'518 Patent, Claim 19; Ex. 1001, 12:27-12:52

Summary of Why The Petition Fails

- It would not have been obvious to a POSITA to combine Gai, Yip, Kwan and Georgiou's disparate memories into the memory circuit recited in claims 15, 17, and 19-21.
- A POSITA would not have been motivated to combine the Gai, Yip and Kwan prior art references to achieve the [dynamic] control list limitations of independent claims 1, 15 and 19.
 - Gai is directed to OSI Layer 3 (Network Layer) devices and was solving the problem of slow switching by achieving higher switching speeds.
 - Yip is directed to an OSI Layer 3 (Network Layer) devices and was focused on Layer 3 IP addresses and not Layer 2 hardware (e.g., MAC) addresses.
 - Kwan is directed to an OSI Layer 2 (Data Link Layer) with limited connectivity of one host per port.

Paper 9, 7-33; Paper 18, 2-19

Ground 2: The Prior Art Does Not Disclose, Teach or Suggest the Claimed Memory Circuit

The '518 Patent Discloses a Single Memory Circuit

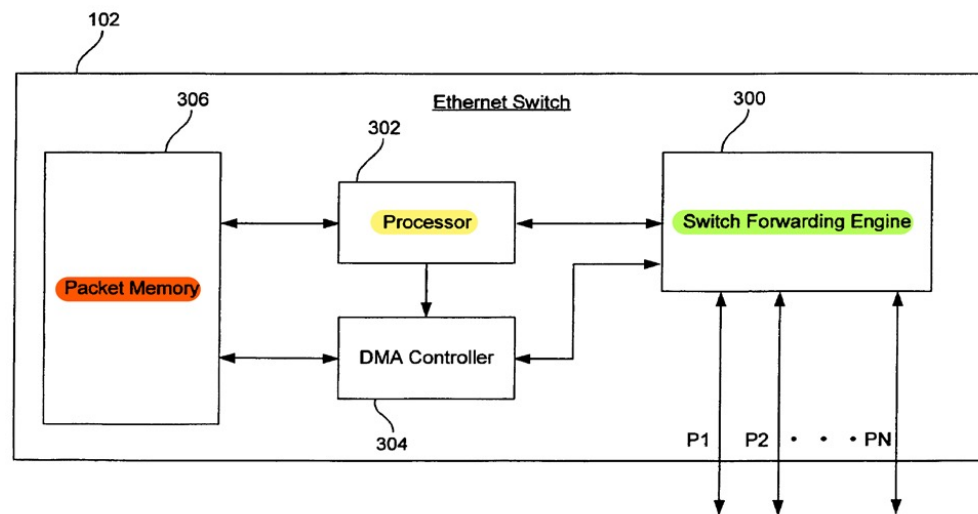


FIG. 3

- The '518 Patent discloses a **Packet Memory 306** corresponding to the “memory circuit” in independent claims 15 and 19.

Paper 9, 4-5, Ex. 2001, ¶¶48-49; Paper 18, 15-17

The '518 Patent Discloses a Single Memory Circuit

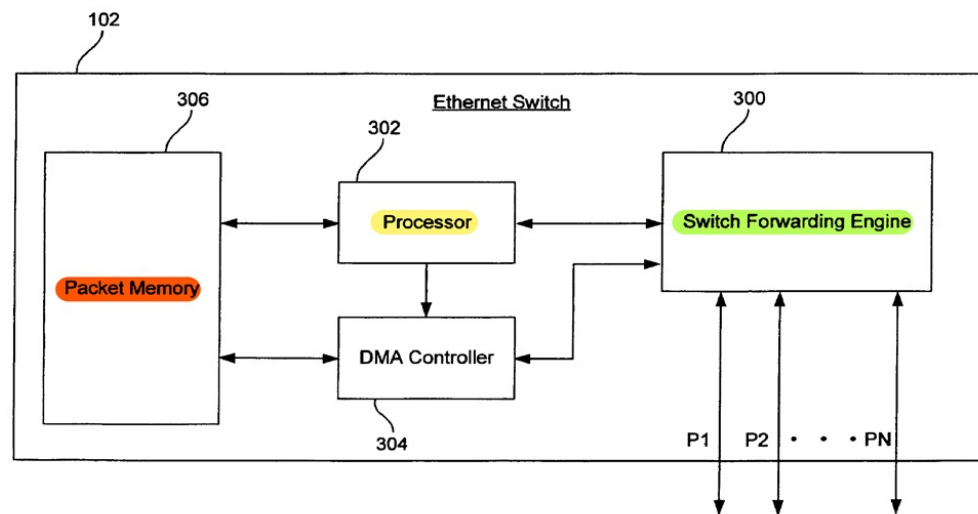


FIG. 3

- **Packet Memory 306** stores selected packets, an enhanced access control list 108 and a dynamic access control list.

Paper 9, 4-5, Ex. 2001, ¶¶48-49; Paper 18, 15-17

The '518 Patent Discloses a Single Memory Circuit

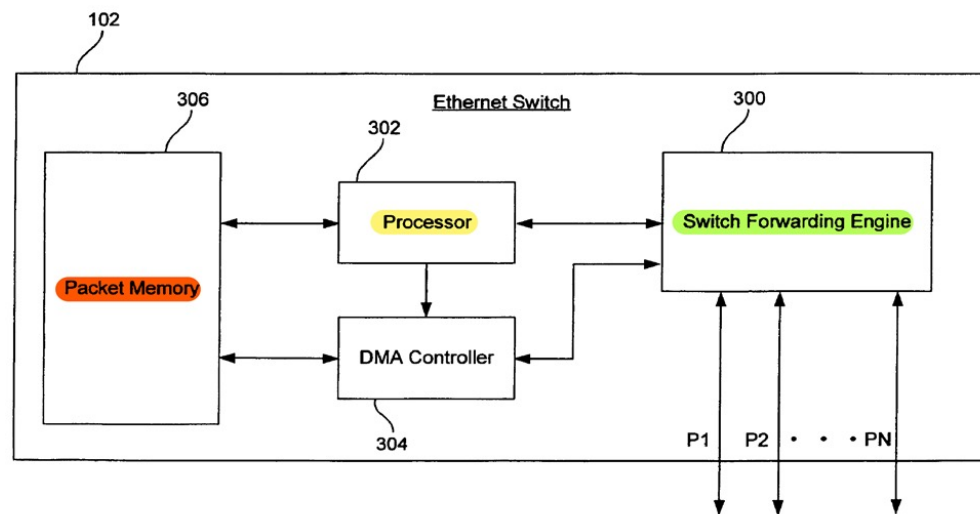


FIG. 3

- **Packet Memory 306** stores selected packets, an enhanced access control list 108 and a dynamic access control list.

Paper 9, 4-5, Ex. 2001, ¶¶48-49; Paper 18, 15-17

“A memory circuit” was emphasized during prosecution.

- The applicant emphasized a single memory circuit.
- “Droms does not disclose or suggest a memory circuit in a network switching circuit that is operable to store an enhanced access control list and a dynamic access control list. Droms also does not disclose or suggest a processor in a network switching circuit that processes specific packets stored in the memory circuit using . the enhanced access control list to generate the dynamic access control list.”
- “Droms also does not disclose or suggest a memory circuit in a network switching circuit that stores an enhance access control list and a dynamic access control list.”

Paper 18, 17-18; Ex. 1002, 102, 104, 140, 142

Claims 15 and 19 Have Identical Memory Circuit Limitations

- a memory circuit coupled to the forwarding circuit, the memory circuit operable to store packets and operable to store an enhanced access control list and a dynamic access control list; and
- a processor coupled ... to the memory circuit, the processor operable to ... process the specific packets stored in the memory circuit ... and store the dynamic access control list in the memory circuit,

'518 Patent, Claim 15, Ex. 1001, 12:4-14; Claim 19, Ex. 1001, 12:37-47

The '518 Patent specification, claims and prosecution history are directed to a single memory circuit

- The relevant context for singular usage of “a” in a claim is the patent specification, claims and prosecution history.
 - The question of whether “a” is treated as singular or plural in a patent claim limitation depends heavily on the context of its use.
 - The general rule that “a” or “an” in a patent claim carries the meaning of “one or more” does not apply when the context clearly evidences that the usage is limited to the singular.
 - Where the claims and the written description make clear that the singular meaning applies, the claims should be interpreted accordingly.

Paper 18, 14-15; *Norian Corp. v. Stryker Corp.*, 432 F.3d 1356, 1359 (Fed. Cir. 2005); *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1344 (Fed. Cir. 2008); *Tivo, Inc. v. Echostar Communications Corp.*, 516 F.3d 1290, 1303 (Fed. Cir. 2008)

In the '518 Patent claims, “a memory circuit” means one and only one memory circuit

- When the claim language and specification indicate that ‘a’ means one and only one, it is appropriate to construe it as such even in the context of an open-ended ‘comprising’ claim.
 - *Insituform Techs., Inc. v. Cat Contracting, Inc.*, 99 F.3d 1098, 1105-06 (Fed. Cir. 1996) (analyzing the ‘claims, specification and file history’ to determine that ‘a vacuum cup’ means one and only one vacuum cup).
 - a memory circuit coupled to the forwarding circuit, the memory circuit operable to store packets and operable to store an enhanced access control list and a dynamic access control list;
 - a processor coupled to the forwarding circuit and to the memory circuit, the processor operable to ... store the dynamic access control list in the memory circuit
 - ...

Paper 18, 17; '518 Patent, Claim 15, Ex. 1001, 12:4-14; Claim 19, Ex. 1001, 12:37-47.

The prior art (Gai) discloses 4 separate memory circuits.

- The prior art discloses four memory circuits (in red).

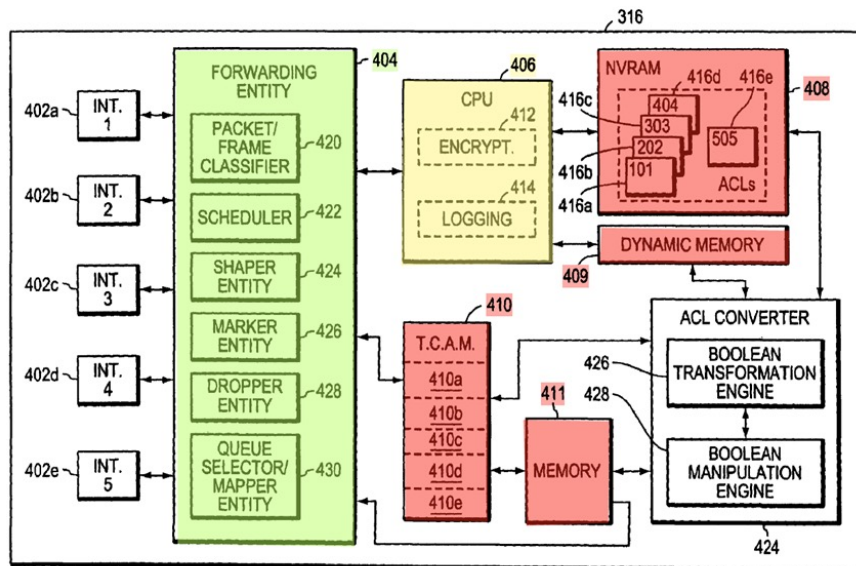


FIG. 4

FIG. 4 is a partial block diagram of the intermediate network device 316. Device 316 preferably includes a plurality of interfaces 402a–402e that provide connectivity to the network 300. That is, interfaces 402a–402e are in communication with LANs 302 and 304 and Internet 318. Each interface 402a–e, moreover, may be associated with one or more physical ports (not shown). Device 316 further includes at least one forwarding entity 404, a central processing unit (CPU) 406, non-volatile random access memory (NVRAM) 408, dynamic memory 409 and at least one content addressable or associative memory 410. The associative memory 410 is preferably a ternary content addressable memory (TCAM), and its cells (not shown) may be associated with or assigned one of three values, such as “0”, “1” or “don’t care”. Associated with and coupled to the TCAM 410 is another memory device 411, such as a dynamic random access memory.

Gai discloses 4 separate memory circuits.

- Gai discloses a yellow processor, green forwarding entity, and 4 red memory circuits.
 - Gai's processor is coupled to NVRAM and dynamic memory
 - Gai's forwarding entity is coupled to TCAM and memory 411
 - Gai's NVRAM is not operable to store packets.
 - Gai's TCAM is not operable to store packets.
 - Gai's CPU and Forwarding Entity are coupled to different memory circuits.

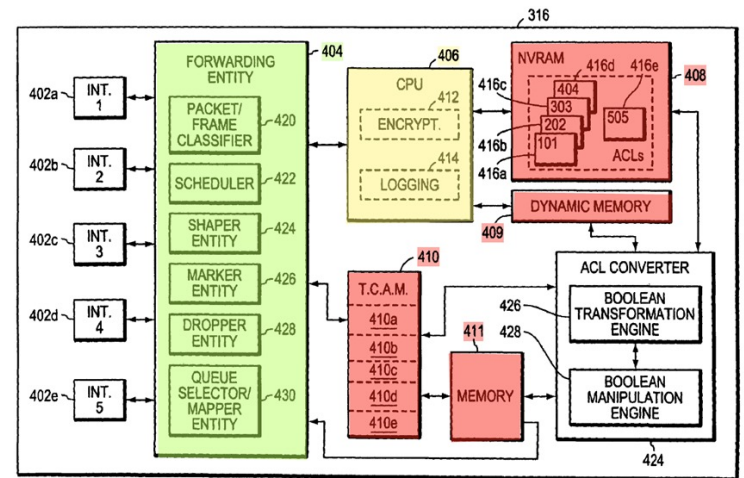


FIG. 4

Paper 9, 28-33; Ex. 1006, Fig. 4

Gai's 4 memory circuits do not disclose, teach or suggest a memory circuit operable to store packets and access lists.

- Gai 4 red memory circuits are not coupled to both the CPU and the Forwarding Entity and are not operable to store packets and access lists as claimed in the '518 Patent.
 - a memory circuit coupled to the forwarding circuit, the memory circuit operable to store packets and operable to store an enhanced access control list and a dynamic access control list;
 - a processor coupled to the forwarding circuit and to the memory circuit, the processor operable to ... store the dynamic access control list in the memory circuit ...

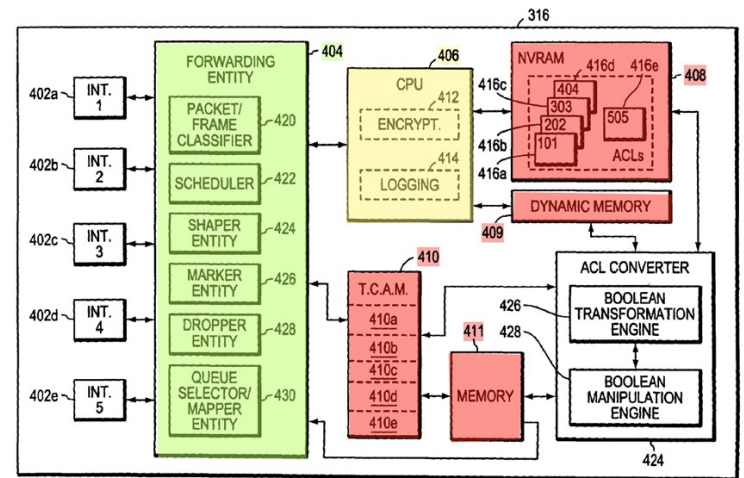


FIG. 4

Paper 9, 28-33; Ex. 1006, Fig. 4

The prior art does not disclose “a memory circuit” as claimed in claims 15 and 19 of the '518 patent.

- Because neither Gai nor Gai in combination with any of the cited references discloses “a memory circuit” storing packets and access lists, the prior art does not disclose, teach or suggest independent claim limitations 15.2.1-15.2.4, 15.3.1, 15.3.4, 19.2.1-19.2.4, 19.3.1, or 19.3.4 the '518 Patent.
- Because the prior art does not teach limitations of independent claims 15 and 19, it does not render obvious dependent claims 17 and 20-21.
- *Synqor, Inc. v. Artesyn Techs., Inc.*, 709 F.3d 1365, 1375 (Fed. Cir. 2013) (“Th[e] court need not consider Defendants’ arguments that certain dependent claim limitations would have been obvious where the base claim has not been proven invalid.”).
- *Callaway Golf Co. v. Acushnet Co.*, 576 F.3d 1331, 1344 (Fed. Cir. 2009) (a judgment is irreconcilably inconsistent where a dependent claim is found obvious and the independent claim from which it depends is nonobvious).

Paper 9, 20, 32.

Ground 1-4: A POSITA Would Not Have Combined the Gai, Yip and Kwan References

A POSITA Would Not Have Combined Prior Art References Directed to Different System Interconnection Layers

- A POSITA would have considered the Gai, Yip and Kwan references in the context of the layers of the Open Systems Interconnection (OSI) Reference Model and especially Layer 2, the data link layer, Layer 3, the network layer, and Layer 4, the transport layer.
- Gai is directed to a Layer 3 device.
- Yip is directed to a Layer 3 device.
- Kwan is directed to a Layer 2 device.

Preferably, intermediate network device **316** is a layer **3** intermediate device and thus operates up to the network layer of the communication protocol stack implemented within the network **300**. For example, device **316** preferably includes an Internet Protocol (IP) software layer. Device **316** may also implement network services such as route processing, path determination and path switching functions.

Ex. 1006, Gai, 5:23-29

Paper 9, 7; Ex 2001, ¶ 51; Ex. 1006, 5:23-29.

Gai is directed to a Layer 3 (Network) Device

- Gai discloses a Layer 3 intermediate device that communicates with the Internet.
 - A POSITA would have considered Gai in the context of Gai's discussion of intermediate devices and Gai's depiction of its preferred embodiment 316.
 - A POSITA would have understood that the access control lists in Gai were directed to Layer 3 switching.
 - A POSITA would have considered Gai's stated goals of processing messages much more quickly and achieving much higher switching speeds than prior art devices.

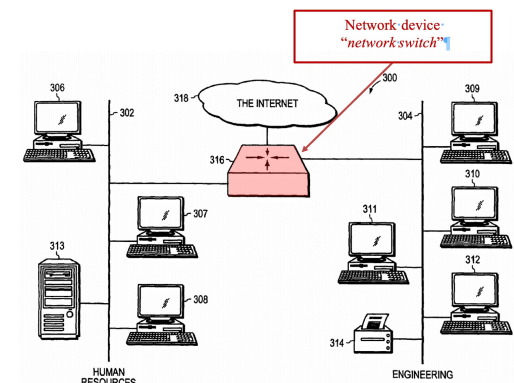


FIG. 3

Ex.1006, Fig. 3 (annotated).

intermediate devices, commonly referred to as routers, may operate at higher communication layers, such as layer 3, which in TCP/IP networks corresponds to the Internet Protocol (IP) layer. IP message packets include a corresponding header which contains an IP source address and an IP destination address. Routers or layer 3 switches may re-assemble or convert received data frames from one LAN standard (e.g., Ethernet) to another (e.g. Token Ring). Thus, layer 3 devices are often used to interconnect dissimilar subnetworks. Some layer 3 intermediate network devices may also examine the transport layer headers of received messages to identify the corresponding TCP or UDP port numbers being utilized by the corresponding network entities.

Paper 9, 6-11; Ex 2001 ¶¶ 52, 55-56; Ex. 1006, 2:9-24.

Yip is directed to a Port-Blocking Layer 3 (Network) Device

- Yip teaches completely blocking access until completion of a lengthy authorization process.
- Yip teaches temporary IP address assignment.
- Yip only references MAC addresses in alternate embodiment, but does not discuss when, why or how a MAC address could be used.
- Yip teaches away from using MAC addresses.

A method and apparatus is provided to control the admission of a user to a network by preventing a port through which the user connects to the network from forwarding data packets until the user is authorized. A network login controller operates in conjunction with a user interface to receive a user identification data from the port user. The network login controller further operates in conjunction with an authorization server to authenticate the user by sending a user authentication request containing the user identification data to the authentication server. The network login controller grants or denies permission to the user to access the network based on the user authentication response from the authentication server. If permission is granted, then the network login controller unblocks the port through which the user is connected to place it in packet-forwarding mode. If permission is denied, then the port remains in packet non-forwarding mode (i.e. it remains blocked).

A major drawback to access lists, DoS, and SYN attack protections is that access to the network is machine- or hardware-based instead of user-based. Therefore, an unauthorized user who has access to an authorized machine can still gain access to the network, completely bypassing the intended security protection.

Paper 9, 12-14; Paper 18, 6-8; Ex 2001 ¶¶ 58-60; Ex. 1013, Abstract; 2:56-61.

A POSITA Would Not Have Been Motivated to Combine Gai and Yip

- A POSITA would not look to Yip's teaching of blocking a port until a lengthy authentication process had been completed in connection with Gai's teaching of high-speed network switching.
- Blocking one or more ports for an indeterminate time would be antithetical to Gai's goal of higher switching speeds and faster processing of messages.
- High speed switching and message processing is incompatible with preventing access to the port until completion of a lengthy authorization process.

Paper 9, 14-16, Ex 2001 ¶¶ 61-64.

Kwan is directed to a Layer 2 (Data Link) Device

- Kwan discloses a Layer 2 network device that communicates with the Internet.
 - Kwan contemplates limiting each port to a single host and limiting the number of IP addresses associated with each port.
 - Kwan discloses and teaches a lengthy and time-consuming process for learning an IP address.
 - A POSITA would have considered Kwan's limited number of associated IP addresses and lengthy learning incompatible with Gai's stated goals of processing messages much more quickly and achieving much higher switching speeds than prior art devices.

FIG. 2 shows a view of an embodiment of a network device **200** of the present invention. This network device provides layer 2 switching functions.

The network device **200** contains a processing device which operates to analyze data, packets received on a port to identify the MAC address of the host sending the data packet. Each data packet can include at least the MAC address of the device sending the data packet (source MAC address) and the MAC address of the device to which the data packet is to be sent to (destination MAC address). As discussed above

In addition to the above, it should be recognized that care must be taken to learn the correct source IP address. For example, in order to support delayed technologies, such as the widely known IEEE 802.1X standard which may postpone IP Address assignment until the port is authenticated, a tiered, or delayed, approach is required to successfully detect the source IP address.

Paper 9, 16-19; Paper 18, 6-9; Ex 2001 ¶¶ 66-73; Ex. 1007, 3:42-45, 3:59-64, 6:1-7

A POSITA Would Not Have Been Motivated to Combine Gai and Yip and Kwan

- A POSITA would not have been motivated to combine Gai, Yip and Kwan because they are directed to different Layers of the OSI Reference Model.
- A POSITA would have considered the drawbacks combining Yip and Kwan's lengthy authentication processes with Gai's stated goals of higher switching speeds and faster processing of messages.
- A POSITA would not have considered blocking ports and limited IP address association compatible with Gai's interworking device trying to achieve higher switching speeds and faster processing of messages.

Paper 9, 7-20, Paper 18, 2-13