

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,
Petitioner

v.

LIONRA TECHNOLOGIES LTD.,
Patent Owner.

IPR2024-00734
Patent 7,623,518 B2

Record of Oral Hearing
Held: July 14, 2025

Before ANNETTE R. REIMERS, STEVEN M. AMUNDSON, and
RUSSELL E. CASS, Administrative Patent Judges.

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The above-entitled matter came on for hearing Monday,
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P-R-O-C-E-E-D-I-N-G-S

11:00 a.m.

JUDGE AMUNDSON: Good morning. I'm Judge Amundson, and with me on the panel are Judges Reimers and Cass. We have our final hearing in IPR2024-00734 involving US Patent No. 7,623,518 between Cisco Systems, Inc., as the Petitioner, and Lionra Technologies Limited, as the Patent Owner. Let's get the parties' appearances. Who do we have for the Petitioner?

MR. FOSTER: Good morning, Your Honors. My name is Theodore Foster for Petitioner, Cisco Systems. With me is my co-counsel, Gregory Huh, and Mr. Huh will be presenting on behalf of Cisco today.

JUDGE AMUNDSON: Very well, thank you. And who do we have for the Patent Owner?

MR. AUCHTER: Good morning, Your Honor. Robert Auchter with Auchter PLLC. I am here on behalf of Patent Owner, Lionra Technologies. Possibly on the line with me, as well, would be backup counsel Mr. Brett Cooper, BC Law Group. I'm not sure if he was able to make it or not.

JUDGE AMUNDSON: All right, very well. Thank you. So, well, welcome to everyone. Because we are conducting the hearing by video, we wanted to start by addressing a few items. First, our main concern is your right to be heard. So, if at any time during the hearing you encounter technical or other difficulties that you feel undermine your ability to adequately represent your client, please let us know

1 immediately. For example, by contacting the team members who
2 provided you with the connection information. Second, when not
3 speaking, please mute yourself. Third, please identify yourself each
4 time you speak. This will help the court reporter prepare an accurate
5 transcript.

6 Fourth, we have the entire record, including the demonstratives.
7 When referring to a demonstrative or an exhibit or a paper, please do
8 so by identifying the slide or page number. Also, please pause a little
9 after identifying the slide or page number to give others time to find it.
10 Fifth, there is a public line for people to call in and listen to the
11 hearing. Sixth, we set forth the procedure for today's hearing in the
12 Order Granting the Requests for Oral Argument, that's Paper 17, but
13 just to remind everyone the way this will work, the Order Granting the
14 Requests for Oral Argument provided that each side will have 45
15 minutes of total argument time to present arguments.

16 Petitioner bears the ultimate burden of proof, and Petitioner will
17 go first. Petitioner may reserve time for rebuttal. Patent Owner will go
18 next. Patent Owner may reserve time for surrebuttal, but Patent
19 Owner's surrebuttal must be limited to the issues in Petitioner's
20 rebuttal. Also, please do not interrupt the other party while that party
21 is presenting its argument. If you have an objection, please raise it
22 during your argument. I will keep time, and I will try to give you a
23 warning when you're nearing the end of your time. So, with that said,
24 are there any questions? All right, it looks like there are no questions.
25 All right, so Mr. Huh, would you like to reserve any time for rebuttal?

1 MR. HUH: Yes, Your Honor, we'd like to reserve 20 minutes
2 for rebuttal.

3 JUDGE AMUNDSON: So, you may begin your argument
4 whenever you're ready.

5 MR. HUH: Thank you and good morning, Your Honors. On the
6 record, this is Gregory Huh on behalf of Petitioner, Cisco Systems,
7 Inc., as noted in IPR2024-00734. If we turn to Petitioner's slides at
8 Slides 2 and 3. For reference, I've provided a copy of the Independent
9 Claim 1, as well as Independent Claim 15 that I'll be addressing
10 today. Independent Claim 1 is a method claim and Claim 15 is a
11 device claim. With respect to Independent Claim 1, I would just
12 briefly note that Patent Owner did not dispute that the claimed
13 elements are present in the prior art, but only presents arguments
14 regarding the proposed combination.

15 With respect to Independent Claim 15 on Slide 3, the main
16 arguments from Patent Owner are with respect to the memory circuit
17 limitation, and that's the second limitation in Claim 15, which is a
18 memory circuit, et cetera. If we turn to Slide 4, I've outlined four key
19 points for discussion. First, I'll address the motivation to combine Gai
20 and Yip, which pertains to Independent Claim 1. Turning to Slide 5,
21 the Petition at Pages 15, and for example 25 to 32, explained how the
22 combination of Gai and Yip discloses in Claim 1 an enhanced access
23 control list, including data related to physical addresses.

24 So, on Slide 5, for example, we have a portion of Gai. On the
25 left is Gai's -- it's a device that's a switch, and Gai calls that

1 intermediate network device 316. And the Petition explained how Gai
2 discloses that the intermediate network device is a multilayer switch
3 that includes an access control list that's initially provided by the
4 administrator. This would be, for example, on Slide 5 on the right, we
5 have a relevant portion of Gai Exhibit 1006, Column 7, 15-21,
6 describing the access control list. That initial access control list
7 provided is enhanced because it has additional features that it
8 facilitates.

9 That's not in dispute between the parties, and we explained that
10 that access control list corresponds to the enhanced access control list.
11 Now, if we turn to Slide 6, Yip complements the Gai reference by
12 disclosing that it was known in the art for access control lists to
13 include MAC addresses provided by the administrator. So, on Slide 6,
14 for example, we have Yip Exhibit 1013, Column 2, 43-47. Now in
15 view of the combined teachings, if we turn to Slide 7 --

16 JUDGE AMUNDSON: This is Judge Amundson. I just had a --

17 MR. HUH: Yes.

18 JUDGE AMUNDSON: I'm just trying to understand the
19 proposed combination.

20 MR. HUH: Sure.

21 JUDGE AMUNDSON: And I wasn't really clear about what
22 Yip adds to Kwan. And is it that Kwan teaches filtering based on IP
23 address/MAC address pairs and Yip teaches filtering based on just
24 MAC addresses?

1 MR. HUH: Right, so really the Kwan reference supplements
2 Yip by teaching that when you have a MAC address you can learn a
3 new IP address based on a known MAC address. So, for example, if
4 you have DHCP and Yip -- I mean, Kwan provides various ways of
5 learning IP addresses that are new. One example would be DHCP
6 assigned IP address is used, is learned, based on a known MAC
7 address. So, Kwan provides teachings relevant to the dynamic access
8 control list, whereas Yip teaches, for example, that the administrator-
9 created access control list was known to have a MAC address.

10 So, if you go back to Slide 6, the relevant portion of Yip
11 teaches that the access lists provided by the administrator were known
12 to have MAC addresses. If we go back to Slide 5, Your Honor, we
13 had mapped the initially administrator-created access control lists as
14 the enhanced access list. So, what you have is, Gai teaches that an
15 administrator creates an access control list with various types of
16 information, and Yip complements that by teaching that the
17 administrator -- it was known in the art for the administrator to also
18 include MAC addresses in that initial access control list.

19 JUDGE AMUNDSON: All right, thank you. I think I
20 understand your position.

21 MR. HUH: Okay, and then really Kwan relates to when you
22 update and generate a dynamic access control list limitation in the
23 claim, it tells you how to do that. So, if we just step back to Slide 7, in
24 view of the combined teachings, we explain, as shown on Slide 7, Dr.
25 Crovella's testimony in his Exhibit 1003 at Paragraph 57, exemplary

1 reasons to combine the teachings of Yip and Gai, including to restrict
2 or permit access based on MAC addresses, which would facilitate
3 improved security. But I would note that the Petition also provided,
4 for example on Page 29, and this might go to what Your Honor was
5 discussing, which is, for example, we explained that the MAC address
6 that's initially provided by the administrator, facilitates automatically
7 learning new IP addresses per Kwan.

8 There is a relationship between the initially provided MAC
9 address because now it facilitates the subsequent learning of a new IP
10 address. That would be another reason to combine Yip with Gai,
11 because it facilitates downstream improvements on learning IP
12 addresses. We also provided in our Petition, Your Honor, reasons to
13 combine that do not require benefit. Now, any one of those reasons to
14 combine would be sufficient to implement the proposed combination
15 of Gai and Yip as presented in the Petition.

16 If we turn to Slide 8, the Petition, and in fact, both experts agree
17 that a person in the art would have been able to implement the
18 proposed combination with the expectation of success. On Slide 8, we
19 have Dr. Crovella's testimony, which is Petitioner's expert, on this
20 point. And he, also, cites a number of evidentiary references, for
21 example, Exhibits 1014, 1017 and 1018, illustrating that it was known
22 in the art to utilize MAC addresses in access control lists. That was
23 knowledge in the art as evidenced by Dr. Crovella's testimony. On
24 this same point during deposition, Dr. Cole, Patent Owner's expert, as
25 shown on the right of Slide 8, Dr. Cole's testimony in Exhibit 1021,

1 Page 50, 22-51, Line 6, conceded that it was known in the art for
2 access control lists to include MAC addresses.

3 Both experts support a reasonable expectation of success in
4 utilizing MAC addresses in Gai's access control list. Now turning to
5 Slide 9, I want to note that Patent Owner attempts to distinguish the
6 proposed combination by arguing that the teachings of Gai and Yip
7 are not combinable because allegedly Gai is directed to Layer 3
8 switching. This is, for example, in Patent Owner's Response at Page
9 11. We can see that that's simply incorrect, Your Honors. Gai is not
10 limited or directed only to Layer 3 switching. On the right side of
11 Slide 9, we have relevant portions of Gai, for example, Gai 5:22-47.
12 And we can see the initially quoted portion that we have on the slide,
13 and I'll read it in the record.

14 It states, intermediate network device 316 is a Layer 3
15 intermediate device and thus operates up to the network layer. So first,
16 I would note that this portion does not limit it to Layer 3, but actually
17 up to Layer 3, which then would include Layer 2 underneath it. But to
18 remove any doubt that Gai, in fact, contemplates that its invention
19 would be applicable to Layer 3, I mean Layer 2, we have the
20 subsequent portion on Slide 9 at the bottom, which makes clear that
21 Gai's invention is not limited to Layer 3 and may be utilized Layer 2
22 intermediate devices. So, Patent Owner's assertion that Gai was
23 directed to Layer 3 switching is simply incorrect and actually ignores
24 the express teachings of Gai.

1 JUDGE AMUNDSON: This is Judge Amundson. I'm just
2 trying to understand --

3 MR. HUH: Sure.

4 JUDGE AMUNDSON: -- this, and so if I could get Cisco's
5 position on this. I don't really understand the difference between a
6 Layer 3 device and a Layer 2. Is it that the Layer 3 device filters based
7 on IP addresses and the Layer 2 device filters based on MAC
8 addresses, or is there something else that is relevant in distinguishing
9 Layer 3 from Layer 2?

10 MR. HUH: What I would say is that this is Patent Owner's
11 argument that's really ambiguous as to what they're trying to
12 distinguish here, but my understanding of how you've summarized it
13 is correct, Your Honors. It appears to us that Patent Owner is asserting
14 that Gai is directed to Layer 3 and therefore would not be able to filter
15 based on MAC addresses because MAC addresses are at Layer 2.
16 That's our understanding of Patent Owner's arguments, but frankly,
17 they're ambiguous. But what we do know for sure is that Patent
18 Owner's assertion that Gai is directed to Layer 3 is incorrect, and all
19 of their arguments regarding the proposed combination, for example,
20 that Gai would not be able to filter at Layer 2 with access control lists,
21 is premised on this incorrect argument that Gai is directed to Layer 3.

22 Again, Gai clearly states that its device is a Layer 3 and
23 operates up to the network layer, up to. That would include lower
24 Layer 2. Nothing within Gai suggests that it cannot perform MAC
25 address access control list filtering.

1 JUDGE AMUNDSON: All right, thank you.

2 MR. HUH: Sure. And, you know, to be clear, if we go further
3 on Slide 10, Patent Owner's own expert, we can see during
4 deposition, Exhibit 1021, 109:10-13, conceded this point, that Gai's
5 invention may be utilized in Layer 2. This is their own expert
6 conceding this during deposition. So, then the question really is what
7 is the basis for Patent Owner's arguments, which are contrary to Gai's
8 express teaching? You know, and as their own expert conceded, that
9 in fact, it teaches that it may operate at Layer 2. We don't have to
10 guess really what the basis is. If we go to Slide 11, we can see, and
11 this is Dr. Cole, Patent Owner's expert's testimony, where he
12 effectively testifies that he limited his understanding of the prior art to
13 what the prior art claims.

14 During deposition, after being confronted with Gai's teachings
15 on, in fact, that its invention is applicable to Layer 2 access control
16 lists, so the question was, do you believe Gai is lying about that, and
17 he answered no. Then he was further asked, so you're limiting your
18 understanding of Gai to what it claims, is that correct? And his answer
19 was, I mean, to me the claims are the invention. So, the specification,
20 talking about the specification of Gai, could talk about sort of
21 hypotheticals and things like that, but to me, the invention is what is
22 in the claims.

23 So, this is Dr. Cole stating that he did not consider the
24 specification of Gai and its disclosure about how it operates at Layer
25 2, although he recognized that it has that disclosure, but he limited his

1 understanding to what Gai claims. That is an erroneous approach to
2 analyzing the prior art. As we can see on Slide 11, Your Honors, the
3 Federal Circuit In re Riggs has held that a reference constitutes prior
4 art for all that it teaches. It's not what it teaches in the claims, it's for
5 all that it teaches. And there's no dispute that, in fact, Gai teaches that
6 its invention is applicable to Layer 3 access control lists.

7 I would want to note also, just to remove any doubt that, in fact,
8 Gai is contemplating operating at Layer 2, if we turn to Slide 12, Your
9 Honors, Gai provides an example of implementing the intermediate
10 network device with a Cisco Systems Catalyst 6000 multilayer switch.
11 And just to remind the Board, the Gai reference is a Cisco patent, and
12 these are the inventors from Cisco stating that their invention, the
13 intermediate network device, can be implemented with Cisco's 6000
14 multilayer switch. This is a multilayer switch, it's not a single-layer
15 switch.

16 If we turn to Slide 13, both experts, we can see, agree that a
17 multilayer switch operates at multiple layers, including Layer 2. We
18 have Dr. Crovella's testimony on Slide 13, Exhibit 1023 with
19 supporting evidence, testifying that it would include operating at
20 Layer 2, to perform access control list filtering, which means it would
21 perform MAC address filtering at Layer 2. Likewise, Patent Owner's
22 own expert, on the right side of Slide 13, Exhibit 1021, Page 111,
23 Line 18-19, this is his testimony, and I'll read it in the record. So,
24 when you're saying multilayer switches, it means it's operating on
25 Layers 2 and 3.

1 So, we have both experts again confirming that Gai, which is
2 implementing a multilayer switch as its intermediate device, would be
3 operating at Layers 2 and 3. That confirms our position, Your Honor,
4 is that it would have been obvious to combine Gai with Yip, because
5 Yip teaches access control filtering based on MAC addresses, which
6 is Layer 2, and Gai is operable at both Layers 2 and 3.

7 JUDGE AMUNDSON: This is Judge Amundson. I think on
8 your Slide 13 you include a paragraph from Dr. Crovella's second
9 Declaration, Exhibit 1023, that includes Figure 7.5 from Exhibit 1022,
10 which seems to be a 2018 book chapter. What's your response to
11 Patent Owner's argument that the Cisco 6000 multilayer switch
12 probably changed a whole lot between 2018 and 1999, Gai's filing
13 date?

14 MR. HUH: Right, so our position, Your Honor, is setting aside
15 that reference, which is merely supporting the testimony of both
16 experts that multilayer switches operate at multiple layers. That's why
17 they're called multilayer switches. Even if the Board was to say well,
18 that reference comes after the critical date of the patent at issue, and it
19 doesn't constitute prior art, we're just using it as an evidentiary
20 reference, and per the Federal Rules of Evidence, an expert can cite
21 documents that aren't necessarily admissible as prior art. Even if the
22 Board was not to consider that evidentiary reference on its own, we
23 would still have the testimony of both experts on this point, which do
24 not conflict.

1 JUDGE AMUNDSON: All right, I think I understand your
2 position.

3 MR. HUH: Yes. Now I want to make one more note with
4 respect to the combination of Gai and Yip, which is on Slide 14, and
5 that is that Patent Owner's Surreply presents new arguments regarding
6 the Yip reference. In the Surreply, Patent Owner argues that Yip
7 teaches away from using MAC addresses. This is the Surreply at Page
8 7. This argument, the teaching way argument, was nowhere present in
9 the Patent Owner Response, and now we have the Patent Owner's
10 Surreply for the first time raising this argument. In fact, I believe
11 numerous instances of the assertion of teaching away. Those
12 arguments regarding teaching away, Your Honors, were waived, and
13 are not proper arguments responsive to the Petitioner's Reply, and we
14 would ask that the Board not consider them because we did not have
15 an opportunity to submit a responsive brief.

16 But I would also note for the record that this argument that Yip
17 teaches away from using MAC addresses is simply incorrect. For the
18 record, I would identify Yip at Column 6, Lines 24-27. I want to read
19 this in the record so it's clear, and I'll start from Line 25 just for
20 brevity. Here's what the Yip reference states, MAC addresses may be
21 adequate for purposes of obtaining access to the network login
22 controller and user interface on packet forwarding device 200. End
23 quote. So again, this says MAC addresses may be adequate for
24 purposes of obtaining access.

1 We have Yip actually teaching to utilize MAC addresses to
2 obtain access. They don't teach away -- it never teaches away. It
3 actually teaches the opposite in its embodiments. But nonetheless,
4 their argument was waived and it's improper.

5 JUDGE AMUNDSON: This is Judge Amundson. I have you
6 about 20 minutes into your initially requested 25.

7 MR. HUH: Thank you, Your Honor. Let me briefly touch on --

8 JUDGE CASS: This is Judge Cass. Could you do me a favor
9 and just repeat the cite from Yip that you just gave us. You don't have
10 to read it, just give us the cite.

11 MR. HUH: Yes, Yip Column 6, 24-27.

12 JUDGE CASS: Thank you.

13 MR. HUH: You're welcome, Your Honor. Let me just briefly
14 touch on the second key point on Slide 15. We presented sufficient
15 evidence regarding the Gai and Kwan combination, including
16 providing motivation to combine and expectation of success. Patent
17 Owner's arguments regarding Gai and Kwan again are premised on
18 the erroneous assertion that Gai is limited or directed to Layer 3,
19 which I just discussed is incorrect. I'm going to not go into this detail
20 on the second point unless the Board has any specific questions. In
21 light of no questions let's, in the interest of time, go to the third key
22 point, which is the motivation to combine Gai, Kwan and Georgiou,
23 which pertains to Claim 15 on Slide 21.

24 If we now shift focus, Claim 15 is a device claim and the
25 limitation at issue is the memory circuit limitation, which recites a

1 memory circuit that's operable to store packets. The Petition
2 explained how the combined teachings of the three references would
3 render obvious this claim, including this limitation. Turning to Slide
4 22, just note here on Slide 22 that Gai teaches receiving packets at the
5 forwarding circuit, and it further teaches that based on the access
6 control list, certain action is taken on different packets, for example,
7 as shown on Slide 22, Column 4, 29 through 36. Gai teaches that
8 actions taken on incoming packets may include forwarding to the final
9 destination, discarding the packets, or, for example, transferring them
10 to CPU for additional processing.

11 A similar disclosure is at Gai 13, 38 through 45. Additional
12 processing, for example, would include encryption, so if you have
13 specific packets that require encryption, then you would send those to
14 the CPU, but the other ones we forwarded over to the ultimate
15 destination. Now Gai does not describe necessarily how to store the
16 packets as they await encryption or additional processing. In that
17 respect, if we turn to Slide 23, Georgiou teaches that, when you have
18 incoming packets that require subsequent processing, they are going
19 to be stored in memory. It utilizes hardware for that, such as, for
20 example, a DMA circuit or DMA controller, and DMA stands for
21 Direct Memory Access controller.

22 So Georgiou complements Gai's teachings by saying that when
23 you have incoming packets that require processing, store them in this
24 dynamic memory, until the processor can actually have time to
25 process them. We explained in our Petition, shown in Slide 24, citing

1 Dr. Crovella's testimony, that there are multiple reasons to combine
2 the teachings. I won't belabor each specific reason, but suffice it to
3 say the specific reasons were not disputed by Patent Owner. Further,
4 the Petition on Slide 25 citing Dr. Crovella, provided a reasonable
5 expectation of success in implementing the combination. Dr. Crovella
6 provides testimony on that point, as well as citing multiple evidentiary
7 references.

8 For example, Exhibit 1008 states that often a simple DMA
9 circuit that receives packets and writes it to memory is utilized. This is
10 a simple DMA circuit, these are simple circuits. As another example,
11 Exhibit 1009, cited in Dr. Crovella's Declaration, states that a direct
12 memory access controller is often used. So these are simple circuits
13 often used for the purpose of storing incoming packets that need
14 subsequent processing, very simple and often used. Now if we turn to
15 Slide 26, we have Dr. Crovella's testimony responsive to Patent
16 Owner's arguments on the point in Patent Owner's Response, and
17 Patent Owner first argues, Your Honors, that incoming packets --
18 storing the packets based on Georgiou's teachings, well, that would
19 slow down Gai's processing and forwarding of the packets.

20 But that's simply incorrect, because not all the packets would
21 be stored in the memory, as taught by Georgiou. Only a very small
22 subset that needs subsequent processing would be stored. The
23 majority would be forwarded, and only specific packets that need
24 additional processing by the CPU, in fact, would be stored until the
25 CPU was free to process those packets. That argument raised by

1 Patent Owner you'll hear today is incorrect. As another argument,
2 Patent Owner argued that well, these are complex circuits and would
3 be extremely costly and inefficient. Again, this is simply incorrect.
4 DMA circuits were considered simple and often used for the purpose
5 of storing incoming packets. So, both arguments raised by Patent
6 Owner on this point are simply incorrect. Are there any questions on
7 the third point?

8 If not, I'll address the last point for discussion, which is how
9 the prior art teaches the memory circuit of Claim 15. Just for context,
10 if we turn to Slide 28, we have Claim 15 with the relevant limitation
11 highlighted in yellow. I just want to make a couple of observations
12 here. First is that the claim requires that the memory circuit is coupled
13 to the forwarding circuit, so that's the physical connection between
14 the two. Secondly, the claim requires that the memory circuit store
15 three pieces of information. One is it stores packets that need
16 processing, second, the memory circuit in the claim stores an
17 enhanced access control list, and third, the memory circuit stores a
18 dynamic access control list.

19 The enhanced was the initial one, the dynamic is the one that's
20 updated after some point in time. So, we had the memory circuit
21 storing three pieces of information. If we turn to Slide 29, I have a
22 portion of the Petition also identified in the Petitioner's expert
23 testimony, and we can see that the Petition mapped Gai's memory
24 circuit as corresponding to NVRAM 408, which is the red box on the
25 upper right, dynamic memory 409, as well as TCAM memory 410.

1 We explained that the NVRAM is what stores the initial access
2 control list which is enhanced, which is stored by the administrator.
3 The dynamic memory in the proposed combination is what stores the
4 incoming packets that need additional processing by the CPU.

5 Then we also explained that the TCAM stores the dynamic
6 access control list. All of that is not in dispute. I just want to give
7 Your Honors some orientation on the three elements that correspond
8 to the memory circuit. Now Patent Owner, makes an implicit claim
9 construction argument if we look on Slide 30, asserting that in the
10 context of the claim, there must be a single memory circuit -- this is
11 Patent Owner's Response, Page 30 -- arguing that there must be a
12 single memory circuit operable to store packets, enhanced access
13 control lists and dynamic access control list. They make the same
14 argument in the Surreply, arguing that Independent Claims 15 and 19
15 require a single memory circuit.

16 This is simply incorrect. The claim is open-ended, Your
17 Honors, a comprising claim, and it recites a memory circuit. The word
18 single is nowhere present in the claim. We also have the assertion that,
19 the written description supports a single memory circuit raised in the
20 Patent Owner's Surreply is also wrong. If we turn to Slide 31, for
21 reference I provided relevant portions of the 518 patent, which
22 described where things are stored. The 518 patent, Column 9, 28
23 through 36, and we can see a number of things here. First, the 518
24 patent teaches that selected packets are stored in packet memory 306.
25 If we look to the right on Slide 31, you have Figure 3. You can see

1 that the packet memory is the red box on the left of the ethernet
2 switch.

3 But additionally, the 518 specification teaches that in the
4 memory in the processor 302 is the Enhanced Control List, and that's
5 going to be the processor on the right. These are two separate
6 components that store the claim information, so you have at least one
7 embodiment in the 518 patent where the Enhanced Access Control
8 List is not stored in the Packet Memory 308. It's in fact stored in the
9 processor, but that addresses the first and the second items that are
10 stored. With respect to the third item, Dynamic Access Control List,
11 the 518 patent is completely silent as to where that access control list
12 is stored. It could be stored, perhaps, in the forwarding engine,
13 because that's going to implement where things are forwarded right
14 away.

15 So, what we have is, a partial disclosure in the 518 patent about
16 where things are stored, but at least that partial disclosure is
17 inconsistent with Patent Owner's assertion and their implicit
18 construction. The third item in the claim is nowhere described where
19 it's being stored. To confirm, if we go to Slide 32, we have the
20 testimony of both experts on this point. Dr. Crovella reviewed the 518
21 patent and the arguments raised by Patent Owner, and his testimony
22 was that there is no such embodiment in the 518 patent. That is, there
23 is no embodiment with a single memory circuit that stores all three
24 pieces of information.

1 Then on the right of Slide 32, we have Dr. Cole's testimony,
2 where he testifies, and he was asked -- questioned, but you cannot
3 identify a single embodiment where it discloses a single memory
4 circuit that stores received packets, an Enhanced Access Control List
5 and a Dynamic Access Control List, correct? His answer was, so no, I
6 cannot find a specific reference in the specification that has the exact
7 claim. He further testified, and I'll quote it in the record, so no, the
8 specification does not have the specifics of the claims. Here we have
9 both experts agreeing that the 518 specification does not have an
10 embodiment with a single memory circuit that stores all three pieces
11 of information.

12 Patent Owner's argument with the implicit claim construction
13 that it requires a single memory circuit is unsupported, and in fact, is
14 contrary to an embodiment of the 518 patent, where the Enhanced
15 Access Control List is stored in the processor. It's also contrary to
16 Federal Circuit precedent shown on Slide 30, Celgene Corp. v. Peter.
17 Are there any questions on the memory circuit limitation? If there are
18 no questions, then I'll stop here in the interest of time.

19 JUDGE AMUNDSON: All right, I have you about 34 minutes
20 into the 45 minutes, so I guess that would mean your rebuttal is
21 around 11 minutes. Okay, all right. Let's go to Mr. Auchter. Let me
22 ask if you would like to reserve any time for surrebuttal.

23 MR. AUCHTER: We would like to reserve 10 minutes, Your
24 Honor.

1 JUDGE AMUNDSON: All right, very well. You may begin
2 your argument whenever you are ready.

3 MR. AUCHTER: Thank you, Your Honor. Does the Board
4 have a copy of the slides in front of them, or would you prefer that I
5 try to share the screen on them.

6 JUDGE AMUNDSON: This is Judge Amundson, I believe all
7 of the panel members have the demonstratives -- both sides'
8 demonstratives. If you tried to share, we might only get one small
9 panel showing the slides. I'm not sure how this works, but if you want
10 to try, go ahead. It's up to you.

11 MR. AUCHTER: No, Your Honor, my preference would be to
12 keep it simple, if possible.

13 JUDGE REIMERS: Yeah, I would suggest just doing like the
14 other counsel has done and just give us the page numbers and we can
15 follow along.

16 MR. AUCHTER: So turning to Slide 2, Your Honor, which is
17 Slide 2 of Exhibit 2003, there are three independent claims, the first
18 independent claim being Claim 1, that are at issue here. With respect
19 to Claim 1, the issues are whether or not a POSITA would have been
20 motivated to combine the references in such a way as to achieve the
21 limitations, specifically with respect to the dynamic access control
22 list, or ACL, as shown highlighted on Slide 2.

23 The other two independent claims that are at issue are Claims
24 15, and as Mr. Huh referenced, the limitation that Patent Owner is
25 focusing on there is the memory circuit limitation or a memory circuit,

1 and specifically that the claimed memory circuit is coupled in very
2 particular ways and operable to store three things: packets, enhanced
3 access control lists and a dynamic access control list.

4 Those limitations appeared in the claims from the day they were
5 originally filed in this Application. Also, the specific coupling, that it
6 be coupled to the forwarding circuit, that the processor is coupled to
7 the memory circuit, and that the forwarding circuit is also coupled to
8 the memory circuit, so you had the three there. Moving on to Slide 3,
9 or 4, I'm sorry -- they're cutting off just a little on my screen here --
10 the same limitations in essence appear in Claim 19, the two apparatus
11 claims recite the memory circuit limitation.

12 Turning to the next slide, Slide 5, Patent Owner makes two
13 arguments, in essence, with respect to the two grounds that were
14 asserted in this IPR. The first is that it would not have been obvious to
15 a POSITA to combine the Gai, Yip, Kwan and Georgiou disparate
16 memories into the memory circuit that was recited in the Claims 15,
17 17 and the dependent claims, 19-21. We'll explain why that is our
18 position and the reasoning behind that in a second. The next
19 argument, which is going back to ground 1, is that a POSITA would
20 not have been motivated to combine the Gai, Yip and Kwan prior art
21 references to achieve the dynamic control list limitations. Those
22 actually appear in Claims 1, 15 and 19, but we can focus on them as
23 they appear in Claim 1 with respect to the arguments, as Petitioner's
24 arguments on these points specifically reference back Claim 1.

1 The argument here is that a POSITA considering a Layer 3
2 device would've been looking at Layer 3 devices and technology,
3 which are on the network layer and are concerned about
4 interconnecting LANs or connecting to the internet or otherwise a
5 more large-scale interconnection. Whereas a POSITA working on
6 ethernet switches or something of that nature would be looking at
7 Layer 2 technology, which is specifically related to MAC addresses
8 and the kinds of ways in which physical devices would be connected,
9 typically over a LAN or a smaller network device. That's the essential
10 difference between Layer 2 and Layer 3.

11 JUDGE AMUNDSON: This is Judge Amundson, and so just let
12 me follow up on that, if I may. In Lionra's view, what distinguishes a
13 Layer 2 device from a Layer 3 device?

14 MR. AUCHTER: The essential difference, Your Honor, would
15 be that the Layer 3 devices which are concerned with IP addresses and
16 internet communications were using a different form of
17 communications entirely in terms of larger port compatibility and
18 capacity. When you're connecting an enterprise or anything to the
19 internet, you're concerned with a much greater number of ports and
20 possible connections and things of that nature, whereas if you're on a
21 Layer 2 device, you're basically limited to the number of devices
22 you're going to have on a typical ethernet network, so the scale is
23 quite different.

24 Also, the variability is quite different in the sense that on Layer
25 2 devices you're dealing with MAC addresses and fixed addresses,

1 whereas in Layer 3 devices you're frequently dealing with variable
2 information because IP addresses can be fixed and static, and they can
3 also be variable because of DHCP, and the issues with having a
4 limited number of potential IP addresses going through a router or a
5 connection to an ethernet LAN, and then basically you run out of the
6 last couple of digits that you need. These are different issues that a
7 POSITA would be confronting, and that's why a Layer 2 device and a
8 Layer 3 device would not, at least at the time of the invention in 2004,
9 would not have been something that a POSITA would have looked at
10 to combine the two types of devices.

11 JUDGE AMUNDSON: This is Judge Amundson again. Just to
12 sort of follow up on that, it seems to -- and correct me if I'm wrong --
13 if I'm a Layer 3 device, don't I also have to operate at Layer 2
14 because I need to send a packet to the next Layer 2 device on its way
15 to the terminal IP address?

16 MR. AUCHTER: In general, Your Honor, obviously a Layer 3
17 device -- a router, if you will, -- which is your typical Layer 3 device,
18 will have to have some Layer 2 capability because it has to be
19 connected to the ethernet and to the LAN, which is going to be
20 sending information to it. Whether or not it would include access
21 control lists internally, and whether or not it would require the kind of
22 switching logic for sending information in between all the other
23 devices on an ethernet LAN is the issue there. So yes, it would have to
24 have a Layer 2 connection capability, but it would not necessarily
25 have to have the capabilities that you have for Layer 2 switching. That

1 particularly comes into play if you've got virtual LANs and VLANs,
2 but that's not an argument that we raised in the papers.

3 JUDGE AMUNDSON: All right, thank you. I think I
4 understand your position.

5 MR. AUCHTER: Thank you, Your Honor.

6 JUDGE CASS: This is Judge Cass, let me follow up. So,
7 Petitioner, as we saw, points to portions of Gai in Column 5 -- this is
8 their Slide 9 -- where they say that it should be understood that Layer
9 2 intermediate devices, or that the present invention may be used with
10 Layer 2 intermediate devices. Gai also mentions the Cisco Catalyst
11 6000 switch, which it seems that the experts agree can operate on
12 Layers 2 and 3. So what's your response to that?

13 MR. AUCHTER: Sure, Your Honor, if you'll just give me a
14 second to --

15 JUDGE CASS: Sure.

16 MR. AUCHTER: -- address my notes here. The first is, of
17 course, that Gai's invention -- and it might be pronounced gay
18 because it's Italian, but my Italian is not good enough to know, so Gai
19 works -- is that his invention is not the Cisco Catalyst 6000, nor is it
20 the 8000. It is specifically rather optimizing access control lists into
21 binary decision diagrams, BDDs, in various ways so as to be able to
22 optimize an access control list. The Cisco 6000 he's referenced, as we
23 said, it's a product, it's not a patent or a printed publication. It doesn't
24 show any use of ACLs that are both Layer 2 and Layer 3 in the Gai
25 disclosure that don't combine MAC and IP addresses.

1 Gai's disclosure is actually, with the exception of a few
2 references which I'll have on one of the slides, is directed entirely to a
3 Layer 3 device, with some issues with possibly a Layer 4 device in the
4 transport layer where it talks about port numbers, as well, but it
5 doesn't ever reference a MAC address or really refer to it. It does
6 include a paragraph that one might characterize as a gratuitous
7 statement that it could also be used in Layer 2 devices. I would argue
8 that Gai's invention, which is the use of combining ACLs into a
9 binary decision diagram may well be agnostic as to what kind of
10 device it was used in, insofar as it's talking about using an ACL, but
11 his specification is entirely devoted to a Layer 3 device very
12 specifically. There is an argument to be made that it's not directed to
13 Layer 2 devices because it talks about TCAMs and not CAMs, but
14 that again, is an argument that was not sufficiently developed in the
15 papers.

16 JUDGE CASS: So, it's your position that when Gai says that it
17 should be understood that the present invention may be utilized with
18 Layer 2 intermediate devices, it doesn't mean all of the invention, it
19 just means certain aspects of the invention, and that those aspects do
20 not include the MAC address --

21 MR. AUCHTER: Yes, yes, yes, Your Honor, exactly that.
22 When it says the present invention, it would be referring to what was
23 in the claims, and what was in the claims of Gai's patent was
24 optimizing ACLs, access control lists, into a binary decision diagram
25 and some other variations of that, sum of products algorithm

1 application and things like that. But Gai's focus, and it's plain from
2 the specification and the detailed description in the specification, is
3 implementing combined ACLs in a way that you could basically
4 speed up processing by not having to execute multiple if-then
5 statements, but just quickly go down a binary decision diagram, which
6 would be contained in a TCAM or form of content addressable
7 memory, which per Gai you could just go through once and very
8 quickly decide whether or not you permitted access. Gai also
9 discusses possibly quality of service and other features that could be
10 implemented using Gai, not just security.

11 JUDGE CASS: Thank you. As I'm looking at this --
12 (Simultaneous speaking.)

13 JUDGE CASS: Sorry, didn't mean to interrupt.

14 MR. AUCHTER: No, I'm sorry, Your Honor, please go ahead.

15 JUDGE CASS: As I'm looking at this statement from Gai, it
16 does say that it should be understood that the present invention may
17 also be utilized in whole or in part with Layer 2 intermediate devices.
18 So, it does seem like it's saying that the invention could be used in
19 whole with Layer 2 intermediate devices. Are you suggesting that
20 that's inconsistent with other parts of the specification and we should
21 disregard it?

22 MR. AUCHTER: No, Your Honor, I am suggesting that the
23 invention in whole or in part would refer to the inventions as claimed,
24 and then as the various claims, some of the claims require merging
25 multiple ACLs, some of the claims require just creating a binary

1 decision diagram, some of them say you can use the sum of products
2 system, and some of them have other variations on what is the actual
3 invention of Gai. So you wouldn't have to do sum of products, for
4 example, or you might not have to combine ACLs. You just put them
5 into a binary decision diagram, and using the CAM, go through that.
6 That would not be using the whole, that would be using a part of the
7 invention. The whole invention would be the dependent claims and
8 what further limitations they had to fully optimize it to achieve --
9 assist in achieving the high processing speeds that Gai talks about.

10 JUDGE CASS: All right, thank you. I think I understand your
11 position.

12 JUDGE AMUNDSON: This is Judge Amundson. I would just
13 maybe explore this point a little more, and if you could look at Figure
14 2 in the '518 patent?

15 MR. AUCHTER: Give me one second, please, Your Honor.

16 JUDGE AMUNDSON: Sure.

17 MR. AUCHTER: All right, Your Honor. I have Figure 2 in
18 front of me.

19 JUDGE AMUNDSON: All right, so it looks to me, in that
20 preferred embodiment in Figure 2, that the dynamic access control list
21 is based on IP addresses. So my question is, would you characterize
22 that preferred embodiment as a Layer 3 device or not?

23 MR. AUCHTER: I would -- Your Honor, I would characterize
24 the preferred embodiments of the '518 patent as actually being
25 somewhat revolutionary in the sense that they combined the Layer 2

1 and the Layer 3 devices. And that was sort of the invention, if you
2 will, of the '518 patent and what was key about it, because it was
3 talking about using the -- well, not just MAC addresses, also
4 usernames and DNS names, working through a mapping database,
5 performing the conversion processes that are shown in Figure 2 here,
6 and then coming up with linked IP addresses. Linked in the sense of
7 associated with one of the usernames, DNS names, Windows domain
8 names and/or physical addresses, which are MAC addresses in this
9 case, to have the dynamic access control list.

10 JUDGE AMUNDSON: All right, I think I understand. Well,
11 but on that point, if that's the way we should view the '518 patent,
12 why wouldn't we view Kwan in the same way where it's obtaining
13 information at Layer 2, the MAC addresses, and obtaining
14 information at Layer 3, the IP addresses, and storing IP address/MAC
15 address pairs?

16 MR. AUCHTER: Because, Your Honor, Kwan is directed more
17 towards security concerns and specifically has issues in its
18 specification that we believe would clearly limit it to a person of
19 ordinary skill in the art. Those would include the fact that Kwan is
20 saying okay, I'm going to limit the number of IP addresses associated
21 with each port. So that would be something that you might do if you
22 were on a Layer 2 device, because you have a switch that you're
23 connecting to multiple devices within a local area network, and that's
24 why you can limit the number of IP addresses. If you were doing that
25 in a Layer 3 device, the kind that was linking to the internet and was

1 connecting the local area network or the hosts that are on that local
2 area network to a limited number of IP addresses, essentially saying
3 okay, I'm going to let you go to CNN and Fox News, but Bloomberg
4 is out because I'm limiting the number of IP addresses.

5 So that would be something that a Layer 2 device would be
6 doing. It would be limiting the number of IP addresses associated with
7 each port, but it's not something that a Layer 3 device could
8 realistically do, given the number of possible connections. And even if
9 you weren't talking about the internet, but just multiple VLANs, for
10 example, in a network, you'd still have the same issues as to why you
11 wouldn't be limiting the number of ports. And then there's the other
12 issue of Kwan's specific teaching about how you learn the IP
13 addresses and the delay process. Again, that would be blocking a port
14 for an indeterminate period of time.

15 In fact, you -- so you have to both learn those and then he
16 deletes the number of learned -- Kwan teaches deleting some of the
17 learned addresses, so you even have less of the learned IP addresses,
18 which means you're going to spend more time learning new IP
19 addresses. The combination is why we think that Kwan is more of a
20 Layer 2 device, looking at the reference for all it teaches.

21 JUDGE AMUNDSON: All right, thank you. I think I
22 understand your position.

23 JUDGE REIMERS: Yeah, Counsel, I just want to clarify here --
24 so, you know, looking at your Slide 5 in your slide deck, so you're
25 saying Kwan is directed to a Layer 2, whereas both Gai and Yip are

1 directed to Layer 3s, and because of the limited connectivity of Kwan
2 and because of it being a Layer 2, a skilled artisan would not look to
3 Kwan to combine it with Gai and Yip? Is that your position?

4 MR. AUCHTER: Yes, Your Honor. Our position is that Layer
5 2 and Layer 3 were different animals, if you will, and a person of
6 ordinary skill in the art would have been looking within the same
7 layer and the same types of devices that they were considering for
8 purposes of connection, and that one of the breakthroughs, if you will,
9 of the '518 patent is saying, you know, we can take these two types of
10 information and put them in a Layer 3 device and provide this
11 dynamic access control list that is more effective than an enhanced
12 access control list to provide better security and more robust
13 connections and access control lists in the environment. That now, in
14 this year, 2025, certainly looking at Layer 3, Layer 2, combining them
15 is something that a person of ordinary skill in the art would
16 understand, but that is, in part, the developments and advances in the
17 field since Mr. Faulk's invention in 2004.

18 JUDGE REIMERS: Thank you. I understand your position,
19 thank you.

20 MR. AUCHTER: Okay. Going to Slide number 7, we can
21 discuss the '518 patent's disclosure. When one looks at the '518
22 patent, it does clearly disclose the packet memory, which we assert
23 corresponds to the memory circuit in Independent Claims 15 and 19.
24 And that packet memory, looking at Slide 8, has to store selected
25 packets and enhanced access control lists, and a dynamic access

1 control list. Storage of the dynamic access control list is admittedly
2 not within the detailed description of the specification, but it was
3 claimed in the original claims, as filed within the '518 patent, and is
4 therefore appropriately part of the written description consideration in
5 terms of whether or not there is a written description.

6 The patent does say that you could store some packets within
7 the processor. A person of ordinary skill in the art would say that
8 there's an alternative embodiment, perhaps, or it could be a cache
9 memory. But the patent also specifically does disclose that the
10 packets, the enhanced access control list, and the dynamic access
11 control list would be stored in the memory circuit, and that was
12 consistent with the operation that is explained within the '518 patent,
13 as well. And that would also be consistent with the various coupled-to
14 limitations of having the forwarding circuit coupled to the packet
15 memory, as well as having the processor coupled to the packet
16 memory so that you could put the dynamic access control list,
17 enhanced access control list, which would need to be accessed by the
18 switch forwarding engine, into the packet memory.

19 I apologize, there's a duplicate, Slide 9. The Federal Circuit has
20 noted that when you have an issue of claim construction related to
21 whether or not "a" or "an" should mean one or more or multiple or
22 just one, a single device. The prosecution history is also relevant to
23 that consideration. As shown in Slide 10 and quoted, the single
24 memory circuit, arguably through these quotes -- the distinction is
25 over the Droms prior art reference -- show that the Patent Owner was

1 relying on a memory circuit that was operable to store the list during
2 the prosecution, and that the packets had to be stored in the memory
3 circuit. And that was also emphasized during the prosecution as a
4 distinction over the Droms reference.

5 The second distinction is based on a further -- and slightly a
6 typo, but these are accurate quotes -- argument made that again, it
7 doesn't disclose a memory circuit that has both an enhanced access
8 control list and a dynamic access control list. Although this argument
9 doesn't reference the patent, it's within the same Office action
10 responses that were cited by the Applicant, or provided by the
11 Applicant during the prosecution. So it's Lionra's contention that the
12 specification and the prosecution history show a single memory
13 circuit that would've met the limitations with respect to being coupled
14 and with respect to being able to store both packets and the two types
15 of access control lists.

16 In turning to Slide 11, talking about the coupled limitations
17 specifically, the memory circuit is coupled to the forwarding circuit
18 and is operable to store the various packets, but it also has to be
19 coupled to the processor. That's what's shown in Figure 3 of the '518
20 patent. In that case, it appears that the forwarding circuit is coupled
21 through the direct memory access controller to the memory circuit,
22 but a DMA controller is a device that is used to couple one device to
23 another for the purpose of conveying memory packets or other data
24 that are then stored somewhere else. Essentially, it's a memory
25 interface.

1 Turning to Slide 12, basically summarizing the Federal Circuit
2 law on the construction of “a” or “an,” and why, in this particular
3 case, the singular meaning applies, with the appropriate case law. Just
4 to be clear, the Federal Circuit has also noted that, just because the
5 term “comprising” was used as the transition within the patent, that
6 does not mean that “a,” the singular, the one and only meaning of “a”
7 would be subsumed by the open transition phrase. It is appropriate to
8 construe it as such, even if you are using a comprising or other open-
9 ended transition phrase instead of just consisting of, or even
10 consisting essentially of, but those weren’t used here.

11 JUDGE CASS: Counsel, this is Judge Cass.

12 MR. AUCHTER: Yes.

13 JUDGE CASS: Looking at Claim 15, and I’m specifically
14 looking at your Slide 3, although we can look at some other slides,
15 too. Isn’t the better -- I don’t know if better is right -- but the better
16 way to look at this would be to say when the limitation says a memory
17 circuit, “a” could be one or more, so you could have multiple memory
18 circuits in the claim, but then in the subsequent limitations where it
19 uses the word “the,” the memory circuit, that that’s referring back to
20 one of the memory circuits and therefore, those have to all be within
21 the same single-memory circuit, although the claim could also
22 encompass other memory circuits, as well. Is that different than the
23 way you’re reading the claim, and if so, you know, why would that
24 not be correct of you to claim that?

1 MR. AUCHTER: No, Your Honor, it's not different. I believe
2 the antecedent basis here does strongly support that it's a single
3 memory circuit because the claim language does not use "a" and then
4 a second. It does use "the" and properly refer back to the "a" -- to the
5 "a," I'm sorry -- to "a" memory circuit for the antecedent basis in each
6 of the subsequent limitations.

7 JUDGE CASS: Maybe this is a distinction without a difference,
8 because whether there might be -- whether "a" might encompass other
9 memory circuits may not matter if the use of the word "the" provides
10 antecedent basis all back to a single one of those. But yeah, that's kind
11 of what I was getting at. I don't know if there's a question in there,
12 but I open it to comment if you want to comment. If not, that's fine,
13 too.

14 MR. AUCHTER: Your Honor, it's our opinion that that is the
15 better interpretation of the claim language, but it's also our
16 understanding that if one starts with the context that "a" memory
17 circuit just means memory -- in other words, that you didn't have "a"
18 in there at all -- then referring back to "the" memory could encompass
19 multiple memory circuits, in theory, one would assume. But that's not
20 what was used here, it was "a" memory circuit. And then also, it
21 wasn't a first memory circuit, it was "a" memory circuit, probably
22 because there was no second memory circuit so there would be no
23 reason to single it out as a first memory circuit.

24 JUDGE CASS: Thank you, Counsel.

1 JUDGE AMUNDSON: This is Judge Amundson. I have you
2 about 30 minutes into your initially requested 35 minutes, but let me
3 follow up on the memory circuit limitation. It seems to me maybe
4 there is another way to look at this, in that a memory circuit isn't
5 limited to a single component. Cisco points to a memory circuit
6 comprising three components, component whatever, 409, 408, and the
7 TCAM. What's your view on that?

8 MR. AUCHTER: Well, our view would be that they're wrong,
9 Your Honor, but that doesn't answer your question. If you look at
10 Slide 14, you'll see that we've identified the various, some of the
11 memory circuit -- well, all four of the memory circuits they have
12 there. First off, what they've done here is they've identified the
13 various memory circuits, and if I understand, Counsel's discussion of
14 the proposed combination of Georgiou and Gai, they are not
15 proposing adding a fifth memory circuit, they are proposing adding a
16 DMA device somewhere within that box. But either way, these are
17 multiple memory circuits, each one, some of which are not operable to
18 store packets.

19 A TCAM is a Ternary Content Addressable Memory, which is
20 a form of content addressable memory, which has a don't care
21 situation. Essentially, it's a set of rows where you can use an and
22 operation or a compare operation to identify quickly what's located
23 there, hence the ability to use it for access control lists, why it's
24 considered desirable for that role, but it is not something that you
25 would store packets in because of that. Packets, first of all, they're

1 variable length, and secondly you tend to be wanting to store them in
2 a range of addresses, and you don't have the ability to point to a
3 specific address in a content addressable memory. Moreover, of
4 course, the non-volatile RAM is completely unsuitable for storing
5 packets, as well.

6 It probably would be unsuitable, frankly, for storing a Dynamic
7 Access Control List since it's non-volatile. It would be very difficult
8 to be dynamic if you don't have the ability to rewrite it -- at least not
9 quickly -- in the same way that dynamic memory, or the memory --
10 what's that number, I apologize, I don't have my right glasses with me
11 here -- associated memory 410, I believe is what that is. It could be --
12 no, that's the CAM is 410. I think it's just a basic memory device 411,
13 so that could be dynamic RAM memory, it could be something else, is
14 what they say in the Gai disclosure. Our point there is that the
15 memory circuits that Cisco is pointing to are neither connected or
16 coupled to the various other elements as required by the claim, nor are
17 they operable to store the information in the sense that, for example,
18 as you look at Slide 15, you see that Gai's processor is coupled to the
19 non-volatile RAM and the dynamic memory below that, and that
20 Gai's forwarding entity is coupled to the TCAM, and the memory
21 411, but that Gai's NVRAM would not be operable to store packets,
22 and Gai's TCAM is not operable to store packets, and that Gai's CPU
23 or processor and forwarding entity are coupled to different memory
24 circuits, so therefore not meeting the limitations of the claim.

1 JUDGE AMUNDSON: This is Judge Amundson. On this
2 coupling point, I thought you said earlier when we were looking at
3 Figure 3 of the 518 patent that indirect coupling suffices. Do I have
4 that wrong?

5 MR. AUCHTER: Slightly, Your Honor. I was saying that a
6 Direct Memory Access device, a DMA device, is like any memory
7 interface. Memory controller provides a way -- it doesn't store
8 information, it moves the information from one location to another for
9 storage. That's the function that the DMA performs both in the 518
10 patent or in other locations. There is no DMA, there is no indirect
11 coupling of these various memories here. They're going through an
12 ACL converter, which is a device that creates the binary decision
13 diagrams, or performs the sum of products, or performs the conflict
14 resolution, or what have you. But that's not a device that is used to
15 couple data from one location to another location in the way that a
16 DMA would.

17 JUDGE AMUNDSON: All right, I think I understand your
18 position. Thank you.

19 MR. AUCHTER: It's essentially, Your Honor, that the DMA is
20 a memory interface, and that a memory interface would be how
21 memory is coupled to a specific device. It's a particular memory
22 interface.

23 JUDGE AMUNDSON: So, if the memory circuit is only
24 coupled to the CPU and the CPU is coupled to the forwarding entity,
25 that wouldn't count for purposes of the --

1 MR. AUCHTER: No, Your Honor, because that would provide
2 for a separate connection. It wouldn't be a memory interface. It would
3 actually be an intervening device of some kind, much like the ACL
4 converter here is an intervening device between the NVRAM and
5 what have you isn't directly coupled.

6 JUDGE AMUNDSON: All right, I got it. Thank you.

7 MR. AUCHTER: And by the same logic, Your Honor, of
8 course the CPU is not coupled to the TCAM, directly, either, or the
9 411 memory. Slide 16 essentially repeats those arguments with
10 respect to focusing on the coupling.

11 Now if I could move to Slide 19, I believe I've addressed most
12 of these issues in responding to the Board's questions on that. I hope
13 I've addressed and responded to your questions on those issues, so I
14 will -- I'm looking at, I have 40 minutes, so unless there are any
15 further questions, I would like to reserve the remainder of my time for
16 rebuttal.

17 JUDGE REIMERS: I just have one remaining question. I'm
18 just looking, for example, at your Claim 15 on Page 3 of your --

19 MR. AUCHTER: Yes, Your Honor.

20 JUDGE REIMERS: -- the limitation is a memory circuit
21 coupled to the forwarding circuit, so based on what you previously
22 said, are you asking us to interpret it even though it's not claimed as
23 such as a direct coupling, as opposed to just being coupled? Because
24 it's not claimed as being directly coupled, it's just saying that it's
25 coupled, and under a POSA or POSITA's interpretation, that would

1 typically be something that could also be indirectly coupled. It didn't
2 necessarily have to be directly coupled because it's not claimed like
3 that.

4 MR. AUCHTER: Yes, Your Honor, I understand that position.
5 Our position on that is that in the context of this circuit, it requires
6 direct coupling, or coupling through a DMA memory interface of
7 some kind, as opposed to some of the cases I've read on coupling
8 versus direct coupling. They were more on the nature of a much
9 broader circuit or coupling in between communications and telecom
10 devices and things of that nature where the question becomes, when I
11 say coupled, do I mean I have to have a wired interface? What about
12 if I have a fiber optic or an electromagnetic interface or I'm coupled
13 that way? The question then becomes how loosely coupled does it
14 have to be, and how uncoupled are things? One could argue that any
15 circuit everything is tied to ground, so everything in a circuit is
16 coupled. That's, I think, the absurd position, if you will.

17 There is a line to be drawn, and our position is that within this
18 patent and these claims, coupled refers to more or less directly
19 coupled except for there could be a memory interface, which we
20 normally use to communicate data from a processor or whatever, to
21 the memory where it's stored. But it doesn't do anything for it, it just
22 takes it, moves it over there and stores it, it sits in the storage.

23 JUDGE REIMERS: Okay, thank you. I understand your
24 position.

1 MR. AUCHTER: Thank you, Your Honor. So, I think if I'm
2 going to reserve time for rebuttal, Your Honor, I should stop now.

3 JUDGE AMUNDSON: All right, okay, so I have you about 40
4 minutes into the argument time. Let's go back to Mr. Huh, you may
5 begin whenever you're ready.

6 MR. HUH: Very good, Your Honors. This is Gregory Huh on
7 behalf of Petitioner. Just a few points here, and I'll kind of work
8 backwards from the arguments just because they're fresh in
9 everybody's mind. With respect to the coupling, let's just briefly look
10 at our Slide 29. First, I want to note that just like the patent at issue,
11 we have a CPU going between the forwarding entity, and the dynamic
12 memory, for example. Our position was, for example, that the packets
13 would be stored in dynamic memory, which is 409. The CPU in that
14 implementation facilitates as the interface, just like Counsel for Patent
15 Owner argued. That would be the one transferring the packets from
16 the forwarding entity to the storage, to be stored until the CPU is free
17 to actually process.

18 With respect to any indirect or direct coupling, to the extent the
19 CPU or processor is permitted, as Patent Owner argued, well, that
20 prior art shows exactly that, a CPU, right? But I would also note,
21 going to the single memory argument from Patent Owner, our position
22 is that multiple memory elements correspond to the memory circuit,
23 NVRAM, dynamic memory and TCAM. Those collectively are a
24 memory circuit. They form a circuit, and they are a memory circuit,
25 corresponding multiple elements. It is a circuit, and, I would note that

1 the argument by Patent Owner -- that somehow the prosecution
2 history distinguished a single memory circuit is actually incorrect. The
3 word single memory was never argued by the Patentee in the
4 prosecution history.

5 That argument wasn't made, and in fact, the argument, in the
6 prosecution history, for example, at Page 102, wasn't about memory,
7 but it was really about whether or not the prior art taught the dynamic
8 and enhanced access control lists, a whole different, separate issue.
9 The word single was never disputed by Patentee during prosecution.
10 They argued about a memory circuit, but never argued that that
11 required a showing of a single memory circuit. That's another point
12 that Patent Owner's counsel is really incorrect with respect to the
13 prosecution history.

14 JUDGE CASS: Counsel, this is Judge Cass. I'm going to try to
15 drill down on this a little bit more. Is your position that when Claim
16 15 says, a memory circuit that that can include multiple memory
17 circuits and Gai teaches multiple memory circuits? Or is your position
18 that when it says a memory circuit, even if it means just one memory
19 circuit, Gai teaches that because a combination of the dynamic
20 memory, the TCAM and --

21 MR. HUH: And the NVRAM.

22 JUDGE CASS: So, a combination of those is a single memory
23 circuit, and therefore Gai would teach a single memory circuit?

24 MR. HUH: Great, a great question. Our answer is both. Our
25 position is that the claim has no requirement of a single memory

1 circuit, quote unquote single. That was never argued by the Patentee
2 during prosecution. The patent itself has no such embodiment, and the
3 claim has no such requirement. It does not use the word single, so the
4 claims, in the specification do not support Patent Owner's assertion
5 that it requires a single memory circuit. But I would also note, shown
6 on Slide 29, that the NVRAM is connected to the dynamic memory,
7 also to the TCAM, right? So, you have connectivities between those
8 three elements, and those three different types of memory correspond
9 to a circuit.

10 Just to be clear, for example, the administrator stores the
11 enhanced access control list in NVRAM, right? Ultimately, that
12 enhanced access control list is processed and optimized and stored in
13 TCAM, that forms a circuit. That is a circuit. Now you have also, in
14 the combination with the Georgiou reference, that the incoming
15 packets are stored in dynamic memory 409, and those are all
16 connected together -- those form a circuit, right? NVRAM, dynamic
17 memory and TCAM are all connected together electrically, as an
18 electrical circuit. To the extent even that was required to have a single
19 memory circuit, we have a single memory circuit corresponding to
20 multiple different types of NVRAM, dynamic memory and TCAM.

21 That still forms a circuit. That is a memory circuit, if that was
22 required, but we don't believe that's required. But if it is, we would
23 win regardless because we have a memory circuit as illustrated on our
24 Slide 29. With respect to the coupling limitation, the CPU is exactly

1 like the patent itself where they have the processor between the
2 forwarding entity and the memory.

3 JUDGE CASS: So Counsel, what I'm struggling with a little
4 bit, and I can understand what you just said, is when you look at
5 Claim 15 -- and maybe this can be most easily seen on Patent Owner's
6 Slide 3 -- it has a memory circuit coupled with a forwarding circuit,
7 then the memory circuit operable to store packets, the memory circuit
8 operable to store an enhanced access control list, et cetera. When it
9 uses the word -- the -- that seems to be providing an antecedent basis
10 referring back to a memory circuit. That makes sense to me if we're
11 talking about one memory circuit, but if we're talking about multiple
12 memory circuits, I'm having a little trouble understanding how to
13 interpret the -- the -- term. What could be the antecedent basis of the if
14 you had multiple memory circuits? What would be the basis for that
15 interpretation?

16 MR. HUH: Right, so we identified different components
17 collectively corresponding to a memory circuit. We identified three
18 memories that are formed as a circuit that correspond to the memory
19 circuit in the claim. That was on our Slide 21. The word "the"
20 provides antecedent basis in the context of the claim to the previously
21 recited a memory circuit. The claim never requires that there be a
22 single component as part of the memory circuit, right? And the patent
23 itself, in fact, contemplates, as we identified in our Slide 31, that -- go
24 to Slide 31 -- the enhanced access control list is stored in the
25 processor and the packets are stored in 306, which is the packet

1 memory, right? Where exactly is the dynamic access control list? We
2 don't know because it never describes that.

3 What we do know is that the patent itself contemplates that
4 different components correspond to a circuit, and where those
5 elements would be stored in a claim, the packets would be stored in
6 packet memory 306. The enhanced access control list would be stored
7 in processor 302. This is the patent itself describing this. It's
8 describing that the memory circuit has multiple components, just like
9 we have identified in the prior art. When the patent recites a memory
10 circuit -- if we go to Slide 31 -- it is talking about the circuit of packet
11 memory 306 and the memory in processor 302, multiple components
12 corresponding to a circuit. Likely, the dynamic access control list is
13 probably stored in the forward switching engine, because that's where
14 you have to have the actual access list that you apply to incoming
15 packets, whether you forward, likely, the dynamic access control list
16 is actually stored in the forwarding engine here.

17 JUDGE AMUNDSON: This is Judge Amundson. On that last
18 point, is there any expert testimony supporting what you just said
19 about where the dynamic access control list is likely stored?

20 MR. HUH: All that I would say is that both experts agreed that
21 the specification does not support a single memory circuit on Slide 32.
22 What we do know is that this description in the 518 patent nowhere
23 supports having a single element, that the circuit has a single element,
24 a single memory alone. With respect to the dynamic access control list
25 being stored, in order to process packets quickly, it would be in

1 TCAM. It would be in CAM or TCAM is where you end up storing it
2 in order to apply it quickly. Give me one minute. Let me just --

3 JUDGE AMUNDSON: I'm not saying you're wrong. I think
4 what you're saying makes sense, but I'm just wondering if there's
5 evidentiary support in our record.

6 MR. HUH: Right. I think neither expert wanted to go beyond
7 the four corners of the 518 patent and state that the dynamic access
8 control list is in CAM. But normally that's the way it's implemented
9 because you want to have fast switching, and that's because you have
10 it in CAM. CAM would not be in the processor or in the dynamic
11 memory portal. I don't want to speculate on that, but I will say that we
12 know for sure that the patent itself, in this context, has a circuit that
13 has multiple components. Packet memory is dynamic. The processor
14 has its own internal memory. That's a different component than the
15 packet memory, but they're connected together as a circuit. I'll leave
16 it at that, but just state that the prior art's configuration of multiple
17 components corresponding to a circuit is consistent with the 518
18 patent's embodiment.

19 Nowhere in the prosecution history is the argument made that
20 the memory must be a single component itself, right? That's never
21 made in the prosecution history. There are other reasons for
22 distinguishing the prior art during prosecution, and that wasn't one of
23 them.

24 JUDGE CASS: Counsel, this is Judge Cass.

25 MR. HUH: Yes.

1 JUDGE CASS: I took a look at the 518 specification, and I
2 didn't see any place really -- other than in the claims -- that they used
3 memory circuit, those two words put together. I just wanted to get a
4 sense if you had seen that anywhere in the spec itself or somewhere
5 else in the intrinsic evidence other than the claims because it's not
6 something that I saw.

7 MR. HUH: No -- to answer your question, the answer is the 518
8 patent specification, we didn't find the phrase memory circuit. This is
9 why our perspective would be is that the memory circuit can, in fact,
10 correspond to different components collectively creating a circuit, just
11 like on Slide 31. And that's our position, is that whether you require a
12 single circuit or whether -- but the patent itself clearly shows that you
13 have different components that make up a circuit, and those different
14 components will, in fact, store the different claimed elements.

15 JUDGE CASS: Thank you, Counsel.

16 MR. HUH: Sure, my pleasure. I want to make two more points
17 just briefly, just for the record. We heard Patent Owner's counsel
18 argue about Gai's claims, that the claims are directed to Layer 3. That
19 argument was never made in any brief, and that was an admission by
20 their own expert during deposition who admitted that he improperly
21 limited the prior art understanding to what the prior art allegedly
22 claims. But there is no evidence or support in the record to buttress
23 Patent Owner's assertion that Gai is somehow claiming only Layer 3.
24 That was never developed. I would also note we heard Patent Owner's
25 counsel argue about the number of connections to a port. That

1 argument is irrelevant because nothing in the claim recites the number
2 of connections.

3 Lastly, I would note, and I think the Board already properly
4 recognized that the Kwan reference clearly teaches utilizing both
5 MAC addresses and IP addresses. It's not limited to Layer 2, and the
6 patent itself -- the 518 patent -- did not invent using MAC addresses
7 with IP addresses. Kwan teaches that, and their own expert admitted
8 during deposition that that was known in the art. I went through that
9 initially this morning, Your Honors, that their expert admitted, as
10 shown on Slide 8, that it was known in the art to use access control
11 lists and IP addresses. The 518 patent did not invent this concept of
12 using IP addresses and MAC addresses together, and Kwan is not
13 limited to Layer 2 because it also uses IP addresses and access control
14 lists. I'll stop here in the interest of time. Are there any questions?

15 JUDGE AMUNDSON: It looks like the panel has no questions.
16 Okay, very well. Let's go back to Mr. Auchter. You may begin
17 whenever you're ready.

18 MR. AUCHTER: Thank you, Your Honor. I'm Robert Auchter
19 on behalf of Patent Owner. Just a couple of points in rebuttal -- I'm
20 trying to be precisely on point on the rebuttals. With respect to
21 Petitioner's Slide 29, it does show a processor coupled with a
22 forwarding circuit, and it also shows a processor coupled to the
23 memory. Those are two separate couplings. That does not mean that
24 the forwarding circuit would be coupled to the memory. The claim
25 says, for example, at 15.3.1 on Patent Owner's Slide 3, that a

1 processor coupled with a forwarding circuit and a memory circuit,
2 which is consistent with what's shown in Figure 3 of the 518 patent. I
3 also would note that the NVRAM is, in fact, not coupled to the
4 TCAM in Gai's disclosure.

5 There is an ACL device in between there that converts at the
6 ACL converter, which changes its format and converts it into a binary
7 decision diagram and what have you, depending on how far into the
8 disclosure you go into Gai. Therefore, one would have to say that
9 looking at the entirety of what's disclosed, the NVRAM memory is, in
10 fact, not coupled to the forwarding entity. Clearly the TCAM is
11 coupled to the forwarding entity in Gai's disclosure. With respect to
12 Dr. Cole's inability to remember the specific disclosure, I think the
13 518 patent specification speaks for itself. It does include a disclosure
14 where the packets and the enhanced access control list are specifically
15 stored in the memory circuit or the packet memory as corresponding
16 in the figure. Again, the dynamic access control list at least was in the
17 claims which were part of the originally filed specification, do
18 specifically claim that the dynamic access control list is stored in the
19 packet memory.

20 Lastly, I would say that even in the Gai reference -- the
21 dynamic ACL -- is not stored in the forwarding entity. It is in fact
22 stored in the TCAM memory, which is shown to the right of the
23 forwarding entity. I believe that's consistent in the art. If there are no
24 further questions, then I'd like to thank the Board very much. If there
25 are questions, I'm glad to --

1 JUDGE CASS: Counsel, I have a couple questions. This is
2 Judge Cass. I want to follow-up on some questions that I asked
3 Petitioner's counsel. First of all, other than the claim language itself,
4 is there anything in the intrinsic evidence that defines or helps us
5 define what the term memory circuit means, because we have an issue
6 here, can it be one component, can it be multiple components. Is there
7 anything we can look to there?

8 MR. AUCHTER: Not that I know of, Your Honor. I've looked
9 at the specification, how the apparatus was described, that it had these
10 three capabilities operable to store these three separate items, and
11 thought about it in terms of it has to be a memory or a kind of memory
12 that could store all three, and then with respect to the specific
13 coupling limitations, how it was coupled within the network switch or
14 whatever the Claim 19 apparatus was -- sorry, I can't remember that
15 right now.

16 JUDGE CASS: So, in your view, could a memory circuit
17 include multiple memory components linked together?

18 MR. AUCHTER: I would not think of that as being a memory
19 circuit, Your Honor. I would think of that as being multiple memories.
20 There are a couple of reasons why. First off, they're incompatible
21 memories in the sense that the TCAM can't be used to store a packet,
22 and an NVRAM would not be used to store a packet, that a POSITA
23 would not look at that as being a single memory circuit. Also, and this
24 is going very far afield, I think just the fabrication of the different

1 kinds of memory circuits would be complicated, but there is nothing
2 in the record that addresses that issue.

3 JUDGE CASS: All right, thank you, Counsel.

4 JUDGE AMUNDSON: This is Judge Amundson. Just to follow
5 up on the point about the intrinsic evidence, do you have the 518
6 patent there?

7 MR. AUCHTER: yes, Your Honor, somewhere.

8 JUDGE AMUNDSON: Okay, and if you can go to Column 10 -

9 -

10 MR. AUCHTER: I have the figures in front of me, but where
11 did I put the text? Oh, there it is. All right, Your Honor, Column 10?

12 JUDGE AMUNDSON: Column 10, yes. If we could focus on
13 the top of Column 10, starting in Line 1, and I'll quote from Lines 1
14 through 3. It states, components 300 to 306 may be combined to be
15 performed by fewer elements or divided out and performed by more
16 elements, unquote. Could you explain why that doesn't support
17 Petitioner's position that three components could comprise the
18 memory circuit?

19 MR. AUCHTER: Yes, Your Honor. First off, because they
20 didn't cite to it, but of course, it is part of the specification. Secondly,
21 because it's prefaced, if one looks down at Column 9 beginning at
22 Line 65, by a description that you could have different functions
23 performed, that the functions performed by these various elements
24 could be performed by other -- could be combined, et cetera. I believe
25 that the predicate to the fewer elements are divided out and performed

1 by more elements in Column 10 is that the functions would be
2 performed by different or other elements, as well. Also, it's been a
3 long time since I wrote claims or a spec, but there is a bad habit of
4 having broad language at the end of a detailed description.

5 JUDGE AMUNDSON: Well, but okay, on that point you make
6 about functions, but why wouldn't one function be function 1, storing
7 packets, function 2, storing enhanced access control lists, function 3,
8 storing dynamic access control lists?

9 MR. AUCHTER: That could be, Your Honor, but then I don't
10 believe that would meet the claim limitations.

11 JUDGE AMUNDSON: All right, okay, I think I understand
12 your position. Let's see if there are any further questions from the
13 panel.

14 JUDGE REIMERS: Nothing further from me.

15 JUDGE CASS: Nothing further from me, either.

16 JUDGE AMUNDSON: All right, all right. With that, that
17 concludes our hearing. Thank you to both parties for your time and
18 your helpful presentations. The case is submitted and the hearing is
19 adjourned.

20 (Whereupon, the above-entitled matter went off the record at
21 12:47 p.m.)

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