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(54) [Title the Invention]

Semiconductor Integrated Circuit Device, Nonvolatile Semiconductor Storage Device, and Manufacturing Method

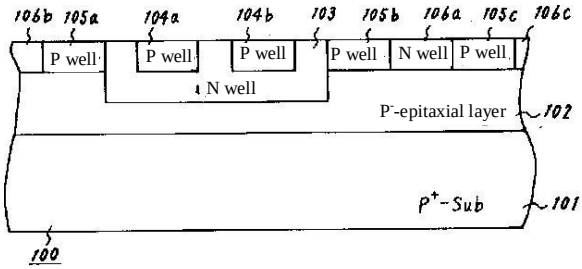
(57) Abstract

[OBJECT]

To provide a nonvolatile semiconductor storage device with improved latch-up resistance and punch-through breakdown voltage and improved junction breakdown voltage between the well regions and the semiconductor substrate.

[STRUCTURE]

A lightly-doped P-type epitaxial layer 102a is formed on the surface of a first semiconductor layer 101 that is made from a heavily-doped P-type silicon substrate. Boron [B] is implanted into the surface of this epitaxial layer 102a and a heat treatment is carried out to produce a lightly-doped P-type second semiconductor layer 102. Regions other than a desire region are masked, phosphorus is implanted, and a heat treatment is carried out to form an N-type first well region 103. Regions other than the desired region are masked, boron [B] is implanted, and the boron implantation layer is then masked and phosphorus is implanted, and a heat treatment is carried out to form P-type second well regions 104a and 104b, P-type third well regions 105a through 105c, and N-type fourth well regions 106a through 106c.



[PATENT CLAIMS]
[CLAIM 1]
A semiconductor integrated circuit device comprising:
a semiconductor substrate having a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, a first well region of a second conductivity type, formed in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, a second well region, of the first semiconductor type, formed in the surface of the first well region, a third well region, of the first conductivity type, formed in the surface of the second semiconductor layer, with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and a fourth well region, of the second conductivity type, formed separated from the first well region, in the second semiconductor layer;
a first semiconductor device that is formed in the second well region of the semiconductor substrate;
a second semiconductor device that is formed in the third well region of the semiconductor substrate; and
a third semiconductor device that is formed in the fourth well region of the semiconductor substrate.
[CLAIM 2]
A nonvolatile semiconductor storage device, comprising:
a semiconductor substrate having a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, a first well region of a second conductivity type, formed in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, a second well region, of the first semiconductor type, formed in the surface of the first well region, a third well region, of the first conductivity type, formed in the surface of the second semiconductor layer, with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and a fourth well region, of the second conductivity type, formed separated from the first well region, in the second semiconductor layer;
a nonvolatile memory cell having a source region, formed in the second well region of the semiconductor substrate, comprising a diffusion layer, of the second conductivity type, that is connected to a corresponding source line, a drain region, formed separate from the source region, comprising a diffusion layer, of the second conductivity type, that is connected to a corresponding bit line, a floating gate electrode formed over the second well region, positioned between the source region and the drain region, with a gate oxide film, comprising a tunnel oxide film, interposed therebetween, and a control gate electrode, disposed facing the floating gate electrode, with an interlayer insulating film interposed therebetween, and connected to a corresponding word line;
an MOS transistor of the second conductivity type having a source region, formed in the third well region of the semiconductor substrate and comprising a diffusion layer of the second conductivity type, a drain region, formed separated from the source region and comprising a diffusion layer of the second conductivity type, and a gate electrode formed over the third well region, positioned between the source region and the drain region, with a gate oxide film interposed therebetween; and
an MOS transistor of a first conductivity type, formed in the fourth well region of the semiconductor substrate, having a source region comprising a diffusion layer of the first conductivity type, a drain region formed separated from the source region and having a diffusion layer of the first conductivity type, and a gate electrode formed over the fourth well region, positioned between the source region and the drain region, with a gate oxide film interposed therebetween.
[CLAIM 3]
A nonvolatile semiconductor storage device comprising:
a memory cell array having a plurality of memory cells, each having a source region that is connected to a corresponding source line, a drain region that is connected to a corresponding bit line, a floating gate electrode for storing information, and a control gate electrode that is connected to a corresponding word line; and peripheral circuitry for writing information to a memory cell of the memory cell array, reading out information that has been stored in the memory cell, and erasing information that has been stored in the memory cell; wherein: the plurality of memory cells in the memory cell array is divided into a plurality of blocks of a plurality of memory cells each, where the erasing operation is carried out as multiple bits by the block unit, comprising:
a semiconductor substrate having a P-type first semiconductor layer, a P-type second semiconductor layer, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, an N-type first well region, formed in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, a plurality of P-type second well regions formed separated from each other in the surface of the first well region, a P-type third well region formed in the surface of the second semiconductor layer with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and an N-type fourth well region formed separated from the first well region in the second semiconductor layer, wherein:
for each block unit, the plurality of memory cells for the individual block unit, corresponding to one of the plurality of second well regions, is formed in the corresponding second well region;
at least some N-channel MOS transistors of the plurality of the N-channel MOS transistors that structure the peripheral circuitry are formed in the third well region; and

at least some of the P-channel MOS transistors of the plurality of P-channel MOS transistors that structure the peripheral circuitry are formed in the fourth well region.

[CLAIM 4]

A nonvolatile semiconductor storage device comprising:

a memory cell array having a plurality of memory cells, each having a source region that is connected to a corresponding source line, a drain region that is connected to a corresponding bit line, a floating gate electrode for storing information, and a control gate electrode that is connected to a corresponding word line; and peripheral circuitry for writing information to a memory cell of the memory cell array, reading out information that has been stored in the memory cell, and erasing information that has been stored in the memory cell; wherein: the plurality of memory cells in the memory cell array is divided into a plurality of blocks of a plurality of memory cells each, where the erasing operation is carried out as multiple bits by the block unit, comprising:

a semiconductor substrate having a P-type first semiconductor layer, a P-type second semiconductor layer, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, a plurality of N-type first well regions formed separated from each other in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well regions and the surface of the first semiconductor layer, a plurality of P-type second well regions formed respectively in the surfaces of the respective first well regions, a P-type third well region formed in the surface of the second semiconductor layer with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and an N-type fourth well region formed separated from the first well region in the second semiconductor layer, wherein:

for each block unit, the plurality of memory cells for the individual block unit, corresponding to one of the plurality of second well regions, is formed in the corresponding second well region;

at least some N-channel MOS transistors of the plurality of the N-channel MOS transistors that structure the peripheral circuitry are formed in the third well region; and

at least some of the P-channel MOS transistors of the plurality of P-channel MOS transistors that structure the peripheral circuitry are formed in the fourth well region.

[CLAIM 5]

A nonvolatile semiconductor storage device comprising:

a memory cell array having a plurality of memory cells, each having a source region that is connected to a corresponding source line, a drain region that is connected to a corresponding bit line, a floating gate electrode for storing information, and a control gate electrode that is connected to a corresponding word line; and peripheral circuitry for writing information to a memory cell of the memory cell array, reading out information that has been stored in the memory cell, and erasing information that has been stored in the memory cell; the peripheral circuitry has a voltage step-up circuit for receiving a power supply voltage that is applied to a power supply voltage node and outputting a stepped-up electropotential that is higher than that of the power supply voltage, comprising:

a semiconductor substrate having a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, a first well region of a second conductivity type, formed in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, a second well region, of the first semiconductor type, formed in the surface of the first well region, a third well region, of the first conductivity type, formed in the surface of the second semiconductor layer, with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and a fourth well region, of the second conductivity type, formed separated from the first well region, in the second semiconductor layer, wherein:

a semiconductor device for structuring and output stage of the voltage step-up circuit is formed in the second well region;

at least some MOS transistors of the plurality of the MOS transistors of the second conductivity type that structure the peripheral circuitry are formed in the third well region; and

at least some MOS transistors of the plurality of the MOS transistors of the first conductivity type that structure the peripheral circuitry are formed in the third well region.

[CLAIM 6]

The nonvolatile semiconductor storage device set forth in claim 5, wherein:

a semiconductor device for structuring the output stage of the voltage step-up circuit is a bipolar transistor wherein the diffusion region of a second conductivity type that is formed in the surface of the second well region is used as the emitter region, the second well region is used as the base region, the first well region is used as the collector region, and the base region and the collector region are connected electrically.

[CLAIM 7]

A method for manufacturing a semiconductor integrated circuit device, including:

a step for forming an epitaxial layer through epitaxial deposition on a surface of a first semiconductor layer of a first conductivity type;

a step for forming, on the surface of the first semiconductor layer, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through ion implantation of a dopant of the first conductivity type into the surface of the epitaxial layer and performing thermal diffusion;

a step for forming, in the surface of the second semiconductor layer, a first well region of a second conductivity type, with the second semiconductor layer interposed between the surface of the first semiconductor layer and the first well region;

a step for forming a second well region of the first conductivity type in the surface of the first well region;

a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer;

a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region;

a step for forming a first semiconductor device in the second well region;

a step for forming a second semiconductor device in the third well region; and

a step for forming a third semiconductor device in the fourth well region.

[CLAIM 8]

A method for manufacturing a semiconductor integrated circuit device, including:

a step for forming, on the surface of a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through epitaxial deposition onto the surface of the first semiconductor layer of the first conductivity type;

a step for forming a first well region of a second conductivity type, in the surface of the second semiconductor layer, with the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, including a step for ion implantation of a dopant of the second conductivity type such that the peak of the dopant concentration will be positioned at a position of a prescribed depth from the surface of the second semiconductor layer;

a step for forming, in the surface of the first well region, a second well region of the first conductivity type at a prescribed position in the first well region above the position of the peak of the dopant concentration;

a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer;

a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region;

a step for forming a first semiconductor device in the second well region;

a step for forming a second semiconductor device in the third well region; and

a step for forming a third semiconductor device in the fourth well region.

[CLAIM 9]

A method for manufacturing a semiconductor integrated circuit device, including:

a step for forming an epitaxial layer through epitaxial deposition on a surface of a first semiconductor layer of a first conductivity type;

a step for forming, on a surface of the first semiconductor layer, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through ion implantation of a dopant of the first conductivity type so that the peak of the dopant concentration will be positioned at a position that is a prescribed depth from the surface of the epitaxial layer;

a step for forming, in the surface of the second semiconductor layer, a first well region of a second conductivity type, with the peak position of the second semiconductor layer interposed between the first well region and a surface of the first semiconductor layer;

a step for forming a second well region of the first conductivity type in the surface of the first well region;

a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer;

a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region;

a step for forming a first semiconductor device in the second well region;

a step for forming a second semiconductor device in the third well region; and

a step for forming a third semiconductor device in the fourth well region.

[CLAIM 10]

A method for manufacturing a semiconductor integrated circuit device, including:

a step for forming an epitaxial layer through epitaxial deposition on a surface of a first semiconductor layer of a first conductivity type;

a step for forming, on a surface of the first semiconductor layer, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through ion implantation of a dopant of the first conductivity type so that the peak of the dopant concentration will be positioned at a position that is a prescribed depth from the surface of the epitaxial layer;

a step for forming a first well region of a second conductivity type, in the surface of the second semiconductor layer, with a peak position of the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, including a step for ion implantation of a dopant of the second conductivity type such that the peak of the dopant concentration will be positioned at a position of a prescribed depth from the surface of the second semiconductor layer;

a step for forming, in the surface of the first well region, a second well region of the first conductivity type at a prescribed position in the first well region above the position of the peak of the dopant concentration;

a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer;

a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region;

a step for forming a first semiconductor device in the second well region;

a step for forming a second semiconductor device in the third well region; and

a step for forming a third semiconductor device in the fourth well region.

[CLAIM 11]

A method for manufacturing a semiconductor integrated circuit device, including:

a step for forming, on the surface of a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through epitaxial deposition onto the surface of the first semiconductor layer of the first conductivity type;

a step for forming, in the surface of the second semiconductor layer, a first well region of a second conductivity type, through implantation, into the surface of the second semiconductor layer, dopant of the second semiconductor type, to form an ion implantation layer in the surface layer of the second semiconductor layer, followed by thermally diffusing the dopant that has been implanted into the ion implantation layer with the value of $4\sqrt{Dt}$ (where D is a diffusion coefficient of the dopant of the second conductivity type that is implanted through ion implantation and t is the diffusion time) at a value that is less than the thickness of the second semiconductor layer;

a step for forming a second well region of the first conductivity type in the surface of the first well region;

a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer;

a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region;

a step for forming a first semiconductor device in the second well region;

a step for forming a second semiconductor device in the third well region; and

a step for forming a third semiconductor device in the fourth well region.

[CLAIM 12]

A method for manufacturing a semiconductor integrated circuit device, including:

a step for forming, on the surface of a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through epitaxial deposition onto the surface of the first semiconductor layer of the first conductivity type;

a step for forming, in a surface of the second semiconductor layer, a first well region of a second conductivity type through ion implantation, into the surface of the second semiconductor layer, of a dopant of the second conductivity type with the value of $(Rp + 3\Delta Rb)$ being a value that is less than the thickness of the second semiconductor layer;

a step for forming a second well region of the first conductivity type in the surface of the first well region;

a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer;

a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region;

a step for forming a first semiconductor device in the second well region;

a step for forming a second semiconductor device in the third well region; and

a step for forming a third semiconductor device in the fourth well region.

[DETAILED EXPLANATION OF THE INVENTION]

[0001]

[FIELD OF APPLICATION IN INDUSTRY]

The present invention relates to a semiconductor integrated circuit device, to a nonvolatile semiconductor storage device, and to methods of manufacturing thereof, and, in particular, relates to a nonvolatile semiconductor storage device wherein a triple-well structure is formed in an epitaxial substrate.

[0002]

[PRIOR ART]

With the ability to manufacture flash memory, which is a type of nonvolatile semiconductor storage device, less expensively than dynamic random access memory (DRAMs) in recent years, these are anticipated to be the memory devices for the next generation. Memory cells in this type of flash memory have source regions that are connected to corresponding source lines, drain regions that are connected to corresponding bit lines, floating gate electrodes for storing information, and control gate electrodes that are connected to corresponding word lines, and while electrons are injected into the floating gate electrodes through, for example, the channel hot electron phenomenon or FN tunneling phenomenon of the gate insulating film that is made from a tunnel oxide film that is positioned directly below the floating gate electrode, erasure or writing is carried out through extracting electrons that are stored in the floating gate electrode, and a binary state of the threshold value is produced depending on the state of the electrons in the floating gate electrode, and a "0" or a "1" is read out depending on that state.

Typically, in a flash memory, all memory cells are erased electrically simultaneously, but recently multibit erasure by block units that have a plurality of memory cells has become predominant. Such a device is described as DINOR-type flash memory in, for example, "IEEE Journal of Solid-State Circuits, Vol. 29, No. 4, April 1994," Pages 454 through 460, or IEICE Trans. Electron., Vol. E77C, No. 8, August 1994, Pages 1279 through 1286.

[0004]

[PROBLEM SOLVED BY THE PRESENT INVENTION]

In such a flash memory, when a plurality of memory cells is erased as multiple bits by the block unit, a back gate (Vbb) voltage is applied to the well region in which the memory cells are formed, and a higher voltage is applied than the power supply voltage in the drain region or source region of the memory cells when erasing or writing. Consequently, there is a tendency to become a structure

wherein latch-up is inherently likely to occur due to transistors of a parasitic thyristor structure.

[0005]

Additionally, because a triple-well structure, wherein a well region that further surrounds the well region in which the memory cells are formed are further provided in order to electrically insulate, from the semiconductor substrate, the well regions wherein memory cells are formed in the block units, it is necessary to consider also the punch-through breakdown voltage between the semiconductor substrate and the well regions in which the memory cells are formed. Moreover, as the level of integration increases and the areas occupied by the memory cells become smaller, it will be necessary to improve further the quality of the gate insulating films for injecting and extracting electrons. Moreover, there is a tendency for the high-voltage generating circuits, for generating the high voltages that are used when erasing or writing, to be formed together on the semiconductor substrate where the memory cells are formed, in which case it is necessary to consider the junction breakdown voltage between the semiconductor substrate and the well region wherein the semiconductor devices that structure the high-voltage generating circuit are formed.

[0006]

This invention was created in consideration of the points set forth above, and the object thereof is to provide a semiconductor integrated circuit device and nonvolatile semiconductor storage device with improved resistance to latch-up, and to provide manufacturing methods thereof. Moreover, a second object of the invention is to provide a semiconductor integrated circuit device and a nonvolatile semiconductor storage device that has an improved punch-through breakdown voltage between a well region and the semiconductor substrate, and to provide manufacturing methods thereof. Furthermore, a third object of the present invention is to provide a nonvolatile semiconductor storage device that has a long service life, wherein information can be written many times, and to provide a manufacturing method thereof. Moreover, a fourth object of the present invention is to provide a semiconductor integrated circuit device and a nonvolatile semiconductor storage device wherein the junction breakdown voltage between a well region and the semiconductor substrate is improved, and to provide a manufacturing methods thereof.

[0007]

[MEANS FOR SOLVING THE PROBLEM]

A semiconductor integrated circuit device according to a first aspect of the present invention comprises: a semiconductor substrate having a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, a first well region of a second conductivity type, formed in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, a second well region, of the first semiconductor type, formed in the surface of the first well region, a third well region, of the first conductivity type, formed in the surface of the second semiconductor layer, with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and a fourth well region, of the second conductivity type, formed separated from the first well region, in the second semiconductor layer; provided with: a first semiconductor device that is formed in the second well region of the semiconductor substrate; a second semiconductor device that is formed in the third well region of the semiconductor substrate; and a third semiconductor device that is formed in the fourth well region of the semiconductor substrate.

[0008]

A nonvolatile semiconductor storage device according to a second aspect of the present invention comprises: a semiconductor substrate having a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, a first well region of a second conductivity type, formed in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, a second well region, of the first semiconductor type, formed in the surface of the first well region, a third well region, of the first conductivity type, formed in the surface of the second semiconductor layer, with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and a fourth well region, of the second conductivity type, formed separated from the first well region, in the second semiconductor layer; provided with: a nonvolatile memory cell that is formed in the second well region of the semiconductor substrate; an MOS transistor of the second conductivity type that is formed in the third well region of the semiconductor substrate; and an MOS transistor of the first conductivity type that is formed in the fourth well region of the semiconductor substrate.

[0009]

A nonvolatile semiconductor storage device according to a third aspect of the present invention comprises: a memory cell array having a plurality of memory cells; and peripheral circuitry for writing information to a memory cell of the memory cell array, reading out information that has been stored in the memory cell, and erasing information that has been stored in the memory cell; wherein: the plurality of memory cells in the memory cell array is divided into a plurality of blocks of a plurality of memory cells each, where the erasing operation is carried out as multiple bits by the block unit, comprising: a semiconductor substrate having a P-type first semiconductor layer, a P-type second semiconductor layer, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, an N-type first well region, formed in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, a plurality of P-type second well regions formed separated from each other in the surface of the first well region, a P-type third well region formed in the surface of the second

semiconductor layer with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and an N-type fourth well region formed separated from the first well region in the second semiconductor layer, wherein: for each block unit, the plurality of memory cells for the individual block unit, corresponding to one of the plurality of second well regions, is formed in the corresponding second well region; at least some N-channel MOS transistors of the plurality of the N-channel MOS transistors that structure the peripheral circuitry are formed in the third well region; and at least some of the P-channel MOS transistors of the plurality of P-channel MOS transistors that structure the peripheral circuitry are formed in the fourth well region.

[0010]

A nonvolatile semiconductor storage device according to a fourth aspect of the present invention comprises: a memory cell array having a plurality of memory cells; and peripheral circuitry for writing information to a memory cell of the memory cell array, reading out information that has been stored in the memory cell, and erasing information that has been stored in the memory cell; wherein: the plurality of memory cells in the memory cell array is divided into a plurality of blocks of a plurality of memory cells each, where the erasing operation is carried out as multiple bits by the block unit, comprising: a semiconductor substrate having a P-type first semiconductor layer, a P-type second semiconductor layer, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, a plurality of N-type first well regions formed separated from each other in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well regions and the surface of the first semiconductor layer, a plurality of P-type second well regions formed respectively in the surfaces of the respective first well regions, a P-type third well region formed in the surface of the second semiconductor layer with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and an N-type fourth well region formed separated from the first well region in the second semiconductor layer, wherein: for each block unit, the plurality of memory cells for the individual block unit, corresponding to one of the plurality of second well regions, is formed in the corresponding second well region; at least some N-channel MOS transistors of the plurality of the N-channel MOS transistors that structure the peripheral circuitry are formed in the third well region; and at least some of the P-channel MOS transistors of the plurality of P-channel MOS transistors that structure the peripheral circuitry are formed in the fourth well region.

[0011]

A nonvolatile semiconductor storage device according to a fifth aspect of the present invention comprises: a memory cell array having a plurality of memory cells; and peripheral circuitry for writing information to a memory cell of the memory cell array, reading out information that has been stored in the memory cell, and erasing information that has been stored in the memory cell; the peripheral circuitry has a voltage step-up circuit for receiving a power supply voltage that is applied to a power supply voltage node and outputting a stepped-up electropotential that is higher than that of the power supply voltage, comprising: a semiconductor substrate having a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, a first well region of a second conductivity type, formed in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, a second well region, of the first semiconductor type, formed in the surface of the first well region, a third well region, of the first conductivity type, formed in the surface of the second semiconductor layer, with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and a fourth well region, of the second conductivity type, formed separated from the first well region, in the second semiconductor layer, wherein: a semiconductor device for structuring and output stage of the voltage step-up circuit is formed in the second well region; at least some MOS transistors of the plurality of the MOS transistors of the second conductivity type that structure the peripheral circuitry are formed in the third well region; and at least some MOS transistors of the plurality of the MOS transistors of the first conductivity type that structure the peripheral circuitry are formed in the third well region.

[0012]

A method for manufacturing a semiconductor integrated circuit device according to a sixth aspect of the present invention includes: a step for forming an epitaxial layer through epitaxial deposition on a surface of a first semiconductor layer of a first conductivity type; a step for forming, on the surface of the first semiconductor layer, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through ion implantation of a dopant of the first conductivity type into the surface of the epitaxial layer and performing thermal diffusion; a step for forming, in the surface of the second semiconductor layer, a first well region of a second conductivity type, with the second semiconductor layer interposed between the surface of the first semiconductor layer and the first well region; a step for forming a second well region of the first conductivity type in the surface of the first well region; a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer; a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region; a step for forming a first semiconductor device in the second well region; a step for forming a second semiconductor device in the third well region; and a step for forming a third semiconductor device in the fourth well region.

[0013]

A method for manufacturing a semiconductor integrated circuit device according to a seventh aspect of the present invention includes: a step for forming, on the surface of a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through epitaxial deposition onto the surface of the first semiconductor layer of the first conductivity type; a step for forming a first well region of a second conductivity type, in the surface of the second semiconductor layer, including a step for ion implantation of a dopant of the second conductivity type such that the peak of the dopant concentration will be positioned at a position of a prescribed depth from the surface of the second semiconductor layer; a step for forming, in the surface of the first well region, a second well region of the first conductivity type at a prescribed position in the first well region above the position of the peak of the dopant concentration; a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer; a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region; a step for forming a first semiconductor device in the second well region; a step for forming a second semiconductor device in the third well region; and a step for forming a third semiconductor device in the fourth well region.

[0014]

A method for manufacturing a semiconductor integrated circuit device according to an eighth aspect of the present invention includes: a step for forming an epitaxial layer through epitaxial deposition on a surface of a first semiconductor layer of a first conductivity type; a step for forming, on a surface of the first semiconductor layer, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through ion implantation of a dopant of the first conductivity type so that the peak of the dopant concentration will be positioned at a position that is a prescribed depth from the surface of the epitaxial layer; a step for forming, in the surface of the second semiconductor layer, a first well region of a second conductivity type; a step for forming a second well region of the first conductivity type in the surface of the first well region; a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer; a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region; a step for forming a first semiconductor device in the second well region; a step for forming a second semiconductor device in the third well region; and a step for forming a third semiconductor device in the fourth well region.

[0015]

A method for manufacturing a semiconductor integrated circuit device according to a ninth aspect of the present invention including: a step for forming an epitaxial layer through epitaxial deposition on a surface of a first semiconductor layer of a first conductivity type; a step for forming, on a surface of the first semiconductor layer, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through ion implantation of a dopant of the first conductivity type so that the peak of the dopant concentration will be positioned at a position that is a prescribed depth from the surface of the epitaxial layer; a step for forming a first well region of a second conductivity type, in the surface of the second semiconductor layer, with a peak position of the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, including a step for ion implantation of a dopant of the second conductivity type such that the peak of the dopant concentration will be positioned at a position of a prescribed depth from the surface of the second semiconductor layer; a step for forming, in the surface of the first well region, a second well region of the first conductivity type; a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer; a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region; a step for forming a first semiconductor device in the second well region; a step for forming a second semiconductor device in the third well region; and a step for forming a third semiconductor device in the fourth well region.

[0016]

A method for manufacturing a semiconductor integrated circuit device according to a tenth aspect of the present invention includes: a step for forming, on the surface of a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through epitaxial deposition onto the surface of the first semiconductor layer of the first conductivity type; a step for forming, in the surface of the second semiconductor layer, a first well region of a second conductivity type, through implantation, into the surface of the second semiconductor layer, dopant of the second semiconductor type, followed by thermally diffusing the dopant that has been implanted with the value of $4\sqrt{Dt}$ at a value that is less than the thickness of the second semiconductor layer; a step for forming a second well region of the first conductivity type in the surface of the first well region; a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer; a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region; a step for forming a first semiconductor device in the second well region; a step for forming a second semiconductor device in the third well region; and a step for forming a third semiconductor device in the fourth well region.

[0017]

A method for manufacturing a semiconductor integrated circuit device according to a tenth aspect of the present invention includes: a step for forming, on the surface of a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through epitaxial deposition onto the surface of the first semiconductor layer of the first conductivity type; a step for forming, in the surface of the second semiconductor layer, a first well region of a second conductivity type, through implantation, into the surface of the second semiconductor layer, dopant of the second semiconductor type, with the value of ($Rp+3\Delta Rp$) at a value that is less than the thickness of the second semiconductor layer; a step for forming a second well region of the first conductivity type in the surface of the first well region; a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer; a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region; a step for forming a first semiconductor device in the second well region; a step for forming a second semiconductor device in the third well region; and a step for forming a third semiconductor device in the fourth well region.

[0018]

[OPERATION]

In the first aspect of this invention, the lightly-doped second semiconductor layer that is formed through epitaxial deposition is interposed between the first well region and the heavily-doped first semiconductor layer, reducing the tendency for latch-up and for punch-through between the second well region and the second semiconductor layer, and increasing the junction breakdown voltage between the first well region and the second semiconductor layer.

[0019]

In the second aspect of this invention, the lightly-doped second semiconductor layer that is formed through epitaxial deposition is interposed between the first well region and the heavily-doped first semiconductor layer, reducing the tendency for latch-up and for punch-through between the second well region and the second semiconductor layer, and increasing the junction breakdown voltage between the first well region and the second semiconductor layer, where the second semiconductor layer also reduces the gate insulating film dopant concentration and defect density.

[0020]

In the third aspect of this invention, the first well region makes it possible to apply electropotentials independently to the second well regions, and the lightly-doped second semiconductor layer that is formed through epitaxial deposition is interposed between the first well region and the heavily-doped first semiconductor layer, reducing the tendency for latch-up and for punch-through between the second well region and the second semiconductor layer, and increasing the junction breakdown voltage between the first well region and the second semiconductor layer, where the second semiconductor layer also reduces the gate insulating film dopant concentration and defect density.

[0021]

In the fourth aspect of this invention, the first well region makes it possible to apply electropotentials independently to the second well regions, and the lightly-doped second semiconductor layer that is formed through epitaxial deposition is interposed between the first well region and the heavily-doped first semiconductor layer, reducing the tendency for latch-up and for punch-through between the second well region and the second semiconductor layer, and increasing the junction breakdown voltage between the first well region and the second semiconductor layer, where the second semiconductor layer also reduces the gate insulating film dopant concentration and defect density.

[0022]

In the fifth aspect of this invention, the lightly-doped second semiconductor layer that is formed through epitaxial deposition is interposed between the first well region and the heavily-doped first semiconductor layer, reducing the tendency for latch-up and for punch-through between the second well region and the second semiconductor layer, and increasing the junction breakdown voltage between the first well region and the second semiconductor layer for the semiconductor devices that structure the output stage of a voltage step-up circuit.

[0023]

In the sixth aspect of the present invention, the first well region is formed with a lightly-doped second semiconductor layer that is formed through epitaxial deposition interposed between the first well region and the surface of the first semiconductor layer, reducing the tendency for latch-up, with the interposed lightly-doped second semiconductor layer reducing the tendency for latch-up and for punch-through between the second well region and the second semiconductor layer, and increasing the junction breakdown voltage between the first well region and the second semiconductor layer.

[0024]

In the seventh aspect of the present invention, the first well region is formed with a lightly-doped second semiconductor layer that is formed through epitaxial deposition interposed between the first well region and the surface of the first semiconductor layer, reducing the tendency for latch-up, with the interposed lightly-doped second semiconductor layer reducing the tendency for latch-up and for punch-through between the second well region and the second semiconductor layer, and increasing the junction breakdown voltage between the first well region and the second semiconductor layer and, additionally, the step for ion implantation of the dopant of the second conductivity type such that the peak of the dopant concentration will be positioned at a position that is a prescribed depth from the surface of the second semiconductor layer enables the profile of the dopant concentration in the bottom portion of the first well region to be selected freely.

[0025]

In the eighth aspect of the present invention, the first well region is formed with a lightly-doped second semiconductor layer that is formed through epitaxial deposition interposed between the first well region and the

surface of the first semiconductor layer, reducing the tendency for latch-up, with the interposed lightly-doped second semiconductor layer reducing the tendency for punch-through between the second well region and the second semiconductor layer, and increasing the junction breakdown voltage between the first well region and the second semiconductor layer and, additionally, the step for ion implantation of the dopant of the first conductivity type such that the peak of the dopant concentration will be positioned at a position that is a prescribed depth from the surface of the epitaxial layer, for the second semiconductor layer, enables the profile of the dopant concentration in the bottom portion of the second semiconductor layer to be selected freely.

[0026]

In the ninth aspect of the present invention, the first well region is formed with a lightly-doped second semiconductor layer that is formed through epitaxial deposition interposed between the first well region and the surface of the first semiconductor layer, reducing the tendency for latch-up, with the interposed lightly-doped second semiconductor layer reducing the tendency for punch-through between the second well region and the second semiconductor layer, and increasing the junction breakdown voltage between the first well region and the second semiconductor layer and, additionally, and the step for ion implantation of the dopant of the first conductivity type such that the peak of the dopant concentration will be positioned at a prescribed depth from the surface of the epitaxial layer, for the second semiconductor layer, enables the profile of the dopant concentration of the bottom portion of the second semiconductor layer to be selected freely.

[0027]

In the 10th aspect of the present invention, the step for forming a first well region through ion implantation of the dopant of the second conductivity type into the surface of the second semiconductor layer followed by thermal diffusion of the ion-implanted dopant so that the value of $4\sqrt{Dt}$ will be a value that is less than the thickness of the second semiconductor reliably interposes, between the first well region and the heavily-doped first semiconductor layer, a lightly-doped second semiconductor layer that is formed through epitaxial deposition, reducing the tendency for latch-up and for punch-through between the second well region and the second semiconductor layer, and increasing the junction breakdown voltage between the first well region and the second semiconductor layer.

[0028]

In the 11th aspect of the present invention, the step for forming a first well region of the second conductivity type in the surface of the second semiconductor layer through ion implantation of the dopant of the second conductivity type into the surface of the second semiconductor layer so that the value of $(Rp+3\Delta Rp)$ will be a value that is less than the thickness of the second semiconductor reliably interposes, between the first well region and the heavily-doped first semiconductor layer, a lightly-doped second semiconductor layer that is formed through epitaxial deposition, reducing the tendency for latch-up and for punch-through between the second well region and the second semiconductor layer, and increasing the junction breakdown voltage between the first well region and the second semiconductor layer.

[0029]

[EMBODIMENTS]

EMBODIMENT 1

A first embodiment according to the present invention will be explained below based on the drawings. The configuration of a flash memory that is one type of a semiconductor nonvolatile storage device to which this first embodiment is applied will be explained first based on FIG. 1. In FIG. 1, 1_{11} through 1_{42} is each a memory cell having a source region comprising an N-type diffusion layer, a drain region comprising an N-type diffusion layer that is separate from the source region, a floating electrode formed over a channel region that is positioned between the source region and the drain region, with a gate oxide film, comprising a tunnel oxide film, interposed therebetween, and a control gate electrode disposed facing the floating gate electrode with an interlayer insulating films interposed therebetween.

[0030]

For ease in the explanation, only blocks 2a and 2b, for which erasing operations are carried out as multiple bits by two-row and two-column units, are shown; however a memory cell array is structured from a plurality of memory cells 1 that is arranged in the form of a matrix of a plurality of rows and a plurality of columns, where the memory cell array has a plurality of blocks 2 that are a multibit-erasure unit, where each block 2 has memory cells 1 of a plurality of rows and a plurality of columns. The structure is such that the plurality of memory cells 1 that structure each block 2, although described in detail below, are formed in one N-type well region of a plurality of N-type well regions that are formed, separated from each other, in a P-type well region that is formed in the semiconductor substrate, where the application of a substrate electropotential to this N-type well religion applies the substrate electropotential independently for each individual block 2. Note that the suffix number in a reference symbol indicates a row and/or column, where an alphabetic character indicates a separate block unit, where, when indicated in general, this is indicated by omitting the suffix. The same holds true below.

[0031]

3_1 through 3_4 are word lines, arranged at the respectively corresponding rows, that are connected to control gate electrodes of a plurality of memory cells 1 that are arranged in the respectively corresponding rows, structured from a polysilicon layer formed integrally with a control gate electrode that is formed from a polysilicon layer of a second layer (where the floating gate electrode is formed by a polysilicon layer of a first layer), and a metal layer of a first layer that is arranged in parallel on the top of the polysilicon layer. 4_1 through 4_2 are primary bit lines that are disposed in the respectively corresponding columns, formed through a metal layer of a second layer that is disposed over the aforementioned word lines 3. 5_{1a} through 5_{2b} are secondary bit lines that are connected to drain regions of a plurality of memory cells 1 of a block 2 that corresponds to the corresponding column, arranged for each corresponding block 2 and the respectively corresponding columns, formed from a polysilicon layer of

a third layer, disposed over the polysilicon layer of the word line 3.

[0032]

6_{1a} through 6_{2b} are select gates for structuring N-channel MOS transistors, connected between a corresponding secondary bit line 4 and a primary bit line 3 that is disposed in a corresponding column, provided for each of the respectively corresponding secondary bit lines 4, where the gate electrode thereof is formed from the polysilicon layer of the second layer. 7a through 7b are source lines that are connected to source regions of a plurality of memory cells 1 of the corresponding blocks 2, provided for each of the respectively corresponding blocks 2, and 8a through 8b are well electropotential lines that are connected to P-type well regions wherein pluralities of memory cells 1 are formed, in order to apply substrate electropotentials to the plurality of memory cells 1 of the corresponding block 2, provided for each of the respectively corresponding blocks 2.

[0033]

9a through 9b are block select signal lines connected to gate electrodes (control electrodes) of a plurality of select gates 6 that are provided for the corresponding blocks 2, provided for each of the respectively corresponding blocks 2; 10 is an input/output line for sending information for writing to the memory cell 1 and for reading out information stored in the memory cell 1; and 11_1 through 11_2 are transfer gates for structuring N-channel MOS transistors that are connected between corresponding primary bit lines 3 and the input/output line 10, provided for each of the respectively corresponding primary bit lines 4, where the gate electrodes thereof are formed through the polysilicon layer of the second layer. 12_1 through 12_2 are column select signal lines that are connected to the gate electrodes (control electrodes) of the corresponding transfer gates, provided for each of the respectively corresponding transfer gates 11.

[0034]

13 is a row decoder for receiving a row address signal, a write/erase control signal, a first high voltage level (for example, 10 V) that is higher than the power supply voltage (for example, 3.3 V), and a negative electropotential (for example, -8 V), to select, based on the row address signal, a desired number of the plurality of word lines 3 (the number of word lines for the block unit when erasing), to apply, to the selected word line 3, an electropotential selected based on the write/erase control signal, for example, the negative electropotential when writing (where, in this example, an operation that extracts electrons that are stored in the floating gate electrode is termed "writing"), the first high voltage level when erasing (where, in this example, the operation for injecting electrons into the floating gate electrode is termed "erasing"), and the power supply voltage when reading out, while maintaining the other word lines 3 at the ground electropotential.

[0035]

14 is a source/well decoder for receiving a portion of the row address signal, a portion of the column address signal, the write/erase signal, and a negative electropotential (for example, -8 V), and placing the source line 7 and the well electropotential line 8 to the desired electropotential based on the write/erase control signal, the portion of the row address signal and the portion of the column address signal, for example, placing all of the source lines 7 into a floating state and all of the well electropotential lines 8 to the ground electropotential when writing, placing all of the source lines 7 and all of the well electropotential lines 8 to the ground electropotential when reading, and applying the negative electropotential to the well electropotential lines 8 and source lines 7 corresponding to the block 2 selected by the portion of the row address signals and the portion of the column address signals and placing the other source lines 7 and the well electropotential lines 8 to the ground electropotential when erasing.

[0036]

15 is a select gate decoder for receiving a portion of the row address signal, a portion of the column address signal, the write/erase control signal, and a second high-voltage signal (for example, 6 V) that is higher than the power supply voltage (for example, 3.3 V) and lower than the first high voltage level, to select, based on the portion of the row address signal and the portion of the column address signal, one of the plurality of block select signal lines 9, and, based on the write/erase control signal, apply a selected electropotential to the selected block select signal line, for example, the second high voltage level when writing, the ground electropotential when erasing, and the power supply voltage when reading, while maintaining the other block select signal lines 9 in the ground electropotential state.

[0037]

16 is a column decoder for receiving a column address signal, a write/erase control signal, and a second high-voltage level (for example, 6 V) that is higher than the power supply voltage (for example, 3.3 V) and lower than the first high-voltage level, to select, based on the column address signal, one of the plurality of column select signal lines 12 and, based on the write/erase control signal, to apply a selected electropotential to the selected column select signal line 12, for example, the second high-voltage level when writing, the ground electropotential when erasing, or the power supply voltage when reading, while maintaining the other column select signal lines 12 at the ground electropotential state. 17 is an address buffer circuit that receives an address signal inputted into address input pads 18… 18 (where the row address signal and the column address signal are inputted in a time series), to apply address signals to the row decoder 13, the source/well decoder 14, the select gate decoder 15, and the column decoder 16.

[0038]

19 is a writing circuit for receiving the write/erase control signal, data information, and a second high-voltage level (for example, 6 V) that is higher than the power supply voltage (for example, 3.3 V) and lower than the first high-voltage level, to apply the second high-voltage to the input/output line 10 when the writing/erase control signal indicates writing and the data information inputted through the input/output pad 21 and the data input/output buffer 20 indicates programming, where otherwise the output is in a high impedance state, and 22 is a sense amp that receives the write/erase control signal, to be placed into an active state and apply a low-voltage signal (for example, 1.2 V) to the input/output line 10 when the write/erase control signal indicates reading, to detect whether or not there is an electric current, and to perform amplification, to read out

from the selected memory cell 1, to output the information through the data input/output buffer 20 to the input/output pad 21.

[0039]

23 is a first high-voltage generating circuit for receiving the write/erase control signal and applying a first high-voltage level (10 V) to the row decoder 13 based on the write/erase control signal; 24 is a first high-voltage generating circuit for receiving the write/erase control signal and for applying a second high-voltage level (for example, 6 V) to the selected gate decoder 15, column decoder 16, and writing circuit 19, based on the write/erase control signal; 25 is a negative electropotential generating circuit for receiving the write/erase control signal and for applying a negative electropotential (for example, - 8 V) to the row decoder 13 and the source/well decoder 14 based on the write/erase control signal; and 26 is a write/erase controlling circuit for applying the right/erase control signal to the row decoder 13, the source/well decoder 14, the select gate decoder 15, the column decoder 16, the writing circuit 19, the sense amp 22, the first and second high-voltage generating circuits 23 and 24, and the negative voltage generating circuit 25. 27 indicates a chip in a nonvolatile semiconductor storage device.

[0040]

Note that the row decoder 13, the source/well decoder 14, the select gate decoder 15, the column decoder 16, the address buffer circuit 17, the writing circuit 19, the input/output buffer circuit 20, the sense amp 22, the first and second high-voltage generating circuits 23 and 24, the negative voltage generating circuit 25, and the write/erase controlling circuit 26 structure the peripheral circuitry for writing information to a memory cell 1 of the memory cell array, reading information stored in the memory cell 1, and erasing information that is stored in the memory cell 1, where each has a plurality of N-channel MOS transistors and a plurality of P-channel MOS transistors, where the gate electrodes are formed from the polysilicon layer of the second layer.

[0041]

The semiconductor substrate 100 applied in this first embodiment in order to form flash memory that is structured in this way will be explained based on FIG. 2. FIG. 2 depicts critical portions of the semiconductor substrate that is applied to the first embodiment of the present invention; however the number of well regions, and like, are not limited to that which is depicted in FIG. 2. In FIG. 2, 101 is a first semiconductor layer made from a heavily-doped (for example, about 1 x $10^{19}/cm^3$) P-type silicon substrate, and 102 is a P-type second semiconductor layer having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer 101 (for example 1 x $10^{15}/cm^3$, and may be between 1 x $10^{15}/cm^3$ and 1 x 10^{18}), deposited through epitaxial deposition to a thickness of between 1 and 10 µm onto the surface of the first semiconductor layer.

[0042]

103 is an N-type first well region formed in a surface of the second semiconductor layer with the second semiconductor layer 102 interposed between the N-type first well region and the surface of the first semiconductor layer 101, with a depth of, for example, between 1 and about 9 µm, and a dopant concentration between 1 x 10^{15} and 1 x $10^{18}/cm^3$. 104a and 104b are P-type second well regions that are formed in the surface of the first well region with a depth of between 0.5 and about 8.5 µm and a dopant concentration of between 1 x 10^{15} and 1 x $10^{18}/cm^3$. 105a, 105b, and 105c are P-type third well regions formed in the surface of the second semiconductor layer 102, with the second semiconductor layer 102 interposed between the P-type third well region and the surface of the first semiconductor layer 101, with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer 102 (for example, between 1 x $10^{15}/cm^3$ and 1 x 10^{18}), with a depth of, for example, between 0.5 about 8.5 µm, but the depth may be such that it contacts the surface of the first semiconductor layer 101 without intervention of the second semiconductor layer 102. 106a, 106b, and 106c are N-type fourth well regions formed, separated from the first well regions 103, in the surface of the second semiconductor layer 102, with a depth of, for example, between 0.5 and about 9 µm, and a dopant concentration between 1 x 10^{15} and 1 x $10^{18}/cm^3$.

[0043]

The way of thinking about a case wherein a flash memory that is structured as depicted in FIG. 1 is formed on the semiconductor substrate 100 that is structured in this way is depicted in FIG. 3. That is, the memory cells 1 for structuring the memory cell array are formed in second well regions 104a and 104b. In this case, each block unit that is a multibit-erasure unit corresponds to 1 of the plurality of second well regions, where the plurality of memory cells for each block unit is formed in the corresponding second well region, for example, the memory cells 1_{11}, 1_{12}, 1_{21}, and 1_{22} that structure the block 2a are formed in the second well region 104a, and the memory cells 1_{31}, 1_{32}, 1_{41}, and 1_{42} that structure the block 2b are formed in the second well region 104b.

[0044]

On the other hand, in the row decoder 13, the source/well decoder 14, the select gate decoder 15, the column decoder 16, the address buffer circuit 17, the writing circuit 19, the input/output buffer circuit 20, the sense amp 22, the first and second high-voltage generating circuits 23 and 24, the negative voltage generating circuit 25, and the write/erase controlling circuit 26 that structure the peripheral circuitry are formed in the third well regions 105a, 105b, and 105c, the plurality of N-channel MOS transistors is formed in the third well regions 105a, 105b, and 105c, and the plurality of P-channel MOS transistors is formed in the fourth well regions 106a, 106b, and 106c.

[0045]

Note that the N-channel MOS transistors that serve as the select gates 6 that are formed inside the memory cell array are, as with the memory cell 1, formed in the second well region (not shown) that is formed separately from the second well regions 104a and 104b wherein memory cells 1 are formed. Moreover, electrical isolation between each of the plurality of memory cells 1, formed respectively in the second well regions 104a and 104b, is carried out through a device isolating oxide film (LOCOS) 107 that is formed surrounding each individual memory cell 1, as depicted in FIG. 3, where the electrical isolation between the plurality of MOS transistors that are formed in the third and fourth

well regions 105a, 105b, 15c, 106a, 106b, and 106c is also carried out through a device isolating oxide film (LOCOS) 107 that is formed surrounding the individual MOS transistors, as depicted in FIG. 3.

[0046]

A method for manufacturing a flash memory structured in this way, and, in particular, an example of a method for manufacturing a semiconductor substrate 100 that is applied to a flash memory, will be explained next based primarily FIG. 4 through FIG. 8. First, as illustrated in FIG. 4, a lightly-doped P-type epitaxial layer 102a with a dopant concentration of 1 x $10^{15}/cm^3$, formed with a thickness of about 5 µm, is formed through carrying out epitaxial deposition, through a typical known method, onto the surface of a first semiconductor layer 101, which comprises a heavily-doped P-type silicon substrate (silicon wafer) with a dopant concentration of 1 x $10^{19}/cm^3$, as illustrated in FIG. 4. The concentration distribution at this time, from the surface of the epitaxial layer 102a into the first semiconductor layer 101, will be as depicted by the dash-dot line A, depicted in FIG. 9.

[0047]

Thereafter, boron [B], which is a P-type dopant, is implanted into the surface of the epitaxial layer 102a at 100 keV and 1 x 10^{12} through $1\times10^{13}/cm^2$, to form an ion implantation layer 102b. Following this, a heat treatment is carried out for 10 hours at between 1130 and 1180°C in a nitrogen gas ambient to thermally diffuse the boron [B] of the ion implantation layer 102b, to produce a lightly-doped P-type second semiconductor layer 102 wherein the epitaxial layer 102a, as a whole, is between 1 x 10^{16} and 1 x $10^{18}/cm^3$, as illustrated in FIG. 5. At this time, the dopant concentration by the boron [B] will be as depicted by the solid line B shown in FIG. 9.

[0048]

As depicted in FIG. 6, the regions other than the desired region (in this example, the region where the memory cell array is formed) are next masked (not shown), phosphorus [P], which is an N-type dopant, is implanted through the mask into the desired region at 150 keV and between 1 x 10^{12} and 1 x $10^{13}/cm^2$, after which a heat treatment is carried out at between 1130 and 1180°C for five hours in a nitrogen gas ambient to thermally diffuse the phosphorus [P] to form an N-type first well region 103 with a depth of about 3 µm and a dopant concentration of between 1 x 10^{15} and 1 x $10^{18}/cm^3$. The dopant concentration due to the phosphorus [P] at this time will be as depicted by the dotted line C shown in FIG. 9.

[0049]

Thereafter, as illustrated in FIG. 7, the regions other than the desired region (the memory cell forming region corresponding to each block unit that is the multibit-erasure unit within of the memory cell array, and the region wherein the N-channel MOS transistors that structure the peripheral circuitry are formed) are masked (not shown), and boron [B], which is a P-type dopant, is implanted through the mass into the desired region at 100 keV and between 1×10^{12} and 1 x $10^{13}/cm^2$, to form boron implantation layers 104A, 104B, 105A, 105B, and 105C. Thereafter, the mask is removed, the boron implantation layers 104A, 104B, 105A, 105B, and 105C, are masked, and phosphorus [P], which is an N-type dopant, is implanted through the mass into the regions other than the boron implantation layers 104A, 104B, 105A, 105B, and 105C at 150 keV and between 1 x 10^{12} and 1 x $10^{13}/cm^2$, to form phosphorus implantation layers 106A through 106D.

[0050]

In this state, a heat treatment is carried out for several hours at between 1130 and 1180°C in a nitrogen gas ambient to thermally diffuse the boron [B] and phosphorus [P] of the boron implantation layers 104A, 104B, 105A, 105B, and 105C to form, as illustrated in FIG. 8, P-type second well regions 104a and 140b with a depth of about 1.5 µm and a dopant concentration between 1 x 10^{15} and 1 x $10^{18}/cm^3$ in the surface of the first well region 103 and P-type third well regions 106a through 106c with a depth of about 1.5 µm in the dopant concentration of between 1 x 10^{15} and 1 x $10^{18}/cm^3$, and N-type fourth well regions 106a through 106c with a depth of about 3 µm and a dopant concentration of between 1 x 10^{15} and 1 x $10^{18}/cm^3$, in the surface of the second semiconductor layer 102. The dopant concentration due to the boron [B] at this time will be as depicted by the dotted line D shown in FIG. 9.

[0051]

The semiconductor substrate 100 that is depicted in FIG. 2 is formed in this way. Note that FIG. 8 and FIG. 2 depict semiconductor substrates 100 in identical states. In the semiconductor substrate 100 that is structured in this way, the dopant profile that is appearing in the A-A' cross-section in FIG. 8 will be as depicted in FIG. 10. As can be appreciated from FIG. 10, a second well region 104a is formed up to a depth of about 1.5 µm from the surface of the second semiconductor layer 102, where the first well region 103 is interposed from the bottom surface of the second well region 104a up to a depth of about 3 µm, and the second semiconductor layer 102 is interposed from the bottom surface of the first well 103 up to the surface of the first semiconductor layer 101.

[0052]

Additionally, the dopant profile appearing in the B-B' cross-section in FIG. 8 will be as shown in FIG. 11. As can be appreciated from FIG. 11, a third well region 105a is formed up to a depth of about 1.5 µm from the surface of the second semiconductor layer 102, and the second semiconductor layer 102 is interposed from the bottom surface of the third well region 105a up to the surface of the first semiconductor layer 101. Note that, as depicted in FIG. 11, both the third well region 105a and the second semiconductor layer 102 are of the same conductivity type, that is, P-type, so there is no clear boundary between the third well region 105a and the second semiconductor layer 102, but rather the dopant concentration falls off smoothly.

[0053]

Additionally, the dopant profile appearing in the C-C' cross-section in FIG. 8 will be as shown in FIG. 12. As can be appreciated from FIG. 12, a fourth well region 106a is formed up to a depth of about 3 µm from the surface of the second semiconductor layer 102, and the second semiconductor layer 102 is interposed from the bottom surface of the fourth well region 106a up to the surface of the first semiconductor layer 101. Note that in this embodiment the first through fourth well regions are all formed through thermal diffusion, and thus the dopant profiles thereof are profiles that approximate Gaussian

distributions with the concentrations at maxima near the surface.

[0054]

Next, a normal typically known method is used to form a device isolating oxide film (LOCOS) 170 is formed surrounding each memory cell 1 in order to provide electrical isolation between the plurality of memory cells 1, and a device isolating oxide film (LOCOS) 107 is formed so as to surround each MOS transistor in order to provide electrical isolation between the plurality of MOS transistors that are formed in the respective third and fourth well regions 105a, 105b, 105c, 106a, 106b, and 106c, in the semiconductor substrate 101 that is depicted in FIG. 8.

[0055]

Thereafter, using normal typically known methods, a memory cell is formed in the regions surrounded by the device isolating oxide films in the second well regions 104a and 104b, N-channel MOS transistors are formed in the regions surrounded by the device isolating films in the third well regions 105a through 105c, and P-channel MOS transistors are formed in the regions surrounded by the device isolating films in the fourth well regions 106a through 106c. Additionally, flash memories are completed through carrying out contact formation, interconnection formation, and the like, through normal typically known methods.

[0056]

The erasing operation (which, in this case, is an operation for injecting electrons into the floating gate electrode), the writing operation (which, in this case, is an operation for extracting electrons accumulated in the floating gate electrode), and the reading operation for the flash memory structured in this way will be explained next using FIG. 1.

[ERASING OPERATION]

In the present embodiment, this is through multibit erasing by the block unit, where here the memory cells 1_{11}, 1_{12}, 1_{21}, and 1_{22} of the block 2a are multibit-erased, and the memory cells 1_{31}, 1_{32}, 1_{41}, and 1_{42} of other blocks 2b are not erased.

[0057]

When a signal for instructing multibit erasure is inputted from the outside into the write/erase controlling circuit 26, the write/erase controlling circuit 26 applies, to the row decoder 13, the source/well decoder 14, the select gate decoder 15, the column decoder 16, the writing circuit 19, the sense amp 22, the first and second high-voltage generating circuit 23 and 24, and the negative voltage generating circuit 25, a write/erase signal that indicates erasure, placing these circuits into a state for carrying out multibit erasure. On the other hand, an address signal, which in this case is the row address signal and column address signal that are inputted in time-series to indicate the selection of the block 2a, is inputted through the address input pad 18 into the address buffer circuit 17.

[0058]

The row decoder 13 that has received the write/erase signal indicating erasing, from the write/erase controlling circuit 26, and the address signal from the address buffer 17, applies, to the word lines 3_1 and 3_2 that are connected to the memory cells 1_{11}, 1_{12}, 1_{21}, and 1_{22} of the selected block 2a, the first high-voltage level (for example, 10 V) from the first high-voltage generating circuit 23, and maintains, at the ground electropotential, the electropotentials of the word lines 3_3 and 3_4 that are connected to the memory cells 1_{31}, 1_{32}, 1_{41}, and 1_{42} of the non-selected block 2b.

[0059]

Moreover, the source/well decoder 14 that has received the write/erase signal indicating erasing from the writing/controlling circuit 26 and the address signal from the address buffer 17 applies the negative electropotential (for example, -8 V) from the negative voltage generating circuit 25 to the source line 7a that is connected to the memory cells 1_{11}, 1_{12}, 1_{21}, and 1_{22} of the selected block 2a, and maintains, at the ground electropotential, the electropotential of the source line 7b that is connected to the memory cells 1_{31}, 1_{32}, 1_{41}, and 1_{42} of the non-selected block 2b, and also applies the negative electropotential (for example, -8 V) from the negative voltage generating circuit 25 to the substrate, that is, to the well electropotential line 8a that is connected to the second well region 104a that is depicted in FIG. 2, of the memory cells 1_{11}, 1_{12}, 1_{21}, and 1_{22} of the selected block 2a while maintaining, at the ground electropotential, the electropotential of the substrate, that is, of the well electropotential line 8b that is connected to the second well region 104b that is depicted in FIG. 2, for the memory cells 1_{31}, 1_{32}, 1_{41}, and 1_{42} of the non-selected block 2b.

[0060]

Additionally, the select gate decoder 15 that receives the write/erase signal that indicates erasure, from the write/erase controlling circuit 26, and the address signal from the address buffer 17, maintains the nonconductive state of select gates 6_{1a} through 6_{2b} in order to maintain the electropotentials of all of the block select signal lines 9a and 9b at the ground electropotential, and places the primary bit lines 4_1 and 4_2 and the secondary bit lines 5_{1a} through 5_{2b} into an electrically non-connected state, so that the secondary bit lines 5_{1a} through 5_{2b} will be, electrically, in a floating state.

[0061]

Additionally, the column decoder that receives the write/erase signal that indicates erasure, from the write/erase controlling circuit 26, and the address signal from the address buffer 17, maintains the nonconductive state of transfer gates 11_1 through 11_2 in order to maintain the electropotentials of all of the column select signal lines 12_1 and 12_2 at the ground electropotential, and places the input/output line 10 and the primary bit lines 4_1 and 4_2 into an electrically non-connected state, so that the primary bit lines 4_1 and 4_2 will be, electrically, in a floating state.

[0062]

Furthermore, the writing circuit 19 that receives the write/erase signal indicating erasing, from the write/erase controlling circuit 26, puts its output into a high impedance state, placing the sense amp 22 into a non-active state. Consequently, in the memory cells 1_{11}, 1_{12}, 1_{21}, and 1_{22} of the selected block 2a, the control gate electrode will be at the first high-voltage level (for example, 10 V), the source region will be at the negative electropotential (for example, -8 V), the drain region will be floating, and the substrate (the second well region 104a) will be at the negative electropotential (for example, -8 V), and thus a strong electric field will be applied across the source region and

the control gate region, and applied to the substrate surface region that is positioned between the source region and the drain region, that is, across the channel region and the control gate region, so that electrons will be injected, through a tunneling phenomenon, through the gate oxide film that is positioned over the channel region and the source region, positioned directly below the floating gate electrode, into the floating gate electrode from the channel region and the source region. The result is that electrons will accumulate in the floating gate electrode, causing the threshold voltage of the memory cell to be high, thereby erasing the memory cell.

[0063]

On the other hand, in the memory cells 1_{31}, 1_{32}, 1_{41}, and 1_{42} of the non-selected block 2b, the control gate electrode will be at the ground electropotential, the source region will be at the ground electropotential, and the drain region will be floating, and thus no strong electric field will be produced across the control gate electrode and the source region, drain region, and channel region, so electrons will not be injected into the floating gate region, nor will electrons that have accumulated in the floating gate electrode be extracted. Multibit erasure is carried out by the block unit in this way.

[0064]

[WRITING OPERATION]

Now let us assume that information is to be written (programmed) to memory cell 1_{11} of block 2a without writing information to the other memory cells 1_{12}, 1_{21}, and 1_{22} thereof, nor to memory cells 1_{31}, 1_{32}, 1_{41}, and 1_{42} of the other block 2b.

[0065]

When a signal indicating writing is inputted from the outside into the write/erase controlling circuit 26, the write/erase controlling circuit 26 applies, to the row decoder 13, the source/well decoder 14, the select gate decoder 15, the column decoder 16, the writing circuit 19, the sense amp 22, the first and second high-voltage generating circuit 23 and 24, and the negative voltage generating circuit 25, a write/erase signal that indicates writing, placing these circuits into a state for carrying out writing. On the other hand, an address signal, which in this case is the row address signal and column address signal that are inputted in time-series to indicate the selection of the memory cell 1_{11}, is inputted through the address input pad 18 into the address buffer circuit 17.

[0066]

The row decoder 13 that has received the write/erase signal indicating writing, from the write/erase controlling circuit 26 and the address signal from the address buffer 17 applies the negative electropotential (for example, -8 V), from the negative voltage generating circuit 25, to the word line 3_1 that is connected to the memory cell 1_{11} that is selected based on the row address signal, and maintains the electropotentials of all of the other word lines 3_2, 3_3, and 3_4 at the ground electropotential.

[0067]

Moreover, the source/well decoder 14 that has received the write/erase signal indicating writing, from the write/erase controlling circuit 26 and the address signal from the address buffer 17 places all of the source lines 7a and 7b into the floating state, and maintains the electropotential of the substrate of all of the memory cells, that is, of the well electropotential lines 8a and 8b that are connected to the second well regions 104a and 104b that are depicted in FIG. 2, at the ground electropotential.

[0068]

Moreover, the select gate decoder 15 that has received the write/erase signal indicating writing, from the write/erase controlling circuit 26 and the address signal from the address buffer 17 applies the second high-voltage level (for example, 6 V) from the second high-voltage generating circuit 24 to the block select signal line 9a that corresponds to the block that includes the memory cell 1_{11} that is selected based on a portion of the row address signal and a portion of the column address signal, and maintains the electropotential of the other block select signal line 9b at the ground electropotential. The result is that the select gates 6_{1a} and 6_{2a} that are connected to the block select signal line 9a will go into a conductive state, causing the primary bit lines 4_1 and 4_2 and secondary bit lines 5_{1a} and 52a to go into an electrically connected state, causing the electropotentials of the primary bit lines 4_1 and 4_2 to be relayed to the secondary bit lines 5_{1a} and 52a. Moreover, the select gates 6_{1b} and 6_{2b} that are connected to the block select signal line 9b will be maintained in the nonconductive state, causing the primary bit lines 4_1 and 4_2 and the secondary bit lines 5_{1b} and 5_{2b} to be in the electrically non-connected state, causing the secondary bit lines 5_{1b} and 5_{2b} to be in an electrically floating state.

[0069]

Furthermore, the column decoder that has received the write/erase signal indicating writing, from the write/erase controlling circuit 26 and the address signal from the address buffer 17 applies the second high-voltage level (for example, 6 V) from the second high-voltage generating circuit 24 to the column select signal line 12_1 that is connected to the transfer gate 11_1 that is connected to the primary bit line 4_1 that is arranged in the column wherein the memory cell 1_{11} that is selected based on the column address signal is located, and maintains the electropotential of the other column select signal line 12_2 at the ground electropotential. The result is that the transfer gate 11_1 that is connected to the column select signal line 12_1 goes into a conductive state, causing the input/output line 10 and the primary bit lines 4_1 and 4_2 to go into an electrically connected state, causing the electropotential of the input/output line 10 to be relayed to the primary bit line 4_1. Moreover, the transfer gate 11_2 that is connected to the column select signal line 12_2 is maintained in the nonconductive state, causing the input/output line 10 and the primary bit line 4_2 to be in an electrically non-connected states, so that the primary bit line 4_2 will be in an electrically floating state.

[0070]

Moreover, the writing circuit 19 that has received the write/erase signal indicating writing, from the write/erase controlling circuit 26, applies the second high-voltage level (for example, 6 V) from the second high-voltage generating circuit 24 to the input/output line 10 based on information inputted through the data input/output buffer 20 from the input/output pad 21. The sense amp 22 that has received has received the write/erase signal indicating writing, from

the write/erase controlling circuit 26, goes into the non-active state.

[0071]

As a result, in the selected memory cell 1_{11}, the gate control electrode will be at the negative electropotential (for example, -8 V), the source region will be floating, the drain region will be at the second high-voltage level (for example, 6 V), and the substrate (the second well region 104a) will be at the ground electropotential, and thus a strong electric field will be applied across the drain region and control gate electrode, so that the electrons accumulated in the floating gate electrode will be extracted to the drain electrode through the tunneling phenomenon through the gate oxide film that is positioned over the drain electrode, positioned directly below the floating gate electrode.

[0072]

Moreover, in a non-selected memory cell 1_{12} that is connected to a word line 3_1, the control gate electrode is put to the negative electropotential (for example, -8 V), the source region is set to floating, the drain region is set to floating, and the substrate (the second well region 104a) is set to the ground electropotential, and thus no strong electric field is produced between the control gate electrode and the source region, drain region, or channel region, so the electrons accumulated in the floating gate electrode will not be extracted, nor will electrons be injected into the floating gate electrode.

[0073]

Moreover, in a non-selected memory cells 12_1 and 12_2 that are connected to the word line 3_2, the control gate electrode is put to the ground electropotential, the source region is set to floating, the drain region is set to floating, and the substrate (the second well region 104a) is set to the ground electropotential, and thus no strong electric field is produced between the control gate electrode and the source region, drain region, or channel region, so the electrons accumulated in the floating gate electrode will not be extracted, nor will electrons be injected into the floating gate electrode.

[0074]

Moreover, in the non-selected memory cells 1_{31}, 1_{32}, 1_{41}, and 1_{42} that are connected to the word lines 3_3 and 3_4, the control gate electrode is put to the ground electropotential, the source region is set to floating, the drain region is set to floating, and the substrate (the second well region 104a) is set to the ground electropotential, and thus no strong electric field is produced between the control gate electrode and the source region, drain region, or channel region, so the electrons accumulated in the floating gate electrode will not be extracted, nor will electrons be injected into the floating gate electrode. In this way, the electrons accumulated in the floating gate electrode can be extracted to the drain electrode side, to carry out writing, for only the single memory cell 1_{11} that is selected based on the row address signal and the column address signal that have been inputted from the outside.

[0075]

[READING OPERATION]

Here let us assume that information stored in the memory cell 1_{11} of the block 2a is to be read out, without reading out information stored in the other memory cells 1_{12}, 1_{21}, and 1_{22} thereof, and in memory cells 1_{31}, 1_{32}, 1_{41}, and 1_{42} of the other memory block 2b.

[0076]

When a signal indicating reading is inputted from the outside into the write/erase controlling circuit 26, the write/erase controlling circuit 26 applies, to the row decoder 13, the source/well decoder 14, the select gate decoder 15, the column decoder 16, the writing circuit 19, the sense amp 22, the first and second high-voltage generating circuit 23 and 24, and the negative voltage generating circuit 25, a write/erase signal that indicates reading, placing these circuits into a state for carrying out reading. On the other hand, an address signal, which in this case is the row address signal and column address signal that are inputted in time-series to indicate the selection of the memory cell 1_{11}, is inputted through the address input pad 18 into the address buffer circuit 17.

[0077]

The row decoder 13 that has received the write/erase signal indicating reading, from the write/erase controlling circuit 26 and the address signal from the address buffer 17 applies the power supply electropotential (for example, 3.3V) to the word line 3_1 that is connected to the memory cell 1_{11} that is selected based on the row address signal, and maintains the electropotentials of all of the other word lines 3_2, 3_3, and 3_4 at the ground electropotential.

[0078]

Moreover, the source/well decoder 14 that has received the write/erase signal indicating reading, from the write/erase controlling circuit 26 and the address signal from the address buffer 17 maintains the electropotential of all of the source lines 7a and 7b and of the substrate of all of the memory cells, that is, of the well electropotential lines 8a and 8b that are connected to the second well regions 104a and 104b that are depicted in FIG. 2, at the ground electropotential.

[0079]

Moreover, the select gate decoder 15 that has received the write/erase signal indicating reading, from the write/erase controlling circuit 26 and the address signal from the address buffer 17 applies the power supply electropotential (for example, 3.3V) to the block select signal line 9a that corresponds to the block that includes the memory cell 1_{11} that is selected based on a portion of the row address signal and a portion of the column address signal, and maintains the electropotential of the other block select signal line 9b at the ground electropotential. The result is that the select gates 6_{1a} and 6_{2a} that are connected to the block select signal line 9a go into a conductive state, so the primary bit lines 4_1 and 4_2 and secondary bit lines 5_{1a} and 52a go into an electrically connected state. Moreover, the select gates 6_{1b} and 6_{2b} that are connected to the block select signal line 9b will be maintained in the nonconductive state, causing the primary bit lines 4_1 and 4_2 and the secondary bit lines 5_{1b} and 5_{2b} to be in the electrically non-connected state, causing the secondary bit lines 5_{1b} and 5_{2b} to be in an electrically floating state.

[0080]

Furthermore, the column decoder that has received the write/erase signal indicating reading, from the write/erase controlling circuit 26 and the address signal from the address buffer 17 applies the power supply electropotential

to the column select signal line 12_1 that is connected to the transfer gate 11_1 that is connected to the primary bit line 4_1 that is arranged in the column wherein the memory cell 1_{11} that is selected based on the column address signal is located, and maintains the electropotential of the other column select signal line 12_2 at the ground electropotential. The result is that the transfer gate 11_1 that is connected to the column select signal line 12_1 goes into a conductive state, so the input/output line 10 and the primary bit lines 4_1 and 4_2 go into an electrically connected state. Moreover, the transfer gate 11_2 that is connected to the column select signal line 12_2 is maintained in the nonconductive state, causing the input/output line 10 and the primary bit line 4_2 to be in an electrically non-connected states, so that the primary bit line 4_2 will be in an electrically floating state.

[0081]

Additionally, the writing circuit 19 that has received, from the write/erase controlling circuit 26, a write/erase signal that indicates reading out places the output thereof in a high impedance state, so has no effect whatsoever on the input/output line 10. The sense amp 22 that has received, from the write/erase controlling circuit 26, a write/erase signal that indicates reading goes into the active state, to apply a low-level voltage (for example, 1.2 V) to the input/output line 10, and detects whether or not a current is flowing in the input/output line 10, and amplifies the detected information to output it as read information to the input/output pad through the data input/output buffer 20.

[0082]

Consequently, when information has been written to the memory cell 1_{11}, that is, when the electrons that had been accumulated in the floating gate electrode have been extracted, the threshold voltage for the memory cell 1_{11} will be low, so the memory cell 1_{11} will go into a conductive state through application of the power supply voltage to the word line 3_1. Because of this, when a low-level voltage is applied to the input/output line 10 from the sense amp 22, a current will flow on the source line 7a through the transfer gate 11_1, the primary bit line 4_1, the select gate 6_{1a}, the secondary bit line 5_{1a}, and the memory cell 1_{11}, to be detected by the sense amp 22 and outputted as read information "1" to the data input/output buffer 20.

[0083]

On the other hand, if no information has been written to the selected memory cell 1_{11}, that is, if electrons are accumulated in the floating gate electrode, the threshold voltage of the memory cell 1_{11} will be high, so that even if the power supply voltage is applied to the word line 3_1, the memory cell 1_{11} will remain in the nonconductive state. Because of this, even if a low voltage level is applied to the input/output line 10 from the sense amp 22, no path will be produced that will cause an electric current to flow in the source line 7a, so no current will flow, and the sense amp 22 will detected this, and read information "0" will be outputted to the data input/output buffer 20.

[0084]

At this time, the other word lines 3_2 through 3_4 to which the selected memory cell 1_{11} is not connected will all be at the ground electropotential, and thus the memory cells 12_1 through 1_{42} that are connected to these word lines 3_2 through 3_4 will remain in the nonconductive state, regardless of the information stored therein, and thus no path for an electric current to flow will be produced through these memory cells 1_{21} through 1_{42}. Moreover, the other memory cell 1_{12} that is connected to the word line 3_1 to which the selected memory cell 1_{11} is connected will go into a conductive state or a nonconductive state depending on the information stored therein, but the primary bit line 4_2 to which these memory cells 1_{12} are connected will be placed by the transfer gate 11_2 into a state that is not electrically connected to the input/output line 10, and thus no path for an electric current to flow will be produced through these memory cells 11_2. In this way, it is possible to read out the information that is stored in the memory cell 1_{11} through the ability of the sense amp 22 to detect whether or not an electric current is flowing, based on the stored information, for only the single memory cell 1_{11} that is selected based on the row address signal and the column address signal is that are inputted from the outside.

[0085]

A flash memory that is structured as described above has advantages such as the following. Firstly, multibit erasure is carried out for the memory cells 1 by the block unit. Secondly a negative electropotential that has an absolute value that is higher than that of the power supply voltage (for example, -8 V) is applied to the source regions and the second well regions 104 of the memory cells 1 at the time of multibit erasure by the block unit, and a second high voltage level that is higher than the power supply voltage (for example, 6 V) is applied to the drain region of the memory cell when writing, so that even though inherently there is a tendency for latch-up by transistors of a parasitic thyrister structure, there is a lightly-doped second semiconductor layer 102, formed through epitaxial deposition, that is interposed between the first well region 103 and the heavily-doped first semiconductor layer 101, greatly reducing the resistance of the second semiconductor layer 102, improving the ability to resist latch-up.

[0086]

Thirdly, because a gate insulating film made from a tunnel oxide film of the memory cell 1, for which electrons are injected and extracted, is formed on the surface on the top of the second well region 104 that is formed in the surface of the second semiconductor layer 102 that is formed through epitaxial deposition, the impurities (for example, oxygen concentration) and defect density on the surface of the second well region 104 can be controlled easily, making it possible to produce that wherein the impurities and defect density are low, making it possible to form a high-quality gate insulating film, thereby making it possible to produce a memory cell that has a long service life that can be rewritten a high number of times. Fourthly, the breakdown voltage in relation to the second semiconductor layer 102 of the first well region 103 can be set to be high, and the punch-through breakdown voltage between the second well region 104 and the second semiconductor layer 102 can also be improved, through interposing the lightly-doped second semiconductor layer 102, formed through epitaxial deposition, between the first well region 103 and the heavily-doped first semiconductor layer 101.

[0087]

Note that while, in the first embodiment, set forth above, a structure is depicted wherein the first well region 103, the

third well region 105, and the fourth well region 106 are in contact with each other, the structure may instead be one wherein the first well region 103, third well region 105, and fourth well region 106 are separated from each other, that is, wherein the second semiconductor layer 102 is interposed between the well regions, as depicted in FIG. 13, or may be a structure wherein the first well region 103, the third well region 105, and the fourth well region 106 are mutually overlapping, as depicted in FIG. 14.

[0088]

EMBODIMENT 2

A second embodiment of the present invention is depicted in FIG. 15, where the only point of difference is that, in contrast to a plurality of second well regions 104a and 104b is provided in the first well region 103 in the first embodiment, set forth above, first well regions 103a and 103b are provided for second well regions 104a and 104b, respectively, that is, that first and second well regions 103 and 104 are provided corresponding to the individual block units for each block unit into which the plurality of memory cells is divided, where the other points are the same as indicated in the first embodiment. The same effects as in the first embodiment are achieved in this structure as well.

[0089]

EMBODIMENT 3

A third embodiment of the present invention is depicted in FIG. 16 and FIG. 17, where the distinctive feature is that the first high-voltage generating circuit 23 and/or second high-voltage generating circuit 24 in the first embodiment, set forth above, is structured as depicted in FIG. 16 and FIG. 17, where the other points are the same as shown in the first embodiment. FIG. 16 depicts a circuit diagram of a high-voltage generating circuit, where D1 through Dn are diode devices connected in series between a power supply voltage node Vcc to which the power supply voltage (for example, 3.3 W) is applied, and the output node OUT, structured from NPN bipolar transistors of diode connections, where base electrodes and collector electrodes are connected as depicted in (b). C1 through Cn are capacitive devices that have one electrode connected to the respectively corresponding cathodes of the diode devices D1 through Dn, where the other electrodes of the capacitive devices at odd-numbered positions receive clock signals φ that repetitively alternate between the power supply voltage and the ground potential, and the other electrodes of the capacitive devices at even-numbered positions receive clock signals /φ that repetitively alternate between the power supply voltage and the ground electropotential in a relationship that is exactly inverted from the clock signals φ.

[0090]

When the high-voltage generating circuit that is structured in this way is built into the semiconductor substrate 100 according to the first embodiment, set forth above, it will be as depicted in FIG. 17. In FIG. 17, 103_1 through 103_n are N-type first well regions that are formed in the surface of the second semiconductor layer 102, where the second semiconductor layer 102 is interposed between the first well regions and the surface of the first semiconductor layer 101, formed isolated from, and simultaneously with, the first well region 103 for forming the memory cell 1, to serve as the collector regions of NPN bipolar transistors that are diode-connected, where, as with the first well regions 103, the depth is, for example, between 1 and about 9 μm, with a dopant concentration between 1×10^{15} and $1 \times 10^{18}/cm^3$.

[0091]

104_1 through 104_n and are P-type second well regions formed in the respective surfaces of these first well regions 103_1 through 103_n, formed simultaneously with the second well regions 104a and 104b wherein the memory cells 1 are formed, and serve as base regions for the NPN bipolar transistors that are diode-connected, where, as with the second well regions 104a and 104b, the depth is, for example, between 0.5 at about 8.5 μm, and the dopant concentration is between 1×10^{15} and $1 \times 10^{18}/cm^3$. 1071 through 107n are emitter regions for the NPN bipolar transistors that are diode-connected, made from N-type diffusion regions that are formed in the respective surfaces of these second well regions 104_1 through 104_n, and are formed simultaneously with, for example, the source regions and drain regions for the memory cells 1 and the source regions and drain regions for the N-channel MOS transistors of the peripheral circuitry.

[0092]

108_1 through 108_n are diffusion regions for the N-type collector electrodes that are more heavily doped than the dopant concentrations of the first well regions 103_1 through 103_n, and are formed in the respective surfaces of the first well regions 103_1 through 103_n, where 109_1 through 109_n are diffusion regions for the P-type base electrodes that are more heavily doped than the dopant concentrations of the second well regions 104_1 through 104_n, and are formed in the respective surfaces of the second well regions 104_1 through 104_n.

[0093]

In a high-voltage generating circuit that is structured in this way, the closer to the output node, the higher the electropotentials of the anode and cathodes of the diode devices will be. That is, the electropotential of the first well region 103, depicted in FIG. 17, will also be high. The result is that, despite the need to increase the junction breakdown voltage between the first well region 103 and the second semiconductor layer 102, a junction breakdown voltage that is adequate for the need is produced, in this third embodiment, because the second semiconductor layer 102 is a lightly-doped semiconductor layer formed through epitaxial deposition.

[0094]

EMBODIMENT 4

FIG. 18 through FIG. 20 depict a fourth embodiment of the present invention, where only the method for forming the first well region 103 differs from the first embodiment, set forth above, with the other points being the same as in the first embodiment. In order to explain in general the point of difference from the first embodiment, set forth above, the method for manufacturing the semiconductor substrate will be described below.

[0095]

First, as with the first embodiment, set forth above, a lightly-doped P-type epitaxial layer 102a is formed on the surface of the first semiconductor layer 101 (where the concentration distribution within the first semiconductor layer 101 from the surface of the epitaxial layer 102a at this

time will be the same as that in the first embodiment, depicted by the dash-dot line A in FIG. 21), followed by implantation of boron [B], which is a P-type dopant, into the surface of the epitaxial layer 102a, and carrying out a heat treatment within a nitrogen gas ambient to thermally defuse the boron [B], to cause the epitaxial layer 102a to become the lightly-doped P-type second semiconductor layer 102, as depicted in FIG. 4 and FIG. 5. The dopant concentration by the boron [B] at this time will be as depicted by the solid line B in FIG. 21, the same as in the first embodiment.

[0096]

Next, as illustrated in FIG. 7, the regions other than the desired region (which, in this example, is the region wherein the memory cell array will be formed and the region wherein the P-channel MOS transistors of the peripheral circuitry will be formed) are masked (not shown), and phosphorus [P], which is an N-type dopant, is implanted through the mask into the desired region at between 1 and 5 MeV and 1 x 10^{12} through 1 x $10^{14}/cm^2$, so that the peak will be positioned at a prescribed depth, to form the bottom portion region 103A of the first well region 103 and also to form the bottom portion regions $106A_0$ through $106C_0$ of the fourth well regions 106a through 106c. At this time the dopant concentration at the bottom portion region 103A and the bottom portion regions $106A_0$ through $106C_0$ will be formed so as to have a peak dopant concentration (1 x 10^{15} through 1 x $10^{18}/cm^3$) at a position with a depth of 2 µm from the surface of the second semiconductor layer 102, as depicted by the dotted line C1 in FIG. 20. Note that ion implantation is carried out also for forming the regions wherein the P-channel MOS transistors of the peripheral circuitry will be formed, that is, for forming the fourth well regions, but it need not necessarily be ion implantation, in particular, that is performed into these regions.

[0097]

Thereafter, as with the first embodiment, set forth above (depicted in FIG. 19), the regions other than the desired region (the memory cell forming regions corresponding to each block unit that are the multibit erasure units within the memory cell array, and the regions wherein the N-channel MOS transistors for structuring the peripheral circuitry are to be formed) are masked (not shown), and, through this mask, boron [B], which is a P-type dopant, is implanted into the desired regions to form boron implantation layers 104A, 104B, 105A, 105B, and 105C. Thereafter, the mask is removed and the boron implantation layers 104A, 104B, 105A, 105B, and 105C are masked, and, through this mask, phosphorus [P], which is an N-type dopant, is implanted to form phosphorus implantation layers 106A through 106D in regions other than the boron implantation layers 104A, 104B, 105A, 105B, and 105C.

[0098]

In this state a heat treatment is carried out to cause thermal diffusion of the boron [B] and phosphorus [P], to cause formation of the first well region 103 through the bottom portion region 103A and the phosphorus implantation layer 106D, the formation of these P-type second well regions 104a and 104b in surfaces of these first well regions 103, the formation of P-type third well regions 105a through 105c in surfaces of the second semiconductor layer 102, and the formation of N-type fourth well regions 106a through 106c, through the bottom portion regions $106A_0$ through $106C_0$ and the phosphorus implantation layers 106A through 106C in surfaces of the second semiconductor layer 102, as depicted in FIG. 20. The dopant concentration by the boron [B] at this time will be the same as in the first embodiment, depicted by the dotted line D in FIG. 21.

[0099]

The semiconductor substrate 100 is formed in this way. In the semiconductor substrate 100 that is structured in this way, the dopant profile that is appearing in the A-A' cross-section in FIG. 20 will be as depicted in FIG. 21. As can be appreciated from FIG. 22, the second well region 104a is formed from the surface of the second semiconductor layer 102 to a depth of about 1.5 µm, a first well region 103, having a dopant concentration peak positioned at a depth of about 2 µm, is interposed at a depth of about 2.5 µm from the bottom surface of the second well region 104a, and a second semiconductor layer 102 is interposed from the bottom surface of the first well region 103 to the surface of the first semiconductor layer 101.

[0100]

Moreover, the dopant profile appearing in the B-B' cross-section in FIG. 20 will be the same as in the first embodiment, set forth above, and is depicted in FIG. 23. As can be appreciated from FIG. 23, a third well region 105a is formed up to a depth of about 1.5 µm from the surface of the second semiconductor layer 102, and the second semiconductor layer 102 is interposed from the bottom surface of the third well region 105a up to the surface of the first semiconductor layer 101. Note that, as depicted in FIG. 23, both the third well region 105a and the second semiconductor layer 102 are of the same conductivity type, that is, P-type, so there is no clear boundary between the third well region 105a and the second semiconductor layer 102, but rather the dopant concentration falls off smoothly.

[0101]

Additionally, the dopant profile appearing in the C-C' cross-section in FIG. 20 will be as shown in FIG. 24. As can be appreciated from FIG. 24, a fourth well region 106a is formed up to a depth of about 2.5 µm from the surface of the second semiconductor layer 102 and has a peak dopant concentration at a position with a depth of about 2 µm, and the second semiconductor layer 102 is interposed from the bottom surface of the fourth well region 106a up to the surface of the first semiconductor layer 101.

[0102]

Along with the fourth embodiment, formed in this way, having the same effects as with the first embodiment, there is also the benefit of being able to select freely the central depth of the bottom portion region of the first well region 103, and the thickness thereof in the depth direction, through the use of an ion implantation method such that will have a dopant concentration peak at a prescribed depth when forming the first well region 103 (and the fourth well regions 106a through 106c).

[0103]

EMBODIMENT 5

FIG. 25 and FIG. 26 depict a fifth embodiment of the present invention, where only the method for forming the second semiconductor layer 102 differs from the first

embodiment, set forth above, and the other points are the same as with the first embodiment. In order to explain in general the point of difference from the first embodiment, set forth above, the method for manufacturing the semiconductor substrate will be described below.

[0104]

First, as illustrated in FIG. 25, a lightly-doped P-type epitaxial layer 102a with a dopant concentration of 1 x $10^{15}/cm^3$, formed with a thickness of about 5 µm, is formed through carrying out epitaxial deposition, through a typical known method, onto the surface of a first semiconductor layer 101, which comprises a heavily-doped P-type silicon substrate (silicon wafer) with a dopant concentration of 1 x $10^{19}/cm^3$, as illustrated in FIG. 4. The concentration distribution from the surface of the epitaxial layer 102a into the first semiconductor layer 101 at this time will be the same as in the first embodiment, set forth above, and is indicated by the dash-dot line A in FIG. 27.

[0105]

Thereafter, boron [B], a P-type dopant, is implanted at between 1.5 and 5 MeV, at 1 x 10^{12} through 1 x $10^{14}/cm^2$, so that the peak of the dopant concentration will be positioned at a position that is a prescribed depth from the surface of the epitaxial layer 102a, to form an ion implantation layer 102c that is positioned at a prescribed depth. At this time, the dopant concentration by the boron [B] will be as depicted by the solid line B1 shown in FIG. 27.

[0106]

Formation is next in the same manner as in the first embodiment, set forth above. Specifically, as depicted in FIG. 6, the regions other than the desired region (which, in this example, is the region for forming a memory cell array) are masked (not shown), phosphorus [P], which is an N-type dopant, is implanted through the mask into the desired region, after which a heat treatment is carried out to cause thermal diffusion of the phosphorus [P], to form an N-type first well region 103. The dopant concentration of the phosphorus [P] at this time will be the same as in the first embodiment, set forth above, as depicted by the dotted line C in FIG. 27, where the first well region 103 will be positioned shallower than the peak of the dopant concentration that is at the prescribed position in the second semiconductor layer 102.

[0107]

Thereafter, as illustrated in FIG. 7, the regions other than the desired region (the memory cell forming region corresponding to each block unit that is the multibit-erasure unit within of the memory cell array, and the region wherein the N-channel MOS transistors that structure the peripheral circuitry are formed) are masked (not shown), and boron [B], which is a P-type dopant, is implanted through the mass into the desired region to form boron implantation layers 104A, 104B, 105A, 105B, and 105C. Thereafter, the mask is removed and the boron implantation layers 104A, 104B, 105A, 105B, and 105C are masked, and, through this mask, phosphorus [P], which is an N-type dopant, is implanted into regions other than the boron implantation layers 104A, 104B, 105A, 105B, and 105C, to form phosphorus implantation layers 106A through 106D .

[0108]

In this state, a heat treatment is carried out in a nitrogen gas ambient to cause thermal diffusion of the boron [B] and phosphorus [P], so as to form the P-type second well regions 104a and 104b in the surface of the first well region 103, and the P-type third well regions 105a through 105c and N-type fourth well regions 106a through 106c in the surface of the second semiconductor layer 102, as depicted in FIG. 26. The dopant concentration by the boron [B] at this time will be the same as in the first embodiment, , described above, depicted by the dotted line D in FIG. 27.

[0109]

In the semiconductor substrate 100 that is structured in this way, the dopant profile that is appearing in the A-A' cross-section in FIG. 26 will be as depicted in FIG. 28. As can be appreciated from FIG. 28, a second well region 104a is formed up to a depth of about 1.5 µm from the surface of the second semiconductor layer 102, where the first well region 103 is interposed from the bottom surface of the second well region 104a up to a depth of about 3.5 µm, and the second semiconductor layer 102 is interposed from the bottom surface of the first well 103 up to the surface of the first semiconductor layer 101. Moreover, the peak of the dopant concentration in the second semiconductor layer 102 will be positioned between the bottom of the first well 103 and the surface of the first semiconductor layer 101.

[0110]

Additionally, the dopant profile appearing in the B-B' cross-section in FIG. 26 will be as shown in FIG. 29. As can be appreciated from FIG. 29, a third well region 105a is formed up to a depth of about 3 µm from the surface of the second semiconductor layer 102, and the second semiconductor layer 102 is interposed from the bottom surface of the third well region 105a up to the surface of the first semiconductor layer 101. Moreover, the peak of the dopant concentration in the second semiconductor layer 102 will be positioned between the bottom of the third well 105a and the surface of the first semiconductor layer 101.

[0111]

Additionally, the dopant profile appearing in the C-C' cross-section in FIG. 26 will be as shown in FIG. 30. As can be appreciated from FIG. 30, a fourth well region 106a is formed up to a depth of about 3.5 µm from the surface of the second semiconductor layer 102, and the second semiconductor layer 102 is interposed from the bottom surface of the fourth well region 106a up to the surface of the first semiconductor layer 101. Moreover, the peak of the dopant concentration in the second semiconductor layer 102 will be positioned between the bottom of the fourth well 106a and the surface of the first semiconductor layer 101.

[0112]

In this fifth embodiment as well, formed in this way, when forming the second semiconductor layer 102 an ion implantation method is used that has a dopant concentration peak at a prescribed depth, that is, between the first semiconductor layer 101 and the first, third, and fourth well regions 103, 105, and 106, and thus, in addition to the same effects as in the first embodiment, there is the benefit of being able to select freely the central depths in these parts, and the thicknesses thereof in the depth direction.

[0113]

Note that in this fifth embodiment, the formation of the first well region 103 may instead be through ion implantation of the dopant so that the peak of the dopant concentration will be positioned at a position of a prescribed depth, as depicted in the fourth embodiment, set forth above.

[0114]

EMBODIMENT 6

FIG. 31 through FIG. 34 depict a sixth embodiment of the present invention, different from the embodiments set forth above only in the method for forming the second semiconductor layer 102, that is, in the use of the epitaxial layer, which has been deposited epitaxially, as-is, as the second semiconductor layer 102, where the other points are identical to those in the first embodiment, described above. Consequently, in order to explain in general the point of difference from the first embodiment, set forth above, the method for manufacturing the semiconductor substrate will be described below.

[0115]

First, as illustrated in FIG. 31, a second semiconductor layer 102, made from a lightly-doped P-type epitaxial layer with a dopant concentration of 1 x $10^{15}/cm^3$, formed with a thickness of about 5 μm, is formed through carrying out epitaxial deposition, through a typical known method, onto the surface of a first semiconductor layer 101, which comprises a heavily-doped P-type silicon substrate (silicon wafer) with a dopant concentration of 1 x $10^{19}/cm^3$, as illustrated in FIG. 4. The concentration distribution at this time from the surface of the second semiconductor layer 102 to the first semiconductor layer 101 will be as depicted by the dash-dot line A shown in FIG. 35.

[0116]

Thereafter, as depicted in FIG. 32, the regions other than the desired region (in this example, the region where the memory cell array is formed) are masked (not shown), phosphorus [P], which is an N-type dopant, is implanted through the mask into the surface layer of the desired region at 150 keV and between 1 x 10^{12} and 1 x $10^{13}/cm^2$, after which a heat treatment is carried out at between 1130 and 1180°C for five hours in a nitrogen gas ambient to thermally diffuse the phosphorus [P] to form an N-type first well region 103 with a depth of about 3.5 μm and a dopant concentration of between 1 x 10^{15} and 1 x $10^{18}/cm^3$. The dopant concentration due to the phosphorus [P] at this time will be as depicted by the dotted line C2 shown in FIG. 35.

[0117]

Given this, the conditions for forming the first well region 103 at this time are determined to be such as the following. Specifically, the dopant diffusion in the LSI process simply follows the Fick's diffusion equation, which, when solved in one dimension for diffusion from a constant-quantity diffusion source becomes as Equation (1), below, where the distribution of the dopant concentration will be the Gaussian distribution indicated by Equation (1), below:

$$C(x,t) = (Q/\sqrt{\pi Dt}) \times \exp(-x2/4Dt) \quad \ldots (1)$$

Here Q is the total quantity of dopant atoms of the dopant implanted in the surface layer of the second semiconductor layer 102; D is the diffusion coefficient; x is the distance (depth) from the surface of the second semiconductor layer 102; and t is the diffusion time. Moreover, $2\sqrt{Dt}$ typically is called the diffusion distance, which corresponds to 1 σ of the Gaussian distribution.

[0118]

On the other hand, when one considers the dopant concentration required as the first well region 103, and the junction breakdown voltage at the PN junction interface in the bottom portion of the first well region 103, it is understood that the difference between the peak concentration of the dopant in the first well region 103 and the concentration of the second semiconductor layer 102 must be about two orders of magnitude. Consequently, in order to interpose the second semiconductor layer 102 between the bottom surface of the first well region 103 and the surface of the first semiconductor layer 101, that is, in order to cause at least a little of the second semiconductor layer 102 to remain, the depth that will be two orders of magnitude below the peak concentration of the first well region 103 (the position of the surface of the second semiconductor layer 102 in this sixth embodiment) must be less than the thickness of the second semiconductor layer 102.

[0119]

That is, because, in a Gaussian distribution, the concentration will be two orders of magnitude from the peak concentration when separated by 2σ from the location of the peak concentration, the 2σ must be less than the thickness of the second semiconductor layer 102. If 2σ were equal to the thickness of the second semiconductor layer 102, or greater than that, the bottom surface of the first well region 103 would contact, or overlap, the surface of the first semiconductor layer 101. The result is that it is possible to interpose the second semiconductor layer 102 between the bottom surface of the first well region 103 and the surface of the first semiconductor layer 101 by satisfying $4\sqrt{Dt}$ (= 2σ) < thickness of the second semiconductor layer 102. The first well region 103 is formed while satisfying such a condition.

[0120]

Thereafter, as illustrated in FIG. 33, the regions other than the desired region (the memory cell forming region corresponding to each block unit that is the multibit-erasure unit within of the memory cell array, and the region wherein the N-channel MOS transistors that structure the peripheral circuitry are formed) are masked (not shown), and boron [B], which is a P-type dopant, is implanted through the mass into the desired region at 100 keV and between 1×10^{12} and 1 x $10^{13}/cm^2$, to form boron implantation layers 104A, 104B, 105A, 105B, and 105C. Thereafter, the mask is removed, the boron implantation layers 104A, 104B, 105A, 105B, and 105C, are masked, and phosphorus [P], which is an N-type dopant, is implanted through the mass into the regions other than the boron implantation layers 104A, 104B, 105A, 105B, and 105C at 150 keV and between 1 x 10^{12} and 1 x $10^{13}/cm^2$, to form phosphorus implantation layers 106A through 106D.

[0121]

In this state, a heat treatment is carried out for several hours at between 1130 and 1180°C in a nitrogen gas ambient to thermally diffuse the boron [B] and phosphorus [P] of the boron implantation layers 104A, 104B, 105A,

105B, and 105C to form, as illustrated in FIG. 34, P-type second well regions 104a and 140b with a depth of about 1 µm and a dopant concentration between 1 x 10^{15} and 1 x $10^{18}/cm^3$ in the surface of the first well region 103 and P-type third well regions 106a through 106c with a depth of about 2 µm in the dopant concentration of between 1 x 10^{15} and 1 x $10^{18}/cm^3$, and N-type fourth well regions 106a through 106c with a depth of about 3 µm and a dopant concentration of between 1 x 10^{15} and 1 x $10^{18}/cm^3$, in the surface of the second semiconductor layer 102. The dopant concentration due to the boron [B] at this time will be as depicted by the dotted line D shown in FIG. 35.

[0122]

In the semiconductor substrate 100 that is structured in this way, the dopant profile that is appearing in the A-A' cross-section in FIG. 34 will be as depicted in FIG. 36. As can be appreciated from FIG. 36, a second well region 104a is formed up to a depth of about 1 µm from the surface of the second semiconductor layer 102, where the first well region 103 is interposed from the bottom surface of the second well region 104a up to a depth of about 3.5 µm, and the second semiconductor layer 102 is interposed from the bottom surface of the first well 103 up to the surface of the first semiconductor layer 101. That is, the dopants implanted through ion implantation into the surface layer of the second semiconductor layer 102 are diffused based on diffusion conditions that satisfy 4 $\sqrt{Dt}$ (= 2σ) < thickness of the second semiconductor layer 102, reliably causing the lightly-doped second semiconductor layer 102 to be interposed between the bottom surface of the first well region 103 and the surface of the heavily-doped first semiconductor layer 101.

[0123]

Additionally, the dopant profile appearing in the B-B' cross-section in FIG. 34 will be as shown in FIG. 37. As can be appreciated from FIG. 37, a third well region 105a is formed up to a depth of about 2 µm from the surface of the second semiconductor layer 102, and the second semiconductor layer 102 is interposed from the bottom surface of the third well region 105a up to the surface of the first semiconductor layer 101.

[0124]

Additionally, the dopant profile appearing in the C-C' cross-section in FIG. 34 will be as shown in FIG. 38. As can be appreciated from FIG. 38, a fourth well region 106a is formed up to a depth of about 3.5 µm from the surface of the second semiconductor layer 102, and the second semiconductor layer 102 is interposed from the bottom surface of the fourth well region 106a up to the surface of the first semiconductor layer 101. Even in the sixth embodiment, formed in this way, there are the same effects as in the first embodiment.

[0125]

EMBODIMENT 7

FIG. 39 through FIG. 42 depict a seventh embodiment of the present invention, different from the embodiments set forth above only in the method for forming the second semiconductor layer 102 and the method for forming the first well region 103, that is, in the use of the epitaxial layer, which has been deposited epitaxially, as-is, as the second semiconductor layer 102 and the formation of the first well region 103 through ion implantation of dopants to a prescribed depth, where the other points are identical to those in the first embodiment, described above. Consequently, in order to explain in general the point of difference from the first embodiment, set forth above, the method for manufacturing the semiconductor substrate will be described below.

[0126]

First, as illustrated in FIG. 39, a second semiconductor layer 102, made from a lightly-doped P-type epitaxial layer with a dopant concentration of 1 x $10^{15}/cm^3$, formed with a thickness of about 3 µm, is formed through carrying out epitaxial deposition, through a typical known method, onto the surface of a first semiconductor layer 101, which comprises a heavily-doped P-type silicon substrate (silicon wafer) with a dopant concentration of 1 x $10^{19}/cm^3$, as illustrated in FIG. 4. The concentration distribution at this time from the surface of the second semiconductor layer 102 to the first semiconductor layer 101 will be as depicted by the dash-dot line A shown in FIG. 43.

[0127]

Next, as illustrated in FIG. 40, the regions other than the desired region (which, in this example, is the region wherein the memory cell array will be formed) are masked (not shown), and phosphorus [P], which is an N-type dopant, is implanted through the mask into the desired region at between 1.75 MeV and 1 x $10^{13}/cm^2$, so that the peak will be positioned at a prescribed depth, to form the bottom portion region 103A of the first well region 103 and also to form the bottom portion regions $106A_0$ through $106C_0$ of the fourth well regions 106a through 106c. At this time the dopant concentration at the bottom portion region 103A and the bottom portion regions $106A_0$ through $106C_0$ will be formed so as to have a peak dopant concentration (1 x 10^{15} through 1 x $10^{18}/cm^3$) at a position with a depth of 1.7 µm from the surface of the second semiconductor layer 102, as depicted by the dotted line C3 in FIG. 43. Note that ion implantation is carried out also for forming the regions wherein the P-channel MOS transistors of the peripheral circuitry will be formed, that is, for forming the fourth well regions 106a through 106c, but it need not necessarily be ion implantation, in particular, that is performed into these regions.

[0128]

Given this, the conditions for forming the bottom portion region 103A of the first well region 103 at this time are determined to be such as the following. Specifically, LSS theory is used for the typical solution for implanted ions in ion implantation of dopants in LSI processing. The projected range Rp, and variance ΔRp thereof, in LSS theory is tabulated in "Projected Range Statistics in Semiconductors" (by J. F. Gibbons, et al.), where the implantation distribution N(x) can be approximated easily as having a Gaussian distribution with the mean Rp and variance ΔRp, producing Equation (2), below, where the distribution of the dopant concentration will be the Gaussian distribution indicated by Equation (2), below:

$$N(x) = (NI/\sqrt{(2\pi\Delta Rp)}) \times \exp(-(x-Rp)2/2\Delta Rp2) \ldots\ldots (2)$$

Here NI is the per-unit-area quantity of ions implanted, and x is the distance (depth) from the surface of the second semiconductor layer 102.

[0129]

On the other hand, when one considers the dopant concentration required as the first well region 103, and the junction breakdown voltage at the PN junction interface in the bottom portion of the first well region 103, it is understood that the difference between the peak concentration of the dopant in the first well region 103 and the concentration of the second semiconductor layer 102 must be about two orders of magnitude. Consequently, in order to interpose the second semiconductor layer 102 between the bottom surface of the first well region 103 and the surface of the first semiconductor layer 101, that is, in order to cause at least a little of the second semiconductor layer 102 to remain, the depth that will be two orders of magnitude below the peak concentration of the first well region 103 (a position in the interior of the second semiconductor layer 102, for example, a depth of 1.7 μm, in this seventh embodiment) must be less than the thickness of the second semiconductor layer 102.

[0130]

That is, (Rp +3ΔRp) must be less than the thickness of the second semiconductor layer 102. If (Rp +3ΔRp) were equal to the thickness of the second semiconductor layer 102, or greater than that, the bottom surface of the first well region 103 would contact, or overlap, the surface of the first semiconductor layer 101. The result is that it is possible to interpose the second semiconductor layer 102 between the bottom surface of the first well region 103 and the surface of the first semiconductor layer 101 by satisfying (Rp +3ΔRp) < thickness of the second semiconductor layer 102. The first well region 103 is formed while satisfying such a condition.

[0131]

Thereafter, as illustrated in FIG. 41, the regions other than the desired region (the memory cell forming region corresponding to each block unit that is the multibit-erasure unit within of the memory cell array, and the region wherein the N-channel MOS transistors that structure the peripheral circuitry are formed) are masked (not shown), and boron [B], which is a P-type dopant, is implanted through the mass into the desired region at 100 keV and between 1×10^{12} and $1 \times 10^{13}/cm^2$, to form boron implantation layers 104A, 104B, 105A, 105B, and 105C. Thereafter, the mask is removed, the boron implantation layers 104A, 104B, 105A, 105B, and 105C, are masked, and phosphorus [P], which is an N-type dopant, is implanted through the mass into the regions other than the boron implantation layers 104A, 104B, 105A, 105B, and 105C at 150 keV and between 1×10^{12} and $1 \times 10^{13}/cm^2$, to form phosphorus implantation layers 106A through 106D.

[0132]

In this state, a heat treatment is carried out for several hours at between 1130 and 1180°C in a nitrogen gas ambient to thermally diffuse the boron [B] and phosphorus [P] of the boron implantation layers 104A, 104B, 105A, 105B, and 105C to form, as illustrated in FIG. 42, a first well region 103 with a depth of about 2.5 μm, P-type second well regions 104a and 140b with a depth of about 1 μm and a dopant concentration between 1×10^{15} and $1 \times 10^{18}/cm^3$ in the surface of the first well region 103, and P-type third well regions 106a through 106c, with a depth of about 1.5 μm and a dopant concentration of between 1×10^{15} and $1 \times 10^{18}/cm^3$, and N-type fourth well regions 106a through 106c, with a depth of about 2.5 μm and a dopant concentration of between 1×10^{15} and $1 \times 10^{18}/cm^3$, in the surface of the second semiconductor layer 102. The dopant concentration due to the boron [B] at this time will be as depicted by the dotted line D shown in FIG. 43.

[0133]

In the semiconductor substrate 100 that is structured in this way, the dopant profile that is appearing in the A-A' cross-section in FIG. 42 will be as depicted in FIG. 44. As can be appreciated from FIG. 44, a second well region 104a is formed up to a depth of about 1 μm from the surface of the second semiconductor layer 102, where the first well region 103 is interposed from the bottom surface of the second well region 104a up to a depth of about 2.5 μm, and the second semiconductor layer 102 is interposed from the bottom surface of the first well region 103 up to the surface of the first semiconductor layer 101. Furthermore, one dopant peak of the first well region 103 exists between the bottom surface of the second well region 104a and the second semiconductor layer 102. That is, ion implantation is carried out into the surface layer of the second semiconductor layer 102 based on ion implantation conditions that satisfy (Rp+3ΔRp) < thickness of the second semiconductor layer 102, reliably causing the lightly-doped second semiconductor layer 102 to be interposed between the bottom surface of the first well region 103 and the surface of the heavily-doped first semiconductor layer 101, and having one peak concentration under the second well region 104.

[0134]

Additionally, the dopant profile appearing in the B-B' cross-section in FIG. 42 will be as shown in FIG. 45. As can be appreciated from FIG. 45, a third well region 105a is formed up to a depth of about 1.5 μm from the surface of the second semiconductor layer 102, and the second semiconductor layer 102 is interposed from the bottom surface of the third well region 105a up to the surface of the first semiconductor layer 101.

[0135]

Additionally, the dopant profile appearing in the C-C' cross-section in FIG. 42 will be as shown in FIG. 46. As can be appreciated from FIG. 46, a fourth well region 106a is formed up to a depth of about 2.5 μm from the surface of the second semiconductor layer 102, and the second semiconductor layer 102 is interposed from the bottom surface of the fourth well region 106a up to the surface of the first semiconductor layer 101. Note that this fourth well region 106 has a surface layer of a second semiconductor layer 102, and a dopant concentration peak positioned at a depth of 1.7 μm from the second semiconductor layer 102.

[0136]

Along with the seventh embodiment, formed in this way, having the same effects as with the first embodiment, there is also the benefit of being able to select freely the central depth of the bottom portion region of the first well region 103, and the thickness thereof in the depth direction, through the use of an ion implantation method such that will have a dopant concentration peak at a prescribed depth

when forming the first well region 103 (and the fourth well regions 106a through 106c).

[0137]

While in the sixth embodiment 5 µm was given for a specific value for the thickness of the second semiconductor layer 102 and in the seventh embodiment 3 µm was given as a specific value for the thickness of the second semiconductor layer 102, there is no limitation thereto, but rather the thickness should be in a range between 1 and 10 µm. Note that of course specific optimal values, such as the dose of the implanted dopant, the ion implantation acceleration energy, the heat treatment temperature and heat treatment time for diffusing the dopant, and the like, will vary depending on the thickness of the second semiconductor layer 102.

[0138]

Moreover, while that which was depicted in the first through seventh embodiments, set forth above, had a dopant concentration of 1 x $10^{15}/cm^3$ for the epitaxial layer (in the state wherein the dopant of the first conductivity type was implanted through ion implantation) for structuring the second semiconductor layer 102, there is no limitation thereto, but rather the dopant concentration for the epitaxial layer for structuring the second semiconductor layer 102 can be selected freely between 1 x $10^{11}/cm^3$ and 1 x $10^{16}/cm^3$, which is adequately lower than the concentration of the well region. Note that of course specific optimal values, such as the dose of the implanted dopant, the ion implantation acceleration energy, the heat treatment temperature and heat treatment time for diffusing the dopant, and the like, will vary depending on the dopant concentration of the second semiconductor layer 102.

[0139]

Furthermore, while in the first through seventh embodiments, set forth above, 1 x $10^{19}/cm^3$ was given for the dopant concentration for the first semiconductor layer 101, there is no limitation thereto, but rather the dopant concentration for the first semiconductor layer 101 can be selected freely between 1 x $10^{18}/cm^3$, which is adequately higher than the concentration of the well regions, to 1 x $10^{20}/cm^3$.

[0140]

[EFFECTS OF THE INVENTION]

The first aspect of the present invention comprises: a semiconductor substrate having a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, a first well region of a second conductivity type, formed in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, a second well region, of the first semiconductor type, formed in the surface of the first well region, a third well region, of the first conductivity type, formed in the surface of the second semiconductor layer, with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and a fourth well region, of the second conductivity type, formed separated from the first well region, in the second semiconductor layer; provided with: a first semiconductor device that is formed in the second well region of the semiconductor substrate; a second semiconductor device that is formed in the third well region of the semiconductor substrate; and a third semiconductor device that is formed in the fourth well region of the semiconductor substrate, and thus a lightly-doped second semiconductor layer is interposed between the first well region and the heavily-doped first semiconductor layer, having the effect of improving resistance to latch-up, improving the punch-through breakdown voltage between the second well region and the second semiconductor layer, and improving the junction breakdown voltage between the first well region and the second semiconductor layer.

[0141]

The second aspect of the present invention comprises: a semiconductor substrate having a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, a first well region of a second conductivity type, formed in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, a second well region, of the first semiconductor type, formed in the surface of the first well region, a third well region, of the first conductivity type, formed in the surface of the second semiconductor layer, with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and a fourth well region, of the second conductivity type, formed separated from the first well region, in the second semiconductor layer; provided with: a nonvolatile memory cell that is formed in the second well region of the semiconductor substrate; an MOS transistor of the second conductivity type that is formed in the third well region of the semiconductor substrate; and an MOS transistor of the first conductivity type that is formed in the fourth well region of the semiconductor substrate, and thus has the effect of providing a nonvolatile semiconductor storage device wherein a lightly-doped second semiconductor layer is interposed between the first well region and the heavily-doped first semiconductor layer, with improved latch-up resistance, improved punch-through breakdown voltage between the second well region and the second semiconductor layer, improved junction breakdown voltage between the first well region and the second semiconductor layer, and little dopant and a low defect density in the gate insulating film.

[0142]

The third aspect of the present invention comprises: a memory cell array having a plurality of memory cells; and peripheral circuitry for writing information to a memory cell of the memory cell array, reading out information that has been stored in the memory cell, and erasing information that has been stored in the memory cell; wherein: the plurality of memory cells in the memory cell array is divided into a plurality of blocks of a plurality of memory cells each, where the erasing operation is carried out as multiple bits by the block unit, comprising: a semiconductor substrate having a P-type first

semiconductor layer, a P-type second semiconductor layer, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, an N-type first well region, formed in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, a plurality of P-type second well regions formed separated from each other in the surface of the first well region, a P-type third well region formed in the surface of the second semiconductor layer with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and an N-type fourth well region formed separated from the first well region in the second semiconductor layer, wherein: for each block unit, the plurality of memory cells for the individual block unit, corresponding to one of the plurality of second well regions, is formed in the corresponding second well region; at least some N-channel MOS transistors of the plurality of the N-channel MOS transistors that structure the peripheral circuitry are formed in the third well region; and at least some of the P-channel MOS transistors of the plurality of P-channel MOS transistors that structure the peripheral circuitry are formed in the fourth well region, and thus has the effect of providing a nonvolatile semiconductor storage device wherein a first well region can apply electropotentials independently to second well regions, and wherein a lightly-doped second semiconductor layer is interposed between the first well region and the heavily-doped first semiconductor layer, with improved latch-up resistance, improved punch-through breakdown voltage between the second well region and the second semiconductor layer, improved junction breakdown voltage between the first well region and the second semiconductor layer, and little dopant and a low defect density in the gate insulating film.

[0143]

The fourth aspect of the present invention comprises: a memory cell array having a plurality of memory cells; and peripheral circuitry for writing information to a memory cell of the memory cell array, reading out information that has been stored in the memory cell, and erasing information that has been stored in the memory cell; wherein: the plurality of memory cells in the memory cell array is divided into a plurality of blocks of a plurality of memory cells each, where the erasing operation is carried out as multiple bits by the block unit, comprising: a semiconductor substrate having a P-type first semiconductor layer, a P-type second semiconductor layer, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, a plurality of N-type first well regions formed separated from each other in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well regions and the surface of the first semiconductor layer, a plurality of P-type second well regions formed respectively in the surfaces of the respective first well regions, a P-type third well region formed in the surface of the second semiconductor layer with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and an N-type fourth well region formed separated from the first well region in the second semiconductor layer, wherein: for each block unit, the plurality of memory cells for the individual block unit, corresponding to one of the plurality of second well regions, is formed in the corresponding second well region; at least some N-channel MOS transistors of the plurality of the N-channel MOS transistors that structure the peripheral circuitry are formed in the third well region; and at least some of the P-channel MOS transistors of the plurality of P-channel MOS transistors that structure the peripheral circuitry are formed in the fourth well region, and thus has the effect of providing a nonvolatile semiconductor storage device wherein a first well region can apply electropotentials independently to second well regions, and wherein a lightly-doped second semiconductor layer is interposed between the first well region and the heavily-doped first semiconductor layer, with improved latch-up resistance, improved punch-through breakdown voltage between the second well region and the second semiconductor layer, improved junction breakdown voltage between the first well region and the second semiconductor layer, and little dopant and a low defect density in the gate insulating film.

[0144]

The fifth aspect of the present invention comprises: a memory cell array having a plurality of memory cells; and peripheral circuitry for writing information to a memory cell of the memory cell array, reading out information that has been stored in the memory cell, and erasing information that has been stored in the memory cell; the peripheral circuitry has a voltage step-up circuit for receiving a power supply voltage that is applied to a power supply voltage node and outputting a stepped-up electropotential that is higher than that of the power supply voltage, comprising: a semiconductor substrate having a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, deposited through epitaxial deposition on the surface of the first semiconductor layer, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, a first well region of a second conductivity type, formed in the surface of the second semiconductor layer with the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, a second well region, of the first semiconductor type, formed in the surface of the first well region, a third well region, of the first conductivity type, formed in the surface of the second semiconductor layer, with a dopant concentration that is higher than the dopant concentration of the second semiconductor layer, and a fourth well region, of the second conductivity type, formed separated from the first well region, in the second semiconductor layer, wherein: a semiconductor device for structuring and output stage of the voltage step-up circuit is formed in the second well region; at least some MOS transistors of the plurality of the MOS transistors of the second conductivity type that structure the peripheral circuitry are formed in the third well region; and at least some MOS transistors of the plurality of the MOS transistors of the first conductivity type that structure the peripheral circuitry are formed in the

third well region, and thus a lightly-doped second semiconductor layer is interposed between the first well region and the heavily-doped first semiconductor layer, having the effect of improving resistance to latch-up, improving the punch-through breakdown voltage between the second well region and the second semiconductor layer, and improving the junction breakdown voltage between the first well region and the second semiconductor layer for the semiconductor devices that structure the output stage of a voltage step-up circuit.

[0145]

The sixth aspect of the present invention includes: a step for forming an epitaxial layer through epitaxial deposition on a surface of a first semiconductor layer of a first conductivity type; a step for forming, on the surface of the first semiconductor layer, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through ion implantation of a dopant of the first conductivity type into the surface of the epitaxial layer and performing thermal diffusion; a step for forming, in the surface of the second semiconductor layer, a first well region of a second conductivity type, with the second semiconductor layer interposed between the surface of the first semiconductor layer and the first well region; a step for forming a second well region of the first conductivity type in the surface of the first well region; a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer; a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region; a step for forming a first semiconductor device in the second well region; a step for forming a second semiconductor device in the third well region; and a step for forming a third semiconductor device in the fourth well region, and thus a lightly-doped second semiconductor layer is interposed between the first well region and the heavily-doped first semiconductor layer, having the effect of improving resistance to latch-up, improving the punch-through breakdown voltage between the second well region and the second semiconductor layer, and improving the junction breakdown voltage between the first well region and the second semiconductor layer.

[0146]

The seventh aspect of the present invention includes: a step for forming, on the surface of a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through epitaxial deposition onto the surface of the first semiconductor layer of the first conductivity type; a step for forming a first well region of a second conductivity type, in the surface of the second semiconductor layer, including a step for ion implantation of a dopant of the second conductivity type such that the peak of the dopant concentration will be positioned at a position of a prescribed depth from the surface of the second semiconductor layer; a step for forming, in the surface of the first well region, a second well region of the first conductivity type at a prescribed position in the first well region above the position of the peak of the dopant concentration; a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer; a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region; a step for forming a first semiconductor device in the second well region; a step for forming a second semiconductor device in the third well region; and a step for forming a third semiconductor device in the fourth well region, and thus a lightly-doped the second semiconductor layer is interposed between the first well region and the heavily-doped first semiconductor layer, having the effect of improving the punch-through breakdown voltage between the second well region and the second semiconductor layer, improving the junction breakdown voltage between the first well region and the second semiconductor layer, and also enabling the dopant concentration profile at the bottom portion of the first well region to be selected freely because the ion implantation is carried out so as to position the peak of the dopant concentration at a position at a prescribed depth from the surface of the second semiconductor layer.

[0147]

The eighth aspect of the present invention includes: a step for forming an epitaxial layer through epitaxial deposition on a surface of a first semiconductor layer of a first conductivity type; a step for forming, on a surface of the first semiconductor layer, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through ion implantation of a dopant of the first conductivity type so that the peak of the dopant concentration will be positioned at a position that is a prescribed depth from the surface of the epitaxial layer; a step for forming, in the surface of the second semiconductor layer, a first well region of a second conductivity type; a step for forming a second well region of the first conductivity type in the surface of the first well region; a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer; a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region; a step for forming a first semiconductor device in the second well region; a step for forming a second semiconductor device in the third well region; and a step for forming a third semiconductor device in the fourth well region, and thus a lightly-doped the second semiconductor layer is interposed between the first well region and the heavily-doped first semiconductor layer, having the effect of improving the punch-through breakdown voltage between the second well region and the second semiconductor layer, improving the junction breakdown voltage between the first well region and the second semiconductor layer, and also enabling the dopant concentration profile at the bottom portion of the second semiconductor layer to be selected freely because the ion implantation is carried out so as to

position the peak of the dopant concentration at a position at a prescribed depth from the surface of the epitaxial layer of the second semiconductor layer.

[0148]

The ninth aspect of the present invention including: a step for forming an epitaxial layer through epitaxial deposition on a surface of a first semiconductor layer of a first conductivity type; a step for forming, on a surface of the first semiconductor layer, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through ion implantation of a dopant of the first conductivity type so that the peak of the dopant concentration will be positioned at a position that is a prescribed depth from the surface of the epitaxial layer; a step for forming a first well region of a second conductivity type, in the surface of the second semiconductor layer, with a peak position of the second semiconductor layer interposed between the first well region and the surface of the first semiconductor layer, including a step for ion implantation of a dopant of the second conductivity type such that the peak of the dopant concentration will be positioned at a position of a prescribed depth from the surface of the second semiconductor layer; a step for forming, in the surface of the first well region, a second well region of the first conductivity type; a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer; a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region; a step for forming a first semiconductor device in the second well region; a step for forming a second semiconductor device in the third well region; and a step for forming a third semiconductor device in the fourth well region, and thus a lightly-doped the second semiconductor layer is interposed between the first well region and the heavily-doped first semiconductor layer, having the effect of improving the punch-through breakdown voltage between the second well region and the second semiconductor layer, improving the junction breakdown voltage between the first well region and the second semiconductor layer, and also enabling the dopant concentration profile at the bottom portion of the first well region to be selected freely because the ion implantation is carried out so as to position the peak of the dopant concentration at a position at a prescribed depth from the surface of the second semiconductor layer, while also enabling the dopant concentration profile at the bottom portion of the second semiconductor layer to be selected freely because the ion implantation is carried out so as to position the peak of the dopant concentration at a position at a prescribed depth from the surface of the epitaxial layer of the second semiconductor layer.

[0149]

The tenth aspect of the present invention includes: a step for forming, on the surface of a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through epitaxial deposition onto the surface of the first semiconductor layer of the first conductivity type; a step for forming, in the surface of the second semiconductor layer, a first well region of a second conductivity type, through implantation, into the surface of the second semiconductor layer, dopant of the second semiconductor type, followed by thermally diffusing the dopant that has been implanted with the value of $4\sqrt{Dt}$ at a value that is less than the thickness of the second semiconductor layer; a step for forming a second well region of the first conductivity type in the surface of the first well region; a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer; a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region; a step for forming a first semiconductor device in the second well region; a step for forming a second semiconductor device in the third well region; and a step for forming a third semiconductor device in the fourth well region, and thus a second semiconductor layer that is formed through epitaxial growth can be interposed reliably between the first well region and the heavily-doped first semiconductor layer, having the effect of improving resistance to latch-up, improving the punch-through breakdown voltage between the second well region and the second semiconductor layer, and improving the junction breakdown voltage between the first well region and the second semiconductor layer.

[0150]

The eleventh aspect of the present invention includes: a step for forming, on the surface of a first semiconductor layer of a first conductivity type, a second semiconductor layer of the first conductivity type, having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer, through epitaxial deposition onto the surface of the first semiconductor layer of the first conductivity type; a step for forming, in the surface of the second semiconductor layer, a first well region of a second conductivity type, through implantation, into the surface of the second semiconductor layer, dopant of the second semiconductor type, with the value of $(Rp+3\Delta Rp)$ at a value that is less than the thickness of the second semiconductor layer; a step for forming a second well region of the first conductivity type in the surface of the first well region; a step for forming, in the surface of the second semiconductor layer, a third well region of the first conductivity type, having a higher dopant concentration than the dopant concentration of the second semiconductor layer; a step for forming, in the surface of the second semiconductor layer, a fourth well region of the second conductivity type, separated from the first well region; a step for forming a first semiconductor device in the second well region; a step for forming a second semiconductor device in the third well region; and a step for forming a third semiconductor device in the fourth well region, and thus a lightly-doped second semiconductor layer that is formed through epitaxial growth can be interposed reliably between the first well region and the heavily-doped first semiconductor layer, having the effect of improving resistance to latch-up, improving the punch-through breakdown voltage between the second well region and the

second semiconductor layer, and improving the junction breakdown voltage between the first well region and the second semiconductor layer.

[BRIEF DESCRIPTIONS OF THE DRAWINGS]

FIG. 1 depicts a first embodiment of the present invention.

FIG. 2 is a cross-sectional drawing depicting a semiconductor substrate 100 to which the first embodiment of the present invention is applied.

FIG. 3 is a cross-sectional drawing of critical portions, depicting a first embodiment according to the present invention.

FIG. 4 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which the first embodiment according to the present invention is applied.

FIG. 5 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which the first embodiment according to the present invention is applied.

FIG. 6 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which the first embodiment according to the present invention is applied.

FIG. 7 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which the first embodiment according to the present invention is applied.

FIG. 8 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which the first embodiment according to the present invention is applied.

FIG. 9 is a diagram depicting the separate dopant profiles in manufacturing of a semiconductor substrate 100 to which the first embodiment according to the present invention is applied.

FIG. 10 is a diagram showing the dopant profile in the A-A' cross-section in FIG. 8.

FIG. 11 is a diagram showing the dopant profile in the B-B' cross-section in FIG. 8.

FIG. 12 is a diagram showing the dopant profile in the C-C' cross-section in FIG. 8.

FIG. 13 is a cross-sectional drawing illustrating another example of a semiconductor substrate 100 to which the first embodiment according to the present invention is applied.

FIG. 14 is a cross-sectional drawing illustrating yet another example of a semiconductor substrate 100 to which the first embodiment according to the present invention is applied.

FIG. 15 is a cross-sectional drawing of critical portions, depicting a second embodiment according to the present invention.

FIG. 16 is a circuit diagram depicting a voltage step-up circuit in a high-voltage generating circuit to which a third embodiment according to the present invention is applied.

FIG. 17 is a cross-sectional drawing of critical portions depicting an example wherein a voltage step-up circuit of a high-voltage generating circuit to which the third embodiment according to the present invention is applied is incorporated in the semiconductor substrate.

FIG. 18 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which a fourth embodiment according to the present invention is applied.

FIG. 19 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which the fourth embodiment according to the present invention is applied.

FIG. 20 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which the fourth embodiment according to the present invention is applied.

FIG. 21 is a diagram depicting the separate dopant profiles in manufacturing of a semiconductor substrate 100 to which the fourth embodiment according to the present invention is applied.

FIG. 22 is a diagram showing the dopant profile in the A-A' cross-section in FIG. 20.

FIG. 23 is a diagram showing the dopant profile in the B-B' cross-section in FIG. 20.

FIG. 24 is a diagram showing the dopant profile in the C-C' cross-section in FIG. 20.

FIG. 25 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which a fifth embodiment according to the present invention is applied.

FIG. 26 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which the fifth embodiment according to the present invention is applied.

FIG. 27 is a diagram depicting the separate dopant profiles in manufacturing of a semiconductor substrate 100 to which the fifth embodiment according to the present invention is applied.

FIG. 28 is a diagram showing the dopant profile in the A-A' cross-section in FIG. 26.

FIG. 29 is a diagram showing the dopant profile in the B-B' cross-section in FIG. 26.

FIG. 30 is a diagram showing the dopant profile in the C-C' cross-section in FIG. 26.

FIG. 31 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which a sixth embodiment according to the present invention is applied.

FIG. 32 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which the sixth embodiment according to the present invention is applied.

FIG. 33 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which the sixth embodiment according to the present invention is applied.

FIG. 34 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which the sixth embodiment according to the present invention is applied.

FIG. 35 is a diagram depicting the separate dopant profiles in manufacturing of a semiconductor substrate 100 to which the sixth embodiment according to the present invention is applied.

FIG. 36 is a diagram showing the dopant profile in the A-A' cross-section in FIG. 34.

FIG. 37 is a diagram showing the dopant profile in the B-B' cross-section in FIG. 34.

FIG. 38 is a diagram showing the dopant profile in the C-C' cross-section in FIG. 34.

FIG. 39 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which a seventh embodiment according to the present invention is applied.

FIG. 40 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which the seventh embodiment according to the present invention is applied.

FIG. 41 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which the seventh embodiment according to the present invention is applied.

FIG. 42 is a cross-sectional drawing illustrating, in step order, manufacturing of a semiconductor substrate 100 to which the seventh embodiment according to the present invention is applied.

FIG. 43 is a diagram depicting the separate dopant profiles in manufacturing of a semiconductor substrate 100 to which the seventh embodiment according to the present invention is applied.

FIG. 44 is a diagram showing the dopant profile in the A-A' cross-section in FIG. 42.

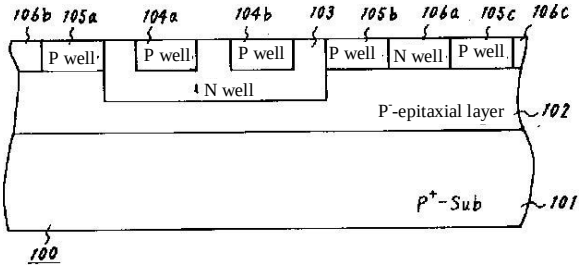
FIG. 45 is a diagram showing the dopant profile in the B-B' cross-section in FIG. 42.

FIG. 46 is a diagram showing the dopant profile in the C-C' cross-section in FIG. 42.

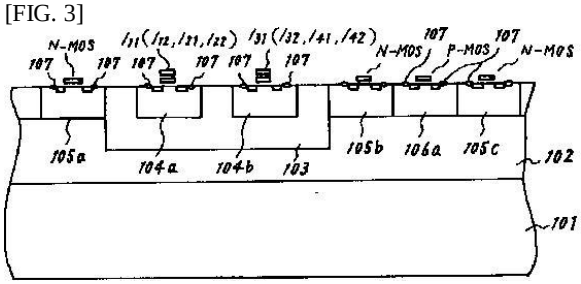
[EXPLANATION OF REFERENCE SYMBOLS]

1_{11} through 1_{41}: Memory Cells
2a through 2b: Blocks
3_1 through 3_4: Word Lines
4_1 through 4_2: Word Lines
5_{1a} through 5_{2b}: Primary Bit Lines
7a through 7b: Source Lines
100: Semiconductor Substrate
101: First Semiconductor Layer
102: Second Semiconductor Layer
103: First Well Region
104a through 104b: Second Well Regions
105a through 105c: Third Well Regions
106a through 106b: Fourth Well Regions

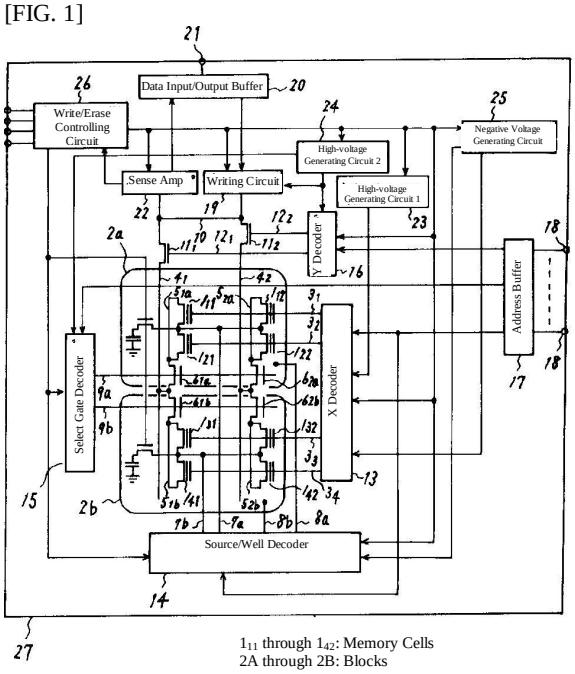
[FIG. 2]



[FIG. 3]

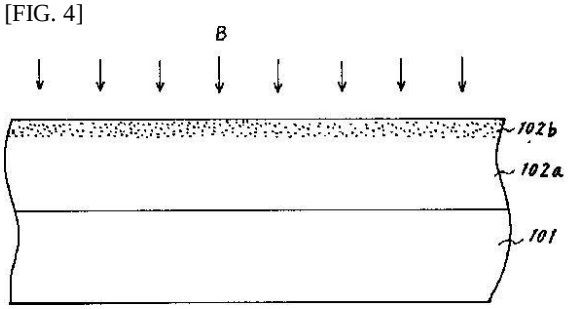


[FIG. 1]

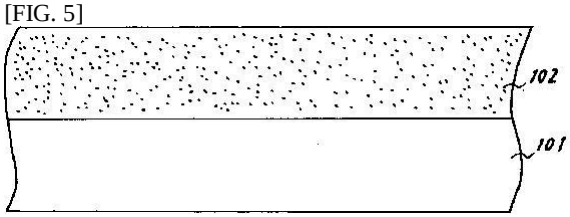


1_{11} through 1_{42}: Memory Cells
2A through 2B: Blocks
3_1 through 3_4: Word Lines
4_1 through 4_2: Primary Bit Lines
5_{1a} through 5_{2b}: Secondary Bit Lines
7a through 7b: Source Lines

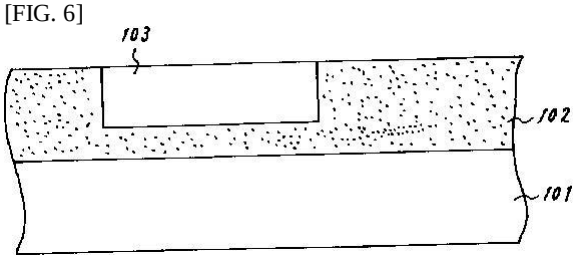
[FIG. 4]



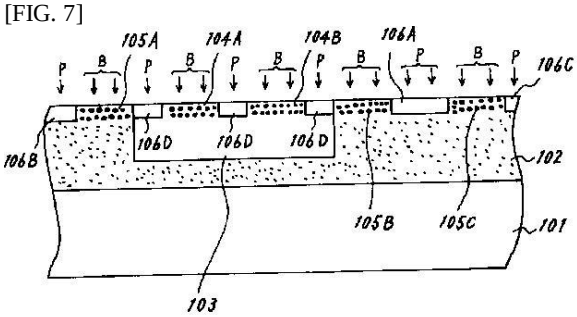
[FIG. 5]



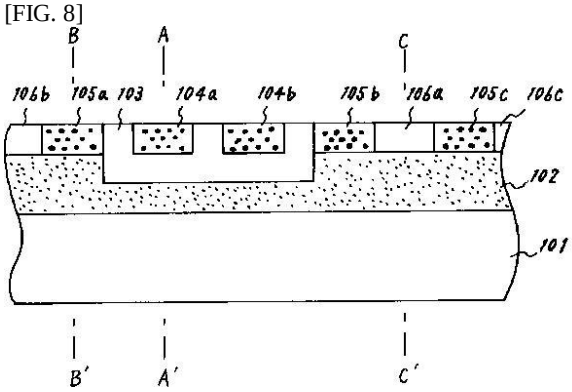
[FIG. 6]



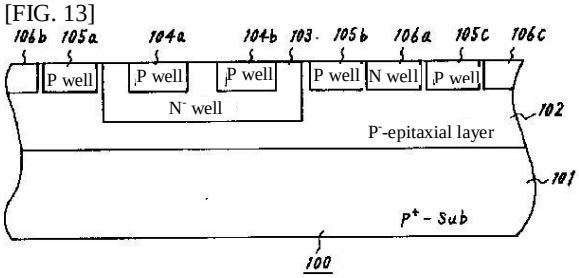
[FIG. 7]



[FIG. 8]



[FIG. 13]



[FIG. 16]

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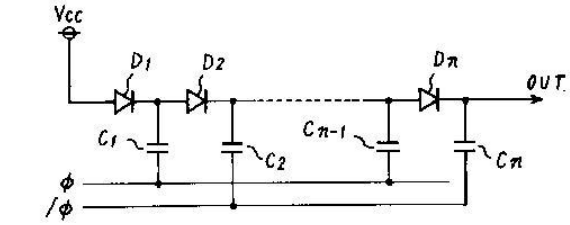

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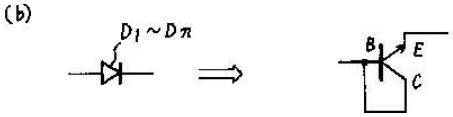
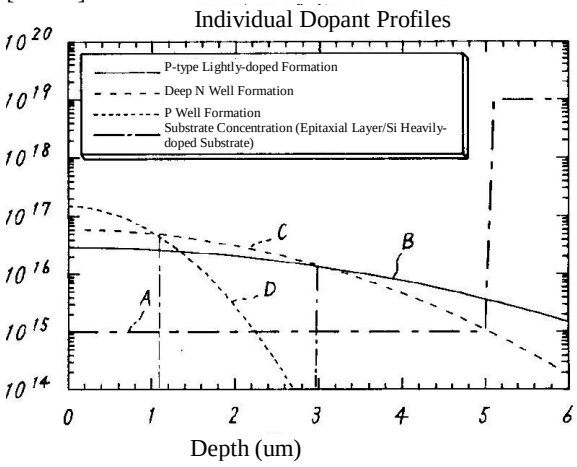
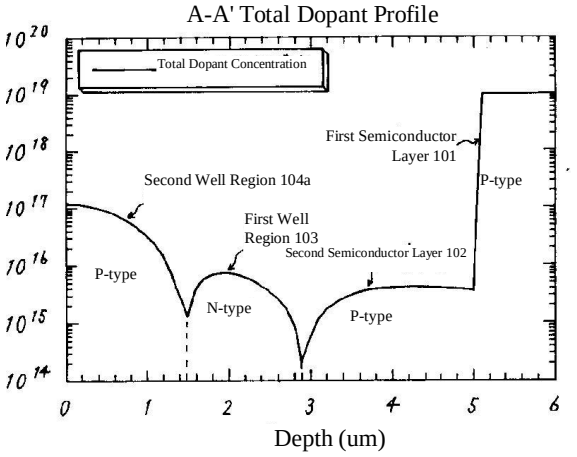


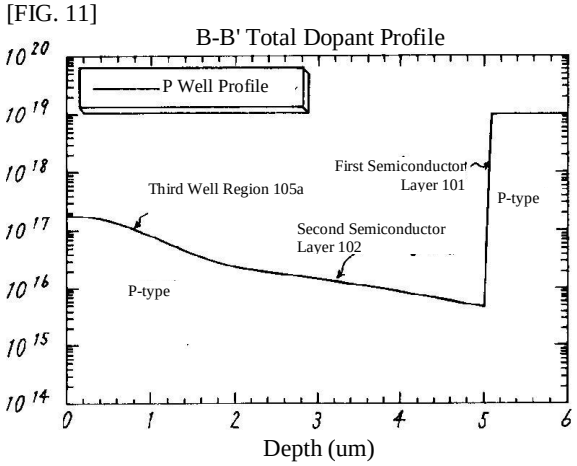
[FIG. 9]



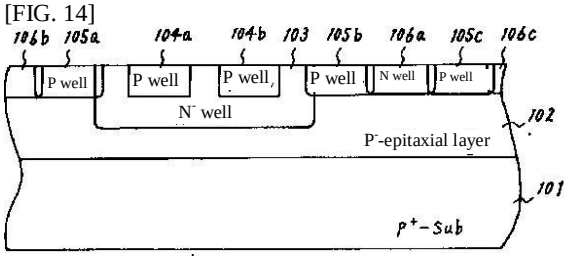
[FIG. 10]



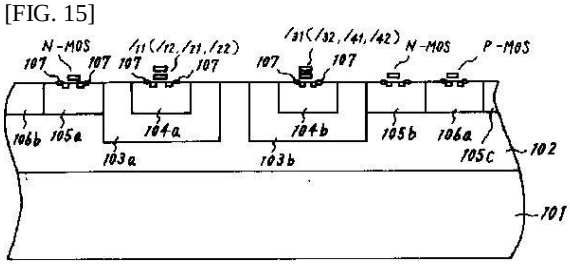
[FIG. 11]



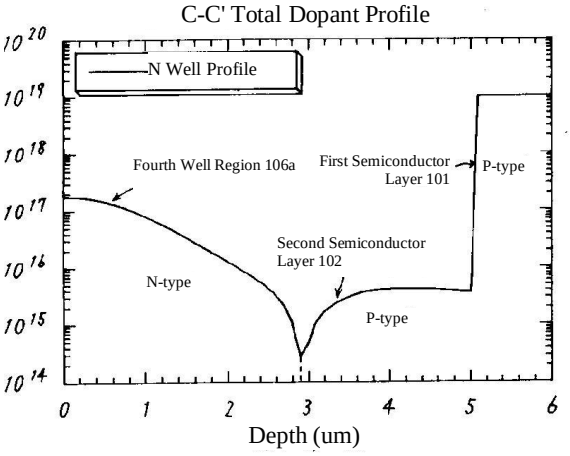
[FIG. 14]



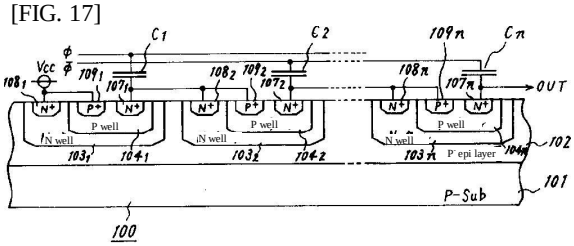
[FIG. 15]



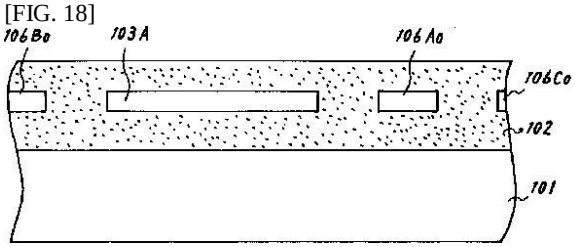
[FIG. 12]



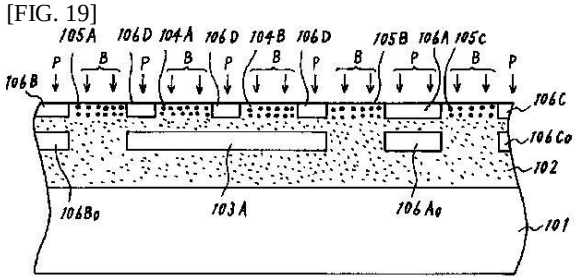
[FIG. 17]



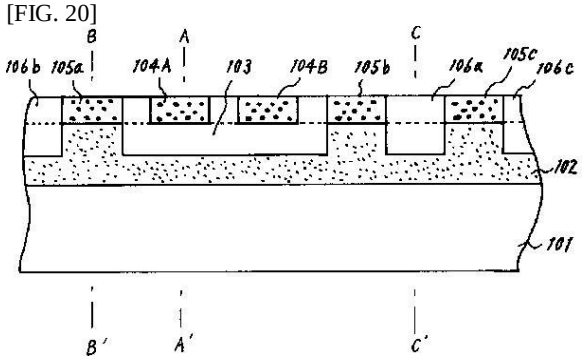
[FIG. 18]



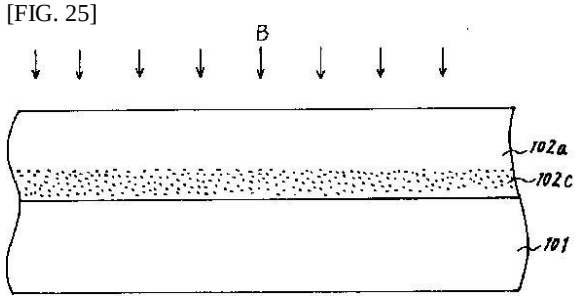
[FIG. 19]



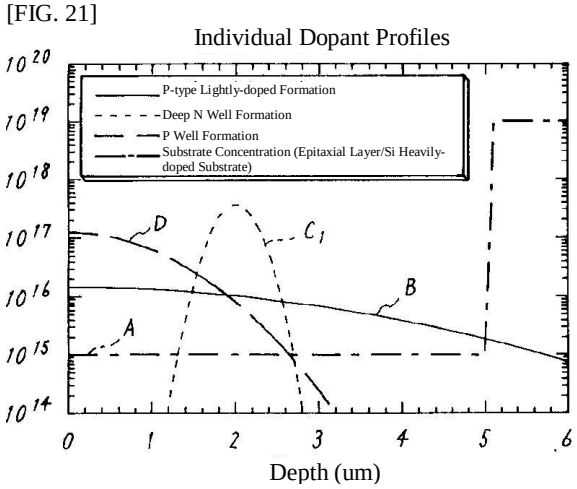
[FIG. 20]



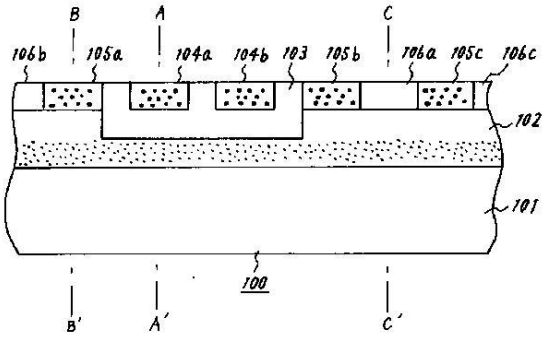
[FIG. 25]



[FIG. 21]



[FIG. 26]



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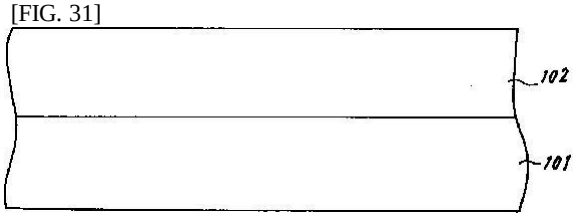

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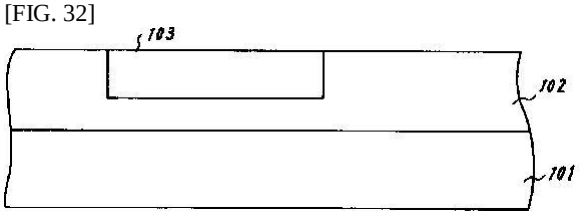

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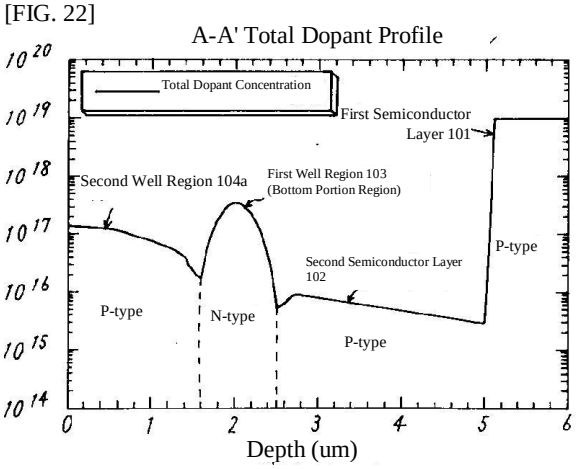

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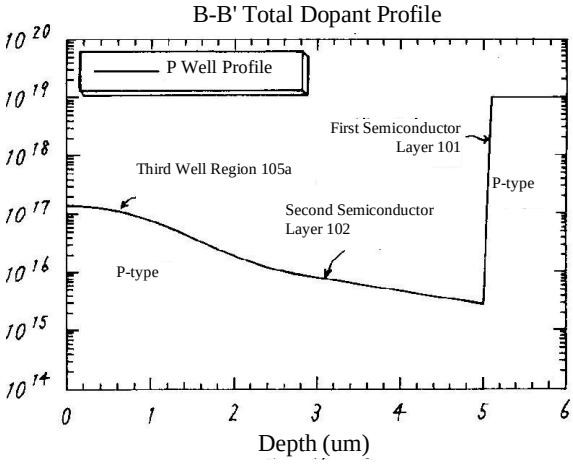

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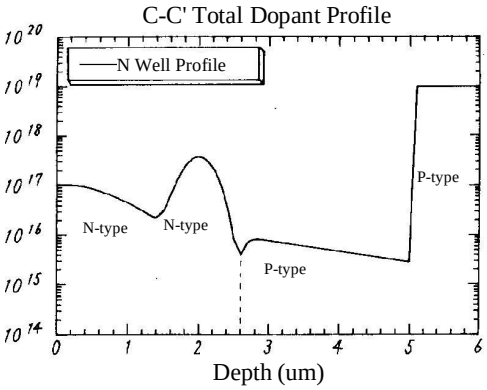

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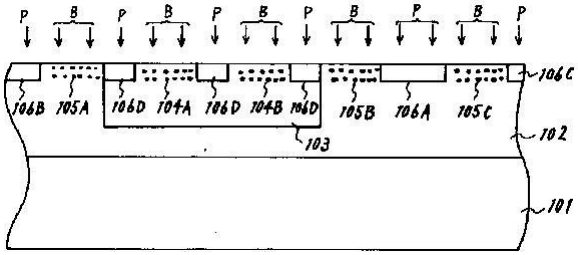

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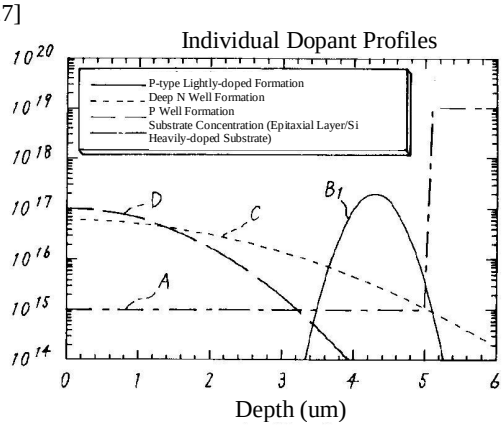

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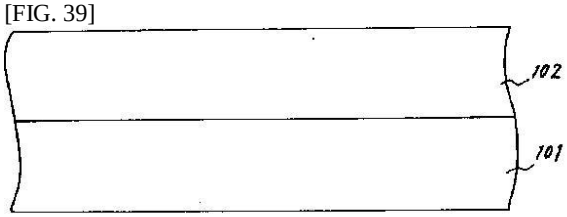

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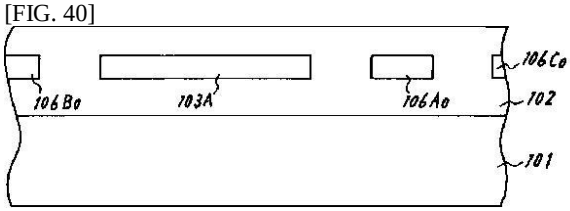

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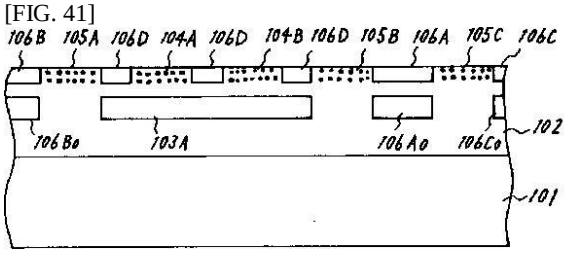

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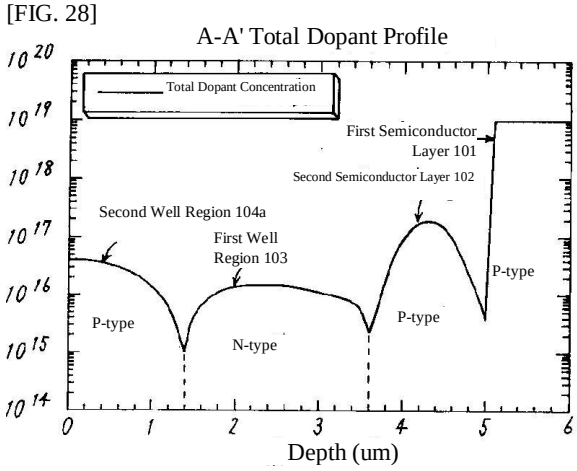

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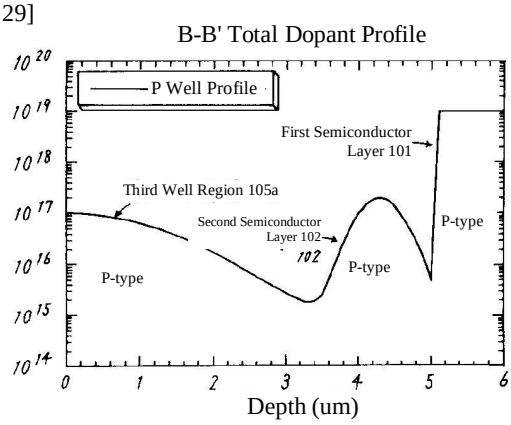

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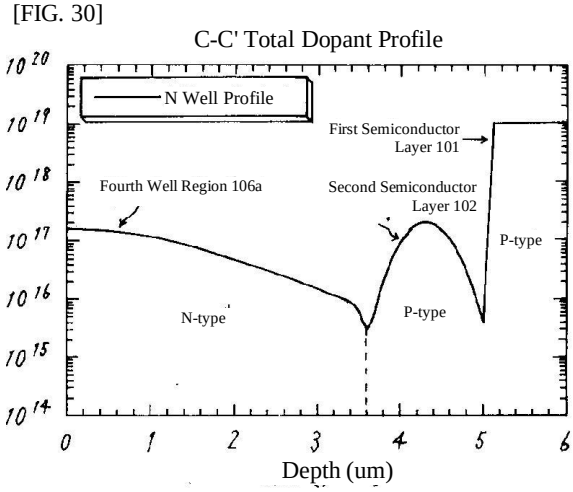

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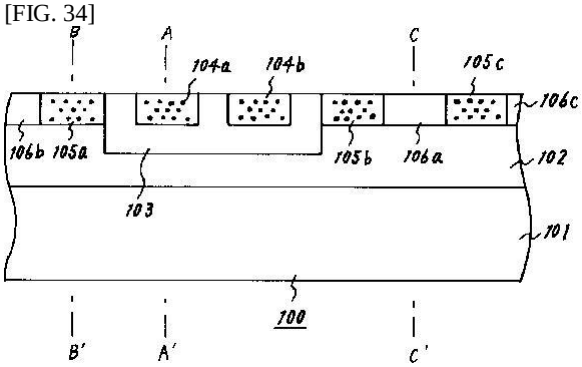

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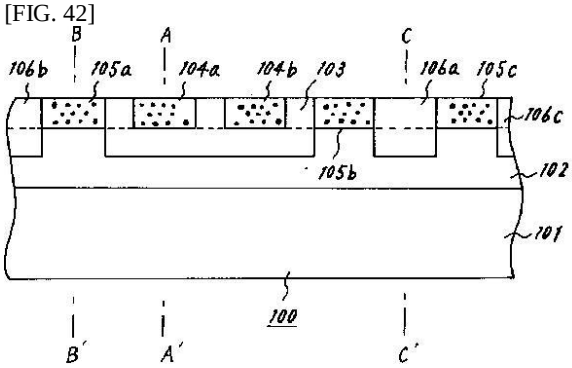

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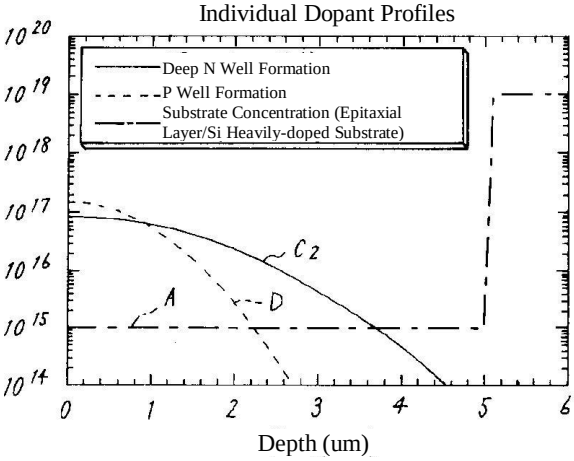

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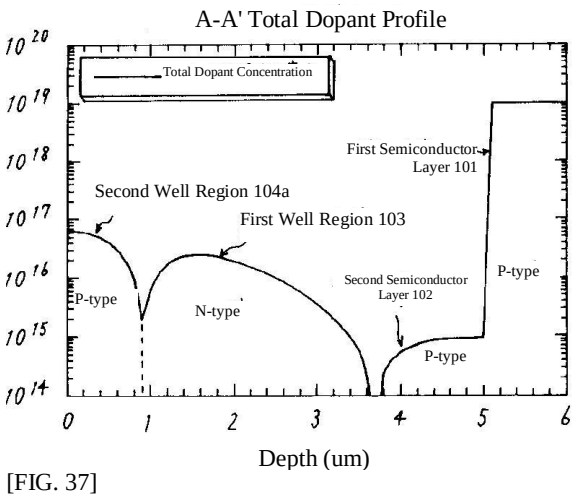

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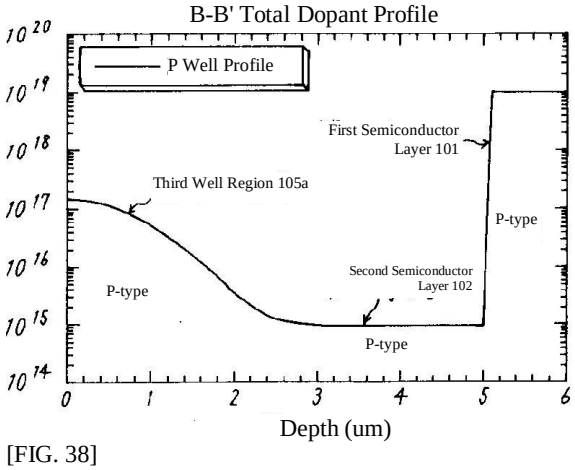

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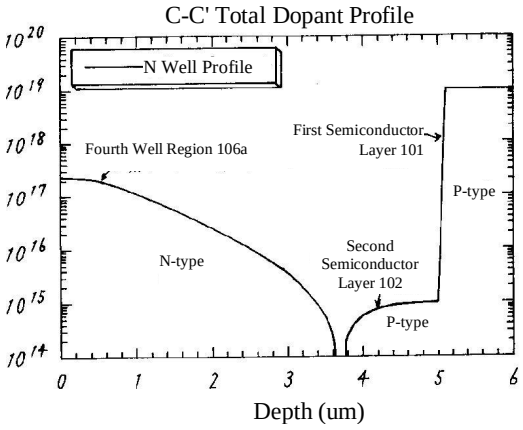

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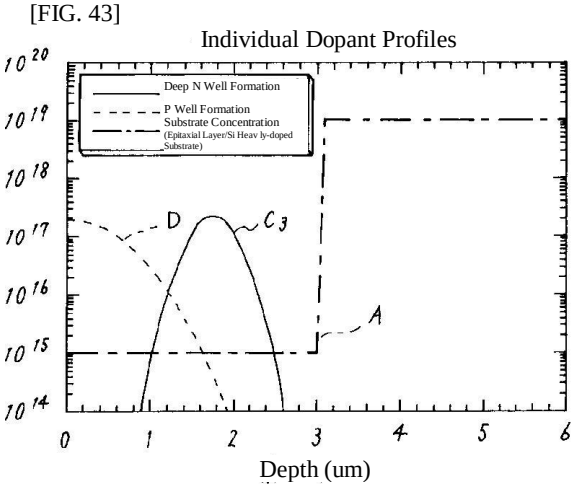

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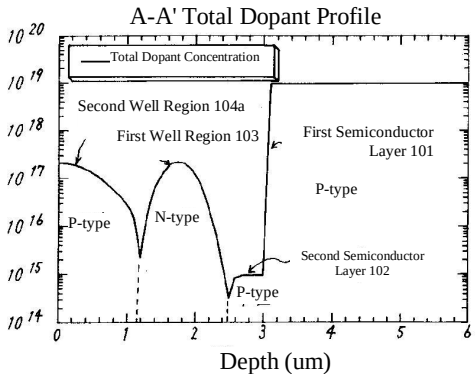

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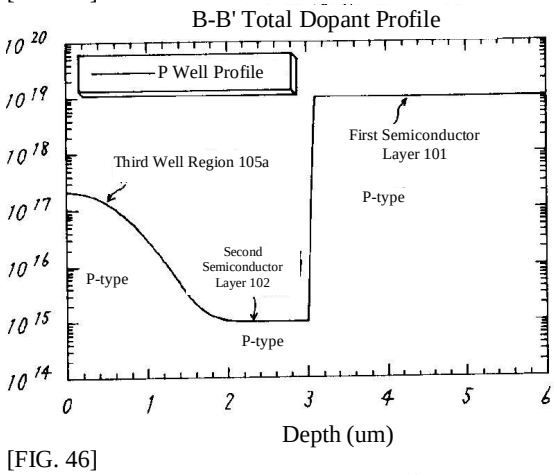

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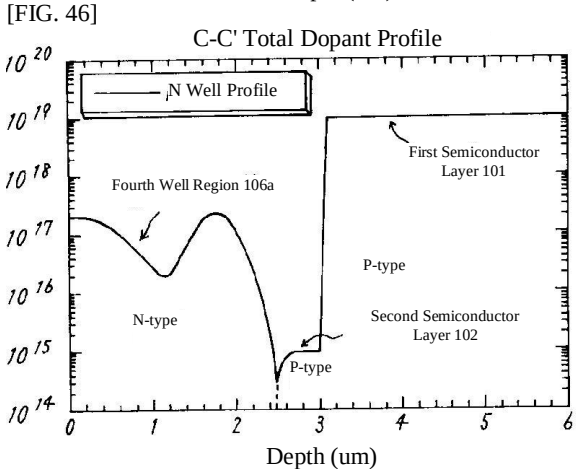

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(51) Int. Cl.[6]	ID codes	JPO file numbers	FI	Technical indications
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29/792				

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I further declare and certify that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001.

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Date: 9/10/2023

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