EXHIBIT 1

UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

Greenthread, LLC *Plaintiff,* *v.* Intel Corporation; Dell Inc.; and Dell Technologies Inc. *Defendants.*	Civil Action No. 6:22-cv-105-ADA JURY TRIAL DEMANDED

DECLARATION OF KONSTANTINOS P. GIAPIS IN SUPPORT OF GREENTHREAD'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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TABLE OF EXHIBITS

Exhibit	Description
1	Intentionally omitted
2	U.S. Patent No. 8,421,195 to G.R. Mohan Rao ("195 patent") (GREENTHREAD-WDTX-000027–40)
3	U.S. Patent No. 10,510,842 to G.R. Mohan Rao ("842 patent") (GREENTHREAD-WDTX-000070–84)
4	Excerpts from Chen, J. Y., CMOS Devices and Technology for VLSI, Prentice-Hall (1990) (GREENTHREAD-WDTX-007426–007682) ("Chen")
5	*Greenthread, LLC v. Samsung Elecs. Co., Ltd.*, No. 2:19-cv-00147-JRG, Dkt. 67 (Claim Construction Memorandum Opinion and Order), E.D. Tex. Apr. 20, 2020 (GREENTHEAD-WDTX-002761–002792) ("EDTX *Markman* Order")
6	*Samsung Elecs. Co., Ltd. v. Greenthread, LLC*, IPR2020-00289, Ex. 1003 (Apr. 14, 2020) (GREENTHREAD-WDTX-003869–003959) ("Dr. Smith declaration")
7	The American Heritage Dictionary of the English Language, Third Edition (2002), at 1792 (defining "substrate") (GREENTHREAD-WDTX-007794–007797)
8	Excerpts from Webster's Third New International Dictionary of the English Language Unabridged, Merriam-Webster, Inc. (1992) (GREENTHREAD-WDTX-002826 – GREENTHREAD-WDTX–002834, GREENTHREAD-WDTX-007793)
9	Excerpts from Baker, R. J., CMOS Circuit Design, Layout, and Simulation, IEEE (1998) (GREENTHREAD-WDTX-002674–002715) ("Baker")
10	Defendants' Preliminary Claim Constructions, No. 6:22-cv-105-ADA (W.D. Tex.) (served Sept. 19, 2022)
11	File History of U.S. Patent No. 10,510,842 ("842 file history") (GREENTHREAD-WDTX-001059–1246)
12	Excerpts from Howe, R. T., Microelectronics: An Integrated Approach, Prentice-Hall (1997) ("Howe") (GREENTHREAD-WDTX-002793–2813)
13	Excerpts from Wolf S., Silicon Processing for the VLSI Era Volume 2: Process Integration, Lattice Press (1990)
14	Excerpts from Wolf S., Silicon Processing for the VLSI Era Volume 3: The Submicron MOSFET, Lattice Press (1995) (GREENTHREAD-WDTX-002877–2883)

DISPUTED CLAIM CONSTRUCTIONS

#	Claim(s)[1]	Terms	Greenthread	Defendants
1	195:1 502:7 222:44	"surface layer" and related terms ("an active region . . . disposed on one surface of said surface layer" / "a single drift layer disposed between the other surface of said surface layer and [said/the] substrate")	Plain and ordinary meaning, where the plain and ordinary meaning is "a layer at the surface"	Indefinite
2	195:1 502:7 842:1, 9 481:1, 20 222:1, 21, 39, 41, 42, 44 014:1, 21	"substrate"	Plain and ordinary meaning, where the plain and ordinary meaning is an "underlying layer"	"the initial material within which or on which the semiconductor device is fabricated"
3	195:1 502:7 842:1, 9 481:1, 20 222:1, 21, 39, 41, 42, 44 014:1, 21	"active region"	Plain and ordinary meaning	"region that forms the current path of a device"
4	195:1 502:7 222:44	"said [drift layer further/well region …] having a [first/second] static unidirectional electric drift field"	Plain and ordinary meaning	"said [drift layer further/well region …] having a [first/second] static electric drift field that is unidirectional over the [drift layer/well region"
		"said [drift layer further/well region] having a graded		"said [drift layer further/well region] having a

[1] The notation "195:1" (for example) denotes claim 1 of the '195 patent. Patent numbers are specified below in Section I.

		concentration of dopants generating a [first/second] static unidirectional electric drift field"		graded concentration of dopants generating a [first/second] static electric drift field that is unidirectional over the [drift layer/well region]"
5	195:1 502:7 842:1, 9 481:1, 20 222:1, 21, 39, 41, 42, 44 014:1, 21	"to aid the movement of minority carriers from ... to …"	Plain and ordinary meaning	Indefinite Alternative construction: "to sweep the minority carriers from … to …
		"to aid carrier movement from ... [to/towards]"		Indefinite Alternative construction: "to sweep the carriers from … [to/towards] …
6	195:1 502:7 842:1, 9 481:1, 20 222:1, 21, 39, 41, 42, 44 014:1, 21	"well region"	Plain and ordinary meaning, where portions of a well are not well regions.	"A well, whether formed by single or multiple implants. Portions of a well are not well regions."
7	842:1, 9 481:1, 20 222:1, 21, 39, 41, 42 014:1, 21	"active region … within which transistors can be formed"	Plain and ordinary meaning	Indefinite

DECLARATION OF KONSTANTINOS P. GIAPIS

I, Konstantinos P. Giapis, do hereby declare as follows:

I. INTRODUCTION

1. I have been retained on behalf of Greenthread, LLC ("Greenthread"), and its counsel, McKool Smith, P.C., as an expert in this proceeding, in which I understand Intel Corporation, Dell Inc., and Dell Technologies Inc. are the defendants ("Defendants"). I am personally knowledgeable about the matters stated herein and am competent to make this declaration.

2. I understand that Greenthread will submit this Declaration in connection with a brief supporting its proposed construction of various terms in certain claims of U.S. Patent Nos. 8,421,195 ("the '195 patent); 9,190,502 ("the '502 patent"); 10,510,842 ("the '842 patent"); 10,734,481 ("the '481 patent"); 11,121,222 ("the '222 patent"); and 11,316,014 ("the '014 patent") (collectively, "the Patents-in-Suit" or "the Asserted Patents" or "Dr. Rao's patents").

3. I receive compensation at an hourly rate of $700 per hour for my time working on technical consulting in this matter, plus expenses. I have no financial interest in Greenthread or in the patents involved in this litigation, and my compensation is not dependent on the outcome of this litigation. The conclusions I present are due to my own judgment.

II. BACKGROUND AND QUALIFICATIONS

4. I am a Professor of Chemical Engineering at the California Institute of Technology ("Caltech"). I have held that position since 1992. My research relates to processing of semiconductors, dielectrics, and metals, as performed in the fabrication of semiconductor devices, including microprocessors and digital memories. In particular, my work has focused upon patterning layers of electronic materials to fabricate sub-micron features such as transistor gates, vias, and metal lines found in VLSI circuits. I have also conducted modeling and simulations of the evolution of poly-silicon and metal gate profiles subjected to plasma etching and studied their charging interactions with plasmas. Since the start of my graduate career in 1985, I have

accumulated over 35 years of experience on semiconductor materials, devices, and their processing.

5. In my professorial duties at Caltech, I have developed and taught new undergraduate and graduate level courses on semiconductor device physics and their processing. These innovative courses combined solid state physics and electronic materials processing technologies with the more traditional chemical engineering subjects of transport phenomena and chemical thermodynamics. The courses have prepared several generations of students for successful careers in the semiconductor industry.

6. During my research career, I have authored or co-authored 98 peer-reviewed papers, 12 refereed conference proceedings, and two book chapters. Most of my publications relate to semiconductor device processing. My papers on charging damage of high-density integrated devices such as microprocessors, and digital memories are highly cited. I have also been granted 13 patents.

7. My curriculum vitae is provided as Appendix A to this Declaration

III. SCOPE OF ASSIGNMENT AND MATERIALS CONSIDERED

8. I have been retained by Greenthread to provide an explanation to the Court regarding the inventions described in the Patents-In-Suit. I understand that the patents have been asserted by Greenthread against Defendants in this proceeding. I have also been retained to provide my opinion regarding the meaning of certain terms to persons of ordinary skill in the field of the inventions and to address certain issues of claim indefiniteness alleged by the Defendants.

9. In preparing this Declaration, I am relying on my own knowledge and expertise as well as the following documents:

- The Patents-In-Suit:
    - U.S. Patent No. 8,421,195 to Dr. G.R. Mohan Rao ("the '195 patent);
    - U.S. Patent No. 9,190,502 to Dr. G.R. Mohan Rao ("the '502 patent");
    - U.S. Patent No. 10,510,842 to Dr. G.R. Mohan Rao ("the '842 patent");

  - U.S. Patent No. 10,734,481 to Dr. G.R. Mohan Rao ("the '481 patent");
  - U.S. Patent No. 11,121,222 to Dr. G.R. Mohan Rao ("the '222 patent"); and
  - U.S. Patent No. 11,316,014 to Dr. G.R. Mohan Rao ("the '014 patent");
- Prosecution histories for the Patents-In-Suit, which I understand constitute the exchange of correspondence between the Patent Office and the applicant;
- Petitioner Samsung Electronics Co., Ltd. ("Samsung")'s petitions for *inter partes* review, Nos. IPR2021-00289 and -00290 regarding the '195 and '502 patents, the declarations of Dr. Bruce Smith submitted in support thereof, and Greenthread's preliminary responses in those IPRs;
- Defendants' Opening Claim Construction Brief (Dkt. 82)[2] and exhibits to that brief
- Greenthread's extrinsic evidence disclosure statement (September 26, 2022), Greenthread's supplemental extrinsic evidence disclosure statement (October 6, 2022), Defendants' extrinsic evidence disclosure statement (September 26, 2022), Defendants' supplemental extrinsic evidence disclosure statement (October 10, 2022), and extrinsic evidence cited in those statements;
- The exhibits listed in the Table of Exhibits at the beginning of this Declaration; and
- The other references cited within this Declaration.

IV. PERSON OF ORDINARY SKILL IN THE ART (POSITA)

10. When interpreting a patent, I understand that it is important to view the disclosure and claims of that patent from the level of ordinary skill in the relevant art at the time of the invention. My opinion of the level of ordinary skill in the art with regard to the Patents-in-Suit is based on my personal experience working and teaching in the field of semiconductor processing, including work with semiconductor technologies, my knowledge of the background and education

[2] In this Declaration, I cite to certain documents as "Dkt. XXX" where XXX indicates what I am informed is the docket number of such documents on this case's court docket. Regarding such documents, my cites to specific page numbers refer to the page numbers stamped in blue in the header at the top right of each page in the format "Page __ of __."

of colleagues and others working in that general field as of and for several years prior to the 2002 to 2004 time frame, my study of the Patents-in-Suit, and their file histories, and my knowledge of:

- The level of education and experience of persons actively working in the field at the time the subject matter at issue was developed;
- The types of problems encountered in the art at the time the subject matter was developed;
- The prior art patents and publications;
- The activities of others working in that same technical field;
- Prior art solutions to the problems addressed by the relevant art; and
- The sophistication of the technology at issue in this case.

11. In determining the level of ordinary skill in the art, I also considered the following factors: (1) the sophistication of the relevant technology; (2) the rapidity with which innovations are made in that field; and (3) the educational level of active workers in that field. It is my further understanding that these factors are not exhaustive and are merely a useful guide to determining the level of ordinary skill in the art.

12. Taking the above factors into account, in my opinion a POSITA in the technology field of the Patents-in-Suit would be a person with at least a Bachelor's of Science degree in electrical or computer engineering, materials science, chemical engineering, applied physics, or a related field, with emphasis on semiconductor manufacturing, or an equivalent degree, and at least four years of experience in semiconductor design and manufacturing. Additional education in a relevant field, or industry experience may compensate for a deficit in one of the other aspects of the requirements stated above.

13. I understand that Defendants' expert in this proceeding, Dr. Scott Thompson, has stated a different characterization of a POSITA. Dkt. 82-26 (Declaration of Dr. Scott Thompson), ¶2 ("[A] person of ordinary skill in the art at the time of the Asserted Patents would have had a Bachelor's degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work

experience. This description is approximate, and a higher level of education or skill might make up for less experience, and vice-versa."). I agree with his characterization, as chemical engineering is a related field in this context. I was at least a POSITA as of September 3, 2004, which I understand is the filing date of U.S. Application No. 10/934,915, to which the Patents-in-Suit claim priority.

14. My opinions regarding claim construction for the claim terms in dispute in this proceeding are based on the relevant knowledge and skillset of a POSITA for the Patents-in-Suit.

V. GENERAL BACKGROUND OF THE RELEVANT TECHNOLOGY AND THE PATENTS-IN-SUIT

A. Dopants

15. Silicon is an example of a semiconductor. In its pure form it is typically an insulator but it can become a conductor of electricity when impurities called "dopants" are added into the silicon crystal. These dopants are usually phosphorous or boron atoms that have one more or one fewer valence electron than the silicon atom, respectively. If the dopant has one more valence electron than silicon, that electron is available for electronic conduction in the silicon. If the dopant has one fewer valence electron than silicon, then it creates what is called a "hole," which is a positive unit of charge. Such holes are conventionally assumed to be capable of conducting positive current through the silicon. Thus, electric charge in semiconductors is thought to be carried by both electrons and holes, which are then referred to as "charge carriers."

16. The extra electrons or holes in a doped region of silicon disturb the local charge equilibrium and they can create local electric fields, which will influence the motion of other charge carriers passing by. This phenomenon is called "carrier drift." Ex. 12, 38-39. When the dopant concentration is graded in a particular direction, the ensuing electric field points in the direction of the gradient and, thus, charge carriers will also drift in the gradient direction or opposite to it depending on the charge carrier's polarity. *Id.*, 103-106.

B. Overview of Dr. Rao's Inventions

17. At the time of Dr. Rao's inventions claimed in the Patents-In-Suit, most semiconductor devices relied on uniform concentrations of dopants. Ex. 2 (195 patent), Abstract; 1:36-40, 50-51. Dr. Rao recognized that graded concentrations of dopants can be used to improve the performance of transistors and other semiconductor devices. *Id.*, Abstract; 3:3-13, 33-35. Dr. Rao's invention is clearly disclosed in Figures 5B and 5C of his patents, and the corresponding parts of the specification.

18. A surface-channel MOSFET is a well-known type of transistor that is capable of controlling current flow at or along the surface of the semiconductor substrate. Dkt. 82-16 (Wolf Vol 2), 5-6; Ex. 4 (Chen), 27 ("carriers propagate slightly under the semiconductor surface"). The current flow occurs in a thin layer of silicon near the surface, called the "channel", located between two terminals called the source and the drain. MOSFETs come in two flavors, NMOS and PMOS, depending on whether the current flow is based on electrons or holes, respectively. The carrier type in channel conduction requires oppositely doped silicon regions to build the transistors in, specifically, p-type for NMOS, and n-type for PMOS.

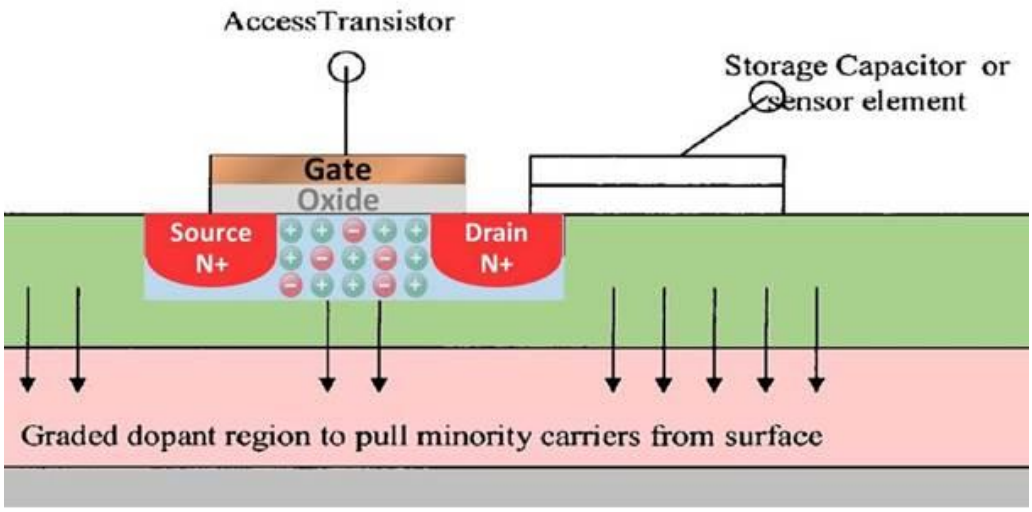
19. MOSFETs are built in active regions, defined on the wafer surface by isolation regions. Ex. 13, 327 (Wolf Vol 2) ("Active region and field region definitions"). Since the substrate is typically doped either n-type or p-type, only one kind of devices can be built on a typical substrate. When both NMOS and PMOS transistors are used in complementary metal oxide semiconductor (CMOS) applications, isolated regions of opposite type dopant than present in the starting material are created within a substrate called "wells." Dkt. 82-16, 17-20. The corresponding transistor is then built in a surface layer located in the upper part of the well. In specialized CMOS applications, wells are created in a substrate for both NMOS and PMOS transistors, known as "twin-wells." Ex. 13, 387-389. Sometimes, wells within wells of the opposite dopant type are used for better isolation from the substrate.

20. Conventional wells are formed by implanting dopants and then diffusing them to the desired depth. However, diffusion occurs laterally as well as vertically, which increases the width of the well and reduces packing density. This problem is avoided by using high energy implants to place the dopants at the desired depth without further diffusion. Such deeply implanted wells are known as "retrograde wells". The retrograde doping profile is different from the conventional uniform or downward sloping profile: the impurity concentration decreases as it approaches the wafer surface. Ex. 13, 389; Ex. 14, 531.

21. Figure 5B of the 195 patent, annotated below, shows an n-channel MOS (NMOS)[3] transistor that is formed in a p-type surface layer of silicon. The transistor comprises (1) a gate; (2) a thin oxide separating the gate from the surface layer; and (3) two doped regions called the source and drain (shaded red). Ex. 2, 3:10-11 ("electrons can be swept from source to drain"); 3:42-43 ("accelerate majority carriers towards the drain"). In Fig. 5B, the N+ means that these regions are heavily doped with an n-type dopant that creates a surplus of negative carriers (*i.e.*, electrons).[4] The specification explains that the NMOS transistor in Fig. 5B can be a surface-channel MOSFET. Ex. 3:41-43.

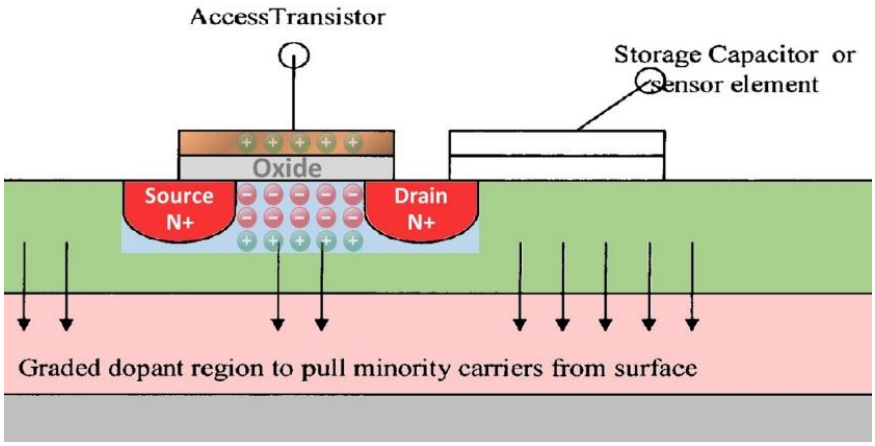
[3] MOS stands for "metal oxide semiconductor." It refers generally to **m**etal and **o**xide layers that are formed on top of a **s**emiconductor (*e.g.*, silicon). In some MOS devices, the metal is replaced with another conductor such as doped polysilicon. Ex. 4, 10.

[4] A helpful way to understand the dopants is that an "N" region or layer will have more electrons, and thus an abundance of "**n**egative charge carriers." A "P" layer will have more holes, and thus an abundance of "**p**ositive charge carriers." The "+" or "-" refers to the amount of doping. A "+" means heavily doped; "-" lightly doped.



Ex. 2, Fig. 5B (annotated). Meanwhile, the p-type silicon between the source and drain (shaded blue) has an abundance of positively charged holes (green circles). Electrons are still present in the silicon, but the overwhelming majority of the carriers are holes.

22. In the simplest terms, an NMOS transistor switches between two states, ON and OFF. With no bias applied on the gate, electron conduction between source and drain is not possible in the arrangement described above with a p-type silicon between the N+ source and drain terminals. The transistor is described as being in the OFF state. When a positive voltage is applied to the gate, an electric field forms in the oxide, which extends further into the silicon below the oxide. This electric field perturbs the local charge equilibrium: it repels the holes away from the oxide, while it attracts electrons (red circles) closer to the oxide. When enough electrons have accumulated in the surface layer of silicon below the oxide, they form a conductive channel for electrons between the source and the drain, and current can begin to flow through the transistor. Current flow through the transistor corresponds to the transistor turning ON.



Ex. 2, Fig. 5B (annotated)[5] In order to turn the transistor OFF, the positive voltage is removed from the gate, causing the conductive channel of electrons to vanish as the holes return to the surface layer.

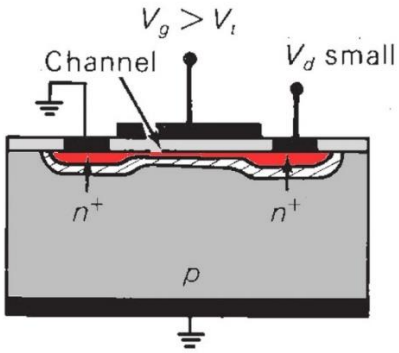
23. The term "well region" describes typically the doped silicon that surrounds the source and drain. Since wells are totally isolated from the substrate, well contacts are made to control the potential of each well. Ex. 14, 523 ("When wells are present, however, the well regions must also be connected to the appropriate circuit voltages….").

24. Dr. Rao recognized that by using graded concentrations of dopants in the well region and a drift layer (shaded pink), it is possible to "pull" carriers from the silicon's surface. In this example, pulling the repelled holes further away from the surface layer when a positive voltage is applied to the gate, allows the transistor to turn "on" more quickly. This improves the speed and performance of the transistor. Ex. 2, 3:8-13.

25. As its name suggests, the channel in a surface channel MOSFET forms at or along the surface. But it is slightly more complicated that. As shown in the well-known figure below, the n-channel starts at the source (on the left) and expands towards the drain (on the right) as the

[5] Because the channel is formed by electrons with a **n**egative charge, the MOSFET is referred to as an **n**-channel MOSFET. In an n-channel MOSFET, the electrons are referred to as the "majority carriers," and the "minority carriers" are holes.

voltage applied to the gate increases. There is a thin layer below the surface (shaded red) where the channel actually forms. The cross-hatched region underneath is known as the depletion region.



Ex. 4, 19 (shaded). As shown above, the n-channel does not actually form on the surface but rather in the layer just below the surface (*i.e.*, the surface layer).

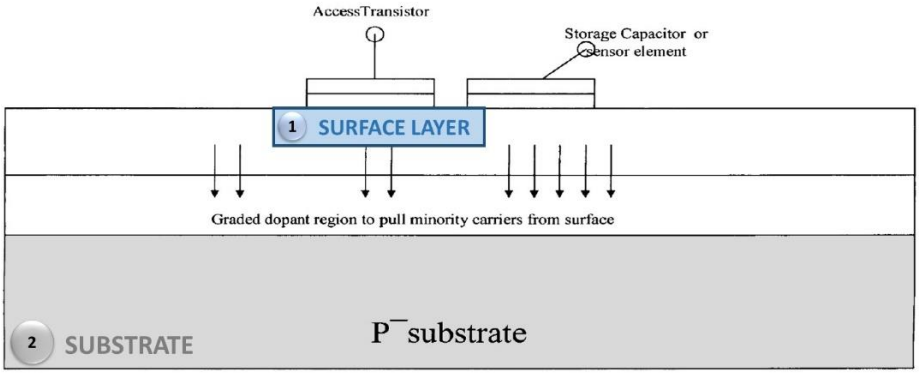
C. Exemplary Claim 1 of the '195 Patent

26. Six of the seven disputed claim terms can be found in exemplary claim 195:1. These six claim terms are numbered and color coded below.

Term	U.S. Patent No. 8,421,195, Claim 1 (195:1)
1	A CMOS Semiconductor device comprising: a **surface layer**;
2	a **substrate**;
3	an **active region** including a source and a drain, disposed on one surface of said surface layer;
4 5	a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static **unidirectional electric drift field** **to aid the movement of minority carriers from said surface layer to said substrate**; and
6	at least one **well region** disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

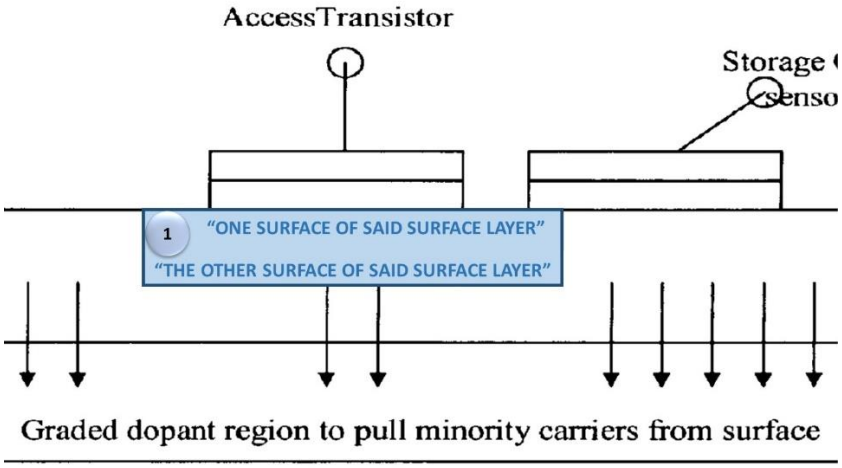
27. I am informed that Defendants contend that certain claim terms render claim 1 of the '195 patent indefinite. In my opinion, far from being indefinite, claim 1 lines up exactly with Fig. 5B and the corresponding parts of the specification. Fig. 5B confirms what is meant by each claim term. As the preamble states, Fig. 5B illustrates a CMOS semiconductor device with metal and oxide layers on a silicon substrate. Ex. 2, 2:27-31; 3:41-43. The specification mentions verbatim that the CMOS device may be a surface channel MOSFET. *Id.*, 3:41-43; *see also* 1:43-45.

28. As seen below, the CMOS semiconductor device comprises a surface layer (blue) and a substrate (gray). *Id.*, 3:30-45. The substrate is lightly doped with holes (P-), and the surface layer is a layer at the surface of the silicon. As explained below, the invention is concerned with moving minority carriers from this surface layer to the substrate.



Ex. 2, Fig. 5B (annotated).[6]

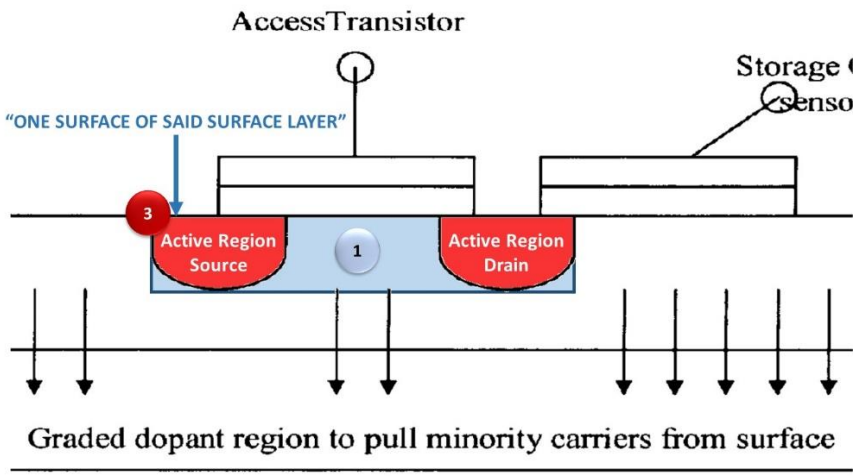
29. The surface layer has at least two surfaces, which claim 195:1 refers to as the "one surface of said surface layer" and "the other surface of said surface layer."



Ex. 2, Fig. 5B (annotated); *id.*, 4:16-19.

30. Next, the claim specifies an active region with a source and drain. *Id.*, 4:16-17. Figure 5B shows how the active region is "disposed on one surface of said surface layer."

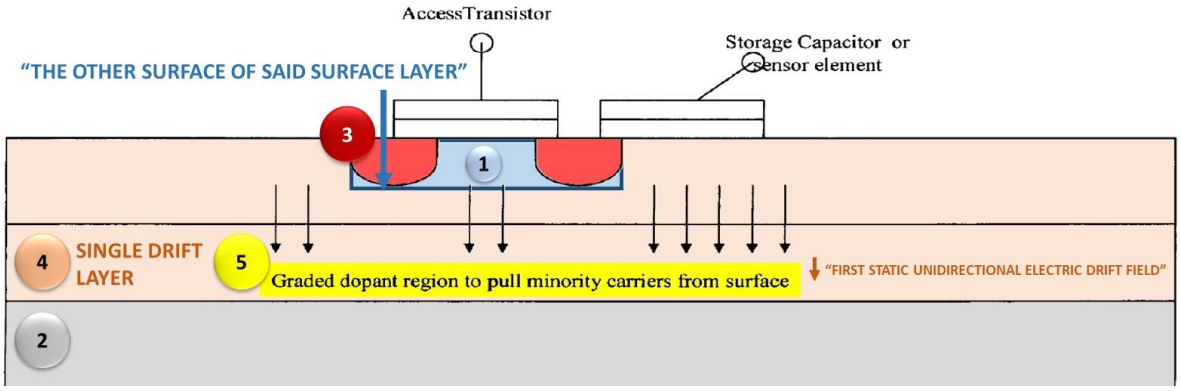
[6] As explained below, "substrate" is a relative term, and Dr. Rao sometimes used it to refer to the bottom layer, and other times he used it to refer to the wells that are underneath the surface layer and active region. In both cases, the "substrate" is an "underlying layer."



Ex. 2, Fig. 5B (annotated).

31. The "active region" is a doped region where a transistor or other active device can be formed. Ex. 2, 1:61-63; 2:18-23; 3:1-3, 30-33. As explained below, Dr. Rao contemplated that the CMOS device may have multiple active regions where transistors are formed in some, but not all of the active regions.

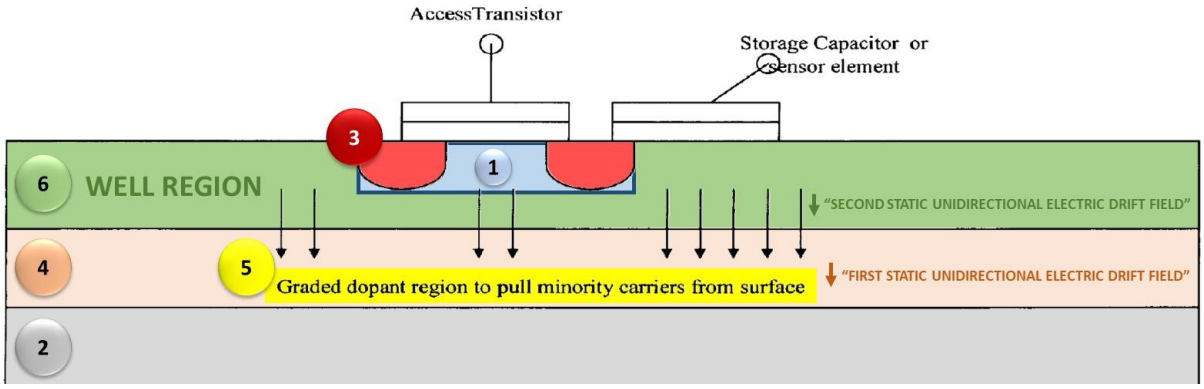
32. Next, the claim specifies there is a single drift layer disposed between "the other surface of said surface layer" and the substrate. This single drift layer has a graded concentration of dopants.



Ex. 2, Fig. 5B (annotated).

33. The graded dopants create an electric field that aids the movement of minority carriers (holes in the case of the n-channel example shown in Fig. 5B) from the surface layer to the substrate. Ex. 2, 3:17-20, 30-37.

34. Finally, the claim specifies there is a well region disposed in the single drift layer, and this well region creates a second electric field that also aids the movement of minority carriers. The specification teaches the retrograding in dopants in the p-well to sweep those carriers away from the surface as well.



Ex. 2, Fig. 5B (annotated); *id.*, 2:27-28; 3:37-40.

D. Exemplary Claim 1 of the '842 Patent

35. According to claim 1 of the '195 patent, the "active region" includes the heavily doped regions called the "source" and the "drain." Exemplary claim 1 (below) of the '842 patent sheds additional light on the "active region" when it specifies the "active region" is a region "within which transistors can be formed."

Term	U.S. Patent No. 10,510,842, Claim 1 (842:1)
8	A semiconductor device, comprising: a substrate of a first doping type at a first doping level having first and second surfaces; a first **active region** disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and **within which transistors can be formed**; a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed; transistors formed in at least one of the first active region or second active region; and at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate.

36. According to claim 842:1, there may be multiple active regions (*i.e.*, the first and second active regions), where a transistor is formed in at least one of them (*i.e.*, transistors formed in at least one of the active regions). Ex. 3, 4:48-56.

VI. APPLICABLE CLAIM CONSTRUCTION LEGAL STANDARDS

37. I understand that the parties do not agree on the meanings of several terms and phrases in the claims of the Patents-In-Suit, and that it is the role of the Court to resolve these disputes. I have reviewed Defendants' positions as summarized in Defendants' Opening Claim Construction Brief (Oct. 10, 2022) (Dkt. 82), and Greenthread's positions as summarized in the "Disputed Claim Constructions" table at the beginning of this Declaration. I agree with the positions taken by Greenthread for each such term or phrase. In my opinion, Greenthread's claim construction proposals reflect how persons of ordinary skill in the field of semiconductor processing would interpret the disputed claim terms.

38. I am not an attorney. Counsel for Greenthread provided me with a set of legal standards to apply to claim construction. These standards, which I applied in forming the opinions expressed in this Declaration are summarized below.

39. The patent claims describe the invention made by the inventors, what the patent owner owns, and what the owner may prevent others from doing. An independent claim sets forth all the requirements that must be met in order to be covered by that claim. A dependent claim refers to another claim and incorporates all of the requirements of the claim to which it refers.

40. The claim terms are given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art at the time of the invention. The person of ordinary skill is considered to read the words used in the patent documents with an understanding of their meaning in the field, and to have knowledge of any special meaning and usage in the field. The ordinary meaning of a claim term is its meaning to the person of ordinary skill after reading the entire patent, including the patent specification. The specification may reveal a special

definition given to a claim term by the inventor, which then governs the meaning of the same term in the claims.

41. The claims themselves provide substantial guidance as to the meaning of claim terms, and the context in which a term appears in the claim can be highly instructive to its meaning. Difference among claims can also be a useful guide. For example, the presence of a dependent claim that adds a particular limitation suggests that the limitation in question is not present in the independent claim to which the dependent claim refers.

42. The patent's prosecution history should also be considered, which includes the record of the proceedings before the U.S. Patent and Trademark Office ("USPTO") and the prior art cited during the examination of the patent. The prosecution history may inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution or post-grant proceedings at the USPTO, making the claim scope narrower than it would otherwise be.

43. I have been informed that the test for indefiniteness is whether the claims, viewed in light of the specification and prosecution history, inform those skilled in the art about the scope of the invention with reasonable certainty.

44. My opinions regarding the meaning that a person of ordinary skill in the art would give to the disputed claim terms are addressed below.

VII. MEANING OF CLAIM TERMS TO PERSONS OF ORDINARY SKILL

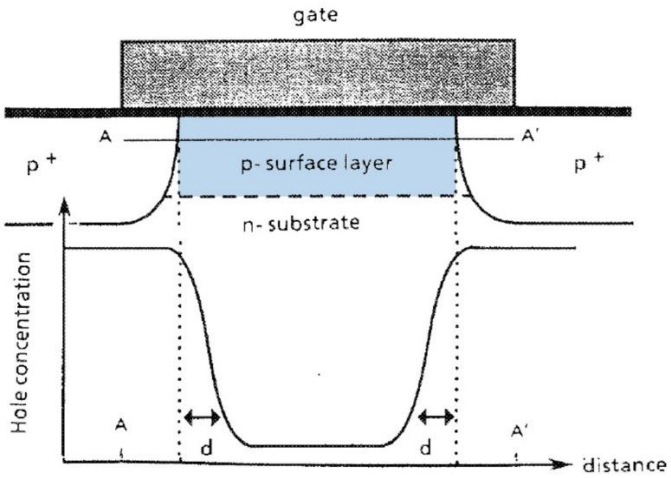
45. If I do not specifically respond to a statement made in Defendants' brief or expert declaration, that does not indicate agreement on my part.

A. Claim Terms Found in Exemplary Claim 195:1

1. "surface layer" terms[7] (195:1; 502:7; 222:44)

Greenthread	Defendants
Plain and ordinary meaning, where the plain and ordinary meaning of "surface layer" is "a layer at the surface"	Indefinite

46. I understand that Defendants contend that the "surface layer" terms are indefinite. In my opinion, these terms are not indefinite. "[S]urface layer" is a lay term that is understood by skilled artisans and lay people alike. Whether it is the surface layer of the ocean, skin, soil in a backyard garden, or a semiconductor device, it is referring to the same thing: a layer at the surface. Even the Wolf textbooks cited by Defendants show that a "surface layer" is a layer at the surface of the semiconductor device where the active region is located.



Dkt. 82-17 (Wolf Vol. 3), 11 (annotated; describing MOSFET with source and drain); Dkt. 82-18 (Wolf Vol. 4), 7, 10 (describing the "surface layer" of the MOSFET as the doped silicon near surface of the silicon).

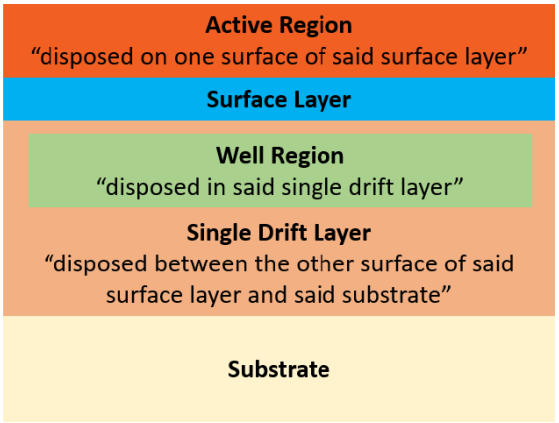
47. Defendants' indefiniteness arguments are incorrect, in my opinion, because (1) they ignore the realities of surface-channel MOSFETs and the preferred embodiment disclosed in Figure 5B, and (2) they wrongly assume the surface layer is "disposed ***under*** the active region."

[7] These are the terms collectively numbered as term 1 in the table above in the "Disputed Claim Constructions" section of this Declaration.

See Dkt. 82, 14 (emphasis in original). The claims do not use the words "disposed under." The claims, specification, and prosecution history show that the "surface layer" is the layer at the surface of the silicon. This is not surprising given this is how the term is normally used in the art.

48. The claim language shows that the "surface layer" is a layer at the surface of the semiconductor device. First, a POSITA would readily understand that a "surface layer" is a layer at the surface of the semiconductor device. This is because it is customary in the field of semiconductors to refer to layers by their relative position in the stack of layers. In other words, a "bottom layer" would be at the bottom; a "middle layer" at the middle; and a "surface layer" at the surface. Defendants do not contend that it is unclear what is meant by the "surface" of a CMOS semiconductor device. It is the doped silicon where the active region is located, and where the channel forms in a surface-channel MOSFET. Therefore, a POSITA would have understood that a "surface layer" is a layer at the surface of the semiconductor device.

49. The claim specifies that the "surface layer" has two surfaces and that the "active region" is "disposed on one surface of said surface layer." From this claim language, Defendants have interpreted various claim terms to be arranged with respect to one another as shown below at left.

Defendants' Interpretation	Correct Interpretation
	

Dkt. 82, 11.

50. Defendants' rendering ignores that the "active region" is part of the "surface layer," just like the "well region" is part of the "single drift layer." When the claim says the "active region" is "disposed on one surface of said layer," it is not saying it is a separate layer on top of the "surface layer." Rather it is specifying where in the "surface layer" the "active region" is located. The "active region" occupies a volume of silicon in the "surface layer." Instead of being anywhere in the surface layer, the "active region" is disposed on the top surface of the surface layer, as shown in the right hand column above.

51. By analogy, if a room has two surfaces—a floor and a ceiling—and a ceiling fan is disposed on the ceiling of the room, it does not mean the ceiling fan is spinning around like a propeller on the roof of the house. Instead it means that the ceiling fan is hanging from the ceiling ***inside*** the room. The same is true about the active region and the surface layer. When the claim says the active region is "disposed on one surface of the surface layer," it means the active region is located on the "ceiling" of the silicon ***inside*** the silicon. The claim never says the "surface layer" is "disposed ***under*** the active region," as Defendants claim in their brief. *See* Dkt. 82, 14.

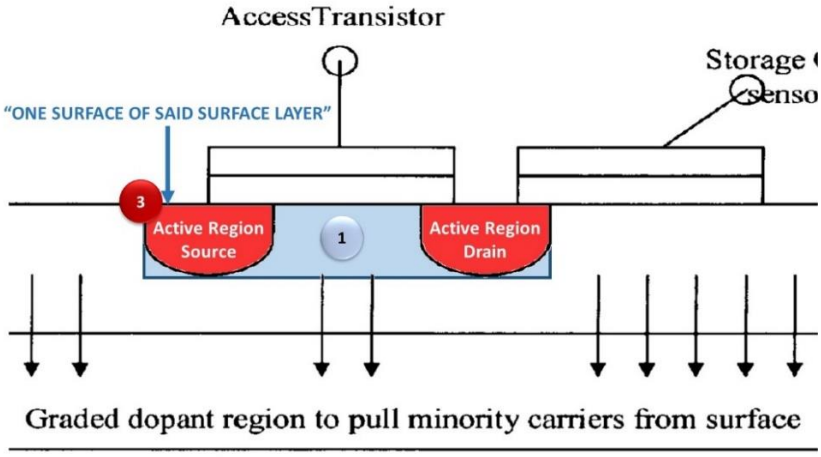
52. The claim specifies that the "active region" includes a source and drain. A POSITA would have realized that these doped silicon regions have to be part of the surface layer beneath the silicon's surface. Otherwise they could not be used to form a transistor.

53. The specification further shows that the "surface layer" is a layer at the surface. Defendants do not appear to dispute what is meant by the "surface" of the CMOS semiconductor device. In my opinion, this is a term that a POSITA would have understood to mean the surface of the silicon where the source and drain are located. This is how the term "surface" is consistently used throughout the specification and the figures. *See, e.g.*, Ex. 2, 1:43-45 (explaining that MOS devices are majority carrier devices and "the channel can be a surface in one plane in planar devices"); 3:30-33 (explaining how Dr. Rao's invention sweeps unwanted minority carriers "from the active circuitry at the surface"); 3:38-43 (explaining how graded dopants "sweep those carriers away from the surface" and that Dr. Rao's invention may be used "in surface channel MOS devices to accelerate majority carriers towards the drain"); 3:43-45 (explaining that when programming

nonvolatile memory devices, "carriers should be accelerated towards the surface"); 3:53-55 (explaining that "minority carriers can be channeled to the surface"); Fig. 5A ("Graded dopant region to pull minority carriers from surface"); and Fig. 5B ("Graded dopant region [a]ccelerates carriers towards surface during programming"). In every single instance, the specification is referring to the surface layer at the surface of the semiconductor device where the active region is located.

54. A POSITA would have known that the carriers-of-interest are actually in the thin layer of silicon just below the silicon's surface (i.e., the "surface layer"). Armed with this knowledge, the term "surface" is frequently used as a shorthand for "surface layer." While POSITA would have known what is meant by carriers "at the surface," it is actually more precise to refer to them as carriers "in the surface layer," like the Wolf textbooks do. Dkt. 82-17, 11; Dkt. 82-18, 7, 10.

55. Turning back to the preferred embodiment shown in Figure 5B, the corresponding surface layer is also shown in blue. We know from the surrounding claim language that the source and drain are disposed on "one surface of the surface layer."



Ex. 2, Fig. 5B (annotated).

56. When the specification refers to a surface channel MOSFET, the channel forms at or along the upper surface of this blue region. Furthermore, when the specification refers to "pull[ing] minority carriers from surface" or "accelerat[ing] minority carriers towards the surface," it is referring to this same blue area where the channel forms. Therefore, the specification

consistently shows that the "surface layer" is a layer at the surface of the semiconductor device where the active region is located.

57. Defendants' interpretation of the claim (*i.e.*, surface layer disposed ***under*** the active region) would exclude the preferred embodiments in Figure 5B.

58. The prosecution history further shows that the surface layer is the top layer of the silicon. During prosecution of the application that eventually issued as the '195 patent, the Applicant elected claims directed to the embodiment shown in Figures 5B and 5C. Dkt. 82-8 (195 file history), 49. These claims, which were part of the original priority application, referred to the "active surface regions." *Id.*, 9. Applicant subsequently amended the claims to change "surface region" to "surface layer," and specified that the "active region" is "disposed on one surface of said surface layer." *Id.*, 165. In the next office action, the Examiner asserted that reference 23 in Fig. 2 of Kamins is a "surface layer." *Id.*, 183; Dkt. 82-10 (Kamins), 3. Notably, the Examiner identified the layer at the surface of the silicon as the "surface layer," and not the oxide layer on top of the silicon. This shows that the Examiner understood the "surface layer" to be a layer at the surface of the silicon.

59. In my opinion, the Wolf textbooks cited by Defendants show how the term "surface layer" was ordinarily used in the art. Dkt. 82-17, 11; Dkt. 82-18, 7, 10. A POSITA would have known that "surface" was (and still is) often used as a shorthand for "surface layer." While the specification may not expressly use the words "surface layer," the specification fully describes the layer at the surface of the semiconductor device where the active region is located, and the channel that is formed in a surface channel MOSFET. *See, e.g.*, Ex. 2, 1:43-45; 3:30-33, 38-45, 53-55; Figs. 5A-B. The Wolf textbooks show that this layer is referred to as a "surface layer." Dkt. 82-17, 11; Dkt. 82-18, 7, 10. Therefore, the specification does, in fact, disclose a surface layer.

60. Defendants rely on four volumes of Wolf textbooks to argue that in some contexts the term "surface layer" is used to refer to an oxide or other non-silicon layer. Dkt. 82, 6-7. But then Defendants state that in the MOSFET context, the term "surface layer" is used to refer to the

layer at the surface of the silicon where the active region is located. *Id.*, 7. This is exactly how the term is used in the preferred embodiment in the Asserted Patents.

61. Defendants argue that surface layer cannot mean "layer at the surface" because the claim language "paradoxically require[s] the '***surface*** layer' to be disposed ***under*** the active region." Dkt. 82, 14. In my opinion, that argument is incorrect. The claims make clear that the active region is part of the surface layer and there is nothing in the claim that says otherwise.

62. Defendants argue that there is no discernible structure or boundaries for the "surface layer." Dkt. 82, 15. But the Wolf textbooks show how the term is ordinarily used in the art, and this is how the term is consistently used in the preferred embodiment and throughout the intrinsic record.

63. In an IPR filed by Samsung against the '195 patent (*see* Dkt. 82-19, 13), Samsung's expert recognized that "the term most related to 'surface layer' found in the specification is 'surface.'" Ex. 6 (Dr. Smith Declaration), ¶ 46. Dr. Smith went on to opine that:

> FIG. 5(b) in combination with the various descriptions of a 'surface' in the '195 Patent specification appear to suggest that ***the "surface layer" may correspond to a region at and along a portion of the surface of the CMOS device, as its ordinary meaning would also suggest***. For instance, the Oxford Dictionary defines a "surface" as being the "outside of a body" or "any of the limitation that terminate a solid," and a "layer" as a "thickness of matter." Thus, my understanding of how the '195 Patent utilizes the term "surface layer is consistent with the ordinary understanding of "surface" and "layer."

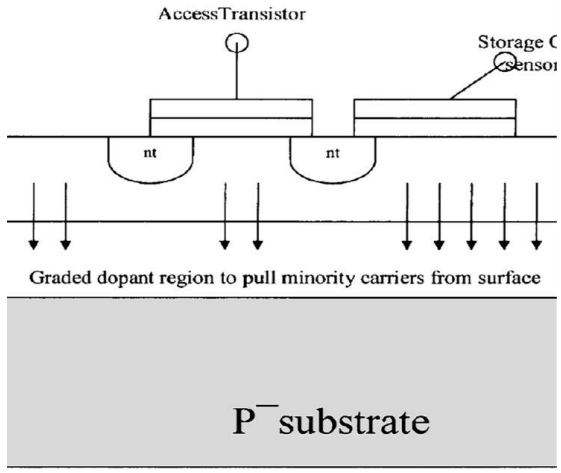
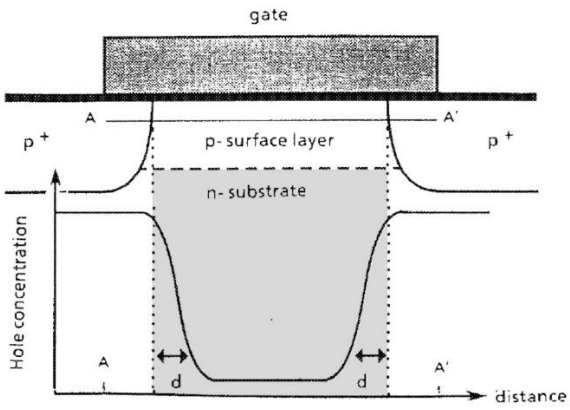
Id., ¶ 49 (emphasis added, citation omitted). The fact that Samsung's expert was able to determine what is meant by "surface layer" is consistent with my opinion that the term is not indefinite.

2. "substrate" (195:1; 502:7; 842:1, 9; 481:1, 20; 222:1, 21, 39, 41, 42, 44; 014:1, 21)

Greenthread	Defendants
Plain and ordinary meaning, where the plain and ordinary meaning is "an underlying layer"	"the initial material within which or on which the semiconductor device is fabricated

64. In my opinion, "substrate" is a term that is readily understood by a POSITA. A substrate is simply an "underlying layer." *See* Ex. 7 (American Heritage Dictionary) (defining "substrate" as "an underlying layer"); Ex. 8 (Webster's Dictionary) (explaining that "substrate" is synomous with its latin origin "substratum," which means "underlying structure, layer, or part"). This is how the term is consistently used in the claims, specification, and prosecution history. This term does not require construction.

65. In Fig. 5B, the "P- substrate" (shaded gray) is an "underlying layer." In the Wolf textbook, the "n- substrate" (shaded gray) is also an "underlying layer." Dkt. 82-17, 11. This is how the term "substrate" is ordinarily used in the art.

195 Patent, Fig. 5B	Wolf
	

Ex. 2, Fig. 5B; Dkt. 82-17, 11.

66. There is nothing in the intrinsic record that departs from the term's plain meaning. Every time "substrate" is used in the specification or prosecution history, it is merely referring to an "underlying layer." Ex. 2, 1:50, 62 ("twin well substrate"); 2:18-23, 27-28 ("a MOS silicon

substrate with two wells, and, an underlying layer"); 3:31-32 ("sweep these unwanted minority carriers into the substrate"); 3:35 ("deep into the substrate"); Figs. 2, 3A-D, 4, 5A-C (all showing substrate as an underlying layer).

67. Defendants state that the claims require a substrate, active region, well region, drift layer, and surface layer. This part is true. But then Defendants contend that these structures must be formed in a particular order with the substrate being the "initial" layer, and the other structures being "subsequent" structures. Dkt. 82, 6. But claim 195:1 never says the substrate has to be made first. In fact, the specification specifically teaches that "[d]ifferent layers of dopan[t] regions can be transferred through wafer to wafer bonding (or other similar transfer mechanisms) for eventual device fabrication." Ex. 2, 3:1-3; *see also* 3:35-37 ("One or more of such layers can also be implanted through wafer to wafer bondings or similar 'transfer' mechanisms."). Therefore, a POSITA would have understood that the specification contemplates that the substrate could be fabricated ***after*** the other layers and bonded to the other layers when the device is actually fabricated.

68. Furthermore, Defendants' brief implies that the substrate and other structures must be mutually exclusive. While each of the structures must be present in the claimed device, the claim never says the well region and drift layer cannot be part of the substrate. In fact, the specification says the opposite when it specifically mentions a "MOS silicon substrate with two wells, and the underlying layer." Ex. 2, 2:27-28. In this scenario, the two wells and underlying layer can all be part of the substrate.

69. Defendants misquote the following sentence to argue that the claimed substrate must be the initial material, and the substrate must be different from the wells, layers, and transistor. Dkt. 82, 9. The full sentence reads: "FIG. 3(a) shows a typical CMOS VLSI device employing a twin well substrate, on which active devices are subsequently fabricated." Ex. 2, 1:61-63. This sentence is referring to a prior art figure that is not claimed. The sentence does not say that in the claimed invention the substrate ***must be*** fabricated before the other layers. Furthermore, the specification expressly says the layers can be individually formed and

subsequently bonded together. *Id.*, 3:1-3, 35-37. Finally, this sentence does not say the substrate is different from the wells and other layers. In fact, it says the opposite. More specifically, it says the substrate is a "twin well substrate," which means the two wells are part of the substrate (*i.e.*, the underlying layer on which the active devices are subseqently fabricated).

70. Defendants cite other references to argue that the initial substrate ***can be*** a "uniformly doped 'bulk' silicon substrate." Dkt. 82, 17. But the 195 specification specifically teaches that (1) the substrate can be a twin-well substrate, which means that it is not uniformly doped; and (2) the layers may be separately formed and then bonded together. Ex. 2, 1:61-63; 3:1-3, 35-37.

3. "active region" (195:1; 502:7; 842:1, 9; 481:1, 20; 222:1, 21, 39, 41, 42, 44; 014:1, 21)

Greenthread	Defendants
Plain and ordinary meaning	"region that forms the current path of a device"

71. In my opinion, "active region" is a term that a POSITA would have readily understood. A POSITA reading the claims and intrinsic record would have understood that an active region is an isolated doped silicon region at the surface of a semiconductor device where a transistor can be formed. This is how the term is used in the relevant claims and throughout the intrinsic record. There is no need to construe the term, and to do so would only introduce ambiguity where there is none.

72. Claim 842:1 states there are two active regions—a "first active region" and a "second active region"—and that transistors are formed "in at least one of the first active region or second active region." Ex. 3, 4:48-56. This means that some, but not necessarily all, of the active regions will form a transistor. If the active region does not form a transistor, then the active region will not necessarily form the current path of a device.

73. To form, for example, a CMOS transistor in an active region, a number of things must be true. *First*, there must be an oxide layer on top of the doped silicon. *Second*, a metal or other conducting layer must be on top of the oxide layer to form a gate. *Third*, the source and drain regions must be implanted with dopants and annealed. *Fourth*, terminals must be connected

to the source, drain, and gate. *Finally*, a sufficient voltage must be applied to the gate to turn the transistor "on." Dr. Rao contemplated that the transistors may be formed later. Ex. 2, 1:61-63; 2:18-23 ("subsequently fabricated"); 3:1-3 ("for eventual device fabrication"). Therefore, Defendants' construction would exclude a preferred embodiment.

74. Defendants cite to extrinsic evidence where the term active region is used to refer to a region that forms the current path of a device. In some contexts, this may be true. But there are numerous other references where the term active region is used to refer to simply the source, drain, and space between them of a MOSFET regardless of whether current flows between them. A well-known textbook explains how a MOSFET transistor is built in the active region. *See* Ex. 9 (Baker), 65 ("The active layers are used to make the source and drain regions."). Similarly, another well-known textbook describes forming the source and drain as forming the "active region." *See* Ex. 4 (Chen), 239 ("Active channel regions are first defined by etching windows in a thick field oxide…The boron impurities in the active regions are counter doped…"). This is how active region is used in the claims-at-issue and the intrinsic record. Therefore, in the context of Dr. Rao's inventions it is more accurate to refer to an active region as a doped silicon region where a transistor can be formed (e.g., including source and drain, and silicon between them).

75. Interestingly, defendants omit a citation to Wolf, despite their heavy use of this reference for other terms. Wolf has an entire section devoted to the definition of the disputed term, aptly titled: "Active Region and Field Region Definitions," which supports a POSITA's plain understanding of the term. Ex. 13, 327-331.

4. "unidirectional electric drift field" terms[8] (195:1; 502:7; 222:44)

Greenthread	Defendants
Plain and ordinary meaning	"said [drift layer further/well region…] having a [first/second] static electric drift field that is unidirectional over the [drift layer/well region]" "said [drift layer/well region] having a graded concentration of dopants generating a [first/second] static electric drift field that is unidirectional over the [drift layer/well region]"

[8] These are the terms collectively numbered as term 4 in the table above in the "Disputed Claim Constructions" section of this Declaration.

76. In my opinion, the "unidirectional electric drift field" terms do not need to be construed, and plain meaning suffices for a POSITA to understand them. Based on Defendants' proposed constructions, I see that Defendants are not contending that "electric drift field" or "unidirectional" need to be construed. Instead, Defendants are contending the following language from exemplary claim 195:1: ***said drift layer further having a first static unidirectional electric drift field*** should be construed to mean: ***said drift layer further having a first static electric drift field <u>that is</u> unidirectional <u>over the drift layer</u>***. Dkt. 82, 22. Defendants indicate in their brief that by "over the drift layer" they mean: ***said drift layer further having a first static electric drift field <u>that is</u> unidirectional <u>over the entire drift layer</u>***. *Id*. Defendants make a similar argument for the "well region." *Id.* In my opinion, there is no need to rewrite the claim to say the electric field is "unidirectional *over the drift layer*," much less "unidirectional *over the entire drift layer*." A careful review of the prosecution history reveals that there was no clear disavowal. There is no justification anywhere else in the intrinsic record to limit the terms like Defendants suggest.

77. To begin, Defendants argue that that the "claim language itself *implies* a single unidirectional field across the *entire* layer or region." Dkt. 82, 22 (emphasis added). First, the claim says "single drift layer," not "single unidirectional field." There is nothing in the claim preventing additional electric fields. The Applicant merely said the drift layer has a unidirectional field. The fact that the field may stop before the end of the layer does not mean that the drift layer does not have a unidirectional field.

78. Next, Defendants incorrectly characterize the specification and figures. Defendants cite to several instances where the specification mentions that a graded concentration of dopants creates an electric field. But nothing in the specification says there is only one field per layer, much less that the field must continue across the entire layer or region. *See* Dkt. 82, 22 (citing to the following portions of 195 specification); Ex. 2, 1:34-36 (describing prior art, merely says "aiding drift field" without any mention of a layer, direction of the field, or the total number of fields); 2:13-15 (merely says "doping profiles" without *any* mention of a field); 2:35-47 (discussing how a graded dopant concentration "creates a suitable aiding drift electric field"

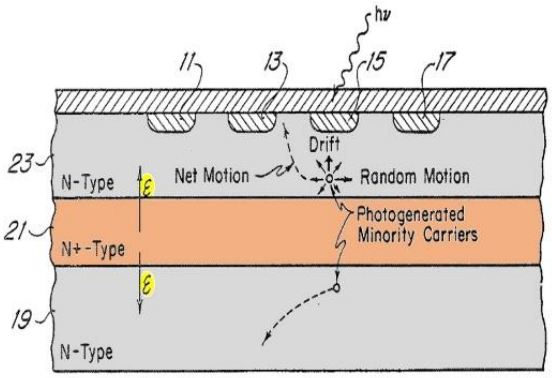
without any mention of a layer, direction of field, or the total number of fields); 3:30-35 (discussing how the graded dopants create a drift field to sweep the minority carriers into the substrate without any mention of the location or duration of the drift field or the total number of fields); Fig. 1 and 5A (showing no field at all). Defendants also cite Figures 5B and 5C, which support Greenthread, not Defendants. These figures show multiple fields that traverse only part of the well region, and only part of the drift layer. Defendants' construction would exclude both of these preferred embodiments.

79. The prosecution history shows that: (1) the limitation "unidirectional" was merely added to clarify that there was a single layer with a graded dopant (as opposed to two layers with uniform dopants); (2) the Applicant never said the claims require the electric field to be unidirectional over any of the layers, much less the entire layer; and (3) the Applicant did not need to limit the claims to require that the electric field was unidirectional over any of the layers, and there would have been no reason for doing so. In an Amendment dated January 26, 2011, the Applicant argued that then-pending claim 10 (now claim 1) was patentable over Kamins. Dkt. 82-8, 209-216. At that time, the claim read in relevant part:

> 10. A CMOS Semiconductor device comprising: …
>
> a drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate to create a drift field drawing minority carriers from said surface layer to said substrate.

Id., 212. In the Remarks, the Applicant argued that Kamins did not disclose the highlighted language. In doing so, the Applicant explained that Kamins did not disclose "a single layer" with graded dopants; instead, Kamins has three layers with uniform dopants. *Id.*, 215.

80. In the figure below, Kamins has three layers: a lightly doped layer 23, a heavily doped layer 21, and a lightly doped layer 19.



Dkt. 82-10, Fig. 2; 2:39-53. None of these layers have a graded concentration of dopants where the dopants gradually change from heavily doped to lightly doped or *vice versa*. Instead, each of the layers has a uniform concentration of dopants, where the concentration of dopants abruptly changes where the layers meet. One can readily see how these two scenarios are different. It is like "grading" a backyard to slope away from a house, versus putting in a retaining wall where a flat area abruptly drops off to a lower flat area.

81. In the next Office Action, the Examiner did not disagree with the Applicants' assessment of Kamins. Dkt. 82-8, 220-229. Instead the Examiner took the position that "single layer" was not a limitation of the claim. *Id.*, 227 ("it is noted that the features upon which applicant relies (i.e., drift layer is required to be a "single layer"; i.e., the drift layer cannot have multilayer structure) are not recited in the rejected claim(s)."). To clarify this point, the Applicant amended the claims in the next amendment to read:

> a <u>single</u> drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate to create a <u>unidirectional</u> drift field drawing <u>all</u>[9] minority carriers from said surface layer to said substrate.

[9] The word "all" was subsequently removed from the claims, which is evidence that it is not a requirement of the claims. Dkt. 82-8, 286-294.

Id., 235. In the Remarks, the Applicant clarified that the graded dopant concentration draws the minority carriers away from the surface. *Id*., 238.

82. The Applicant did not state the claims require the electric field to be unidirectional over the entire drift layer. Also, the Applicant did not state that there could not be multiple electric fields in any of the layers. Instead, Applicant merely distinguished Kamins, where there are multiple layers with uniform dopant concentrations.

83. Moreover, the Applicant did not need to limit the claims to require that the electric field was unidirectional over any of the layers, and there would have been no reason for doing so. Turning back to Kamins' Figure 2, there is no electric field that draws a minority carrier from the surface layer to the substrate. Rather, in Kamins, the top electric field would propel a minority carrier from the substrate to the surface layer, and the bottom electric field would draw a minority carrier from the substrate to a deeper part of the substrate. Thus, then-pending claim 10 was patentable over Kamins regardless of whether the electric field is unidirectional over the entire drift layer or just part of it.

84. In an earlier litigation involving the '195 and '502 patents, the Court stated that there was no prosecution disclaimer regarding a similar term as the present terms. Ex. 5, 14-17. There, the Court found no prosecution disclaimer that would limit the claim so that "the slope of the dopant concentration is of one direction across the layer." *Id*., 11. Defendants are now arguing that the electric field must be "unidirectional over the entire layer." But there is nothing in the prosecution history that mandates that the electric field has to be unidirectional "over the entire layer" and that there cannot be multiple electric fields.

5. "to aid the movement" terms[10] (195:1; 502:7; 842:1, 9; 481:1, 20; 222:1, 21, 39, 41, 42, 44; 014:1, 21)

Greenthread	Defendants
Plain and ordinary meaning	Indefinite. Alternative constructions: "to sweep the minority carriers from…to…" or "to sweep the carriers from…[to/towards]…"

85. I agree with Greenthread's position that plain meaning is appropriate for these "to aid the movement" terms. In my opinion, "to aid the movement" is a simple term that is readily understood by a POSITA. Any one that has put a little WD40 on a rusty hinge, or stretched before exercising, knows what it means "to aid the movement" of something. Likewise, nobody would dispute that a wheelchair ramp "aids the movement" of someone in a wheelchair.

86. Turning to the claims themselves, the claims specify exactly ***who*** and ***what*** is "aiding the movement," and ***where*** and ***when*** the movement occurs. Moreover, the specification provides specific examples of each of these, and the prosecution history shows these examples. The face of the claim and the preferred embodiment in Fig. 5B explain exactly what is meant by "to aid the movement of the minority carriers from the surface layer to the substrate." Claim 195:1 reads in relevant part:

> a single drift layer disposed between the other surface of said surface layer and said substrate, said single drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a **first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate**;

Ex. 2, 4:18-24.

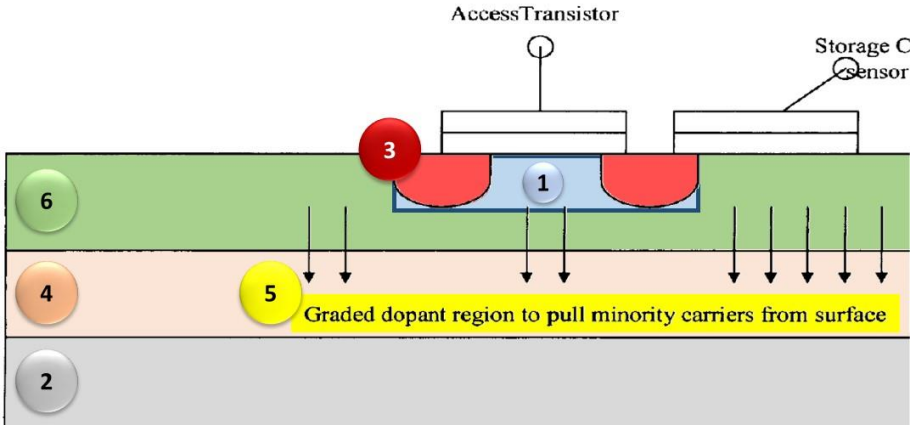
87. The claim contains similar language for the well region. *Id.*, 25-29. The claim language above explains ***who*** is aiding the movement: it is the single drift layer, and more specifically the graded dopants in the single drift layer. Next, it explains ***what*** is aiding the

[10] These are the terms collectively numbered as term 5 in the table above in the "Disputed Claim Constructions" section of this Declaration.

movement: it is the first static unidirectional electric drift field. The claim even says where the movement occurs: it is in the drift layer, and the carriers move downward. Finally, the claim specifies when it occurs: when the minority carriers are exposed to the electric field.

88. The Applicant did not just claim "to aid movement" in a vacuum. Rather, the Applicant claimed a specific drift layer with graded dopants that create a particular type of electric field. By the time the claim gets to the phrase "to aid movement," it is my opinion that the claim is merely clarifying what the electric field does. Any question about what is meant by "to aid the movement" is answered by the preceding claim language. Electric drift fields are a well-known phenomenon that cause carriers to move, and a POSITA would have readily recognized that when a "static unidirectional electric drift field" is present then it aids the movement of the minority carriers. *Id.* If it is not present, then it does not aid such movement. The claim turns on the presence of the "unidirectional electric drift field," and the phrase "to aid the movement of minority carriers" merely states what the "unidirectional electric drift field" does. The drift field points to one direction and charge carriers, when free to move, respond to the drift field by moving in one direction or the other depending on their charge polarity.

89. This is exactly what is shown in Fig. 5B and the corresponding parts of the specification.



Ex. 2, Fig. 5B (annotated).

90. The specification explains how the unidirectional electric field aids movement of

the carriers. Ex. 2, 2:40-47, 3:30-35. The prosecution history further shows this. Dkt. 82-8, 57, 82-83, 113-114. Thus, a POSITA reading the claims in light of the intrinsic record would have readily understood what is meant by "to aid the movement of the minority carriers." The claim is not referring to just any movement. Rather the claim, is specific to the movement of carriers away from the surface layer.

6. "well region" (195:1; 502:7; 842:1, 9; 481:1, 20; 222:1, 21, 39, 41, 42, 44; 014:1, 21)

Greenthread	Defendants
Plain and ordinary meaning, where portions of a well are not well regions.	"A well, whether formed by single or multiple implants. Portions of a well are not well regions."

91. In my opinion, "[w]ell region" is a term that a POSITA would have readily understood. The term well is commonly used to refer to a doped region at the surface where the transistor is built. Dkt. 82-16, 17-19. The well region surrounds the active region. *Id.*, 18 (Fig. 6-8). This is how the term is consistently used in the claims, specification, and prosecution history. This term does not require construction, and it should be given the full scope of its plain meaning.

92. There are two parts to Defendants' proposed construction (the two parts are the first and second sentences of their construction). I understand that Greenthread has adopted the second part of Defendants' construction (i.e., that portions of a well are not well regions).

93. In my opinion, the first part of Defendants' construction ("A well, whether formed by single or multiple implants") is unnecessary and introduces ambiguity where there is none. To say that the well is "formed by single or multiple implants" is unnecessary, because "single or multiple" describes all possible options for implants. A POSITA would have understood that a well is formed by ion implantation, and it would have been unnecessary and confusing to describe forming a well "by single or multiple implants."

B. Claim Term Found in Exemplary Claim 842:1

7. "active region…within which transistors can be formed" (842:1, 9; 481:1, 20; 222:1, 21, 39, 41, 42; 014:1, 21)

94. In my opinion, this term is not indefinite, and it would have been readily understandable to a POSITA. As I explained above in Section VII.A.3, a POSITA reading the claims and intrinsic record would have understood that this term means exactly what it says: an active region (i.e., a doped region at the surface of a semiconductor device) where a transistor can be formed. Claim 195:1 specifies, for example, that an active region includes a source and drain (two heavily doped regions at the surface of a semiconductor device where a transistor can be formed).

95. In the specification and entire prosecution history, Dr. Rao consistently used "active region" to refer to the doped regions at the surface of a semiconductor device (e.g., the source and drain) where, for example, a MOSFET transistor is built or can be built. The term "well region" can be used to refer to the doped silicon that surrounds the "active region" where the source and drain are formed. Defendants confuse the two. While the active region may be "located within" or "surrounded by" the well region, Dr. Rao made it clear that the active region is where the transistors are built or may be built. When the term "active region…within which transistors can be formed" is properly viewed in this context through the eyes of a POSITA, there is nothing indefinite about it.

96. An "active region" does not require current flow. Defendants state that "a region is 'active' when an existing device is formed there causing electrical current to flow." Dkt. 82, 31. This is not correct, in my opinion. An active region does not have to be "electrified" to form a channel between a source and drain in order to qualify as an active region. For example, in order for a channel to form in a MOSFET, terminals must be attached to the source, drain, and gate, and a voltage must be applied to the gate to repel the minority carriers away from the surface layer. The fact that the transistor is not "electrically active" such that current is not flowing through the transistor does not mean that an active region does not exist.

97. The specification shows that an "active region" is a doped region at the surface of a semiconductor device where a transistor can be built. Defendants' claim construction brief includes several citations regarding the present claim term, but in my opinion they support Greenthread's position regarding this term (plain meaning), not Defendants' contention of indefiniteness. *See* Dkt. 82, 37 fn18 (citing the following); Abstract (referring to "active region" without any mention of current flow); 2:16-18 (referring to "active devices," not "active regions"); 2:25-26 (referring to Figs. 3B-D, where the "active regions" are shown as doped regions at the surface where transistors are built; none of the figures show a current flow); 3:62-63 (referring to "active circuitry," not "active regions"); Fig. 3A and 5A (referring to "active devices," not "active regions"); Figs. 3C and 5B-C (all showing the active regions has doped regions at the surface where transistors are built); claim 5 (merely saying that a particular type of transistor can be built in the active regions); claim 7 (merely saying that the active regions are separated by an isolation regions; claim 18 (merely saying that the transistor that can be built in the active region is a typical MOSFET).

98. Defendants incorrectly claim that the specification never describes a regions that is both an "active region," and a "region…within which transistors can be formed." Dkt. 82, 38. But the 842 patent repeatedly describes active regions where transistors are built. Ex. 2, 2:24-27, 3:10-13; Fig. 3C, 5B-5C. In my opinion, this shows that these "active regions" are "regions…within which transistors can be formed."

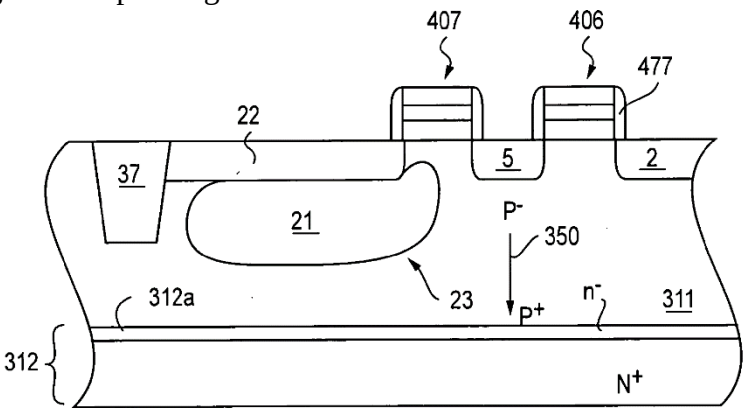
99. The prosecution history for the 195 and 502 patents shows that an "active region" is a doped region where a transistor can be built. Defendants state that during prosecution, Greenthread repeatedly referred to the claimed "active region" as the current path of an existing transistor. Dkt. 82, 38. This does not appear to be correct. In my opinion, Defendants' citations to the prosecution history actually support Greenthread, not Defendants. First, Defendants cite to where the Applicant first mentions "active and well regions" (this shows that the active region is different from the well region), and then the Applicant states that an "active element" (i.e., a pair of transistors) "can be active when a voltage (or current) is applied." Dkt. 82, 38, fn20. This

statement shows that an "active region" is an "active region" regardless of whether the "active element" is turned "on."

100. Next, Defendants cite to one of the prior art references cited during prosecution (Rhodes). Dkt. 82, 38 (citing Dkt. 82-13 (Rhodes)). But the fact that Rhodes uses the term "electrically active" (as opposed to just "active") shows that an active region does ***not*** have to have an electrical current, in my opinion. If an active region necessarily required an electrical current, then it would have been redundant to say "electrically active."

101. As Defendants correctly note, the Applicant distinguished the "active regions," where the transistors are built, from the surrounding wells. *See* Dkt. 82, 38.

102. In my opinion, the prosecution history for the later patents also shows that an "active region" is a doped region at the surface of a semiconductor device where a transistor can be built. It appears that Dr. Rao was merely explaining that even if one incorrectly reads the prior art, like the Examiner did, his invention is still patentable over the prior art. In an Office Action dated May 16, 2019, the Examiner relied on the following Figure 4D from a prior art reference called "Hong" to reject then-pending claim 1.



Ex. 11 (842 file history), 107-115; Dkt. 82-14 (Hong), Figure 4D.

103. Hong makes clear that reference numeral 311 is the substrate, *id.*, [0030]; and 2 is the "source/drain region," *id.*, [0040]. Nonetheless, the Examiner took the position that "311, which includes wells such as 21, 22, 5, 2" could be the "first active region"; and "source/drain region 2" could be the "second active region." In my opinion, this rejection by the Examiner was

incorrect. But this is the rejection that the Applicant responding to in the next Amendment dated September 16, 2019. Ex. 11, 124-132

104. The Applicant did not state that reference numeral 311 was an active region, as Defendants suggest. Rather, the Applicant was explaining that even under the Examiner's incorrect rejection Figure 4B did not meet the limitations of the pending claim. This is why he wrote:

> The Examiner has referred to the first active region as the region 311, but has referred to the regions 21, 22, 5 and 2 as "wells." As discussed in the prior Response, there is no support for such a construction, as the term "wells" in semiconductor technology typically refers to a region formed in a substrate within which active components are formed. The Examiner has referred to the second active region as being that defined by the source/drain region 2 or the regions 2 or 5 or 22 of the pixel cell.

Id., 129-130.

105. It appears that Defendants have not included, in their statements in their brief, the most important language highlighted above. *See* Dkt. 82, 40. It appears that the Applicant indicated that he did not agree with the Examiner's construction for the "first active region." Meanwhile, the Applicant did not dispute that a source/drain region could be an active region where a transistor could be built. Thus, the prosecution history supports Greenthread, not the Defendants.

106. Defendants ask whether the "active region" is the current path in an existing transistor, or the area where a transistor can be formed. Dkt. 82, 41. The intrinsic record shows that the answer is the latter. But to be more precise, the "active region" is a doped region at the surface of a semiconductor device where a transistor can be formed. The face of claim 842:1 shows this when it says the "first active region" is (1) disposed adjacent the first surface of the substrate, (2) with a second doping type; and (3) "within which transistors can be formed."

Therefore, the face of claim 842:1 answers this question, and the specification and prosecution history further shows it.

107. Defendants also ask if the "active region" is the current path, how can additional transistors be formed in that existing device. Dkt. 82, 41. But as explained above, an active region does not necessarily have to have a current path.

108. Defendants further ask if the "active region" is the surrounding region where current does not flow, what makes that region "active"? Dkt. 82, 41-42. If by "surrounding region where current does not flow," Defendants mean the well region that surrounds the active region, as opposed to the active region where a transistor is built or could be built, then it would not necessarily be "active."

109. Defendants also ask what is the difference between the claimed "active region" and other regions where transistors can be formed. Dkt. 82, 42. The claimed "active region" must meet the other limitations of the claim, and this is what differentiates it from other regions where transistors can be formed.

VIII. CONCLUSION

110. I declare under penalty of perjury that the foregoing is true and correct.

Respectfully submitted,

Date: October 31, 2022 By: _____
Konstantinos P. Giapis

APPENDIX A

Curriculum Vitae

Konstantinos P. Giapis, Ph.D.

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Expertise

Semiconductor physics, devices, and processing
Nanotechnology, nanodevices, and nanofabrication
Low temperature plasma deposition and etching
Chemical dynamics at surfaces
Thermodynamics of nanoscale confinement

Professional Preparation

National Technical University (Greece)	Chemical Engineering	Diploma, 1984
University of Minnesota (USA)	Chemical Engineering	Ph.D., 1989
Bell Laboratories, Murray Hill, NJ (USA)	Postdoctoral Fellow	10/89—3/91

Appointments

2010—now	*Professor* of Chemical Engineering, Caltech (USA)
2010	*Visiting Professor*, Mechanical Engineering, ETH (Zürich, Switzerland)
1999–2009	*Associate Professor of Chemical Engineering,* Caltech (USA)
1998	*Visiting Professor,* France Telecom, Branche CNET (Grenoble, France)
1994–1998	*Assistant Professor of Chemical Engineering,* Caltech (USA)
1992–1993	*Lacey Instructor of Chemical Engineering,* Caltech (USA)
1/92–7/92	*Consultant,* AT&T Bell Laboratories, Murray Hill, NJ (USA)
1991	*Research Associate,* Physics Department, University of Crete (Greece)

Awards and Honors

1993	Camille and Henry Dreyfus New Faculty Award
1996	National Science Foundation Career Award
1997	Camille Dreyfus Teacher-Scholar Award

Committees

External Evaluation Committee, Chemical Engineering Department, NTU, Greece (2013)
International Symposium on Advanced Fluid Information and Trans-disciplinary Fluid Integration (AFI/TFI), Japan, 2007-2014
International Conference on Ion Beam Modification of Materials (IBMM), 2009-2011
Executive Committee, Plasma Science and Technology Division, AVS, 2005-2007
International Advisory Board, Dry Process Symposium, Japan, 1998-2010
International Program Committee, Micro- and Nano-Engineering Conference, 2003-2005
International Conference on Plasma Process Induced Damage (P2ID), 1999-2001

Peer-Reviewed Publications

1. K.P. Giapis, D.C. Lu and K.F. Jensen, *Appl. Phys. Lett.* **54**, 353 (1989).
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