

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CIRRUS LOGIC, INC.;
OMNIVISION TECHNOLOGIES, INC.; AND
AMS SENSORS USA INC.,
Petitioner,

v.

GREENTHREAD LLC,
Patent Owner.

Case No. IPR2023-00001
Patent No. 10,734,481

**DECLARATION OF DR. SANJAY BANERJEE IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO.
10,734,481**

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I, Dr. Sanjay Banerjee, declare as follows:

1. My Name is Sanjay Banerjee.
2. I have been retained as an expert witness on behalf of Cirrus Logic, Inc., OmniVision Technologies, Inc., and ams Sensors USA, Inc. (collectively, “Petitioner”) for the above-captioned Petition for *Inter Partes* Review (“Petition”) of U.S. Patent No. 10,734,481 (the “’481 Patent”) (Ex. 1001). I am being compensated for my time in connection with this Petition at my standard consulting rate of \$675 per hour. My compensation is not affected by the outcome of, or my testimony in, this *Inter Partes* Review, or any litigation proceedings. I am informed that the assignee for the patent in the present proceeding is Greenthread, LLC (“Patent Owner”). I am also informed that the Petition names Cirrus Logic, OmniVision, ams Sensors USA, ams-OSRAM AG, OSRAM GmbH, and GlobalFoundries as real-parties-in-interest.
3. I have been asked to provide my opinions regarding whether claims 1-9, 12-27, and 30-36 of the ’481 Patent (the “Challenged Claims”) are invalid as obvious to a person having ordinary skill in the art at the time of the alleged invention. In connection with this effort, I have reviewed declarations provided in connection with another *Inter Partes Review* Petition filed against the ’481 Patent (specifically, Ex. 1003 in IPR2023-00260 filed on behalf of Petitioner Intel Corporation), and with another *Inter Partes Review* Petition filed against the

related '222 Patent (specifically, Ex. 1003 in IPR2023-01242 filed on behalf of Petitioner Semiconductor Components Industries, LLC). After having conducted my own independent analysis on the '481 Patent, I concur with the analyses provided in those declarations. For efficiency, I have excerpted portions of those declarations in drafting this declaration.

4. The '481 Patent issued on August 4, 2020 from Application No. 16/717,950, filed on December 17, 2019. The '481 Patent claims priority to Application No. 10/934,915, filed on September 3, 2004.

5. I am not currently, and have not at any time in the past been, an employee of any Petitioner or Real-party-in-interest. Other than set out above, I have no affiliation, contractual connection, or financial connection with any Petitioner or Real-party-in-interest, or any of their respective subsidiaries or parents. I similarly have no financial interest in, or affiliation with the Patent Owner.

I. BACKGROUND AND QUALIFICATIONS

6. I am currently the Cockrell Family Chair Professor of Electrical and Computer Engineering at the University of Texas at Austin. At UT Austin, I am also the director of the Microelectronics Research Center. I have been a faculty member at UT Austin since 1987.

7. I have also been active in industries related to the relevant field of art. As a Member of the Technical Staff, Corporate Research, Development and

Engineering of Texas Instruments Incorporated from 1983–1987, I worked on polysilicon transistors and dynamic random access trench memory cells used by Texas Instruments in the world’s first 4-Megabit DRAM, for which I was co-recipient of the Best Paper Award, IEEE International Solid State Circuits Conference, 1986.

8. I received a B. Tech. degree from the Indian Institute of Technology, Kharagpur, and M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign, all in Electrical Engineering.

9. I am a leading researcher and educator in various areas of transistor device fabrication technology, including the fabrication, characterization and application of memory devices, transistors, and nanotechnology. My research has been funded by the Texas Advanced Technology Program (ATP), the Texas Higher Education Coordinating Board, the National Science Foundation, the SEMATECH (Semiconductor Manufacturing Technology) consortium, the SRC (Semiconductor Research Corporation) consortium, DARPA, and the Department of Energy, among others.

10. At the University of Texas, I am the director of the Microelectronics Research Center, comprised of faculty colleagues, graduate, and undergraduate students. I also served as the director of the South West Academy of

Nanoelectronics from its inception through the end (Dec. 2017), one of three centers in the United States established to develop a replacement for MOSFETs.

11. I have published over 1,200 technical articles, many related to semiconductor fabrication technology, most at highly competitive refereed conferences and rigorously reviewed journals. I have also published 8 books or chapters on transistor device physics and fabrication, and have supervised over 50 Ph.D. and 60 MS students.

12. I have been a member of scientific organizations and committees, including the IEEE Dan Noble Award Committee from 2010–2013, serving as Chair from 2012–2013, the International Technology Roadmap for Semiconductors, the International Conference on MEMS (Microelectromechanical Systems) and Nanotechnology, the IEEE International Conference on Communications, Computers, Devices, the International Electron Devices Meeting, the International Conference on Simulation of Semiconductor Processes and Devices, and the IEEE Symposium on VLSI (Very-Large-Scale Integration) Technology. I have served as the Session Chair for the “Device Technology” Session conducted at the IEEE International Electron Devices Meeting in 1989–1990. I have also served as the General Chairman for the IEEE University Government Industry Microelectronics Symposium in 1994–1995, and Chair of the IEEE Device Research Conference.

13. I have served on the Technical Advisory Boards of AstroWatt, DSM Semiconductors, Cambrios, Nanocoolers Inc., BeSang Memories, Organic ID and ITU Ventures; Gerson Lehmann Group, NY; Austin Community College; Asia Pacific IIT; Rochester Institute of Technology, and HSMC Foundry.

14. I received the Engineering Foundation Advisory Council Halliburton Award (1991), the Texas Atomic Energy Fellowship (1990–1997), Cullen Professorship (1997–2001) and the Hocott Research Award from UT Austin (2007). I also received the IEEE Grove Award (2014), Distinguished Alumnus Award, IIT (2005), Industrial R&D 100 Award (2004), ECS Callinan Award, 2003, IEEE Millennium Medal, 2000, NSF Presidential Young Investigator Award in 1988, and several SRC Inventor Recognition and Best Paper Awards. I was a Distinguished Lecturer for IEEE Electron Devices Society, and am a Fellow of the Institute of the Electrical and Electronics Engineers (IEEE), the American Physical Society (APS) and the American Association for the Advancement of Science (AAAS).

15. I am the inventor or co-inventor of over 35 United States patents in various areas of transistor device fabrication technology. I was elected a Fellow of the National Academy of Inventors in 2021.

16. Additional details about my employment history, fields of expertise, and publications are further included in my curriculum vitae, attached as Ex. 1004.

II. MATERIALS AND OTHER INFORMATION CONSIDERED

17. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art and have considered the viewpoint of a person having ordinary skill in the art (POSITA) at the time of the alleged invention.

18. I have considered the materials referenced herein, including the '481 Patent (Ex. 1001), the file history of the '481 Patent (Ex. 1002), the parent and related applications, the file histories of the parent and related applications, including for the parent '195 Patent (Ex. 1016), the Petition, and other documents listed in the Exhibit List of the Petition, including:

Description	Date of Public Availability
U.S. Patent Application Publication No. 2003/0183856 to Wieczorek ("Wieczorek") (Ex. 1006)	Filed on October 29, 2002 (with priority to March 28, 2002).
U.S. Patent No. 6,043,114 to Kawagoe, et al. ("Kawagoe") (Ex. 1007)	Filed on September 22, 1997 (with priority to July 28, 1995) and issued on March 28, 2000.
Wolf and Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol 1, Lattice Press (2000) ("Wolf.1") (Ex. 1008A)	Published and publicly available no later than 2002.
Wolf and Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol 2, Lattice Press (2000) ("Wolf.2") (Ex. 1008B)	Published and publicly available no later than 2002.
Wolf and Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol 3, Lattice Press (2000) ("Wolf.3") (Ex. 1008C)	Published and publicly available no later than 2002.
Wolf and Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol 4, Lattice Press (2000) ("Wolf.4") (Ex. 1008D)	Published and publicly available no later than 2002.
Wang and Agrawal, <i>Single Event Upset: An Embedded Tutorial</i> , 21st	Published and publicly available in 2008.

Description	Date of Public Availability
<i>Intl Confon VLSI Design</i> , IEEE 2008 (“Wang”) (Ex. 1009)	
U.S. Patent No. 4,481,522 (“Jastrzebski”) (Ex. 1010)	Filed March 24, 1982 and issued on November 6, 1984.
U.S. Patent No. 6,163,877 (“Gupta”) (Ex. 1014)	Filed November 5, 1996 and issued on December 19, 2000.
U.S. Patent No. 6,534,805 (“Jin”) (Ex. 1015)	Filed April 9, 2001 and issued on March 18, 2003.
Sze, <i>Semiconductor Devices Physics and Technology</i> , 2d Ed., John Wiley & Sons (2002) (Ex. 1022)	Published and publicly available in 2002.
Maziasz and Hayes, <i>Layout Minimization of CMOS Cells</i> , Kluwer Academic Publishers (1992) (“Maziasz”) (Ex. 1023)	Published and publicly available in 1992.
Rabaey <i>et al.</i> , <i>Digital Integrated Circuits, A Design Perspective</i> , Prentice Hall Electronics and VLSI Series (2003) (“Rabaey”) (Ex. 1025)	Published and publicly available in 2003.
Gregory and Shafer, “Latch-Up In CMOS Integrated Circuits,” IEEE Transactions on Nuclear Science, Volume 20, Issue 6 (1973) (Ex. 1026)	Published and publicly available in 1973.
U.S. Patent No. 4,160,985 to Kamins <i>et al.</i> (“Kamins”) (Ex. 1031)	Filed November 25, 1977 and issued July 10, 1979.
McGraw-Hill Dictionary of Scientific and Technical Terms (2003) (Ex. 1032)	Published and publicly available in 2003.
U.S. Patent Application Publication No. 2003/0030488 to Hueting <i>et al.</i> (“Hueting”) (Ex. 1035)	Filed July 25, 2002 (with priority to August 7, 2001).
U.S. Patent No. 6,614,560 to Silverbrook (“Silverbrook”)	Filed July 10, 1998 and issued September 2, 2003.
Wong <i>et al.</i> , “CMOS Active Pixel Image Sensors Fabricated Using a 1.8V, 0.25 um CMOS Technology.” (Ex. 1044)	Published and publicly available in 1998.

19. The references listed above include prior art to the '481 Patent which is entitled to a priority date not earlier than September 3, 2004. None of the prior art references were before the Patent Office during prosecution. I am also relying on the declaration of D. Sylvia Hall-Ellis who opined that the Wolf reference was publicly available before September 3, 2004.

III. UNDERSTANDING OF PATENT LAW

20. I am not an attorney. For purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

A. Claim Construction

21. I understand that in an IPR petition filed after November 13, 2018, a claim must be construed under the *Phillips* standard. Under that standard, words of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent.

B. Obviousness

22. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject

matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed.

23. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

24. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a modification or combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known elements in the manner described in the claim;

- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

25. I understand that a POSITA has ordinary creativity, and is not an automaton.

26. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

27. I understand that prior art to the '481 Patent includes patents and printed publications in the relevant art that predate the priority date of the '481 Patent.

28. I understand that certain factors—often called “secondary considerations”—may support or rebut an assertion of obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention.

I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

IV. SUMMARY OF OPINIONS

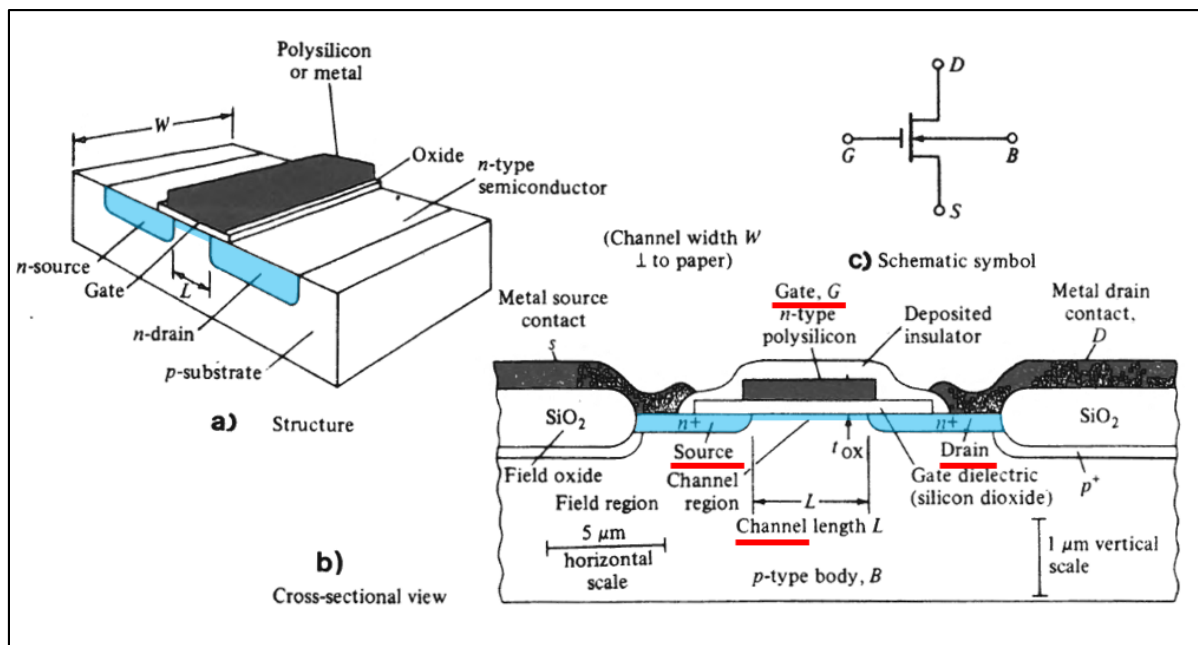
29. It is my opinion that the challenged claims are unpatentable for at least the following reasons:

- Claims 1-9, 12-14, 16-27, and 30-36 are disclosed or, at a minimum, rendered obvious by Kawagoe (Ground I);
- Claims 1-2, 4-9, 12-22, 24-27, and 30-36 obvious are rendered obvious by Wieczorek in combination with Wolf (Ground II);
- Claims 1-9, 12-14, 16-27, and 30-36 are rendered obvious by Kawagoe in view of Gupta (Ground III);
- Claims 1-2, 4-9, 12-22, 24-27, and 30-36 are rendered obvious by Wieczorek in combination with Wolf and Gupta (Ground IV);
- Claims 19 and 36 are rendered obvious by Kawagoe in combination with Silverbrook (Ground V); and
- Claims 19 and 36 are rendered obvious by Wieczorek in combination with Wolf and Silverbrook (Ground VI).

30. It is my opinion that for purposes of this proceeding, the claim terms need not be construed to resolve the prior art issues presented in this Petition.

V. OVERVIEW OF THE TECHNOLOGY

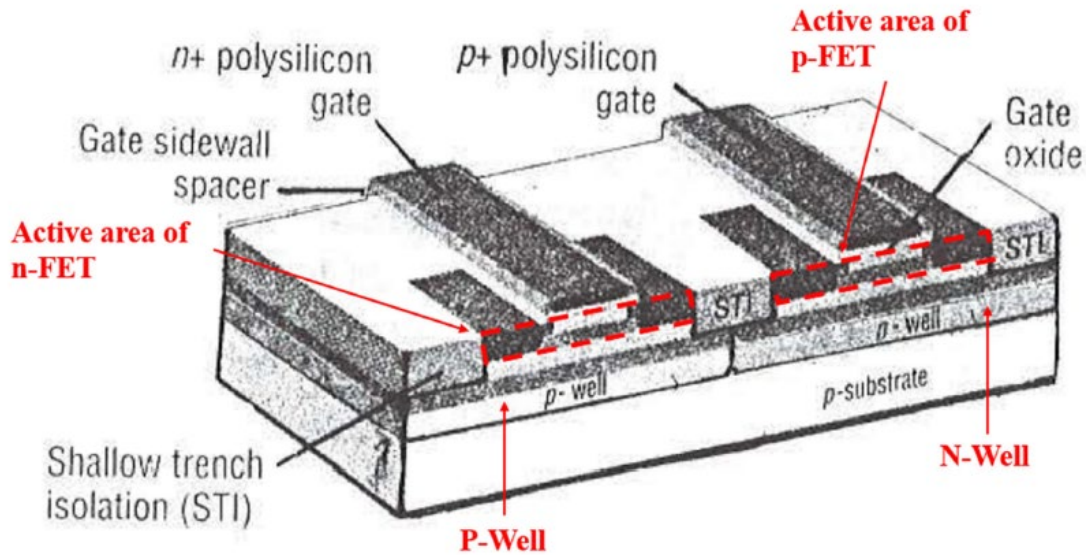
31. A Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a transistor that switches from an OFF state to an ON state when a voltage is applied to a gate terminal. Ex. 1008B, 402. In the ON, or active state, current flows from a source to a drain through a channel region (the length of such channel region is labelled “ L ” below). The channel region is under the gate and gate oxide, and between the source and drain.



Ex. 1008B, FIG. 5-1; *id.*, 298-301, FIGS. 5-2, 6-4. The combination of the source, drain, and channel regions of a transistor may be an example of an active region, as Wolf teaches. Ex. 1008B, 299-300 (“The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The **active regions** are those in which transistor action occurs; i.e., the **channel** and the heavily doped

source and *drain* regions.”), FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e).

32. MOSFETs are characterized by the material used in the source and drain. A MOSFET with source/drain regions made from “p- type” material in such areas (as shown in the figure above, labelled “p⁺”) is known as a PMOS or p-FET, while a MOSFET with source/drain regions made from “n- type” material (“n⁺”) in such areas is known as a NMOS or n-FET. In the mid-1980s, Complementary MOS (CMOS) devices became popular, which have both PMOS (p-FET) and NMOS (n-FET) transistors on the same substrate or integrated circuits (ICs). In such ICs, the active areas (and associated transistors) are generally formed in regions called “wells.” Impurities known as “dopants” are added to the active areas and wells to add charge carriers and tailor the electrical properties of these regions such as their conductivity. The wells have opposite dopant type to the dopants of the source/drain. As illustrated below, an n-FET is formed in a p-well and a p-FET is formed in an n-well.



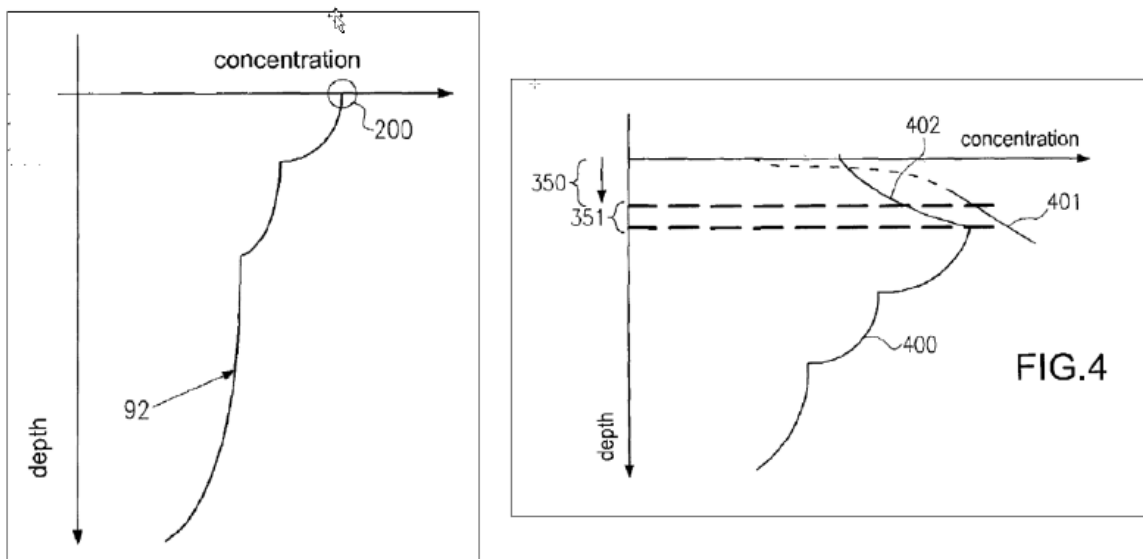
Ex. 1008A, FIG. 16-28 (annotations in red).¹

33. With respect to dopants, charge carriers can be electrons (which are negatively charged) or holes (which are positively charged). Ex. 1008C, 86. When a region is doped with p- type dopants, the holes are majority carriers and the electrons are minority carriers. Ex. 1008C, 86. When a region is doped with n- type dopants, the electrons are majority carriers and the holes are minority carriers. Ex. 1008C, 86.

34. A “dopant profile” refers to the “map” of concentration of dopants over a doped region and, in certain simplified scenarios, can be expressed as a function of depth. For example, a dopant concentration that does not change with depth is a uniform concentration. A non-uniform dopant concentration that varies for example with depth, e.g., increases or decreases with depth, is a non-uniform dopant

¹ All emphases and annotations added unless otherwise noted.

concentration called “graded.” A graded dopant concentration that peaks at some depth of the doped region(s) instead of at the top or bottom of the doped region(s) is called “retrograde.” All such doping profiles were known in the art, as shown in the Wieczorek figures below. I note that the specification of the challenged ’481 patent itself admits that, at the time of the invention, “[r]etrograde wells ha[d] been attempted.” Ex. 1001, 2:18-31.



See Ex. 1006, FIG. 2B (left) and FIG. 4 (right).

VI. THE ’481 PATENT

35. The ’481 Patent issued on August 4, 2020 from Application No. 16/717,950, filed on December 17, 2019. The ’481 Patent claims priority to Application No. 10/934,915, filed on September 3, 2004. Ex. 1001, cover.

A. Claims

36. The '481 Patent has 36 claims, including two independent claims numbered 1 and 20. Ex. 1001, 4:49-6:60. Claims 1-9, 12-27, and 30-36 are the Challenged Claims.

37. Exemplary Claim 1 is reproduced below:

1. A semiconductor device, comprising:

a substrate of a first doping type at a first doping level having first and second surfaces;

a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;

a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;

transistors formed in at least one of the first active region or second active region;

at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and

at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.

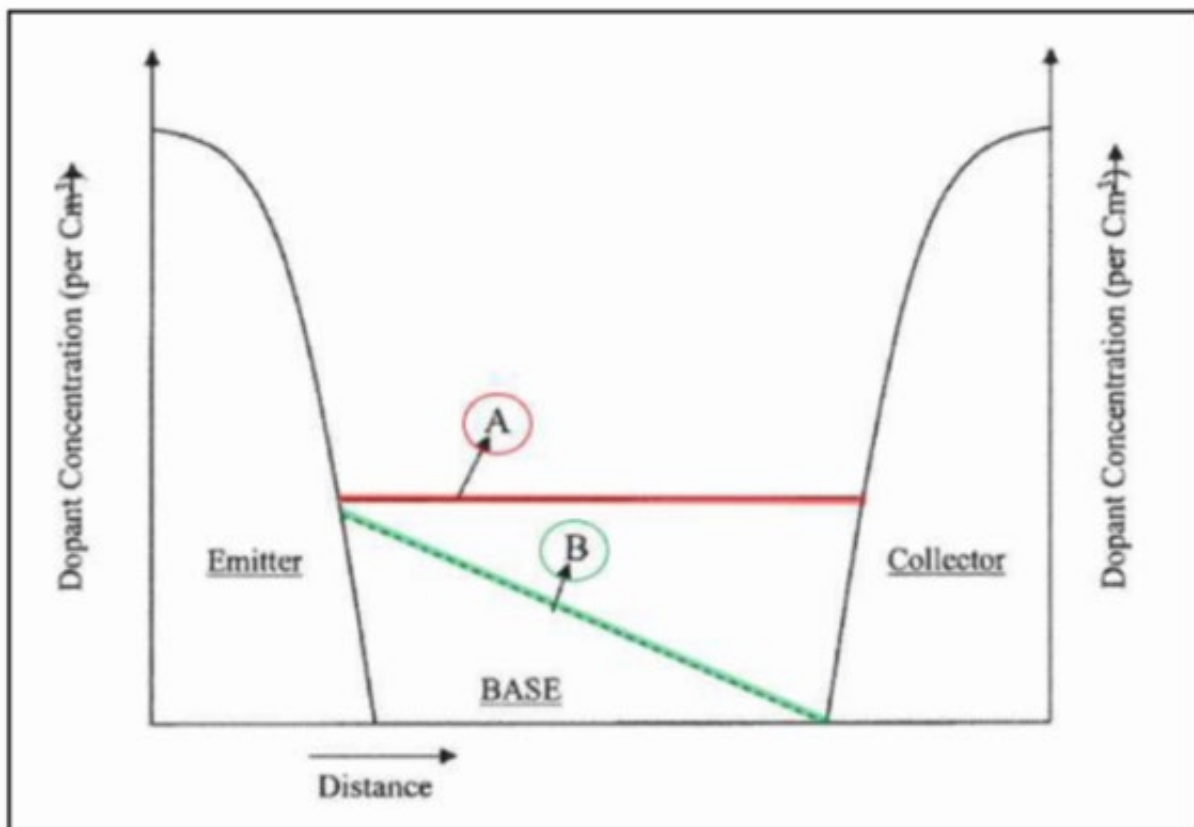
Ex. 1001, 4:50-5:3.

B. Summary of the Specification

38. The '481 Patent is directed to “grading the dopant concentration” in certain regions of a semiconductor device. Ex. 1001, Abstract. In particular, the Challenged Claims claim that an active region and a well region of a semiconductor device have graded dopant concentrations to aid carrier movement. *Id.*, Cl. 1 (“at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement ...” and “at least one well region ... containing at least one graded dopant region to aid carrier movement ...”). I understand that Patent Owner asserts that at least one of the claims of the '481 Patent are infringed by a CMOS product in a case against Petitioner/Real-Party-In-Interest (*Greenthread, LLC v. Cirrus Logic, Inc.*, Civil Action No. 1:23-cv-00443 in the Western District of Texas, filed March 31, 2023 (“Cirrus District Court Case”)). Moreover, it is my understanding that Patent Owner has previously asserted that one or more claims of the '481 were infringed by CMOS products in other district court cases (*Greenthread, LLC v. ON Semiconductor Corporation and Semiconductor Components Industries, LLC*, Civil Action No. 1:23-cv-00443 in the District of Delaware, filed April 21, 2023 (“On Semiconductor Litigation”); *Greenthread, LLC v. Intel Corporation, Dell Inc., and Dell Technologies Inc.*, Civil Action No. 6:22-cv-105 in the Western District of Texas, filed January 27, 2022 (“Intel Litigation”)).

In my opinion, the references relied on in the Petition (*i.e.*, Kawagoe, Wieczorek, Wolf, and Gupta) are also directed to CMOS devices and technology.

39. According to the '481 Patent, the figure below “illustrates the relative doping profiles of emitter, base and collector for the two most popular bipolar junction transistors: namely, uniform base (‘A’) [(red)] and graded base (‘B’) [(green)].” Ex. 1001, 2:39-42.



Id., FIG. 1 (“Prior Art”).² The ’481 Patent states that such “uniform base” and “graded base” bipolar junction transistors existed in the prior art. *Id.*

40. The ’481 Patent explains that “[r]etrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits.” Ex. 1001, 2:18-20. The ’481 Patent further states that “[r]etrograde and halo wells have also been attempted to improve refresh time in DRAMs (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs.”³ *Id.*, 2:24-28. The ’481 Patent also explains that “these techniques” in the prior art “either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.” *Id.*, 2:28-32.

41. In my opinion, the only description of graded dopant concentrations and purported carrier movement in CMOS devices in the ’481 Patent is in two paragraphs of the specification and associated Figures 5A-5C. Ex. 1001, 3:48-4:30, FIGS. 5A-5C. In my opinion, the specification does not provide any guidance, such

² As to all subsequent figures, all colors and colored annotations to figures added.

³ In a “halo” implantation, dopant of the same type as the major well dopant is implanted beneath the drain extension junction. The term “halo” stems from the fact that the implantation is done after the gate is formed, causing the dopant to surround the gate in a ring formation. *See, e.g.*, Ex. 1008A at 105.

as dopant concentration ranges or doping gradients, on the grading of dopant concentration that would accomplish “sweep[ing] [] carriers from the active circuitry at the surface into the substrate” or “aid[ing]” carrier movement in CMOS devices as recited in the Challenged Claims. It is my further opinion that the specification does not provide any guidance as to the degree or nature of the “aiding” referenced in the Challenged Claims. Instead, the specification contrasts “graded channel[s]” with “uniformly doped channel (as practiced in the prior art).” *Id.* at 4:15-18.

42. Thus, in my opinion, the specification uses “graded” dopant to describe a dopant concentration that is not uniform.

C. Summary of the Prosecution History

43. I understand that the Challenged Claims issued without any office action rejection, and none of the prior art relied on in this Petition was cited or considered by the Examiner. I understand that in the Notice of Allowance, the Examiner stated that the claimed “aiding of carrier movement [] ‘from the first surface to the second surface of the substrate’ [was] known in the art.” Ex. 1002, 81-83. According to the Examiner, the claims issued over the “closest reference” (U.S. Patent Application Publication No. 2007/0045682 (“Hong”)) because Hong does not disclose “active” regions within which transistors can be formed. *Id.* I note that Hong is not prior art and was also the only reference discussed in prosecution of the immediate parent application that issued as U.S. Patent No. 10,510,842 (“the

'842 Patent"). I also note that none of the claims at issue during prosecution of the earlier parent applications to both the '842 and '481 Patents are of the same or similar scope as the Challenged Claims. Importantly, I see that none of the claims prosecuted in the parent applications of the '842 Patent claim graded dopants *in an active region* to aid carrier movement "*to the second surface of the substrate*" as required by Claim 1 of the '481 Patent and Claim 1 of the '842 Patent. For example, the claims of the parent U.S. Patent No. 9,647,070 ("the '070 Patent") are directed to bipolar devices and claim aiding carrier movement "from an *emitter* in the active region to a *collector* in the substrate," and not "from the first surface to the second surface of the substrate" as recited in the Challenged Claims. Ex. 1034, Cl. 1. Other pending claims that recited graded dopant in an active region were withdrawn prior to substantive examination. Ex. 1016, 73 (withdrawing claims 1-2); Ex. 1028, 9 (same); Ex. 1029, 7 (canceling claims 1-2); Ex. 1030, 18 (same).

VII. LEVEL OF ORDINARY SKILL IN THE ART

44. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

45. In determining the characteristics of a hypothetical person of ordinary skill in the art of the '481 Patent at the time of the alleged invention, I considered several things, including the type of problems encountered in this field, and the rapidity with which innovations were made. I also considered the sophistication of the technology involved, and the educational background and experience of those actively working in the field, and the level of education that would be necessary to understand the '481 Patent. Finally, I placed myself back in the relevant periods of time, and considered the state of the art and the level of skill of the engineers working in this field in those times.

46. It is my opinion that a POSITA at the time of the '481 Patent would have had a Bachelor's degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. Additional education might compensate for a deficiency in experience, and vice-versa. I understand that, in the Intel Litigation, the Patent Owner agreed with my characterization of a POSITA. Ex. 1039, ¶13.

47. I also note that my opinions provided in this Declaration would not change in view of any minor modifications to this level of skill.

VIII. CLAIM CONSTRUCTION

48. It is my opinion that for purposes of this proceeding, the claim terms need not be construed to resolve the prior art issues presented in this Petition.

49. Nothing in this section should be construed as expressing any opinion as to whether the claims constitute patentable subject matter under 35 U.S.C. § 101, or whether they satisfy the definiteness, enablement, best mode, or written description requirements under § 112.

50. I understand that Patent Owner took positions on the meaning of certain claim terms in the Intel Litigation, which are listed below. Exs. 1017, 2020.

Claim Term	Patent Owner's Proposed Construction
"substrate"	Plain and ordinary meaning, where the plain and ordinary meaning is an "underlying layer"
"active region"	Plain and ordinary meaning ("a doped silicon region at the surface of a semiconductor device where a transistor can be formed")
"to aid carrier movement from .. [to/towards] .."	Plain and ordinary meaning
"well region"	Plain and ordinary meaning ("a doped region that surrounds the active region of a semiconductor device")
"active region .. within which transistors can be formed"	Plain and ordinary meaning ("a doped silicon region at the surface of a semiconductor device where a transistor can be formed")

51. I further understand that, in the Intel Litigation, the Court provided its “preliminary constructions” in advance of the claim construction hearing, in which the Court offered a “preliminary construction” of plain and ordinary meaning as to each of the above-listed terms. Ex. 1038. As mentioned above, I do not believe any terms need be construed to resolve the issues presented in this Petition because, in my opinion, as the Challenged Claims are unpatentable under either party’s proposed constructions (except for the term “active region ... within which transistors can be formed,” which I address under Patent Owner’s proposed construction). I reserve the right to respond to any purported claim constructions that Patent Owner raises.

IX. OVERVIEW OF THE PRIOR ART

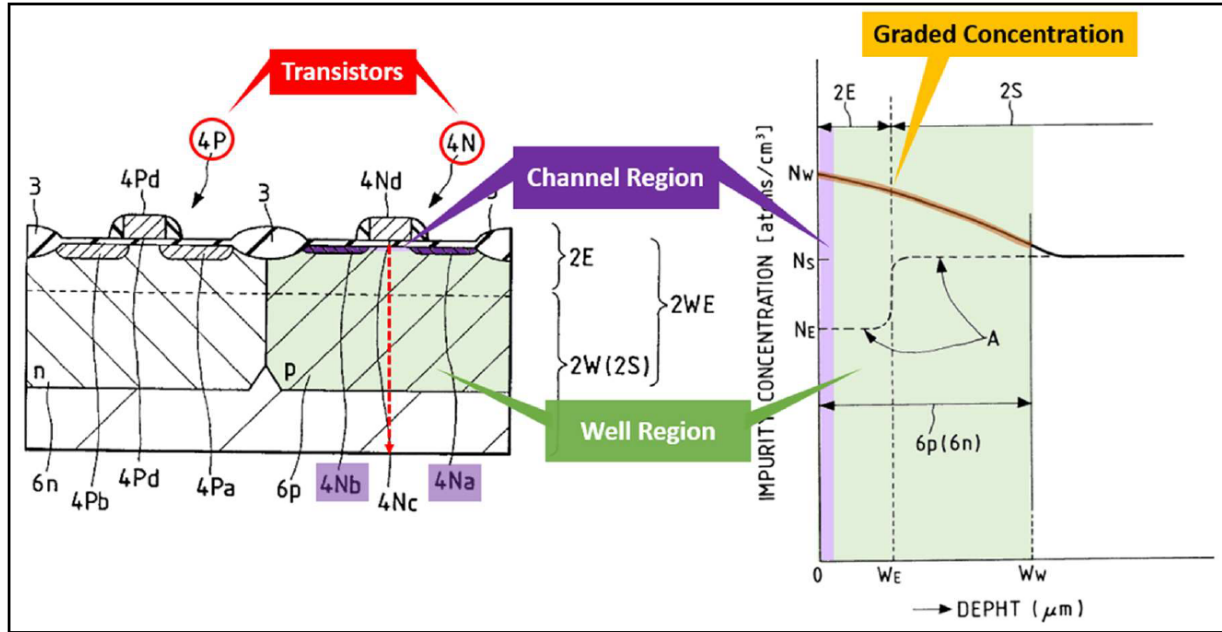
A. Kawagoe

52. Kawagoe discloses “a semiconductor integrated circuit device manufacturing method characterized in that said first semiconductor region is a well to be used for forming a complementary MOSFET CMOS (Metal-Oxide-Semiconductor-Field Effect-Transistor) circuit (*i.e.*, for forming a complementary MIS (Metal-Insulator-Semiconductor) FET circuit).” Ex. 1007, 3:32-38.

53. Kawagoe explains that, in its Embodiment 1, the “epitaxial layer 2E is doped ... in a concentration equal to the [concentration] of the substrate body 2S.” Ex. 1007, 6:65-7:3; *see also id.*, 8:40-52. In its Embodiment 4, “the impurity concentration of the semiconductor substrate body 2S is made higher than that of the

epitaxial layer 2E ... to improve the resistance to the latchup.” *Id.*, 15:13-17; *see also id.*, 15:26-40.

54. The figure below from Kawagoe illustrates a conventional twin-well CMOS structure. For context, a conventional twin-well CMOS structure includes “two separate wells [] formed for *n*- and *p*-channel transistors.” Ex. 1008B, 387; *see also, e.g.*, Ex. 1008A, 227, FIG. 7-3 (showing a “[c]ross-section of a twin-well CMOS structure built in a *p*-epitaxial layer and a *p*⁺ substrate”); Ex. 1008B, 382, FIG. 6-8(c) (illustrating a “CMOS circuit[] [] designed using ... twin-well technology”). The figure below from Kawagoe (relating to Embodiment 4) shows source-drain regions (purple) of an NMOS transistor formed in a *p*-well (light green) and the source-drain regions (green) of a PMOS transistor formed in an *n*-well (light purple). Ex. 1007, 8:46-9:6, 9:32-54, 14:46-55, 15:26-40, 18:18-23.



Id., FIGS. 17 and 23.

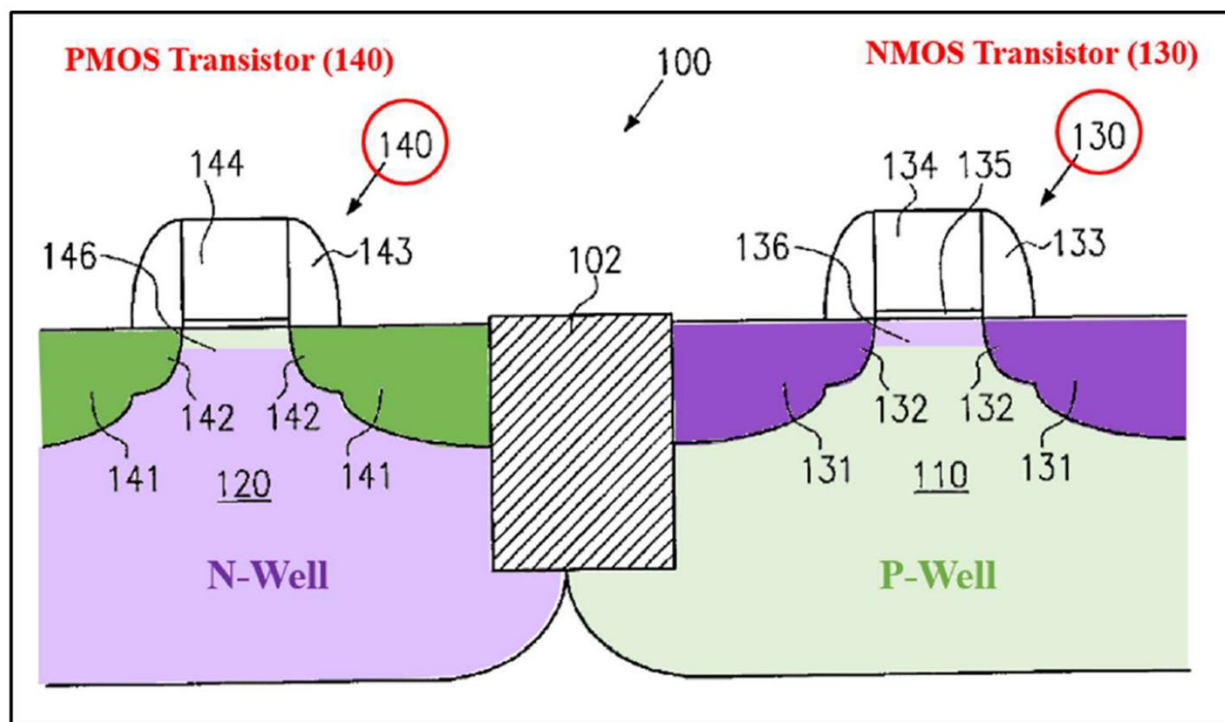
56. Kawagoe explains that “the impurity concentration of the p-well 6p is given such a gradient that it is *gradually lowered* in the depthwise direction from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α -ray is lowered.” Ex. 1007, 16:2-7.⁴ Kawagoe further explains that “the electrons produced by the α -ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well 6p so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p.” *Id.*, 16:7-11.

B. Wiczorek

⁴ All emphases added unless otherwise noted.

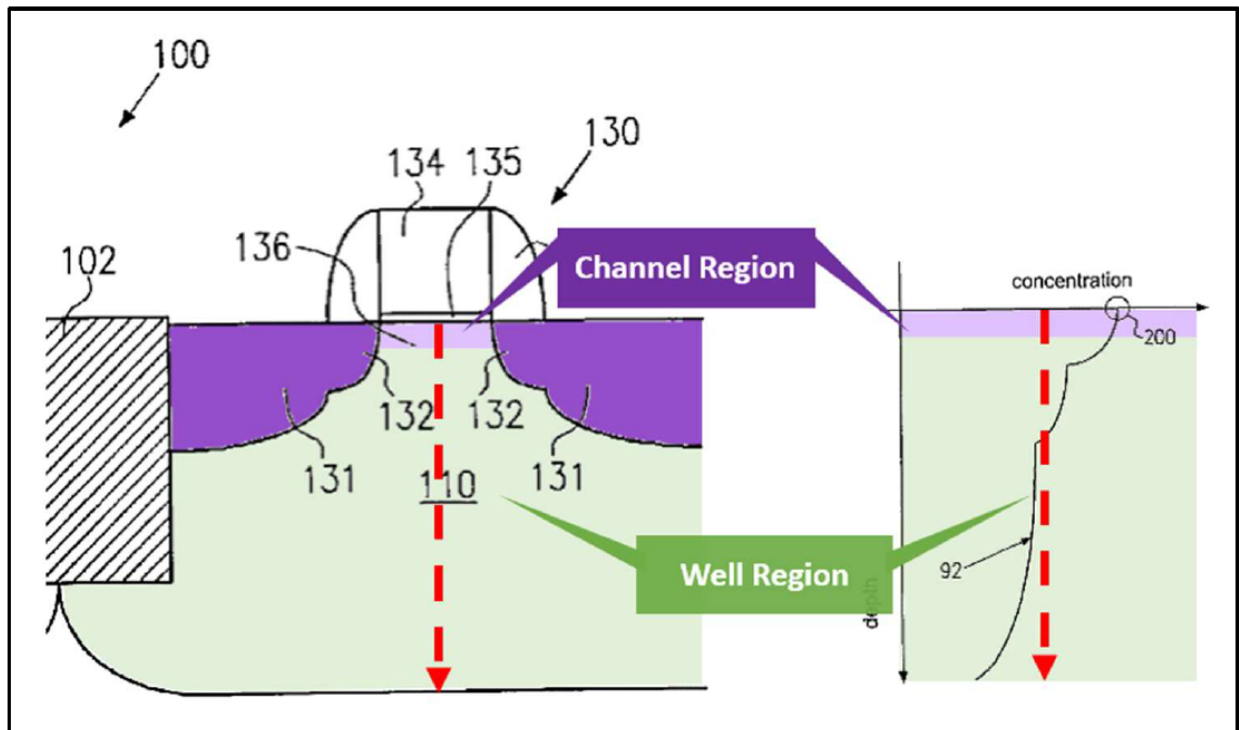
57. For purposes of this Petition, I rely on Wieczorek's description of conventional prior art CMOS devices, such as the twin-well CMOS device illustrated in Figure 1b below. Ex. 1006, [0007], [0012], [0020]-[0021]; *see also* Section IX.A (discussing conventional twin-well CMOS devices).

58. The semiconductor device 100 illustrated in the figure below from Wieczorek is "a complementary MOS transistor pair." Ex. 1006, [0007]. The figure below illustrates an NMOS transistor (right) having source-drain and channel regions (purple/light purple) formed in a p-well (light green), and a PMOS transistor (left) having source-drain and channel regions (green/light green) formed in an n-well (light purple). *Id.*, [0007], [0012].



Ex. 1006, FIG. 1b.

59. Referring to Figs. 1b and 2b below, Wieczorek teaches that, following heat treatments, the dopant profile (200) becomes substantially uniformly distributed in the vicinity of the surface of the semiconductor device 100, compared to the initially retrograde profile. Ex. 1006, [0011]. Nonetheless, Wieczorek explains that graded dopant concentrations in such prior art CMOS devices peak at the surface of the substrate and decrease with depth, as shown below. Ex. 1006, [0004], [0007]-[0013], [0020]-[0021].



Id., FIGS. 1b and 2b; *see also id.*, [0021] (explaining that the Fig. 2b profile (right) corresponds to the Fig. 1b semiconductor device (left)).

C. Wolf

60. *Silicon Processing For The VLSI Era* by Stanley Wolf is a four volume textbook related to semiconductor devices, with particular focus on CMOS devices. Exs. 1008A-D. I am familiar with the Wolf textbook. An internet search for this textbook title limited to the “.edu” domain yields over 800 results. Thus, it is clearly used as a teaching resource in engineering courses in many, many universities and is widely cited in scientific works. The Wolf textbook provides helpful context regarding the disclosures of Kawagoe and Wieczorek regarding CMOS technology.

D. Gupta

61. Gupta “relates to the field of complimentary [(sic)] metal oxide semiconductor (CMOS) circuits, and more particularly to [] layouts for CMOS circuits.” Ex. 1014. 1:7-10. Gupta reflects the common knowledge of a POSITA when it explains that “[c]onservation of semiconductor area is a primary goal in semiconductor chip development” and a common technique to conserve area is “by placing transistors so as to share diffusion area [(active region)].” *Id.*, 1:32-54, 2:17-21.

E. Silverbrook

62. Silverbrook “relates substantially to the concept of a disposable camera having instant printing capabilities and in particular, discloses An Integrated Camera Circuit included Sensor and Drive Transistors.” Ex. 1042, 1:8-11. Silverbrook discloses that the camera system could include (among other components): “a

processing unit for controlling the operation of the camera system; a program ROM utilized by the processing unit; a CMOS active pixel image sensor for sensing the image; [and] a memory store for storing images and associated program data[.]” *Id.*, 2:10-26. As such Silverbrook reflects the common knowledge of a POSITA at the time that CMOS techniques and devices can be applied to optical image sensors.

X. SPECIFIC GROUNDS FOR PETITION

A. Ground I:

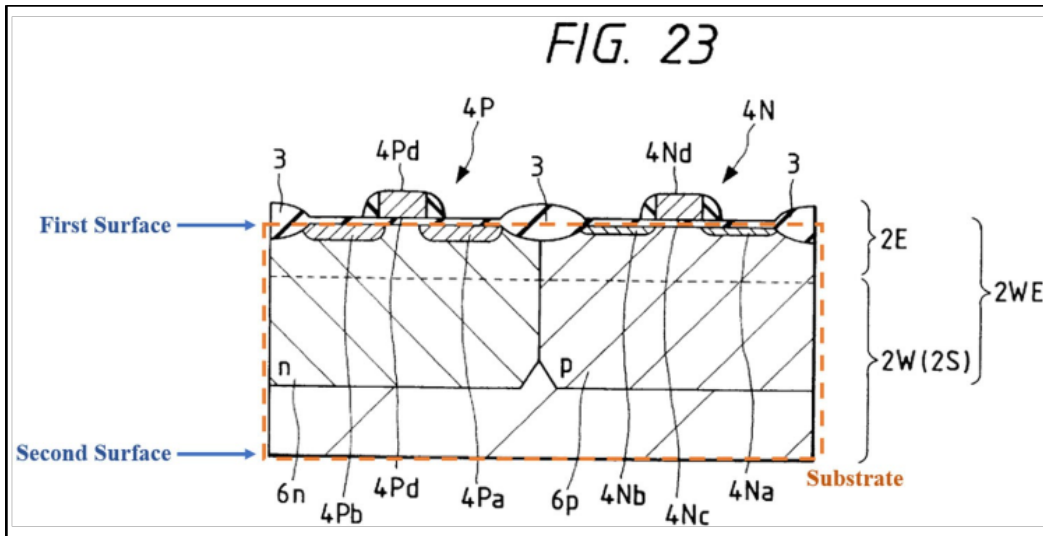
63. In my opinion, Kawagoe renders claims 1-9, 12-14, 16-27, and 30-36 obvious.

1. Independent Claim 1

a. Preamble: “A semiconductor device, comprising”

64. To the extent the preamble is limiting, in my opinion, Kawagoe discloses it. Kawagoe discloses a “semiconductor integrated circuit device” and process for making the same. *See* Ex. 1007, Title, 1:13-23, 14:46-67, FIGS. 16-17, 23. For Ground I, I primarily focus on the twin-well CMOS device in Figure 23 (Embodiment 4) of Kawagoe, fabricated on a uniformly-doped epitaxial substrate, as taught in Embodiment 1 of Kawagoe.⁵ *See* Section X.A.1.b.

⁵ Figures 16, 17 and 23 are all directed to the same Embodiment 4 of Kawagoe. *See* Ex. 1007, 14:46-60. Figure 23 shows the same twin-well CMOS structures depicted

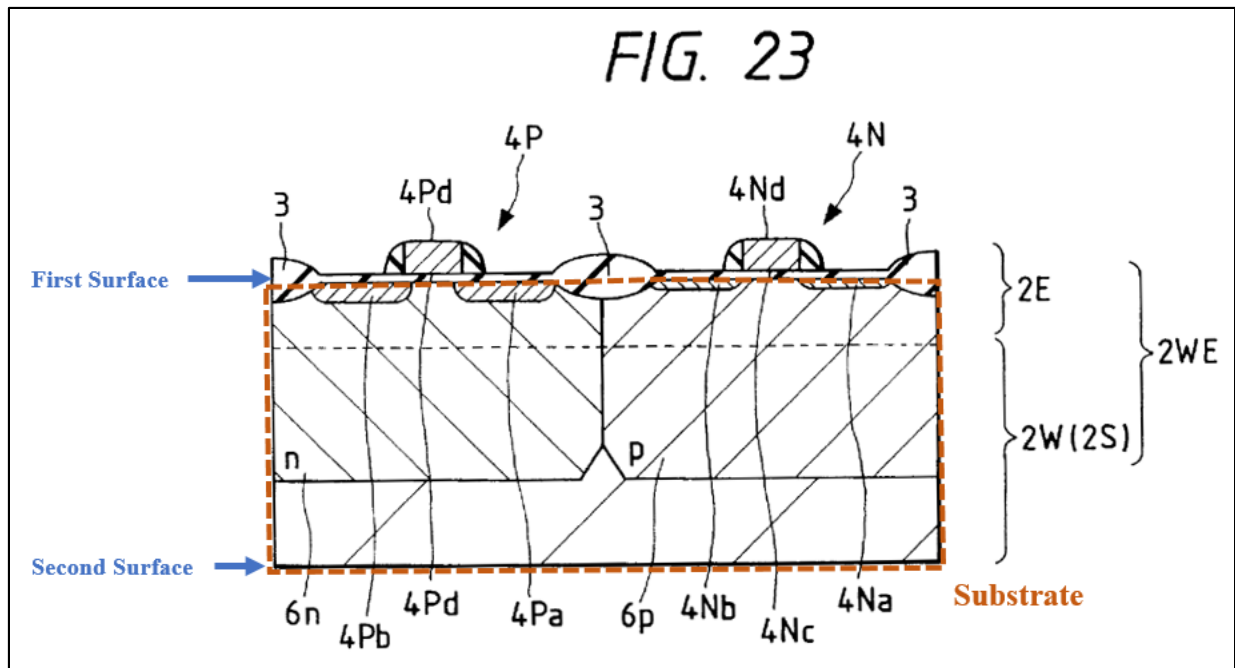


Ex. 1007, FIG. 23.

b. Element [1.1]: “a substrate of a first doping type at a first doping level having first and second surfaces;”

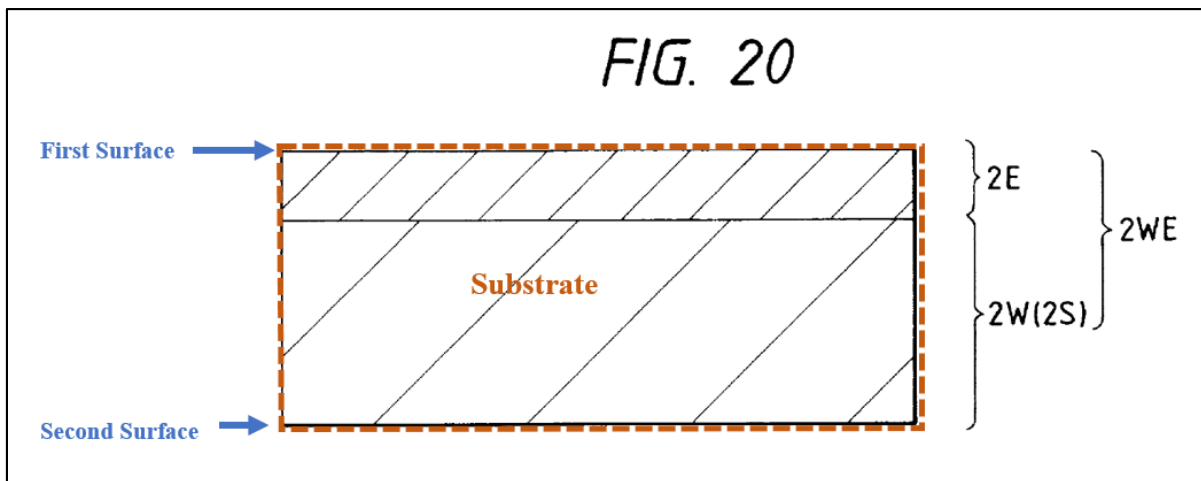
65. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. Kawagoe discloses a substrate (“semiconductor substrate 2”) of a first doping type (p- type) having a silicon “epitaxial layer 2E [that] is doped with a *p-type* impurity such as boron” formed over non-epitaxial “semiconductor substrate body 2S [also] doped with a *p- type* impurity such as boron...” Ex. 1007, 14:61-15:12, 6:50-7:3. The substrate (shown below in orange) has a top surface (“first surface”) and a bottom surface (“second surface”), as labeled below.

in Figure 16 without the metal layers that are not recited in the Challenged Claims.
Id., 17:10-18:38.



Ex. 1007, FIG. 23.

66. In my opinion, Kawagoe satisfies element [1.1] under Patent Owner's position that the term "substrate" should be given its plain meaning and under Petitioner's proposed construction that a substrate is the initial material within which or on which Kawagoe's "semiconductor integrated circuit device 1" is later fabricated. *See* Section VIII; Ex. 1007, 6:51-56, 14:61-67, 17:10-18:38.



Ex. 1007, FIG. 20. Specifically, 2WE epitaxial wafers are produced by manufacturers and supplied as the starting point material for subsequent processing by integrated circuit (IC) foundries.

67. As I explain in more detail below, Ground I relies on a uniformly-doped epitaxial substrate in which the silicon epitaxial layer 2E of the substrate is doped at the same level as the silicon substrate body 2S, so that the entire substrate in Figure 20 is “at a first doping level” as recited in the claims. Ex. 1007, 6:60-7:3.

68. **“at a first doping level”** – Kawagoe teaches an epitaxial substrate (2S+2E), illustrated in Figure 20, in which the non-epitaxial silicon substrate body (2S) is either doped at the same level or at a higher level compared to the epitaxial silicon layer (2E). For example, Embodiment 1 describes a uniformly-doped epitaxial substrate in which the “epitaxial layer 2E is doped ... in a concentration *equal* to the [concentration] of the semiconductor substrate body 2S, e.g., 1.3×10^{15} atoms/cm³.” Ex. 1007, 6:60-7:3; *see also id.*, Abstract (describing “an epitaxial layer which contains an impurity of the *same* conduction type [and at] ... the *same concentration*” as the bulk substrate), 2:57-3:9 (same). I note that this uniformly-doped epitaxial substrate is Kawagoe’s “benchmark” substrate that is repeatedly discussed in other embodiments, including in Embodiment 4. *Id.*, 12:64-65, 13:12-15, 13:66-67, 14:18-20, 15:7-25.

69. Embodiment 4 introduces the option of a latchup-resistant substrate in which “the impurity concentration of the semiconductor substrate body 2S is made **higher** than that of the epitaxial layer 2E . . . **to improve** the resistance to latchup.” Ex. 1007, 15:13-17; *see also id.*, 3:60-63 (explaining that there is a high “degree of freedom for setting the impurity concentration” in the disclosed semiconductor substrate so “as to facilitate the control of the formation”). In this regard, Kawagoe teaches that the “substrate body 2S is doped with a p-type impurity such as boron at a concentration of about 1.5×10^{15} atoms/cm³. *Id.*, 14:64-67.

70. In my opinion, a POSITA would have understood that Kawagoe teaches forming the twin-well CMOS device illustrated in Figure 23 (Embodiment 4) on either a uniformly-doped epitaxial substrate described in Embodiment 1 or the optional latchup-resistant substrate described in Embodiment 4. Kawagoe emphasizes the benefits of Embodiment 1’s uniformly-doped epitaxial substrate and explains that the substrate used in Embodiment 4 is formed “**as in the foregoing embodiment 1** so that . . . the cost for the semiconductor substrate 2 is lowered to about one half.” Ex. 1007, 15:7-25. A POSITA would have understood that using an epitaxial layer may increase yield and reduce overall cost. Specifically, a POSITA would have appreciated that Kawagoe teaches that there is a tradeoff between improving latchup resistance and minimizing manufacturing cost. This understanding is consistent with the teachings of Wolf, for example. *See* Ex. 1008C,

524 (“There are many trade-offs involved in the optimization of a CMOS process” including “fabrication cost[] and susceptibility to latchup.”).

71. In my opinion, a POSITA would have been motivated to use a uniformly-doped epitaxial substrate (as discussed for Embodiment 1) to form the twin-well CMOS device of Figure 23 because this substrate provides “excellent film quality” that “drastically reduce[s] the defect densities of the gate insulating films” and thus “improve[s] the performance, reliability and production yield” of the device. Ex. 1007, 12:8-40; *see also id.*, 15:7-25. This substrate is also easier to manufacture, which helps “lower the cost” of the substrate and the chip. *Id.*, 12:8-40. In particular, POSITA would have appreciated Kawagoe’s recognition that a semiconductor substrate having an “impurity high in concentration[] is [undesirably] expensive.” *Id.*, 2:15-18. To avoid this, Kawagoe repeatedly teaches that using a lower-doped substrate body (as in Embodiment 1) as opposed to a more heavily-doped substrate body, can result in lower cost. *See id.*, 3:38-45; 7:13-18; 12:19-24. Notably, while the Embodiment 4 is disclosed as having an improved latchup resistance as an effect, this comes with a trade-off—the substrate body is doped at a higher concentration (1.5×10^{15} atoms/cm³) as compared to the substrate body of Embodiment 1 (1.3×10^{15} atoms/cm³). *See id.*, 6:62-64, 14:64-67.

72. Thus, in my opinion, a POSITA opting to maximize cost savings over latchup resistance would have been motivated to instead use the uniformly-doped

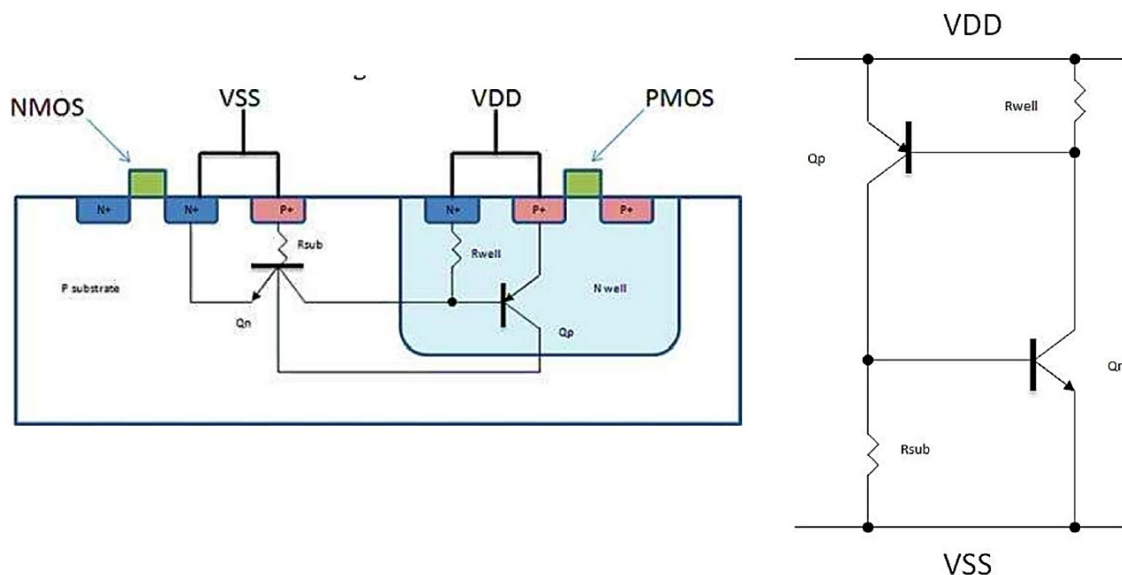
epitaxial substrate (i.e., doped at both 1.3×10^{15} atoms/cm³ for the substrate body and epitaxial layer, as disclosed for Embodiment 1) as the starting material in lieu of Embodiment 4's latchup-resistant substrate to form the twin-well CMOS devices of Figure 23. A POSITA would understand that the use of a uniformly-doped epitaxial substrate as the starting material in lieu of Embodiment 4's latchup-resistant substrate to form the twin-well CMOS devices of Figure 23 is a simple substitution of one known element with another known, closely related element, both of which are described in Kawagoe. In addition, this substitution would have been obvious to try because it involves nothing more than choosing one of two ways of doping an epitaxial substrate that are both described in Kawagoe, and both ways of doping the substrate have predictable effects on the devices formed using those substrates.

73. In my opinion, twin-well CMOS devices (illustrated in Figure 23) fabricated on a uniformly-doped epitaxial substrate would have worked for their intended purpose. As discussed in Wolf, twin-well CMOS devices were commonly formed over a “*uniform*, lightly doped p^- or n^- type substrate” that provides no improved latchup resistance. Ex. 1008C, 523, *id.*, 530 (“With the twin-tub [(twinwell)] approach, ... two separate wells are formed for n- and p-channel transistors on a lightly doped substrate ...”); Ex. 1008B, 387-389; Ex. 1007, 2:57-65 (discussing a uniform “lightly doped” epitaxial substrate).

74. In my opinion, there would be a reasonable expectation of success because Kawagoe describes in detail the use of both the uniformly-doped epitaxial substrate and the latchup-resistant substrate in forming CMOS devices, and repeatedly emphasizes their similarity. Ex. 1007, 8:40-52, 12:8-40, 14:58-60, 15:7-12 (substrate), 15:18-25 (epitaxial layer), 15:26-40 (transistors), 19:48-63 (describing latchup resistance as just another “effect” over Embodiment 1). A uniformly-doped *epitaxial* substrate is also better, in my opinion, than the bulk (non-epitaxial) substrate commonly used to fabricate twin-well CMOS devices. *Id.*, 1:33-40 (“The epitaxial wafer is advantageous [compared to bulk wafer/substrate] in that ... the gate insulating film to be formed over the epitaxial layer can have excellent breakdown characteristics to drastically reduce the defect density of the gate insulating film.”); *id.*, 12:8-40; Ex. 1008B, 387-88 (discussing twin-well CMOS devices fabricated over bulk substrate).

75. Kawagoe characterizes the improved latchup tolerance provided by Embodiment 4’s optional latchup-tolerant substrate as just another “effect[] [that] can be achieved in addition to those of the foregoing embodiment 1,” Ex. 1007, 19:49-63, as opposed to being vital to its operation. In my opinion, and consistent with Kawagoe’s teachings, a POSITA would have understood that having a uniformly-doped epitaxial substrate is a perfectly suitable choice of substrate because, among other benefits, it “drastically reduce[s] the defect densities of the

gate insulating films” of CMOS transistors. Ex. 1007, 12:8-40. Moreover, in my opinion, a POSITA would have understood that susceptibility to latchup (a “short-circuit” failure condition in poorly designed circuits) may not be a concern for all CMOS chip. *See* Ex. 1008B, 406 (“four conditions must exist in a CMOS circuit in order for latchup to occur.”); Ex. 1026, 1 (“several conditions must be met” to cause latchup). For example, in my opinion, a POSITA would have understood that latchup is dependent upon parasitic bipolar devices associated with the NMOS and PMOS structures of typical CMOS. The latchup phenomenon was first described in 1973 in a paper by Gregory and Shafer (Ex. 1026) and has been analyzed in more detail in numerous publications and books since that time. The simplified figure below is commonly used to illustrate the basic issue. The circuit on the right is a redrawing of the circuit super imposed on the device structure shown on the the[sic] left.



If there is enough current (and associated voltage drop) through R_{sub} and/or R_{well} , and the current gain through the parasitic bipolar transistors is greater than 1, the cross coupled parasitic bipolar devices create a self-sustaining current that will flow through the circuit between VDD and VSS. That condition is known as latchup. This condition is avoided if the current gain of the parasitic bipolar devices is reduced, typically by increasing spacing as was well-known in the art and described in Wolf, Ex. 1008B, 381 (“Latchup tolerance can [] be improved by spacing n - and p -channel transistors farther apart”). The R_{sub} and R_{well} resistors can be reduced by increasing dopant densities or using retrograde wells. Currents which lead to latchup can also be removed from the structure via additional well and substrate contacts and/or the addition of guard rings. Ex. 1008B, 419 (“Increasing the number of well contacts to V_{DD} reduces latchup susceptibility” and thus “can serve as an alternative approach to improving latchup immunity.”). If these steps are taken, as was well-known in the art and described in Wolf, a chip can be fabricated on an epitaxial substrate that is uniformly doped, whereby the bulk substrate 2S and epitaxial layer 2E are doped at the same level, as described in Kawagoe’s Embodiment 1, without being susceptible to latchup.

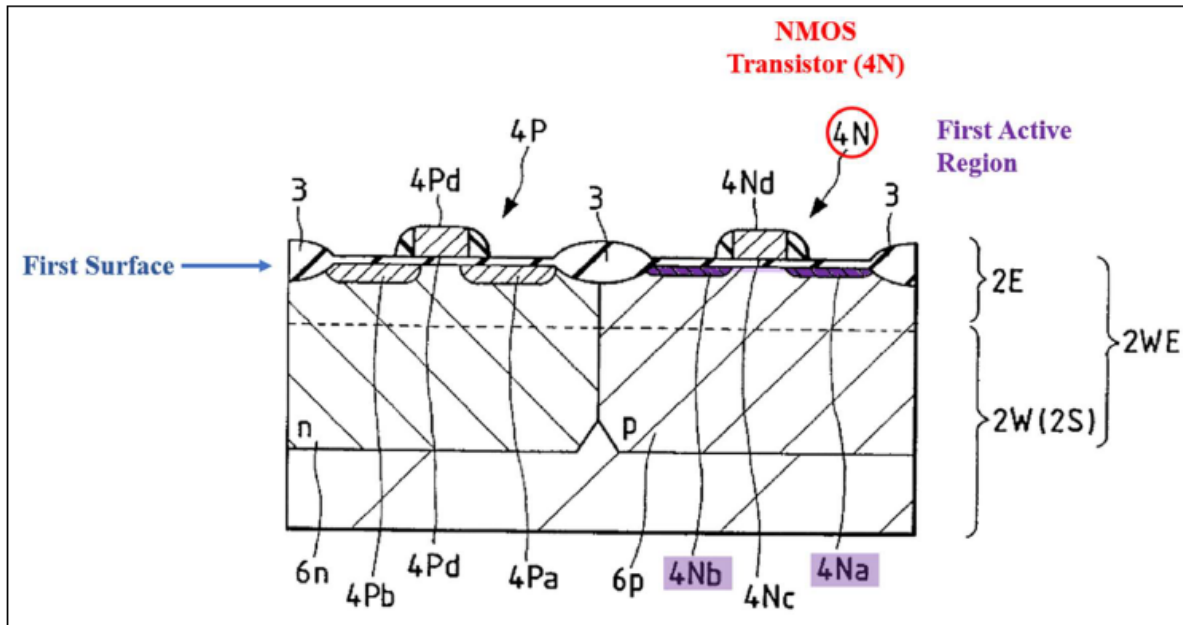
76. My opinion is also grounded in the well-known fact that both single-well and twin-well CMOS devices were commonly fabricated on uniformly-doped bulk substrates that provide no improved latchup resistance. *See, e.g.*, Ex. 1008B,

387-388 (“With the [twin-well] approach, ... [t]he substrate may be [] a lightly doped wafer ...”), 452 (example 6.7). And as I described above, even if latchup were to remain a concern, a POSITA would have understood, in my opinion, that improved latchup resistance can be achieved by other means unrelated to the choice of substrate, such as through careful circuit layout. Ex. 1008B, 381 (“Latchup tolerance can [] be improved by spacing *n*- and *p*-channel transistors farther apart”), 419 (“Increasing the number of well contacts to V_{DD} reduces latchup susceptibility” and thus “can serve as an alternative approach to improving latchup immunity.”).

c. Element [1.2]: “a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;”

77. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. Kawagoe discloses “semiconductor regions 4Na and 4Nb ... for forming the *source-drain regions* of the nMOS [n-channel transistor] 4N.” Ex. 1007, 8:66-67; *see also, id.*, 3:35-37, 8:46-52, 14:46-55, 15:26-40. The source-drain regions 4Na and 4Nb (purple) form part of the claimed first active region, which also includes the channel region (light purple) in between the source-drain regions 4Na and 4Nb and below the gate insulating film 4Nc. Ex. 1007, 8:46-65, 14:46-55, 15:26-40; Ex. 1008B, 299-300 (“The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The active regions are those in which transistor action occurs; i.e., the *channel* and the heavily doped *source* and

drain regions.”), FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e). As shown in Figure 23 below, nMOS transistor 4N is formed in the first active region, which is adjacent the first surface of the substrate.

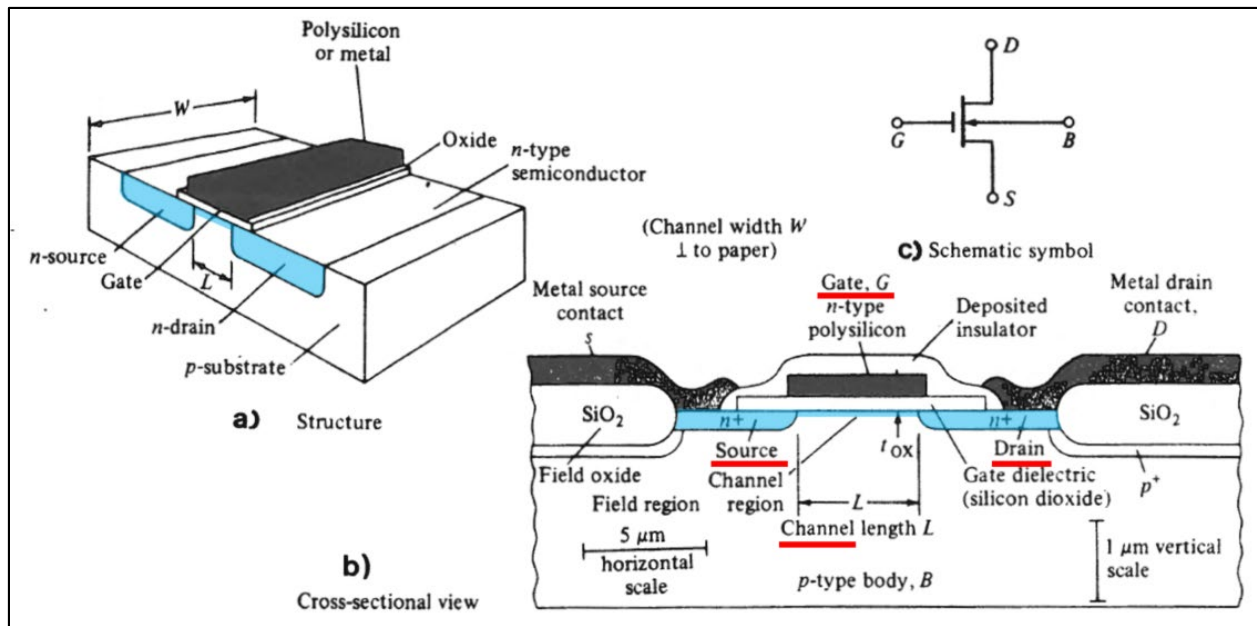


Ex. 1007, FIG. 23. “The semiconductor regions 4Na and 4Nb are doped with an ***n-type impurity***” and thus, in my opinion, have a second doping type (n- type) opposite in conductivity to the first doping type (p- type) of the substrate. *Id.*, 8:67-9:3, 14:46-55, 15:26-40.

78. While Figure 23 above shows an exemplary nMOS (n-channel) transistor 4N formed in the first active region for illustrative purposes, in my opinion, forming multiple nMOS transistors would have been obvious as a mere duplication of parts lacking unexpected results. Indeed, a POSITA would have recognized that forming multiple transistors in Kawagoe's active region would minimize chip area,

as good layout practice dictates and as described in many references such as Gupta and Maziasz. Ex. 1014, 1:52-54, 2:17-21. Further, POSITA would have appreciated that at the relevant time, an actual device would have had many transistors in the same active region. In any event, I understand that according to Patent Owner's representations in the Intel Litigation, an "active region ... within which transistors can be formed" means "an active region ... where *a transistor* can be formed." Ex. 1020, 31.

79. In my opinion, Kawagoe satisfies element [1.2] under Patent Owner's position that the term "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed." Ex. 1020, 20; *see also* Section VIII. This is consistent with my understanding, and Wolf's teaching, that an active region of a MOS transistor is "[its] channel and [its] heavily doped source and drain regions," highlighted in blue in the figure from Wolf below. Ex. 1008B, 299.



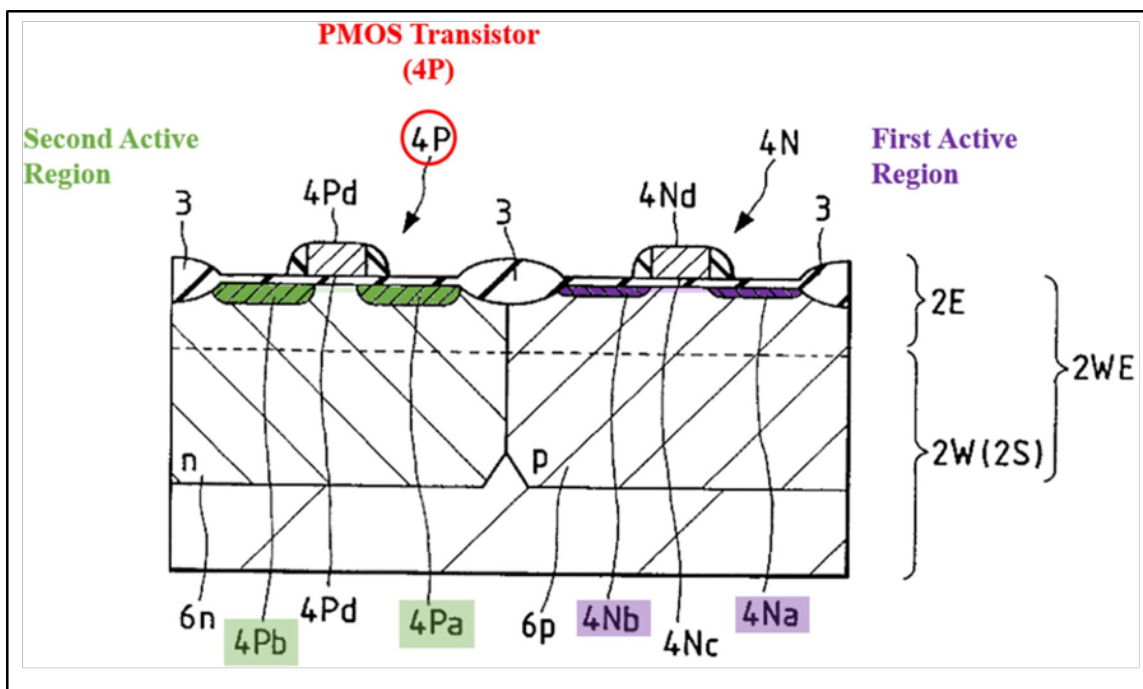
Ex. 1008B, 299, FIG. 5-1; *see also id.*, 298-301, FIGS. 5-2, 6-4.

- d. **Element [1.3]: “a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;”**

80. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. Kawagoe discloses “semiconductor regions 4Pa and 4Pb ... for forming the source-drain regions of the pMOS [p-channel transistor] 4P.” Ex. 1007, 3:35-37, 8:46-52, 9:41-48, 15:26-40. The source-drain regions 4Pa/4Pb (green) are part of the claimed second active region, which also includes the channel region (light green) in between them and below the gate 4Pd. Ex. 1007, 8:46-57, 9:41-46, 14:46-55, 15:26-40; Ex. 1008B, 299-301, FIGS. 5-1, 5-2, 6-4; Section X.A.1.c. As shown in Figure 23 below, pMOS transistor 4P is formed in the second active region

(green/light green), which is separate from and disposed adjacent to the first active region (purple/light purple). Ex. 1007, 14:46-55.

81. In my opinion, a POSITA would understand that adjacent active regions are separated by an isolation region (such as insulating film 3). Ex. 1008A, 818-20, FIG. 16-11(f). In fact, claim 6, which depends from claim 1, claims that “the first active region and second active region are each separated by at least one isolation region.” Ex. 1001, Cl. 6.



Ex. 1007, FIG. 23.

82. While Figure 23 illustrates an exemplary pMOS (p-channel) transistor 4P formed in the second active region, in my opinion, forming multiple pMOS transistors in the second active region would have been obvious. Section X.A.1.c. In any event, I understand that according to Patent Owner’s representations in the

District Court Case, an “active region ... within which transistors can be formed” means “an active region ... where *a transistor* can be formed.” Ex. 1020, 31.

83. In my opinion, Kawagoe satisfies element [1.3] under Patent Owner’s position that the term “active region” means “a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed.” Section X.A.1.c.

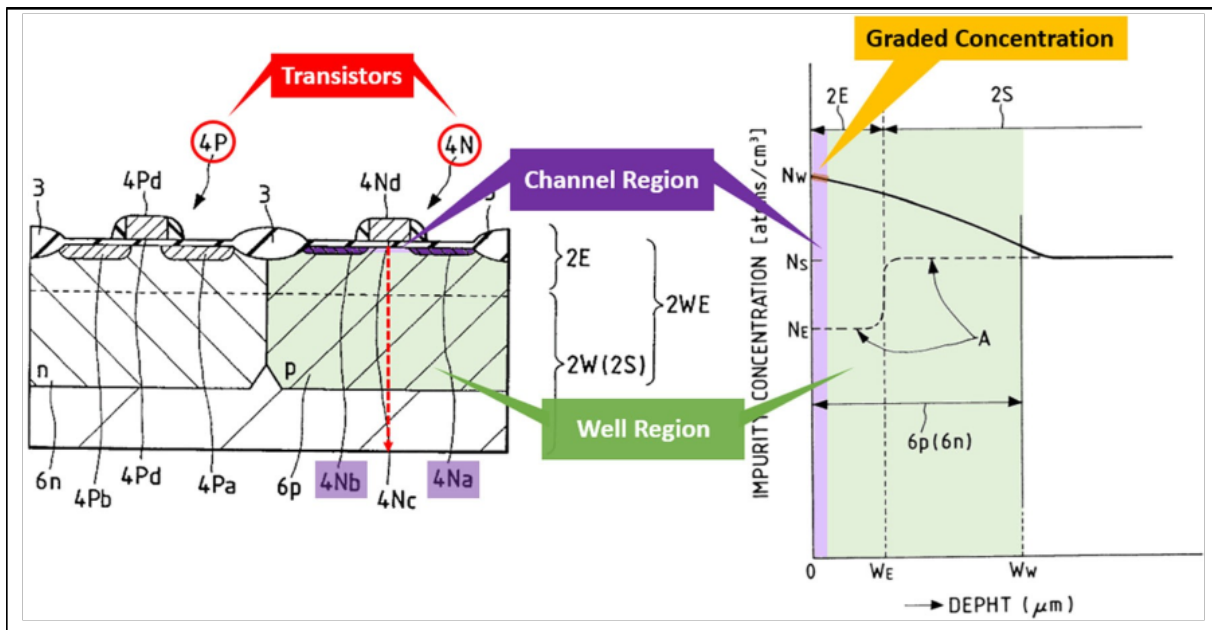
e. Element [1.4]: “transistors formed in at least one of the first active region or second active region;”

84. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. *See* Sections X.A.1.c-d.

f. Element [1.5]: “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and”

85. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. As illustrated in my annotation of Figure 23 (below left), a channel region (light purple) formed at the top surface of the substrate connects the source-drain regions 4Na and 4Nb (purple) of transistor 4N. *See* Ex. 1008B, 298 (“A channel region in the semiconductor under the gate electrode separates the source and drain”), 300-301 (“When positive bias is applied to an NMOS transistor gate ... an *n-type* channel connects the source and drain regions”), FIG. 5-2; Ex. 1007, 8:46-47 (“nMOS” is a shorthand for “n-*channel* MOS.FET”), 8:60-67 (“The

semiconductor regions 4Na and 4Nb are regions for forming the source-drain regions of the NMOS 4N.”), 14:46-55, 15:26-30 (“The p-well 6p is formed with the nMOS 4N.”), 15:37-40. Based on Patent Owner’s representation in the District Court Case that the channel is “a thin layer below the surface” connecting the source and drain, Patent Owner does not appear to dispute this.



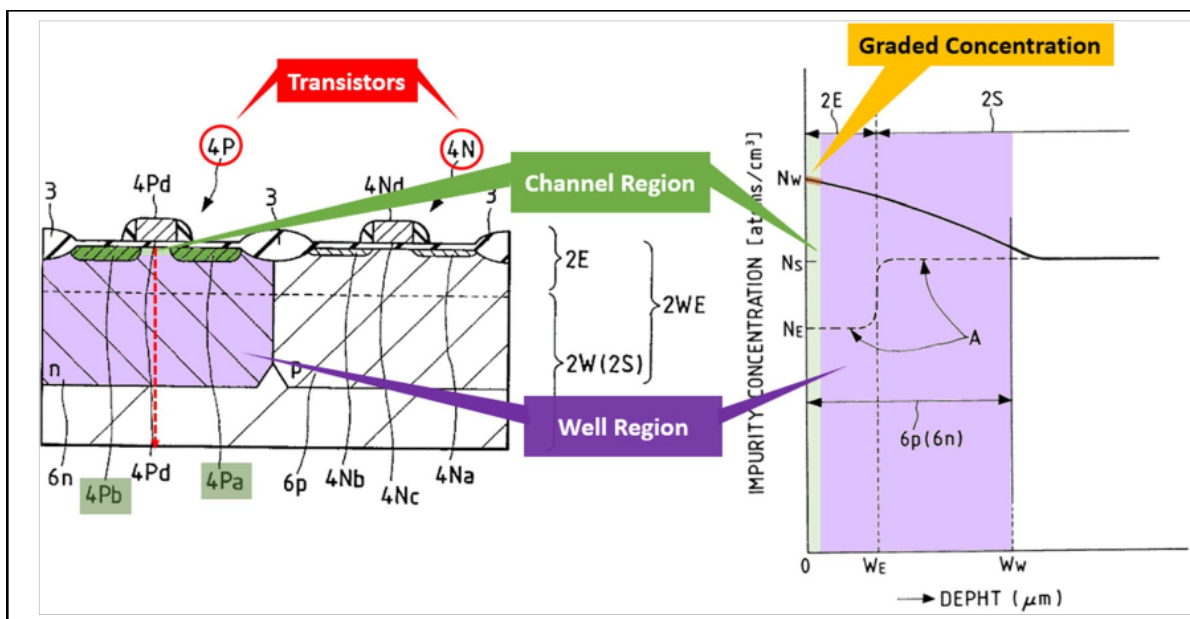
Ex. 1007, FIGS. 17, 23.

86. Kawagoe’s Figure 17 (above right) illustrates the doping concentration measured for example along the red dotted line in Figure 23 (above left), which starts from the top surface of the substrate (at depth 0) and includes the doping profile in the channel region (light purple). Ex. 1007, 5:41-45 (“Figure 17 is an impurity distribution diagram in the semiconductor integrated circuit device of FIG. 16 and has an abscissa indicating the depth from the surface of an epitaxial layer 2E and an

ordinate indicating an impurity concentration”). As Figure 17 shows, the dopant concentration is “gradually lowered in the depthwise direction *from the principal surface* (having an impurity concentration N_w) of the epitaxial layer 2E.” Ex. 1007, 15:62-16:40; *see also id.*, 16:21-26 (noting that N_w is the concentration at the well surface). The dopant concentration is thus graded in at least the channel region of transistor 4N, which is a portion of the first active region formed at “the principal surface” (top surface) of the epitaxial layer 2E. As shown in Figure 17, Kawagoe’s graded dopant concentration is in fact downward-sloping from the top surface of the substrate and all the way through the entire depth of the channel region (light purple) and the underlying well region (green)—from depth=0 at the top surface of the epitaxial substrate to beyond depth= W_w where W_w is the depth at the bottom of the p-well 6p. Ex. 1007, 15:32-36. I note that, while Figure 17 depicts the dopant concentration sloping at such a degree so as to level off at N_s (the dopant concentration of the substrate body) beyond the depth W_w , a POSITA would have appreciated that when the device of Figure 23 is implemented using a uniformly-doped substrate as in Embodiment 1, in which the doping levels of the epitaxial layer (N_E) and substrate body (N_s) are equal, the downward slope through the p-well 6p would have the same general profile but steeper than as depicted in Figure 17 above.

87. In my opinion, the same applies to the channel region of pMOS transistor 4P (a portion of the second active region), as illustrated below. Ex. 1007,

15:62-16:2 (“p-well 6p and n-well 6n have their impurity concentrations gradually lowered in the depthwise direction from the principal surface [] of the epitaxial layer 2E.”), 9:41-48, 14:46-55, 15:32, 15:37-40; Ex. 1008B, 298-301, FIGS. 5-2, 6-4.



Ex. 1007, FIGS. 17, 23. Thus, in my opinion, Kawagoe discloses “at least a portion of” the first and second active regions (the channel regions) having a downward-sloping graded dopant concentration. I again note that, as POSITA would have appreciated, when the device of Figure 23 is implemented using a uniformly-doped substrate as in Embodiment 1, in which the doping levels of the epitaxial layer (N_E) and substrate body (N_s) are equal, the downward slope through the n-well 6n would have the same general profile but steeper than as depicted in Figure 17 above.

88. Kawagoe further explains that, consistent with the claimed requirement, such downward-sloping graded dopant concentration aids the

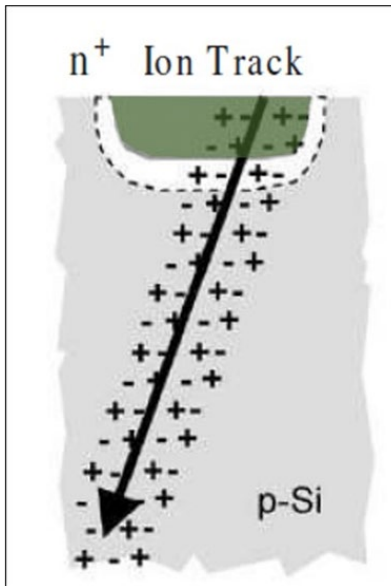
movement of carriers from the top surface of the epitaxial layer (claimed “first surface”) to the bottom surface of the substrate (claimed “second surface”):

[T]he impurity concentration of the p-well 6p is given such a gradient that it is ***gradually lowered in the depthwise direction*** from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α -ray is lowered. Specifically, the ***electrons produced by the α -ray are attracted to the substrate body 2S by that concentration gradient*** [] so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p.

Ex. 1007, 16:2-11.⁶

89. During a so-called single event upset (SEU), an α -ray generates millions of carriers, some of which are produced in or near the active region at the top surface of the substrate, as illustrated in the figure below. Ex. 1009, 431 (“A[n] [α -]particle can induce SEU when it strikes at the channel region of an off nMOS transistor or the drain region [(green)] of an off pMOS transistor.”)

⁶ Kawagoe also states that “electrons produced by the α -ray [are] ... prevented from entering the p-well 6p ...” Ex. 1007, 16:7-9. This refers to electrons created by an α -ray in the substrate body below the wells, which is by far the largest volumetric region of any chip. See Ex. 1009, FIG. 2.



Id., FIG. 2. Kawagoe teaches that those carriers are “attracted to the substrate body by [the] concentration gradient” of the graded dopant concentration illustrated in Figure 17. Ex. 1007, 16:2-11.

90. In light of the above, it is my opinion that Kawagoe satisfies element [1.5] under Patent Owner’s position that the term “to aid carrier movement from the first surface to the second surface of the substrate” should be accorded plain meaning. *See* Section VIII. I understand that, according to Patent Owner’s representations in the District Court Case, the claims recite that “carriers [must move] in a particular direction (from the surface layer to the substrate).” Ex. 1020, 29. Also, according to Patent Owner’s statements in the District Court case, “when the dopant concentration is graded in a particular direction, [certain] charge carriers will move in the [same] gradient direction ...”. *Id.*, 2. Here, Kawagoe’s Figure 17 shows that the dopant concentration is downward-sloping, with concentration

decreasing with increasing depth from the top towards the bottom of the substrate, and thus, according to Patent Owner's representations in the District Court Case and Patent Owner's representation to the Patent Office, discussed below in Section X.A.1.g, this graded dopant concentration causes carriers to move deeper into the substrate.

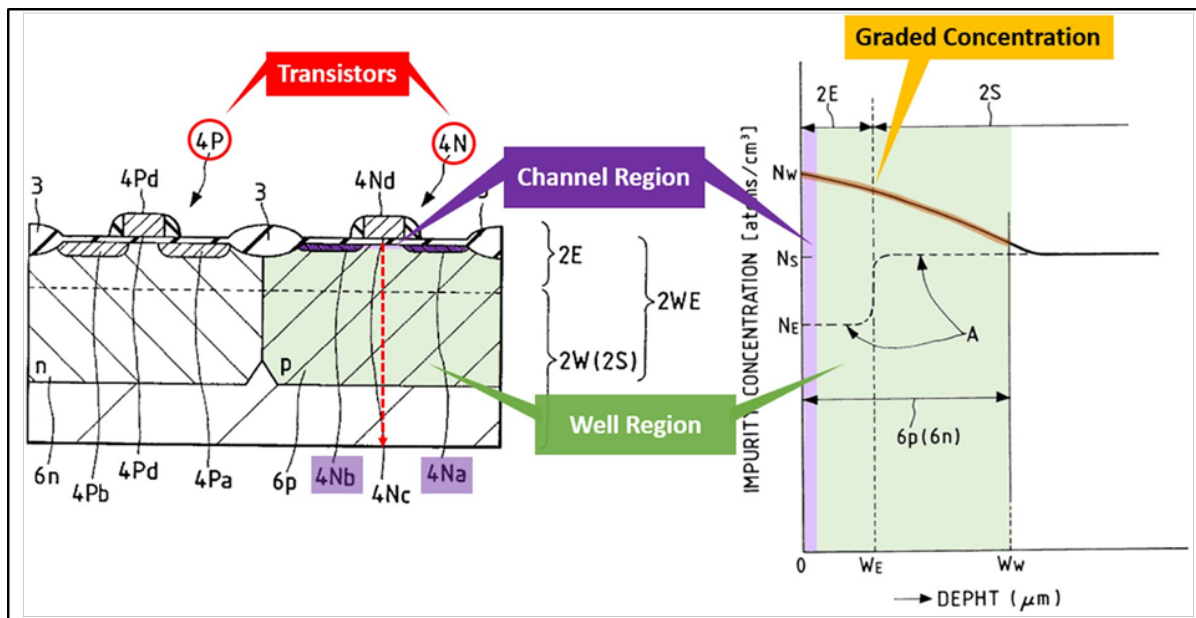
91. Further, during prosecution of the parent '195 Patent, and with respect to pending claims that likewise required aiding carrier movement from the first surface to the second surface of the substrate, Applicant represented to the Patent Office that a downward-sloping graded dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that sweeps carriers down into the substrate, as detailed below in Section X.A.1.g. Ex. 1016, 289-290.

g. Element [1.6]: "at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate."

92. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. As shown in Figure 23 (below left), Kawagoe discloses "a p-well 6p" (light green) adjacent to the first active region (purple/light purple). Ex. 1007, 8:66-67, 14:46-55, 15:26-40.

93. In addition, as discussed above and as shown in the dopant concentration profile (brown) of Figure 17 (below right), the dopant concentration

in the p-well 6p—measured along the exemplary red dotted line in Figure 23 is gradually decreasing with depth. Section X.A.1.f; Ex. 1007, 14:46-55, 15:62-16:40 (“the p-well 6p and n-well 6n have their impurity concentrations *gradually lowered* in the depthwise direction from the principal surface (having an impurity concentration N_w) of the epitaxial layer 2E.”), 16:11-15 (“The impurity concentration N_w in the principal surface of the epitaxial layer 2E of the p-well 6p and the n-well 6n is at about 6×10^{16} atoms/cm³”). Thus, in my opinion, Kawagoe discloses a well region containing at least one graded dopant region (*e.g.*, the region highlighted in light green in both Figures 23 and 17) having a downward-sloping graded dopant concentration.



Ex. 1007, FIGS. 17 and 23.

94. Kawagoe further explains that, consistent with the claimed requirement, this downward-sloping graded dopant concentration aids carrier

movement from the top surface of the epitaxial layer (claimed first surface) to the bottom surface of the substrate (claimed second surface):

[T]he impurity concentration of the p-well 6p is given such a gradient that it is ***gradually lowered in the depthwise direction*** from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α -ray is lowered. Specifically, the ***electrons produced by the α -ray are attracted to the substrate body 2S by that concentration gradient*** [] so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p.

Ex. 1007, 16:2-11.

95. In my opinion, Kawagoe's teaching is consistent with Applicant's representation to the Patent Office during prosecution of the parent '195 Patent that a downward-sloping graded dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that moves carriers deep into the substrate (while an upward-sloping concentration, not at issue in Kawagoe, would move carriers in the opposite direction towards the surface):

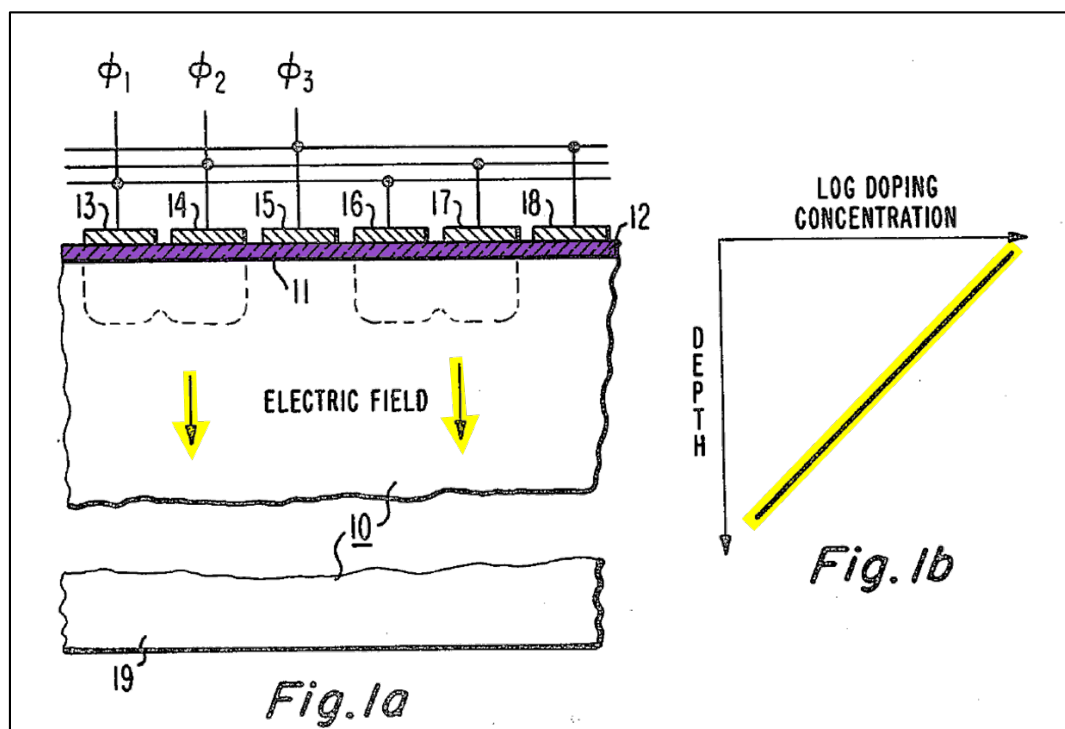
"[T]he graded dopant concentration itself creates a ***'built-in' electrical field*** that forces the movement of carriers into a particular direction, whereby ***the 'direction' of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.***"

Ex. 1016, 289-290 (underlining in original, addressing amended claim 10 (*id.*, 286)).

Applicant also represented that "a unidirectional drift (electric) field necessarily affects ***all*** the present minority carriers in the same way.... Depending on the particular slope of the graded concentration of dopant, ***all*** minority carriers are either

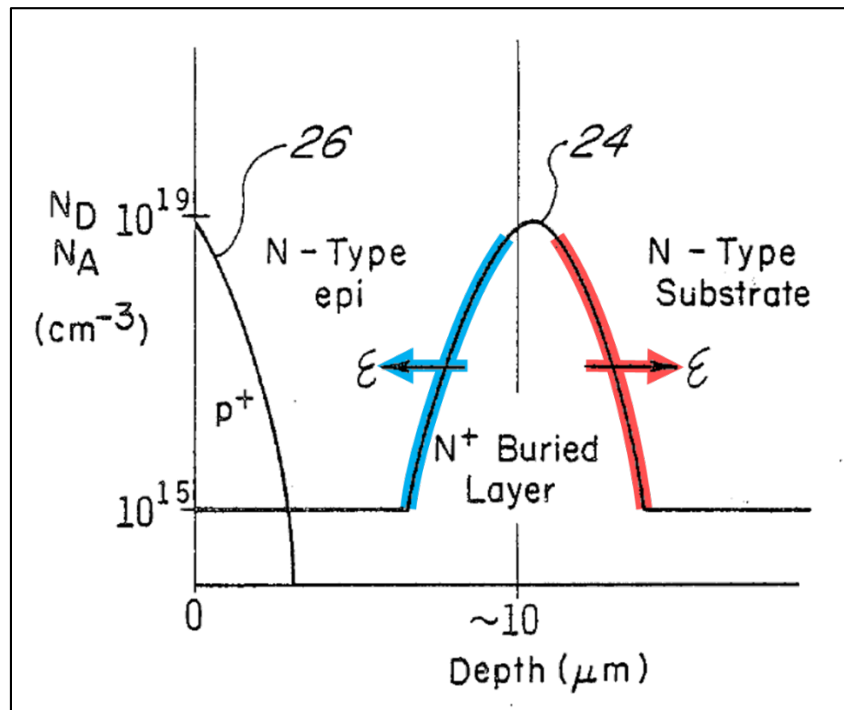
swept ‘down’ ... or ‘up.’” *Id.*, 289. A POSITA would have known that minority carriers exhibit random Brownian motion at room temperature at speeds that are much higher than the additional drift velocity imparted by the graded doping profile. In addition, when one applies external voltages to the device, the fields generated will typically be much higher than the built-in fields created by the graded doping.

96. Applicant cited Jastrzebski in support. *See* Ex. 1016, 290. In Jastrzebski, the doping concentration is “decreasing with depth” from the top surface 11 (purple) of the substrate 10, as shown in Figure 1b below. Ex. 1010, 5:14-22. According to Jastrzebski, this downward-sloping graded dopant concentration creates an electric drift field that “force[s] most of the charge carriers ... *deep into the substrate* [.]” *Id.*, 2:27-32, 5:14-22.



Id., FIGS. 1a-1b.

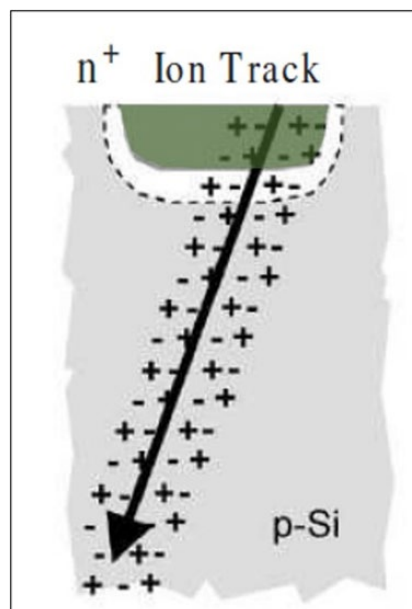
97. Applicant made the same representation to the Patent Office regarding Kamins. Ex. 1016, 237-238. According to Applicant, Kamins' Figure 3 shows "two electric fields with opposing directions" (highlighted in blue and red) that correspond to increasing and decreasing graded dopant concentrations, respectively. *Id.*, 237 (citing Ex. 1031, 3:6-13). Applicant explained that the electric field associated with the downward-sloping graded concentration at a depth beyond $\sim 10\mu\text{m}$ (red) causes "carriers created [in that region to be] *accelerated into the substrate ...*" *Id.* (citing Ex. 1031, 3:6-13, FIGS. 2-3).



Ex. 1031, FIG. 3.

98. In my opinion, and in light of the above, Kawagoe satisfies element [1.6] under Patent Owner's construction that the term "well region" means "a doped region that surrounds the active region of a semiconductor device." Ex. 1020, 30; *see also* Section VIII. As shown in Figure 23 above, the p-well region (light green) is a doped region that surrounds the first active region (purple/light purple). Kawagoe also satisfies element [1.6], in my opinion, under Patent Owner's construction that "to aid carrier movement from the first surface to the second surface of the substrate" should be accorded plain meaning. Section VIII.

99. Further, as discussed in Wang and as was well understood in the art, an α -ray generates a stream of millions of carriers (*e.g.*, electrons) that can cause single-event upset (SEU) soft errors. Ex. 1009, 431; Section X.A.1.f.



Ex. 1009, FIG. 2.

100. Kawagoe also explains that the graded dopant concentration illustrated in Figure 17 reduces soft errors by sweeping those carriers down to the second surface of the substrate. Ex. 1007, 16:2-11.

2. Dependent Claim 2: “The semiconductor device of claim 1, wherein the substrate is a p- type substrate.”

101. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 2. *See* Section X.A.1.b; Ex. 1007, 14:61–15:12, 6:50–7:3, Fig. 23.

3. Dependent Claim 3: “The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.”

102. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 3. *See* Section X.A.1.b; Ex. 1007, 6:50-7:3, 14:61–15:12, 17:10–18:38, Fig. 23.

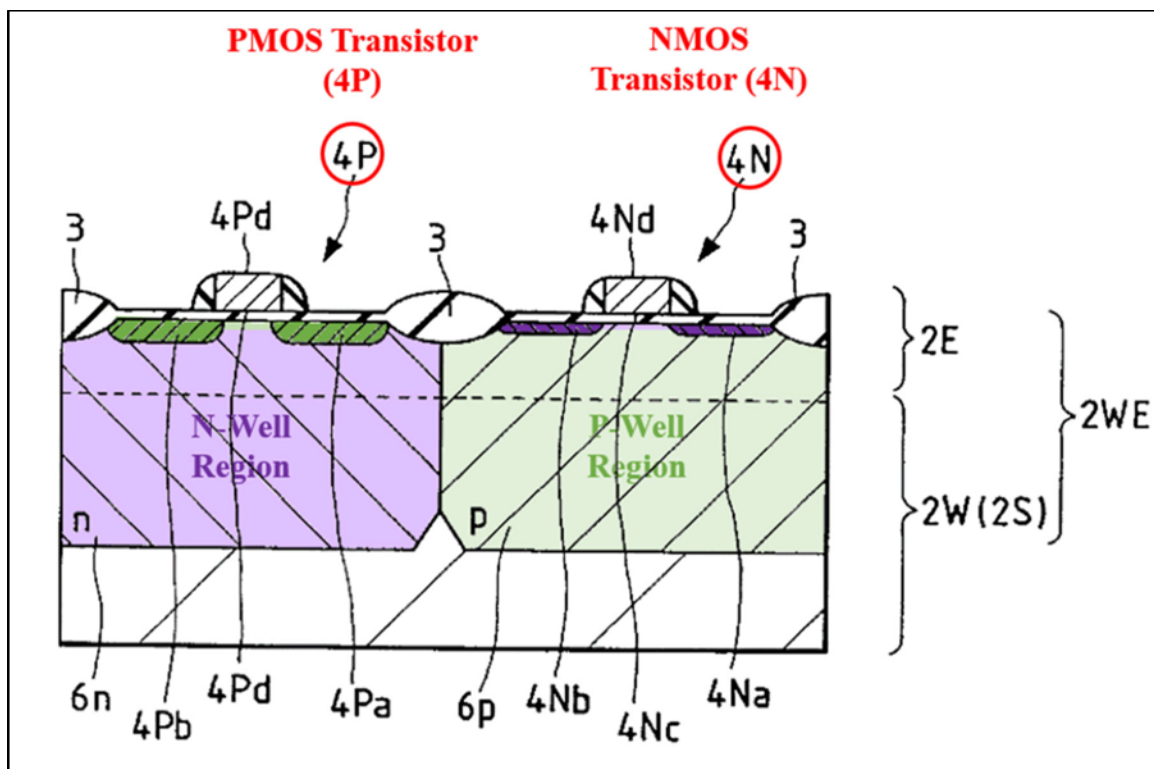
4. Dependent Claim 4: “The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p- channel and n-channel devices.”

103. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 4. *See* Sections X.A.1.c-e; Ex. 1007, 3:35-37, 8:46-9:3; 14:46-55, 15:26-40, Fig. 23.

5. Dependent Claim 5: “The semiconductor device of claim 1, wherein the first active region and second active region contain either p- channel or n-channel devices in n-wells or p-wells respectively, and each well has at least one graded dopant.”

104. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 5. Kawagoe's Figure 23 illustrates a conventional twin-well architecture, whereby the first active region contains nMOS (n-channel) transistor 4N) formed in "p-well 6p" and the second active region contains pMOS (p- channel) transistor 4P formed in "n-well 6n." Ex. 1007, 8:46-52, 14:46-55, 15:26-43; Sections X.A.1.c-d; Ex. 1008B, 387-88.

105. In my opinion, this mapping satisfies this claim under Patent Owner's interpretation that an active region in the claims can contain only "*a transistor.*" Ex. 1020, 31. A POSITA would have also understood that Kawagoe teaches forming multiple transistors in an active region to save chip area, as good layout practice dictates. Ex. 1014, 1:52-54, 2:17-21.

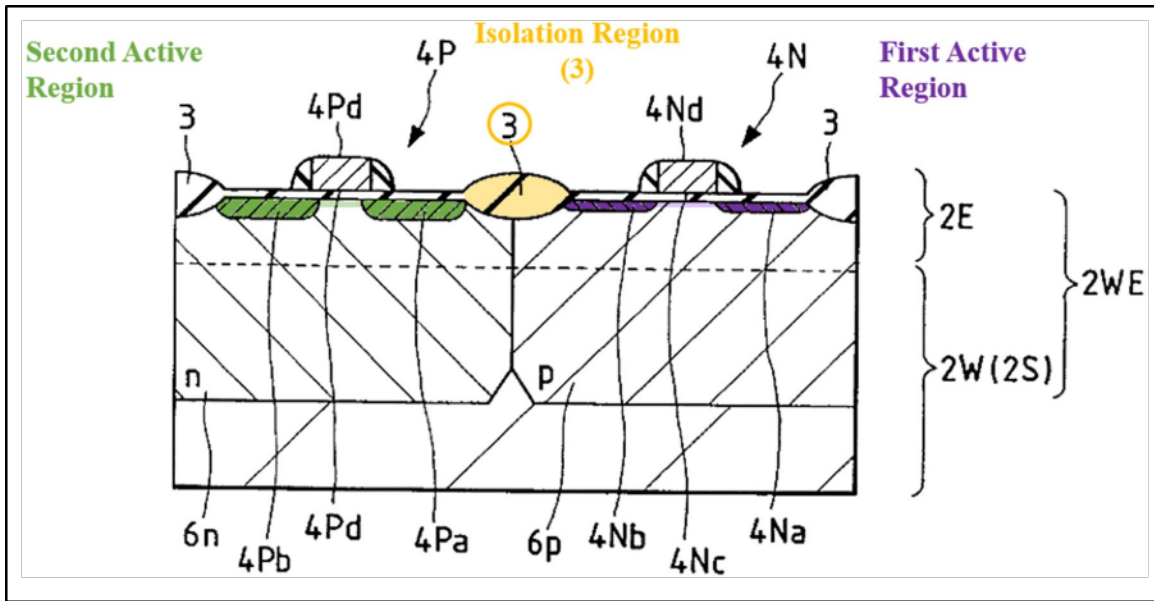


Ex. 1007, FIG. 23.

106. Further, in my opinion, Kawagoe's n-wells and p-wells have graded dopants. Ex. 1007, 14:46-55, 15:62-16:2 ("as shown in FIGS. 16 and 17, ... the p-well 6p and n-well 6n have their impurity concentrations *gradually lowered* in the depthwise direction from the principal surface (having an impurity concentration N_w) of the epitaxial layer 2E."); *see also* Section X.A.1.g (discussing the graded dopants in p-well 6p).

6. Dependent Claim 6: "The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region."

107. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 6. As shown below, the first active region (purple/light purple) and second active region (green/light green) are separated by a "field insulating film 3" (claimed "isolation region") (yellow). Ex. 1007, 8:40-52, 15:37-40, 17:62-18:8; Ex. 1008A, 818-820, FIG. 16-11(f).



Ex. 1007, FIG. 23.

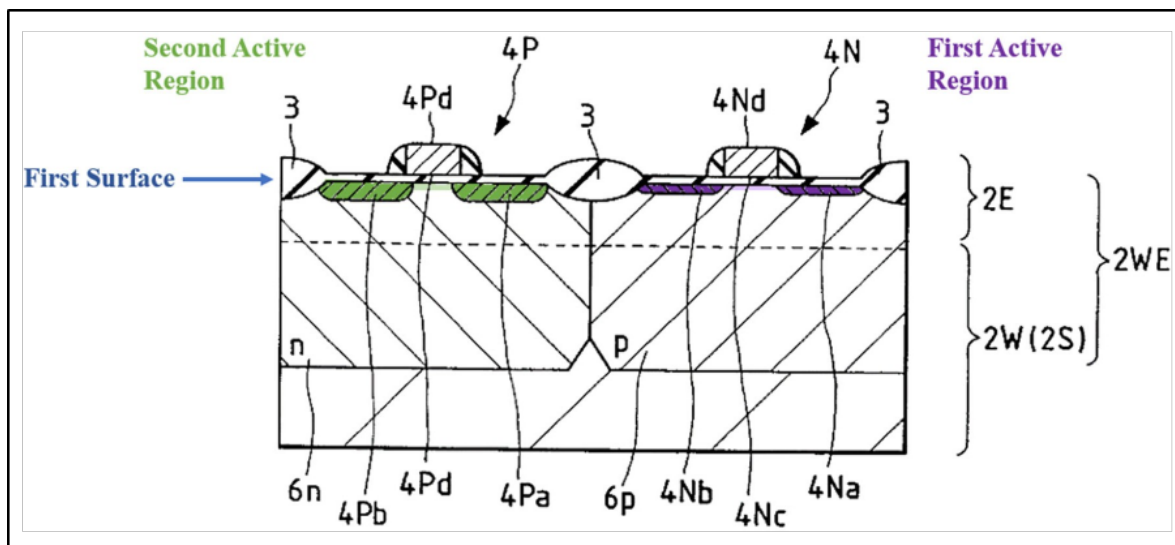
7. Dependent Claim 7: “The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.”

108. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 7. In my opinion, Kawagoe discloses that the graded dopants in n-well 6n and p-well 6p are “formed by the ion implantation method.” Ex. 1007, 4:11-12, 15:26-36, 17:10-12, 17:31-39 (n-well 6n formed by implanting “ions of an n- type impurity”), 17:43-49 (p-well 6p formed by implanting ions of “a p- type impurity”); Sections X.A.1.f-g.

8. Dependent Claim 8: “The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.”

109. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 8. In my opinion, and as shown in Figure 23 below,

Kawagoe discloses that the first (purple/light purple) and second (green/light green) active regions are formed adjacent the first surface of the substrate (indicated in blue). Ex. 1007, 8:66-9:6, 9:47-54, 15:37-40, 17:10-12, 17:31-18:35; Ex. 1008B, 299 (“The top surface of the [substrate] body consists of active or transistor regions....”), 298, 300-301, FIG. 5-2; Sections X.A.1.c-d.



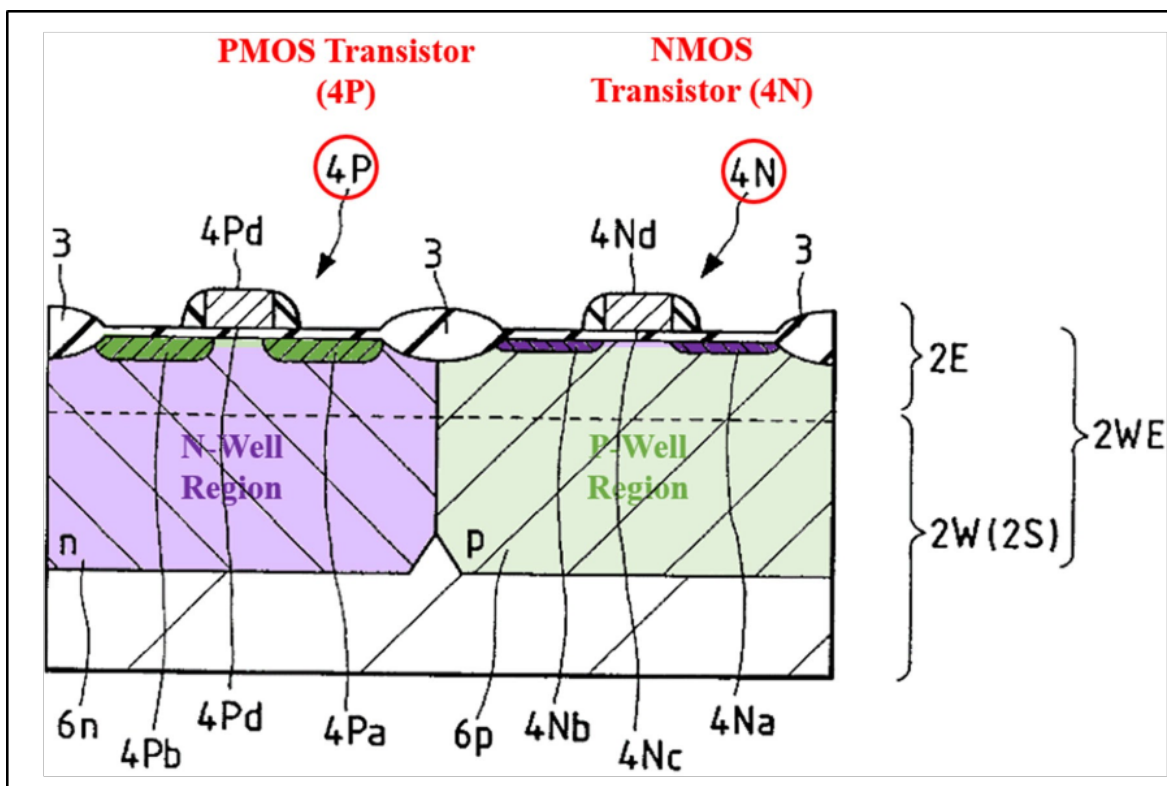
Ex. 1007, FIG. 23.

9. Dependent Claim 9: “The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.”

110. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 9. As discussed above and shown in my annotation of Figure 23 below, the channel region (light purple) of the first active region (between the source-drain regions 4Na and 4Nb and below the insulating film 4Nc, and formed at the top of p-well 6p) is of the same doping type (p-type) as p-well 6p.

Ex. 1007, 15:26-36 (“The p-well 6p is doped with a p-type impurity.”); *id.*, 17:10-12, 17:43-49.

111. Likewise, in my opinion, the channel region (light green) of the second active region (between the source-drain regions 4Pa and 4Pb and below the insulating film 4Pc, and formed at the top of n-well 6n) is of the same doping type (n- type) as n-well 6n. Ex. 1007, 15:26-36 (“an n-well 6n is doped with an n-type impurity.”), 17:10-12, 17:33-39.



Ex. 1007, FIG. 23.

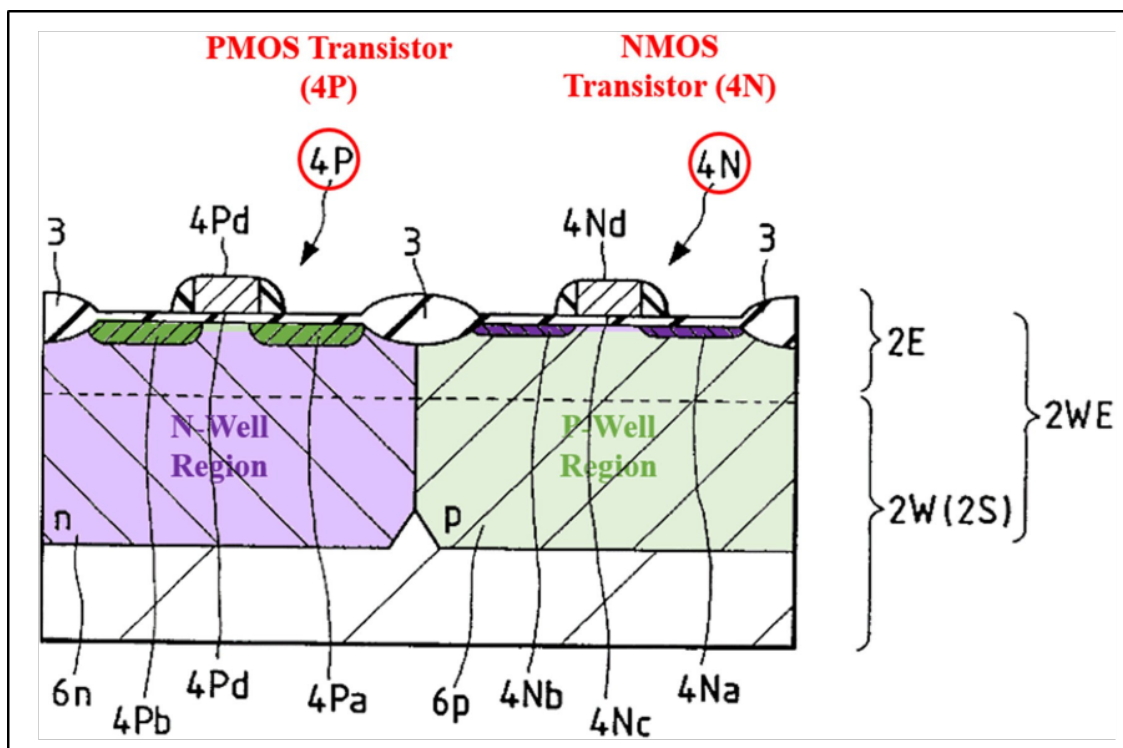
112. In my opinion, those channel regions all have graded dopant concentrations, as discussed above. Section X.A.1.f.

10. Dependent Claim 12: “The semiconductor device of claim 1, wherein dopants of the graded dopant region in the well region are both p-type and n-type.”

113. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 12. As I explained above for elements [1.5]-[1.6], *see* Sections X.A.1.f-g, Kawagoe’s Figure 23 includes an “n-well 6n [that] is doped with an n-type impurity.” Ex.1007, 15:31-36. Further, n-well 6n is formed into a substrate “doped with a p-type impurity.” *Id.*, 15:1-12 (discussing, for Embodiment 4, that “[t]he epitaxial layer 2E made of a p-type Si single crystal or the like is formed over a principal surface of the semiconductor substrate body 2S. The epitaxial layer 2E is doped with a p-type impurity such as boron in a concentration lower than the designed one of the semiconductor substrate body 2S.”); *see also id.*, 9:32-40 (“the n-well 6 is **formed in** the epitaxial layer 2E and the semiconductor substrate body 2S to have a larger depth than the film thickness of the epitaxial layer 2E.”). The uniformly-doped substrate of Embodiment 1 is likewise “doped with a p-type impurity.” *Id.*, 6:60-7:18. Because the implantation of an n-type impurity to form n-well 6n does not remove the substrate’s p-type dopants, n-well 6n includes “both p-type and n-type” dopants, as claim 12 requires.

11. Dependent Claim 13: “The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.”

114. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 13. As explained above and shown below, Kawagoe teaches an nMOS transistor 4N formed in the first active region and a pMOS transistor 4P formed in the second active region, which are CMOS transistors. Ex. 1007, 8:45-52 (“[T]hese nMOS 4N and pMOS 4P constitute a CMOS (i.e., Complementary Metal Oxide Semiconductor) circuit.”), 14:46-55, 15:37-40; Sections X.A.1.c-d, X.A.1.f.



Ex. 1007, FIG. 23. Each of the CMOS transistors includes a source, drain, gate, and channel. For example, the nMOS transistor 4N includes “source-drain regions” 4Na and 4Nb spaced apart by an “n-channel” region, and a gate electrode 4Nd. Ex. 1007, 8:60-67, 8:42-48, 8:55-57, 14:46-55, 15:37-40, FIG. 23. Similarly, the

pMOS transistor 4P includes “source-drain regions” 4Pa and 4Pb spaced apart by a “p-channel” region, and a gate electrode 4Pd. Ex. 1007, 8:42-67, 9:41-48, 14:46-55, 15:37-40, FIG. 23; Sections X.A.1.c-d, X.A.1.f

12. Dependent Claim 14: “The semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM).”

115. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 14. Kawagoe explains that “Embodiment 4” (Figures 16-17, 20-24), relied upon for claim 1, can be advantageously used to fabricate a DRAM device with reduced soft errors, reduced defect density, and “excellent gate breakdown performance.” Ex. 1007, 16:2-11 (explaining that the graded dopant concentration in p-well 6p that is illustrated in Figure 17 moves “electrons produced by the α -ray” to the substrate body 2S so that “soft errors can be reduced in case ... DRAM or the like is formed in the p-well 6p”), 19:15-23 (“the structure of the present embodiment 4 is applied to a 4M DRAM (i.e., 4 Megabit Dynamic RAM”), 19:43-48, 20:1-33 (DRAM formed in accordance with embodiment 5, which uses the same downward sloping graded dopant concentration described for embodiment 4). Based on these teachings, a POSITA would have further appreciated that the twin-well CMOS device of Figure 23, when implemented using a uniformly-doped substrate as in Embodiment 1, in which the doping levels of the epitaxial layer (N_E) and substrate body (N_S) are equal (as I

discussed above for claim 1), would likewise been advantageously used for a DRAM device.

13. Dependent Claim 16: “The semiconductor device of claim 1, wherein the device is a flash memory.”

116. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 16. Kawagoe teaches a semiconductor flash memory device. Ex. 1007, 22:14-18 (“The semiconductor integrated circuit device 1 of the present embodiment 7, as shown in FIG. 28, is exemplified by a flash memory.”). The flash memory device includes a CMOS “peripheral circuit region [] formed with the nMOS 4N and the pMOS 4P....” *Id.*, 22:51-23:2. This peripheral circuit is fabricated according to twin-well CMOS technology, whereby NMOS transistors (*e.g.*, 4N) are formed in “p-well 6p3,” and PMOS transistors (*e.g.*, 4P) are formed in “n-well 6n2.” *Id.*, 22:51-65, FIG. 28.

117. Kawagoe explains that the teachings of Embodiment 4 (relied upon in the claim mapping for claim 1) are applicable to Embodiment 7 and therefore, to flash memory. In particular, Embodiment 7 applies the teachings of Embodiment 4 relating to the use of an epitaxial substrate to form a twin-well architecture with a pMOS transistor 4P formed in an n-well and nMOS transistor 4N formed in a p-well, where both wells have a downward-sloping graded dopant concentration. Ex. 1007, 22:22-29 (“In the present embodiment 7, too, the semiconductor substrate 2 is formed thereover with a p-well 6p3 and an n-well 6n2. The p-well 6p3 and n-well

6n2 are formed, *as in the foregoing embodiments 4 and 6*, to extend from the surface of the epitaxial layer 2E to the upper portion of the semiconductor substrate body 2S. Moreover, their impurity concentrations are made gradually lower depthwise of the semiconductor region 2, *as in the foregoing embodiment 4.*”), FIG. 28. Based on these teachings, a POSITA would have further appreciated that the twin-well CMOS device of Figure 23, when implemented using a uniformly-doped substrate as in Embodiment 1 (as I discussed above for claim 1), would likewise have been used for a flash memory device.

14. Dependent Claim 17: “The semiconductor device of claim 1, wherein the device is a logic device.”

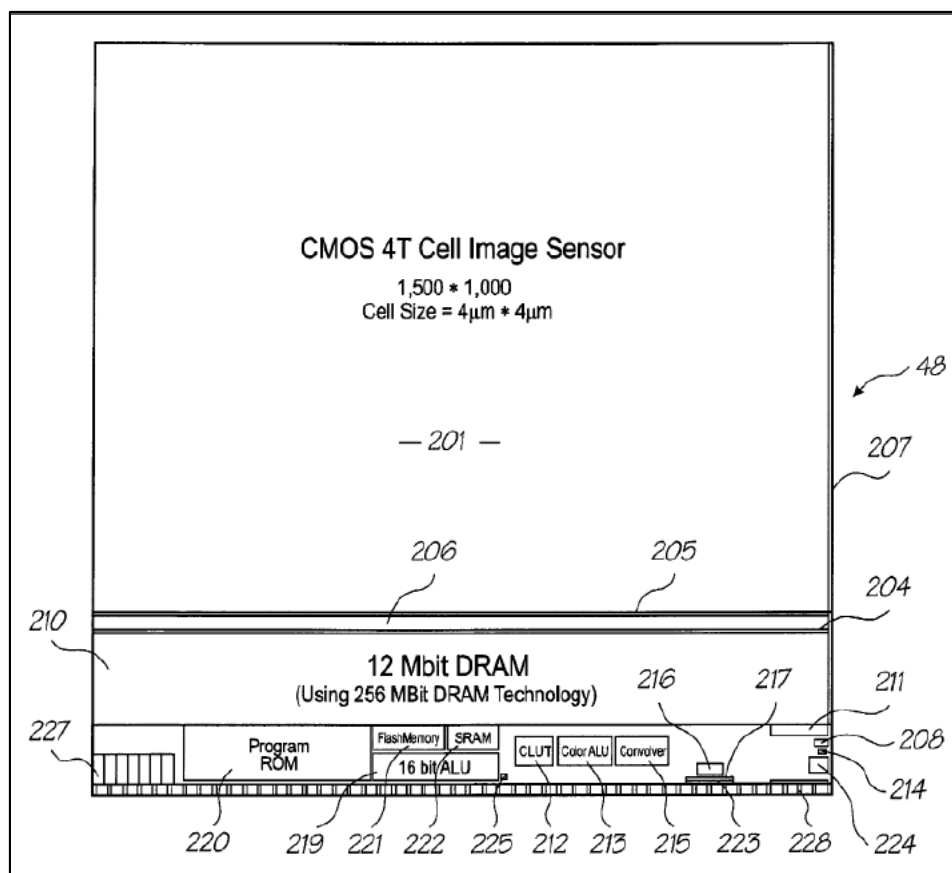
118. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 17. Kawagoe teaches that its disclosed “techniques of the foregoing embodiments 1 to 7 can ... be applied to the semiconductor integrated circuit device which has a *logic circuit* such as the so-called ‘microcomputer.’” Ex. 1007, 24:28-31. Based on this teaching, a POSITA would have further appreciated that the twin-well CMOS device of Figure 23, when implemented using a uniformly-doped substrate as in Embodiment 1 (as I discussed above for claim 1), would likewise have been used for a logic device.

15. Dependent Claim 18: “The semiconductor device of claim 17, wherein the device is central processing unit.”

119. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 18. Kawagoe teaches that its disclosures can be applied to a “microcomputer.” Section X.A.13; Ex. 1007, 24:28-31. In my opinion, a POSITA would have understood that a microcomputer includes a central processing unit (CPU). Ex. 1032, 1334. Based on this teaching, a POSITA would have further appreciated that the twin-well CMOS device of Figure 23, when implemented using a uniformly-doped substrate as in Embodiment 1 (as I discussed above for claim 1), would likewise have been used for a central processing unit.

16. Dependent Claim 19: “The semiconductor device of claim 1, wherein the device is an image sensor.”

120. In my opinion, it would have been obvious to a POSITA to implement the semiconductor device disclosed in Kawagoe in an image sensor. Kawagoe discloses a circuit comprising an “nMOS 4N and pMOS 4P [which] constitute a CMOS (*i.e.*, Complementary Metal Oxide Semiconductor) circuit” and a POSITA would have understood that CMOS circuits are commonly used in a variety of applications. Ex. 1007, 8:46-52. Moreover, Kawagoe teaches that the disclosed techniques can be applied to semiconductor integrated circuit devices with other logic circuits. *Id.*, 24:21-31. A POSITA would have understood that one example of such an application would be an image sensor. An example of such an image sensor is shown in U.S. Patent No. 6,614,560 (“Silverbrook”), pictured below. Ex. 1042, 6:41-13:39, FIG. 15.



Consistent with the applications hypothesized in Kawagoe, Silverbrook’s image sensor includes “CMOS logic, a CMOS image sensor, DRAM, and analog circuitry.” *Id.*, 6:56-57. As such, it would have been obvious to a POSITA that the designs in Kawagoe could be implemented in an image sensor.

17. Independent Claim 20

a. Preamble: “A semiconductor device, comprising:”

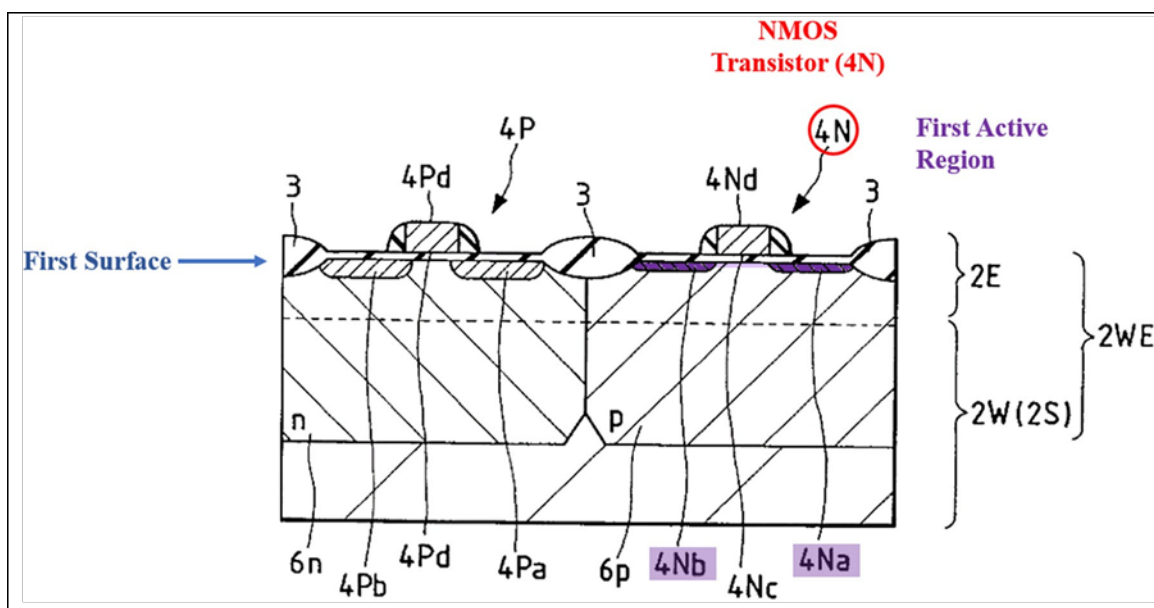
121. To the extent the preamble is limiting, in my opinion, Kawagoe discloses it. *See* Section X.A.1.a.

b. Element [20.1]: “a substrate of a first doping type at a first doping level having first and second surfaces;”

122. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. *See* Section X.A.1.b.

- c. **Element [20.2]: “a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;”**

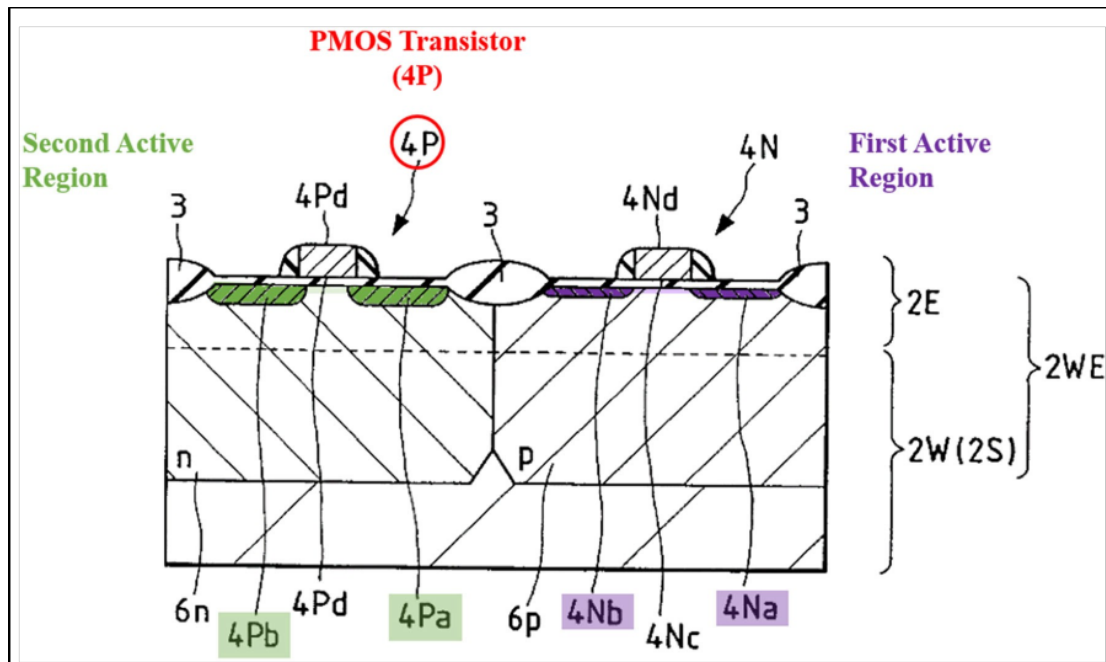
123. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. *See* Section X.A.1.c. Kawagoe discloses nMOS transistor 4N formed in the surface of the first active region, as shown below.



Ex. 1007, FIG. 23.

- d. **Element [20.3]: “a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;”**

124. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. *See* Section X.A.1.d. Kawagoe discloses pMOS transistor 4P formed in the surface of the second active region, as shown below.



Ex. 1007, FIG. 23.

- e. **Element [20.4]: “transistors formed in at least one of the first active region or second active region;”**

125. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. *See* Section X.A.1.e.

- f. **Element [20.5]: “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and”**

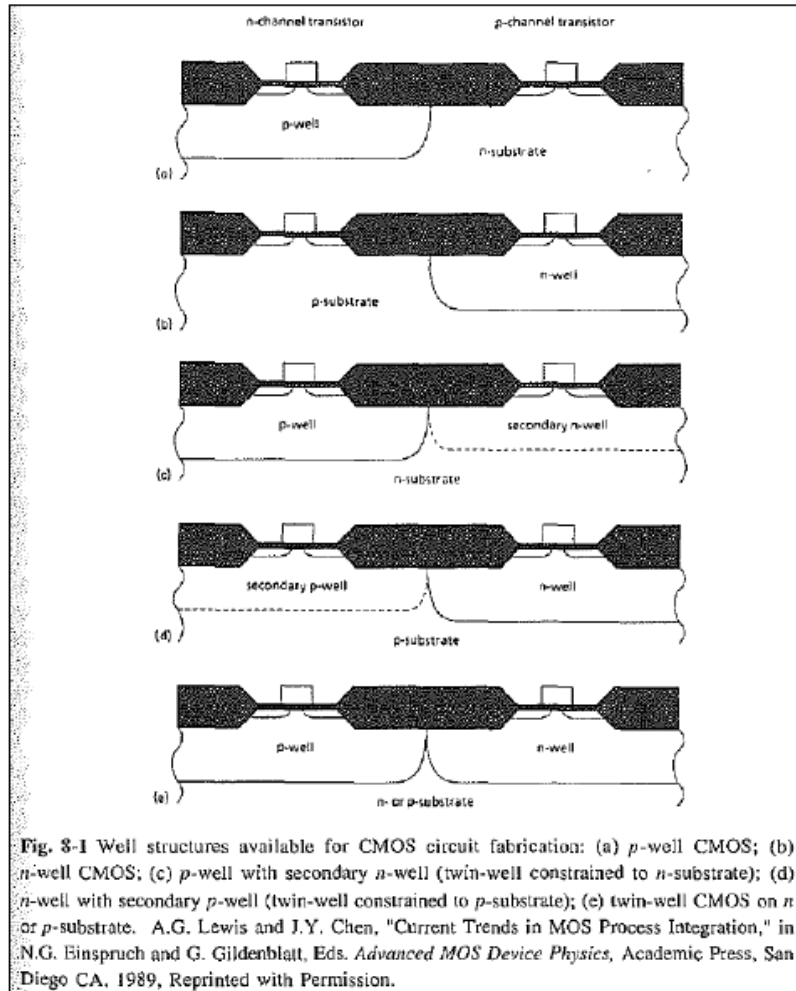
126. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. *See* Section X.A.1.f.

- g. Element [20.6]: “at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.”**

127. In my opinion, Kawagoe discloses or, at a minimum, renders obvious this element. *See* Section X.A.1.g.

18. Dependent Claim 21: “The semiconductor device of claim 20, “wherein the substrate is an n- type substrate.”

128. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claims 3 and 11. At the time of the alleged invention, it was well-known that twin-well (also called twin-tub) CMOS devices, like those of Kawagoe, could be formed on either p-type or n-type substrates. Moreover, it was well-known that CMOS devices, like the nMOS and pMOS transistors described by Kawagoe, could be fabricated within wells formed on either n-type or p-type substrates. Indeed, Wolf confirms that “[w]ith the twin tub approach, two separate wells are formed for n- and p-channel transistors on a lightly doped substrate (Figs. 8-1c and 8-3). *The substrate may be either a lightly doped wafer of n or p material*” Ex. 1008C, 530. Wolf depicts various design options “available for CMOS circuit fabrication,” including “twin-well CMOS on n or p-substrate.” Ex. 1008C, 525, reproduced below:



Ex. 1008C, 525. *See also* Ex. 1008A, 811-813; Ex. 1008B, 387, Fig. 6-10. Further, Kawagoe teaches that its disclosed devices could be implemented on an *n*-type substrate. Specifically, Kawagoe teaches that “embodiments 1, 2 and 4 to 7 have been described in case the semiconductor substrate body and the epitaxial layer are made of *p*⁻-type Si. ***However, the present invention should not be limited thereto but can be modified such that the semiconductor substrate body and the epitaxial layer are made of *n*-type Si.***” Ex. 1007, 23:56-61. In this disclosed alternative to a twin-well CMOS structure formed on a *n*-type substrate, a POSITA would

understand that the claimed “first active region. . . with a second [opposite] doping type” would be a p-type region (instead of an n-type region, as discussed for claim 1). Thus, Kawagoe expressly discloses the limitation of claims 3 and 11 “wherein the substrate is an n-type substrate.”

19. Dependent Claim 22: “The semiconductor device of claim 20, wherein the substrate is a p- type substrate.”

129. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 22. *See* Section X.A.2.

20. Dependent Claim 23: “The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.”

130. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 23. *See* Section X.A.3.

21. Dependent Claim 24: “The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.”

131. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 24. *See* Section X.A.4.

22. Dependent Claim 25: “The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

132. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 25. *See* Section X.A.5.

- 23. Dependent Claim 26: “The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.”**

133. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 26. *See* Section X.A.6.

- 24. Dependent Claim 27: “The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p- type or n-type.”**

134. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 27. *See* Section X.A.9.

- 25. Dependent Claim 30: “The semiconductor device of claim 20, wherein dopants of the graded dopant region in the well region are both p-type and n-type.”**

135. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 30. *See* Section X.A.10.

- 26. Dependent Claim 31: “The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.”**

136. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 31. *See* Section X.A.7.

- 27. Dependent Claim 32: “The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.”**

137. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 32. Kawagoe teaches that “nMOS 4N and pMOS

4P constitute a CMOS” device formed in and including a substrate. Ex. 1007, 8:46-52 (“[T]hese nMOS 4N and pMOS 4P constitute a CMOS (i.e., Complementary Metal Oxide Semiconductor) circuit.”), 15:26-40, 8:60-9:6, 9:41-54, 14:46-55; *see also* Section X.A.17.b.

28. Dependent Claim 33: “The semiconductor device of claim 20, wherein the device is a flash memory.”

138. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 33. *See* Section X.A.13.

29. Dependent Claim 34: “The semiconductor device of claim 20, wherein the device is a logic device.”

139. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 34. *See* Section X.A.14.

30. Dependent Claim 35: “The semiconductor device of claim 34, wherein the device is central processing unit.”

140. In my opinion, Kawagoe discloses or, at a minimum, renders obvious the additional limitation of claim 35. *See* Section X.A.15.

31. Dependent Claim 36: “The semiconductor device of claim 20, wherein the device is an image sensor.”

141. In my opinion, Kawagoe combined with Silverbrook renders obvious the additional limitation of claim 36. *See* Section X.A.16.

B. Ground II:

142. In my opinion, Wieczorek in combination with Wolf renders claims 1-2, 4-9, 12-22, 24-27, and 30-36 obvious. In my opinion, a POSITA would have been

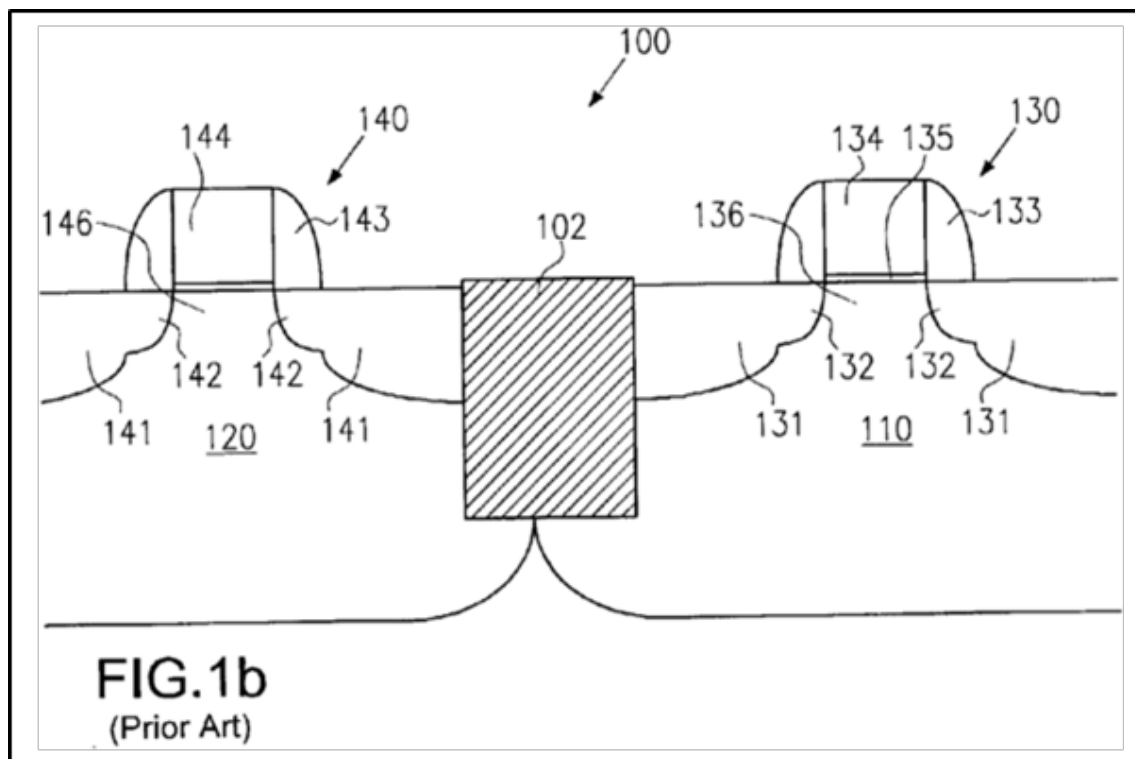
motivated to combine Wieczorek with Wolf. I rely herein on Wieczorek's description of a conventional prior-art CMOS device. *See, e.g.*, Ex. 1006, [0020]-[0021], [0004] (“Field effect transistors, such as MOS transistors, represent one of the most frequently used circuit elements in modern [*sic*] integrated circuits.”), [0007]-[0008] (describing “[a] typical process flow for forming the semiconductor device 100” which is “a complementary MOS transistor pair”), [0012], FIG. 1b. I note that Wieczorek does discuss some difficulties associated with the conventional prior art CMOS device, with respect to obtaining or maintaining a retrograde dopant profile. *Id.*, [0013]-[0014]. In my opinion, however, the prior-art CMOS device disclosed in Wieczorek's background section was nonetheless operable and widely used, and a POSITA would have recognized that the difficulties associated with maintaining a retrograde dopant profile may have been adequately managed by known techniques—for example, by using a more advanced furnace than as contemplated by Wieczorek (*see id.*, [0013]), which would have allowed further optimizing of the annealing process in terms of time and temperature. For instance, rapid thermal annealing would have enabled a POSITA to reduce dopant diffusion compared to that in a conventional furnace, and thereby obtain retrograde profiles. As discussed earlier, Wolf is a well-known textbook that teaches known fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on CMOS devices. *See generally* Ex. 1008A; *id.*, Chapter 16 (“CMOS

Process Integration”). In my opinion, a POSITA would have therefore understood and expected that the teachings of Wolf would apply to Wieczorek’s conventional CMOS device. *Id.* A POSITA would have looked to Wolf for additional details related to conventional CMOS devices, as further detailed below.

1. Independent Claim 1

a. Preamble: “A semiconductor device, comprising”

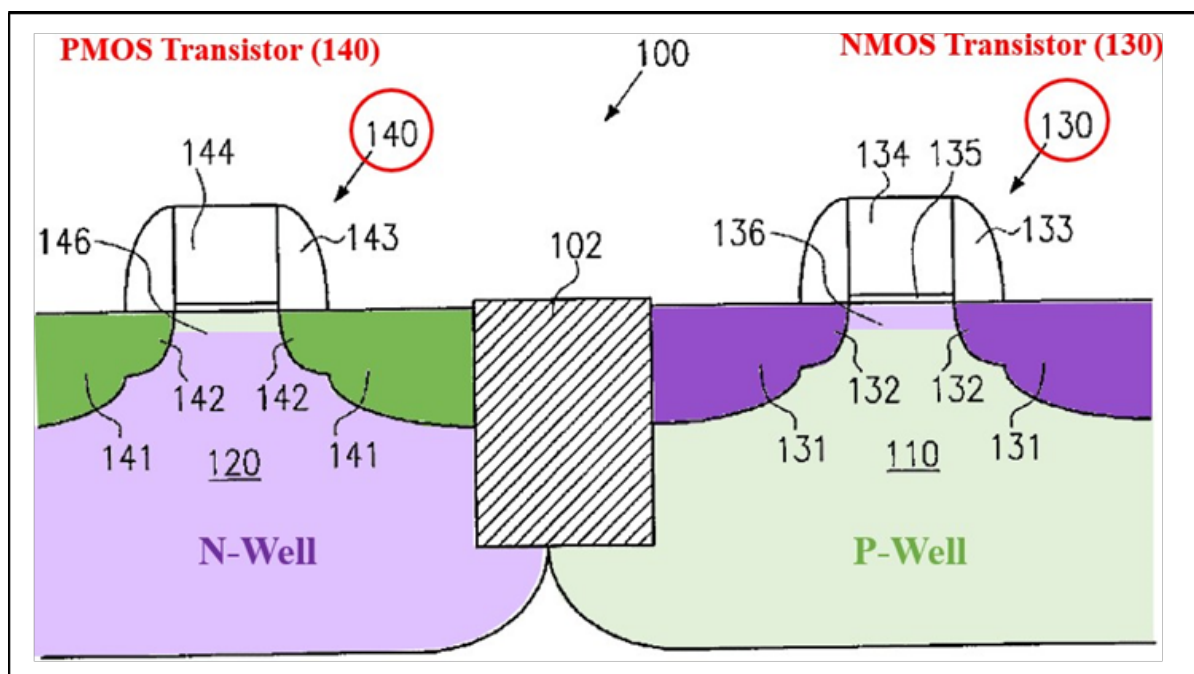
143. To the extent the preamble is limiting, in my opinion, Wieczorek discloses it. Wieczorek teaches a “semiconductor device 100” illustrated in the figure below. Ex. 1006, [0012].



Id., FIG. 1b.

b. Element [1.1]: “a substrate of a first doping type at a first doping level having first and second surfaces;”

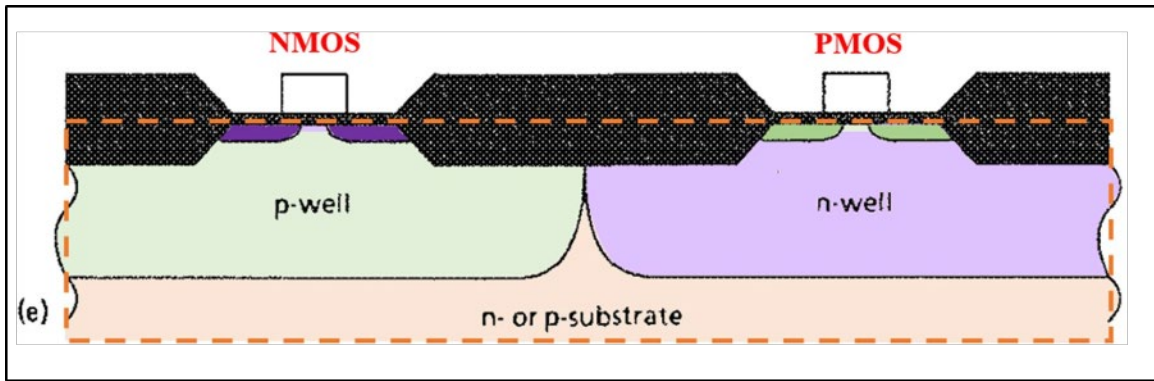
144. In my opinion, Wieczorek, alone or in combination with Wolf (hereinafter “Wieczorek-Wolf”), renders this element obvious. Wieczorek’s Figure 1b, which I have annotated below, illustrates a conventional twin-well CMOS device, in which N-channel transistor 130 (nMOS) with source/drain regions 131-132 (purple) and channel region 136 (light purple) is formed in P-well 110 (light green) and P-channel transistor 140 (pMOS) with source/drain regions 141-142 (green) and channel region 146 (light green) is formed in N-well 120 (light purple). Ex. 1006, [0007], [0012], [0020]-[0021]; Ex. 1008C, 525, FIG. 8-1(e); see also Section IX.A (discussing conventional twin-well CMOS devices). Wieczorek explains that the P-well and N-well structures are formed in a “semiconductor region 101, such as a silicon region” of a semiconductor element 100. *See* Ex. 1006, [0007]. Wieczorek further recognizes that such CMOS devices would be “formed on” any “appropriate substrate.” *Id.*, [0004].).



Ex. 1006, FIG. 1b (labelled as “Prior Art”).

145. In my opinion, a POSITA would have understood that a twin well (or twin-tub) CMOS approach “is independent of starting material type” for the substrate. Ex. 1008C, 524; Ex. 1006, [0004] (discussing the use of “an appropriate substrate” for forming MOS transistors without further specificity).

146. In my opinion, because Wieczorek does not specify what constitutes an appropriate substrate, a POSITA would have been motivated to consult the teachings of Wolf, which confirms that a “uniform, lightly doped p-or n- type substrate” is a suitable substrate commonly used in twin-well CMOS devices. Ex. 1008C, 523, 530 (“With the twin-tub [(twin-well)] approach, two separate wells are formed for n- and p-channel transistors on a lightly doped substrate ... of n or p material.”); Ex. 1008B, 387-389.

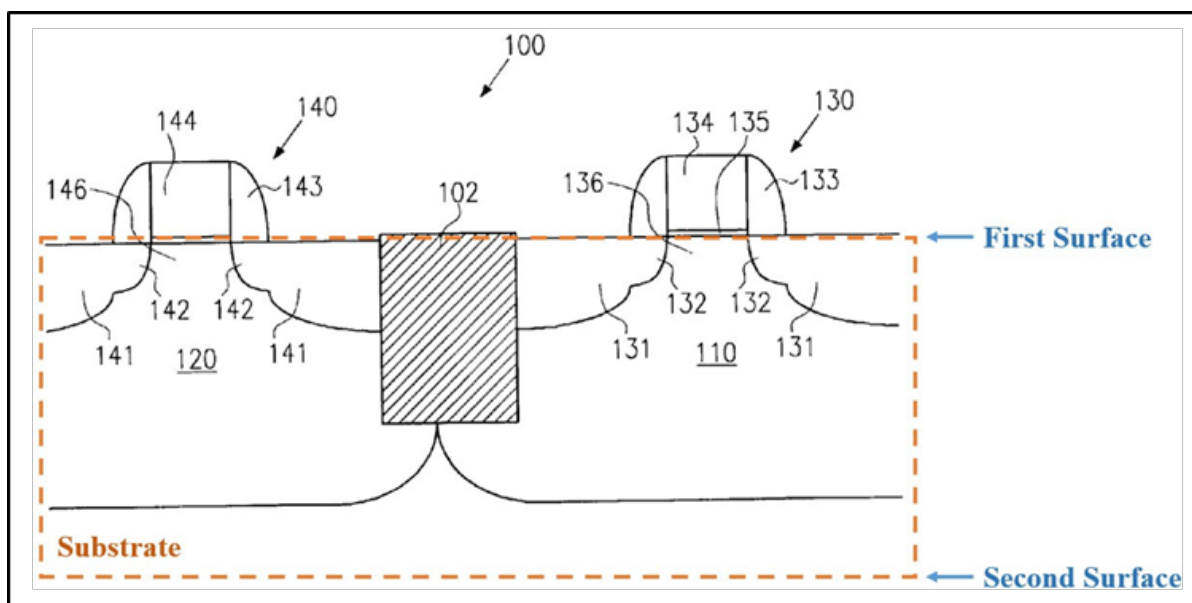


Ex. 1008C, 525, FIG. 8-1(e) (“twin-well CMOS on n or p-substrate”).

147. In my opinion, and consistent with Wieczorek’s teaching, a POSITA would have found it obvious to use a uniformly doped n- or p- type substrate (“a substrate of a first doping type at a first doping level”) as a suitable substrate for the CMOS device in Wieczorek’s Figure 1b. Doing so would amount to combining known prior art elements (*i.e.*, the use of a uniform, lightly doped n- or p- type substrate with Wieczorek’s process for forming a conventional CMOS device) according to known methods (*i.e.*, the known use of an “appropriate substrate” for the conventional process of forming the CMOS device in Wieczorek [0007]-[0013]) to obtain predictable results (*i.e.*, the conventional CMOS device in Wieczorek’s Figure 1b). Doing so would have also been obvious to try because it involves nothing more than choosing one of a finite number of known appropriate substrates that are described by Wolf as suitable for use in forming a twin-well CMOS device like Wieczorek’s. See 1008C at 530 (“With the twin-tub approach, two separate wells are formed for *n*- and *p*-channel transistors on a lightly doped substrate. ... The

substrate may be either a lightly doped wafer of n or p material, or a thin, lightly-doped epitaxial layer on a heavily doped substrate”); Ex. 1008A, 816. (As I discussed above, another substrate option for a twin-well CMOS structure is a lightly-doped epitaxial layer atop substrate body having the same doping level, as reflected in Kawagoe’s Embodiment 1). There would have been reasonable expectation of success because Wolf shows that a POSITA would have known how to use a uniformly doped n - or p - type substrate to form a twin-well CMOS device similarly as described in Wieczorek.

148. For purposes of claim mapping, and without loss of generality, I have considered Wieczorek-Wolf’s substrate is taken as a p - type nonepitaxial substrate, a widely used choice in my experience and which has the advantage of lower cost compared to an epitaxial substrate. Ex. 1008A, 816 (“Typically, in twin-well CMOS the starting material is also *either* a lightly p -doped wafer (***p-bulk wafer***, Fig. 16-7a), or a heavily p -doped wafer on which a thin, lightly p -doped epi layer is grown” and noting the cost disadvantage of epitaxial wafers), FIG. 16-7. Consistent with the teachings of Wolf, Wieczorek’s substrate (orange dotted line) in Figure 1b below, has a top surface (“first surface”) and a bottom surface (“second surface”). Ex. 1008B, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e).

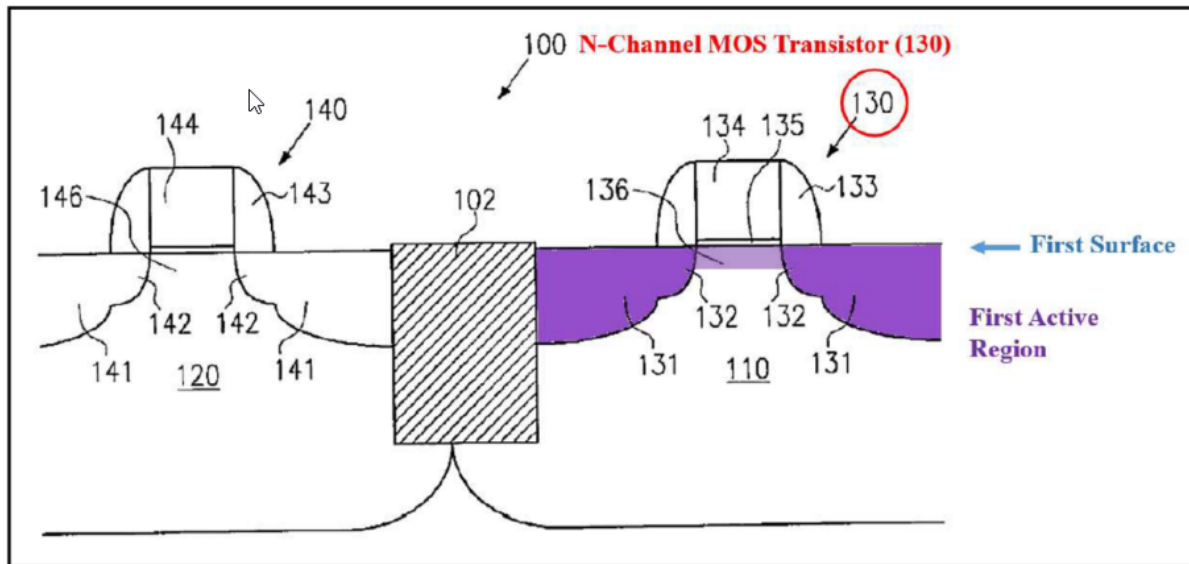


Ex. 1006, FIG. 1b. While Wieczorek does not explicitly indicate the semiconductor substrate in Figure 1b a POSITA would have clearly understood that the substrate is the starting point material for subsequent processing of transistor devices. Elsewhere, Wieczorek acknowledges this. *See* Ex. 1006, [0027] (describing, for Figure 3a, that the N-well and P-well structures therein are “formed in a semiconductor substrate 301”); *see also id.*, cls. 1, 31. The bottom of such a substrate (i.e., opposite the side on which devices are formed) has a “surface.”

149. In my opinion, Wieczorek-Wolf satisfies element [1.1] under Patent Owner’s position that the term “substrate” should be given its plain meaning. *See* Section VIII; Ex. 1006, [0004], [0012].

- c. **Element [1.2]: “a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;”**

150. In my opinion, Wieczorek-Wolf renders obvious this element. Wieczorek discloses “an N-channel transistor 130” that includes “heavily N-doped *source and drain regions* 131, including lightly doped extensions 132,” and “*channel region* 136.” Ex. 1006, [0012]-[0013]; *id.*, [0004] (“[A] field effect transistor comprises two highly doped semiconductor regions ... referred to as *drain and source regions*, and which are embedded in a lightly and inversely doped semiconductor region, the so-called N-well or P-well ... The drain and source regions are spaced apart with a *channel region* interposed, wherein a conductive channel forms between the drain and source regions in the channel region” when the transistor is active). As illustrated in the figure below, the source-drain regions 131-132 (purple) form part of the claimed first active region, which also includes channel region 136 (light purple) in between them. *Id.*, [0012]; Ex. 1008B, 299 (“The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The active regions are those in which transistor action occurs; i.e., the *channel* and the heavily doped *source and drain* regions.”), 300, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e). As shown below in Figure 1b, nMOS transistor 130 is formed in the first active region, which is adjacent the first surface of the substrate.



Ex. 1006, FIG. 1b, [0007].

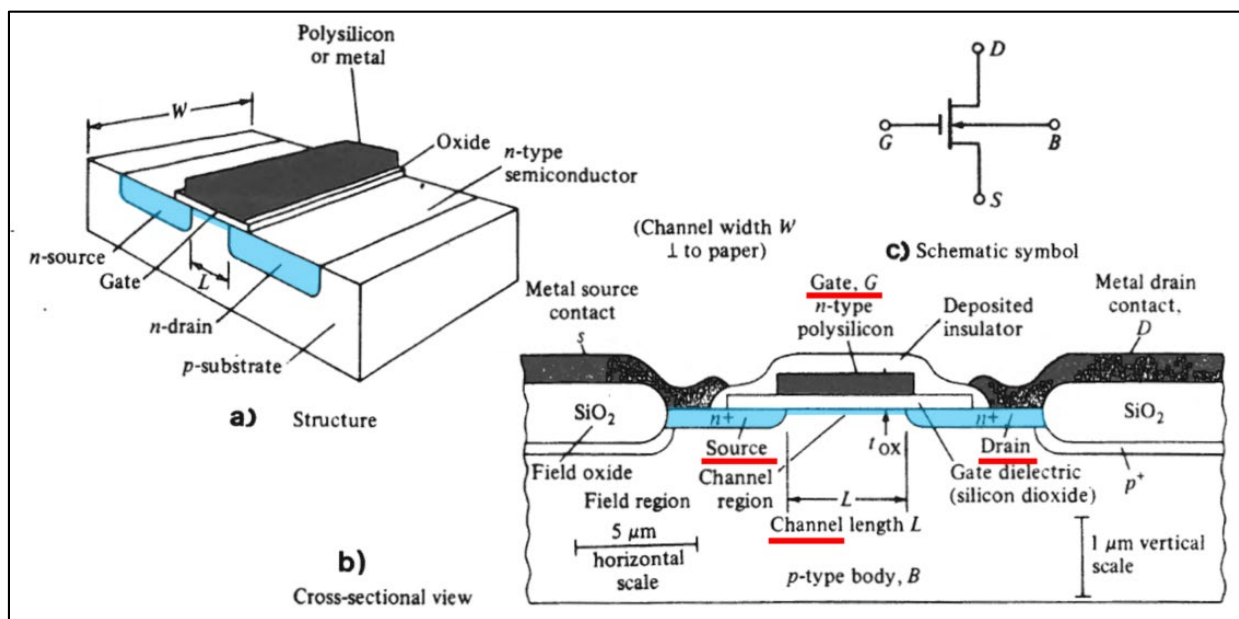
151. In my opinion, because the source-drain regions of the first active region are N-doped, Wieczorek-Wolf's first active region has a second doping type (N- type) opposite in conductivity to the first doping type (P- type) of the substrate.

Ex. 1006, [0012].

152. While Figure 1b illustrates a single exemplary nMOS transistor 130 formed in the first active region, in my opinion, a POSITA would have understood that Wieczorek contemplates forming multiple nMOS transistors in the first active region to minimize chip area, as good layout practice dictates. Ex. 1006, [0004]; ("Typically, a huge number of field effect transistors is simultaneously formed on an appropriate substrate and are connected to provide the required functionality of the circuit."); Ex. 1014, 1:52-54, 2:17-21; *see* Section X.A.1.c. In any event, I understand that according to Patent Owner's representations in the Intel Litigation,

an “active region ... within which transistors can be formed” means “an active region ... where a transistor can be formed.” Ex. 1020, 31.

153. In my opinion, Wieczorek satisfies element [1.2] under Patent Owner’s construction that the term “active region” means “a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed.” Ex. 2020, 20; *see also* Section VIII. In my opinion, the active region of a CMOS transistor is “[its] channel and [its] heavily doped source and drain regions” as illustrated in blue in the figure below. Ex. 1008B, 299.



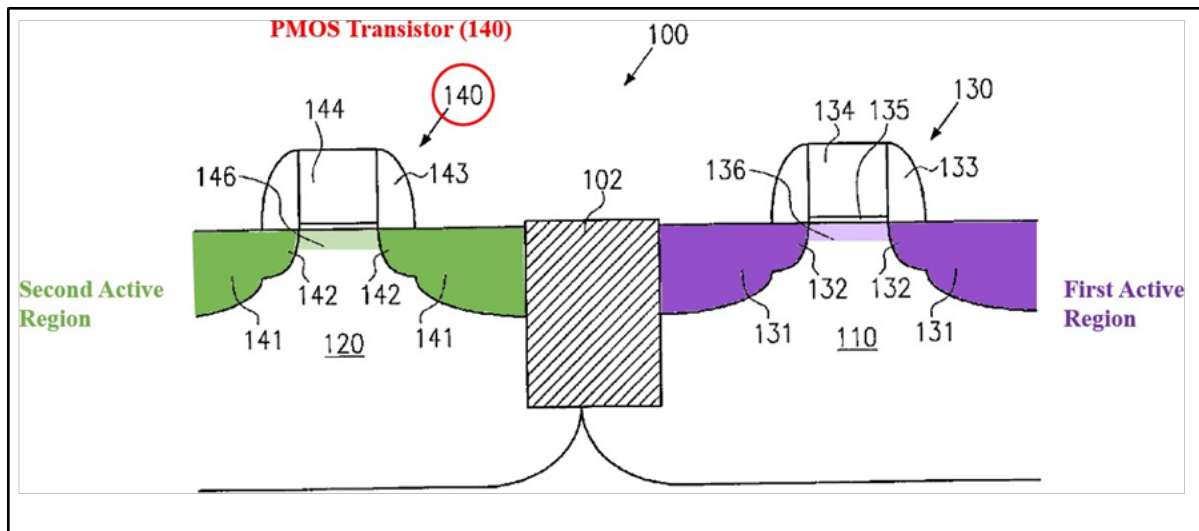
Ex. 1008B, FIG. 5-1; *id.*, 298-301, FIGS. 5-2, 6-4.

d. Element [1.3]: “a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;”

154. Wieczorek discloses or, at a minimum, renders obvious this element.

Wieczorek discloses “a P-channel transistor 140” that includes “heavily P-doped source and drain regions 141, including lightly doped extensions 142,” and “channel region 146.” Ex. 1006, [0004], [0007], [0012]-[0013]. The source and drain regions 141-142 (green) are part of the claimed second active region, which also includes channel region 146 (light green) in between them and below the gate insulation layer 135. Ex. 1006, [0012]; Ex. 1008B, 298-301, FIGS. 5-1, 5-2, 6-4; Section X.B.1.c.

155. As shown in Figure 1b, pMOS transistor 140 is formed in the second active region (green/light green), which is separate from and disposed adjacent to the first active region (purple/light purple). Ex. 1006, [0012]. Adjacent active regions are separated by an isolation region (such as shallow trench isolation 102). Ex. 1006, [0007]; Ex. 1008A, 818-20, FIG. 16-11(f); Ex. 1001, Cl. 6; Section X.A.1.d.



Ex. 1006, FIG. 1b, [0007].

156. While the figure shows an exemplary pMOS transistor 140 formed in the second active region, a POSITA would have understood that Wieczorek contemplates forming multiple pMOS transistors in the second active region to minimize chip area, as good layout practice dictates. Ex. 1006, [0004]; Section X.B.1.c. In any event, I understand that according to Patent Owner’s representations in the District Court Case, an “active region ... within which transistors can be formed” means “an active region ... where *a transistor* can be formed.” Ex. 1020, 31.

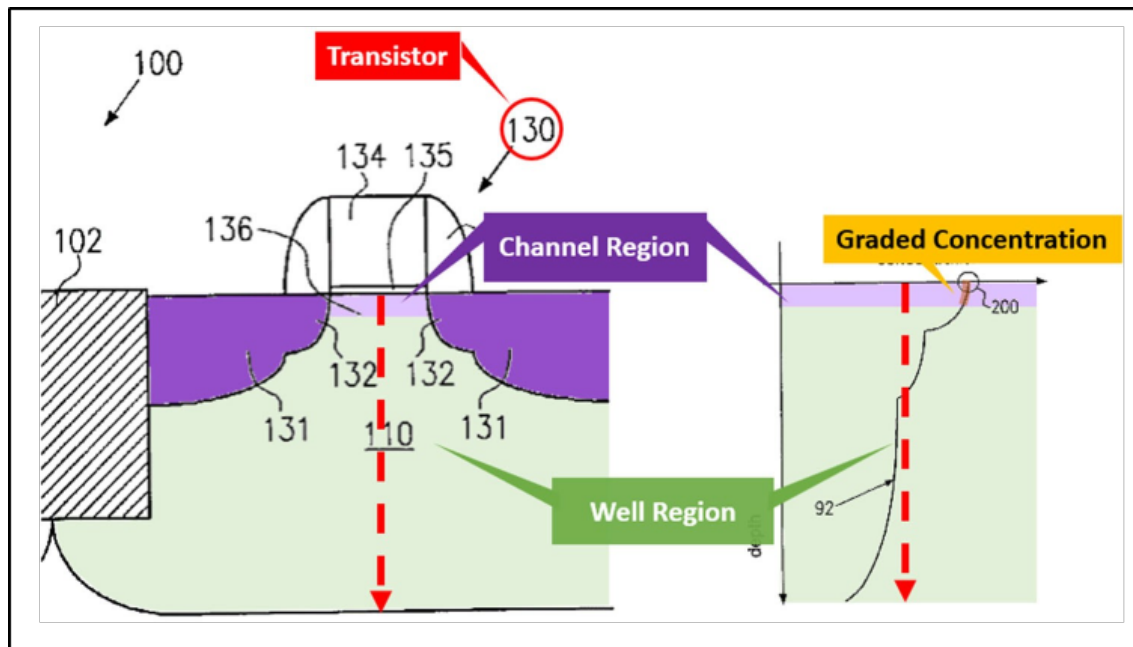
157. In my opinion, Wieczorek satisfies element [1.3] under Patent Owner’s position that the term “active region” means “a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed.” Section X.B.1.c.

e. **Element [1.4]: “transistors formed in at least one of the first active region or second active region;”**

158. It is my opinion that Wieczorek discloses or, at a minimum, renders obvious this element. *See* Sections X.B.1.c-d.

f. **Element [1.5]: “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and”**

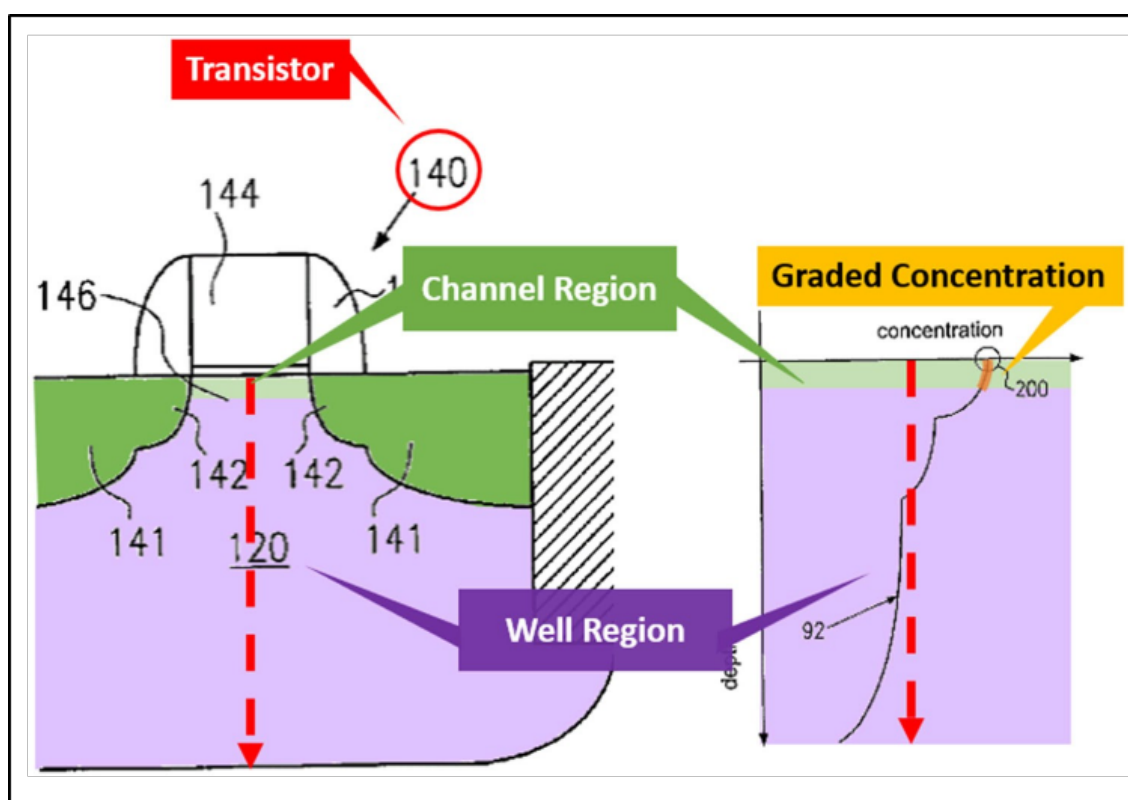
159. It is my opinion that Wieczorek-Wolf renders obvious this element. As illustrated in Figure 1b (below left), the channel region (light purple, as indicated by lead line 136) of nMOS transistor 130, formed at the top surface of the substrate, is a portion of the first active region. Ex. 1006, [0012]-[0013], [0004] (“The drain and source regions are spaced apart with a *channel region* interposed”); Ex. 1008B, 298-301 (“The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The *active regions* are those in which transistor action occurs; *i.e.*, the *channel* and the heavily doped *source and drain* regions.”), FIG. 5-2.



Ex. 1006, FIGS. 1b, 2b. The doping concentration in the channel region is highlighted in brown in the doping profile of Figure 2b (above right), which is measured for example along the red dotted line in Figure 1b that traverses the channel region. *Id.*, [0011] (“FIG. 2b shows ... a typical dopant profile with respect to the depth of the respective well structure.”), [0013] (“after the plurality of heat treatments, the actual dopant concentration will be represented by the graph shown in FIG. 2b.”), [0009], FIG. 2a.

160. In my opinion, and as Figure 2b shows, the dopant concentration is highest at the surface of the substrate and decreases with depth. Therefore, the channel region 136 has a graded dopant concentration. As shown in Figure 2b above, Wieczorek’s graded dopant concentration is in fact downward-sloping from the top surface of the substrate and all the way through the entire depth of the channel region

(light purple) and the underlying well-region (P-well 110) (green). Ex. 1006, [0011]. And as shown in the figures below, Wieczorek teaches that the channel region (light green, as indicated by lead line 146) of pMOS transistor 140, which is a portion of the second active region, also has a graded dopant concentration for the same reasons. Ex. 1006, [0004], [0009], [0011]-[0013], FIGS. 2a-2b; Ex. 1008B, 298-301, FIG. 5-2.

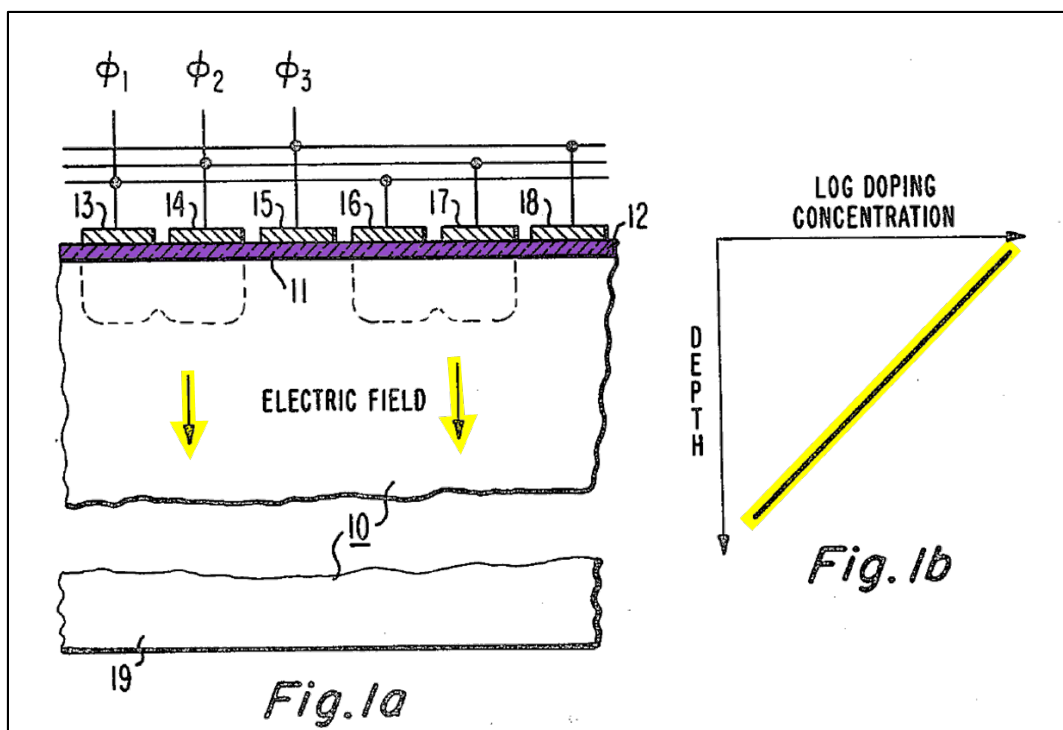


Ex. 1006, FIGS. 1b, 2b. I note that Wieczorek, in discussing Figure 2b, mentions that following heat treatment, the profile “in the vicinity of the surface of the semiconductor device 100, as indicated by reference number 200, may have become substantially uniformly distributed,” *id.* at [0011], but this description is made relative to the “initially retrograde profile “ shown in Figure 2a; this is not

inconsistent with my understanding that Wieczorek still teaches and depicts a graded dopant concentration that is downward-sloping from the top surface of the substrate. Thus, in my opinion, Wieczorek discloses “at least a portion of” the first and second active regions (the channel regions) having a downward-sloping graded dopant concentration. Ex. 1006, [0009]. [0011], [0013].

161. Further, Wieczorek’s downward-sloping graded dopant concentration aids the movement of carriers (*i.e.*, electrons in the *p*-type layer and holes in the *n*-type layer) from the first surface to the second surface of the substrate to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. As detailed in Section X.A.1.g, during prosecution of the parent ’195 Patent, Applicant represented to the Patent Office that a downward-sloping graded dopant concentration was known in the prior art to move carriers deep into the substrate. Applicant cited Jastrzebski and Kamins in support. Section X.A.1.g.

162. According to Jastrzebski, a downward-sloping graded dopant concentration creates an electric drift field that “force[s] most of the charge carriers ... *deep into the substrate*[.]”. Ex. 1010, 2:27-32, 5:14-22.



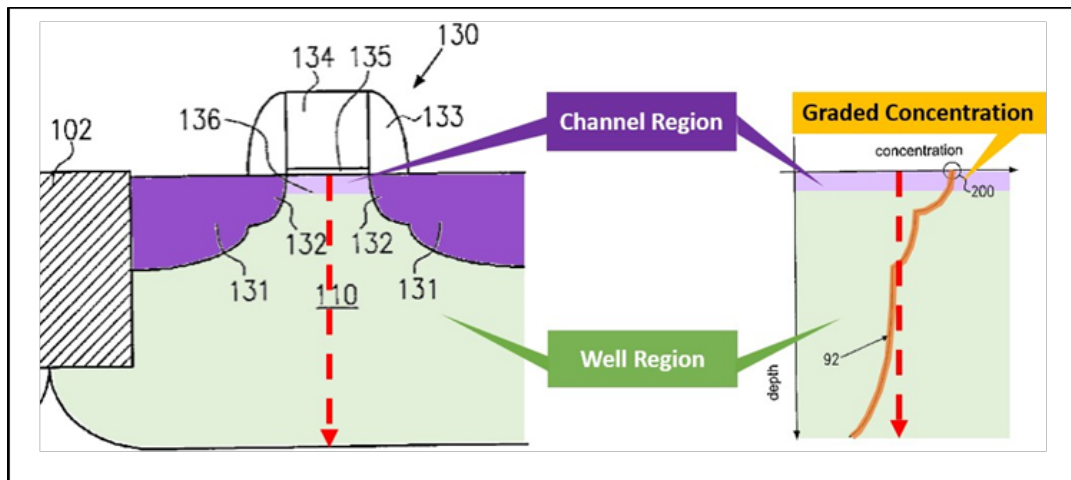
Id., FIGS. 1a-1b.

163. In light of the above, it is my opinion that Wieczorek satisfies element [1.5] under Patent Owner’s position that the term “to aid carrier movement from the first surface to the second surface of the substrate” should be accorded plain meaning. *See* Section VIII. According to Patent Owner’s representations in the District Court Case, the claims make clear that “carriers [must move] in a particular direction (from the surface layer to the substrate).” Ex. 1020, 29. Also, according to Patent Owner’s statements in the District Court Case, “when the dopant concentration is graded in a particular direction, [certain] charge carriers will move in the [same] gradient direction ...”. *Id.*, 2. Here, in my opinion, Wieczorek’s Figure 2b shows that the dopant concentration is downward-sloping with increasing depth

towards the bottom of the substrate, and thus, according to Patent Owner, this graded dopant concentration causes carriers to move deeper into the substrate as well.

- g. Element [1.6]: “at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.”**

164. In my opinion, Wieczorek-Wolf renders obvious this element. As shown in Figure 1b (below left), Wieczorek discloses a “P-well structure 110” (light green) adjacent to the first active region (purple/light purple). Ex. 1006, [0012]-[0013]. As discussed above and shown in the dopant concentration profile (brown) of Figure 2b (below right), the dopant concentration in P-well 110—measured along the exemplary red dotted line in Figure 1b—is gradually decreasing with depth. Section X.B.1.f; Ex. 1006, [0009], [0011] (“FIG. 2b shows ... a typical dopant profile with respect to the depth of the respective well structure [110 and 120]”), [0013]. Thus, Wieczorek discloses a well region containing at least one graded dopant region (*e.g.*, the region highlighted in light green in both Figures 1b and 2b) having a downward-sloping graded dopant concentration.



Ex. 1006, FIGS. 1b, 2b.

165. Under Applicant’s representation to the Patent Office, discussed above in Section X.B.1.f, such a downward-sloping graded dopant concentration was known in the prior art to create a “built-in” electric field that moves carriers deep into the substrate and thus aids carrier movement from the first surface to the second surface of the substrate. *See* Section X.B.1.f.

166. In light of the above, in my opinion, Wieczorek satisfies element [1.6] under Patent Owner’s construction that the term “well region” means “a doped region that surrounds the active region of a semiconductor device.” Ex. 1020, 30; *see also* Section VIII. As shown in Figure 1b above, the p-well region 110 (light green) is a doped region that surrounds the first active region (purple/light purple). *Id.* In my opinion, Wieczorek also satisfies this element under Patent Owner’s construction that “to aid carrier movement from the first surface to the second surface of the substrate” should be accorded plain meaning. *See* Section VIII.

167. In addition, Applicant represented to Patent Office during prosecution of the parent '195 Patent that a downward-sloping graded dopant concentration was known in the prior art to create an “inherent ‘built-in’ unidirectional electric field” that sweeps carriers into the substrate, as further detailed in Section X.A.1.g. Ex. 1016, 4/17/2012 Resp. at 6-7.

2. Dependent Claim 2: “The semiconductor device of claim 1, wherein the substrate is a p- type substrate.”

168. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 2. *See* Section X.B.1.b.

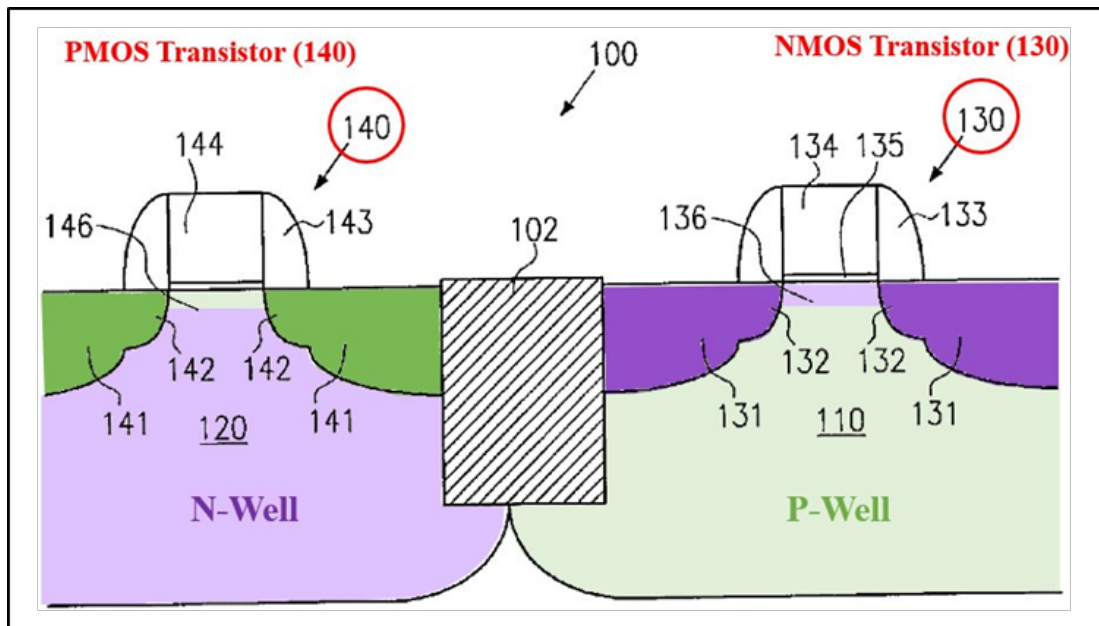
3. Dependent Claim 4: “The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.”

169. In my opinion, Wieczorek discloses or renders obvious the additional limitation of claim 4. *See* Section X.B.1.c-e.

4. Dependent Claim 5: “The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

170. In my opinion, Wieczorek discloses or renders obvious the additional limitation of claim 5. Wieczorek’s Figure 1b illustrates a conventional twin-well architecture, whereby the first active region contains an “N-channel transistor 130” in “P-well structure 110” and the second active region contains a “P-channel transistor 140” in “N-well structure 120.” Ex. 1006, [0012]-[0013], [0004]; Sections

X.B.1.c-d. In my opinion, this mapping satisfies this claim element under Patent Owner’s interpretation that an active region in the claims can contain only “*a transistor*.” Ex. 1020, 31. A POSITA would have also understood that Wieczorek teaches forming multiple transistors in an active region to save chip area, as good layout practice dictates. Ex. 1014, 1:52-54, 2:17-21.

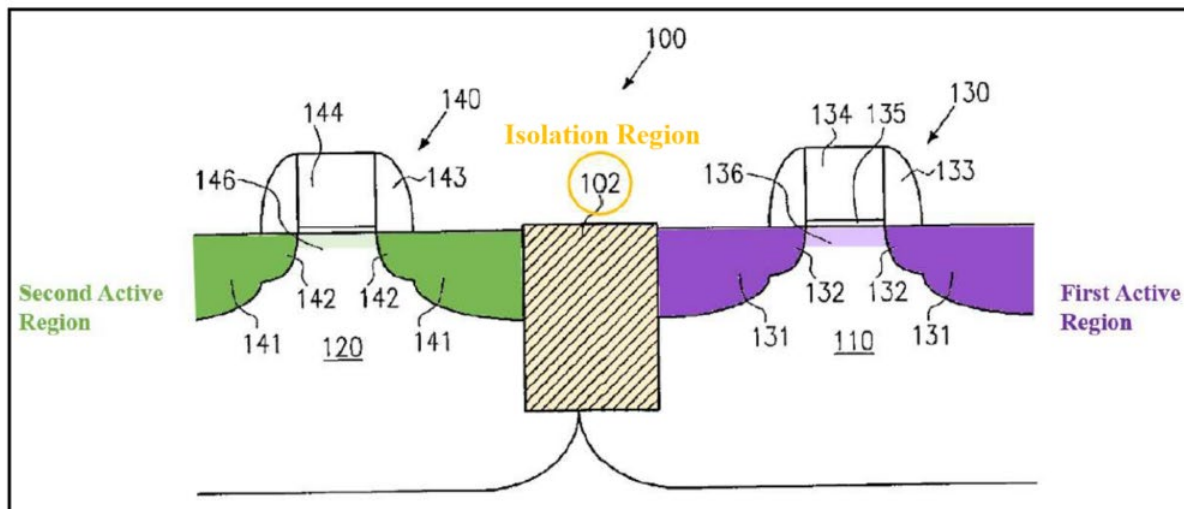


Ex. 1006, FIG. 1b. Further, in my opinion, Wieczorek's wells have a graded concentration of dopants. Ex. 1006, [0009]-[0011] ("FIG. 2b shows ... a typical dopant profile with respect to the depth of the respective well structure [110/120]."), [0013], FIGS. 2a-2b; Section X.B.1.g (discussing graded dopants in P-well 110).

5. Dependent Claim 6: “The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.”

171. In my opinion, Wieczorek discloses or renders obvious the additional limitation of claim 6. As shown below, the first active region (purple/light purple)

and second active region (green/light green) are separated by the “shallow trench isolation 102” (yellow). Ex. 1006, [0007]; Ex. 1008A, 818-820, FIG. 16-11(f).



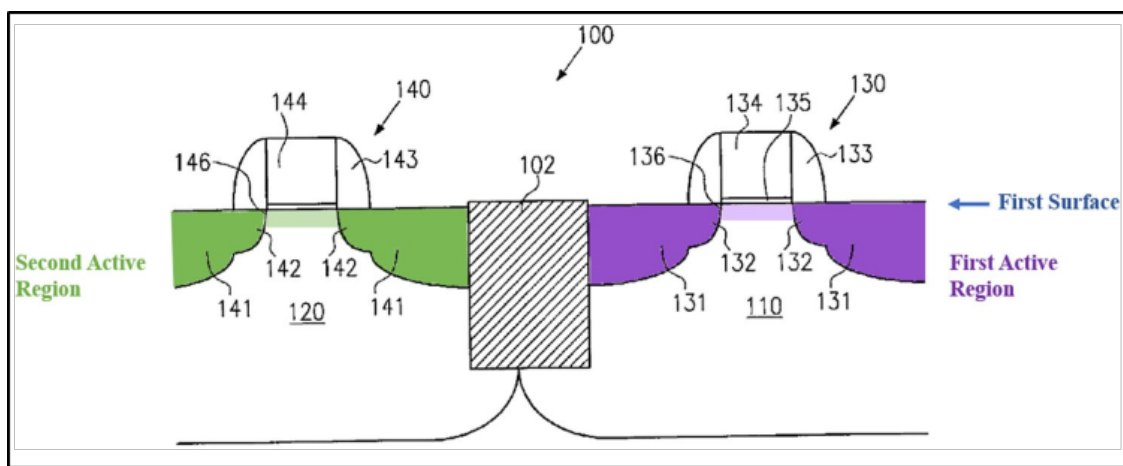
Ex. 1006, FIG. 1b.

6. Dependent Claim 7: “The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.”

172. In my opinion, Wieczorek discloses or renders obvious the additional limitation of claim 7. Wieczorek teaches, in my opinion, that the graded dopants in “the P-well structure 110 and the N-well structure 120 are defined by sequentially performed ion implantation processes.” Ex. 1006, [0008], [0007]-[0011], FIGS. 1a, 2a-2b; Sections X.B.1.f-g. At the relevant time, ion implantation, given its precision and flexibility, was the technique typically used for introducing dopants during semiconductor processing.

7. Dependent Claim 8: “The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.”

173. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 8. As shown below, Wieczorek discloses that the first active region (purple/light purple) and second active region (green/light green) are formed adjacent the first surface of the substrate (blue). Ex. 1006, [0007]-[0010], [0012]-[0013]; Ex. 1008B, 299 (“The top surface of the [substrate] body consists of active or transistor regions....”), 298-301, FIG. 5-2; Sections X.B.1.c-d.



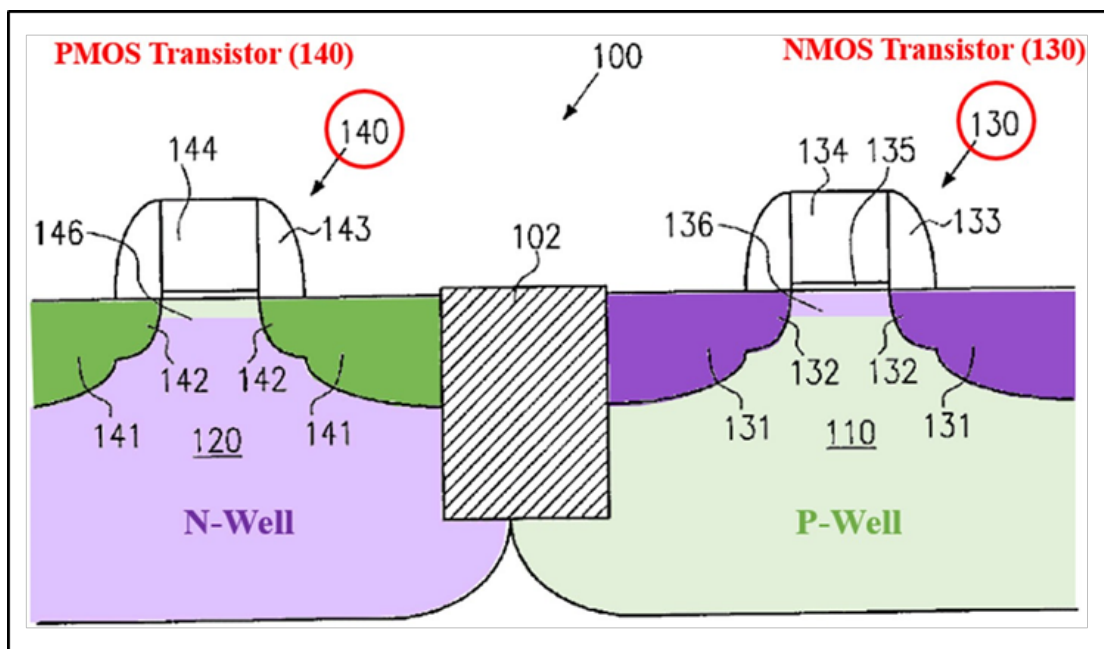
Ex. 1006, FIG. 1b.

8. Dependent Claim 9: “The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n- type.”

174. In my opinion, Wieczorek discloses or renders obvious the additional limitation of claim 9. As discussed above and illustrated in Figure 1b below, the channel region (light purple, indicated by lead line 136) of the first active region is formed at the top of P-well 110 is, in my opinion, of the same doping type (p-type) as P-well 110. Ex. 1006, [0008] (“for defining the P-well structure 110, typically

boron ions are employed”). Boron ions are p-type dopants. *See, e.g.*, Ex. 1007, 15:28-29.

175. Likewise, the channel region (light green, indicated by lead line 146) of the second active region is formed at the top of N-well 120 and is of the same doping type (n-type) as N-well 120. Ex. 1006, [0008] (“[f]or defining the N-well structure 120, typically phosphorous or arsenic ions are used”). Phosphorous and arsenic ions are n-type dopants. *See, e.g.*, Ex. 1007, 9:33-35.



Ex. 1006, FIG. 1b.

176. In my opinion, those channel regions have a graded dopant concentration, as discussed above. Section X.B.1.f.

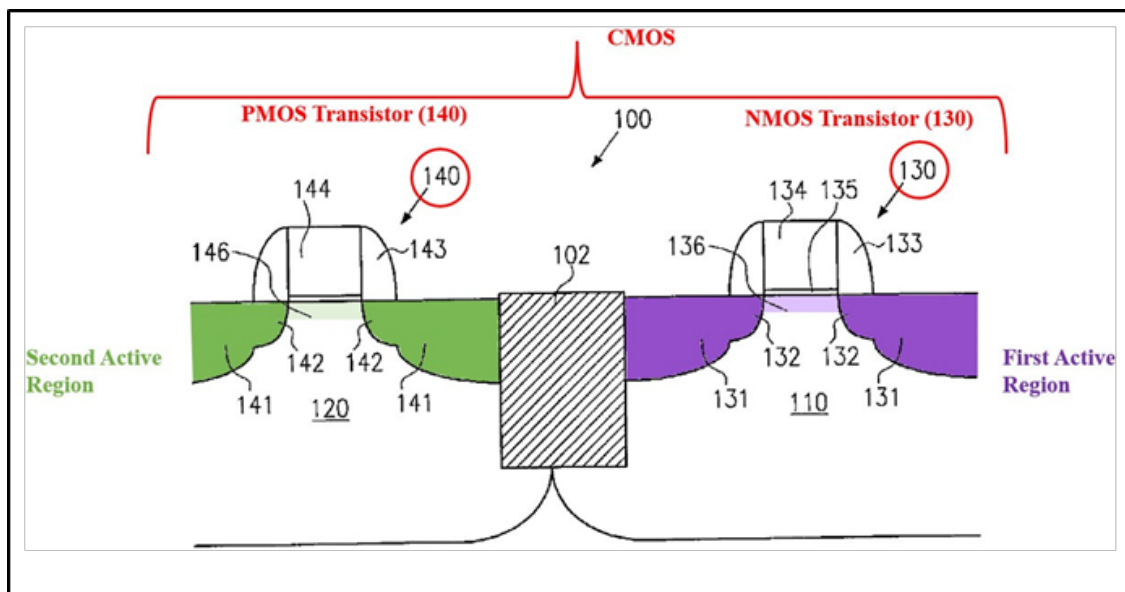
9. **Dependent Claim 12: “The semiconductor device of claim 1, wherein dopants of the graded dopant region in the well region are both p-type and n-type.”**

177. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 12. As I explained above for element [1.1], *see* Section X.B.1.b, Wieczorek discloses a conventional twin-well CMOS device that includes an “N-well structure 120,” Ex.1006, [0007], which is formed by ion implantation of n-type dopants, “typically phosphorous or arsenic ions.” *Id.*, [0008]. While not shown, Wieczorek explains that N-well 120 would be “formed on” any “appropriate substrate.” *Id.*, [0004]; *see also id.*, [0027] (describing, for Figure 3a, that the N-well and P-well structures therein are “formed in a semiconductor substrate 301”). Since Wieczorek does not specify what constitutes an “appropriate substrate,” a POSITA would have been motivated to consult Wolf, which confirms that a “uniform, lightly doped p- or n-type substrate” is a suitable substrate commonly used in twin-well CMOS devices. Ex.1008C, 523, 530 (“With the twin-tub [(twin-well)] approach, two separate wells are formed for n- and p-channel transistors on a lightly doped substrate ... of n or p material.”), FIG. 8-1(e); Ex.1008B, 387-389. For the reasons I explained above for element [1.1], *see* Section X.B.1.b, for claim mapping purposes, the Wieczorek-Wolf substrate is taken as a p-type nonepitaxial substrate (*i.e.*, doped with p-type impurities). Accordingly, the Wieczorek-Wolf combination entails implanting an n-type impurity to form N-Well 120 into a p-type substrate. Because the implantation of the n-type impurity to form N-well 120 does not remove

the substrate's p-type dopants, the N-well 120 of the Wiczorek-Wolf combination would include “both p-type and n-type” dopants, as claim 12 requires.

10. Dependent Claim 13: “The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.”

178. In my opinion, Wiczorek discloses or renders obvious the additional limitation of claim 13. Wiczorek discloses “a complementary MOS [(CMOS)] transistor pair” comprising “an N-channel transistor 130” in the first active region (purple/light purple) and “a P-channel transistor 140” in the second active region (green/light green). Ex. 1006, [0007], [0012]-[0013].



Ex. 1006, FIG. 1b. Each of the CMOS transistors include a source, drain, gate, and channel. For example, N-channel transistor 130 includes “heavily N-doped source and drain regions 131” (purple), “gate electrode 134,” and “channel region 136” (light purple). Ex. 1006, [0012]-[0013]. Similarly, P-channel transistor 140 includes

“heavily P-doped source and drain regions 141” (green), “gate electrode 144,” and “channel region 146” (light green). Ex. 1006, [0012]-[0013]; Sections X.A.1.c-d, X.A.1.f.

11. Dependent Claim 14: “The semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM).”

179. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 14. Wieczorek’s teaching relied on in this declaration is directed to conventional CMOS technology. Section X.B.1.b; Ex. 1006, [0007], [0020]-[0021]. It would have been obvious, in my opinion, apply Wieczorek’s conventional CMOS technology to fabricate a DRAM device in order to realize “the advantages of cost per bit, device density, and flexibility of use (i.e., both read and write operations are possible)” which “have made DRAMs the most widely used form of semiconductor memory to date.” Ex. 1008B, 587, 597. Wieczorek also suggests doing so in teaching the frequent application of its technology to “mode[m] integrated circuits.” Ex. 1006, [0004], [0026]. Likewise, at the relevant time, DRAMs were known to be designed using conventional CMOS technology, and a POSITA would have appreciated that fabricating a DRAM using CMOS technology, such as that of Wieczorek, would have provided a number of advantages, including “lower power dissipation [] and smaller soft error rates,” lower design complexity, lower operating voltage, and reduced memory access time. Ex. 1008B, 596-597.

180. Additionally, in my opinion, using Wieczorek's technology to form a DRAM device would have merely amounted to combining known, conventional prior art elements (*i.e.*, Wieczorek's CMOS process and known CMOS DRAM designs) according to known methods (*i.e.*, Wieczorek's CMOS process) and, at most, involves a simple substitution of one known element (*i.e.*, CMOS technology contemplated by Wolf for DRAM) with another (*i.e.*, Wieczorek's conventional CMOS technology). In my opinion, there would have been a reasonable expectation of success with predictable results because Wieczorek's conventional CMOS process was a known technique and would have been used for its intended purpose in manufacturing DRAM devices, which were commonly implemented using CMOS technology in order to gain the benefits I mentioned above.

12. Dependent Claim 15: "The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate."

181. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 15. *See* Section X.B.1.b.

13. Dependent Claim 16: "The semiconductor device of claim 1, wherein the device is a flash memory."

182. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 16. Wieczorek's teaching relied on in this declaration is directed to conventional CMOS technology. Section X.B.1.b; Ex. 1006, [0007], [0020]-[0021]. Further, in my opinion, it would have been obvious to apply Wieczorek's

conventional CMOS technology to fabricate a flash memory device in order to achieve the benefits of “lower power dissipation” of CMOS technology and the “high density [], small-die size, lower cost, and hot-electron writability of EPROMs, together with the easy erasability, on-board reprogrammability, and electron-tunneling erasure features of EEPROMs.” Ex. 1008B, 634; Ex. 1008A, 808-810. Wieczorek also suggests doing so in teaching the frequent application of its technology to “mode[*rn*] integrated circuits.” Ex. 1006, [0004], [0026]. Indeed, flash memory devices commonly used CMOS technology. Ex. 1008B, 633-635 (describing known “CMOS flash-EEPROM” devices); Ex. 1007, 22:16-17 (flash EEPROM is flash memory), 22:10-23:2, FIG. 28 (peripheral flash memory circuit with CMOS transistors); Section X.A.12.

183. Additionally, in my opinion, using Wieczorek’s technology to form flash memory would have merely amounted to combining known, conventional prior art elements (*i.e.*, Wieczorek’s CMOS process and known CMOS flash memory designs) according to known methods (*i.e.*, Wieczorek’s CMOS process) and, at most, involves a simple substitution of one known element (*i.e.*, CMOS technology for prior art flash memory) with another (*i.e.*, Wieczorek’s conventional CMOS technology). There would have been, in my opinion, a reasonable expectation of success with predictable results because Wieczorek’s conventional CMOS process was a known technique and would have been used for its intended purpose in

manufacturing flash memory devices, which were commonly implemented using CMOS technology in order to gain the benefits I mentioned above.

14. Dependent Claim 17: “The semiconductor device of claim 1, wherein the device is a logic device.”

184. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 17. Section X.B.1.a; Ex. 1006, Title, [0007]. Wieczorek’s teaching relied on in this declaration is directed to conventional CMOS technology. Section X.B.1.b; Ex. 1006, [0007], [0020]-[0021]. In my opinion, it would have been obvious to apply Wieczorek’s conventional CMOS technology to fabricate known logic devices, including inverters and microprocessors (CPUs), in order to achieve the benefits of “lower power-dissipation” of CMOS technology in such devices. Ex. 1008B, 368-370; Ex. 1032, 1334. Wieczorek suggests doing so in teaching the frequent application of its technology to “mode[*rn*] integrated circuits.” Ex. 1006, [0004], [0026]. Indeed, twin-well CMOS technology was, by the early 2000s, “the dominant CMOS technology in IC production.” Ex. 1008D, 181.

185. Rabaey confirms this. Ex. 1025, 180 (“The [CMOS] inverter is truly the nucleus of all digital [logic] designs” and, together with other “[logic] gates such as NAND, NOR, or XOR ... form the building blocks for modules such as multipliers and processors.”); *id.*, 37 (“Modern [CMOS] processes are increasingly using a dual-well [(twin-well)] approach that uses both n- and p-wells ...”), 383-

384, FIG. 8-6 (showing Intel Pentium processor “designed in a 0.18 μ m CMOS technology”). Inverters and processors are logic devices.

186. Sze also confirms this, describing a system-on-a-chip that includes CMOS “logic IC (e.g., CPU)” fabricated using twin-well CMOS technology. Ex. 1022, 525-26, FIGS. 37-38.

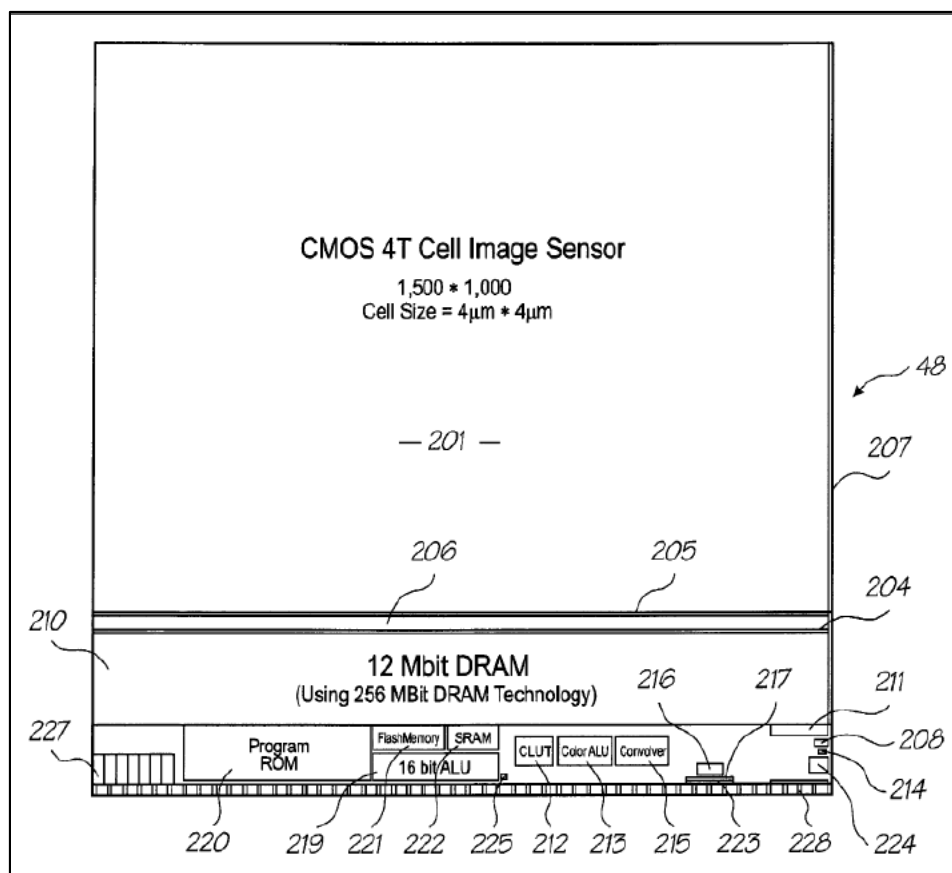
187. Additionally, in my opinion, using Wieczorek’s technology to form logic devices such as CPUs would have merely amounted to combining known, conventional prior art elements (*i.e.*, conventional twin-well CMOS process described in Wieczorek and known digital device designs, including CPUs) according to known methods (*i.e.*, Wieczorek’s conventional twin-well CMOS process) and, at most, involves a simple substitution of one known element (*i.e.*, CMOS technology for prior art logic devices, including CPUs) with another (*i.e.*, Wieczorek’s conventional CMOS technology). There would have been a reasonable expectation of success with predictable results because Wieczorek’s conventional twin-well CMOS process was a known technique and would have been used for its intended purpose in manufacturing known logic devices, including CPUs, designed for implementation using CMOS technology, in order to achieve the benefits I described above.

15. Dependent Claim 18: “The semiconductor device of claim 17, wherein the device is central processing unit.”

188. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 18. *See* Section X.B.13. In my opinion, a POSITA would have understood that a microprocessor includes a central processing unit (CPU). Ex. 1032, 1334.

16. Dependent Claim 19: “The semiconductor device of claim 1, wherein the device is an image sensor.”

189. In my opinion, it would have been obvious to a POSITA to implement the semiconductor device disclosed in Wieczorek and Wolf in an image sensor. The semiconductor device illustrated in Wieczorek is “a complementary MOS [or CMOS] transistor pair.” Ex. 1006, [0007]. CMOS designs were routinely used in numerous types of devices, as Wolf noted “CMOS is now the dominant integrated circuit technology[.]” Ex. 1008B, 104. As explained above, Kawagoe teaches that the CMOS techniques can be applied to semiconductor integrated circuit devices with other logic circuits. *Supra*, X.A.19; Ex. 1007, 24:21-31. A POSITA would have understood that one example such an application would be an image sensor. One example of such an image sensor is shown in Silverbrook, pictured below. Ex. 1042, 6:41-13:39, FIG. 15.



190. Consistent with the applications hypothesized in Wieczorek-Wolf, Silverbrook’s image sensor includes “CMOS logic, a CMOS image sensor, DRAM, and analog circuitry.” *Id.*, 6:56-57. As such, it would have been obvious to a POSITA that the designs in Wieczorek-Wolf could be implemented in an image sensor.

17. Independent Claim 20

a. Preamble: “A semiconductor device, comprising:”

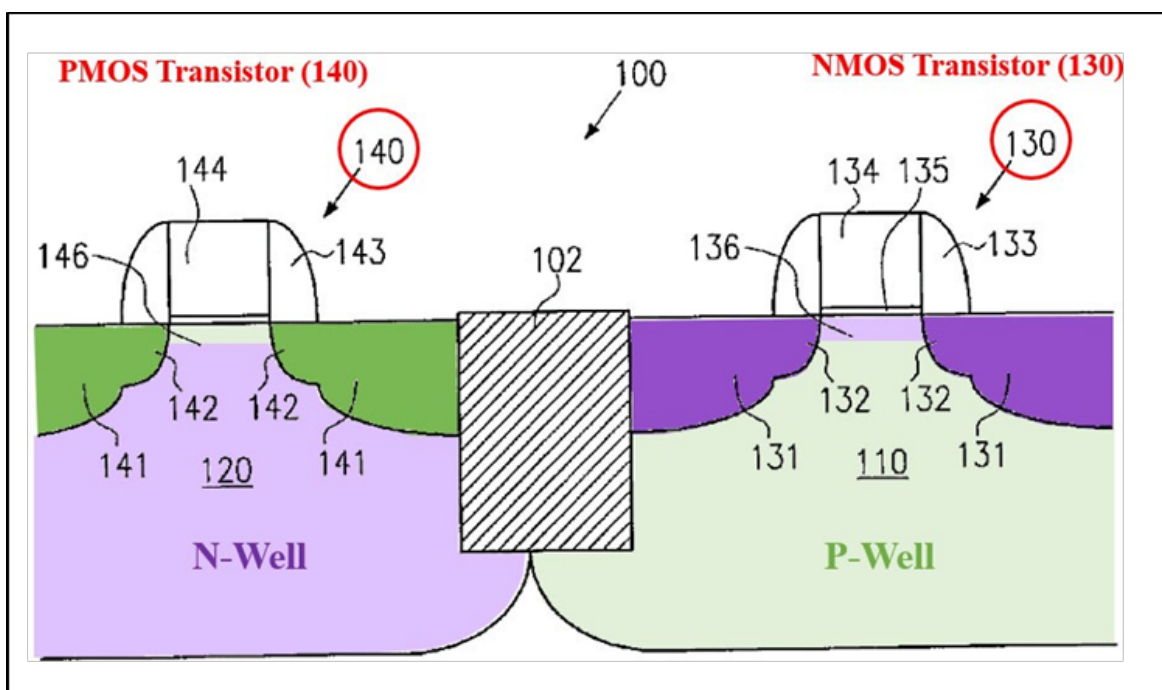
191. To the extent the preamble is limiting, in my opinion, Wieczorek discloses it. *See* Section X.B.1.a.

b. Element [20.1]: “a substrate of a first doping type at a first doping level having first and second surfaces;”

192. In my opinion, Wieczorek-Wolf renders this element obvious. *See* Section X.B.1.b.

- c. **Element [20.2]: “a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;”**

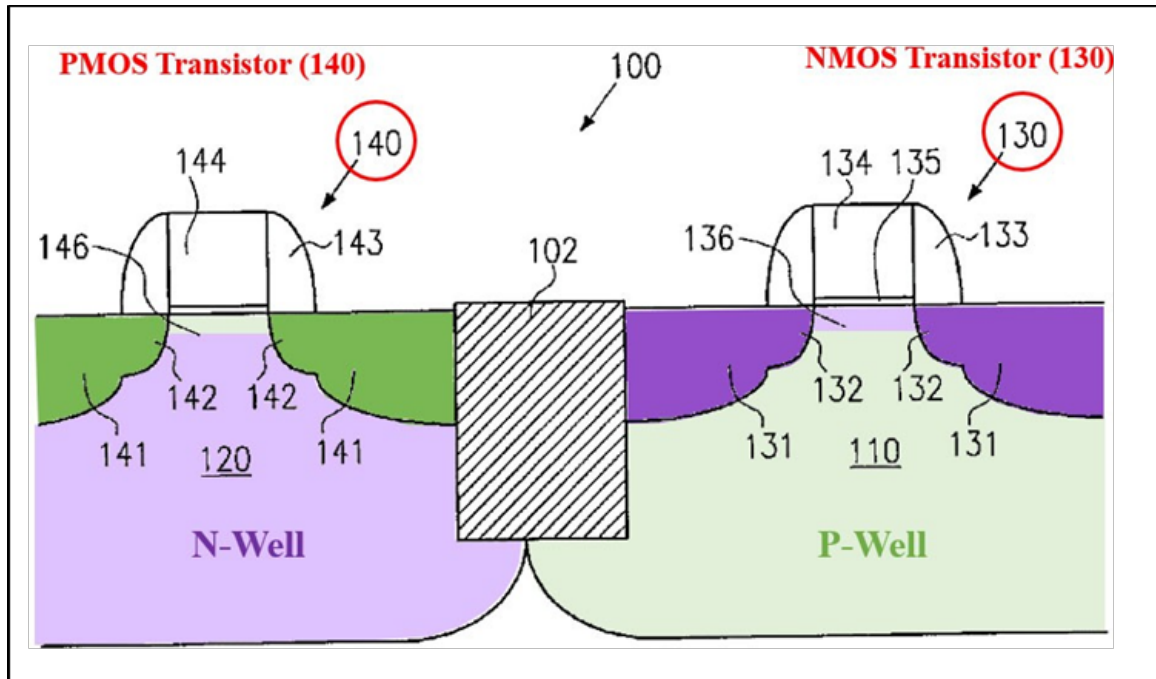
193. In my opinion, Wieczorek-Wolf renders obvious this element. *See* Section X.B.1.c. As shown below, Wieczorek discloses an N-channel transistor 130 formed in the surface of the first active region.



Ex. 1006, FIG. 1b.

- d. **Element [20.3]: “a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;”**

194. In my opinion, Wieczorek discloses or renders obvious this element. *See* Section X.B.1.d. As shown below, Wieczorek discloses a P-channel transistor 140 formed in the surface of the second active region.



Ex. 1006, FIG. 1b.

- e. **Element [20.4]: “transistors formed in at least one of the first active region or second active region;”**

195. In my opinion, Wieczorek discloses or, at a minimum, renders obvious this element. *See* Section X.B.1.e.

- f. **Element [20.5]: “at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and”**

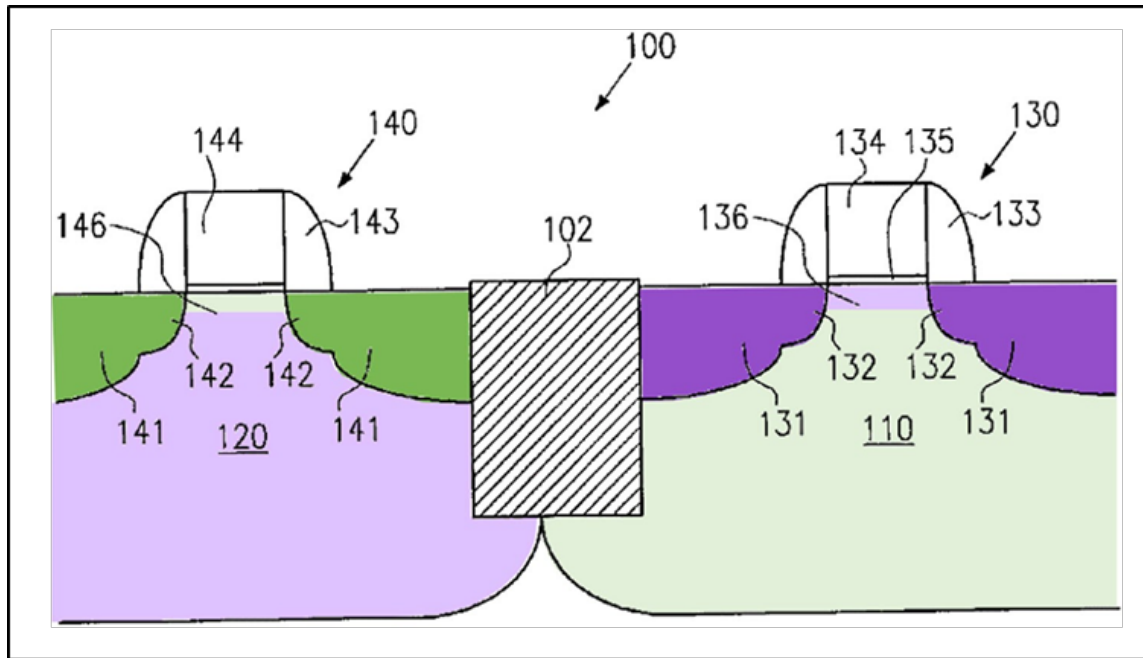
196. In my opinion, Wieczorek-Wolf renders obvious this element. *See* Section X.B.1.f.

- g. Element [20.6]: “at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.”**

197. In my opinion, Wieczorek-Wolf renders obvious this element. *See* Section X.B.1.g.

18. Dependent Claim 21: “The semiconductor device of claim 20, “wherein the substrate is an n- type substrate.”

198. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 21. As I explained in Section X.B.1.b, n- type and p- type substrates are both suitable for Wieczorek’s CMOS device, and a p- type substrate is chosen for claim mapping of claims 1 and 20. Section X.B.1.b. With an n- type substrate, claim element [20.2] requiring “a first active region ... with a second doping type opposite in conductivity to the first doping type” of the substrate is met by mapping the first active region to the source/drain/channel regions 141/142/146 (green/light green) of pMOS transistor 140, and claim element [20.3] is met by mapping the second active region to the source/drain/channel regions 131/132/136 (purple/light purple) of nMOS transistor 130. *Id.*



Ex. 1006, FIG. 1b.

19. Dependent Claim 22: “The semiconductor device of claim 20, wherein the substrate is a p-type substrate.”

199. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 22. *See* Section X.B.2.

20. Dependent Claim 24: “The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.”

200. In my opinion, Wieczorek discloses or, at a minimum, renders obvious the additional limitation of claim 24. *See* Section X.B.3.

21. Dependent Claim 25: “The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.”

201. In my opinion, Wieczorek discloses or, at a minimum, renders obvious the additional limitation of claim 25. *See* Section X.B.4.

22. Dependent Claim 26: “The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.”

202. In my opinion, Wieczorek discloses or, at a minimum, renders obvious the additional limitation of claim 26. *See* Section X.B.5.

23. Dependent Claim 27: “The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.”

203. In my opinion, Wieczorek discloses or, at a minimum, renders obvious the additional limitation of claim 27. *See* Section X.B.8.

24. Dependent Claim 30: “The semiconductor device of claim 20, wherein dopants of the graded dopant region in the well region are both p-type and n-type.”

204. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 30. *See* Section X.B.9.

25. Dependent Claim 31: “The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.”

205. In my opinion, Wieczorek discloses or, at a minimum, renders obvious the additional limitation of claim 31. *See* Section X.B.6.

26. Dependent Claim 32: “The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.”

206. In my opinion, Wieczorek discloses or, at a minimum, renders obvious the additional limitation of claim 32. *See* Section X.B.17.b. Wieczorek teaches a “complementary MOS [(CMOS)] transistor pair” formed in and including a substrate. Ex. 1006, [0007], [0012]-[0013].

27. Dependent Claim 33: “The semiconductor device of claim 20, wherein the device is a flash memory.”

207. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 33. *See* Section X.B.13.

28. Dependent Claim 34: “The semiconductor device of claim 20, wherein the device is a logic device.”

208. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 34. *See* Section X.B.14.

29. Dependent Claim 35: “The semiconductor device of claim 34, wherein the device is central processing unit.”

209. In my opinion, Wieczorek-Wolf renders obvious the additional limitation of claim 35. *See* Section X.B.15.

30. Dependent Claim 36: “The semiconductor device of claim 34, wherein the device is an image sensor.”

210. In my opinion, Wieczorek combined with Wolf and Silverbrook renders obvious the additional limitation of claim 36. *See* Section X.B.16.

C. GROUNDS III/IV

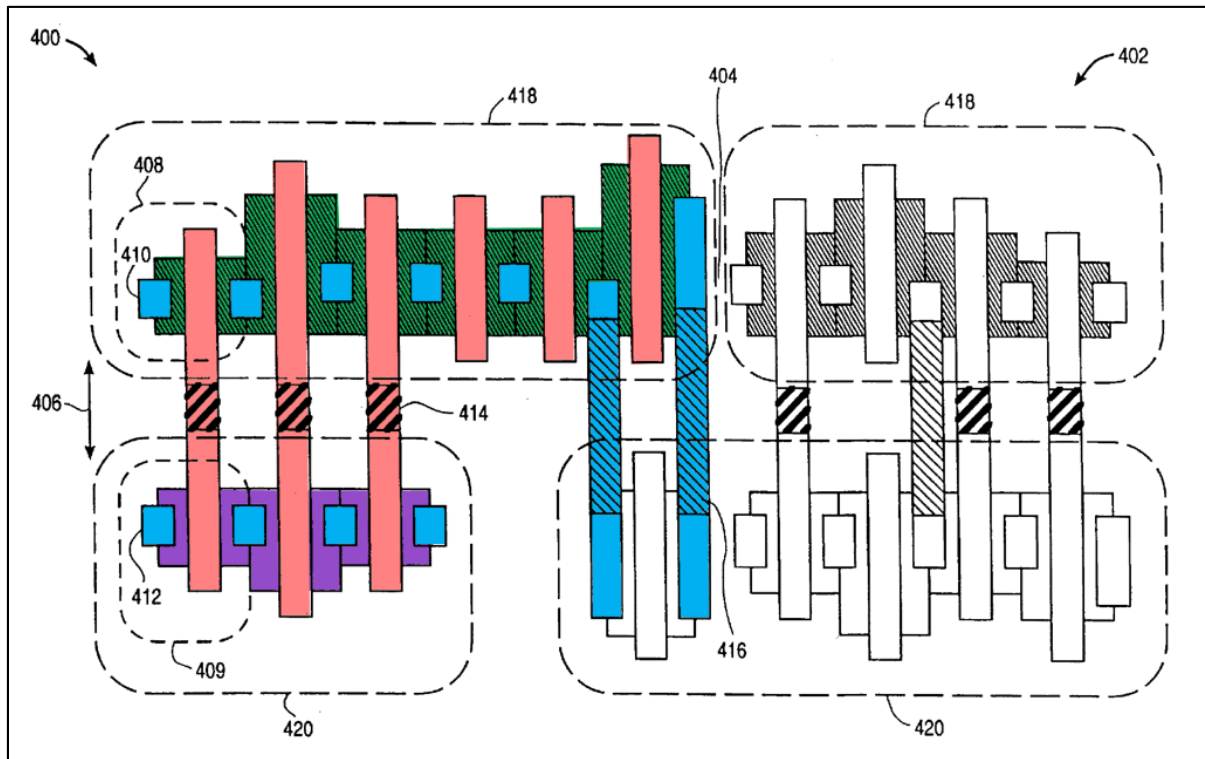
211. Several claim elements of the Challenged Claims recite “transistors” or “devices.” *See* Claim Elements [1.2]-[1.4], [20.2]-[20.4] and Dependent Claims 4,

5, 13, 24, 25. As I discussed above under Grounds I and II, I understand that the Patent Owner interprets these claim elements as requiring one or more transistors, and not a plurality of transistors. *See* Sections X.A.1.c-d, X.B.1.c-d. Notably, I understand that according to Patent Owner, an “active region ... within which transistors can be formed” means “an active region ... where a transistor can be formed.” Ex. 1020, 31. The present Grounds III and IV mirror grounds I and II, respectively, except that I have combined Gupta with the ground references (Kawagoe of Ground I, Wiczorek-Wolf of Ground II) to render obvious those claim elements under an interpretation of “transistors” or “devices” to require a plurality of such devices.

212. Gupta is directed to “automatically producing layouts for CMOS circuits,” recognizing that “semiconductor chips [have] become ever larger, incorporating ever more devices.” Ex. 1014, 1:7-10, 1:28-31. Wolf confirms that, at the time, various chips (*e.g.*, DRAM, microprocessors, and flash memory) were fabricated with tens of millions to more than a billion devices. Ex. 1008A, xxxiii, FIG. 1; Ex. 1008B, 634. In my opinion, Gupta reflects the knowledge of a POSITA by explaining that a “primary goal” of semiconductor chip development has therefore been to minimize the chip area required to form any circuit so that more transistors can be packed in the same chip (or so that the same number of transistors can be formed on a smaller chip area), regardless of the technology and chip

fabrication process. Ex. 1014, 1:28-35 (“As semiconductor chips become ever larger, incorporating ever more devices, it becomes increasingly important to minimize semiconductor area used by a given number of devices. Conservation of semiconductor area is a *primary goal* in semiconductor chip development....”). Gupta further reflects the knowledge of a POSITA by explaining that good circuit layout practice dictates forming as many transistors in the same active region through diffusion abutment as possible, to minimize area-wasting diffusion gaps. *Id.*, 1:52-54 (“One technique conserves area by placing transistors so as to *share diffusion area.*”), 2:17-21 (“Transistors which are abutted in a layout form transistor chains. It is desirable to produce a layout with a *maximum number of transistors chained* so as to minimize diffusion gaps.”); Ex. 1023, 5 (“An important layout task is to place and orient the transistors on the chip to *minimize the layout area* of the circuit” by avoiding “area-wasting diffusion gap[s]”). Gupta describes several techniques to perform this, such as transistor folding and chaining, to achieve an optimal layout. Ex. 1014, 1:49-2:24, 3:64-4:1, FIGS. 2-3.

213. Gupta’s Figure 4 (below)—where transistor gates and metal contacts that overlay the active regions are colored in red and blue respectively—illustrates *six* chained PMOS transistors formed in a p-channel active region (green) and *three* chained NMOS transistors formed in an n-channel active region (purple). Ex. 1014, 4:23-43.



214. In my opinion, Jin further confirms that transistors arranged as in Gupta are formed in a common active region. The first image below is the circuit schematic of a conventional 6T SRAM cell, and the cell layout, second image below, shows two transistors (1 and 2) formed in active region 21 (red), and two other transistors (3 and 4) formed in active region 24 (blue). Ex. 1015, 6:17-29; Ex. 1025, 48 (“*Diffusion regions* (n⁺ and p⁺), which define the areas where transistors can be formed[,] are often called the *active areas*.”) (italics in original).

216. In my opinion, the combinations gain the additional benefit of improved immunity to soft errors through appropriate well doping. Ex. 1007, 15:62-16:11 (“the electrons produced by the α -ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well 6p so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p”). Combining the teachings of Gupta with those of Kawagoe or Wieczorek-Wolf merely amounts to (1) use of a known technique (*i.e.*, Kawagoe’s or Wieczorek-Wolf’s CMOS fabrication process) to improve similar devices (*i.e.*, CMOS chips designed with Gupta’s layout) in the same way (*i.e.*, to achieve submicron dimensions and improve immunity to soft errors); (2) use of a known technique (*i.e.*, Gupta’s optimal layout generation) to improve similar devices (*i.e.*, submicron CMOS chips fabricated according to Kawagoe or Wieczorek-Wolf’s CMOS fabrication process) in the same way (*i.e.*, to minimize chip area and increase packing density); and (3) combining prior art elements (*i.e.*, Kawagoe or Wieczorek-Wolf’s CMOS fabrication process and Gupta’s CMOS layout generation) according to known methods (*i.e.*, as taught by Kawagoe or Wieczorek-Wolf and Gupta). There is reasonable expectation of success with predictable results because Kawagoe’s and Wieczorek-Wolf’s CMOS fabrication process would be used for their intended purpose of fabricating CMOS circuits according to known CMOS layouts generated by Gupta, which would also be used for its intended purpose. Further, it is my

opinion that Gupta's optimal circuit layout is process-agnostic, and applies to the layout of *any* CMOS semiconductor chip, including the layout of CMOS chips fabricated according to the teachings of Kawagoe and/or Wieczorek-Wolf. *See generally* Ex. 1014, 1:7-10, 3:64-4:11.

217. In my opinion, a POSITA would have understood that, in such a combination, the active regions would be laid out as shown in Gupta's figures (*e.g.*, Fig. 4) and those active regions would be formed in wells (*i.e.*, n-channel active regions are formed in p-wells, and p-channel active regions are formed in n-wells as taught in Kawagoe and Wieczorek), whereby the wells have downward-sloping graded dopant concentrations as shown in Kawagoe's Figure 17 and Wieczorek's Figure 2b. *Id.* I am also of the opinion that, assuming a p-type substrate is used, the n-channel active region (purple) in Gupta's Figure 4 is an example of the claimed first active region, and that the p-channel active region (green) is an example of the claimed second active region. Conversely, if instead an n-type substrate is used, the p-channel active region (green) is an example of the claimed first active region, and the n-channel active region (purple) is an example of the claimed second active region. In either case, the two active regions are adjacent and separated by an isolation region (field oxide), as required under elements [1.3], [20.3] and claims 6 and 26. Ex. 1014, 1:16-19, 4:39; Ex. 1008A, 818-820; Sections X.A.1.d, X.A.6, X.B.1.d, X.B.5.

218. Conversely, in my opinion, a POSITA would have understood that each of the active regions of Kawagoe's and Wieczorek's CMOS devices typically contains many transistors, as taught by Gupta and illustrated in Gupta's Figure 4. This is the case whether the device is a DRAM, flash memory, logic device or CPU (as claimed in claims 14, 16-18, 33-35). Each such device is a "very large scale integrated circuit" for which "it becomes increasingly important to minimize semiconductor area used[,]" and this requires forming as many transistors as possible in any active region. Ex. 1014, 1:13-14, 1:28-34, 2:17-21.

219. In light of the above, in my opinion, Kawagoe in view of Gupta renders claims 1-9, 12-14, 16-27, and 30-36 obvious (Ground III). Likewise, in my opinion, Wieczorek-Wolf in view of Gupta renders claims 1-2, 4-9, 12-22, 24-27, and 30-36 obvious (Ground IV).

D. GROUNDS V/VI

220. Claims 19 and 36 recite "[t]he semiconductor device of claim [1/20], wherein the device is an image sensor." As discussed under Grounds I-II, it would have been obvious to a POSITA to implement either the CMOS designs in Kawagoe (X.A.15) or in Wieczorek-Wolf (X.B.15) in an image sensor.

221. Both Kawagoe and Wieczorek-Wolf expressly disclose CMOS designs (Ex. 1007, 14:46-19:64; Ex. 1006, [0007]-[0014]), and Silverbrook discloses use of a "CMOS pixel image sensor." Ex. 1042, 6:41-67. Because Silverbrook calls for a

“CMOS” image sensor, but does not include any details about the fabrication of CMOS devices, a POSITA would have been motivated to implement the CMOS devices designs disclosed by Kawagoe and Wieczorek-Wolf, respectively. Indeed, Silverbrook expressly seeks incorporation of existing CMOS designs into its image sensor device, highlighting that “[t]he CPU, DRAM, Image Sensor, ROM, Flash memory ... can be vendor supplied cores.” Ex. 1042, 7:28-30. Silverbrook also refers to an academic paper disclosing “[t]he latest advances in the field of image sensing and CMOS image sensing in particular,” which discloses techniques consistent with the teachings of Kawagoe and Wieczorek-Wolf. *Id.*, 7:41-48 (citing [Ex. 1044] Wong et al., “CMOS Active Pixel Image Sensors Fabricated Using a 1.8V, 0.25 μm CMOS Technology.”). Silverbrook tells us that Wong discloses “a specific implementation similar to that disclosed in the present application.” Ex, 1042, 7:44-46. Because of the consistency in the technologies used in Silverbrook/Wong with respect to Kawagoe and Wieczorek-Wolf, a POSITA would have understood that the techniques used in Kawagoe and Wieczorek-Wolf could also be applied to an image sensor such as in Silverbrook/Wong. Using the CMOS device designs from Kawagoe and Wieczorek-Wolf in the CMOS image sensor from Silverbrook would have been nothing more than the combination of familiar elements according to known methods yielding predictable results. Accordingly, a POSITA would also have had a reasonable expectation of success in combining the

CMOS designs from Kawagoe and Wieczorek-Wolf with Silverbrook's CMOS image sensor. Thus, claims 19 and 36 are rendered obvious by Kawagoe in view of Silverbrook (Ground V) and also by Wieczorek-Wolf in view of Silverbrook (Ground VI).

XI. CONCLUSION

222. For the aforementioned reasons, in my opinion, to a person of ordinary skill in the art, the Challenged Claims of the '481 Patent are rendered obvious by the prior art.

223. I understand that the Patent Owner has not asserted secondary considerations of non-obviousness. I reserve the right to respond to any such assertions.

224. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the results of the proceedings.

Executed on October 10, 2023

Respectfully submitted,



Sanjay Banerjee

LISTING OF CHALLENGED CLAIMS

Element	Claim Language
[1.pre]	“A semiconductor device, comprising”
[1.1]	“a substrate of a first doping type at a first doping level having first and second surfaces;”
[1.2]	“a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;”
[1.3]	“a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;”
[1.4]	“transistors formed in at least one of the first active region or second active region;”
[1.5]	“at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and”
[1.6]	“at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.”
2	The semiconductor device of claim 1, wherein the substrate is a p- type substrate.
3	The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.
4	The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.
5	The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.
6	The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.

7	The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.
8	The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.
9	The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p- type or n- type.
12	The semiconductor device of claim 1, wherein dopants of the graded dopant region in the well region are both p-type and n-type.
13	The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.
14	The semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM).
15	The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.
16	The semiconductor device of claim 1, wherein the device is a flash memory.
17	The semiconductor device of claim 1, wherein the device is a logic device.
18	The semiconductor device of claim 17, wherein the device is central processing unit.
19	The semiconductor device of claim 1, wherein the device is an image sensor.
[20.pre]	A semiconductor device, comprising:
[20.1]	a substrate of a first doping type at a first doping level having first and second surfaces;
[20.2]	a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;
[20.3]	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;

[20.4]	transistors formed in at least one of the first active region or second active region;
[20.5]	at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and
[20.6]	at least one well region adjacent to the first or second active region containing at least one graded dopant region, the
	graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.
21	The semiconductor device of claim 20, wherein the substrate is an n- type substrate.
22	The semiconductor device of claim 20, wherein the substrate is a p- type substrate.
23	The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.
24	The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.
25	The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.
26	The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.
27	The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p- type or n- type.
30	The semiconductor device of claim 20, wherein dopants of the graded dopant region in the well region are both p-type and n-type.
31	The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.
32	The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.
33	The semiconductor device of claim 20, wherein the device is a flash memory.

34	The semiconductor device of claim 20, wherein the device is a logic device.
35	The semiconductor device of claim 34, wherein the device is central processing unit.
36	The semiconductor device of claim 20, wherein the device is an image sensor.