UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TEXAS INSTRUMENTS INCORPORATED,

Petitioner

v.

GREENTHREAD LLC,

Patent Owner

Patent No. 10,734,481
Case No. IPR2024-00772

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,734,481

UNDER 35 U.S.C. §§ 312 AND 37 C.F.R. § 42.104

TABLE OF CONTENTS

I. INTRODUCTION 1
II. MANDATORY NOTICES 1
A. Real Party-in-Interest 1
B. Related Matters 1
C. Counsel Service Information 3
D. 37 C.F.R. §42.8(b)(4): Service Information 3
III. PAYMENT OF FEES UNDER 37 C.F.R. §42.103 3
IV. CERTIFICATION OF GROUNDS FOR STANDING 4
V. OVERVIEW OF CHALLENGE AND REQUESTED RELIEF 4
A. Prior Art Printed Publications 4
B. Relief Requested 5
VI. THE '481 PATENT 5
VII. PERSON OF ORDINARY SKILL IN THE ART 8
VIII. CLAIM CONSTRUCTION 8
IX. OVERVIEW OF THE PRIOR ART 10
A. Kawagoe 10
B. Wieczorek 11
C. Wolf 12
D. Gupta 13
E. Silverbrook 13
X. SPECIFIC GROUNDS FOR PETITION 13
A. Ground I: 13

1. Independent Claim 1[7] 14
2. Claim 2 36
3. Claim 3 36
4. Claim 4 36
5. Claim 5 36
6. Claim 6 38
7. Claim 7 38
8. Claim 8 39
9. Claim 9 39
10. Claim 12 40
11. Claim 13 41
12. Claim 14 42
13. Claim 16 42
14. Claim 17 44
15. Claim 18 44
16. Claim 19 44
17. Independent Claim 20.....46
18. Claim 21 47
19. Claim 22 48
20. Claim 23 48
21. Claim 24 48
22. Claim 25 48
23. Claim 26 48

24. Claim 27 49
25. Claim 30 49
26. Claim 31 49
27. Claim 32 49
28. Claim 33 49
29. Claim 34 49
30. Claim 35 49
31. Claim 36 49

B. Ground II 50

1. Independent Claim 1 51
2. Claim 2 65
3. Claim 4 66
4. Claim 5 66
5. Claim 6 67
6. Claim 7 67
7. Claim 8 68
8. Claim 9 68
9. Claim 12 69
10. Claim 13 70
11. Claim 14 71
12. Claim 15 72
13. Claim 16 72
14. Claim 17 73

15. Claim 18 75
16. Claim 19 75
17. Independent Claim 20 76
18. Claim 21 78
19. Claim 22 79
20. Claim 24 79
21. Claim 25 80
22. Claim 26 80
23. Claim 27 80
24. Claim 30 80
25. Claim 31 80
26. Claim 32 80
27. Claim 33 80
28. Claim 34 80
29. Claim 35 81
30. Claim 36 81

C. GROUNDS III/IV 81

D. GROUNDS V/VI 87

XI. THE BOARD SHOULD INSTITUTE IPR 88

A. 35 U.S.C. § 314(a) 88

B. 35 U.S.C. § 325(d) 89

C. Prior Terminated Petitions Do Not Warrant Denying Institution 92

CERTIFICATE OF SERVICE 99

TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 10,734,481 to Rao (the "'481 Patent")
1002	Prosecution History of the '481 Patent
1003	Declaration of Sanjay Banerjee, PhD
1004	Curriculum Vitae of Sanjay Banerjee, PhD
1005	Publication Declaration of Sean O'Bryan for Maziasz ("O'Bryan Decl.")
1006	U.S. Patent Application Publication No. 2003/0183856 to Wieczorek ("Wieczorek")
1007	U.S. Patent No. 6,043,114 to Kawagoe, et al. ("Kawagoe")
1008A	Wolf and Tauber, *Silicon Processing For The VLSI Era*, Vol 1, Lattice Press (2000) ("Wolf.1")
1008B	Wolf and Tauber, *Silicon Processing For The VLSI Era*, Vol 2, Lattice Press (2000) ("Wolf.2")
1008C	Wolf and Tauber, *Silicon Processing For The VLSI Era*, Vol 3, Lattice Press (2000) ("Wolf.3")
1008D	Wolf and Tauber, *Silicon Processing For The VLSI Era*, Vol 4, Lattice Press (2000) ("Wolf.4")
1009	Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Intl Conf on VLSI Design, IEEE 2008 ("Wang")
1010	U.S. Patent No. 4,481,522 ("Jastrzebski")
1011	Publication Declaration of Martin L. Knott for Rabaey ("Knott Decl.")
1012	Publication Declaration of Alyssa G. Resnick for Wolf.1 and Wolf.2 ("Resnick Decl.")
1013	Publication Declaration of Rachel J. Watters for Wolf.3 and Wolf.4 ("Watters Decl.")
1014	U.S. Patent No. 6,163,877 ("Gupta")
1015	U.S. Patent No. 6,534,805 ("Jin")
1016	Excerpts from the Prosecution History of U.S. Patent No. 8,421,195 (the "'195 Patent")
1017	Patent Owner's Proposed Constructions
1018	Blank
1019	Blank
1020	Patent Owner's Responsive Claim Construction Brief
1021	Blank

Exhibit No.	Description
1022	Sze, *Semiconductor Devices Physics and Technology*, 2d Ed., John Wiley & Sons (2002)
1023	Maziasz and Hayes, *Layout Minimization of CMOS Cells*, Kluwer Academic Publishers (1992) ("Maziasz")
1024	U.S. District Courts – Case Statistics, obtained at https://www.uscourts.gov/statistics-reports/analysis- reports/ federal-court-management-statistics, dated June 30, 2023
1025	Rabaey et al., *Digital Integrated Circuits, A Design Perspective*, Prentice Hall Electronics and VLSI Series (2003) ("Rabaey")
1026	Gregory and Shafer, "Latch-Up In CMOS Integrated Circuits," IEEE Transactions on Nuclear Science, Volume 20, Issue 6 (1973)
1027	U.S. Patent Application Publication No. 2007/0045682 to Hong et al. ("Hong")
1028	Excerpts from the Prosecution History of U.S. Patent Application Publication No. 10/934,915 (the "'915 App.")
1029	Excerpts from the Prosecution History of U.S. Patent No. 9,190,502 (the "'502 Patent")
1030	Excerpts from the Prosecution History of U.S. Patent Application Publication No. 13/854,319 (the "'319 App.")
1031	U.S. Patent No. 4,160,985 to Kamins et al. ("Kamins")
1032	McGraw-Hill Dictionary of Scientific and Technical Terms (2003)
1033	Excerpts from the Prosecution History of U.S. Patent No. 11,121,222 (the "'222 Patent")
1034	U.S. Patent No. 9,647,070 to Rao (the "'070 Patent")
1035	U.S. Patent Application Publication No. 2003/0030488 to Hueting *et al*. ("Hueting")
1036	Publication Declaration of Sylvia Hall-Ellis for Wolf
1037	Law360 Article "Stays Pending IPR In Del. District Courts Are Here To Stay," Kraning and Del Dotto, March 11, 2022.
1038	Dec. 21, 2022 Preliminary Claim Constructions in 6:22-CV-00105
1039	Oct. 31, 2022 Giapis Declaration, 6:22-CV-00105
1040	Blank
1041	Blank
1042	U.S. Patent No. 6,614,560 to Silverbrook ("Silverbrook")
1043	Blank
1044	Wong et al., "CMOS Active Pixel Image Sensors Fabricated Using a 1.8V, 0.25 um CMOS Technology."
1101	Petitioner's *Sotera* stipulation sent to Patent Owner on April 10,

Exhibit No.	Description
	2024

Texas Instruments Incorporated ("Petitioner" or "TI"), requests *inter partes* review ("IPR") of claims 1-9, 12-27, and 30-36 (the "Challenged Claims") of U.S. Patent No. 10,734,481 (Ex.1001, "the '481 Patent"). This Petition is accompanied by a Motion for Joinder to join pending IPR proceeding *Cirrus Logic, Inc., et al. v. Greenthread, LLC*, IPR2024-00001.

I. INTRODUCTION

The '481 Patent is directed to a semiconductor device having graded dopant concentrations in its active and well regions to aid carrier movement. Ex.1001, 4:50¬5:3 (claim 1), 5:54-6:15 (claim 20). The Challenged Claims are unpatentable as obvious.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner Texas Instruments Incorporated is the real party-in-interest.

B. Related Matters

The '481 Patent is the subject of the following active proceedings:

- *Greenthread, LLC v. Cirrus Logic, Inc.*, Civil Action No. 1:23-cv-00369 in the Western District of Texas, filed March 31, 2023 ("Cirrus District Court Case");
- *Greenthread, LLC v. OmniVision Technologies, Inc.*, Civil Action No. 2:23-cv-00212 in the Eastern District of Texas, filed May 10, 2023 ("OmniVision District Court Case");

- *Greenthread, LLC v. OSRAM GmbH et al.*, Civil Action No. 2:23-cv-00179 in the Eastern District of Texas, filed April 19, 2023 ("ams-OSRAM District Court Case");
  - *Greenthread, LLC v Texas Instruments Incorporated*, Civil Action No. 2:23-cv-00157 in the Eastern District of Texas, filed April 6, 2023;
  - *Greenthread, LLC v. Monolithic Power Systems, Inc.*, Civil Action No. 1:23-cv-00579 in the District of Delaware, filed May 26, 2023;
  - *Cirrus Logic, Inc., et al. v. Greenthread, LLC*, IPR2024-00001 before the Patent Trial and Appeal Board, filed October 12, 2023;
  - *Semiconductor Components Industries, LLC v. Greenthread, LLC*, IPR2024-00264 before the Patent Trial and Appeal Board, filed December 11, 2023; and
  - *Monolithic Power Systems, Inc. v. Greenthread, LLC*, IPR2024-00551 before the Patent Trial and Appeal Board, filed March 18, 2024.

The '481 Patent was previously subject to the following proceedings, which are no longer pending:

- *Greenthread, LLC v. Intel Corporation, Dell Inc.*, *and Dell Technologies Inc.*, Civil Action No. 6:22-cv-105 in the Western District of Texas ("Intel Litigation"), filed January 27, 2022;
- *Greenthread, LLC v. Intel Corporation*, Civil Action No. 6:22-cv-01293

in the Western District of Texas, severed December 21, 2022, and transferred to District of Oregon as 3:22-cv-02001;

- *Greenthread, LLC v. Micron Technology, Inc. et al., Civil Action No.* 1:23-cv-00333 in the District of Delaware, filed March 24, 2023;
- *Greenthread, LLC v. Western Digital Corporation et al*, Civil Action No.
- *Intel Corporation v. Greenthread, LLC*, IPR2023-00260, before the Patent Trial and Appeal Board, filed November 28, 2022;
- *Dell Technologies Inc. et al v. Greenthread, LLC*, IPR2023-00507, before the Patent Trial and Appeal Board, filed January 27, 2023; and
- *Sony Group Corporation v. Greenthread, LLC*, IPR2023-00375, before the Patent Trial and Appeal Board, filed December 17, 2022.

C. Counsel Service Information

Lead Counsel	Backup Counsel
Joshua A. Griswold, Reg. No. 46,310 Fish & Richardson P.C. 60 South Sixth Street, Suite 3200 Minneapolis, MN 55402 Tel: 214-292-4034 Fax: 877-769-7945 Email: IPR12189-0087IP1@fr.com	Patrick J. Bisenius, Reg. No. 63,893 Fish & Richardson P.C. 60 South Sixth Street, Suite 3200 Minneapolis, MN 55402 Tel: 612-766-2048 Fax: 877-769-7945 PTABInbound@fr.com

D. 37 C.F.R. §42.8(b)(4): Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR12189-0087IP1@fr.com (referencing No. 12189-0087IP1 and cc'ing PTABInbound@fr.com,

griswold@fr.com and bisenius@fr.com).

III. PAYMENT OF FEES UNDER 37 C.F.R. §42.103

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. 06-1050. Review of 25 claims is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

IV. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under Rule 42.104(a) that the '481 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the grounds identified in this Petition.

V. OVERVIEW OF CHALLENGE AND REQUESTED RELIEF

A. Prior Art Printed Publications

The '481 Patent claims priority to September 3, 2004. Petitioner's challenge is based on the following prior-art references, none of which were before the Patent Office during prosecution of the '481 Patent:

- **Kawagoe**: U.S. Patent No. 6,043,114 to Kawagoe et al. (Ex.1007) issued on March 28, 2000 and is prior art under 35 U.S.C. §102(b).[1]
- **Wieczorek**: U.S. Patent Application Publication 2003/0183856 to Wieczorek *et al.* (Ex.1006) was filed on October 29, 2002 and published on October 2,

[1] Cites to 35 U.S.C. §§102-103 are to the pre-America Invents Act.

2003. Wieczorek is prior art under 35 U.S.C. §102(a) and §102(e).

- **Wolf:** Wolf and Tauber, Silicon Processing for the VLSI Era, Lattice Press (2000) (Exs. 1008A-D), was published and publicly available no later than 2002, and is prior art under 35 U.S.C. §102(b). Exs. 1012-1013; Ex.1036.[2]
- **Gupta**: U.S. Patent No. 6,163,877 to Gupta (Ex.1014) issued on December 19, 2000 and is prior art under 35 U.S.C. §102(b).
- **Silverbrook**: U.S. Patent No. 6,614,560 to Silverbrook (Ex.1042) issued September 2, 2003 and is prior art under §102(b).

B. Relief Requested

The specific grounds of the challenge are set forth below and are supported by Dr. Banerjee (Ex.1003).

Ground	Basis	Challenged Claims	Reference(s)
I	§103	1-9, 12-14, 16-27, 30-36	Kawagoe
II	§103	1-2, 4-9, 12-22, 24-27, 30-36	Wieczorek, Wolf
III	§103	1-9, 12-14, 16-27, 30-36	Kawagoe, Gupta
IV	§103	1-2, 4-9, 12-22, 24-27, 30-36	Wieczorek, Wolf, Gupta
V	§103	19, 36	Kawagoe, Silverbrook
VI	§103	19, 36	Wieczorek, Wolf, Silverbrook

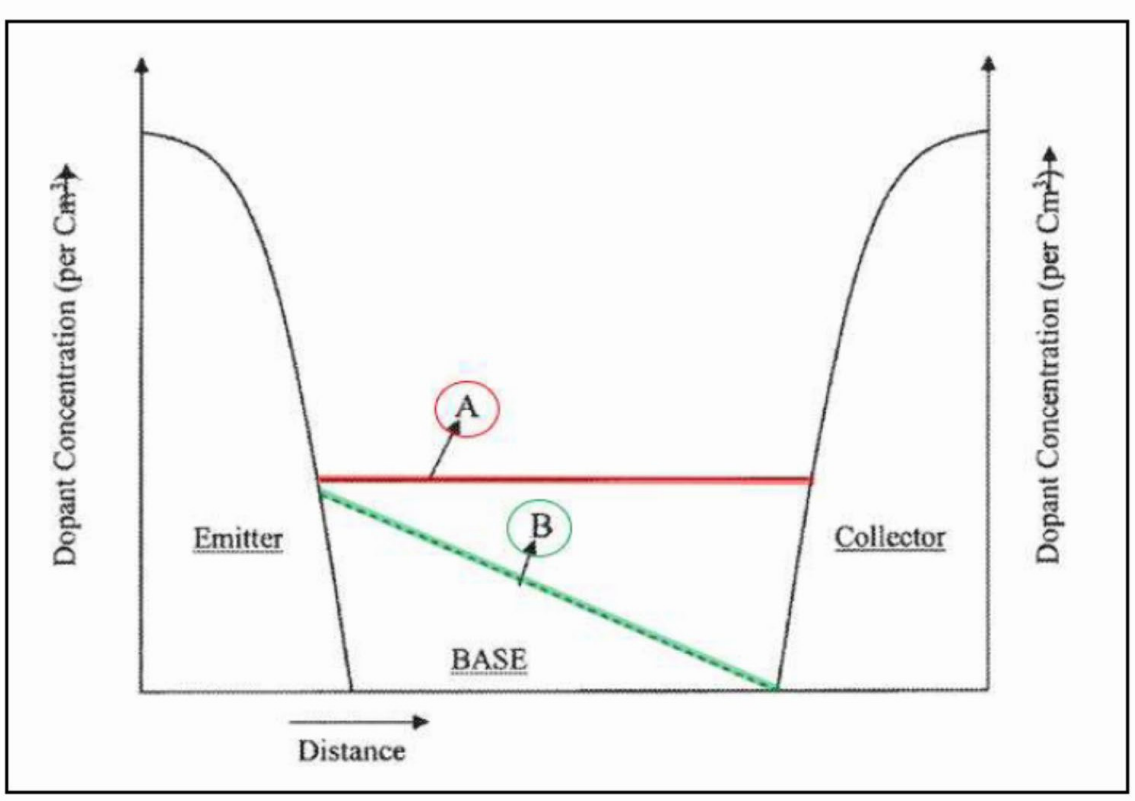
VI. THE ’481 PATENT

The ’481 Patent is directed to “grading the dopant concentration” in certain

[2] Petitioner is relying on independent librarian expert, Dr. Sylvia Hall-Ellis, to verify the public availability of Wolf.

regions of a semiconductor device. Ex.1001, Abstract. The Challenged Claims specifically recite an "active region" and a "well region" of a semiconductor device, and that each of those regions have a "graded dopant concentration to aid carrier movement." *Id*., Cl. 1.

The '481 Patent admits that graded dopant concentrations were known. For example, the graded dopant concentration "B" (green) in Figure 1 below is described as one of "the two most popular" doping profiles used in prior art bipolar transistors, in contrast to the uniform doping profile "A" (red). Ex.1001, 2:39-42.



Ex.1001, FIG. 1 ("Prior Art").[3] The '481 Patent further admits that it was known to grade the dopant concentration in well regions of CMOS devices to affect the

[3] All colors and colored annotations to figures added.

movement of carriers, but alleges, without support, that prior attempts demonstrated "little success" in "improv[ing] soft error immunity in SRAMs and visual quality in imaging circuits." *Id*., 2:18-32.

The entire description of graded dopant concentrations and purported carrier movement in CMOS devices is confined to two short paragraphs and associated Figures 5A-5C. Ex.1001, 3:48-4:30, FIGS. 5A-5C.

These paragraphs provide no guidance on how to grade a dopant concentration to "aid" carrier movement or the nature of such "aiding." The specification uses "graded" dopant broadly to describe a non-uniform dopant concentration. *Id.* at 4:15-18. The specification also does not describe grading in an active region of a CMOS device to move carriers to the substrate as claimed. Ex.1001, Cl. 1. Instead, the specification only discusses grading the channel region of an active region "to accelerate majority carriers towards the drain." Ex.1001, 4:9-11. The Challenged Claims issued without any rejection, and none of the prior art relied on in this Petition was cited or considered. In the Notice of Allowance, the Examiner stated that the claimed "aiding of carrier movement [] 'from the first surface to the second surface of the substrate'... [was] known in the art." Ex.1002, 81-83. According to the Examiner, the claims issued over the "closest reference" (Hong) because Hong does not disclose "active" regions within which transistors can be formed. *Id*.

VII. PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art ("POSITA") of the subject matter of the '481 Patent would have had a Bachelor's degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. Ex.1003, ¶¶44-47. Additional education might compensate for a deficiency in experience, and vice-versa. *Id*. In the Intel Litigation, Patent Owner ("PO") agreed with this POSITA characterization. Ex.1039, ¶13.

VIII. CLAIM CONSTRUCTION

Claims in an IPR are construed under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. §42.100(b). Petitioner is aware that PO took positions on the meaning of certain claim terms, listed below. *See* Exs. 1017, 1020.[4]

Claim Term	Patent Owner's Proposed Construction
"substrate"	Plain and ordinary meaning ("an underlying layer")
"active region"	Plain and ordinary meaning ("a doped silicon region at the surface of a semiconductor device where a transistor can be formed")

[4] For the "active region" and "well region" terms, PO's position is reflected in its claim construction briefing. *See* Ex. 1020, 28, 39-40.

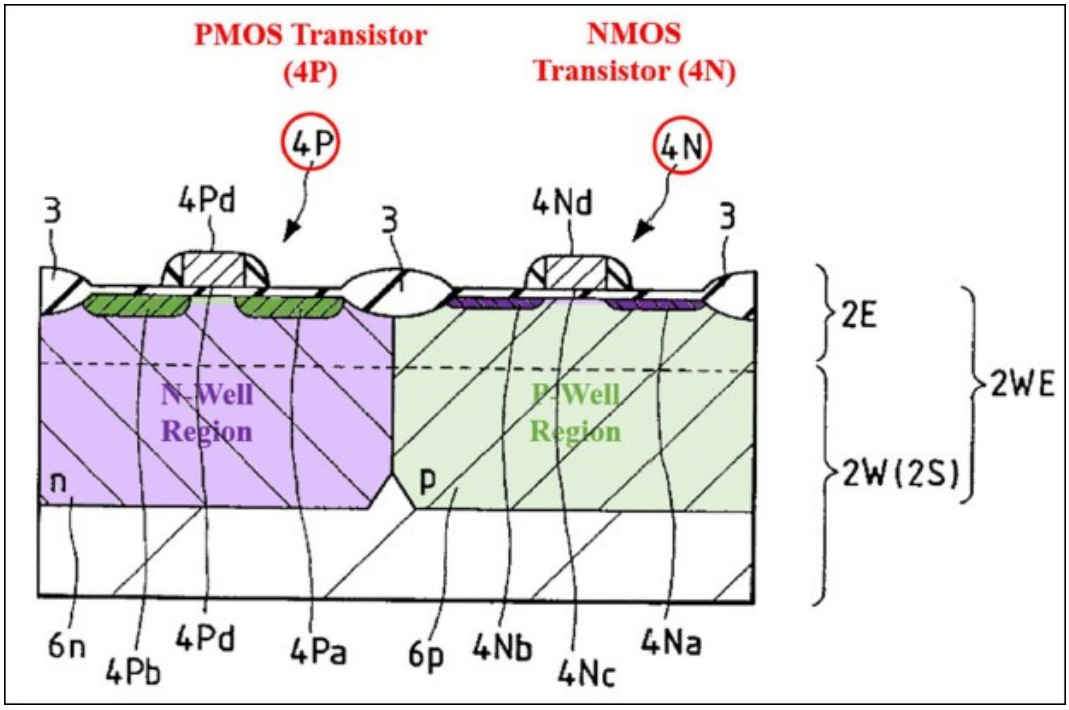
Claim Term	Patent Owner's Proposed Construction
"to aid carrier movement from … [to/towards] …"	Plain and ordinary meaning
"well region"	Plain and ordinary meaning ("a doped region that surrounds the active region of a semiconductor device")
"active region … within which transistors can be formed	Plain and ordinary meaning ("a doped silicon region at the surface of a semiconductor device where a transistor can be formed")

Petitioner is further aware that, in the Intel Litigation, the Court provided its "preliminary constructions" in advance of the claim construction hearing, in which the Court offered a "preliminary construction" of plain and ordinary meaning as to each of the above-listed terms. *See* Ex.1038. Petitioner does not believe any terms need be construed to resolve this Petition, and Petitioner takes no position regarding claim construction at this time. The Challenged Claims are unpatentable under either their plain and ordinary meaning, or under PO's proposed constructions (except for the term "active region ... within which transistors can be formed," addressed further below). Ex.1003 ¶51.

IX. OVERVIEW OF THE PRIOR ART

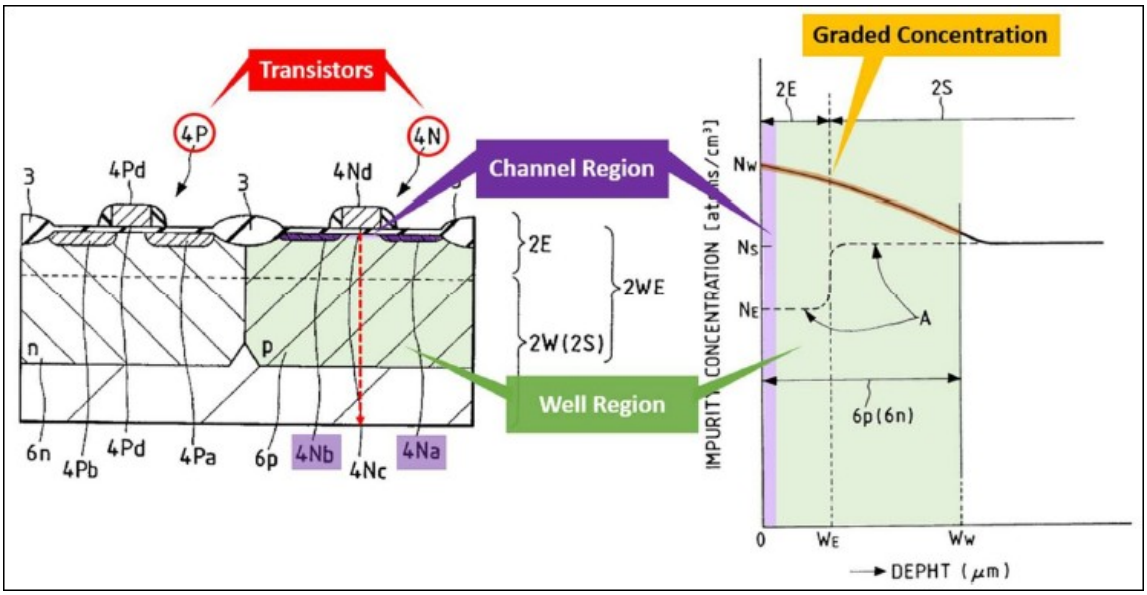
A. Kawagoe

Kawagoe describes CMOS devices fabricated using twin-well CMOS technology and an epitaxial substrate, whereby the epitaxial layer can be doped at the same or lower level than the substrate body. Ex.1007, 3:32-38, 6:65- 7:3, 8:40-53, 15:13-17, 15:26-40. Kawagoe's figure below depicts a twin-well CMOS structure. Ex.1007, 15:26-40, 18:18-23.



Id., FIG. 23. Kawagoe further teaches that the well regions have a graded dopant concentration that decreases with depth, as illustrated in Figure 17 (corresponding to Figure 23).

Id., 14:46¬55, 15:62-16:40 ("p-well 6p and n-well 6n have their impurity concentrations gradually lowered in the depthwise direction ...").[5]

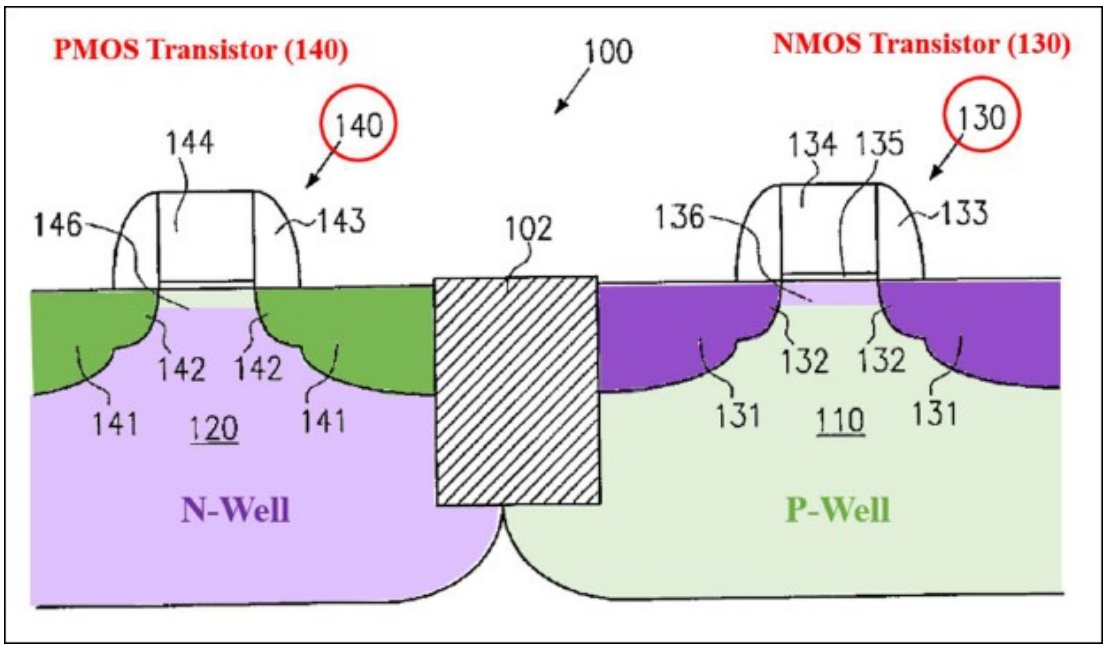


Id., FIGS. 17, 23. The graded dopant concentration reduces soft errors by sweeping unwanted carriers into the substrate body. Id., 16:2-11 ("electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient...so that the soft errors can be reduced.").

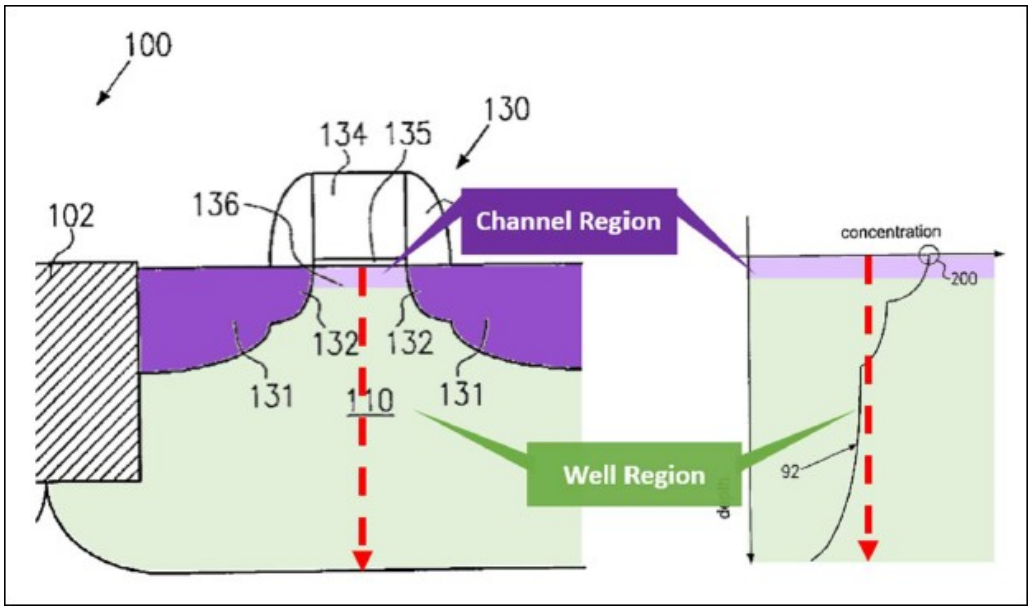
B. Wieczorek

Wieczorek describes conventional prior art CMOS devices, such as the twin- well CMOS device in Figure 1b. Ex.1006, [0007], [0012], [0020]-[0021].

[5] All emphases added unless otherwise noted.



Id., FIG. 1b. Wieczorek explains that graded dopant concentrations in prior art CMOS devices peak at the surface of the substrate and decrease with depth, as shown below. *Id*., [0004], [0007]-[0013].



Id., FIGS. 1b, 2b.

C. Wolf

Wolf is a four-volume textbook directed to semiconductor devices, with

particular focus on CMOS devices. Exs. 1008A-D.

D. Gupta

Gupta is directed to circuit layout of CMOS devices. Ex.1014. 1:7-10. As Gupta explains, "[c]onservation of semiconductor area is a primary goal in semiconductor chip development" and a common technique to conserve area is "by placing transistors so as to share diffusion area." *Id*., 1:32-54, 2:17-21.

E. Silverbrook

Silverbrook discloses "An Integrated Camera Circuit included Sensor and Drive Transistors." Ex. 1042, 1:8-11. Silverbrook discloses that the camera system could include "a processing unit for controlling the operation of the camera system; a program ROM utilized by the processing unit; a CMOS active pixel image sensor for sensing the image; [and] a memory store for storing images and associated program data[.]" *Id*., 2:10-26. Silverbrook reflects the common knowledge of a POSITA at the time that CMOS techniques and devices can be applied to image sensors.

X. SPECIFIC GROUNDS FOR PETITION

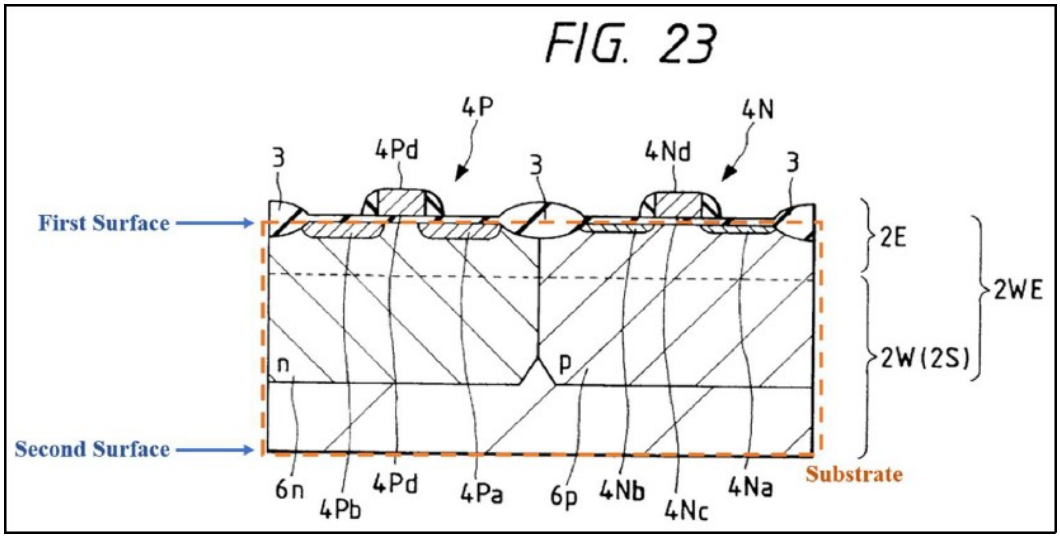
A. Ground I:

Kawagoe renders claims 1-9, 12-14, 16-27, and 30-36 obvious. Ex.1003, ¶¶63-141.

1. Independent Claim 1[6]

a) Preamble

Kawagoe discloses a "semiconductor integrated circuit device" and process for making the same. Ex.1007, Title, 1:13-23, 14:46-67, FIGS. 16-17, 23. Ground I primarily focuses on the twin-well CMOS device in Figure 23 (Embodiment 4), fabricated on a uniformly-doped epitaxial substrate taught in Embodiment 1.[7] *See* X.A.1.b.



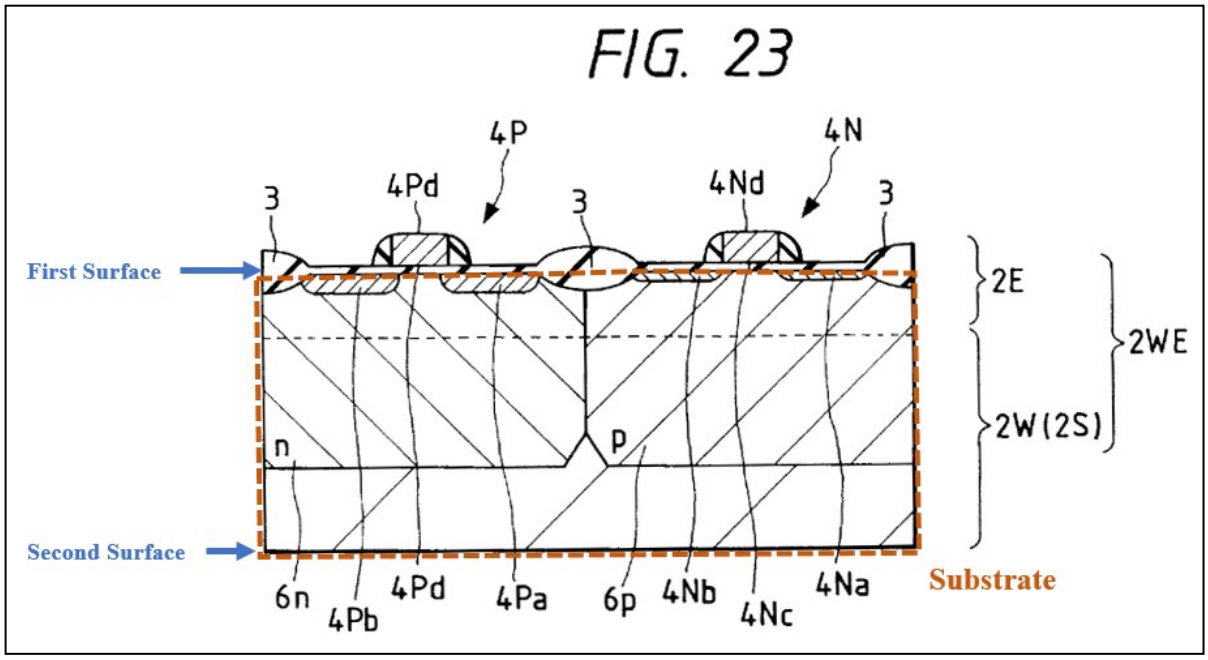
Ex.1007, FIG 23.

[6] Appendix A lists the elements and corresponding language for all Challenged Claims.

[7] Figures 16-17 and 23 are directed to Kawagoe's Embodiment 4. Ex. 1007, 14:46-60. Figure 23 shows the same twin-well CMOS structures depicted in Figure 16 without the metal layers (not recited in the Challenged Claims). Ex. 1007, 17:10-18:38; Ex. 1003, ¶64.

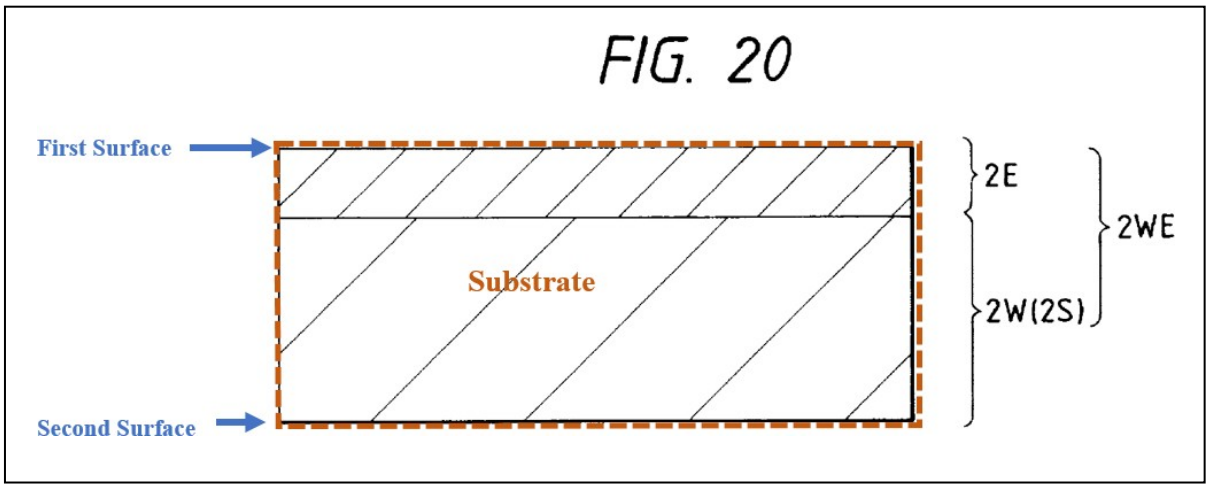
b) Element[1.1]

Kawagoe discloses a substrate ("semiconductor substrate 2") of a first doping type (***p-type***) having a silicon "epitaxial layer 2E [] doped with a p-type impurity such as boron" formed over non-epitaxial "semiconductor substrate body 2S [also] doped with a p-type impurity such as boron. " Ex.1007, 14:61-15:12, 6:50-7:3. The substrate (orange) has top ("first surface") and bottom ("second surface") surfaces, as indicated below. Ex.1003, ¶65.



Ex.1007, FIG. 23.

Kawagoe satisfies element[1.1] under PO's plain meaning construction. Section VIII; Ex.1007, 6:50-56, 14:61-67, 17:10-18:38; Ex.1003, ¶66.



Ex.1007, FIG. 20. Ground I relies on a uniformly-doped epitaxial substrate in which silicon epitaxial layer 2E of the substrate is doped at the same level as silicon substrate body 2S, so that the entire substrate in Figure 20 is "at a first doping level." Ex.1007, 6:60-7:3; Ex.1003, ¶67.

"at a first doping level" - Kawagoe teaches an epitaxial substrate (2S+2E), illustrated in Figure 20, in which the non-epitaxial silicon substrate body (2S) is either doped at the same or higher level compared to the epitaxial silicon layer (2E). For example, Embodiment 1 describes a uniformly-doped epitaxial substrate in which the "epitaxial layer 2E is doped...in a concentration ***equal*** to the [concentration] of the semiconductor substrate body 2S, e.g., $1.3x10^{15}$ atoms/cm^3." Ex.1007, 6:60-7:3; *id.*, Abstract (describing "an epitaxial layer which contains an impurity of the ***same*** conduction type [and at] ... the ***same concentration***" as the bulk substrate), 2:57-3:9 (same). This uniformly-doped epitaxial substrate is Kawagoe's benchmark substrate discussed in other embodiments, including

Embodiment 4. Ex.1007, 12:64-65, 13:12-15, 13:66-67, 14:18-20, 15:7-25.

Embodiment 4 introduces the option of a latchup-resistant substrate in which "the impurity concentration of the semiconductor substrate body 2S is made ***higher*** than that of the epitaxial layer 2E ... ***to improve*** the resistance to the latchup." Ex.1007, 15:13-17; *see also id.*, 3:60-63 (there is a high "degree of freedom for setting the impurity concentration" in the disclosed semiconductor substrate so "as to facilitate the control of the formation"). Kawagoe teaches that the "substrate body 2S is doped with a p-type impurity such as boron at a concentration of about 1.5 x 10^{15} atoms/cm^3." *Id.*, 14:64-67; Ex.1003, ¶69.

"[A] POSITA would have understood that Kawagoe teaches forming Figure 23's twin-well CMOS device (Embodiment 4) on either a uniformly-doped epitaxial substrate described in Embodiment 1 or the optional latchup-resistant substrate described in Embodiment 4." Ex.1003, ¶70. Specifically, a POSITA would have appreciated that Kawagoe teaches that a tradeoff between improving latchup resistance and minimizing manufacturing cost. This understanding is consistent with the teachings of Wolf. *See* Ex.1008C, 524 ("There are many trade-offs involved in the optimization of a CMOS process" including "fabrication cost[] and susceptibility to latchup."); Ex.1003, ¶70. Kawagoe emphasizes the benefits of Embodiment 1's uniformly-doped epitaxial substrate and explains that the substrate used in Embodiment 4 is formed "as in the foregoing embodiment 1 so that...the cost of the semiconductor substrate 2 is lowered to about one half."

Ex.1007, 15:7-25.

Accordingly, a POSITA would have been motivated to use a uniformly-doped epitaxial substrate (disclosed for Embodiment 1) to form Figure 23's twin-well CMOS device because this substrate provides "excellent film quality" that "drastically reduce[s] the defect densities of the gate insulating films" and "improve[s] the [device's] performance, reliability and production yield." Ex.1003, ¶71; Ex.1007, 12:8-40; id., 15:7-25. This substrate is also easier to manufacture, helping "lower the cost" of the substrate and chip. Ex.1007, 12:8-40. As a POSITA would have appreciated, Kawagoe teaches that a semiconductor substrate having an "impurity high in concentration[] is [undesirably] expensive." Id., 2:15-18. To avoid this, Kawagoe repeatedly teaches that using a less heavily-doped substrate body (as in Embodiment 1) can result in lower cost, relative to a more heavily-doped substrate body. See id., 3:38-45; 7:13-18; 12:19-24. While Embodiment 4 is disclosed as having an improved latchup resistance, this requires that the substrate body is doped at a higher concentration (1.5 x 1015 atoms/cm3) compared to the substrate body of Embodiment 1 (1.3 x 1015 atoms/cm3). See id., 6:62-64, 14:64-67.

Thus, a POSITA, opting to maximize cost savings over latch-up resistance, would have been motivated to instead use the uniformly-doped epitaxial substrate (*i.e.*, doped at both 1.3 x 10^{15} atoms/cm^3 for the substrate body and epitaxial layer, as disclosed for Embodiment 1) as the starting material in lieu of Embodiment 4's

latchup-resistant substrate to form the twin-well CMOS device of Figure 23. The use of uniformly-doped epitaxial substrate as the starting material in lieu of Embodiment 4's latchup-resistant substrate to form Figure 23's twin-well CMOS devices is a simple substitution of one known element with another known, closely-related element, both of which are described in Kawagoe. Additionally, this substitution would have been obvious to try because it merely involves choosing one of two ways of doping an epitaxial substrate, both described in Kawagoe, and both options have predictable effects on the devices formed using those substrates.[8] Ex.1003, ¶72. Twin-well CMOS devices (illustrated in Figure 23) fabricated on a uniformly-doped epitaxial substrate would have worked for their intended purpose. *Id.*, ¶73. As discussed in Wolf, twin-well CMOS devices were commonly formed over a "***uniform***, lightly doped *p*- or *n*-type substrate" that provides no improved latchup resistance. Ex.1008C, 523; *id.*, 530 ("With the twin-tub [(twin-well)] approach, two separate wells are formed for *n*- and *p*-channel transistors on a lightly doped substrate..."); Ex.1008B, 387-389; Ex.1007, 2:57-65 (discussing a uniform, "lightly doped" epitaxial substrate).

There would have been a reasonable expectation of success because

[8] *Bos. Sci. Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009) ("Combining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness.").

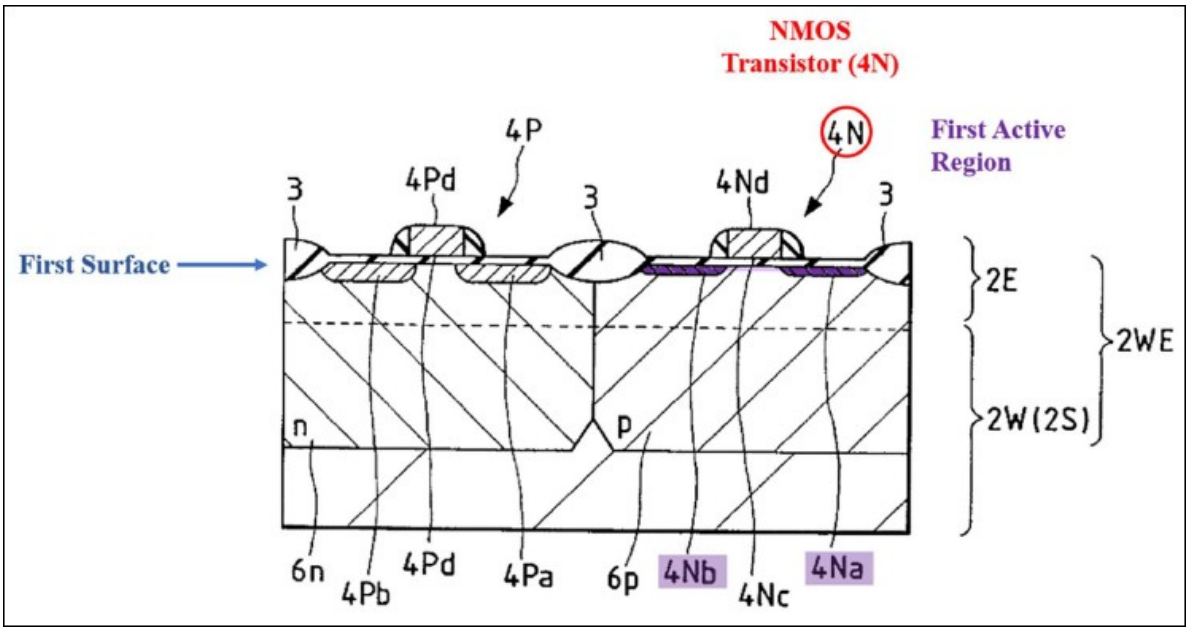
Kawagoe details the use of both uniformly-doped epitaxial substrates and latchup-resistant substrates in forming CMOS devices, and repeatedly emphasizes their similarity. Ex.1007, 8:40-52; 12:8-40, 14:58-60, 15:7-12 (substrate), 15:18-25 (epitaxial layer), 15:26-40 (transistors); Ex.1003, ¶74. A uniformly-doped epitaxial substrate is also better than the bulk (non-epitaxial) substrate commonly used to fabricate twin-well CMOS devices. Ex.1007, 1:33-40 ("The epitaxial wafer is advantageous [compared to bulk wafer/substrate] in that ... the gate insulating film to be formed over the epitaxial layer can have excellent breakdown characteristics to drastically reduce the defect density of the gate insulating film."); *id.*, 12:8-40; Ex.1008B, 387-88 (discussing twin-well CMOS devices fabricated over bulk substrate); Ex.1003, ¶74. Kawagoe characterizes the improved latchup tolerance provided by Embodiment 4's optional latchup-tolerant substrate as just another "effect[] [that] can be achieved in addition to those of the foregoing embodiment 1," Ex.1007, 19:49-63, as opposed to being vital to its operation. Consistent with Kawagoe's teachings, a POSITA would have understood that a uniformly-doped epitaxial substrate is a suitable substrate because, among other benefits, it "drastically reduce[s] the defect densities of the gate insulating films" of CMOS transistors. Ex.1007, 12:8-40; Ex.1003, ¶75. Moreover, a POSITA would have understood that susceptibility to latchup (a "short-circuit" failure condition in poorly designed circuits) may not be a concern for all CMOS chips—*see* Ex.1008B, 406 ("four conditions must exist

in a CMOS circuit in order for latchup to occur."); Ex.1026, 1 ("several conditions must be met" to cause latchup)—in which case it is unnecessary to improve latchup resistance. Ex.1003, ¶75. Indeed, both single-well and twin-well CMOS devices were commonly fabricated on uniformly-doped bulk substrates that provide no improved latchup resistance. *See, e.g.*, Ex.1008B, 387-388 ("With the [twin-well] approach, ... [t]he substrate may be [] a lightly doped wafer..."), 652 (example 6.7); Ex.1003, ¶76. Even if latchup were to remain a concern, a POSITA would have understood that improved latchup resistance can be achieved by other means unrelated to the choice of substrate, such as careful circuit layout. Ex.1003, ¶76; Ex.1008B, 381 ("Latchup tolerance can [] be improved by spacing *n*- and *p*-channel transistors farther apart"), 419 ("Increasing the number of well contacts to VDD reduces latchup susceptibility" and thus "can serve as an alternative approach to improving latchup immunity.").

c) Element[1.2]

Kawagoe discloses "semiconductor regions 4Na and 4Nb...for forming the source-drain regions of the nMOS [n-channel transistor] 4N." Ex.1007, 8:66-67; *id.*, 3:32-38, 8:45-52, 14:46-55, 15:26-40. Source-drain regions 4Na/4Nb (purple) form part of the claimed first active region, which also includes the channel region (light purple) between source-drain regions 4Na/4Nb and below insulating film 4Nc. Ex.1007, 8:46-65, 14:46-55, 15:26-40; Ex.1003, ¶77; Ex.1008B, 299-300 ("The top surface of the [substrate] body consists of active or transistor regions as

well as passive or (field) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source*** and ***drain*** regions."), FIG. 5¬2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex.1008C, 525, FIG. 8-1(e). As shown in Figure 23, nMOS transistor 4N is formed in the first active region, which is adjacent the first surface of the substrate. Ex.1003, ¶77.

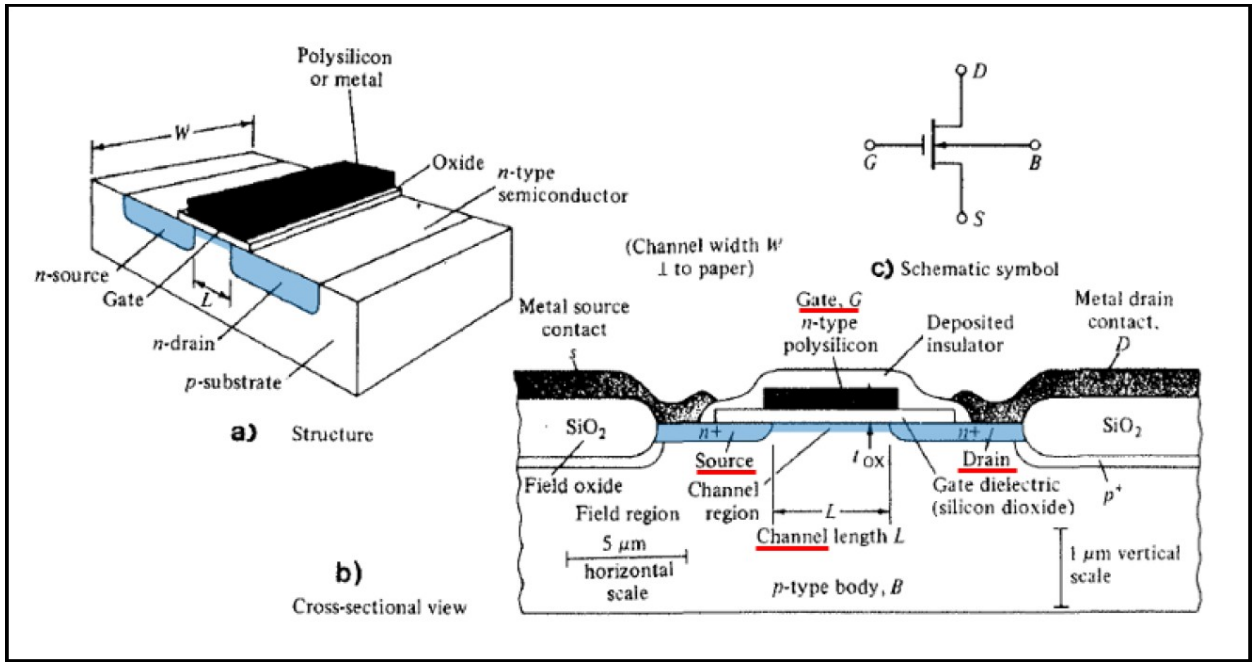


Ex.1007, FIG. 23. "[S]emiconductor regions 4Na and 4Nb are doped with an ***n-type impurity***" and thus have a second doping type (n-type) opposite in conductivity to the first doping type (p-type) of the substrate. Ex.1007, 8:67-9:3, 14:46-55, 15:26¬40; Ex.1003, ¶77.

While Figure 23 illustrates an exemplary nMOS transistor 4N in the first active region, forming multiple nMOS transistors would have been obvious as a mere duplication of parts lacking unexpected results. *See In re Harza*, 274 F.2d 669, 671 (C.C.P.A. 1960). Indeed, a POSITA would have recognized that forming

multiple transistors in Kawagoe's active region would minimize chip area, as good layout practice dictates. Ex.1003 ¶78; Ex.1014, 1:52-54, 2:17-21. Regardless, according to PO, an "active region ... within which transistors can be formed" means "an active region ... where a ***transistor*** can be formed." Ex.1020, 31.

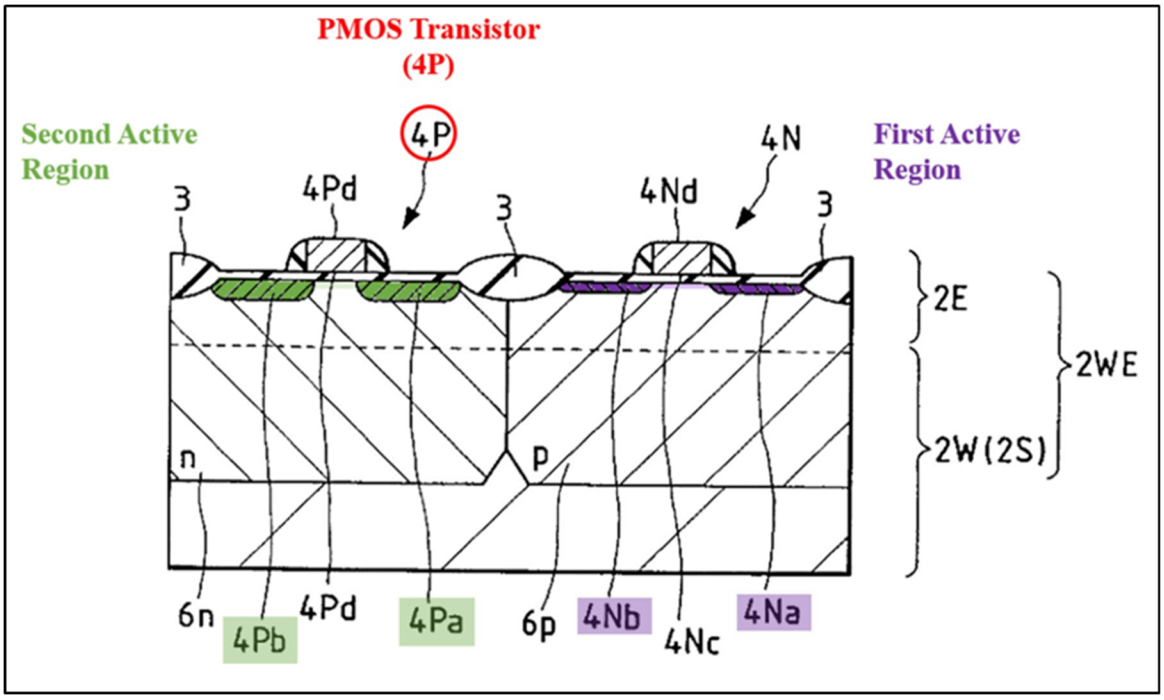
Kawagoe satisfies element[1.2] under PO's position that "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed" because, as indicated in Wolf below (in blue), the active region of a MOS transistor is "[its] channel and [its] heavily doped source and drain regions." Section VIII; Ex.1008B, 299; Ex.1003, ¶79.



Ex.1008B, FIG. 5-1; *id.*, 298-301, FIGS. 5-2, 6-4.

d) Element[1.3]

Kawagoe discloses "semiconductor regions 4Pa and 4Pb ... for forming the source-drain regions of the pMOS [p-channel transistor] 4P." Ex.1007, 3:32-38, 8:46-52, 9:41-48, 15:26-40. Source-drain regions 4Pa/4Pb (green) are part of the claimed second active region, which also includes the channel region (light green) between them and below gate 4Pd. Ex.1007, 8:46-58, 9:41-46, 14:46-55, 15:26-40; Ex.1008B, 299-301, FIGS. 5-1, 5-2, 6-4; Section X.A.1.c; Ex.1003, ¶80. As shown in Figure 23, pMOS transistor 4P is formed in the second active region (green/light green), which is separate from and disposed adjacent to the first active region (purple/light purple). Ex.1007, 14:46-55; Ex.1003, ¶80. Adjacent active regions are separated by an isolation region (e.g., insulating film 3). Ex.1008A, 818-20, FIG. 16-11(f); Ex.1003, ¶81. Indeed, claim 6 (which depends from claim 1) recites, "the first active region and second active region are each separated by at least one isolation region." Ex.1001, Cl. 6.



Ex.1007, FIG. 23.

While Figure 23 illustrates an exemplary pMOS transistor 4P formed in the second active region, a POSITA would have understood that forming multiple pMOS transistors in this region would have been obvious. Ex.1003, ¶82; Section X.A.1.c. Regardless, according to PO, an "active region ... within which transistors can be formed" means "an active region ... where a ***transistor*** can be formed." Ex.1020, 31.

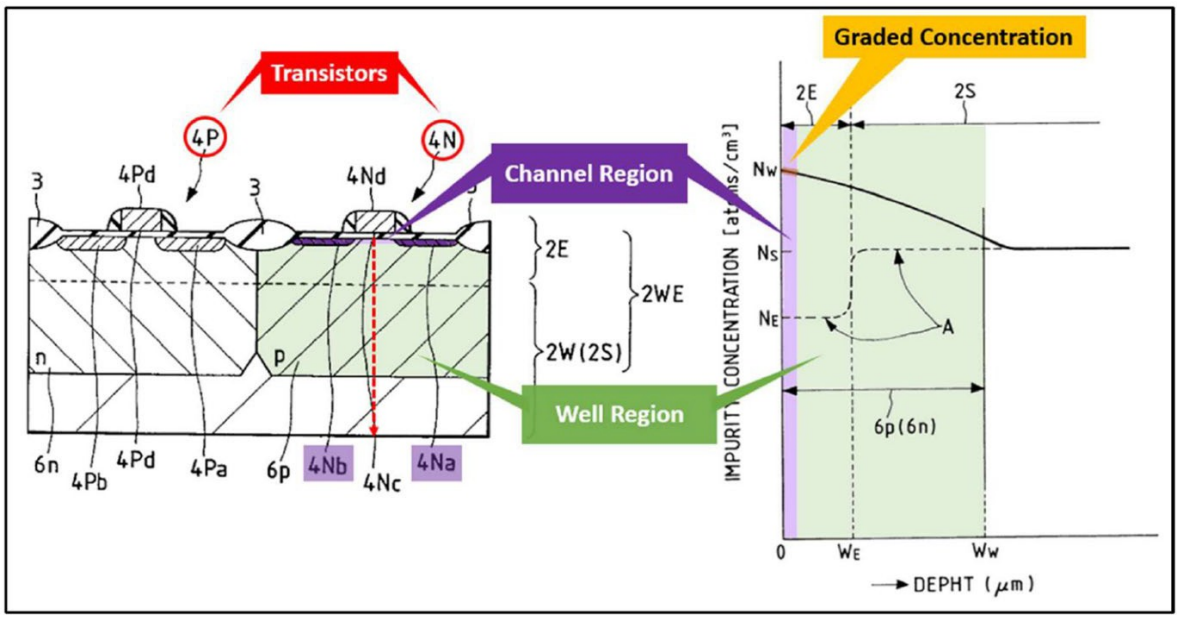
Kawagoe satisfies element[1.3] under PO's position that "active region" means "a doped silicon region at the surface of a semiconductor device (e.g., the source and drain and silicon between them) where a transistor can be formed." Ex.1003, ¶83; Section X.A.1.c.

e) Element[1.4]

Sections X.A.1.c-d.

f) Element[1.5]

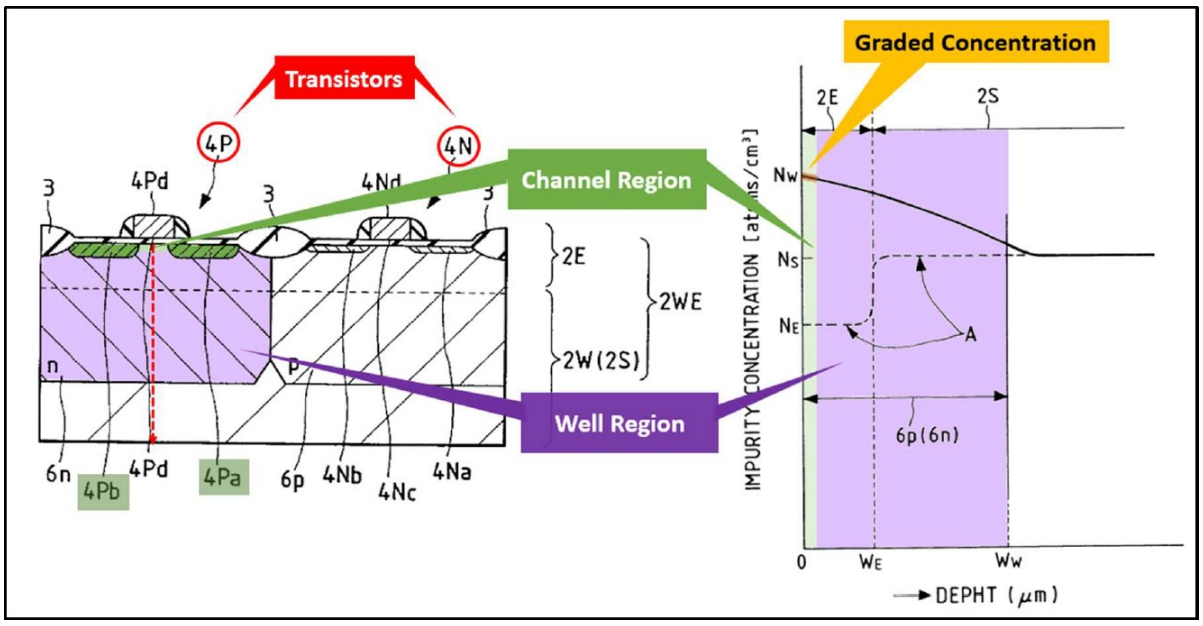
As illustrated the below annotation of Figure 23 (left), a channel region (light purple) formed at the top surface of the substrate connects source-drain regions 4Na/4Nb (purple) of transistor 4N. Ex.1008B, 298 ("A channel region in the semiconductor under the gate electrode separates the source and drain"), 300-301 ("When positive bias is applied to an NMOS transistor gate ... an *n*-type ***channel*** connects the ***source*** and ***drain*** regions"), FIG. 5-2; Ex.1007, 8:46-47 ("nMOS" is a shorthand for "n-channel MOS.FET"), 8:60-67, 14:46-55, 15:26-30, 15:37-40; Ex.1003, ¶85. PO does not dispute this. Ex.1020, 4 (the channel is "a thin layer below the surface" connecting the source and drain).



Ex.1007, FIGS. 17, 23. Kawagoe's Figure 17 (above right) illustrates the doping

concentration measured along the red dotted line in Figure 23 (above left), which starts from the top surface of the substrate (depth=0) and includes the doping profile in the channel region (light purple). *Id.*, 5:41-45. As Figure 17 shows, the dopant concentration is "gradually lowered in the depthwise direction ***from the principal surface*** (having an impurity concentration N_W) of the epitaxial layer 2E." *Id.*, 15:62- 16:40; *see also id.*, 16:21-26 (N_W is the concentration at the well surface). The dopant concentration is thus graded in the channel region of transistor 4N, which is a portion of the first active region formed at "the principal surface" (top surface) of epitaxial layer 2E. Ex.1003, ¶86. Kawagoe's graded dopant concentration is in fact downward-sloping from the top surface of the substrate and all the way through the entire depth of the channel region (light purple) and the underlying well region (green)—from depth=0 at the top surface of the epitaxial substrate to beyond depth=W_W where W_W is the depth at the bottom of the p-well 6p. Ex. 1007, 15:32-While Figure 17 depicts the dopant concentration sloping at such a degree so as to level off at the at N_S (the dopant concentration of the substrate body) beyond the depth W_W, a POSITA would have appreciated that when the device of Figure 23 is implemented using a uniformly-doped substrate as in Embodiment 1, in which the doping levels of the epitaxial layer (N_E) and substrate body (N_S) are equal, the downward slope through the p-well 6p would have the same general profile but steeper than as depicted in Figure 17 above. Ex. 1003, ¶86.

The same applies to the channel region of pMOS transistor 4P (a portion of the second active region), as illustrated below. Ex.1007, 15:62-16:2 ("p-well 6*p* and n-well 6n have their impurity concentrations gradually lowered in the depthwise direction from the principal surface [] of the epitaxial layer 2E."), 9:41-48, 14:46¬55, 15:32, 15:37-40; Ex.1008B, 298-301, FIGS. 5-2, 6-4. As with the Nmos transistor, when the device of Figure 23 is implemented using a uniformly-doped substrate as in Embodiment 1, the downward slope through the n-well 6n would have the same general profile but steeper than as depicted in Figure 17 above. Ex.1003, ¶87.



Ex.1007, FIGS. 17, 23. Thus, Kawagoe discloses "at least a portion of" the first and second active regions (the channel regions) having a downward-sloping graded dopant concentration. Ex.1003, ¶¶86-87.

Kawagoe further explains that such downward-sloping graded dopant

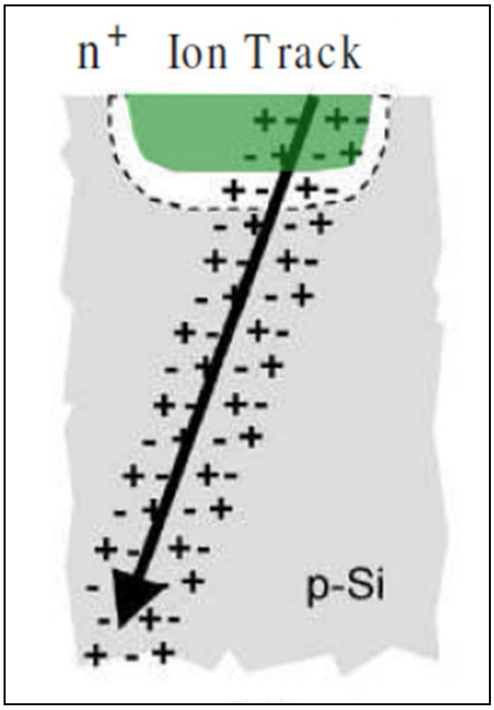
concentration aids the movement of carriers from the top surface of the epitaxial layer (claimed "first surface") to the bottom surface of the substrate (claimed "second surface"):

> [T]he impurity concentration of the p-well 6p is given such a gradient that it is ***gradually lowered in the depthwise direction*** from the surface of the epitaxial layer 2E, so that the influence to be caused by the carriers (or electrons) due to the α-ray is lowered. Specifically, the ***electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient*** [] so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6*p*.

Ex.1007, 16:2-11.[9]

Dr. Banerjee explains that "during a so-called single event upset (SEU), an α- ray generates millions of carriers, some of which are produced in or near the active region at the top surface of the substrate," as illustrated below. Ex.1003, ¶89; Ex.1009, 431 ("A[n] [α-]particle can induce SEU when it strikes at the ***channel region*** of an off NMOS transistor or the ***drain region*** [(green)] of an off PMOS transistor.").

[9] Kawagoe also states that "electrons produced by the α-ray [are]... prevented from entering the p-well 6p....." Ex. 1007, 16:7-9. This refers to electrons created by an α-ray in the substrate body below the wells, by far the largest volumetric region of any chip. Ex. 1003, ¶88; Ex. 1009, FIG. 2.



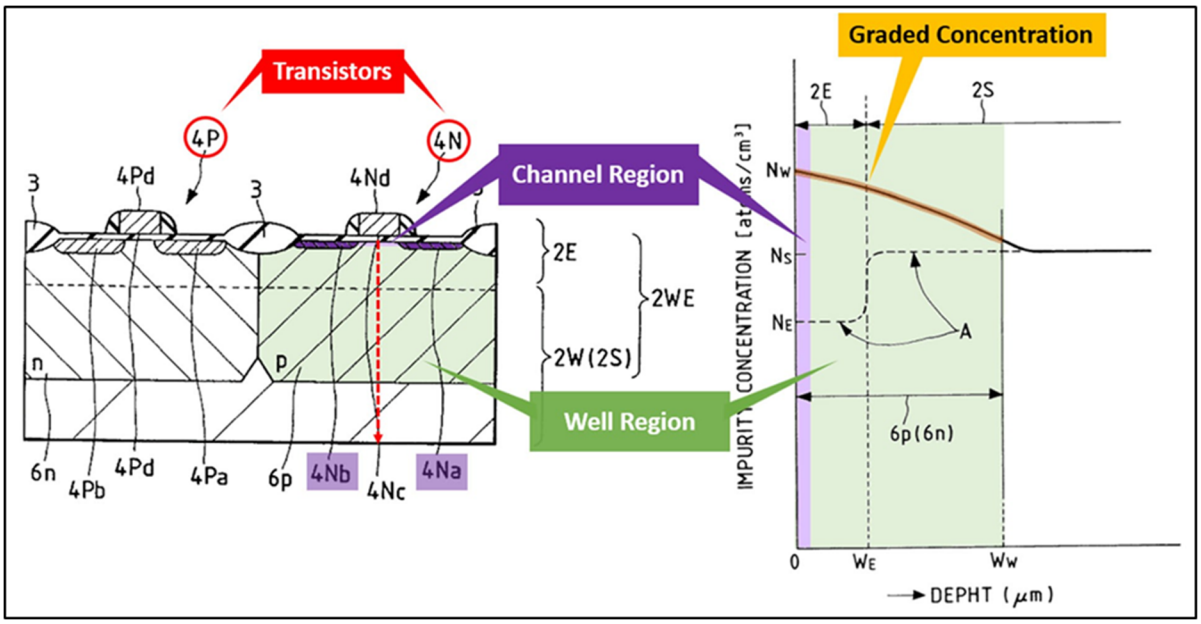
Ex.1009, FIG. 2. Kawagoe teaches that those carriers are "attracted to the substrate body by [the] concentration gradient" of the graded dopant concentration illustrated in Figure 17. Ex.1007, 16:2-11.

Accordingly, Kawagoe satisfies element[1.5] under PO's plain meaning construction of the "to aid carrier movement" term. Section VIII; Ex.1003, ¶90. According to PO, the claims make clear that "carriers [must move] in a particular direction (from the surface layer to the substrate)" and "[w]hen the dopant concentration is graded in a particular direction, [certain] charge carriers will move in the [same] gradient direction ...." Ex.1020, 2, 29. Here, Kawagoe's Figure 17 shows that the dopant concentration is downward-sloping with increasing depth towards the bottom of the substrate, and thus, according to PO, this graded dopant concentration causes carriers to move deeper into the substrate as well. Ex.1003 90.

Notably, Applicant represented to the Patent Office during prosecution of the parent '195 Patent that a downward-sloping graded dopant concentration was known to create an "inherent 'built-in' unidirectional electric field" that sweeps carriers down into the substrate. *See* Section X.A.1.g. Ex.1016, 289-290; Ex.1003, ¶91.

g) Element[1.6]

As shown in Figure 23 (below left), Kawagoe discloses "p-well 6p" (light green) adjacent to the first active region (purple/light purple). Ex.1007, 8:66-67, 14:46-55, 15:26-40; Ex.1003, ¶92. And, as discussed above and as shown in the dopant concentration profile (brown) of Figure 17 (below right), the dopant concentration in p-well 6p—measured along the exemplary red dotted line in Figure 23—gradually decreases with depth. Section X.A.1.f; Ex.1007, 14:46-55, 15:62- 16:40 ("p-well 6p and n-well 6n have their impurity concentrations ***gradually lowered*** in the depthwise direction from the principal surface (having an impurity concentration N_W) of the epitaxial layer 2E"), 16:11-15. Thus, Kawagoe discloses a well region containing at least one graded dopant region (e.g., the region highlighted in light green in both Figures 23 and 17) having a downward-sloping graded dopant concentration. Ex.1003, ¶93.



Ex.1007, FIGS. 17, 23.

Kawagoe further explains that this downward-sloping graded dopant concentration aids carrier movement from the top surface of the epitaxial layer (claimed "first surface") to the bottom surface of the substrate (claimed "second surface"). *Id*., 16:2-11. Kawagoe's teaching is consistent with Applicant's representation to the Patent Office during prosecution of the parent '195 Patent that a downward-sloping graded dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that moves carriers deep into the substrate (while an upward-sloping concentration, not at issue in Kawagoe, would move carriers in the opposite direction towards the surface):

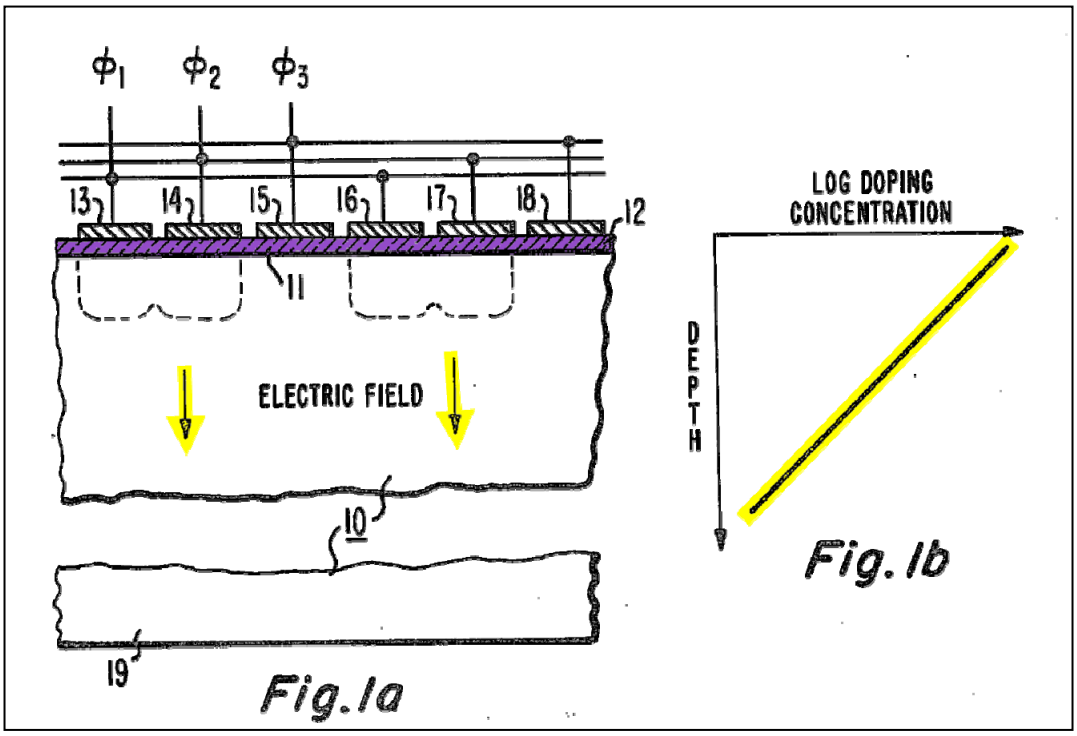
> [T]he graded dopant concentration itself creates a '***built- in' electrical field*** that forces the movement of carriers into a particular direction, whereby ***the 'direction' of the electrical field and the resulting direction of the carrier***

> ***movement depends solely on the slope of the graded concentration of dopant***.

Ex.1016, 289-290 (underlining in original, addressing amended claim 10 (*id.*, 286)); Ex.1003, ¶95. Applicant also represented that "a unidirectional drift (electric) field necessarily affects ***all*** the present minority carriers in the same way Depending on

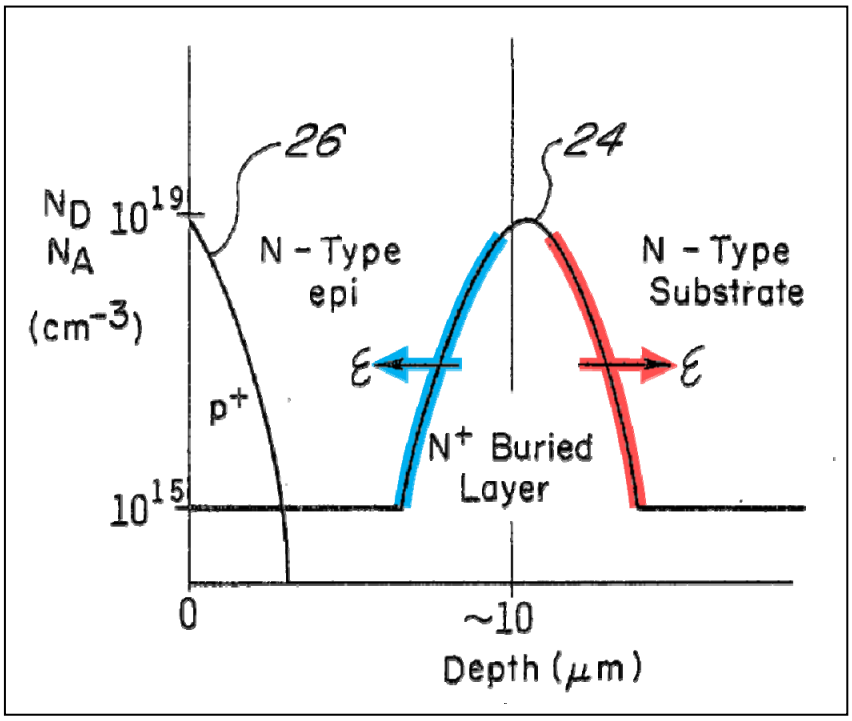
the particular slope of the graded concentration of dopant, ***all*** minority carriers are either swept 'down' ... or 'up.'" Ex.1016, 289.

Applicant cited Jastrzebski in support. *Id.*, 290. In Jastrzebski, the doping concentration is "decreasing with depth" from the top surface 11 (purple) of the substrate 10, as shown in Figure 1b below. Ex.1010, 5:14-22. Jastrzebski teaches that this downward-sloping graded dopant concentration creates an electric drift field that "force[s] most of the charge carriers .. ***deep into the substrate***[.]" *Id*., 2:27-32, 5:14-22.



Id., FIGS. 1a-1b.

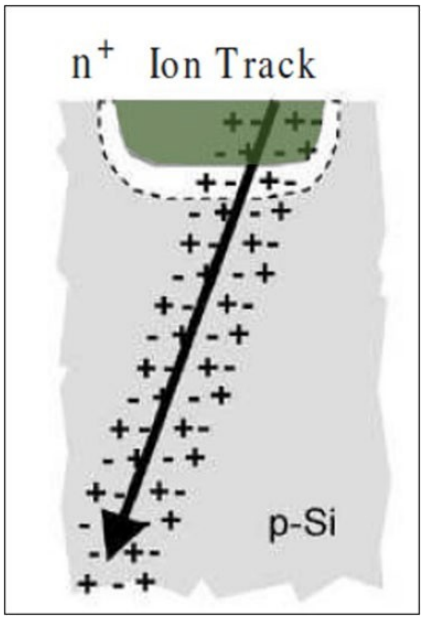
Applicant made the same representation to the Patent Office regarding Kamins. Ex.1016, 237-238. According to Applicant, Kamins' Figure 3 shows "two electric fields with opposing directions" (highlighted in blue and red) that correspond to increasing and decreasing graded dopant concentrations, respectively. *Id.*, 237 (citing Ex.1031, 3:6-13). Applicant explained that the electric field associated with the downward-sloping graded concentration at depth beyond ~10μm (red) causes "carriers created [in that region to be] .. ***accelerated into the substrate*** ..." *Id.* (citing Ex.1031, 3:6-13, FIGS. 2-3).



Ex.1031, FIG. 3.

Accordingly, Kawagoe satisfies element[1.6] under PO's construction that "well region" means "a doped region that surrounds the active region of a semiconductor device." Ex.1020, 30; *see also* Section VIII; Ex.1003, ¶98. As shown in Figure 23 above, p-well 6p (light green) is a doped region that surrounds the first active region (purple/light purple). Ex.1003, ¶98. Kawagoe also satisfies element[1.6] under PO's plain meaning construction of the "to aid carrier movement" term. Section VIII; Ex.1003 ¶98.

Further, as discussed in Wang and as was well understood in the art, an α-ray generates a stream of millions of carriers (electrons) that can cause single-event upset (SEU) soft errors. Ex.1009, 431; Section X.A.1.f; Ex.1003, ¶99.



Ex.1009, FIG. 2. Kawagoe explains that the graded dopant concentration illustrated in Figure 17 reduces soft errors by sweeping those carriers to the second surface of the substrate. Ex.1007, 16:2-11; Ex.1003, ¶100.

2. Claim 2

Section X.A.1.b.

3. Claim 3

Section X.A.1.b.

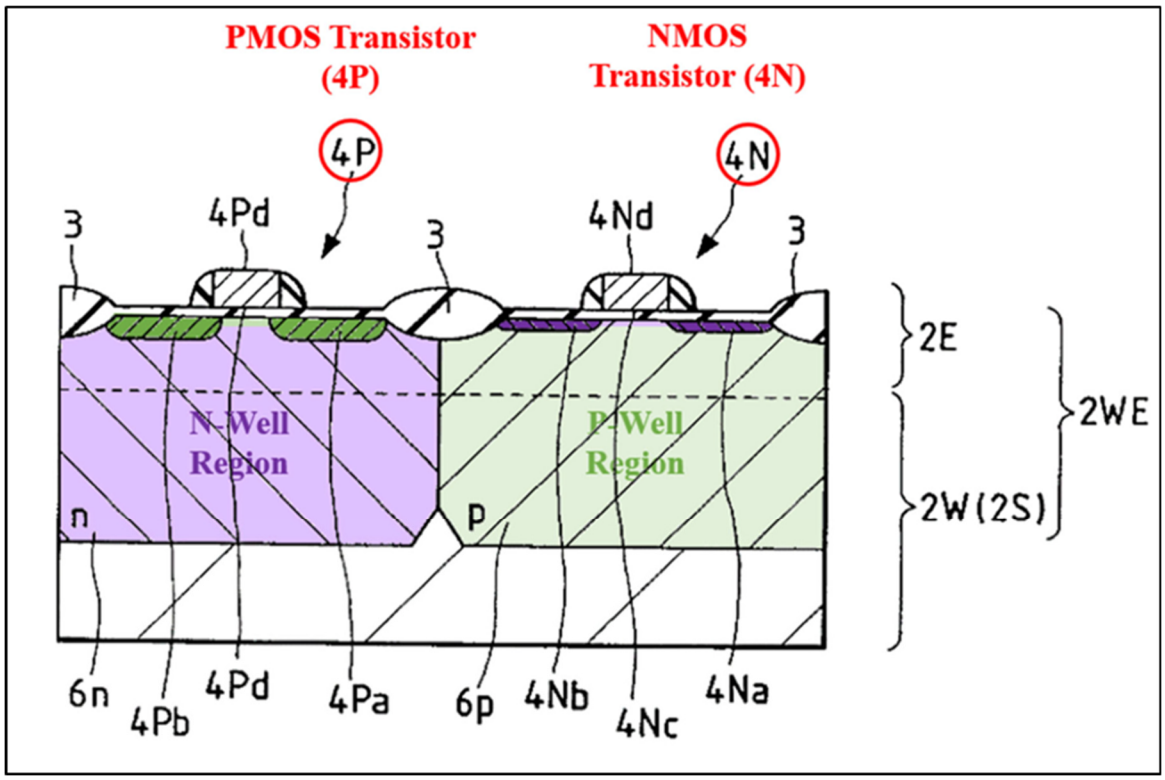
4. Claim 4

Sections X.A.1.c-e.

5. Claim 5

Kawagoe's Figure 23 illustrates conventional twin-well architecture,

whereby the first active region contains nMOS (n-channel) transistor 4N formed in p-well 6p, and the second active region contains pMOS (p-channel) transistor 4P formed in n-well 6n. Ex.1007, 8:46-52, 14:46-55, 15:26-43; Sections X.A.1.c-d; Ex.1008B, 387-88; Ex.1003, ¶104. This mapping satisfies this claim under PO's interpretation that a claimed active region can contain "a ***transistor***." Ex.1020, 31; Ex.1003, ¶105. A POSITA would have also understood that Kawagoe teaches forming multiple transistors in an active region to save chip area. Ex.1003, ¶105.

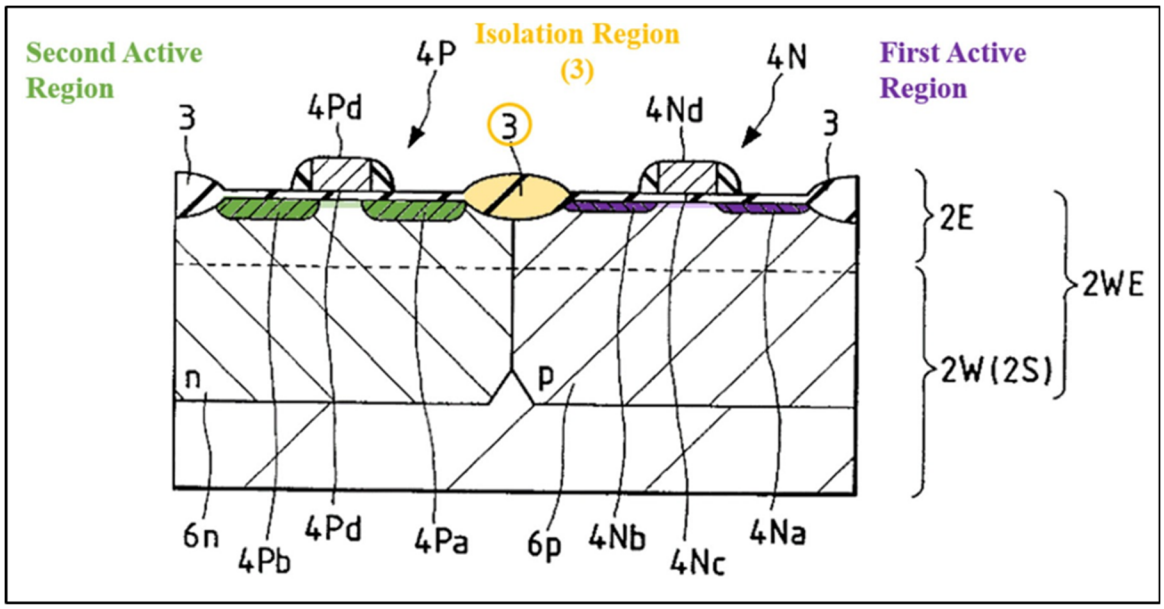


Ex.1007, FIG. 23. Further, Kawagoe's n-wells and p-wells have graded dopants. *Id.*, 14:46-55, 15:62-16:2 ("as shown in FIGS. 16 and 17, ...the p-well 6p and n-well 6n have their impurity concentrations ***gradually lowered*** in the depthwise direction from the principal surface (having an impurity concentration N_W) of the

epitaxial layer 2E."); Section X.A.1.g (discussing graded dopants in p-well 6p); Ex.1003, ¶106.

6. Claim 6

As shown below, the first (purple/light purple) and second active regions (green/light green) are separated by "field insulating film 3" (claimed "isolation region") (yellow). Ex.1007, 8:40-52, 15:37-40, 17:62-18:8; Ex.1008A, 818-20, FIG. 16-11(f); Ex.1003, ¶107.



Ex.1007, FIG. 23.

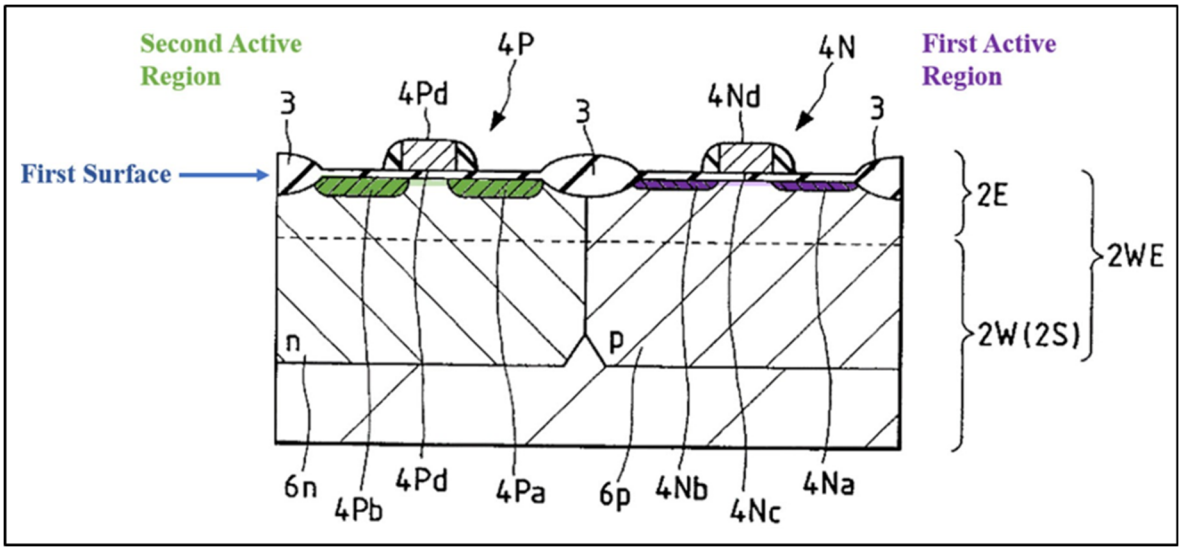
7. Claim 7

Kawagoe discloses that the graded dopants in n-well 6n and p-well 6p are "formed by the ion implantation method." Ex.1007, 4:11-12, 15:26-36, 17:10-12, 17:31-39 (n-well 6n formed by implanting "ions of an n-type impurity"), 17:43-49 (p-well 6p formed by implanting ions of "a p-type impurity"); Sections X.A.1.f-g;

Ex.1003, ¶108.

8. Claim 8

As shown in Figure 23 below, Kawagoe discloses that the first (purple/light purple) and second (green/light green) active regions are formed adjacent the first surface of the substrate (blue). Ex.1007, 8:66-9:6, 9:47-54, 15:37-40, 17:10-12, 17:31-18:35; Ex.1003, ¶109; Ex.1008B, 299 ("The top surface of the [substrate] body consists of active or transistor regions...."), 298, 300-301, FIG. 5-2; Sections X.A.1.c-d.

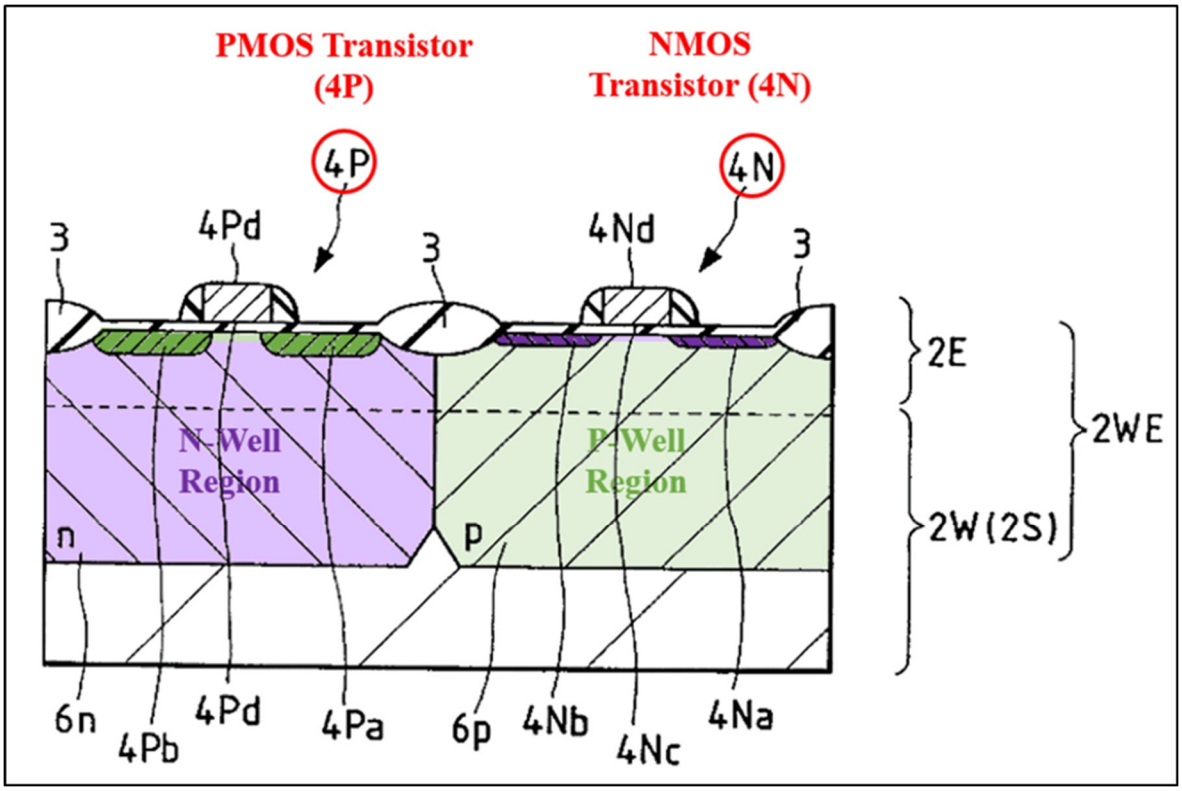


Ex.1007, FIG. 23.

9. Claim 9

As shown in the below Figure 23 annotation, the channel region (light purple) of the first active region—between source-drain regions 4Na/4Nb and below insulating film 4Nc—formed at the top of p-well 6p is of the same doping type (p- type) as p-well 6p. Ex.1007, 15:26-36 ("The p-well 6p is doped with a p-

type impurity"); *id*., 17:10-12, 17:43-49; Ex.1003, ¶110. Likewise, the channel region (light green) of the second active region—between source-drain regions 4Pa/4Pb and below insulating film 4Pc—formed at the top of n-well 6n is of the same doping type (n-type) as n-well 6n. Ex.1007, 15:26-36 ("n-well 6n is doped with an n-type impurity"), 17:10-12, 17:33-39; Ex.1003, ¶111.



Ex.1007, FIG. 23. Those channel regions have graded dopant concentrations, as discussed above. Section X.A.1.f; Ex.1003, ¶112.

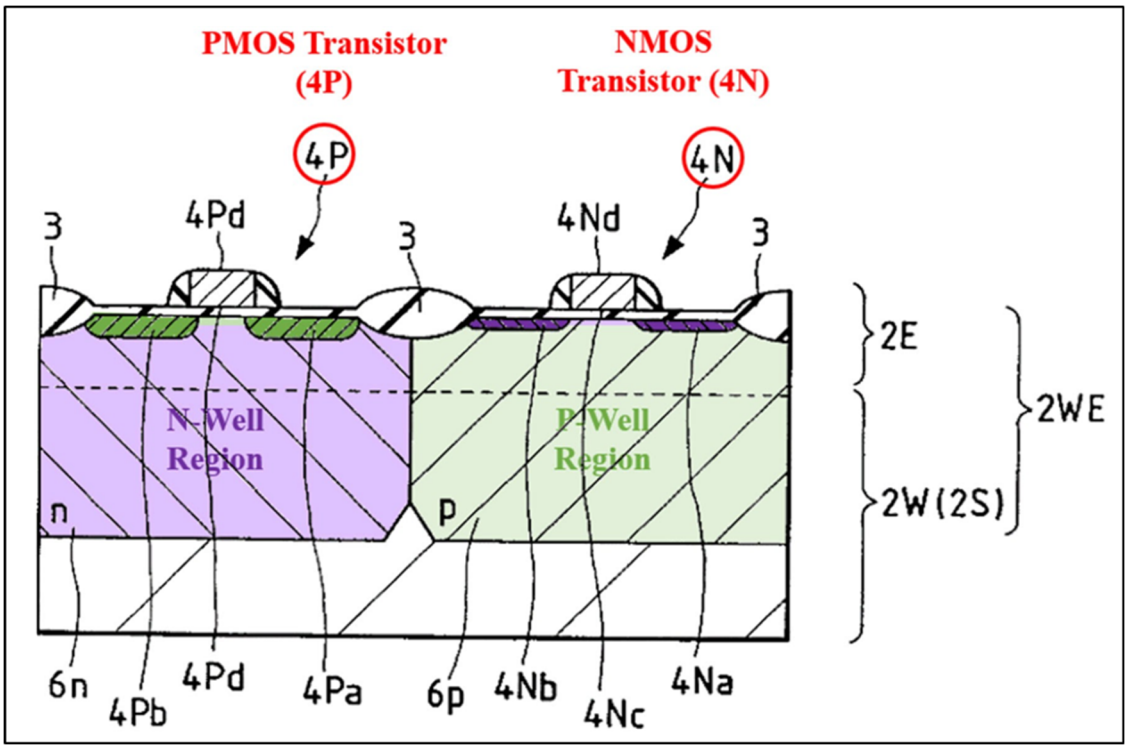
10.Claim 12

See Sections X.A.1.f-g (elements[1.5]-[1.6]). Kawagoe's Figure 23 includes "n-well 6n…doped with an n-type impurity" (Ex.1007, 15:31-36) that is formed

into a substrate "doped with a p-type impurity." *Id.*, 15:1-12; 6:60-7:18; 9:32-40. Because the implantation of n-type impurity does not remove the substrate's p-type dopants, n-well 6n includes "both p-type and n-type" dopants. Ex.1003, ¶113.

11. Claim 13

Kawagoe teaches nMOS transistor 4N formed in the first active region and pMOS transistor 4P formed in the second active region, which are CMOS transistors. Ex.1007, 8:45-52, 14:46-55, 15:37-40; Ex.1003, ¶114.



Ex.1007, FIG. 23. Each of the CMOS transistors includes a source, drain, gate, and channel. Ex.1003, ¶114. The nMOS transistor 4N includes "source-drain regions" 4Na/4Nb spaced apart by an "n-channel" region, and gate electrode 4Nd, and pMOS transistor 4P includes "source-drain regions" 4Pa/4Pb spaced apart by a

"p-channel" region, and gate electrode 4Pd. Ex.1007, 8:42-67, 9:41-48, 14:46-55, 15:37-40, FIG. 23; Ex.1003, ¶114; Sections X.A.1.c-d, X.A.1.f.

12.Claim 14

Kawagoe explains that "embodiment 4" (Figures 16-17, 20-24), relied upon for claim 1, can be advantageously used to fabricate DRAM devices with reduced soft errors, reduced defect density, and "excellent gate breakdown performance." Ex.1007, 16:2-11 (explaining that the graded dopant concentration in p-well 6p (illustrated in Figure 17) moves "electrons produced by the α-ray" to the substrate body 2S so that "soft errors can be reduced in case ... DRAM or the like is formed in the p-well 6p"), 19:15-23 ("the structure of the present embodiment 4 is applied to a 4M.DRAM"), 19:43-48, 20:1-33 (DRAM formed in accordance with embodiment 5, which uses Embodiment 4's downward sloping graded dopant concentration). A POSITA would have further appreciated that the twin-well CMOS device of Figure 23, when implemented using a uniformly-doped substrate as in Embodiment 1, would likewise been advantageously used for a DRAM device. Ex.1003, ¶115; Section X.A.1.b.

13.Claim 16

Kawagoe teaches a semiconductor flash memory device. Ex.1007, 22:14-18 ("The semiconductor integrated circuit device 1 of the present embodiment 7, as shown in FIG. 28, is exemplified by a flash memory."); Ex.1003, ¶116. The flash

memory device includes a CMOS "peripheral circuit region [] formed with the nMOS 4N and the pMOS 4P...." Ex.1007, 22:51-23:2. This peripheral circuit is fabricated according to twin-well CMOS technology, whereby NMOS transistors (e.g., 4N) are formed in "p-well 6*p*3," and PMOS transistors (e.g., 4P) are formed in "n-well 6*n*2." *Id.*, 22:51-65, FIG. 28. Significantly, Kawagoe explains that the teachings of Embodiment 4 (relied upon in mapping for claim 1) are applicable to Embodiment 7 and therefore flash memory. In particular, Embodiment 7 applies the teachings of Embodiment 4 relating to the use of an epitaxial substrate to form a twin-well architecture with pMOS transistor 4P formed in an n-well and nMOS transistor 4N formed in a p-well, where both wells have a downward-sloping graded dopant concentration. Ex.1007, 22:22-29 ("In the present embodiment 7, too, the semiconductor substrate 2 is formed thereover with a p-well 6*p*3 and an n-well 6*n*2. The p-well 6*p*3 and n-well 6*n*2 are formed, ***as in the foregoing embodiments 4 and 6***, to extend from the surface of the epitaxial layer 2E to the upper portion of the semiconductor substrate body 2S. Moreover, their impurity concentrations are made gradually lower depthwise of the semiconductor region 2, ***as in the foregoing embodiment 4***."), FIG. 28. The twin-well CMOS device of Figure 23, when implemented on a uniformly-doped substrate as in Embodiment 1 (as discussed for claim 1) would likewise have been used for a flash memory device. Ex.1003, ¶117; Section X.A.1.b.

14. Claim 17

Kawagoe teaches that its disclosed "techniques of the foregoing embodiments 1 to 7 can ... be applied to the semiconductor integrated circuit device which has a ***logic circuit*** such as the so-called 'microcomputer.'" Ex.1007, 24:28-31. The twin- well CMOS device of Figure 23, when implemented using a uniformly-doped substrate as in Embodiment 1, would likewise have been used for a logic device. Ex.1003, ¶118.

15. Claim 18

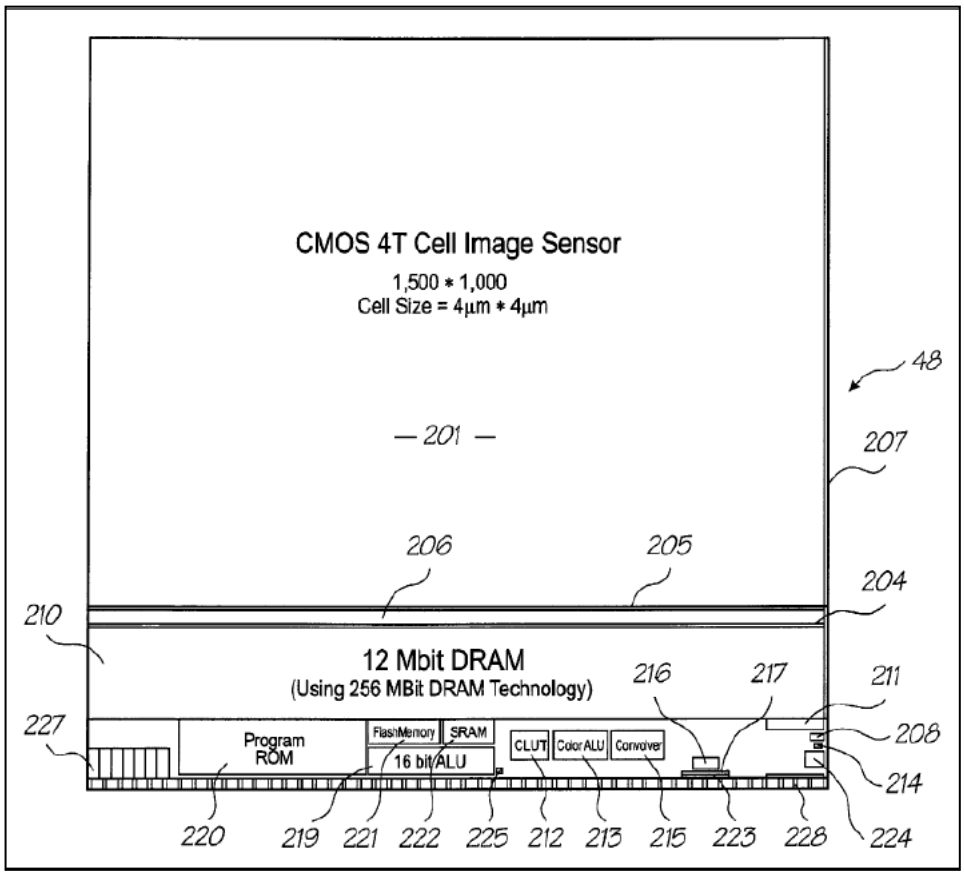
Kawagoe teaches that its disclosures can be applied to a "microcomputer." Section X.A.13. A POSITA would have understood that that a microcomputer includes a central processing unit (CPU). Ex.1032, 1334. The twin-well CMOS device of Figure 23, when implemented using a uniformly-doped substrate as in Embodiment 1, would likewise have been used for a central processing unit. Ex.1003, ¶119.

16. Claim 19

It would have been obvious to a POSITA to implement Kawagoe's semiconductor device in an image sensor. Ex.1003, ¶120. Kawagoe discloses a circuit comprising an "nMOS 4N and pMOS 4P [which] constitute a CMOS…circuit." Ex.1007, 8:46-52. A POSITA would have understood that

CMOS circuits are commonly used in a variety of applications. Ex.1003, ¶120. Moreover, Kawagoe teaches that the disclosed techniques can be applied to semiconductor integrated circuit devices with other logic circuits. *Id.*, 24:21-31, 19:15-18. A POSITA would have understood that one such an application would be an image sensor. Ex.1003, ¶120.

An example of such an image sensor is shown in U.S. Patent No. 6,614,560 ("Silverbrook"), pictured below. Ex.1042, 6:41-13:39, FIG. 15.



Consistent with Kawagoe's hypothesized applications, Silverbrook's image sensor includes "CMOS logic, a CMOS image sensor, DRAM, and analog circuitry." *Id.*, 6:56-57. As such, it would have been obvious to a POSITA that the

designs in Kawagoe could be implemented in an image sensor.

17. Independent Claim 20

a) Preamble

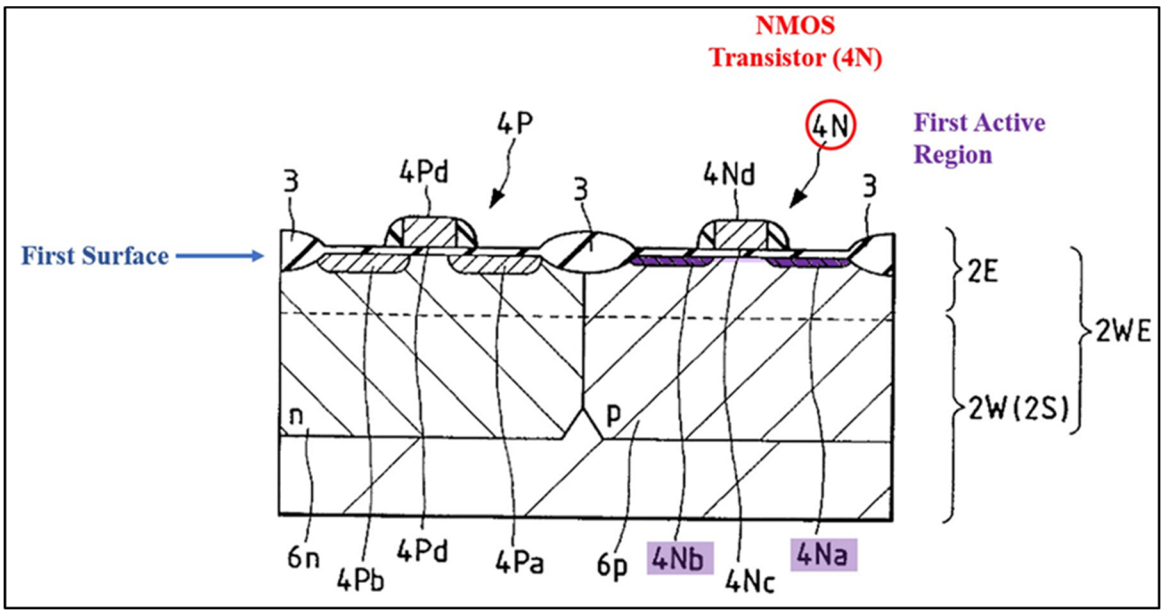
Section X.A.1.a.

b) Element[20.1]

Section X.A.1.b.

c) Element[20.2]

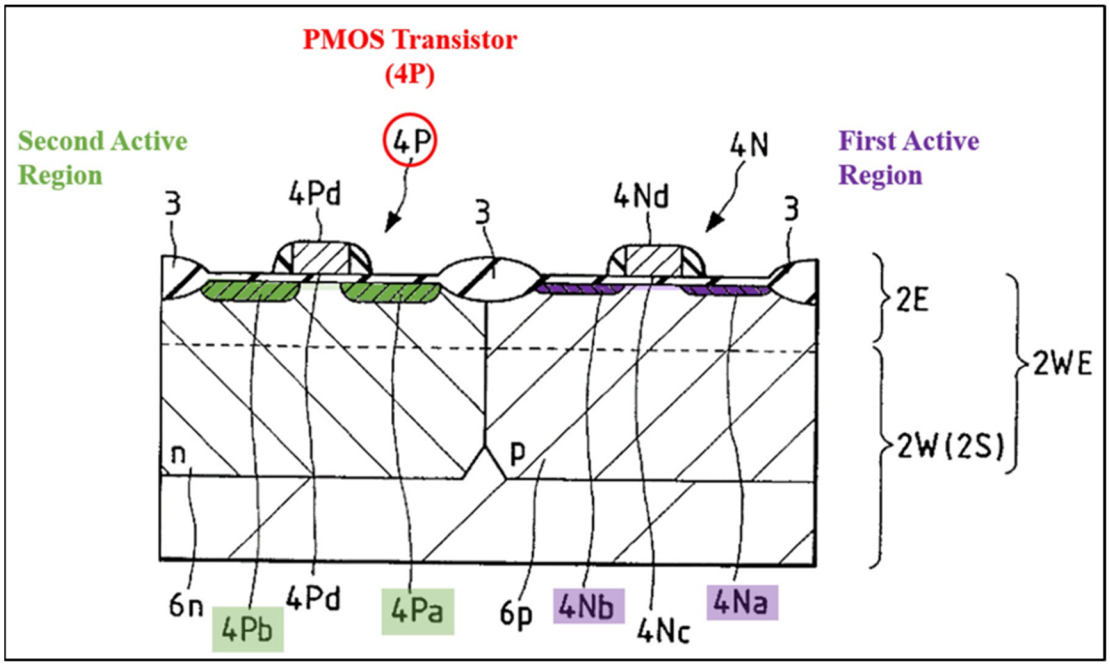
Section X.A.1.c. Kawagoe discloses nMOS transistor 4N formed in the surface of the first active region, as shown below. Ex.1003, ¶123.



Ex.1007, FIG. 23.

d) Element[20.3]

Section X.A.1.d. Kawagoe discloses pMOS transistor 4P formed in the surface of the second active region, as shown below. Ex.1003, ¶124.



Ex.1007, FIG. 23.

e) Element[20.4]

Section X.A.1.e.

f) Element[20.5]

Section X.A.1.f.

g) Element[20.6]

Section X.A.1.g.

18. Claim 21

Kawagoe discloses a substrate ("semiconductor substrate 2") of a first doping type. *See* Section X.A.1.b. At the time of the '481 Patent, it was well-known that CMOS devices, like Kawagoe's, could be fabricated within wells

formed on either n-type or p-type substrates. A POSITA would thus have understood that Kawagoe's devices could also be implemented on an n-type substrate. Kawagoe's "semiconductor substrate body and []epitaxial layer are made of p^--type Si. ***However, the present invention should not be limited thereto but can be modified such that the semiconductor substrate body and the epitaxial layer are made of n^--type Si."*** Ex. 1007, 23:56-61. In this n-type substrate alternative, the "first active region…with a second [opposite] doping type" would be a p-type region. *See* Ex. 1003, ¶128.

19. Claim 22

Section X.A.2.

20. Claim 23

Section X.A.3.

21. Claim 24

Section X.A.4.

22. Claim 25

Section X.A.5.

23. Claim 26

Section X.A.6.

24. Claim 27

Section X.A.9.

25. Claim 30

Section X.A.10.

26. Claim 31

Section X.A.7.

27. Claim 32

Kawagoe teaches that "nMOS 4N and pMOS 4P constitute a CMOS" device formed in and including a substrate. Ex.1007, 8:46-52, 15:26-40, 8:60-9:6, 9:41-54, 14:46-55; Ex.1003, ¶137; Section X.A.17.b.

28. Claim 33

Section X.A.13.

29. Claim 34

Section X.A.14.

30. Claim 35

Section X.A.15.

31. Claim 36

Section X.A.16.

B. Ground II

Wieczorek in combination with Wolf renders claims 1-2, 4-9, 12-22, 24-27, and 30-36 obvious. Ex.1003, ¶¶143-210. A POSITA would have been motivated to combine Wieczorek with Wolf. *Id.*, ¶142. This Petition relies on Wieczorek's description of a conventional prior-art CMOS device. Ex.1006, [0020]-[0021], [0004] ("Field effect transistors, such as MOS transistors, represent one of the most frequently used circuit elements in modem [sic] integrated circuits."), [0007]-[0008] (describing "[a] typical process flow for forming the semiconductor device 100" which is "a complementary MOS transistor pair"), [0012], FIG. 1b. Wolf is a well- known textbook that teaches known fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on CMOS devices. *See generally* Ex.1008A; *id.*, Chapter 16 ("CMOS Process Integration"); Ex.1003, ¶142. A POSITA would have therefore understood and expected that the teachings of Wolf would apply to Wieczorek's conventional CMOS device. *Id*. A POSITA would have looked to Wolf for additional details related to conventional CMOS devices, as further detailed below. *Id.*

While Wieczorek proposed a different approach to address some perceived difficulties in maintaining a retrograde profile in conventional prior art device, Ex.1006, [0013]-[0014], the conventional device can nonetheless serve as the basis for an obviousness challenge. *Netflix, Inc. v. DivX, LLC*, No. 2022-1083, 2023 WL

2298768, (Fed. Cir. Mar. 1, 2023) ("[A] prior-art reference 'must be considered for everything it *teaches* by way of technology and is not limited to the particular *invention* it is describing and attempting to protect.'") (citing *EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985) (emphases in original). Further, as Dr. Banerjee explains, at the relevant time, the conventional device was operable and widely-used, and techniques (for example, rapid thermal annealing) were available to manage the perceived difficulties with maintaining a retrograde dopant profile. Ex.1003, ¶142.

1. Independent Claim 1

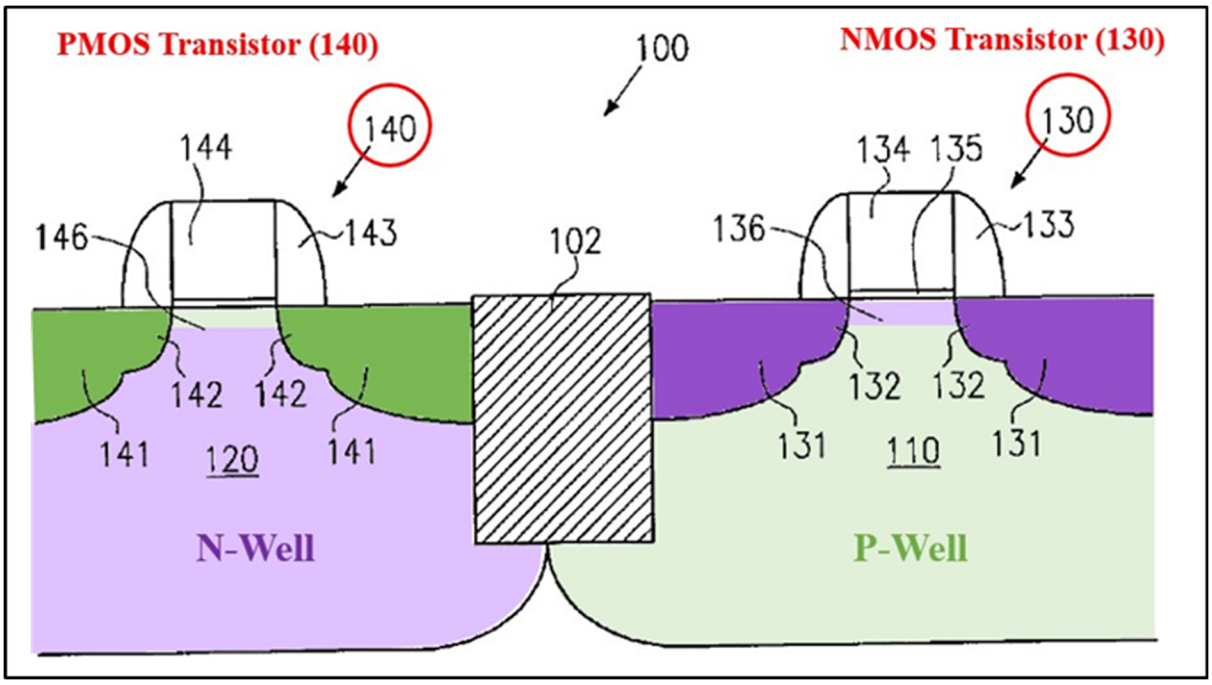
a) Preamble

Wieczorek teaches a "semiconductor device 100." Ex.1006, [0012]; Ex.1003, ¶143.

b) Element[1.1]

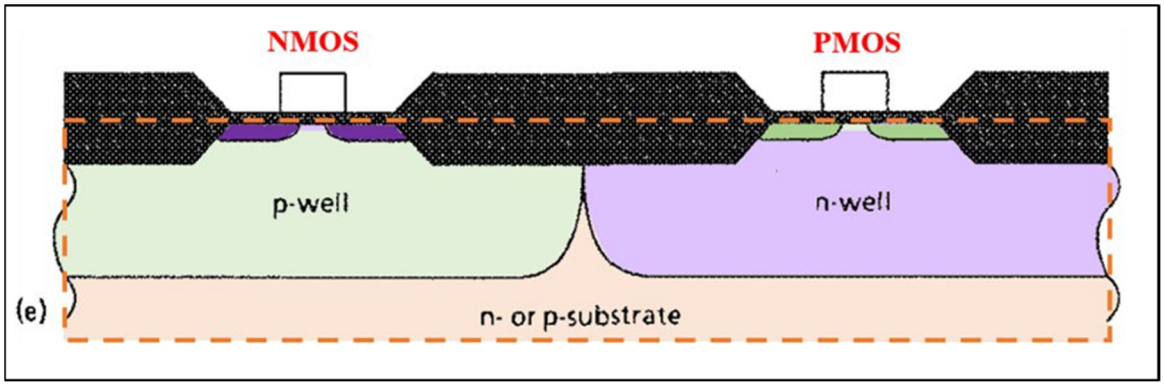
Wieczorek in combination with Wolf (hereinafter, "Wieczorek-Wolf") renders this element obvious. Ex.1003, ¶¶144-149. The below annotation of Wieczorek's Figure 1b shows a conventional twin-well CMOS device, in which N- channel transistor 130 (nMOS) with source/drain regions 131-132 (purple) and channel region 136 (light purple) is formed in P-well 110 (light green) and P-channel transistor 140 (pMOS) with source/drain regions 141-142 (green) and channel region 146 (light green) is formed in N-well 120 (light purple). Ex.1006, [0007], [0012], [0020]-[0021]; Ex.1008C, 525, FIG. 8-1(e). Wieczorek explains

that the P-well and N-well structures are formed in a "semiconductor region 101, such as a silicon region" of a semiconductor element 100, and recognizes that such CMOS devices would be "formed on" any "appropriate substrate." Ex.1006, [0004], [0007] Ex.1003, ¶144.



Ex.1006, FIG. 1b ("Prior Art"). A POSITA would have understood that a twin well (or twin-tub) approach "is independent of starting material type" for the substrate. Ex.1008C, 524; Ex.1006, [0004] (discussing use of "an appropriate substrate" for forming MOS transistors without further specificity); Ex.1003, ¶145. Because Wieczorek does not specify what constitutes an appropriate substrate, a POSITA would have been motivated to consult Wolf, which confirms that a "uniform, lightly doped p- or n-type substrate" is a suitable substrate commonly used in twin-well CMOS devices. Ex.1008C, 523, 530 ("With the twin-

tub [(twin-well)] approach, two separate wells are formed for n- and p-channel transistors on a lightly doped substrate ... of n or p material."); Ex.1008B, 387-389; Ex.1003, ¶146.

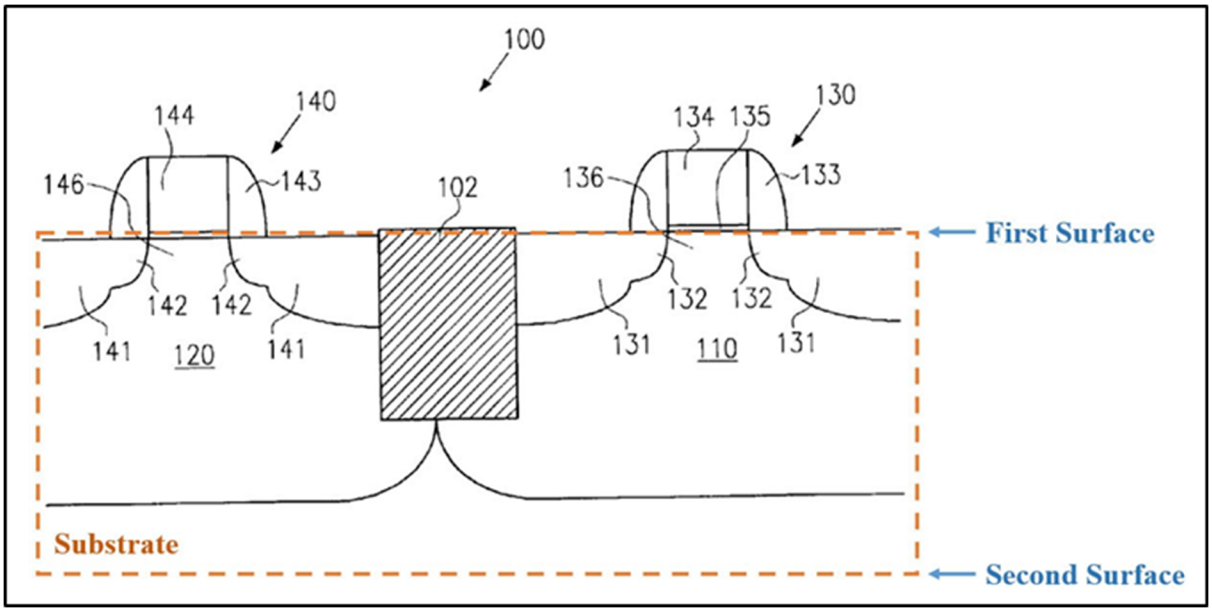


Ex.1008C, 525, FIG. 8-1(e) ("twin-well CMOS on *n*- or *p*-substrate").

Thus, consistent with Wieczorek's teaching, a POSITA would have found it obvious to use a uniformly doped n- or p-type substrate ("a substrate of a first doping type at a first doping level") as a suitable substrate for Wieczorek's CMOS device in Figure 1b. Ex.1003, ¶147. Doing so would amount to combining known prior art elements (*i.e.*, the use of a uniform, lightly doped *n*- or *p*-type substrate with Wieczorek's process for forming a conventional CMOS device) according to known methods (*i.e.*, the known use of an "appropriate substrate" for the conventional process of forming the CMOS device in Wieczorek [0007]-[0013]) to obtain predictable results (*i.e.*, the conventional CMOS device in Wieczorek's Figure 1b). Ex.1003, ¶147. Doing so would have also been obvious to try because it involves nothing more than choosing one of a finite number of known appropriate substrates that are described by Wolf as suitable for use in forming a

twin-well CMOS device like Wieczorek's. *See* Ex.1008C, 530 ("With the twin-tub approach, two separate wells are formed for n- and p-channel transistors on a lightly doped substrate. … The substrate may be either a lightly doped wafer of n or p material, or a thin, lightly- doped epitaxial layer on a heavily doped substrate"); Ex.1008A, 816; (as explained above, another substrate option for a twin-well CMOS structure is a lightly-doped epitaxial layer atop substrate body having the same doping level, as reflected in Kawagoe's Embodiment 1); Ex.1003, ¶147. There would have been reasonable expectation of success because Wolf shows that a POSITA would have known how to use a uniformly doped *n*- or *p*-type substrate to form a twin-well CMOS device similarly as described in Wieczorek. *Id*.

For claim mapping purposes, Wieczorek-Wolf's substrate is taken as a p-type nonepitaxial substrate, which has the advantage of lower cost compared to an epitaxial substrate. Ex.1003, ¶148; Ex.1008A, 816 ("in twin-well CMOS the starting material is also ***either*** a lightly p-doped wafer (***p-bulk wafer***, Fig. 16-7a), or a heavily p-doped wafer on which a thin, lightly p-doped epi layer is grown" and noting the cost disadvantage of epitaxial wafers), FIG. 16-7. Consistent with the teachings of Wolf, Wieczorek's substrate (orange dotted line) in Figure 1b below, has a top surface ("first surface") and a bottom surface ("second surface"). Ex.1008B, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex.1008C, 525, FIG. 8-1(e); Ex.1003, ¶148.



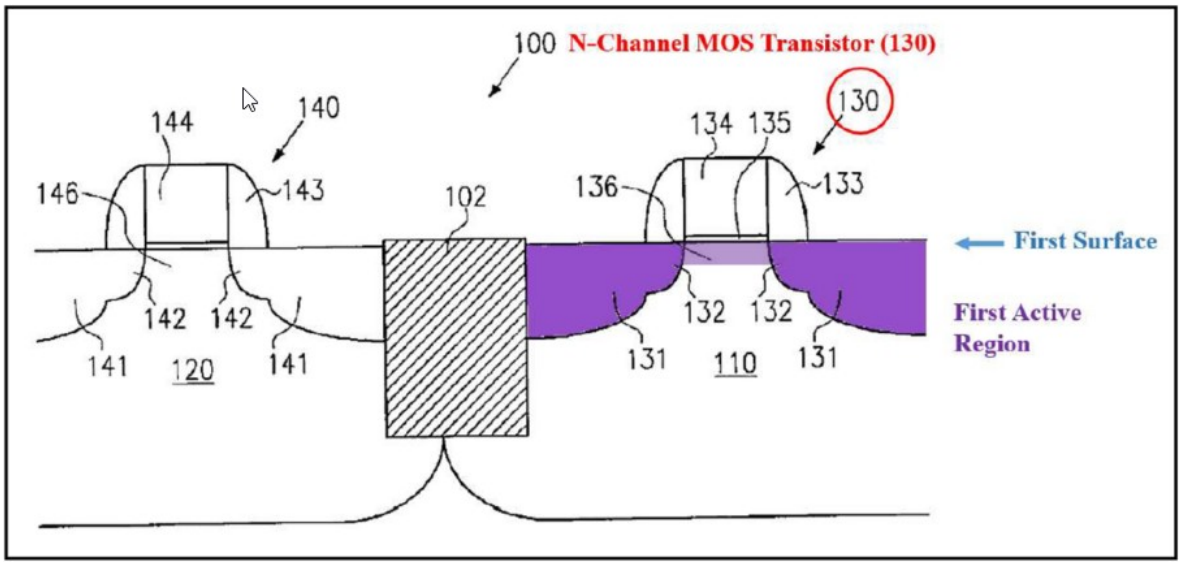
Ex.1006, FIG. 1b. While the semiconductor substrate is not explicitly labeled in Figure 1b, a POSITA would have understood that the substrate is the starting point material for subsequent processing of transistor devices. Ex.1003, ¶148; *see also* Ex.1006, [0027] (describing, for Figure 3a, that the N-well and P-well structures therein are "formed in a semiconductor substrate 301"); *id.*, cls. 1, 31.

Wieczorek-Wolf satisfies element[1.1] under PO's plain meaning construction. Section VIII; Ex.1006, [0004], [0012]; Ex.1003, ¶149.

c) Element[1.2]

Wieczorek-Wolf renders obvious this element. Ex.1003, ¶¶150-153. Wieczorek discloses "an N-channel transistor 130" that includes "heavily N-doped ***source and drain regions*** 131, including lightly doped extensions 132," and "***channel region 136***." Ex.1006, [0012]-[0013]; *id.*, [0004] ("[A] field effect transistor comprises two highly doped semiconductor regions...referred to as

drain and source regions, and which are embedded in a lightly and inversely doped semiconductor region, the so-called N-well or P-well ... The drain and source regions are spaced apart with a ***channel region*** interposed, wherein a conductive channel forms between the drain and source regions in the channel region" when the transistor is active). The source-drain regions 131-132 (annotated in purple in Figure 1b, below) form part of the claimed first active region, which also includes channel region 136 (light purple) between them. Ex.1006, [0012]; Ex.1003, ¶150; Ex.1008B, 299 ("The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source and drain*** regions."), 300, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex.1008C, 525, FIG. 8-1(e). As shown in Figure 1b, nMOS transistor 130 is formed in the first active region, which is adjacent the first surface of the substrate. Ex.1003, ¶150.



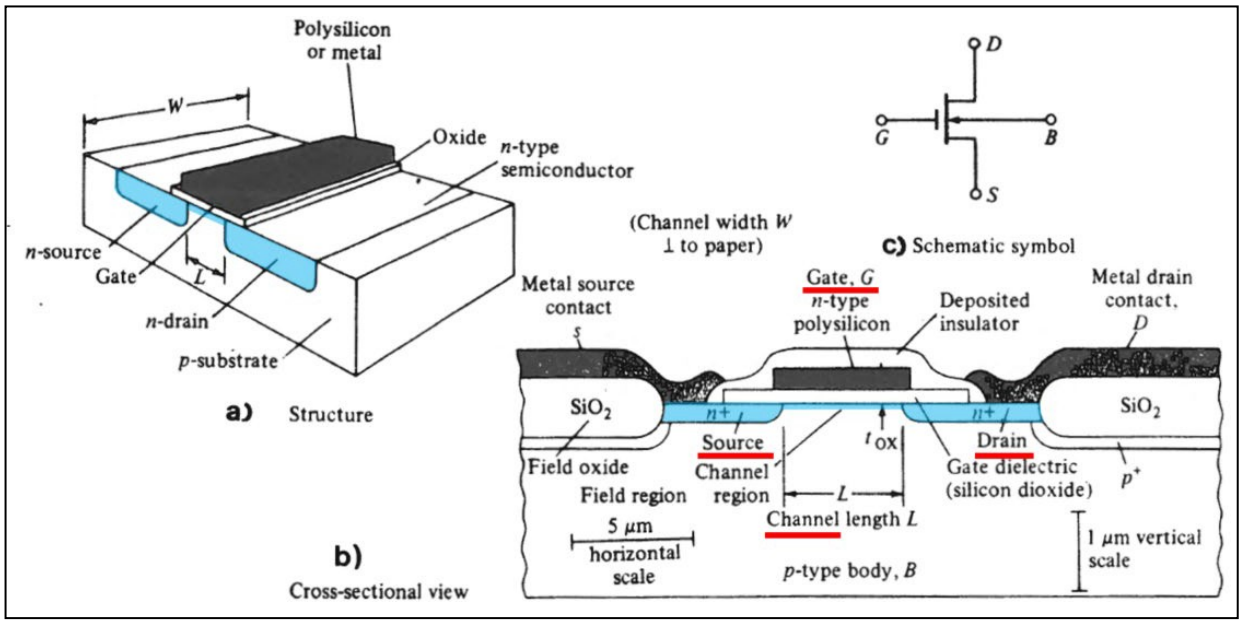
Ex.1006, FIG. 1b, [0007].

Because the source-drain regions of the first active region are N-doped, Wieczorek-Wolf's first active region has a second doping type (N-type) opposite in conductivity to the first doping type (P-type) of the substrate. Ex.1006, [0012]; Ex.1003, ¶151.

While Figure 1b illustrates a single exemplary nMOS transistor 130 formed in the first active region, a POSITA would have understood that Wieczorek teaches forming multiple nMOS transistors in the first active region to minimize chip area, as good layout practice dictates. Ex.1006, [0004]; Ex.1003 ¶152; Ex.1014, 1:52-54, 2:17-21. In any event, according to PO, "active region...within which transistors can be formed" means "an active region...where a ***transistor*** can be formed." Ex.1020, 31.

Wieczorek satisfies element[1.2] under PO's construction that "active region" means "a doped silicon region at the surface of a semiconductor device (e.g., the

source and drain and silicon between them) where a transistor can be formed." Ex.1020, 20; Section VIII; Ex.1003, ¶153. Indeed, the active region of a MOS transistor is "[its] channel and [its] heavily doped source and drain regions" (blue). Ex.1008B, 299.

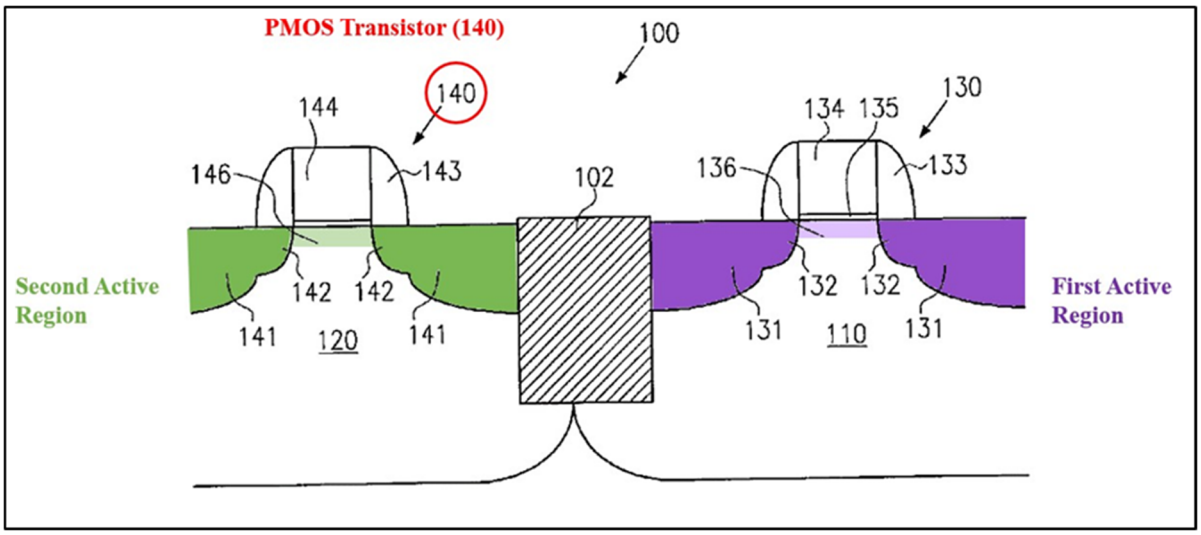


Ex.1008B, FIG. 5-1; *id.*, 298-301, FIGS. 5-2, FIG. 6-4.

d) Element[1.3]

Wieczorek discloses "a P-channel transistor 140," including "heavily P-doped source and drain regions 141, including lightly doped extensions 142," and "channel region 146." Ex.1006, [0004], [0007], [0012]-[0013]; Ex.1003, ¶154. The source and drain regions 141-142 (green) are part of the claimed second active region, which also includes channel region 146 (light green) between them. Ex.1006, [0012]; Ex.1008B, 298-301, FIGS. 5-1, 5-2, 6-4; Section X.B.1.c; Ex.1003, ¶154. As shown in Figure 1b, pMOS transistor 140 is formed in the

second active region (green/light green), which is separate from and disposed adjacent to the first active region (purple/light purple). Ex.1006, [0012]; Ex.1003, ¶155. Adjacent active regions are separated by an isolation region (*e.g.*, shallow trench isolation 102). Ex.1006, [0007]; Ex.1008A, 818-20, FIG. 16-11(f); Ex.1001, Cl. 6; Ex.1003, ¶155; Section X.A.1.d.



Ex.1006, FIG. 1b, [0007].

While the figure shows an exemplary pMOS transistor 140 formed in the second active region, a POSITA would have understood that Wieczorek teaches forming multiple pMOS transistors in the second active region. Ex.1006, [0004]; Ex.1003, ¶156; Section X.B.1.c. Regardless, according to PO, "active region ... within which transistors can be formed" means "an active region ... where ***a transistor*** can be formed." Ex.1020, 31.

Wieczorek satisfies element[1.3] under PO's position that "active region" means "a doped silicon region at the surface of a semiconductor device (e.g., the

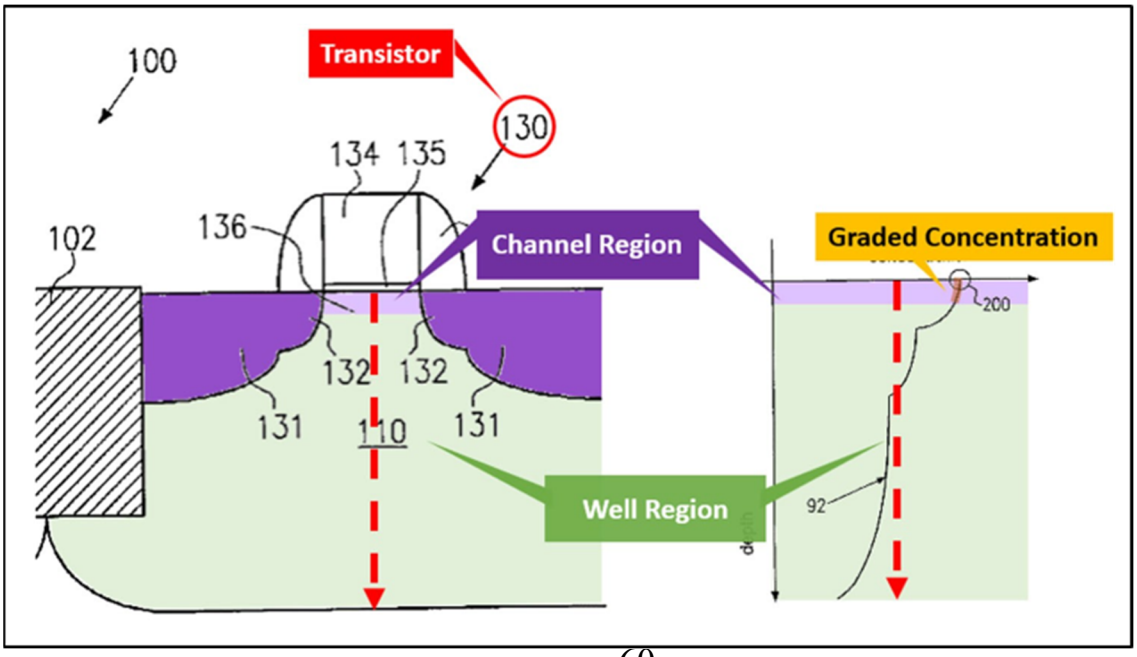
source and drain and silicon between them) where a transistor can be formed." Section X.B.1.c; Ex.1003, ¶157.

e) Element[1.4]

See Sections X.B.1.c-d.

f) Element[1.5]

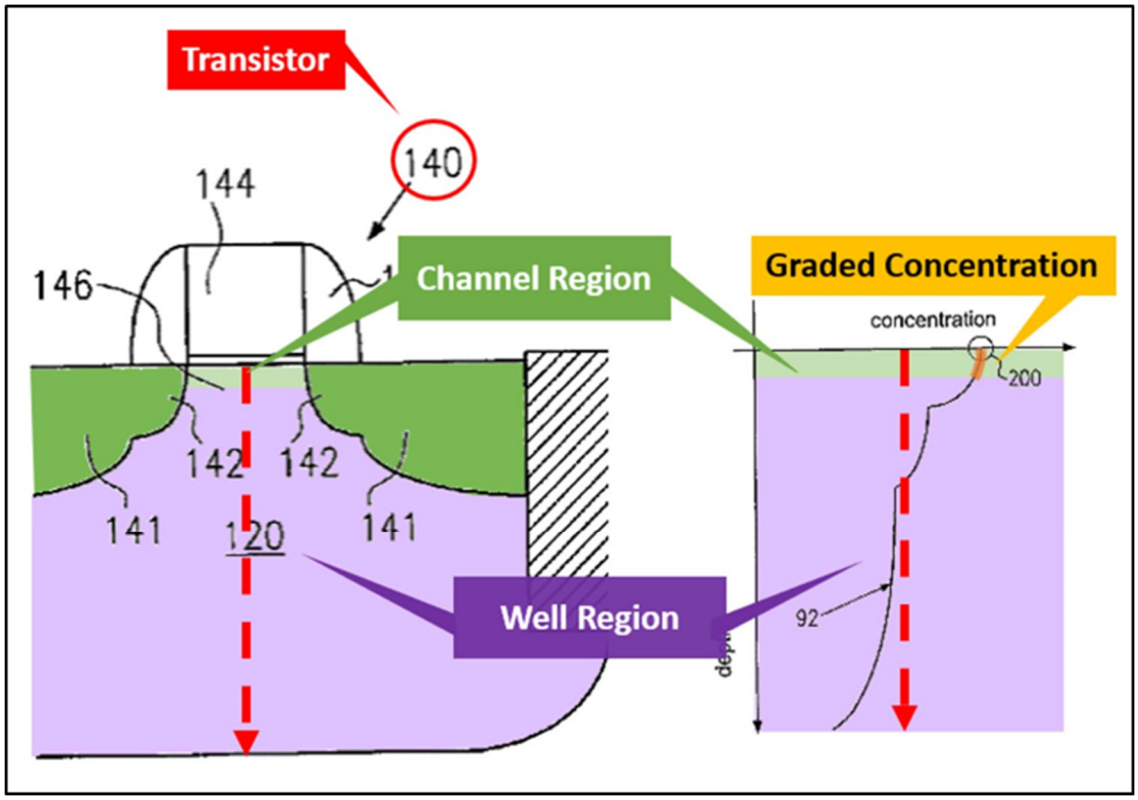
Wieczorek-Wolf renders obvious this element. Ex.1003, ¶¶159-163. In Figure 1b (below left), the channel region (light purple, indicated by lead line 136) of nMOS transistor 130, formed at the top surface of the substrate, is a portion of the first active region. Ex.1006, [0012]-[0013], [0004] ("The drain and source regions are spaced apart with a channel region interposed"); Ex.1008B, 298-301 ("The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source and drain*** regions."), FIG. 5- 2; Ex.1003, ¶159.



Ex.1006, FIGS. 1b, 2b. The doping concentration in the channel region is highlighted in brown in the doping profile of Figure 2b (above right), which is measured for example along the red dotted line in Figure 1b that traverses the channel region. *Id.*, [0011] ("FIG. 2b shows ... a typical dopant profile with respect to the depth of the respective well structure."), [0013] ("after the plurality of heat treatments, the actual dopant concentration will be represented by the graph shown in FIG. 2b."), [0009], FIG. 2a.

As Figure 2b shows, the dopant concentration is highest at the surface of the substrate and decreases with depth. Ex.1003, ¶160. Therefore, the channel region 136 has a graded dopant concentration. *Id.* As shown in Figure 2b above, Wieczorek's graded dopant concentration is in fact downward-sloping from the top surface of the substrate and all the way through the entire depth of the channel region (light purple) and the underlying well-region (P-well 110) (green). Ex.1006, [0011]; Ex.1003, ¶160.

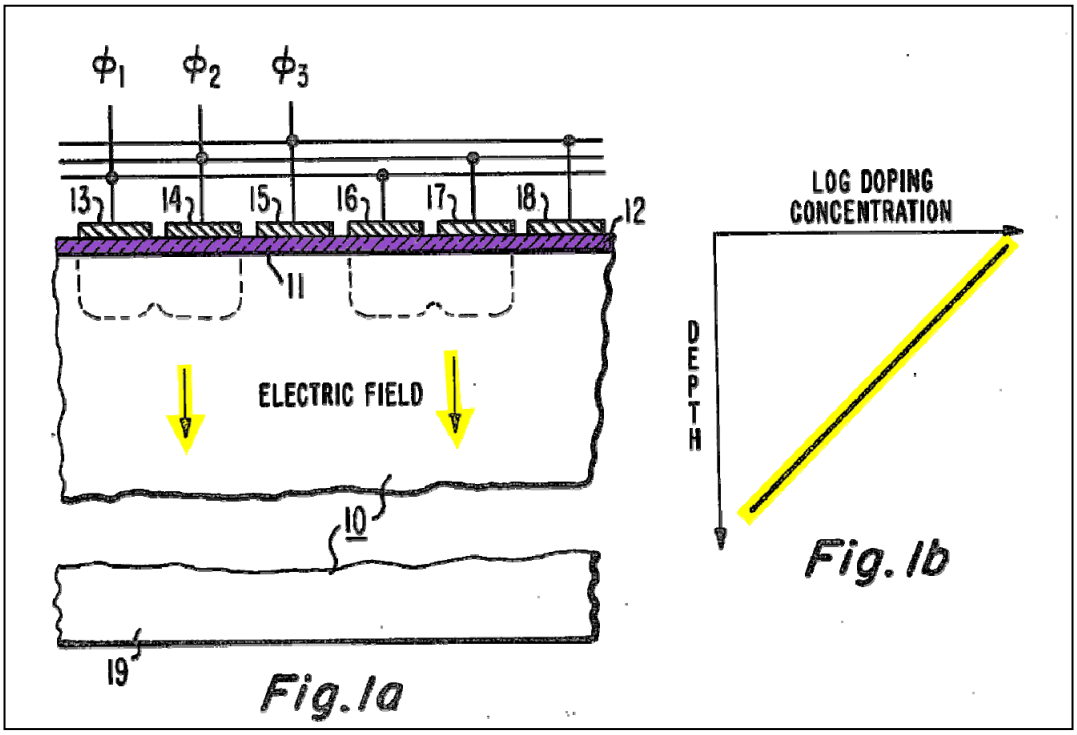
As shown below, Wieczorek teaches that the channel region (light green, indicated by lead line 146) of pMOS transistor 140, which is a portion of the second active region, also has a graded dopant concentration for the same reasons. Ex.1006, [0004], [0009], [0011]-[0013], FIGS. 2a-2b; Ex.1008B, 298-301, FIG. 5-2; Ex.1003, ¶160.



Ex.1006, FIGS. 1b, 2b. Thus, Wieczorek discloses "at least a portion of" the first and second active regions (channel regions) having a downward-sloping graded dopant concentration. Ex.1006, [0009], [0011], [0013]; Ex.1003, ¶160. In discussing Figure 2b, Wieczorek mentions that following heat treatment, the profile "in the vicinity of the surface of the semiconductor device 100 (reference number 200), may have become substantially uniformly distributed," *id.* at [0011], but this description is made relative to the "initially retrograde profile" shown in Figure 2a; Wieczorek still teaches and depicts a graded dopant concentration that is downward-sloping from the top surface of the substrate. Ex.1003, ¶160.

Further, Wieczorek's downward-sloping graded dopant concentration aids movement of carriers (*i.e.*, electrons in *p*-type layer, holes in *n*-type layer) from the

first surface to the second surface of the substrate to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. Ex.1003, ¶¶161-162. As detailed in Section X.A.1.g, during prosecution of the parent '195 Patent, Applicant represented to the Office that a downward-sloping graded dopant concentration was known to move carriers deep into the substrate. Applicant cited Jastrzebski and Kamins in support. Section X.A.1.g. Notably, according to Jastrzebski, a downward- sloping graded dopant concentration creates an electric drift field that "force[s] most of the charge carriers ... ***deep into the substrate***[.]" Ex.1010, 2:27-32, 5:13-22.



Id., FIGS. 1a-1b.

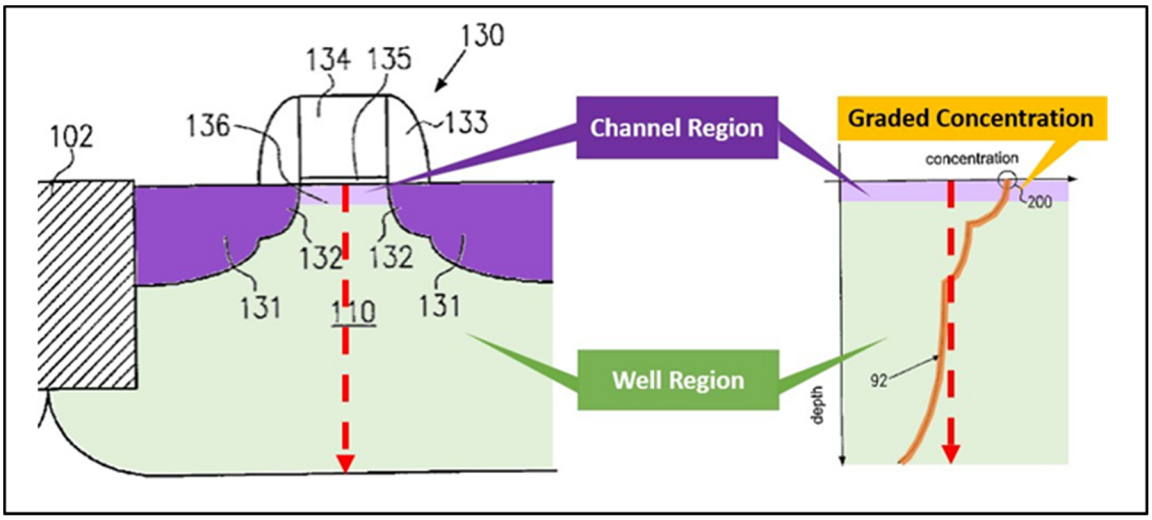
Accordingly, Wieczorek satisfies element[1.5] under PO's plain meaning

construction of the "to aid carrier movement" term. Section VIII; Ex.1003, ¶163. According to PO, the claims make clear that "carriers [must move] in a particular direction (from the surface layer to the substrate)." Ex.1020, 29. Also, according to PO, "[w]hen the dopant concentration is graded in a particular direction, [certain] charge carriers will move in the [same] gradient direction." *Id.*, 2. Here, Wieczorek's Figure 2b shows that the dopant concentration is downward-sloping with increasing depth towards the bottom of the substrate, and thus, according to PO, this graded dopant concentration causes carriers to move deeper into the substrate as well. Ex.1003 ¶163.

g) Element[1.6]

Wieczorek-Wolf renders obvious this element. Ex.1003, ¶¶164-167. As shown in Figure 1b (below left), Wieczorek discloses a "P-well structure 110" (light green) adjacent to the first active region (purple/light purple). Ex.1006, [0012]- [0013]; Ex.1003, ¶164. And, as shown in the dopant concentration profile (brown) of Figure 2b (below right), the dopant concentration in P-well 110—measured along the exemplary red dotted line in Figure 1b—is gradually decreasing with depth. Ex.1006, [0009], [0011] ("FIG. 2b shows ... a typical dopant profile with respect to the depth of the respective well structure [110 and 120]"), [0013]; Ex.1003, ¶164. Thus, Wieczorek discloses a well region containing at least one graded dopant region (e.g., the region highlighted in light green in both Figures 1b and 2b) having a downward-sloping graded dopant concentration.

Ex.1003, ¶164.



Ex.1006, FIGS. 1b, 2b. Under Applicant's representation to the Patent Office, discussed above in Section X.A.1.g, such a downward-sloping graded dopant concentration was known in the prior art to create a "built-in" electric field that moves carriers deep into the substrate and thus aids carrier movement from the first surface to the second surface of the substrate. Ex.1003, ¶165.

Accordingly, Wieczorek satisfies element[1.6] under PO's construction that "well region" means "a doped region that surrounds the active region of a semiconductor device." Ex.1020, 30; Section VIII; Ex.1003, ¶166. As shown in Figure 1b above, P-well 110 (light green) is a doped region that surrounds the first active region (purple/light purple). *Id*. Wieczorek also satisfies element[1.6] under PO's plain meaning construction of the "to aid carrier movement" term. *Id.*

2. Claim 2

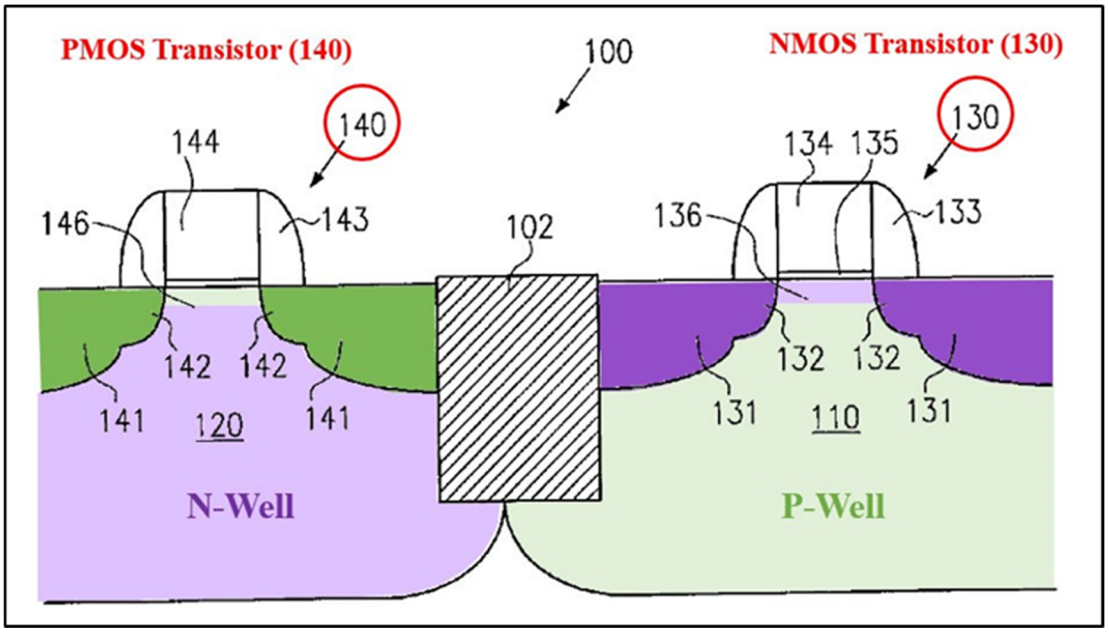
Section X.B.1.b.

3. Claim 4

Sections X.B.1.c-e.

4. Claim 5

Wieczorek's Figure 1b illustrates a conventional twin-well architecture, whereby the first active region contains an "N-channel transistor 130" in "P-well" 110, and the second active region contains a "P-channel transistor 140" in "N-well" 120. Ex.1006, [0012]-[0013], [0004]; Ex.1003, ¶170; Sections X.B.1.c-d. This mapping satisfies this element under PO's interpretation that a claimed active region can contain "***a transistor***." Ex.1020, 31; Ex.1003, ¶170. A POSITA would have also understood that Wieczorek teaches forming multiple transistors in an active region to save chip area. Ex.1003, ¶170.

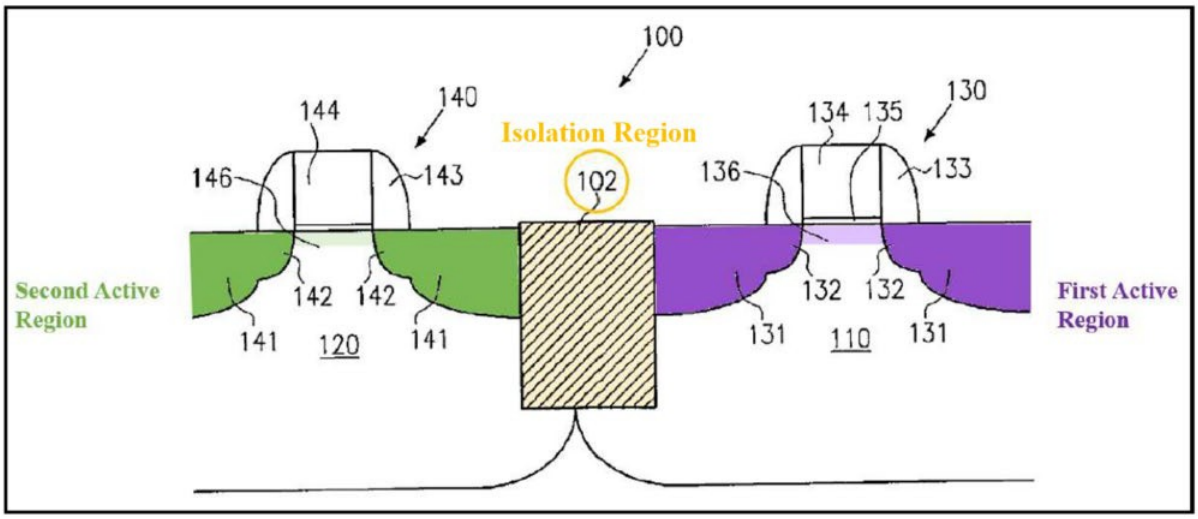


Ex.1006, FIG. 1b. Further, Wieczorek's wells have a graded concentration of

dopants. Ex.1006, [0009]-[0011] ("FIG. 2b shows ... a typical dopant profile with respect to the depth of the respective well structure [110/120]."), [0013], FIGS. 2a-2b; Section X.B.1.g (discussing graded dopants in P-well 110); Ex.1003, ¶170.

5. Claim 6

As shown below, the first (purple/light purple) and second (green/light green) active regions are separated by "shallow trench isolation 102" (yellow). Ex.1006, [0007]; Ex.1003, ¶171.



Ex.1006, FIG. 1b.

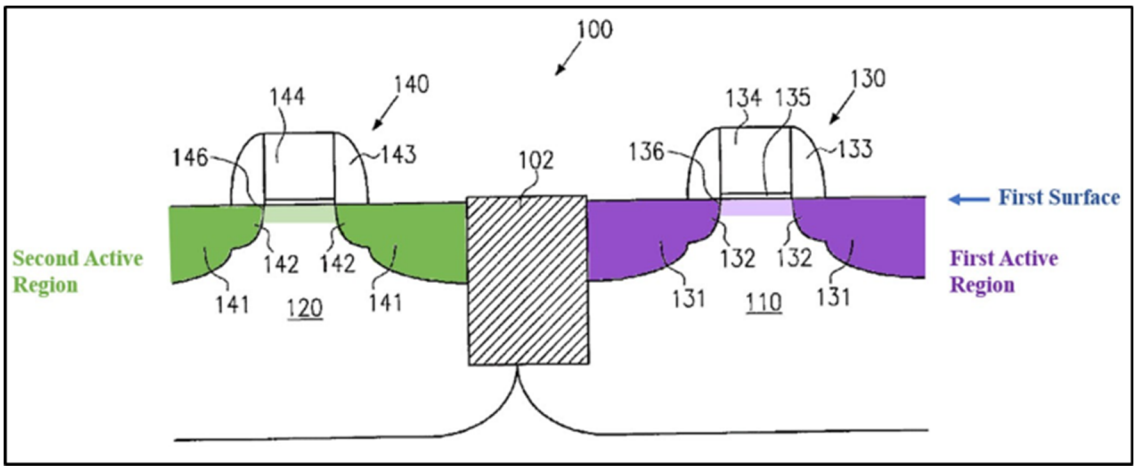
6. Claim 7

Wieczorek teaches that the graded dopants in "P-well structure 110 and [] N- well structure 120 are defined by sequentially performed ion implantation processes." Ex.1006, [0008], [0007]-[0011], FIGS. 1a, 2a-2b; Ex.1003, ¶172; Sections X.B.1.f-g. At the relevant time, ion implantation, given its precision and flexibility, was the technique typically used for introducing dopants

during semiconductor processing. Ex.1003, ¶172.

7. Claim 8

As shown below, the first (purple/light purple) and second (green/light green) active regions are formed adjacent the first surface of the substrate (blue). Ex.1006, [0007]-[0010], [0012]-[0013]; Ex.1008B, 299 ("The top surface of the [substrate] body consists of active or transistor regions..."), 298-301, FIG. 5-2; Ex.1003, ¶173; Sections X.B.1.c-d.

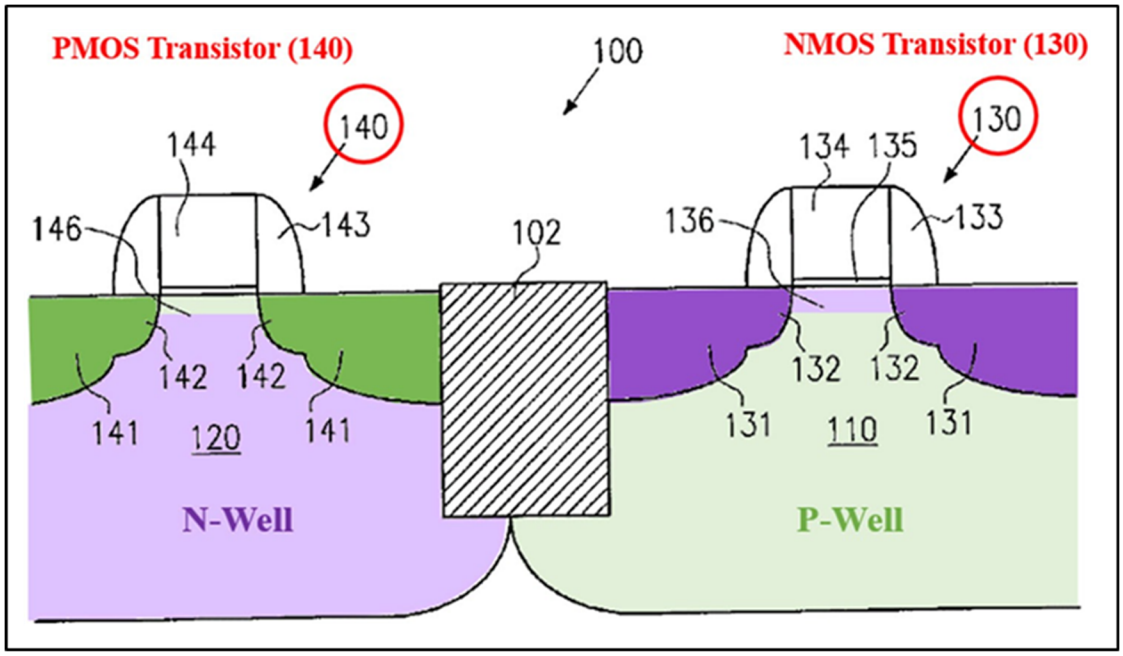


Ex.1006, FIG. 1b.

Claim 9

As shown in Figure 1b below, channel region (light purple, indicated by lead line 136) of the first active region is formed at the top of P-well 110 and is of the same doping type (p-type) as P-well 110. Ex.1006, [0008] ("for defining the P-well structure 110, typically boron ions are employed"); Ex.1007, 15:28-29; Ex.1003, ¶174. Likewise, channel region (light green, indicated by lead line 146) of

the second active region is formed at the top of N-well 120 and is of the same doping type (n- type) as N-well 120. Ex.1006, [0008] ("[f]or defining the N-well structure 120, typically phosphorous or arsenic ions are used"); Ex.1007, 9:33-35; Ex.1003, ¶175.



Ex.1006, FIG. 1b. Those channel regions have a graded dopant concentration, as discussed above. Section X.B.1.f; Ex.1003, ¶176.

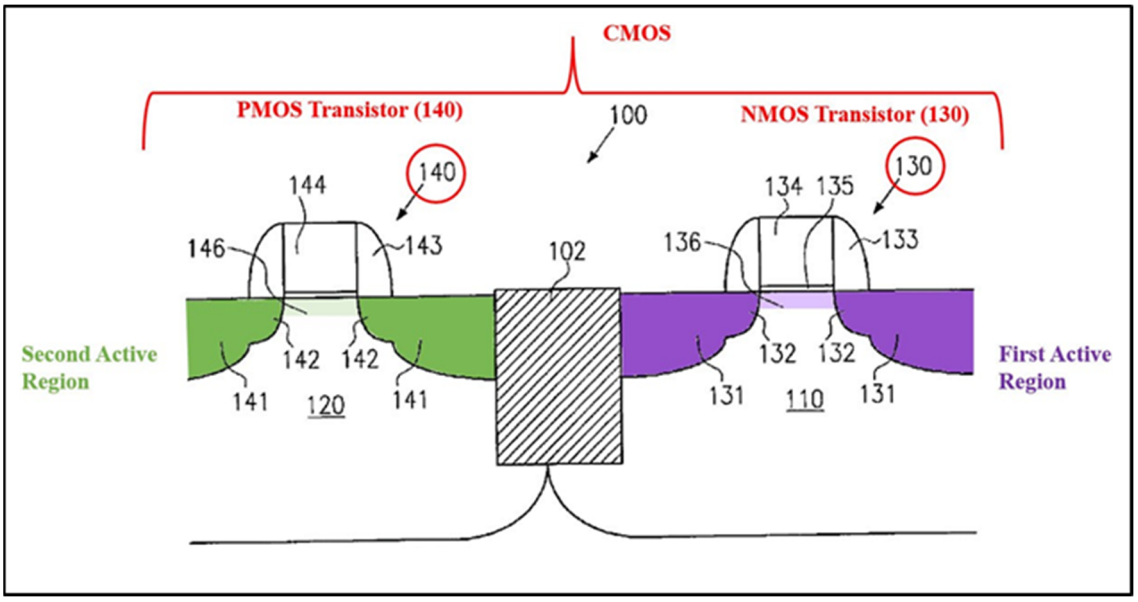
8. Claim 12

Wieczorek-Wolf renders obvious an N-well (doped with n-type impurity) formed within a p-type substrate. *See* Section X.B.1.b (element [1.1]). Ex.1006, [0004]-[0008], [0027]; Ex.1008B, 387-389; Ex.1008C, 523-530, FIG. 8-1(e). Because the implantation of n-type impurity does not remove the substrate's p-type dopants, the N-well includes "both p-type and n-type" dopants. Ex.1003,

¶177.

9. Claim 13

Wieczorek discloses "a complementary MOS [(CMOS)] transistor pair" comprising "N-channel transistor 130" in the first active region (purple/light purple) and "P-channel transistor 140" in the second active region (green/light green). Ex.1006, [0007], [0012]-[0013]; Ex.1003, ¶178.



Ex.1006, FIG. 1b. Each of the CMOS transistors include a source, drain, gate, and channel. Ex.1003, ¶178. N-channel transistor 130 includes "heavily N-doped source and drain regions 131" (purple), "gate electrode 134," and "channel region 136" (light purple). Ex.1006, [0012]-[0013]; Ex.1003, ¶178. P-channel transistor 140 includes "heavily P-doped source and drain regions 141" (green), "gate electrode 144," and "channel region 146" (light green). *Id.*; Sections X.B.1.c-d, X.B.1.f.

10.Claim 14

Wieczorek's teaching relied on in this Petition is directed to conventional CMOS technology. Section X.B.1.b; Ex.1006, [0007], [0020]-[0021]; Ex.1003, ¶179. It would have been obvious to apply Wieczorek's conventional CMOS technology to fabricate a DRAM device to realize "the advantages of cost per bit, device density, and flexibility of use (both read and write operations are possible) [which] have made DRAMs the most widely used form of semiconductor memory to date." Ex.1008B, 587, 597; Ex.1003, ¶179. Wieczorek also suggests doing so in teaching the frequent application of its technology to "mode[rn] integrated circuits." Ex.1006, [0004], [0026]; Ex.1003, ¶179. Likewise, at the relevant time, DRAMs were known to be designed using conventional CMOS technology, and a POSITA would have appreciated that fabricating a DRAM using CMOS technology, such as Wieczorek, would have provided a number of advantages, including "lower power dissipation [] and smaller soft error rates," lower design complexity, lower operating voltage, and reduced memory access time. Ex.1008B, 596-597; Ex.1003, ¶179.

Additionally, using Wieczorek's technology to form a DRAM device would have merely amounted to combining known, conventional prior art elements (Wieczorek's CMOS process and known CMOS DRAM designs) according to known methods (Wieczorek's CMOS process) and, at most, involves a simple

substitution of one known element (CMOS technology contemplated by Wolf for DRAM) with another (Wieczorek's conventional CMOS technology). Ex.1003, ¶180. There would have been reasonable expectation of success with predictable results because Wieczorek's conventional CMOS process was a known technique and would have been used for its intended purpose in manufacturing DRAM devices, which were commonly implemented using CMOS technology in order to gain the aforementioned benefits. *Id*.

11. Claim 15

Section X.B.1.b.

12. Claim 16

Wieczorek's teaching relied on in this Petition is directed to conventional CMOS technology. Section X.B.1.b; Ex.1006, [0007], [0020]-[0021]; Ex.1003, ¶182. It would have been obvious to apply Wieczorek's conventional CMOS technology to fabricate a flash memory device in order to achieve the benefits of "lower power-dissipation" of CMOS technology and "high density [], small-die size, lower cost, and hot-electron writability of EPROMs, together with the easy erasability, on-board reprogrammability, and electron-tunneling erasure features of EEPROMs." Ex.1008B, 634; Ex.1008A, 808-810; Ex.1003, ¶182. Wieczorek also suggests doing so in teaching the frequent application of its technology to "mode[rn] integrated circuits." Ex.1006, [0004], [0026]; Ex.1003,

¶182. Indeed, flash memory devices commonly used CMOS technology. Ex.1008B, 633-635 (describing known "CMOS flash-EEPROM" devices); Ex.1007, 22:16-17 (flash EEPROM is flash memory), 22:10-23:2, FIG. 28 (peripheral flash memory circuit with CMOS transistors); Ex.1003, ¶182; Section X.A.12.

Using Wieczorek's technology to form flash memory would have merely amounted to combining known, conventional prior art elements (Wieczorek's CMOS process and known CMOS flash memory designs) according to known methods (Wieczorek's CMOS process) and, at most, involves a simple substitution of one known element (CMOS technology for prior art flash memory) with another (Wieczorek's conventional CMOS technology). Ex.1003, ¶183. There would have been reasonable expectation of success with predictable results because Wieczorek's conventional CMOS process was a known technique and would have been used for its intended purpose in manufacturing flash memory devices, which were commonly implemented using CMOS technology in order to gain the abovementioned benefits. *Id*.

13. Claim 17

Wieczorek's teaching relied on in this Petition is directed to conventional twin-well CMOS technology. Section X.B.1.b; Ex.1006, [0007], [0020]-[0021]; Ex.1008B, 387-389; Ex.1003, ¶184. It would have been obvious to apply

Wieczorek's conventional CMOS technology to fabricate known logic devices, including inverters and microprocessors (CPUs), to achieve the benefits of "lower power-dissipation" of CMOS technology in such devices. Ex.1008B, 368-370; Ex.1032, 1334; Ex.1003, ¶184. Wieczorek suggests doing so in teaching the frequent application of its technology to "mode[rn] integrated circuits." Ex.1006, [0004], [0026]; Ex.1003, ¶184. Twin-well CMOS technology was, by the early 2000s, "the dominant CMOS technology in IC production." Ex.1008D, 181; Ex.1003, ¶184.

Using Wieczorek's technology to form logic devices such as CPUs would have merely amounted to combining known, conventional prior art elements (i.e., conventional twin-well CMOS process described in Wieczorek and known digital device designs, including CPUs) according to known methods (i.e., Wieczorek's conventional twin-well CMOS process) and, at most, involves a simple substitution of one known element (CMOS technology for prior art logic devices, including CPUs) with another (Wieczorek's conventional CMOS technology). Ex.1003, ¶187. There would have been a reasonable expectation of success with predictable results because Wieczorek's conventional twin-well CMOS process was a known technique and would have been used for its intended purpose in manufacturing known logic devices, including CPUs, designed for implementation using CMOS technology, in order to achieve the aforementioned benefits. *Id*.

14. Claim 18

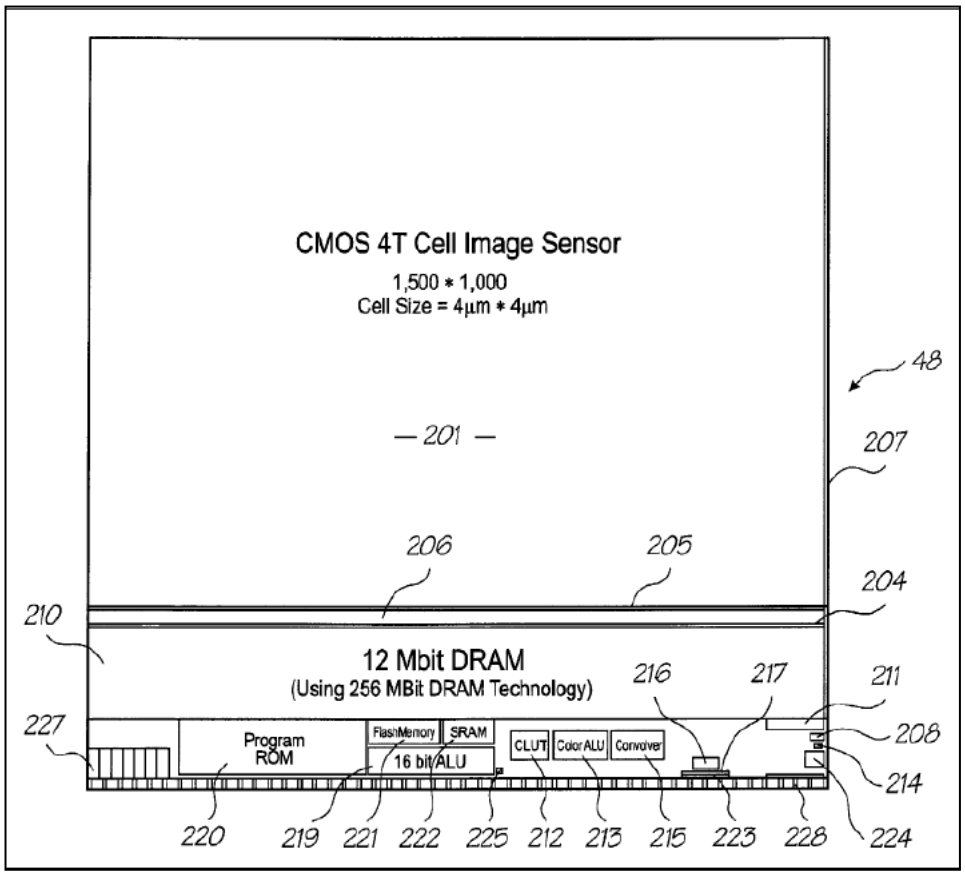
Section X.B.13. A POSITA would have understood that a microprocessor includes a central processing unit (CPU). Ex.1032, 1334; Ex.1003, ¶188.

15. Claim 19

It would have been obvious to a POSITA to implement Wieczorek-Wolf's semiconductor device in an image sensor. Ex.1003, ¶189. Wieczorek's semiconductor device is a CMOS transistor pair. Ex.1006, [0007]. CMOS designs were routinely used in various devices; Wolf noted "CMOS is now the dominant integrated-circuit technology[.]" Ex.1008B, 104. As explained above, Kawagoe teaches that CMOS techniques can be applied to semiconductor integrated circuits with other logic circuits. Section VIII.A.15; Ex.1007, 24:21-31, 19:15-18. A POSITA would have understood that one such application is an image sensor. Ex.1003, ¶189.

> An example of such an image sensor is shown in Silverbrook, pictured below.

Ex.1042, 6:41-13:39, FIG. 15.



Consistent with Kawagoe's hypothesized applications, Silverbrook's image sensor includes "CMOS logic, a CMOS image sensor, DRAM, and analog circuitry." *Id.*, 6:56-57. As such, it would have been obvious to a POSITA that the Wieczorek-Wolf designs could be implemented in an image sensor. Ex.1003, ¶190.

16. Independent Claim 20

a. Preamble

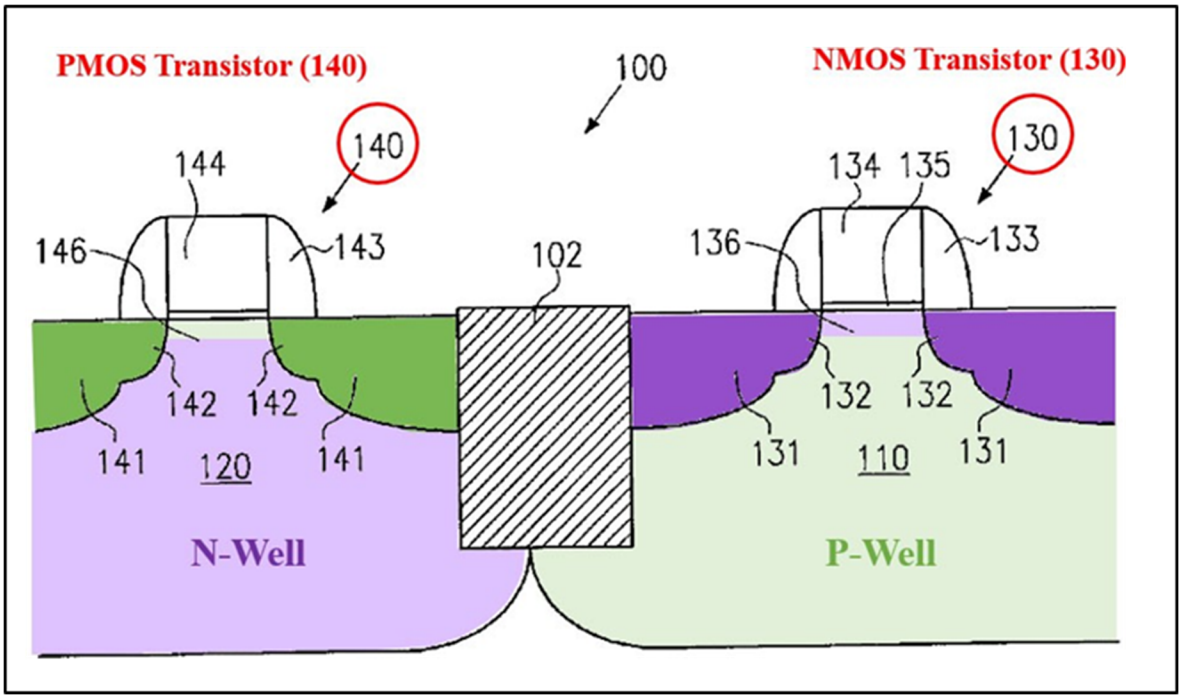
Section X.B.1.a.

b. Element[20.1]

Section X.B.1.b.

c. Element[20.2]

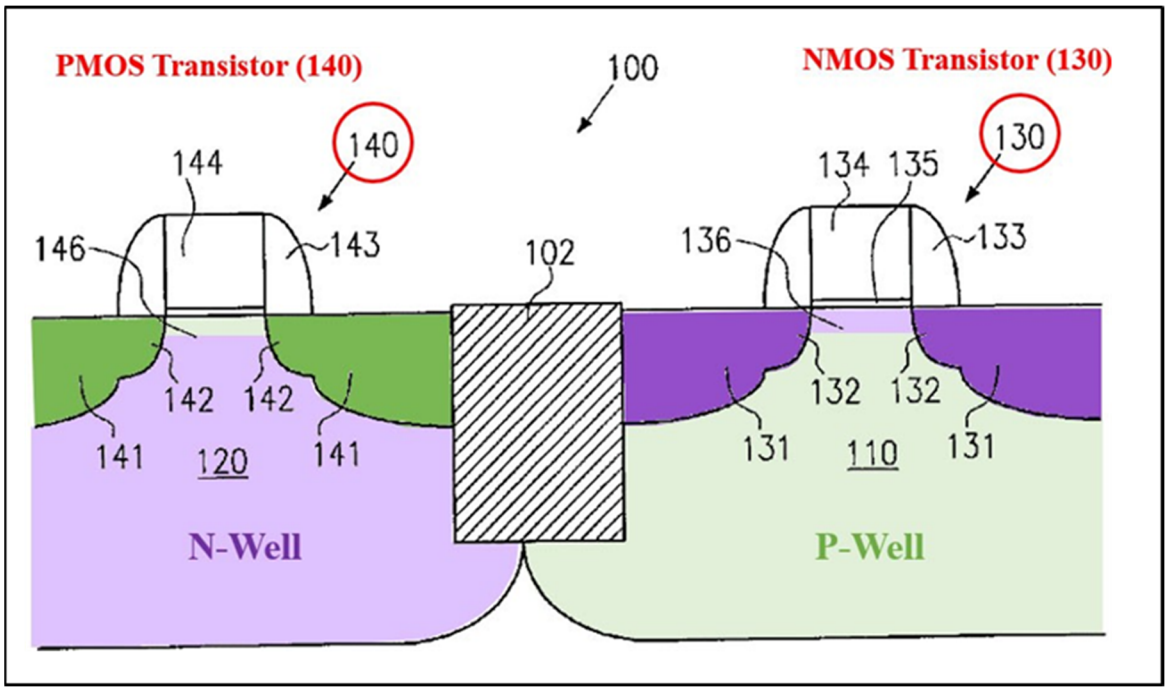
Section X.B.1.c. As shown below, Wieczorek discloses N-channel transistor 130 formed in the surface of the first active region. Ex.1003, ¶193.



Ex.1006, FIG. 1b.

d. Element[20.3]

Section X.B.1.d. As shown below, Wieczorek discloses P-channel transistor 140 formed in the surface of the second active region. Ex.1003, ¶194.



Ex.1006, FIG. 1b.

e. Element[20.4]

Section X.B.1.e.

f. Element[20.5]

Section X.B.1.f.

g. Element[20.6]

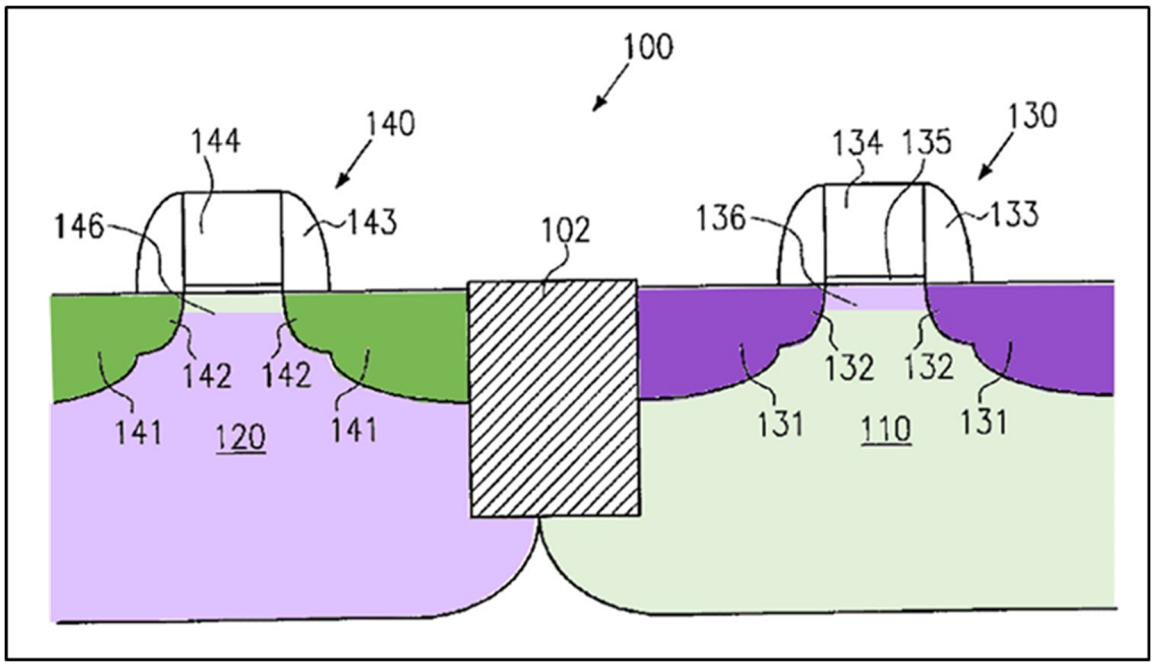
Section X.B.1.g.

17. Claim 21

N-type and p-type substrates are both suitable for Wieczorek's CMOS device. Section X.B.1.b; Ex.1003, ¶198. With an n-type substrate, element[20.2] requiring "a first active region ... with a second doping type opposite in conductivity to the first doping type" of the substrate is met by mapping the

first active region to source/drain/channel regions 141/142/146 (green/light green) of pMOS transistor 140, and element[20.3] is met by mapping the second active region to source/drain/channel regions 131/132/136 (purple/light purple) of nMOS transistor

130. *Id*.



Ex.1006, FIG. 1b.

18. Claim 22

Section X.B.2.

19. Claim 24

Section X.B.3.

20. Claim 25

Section X.B.4.

21. Claim 26

Section X.B.5.

22. Claim 27

Section X.B.8.

23. Claim 30

Section X.B.9.

24. Claim 31

Section X.B.6.

25. Claim 32

Wieczorek teaches a "complementary MOS [(CMOS)] transistor pair" formed in and including a substrate. Ex.1006, [0007], [0012]-[0013]; Ex.1003, ¶206; Section X.B.17.b.

26. Claim 33

Section X.B.13.

27. Claim 34

Section X.B.14.

28. Claim 35

Section X.B.15.

29. Claim 36

Section X.B.16.

C. GROUNDS III/IV

Several claim elements of the Challenged Claims recite "transistors" or "devices." See elements-[1.2]-[1.4], [20.2]-[20.4] and claims 4, 5, 13, 24, 25. As discussed under Grounds I and II, PO interprets these claim elements as requiring one or more transistors, and not a plurality of transistors. Sections X.A.1.c-d, X.B.1.c-d. Notably, according to PO, an "active region ... within which transistors can be formed" means "an active region ... where ***a transistor*** can be formed." Ex.1020, 31.

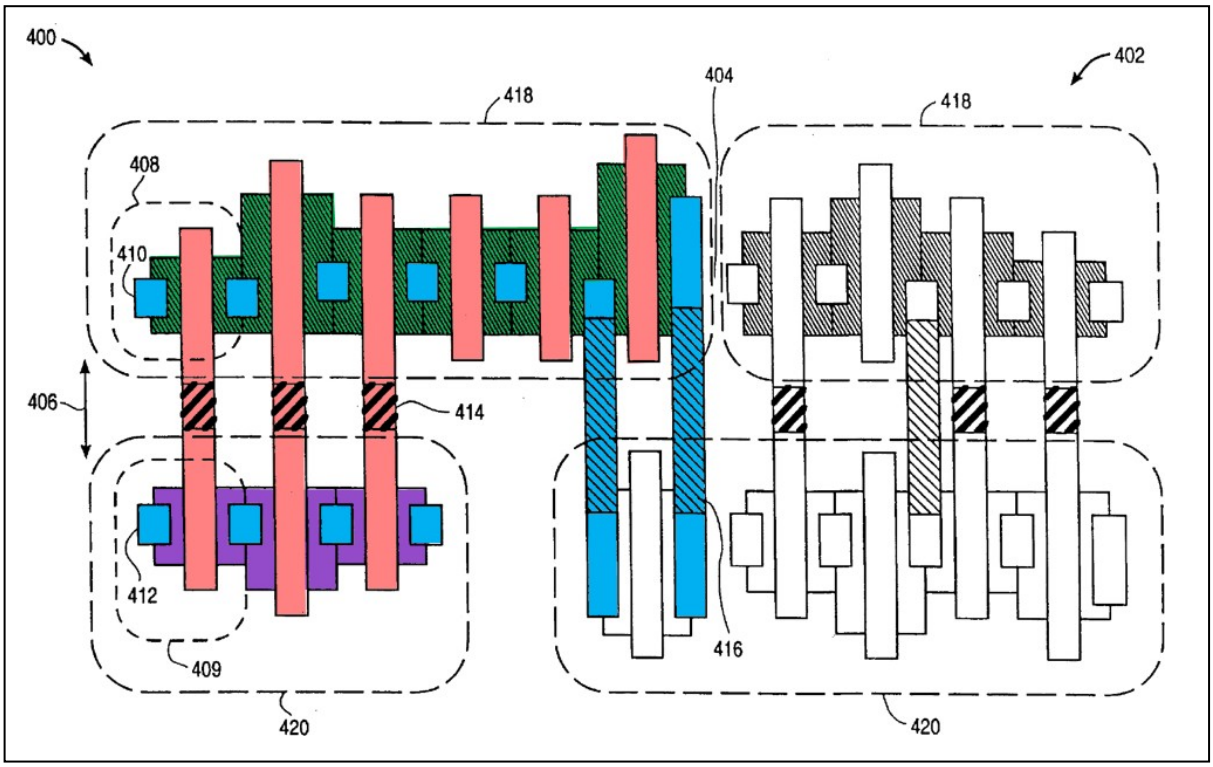
Grounds III and IV mirror grounds I and II, respectively, except that Gupta is explicitly combined with Kawagoe (Ground III) or with Wieczorek-Wolf (Ground IV) to render obvious those claim elements under an interpretation of "transistors" or "devices" to require a plurality of such devices. Ex.1003, ¶211.

Gupta is directed to "automatically producing layouts for CMOS circuits," recognizing that "semiconductor chips [have] become ever larger, incorporating ever more devices." Ex.1014, 1:7-10, 1:28-31. Wolf confirms that, at the time,

various chips (e.g., DRAM, microprocessors, and flash memory) were fabricated with tens of millions to more than a billion devices. Ex.1008A, xxxiii, FIG. 1; Ex.1008B, 634. A "primary goal" of semiconductor chip development has therefore been to minimize the chip area so that more transistors can be packed in the same chip (or so that the same number of transistors can be formed on a smaller chip area), regardless of the technology and chip fabrication process. Ex.1014, 1:28-35 ("[I]t becomes increasingly important to minimize semiconductor area used by a given number of devices. Conservation of semiconductor area is a primary goal in semiconductor chip development ...."); Ex.1003, ¶212. Gupta further explains that good circuit layout practice dictates forming as many transistors in the same active region through diffusion abutment as possible, to minimize area-wasting diffusion gaps. Ex.1014, 1:52-54 ("One technique conserves area by placing transistors so as to ***share diffusion area***."), 2:17-21 ("Transistors which are abutted in a layout form transistor chains. It is desirable to produce a layout with a ***maximum number of transistors chained*** so as to minimize diffusion gaps."); Ex.1023, 5 ("An important layout task is to place and orient the transistors on the chip to ***minimize the layout area***" by avoiding "area-wasting diffusion gap[s]"). Gupta describes several techniques to perform this, such as transistor folding and chaining, to achieve an optimal layout. Ex.1014, 1:49-2:24, 3:64-4:1, FIGS. 2-3.

Gupta's Figure 4 (below)—where transistor gates and metal contacts that

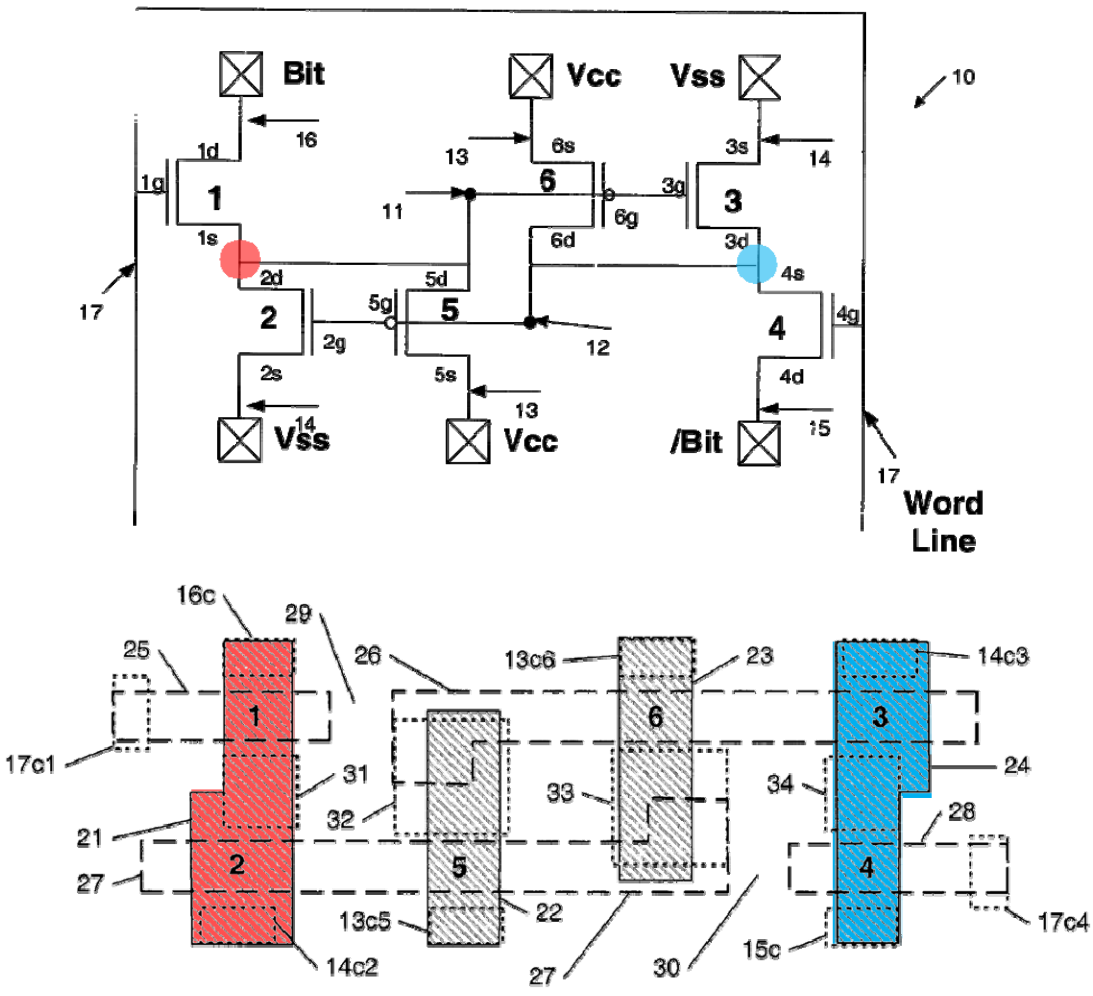
overlay the active regions are colored red and blue, respectively—illustrates ***six*** chained PMOS transistors formed in a p-channel active region (green) and three chained NMOS transistors formed in an n-channel active region (purple). Ex.1014, 4:12-43; Ex.1003, ¶213.



Ex.1014, FIG. 4.

Jin confirms that transistors arranged as in Gupta are formed in a common active region. Ex.1003, ¶214. The first image below is the circuit schematic of a conventional 6T SRAM cell, and the cell layout (second image below) shows transistors 1 and 2 in active region 21 (red), and transistors 3 and 4 in active region 24 (blue). Ex.1015, 6:17-29; Ex.1025, 48 ("Diffusion regions (n+ and p+), which

define the areas where transistors can be formed[,] are often called the active areas.") (italics in original).



Ex.1015, FIGS. 1 and 2.

A POSITA would have been motivated to fabricate a CMOS chip according to the combined teachings of Kawagoe and Gupta (and likewise, of Wieczorek-Wolf and Gupta) to achieve high packing density (taught by Gupta) at submicron dimensions (for which a twin-well CMOS process of the type taught in Kawagoe and Wieczorek-Wolf was known to be the technology of choice (Ex.1008B, 373,

388)). Ex.1003, ¶215. The combinations gain the additional benefit of improved immunity to soft errors through appropriate well doping. Ex.1007, 15:62-16:11 ("the electrons produced by the α–ray are attracted to the substrate body 2S by that concentration gradient and prevented from entering the p-well 6p so that the soft errors can be reduced in case the MIS memory of the DRAM or the like is formed in the p-well 6p"); Ex.1003, ¶216. Combining Gupta with Kawagoe or Wieczorek-Wolf merely amounts to (1) use of a known technique (*i.e.*, Kawagoe's or Wieczorek-Wolf's CMOS fabrication process) to improve similar devices (i.e., CMOS chips designed with Gupta's layout) in the same way (i.e., to achieve submicron dimensions and improve immunity to soft errors); (2) use of a known technique (*i.e.*, Gupta's optimal layout generation) to improve similar devices (*i.e.*, submicron CMOS chips fabricated according to Kawagoe or Wieczorek-Wolf's CMOS fabrication process) in the same way (*i.e.*, to minimize chip area and increase packing density); and (3) combining prior art elements (*i.e.*, Kawagoe or Wieczorek- Wolf's CMOS fabrication process and Gupta's CMOS layout generation) according to known methods (i.e., as taught by Kawagoe or Wieczorek-Wolf and Gupta). Ex.1003, ¶216. There would have been a reasonable expectation of success with predictable results because Kawagoe's and Wieczorek-Wolf's CMOS fabrication process would be used for their intended purpose of fabricating CMOS circuits according to known CMOS layouts generated by Gupta, which would also be used for its intended purpose. *Id*.

Further, Gupta's optimal circuit layout is process- agnostic, and applies to the layout of any CMOS semiconductor chip, including the layout of CMOS chips fabricated according to the teachings of Kawagoe and/or Wieczorek-Wolf. *Id*; Ex.1014, 1:7-10, 3:64-4:11.

A POSITA would have understood that, in such a combination, the active regions in Gupta's figures are formed in wells (n-channel active regions are formed in p-wells, and p-channel active regions are formed in n-wells), whereby the wells have downward-sloping graded dopant concentrations as shown in Kawagoe's Figure 17 and Wieczorek's Figure 2b. *Id*., ¶217 Assuming a p-type substrate is used, the n-channel active region (purple) in Gupta's Figure 4 is an example of the claimed first active region, and the p-channel active region (green) is an example of the claimed second active region. Conversely, if instead an n-type substrate is used, the p-channel active region (green) is an example of the claimed first active region, and the n-channel active region (purple) is an example of the claimed second active region. Ex.1003, ¶216-217. In either case, the two active regions are adjacent and separated by an isolation region (field oxide), as required under elements [1.3], [20.3] and claims 6 and 26. Ex.1014, 1:16-19, 4:23-39; Ex.1008A, 818-820; Sections X.A.1.d, X.A.6, X.B.1.d, X.B.5; Ex.1003, ¶217.

Conversely, a POSITA would have understood that each of the active regions of Kawagoe's and Wieczorek's CMOS devices typically contain many transistors, as taught by Gupta and illustrated in Gupta's Figure 4. Ex.1003, ¶218.

This is the case whether the device is a DRAM, flash memory, logic device or CPU (as claimed in claims 14, 16-18, 33-35). *Id.* Each such device is a "very large scale integrated circuit" for which "it becomes increasingly important to minimize semiconductor area used[,]" and this requires forming as many transistors as possible in any active region. Ex.1014, 1:13-14, 1:28-34, 2:17-21; Ex.1003, ¶218.

Accordingly, Kawagoe in view of Gupta renders claims 1-9, 12-14, 16-27, and 30-36 obvious (Ground III). Ex.1003, ¶¶211-219. Likewise, Wieczorek-Wolf in view of Gupta renders claims 1-2, 4-9, 12-22, 24-27, and 30-36 obvious (Ground IV). *Id.*

D. GROUNDS V/VI

Claims 19 and 36 recite "[t]he semiconductor device of claim [1/20], wherein the device is an image sensor." As discussed under Grounds I-II, it would be obvious to a POSITA to implement either the CMOS designs in Kawagoe (VIII.A.15) or in Wieczorek-Wolf (VIII.B.15) in an image sensor.

Grounds V-VI mirror Grounds I-II, respectively, except that Silverbrook is explicitly combined with Kawagoe (Ground V) or Wieczorek-Wolf (Ground VI) to render obvious the implementation of the disclosed design in an image sensor. Both Kawagoe and Wieczorek-Wolf expressly disclose CMOS designs (Ex. 1007, 14:46- 19:64; Ex. 1006, [0007]-[0014]), and Silverbrook discloses a "CMOS image sensor." Ex.1042, 6:41-67. Because Silverbrook calls for a "CMOS" image sensor, but does not include any details about the fabrication of CMOS devices, a

POSITA would have been motivated to implement the CMOS device designs disclosed by Kawagoe and Wieczorek-Wolf, respectively. Ex.1003, ¶221. Silverbrook expressly seeks incorporation of existing CMOS designs into its image sensor device, highlighting that "[t]he CPU, DRAM, Image Sensor, ROM, Flash memory … can be vendor supplied cores." Ex.1042, 7:28-30; *see also* Ex.1044, 1, Fig. 2. Using the CMOS device designs from Kawagoe and Wieczorek-Wolf in Silverbrook's CMOS image sensor would have been nothing more than the "combination of familiar elements according to known methods […] yield[ing] predictable results." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). Accordingly, a POSITA would have had a reasonable expectation of success in combining the CMOS designs from Kawagoe and Wieczorek-Wolf with Silverbrook's CMOS image sensor. Ex.1003, ¶221.

Thus, claims 19 and 36 are rendered obvious by Kawagoe in view of Silverbrook (Ground V) and also by Wieczorek-Wolf in view of Silverbrook (Ground VI). Ex.1003, ¶221.

XI. THE BOARD SHOULD INSTITUTE IPR

The Board should decline to exercise its discretion to deny institution for several reasons.

A. 35 U.S.C. § 314(a)

In *Apple Inc. v. Fintiv, Inc*., the Board enumerated six factors that it will assess in determining whether to exercise discretion to deny institution under §314(a) based

on co-pending litigation. IPR2020-00019, Paper 11 at 2-3 (PTAB "precedential" Mar. 20, 2020). The USPTO issued updated discretionary denial guidance in view of the *Fintiv* factors and confirmed that "the PTAB will not discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB." *See* June 21, 2022 Memorandum to Members of the PTAB, 3 (available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf). Here, Petitioner has eliminated any risk of duplicated effort by voluntarily presenting a *Sotera* stipulation to Patent Owner. EX1101; *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020). For at least this reason, and considering the compelling merits of the above-detailed Grounds, discretionarily denial is unwarranted and would be unjust.

B. 35 U.S.C. § 325(d)

The Board should likewise not deny institution under §325(d) because the two-part *Advanced Bionics* framework is not satisfied. *See Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper No. 6 at 8 (P.T.A.B. Feb. 13, 2020) (precedential). Under that framework, in evaluating discretionary denial arguments under §325(d), the Board looks to "(1) whether the same or substantially the same art previously was presented to the Office or

whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims." *Id*.

In applying this test, the PTAB considers the "*Becton, Dickinson*" factors.[10] Among these are "the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection," *Becton, Dickinson*, Paper No. 8 at 17-18; *see also Edwards Life Sciences Corp. v. Colibri Heartinvalve, LLC*, IPR2020-01649, Paper No. 8 at 20-21 (P.T.A.B. Mar. 26, 2021) (declining to exercise discretionary denial where prior art references were not substantively considered during prosecution). Here, the prior art references (Kawagoe, Wieczorek, Wolf, Gupta, and Silverbrook) are not cited in the '481 Patent, and the arguments presented herein are not the same or substantially the same as those considered during prosecution of the '481 Patent. Kawagoe is in fact not cited in any patent related to the '481 Patent. Wieczorek was first disclosed (but not discussed) during prosecution of a later-filed application, after the '481 Patent was allowed. Ex.1033, 2, 5. Additionally, none of the grounds in this

[10] *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (Dec. 15, 2017) (precedential as to § III.C.5, first paragraph) ("*Becton, Dickinson*").

Petition rely on prior art that was evaluated during prosecution of the ’481 Patent.

Wieczorek and Kawagoe are also not cumulative of references considered during prosecution of the ’481 Patent. Hong, the only reference applied to reject the claims pending during prosecution of the ’481 Patent, is not prior art because it claims priority to August 31, 2005, long after the claimed priority date of the ’481 Patent. Ex.1027; Ex.1002, 81-83. Further, Wieczorek and Kawagoe are not cumulative to any art cited or discussed during prosecution of the ’481 Patent’s parents, such as Rhodes, Jastrzebski, Kamins or Hueting. Indeed, other than prosecution of the parent ’842 Patent during which the non-prior-art Hong was also the only reference discussed, prosecution of the other parent applications involves claims that are substantially different from the Challenged Claims. *Fasteners for Retail, Inc. v. RTC Indus., Inc.,* IPR2019-00994, Paper 9 at 10 (P.T.A.B. Nov. 5, 2019) (refusing to deny institution because, despite allegation that the petition art was considered during prosecution of claims related to the challenged claims, “enough differences exist [between the two sets of claims] to convince us that the challenges presented in this petition are not cumulative to those already considered by the examiner.”). Most significantly, none of the claims prosecuted in the parent applications (other than the ’842 Patent) claim graded dopants ***in an active region*** to aid carrier movement “***to the second surface of the substrate***” as recited in the Challenged Claims. For example, the claims of

the parent '070 Patent are directed to bipolar transistors (not at issue in the present Petition) and claim aiding carrier movement "to a collector in the substrate," and not "to the second surface of the substrate." Ex.1034, Cl. 1; Ex.1003, ¶43. Other claims that claim graded dopant in an active region were withdrawn prior to substantive examination. Ex.1016, 73 (withdrawing claims 1-2); Ex.1028, 9 (same); Ex.1029, 7 (canceling claims 1-2); Ex.1030, 18 (same); Ex.1003, ¶43. Accordingly, there is no overlap between arguments made during prosecution and Petitioner's obviousness challenge here. *See Becton, Dickinson*, Paper No. 8 at 17-18.

C. Prior Terminated Petitions Do Not Warrant Denying Institution

The instant Petition is Petitioner's first petition challenging claims of the '481 Patent. Petitioner is not a related company to those who have previously challenged the '481 Patent. None of the prior challenges to the '481 Patent reached an institution decision. In addition, Petitioner is a defendant in the District Court Case, and Petitioner would potentially be severely prejudiced if this Petition is not instituted. *Apple Inc. v. Uniloc 2017 LLC*, IPR2019-01667, Paper No. 7, 11-12 (P.T.A.B. Apr. 21, 2020). In light of the foregoing, *General Plastic* factors weigh strongly against discretionary denial. *Xilinx, Inc. v. Arbor Global Strategies, LLC*, IPR2020-01568, Paper No. 12 at 10 (P.T.A.B. Mar. 5, 2021).

Respectfully submitted,

Dated April 10, 2024

/Patrick J. Bisenius/

Joshua A. Griswold, Reg. No. 46,310
Patrick J. Bisenius, Reg. No. 63,893
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
T: 214-292-4034
F: 877-769-7945

(Control No. IPR2024-00772)

Attorneys for Petitioner

APPENDIX A

Element	Claim Language
[1.pre]	"A semiconductor device, comprising"
[1.1]	"a substrate of a first doping type at a first doping level having first and second surfaces;"
[1.2]	"a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed;"
[1.3]	"a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed;"
[1.4]	"transistors formed in at least one of the first active region or second active region;"
[1.5]	"at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the first surface to the second surface of the substrate; and"
[1.6]	"at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate."
2	The semiconductor device of claim 1, wherein the substrate is a p-type substrate.
3	The semiconductor device of claim 1, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.
4	The semiconductor device of claim 1, wherein the first active region and second active region contain one of either p-channel and n-channel devices.
5	The semiconductor device of claim 1, wherein the first active region and second active region contain either p-channel or n-

Element	Claim Language
	channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.
6	The semiconductor device of claim 1, wherein the first active region and second active region are each separated by at least one isolation region.
7	The semiconductor device of claim 1, wherein the graded dopant is fabricated with an ion implantation process.
8	The semiconductor device of claim 1, wherein the first and second active regions are formed adjacent the first surface of the substrate.
9	The semiconductor device of claim 1, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.
12	The semiconductor device of claim 1, wherein dopants of the graded dopant region in the well region are both p-type and n-type.
13	The semiconductor device of claim 1, wherein the transistors which can be formed in the first and second active regions are CMOS transistors requiring at least a source, a drain, a gate and a channel.
14	The semiconductor device of claim 1, wherein the device is a dynamic random access memory (DRAM).
15	The semiconductor device of claim 1, wherein the device is a complementary metal oxide semiconductor (CMOS) with a nonepitaxial substrate.
16	The semiconductor device of claim 1, wherein the device is a flash memory.
17	The semiconductor device of claim 1, wherein the device is a logic device.

Element	Claim Language
18	The semiconductor device of claim 17, wherein the device is central processing unit.
19	The semiconductor device of claim 1, wherein the device is an image sensor.
[20.pre]	A semiconductor device, comprising:
[20.1]	a substrate of a first doping type at a first doping level having first and second surfaces;
[20.2]	a first active region disposed adjacent the first surface of the substrate with a second doping type opposite in conductivity to the first doping type and within which transistors can be formed in the surface thereof;
[20.3]	a second active region separate from the first active region disposed adjacent to the first active region and within which transistors can be formed in the surface thereof;
[20.4]	transistors formed in at least one of the first active region or second active region;
[20.5]	at least a portion of at least one of the first and second active regions having at least one graded dopant concentration to aid carrier movement from the surface to the substrate; and
[20.6]	at least one well region adjacent to the first or second active region containing at least one graded dopant region, the graded dopant region to aid carrier movement from the first surface to the second surface of the substrate.
21	The semiconductor device of claim 20, wherein the substrate is an n-type substrate.
22	The semiconductor device of claim 20, wherein the substrate is a p-type substrate.
23	The semiconductor device of claim 20, wherein the substrate has epitaxial silicon on top of a nonepitaxial substrate.

Element	Claim Language
24	The semiconductor device of claim 20, wherein the first active region and second active region contain at least one of either p-channel and n-channel devices.
25	The semiconductor device of claim 20, wherein the first active region and second active region contain either p-channel or n-channel devices in n-wells or p-wells, respectively, and each well has at least one graded dopant.
26	The semiconductor device of claim 20, wherein the first active region and second active region are each separated by at least one isolation region.
27	The semiconductor device of claim 20, wherein dopants of the graded dopant concentration in the first active region or the second active region are either p-type or n-type.
30	The semiconductor device of claim 20, wherein dopants of the graded dopant region in the well region are both p-type and n-type.
31	The semiconductor device of claim 20, wherein the graded dopant is fabricated with an ion implantation process.
32	The semiconductor device of claim 20, wherein the substrate is a complementary metal oxide semiconductor (CMOS) device.
33	The semiconductor device of claim 20, wherein the device is a flash memory.
34	The semiconductor device of claim 20, wherein the device is a logic device.
35	The semiconductor device of claim 34, wherein the device is central processing unit.
36	The semiconductor device of claim 20, wherein the device is an image sensor.

CERTIFICATION OF WORD COUNT

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,617 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated April 10, 2024

/Patrick J. Bisenius/

Joshua A. Griswold, Reg. No. 46,310
Patrick J. Bisenius, Reg. No. 63,893
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
T: 214-292-4034
F: 877-769-7945

Attorneys for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on April 10, 2024, a complete and entire copy of this Petition for *Inter partes* Review, Power of Attorney, and all supporting exhibits was provided by Express Mail, to the Patent Owner, by serving the correspondence address of record as follows:

Munck Wilson Mandala LLP
P.O. Drawer 800889
Dallas, TX 75380

/Anastasia Renard/
Anastasia Renard
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
612-204-4675