

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CIRRUS LOGIC, INC.;
OMNIVISION TECHNOLOGIES, INC.; AND
AMS SENSORS USA INC.,
Petitioner,

v.

GREENTHREAD LLC,
Patent Owner

U.S. PATENT NO. 9,190,502

Case IPR2024-00018

**DECLARATION OF DR. SANJAY BANERJEE IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,190,502**

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I, Dr. Sanjay Banerjee, declare as follows:

1. My name is Sanjay Banerjee.

2. I have been retained as an expert witness on behalf of Cirrus Logic, Inc., OmniVision Technologies, Inc., and ams Sensors USA, Inc. (collectively, “Petitioner”) for the above-captioned Petition for *Inter Partes* Review (“Petition”) of U.S. Patent No. 9,190,502 (the “’502 Patent”) (Ex. 1001). I am being compensated for my time in connection with this Petition at my standard consulting rate of \$675 per hour. My compensation is not affected by the outcome of, or my testimony in, this *Inter Partes* Review, or any litigation proceedings. I am informed that the assignee for the patent in the present proceeding is Greenthread, LLC (“Patent Owner”). I am also informed that the Petition names Cirrus Logic, OmniVision, ams Sensors USA, OSRAM GmbH, ams-OSRAM AG, and GlobalFoundries U.S., Inc. as real-parties-in-interest.

3. I have been asked to provide my opinions regarding whether claims 7-12 of the ’502 Patent (the “Challenged Claims”) are invalid as anticipated, or as obvious to a person having ordinary skill in the art at the time of the alleged invention. In connection with this effort, I have reviewed a declaration provided in connection with another *Inter Partes Review* Petition filed against the ’502 Patent (specifically, Ex. 1003 in IPR2023-00541 filed on behalf of Petitioner Intel Corporation). After having conducted my own independent analysis on the ’502

Patent, I concur with the analysis provided in that declaration. For efficiency, I have excerpted portions of that declaration in drafting this declaration.

4. The '502 Patent issued on November 17, 2015, from Application No. 14/515,584, filed on October 16, 2014. The '502 Patent claims priority to Application No. 10/934,915, filed on September 3, 2004.

5. I am not currently, and have not at any time in the past been, an employee of any Petitioner or Real-party-in-interest. Other than set out above, I have no affiliation, contractual connection, or financial connection with any Petitioner or Real-party-in-interest, or any of their respective subsidiaries or parents. I similarly have no financial interest in, or affiliation with the Patent Owner.

I. BACKGROUND AND QUALIFICATIONS

6. I am currently the Cockrell Family Chair Professor of Electrical and Computer Engineering at the University of Texas at Austin. At UT Austin, I am also the director of the Microelectronics Research Center. I have been a faculty member at UT Austin since 1987.

7. I have also been active in industries related to the relevant field of art. As a Member of the Technical Staff, Corporate Research, Development and Engineering of Texas Instruments Incorporated from 1983–1987, I worked on polysilicon transistors and dynamic random access trench memory cells used by

Texas Instruments in the world's first 4-Megabit DRAM, for which I was co-recipient of the Best Paper Award, IEEE International Solid State Circuits Conference, 1986.

8. I received a B. Tech. degree from the Indian Institute of Technology, Kharagpur, and M.S. and Ph.D. degrees from the University of Illinois at Urbana-Champaign, all in Electrical Engineering.

9. I am a leading researcher and educator in various areas of transistor device fabrication technology, including the fabrication, characterization and application of memory devices, transistors, and nanotechnology. My research has been funded by the Texas Advanced Technology Program (ATP), the Texas Higher Education Coordinating Board, the National Science Foundation, the SEMATECH (Semiconductor Manufacturing Technology) consortium, the SRC (Semiconductor Research Corporation) consortium, DARPA, and the Department of Energy, among others.

10. At the University of Texas, I am the director of the Microelectronics Research Center, comprised of faculty colleagues, graduate, and undergraduate students. I also served as the director of the South West Academy of Nanoelectronics from its inception through the end (Dec. 2017), one of three centers in the United States established to develop a replacement for MOSFETs.

11. I have published over 1,200 technical articles, many related to semiconductor fabrication technology, most at highly competitive refereed conferences and rigorously reviewed journals. I have also published 8 books or chapters on transistor device physics and fabrication, and have supervised over 50 Ph.D. and 60 MS students.

12. I have been a member of scientific organizations and committees, including the IEEE Dan Noble Award Committee from 2010–2013, serving as Chair from 2012–2013, the International Technology Roadmap for Semiconductors, the International Conference on MEMS (Microelectromechanical Systems) and Nanotechnology, the IEEE International Conference on Communications, Computers, Devices, the International Electron Devices Meeting, the International Conference on Simulation of Semiconductor Processes and Devices, and the IEEE Symposium on VLSI (Very-Large-Scale Integration) Technology. I have served as the Session Chair for the “Device Technology” Session conducted at the IEEE International Electron Devices Meeting in 1989–1990. I have also served as the General Chairman for the IEEE University Government Industry Microelectronics Symposium in 1994–1995, and Chair of the IEEE Device Research Conference.

13. I have served on the Technical Advisory Boards of AstroWatt, DSM Semiconductors, Cambrios, Nanocoolers Inc., BeSang Memories, Organic ID and

ITU Ventures; Gerson Lehmann Group, NY; Austin Community College; Asia Pacific IIT; Rochester Institute of Technology, and HSMC Foundry.

14. I received the Engineering Foundation Advisory Council Halliburton Award (1991), the Texas Atomic Energy Fellowship (1990–1997), Cullen Professorship (1997–2001) and the Hocott Research Award from UT Austin (2007). I also received the IEEE Grove Award (2014), Distinguished Alumnus Award, IIT (2005), Industrial R&D 100 Award (2004), ECS Callinan Award, 2003, IEEE Millennium Medal, 2000, NSF Presidential Young Investigator Award in 1988, and several SRC Inventor Recognition and Best Paper Awards. I was a Distinguished Lecturer for IEEE Electron Devices Society, and am a Fellow of the Institute of the Electrical and Electronics Engineers (IEEE), the American Physical Society (APS) and the American Association for the Advancement of Science (AAAS).

15. I am the inventor or co-inventor of over 35 United States patents in various areas of transistor device fabrication technology. I was elected a Fellow of the National Academy of Inventors in 2021.

16. My qualifications and publications are set forth more fully in my curriculum vitae, attached as Ex. 1004.

II. MATERIALS AND OTHER INFORMATION CONSIDERED

17. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art and have considered the viewpoint of a person having ordinary skill in the art (POSITA) at the time of the alleged invention.

18. I have considered the materials referenced herein, including the '502 Patent (Ex. 1001), the file history of the '502 Patent (Ex. 1002), the parent and related applications, the file histories of the parent and related applications, the Petition, and other documents listed in the Exhibit List of the Petition, including:

Description	Date of Public Availability
U.S. Patent No. 4,684,971 to Payne ("Payne") (Ex. 1005)	Filed March 13, 1981 and issued August 4, 1987.
U.S. Patent No. 4,907,058 to Sakai ("Sakai") (Ex. 1006)	Filed July 1, 1988 (with priority to July 3, 1987) and issued on March 6, 1990.
U.S. Patent No. 6,043,114 to Kawagoe, et al. ("Kawagoe") (Ex. 1007)	Filed on September 22, 1997 (with priority to July 28, 1995) and issued on March 28, 2000.
Wolf and Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol 1, Lattice Press (2000) ("Wolf.1") (Ex. 1008A)	Published and publicly available no later than 2002.
Wolf and Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol. 2, Lattice Press (2000) ("Wolf.2") (Ex. 1008B)	Published and publicly available no later than 2002.
Wolf and Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol. 3, Lattice Press (2000) ("Wolf.3") (Ex. 1008C)	Published and publicly available no later than 2002.

Wolf and Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol. 4, Lattice Press (2000) (“Wolf.4”) (Ex. 1008D)	Published and publicly available no later than 2002.
U.S. Patent No. 4,160,985 to Kamins <i>et al.</i> (“Kamins”) (Ex. 1009)	Filed November 25, 1977 and issued July 10, 1979.
U.S. Patent No. 4,014,522 (“Jastrzebski”) (Ex. 1010)	Filed March 24, 1982 and issued on November 6, 1984.
U.S. Patent Application Publication No. 2003/0042511 (“Rhodes”) (Ex. 1011)	Filed on August 30, 2001.
U.S. Patent Application Publication No. 2002/0102783 (“Fujimoto”) (Ex. 1012)	Filed on October 24, 2001 (with priority to October 26, 2000).
Wang and Agrawal, <i>Single Event Upset: An Embedded Tutorial</i> , 21 st Intl Conf on VLSI Design, IEEE 2008 (“Wang”) (Ex. 1013)	Published and publicly available in 2008.
U.S. Patent Application Publication No. 2004/0063288 (“Kenney”) (Ex. 1022)	Published and publicly available in 2004.
Jaeger, <i>Introduction to Microelectronic Fabrication</i> , Vol. V, Addison-Wesley Modular Series on Solid State Devices (1988) (“Jaeger”) (Ex. 1023)	Published and publicly available in 1988.
U.S. Patent No. 4,435,896 (“Parrillo”) (Ex. 1025)	Filed on June 29, 1983 (with priority to December 7, 1981) and issued on March 13, 1984.
L.C. Parrillo, R.S. Payne et al., <i>Twin-Tub CMOS - A Technology for VLSI Circuits</i> , IEEE 1980 (“Parrillo2”) (Ex. 1026)	Published and publicly available in 1980.
U.S. Patent Application Publication No. 2007/0045682 to Hong <i>et al.</i> (“Hong”) (Ex. 1027)	Filed on August 31, 2005.

The Oxford American Dictionary and Language Guide, Oxford University Press (1996) (Ex. 1028)	Published and publicly available in 1996.
U.S. Patent Application Publication No. 2003/0183856 to Wieczorek (“Wieczorek”) (Ex. 1038)	Filed on October 29, 2002 (with priority to March 28, 2002).
Dictionary of Scientific and Technical Terms, McGraw Hill (2003) (Ex. 1040)	Published and publicly available in 2003.
Japanese Unexamined Patent Application Publication No. H8-279598 (“Onoda”) (Ex. 1043, certified translation Ex. 1042)	Date of application April 7, 1995 and publication date October 22, 1996.
U.S. Patent No. 6,614,560 to Silverbrook (“Silverbrook”) (Ex. 1047)	Filed July 10, 1998 and issued September 2, 2003.
U.S. Patent No. 5,986,924 (“Yamada”) (Ex. 1049)	Filed June 24, 1998 (with priority to June 25, 1997) and issued November 16, 1999.
Rabaey <i>et al.</i> , <i>Digital Integrated Circuits, A Design Perspective</i> , Prentice Hall Electronics and VLSI Series (2003) (“Rabaey”) (Ex. 1050)	Published and publicly available in 2003.
Sze, <i>Semiconductor Devices Physics and Technology</i> , 2d Ed., John Wiley & Sons (2002) (Ex. 1051)	Published and publicly available in 2002.
Maziasz and Hayes, <i>Layout Minimization of CMOS Cells</i> , Kluwer Academic Publishers (1992) (“Maziasz”) (Ex. 1054)	Published and publicly available in 1992.

19. The references listed above include prior art to the '502 Patent which is entitled to a priority date not earlier than September 3, 2004. I am also relying on the declaration of Dr. Sylvia Hall-Ellis who opined that the Wolf reference was publicly available before September 3, 2004. Payne, Onoda and Wolf.1-4 (Exs. 1008A-D) were not cited during the prosecution of the '502 Patent.

III. UNDERSTANDING OF PATENT LAW

20. I am not an attorney. For purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

A. Claim Construction

21. I understand that in an IPR petition filed after November 13, 2018, a claim must be construed under the *Phillips* standard. Under that standard, words of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent.

B. Anticipation and Obviousness

22. I have been informed that a patent claim is anticipated if a single prior art reference, such as a patent or a publication, discloses all the elements of the claimed invention.

23. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

24. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;

- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known elements in the manner described in the claim;
- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

25. I understand that a POSITA has ordinary creativity, and is not an automaton.

26. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

27. I understand that prior art to the '502 Patent includes patents and printed publications in the relevant art that predate the Priority Date of the '502 Patent.

28. I understand that certain factors—often called “secondary considerations”—may support or rebut an assertion of obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged

invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field.

29. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

C. Cumulativeness

30. I understand that, under 35 U.S.C. § 325(d), the Board may exercise its discretion to deny institution of *inter partes* review if the IPR petition presents the same or substantially the same prior art or arguments that were previously presented to the Patent Office.

31. When deciding whether to exercise its discretion to deny institution under 35 U.S.C. § 325(d), I understand the Board weighs several non-exclusive factors, including:

- (a) the similarities and material differences between the asserted art and the prior art involved during examination;
- (b) the cumulative nature of the asserted art and the prior art evaluated during examination;

- (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;
- (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;
- (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and
- (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

IV. SUMMARY OF OPINIONS

32. It is my opinion that claim 7 is disclosed or, at a minimum, rendered obvious by Payne (Ground I).

33. It is my opinion that claims 7, 8, and 11 are anticipated by Onoda (Ground II) or rendered obvious by Onoda (Ground III).

34. It is my opinion that claim 8 is rendered obvious by Payne in combination with Parrillo (Ground IV).

35. It is my opinion that claims 9-11 are rendered obvious by Payne in view of Wolf (Ground V).

36. It is my opinion that claims 9 and 10 are rendered obvious by Onoda in view of Wolf (Ground VI).

37. It is my opinion that claim 12 is rendered obvious by Payne in combination with Silverbrook (Ground VII).

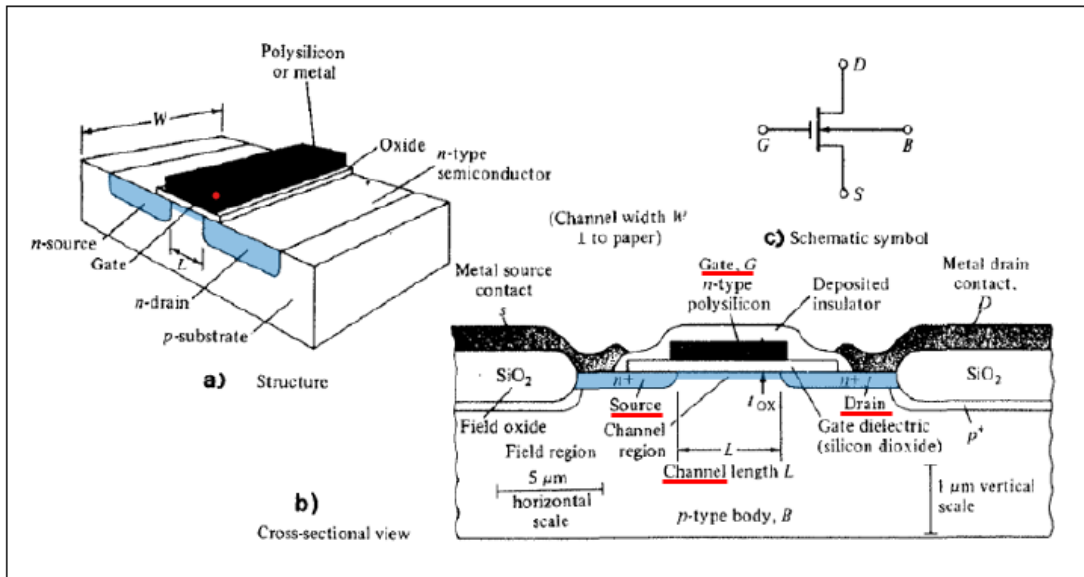
38. It is my opinion that claim 12 is rendered obvious by Onoda in combination with Silverbrook (Ground VIII).

39. It is my opinion that none of the prior art references relied on in this petition are cumulative with prior art considered by the Examiner during prosecution of the '502 Patent.

40. It is my opinion that for purposes of this proceeding, the claim terms need not be construed to resolve the prior art issues presented in this Petition.

V. OVERVIEW OF THE TECHNOLOGY

41. A Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a transistor that switches from an OFF state to an ON state when a voltage is applied to a gate terminal. Ex. 1008B, 402. In the ON, or active state, current flows from a source to a drain through a channel region (the length of such channel region is labelled "L" below). The channel region is under the gate and gate oxide, and between the source and drain.

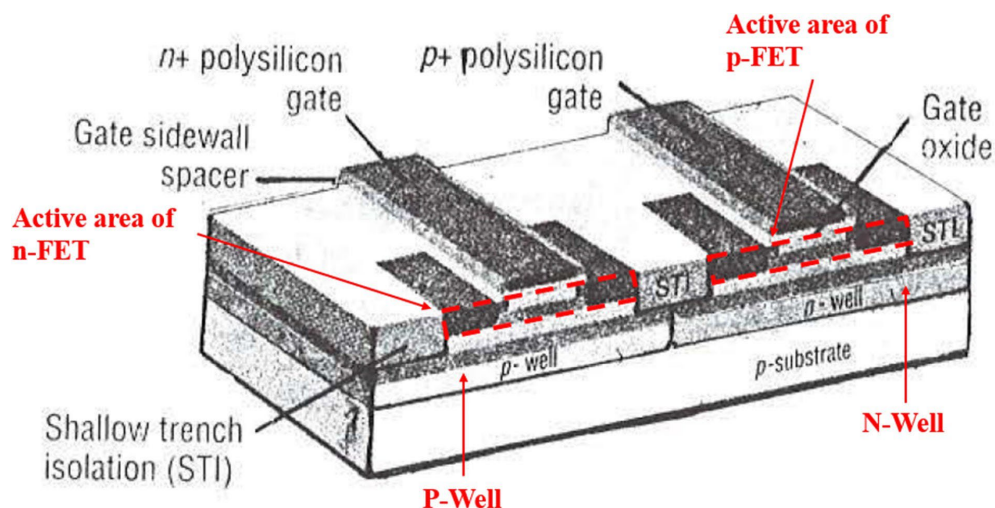


Ex. 1008B, FIG. 5-1 (annotations in red);¹ *id.*, 298-301, FIGS. 5-2, 6-4. The combination of the source, drain, and channel regions of a transistor may be an example of an active region, as Wolf teaches. Ex. 1008B, 299-300 (“The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The active regions are those in which transistor action occurs; i.e., the channel and the heavily doped source and drain regions.”), FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e).

42. MOSFETs are characterized by the material used in the source and drain. A MOSFET with source/drain regions made from “p-type” material in such areas (as shown in the figure above, labelled “p⁺”) is known as a PMOS or p-FET, while a MOSFET with source/drain regions made from “n-type” material (“n⁺”) in

¹ All emphases and annotations added unless otherwise noted.

such areas is known as a NMOS or n-FET. In the mid-1980s, Complementary MOS (CMOS) devices became popular, which have both PMOS (p-FET) and NMOS (n-FET) transistors on the same substrate or integrated circuits (ICs). In such devices, the active areas (and associated transistors) are generally formed in regions called “wells.” Impurities known as “dopants” are added to the active areas and wells to add charge carriers and tailor the electrical properties of these regions such as their conductivity. The wells have opposite dopant type to the dopants of the source/drain. As illustrated below, an n-FET is formed in a p-well, and a p-FET is formed in an n-well.



Ex. 1008A, FIG. 16-28 (annotations in red).

43. With respect to dopants, charge carriers can be electrons (which are negatively charged) or holes (which are positively charged). Ex. 1008C, 86. When a region is doped with p-type dopants, the holes are majority carriers and the electrons are minority carriers. Ex. 1008C, 86. When a region is doped with n-

type dopants, the electrons are majority carriers and the holes are minority carriers. Ex. 1008C, 86.

44. A “dopant profile” refers to the “map” of concentration of dopants over a doped region and, in certain simplified scenarios, can be expressed as a function of depth. For example, a dopant concentration that does not change with depth is a uniform concentration. A non-uniform dopant concentration that varies for example with depth, *e.g.*, increases or decreases with depth, is a non-uniform dopant concentration called “graded.” A graded dopant concentration that peaks at some depth of the doped region(s) instead of at the top or bottom of the doped region(s) is called “retrograde.” In my opinion, all such doping profiles were known in the art.

VI. THE '502 PATENT

45. The '502 Patent issued on November 17, 2015, from Application No. 14/515,584, filed on October 16, 2014. The '502 Patent claims priority to Application No. 10/934,915, filed on September 3, 2004. Ex. 1001, cover.

A. Claims

46. The '502 Patent has 12 claims, including two independent claims numbered 1 and 7. Ex. 1001, 4:23-5:12. Claims 7-12 are the Challenged Claims.

47. Exemplary Claim 7 is reproduced below:

7. A semiconductor device comprising:

a surface layer;

a substrate;

an active region including a source and a drain, disposed on one surface of said surface layer;

a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and

at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

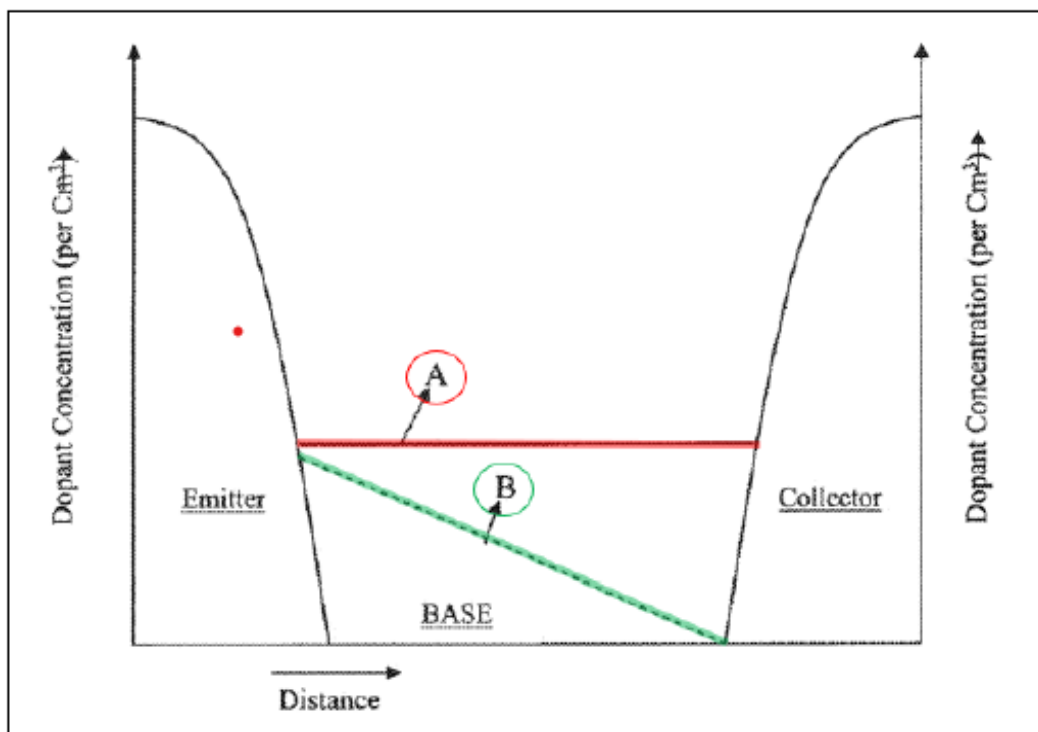
Ex. 1001, 4:24-39.

B. Summary of the Specification

48. The '502 Patent is directed to “grading the dopant concentration” in certain regions of a semiconductor device. Ex. 1001, Title, Abstract. The Challenged Claims claim that a single drift layer and a well region of a semiconductor device have graded dopant concentrations to aid movement of minority carriers from the surface layer to the substrate. *Id.*, Cl. 7. I understand that those claims are asserted against CMOS products in *Greenthread, LLC v. Cirrus Logic, Inc.*, 1:23-cv-00369 (W.D. Tex., filed March 31, 2023), *Greenthread, LLC v. OSRAM GmbH*, 2:23-cv-00179 (E.D. Tex., filed Apr. 19, 2023), and *Greenthread, LLC v. OmniVision Technologies, Inc.*, 2:23-cv-00212 (E.D. Tex., filed May 10, 2023) (collectively, “District Court Cases”). In my opinion, a

majority of the references relied on in the Petition (*i.e.*, Payne, Onoda and Wolf) are also directed to CMOS devices and technology.

49. A bipolar junction transistor (BJT) is a type of transistor that, unlike a FET, uses both electrons and holes as charge carriers. *See, e.g.*, Ex. 1001, 1:27-50. The '502 Patent admits that graded dopant concentrations were known. For example, the graded dopant concentration “B” (green) in Figure 1 below is described as one of “the two most popular” doping profiles used in prior art bipolar transistors, in contrast to the uniform doping profile “A” (red). Ex. 1001, 2:17-19.



Id., FIG. 1 (“Prior Art”).² The ’502 Patent further admits that it was known to grade the dopant concentration in well regions of CMOS devices to affect the movement of carriers, but alleges, without support, that prior attempts were met with “little success.” *Id.*, 1:38-2:9.

50. The ’502 Patent explains that “[r]etrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits.” Ex. 1001, 1:63-65. The ’502 Patent further states that “[r]etrograde and halo wells have also been attempted to improve refresh time in DRAM’s (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs.” *Id.*, 2:1-6.³

51. The ’502 Patent also explains that “these techniques” in the prior art “either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.” *Id.*, 2:6-9.

² All colors and colored annotations to figures added.

³ In a “halo” implantation, dopant of the same type as the major well dopant is implanted beneath the drain extension junction. The term “halo” stems from the fact that the implantation is done after the gate is formed, causing the dopant to surround the gate in a ring formation. *See, e.g.*, Ex. 1008A at 105.

52. In my opinion, the only description of graded dopant concentrations and purported carrier movement in CMOS devices in the '502 Patent is in two paragraphs of the specification and associated Figures 5A-5C. Ex. 1001, 3:22-4:3, FIGS. 5A-5C.

53. In my opinion, the specification does not provide any guidance, such as dopant concentration ranges or doping gradients, on the grading of dopant concentration that would accomplish “aid[ing]” carrier movement in CMOS devices as recited in the Challenged Claims.

54. It is my further opinion that the specification does not provide any guidance as to the degree or nature of the “aiding” referenced in the Challenged Claims. Instead, the specification contrasts “graded channel[s]” with “uniformly doped channel (as practiced in the prior art).” *Id.* at 3:54-58. Thus, in my opinion, the specification uses “graded” dopant to describe a dopant concentration that is not uniform.

C. Summary of the Prosecution History

55. None of the references relied on in this Petition were cited during prosecution. I understand the claims of the '502 Patent issued after a terminal disclaimer was filed to overcome a double patenting rejection over the issued claims of the parent '195 Patent. Ex. 1002, 50-53, 104. There were no prior art rejections. *Id.*, 53. I further understand that during prosecution of the parent '195

Patent, the Examiner found that the prior art, including Kamins and Jastrzebski, teaches all the elements of then-pending independent claim 10. Ex. 1046 (12/20/11 Office Action), 3–5; (8/13/12 Office Action), 3-5.

56. In response, Applicant amended claim 10 to add an element which recites “at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants” And which is substantially the same as current element [7.6] Ex. 1046 (10/15/12 Office Action Response), 3. The Examiner allowed the as-amended claim 10 (issued claim 1 of the ’502 Patent) and claims depending therefrom, citing this added element as the reason for allowance of these claims. Ex. 1046, (12/12/12 Notice), 2-3; Ex. 1048, claim 1. While responding to rejections based on prior art references such as Jastrzebski and Kamins, the Patent Owner made statements that address the scope and interpretation of the issued claims. I cite such statements in the context of claim 1 of the ’502 Patent below.

VII. LEVEL OF ORDINARY SKILL IN THE ART

57. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

58. In determining the characteristics of a hypothetical person of ordinary skill in the art of the '502 Patent at the time of the alleged invention, I considered several things, including the type of problems encountered in this field, and the rapidity with which innovations were made. I also considered the sophistication of the technology involved, and the educational background and experience of those actively working in the field, and the level of education that would be necessary to understand the '502 Patent. Finally, I placed myself back in the relevant periods of time, and considered the state of the art and the level of skill of the engineers working in this field in those times.

59. It is my opinion that a POSITA at the time of the '502 Patent would have had a Bachelor's degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. Additional education might compensate for a deficiency in experience, and vice-versa. I understand that, in the Intel Litigation, the Patent Owner agreed with my characterization of a POSITA. Ex. 1045, ¶13.

60. I also note that my opinions provided in this Declaration would not change in view of any minor modifications to this level of skill.

VIII. CLAIM CONSTRUCTION

61. It is my opinion that for purposes of this proceeding, the claim terms need not be construed to resolve the prior art issues presented in this Petition.

62. Nothing in this section should be construed as expressing any opinion as to whether the claims constitute patentable subject matter under 35 U.S.C. § 101, or whether they satisfy the definiteness, enablement, best mode, or written description requirements under § 112.

63. I understand that Patent Owner took positions on the meaning of certain claim terms in the Intel Litigation, which are listed in the table below. Exs. 1030, 1032-1033.

Claim Term	Patent Owner's Proposed Construction
"surface layer"	Plain and ordinary meaning ("a layer at the surface")
"substrate"	Plain and ordinary meaning ("an underlying layer")
"active region"	Plain and ordinary meaning ("a doped silicon region at the surface of a semiconductor device where a transistor can be formed")
"to aid the movement of minority carriers from ... to ..."	Plain and ordinary meaning
"well region"	Plain and ordinary meaning ("a doped region that surrounds the active region of a semiconductor device")

“active region ... within which transistors can be formed”	Plain and ordinary meaning (“a doped silicon region at the surface of a semiconductor device where a transistor can be formed”)
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64. I further understand that in the Intel Litigation, the Court provided its “preliminary constructions” in advance of the claim construction hearing, in which the Court offered a “preliminary construction” of plain and ordinary meaning as to each of the above-listed-terms. Ex. 1037. As mentioned above, I do not believe any terms need be construed to resolve the issues presented in this Petition because, in my opinion, as the Challenged Claims are unpatentable under either party’s proposed constructions (except for “surface layer” which is addressed under Patent Owner’s proposed construction). I reserve the right to respond to any purported claim constructions that Patent Owner raises.

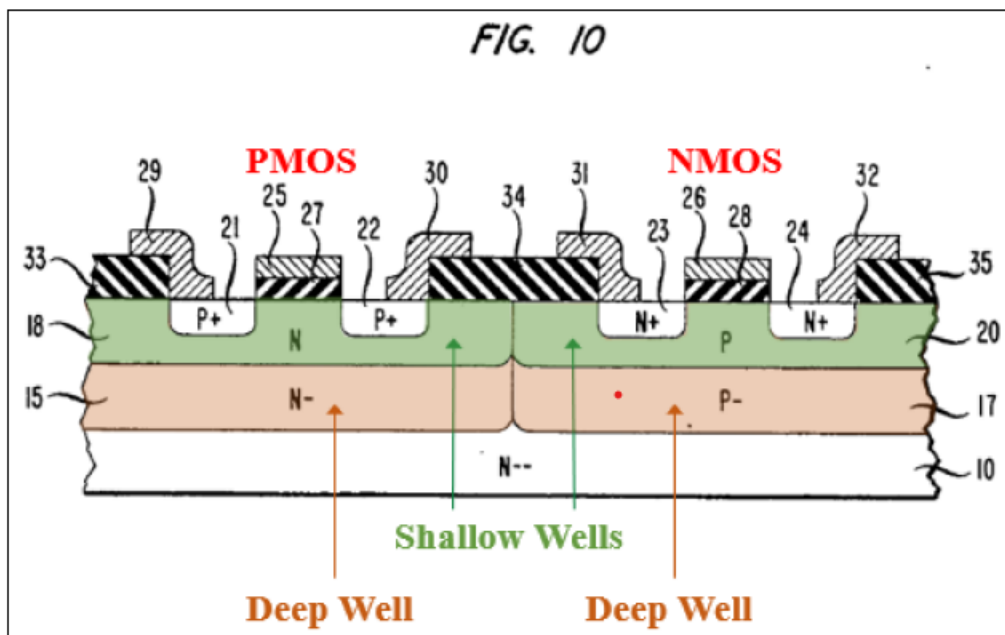
IX. OVERVIEW OF THE PRIOR ART

A. Payne

65. Payne discloses a “CMOS structure and method of manufacture ... for achieving a high packing density in integrated circuits.” Ex. 1005, Abstract. CMOS devices comprise “n-channel” (NMOS) and “p-channel” (PMOS) transistors. *Id.*, 1:1-14, 5:18-27. According to Payne, the traditional CMOS fabrication processes using “single tub or twin tub approach[es]” (single-well or twin-well architecture) require source/drain regions of NMOS and PMOS

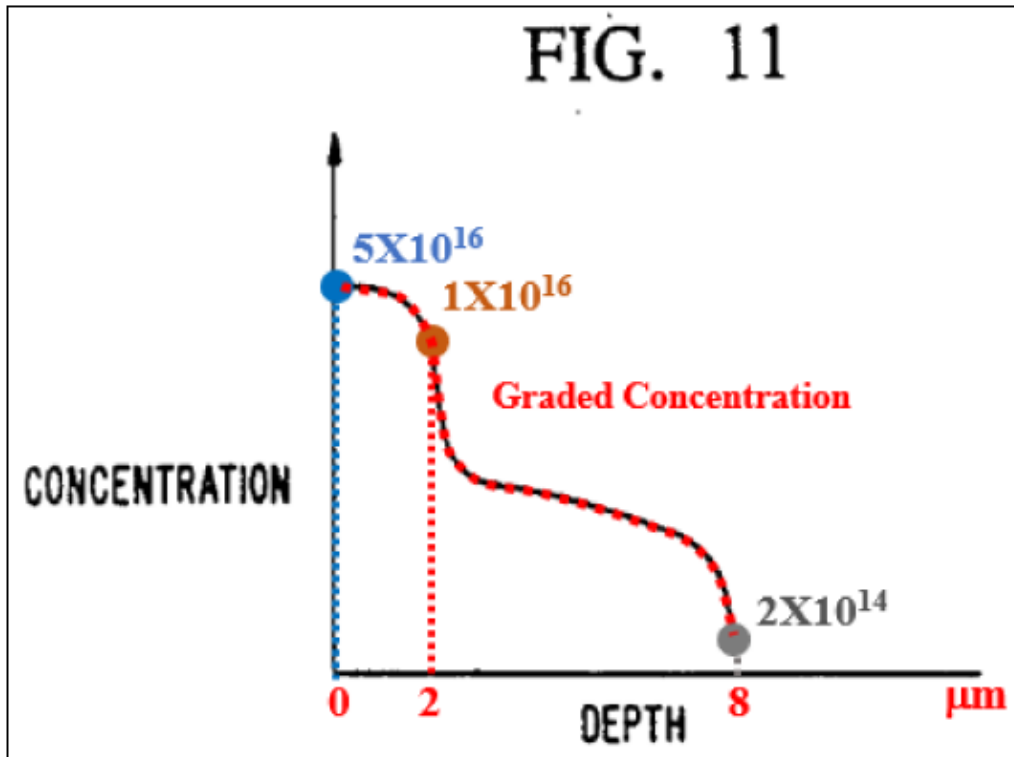
transistors to be sufficiently spaced apart (*e.g.*, at least 12 μ m), which hinders high packing density. *Id.*, 1:10-50.

66. Payne teaches forming a double-deck well structure, whereby shallow twin-wells (18 and 20) of “greater impurity concentration” are formed in deep wells (15 and 17), as shown below. *Id.*, 1:5-15, 1:51-2:2, 5:18-55, 6:35-51.



Id., FIG. 10; see also 2:3-28, 2:56-5:21, 5:44-50, FIGS. 2-9.

67. Payne further teaches that the double-deck well structure has a graded dopant concentration (“high-low implant profile”) that decreases with depth, as shown below in Figure 11. *Id.*, 2:38-41, 5:14-17, 5:51-57 6:7-17, FIG. 11.



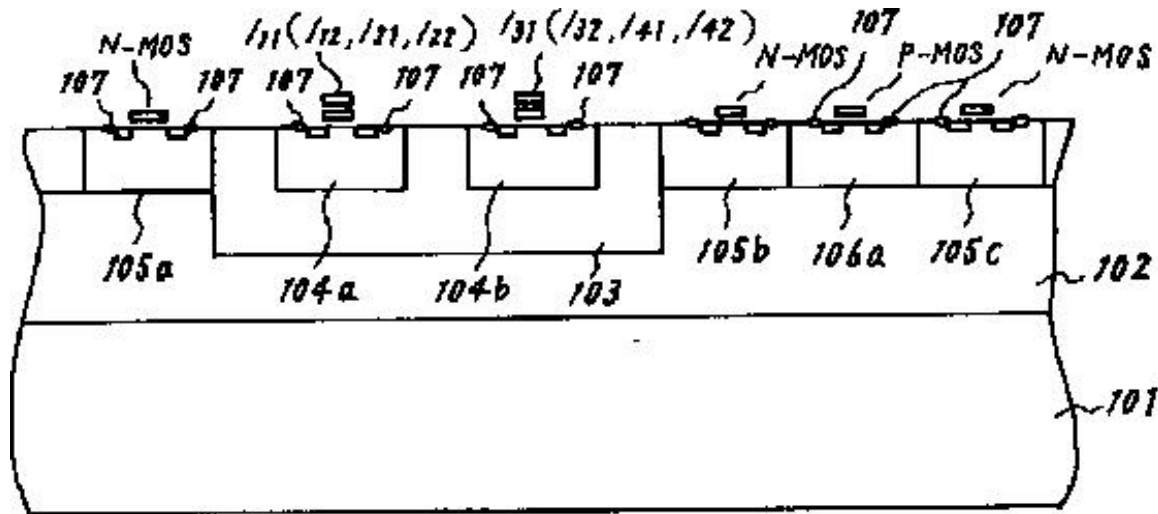
Id., FIG. 11 (annotated with exemplary maximum dopant concentrations at different depths disclosed in Payne); *id.*, 2:56-59, 5:48-55; *see also* Section X.A.1.e. Payne’s double-deck well structure having the “high-low implant profile of FIG. 11” advantageously allows source and drain regions to be placed closer (*e.g.*, less than 5 μm separation) resulting in “a high packing density.” *Id.*, Abstract, 1:43-54, 5:56-6:20.

B. Onoda

68. Onoda discloses a nonvolatile semiconductor storage device (*e.g.*, flash memory) that provides improved latch-up resistance, punch-through resistance, and improved junction breakdown voltage between the well regions and the semiconductor substrate. Ex. 1042, Abstract. Figure 3 depicts the general

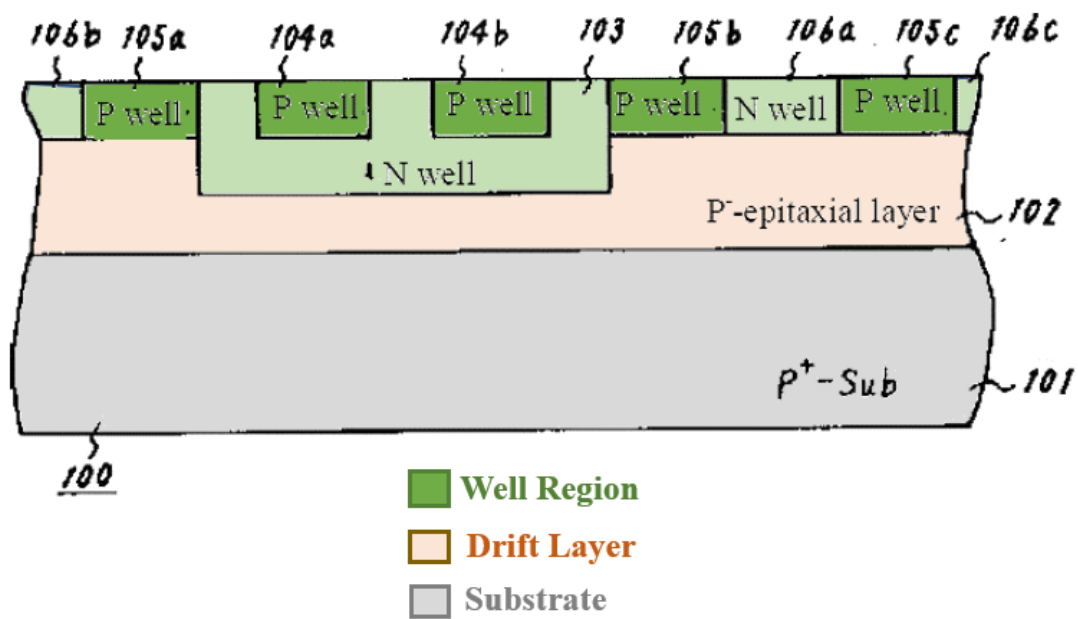
structure of the flash memory according to Embodiment I. Figure 3 depicts memory cells (I₁₁ through I₄₂) and N-channel MOS and P-channel MOS transistors.

Id., [0043].

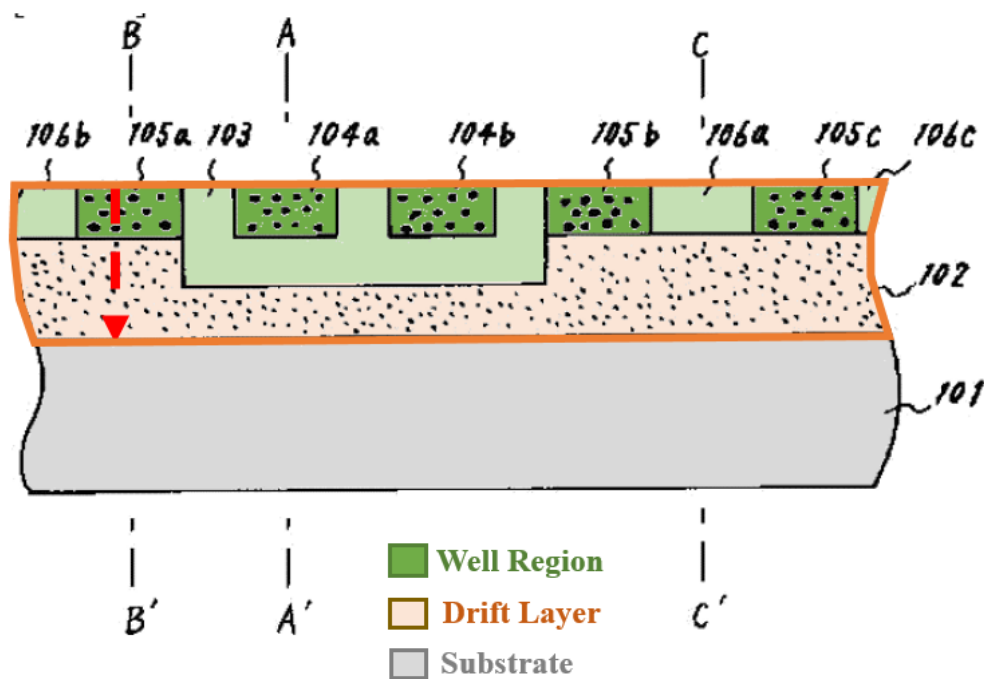


Id., FIG. 3.

69. Onoda discloses that a lightly-doped P-type semiconductor layer (second semiconductor layer 102) is formed over a heavily-doped P-type substrate (the first semiconductor layer 101). *Id.*, [0046]. Thereafter, dopants, such as boron (B) and phosphorus (P), are implanted in the second semiconductor layer 102 to create well regions. For example, Figure 2 (below, top) depicts an N-type first well region 103, P-type second well regions 104a–b, P-type third well regions 105a–c, and N-type fourth well regions 106a–c formed on the second semiconductor layer 102. *Id.*, [0047]–[0050]. Figure 8 (below, bottom) depicts well regions 105a, 104a, 104b, 105b, and 105c where boron B has been implanted.

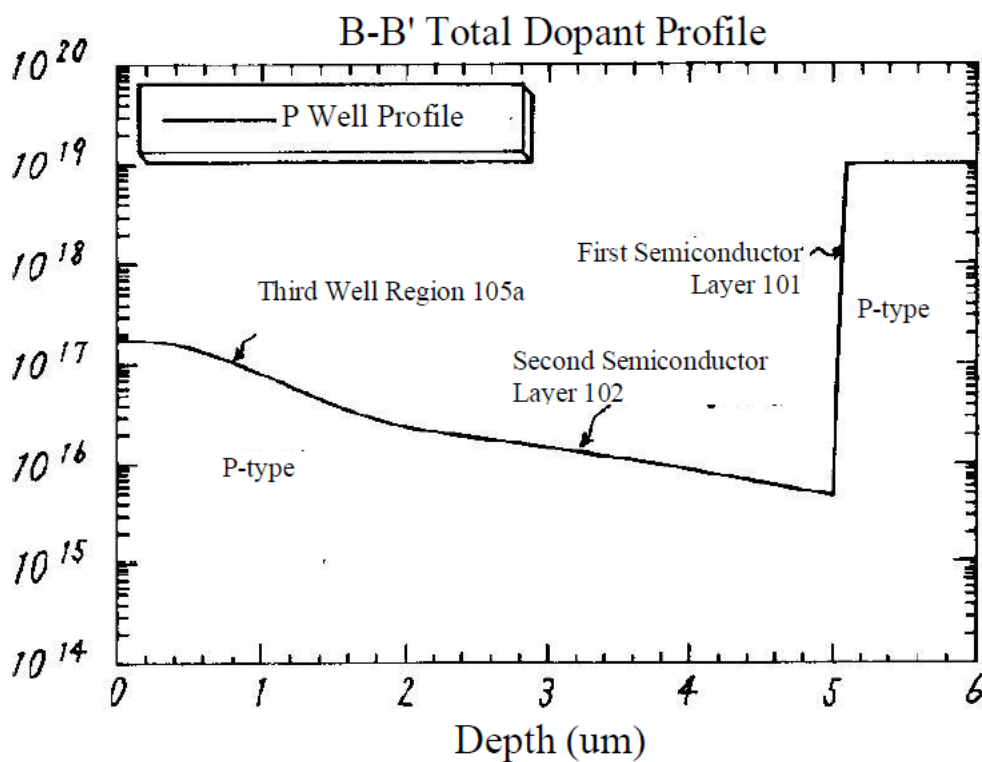


Ex. 1042, FIGS. 2



Ex. 1042, FIG. 8.

70. The dopant profile appearing in the B-B' cross-section in Figure 8 is shown in FIG. 11. As depicted in Figure 11, “a third well region 105a is formed up to a depth of about 1.5 μm from the surface of the second semiconductor layer 102, and the second semiconductor layer 102 is interposed from the bottom surface of the third well region 105a up to the surface of the first semiconductor layer 101.” Ex. 1042, [0052]. Both the third well region 105a and the second semiconductor layer 102 are of the same conductivity type, *i.e.*, P-type, “so there is no clear boundary between the third well region 105a and the second semiconductor layer 102, but rather the dopant concentration falls off smoothly.” *Id.*



Ex. 1042, FIG. 11.

C. Wolf

71. *Silicon Processing For The VLSI Era* by Stanley Wolf is a four volume textbook related to semiconductor devices, with particular focus on CMOS devices. Exs. 1008A-D. I am familiar with the Wolf textbook. An internet search for this textbook title limited to the “.edu” domain yields over 800 results. Thus, it is clearly used as a teaching resource in engineering courses in many, many universities and is widely cited in scientific works.

X. SPECIFIC GROUNDS FOR PETITION

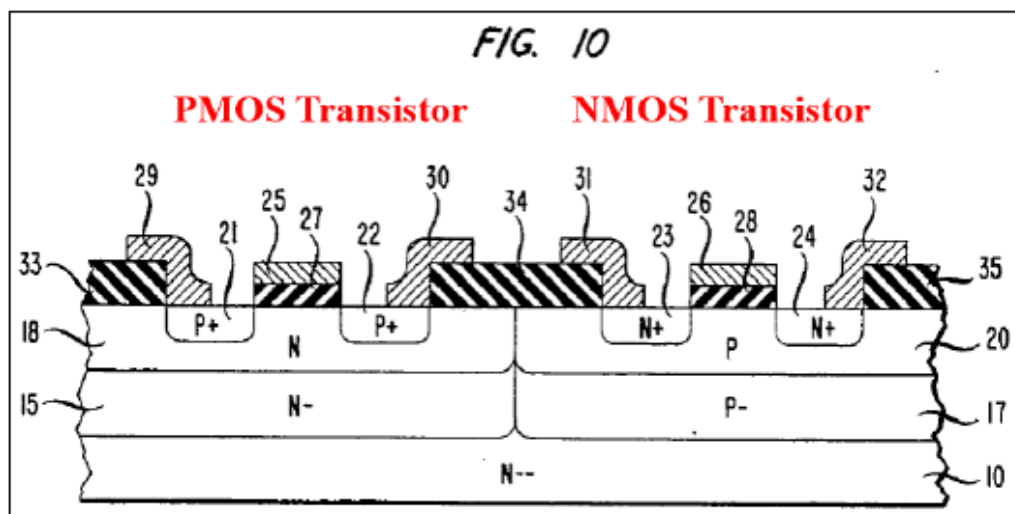
A. Ground I:

72. In my opinion, Payne renders claim 7 obvious.

1. Independent Claim 7

a. Preamble: “A semiconductor device comprising:”

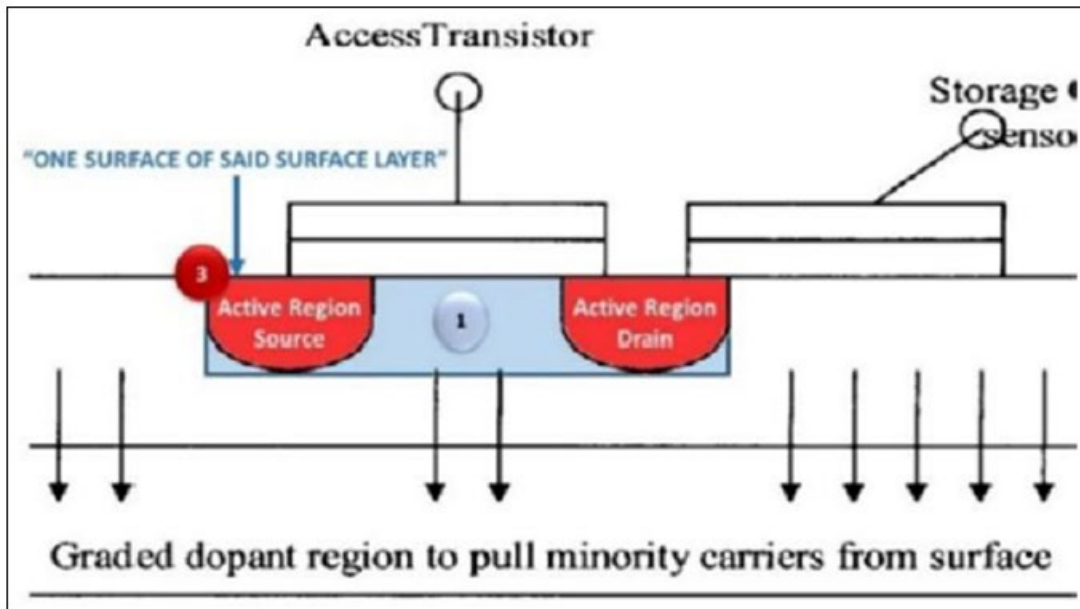
73. In my opinion, Payne discloses this element. Payne is directed to a semiconductor device. Ex. 1005, Title, Abstract, 1:51-54 (“it is a primary object of the invention to provide a CMOS structure and method of manufacture which requires little semiconductor space and therefore permits a high packing density.”); 1:5-15 (“Complementary field effect transistors (hereinafter designated CMOS) [] comprise n-channel and p-channel devices . . .”). Payne’s Figure 10 illustrates a “p-channel” (PMOS) transistor (with “P+” source/drain regions 21/22) adjacent to an “n-channel” (NMOS) transistor (with “N+” source/drain regions 23/24) of a CMOS semiconductor device. *Id.*, 2:50-60, 5:18-34, 6:57-59.



Ex. 1005, FIG. 10.

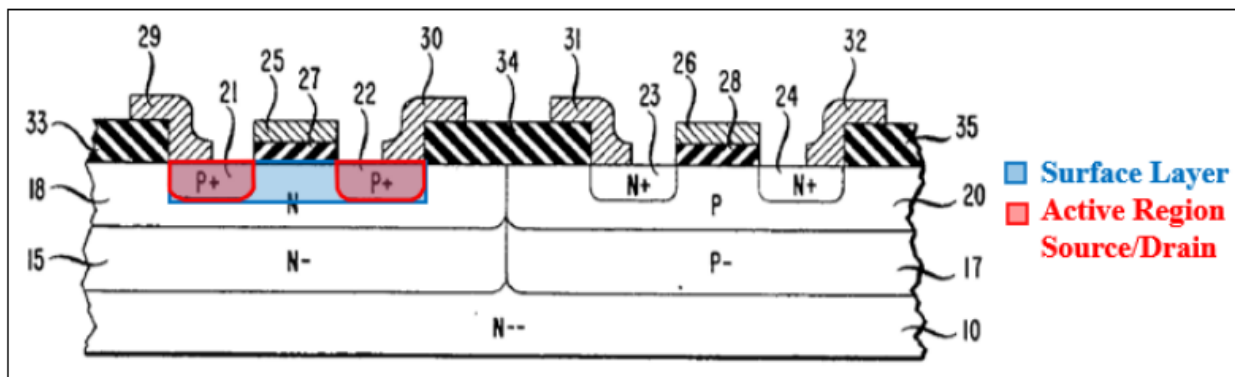
b. Element [7.1]: “a surface layer;”

74. In my opinion, Payne discloses, or at a minimum, renders obvious this element. According to Patent Owner, a “surface layer” is “a layer at the surface of the silicon” (or “a layer at the surface of the semiconductor device”)—which Patent Owner annotated in blue below—“where the active region [(red)] is located.” Ex. 1030, 6, 9, 12, 13; Section VIII.



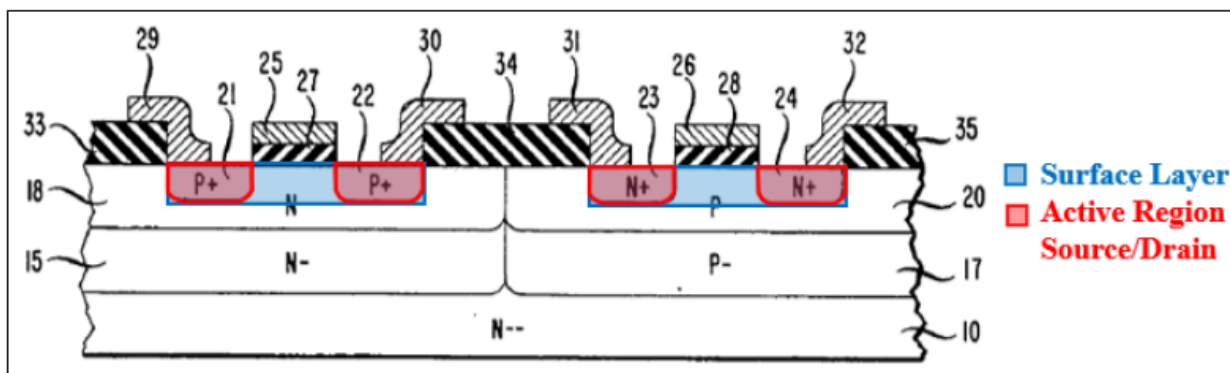
Ex. 1001, FIG. 5(b); Ex. 1030, 7, 12.

75. In my opinion, Payne satisfies element [7.1] to the same extent that Figure 5(b) of the '502 Patent meets it. Payne's Figure 10 discloses a surface layer (blue) that matches the surface layer Patent Owner identified in Figure 5(b). Payne's surface layer, which is a subset of what Payne refers to as "surface region 18," is at the surface of Payne's silicon substrate 10, and "source and drain regions, 21 and 22 [(red)] of P+ conductivity" of Payne's p-channel transistor (left) are located in it. Ex. 1005, 2:50-60; 5:21-27, 6:57-59, FIG. 1.



Ex. 1005, FIG. 10.

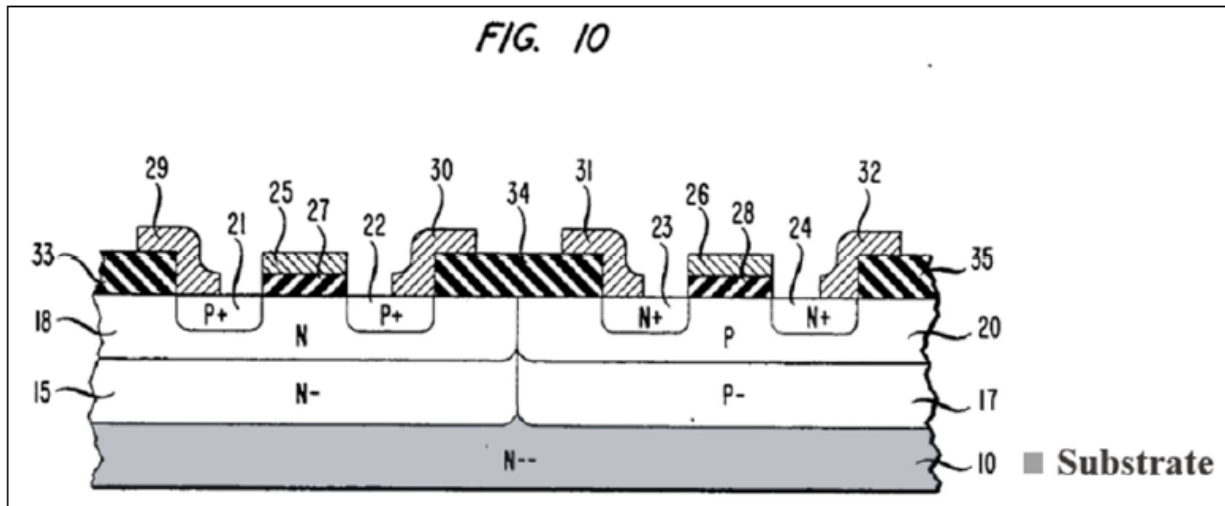
76. Payne likewise discloses another surface layer, a subset of “surface region 20,” containing “source and drain regions, 23 and 24, of N+ conductivity” of Payne’s n-channel transistor (right). *Id.*, 5:24-27, 6:57-59.



Ex. 1005, FIG. 10.

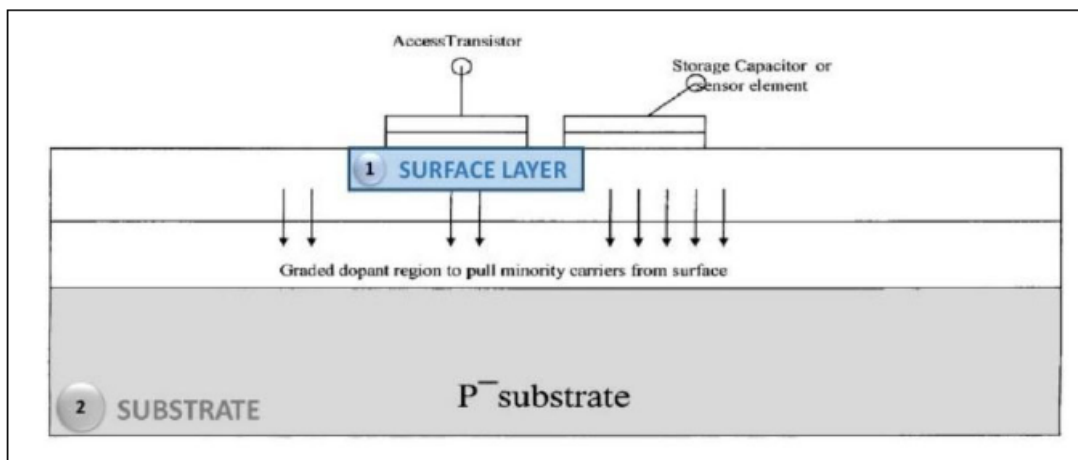
c. Element [7.2]: “a substrate;”

77. In my opinion, Payne discloses this element. Payne’s Figure 10 illustrates a CMOS device “fabricated in a silicon semiconductor **substrate** [(grey)], 10 of ‘N-’ conductivity type which typically has a doping concentration of approximately $1\text{-}2 \times 10^{14}$ ions/cm³[.]” Ex. 1005, 1:60-62, 2:50-60.



Ex. 1005, FIG. 10.

78. In my opinion, Payne satisfies element [7.2] under Patent Owner's proposed construction of "plain and ordinary meaning, [*i.e.*] 'an underlying layer.'" Section VIII. Payne's substrate also matches Patent Owner's identification of the substrate (grey) in Figure 5(b) of the '502 Patent.⁴

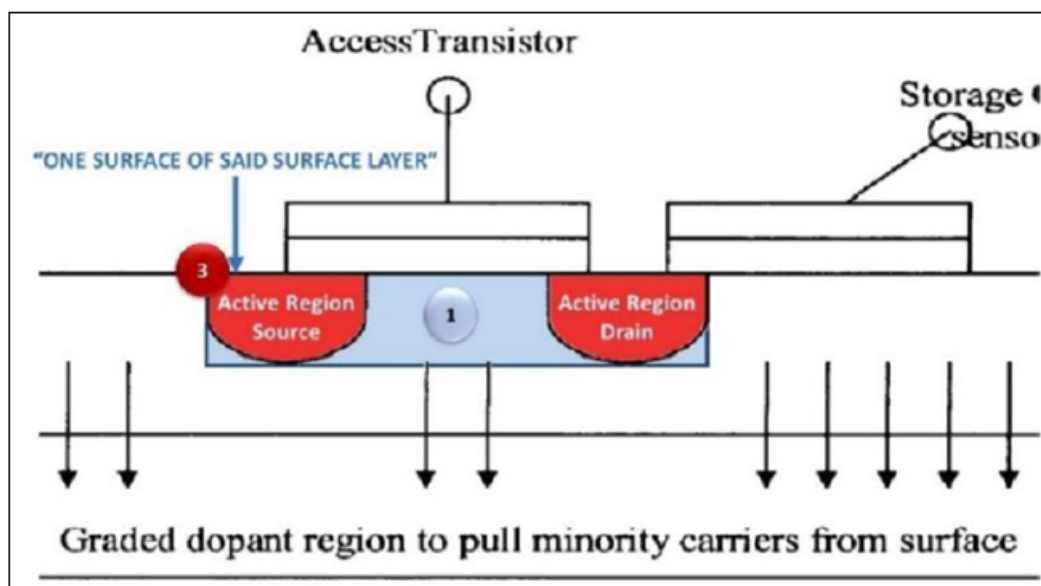


⁴ Patent Owner used Figure 5(b) from the parent '195 Patent as an example. Ex. 1030, 5-6. The '502 Patent and the '195 Patent have the identical specification and figures, including Figure 5(b).

Ex. 1030, 6-7, 16-17 (well region and drift layer can be part of substrate); Ex. 1001, FIG. 5(b).

- d. **Element [7.3]: “an active region including a source and a drain, disposed on one surface of said surface layer;”**

79. In my opinion, Payne discloses or, at a minimum, renders obvious this element. According to Patent Owner, Figure 5(b) of the '502 Patent depicts an active region (red) “disposed on one surface [(top surface)] of said surface layer”:



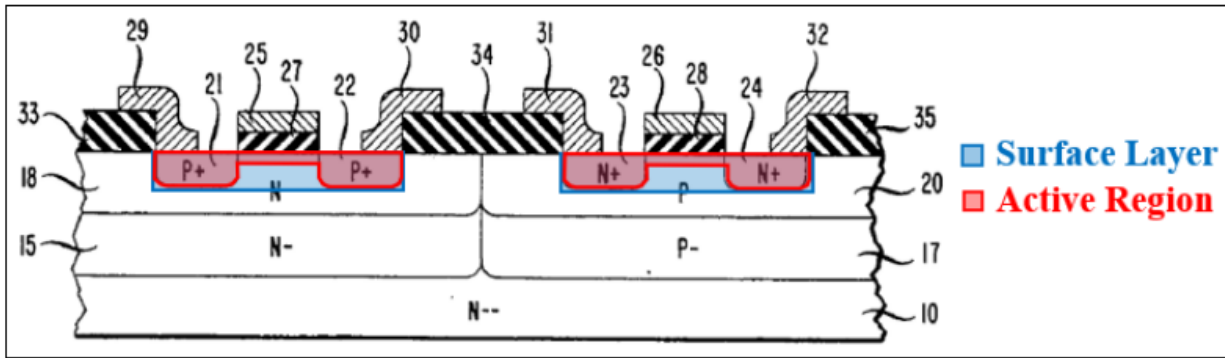
Ex. 1001, FIG. 5(b); Ex. 1030, 6-7, 11 (“[T]he ‘active region’ is part of the ‘surface layer’ ... When the claim says the active region is ‘disposed on one surface of the surface layer,’ it means the active region is located on the ‘ceiling’ of the silicon *inside* the silicon.”) (emphasis in original), 12.

80. In my opinion, Payne satisfies element [7.3] under Patent Owner’s interpretation. Payne’s Figure 10 below illustrates a “p-channel” transistor with

source/drain regions 21/22 (left), and an “n-channel” transistor with source/drain regions 23/24 (right). Ex. 1005, 5:18-29, 1:5-19, 6:57-59. These source/drain regions are formed with “a surface impurity concentration of approximately 10^{19} - 10^{20} ions/cm³.” Ex. 1005, 5:21-29, 1:43-45.

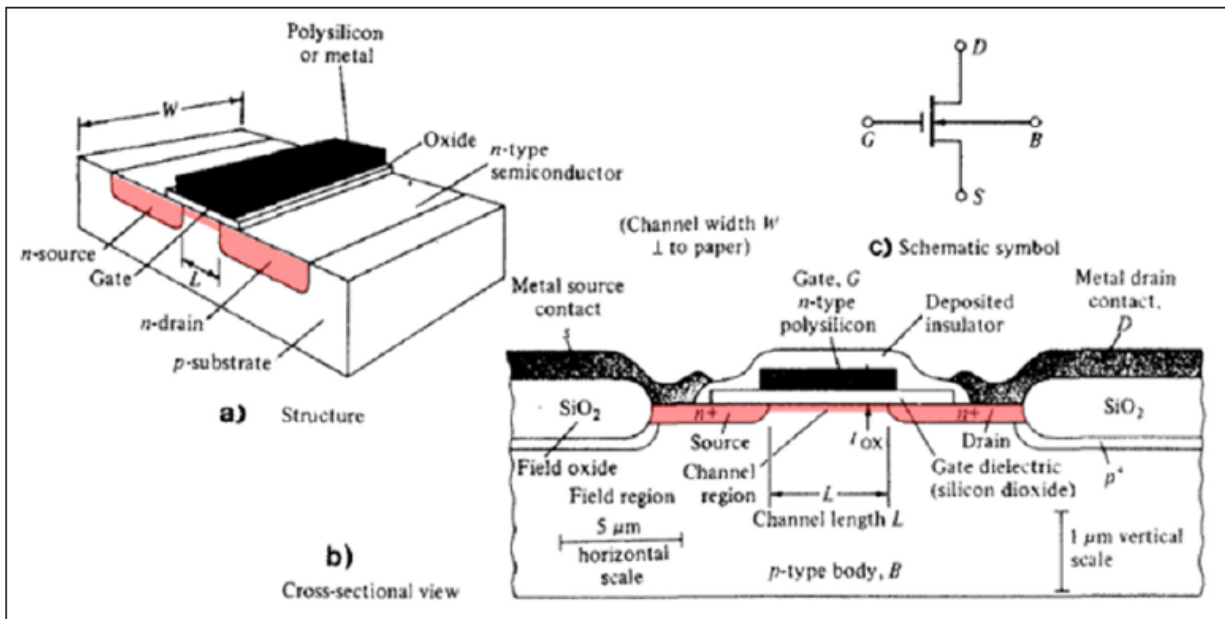
81. The channel region between these source/drain regions is part of the surface region, which has an impurity concentration of “typically $0.5\text{-}5 \times 10^{16}$ ions/cm³.” Ex. 1005, 5:51-52, 4:31-39, 4:63-5:5. The source/drain regions of a transistor, together with the channel region in between them, form an active region. Ex. 1008B, 299 (“The top surface of the [silicon substrate] body consists of active or transistor regions as well as passive or (field) regions. The *active regions* are those in which transistor action occurs; *i.e.*, the *channel* and the heavily doped *source* and *drain* regions.”), 300, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e).

82. The active region (red) of each of Payne’s transistors is disposed on one surface (top surface) of a corresponding surface layer (blue), exactly as depicted in Patent Owner’s annotated Figure 5(b) above. Section X.A.1.b.



Ex. 1005, FIG. 10.

83. In my opinion, Payne satisfies element [7.3] under Patent Owner's position that "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed" (Section VIII) because the active region of a MOS transistor is "[its] channel and [its] *heavily doped* source and drain regions," highlighted in red below. Ex. 1008B, 299.

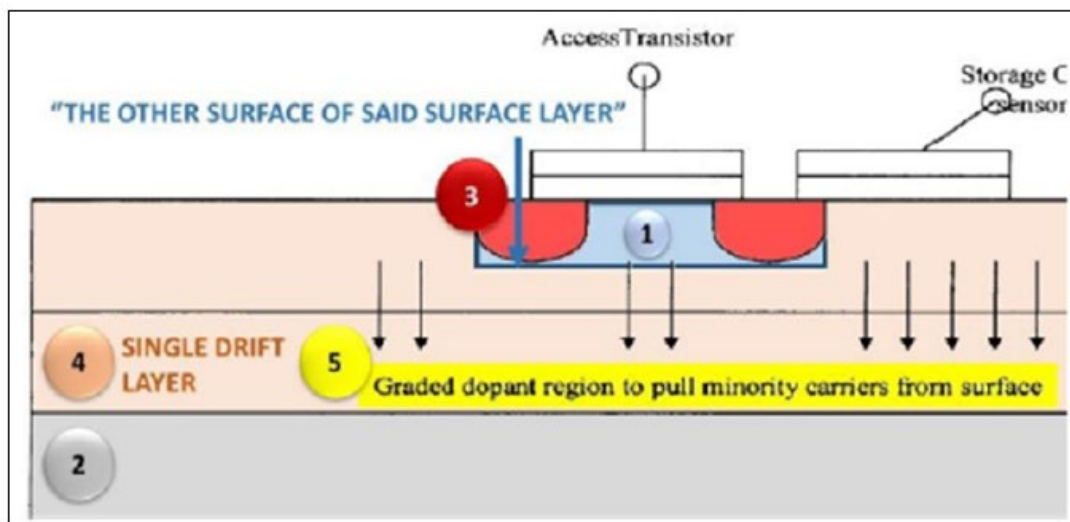


Ex. 1008B, FIG. 5-1; *id.*, 298-301, 374, FIGS. 5-2, 6-4.

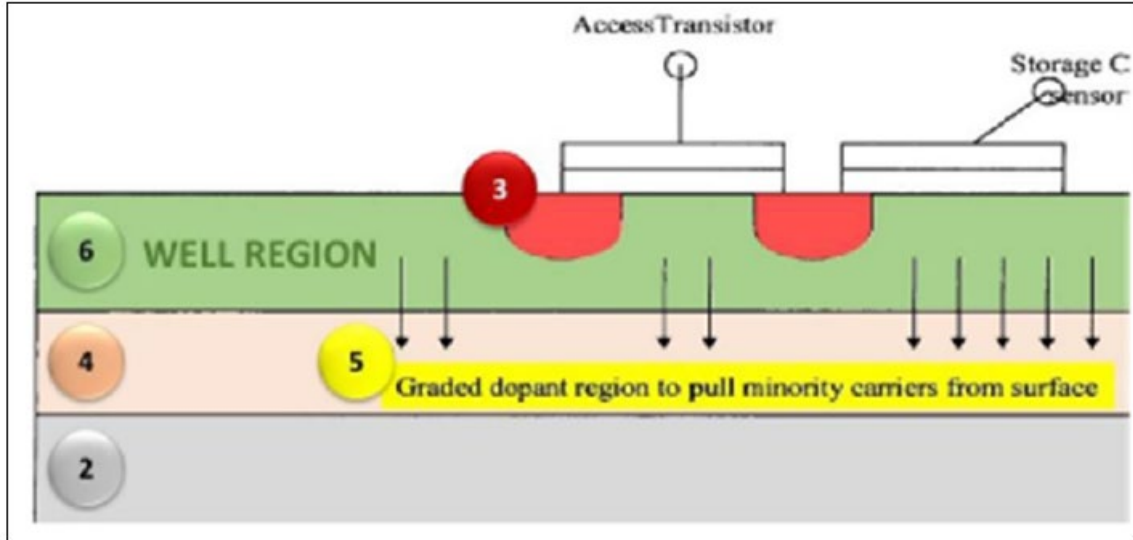
- e. **Element [7.4]: “a single drift layer disposed between the other surface of said surface layer and said substrate,”**

84. In my opinion, Payne discloses or, at a minimum, renders obvious this element.

85. **Single drift layer** – In its claim construction brief, Patent Owner identified the single drift layer in tan in Figure 5(b). Ex. 1030, 7. According to Patent Owner, the single drift layer (tan) is “disposed between ‘the other surface [(bottom surface)] of said surface layer [(blue)]’ and [said] substrate [(grey)]”:



Ex. 1001, FIG. 5(b); Ex. 1030, 7. The single drift layer in Figure 5(b) has a well region (green) disposed in it, forming a nested structure, as required by the claim (see element [7.6]), and as shown below:

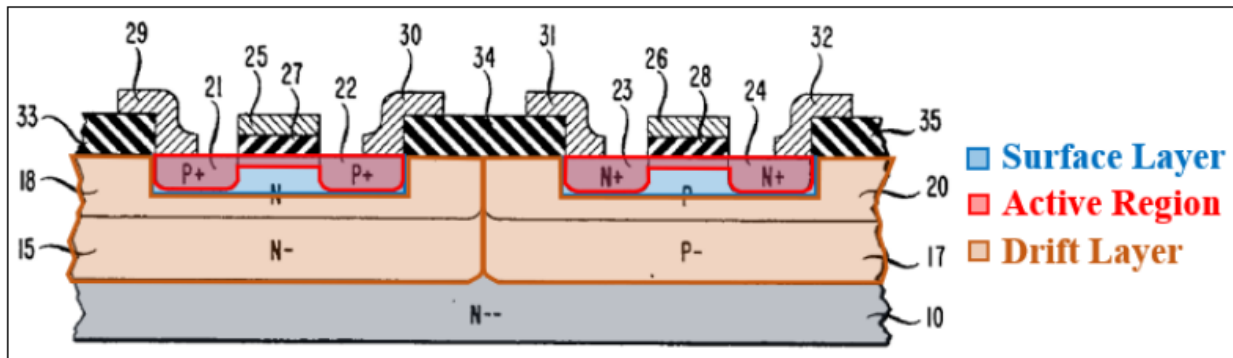


Ex. 1001, FIG. 5(b); Ex. 1030 at 7; *id.*, 11 (“the ‘well region’ is part of the ‘single drift layer.’”).

86. In my opinion, Payne discloses a single drift layer to the same extent the ’502 Patent’s Figure 5(b) does. In Payne’s Figure 10, the **“first tub region” 15 (tan)** of Payne’s nested well structure—with shallow well (“surface region”) 18 disposed in it—is an example of the claimed single drift layer. *Id.*; Ex. 1005, 3:28-42 (ion implantation for tub 15), 4:19-30 (thermal drive-in to achieve the desired depth for tub 15), 4:31-39, 5:7-17, 5:44-48, 5:48-50 (“In a typical device, the final depth of surface regions 18 and 20 would be approximately 1-2 μ and the depth of the **tub regions 15 and 17** would be typically 3-8 μ .”).

87. This single drift layer (tan) is “disposed between the other surface [(bottom surface)] of said surface layer [(blue)] and [said] substrate [(grey)]” under

Patent Owner's interpretation, and in exactly the same way as depicted in Patent Owner's annotated Figure 5(b) above.



Ex. 1005, FIG. 10. Payne's tub 17 (right), in which shallow well 20 is disposed, is likewise a single drift layer (tan) disposed between a surface layer (blue) and the substrate (grey). Ex. 1005, 4:3-30, 4:63-5:17, 5:44-50; Section X.A.1.b.

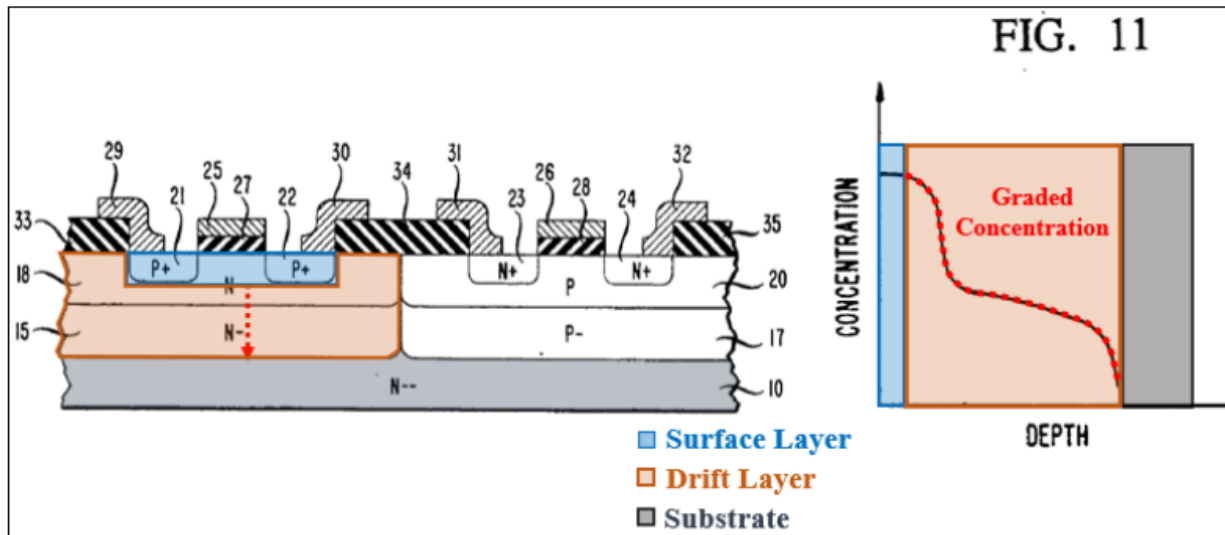
88. In my opinion, Payne meets all other claim requirements associated with the single drift layer to the same extent Figure 5(b) meets them. See below and elements [7.5]-[7.6]. Notably, as detailed in element [7.5], each of Payne's tubs 15/17 is a *single* drift layer because it has a graded-dopant concentration that, according to Patent Owner, creates a unidirectional electric drift field that aids the movement of minority carriers in a *single* direction—from the surface layer to the substrate. Ex. 1030, 7; Ex. 1046, 253-54, 289-290; Section X.A.1.f.

- f. **Element [7.5]: “said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and”**

89. In my opinion, Payne discloses or, at a minimum, renders obvious this element.

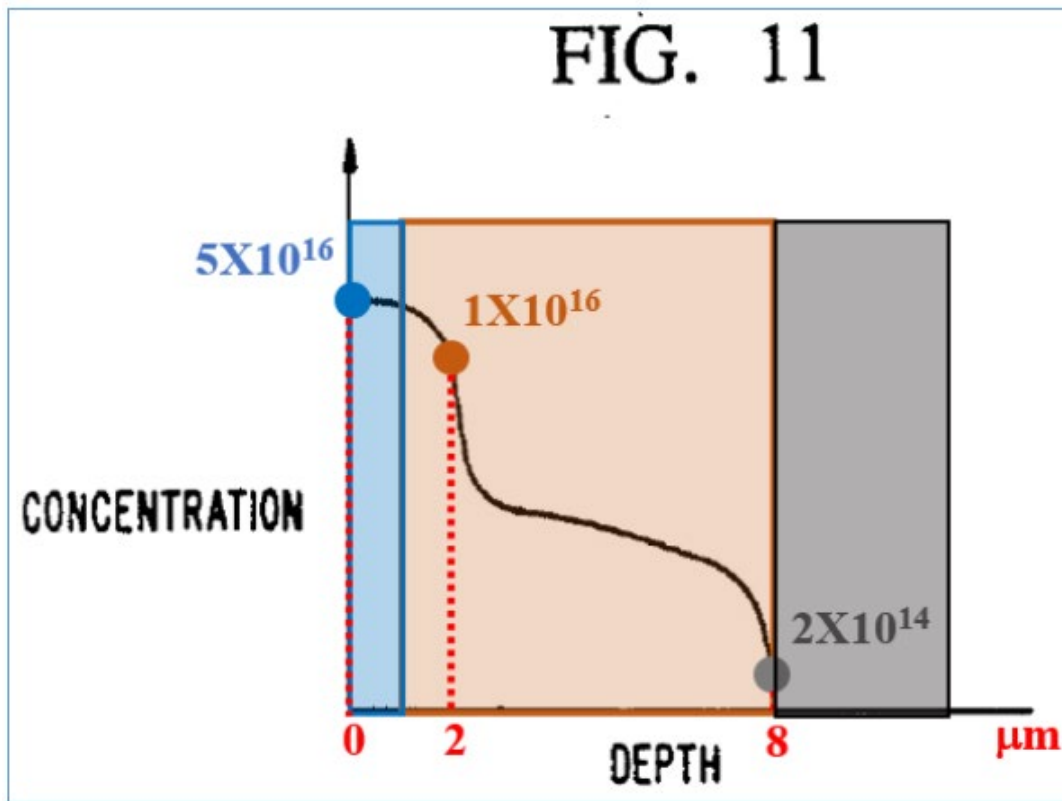
90. **Graded dopant concentration** – The '502 Patent admits that graded-dopant concentrations were known, Ex. 1001, 2:17-19, FIG. 1 (“Prior Art”), and that it was known to grade the dopant concentration in CMOS devices to affect the movement of minority carriers. *Id.*, 1:38-2:9, FIGS. 3(a)-3(d) (all “Prior art”). Payne’s single drift layer has a graded-dopant concentration extending between the surface layer and the substrate. Payne explains that the “impurity profile in both tubs [15/17] thereby has the general shape illustrated in FIG. 11” which exhibits “[t]he major advantage” of a “***high-low implant profile.***” Ex. 1005, 2:38-41, 5:14-17, 5:56-57.

91. Payne’s Figure 11 (below right) illustrates the dopant concentration measured along the red dotted line in Figure 10 (below left), which starts at the bottom of the surface layer (blue) and extends to the substrate (grey). As shown below, Payne discloses a downward-sloping graded-dopant concentration in the single drift layer (tan) associated with Payne’s PMOS transistor (left).



Ex. 1005, FIGS. 10-11.

92. I have annotated Figure 11 to reflect exemplary (maximum) dopant concentrations at various depths disclosed in Payne: (1) 5×10^{16} ions/cm³ at the surface of the shallow wells (depth 0 μ m), (2) 10^{16} ions/cm³ at a depth of $\sim 2\mu$ m (boundary of deep and shallow wells), and (3) 2×10^{14} ions/cm³ at a depth of $\sim 8\mu$ m (boundary of substrate and deep wells).

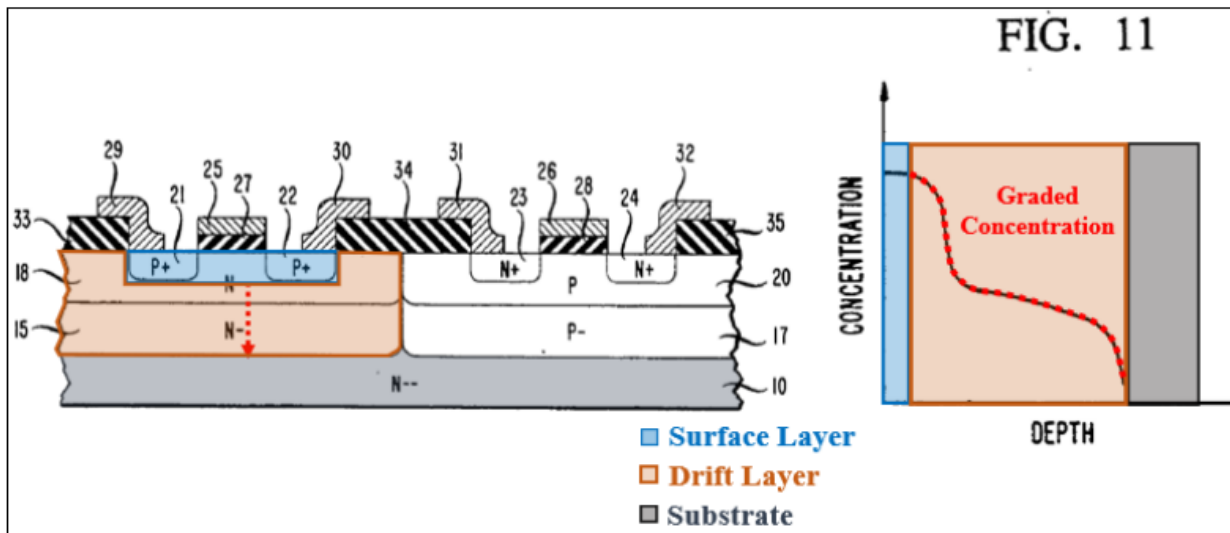


Ex. 1005, FIG. 11.

93. Payne explains that “[t]he surface impurity concentration of the surface regions [18/20] is typically $0.5\text{-}5 \times 10^{16}$ ions/cm³ and that [the surface impurity concentration] of the tub regions [15/17] is typically $10^{15}\text{-}10^{16}$ ions/cm³, with the former concentration being *at least twice as much* as the latter over these ranges.” *Id.*, 5:51-55. The concentration is lowest at the substrate, where it is “ **$1\text{-}2 \times 10^{14}$** ions/cm³.” *Id.*, 2:56-59. Payne also explains that “the final depth of surface regions 18 and 20 would be approximately $1\text{-}2\mu$ and the depth of tub regions 15 and 17 would be typically $3\text{-}8\mu$.” *Id.*, 5:48-50.

94. While the above discusses the single drift layer associated with Payne's PMOS transistor (left in Figure 10), Payne teaches that the single drift layer associated with Payne's NMOS transistor (right) also has a downward-sloping graded dopant concentration. Ex. 1005, 5:14-17.

95. **First static unidirectional electric drift field to aid the movement of minority carriers** – As shown below, Payne's single drift layer (tan) has a downward-sloping graded-dopant concentration extending between the surface layer (blue) and the substrate (grey).



Ex. 1005, FIGS. 10-11.

96. Payne's downward-sloping graded-dopant concentration aids the movement of minority carriers from the surface layer to the substrate to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. During

prosecution of the parent '195 Patent, Applicant represented to the Patent Office that a downward-sloping graded-dopant concentration was known in the prior art to create an “inherent ‘built-in’ unidirectional electric field” that moves carriers deep into the substrate (while an upward-sloping concentration, not at issue in Payne, would move those carriers in the opposite direction towards the surface):

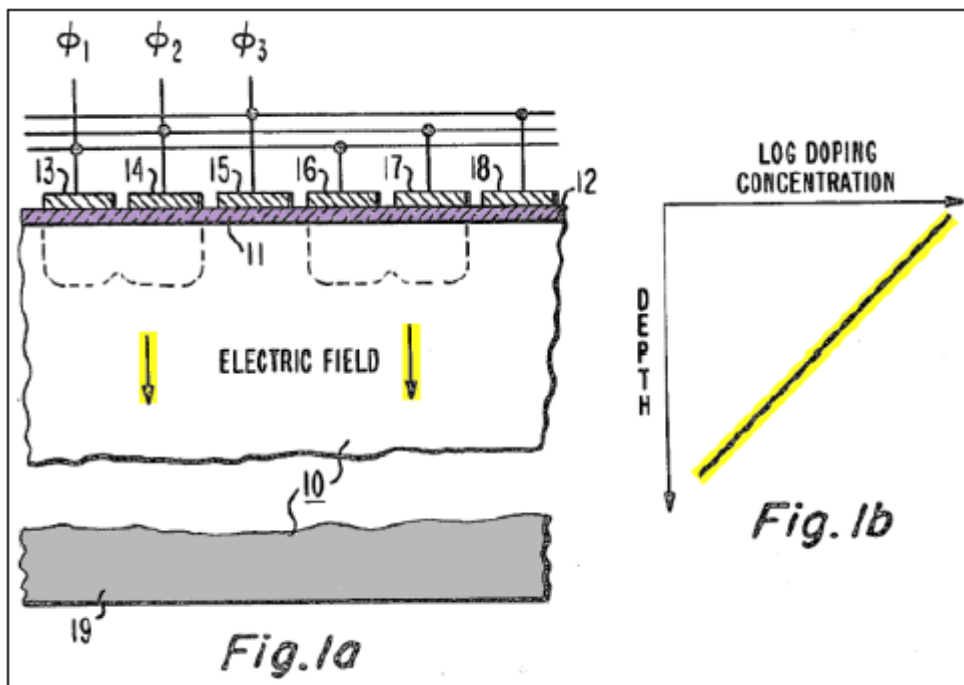
[T]he graded dopant concentration itself creates a **‘built-in’ electrical field** that forces the movement of carriers into a particular direction, whereby *the ‘direction’ of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.*

Ex. 1046, 289-290 (underlining in original).

97. Applicant further represented that “a unidirectional drift (electric) field necessarily affects **all** the present minority carriers in the same way.... Depending on the particular slope of the graded concentration of dopant, **all** minority carriers are either swept ‘down’ ... or ‘up...’” Ex. 1046, 289. Applicant cited Jastrzebski in support. *Id.*, 290. In Jastrzebski, the graded-dopant concentration is “decreasing with depth” from the top surface 11 (purple) of the substrate 10, as shown in Figure 1b below. Ex. 1010, 5:14-22.

98. Jastrzebski teaches that this downward-sloping graded-dopant concentration creates an electric drift field that “force[s] most of the charge

carriers ... *deep into the substrate*[.]” *Id.*, 5:14-22; *Id.*, 2:27-32 (“This is done by creating a field, such as a drift field, in the semiconductor substrate to *sweep minority charge carriers*...into the bulk [substrate], away from the electrode-bearing surface of the substrate.”).

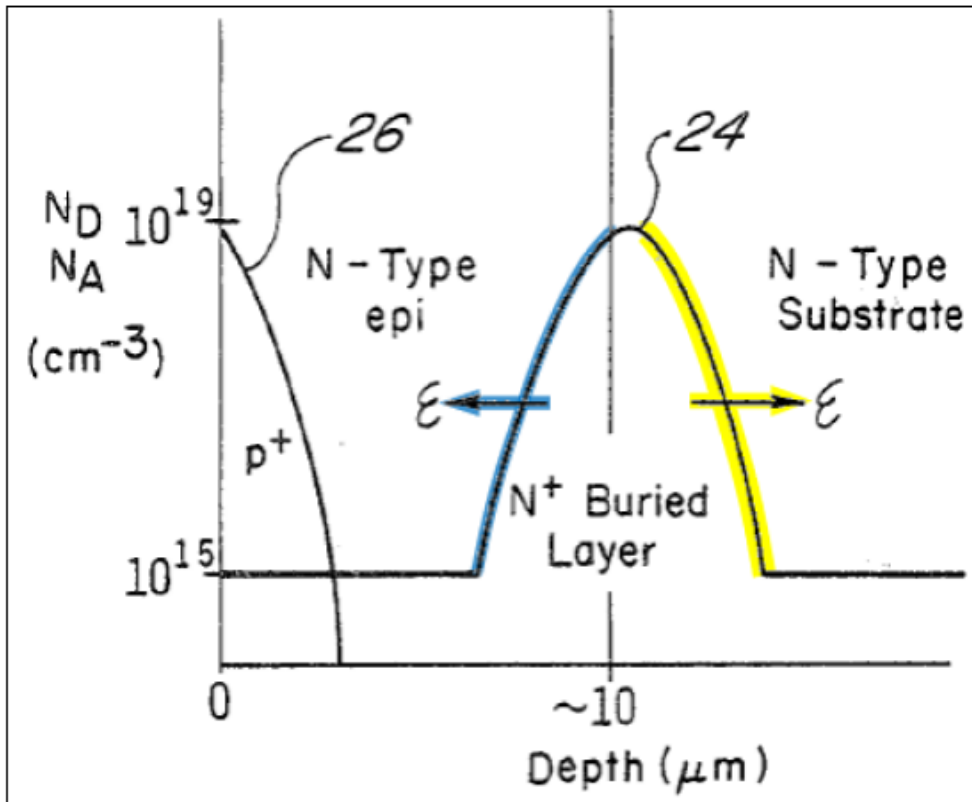


Ex. 1010, FIGS. 1a-1b.

99. Applicant made the same representation to the Patent Office regarding Kamins. Ex. 1046, 237-238, 253-254. According to Applicant, Kamins’ Figure 3 shows “two electrical fields with opposing directions” (highlighted in blue and yellow) that correspond to increasing and decreasing graded-dopant concentrations, respectively. *Id.*, 237, 253 (citing Ex. 1009, 3:6-13, FIGS. 2-3). Applicant explained that Kamins “show[s] *minority carrier*s

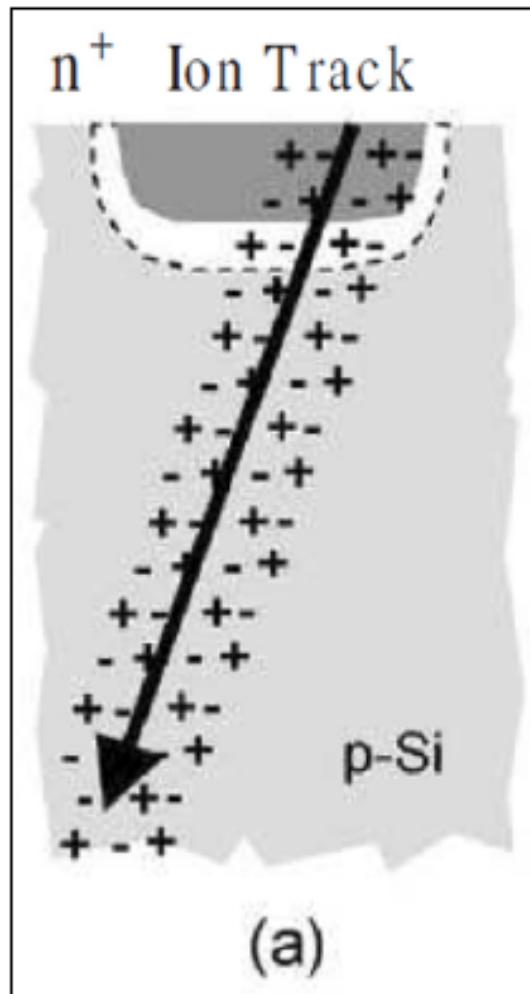
accelerated into the substrate.” Id., (citing Ex. 1009, FIG. 2 and quoting Ex. 1009, 3:6-13 (“carriers... accelerated... *away from the surface... into the substrate*”)).

100. According to Applicant, the electric field associated with the downward-sloping graded concentration at depth beyond $\sim 10\mu\text{m}$ (red) causes “[minority] carriers created [in that region to be] ... *accelerated into the substrate*” *Id.* (citing Ex. 1009, 3:6-13, FIGS. 2-3); Ex. 1030 at 24 (Kamin’s “bottom electric field [(yellow)] draws a *minority carrier* from the substrate to a *deeper* part of the substrate.”); Ex. 1009, 2:67-3:14 (“The non-uniform dopant concentration in the substrate creates electric fields in the substrate indicated by arrows labeled ‘ ϵ ’ in FIGS. 2 and 3” such that “[minority] carriers created below the maximum dopant concentration are accelerated into the substrate.”), FIG. 2 (referring to these carriers as “photogenerated minority carriers”), 2:11-16 (same).



Ex. 1009, FIG. 3.

101. During a so-called single event upset (SEU), an α -ray generates millions of carriers, some of which are produced in or near the active regions at the surface of the substrate. Ex. 1013, 431 (“A[n] [α -]particle can induce SEU when it strikes at the *channel region* of an off NMOS transistor or the *drain region* of an off PMOS transistor.”), FIG. 2. As shown in Figure 2, such an event generates both types of carriers (holes, denoted “+” and electrons, denoted “-”), one of which will be the minority carrier in any given surface layer.



Ex. 1013, FIG. 2(a).

102. Like Jastrzebski and the right-hand side of Kamins Figure 3 (yellow), Payne's graded dopant concentration is downward-sloping, as shown in Figure 11. Moreover, this graded-dopant profile is determined by the ion-implantation and drive-in steps of the chip fabrication processes (described in Payne in relation to Figures 2 and 5-9 in particular) and thus the profile (and any resulting electric field) is static—it is set once the device has been fabricated and does not change.

Ex. 1005, 5:7-17, 5:44-55 (describing “the *final* depth” of tubs and surface regions and their typical ranges of impurity concentrations).

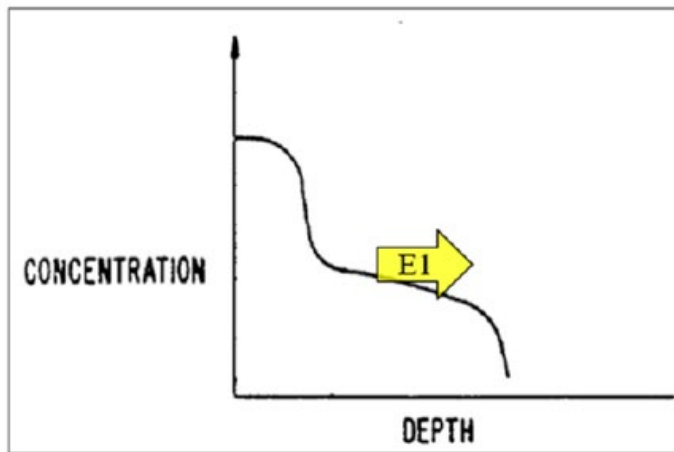
103. I note that during prosecution of the parent ’195 Patent, Applicant described “static” similarly, conceding that “Kamins (US 4,160,985), just like Applicant, discloses the presence of a ‘static’ drift field, ‘because the drift field is created by graded concentration of dopants which does not change over time.’” Ex. 1046, 318 (citing Ex. 1009, 2:15-16, 2:64-3:2, 1:38-46, 3:8-11 and Ex. 1046, 302-03), 333 (same).

104. Thus, according to Jastrzebski, Kamins, Applicant, and Patent Owner, Payne’s profile generates a (first) “built-in” static unidirectional electric drift field (illustrated by the yellow arrow labelled “E1” in Payne FIG. 11, below) that aids the movement of minority carriers from the surface layer to the substrate. As a POSITA would understand, the direction convention of the E-field will depend on the material type, due to electrons for n-type and holes for p-type.

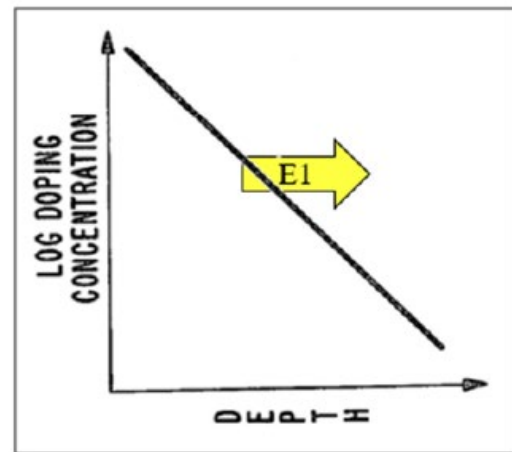
105. The figures of Ground I depict electric fields in N-wells, *e.g.*, Payne’s nested N-wells 15/18. *E.g.*, Section X.A.1.g. The electric fields would be pointing in the opposite direction in Payne’s nested P-wells.

106. In both cases, these electric fields result from the downward-sloping graded concentrations in Payne’s N-wells and P-wells and aid the movement of minority carriers (holes in N-wells, electrons in P-wells) downward to the substrate,

particularly under Patent Owner's and Applicant's position as I discuss for example in Sections X.A.1.g, X.B.1.f-g.

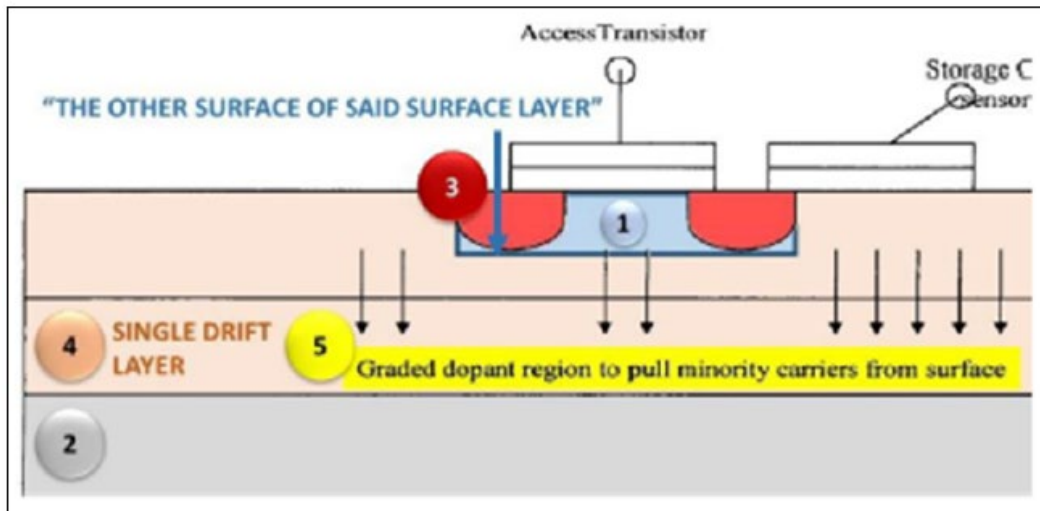


Ex.1005, FIG. 11



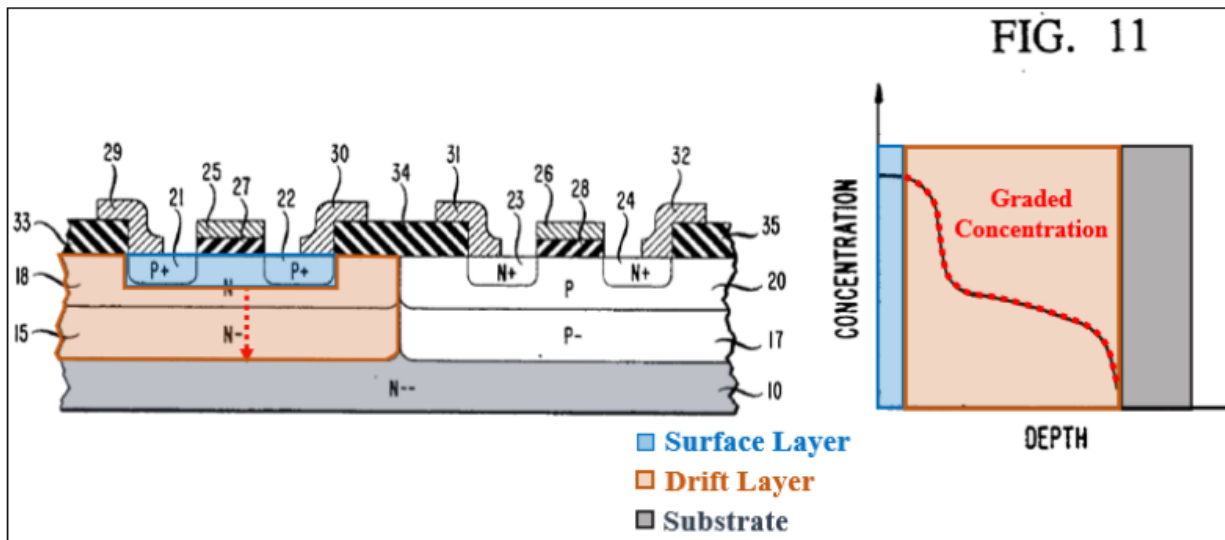
Ex.1010, FIG. 1b

107. In my opinion, Payne satisfies element [7.5] to the same extent the '502 Patent's Figure 5(b) meets it. While the '502 Patent does not disclose any single drift layer's dopant profile, Patent Owner contends that annotated Figure 5(b) below shows that "[t]he single drift layer has a graded concentration of dopants ... [that] create[s] an electric field that aids the movement of minority carriers [] from the surface layer to the substrate." Ex. 1030, 7.



Ex. 1001, FIG. 5(b); Ex. 1030, 7.

108. In light of the above, it is my opinion that Payne satisfies element [7.5] under Patent Owner's plain-meaning constructions. Section VIII. Payne's Figure 11 shows a graded-dopant concentration that is downward-sloping over the entire single drift layer (tan)—in fact, from the top of the silicon/surface layer (blue) to the bottom of the single drift layer—and thus, according to Patent Owner (and Applicant's representations to the Patent Office discussed above), this graded-dopant concentration creates a static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. Ex. 1005, FIG. 11.



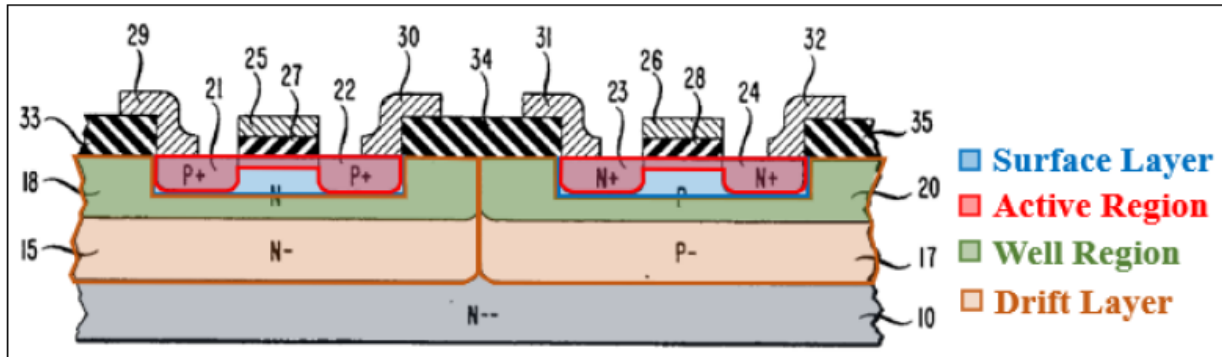
Ex. 1005, FIGS. 10-11.

- g. **Element [7.6]:** “at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.”

109. In my opinion, Payne discloses or, at a minimum, renders obvious this element.

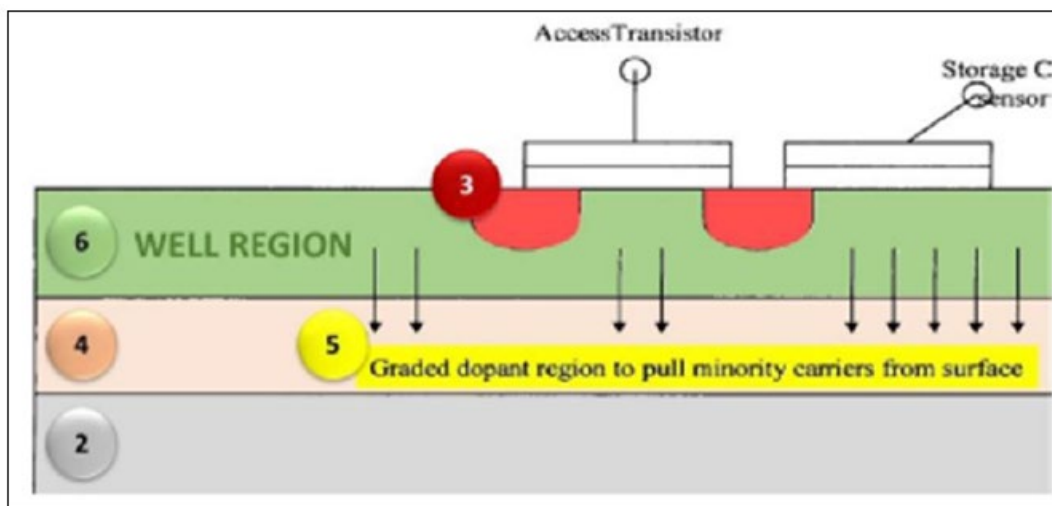
110. **Well region disposed in said single drift layer ... having a graded concentration of dopants** – As detailed above in Sections X.A.1.e-f regarding elements [7.4] and [7.5], Payne’s “tub region” 15 is an example of the claimed single drift layer. As shown below, Payne’s “surface region” 18 (green) disposed in tub region 15 (tan) is an example of a well region (a shallow well) disposed in Payne’s single drift layer (tub). Ex. 1005, 1:65-68, 4:31-39, 5:7-14, 5:44-55;

Payne's **surface region 20 (green)** is another well region disposed in a single drift layer (tub 17). *Id.*, 1:65-68, 4:63-5:14, 5:44-55; *see* Section X.B.1.e.



Ex. 1005, FIG. 10.

111. Notably, Payne satisfies element [7.6] to the same extent that Figure 5(b) of the '502 Patent, annotated by Patent Owner (as shown below), meets it:

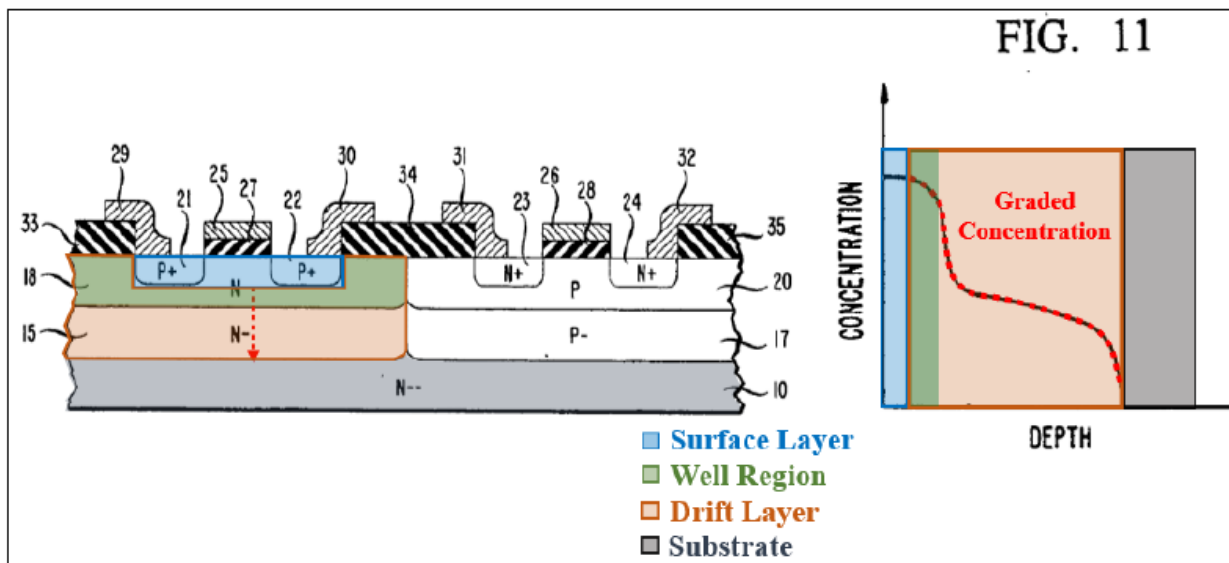


Ex. 1001, FIG. 5(b); Ex. 1030, 7.

112. As detailed above with respect to element [7.4], Payne's Figure 11 (below right) illustrates the dopant concentration measured along the red dotted line in Figure 10 (below left). As shown, Payne's well region ("surface region

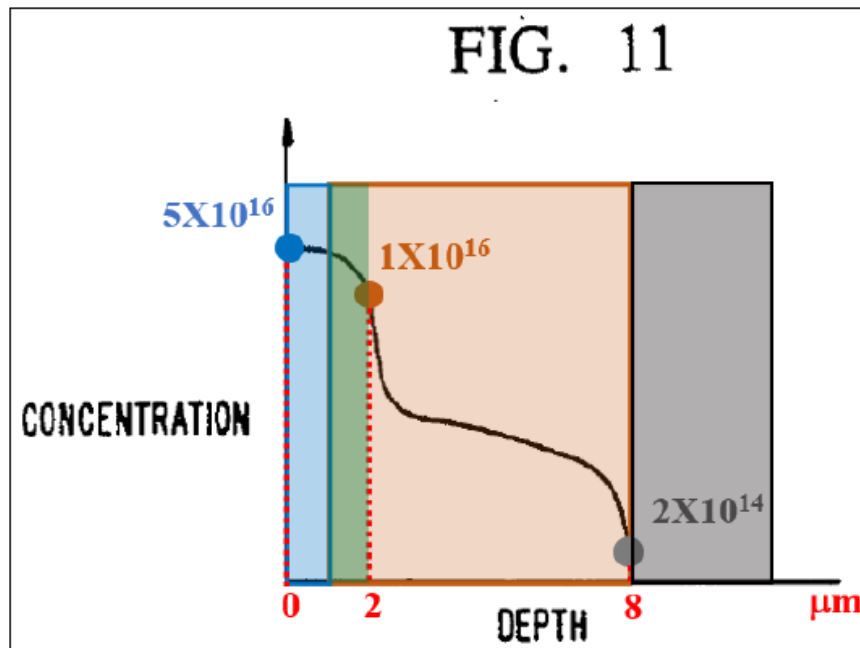
18”) (green)—disposed in the single drift layer (tub 15) (tan border)—has a graded-dopant concentration that is downward-sloping with increasing depth.

Section X.A.1.e.



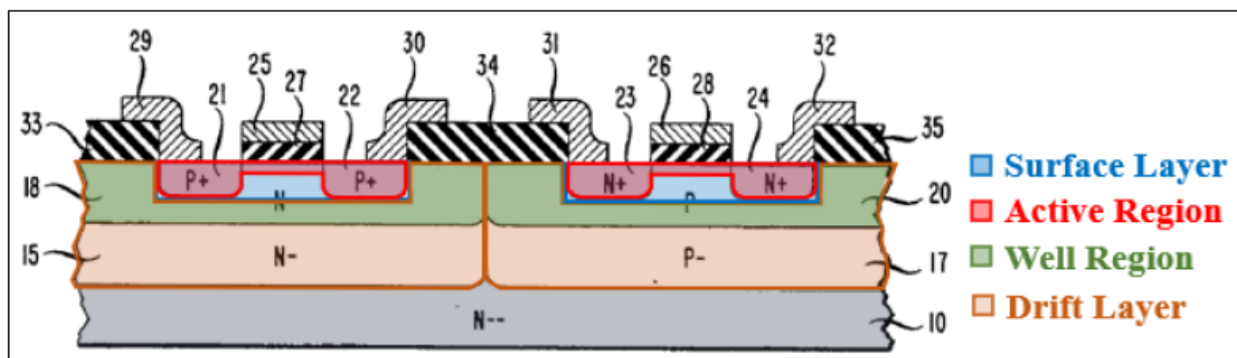
Ex. 1005, FIGS. 10-11.

113. As discussed in Section X.A.1.e, Payne discloses that Figure 11 illustrates a “*high-low implant profile*” that is downward-sloping with depth, such as from 5×10^{16} ions/cm³ (near the top surface of the silicon/surface layer (blue)) to 1×10^{16} ions/cm³ near the bottom of well 18 (green), to 2×10^{14} ions/cm³ near the bottom of the single drift layer (tub 15) (tan). *Id.*, 2:56-59, 5:48-57.



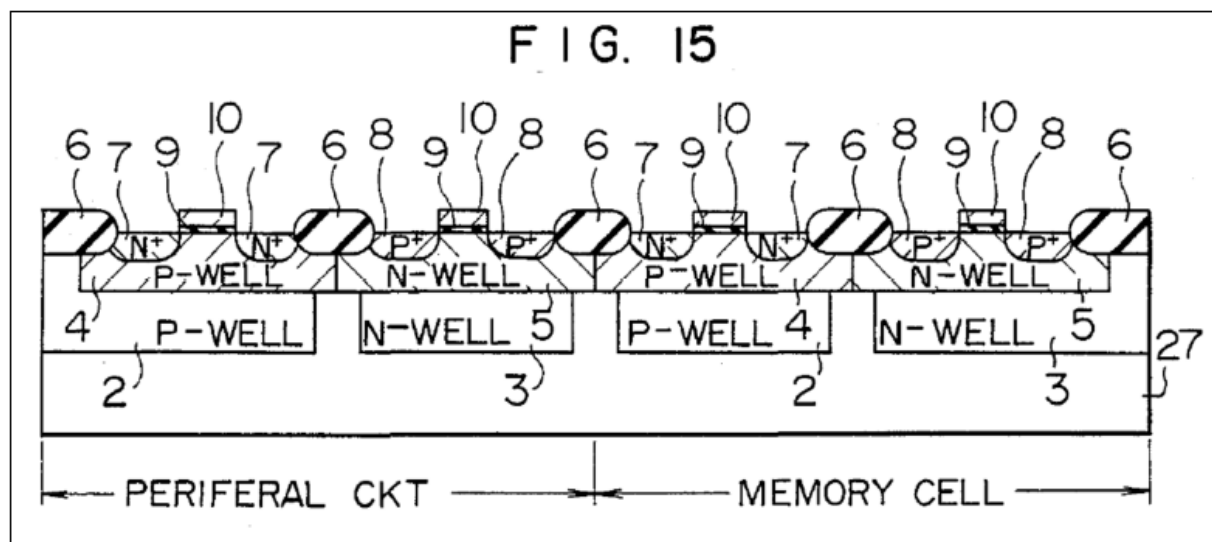
Ex. 1005, FIG. 11.

114. In my opinion and in light of the above, Payne satisfies element [7.6] under Patent Owner’s construction that the term “well region” should be accorded plain meaning and is “a doped region that surrounds the active region of a semiconductor device.” Section VIII. As shown in Figure 10 below, the well region (green) is a doped region that surrounds the surface layer (blue) and the active region (red) therein.



Ex. 1005, FIG. 10.

115. In addition, Sakai teaches a nested structure similar to Payne, which Sakai refers to as “twin double well.” *See, e.g.*, Ex. 1006, 7:19-37 (“The memory of FIG. 15 has a **twin double well** structure ... made up of the **deep** P-well region 2, the **deep** N-well region 3, the **shallow** P-well region 4 and the **shallow** N-well region 5”).



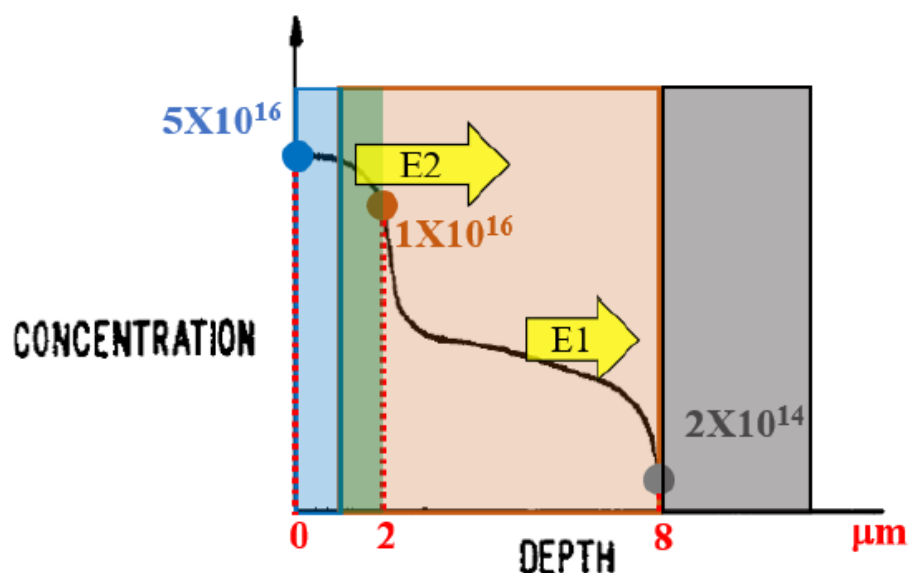
Ex. 1006, FIG. 15; 1:57-67, 5:56-6:4, FIG. 10B, FIGS. 3, 8-9, 11E. Sakai confirms that Payne’s “surface region” is a shallow well region.

116. Second static unidirectional electric drift field to aid the movement of minority carriers – According to Section X.A.1.f—including Applicant’s repeated representations during prosecution of the parent ’195 Patent, Jastrzebski and Kamins relied on by Applicant during the prosecution, and Patent Owner’s statements in its claim construction brief—the downward-sloping graded-

dopant concentration in the well region creates a (second) static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. Section X.A.1.f. Further, Payne's graded-dopant profile, including the profile in the well region, is set once the device has been fabricated and does not change, making the profile (and any resulting electric field) static, as described in Section X.A.1.f.

117. I have further annotated Payne's Figure 11 below to show the exemplary first static unidirectional electric drift field ("E1") present in a deep portion of the single drift layer (discussed in Section X.A.1.f), and a different, exemplary second static unidirectional electric drift field ("E2") present in the well region disposed in the single drift layer. See ¶¶104-105.

FIG. 11



Ex. 1005, FIG. 11.

118. I have also shown E1 and E2 as electric fields having different magnitudes, to reflect the different local slopes (gradients) of the graded-dopant profile. Ex. 1022, [0071] (“the vertical ϵ -field is established by the rate of change in the graded dopant concentration, i.e., the greater the rate of change ... the greater the intensity of the ϵ -field.”).

119. In my opinion and in light of the above, Payne satisfies Element [7.6] under Patent Owner’s plain-meaning construction of “to aid the movement of minority carriers.” Section VIII. Payne’s Figure 11 shows that the dopant concentration is downward-sloping with increasing depth over the entire well region, and thus, according to Patent Owner (and also in light of Applicant’s representations to the Patent Office, discussed in Section X.A.1.f), creates a static unidirectional electric drift field that aids the movement of minority carriers downward from the surface layer to the substrate. Ex. 1030, 2, 29.

B. Grounds II and III

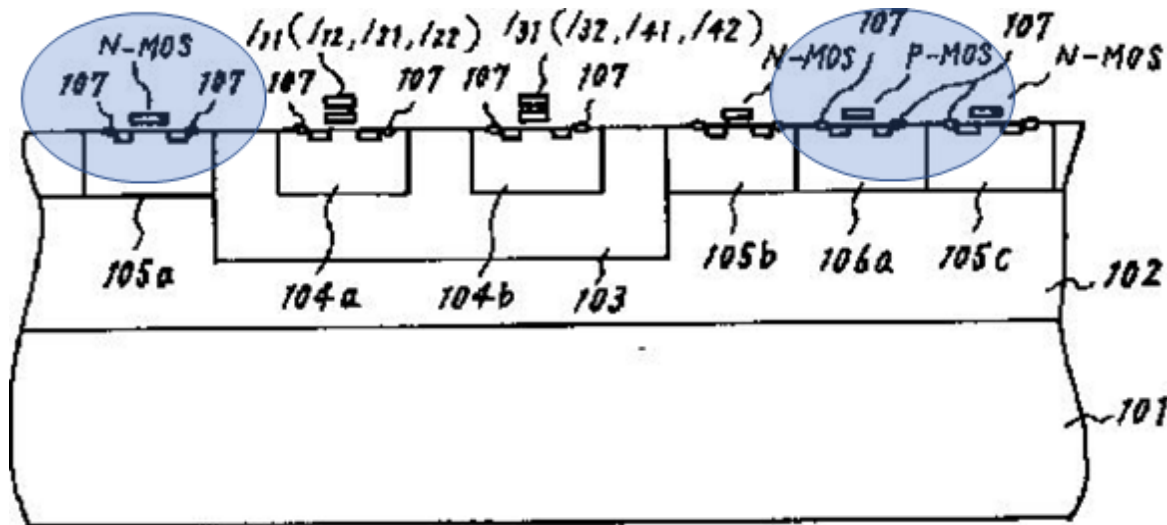
120. In my opinion, claims Onoda anticipates claims 7, 8, and 11 (Ground II), or else renders claims 7, 8, and 11 obvious (Ground III).

1. Independent Claim 7

a. Preamble: “A semiconductor device comprising:”

121. In my opinion, Onoda discloses a semiconductor device.

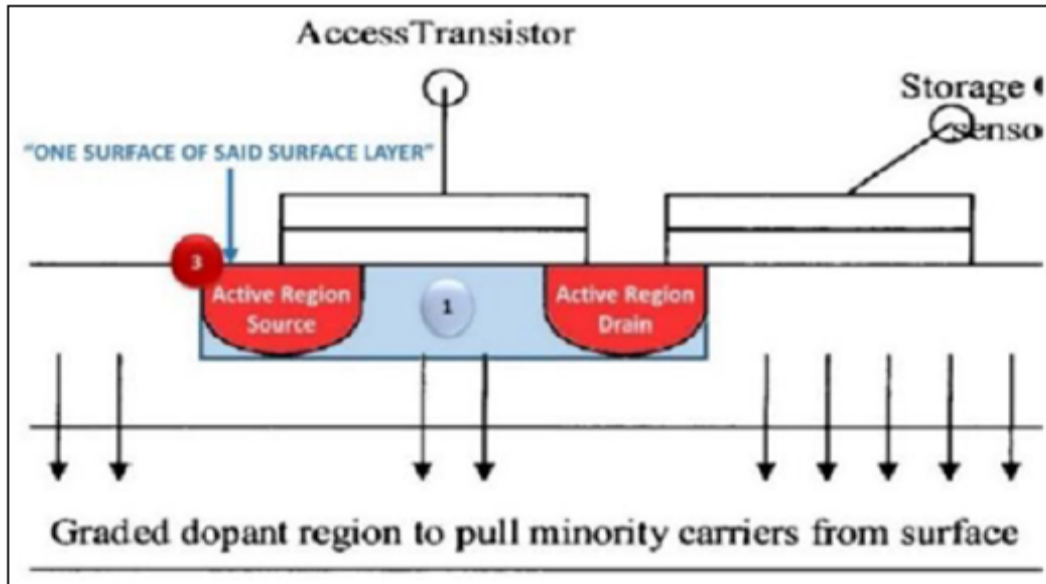
122. Onoda discloses a flash memory device formed atop a semiconductor substrate 100 that includes N-channel MOS (NMOS) transistors and P-channel MOS (PMOS) transistors in its peripheral circuitry. *See, e.g.,* Ex. 1042, [0041], [0044]-[0045], [0052], FIG. 3, claim 2.



Ex. 1042, FIG. 3. Onoda mentions that one of the objectives of the invention “is to provide a semiconductor integrated device” Ex. 1042, [0006].

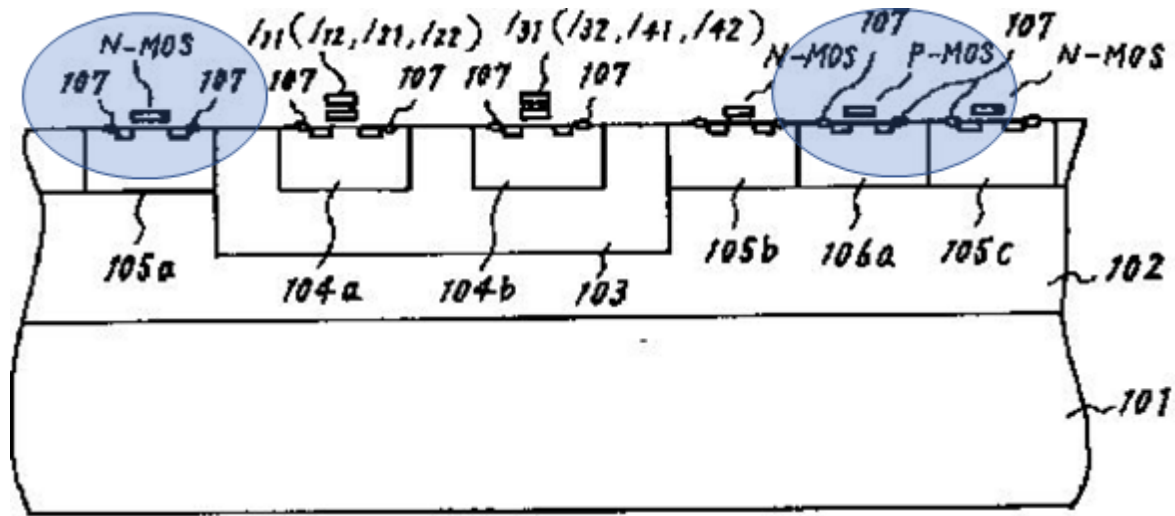
b. Element [7.1]: “a surface layer;”

123. In my opinion, Onoda discloses or else renders obvious this element. According to Patent Owner, a “surface layer” is “a layer at the surface of the silicon” (or “a layer at the surface of the semiconductor device”)—which Patent Owner annotated in blue in Figure 5(b) of the ’502 Patent below—“where the active region [(red)] is located.” Ex. 1030, 6, 9, 12, 13; Section VIII; Section X.A.1.b.

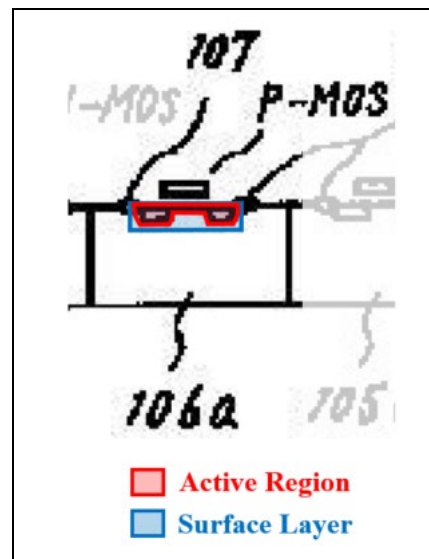
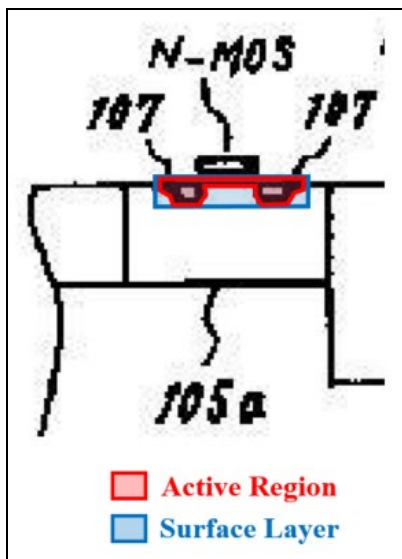


Ex. 1001, FIG. 5(b); Ex. 1030, 7, 12.

124. In my opinion, Onoda satisfies element [7.1] to the same extent that Figure 5(b) of the '502 Patent meets it. Onoda's Figure 3 depicts how the flash memory disclosed in Figure 1 is formed on the semiconductor substrate 100. Ex. 1042, [0043]. Onoda discloses at least one N-channel MOS transistor (labeled as N-MOS in Figure 3) and at least one P-channel MOS transistor (labeled as P-MOS in Figure 3). Ex. 1042, FIG. 3, [0055], [0044].



Ex. 1042, FIG. 3. As I have indicated below, Onoda's surface layer (blue) is at the surface of semiconductor substrate 100, and the source and drain regions (red) of Onoda's N-MOS and P-MOS transistors are located in that surface layer.



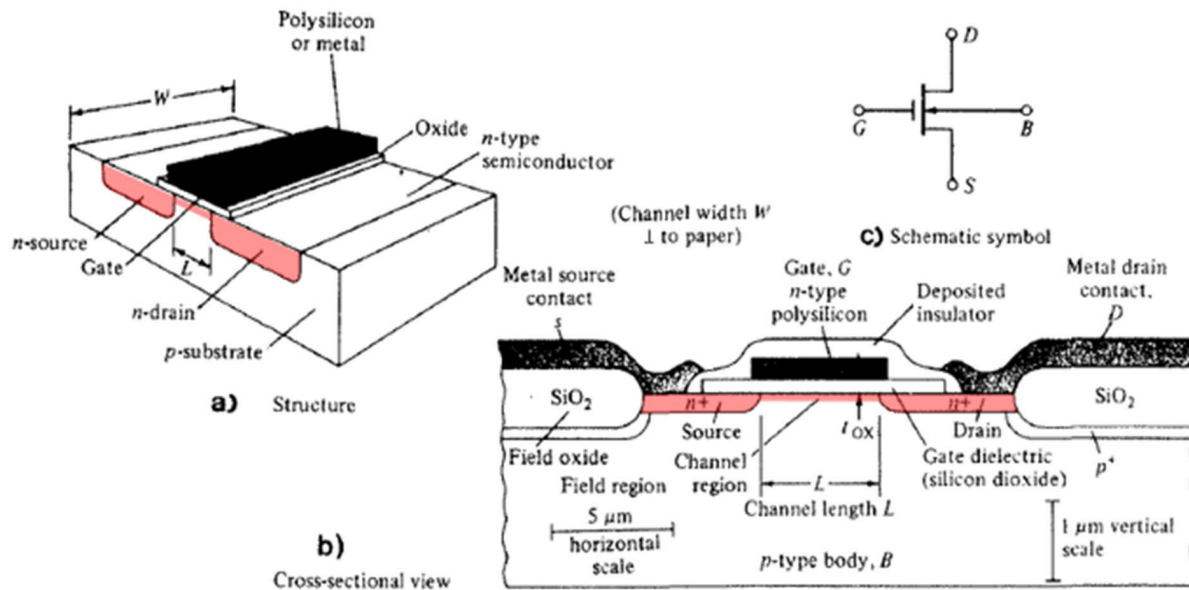
NMOS Active Regions / Surface Layer PMOS Active Regions / Surface Layer

Ex. 1042, FIG. 3 (excerpts of N-MOS (left) and P-MOS (right)).

125. In my opinion, as shown above, a POSITA would have understood that each of the N-channel MOS transistors have a surface layer (blue) that contains a source region, a drain region, and a channel region positioned between the source region and the drain region (collectively, red), which are formed in a P-type well region 104a, 104b, 105a, 105b, or 105c. Ex. 1042, [0042], [0044], [0045], [0055], FIG. 3. In my opinion, a POSITA would have understood that each of the P-channel MOS transistors has a surface layer (blue) that contains a source region, a drain region, and a channel region positioned between the source region and the drain region (collectively, red), which are formed in an N-type well region 106a, 106b, or 106c. *Id.*, [0042], [0055], [0044].

126. Claim 2 of Onoda requires a “MOS transistor of a first conductivity type” and another “MOS transistor of the second conductivity type.” Ex. 1042, Claim 2. In my opinion, a POSITA would have understood this claim to require one of the MOS transistors to be an N-channel MOS transistor and the other MOS transistor to be a P-type MOS transistor. Claim 2 further requires each MOS transistor to have a source region, as well as a drain region that is separate from the source region. *Id.*

127. Consistent with this, Wolf teaches that a MOS transistor consists of a source region, a drain region, and a channel region between the two (as I have indicated in Fig. 5-1 red below). Ex. 1008B, 299.



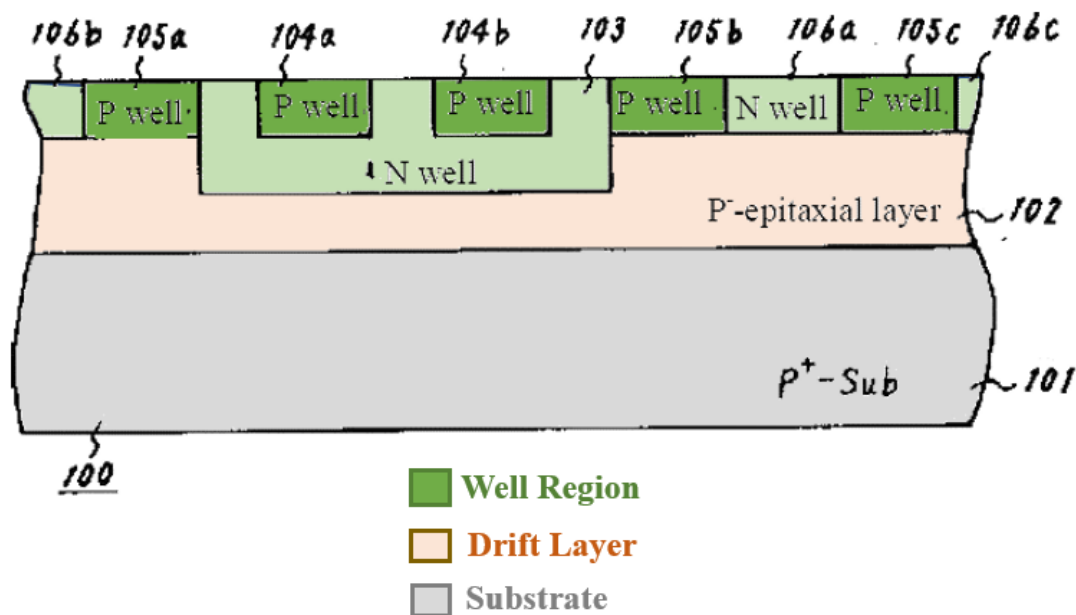
Ex. 1008B, FIG. 5-1; *id.*, 298-301, 374, FIGS. 5-2, 6-4. As a result, a POSITA would have understood that each of the N-channel MOS transistors disclosed in Onoda has a surface layer (blue) that contains a source region, a drain region, and a channel region positioned between the source region and the drain region (collectively, red), which are formed in a P-type well region 104a, 104b, 105a, 105b, or 105c. Ex. 1042, [0042], [0044], [0045], [0055], FIG. 3. Likewise, a POSITA would have further understood that each of Onoda's PMOS transistors has a surface region (blue) that contains a source region, a drain region, and a channel region positioned therebetween (collectively, red), which are formed in an N-type well region 106a, 106b, or 106c. *Id.*, [0042], [0055], [0044]. Thus, Onoda

discloses a surface layer (blue) that matches the surface layer Patent Owner identified in Figure 5(b) of the '502 patent.

128. In addition, Onoda discloses that memory cells are formed on the disclosed surface layer. According to Onoda, “the memory cells I₁₁, I₁₂, I₂₁, and I₂₂ that structure the block 2a are formed in the second well region 104a, and the memory cells I₃₁, I₃₂, I₄₁, and I₄₂ that form the block 2b are formed in the second well region 104b.” *Id.*, [0043]. Onoda discloses that “I₁₁ through I₄₂ is each a memory cell having a source region comprising an N-type diffusion layer, a drain region comprising an N-type diffusion layer that is separate from the source region, a floating electrode formed over a channel region that is positioned between the source region and the drain region.” *Id.*, [0029].

c. Element [7.2]: “a substrate;”

129. In my opinion, Onoda discloses the claimed “substrate.” Specifically, Onoda discloses “a semiconductor substrate 100” (grey below) in Figure 2 on which the flash memory is formed. Ex. 1042, [0041]. Specifically, “FIG. 2 depicts critical portions of the semiconductor **substrate** that is applied to the first embodiment of the present invention” *Id.* Within semiconductor substrate 100, “101 is a first semiconductor layer made from a heavily-doped (for example, about $1 \times 10^{19}/\text{cm}^3$) P-type silicon **substrate**” *Id.*

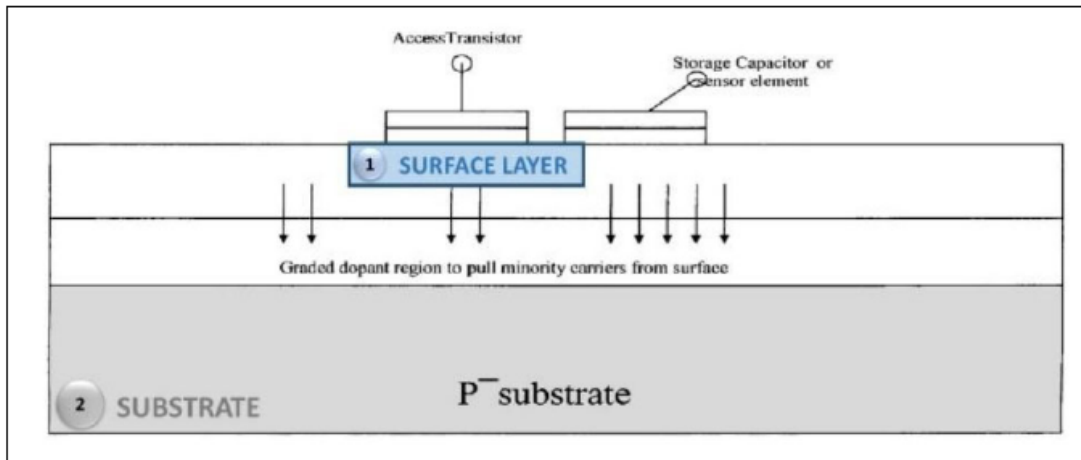


Ex. 1042, FIG. 2,⁵ [0046], [0047], FIGS. 3, 4.

130. In my opinion, Onoda satisfies element [7.2] under Patent Owner's proposed construction of "plain and ordinary meaning [*i.e.*] 'an underlying layer.'"

Section VIII. Onoda's substrate also matches Patent Owner's identification of substrate (grey) in Figure 5(b) of the '502 Patent.

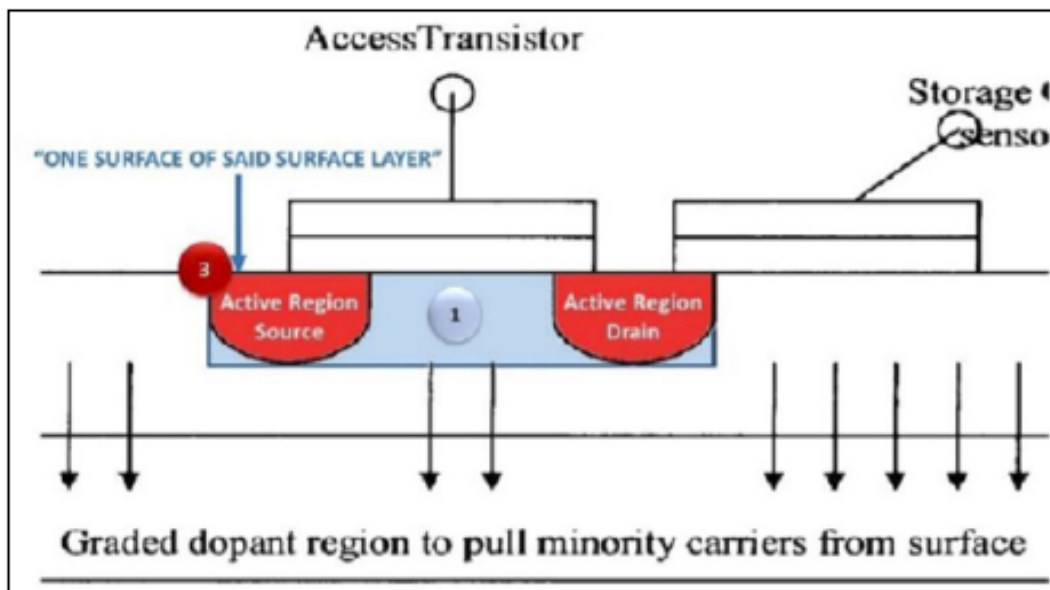
⁵ While the legend here labels "Well Region" in green, for clarity, I have indicated N-Well regions in light green whereas I have indicated P-Well regions in dark green.



Ex. 1030, 6-7, 16-17 (well region and drift layer can be part of substrate); Ex. 1001, FIG. 5(b).

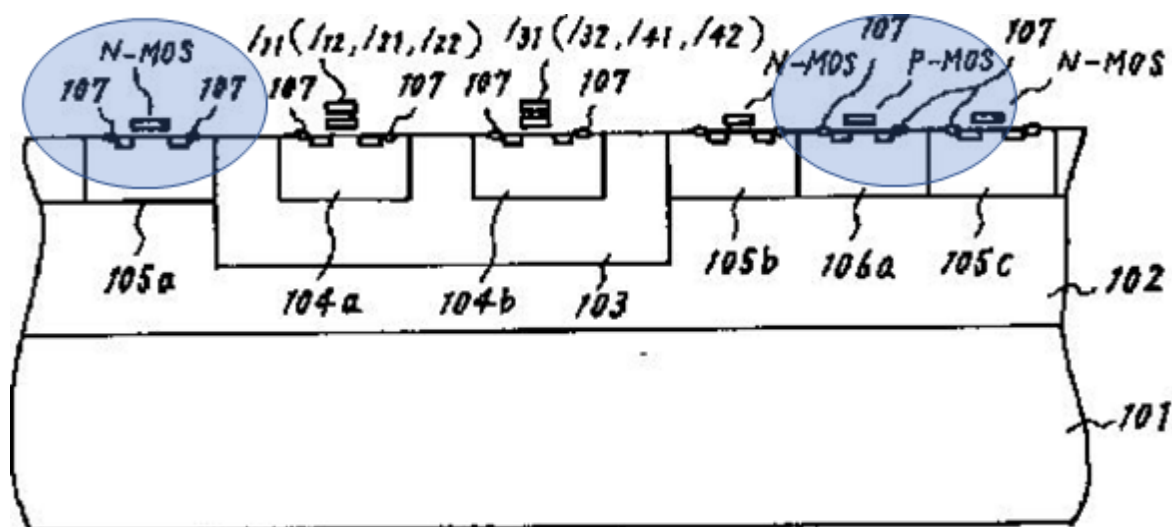
- d. Element [7.3]: “an active region including a source and a drain, disposed on one surface of said surface layer;”**

131. In my opinion, Onoda discloses or else renders obvious this element. As described in Section X.A.1.d, according to Patent Owner, Figure 5(b) of the '502 Patent depicts an active region (red) “disposed on one surface [(top surface)] of said surface layer.”



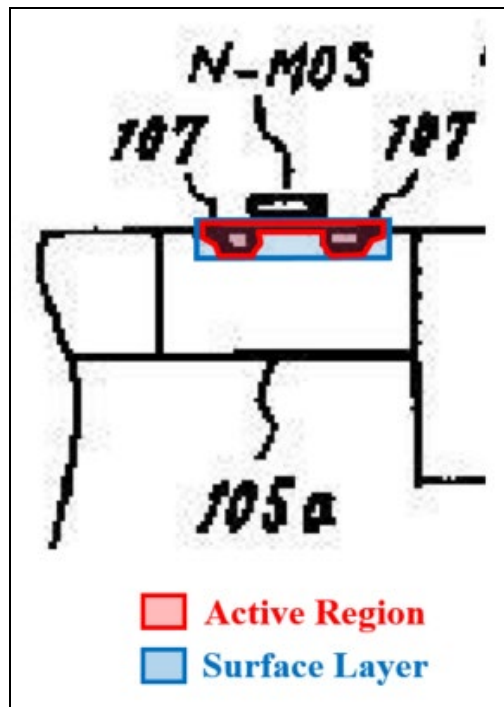
Ex. 1001, FIG. 5(b); Ex. 1030, 6-7, 10-12; Section X.A.1.d.

132. In my opinion, Onoda satisfies element [7.3] under Patent Owner's interpretation. Figure 3 below illustrates an "N-channel" MOS transistor with source/drain regions (left) in a doped P-well 105a, and a "P-channel" MOS transistor with source/drain regions (right) in a doped N-well 106a. Ex. 1042, FIG. 3, [0042], [0055], [0044]; Section X.B.1.b.



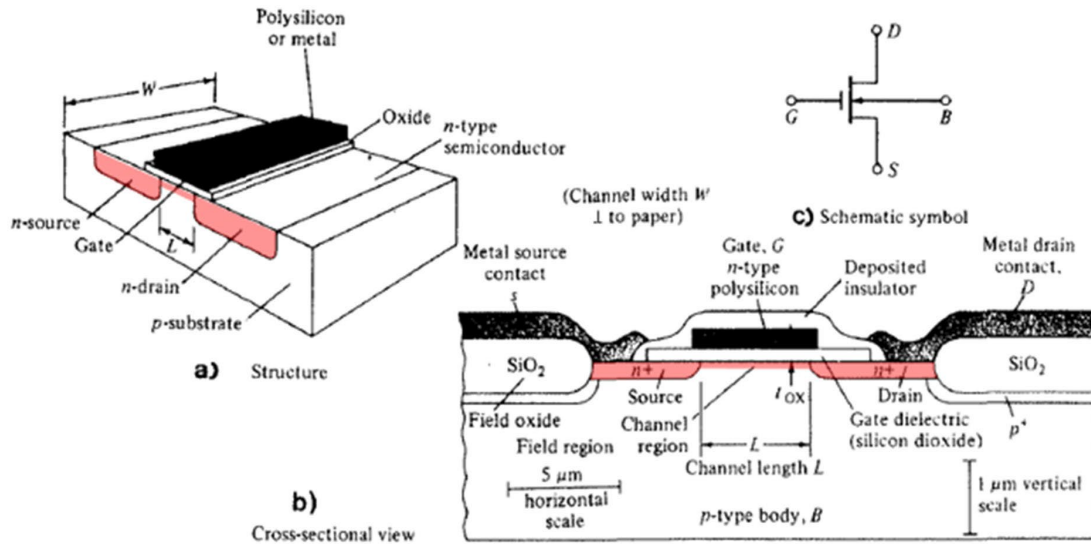
133. As Wolf explains, the source/drain regions of a p-channel or n-channel transistor, together with the channel region between them, form an active region. Section X.A.1.d; Ex. 1008B, 299 (“The top surface of the [silicon substrate] body consists of active or transistor regions as well as passive or (field) regions. The *active regions* are those in which transistor action occurs; i.e., the *channel* and the heavily doped *source* and *drain* regions.”), 300, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e).

134. For clarity, an enlarged version of Onoda’s active regions and surface layers is below. The active region (red) of each of Onoda’s transistors is disposed on one surface (top surface) of a corresponding surface layer (blue), exactly as depicted in Patent Owner’s annotated Figure 5(b) above. Section X.B.1.b.



Ex. 1042, FIG. 3 (excerpted, annotated).

135. In my opinion, Onoda satisfies element [7.3] under Patent Owner’s position that the term “active region” means “a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed” (Section VIII) because the active region of a MOS transistor is “[its] channel and [its] heavily doped source and drain regions,” highlighted in red below, which is consistent with how I map Onoda’s active regions. Ex. 1008B, 299.

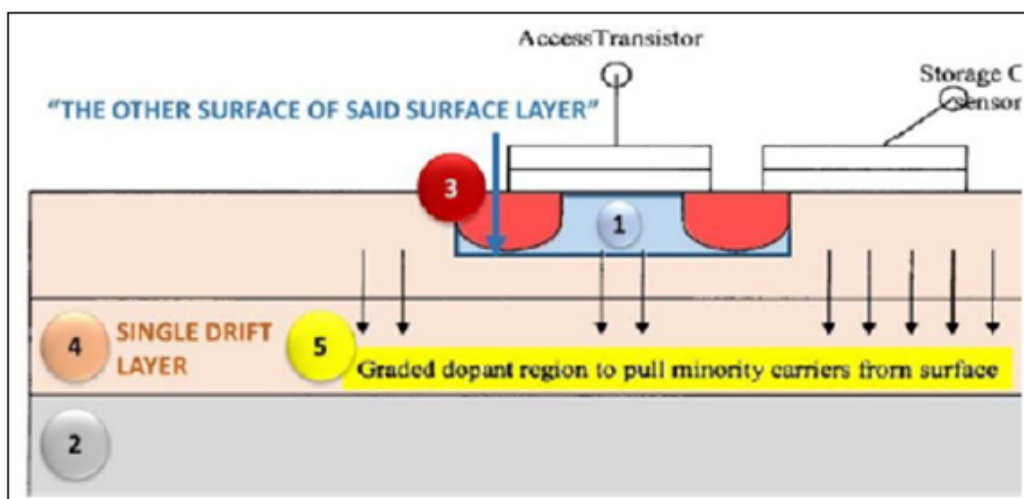


Ex. 1008B, FIG. 5-1; *id.*, 298-301, 374, FIGS. 5-2, 6-4.

- e. **Element [7.4]: “a single drift layer disposed between the other surface of said surface layer and said substrate,”**

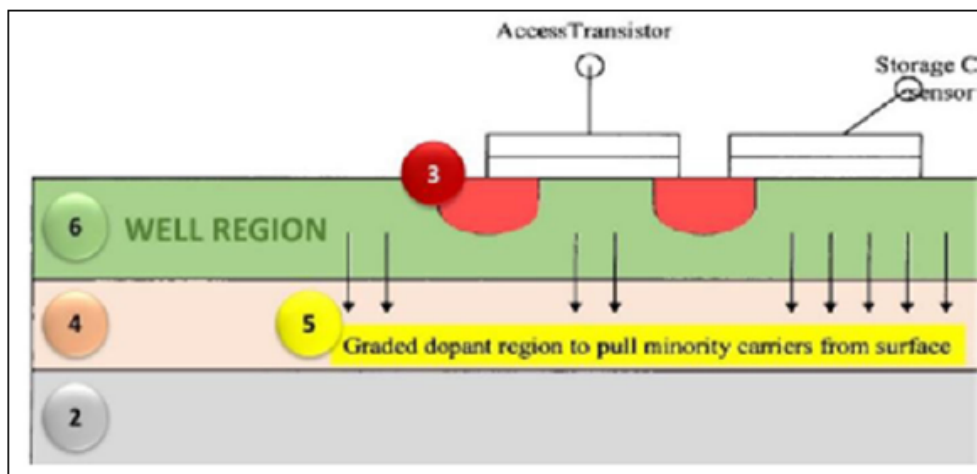
136. In my opinion, Onoda discloses or, at a minimum, renders obvious this element.

137. **Single drift layer** – As described in Section X.A.1.e, according to Patent Owner, Figure 5(b) of the '502 Patent depicts a single drift layer (tan) “disposed between the other surface [(bottom surface)] of said surface layer [(blue)] and said substrate [(grey)]”:



Ex. 1001, FIG. 5(b); Ex. 1030 at 7.

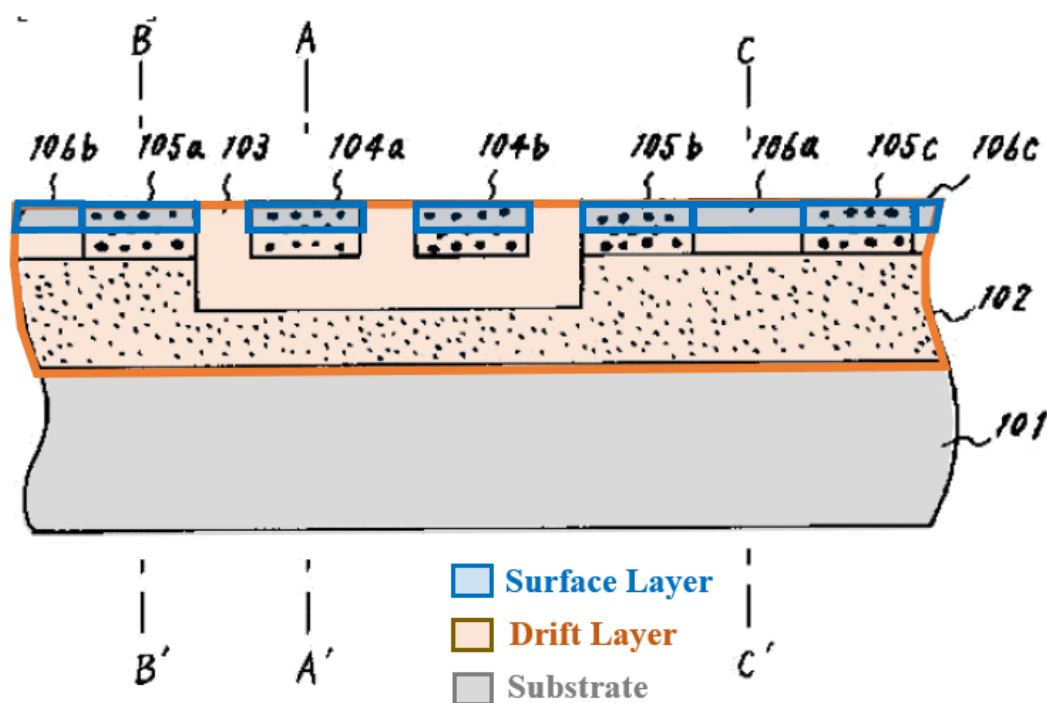
138. The single drift layer in Figure 5(b) has well region (green) disposed in it, forming a nested structure, as required by claim 7 (*see* element [7.6]):



Ex. 1001, FIG. 5(b); Ex. 1030, 7; *id.*, 11 (“the ‘well region’ is part of the ‘single drift layer.’”).

139. Onoda discloses a single drift layer to the same extent Figure 5(b) of the '502 Patent does. In Figure 3 of Onoda, the second semiconductor layer 102 is an example of the claimed drift layer. This single drift layer (tan) is “disposed

between ‘the other surface [(bottom surface)] of said surface layer [(blue)]’ and said substrate [(grey)]” under Patent Owner’s interpretation, and in exactly the same way as depicted in Patent Owner’s annotated Figure 5(b) above. This is demonstrated in Figure 8 of Onoda, which shows the manufacturing process of semiconductor substrate 100. *See* Ex. 1042, [0041]-[0051].



Ex. 1042, FIG. 8, [0041], [0046], [0047]. Onoda’s P-type well regions 105a, 105b, and 105c and N-type well regions 103, 106a, 106b, and 106c are disposed in a single drift layer (tan) disposed between a surface layer (blue) and the substrate (grey). *Id.*; Section X.B.1.b.

140. In my opinion, Onoda meets all of the other claim requirements associated with the single drift layer to the same extent Figure 5(b) of the ’502

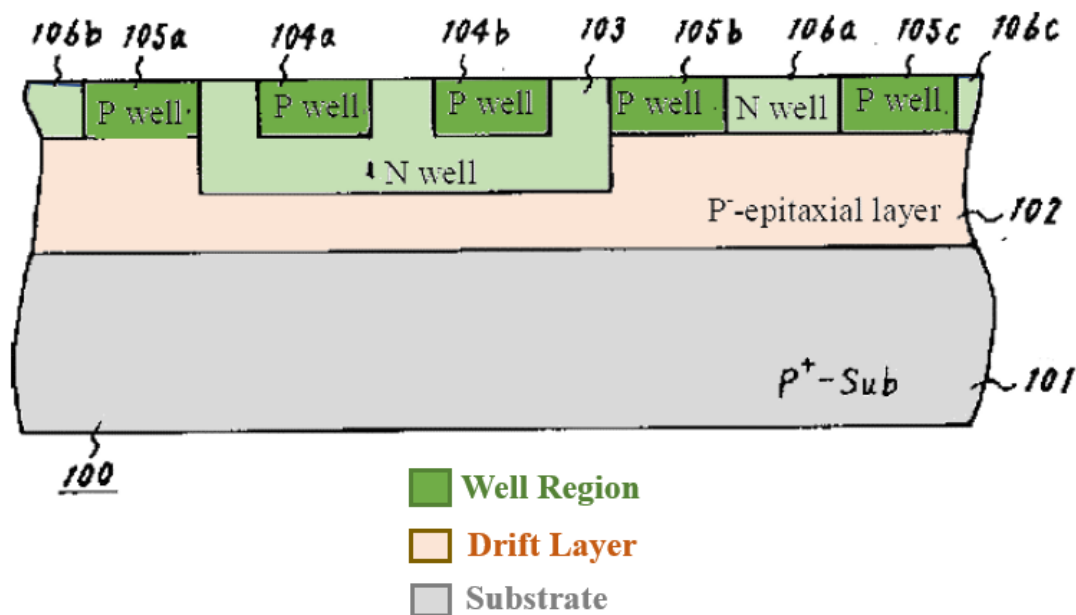
Patent meets them, as explained below. *See* elements [7.5]-[7.6]. Notably, as detailed in element [7.5], the second semiconductor layer 102 in Onoda is a *single* drift layer because it has a graded-dopant concentration that, according to Patent Owner, creates a unidirectional electric drift field that aids the movement of minority carriers in a *single* direction—from the surface layer to the substrate. Ex. 1030, 7: Ex. 1046, 253-54, 289-290; Section X.B.1.f.

- f. **Element [7.5]: “said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and”**

141. In my opinion, Onoda discloses or, at a minimum, renders obvious this element.

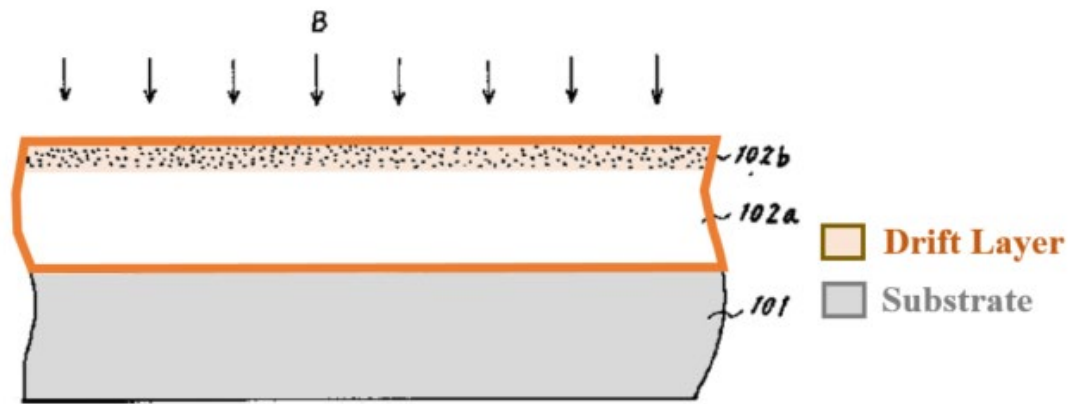
142. **Graded concentration of dopants** – Onoda discloses a single drift layer having a graded concentration of dopants extending between the surface layer and the substrate. In Onoda, “FIG. 2 depicts critical portions of the semiconductor substrate that is applied to the first embodiment of the present invention; . . .” Ex. 1042, [0041]. Within the semiconductor substrate 100, “101 is a first semiconductor layer made from a heavily-doped (for example, about $1 \times 10^{19}/\text{cm}^3$) P-type silicon substrate, and 102 is a P-type second semiconductor layer having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer 101 (for example $1 \times 10^{15}/\text{cm}^3$, and may be between $1 \times$

$10^{15}/\text{cm}^3$ and $1 \times 10^{18}/\text{cm}^3$), deposited through epitaxial deposition to a thickness of between 1 and 10 μm onto the surface of the first semiconductor layer.” *Id.*



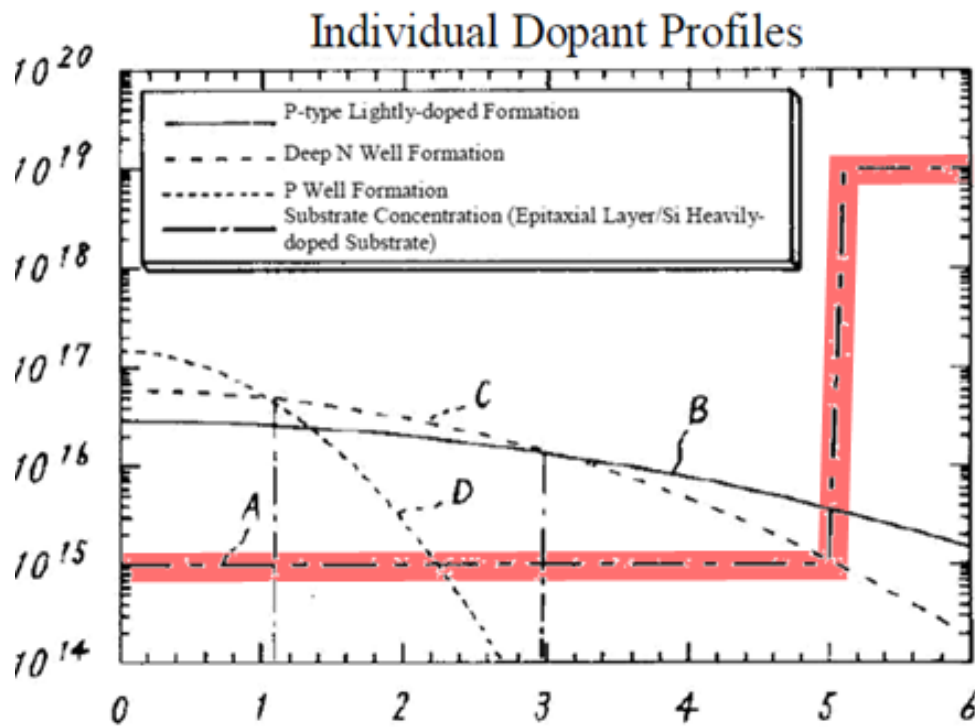
Ex. 1042, FIG. 2.

143. Onoda discloses how the P-type semiconductor layer 102 is formed. As illustrated in Figure 4, a lightly-doped P-type epitaxial layer 102a with a dopant concentration of $1 \times 10^{15}/\text{cm}^3$ is formed with a thickness of about 5 μm through epitaxial deposition onto the surface of a first semiconductor layer 101, which comprises a heavily-doped P-type silicon substrate (silicon wafer) with a dopant concentration of $1 \times 10^{19}/\text{cm}^3$. Ex. 1042, [0046].



Ex. 1042, FIG. 4.

144. The concentration distribution from the surface of the epitaxial layer 102a into the first semiconductor layer 101 at this stage of fabrication is depicted by the dash-dot line A in Figure 9, which I have indicated in red below. *Id.*



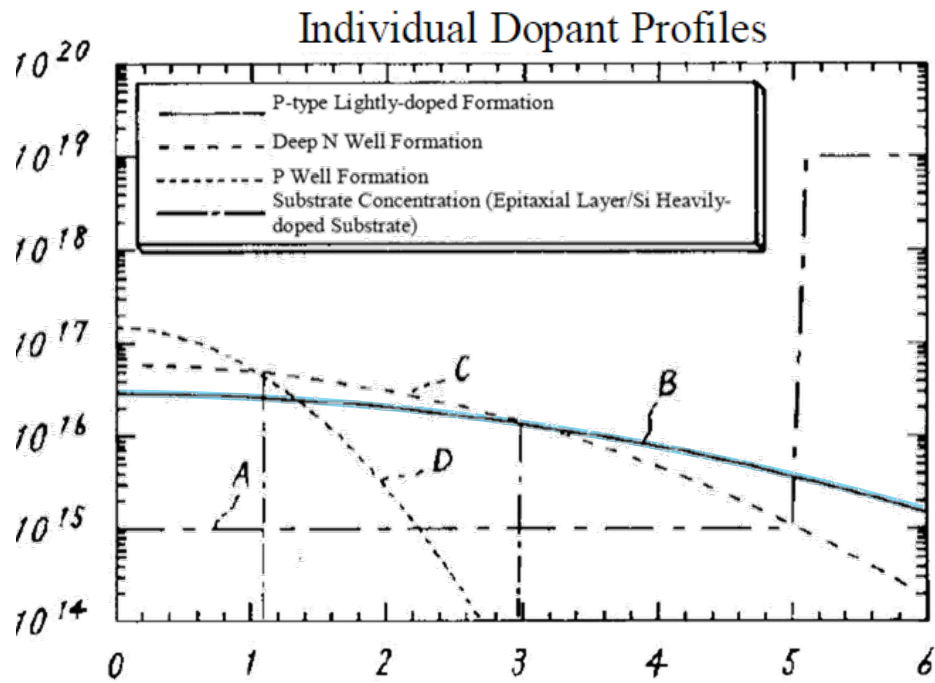
Ex. 1042, FIG. 9.

145. According to Onoda, a P-type dopant (e.g., boron B) is implanted into the epitaxial layer 102a at 100 KeV and 1×10^{12} through $1 \times 10^{13}/\text{cm}^2$ to form an ion implantation layer 102b. Ex. 1042, [0047]. Thereafter, a heat treatment is carried out for 10 hours at between 1130° and 1180° C in a nitrogen gas ambient to thermally diffuse the dopant (boron) in the ion implantation layer 102b to produce a lightly-doped P-type second semiconductor layer 102. *Id.*



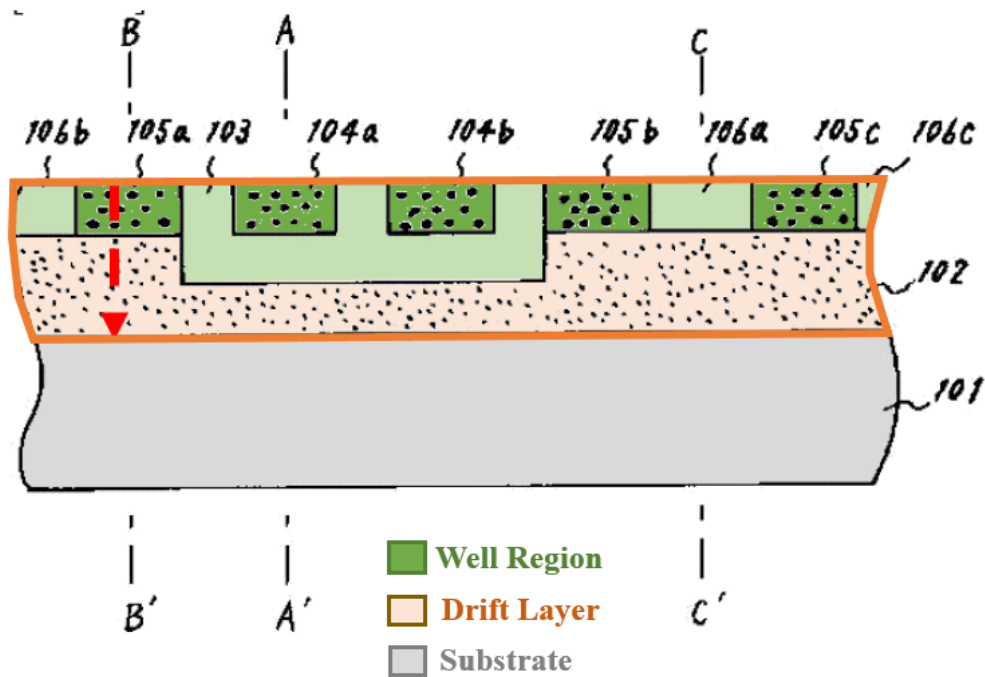
Ex. 1042, FIG. 5, [0046], [0047].

146. As illustrated in Figure 5, the dopant concentration of the epitaxial layer 102a, as a whole, is between 1×10^{16} and $1 \times 10^{18}/\text{cm}^3$. At this time, the dopant concentration of boron (B) is depicted by the solid line B in Figure 9, which I have indicated in blue below.

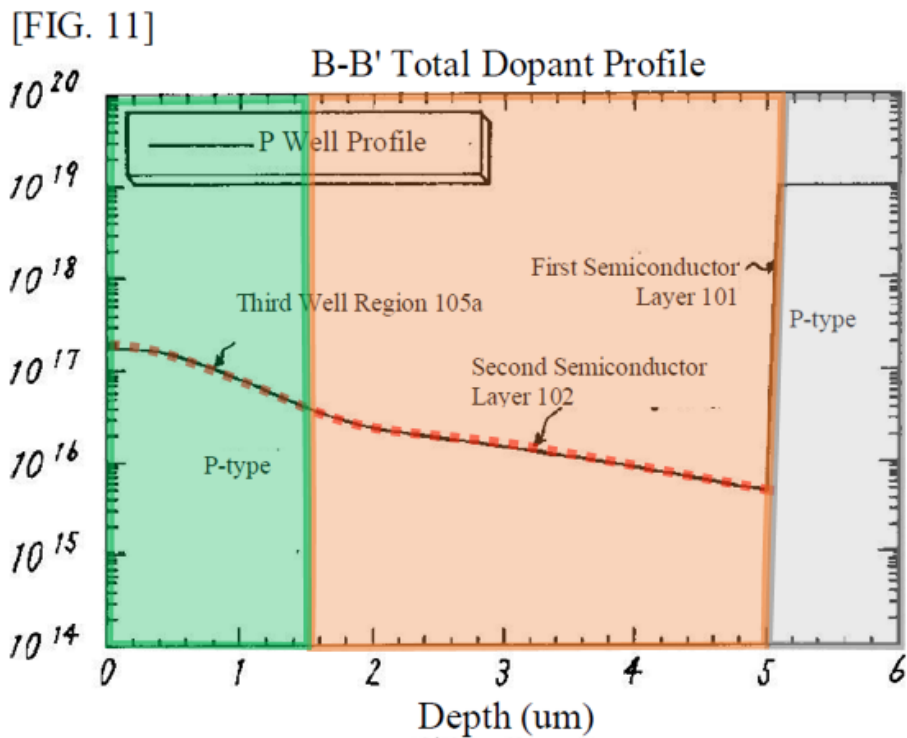


Ex. 1042, FIG. 9.

147. As further discussed below in Section X.B.1.g (element [7.6]), P-well 105a, 105b, 105c, 104a and 104b (dark green) and N-well regions 103, 106a, 106b and 106c (light green) are formed in the semiconductor layer 102 resulting in the structure depicted in Figure 8 below. *Id.*, [0042], [0048]-[0050].



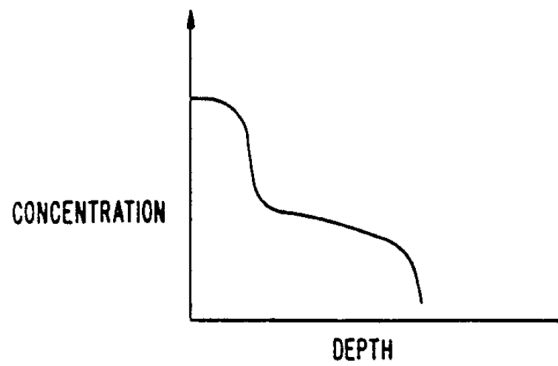
Ex. 1042, FIG. 8. The dopant profile appearing in the B-B' cross-section in Figure 8 is shown in Figure 11 below. *Id.*, [0052]. As Figure 11 illustrates, “both the third well region 105a and the second semiconductor layer 102 are of the same conductivity type, that is, P-type, so there is no clear boundary between the third well region 105a and the second semiconductor layer 102, but rather *the dopant concentration falls off smoothly.*” *Id.*



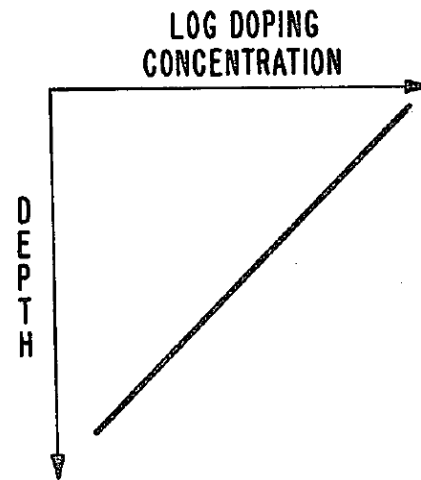
Ex. 1042, FIG. 11.

148. In my opinion a POSITA would have understood that the dopant concentration in Onoda's P-type lightly doped semiconductor layer 102 would *gradually decrease* across Onoda's single drift layer because it is formed through ion implantation techniques and thermal diffusion techniques.

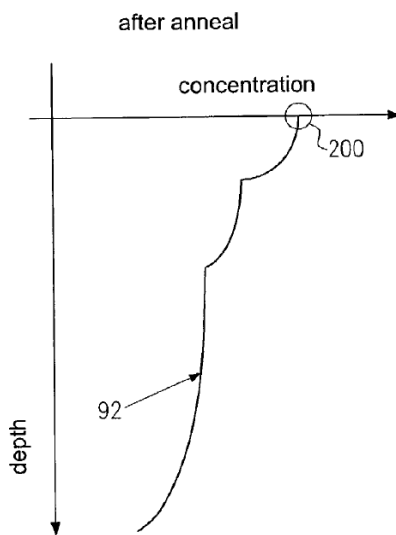
149. Indeed, a downward-sloping graded-dopant concentration formed through ion implantation and thermal diffusion was well-known in the art. Such gradients were disclosed in many prior art references, such as Payne, Kawagoe, Wieczorek and Jastrzebski, as shown below.



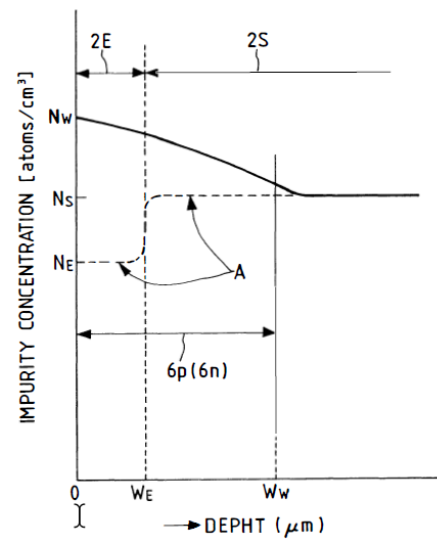
Payne, Figure 11



Jastrzebski, Figure 1b



Wieczorek, Figure 2b



Kawagoe, Figure 17

Ex. 1005, FIG. 11, 3:28-42, 4:19-39, 5:7-17; Ex. 1007, FIG. 17, 15:62-16:2, 17:31-61; Ex. 1038, FIG. 2b, [0008], [0010]-[0011]; Ex. 1010, FIG. 1b, 5:5-27; 9:2-8. Significantly, Payne's Figure 11 illustrates a graded-dopant profile that is

downward-sloping over a *nested well structure* similar to Onoda's P-type lightly doped semiconductor layer 102, as detailed under X.A.1.e-f.

150. Additionally, the '502 Patent mentions "linear [and] quasi linear" dopant gradients only once and does not describe how to make them, *see* Ex. 1001, 2:40-42, confirming implementing them in CMOS devices was well-known. The '502 Patent also lists linear/quasi-linear among a few likewise well-known gradients without giving any reason to use one over another. *Id.*, 2:40-42.

151. It was well-known that various ion-implantation and thermal drive-in processes enable different dopant profiles to be readily engineered and fabricated as needed, Ex. 1008A, 371, 373 (observing that that "[c]omplex-doping profiles can be produced" using ion implantation), and because the prior art is replete with teachings on how to form downward-sloping dopant concentrations, as in Kawagoe, Payne, Jastrzebski and Wieczorek.

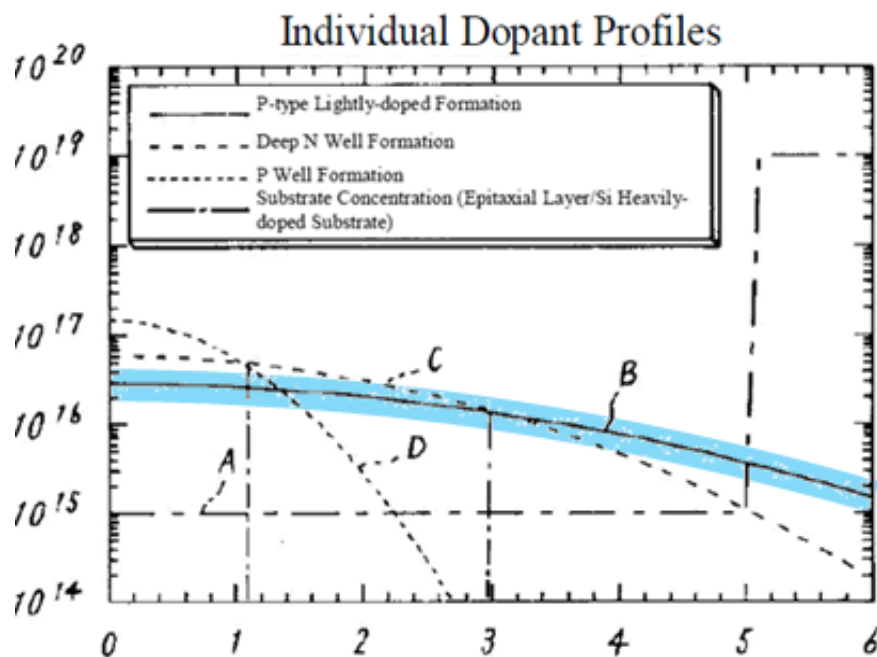
152. Further, the '502 Patent specification mentions various dopant gradients (including ones with a one-way slope, e.g., quasi-linear) and does not illustrate or otherwise describe how to make them, *see* Ex. 1001, 2:40-42, confirming that such gradients were well-known and, in my opinion, a POSITA would have known how to manufacture a CMOS device having them.

153. **First static unidirectional electric drift field to aid the movement of minority carriers** – As illustrated in Figure 5, the dopant concentration of the

epitaxial layer 102, as a whole, is between 1×10^{16} and $1 \times 10^{18}/\text{cm}^3$. Ex. 1042, [0046]-[0047].

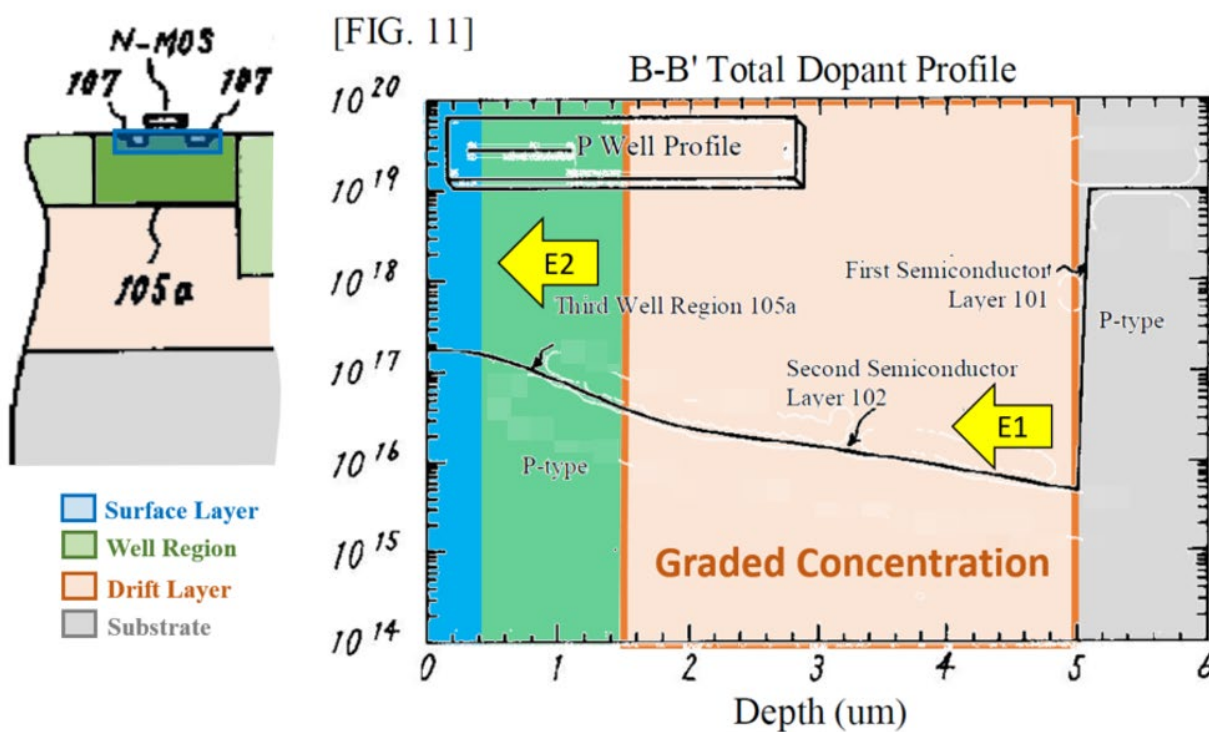


Ex. 1042, FIG. 5. At this time, the dopant concentration of boron (B) is depicted by the solid line B shown in Figure 9, which I have indicated in blue below. *Id.*, [0047].



Ex. 1042, FIG. 9.

154. As discussed above with regard to element [7.4], Onoda discloses a single drift layer (tan) having a downward-sloping dopant concentration extending between the surface layer (blue—*i.e.*, at the 0 μm depth level) and the substrate (grey at depth of 5 μm). Ex. 1042, [0052]; Section X.B.1.e. Onoda's Figure 11, which I have annotated below, depicts the exemplary first static unidirectional electric drift field ("E1") described in Section X.A.1.f, at a depth corresponding to Onoda's second semiconductor layer 102 (tan).



Ex. 1042, FIG. 11, [0041], [0046], [0047], [0052].

155. Thus, according to Section X.A.1.f—including Applicant's repeated representations to the Patent Office and the Jastrzebski and Kamins cited art relied on by Applicant—such a downward-sloping graded-dopant concentration creates a

“built-in” unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate. *See* Section X.A.1.f. I note that the electric fields in Figure 11 are left-facing, because the downward-sloping graded-dopant concentration is in a P-Well (rather than N-well). Nonetheless, as discussed in Section X.A.1.f, the electric fields aid the movement of minority carriers (in this case, electrons in a P-well) from the surface layer to the substrate, as required.

156. Such a profile is created through ion implantation techniques and thermal diffusion techniques, and thus the profile (and any resulting electric drift field) is static—it is set once the transistor has been fabricated and does not change afterwards. Section X.A.1.f. As discussed in Section X.A.1.f, Applicant described the term “static” similarly during prosecution. Ex. 1046, 318 (citing Ex. 1009), 333 (same).

157. It is my opinion, in light of the above, that Onoda satisfies Element [7.5] under Patent Owner’s plain-meaning constructions. Section VIII. Onoda’s graded-dopant concentration is downward-sloping over the entire single drift layer (tan)—in fact, from the top of the silicon/surface layer (blue) to the bottom of the single drift layer—and thus, according to Patent Owner (and also in light of Applicant’s representations to the Patent Office discussed above), has a static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate.

- g. Element [7.6]: “at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.”

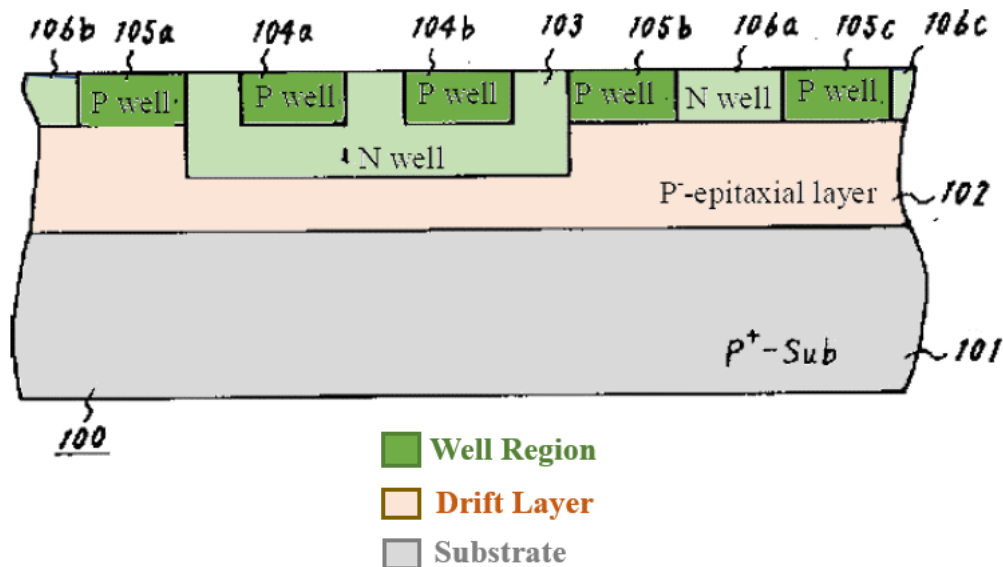
158. In my opinion, Onoda discloses this element.

159. Well region disposed in said single drift layer ... having a graded concentration of dopants – As detailed above, Onoda discloses a single drift layer (semiconductor layer 102 in tan), as shown below. Ex. 1042, [0046], [0047]; Sections X.B.1.e-f.



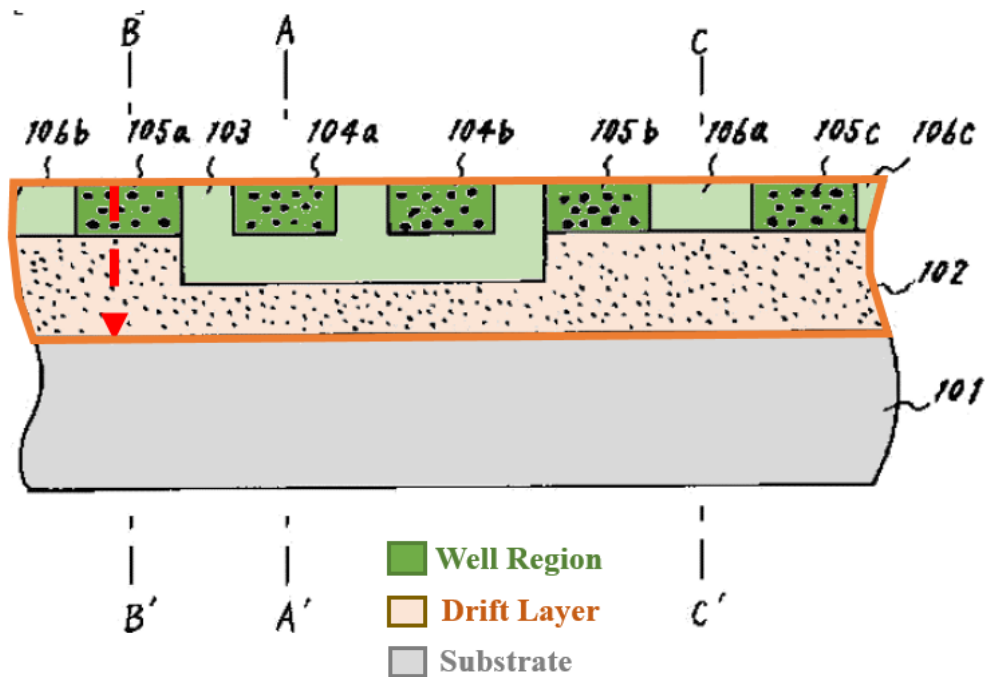
Ex. 1042, FIG. 8; *id.*, FIGS. 2 and 3.

160. Each well in Onoda’s lightly doped P-type semiconductor layer 102—*e.g.*, P-wells 104a, 104b, 105a, 105b, and 105c and N-wells 103, 106a, 106b, and 106c—is an example of a well region (green) disposed in a single drift layer (tan). Ex. 1042, [0041], [0042], [0046]-[0049].



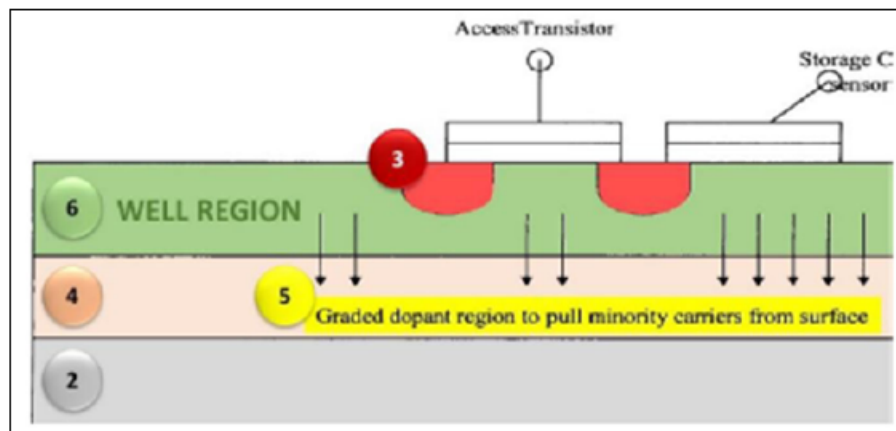
Ex. 1042, FIG. 2.

161. Onoda discloses the steps to form the P-wells and the N-wells in the lightly-doped semiconductor layer 102. Ex. 1042, [0048]-[0050]. After forming the epitaxial second semiconductor layer 102, an N-type dopant (*e.g.*, phosphorus P) is implanted and heat treatment is carried out to form an N-type first well region 103 with a depth of about 3 μm . *Id.*, [0048]. Thereafter, a P-type dopant (*e.g.*, boron B) is implanted to form P-type implantation layers 104a, 104b and 105a through 105c, and an N-type dopant is implanted to form N-type implantation layers 106a through 106c. *Id.*, [0049]. Finally, after carrying out heat treatment, P-type second well regions 104a and 104b, P-type third well regions 105a through 105c, and N-type third well regions 106a through 106c are formed in the second semiconductor layer 102, as illustrated in Figure 8 below. *Id.*, [0050].

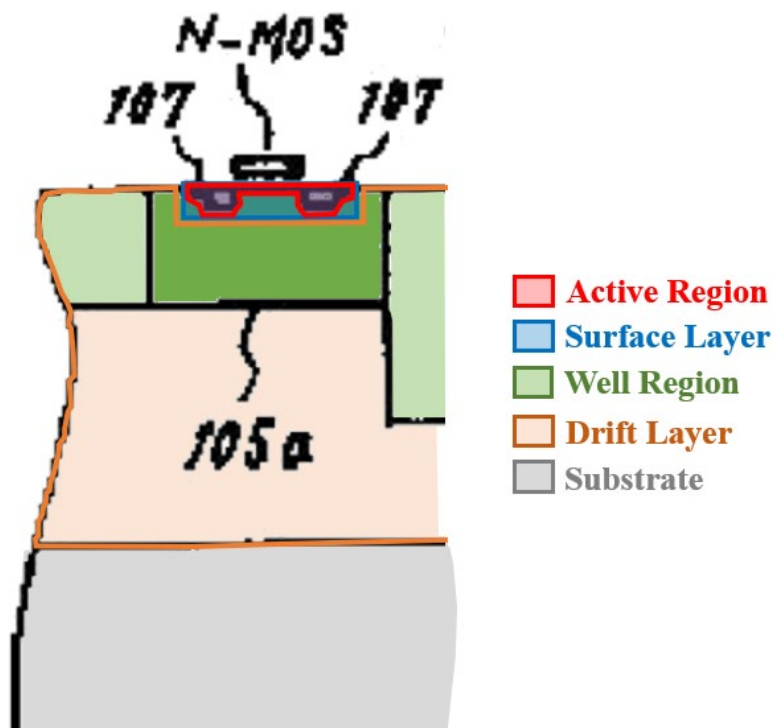


Ex. 1042, FIG. 8.

162. Notably, Onoda satisfies element [7.6] to the same extent that Figure 5(b) of the '502 Patent meets it, as annotated by Patent Owner in its claim construction brief:

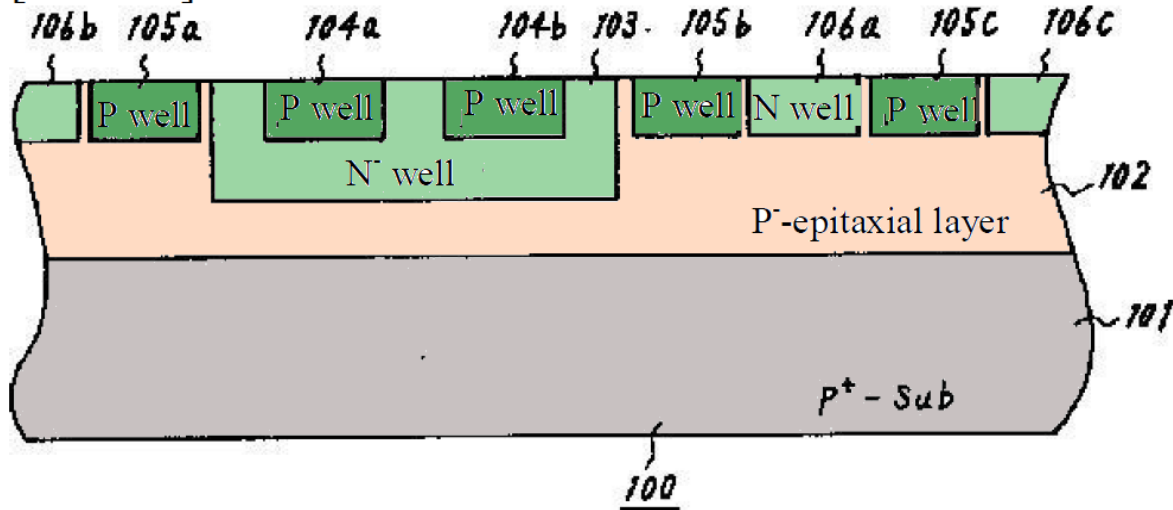


Ex. 1001, FIG. 5(b); Ex. 1030, 7. In my opinion, given that Patent Owner argued that the well region must be entirely contained within the single drift layer, Onoda discloses that too. Figure 3 (which I have excerpted below) shows that the well regions (*e.g.*, 105a) are entirely contained within the drift layer. *See, e.g.*, Ex. 1042, FIGS. 2 and 3.



Ex. 1042, Fig. 3 (excerpted, annotated)). Furthermore, whereas Onoda’s Figure 3 shows well regions in contact with one another, Onoda’s Figure 13 shows an alternate structure “wherein the first well region 103, third well region 105, and fourth well region 106 are separated from each other, that is, wherein the second semiconductor layer 102”—*i.e.*, the drift layer—“is interposed between the well regions.” *Id.*, [0087].

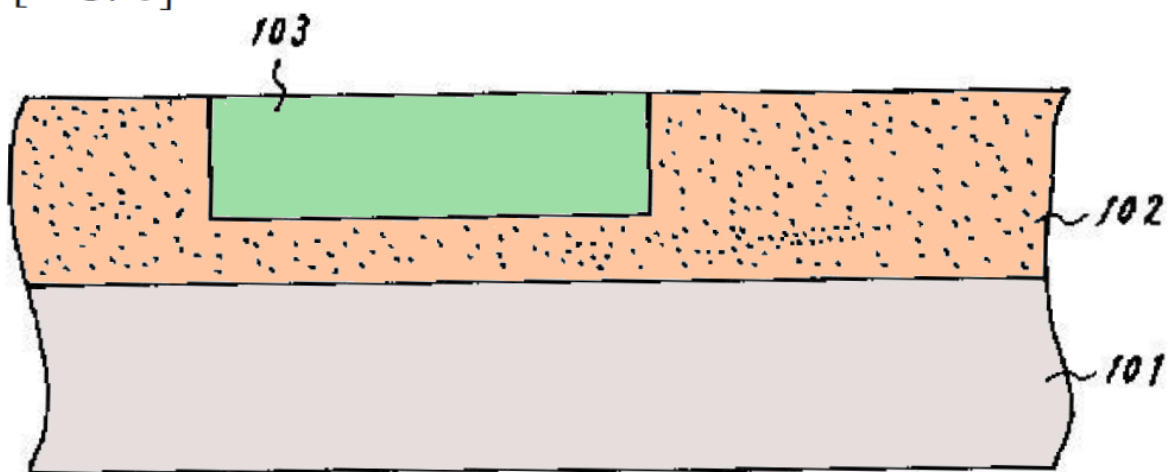
[FIG. 13]



Ex. 1042, Fig. 13 (annotated). This likewise shows the well regions are entirely contained within the SDL.

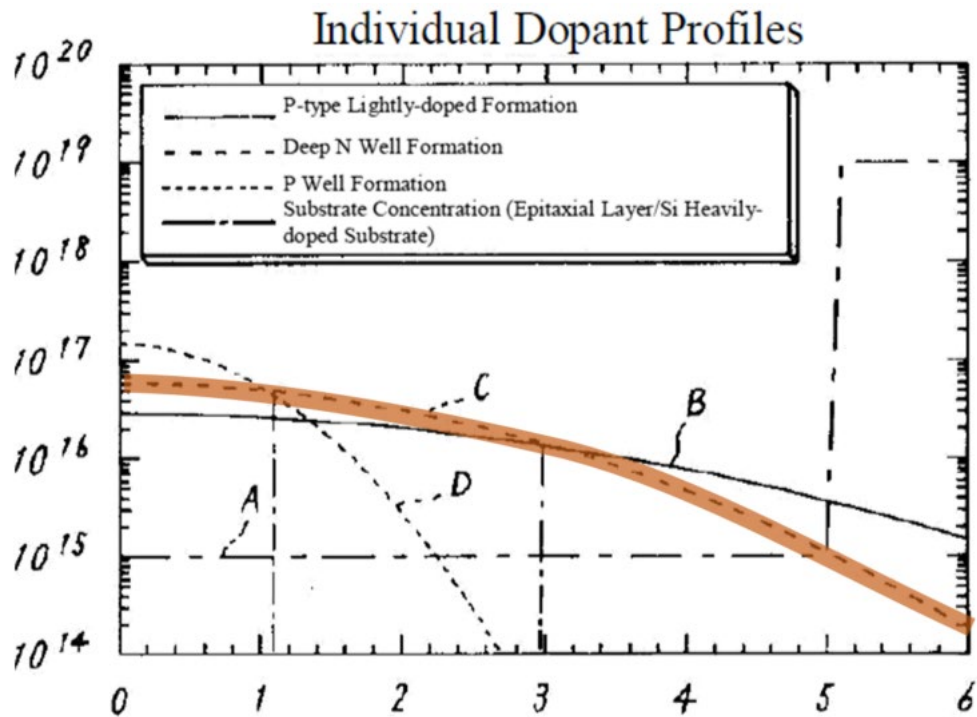
163. As illustrated in Figure 6, the regions where the memory cell array is formed are next masked an N-type dopant (e.g., phosphorus P) is implanted through the mask into the desired region at 150 KeV and between 1×10^{12} and $1 \times 10^{13}/\text{cm}^2$, after which a heat treatment is carried out at between 1130° and 1180° C for five hours in a nitrogen gas ambient to thermally diffuse the dopant (phosphorus P) to form an N-type first well region 103 with a depth of about $3 \mu\text{m}$ and a dopant concentration of between 1×10^{15} and $1 \times 10^{18}/\text{cm}^3$. Ex. 1042, [0048].

[FIG. 6]



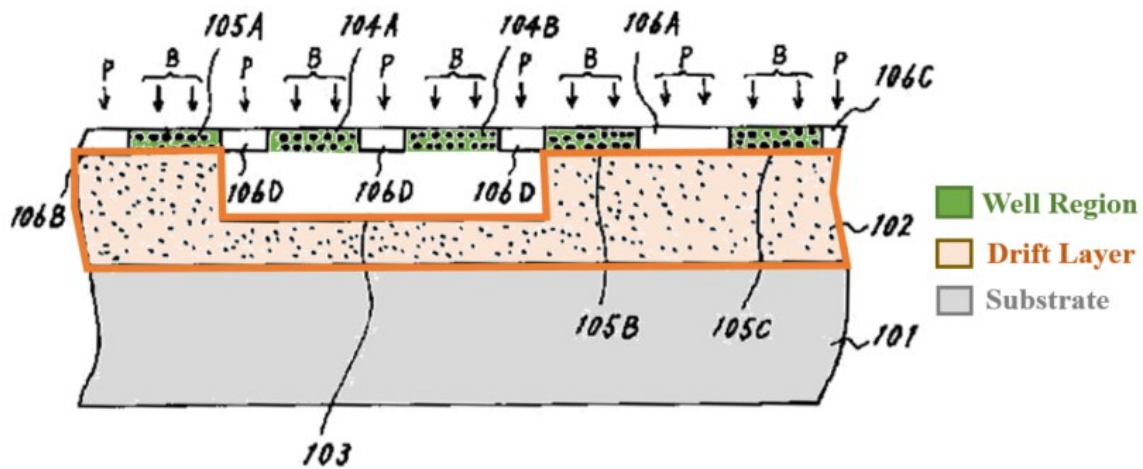
Ex. 1042, FIG. 6.

164. The dopant concentration due to the phosphorus P at this time is depicted by the dotted line C shown in Figure 9, which I have indicated in brown below. Ex. 1042, [0048].



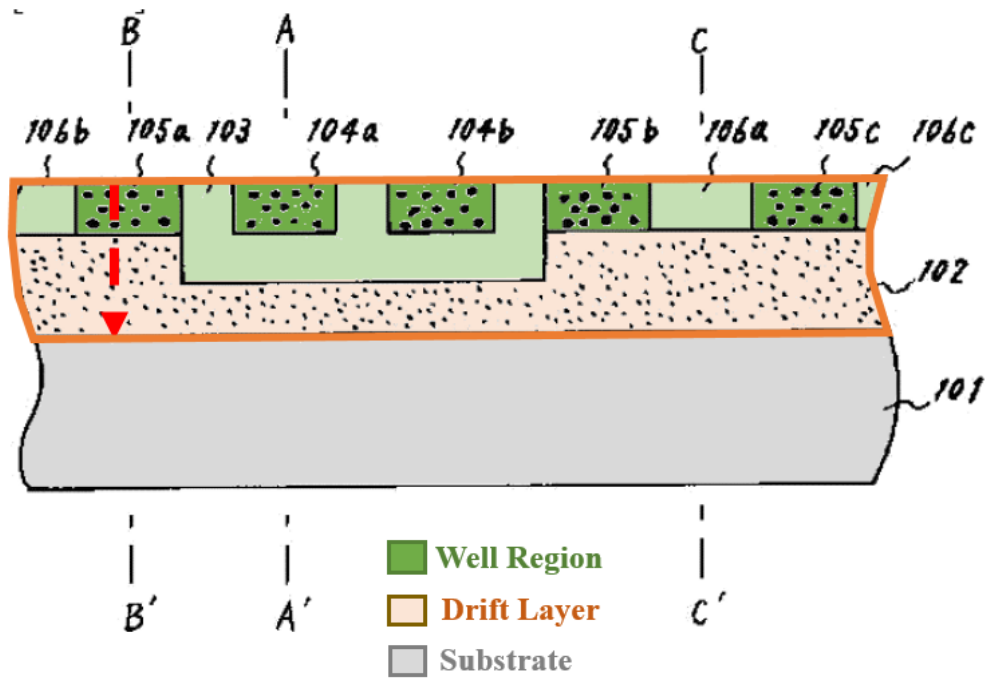
Ex. 1042, FIG. 9.

165. Thereafter, as illustrated in Figure 7, in the regions where the N-channel MOS transistors for the peripheral circuitry are formed, a P-type dopant (e.g., boron B) is implanted at 100 keV and between 1×10^{12} and $1 \times 10^{13}/\text{cm}^2$ to form boron implantation layers 104A, 104B, 105A, 105B, and 105C. Ex. 1042, [0049]. Thereafter, an N-type dopant (e.g., phosphorus P) is implanted at 150 keV and between 1×10^{12} and $1 \times 10^{13}/\text{cm}^3$ to form phosphorus implantation layers 106A through 106D. *Id.*

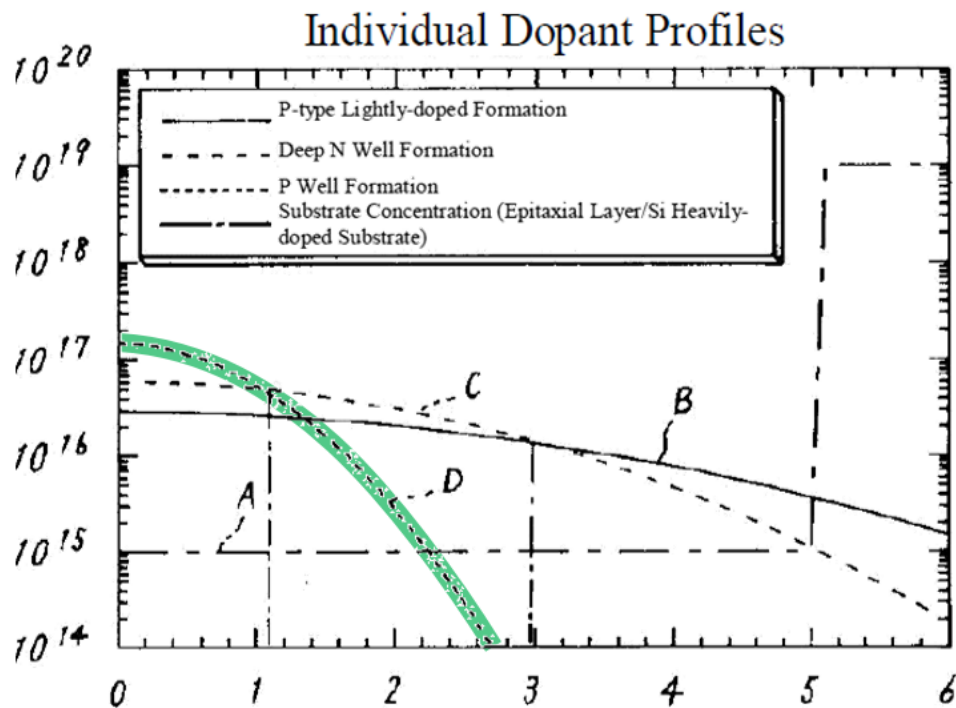


Ex. 1042, FIG. 7.

166. A heat treatment is then carried out for several hours at between 1130° and 1180° C in a Nitrogen gas ambient to thermally diffuse boron dopants B in the boron implantation layers 104A, 104B, 105A, 105B, and 105C, and phosphorus dopants P in the phosphorous implantation layers 106a through 106d to form, as illustrated in FIG. 8, P-type second well regions 104a and 104b with a depth of about 1.5 μm and a dopant concentration between 1×10^{15} and $1 \times 10^{18}/\text{cm}^3$ in the surface of the first well region 103 and P-type third well regions 105a through 105c with a depth of about 1.5 μm and a dopant concentration of between 1×10^{15} and $1 \times 10^{18}/\text{cm}^3$, and N-type fourth well regions 106a through 106c with a depth of about 3 μm and a dopant concentration of between 1×10^{15} and $1 \times 10^{18}/\text{cm}^3$, in the surface of the second semiconductor layer. Ex. 1042, [0050].

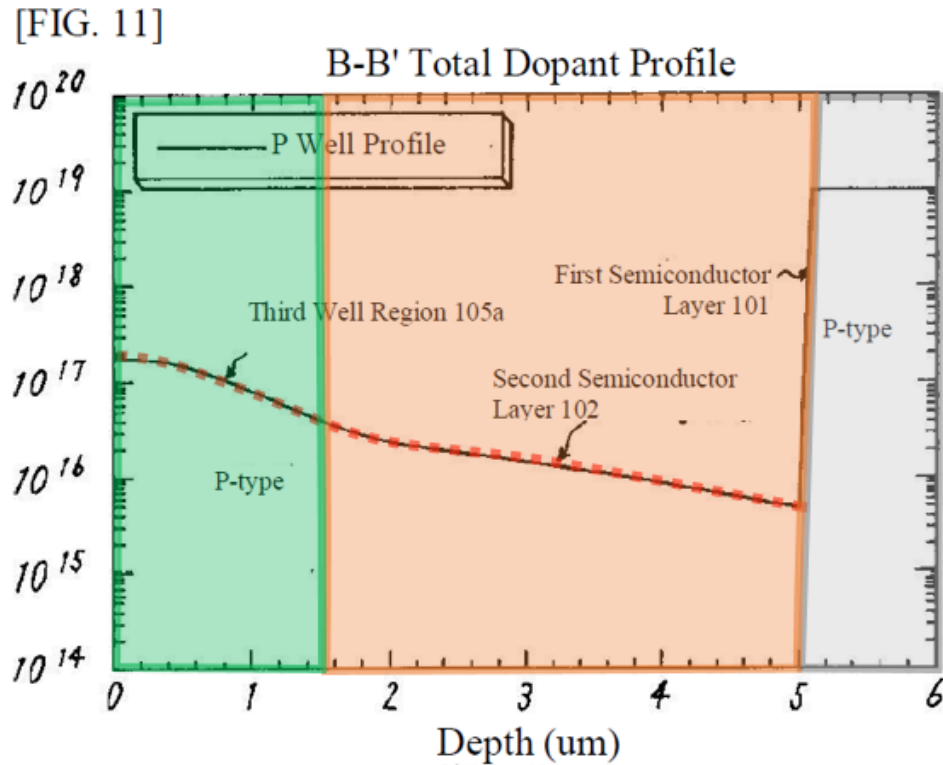


Ex. 1042, FIG. 8. The dopant concentration due to the boron B at this time will be as depicted by the dotted line D shown in FIG. 9, which I have indicated in green below. Ex. 1042, [0050].



Ex. 1042, FIG. 9.

167. The dopant profile appearing in the B-B' cross-section in Figure 8 (above) is shown in Figure 11 (below). As depicted in Figure 11, “a third well region 105a is formed down to a depth of about 1.5 μm from the surface of the second semiconductor layer 102, and the second semiconductor layer 102 is interposed from the bottom surface of the third well region 105a down to the surface of the first semiconductor layer 101.” Ex. 104, [0052]. “[B]oth the third well region 105a and the second semiconductor layer 102 are of the same conductivity type, that is, P-type, so there is no clear boundary between the third well region 105a and the second semiconductor layer 102, but rather the dopant concentration falls off smoothly.” *Id.*



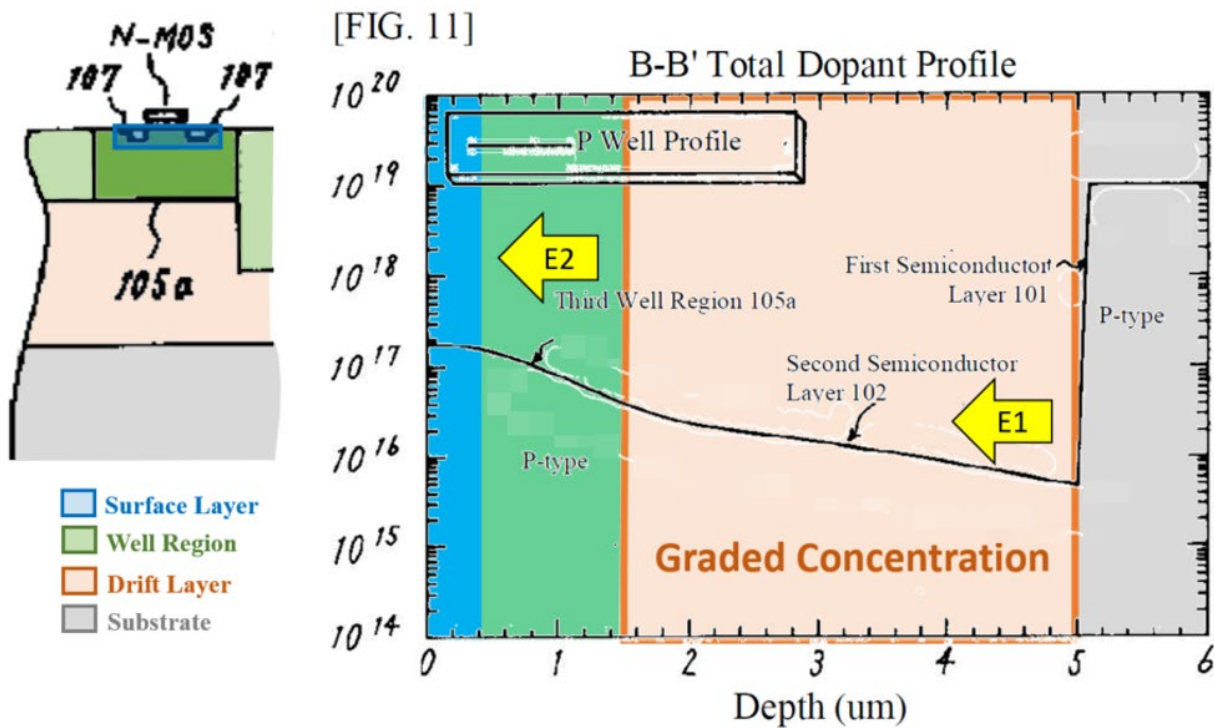
Ex. 1042, FIG. 11.

168. Further, in my opinion and as also detailed above with respect to element [7.4], Onoda's structure has a downward-sloping graded-dopant concentration extending between the surface layer and the substrate, such that each well region (*e.g.*, well) (green) also has such downward-sloping graded-dopant concentration. Ex. 1042, [0052], FIG. 11; Section X.B.1.e. Specifically, Onoda explains that in Embodiment 1, "the first through fourth well regions are all formed through thermal diffusion, and thus the dopant profiles thereof are profiles that

approximate *Gaussian distributions with the concentrations at maxima near the surface.*” Ex. 1042, [0053].

169. In light of the above, it is my opinion that Onoda satisfies element [7.6] under Patent Owner’s construction that the term “well region” means “a doped region that surrounds the active region of a semiconductor device.” Section VIII. As shown in Onoda’s Figures 2 and 3, the exemplary well region (green) is a doped region that surrounds both the surface layer (blue) and the active region therein.

170. **Second static unidirectional electric drift field to aid the movement of minority carriers** – I have annotated Onoda’s Figure 11 below (alongside the relevant excerpt of Figure 3) to show the exemplary first static unidirectional electric drift field (“E1”) described in Section X.A.1.f, at a depth corresponding to Onoda’s well (tan), and an exemplary second static unidirectional electric drift field (“E2”), at a depth corresponding to Onoda’s second semiconductor layer 102 (green) (exemplary well region disposed in the single drift layer).



Ex. 1042, FIG. 3 (excerpted, annotated), FIG. 11 (annotated). Moreover, I have illustrated E1 and E2 as electric fields having different magnitudes, to reflect the different local slopes (gradients) of the dopant profile. Ex. 1022, [0071] (“the vertical ϵ -field is established by the rate of change in the graded dopant concentration, *i.e.*, the greater the rate of change ... the greater the intensity of the ϵ -field.”). Further, Onoda’s graded-dopant profile, including the profile in the well region, is set once the device has been fabricated and does not change, making the profile (and any resulting electric field) static, as described in §X.B.1.f.

171. As discussed in Section X.A.1.f, based on Applicant’s repeated representations during prosecution of the parent ’195 Patent, and according to the Jastrzebski and Kamins prior art relied on by Applicant during prosecution, and

Patent Owner's statements in its claim construction brief, the downward-sloping graded-dopant concentration in each of these well regions creates a (second) static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. Section X.A.1.f.

172. In light of the above, it is my opinion that Onoda satisfies element [7.6] under Patent Owner's plain meaning construction of "to aid the movement of minority carriers." Section VIII. As shown in Figure 11 above, Onoda's graded-dopant concentration is downward-sloping over the entire well region, and thus, according to Patent Owner (and also in light of Patent Owner's representations to the Patent Office, discussed in Section X.A.1.f), creates a static unidirectional electric drift field that aids the movement of minority carriers downward from the surface layer to the substrate.

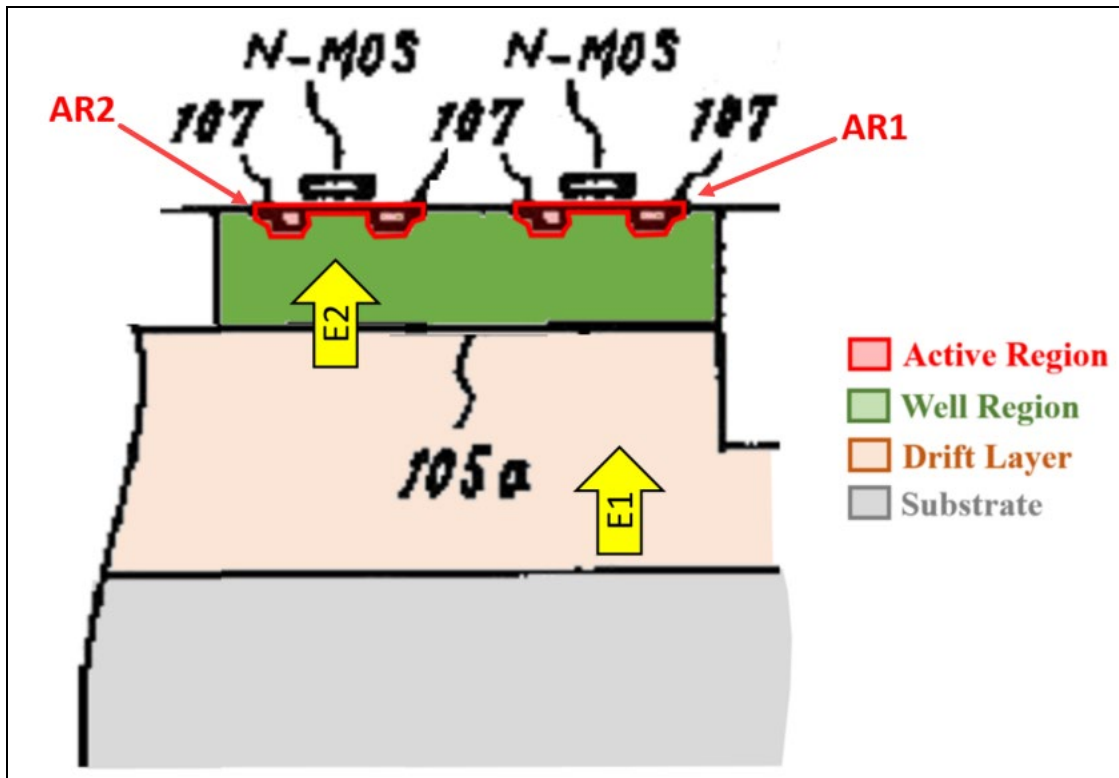
2. Dependent Claim 8: "The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions."

173. As discussed above, it is my opinion that Onoda anticipates or else renders claim 7 obvious. Section X.B.1. In my opinion, Onoda discloses the additional limitation of claim 8.

174. As I discussed in Sections X.B.1.e-f, second semiconductor layer 102 (SDL)(tan) generates a first static unidirectional electric field E1 (yellow) that aids the movement of carriers that are in, or originate from, active region AR1 (red)

above it. As I discussed above in Section X.B.1.d, Figure 3 from Onoda illustrates active regions containing NMOS transistors with source/drain regions in a doped P-well 105a, 105b and 105c, and PMOS transistors with source/drain regions in a doped N-well 106a, 106b, and 106c. Ex.1042, FIG. 3, [0042], [0055], [0044].

175. While Onoda's Figure 3 shows a single NMOS transistor formed in P-well 105a, Onoda expressly discloses that the "P-type third well region [is] formed in the surface of the second semiconductor layer," and that "at least *some N-channel MOS transistors of the plurality of the N-channel MOS* transistors that structure the peripheral circuitry are *formed in the third well region*." Ex. 1042, [0009]. Later in its disclosure, Onoda refers to "the plurality of MOS transistors that are formed in" third well region 105a, among other regions. *Id.*, [0054]. In order to illustrate these express teachings, I have prepared a modification of Onoda's Figure 3 ("Figure 3M") below, which extends the P-Well 105a in Onoda's Figure 3 past to the left and shows two NMOS transistors, each with its active region indicated in red—AR2 (left), AR2 (right)—formed in the P-Well 105a (green). P-well region generates a second static unidirectional field E2 (yellow) that aids movements of carriers that are in, originate from, active region AR2 (red) above it. For this mapping, the surface layer of claim 7 includes both active regions AR1 and AR2. §X.B.1d.



Ex. 1042, FIG. 3M. I note that my Figure 3M modification not only reflects the teachings of Onoda, but also reflects standard practice in CMOS layout and fabrication. Other prior art references confirm this. Ex. 1054 (Maziasz), 27 (“Each cell consists of two horizontal diffusion rows for pMOS and nMOS transistors. This implies that single p- and n-wells can be used.”), Figure 2.3(b); Ex. 1049 (Yamada), 6:51-53 (“diffusion layers [(active regions)] 60 and 61 [of] NMOS transistors” formed in “a common p-well 43” as shown in Figures 5-6).

176. Electric fields E1 and E2 are adapted to the grading of dopants in second semiconductor layer 102 (SDL) (tan) and P-type well regions 105a (well region) (green), respectively, because the direction of electric fields E1 and E2 (*i.e.*, toward the surface or away from the surface) is dependent on the local slope of the

graded dopant profile according to Applicant's repeated representations during prosecution of the parent '195 patent, the Jastrzebski and Kamins prior art relied on by Applicant during its prosecution, and PO's statements in its claim construction brief as discussed in §X.A.1.f. Additionally, the magnitude of electric fields E1 and E2 also depends on the local grading of dopants. §X.B.1.g; Ex. 1022, [0071].

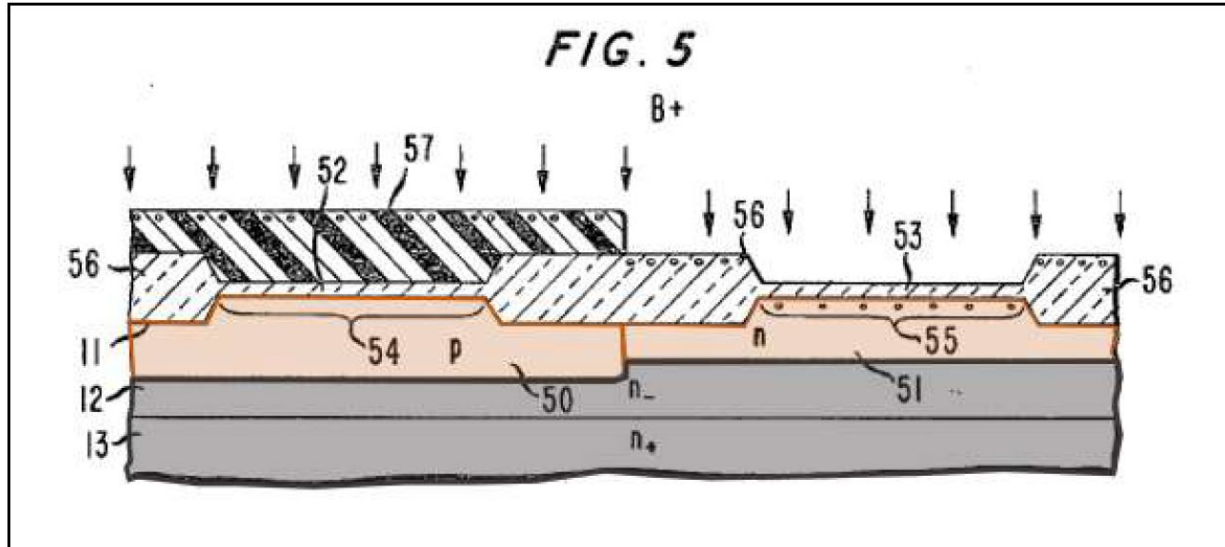
3. Dependent Claim 11: “The semiconductor device of claim 7 wherein the semiconductor device is a flash memory device.”

177. As discussed above, it is my opinion that Onoda anticipates or else renders obvious claim 7. Section X.A.1. In my opinion, Onoda discloses the additional limitation of claim 11. When discussing the first embodiment, Onoda discloses a “configuration of a *flash memory* . . . to which this first embodiment is applied.” Ex.1042, [0029], [0041] (“semiconductor substrate 100 applied in this first embodiment in order to form *flash memory*”), [0046] (“A method of manufacturing a flash memory structured in this way, and, . . . a method for manufacturing a semiconductor substrate 100 that is applied to *a flash memory*, will be explained . . .”).

C. Ground IV

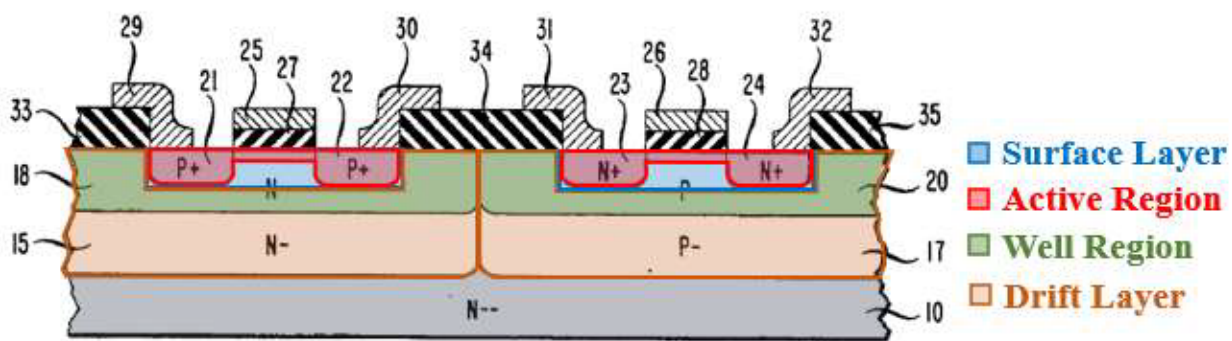
1. Dependent Claim 8: “The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.”

178. As discussed above, it is my opinion that Payne discloses or renders obvious claim 7. Section X.A.1. In my opinion, Payne-Parrillo renders obvious the additional limitation of claim 8. Parrillo and Payne are contemporaneous patents that share a common inventor (Richard S. Payne). Ex. 1025; Ex. 1005. Both patents were originally assigned to AT&T Bell Labs. *Id.*



180. Payne is directed to improving twin-well (“twin-tub”) CMOS technology by adding a shallow well (“surface region”) in each deep well (“tub”) of a twin-well CMOS device. Ex. 1005, 1:5-14, 1:59-2:28, 6:20-21; *id.*, 1:15-50;

Section X.A.1.e. This nested well structure allowed transistors to be closer to improve packing density. Ex. 1005, Abstract, 1:51-54, 6:17-19, 6:57-59. As an example, Payne describes its devices fabricated in a “silicon semiconductor substrate [] of ‘N--’ conductivity type ...”, as shown below. *Id.*, 2:50-60.



Ex. 1005, FIG. 10.

181. In my opinion, a POSITA would have been motivated to apply Payne’s improved CMOS technology to a known twin-tub CMOS semiconductor device that has individual tubs containing multiple transistors, such as that described by Parrillo, to achieve high packing density as taught by Payne. Doing so would have resulted in forming Payne’s nested well structure in the tubs to reduce the spacing between active regions of adjacent transistors. *Id.*; Ex. 1005, Abstract, 1:51-54, 6:17-19, 6:57-59.

182. There would have been a reasonable expectation of success, in my opinion, because the Payne and Parrillo patents are closely related (as discussed

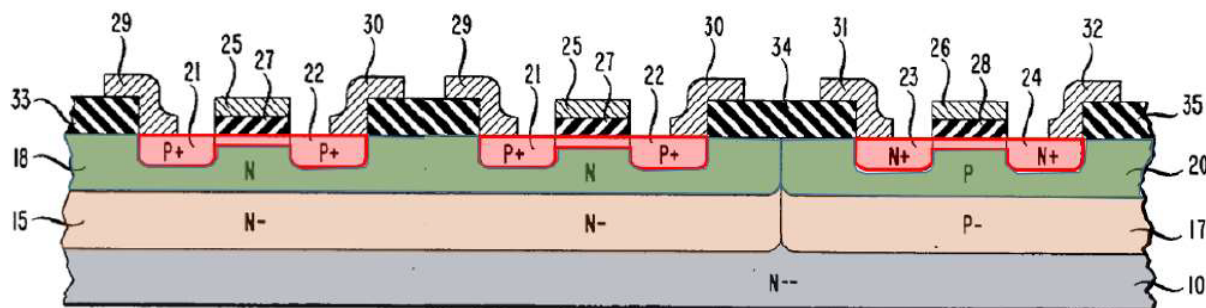
above) and Payne shows that a POSITA knew how to use Payne's CMOS technology to improve a twin-tub CMOS device similar to that described by Parrillo. Ex. 1005, 6:20-21 (Payne's technology "is designed primarily for twin-tub structures").

183. In my opinion, combining Parrillo with Payne in this manner would have merely amounted to (1) use of a known technique (Payne's improved twin-tub CMOS technology) to improve similar devices (known twin-tub CMOS devices with individual tubs having multiple transistors) in the same way (to increase packing density), and (2) a simple substitution of one known element (Parrillo's twin-tub CMOS technology) for another (Payne's —improved twin-tub CMOS technology) to fabricate a known twin-tub CMOS device with individual tubs having multiple transistors.

184. While Payne's Figure 10 illustrates a single transistor formed in each tub, Payne expressly discloses that "the figures show fabrication of a device which is typically part of an integrated circuit including many other [transistor] devices." Ex. 1005, 2:53-55, 6:17-19, 6:57-59. And given the jagged edges to the left and right of Payne's Figure 10, Payne is suggestive that its illustrated tubs contain multiple transistors just like Parrillo describes. Ex. 1025, 3:22-25.

185. To illustrate this, I have prepared a modification of Payne's Figure 10 ("Figure 10M") below, which extends Payne's Figure 10 past its left jagged edge

and shows two PMOS transistors, each with its active region 21/22 (red), formed in the nested n-well structure (left) that consists of n-tub 15 (tan) and shallow n-well 18 (green) disposed in it. As detailed in Sections X.A.1.e-g, tub 15 is an exemplary single drift layer. Sections X.A.1.e-g.



Ex. 1005, FIG. 10M.

186. In my opinion, my Figure 10M modification not only reflects the teachings of Payne and Parrillo, it also reflects standard practice in CMOS layout and fabrication. Other prior art references confirm this. Ex. 1054 (Maziasz), 27 (“Each cell consists of two horizontal diffusion rows for pMOS and nMOS transistors. This implies that single p- and n-wells can be used.”), Figure 2.3(b); Ex. 1046 (Yamada), 6:51-53 (“diffusion layers [(active regions)] 60 and 61 [of] NMOS transistors” formed in “a common p-well 43” as shown in Figures 5-6).

187. This modification is consistent with standard practice in CMOS layout and fabrication. For example, Masiasz, a discussion of layout area minimization techniques, describes placing multiple transistors and active areas within shared wells. Ex. 1054, 27-31. “Each cell consists of two horizontal diffusion rows for

pMOS and nMOS transistors. This implies that single p- and n-wells can be used.”

188. This is further illustrated in Masiasz's example cell in Fig. 2.3. Ex. 1054, 30, FIG. 2.3. Fig. 2.3(a) shows a collection of pMOS transistors (top row) and nMOS transistors (bottom row). *Id.* Following the guidelines in Masiasz Fig. 2.1, each of the rows are contained within a single p-well (top row) or n-well (bottom row). *Id.* Fig. 2.3(b) combines active areas wherever the circuit allows source/drain diffusions to be shared. *Id.* That minimization produces two pMOS active regions (annotated in red below) in the top row, both contained within a single n-well (annotated in green below). *Id.*

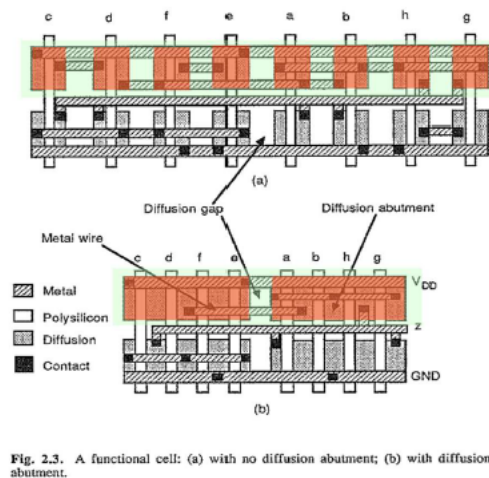
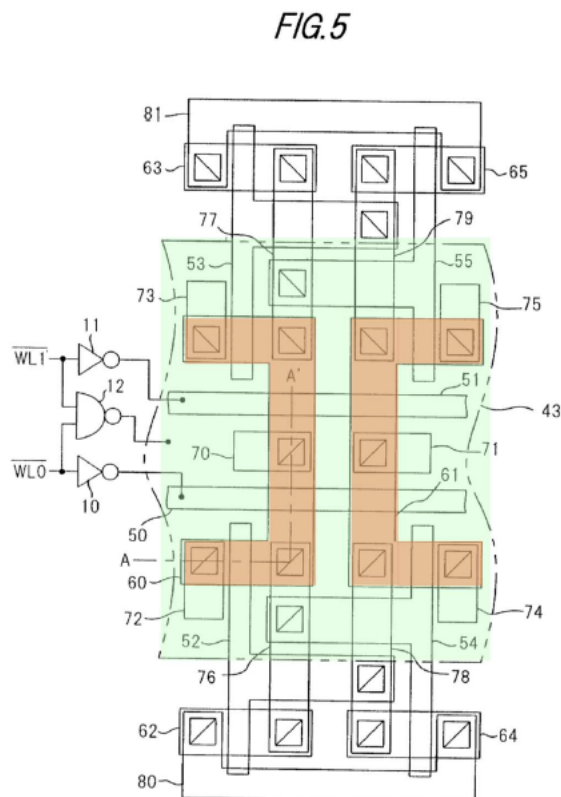


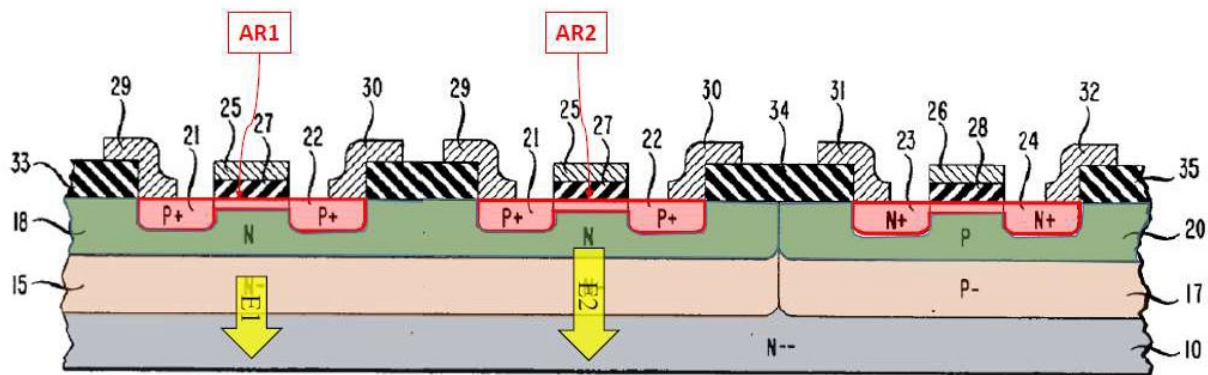
Fig. 2.3. A functional cell: (a) with no diffusion abutment; (b) with diffusion abutment.



Ex. 1054, 30, FIG 2.3; Ex. 1049, FIG. 5.

189. In another example, Yamada's Fig. 5 (above) illustrates how the layout of two six transistor (6T) memory cells can share wells by placing multiple active regions within a single well. Ex. 1049, FIG. 5. Two PMOS active areas (60 and 61) are highlighted red. Id. Each of these diffusions (active areas) contain four transistor gates, 55, 51, 61, 54, and 53, 51, 61, 52 respectively. Id. These two examples show that sharing multiple active regions is a common and obvious practice. In fact, I have used this technique many times in my own designs.

190. In my opinion, Figure 10M, reproduced again below, makes clear that Payne-Parrillo satisfies claim 8. The figure shows that, as discussed in Section X.A.1.f, tub 15 (single drift layer) (tan) generates a first static unidirectional electric field E1 (yellow) that aids movements of carriers that are in, or originate from, active region AR1 (red) above it. Ex. 1005, 1:60-68, 5:21-29; Section X.A.1.f; Ex. 1013, 431; Sections X.A.1.d-g. Likewise, as discussed in Section X.A.1.g, well region 18 (green) generates a second static unidirectional electric field E2 (yellow) that aids movements of carriers that are in, or originate from, active region AR2 (red) above it. Id. For this mapping, the surface layer of claim 7 includes both active regions AR1 and AR2.



Ex. 1005, FIG. 10M.

191. Electric fields $E1$ and $E2$ are adapted to the grading of dopants in tub 15 (single drift layer) (tan) and well region 18 (green), respectively, because the direction of electric fields $E1$ and $E2$ (i.e., toward the surface or away from the surface) is dependent on the local slope of the graded-dopant profile according to Applicant's repeated representations during prosecution of the parent '195 Patent, the Jastrzebski and Kamins prior art relied on by Applicant during its prosecution, and Patent Owner's statements in its claim construction brief as discussed in Section X.A.1.f; ¶¶104-105. Additionally, the magnitude of electric fields $E1$ and $E2$ also depends on the local grading of dopants. Section X.A.1.g; Ex. 1022, [0071].

192. I note that both active regions have an $E2$ and $E1$ static field beneath them as illustrated in Payne's Figure 10, above. Ex. 1005, FIG. 10. In this example, $E2$ has been selected for a PMOS device active region, AR2, within a n-type well. $E1$ was selected for another PMOS device active region AR1 within the same n-

type well. There are similar E1 and E2 fields related to the NMOS devices within the p-type wells on the right side of the figure and these also meet claim 8.

D. Ground V

193. In my opinion, Payne in combination with Wolf (“Payne-Wolf”) renders claims 9-11 obvious. Payne is directed to CMOS devices. Ex. 1005, 1:5-10, 1:51-54, 6:57-59. Wolf is a well-known textbook that teaches fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on CMOS. See generally Ex. 1008A; *id.*, Chapter 16 (“CMOS Process Integration”). Wolf also published over 20 years after Payne was filed. Exs. 1014-15.

194. In my opinion, a POSITA would have therefore understood and expected that the teachings of Wolf would apply to Payne, and would have looked to Wolf for the description of commercial applications of CMOS technologies, as well as advances and additional process details to the extent not covered in Payne. *Id.*

1. Dependent Claim 9: “The semiconductor device of claim 7 wherein the semiconductor device is a central processing unit (CPU).”

195. As discussed above, it is my opinion that Payne renders obvious claim 7. Section X.A.1. Twin-well CMOS technology was, by the early 2000s, “the dominant CMOS technology in IC production.” Ex. 1008D, 181. It was also

known to fabricate microprocessors (CPUs) using CMOS technology to achieve the benefits of “lower power-dissipation” in such devices. Ex. 1008B, 368-370; Ex. 1032, 1334 (see “microcomputer”).

196. Rabaey confirms this, in my opinion. Ex. 1050, 180 (“The [CMOS] inverter is truly the nucleus of all digital [logic] designs” and, together with other “[logic] gates such as NAND, NOR, or XOR ... form the building blocks for modules such as multipliers and processors.”), 37 (“Modern [CMOS] processes are increasingly using a dual-well [(twin-well)] approach that uses both n- and p-wells...”), 383-84, FIG. 8-6 (showing Intel Pentium processor “designed in a 0.18 μ m CMOS technology.”). Sze also confirms this, describing a system-on-a-chip that includes CMOS “*logic IC (e.g., CPU)*” fabricated using twin-well CMOS technology. Ex. 1051, 525-26, FIGS. 37-38.

197. Payne teaches an improvement on “twin tub” (twin-well) CMOS technology to reduce separation “between source and drain regions of adjacent [transistor] devices” and thus increase packing density of CMOS semiconductor devices. Ex. 1005, Abstract, 1:5-8, 1:51-68, 6:17-21, 6:57-59, 1:9-50; Section X.A. In my opinion, it would have been obvious to fabricate known CPUs using Payne’s improved twin-well CMOS technology for the benefit of increased packing density.

198. Additionally, in my opinion, using Payne’s technology to form CPUs would have merely amounted to (1) use of a known technique (Payne’s improved

twin-well CMOS process) to improve similar devices (known CPU designs) in the same way (to increase packing density) and (2) a simple substitution of one known element (CMOS technology for prior art CPUs) with another (Payne's improved CMOS technology).

199. In my opinion, there would have been a reasonable expectation of success with predictable results because Payne's twin-well CMOS process was a known improvement over conventional twin-well CMOS process and would have been used for its intended purpose in manufacturing known CPUs, designed for implementation using CMOS technology.

2. Dependent Claim 10: "The semiconductor device of claim 7 wherein the semiconductor device is a DRAM device."

200. As discussed above, it is my opinion that Payne renders obvious claim 7. Section X.A.1. Twin-well CMOS technology was, by the early 2000s, "the dominant CMOS technology in IC production." Ex. 1008D, 181. It was also known to fabricate DRAM devices for "the advantages of cost per bit, device density, and flexibility of use (i.e., both read and write operations are possible) [which] have made DRAMs the most widely used form of semiconductor memory to date," and to do so using CMOS technology to take advantage of "lower power dissipation [] and smaller soft error rates." Ex. 1008B, 587, 596-597.

201. Payne teaches an improvement on "twin tub" (twin-well) CMOS technology to reduce separation "between source and drain regions of adjacent

[transistor] devices” and thus increase packing density of CMOS semiconductor devices. Ex. 1005, Abstract, 1:5-8, 1:51-68, 6:17-21, 6:57-59, 1:9-50; Section X.A. In my opinion, it would have been obvious to fabricate known DRAM devices using Payne’s improved twin-well CMOS technology for the benefit of increased packing density.

202. Additionally, in my opinion, using Payne’s technology to form DRAMs would have merely amounted to (1) use of a known technique (Payne’s improved twin-well CMOS process) to improve similar devices (known DRAM designs) in the same way (to increase packing density) and (2) a simple substitution of one known element (CMOS technology contemplated by Wolf for DRAM) with another (Payne’s improved CMOS technology).

203. In my opinion, there would have been a reasonable expectation of success with predictable results because Payne’s improved CMOS process was an improvement over conventional twin-well CMOS process and would have been used for its intended purpose in manufacturing a known DRAM designed for implementation using CMOS technology.

3. Dependent Claim 11: “The semiconductor device of claim 7 wherein the semiconductor device is a flash memory device.”

204. As discussed above, it is my opinion that Payne renders obvious claim 7. Section X.A.1. Twin-well CMOS technology was, by the early 2000s, “the

dominant CMOS technology in IC production.” Ex. 1008D, 181. It was also known to fabricate semiconductor flash memory devices to achieve the benefits of “high density [], small-die size, lower cost, and hot-electron writability of EPROMs, together with the easy erasability, on-board reprogrammability, and electron-tunneling erasure features of EEPROMs,” and to do so using CMOS technology for “lower power-dissipation.” Ex. 1008B, 632-634; Ex. 1008A, 808-810.

205. Indeed, flash memory devices commonly used CMOS technology. Ex. 1008B, 633-635 (describing known “CMOS flash-EEPROM” devices); Ex. 1007, 22:16-17 (flash EEPROM is flash memory), 22:10-23:2, FIG. 28 (peripheral flash memory circuit with CMOS transistors).

206. Payne teaches an improvement on “twin tub” (twin-well) CMOS technology to reduce separation “between source and drain regions of adjacent [transistor] devices” and thus increase packing density of CMOS semiconductor devices. Ex. 1005, Abstract, 1:5-8, 1:51-68, 6:17-21, 6:57-59, 1:9-50; Section X.A. It would have been obvious to fabricate known flash memory devices using Payne’s improved twin-well CMOS technology for the benefit of increased packing density.

207. Additionally, in my opinion, using Payne’s technology to form flash memory would have merely amounted to (1) use of a known technique (Payne’s

improved twin-well CMOS process) to improve similar devices (known CMOS flash memory designs) in the same way (to increase packing density) and (2) a simple substitution of one known element (CMOS technology for prior art flash memory) with another (Payne's improved CMOS technology).

208. In my opinion, there would have been a reasonable expectation of success with predictable results because Payne's improved CMOS process was an improvement over conventional twin-well CMOS process and would have been used for its intended purpose in manufacturing a known flash memory designed for implementation using CMOS technology.

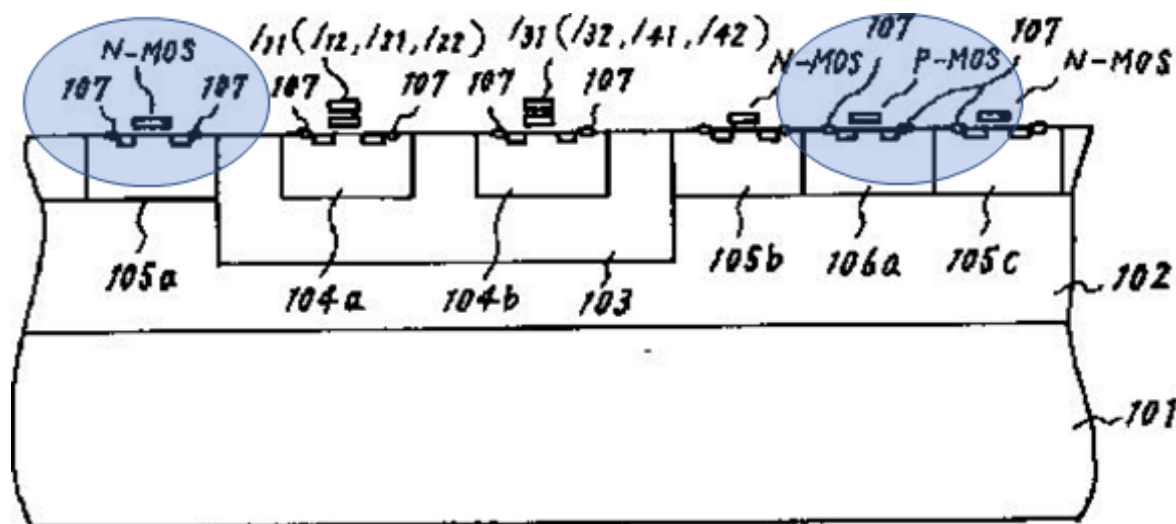
E. Ground VI

1. Dependent Claim 9: "The semiconductor device of claim 7 wherein the semiconductor device is a central processing unit (CPU)."

209. As I discussed above in Section X.B.1, Onoda anticipates or else renders obvious claim 7. §XB.1. In my opinion, Onoda-Wolf renders obvious the additional limitation of claim 9.

210. Onoda discloses N-channel MOS (NMOS) transistors and P-channel MOS (PMOS) transistors in the peripheral circuitry of its flash memory devices. Ex.1042, [0052], [0044], [0045], Fig. 3, claim 2. According to Wolf, a well-known textbook on semiconductor fabrication, a CMOS device, by definition, has "N-channel MOS [(NMOS)] transistor[s]" and "P-channel MOS [(PMOS)]

transistors.” Ex.1008A, 807-09; *see also* Ex.1008B, 368 (“Complementary MOS (CMOS) is so-named because it uses both p- and n-type (complementary) MOS transistors in its circuits.”⁶



Ex.1042, FIG. 3.

211. As I discussed in Section X.D.1, it was known to fabricate microprocessors (CPUs) using CMOS technology to achieve the benefits of “lower power-dissipation” in such devices. Ex.1008B, 368-370; Ex.1032, 1334 (see “microcomputer”). Rabaey confirms this. Ex.1050, 180 (“The [CMOS] inverter is truly the nucleus of all digital [logic] designs” and, together with other “[logic] gates such as NAND, NOR, or XOR ... form the building blocks for modules such

⁶ Though Onoda does not explicitly refer to a CMOS device, a POSITA would have recognized from Onoda’s disclosure that its devices are CMOS devices. My analysis relies on Onoda’s disclosure for Ground VI regardless of whether Onoda’s device is a CMOS device.

as multipliers and processors.”), 37 (“Modern [CMOS] processes are increasingly using a dual- well [(twin-well)] approach that uses both n- and p-wells ...”), 383-84, FIG. 8-6 (showing Intel Pentium processor “designed in a 0.18 μ m CMOS technology.”). Sze also confirms this, describing a system-on-a-chip that includes CMOS “*logic IC (e.g., CPU)*” fabricated using twin-well CMOS technology. Ex.1051, 525-26, FIGS. 37-38.

212. Onoda teaches an improvement on a device containing NMOS and PMOS transistors to improve “latch-up resistance and punch-through breakdown voltage” and “junction breakdown voltage between the well regions and the semiconductor substrate.” Ex. 1042, Cover. It would have been obvious to fabricate known CPUs using Onoda’s improvement. Additionally, using Onoda’s technology to form CPUs would have merely amounted to (1) use of a known technique (Onodas’s processing techniques for making an improved device containing NMOS and PMOS transistors) to improve similar devices (known CPU designs) in the same way (to increase packing density) and (2) a simple substitution of one known element (CMOS technology for prior art CPUs) with another (Onoda’s improved CMOS technology). *Id.* There would have been a reasonable expectation of success with predictable results because Onoda’s CMOS process was a known improvement over conventional CMOS process and would

have been used for its intended purpose in manufacturing known CPUs, designed for implementation using CMOS technology. *Id.*

213. The teachings of Onoda-Wolf relied on in this Petition are directed to conventional twin-well CMOS technology. §§X.B.1.b, IX.E.3; Ex.1042, [0052], [0044], [0045], Fig. 3, claim 2; Ex.1008B, 387-389.

214. It would have been obvious to apply Onoda-Wolf's CMOS technology to fabricate known logic devices, including inverters and microprocessors (CPUs), to achieve the benefits of "lower power-dissipation" of CMOS technology in such devices. Ex.1008B, 368-370; Ex.1032, 1334.

215. Onoda suggests doing so in teaching the application of its technology to a "semiconductor integrated circuit device" Ex.1042, Title. Twin-well CMOS technology was, by the early 2000s, "the dominant CMOS technology in IC production." Ex.1008D, 181.

216. Using Onoda's technology to form logic devices such as CPUs would have been obvious for the same reasons as using Payne's technology to form CPUs, as explained above in Section X.D.1.

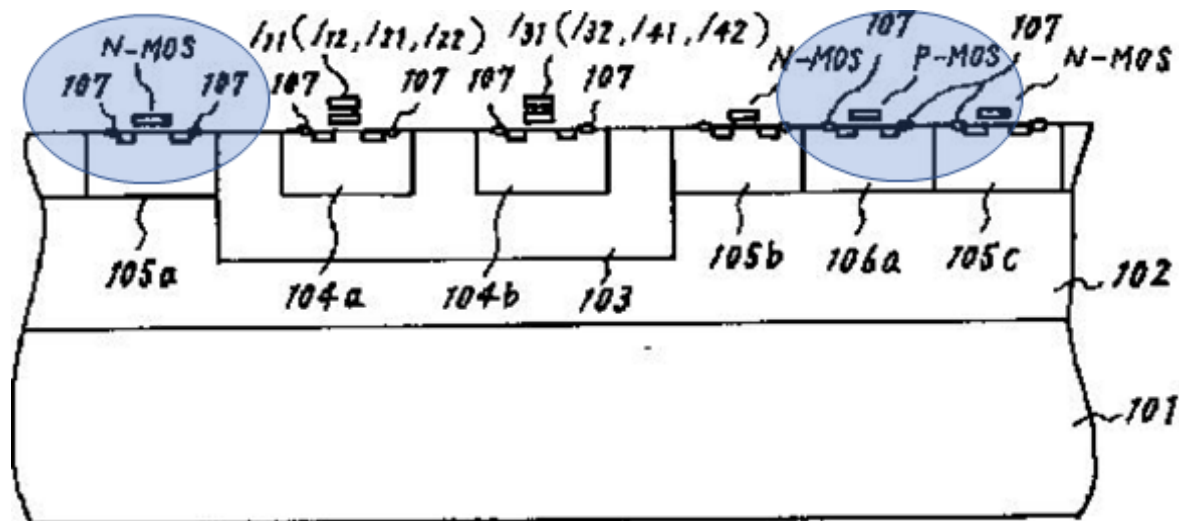
2. Dependent Claim 10: "The semiconductor device of claim 7 wherein the semiconductor device is a DRAM device."

217. As discussed above, it is my opinion that Onoda anticipates or else renders obvious claim 7. Section X.B.1. It is further my opinion that Onoda-Wolf renders obvious the additional limitation of claim 10. Section X.E.1.

218. Twin-well CMOS technology was, by the early 2000s, “the dominant CMOS technology in IC production.” Ex. 1008D, 181. It was also known to fabricate DRAM devices for “the advantages of cost per bit, device density, and flexibility of use (i.e., both read and write operations are possible) [which] have made DRAMs the most widely used form of semiconductor memory to date,” and to do so using CMOS technology to take advantage of “lower power dissipation [] and smaller soft error rates.” Ex. 1008B, 587, 596-597.

3. Motivation to combine Onoda and Wolf

219. According to Wolf, a well-known textbook on semiconductor fabrication, a CMOS device, by definition, has “N-channel MOS [(NMOS)] transistor[s]” and “P-channel MOS [(PMOS)] transistors.” Ex.1008A, 807-09; *see also* Ex.1008B, 368 (“Complementary MOS (CMOS) is so-named because it uses both p- and n-type (complementary) MOS transistors in its circuits.”). As discussed in Sections X.D.1-2, it was known to fabricate microprocessors (CPUs) and DRAMs using CMOS technology. Onoda discloses N-channel MOS (NMOS) transistors and P-channel MOS (PMOS) transistors in the peripheral circuitry of its flash memory devices. Ex.1042, [0052], [0044], [0045], Fig. 3, claim 2.



Ex. 1042, FIG. 3.

220. Onoda teaches an improvement on devices containing NMOS and PMOS by “reducing the tendency for latch-up and for punch-through” and “increasing the junction breakdown voltage.” Ex. 1042, [0018]-[0028]. Though Onoda does not explicitly refer to a CMOS device, a POSITA would have recognized from Onoda’s disclosure that its devices are CMOS devices. However, regardless of whether Onoda’s devices are CMOS, a POSITA would have been motivated to apply Onoda’s processing technique for making improved devices containing NMOS and PMOS to Wolf’s CPU and DRAM devices (as to claims 9 and 10, respectively) using CMOS technology for the benefit of improved latch-up resistance, punch-through breakdown voltage, and junction breakdown voltage.

See id.

improves latch-up resistance, punch-through breakdown voltage, and junction voltage) to improve similar devices (known CPU and DRAM designs) in the same way (fabricating semiconductor devices containing both NMOS and PMOS) and (2) a simple substitution of one known element (CMOS technology in prior art CPUs and DRAMs) with another (Onoda's process technology with improvement to NMOS and PMOS). There would have been a reasonable expectation of success with predictable results because Onoda's process regarding NMOS and PMOS was a known improvement over conventional CMOS process and would have been used for its intended purpose in manufacturing known CPU and DRAM devices using CMOS technology.

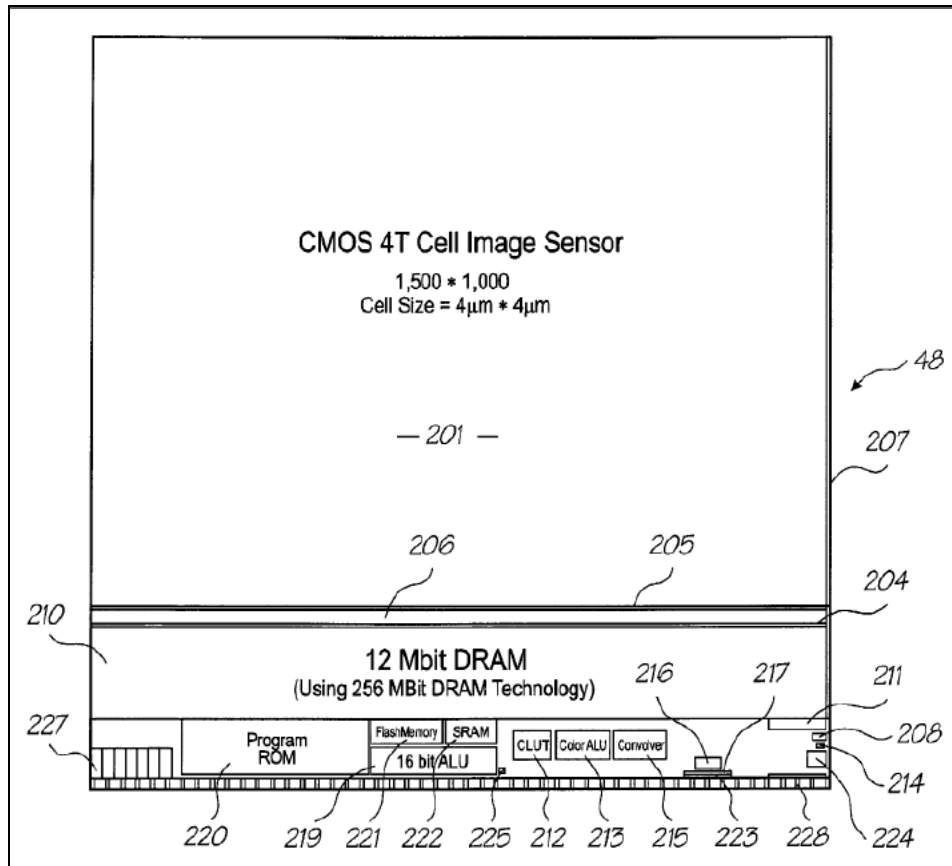
F. Ground VII

1. Dependent Claim 12: "The semiconductor device of claim 7 wherein the semiconductor device is an image sensor."

222. As I discussed in Section X.A.I, Payne renders claim 7 obvious. In my opinion, the combination of Payne and Silverbrook ("Payne-Silverbrook") renders obvious the additional limitation of claim 12.

223. Payne teaches an improvement on "twin tub" (twin-well) CMOS technology to reduce separation "between source and drain regions of adjacent [transistor] devices" and thus increase packing density of CMOS semiconductor devices. Ex.1005, Abstract, 1:5-8, 1:51-68, 6:17-21, 6:57-59, 1:9-50; §X.A. Silverbrook discloses a CMOS image sensor. Ex.1047, 6:41-13:39. An example of

such an image sensor from Silverbrook (called “Image Capture and Processing Chip (ICP)”) is pictured below.



Ex.1047, FIG. 15. Silverbrook’s ICP includes “CMOS logic, a CMOS image sensor, DRAM, and analog circuitry.” *Id.*, 6:56-57.

224. In my opinion, it would have been obvious to fabricate known CMOS logic or CMOS image sensors in Silverbrook’s ICP using Payne’s improved twin-well CMOS technology for the benefit of increased packing density. Additionally, using Payne’s technology to form CMOS logic or CMOS image sensors would have merely amounted to (1) use of a known technique (Payne’s improved twin-well CMOS process) to improve similar devices (known image sensor device

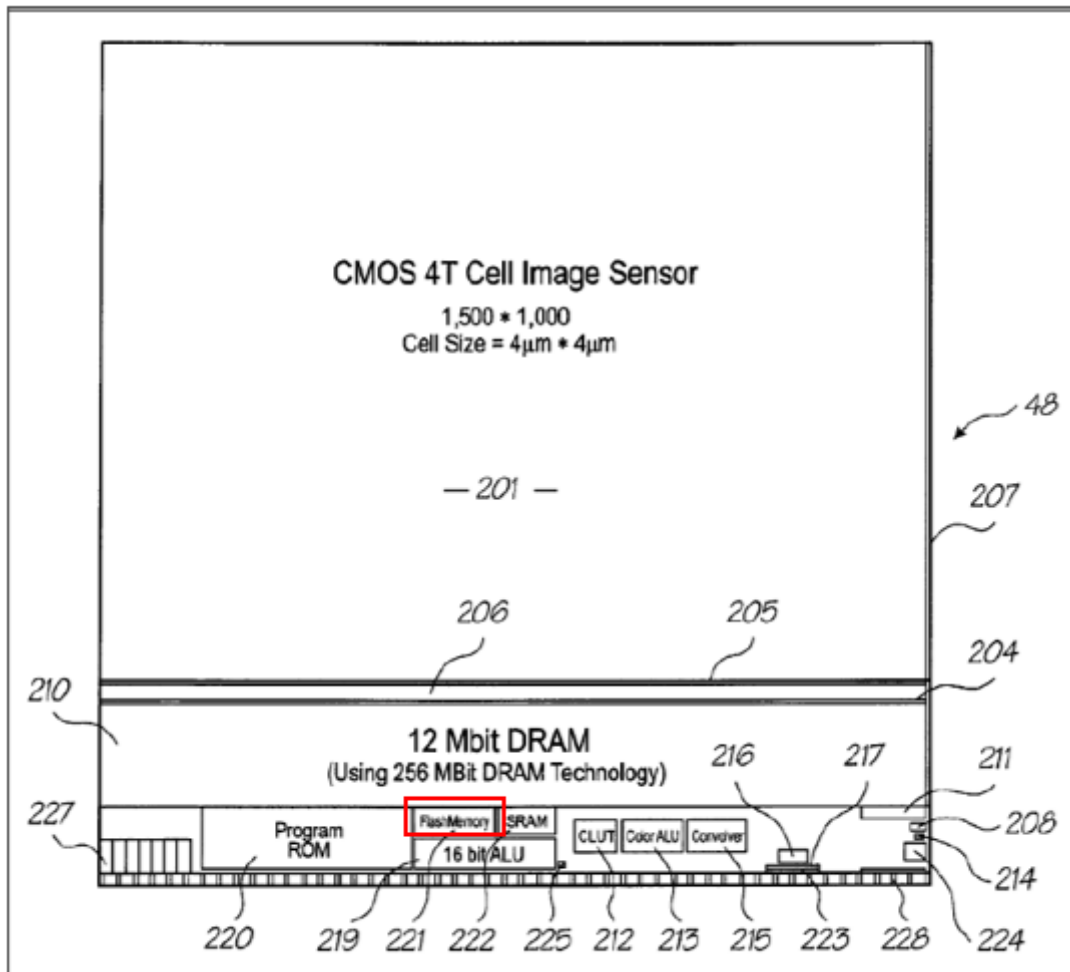
designs) in the same way (to increase packing density) and (2) a simple substitution of one known element (CMOS technology for prior art image sensors, as disclosed in Silverbrook) with another (Payne's improved CMOS technology). *Id.* There would have been a reasonable expectation of success with predictable results because Payne's twin-well CMOS process was a known improvement over conventional twin-well CMOS process and would have been used for its intended purpose in manufacturing known image sensors, designed for implementation using CMOS technology. *Id.*

G. Ground VIII

1. Dependent Claim 12: "The semiconductor device of claim 7 wherein the semiconductor device is an image sensor."

225. As I discussed in Section X.B.I, Onoda anticipates or else renders obvious claim 7. In my opinion, the combination of Onoda and Silverbrook ("Onoda-Silverbrook") renders obvious the additional limitation of claim 12.

226. Onoda discloses N-channel MOS (NMOS) transistors and P-channel MOS (PMOS) transistors in the peripheral circuitry of its flash memory devices. Ex.1042, [0052], [0044], [0045], Fig. 3, claim 2.



Ex.1047, FIG. 15.

228. In my opinion, it would have been obvious to use Onoda’s flash memory as the flash memory used in Silverbrook’s ICP. Onoda teaches that “[a] flash memory that is structured as described [in Onoda] has advantages,” Ex. 1042, [0085], resulting from “reducing the tendency for latch-up and for punch-through” and “increasing the junction breakdown voltage.” *Id.*, [0018]-[0028]. Because Silverbrook does not include any details about the fabrication of the flash memory, a POSITA would have been motivated to implement the flash memory

manufacturing process disclosed in Onoda, given its disclosed advantages. Further, a POSITA would have had a reasonable expectation of success in doing so because a flash memory is a common type of storage medium that can be used in various electronic devices. Further, the flash memory is part of Silverbrook's image sensor device (*i.e.*, ICP), and therefore the use of Onoda's flash memory in Silverbrook's ICP meets the added limitation of claim 12.

229. While the application disclosed in Onoda is flash memory, a POSITA would have been motivated to use Onoda's manufacturing process to make the CMOS logic or CMOS image sensor in Silverbrook's ICP. A CMOS device, by definition, has "N-channel MOS [(NMOS)] transistor[s]" and "P-channel MOS [(PMOS)] transistors." Ex.1008A, 807-09; *see also* Ex.1008B, 368 ("Complementary MOS (CMOS) is so-named because it uses both *p*- and *n*-type (complementary) MOS transistors in its circuits."). Though Onoda does not explicitly refer to a CMOS device, a POSITA would have recognized from Onoda's disclosure that its devices are CMOS devices. However, regardless of whether Onoda's devices are CMOS, in my opinion, a POSITA would have been motivated to apply Onoda's process for making improved devices containing NMOS and PMOS to Silverbrook's CMOS logic or CMOS image sensors for the benefit of improved latch-up resistance, punch-through breakdown voltage, and junction breakdown voltage.

230. Using Onoda's technology to form CMOS logic or CMOS image sensors would have merely amounted to (1) use of a known technique (Onoda's process to improve latch-up resistance, punch-through breakdown voltage, and junction voltage) to improve similar devices (known image sensor device designs) in the same way (to make semiconductor devices containing NMOS and PMOS) and (2) a simple substitution of one known element (CMOS technology for prior art image sensors, as disclosed in Silverbrook) with another (Onoda's technology with improvement to NMOS and PMOS). *Id.* There would have been a reasonable expectation of success with predictable results because Onoda's process regarding NMOS and PMOS was a known improvement over conventional CMOS process and would have been used for its intended purpose in manufacturing known image sensors, designed for implementation using CMOS technology. *Id.*

XI. CUMULATIVENESS

231. In my opinion, none of the references relied on in this petition are cumulative of references cited during prosecution. I understand that in its POPR to the terminated IPR2022-00290, Patent Owner argued that Payne is cumulative with Rhodes on the alleged ground that the nested well structure of Payne is nothing more than a single well formed with multiple implants. Ex. 1016, 25-41. In my opinion, this is incorrect.

232. **First**, Figure 2 of Onoda expressly discloses forming P-type well regions (105a through 105c) and N-type well regions (103, 106a through 106c) in a lightly-doped semiconductor layer 102 that is formed through epitaxial deposition. Ex.1042, FIG. 2. Thus, Onoda's well regions (105a, 105b, 105c, 103, 106a, 106b, and 106c) and semiconductor layer 102 are formed in a manner that is different and distinct than the process disclosed in Rhodes.

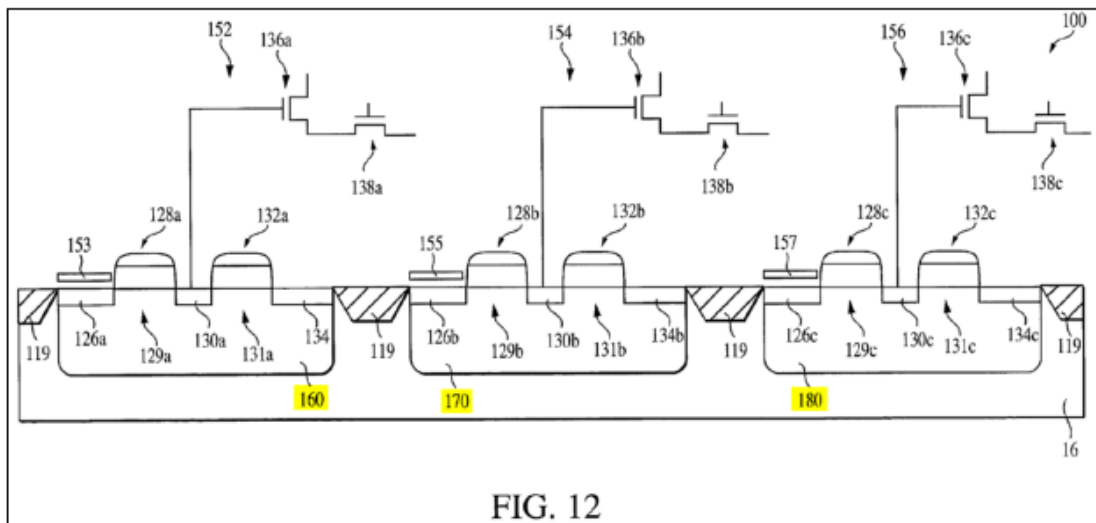
233. **Second**, Payne's nested well structure, in which shallow wells are formed in deeper wells with *separate* implants *and* annealing steps, differentiates Payne from Rhodes which does not teach a nested well structure. As Payne describes and illustrates in Figures 2 and 5-9, the deep wells ("tub regions") of Payne's nested well structure are formed first, using their own specific masks, ion implantation and thermal drive-in process steps. Ex. 1005, 3:17-4:30.

234. The shallow wells ("surface regions") are then separately formed, using different masks, ion implantation and thermal drive-in process steps. Ex. 1005, 4:31-5:17, 5:44-55. Payne's separately formed deep and shallow wells, such as wells 15 and 18, are not a single well formed using multiple implants. *Id.*

235. **Third**, in my opinion, a POSITA would have understood Payne's tub and surface regions to constitute distinct wells. That understanding is consistent with Sakai, which uses separate implants and annealing steps to form each well of

its nested well structure and uses the term “well” to refer to distinct wells. Ex. 1006, 5:56-6:4, 6:24-28, 6:52-58, FIGS. 10A, 10B.

236. In my opinion, in contrast to Payne’s structures, Rhodes teaches a twin-well architecture with side-by-side wells 160/170/180 (shown below) that Payne seeks to improve upon with its nested well structure. Ex. 1011, [0064]; Ex. 1005, 1:24-68; Ex. 1006, 1:6-2:39.



Ex. 1011, FIG. 12, [0064].

237. It is also my opinion that Rhodes does not mention or suggest (in paragraph [0064] or otherwise) forming a nested well structure, and thus does not teach a “well region disposed in [a] single drift layer.” This was the reason the Examiner allowed the claims to issue over Rhodes (and other art, including Kamins and Jastrzebski). Ex. 1046, 346.

238. I have reviewed the file histories. I note that nowhere in the prosecution did the Applicant or Examiner discuss nested well structures, as Payne and Sakai disclose. Thus, in my opinion, there is no support for Patent Owner's argument in the POPR that "it is reasonable to infer that the Examiner agreed with the argument Patent Owner makes explicitly herein that a multiple-implant well does not disclose a well region disposed in a single drift layer." Ex. 1016, 27.

239. I understand that Patent Owner also implied in its POPR that the Applicant overcame Rhodes-based rejections during prosecution by adding the "drift layer" limitation to the pending claims. Ex. 1016, 22-24. In my opinion, this is incorrect. Applicant overcame Rhodes-based rejections on the basis that Rhodes is a "CMOS imaging device," and by amending claims to include a "graded dopant concentration in the...active channel regions," (a limitation that was later removed). Ex. 1046, 94-96. The "drift layer" limitation was added much later in the process after several intervening rejections. There is no indication the Examiner specifically considered Rhodes in relation to the "drift layer" limitation, let alone the "well region disposed in said single drift layer" limitation.

XII. CONCLUSION

240. For the aforementioned reasons, in my opinion, to a person of ordinary skill in the art, the Challenged Claims of the '502 Patent are rendered obvious by the prior art.

241. I understand that the Patent Owner has not asserted secondary considerations of non-obviousness. I reserve the right to respond to any such assertions.

242. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the results of the proceedings.

Date: October 27, 2023

Respectfully submitted,



Sanjay Banerjee, Ph.D.