

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TEXAS INSTRUMENTS INCORPORATED,

Petitioner

v.

GREENTHREAD LLC,

Patent Owner

Patent No. 9,190,502
Case No. IPR2024-00773

**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO.
9,190,502**

UNDER 35 U.S.C. §§ 312 AND 37 C.F.R. § 42.104

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TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 9,190,502 to Rao (the “’502 Patent”)
1002	Prosecution History of the ’502 Patent (“the Prosecution History”)
1003	Declaration of Sanjay Banerjee, PhD
1004	Curriculum Vitae of Sanjay Banerjee, PhD
1005	U.S. Patent No. 4,684,971 (“Payne”)
1006	U.S. Patent No. 4,907,058 to Sakai (“Sakai”)
1007	U.S. Patent No. 6,043,114 to Kawagoe, et al., (“Kawagoe”)
1008A	Wolf and Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol 1, Lattice Press (2000) (“Wolf.1”)
1008B	Wolf and Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol. 2, Lattice Press (2000) (“Wolf.2”)
1008C	Wolf and Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol. 3, Lattice Press (2000) (“Wolf.3”)
1008D	Wolf and Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol. 4, Lattice Press (2000) (“Wolf.4”)
1009	U.S. Patent No. 4,160,985 (“Kamins”)
1010	U.S. Patent No. 4,481,522 (“Jastrzebski”)
1011	U.S. Patent Application Publication No. 2003/0042511 (“Rhodes”)
1012	U.S. Patent Application Publication No. 2002/0102783 (“Fujimoto”)
1013	Wang and Agrawal, <i>Single Event Upset: An Embedded Tutorial</i> , 21st Intl Conf on VLSI Design, IEEE 2008 (“Wang”)
1014	Publication Declaration of Alyssa G. Resnick for Wolf.1 and Wolf.2 (“Resnick Decl.”)
1015	Publication Declaration of Rachel J. Watters for Wolf.3 and Wolf.4 (“Watters Decl.”)
1016	IPR2020-290, Patent Owner Preliminary Response
1017	U.S. Pat. No. 11,121,222 (the “’222 Patent”)
1018	U.S. Pat. No. 11,316,014 (the “’014 Patent”)
1019	Civil Action No. 2:19-cv-00147-JRG, Dkt. 67 (E.D. Tex. Apr. 20, 2019)

Exhibit No.	Description
1020	Prosecution History of U.S. Pat. No. 11,121,222
1021	Prosecution History of U.S. Pat. No. 11,316,014
1022	U.S. Patent Application Publication No. 2004/0063288 (“Kenney”)
1023	Jaeger, <i>Introduction to Microelectronic Fabrication</i> , Vol. V, Addison-Wesley Modular Series on Solid State Devices (1988) (“Jaeger”)
1024	U.S. District Courts – Case Statistics, obtained at https://www.uscourts.gov/statistics-reports/analysis-reports/federal-court-management-statistics , dated June 30, 2023
1025	U.S. Patent No. 4,435,896 (“Parrillo”)
1026	L.C. Parrillo, R.S. Payne et al., <i>Twin-Tub CMOS - A Technology for VLSI Circuits</i> , IEEE 1980 (“Parrillo2”)
1027	U.S. Patent Application Publication No. 2007/0045682 to Hong et al. (“Hong”)
1028	The Oxford American Dictionary and Language Guide, Oxford University Press (1996)
1029	Blank
1030	Patent Owner’s Responsive Claim Construction Brief
1031	Blank
1032	Patent Owner’s Sur-Reply Claim Construction Brief
1033	Proposed Claim Constructions in the District Court Case
1034	Redacted District Court Case Transfer Order
1035	Civil Action No. 2:19-cv-00147-JRG, Dkt. 105 (E.D. Tex. Jul. 9, 2020)
1036	Publication Declaration of Sylvia Hall-Ellis for Wolf
1037	Dec. 21, 2022 Preliminary Claim Constructions in 6:22-CV-00105
1038	U.S. Patent Application Publication No. 2003/0183856 to Wiczorek (“Wiczorek”)
1039	Parrillo IEEE Citation List
1040	Dictionary of Scientific and Technical Terms, McGraw Hill (2003)
1041	Blank
1042	Certified translation of Japanese Unexamined Patent Application Publication No. H8-279598 (“Onoda”)
1043	Japanese Unexamined Patent Application Publication No. H8-279598, published on October 22, 1996
1044	IPR2020-290, Termination Order

Exhibit No.	Description
1045	Oct. 31, 2022 Giapis Declaration, 6:22-CV-00105
1046	Prosecution History of U.S. Patent No. 8,421,195
1047	U.S. Patent No. 6,614,560 to Silverbrook (“Silverbrook”)
1048	U.S. Patent No. 8,421,195 to Rao (the “’195 Patent”)
1049	U.S. Patent No. 5,986,924 (“Yamada”)
1050	Rabaey <i>et al.</i> , <i>Digital Integrated Circuits, A Design Perspective</i> , Prentice Hall Electronics and VLSI Series (2003) (“Rabaey”)
1051	Sze, <i>Semiconductor Devices Physics and Technology</i> , 2d Ed., John Wiley & Sons (2002)
1052	Publication Declaration of Sean O’Bryan for Maziasz (“O’Bryan Decl.”)
1053	Publication Declaration of Martin L. Knott for Rabaey (“Knott Decl.”)
1054	Maziasz and Hayes, <i>Layout Minimization of CMOS Cells</i> , Kluwer Academic Publishers (1992) (“Maziasz”)
1101	Petitioner’s <i>Sotera</i> stipulation sent to Patent Owner on April 10, 2024

Petition for *Inter Partes* Review of U.S. Patent No. 9,190,502

Texas Instruments Incorporated (“Petitioner” or “TI”), requests *inter partes* review (“IPR”) of claims 7-12 (the “Challenged Claims”) of U.S. Patent No. 9,190,502 (Ex.1001, “’502 Patent”). This Petition is accompanied by a Motion for Joinder to join pending IPR proceeding *Cirrus Logic, Inc., et al. v. Greenthread, LLC*, IPR2024-00018.

I. INTRODUCTION

The ’502 Patent is directed to a Complementary Metal-Oxide Semiconductor (CMOS) device having graded dopant concentrations. Ex.1001, 4:52-67. This Petition demonstrates that the Challenged Claims are unpatentable as obvious.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner Texas Instruments Incorporated is the real party-in-interest.

B. Related Matters

The ’502 Patent is the subject of the following active proceedings:

- *Greenthread, LLC v. Cirrus Logic, Inc.*, Civil Action No. 1:23-cv-00369 in the Western District of Texas, filed March 31, 2023 (“Cirrus District Court Case”);
- *Greenthread, LLC v. OmniVision Technologies, Inc.*, Civil Action No. 2:23-cv-00212 in the Eastern District of Texas, filed May 10, 2023 (“OmniVision District Court Case”);

Petition for *Inter Partes* Review of U.S. Patent No. 9,190,502

- *Greenthread, LLC v. OSRAM GmbH et al.*, Civil Action No. 2:23-cv-00179 in the Eastern District of Texas, filed April 19, 2023 (“ams- OSRAM District Court Case”);
- *Greenthread, LLC v Texas Instruments Incorporated*, Civil Action No. 2:23-cv-00157 in the Eastern District of Texas, filed April 6, 2023;
- *Greenthread, LLC v. Monolithic Power Systems, Inc.*, Civil Action No. 1:23-cv-00579 in the District of Delaware, filed May 26, 2023;
- *Cirrus Logic, Inc., et al. v. Greenthread, LLC*, IPR2024-00018 before the Patent Trial and Appeal Board, filed October 27, 2023;
- *Semiconductor Components Industries, LLC v. Greenthread, LLC*, IPR2024-00265 before the Patent Trial and Appeal Board, filed December 11, 2023; and
- *Monolithic Power Systems, Inc. v. Greenthread, LLC*, IPR2024-00469 before the Patent Trial and Appeal Board, filed February 3, 2024.

The '502 Patent was previously subject to the following proceedings, which are no longer pending:

- *Greenthread, LLC v. Samsung Electronics Co., Ltd.. et al*, Civil Action No. 2-19-cv-00147 in the Eastern District of Texas, filed April 30, 2019
- *Samsung Electronics Co., Ltd. v. Greenthread, LLC*, IPR2020-00290

before the Patent Trial and Appeal Board, filed December 23, 2019;

- *Greenthread, LLC v. Intel Corporation, Dell Inc., and Dell Technologies Inc.*, Civil Action No. 6:22-cv-105 in the Western District of Texas (“Intel Litigation”), filed January 27, 2022;
- *Greenthread, LLC v. Intel Corporation*, Civil Action No. 6:22-cv-01293 in the Western District of Texas, severed December 21, 2022, and transferred to District of Oregon as 3:22-cv-02001;
- *Greenthread, LLC v. Micron Technology, Inc. et al.*, Civil Action No. 1:23-cv-00333 in the District of Delaware, filed March 24, 2023;
- *Intel Corporation v. Greenthread, LLC*, IPR2023-00541, before the Patent Trial and Appeal Board, filed January 30, 2023; and
- *Greenthread, LLC v. Western Digital Corporation et al*, Civil Action No. 1:23-cv-00326 in the District of Delaware, filed March 24, 2023.

C. Counsel Service Information

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D. 37 C.F.R. §42.8(b)(4): Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR12189-0085IP1@fr.com (referencing No. 12189-0085IP1 and cc'ing PTABInbound@fr.com, griswold@fr.com and bisenius@fr.com).

III. PAYMENT OF FEES UNDER 37 C.F.R. §42.103

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. 06-1050. Review of 6 claims is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

IV. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under Rule 42.104(a) that the '502 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the grounds identified in this Petition.

V. OVERVIEW OF CHALLENGE AND REQUESTED RELIEF

A. Prior Art Printed Publications

The '502 Patent claims priority to September 3, 2004. Petitioner's challenge is based on the following prior-art references, none of which were before the Patent Office during prosecution of the '502 Patent:

- **Payne** – U.S. Patent No. 4,684,971 to Payne (Ex.1005) issued on August 4,

1987 and is prior art under §102(b).¹

- **Onoda** – Japanese Application H8-279598 to Onoda (Ex.1043, certified translation Ex.1042) published on October 22, 1996 and is prior art under §102(b).
- **Wolf** – Wolf and Tauber, *Silicon Processing*, Lattice Press (2000) (Ex.1008A- D), was published and publicly available no later than 2002, and is prior art under §102(b). Exs. 1014-1015; Ex.1036.²
- **Parrillo** - U.S. Patent No. 4,435,896 to Parrillo and Payne (Ex.1025) issued on March 13, 1984 and is prior art under §102(b).
- **Silverbrook**: U.S. Patent No. 6,614,560 to Silverbrook (Ex.1047) issued September 2, 2003 and is prior art under §102(b).

B. Relief Requested

The specific grounds of the challenge are set forth below and are supported by the declaration of Dr. Banerjee (Ex.1003).

Ground	Basis	Challenged Claims	Reference(s)
I	§ 103	7	Payne
II	§ 102	7, 8, 11	Onoda

¹ Cites to 35 U.S.C. §§102 and 103 are to the pre-America Invents Act (pre-AIA).

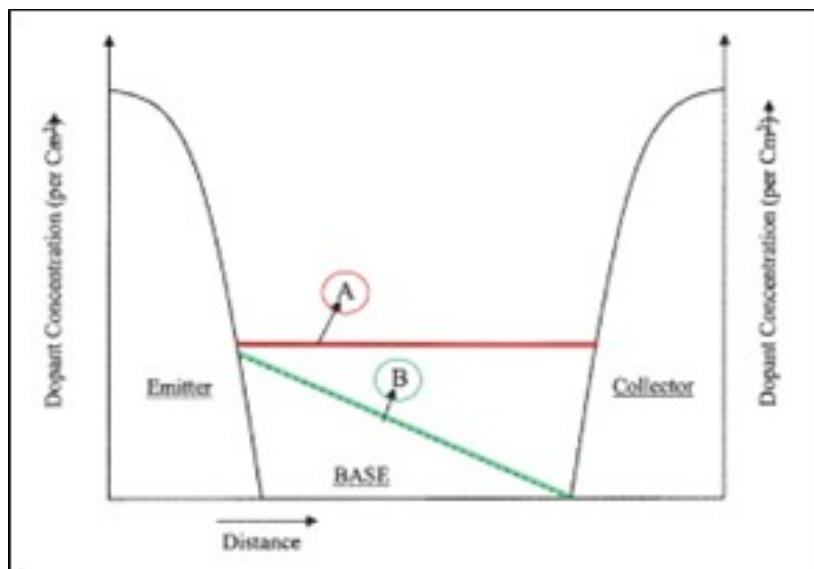
² Petitioner is relying on independent librarian expert, Dr. Sylvia Hall-Ellis, to verify the public availability of the Wolf reference.

III	§ 103	7, 8, 11	Onoda
IV	§ 103	8	Payne, Parrillo
V	§ 103	9-11	Payne, Wolf
VI	§ 103	9, 10	Onoda, Wolf
VII	§ 103	12	Payne, Silverbrook
VIII	§ 103	12	Onoda, Silverbrook

VI. THE '502 PATENT

The '502 Patent is directed to “grading the dopant concentration” in certain regions of a semiconductor device. Ex.1001, Title, Abstract. The Challenged Claims claim that a single drift layer (SDL) and a well region of a semiconductor device have graded dopant concentrations to aid movement of minority carriers from the surface layer to the substrate. *Id.*, Cl. 7.

The '502 Patent admits that graded dopant concentrations were known. For example, the graded dopant concentration “B” (green) in Figure 1 below is described as one of “the two most popular” doping profiles used in prior art bipolar transistors, in contrast to the uniform doping profile “A” (red). Ex.1001, 2:17-19.



Ex.1001, FIG. 1 (“Prior Art”).³ The ’502 Patent further admits that it was known to grade the dopant concentration in well regions of CMOS devices to affect the movement of carriers, but alleges, without support, that prior attempts were met with “little success.” *Id.*, 1:63-2:9.

The claims of the ’502 Patent issued after a terminal disclaimer was filed to overcome a double patenting rejection over the issued claims of the parent patent. Ex.1002, 50-53, 104. There were no prior art rejections. *Id.*, 53. During prosecution of the parent ’195 Patent, the Examiner found that the prior art, including Kamins and Jastrzebski, teaches all the elements of then-pending independent claim 10. Ex.1046 (12/20/11 Office Action), 3–5; (8/13/12 Office Action), 3-5. In response, Applicant amended claim 10 to add an element which recites “at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants” and which is substantially the same

as current element [7.6]. Ex.1046 (10/15/12 Office Action Response), 3. The Examiner allowed the as- amended claim 10 (issued claim 1 of the '195 Patent) and claims depending therefrom, citing this added element as the reason for allowance of these claims. Ex.1046, (12/12/12 Notice), 2-3; Ex.1048, claim 1.

VII. PERSON OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) of the subject matter of the '502 Patent would have had a Bachelor’s degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. Ex.1003, ¶¶57-60. Additional education might compensate for a deficiency in experience, and vice-versa. *Id.* Notably, in the Intel Litigation, Patent Owner agreed with this characterization of a POSITA. Ex.1045, ¶13.

VIII. CLAIM CONSTRUCTION

Claims in an IPR are construed under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). 37 C.F.R. §42.100(b). Petitioner is aware that Patent Owner took positions on the meaning of certain claim terms, which are listed below. *See* Exs. 1030, 1032-1033.⁵

⁵ As to the “active region” terms, Patent Owner’s position is reflected in its claim construction briefing. *See* Ex.1030, 28, 40.

Claim Term	Patent Owner’s Proposed Construction
“substrate”	Plain and ordinary meaning, where the plain and ordinary meaning is an “underlying layer”
“active region”	Plain and ordinary meaning (“a doped silicon region at the surface of a semiconductor device where a transistor can be formed”)
“to aid carrier movement from . . . [to/towards] . . .”	Plain and ordinary meaning
“well region”	Plain Meaning (“a doped region that surrounds the active region of a semiconductor device”)
“active region ... within which transistors can be formed”	Plain Meaning (“a doped silicon region at the surface of a semiconductor device where a transistor can be formed”)

Petitioner is further aware that, in the Intel Litigation, the Court provided its “preliminary constructions” in advance of the claim construction hearing, in which the Court offered a “preliminary construction” of plain and ordinary meaning as to each of the above-listed terms. *See* Ex. 1037. Petitioner does not believe any terms need be construed to resolve the issues presented in this Petition, and Petitioner takes no position regarding claim construction at this time. The Challenged Claims are unpatentable under either their plain and ordinary meaning, or under Patent Owner’s proposed constructions (except for the term “active region ... within which transistors can be formed,” which is addressed in the sections below).

IX. SPECIFIC GROUNDS FOR PETITION

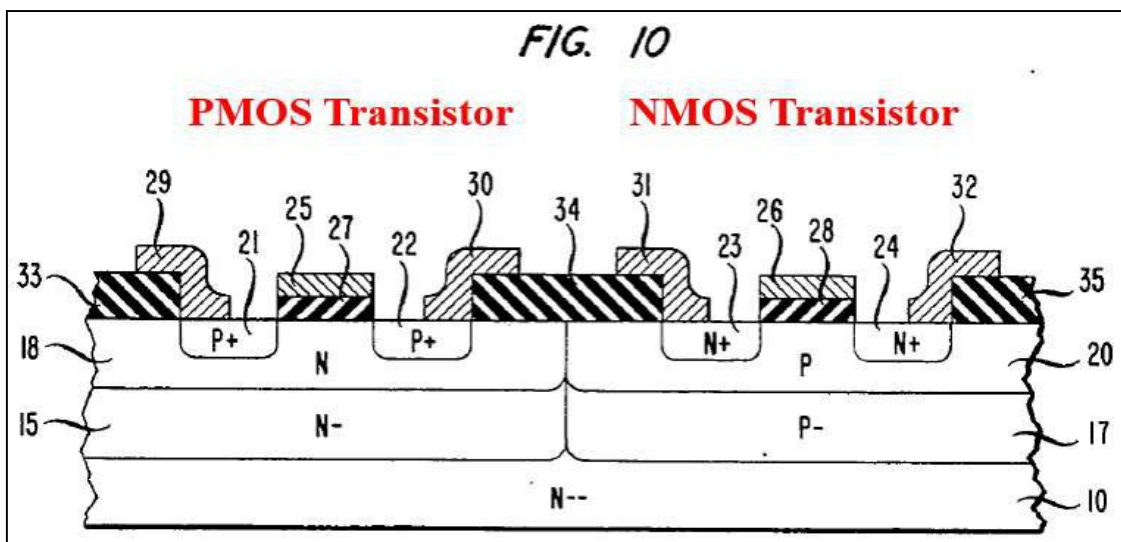
A. Ground I

Payne renders claim 7 obvious. Ex.1003, ¶¶72-119.

1. Independent Claim 7

a. Preamble: “A semiconductor device comprising:”

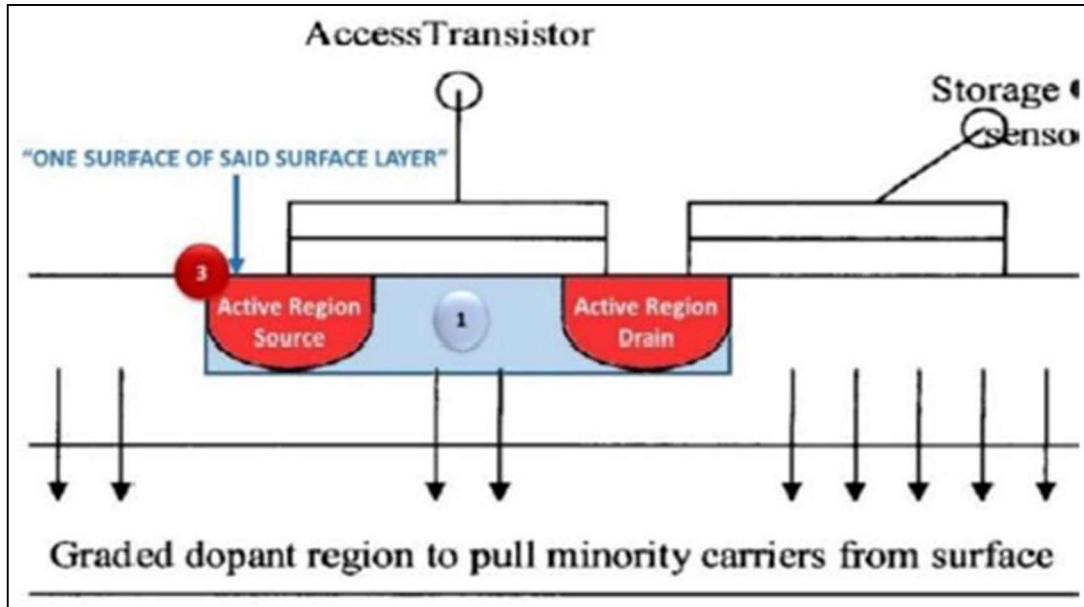
Payne is directed to a semiconductor device. Ex.1003, ¶73; Ex.1005, Title, Abstract, 1:51-54 (“it is a primary object of the invention to provide a CMOS structure and method of manufacture which requires little semiconductor space and therefore permits a high packing density.”), 1:5-15 (“Complementary field effect transistors (hereinafter designated CMOS) [] comprise n-channel and p-channel devices . . .”). Payne’s Figure 10 illustrates a “p-channel” (PMOS) transistor (with “P+” source/drain regions 21/22) adjacent to an “n-channel” (NMOS) transistor (with “N+” source/drain regions 23/24) of a CMOS semiconductor device. *Id.*, 2:50-60, 5:18-34, 6:57-59.



Ex.1005, FIG. 10.³

b. Element [7.1]: “a surface layer;”

Payne discloses, or at a minimum, renders obvious this element. Ex.1003, ¶¶74-76. According to Patent Owner (“PO”), a “surface layer” is “a layer at the surface of the silicon” (or “a layer at the surface of the semiconductor device”)—which PO annotated in blue below—“where the active region [(red)] is located.” Ex.1030, 6, 9, 12, 13; Ex.1033.

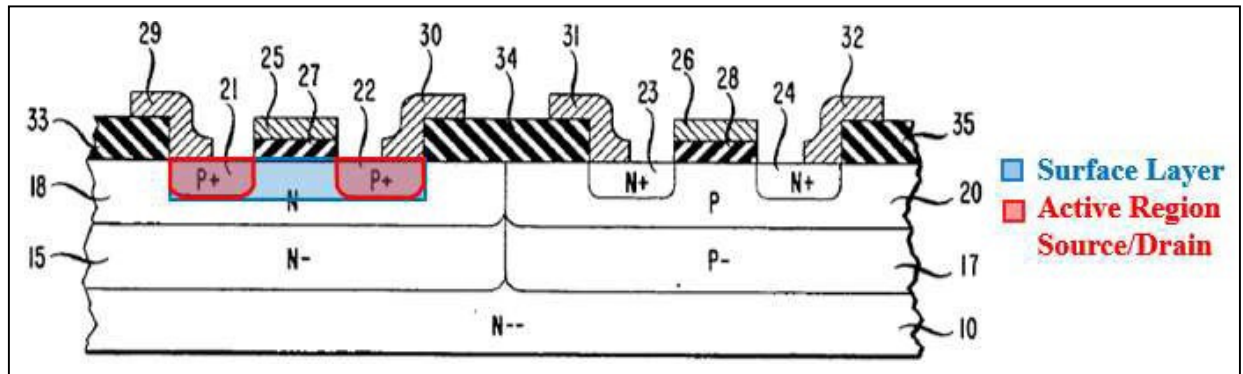


Ex.1001, FIG. 5(b); Ex.1030, 7, 12.

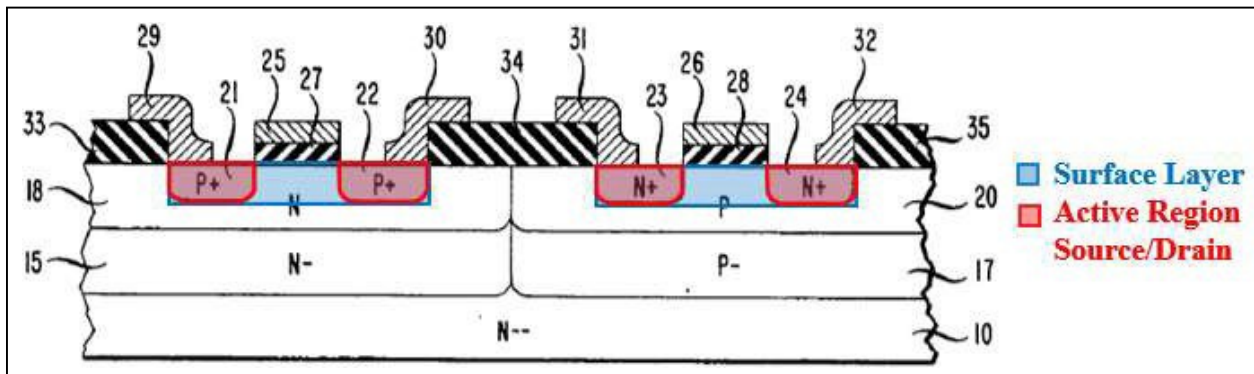
Payne satisfies element [7.1] to the same extent that Figure 5(b) of the '502 Patent meets it. Ex.1003, ¶¶74-75. Payne's Figure 10 discloses a surface layer (blue) that matches the surface layer PO identified in Figure 5(b). Payne's surface layer—

³ All colors and colored annotations to figures added.

a subset of what Payne refers to as “surface region 18”—is at the surface of silicon substrate 10, and “source and drain regions, 21 and 22 [(red)] of P+ conductivity” of Payne’s p-channel transistor (left) are located in it. Ex.1005, 2:50-60; 5:21-27, 6:57-59, FIG. 1.



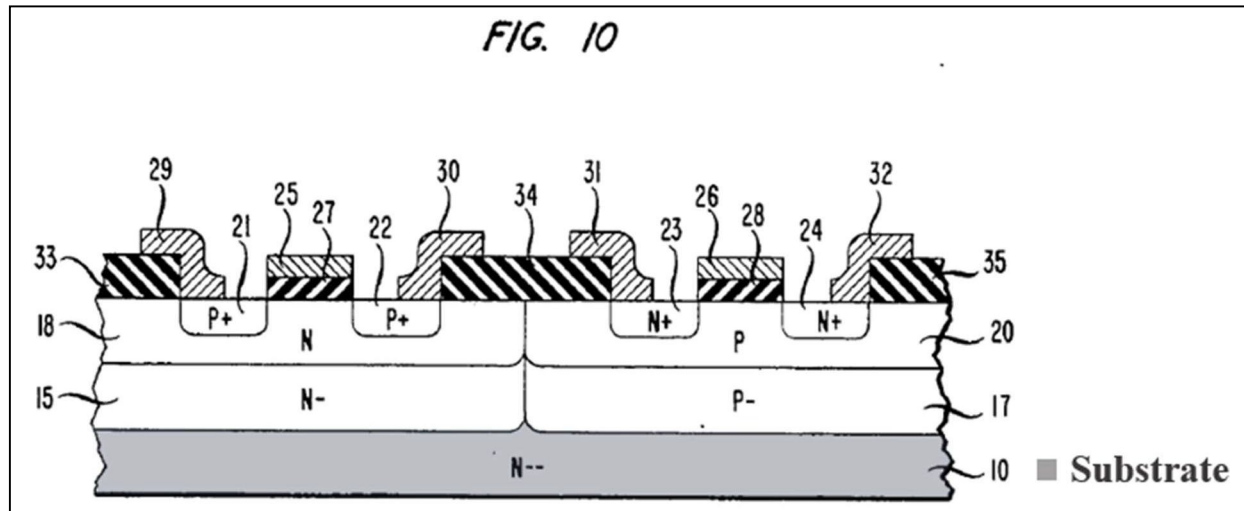
Ex.1005, FIG. 10. Payne likewise discloses another surface layer—a subset of “surface region 20”—containing “source and drain regions, 23 and 24, of N+ conductivity” of Payne’s n-channel transistor (right). *Id.*, 5:24-27, 6:57-59; Ex.1003, ¶76.



Ex.1005, FIG. 10.

c. Element [7.2]: “a substrate;”

Payne discloses this element. Ex.1003, ¶¶77-78. Payne’s Figure 10 illustrates a CMOS device “fabricated in a silicon semiconductor *substrate* [(grey)] 10 of ‘N-’ conductivity type which typically has a doping concentration of approximately $1-2 \times 10^{14}$ ions/cm³[.]” Ex.1005, 1:60-62, 2:50-60.⁴

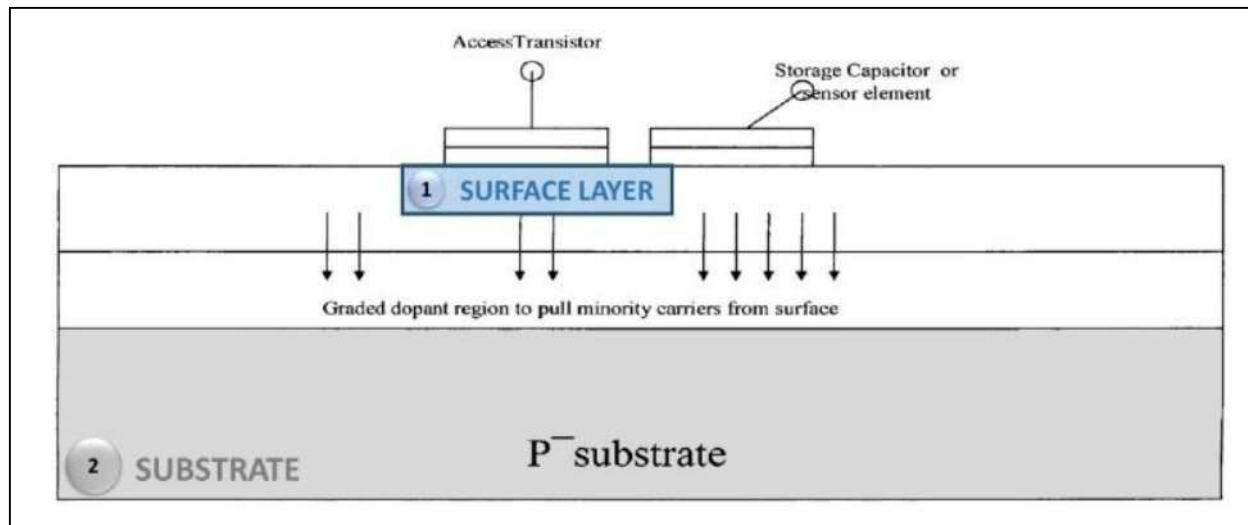


Ex.1005, FIG. 10.

Payne satisfies element [7.2] under PO’s proposed construction of “plain and ordinary meaning [*i.e.*] ‘an underlying layer.’” Ex.1033. Payne’s substrate also matches PO’s identification of the substrate (grey) in Figure 5(b) of the ’502 Patent.⁵

⁴ All emphases added unless otherwise noted.

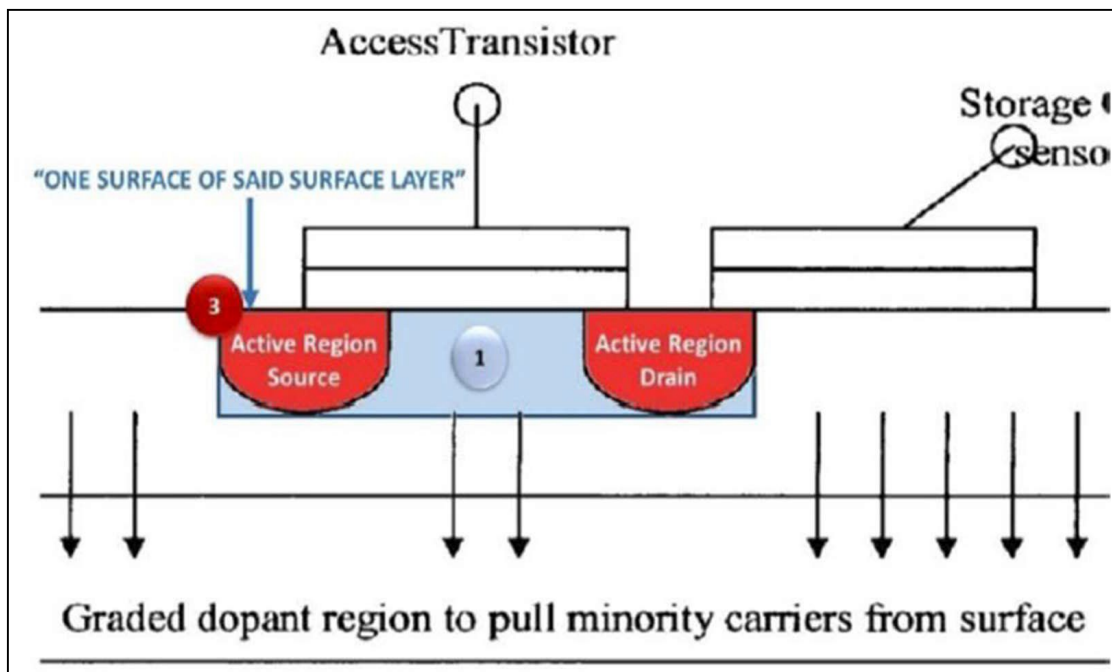
⁵ Patent Owner used Figure 5(b) from the parent '195 Patent as an example. Ex. 1030, 5-6. The '502 Patent and the '195 Patent have the identical specification and figures, including Figure 5(b).



Ex.1030, 6-7, 16-17 (well region and drift layer can be part of substrate);
 Ex.1001, FIG. 5(b). *See also* Ex.1005, 1:60-65, 2:50-60 (“the [CMOS] device is fabricated in a silicon semiconductor substrate, 10”), FIGS. 1, 10.

- d. Element [7.3]: “an active region including a source and a drain, disposed on one surface of said surface layer;”**

Payne discloses or, at a minimum, renders obvious this element. Ex.1003, ¶¶79-83. According to PO, Figure 5(b) of the '502 Patent depicts an active region (red) “disposed on one surface [(top surface)] of said surface layer”:

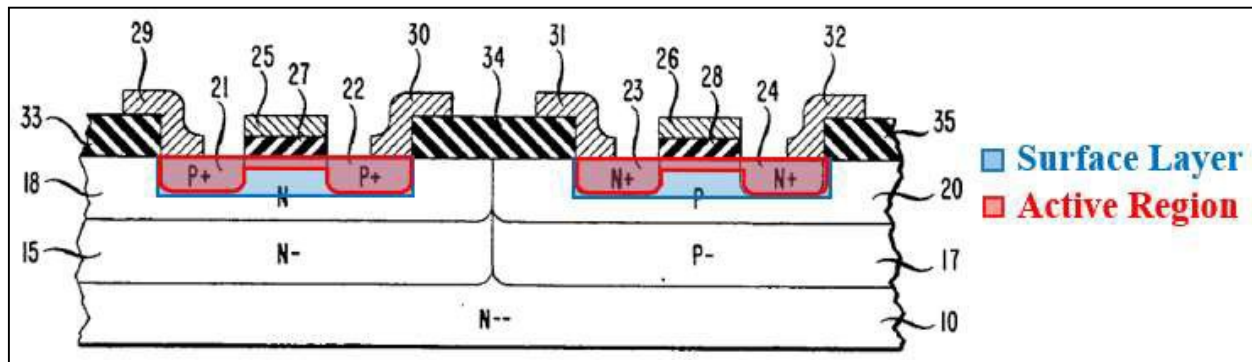


Ex.1001, FIG. 5(b); Ex.1030, 6-7, 11 (“[T]he ‘active region’ is part of the ‘surface layer’ ... When the claim says the active region is ‘disposed on one surface of the surface layer,’ it means the active region is located on the ‘ceiling’ of the silicon *inside* the silicon.”) (emphasis in original), 12.

Payne satisfies element [7.3] under PO’s interpretation. Ex.1003, ¶80. Payne’s Figure 10 below illustrates a “p-channel” transistor with source/drain regions 21/22 (left), and an “n-channel” transistor with source/drain regions 23/24 (right). Ex.1005, 5:18-29, 1:5-19, 6:57-59. These source/drain regions are formed with “a surface impurity concentration of approximately 10^{19} – 10^{20} ions/cm³.” Ex.1005, 5:21-29, 1:43-45. The channel region between these source/drain regions is part of the surface region, which has an impurity concentration of “typically 0.5 – 5×10^{16} ions/cm³.” Ex.1005, 5:51-52, 4:31-39, 4:63-5:5. The source/drain regions of a transistor,

together with the channel region in between them, form an active region. Ex.1003 ¶¶80-81; Ex.1008B, 299 (“The top surface of the [silicon substrate] body consists of active or transistor regions as well as passive or (field) regions. The **active regions** are those in which transistor action occurs; i.e., the **channel** and the heavily doped **source** and **drain** regions.”), 300, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex.1008C, 525, FIG. 8-1(e).

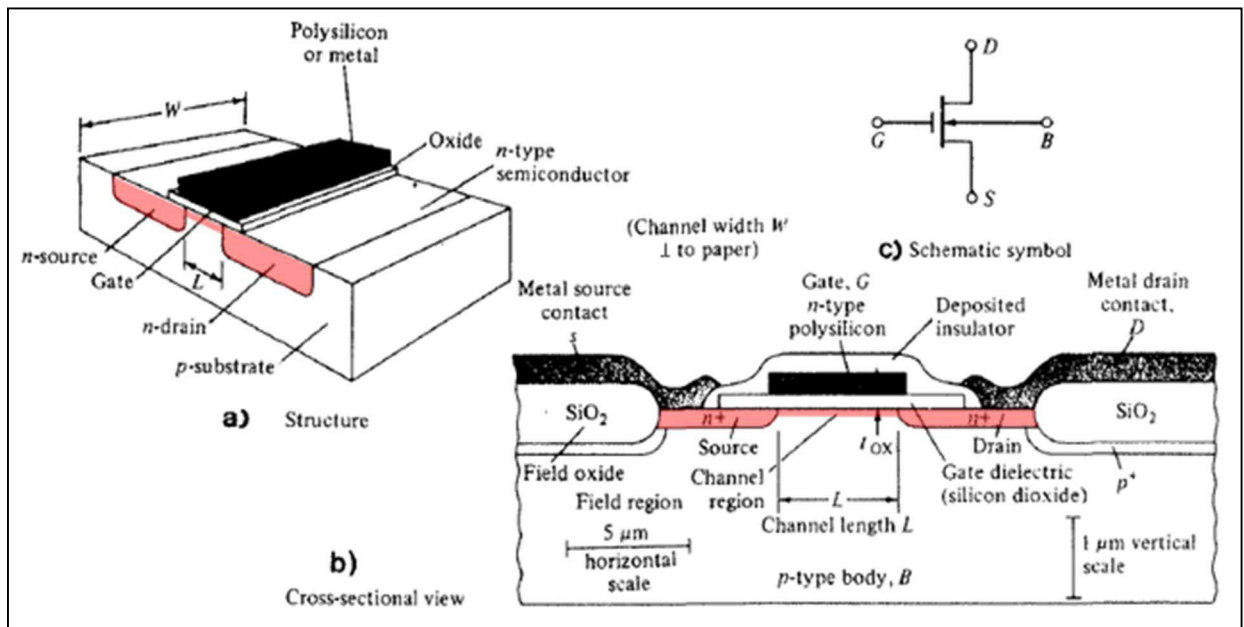
The active region (red) of each of Payne’s transistors is disposed on one surface (top surface) of a corresponding surface layer (blue), exactly as depicted in PO’s annotated Figure 5(b) above. Ex.1003, ¶82; §IX.A.1.b.



Ex.1005, FIG. 10.

Payne satisfies element [7.3] under PO’s position that “active region” means “a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed” (Ex.1033) because the active region of a MOS transistor is “[its] channel and [its] **heavily doped** source and drain regions,” highlighted in red below. Ex.1008B, 299;

Ex.1003, ¶83.

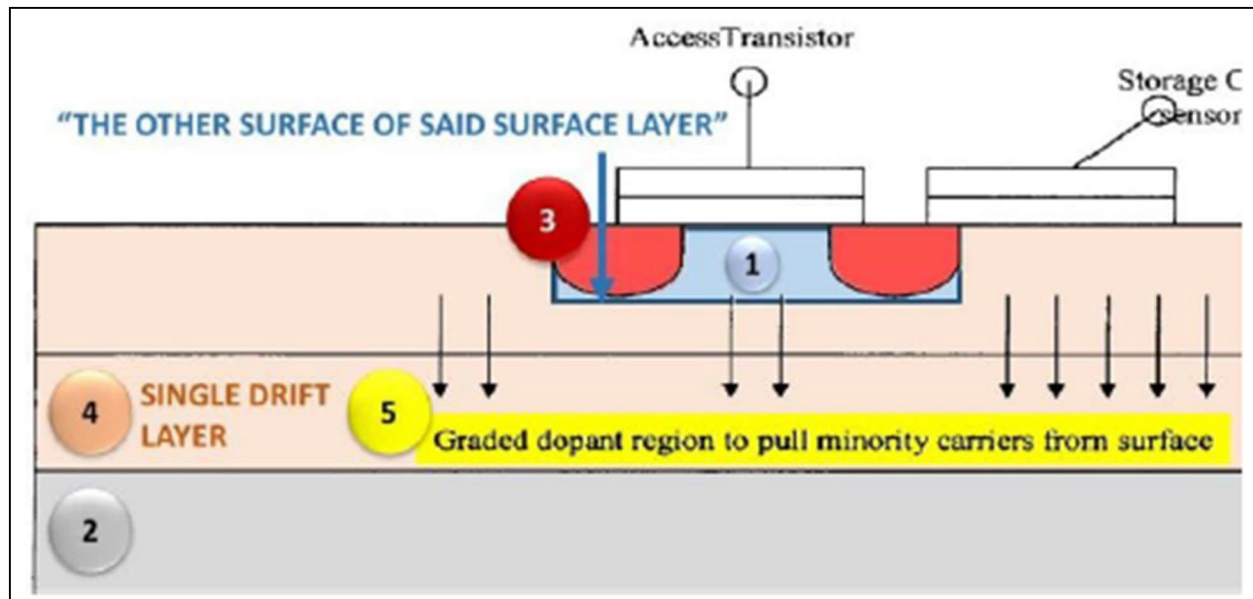


Ex.1008B, FIG. 5-1; *id.*, 298-301, 374, FIGS. 5-2, 6-4.

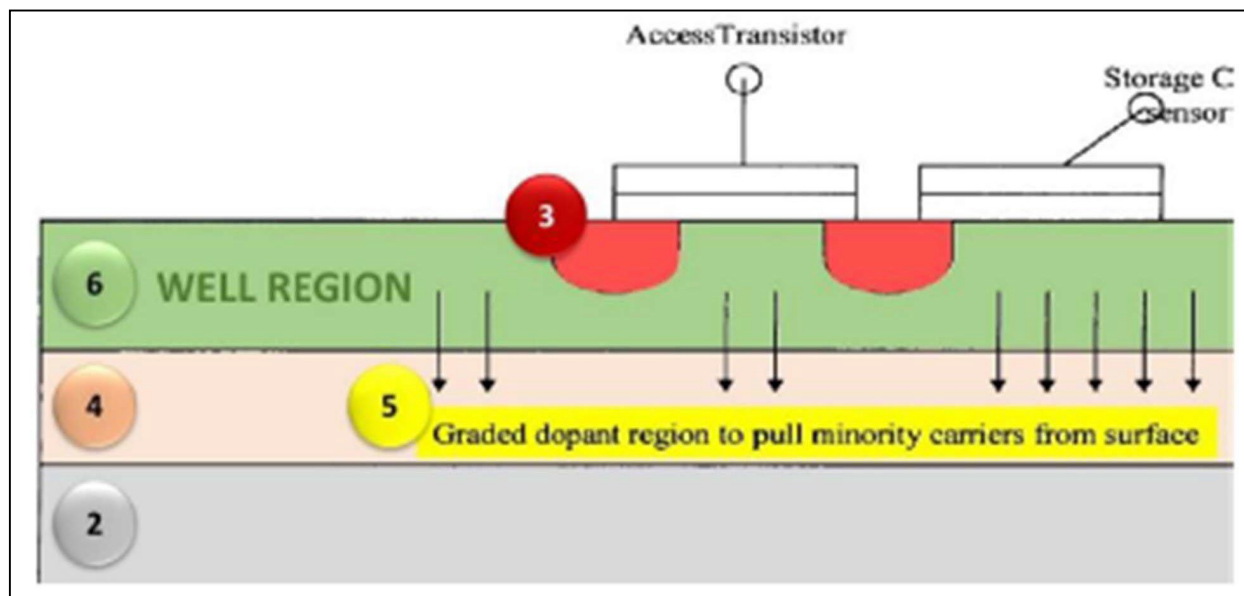
- e. **Element [7.4]: “a single drift layer disposed between the other surface of said surface layer and said substrate,”**

Payne discloses or, at a minimum, renders obvious this element. Ex.1003, ¶¶84-88.

Single drift layer (“SDL”) – In its claim construction brief, PO identified the SDL in tan in Figure 5(b). Ex.1030, 7. According to PO, the SDL (tan) is “disposed between ‘the other surface [(bottom surface)] of said surface layer [(blue)]’ and [said] substrate [(grey)]”:

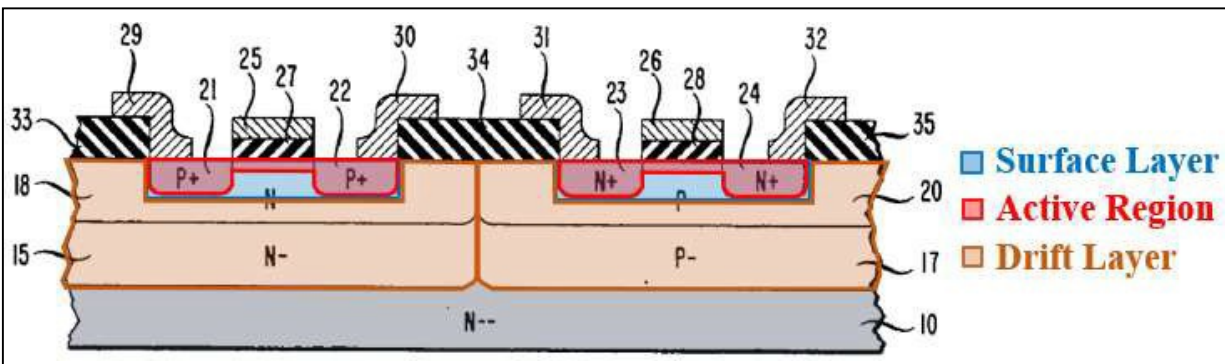


Ex.1001, FIG. 5(b); Ex.1030, 7. The SDL in Figure 5(b) has a well region (green) disposed in it, forming a nested structure, as required by the claim (*see* element [7.6]), and as shown below:



Ex.1001, FIG. 5(b); Ex.1030 at 7; *id.*, 11 ("the 'well region' is part of the 'single drift layer.'").

Payne discloses a single drift layer (SDL) to the same extent the '502 Patent's Figure 5(b) does. Ex.1003, ¶¶86-88. In Payne's Figure 10, the **"first tub region" 15 (tan)** of Payne's nested well structure—with shallow well ("surface region") 18 disposed in it—is an example of the claimed single drift layer. *Id.*; Ex.1005, 3:28-42 (ion implantation for tub 15), 4:19-30 (thermal drive-in to achieve the desired depth for tub 15), 4:31-39, 5:7-17, 5:44-48, 5:48-50 ("In a typical device, the final depth of surface regions 18 and 20 would be approximately 1-2 μ and the depth of the **tub regions 15 and 17** would be typically 3-8 μ ."). This SDL (tan) is "disposed between 'the other surface [(bottom surface)] of said surface layer [(blue)]' and [said] substrate [(grey)]" under PO's interpretation, and in exactly the same way as depicted in PO's annotated Figure 5(b) above.



Ex.1005, FIG. 10. Payne's tub 17 (right), in which shallow well 20 is disposed, is likewise an SDL (tan) disposed between a surface layer (blue) and the substrate (grey). Ex.1005, 4:3-30, 4:63-5:17, 5:44-50; Ex.1003, ¶87; §IX.A.1.b.

Payne meets all other claim requirements associated with the SDL to the same

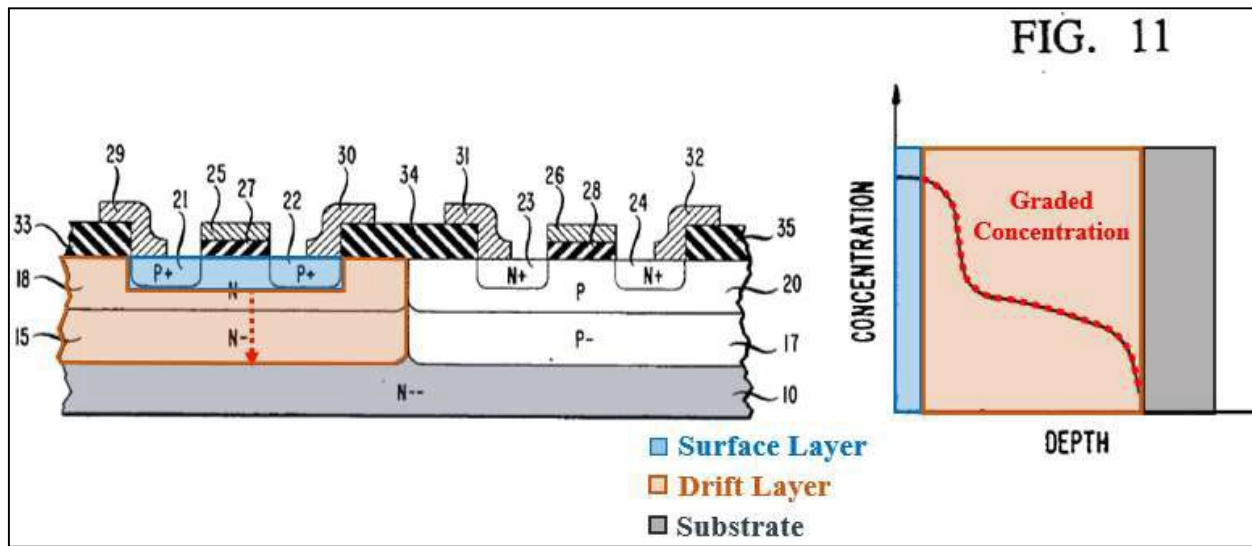
extent Figure 5(b) meets them. *See* below and elements [7.5]-[7.6]; Ex.1003, ¶¶88. Notably, as detailed in element [7.5], each of Payne’s tubs 15/17 is a *single* drift layer (SDL) because it has a graded-dopant concentration that, according to PO, creates a unidirectional electric drift field that aids the movement of minority carriers in a *single* direction—from the surface layer to the substrate. Ex.1030, 7; Ex.1046, 253-54, 289-290; §IX.A.1.f.

f. Element [7.5]: “said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and”

Payne discloses or, at a minimum, renders obvious this element. Ex.1003, ¶¶89-108.

Graded-dopant concentration – The ’502 Patent admits that graded-dopant concentrations were known, Ex.1001, 2:17-19, FIG. 1 (“Prior Art”), and that it was known to grade the dopant concentration in CMOS devices to affect the movement of minority carriers. *Id.*, 1:34-2:5, FIGS. 3(a)-3(d) (all “Prior art”). Payne’s SDL has a graded-dopant concentration extending between the surface layer and the substrate. Ex.1003 ¶90. Payne explains that the “impurity profile in both tubs [15/17] thereby has the general shape illustrated in FIG. 11” which exhibits “[t]he major advantage” of a “*high-low implant profile*.” Ex.1005, 2:38-41, 5:14-17, 5:56-57. Payne’s Figure

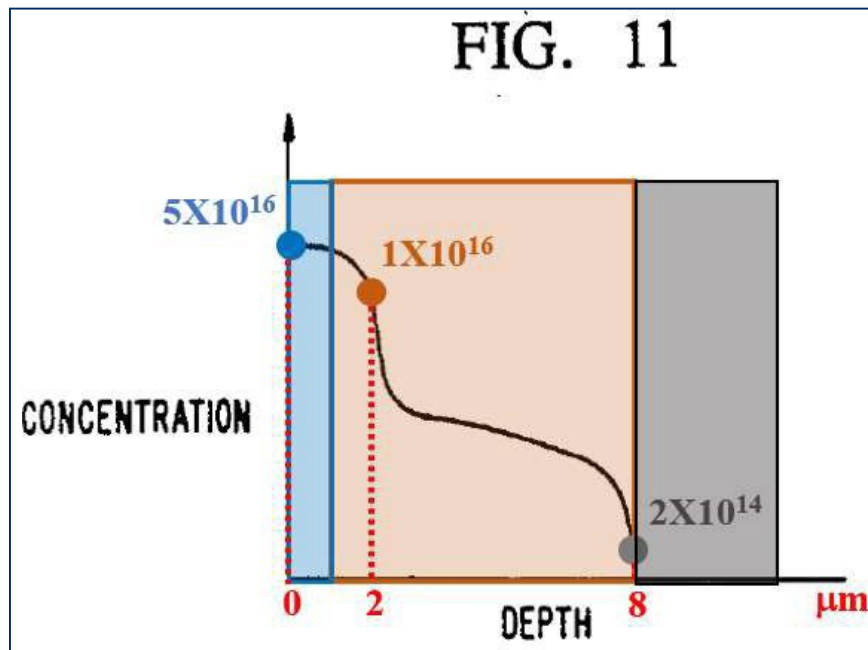
11 (below right) illustrates the dopant concentration measured along the red dotted line in Figure 10 (below left), which starts at the bottom of the surface layer (blue) and extends to the substrate (grey). As shown below, Payne discloses a downward-sloping graded-dopant concentration in the SDL (tan) associated with Payne's PMOS transistor (left).⁶



Ex.1005, FIGS. 10-11. Dr. Banerjee has annotated Figure 11 to reflect exemplary (maximum) dopant concentrations at various depths disclosed in Payne: (1) 5×10^{16} ions/cm³ at the surface of the shallow wells (depth 0 μ m), (2) 10^{16} ions/cm³ at a depth of ~ 2 μ m (boundary of deep and shallow wells), and (3) 2×10^{14} ions/cm³ at a depth of ~ 8 μ m (boundary of substrate and deep wells). Ex.1003,

⁶ Cf. *Kingsford Prod. Co., LLC v. Creative Spark, LLC*, No. IPR2016-01831, Paper 32 at 32 (P.T.A.B. Mar. 9, 2018) (“Figures that are not drawn to scale may be relied upon to disclose *qualitative relationships* between measured quantities ...”).

¶¶91-92.

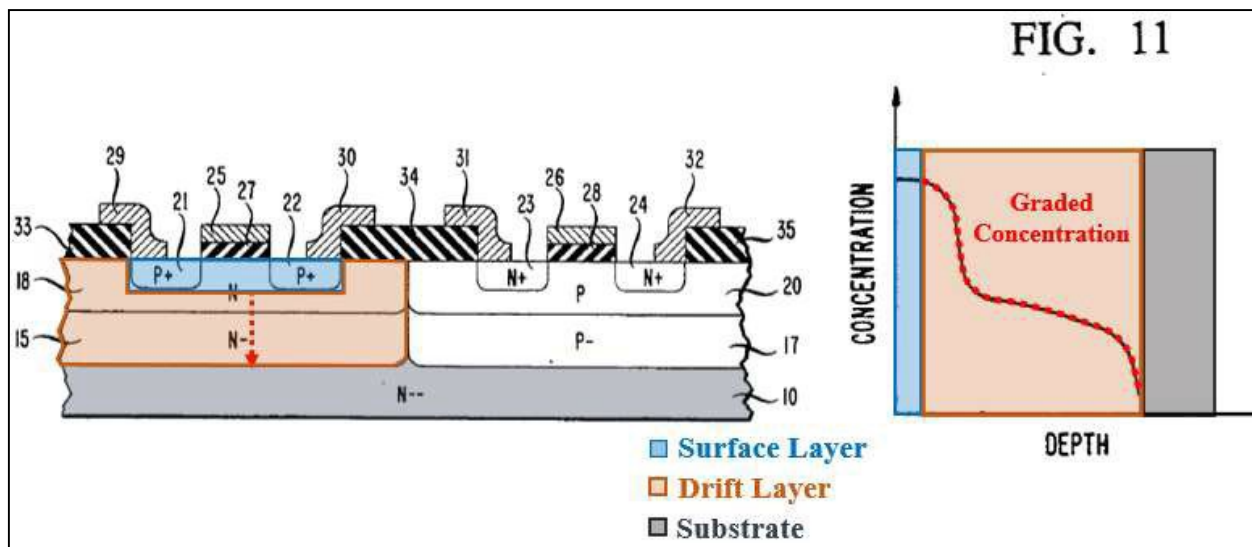


Ex.1005, FIG. 11. Indeed, Payne explains that “[t]he surface impurity concentration of the surface regions [18/20] is typically $0.5\text{-}5 \times 10^{16}$ ions/cm³ and that [the surface impurity concentration] of the tub regions [15/17] is typically $10^{15}\text{-}10^{16}$ ions/cm³, with the former concentration being *at least twice as much* as the latter over these ranges.” *Id.*, 5:51-55. The concentration is lowest at the substrate, where it is “ $1\text{-}2 \times 10^{14}$ ions/cm³.” *Id.*, 2:56-59. Payne also explains that “the final depth of surface regions 18 and 20 would be approximately $1\text{-}2\mu$ and the depth of tub regions 15 and 17 would be typically $3\text{-}8\mu$.” *Id.*, 5:48-50.

While the above discusses the SDL associated with Payne’s PMOS transistor (left in Figure 10), Payne teaches that the SDL associated with Payne’s NMOS

transistor (right) also has a downward-sloping graded-dopant concentration. Ex.1005, 5:14-17; Ex.1003, ¶¶92-94.

First static unidirectional electric drift field to aid the movement of minority carriers - As shown below, Payne's SDL (tan) has a downward-sloping graded-dopant concentration extending between the surface layer (blue) and the substrate (grey). §IX.A.1.e.



Ex.1005, FIGS. 10-11.

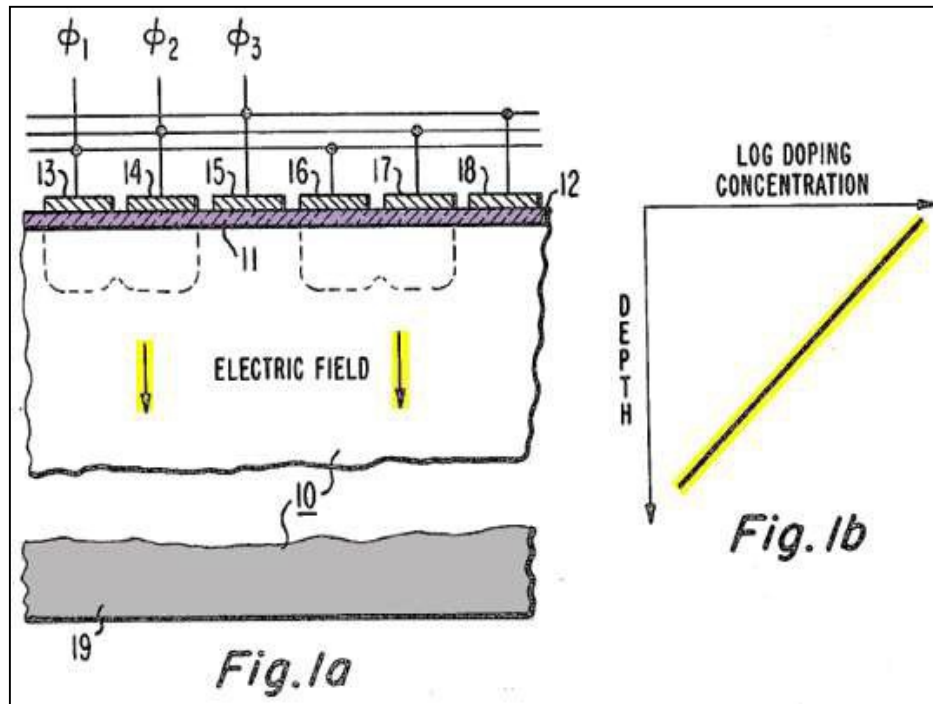
Payne's downward-sloping graded-dopant concentration aids the movement of minority carriers from the surface layer to the substrate to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. Ex.1003, ¶¶95-99. During prosecution of the parent '195 Patent, Applicant represented to the Patent Office that a downward-sloping graded-dopant concentration was known in the prior art to

create an “inherent ‘built- in’ unidirectional electric field” that moves carriers deep into the substrate (while an upward-sloping concentration, not at issue in Payne, would move those carriers in the opposite direction towards the surface):

[T]he graded dopant concentration itself creates a ‘***built-in’ electrical field*** that forces the movement of carriers into a particular direction, whereby ***the ‘direction’ of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.***

Ex.1046, 289-290 (underlining in original); Ex.1003, ¶¶95-96. Applicant further represented that “a unidirectional drift (electric) field necessarily affects ***all*** the present ***minority*** carriers in the same way.... Depending on the particular slope of the graded concentration of dopant, ***all minority*** carriers are either ***swept*** ‘down’ ... or ‘up ...’” Ex.1046, 289. Applicant cited Jastrzebski in support. *Id.*, 290. In Jastrzebski, the graded-dopant concentration is “decreasing with depth” from the top surface 11 (purple) of the substrate 10, as shown in Figure 1b below. Ex.1010, 5:14-22. Jastrzebski teaches that this downward-sloping graded-dopant concentration creates an electric drift field that “force[s] most of the charge carriers ... ***deep into the substrate[.]***” *Id.*, 5:14-22; *id.*, 2:27-32 (“This is done by creating a field, such as a drift field, in the semiconductor substrate to ***sweep minority charge carriers ... into the bulk [substrate], away from the electrode-bearing surface of the***

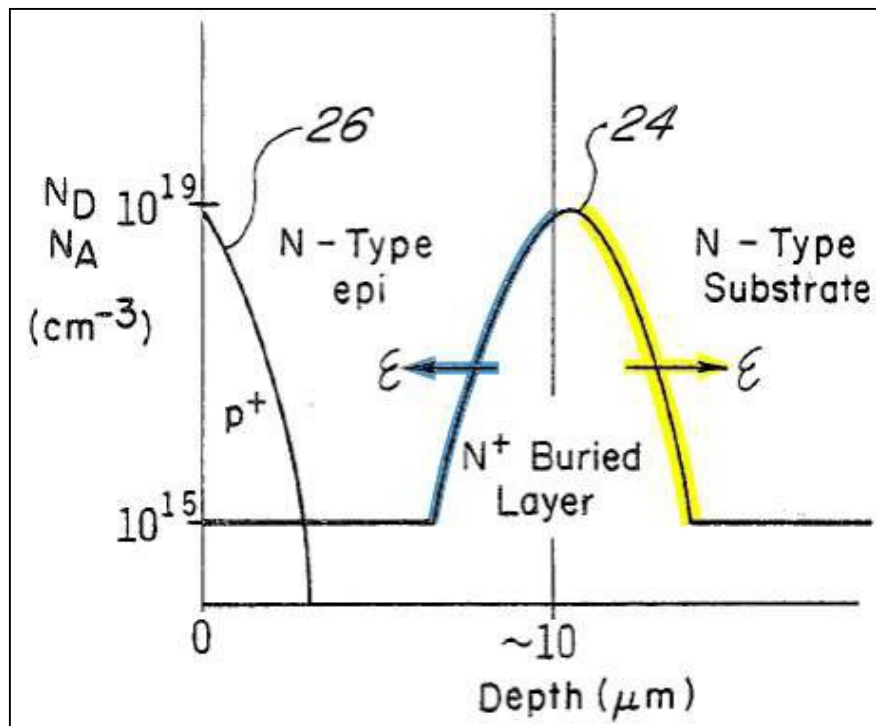
substrate.”).



Ex.1010, FIGS. 1a-1b.

Applicant made the same representation to the Patent Office regarding Kamins. Ex.1046, 237-238, 253-254. According to Applicant, Kamins' Figure 3 shows "two electrical fields with opposing directions" (highlighted in blue and yellow) that correspond to increasing and decreasing graded-dopant concentrations, respectively. *Id.*, 237, 253 (citing Ex.1009, 3:6-13, FIGS. 2-3). Applicant explained that Kamins "show[s] *minority carrier[s] accelerated into the substrate.*" *Id.*, (citing Ex.1009, FIG. 2 and quoting Ex.1009, 3:6-13 ("carriers ... accelerated ... *away from the surface ... into the substrate*")). According to Applicant, the electric field associated with the downward-sloping graded concentration at depth beyond $\sim 10\mu\text{m}$

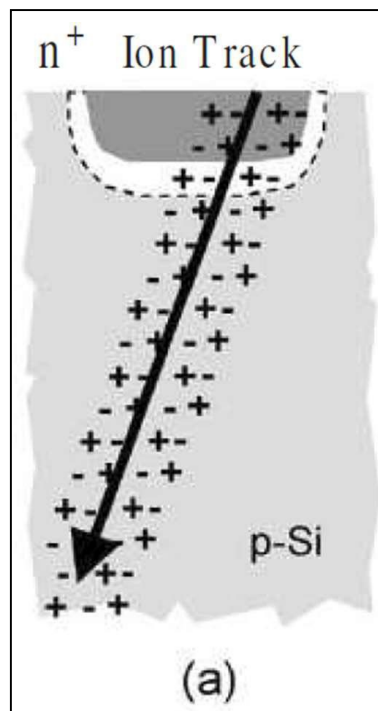
(red) causes “[minority] carriers created [in that region to be] ... **accelerated into the substrate**” *Id.* (citing Ex.1009, 3:6-13, FIGS. 2-3); Ex.1030 at 24 (Kamin’s “bottom electric field [(yellow)] draws a **minority carrier** from the substrate to a **deeper** part of the substrate.”); Ex.1009, 2:67-3:14 (“The non-uniform dopant concentration in the substrate creates electric fields in the substrate indicated by arrows labeled ‘ ϵ ’ in FIGS. 2 and 3” such that “[minority] carriers created below the maximum dopant concentration are accelerated into the substrate.”), FIG. 2 (referring to these carriers as “photogenerated minority carriers”), 2:11-16 (same).



Ex.1009, FIG. 3.

Dr. Banerjee explains that during a so-called single event upset (SEU), an α -ray generates millions of carriers, some of which are produced in or near the active

regions at the surface of the substrate. Ex.1003, ¶100; Ex.1013, 431 (“A[n] α -particle can induce SEU when it strikes at the **channel region** of an off NMOS transistor or the **drain region** of an off PMOS transistor.”), FIG. 2. As shown in Figure 2, such event generates both types of carriers (holes, denoted “+” and electrons, denoted “-”), one of which will be the minority carrier in any given surface layer. Ex.1003, ¶¶100-101.



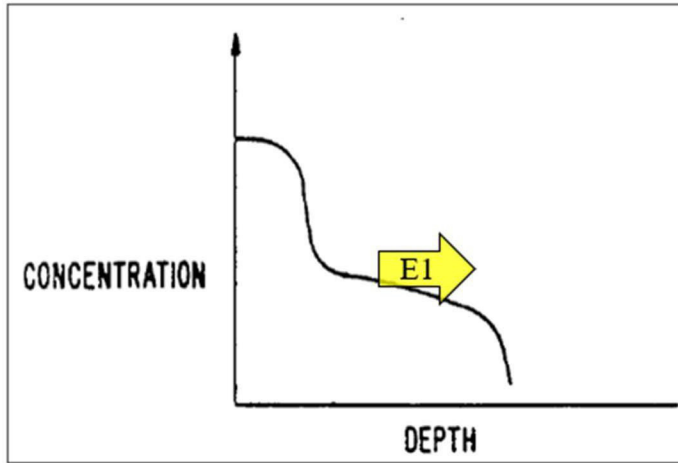
Ex.1013, FIG. 2(a).

Like Jastrzebski and the right-hand side of Kamins Figure 3 (yellow), Payne’s graded-dopant concentration is downward-sloping, as shown in Figure 11. Moreover, this graded-dopant profile is determined by the ion-implantation and drive-in steps of the chip fabrication processes (described in Payne in relation to

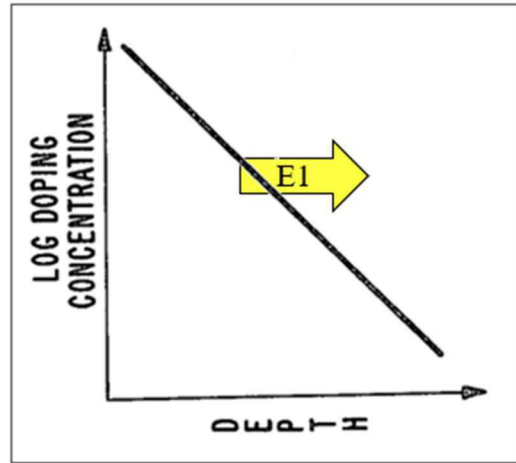
Figures 2 and 5-9 in particular) and thus the profile (and any resulting electric field) is static—it is set once the device has been fabricated and does not change. Ex.1003, ¶102; Ex.1005, 5:7-17, 5:44-55 (describing “the *final* depth” of tubs and surface regions and their typical ranges of impurity concentrations). During prosecution of the parent ’195 Patent, Applicant described “static” similarly, conceding that “Kamins (US 4,160,985), just like Applicant, discloses the presence of a ‘static’ drift field, ‘because the drift field is created by graded concentration of dopants which does not change over time.’” Ex.1046, 318 (citing Ex.1009, 2:15-16, 2:64-3:2, 1:38-46, 3:8-11 and Ex.1046, 302-03), 333 (same).

Thus, according to Jastrzebski, Kamins, Applicant, and PO, Payne’s profile generates a (first) “built-in” static unidirectional electric drift field (illustrated by the yellow arrow labelled “E1” below left) that aids the movement of minority carriers from the surface layer to the substrate.⁷ Ex.1003, ¶¶104-106.

⁷ The Ground I figures depict electric fields in N-wells, *e.g.*, Payne’s nested N-wells 15/18. §§IX.A.1.f-g. The electric fields would be pointing in the opposite direction in Payne’s nested P-wells. In both cases, these electric fields result from the downward-sloping graded dopant concentrations in Payne’s N-wells and P-wells and aid the movement of minority carriers (holes in N-wells, electrons in P-wells) downward to the substrate. *Id.*; Ex.1003, ¶¶105-106.

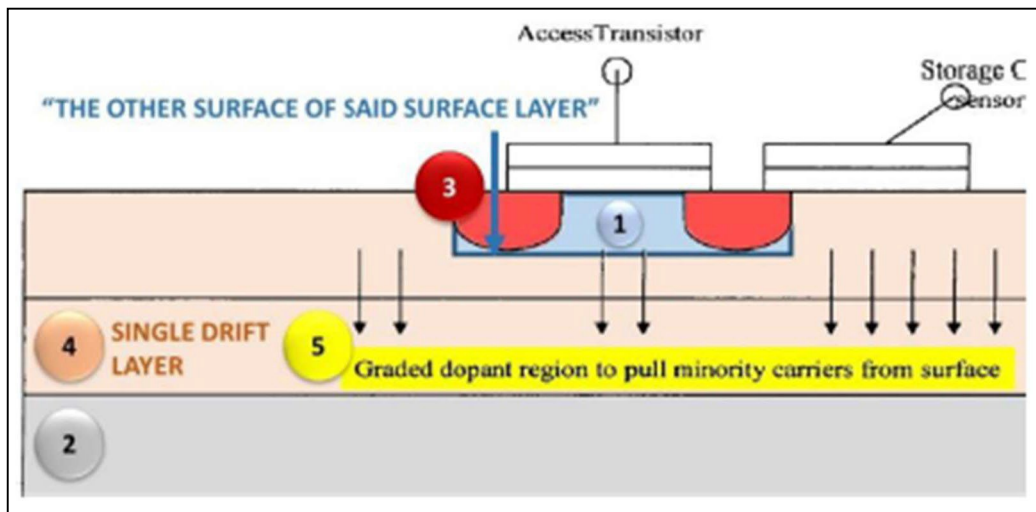


Ex.1005, FIG. 11



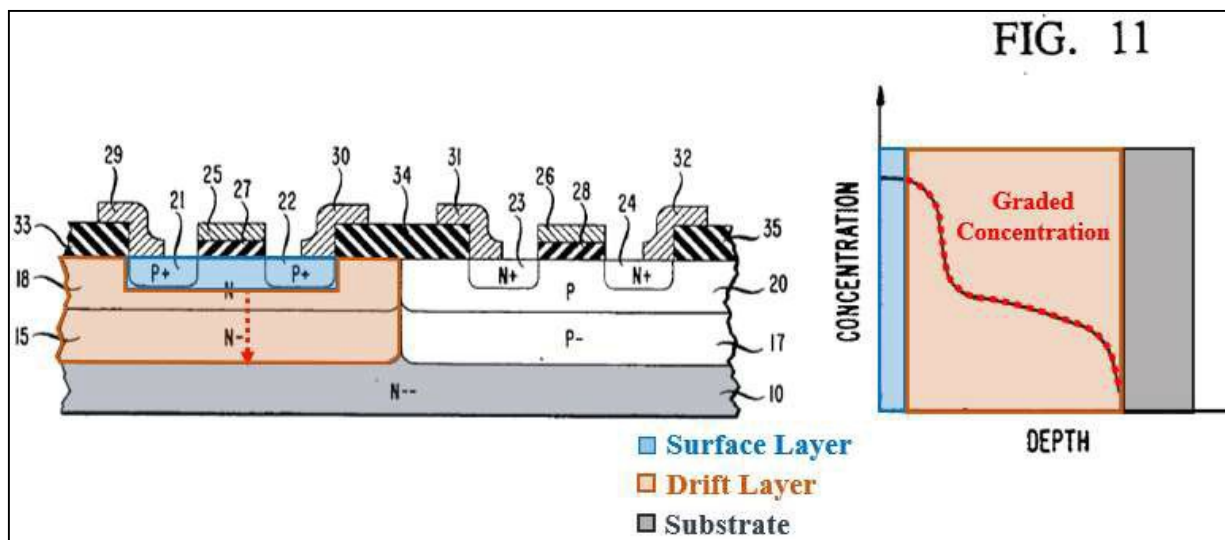
Ex.1010, FIG. 1b

Notably, Payne satisfies element [7.5] to the same extent the '502 Patent's Figure 5(b) meets it. Ex.1003, ¶107. While the '502 Patent does not disclose any SDL's dopant profile, PO contends that annotated Figure 5(b) below shows that “[t]he single drift layer has a graded concentration of dopants ... [that] create[s] an electric field that aids the movement of minority carriers [] from the surface layer to the substrate.” Ex.1030, 7.



Ex.1001, FIG. 5(b); Ex.1030, 7.

In light of the above, Payne satisfies element [7.5] under PO's plain-meaning constructions. Ex.1033. Payne's Figure 11 shows a graded- dopant concentration that is downward-sloping over the entire SDL (tan)—in fact, from the top of the silicon/surface layer (blue) to the bottom of the SDL—and thus, according to PO (and Applicant's representations to the Patent Office discussed above), this graded- dopant concentration creates a static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. Ex.1005, FIG. 11; Ex.1003, ¶108.

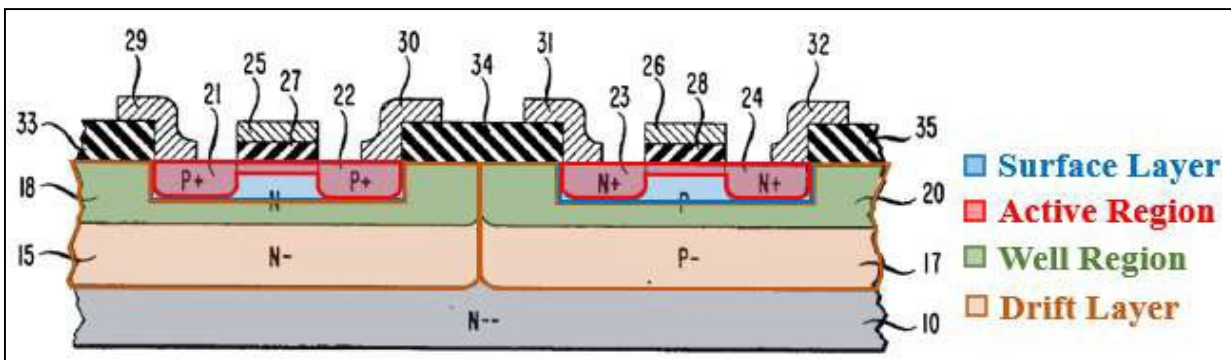


Ex.1005, FIGS. 10-11.

- g. **Element [7.6]: “at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.”**

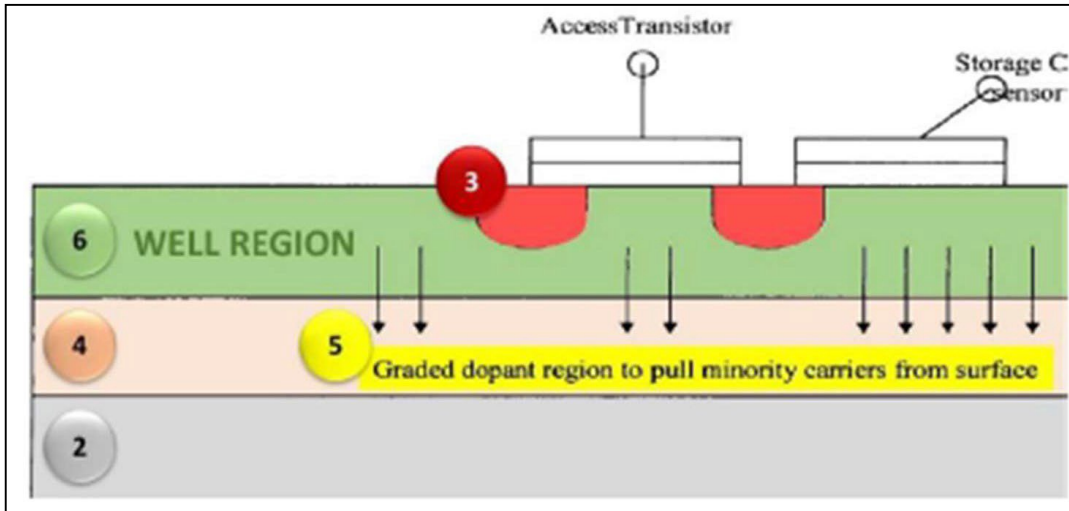
Payne discloses or, at a minimum, renders obvious this element. Ex.1003, ¶¶109-119.

Well region disposed in said single drift layer ... having a graded concentration of dopants – As detailed above in §§IX.A.1.e-f regarding elements [7.4] and [7.5], Payne’s “tub region” 15 is an example of the claimed SDL. As shown below, Payne’s “**surface region**” 18 (**green**) disposed in tub region 15 (tan) is an example of a well region (a shallow well) disposed in Payne’s SDL (tub). Ex.1005, 1:65-68, 4:31-39, 5:7-14, 5:44-55. Payne’s **surface region 20 (green)** is another well region disposed in an SDL (tub 17). *Id.*, 1:65-68, 4:63-5:14, 5:44-55; Ex.1003, ¶¶110-111; §IX.B.1.e.



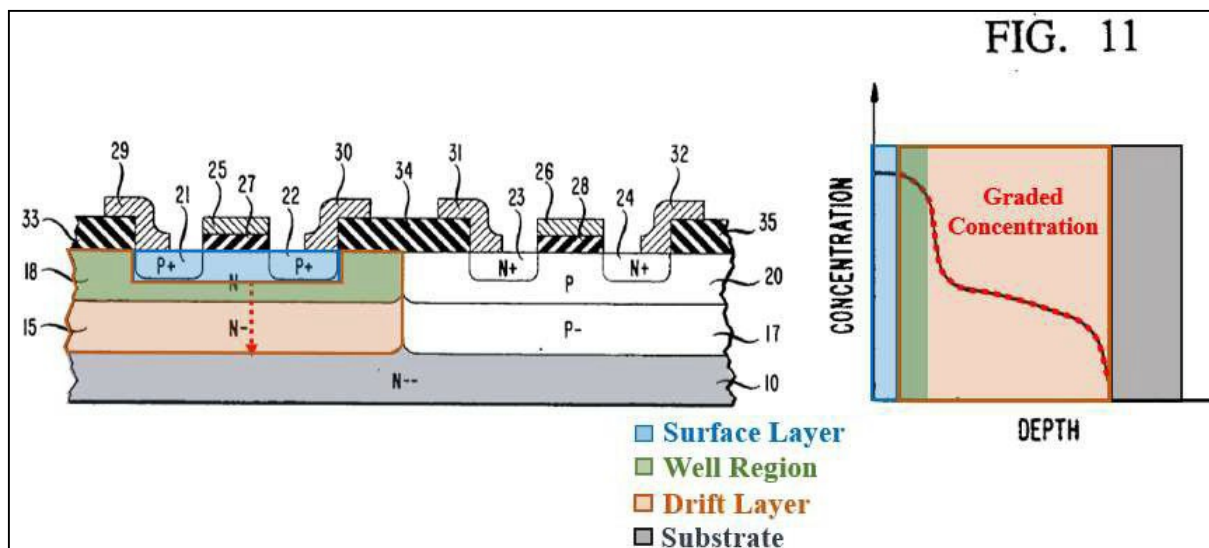
Ex.1005, FIG. 10.

Notably, Payne satisfies element [7.6] to the same extent that Figure 5(b) of the '502 Patent, annotated by PO (as shown below), meets it:

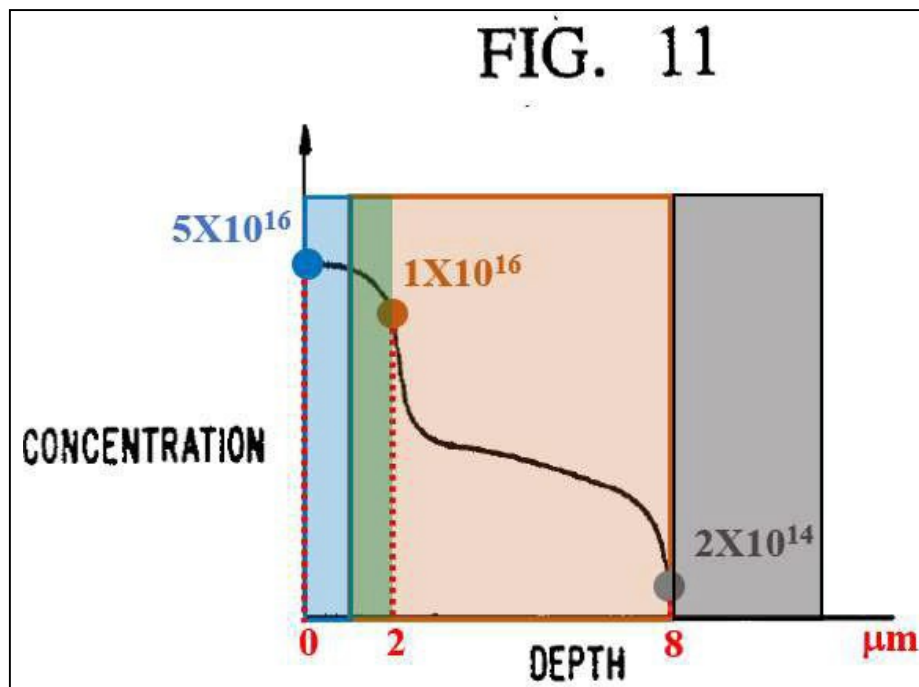


Ex.1001, FIG. 5(b); Ex.1030, 7.

As detailed above with respect to element [7.5], Payne’s Figure 11 (below right) illustrates the dopant concentration measured along the red dotted line in Figure 10 (below left). As shown, Payne’s well region (“surface region 18”) (green)—disposed in the SDL (tub 15) (tan border)—has a graded-dopant concentration that is downward-sloping with increasing depth. Ex.1003, ¶¶112-114; §IX.A.1.e.

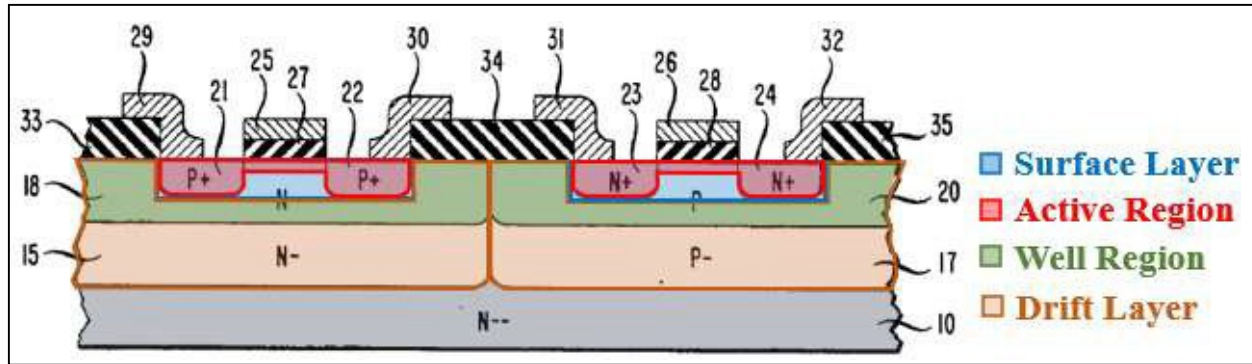


Ex.1005, FIGS. 10-11. As discussed in §IX.A.1.e, Payne discloses that Figure 11 illustrates a “*high-low implant profile*” that is downward-sloping with depth, such as from 5×10^{16} ions/cm³ (near the top surface of the silicon/surface layer (blue)) to 1×10^{16} ions/cm³ near the bottom of well 18 (green), to 2×10^{14} ions/cm³ near the bottom of the single drift layer (tub 15) (tan). *Id.*, 2:56-59, 5:48-57; Ex.1003, ¶¶112- 114.



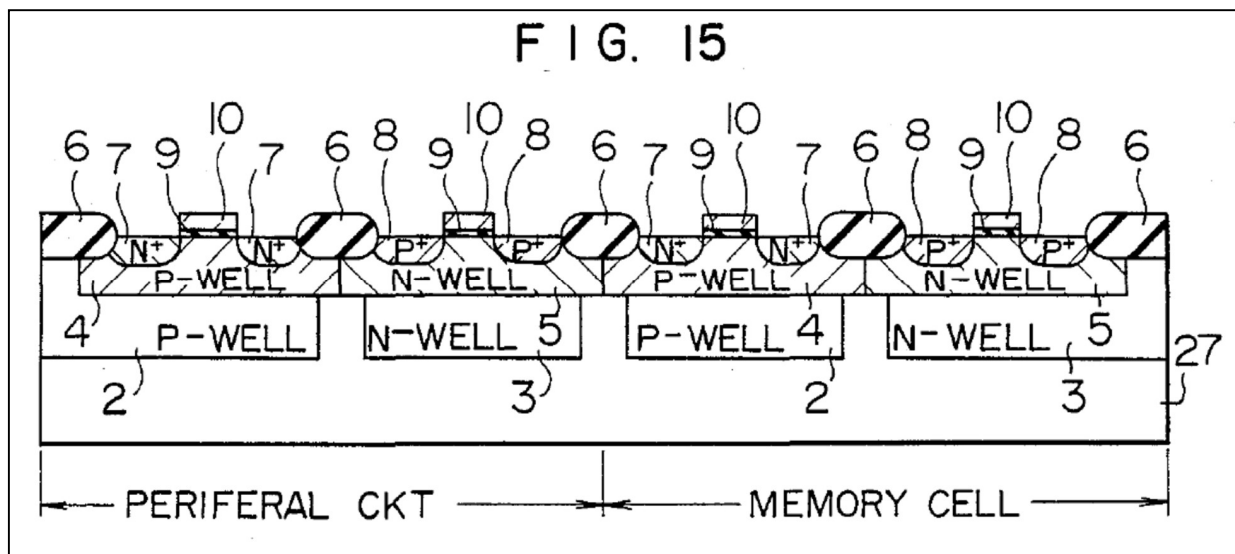
Ex.1005, FIG. 11.

In light of the above, Payne satisfies element [7.6] under PO’s construction that the term “well region” should be accorded plain meaning and is “a doped region that surrounds the active region of a semiconductor device.” Ex.1033. As shown in Figure 10 below, the well region (green) is a doped region that surrounds the surface layer (blue) and the active region (red) therein. Ex.1003, ¶114.



Ex.1005, FIG. 10.

In addition, Sakai teaches a nested structure similar to Payne, which Sakai refers to as “twin double well.” *See, e.g.,* Ex.1006, 7:19-37 (“The memory of FIG. 15 has a *twin double well* structure ... made up of the *deep* P-well region 2, the *deep* N-well region 3, the *shallow* P-well region 4 and the *shallow* N-well region 5”).

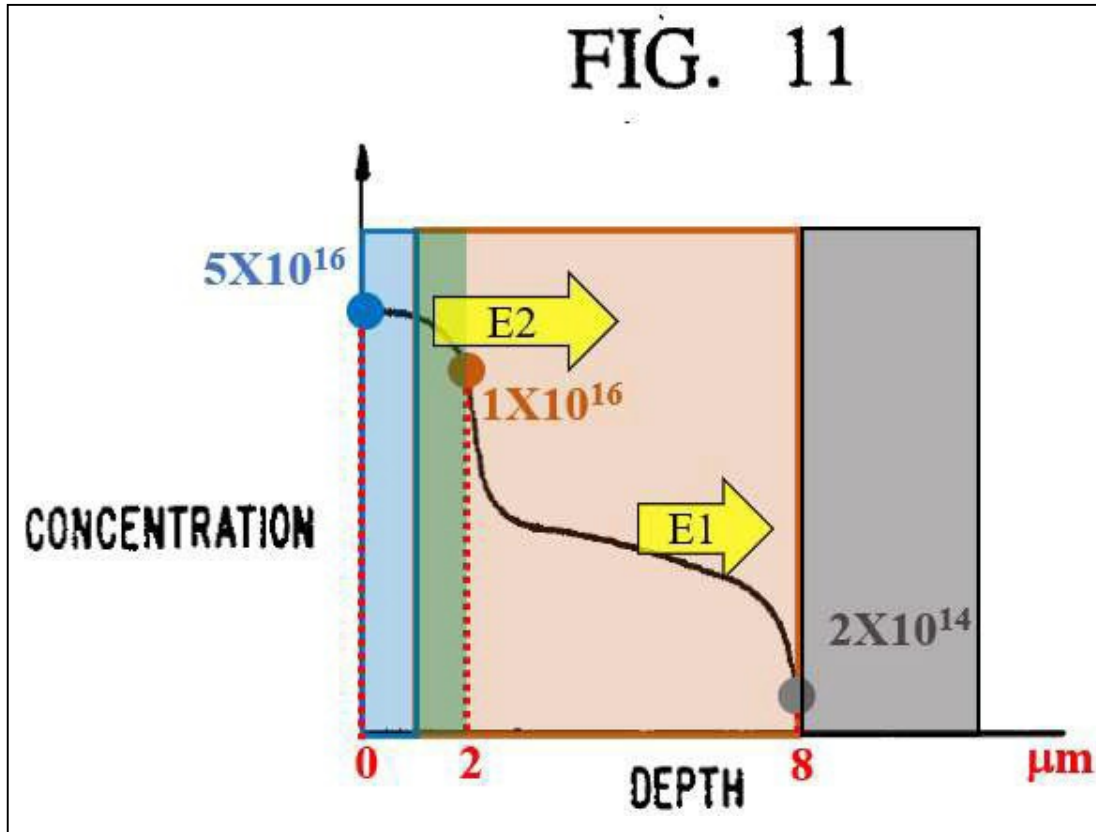


Ex.1006, FIG. 15; 1:57-67, 5:56-6:4, FIG. 10B, FIGS. 3, 8-9, 11E. Sakai confirms that Payne’s “surface region” is a shallow well region. Ex.1003, ¶115.

Second static unidirectional electric drift field to aid the movement of

minority carriers – According to §IX.A.1.f—including Applicant’s repeated representations during prosecution of the parent ’195 Patent, Jastrzebski and Kamins relied on by Applicant during the prosecution, and PO’s statements in its claim construction brief—the downward-sloping graded-dopant concentration in the well region creates a (second) static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. Ex.1003, ¶116; §IX.A.1.f. Further, Payne’s graded-dopant profile, including the profile in the well region, is set once the device has been fabricated and does not change, making the profile (and any resulting electric field) static, as described in §IX.A.1.f.

Payne’s Figure 11 is further annotated below to show the exemplary first static unidirectional electric drift field (“E1”) present in a deep portion of the SDL (discussed in §IX.A.1.f), and a different, exemplary second static unidirectional electric drift field (“E2”) present in the well region disposed in the SDL. Ex.1003, ¶¶117-118; *see also* n.8.



Ex.1005, FIG. 11. Moreover, E1 and E2 are illustrated as electric fields having different magnitudes, to reflect the different local slopes (gradients) of the graded- dopant profile. Ex.1003, ¶¶118-119; Ex.1022, [0071] (“the vertical ϵ -field is established by the rate of change in the graded dopant concentration, i.e., the greater the rate of change ... the greater the intensity of the ϵ -field.”).

In light of the above, Payne satisfies element [7.6] under PO’s plain-meaning construction of “to aid the movement of minority carriers”. Ex.1033; Ex.1003, ¶119. Payne’s Figure 11 shows that the dopant concentration is downward- sloping with increasing depth over the entire well region, and thus, according to PO (and also in light of Applicant’s representations to the Patent Office, discussed in §IX.A.1.f),

creates a static unidirectional electric drift field that aids the movement of minority carriers downward from the surface layer to the substrate. Ex.1030, 2, 29; Ex.1003, ¶119.

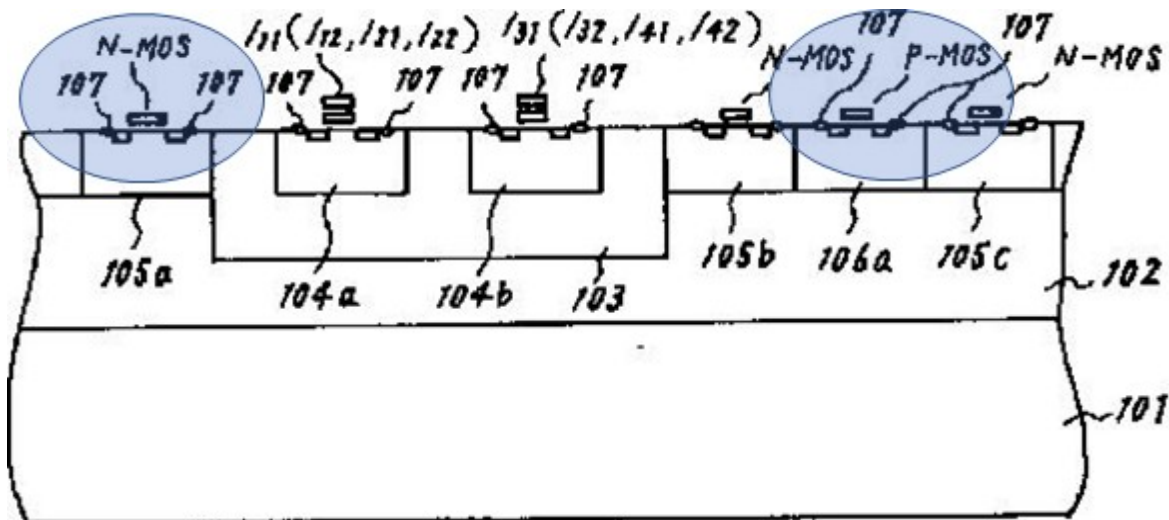
B. Grounds II-III

Onoda anticipates or else renders claims 7, 8 and 11 obvious. Ex.1003, ¶¶120-176.

1. Independent Claim 7

a. Preamble: “A semiconductor device comprising:”

Onoda discloses a semiconductor device. Onoda discloses a flash memory device formed atop a semiconductor substrate 100 that includes N-channel MOS (NMOS) transistors and P-channel MOS (PMOS) transistors its peripheral circuitry. Ex.1042, [0041], [0044]-[0045], [0052], FIG. 3, claim 2; Ex.1003, ¶¶121-122.

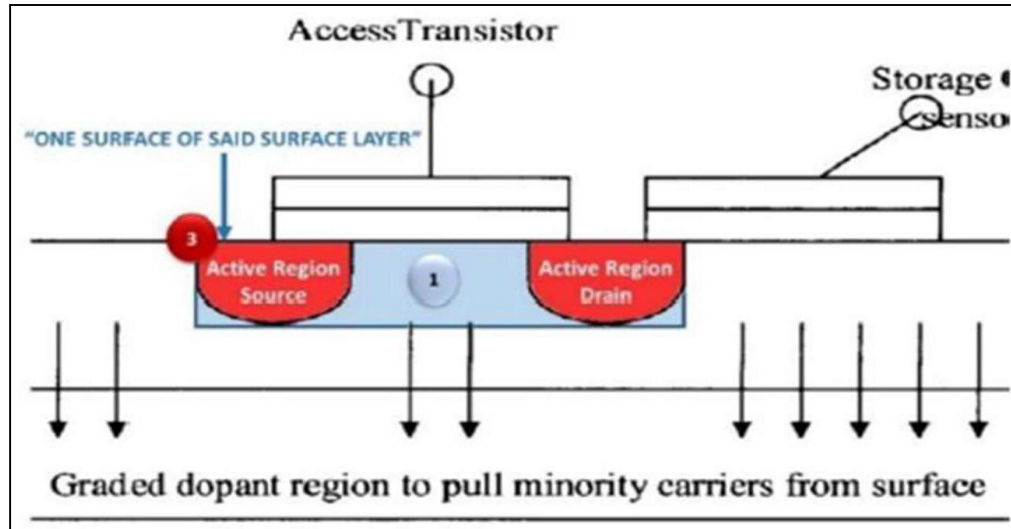


Ex.1042, FIG. 3. Onoda mentions that one of the objectives of the invention

“is to provide a semiconductor integrated device . . .” Ex.1042, [0006].

b. Element [7.1]: “a surface layer;”

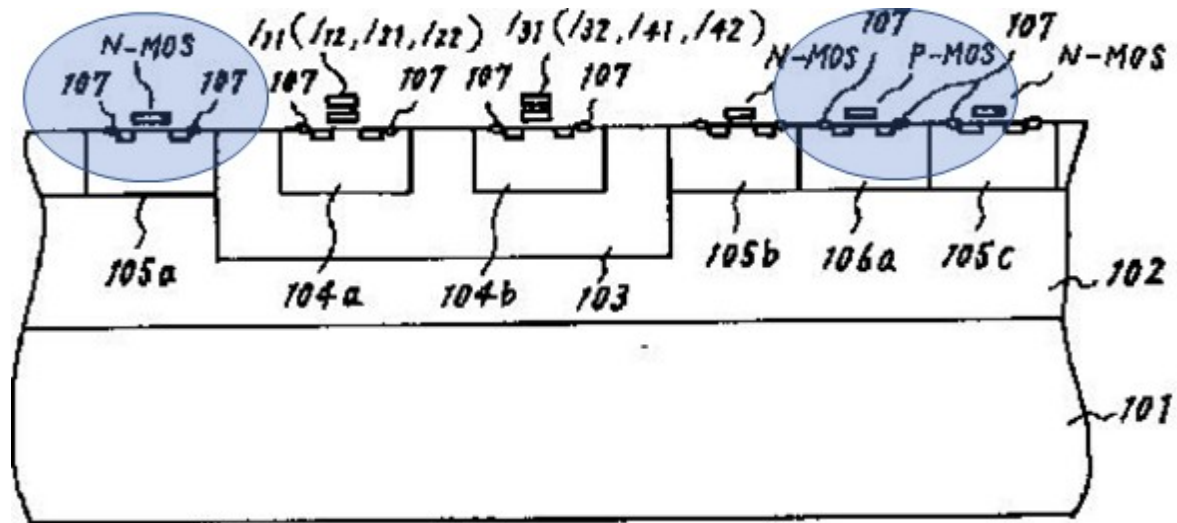
Onoda discloses or else renders obvious this element. Ex.1003, ¶¶123-128. According to PO, a “surface layer” is “a layer at the surface of the silicon” (or “a layer at the surface of the semiconductor device”)—which PO annotated in blue in Figure 5(b) of the ’502 Patent below—“where the active region [(red)] is located.” Ex.1030, 6, 9, 12, 13; Ex.1033; §IX.A.1.b.



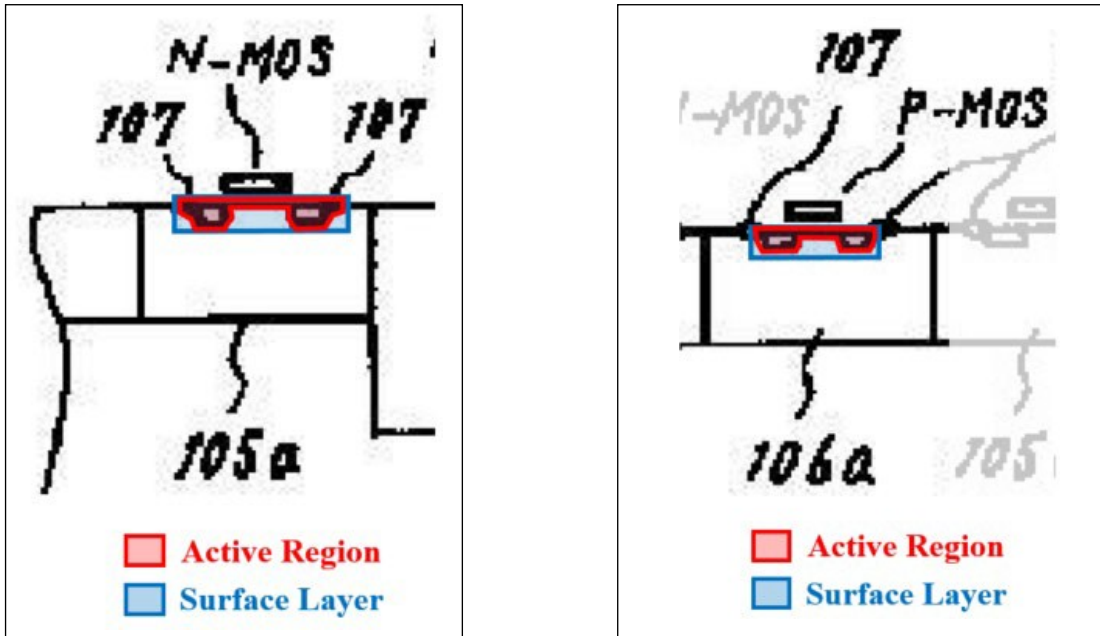
Ex.1001, FIG. 5(b); Ex.1030, 7, 12.

Onoda satisfies element [7.1] to the same extent that Figure 5(b) of the ’502 Patent meets it. Ex.1003, ¶¶124-125. Onoda’s Figure 3 depicts how the flash memory is formed on the semiconductor substrate 100. Ex.1042, [0043]. Onoda likewise discloses at least one N-channel MOS transistor (labeled N-MOS in Figure 3) and at least one P-channel MOS transistor (labeled P-MOS in Figure 3). Ex.1042,

FIG. 3, [0055], [0044].



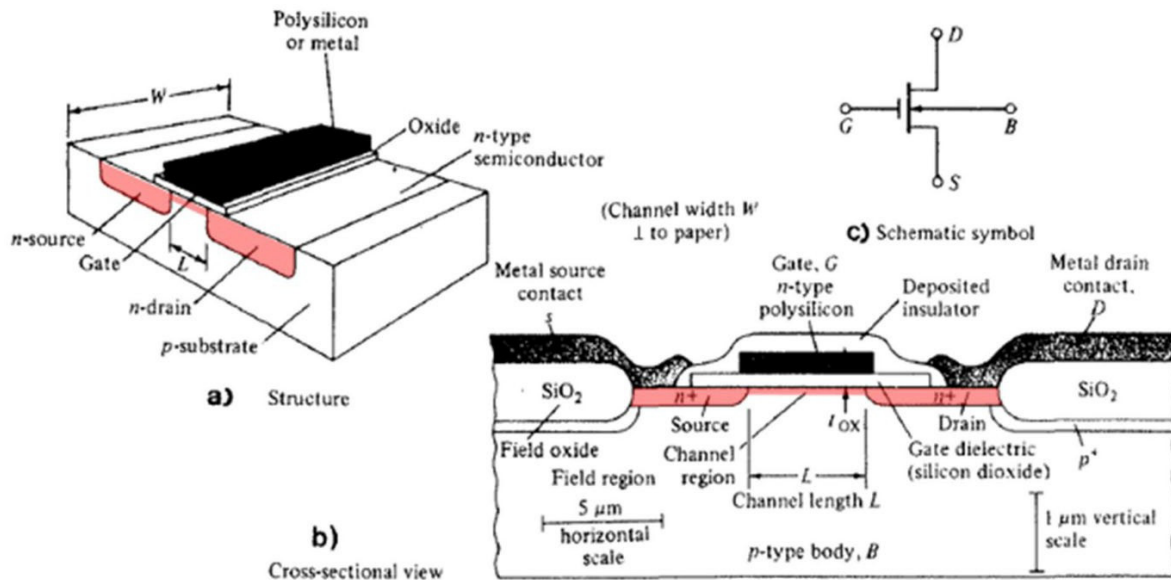
Ex.1042, FIG. 3. As indicated below, Onoda's surface layer (blue) is at the surface of semiconductor substrate 100, and the source and drain regions (red) of Onoda's NMOS and PMOS transistors are located in that surface layer. Ex.1003, ¶¶124- 125.



NMOS Active Regions/Surface Layer PMOS Active Regions/Surface Layer

Ex.1042, FIG. 3 (excerpts of NMOS (left) and of PMOS (right)).

Likewise, Wolf teaches that a MOS transistor consists of a source, a drain and a channel regions between the two (collectively, red):

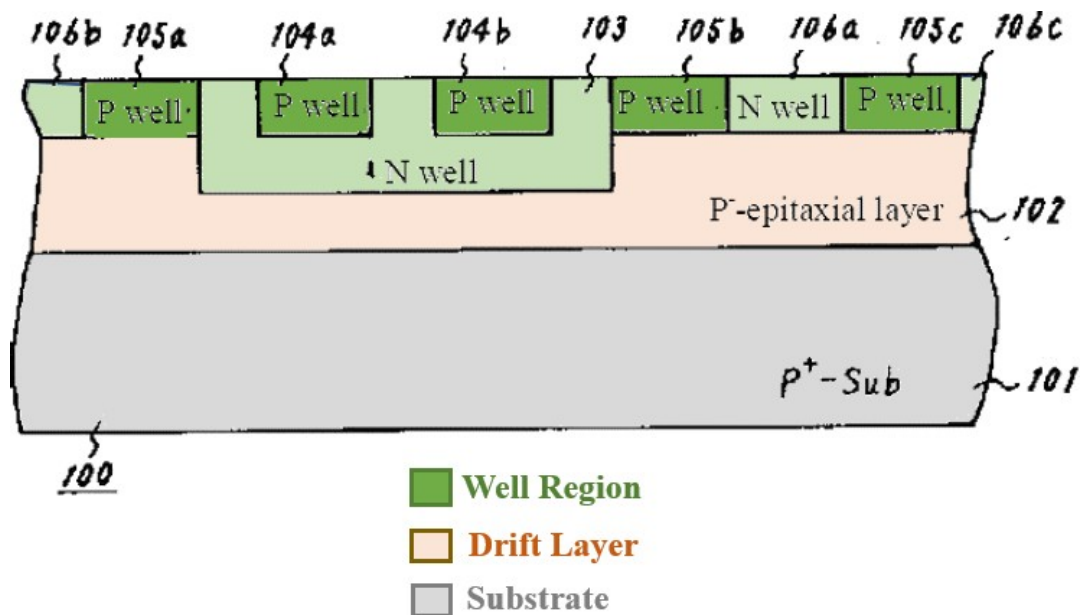


Ex.1008B, FIG. 5-1; *id.*, 298-301, 374, FIGS. 5-2, 6-4.

As a result, a POSITA would have understood that each of Onoda's NMOS transistors has a surface region (blue) that contains a source region, drain region, and a channel region positioned therebetween (collectively, red), which are formed in a P-type well region 104a, 104b, 105a, 105b, or 105c. Ex.1042, [0042], [0044], [0045], [0055], FIG. 3. Thus, Onoda discloses a surface layer (blue) that matches the surface layer Patent Owner identified in Figure 5(b) of the '502 patent. Likewise, a POSITA would have further understood that each of Onoda's PMOS transistors have a surface region (blue) that contains a source region, a drain region, and a channel region positioned therebetween (collectively, red), which are formed in an N-type well region 106a, 106b, or 106c. *Id.*, [0042], [0055], [0044]. Ex.1003, ¶¶125-128. Onoda further discloses that the memory cells are formed on the disclosed surface layer. Ex.1042, [0029], [0043]; Ex.1003, ¶¶125-128.

c. Element [7.2]: “a substrate;”

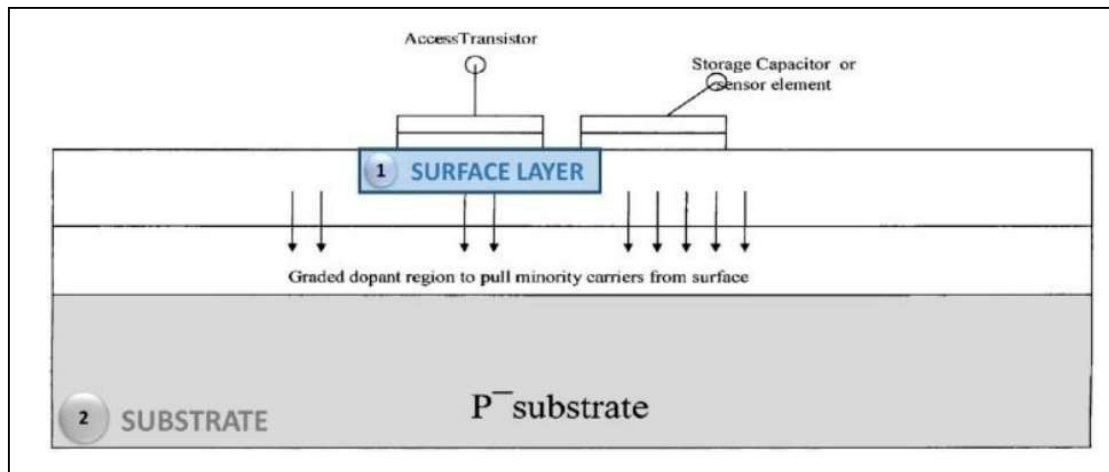
Onoda discloses “a semiconductor substrate 100” (grey below) in Figure 2 on which the flash memory is formed. Ex.1042, [0041]. “FIG. 2 depicts critical portions of the semiconductor *substrate* that is applied to the first embodiment of the present invention . . .” *Id.* Within the semiconductor substrate 100, “101 is a first semiconductor layer made from a heavily-doped (for example, about $1 \times 10^{19}/\text{cm}^3$) P-type silicon *substrate*” *Id.*; Ex.1003, ¶129.



Ex.1042, FIG 2,⁸ [0046], [0047], FIGS. 3, 4.

Onoda satisfies element [7.2] under PO's proposed construction of "plain and ordinary meaning [*i.e.*] 'an underlying layer.'" §VIII; Ex.1033. Onoda's substrate also matches PO's identification of substrate (grey) in Figure 5(b) of the '502 Patent. Ex.1003, ¶130.

⁸ While the legend here labels "Well Region" in green, for clarity, the light green regions indicate N-Well regions whereas dark green regions indicate P-Well regions.

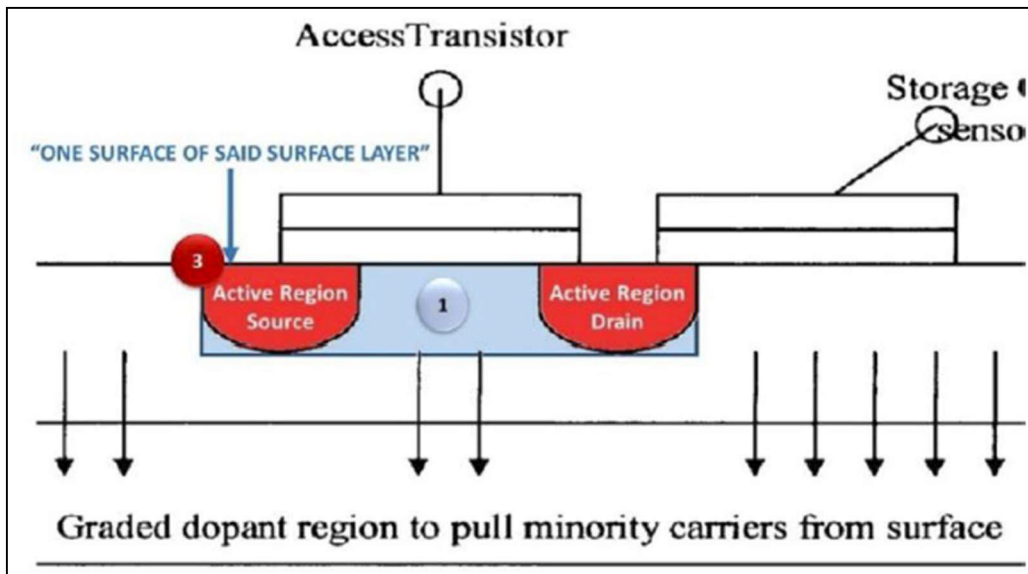


Ex.1030, 6-7, 16-17 (well region and drift layer can be part of substrate);

Ex.1001, FIG. 5(b).

- d. Element [7.3]: “an active region including a source and a drain, disposed on one surface of said surface layer;”**

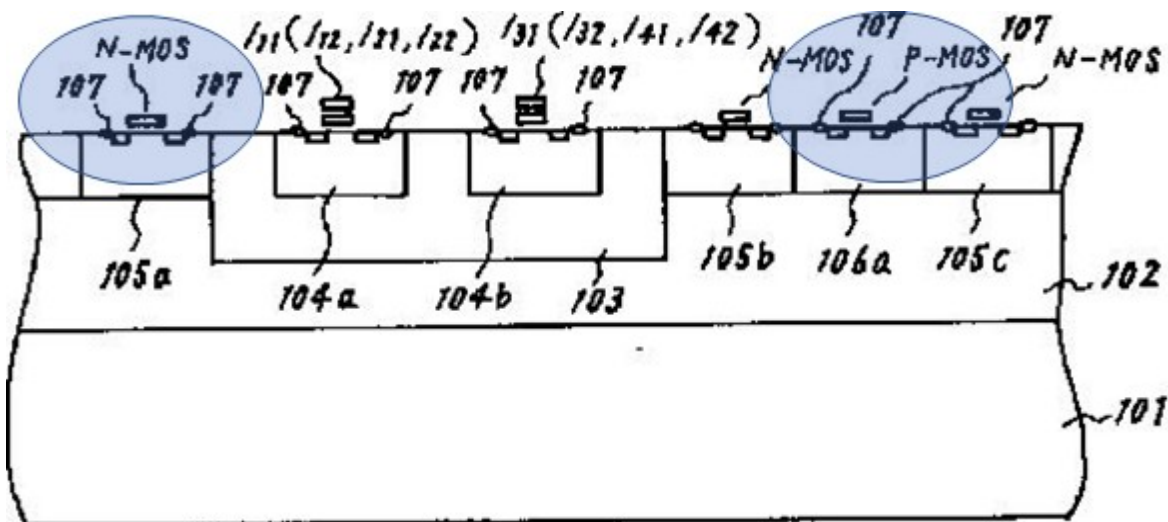
Onoda discloses or else renders obvious this element. Ex.1003, ¶¶131-135. As described in Section IX.A.1.d, according to PO, Figure 5(b) of the '502 Patent depicts an active region (red) “disposed on one surface [(top surface)] of said surface layer.”



Ex.1001, FIG. 5(b); Ex.1030, 6-7, 10-12; §IX.A.1.d.

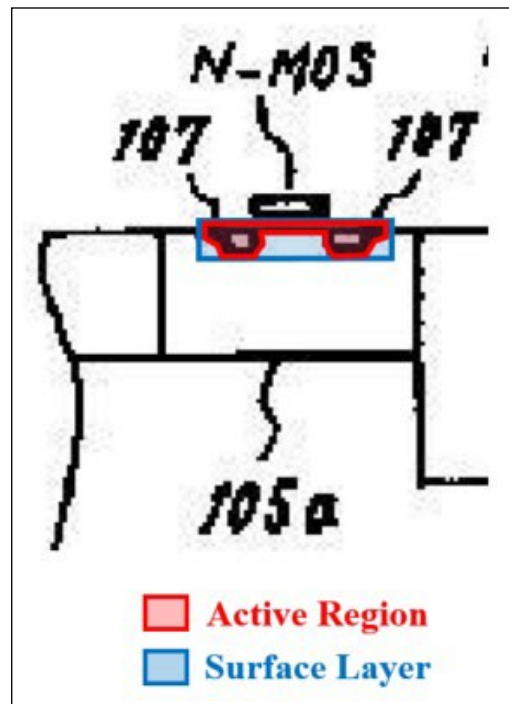
Onoda satisfies element [7.3] under PO's interpretation. Ex.1003, ¶¶132-133.

As shown below, Figure 3 from Onoda illustrates an NMOS transistor (left) with source/drain regions in a doped P-well 105a, and a PMOS transistor (right) with source/drain regions in a doped N-well 106a. Ex.1042, FIG. 3, [0042], [0055], [0044]; §IX.B.1.b.



Ex.1042, FIG. 3.

As indicated below, a POSITA would have understood that the active region (red) of each of Onoda's transistors is disposed on one surface (top surface) of a corresponding surface layer (blue), exactly as depicted in Patent Owner's annotated Figure 5(b) above. Section IX.B.1.b.

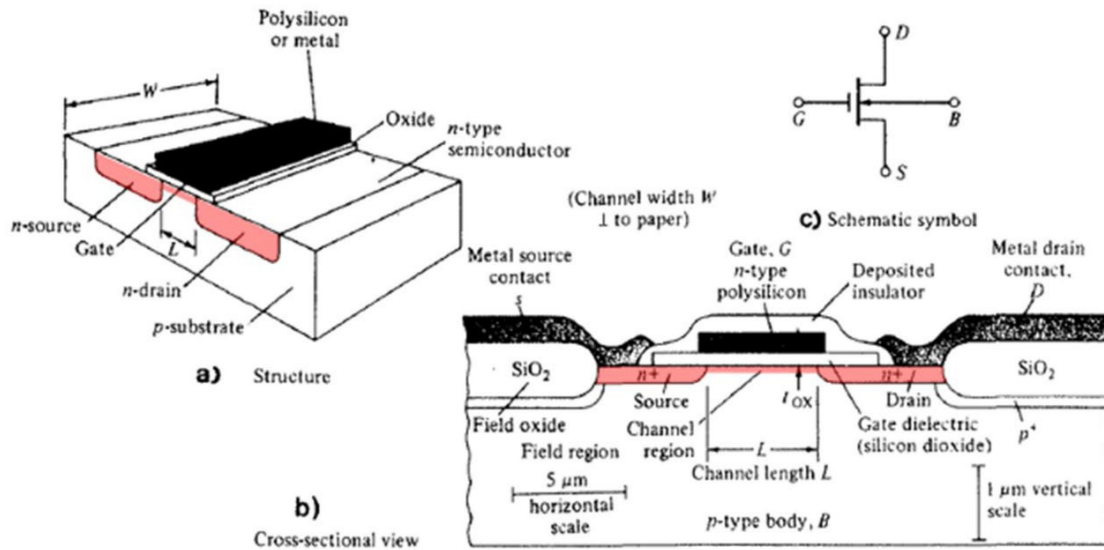


Ex.1042, FIG. 3 (excerpted).

Onoda satisfies element [7.3] under Patent Owner's position that the term "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed" (§IX.B and Ex.1033) because the active region of a MOS transistor is "[its] channel and [its] heavily doped source and drain regions," indicated in red

below, which is consistent with how Petitioner maps Onoda's active regions.

Ex.1008B, 299; Ex.1003, ¶135.

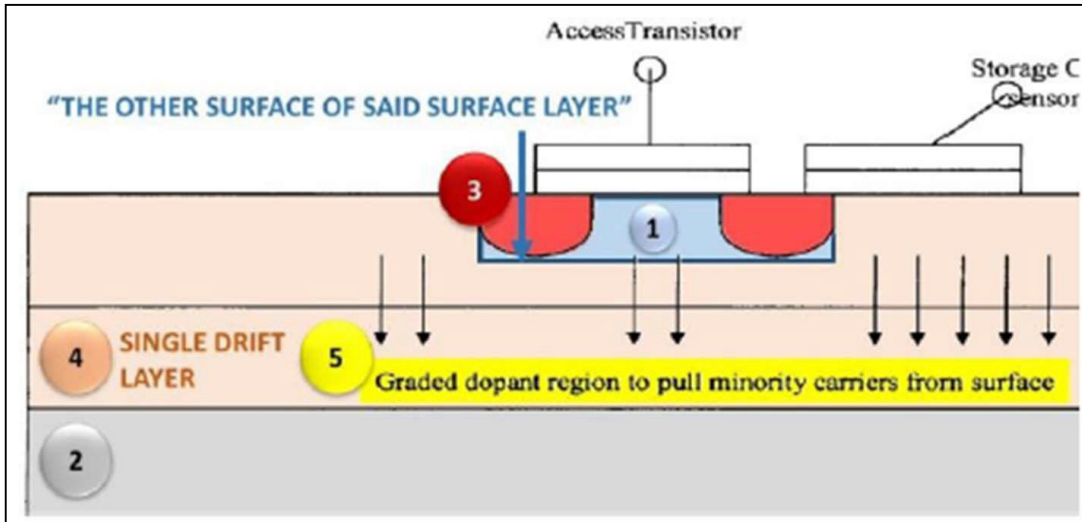


Ex.1008B, FIG. 5-1; *id.*, 298-301, 374, FIGS. 5-2, 6-4.

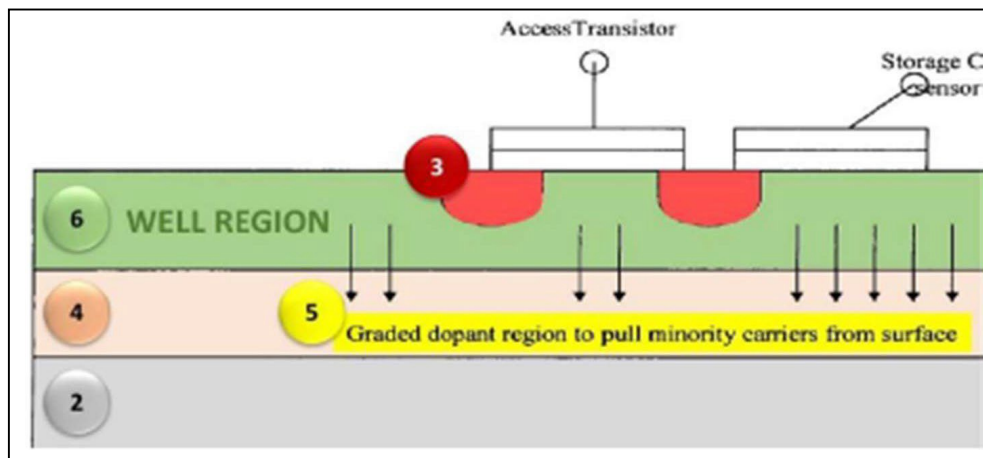
- e. **Element [7.4]: “a single drift layer disposed between the other surface of said surface layer and said substrate,”**

Onoda discloses this element. Ex.1003, ¶¶136-140.

Single drift layer (“SDL”) – As described in Section IX.A.1.e, according to PO, Figure 5(b) of the ’502 Patent depicts a single drift layer (tan) “disposed between ‘the other surface [(bottom surface)] of said surface layer [(blue)]’ and [said] substrate [(grey)]”:



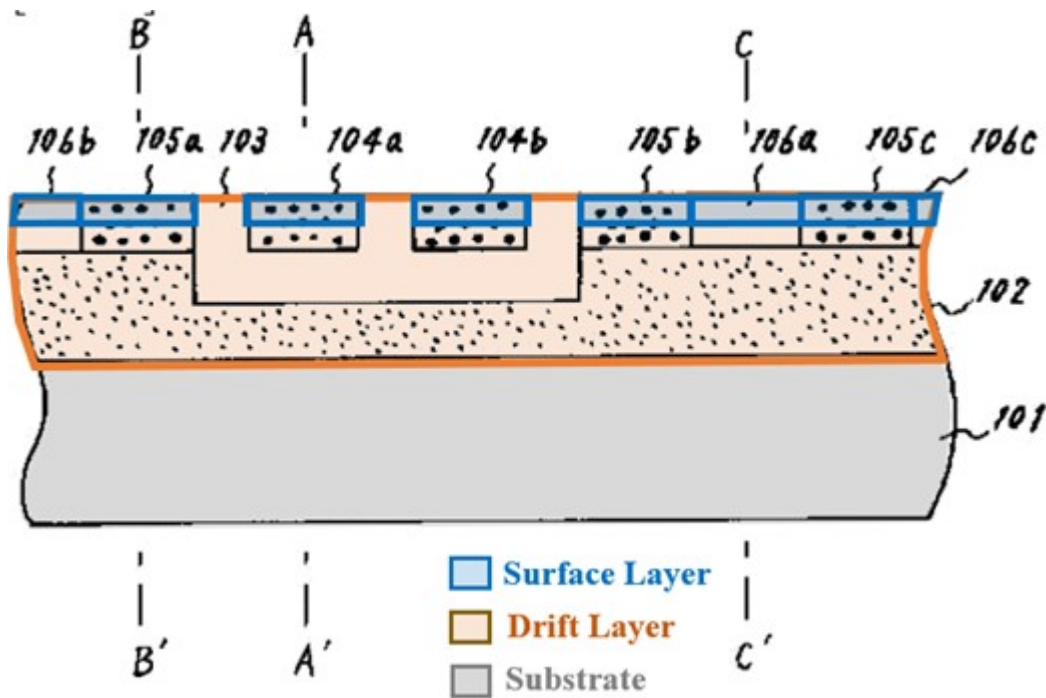
Ex.1001, FIG. 5(b); Ex.1030 at 7. The SDL in Figure 5(b) has a well region (green) disposed in it, forming a nested structure, as required by the claim (*see* element [7.6]):



Ex.1001, FIG. 5(b); Ex.1030, 7; *id.*, 11 (“the ‘well region’ is part of the ‘single drift layer.’”).

Onoda discloses a SDL to the same extent Figure 5(b) of the ’502 Patent does. Ex.1003, ¶¶139-140. In Onoda’s Figure 3, the second semiconductor layer 102 is an example of the claimed drift layer. *Id.* This SDL (tan) is “disposed between ‘the

other surface [(bottom surface)] of said surface layer [(blue)]' and said substrate [(grey)]" under PO's interpretation, and in exactly the same way as depicted in PO's annotated Figure 5(b) above. This is demonstrated in Figure 8 of Onoda, which shows the manufacturing process of semiconductor substrate 100. See Ex.1042, [0041]-[0051].



Ex.1042, FIG. 8, [0041], [0046], [0047]. Onoda's P-type well regions 105a, 105b and 105c and N-type well regions 103, 106a, 106b, and 106c are disposed in a single drift layer (tan) disposed between a surface layer (blue) and the substrate (grey). *Id.*; §IX.B.1.b.

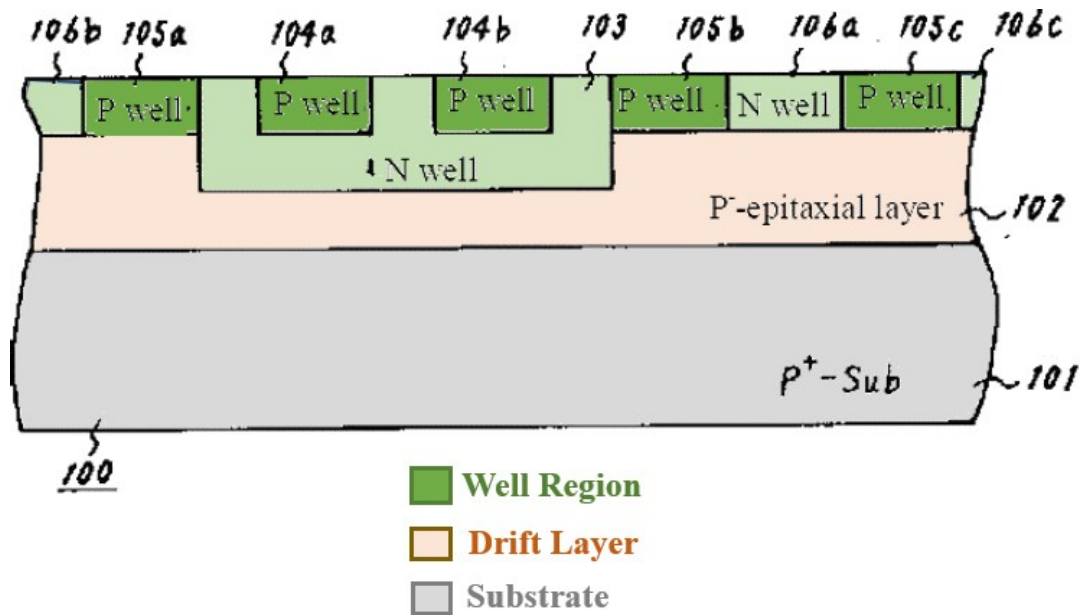
Onoda meets all other claim requirements associated with the SDL to the same extent Figure 5(b) meets them, as explained below. See §§IX.B.1.f–g (elements

[7.5]-[7.6]); Ex.1003, ¶¶140. Notably, as detailed in element [7.5], the second semiconductor layer 102 in Onoda is a *single* drift layer because it has a graded-dopant concentration that, according to PO, creates a unidirectional electric drift field that aids the movement of minority carriers in a *single* direction—from the surface layer to the substrate. Ex.1030, 7; Ex.1046, 253-54, 289-290; §IX.B.1.f.

- f. **Element [7.5]: “said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and”**

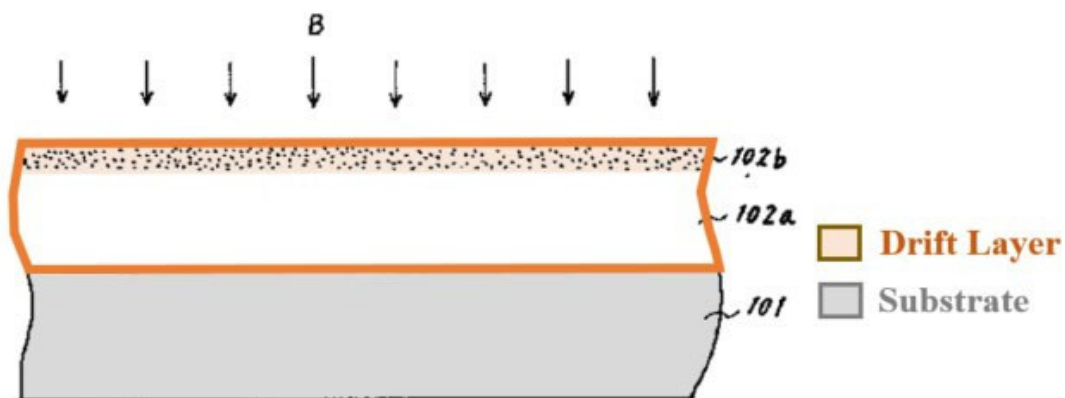
Onoda discloses this element. Ex.1003, ¶¶141-157.

Graded concentration of dopants – Onoda discloses a SDL having a graded concentration of dopants extending between the surface layer and the substrate. Ex.1003, ¶¶142-152. In Onoda, “FIG. 2 depicts critical portions of the semiconductor substrate that is applied to the first embodiment of the present invention; . . .” Ex.1042, [0041]. Within the semiconductor substrate 100, “101 is a first semiconductor layer made from a heavily-doped . . . P-type silicon substrate, and 102 is a P-type second semiconductor layer having a dopant concentration that is lower than the dopant concentration of the first semiconductor layer 101 . . . deposited through epitaxial deposition to a thickness of between 1 and 10 μm onto the surface of the first semiconductor layer.” *Id.*



Ex.1042, FIG. 2.

Onoda discloses how the P-type semiconductor layer 102 is formed. As illustrated in Figure 4, “a lightly-doped P-type epitaxial layer 102a . . . is formed with a thickness of about 5 μm through epitaxial deposition onto the surface of a first semiconductor layer 101, which comprises a heavily-doped P-type silicon substrate (silicon wafer).” Ex.1042, [0046]; Ex.1003, ¶¶143-144.

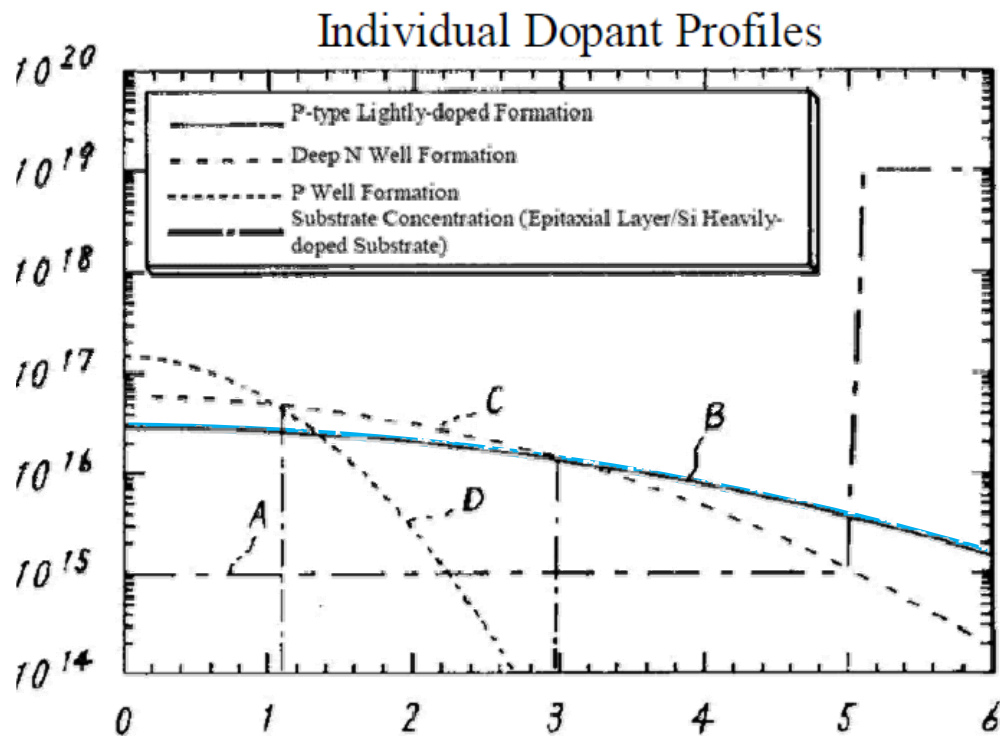


Ex.1042, FIG. 4. According to Onoda, a P-type dopant (e.g., boron B) is

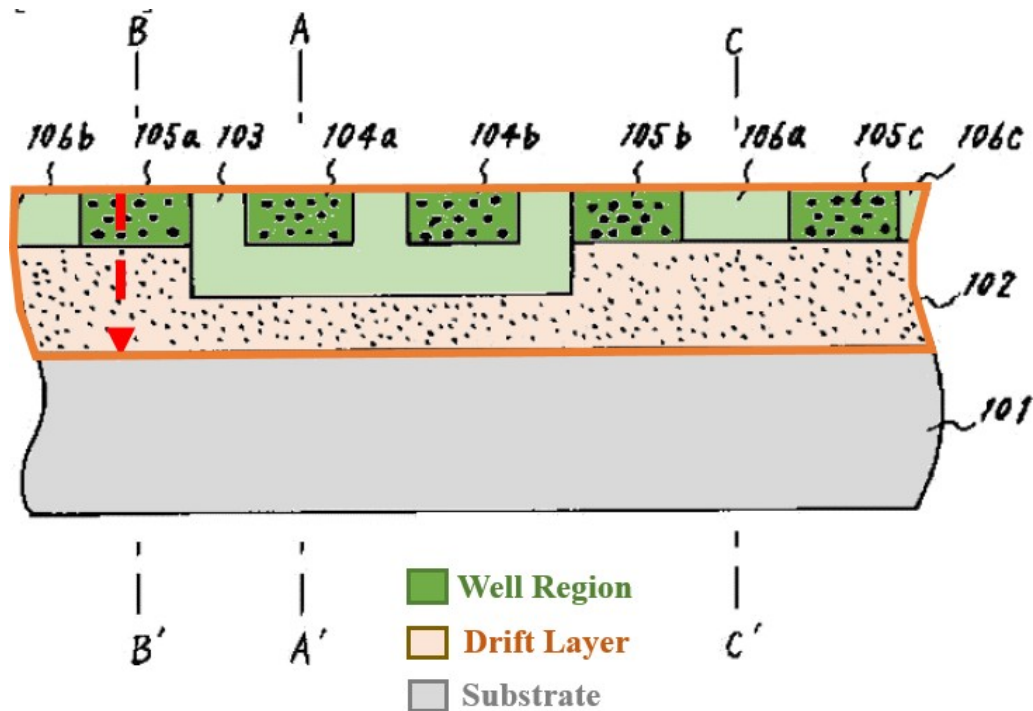
implanted into the epitaxial layer 102a to form an ion implantation layer 102b. *Id.*, [0047]. Thereafter, a heat treatment is carried out to thermally diffuse the dopant (boron) in the ion implantation layer 102b to produce a lightly-doped P-type second semiconductor layer 102. *Id.*; Ex.1003, ¶145.



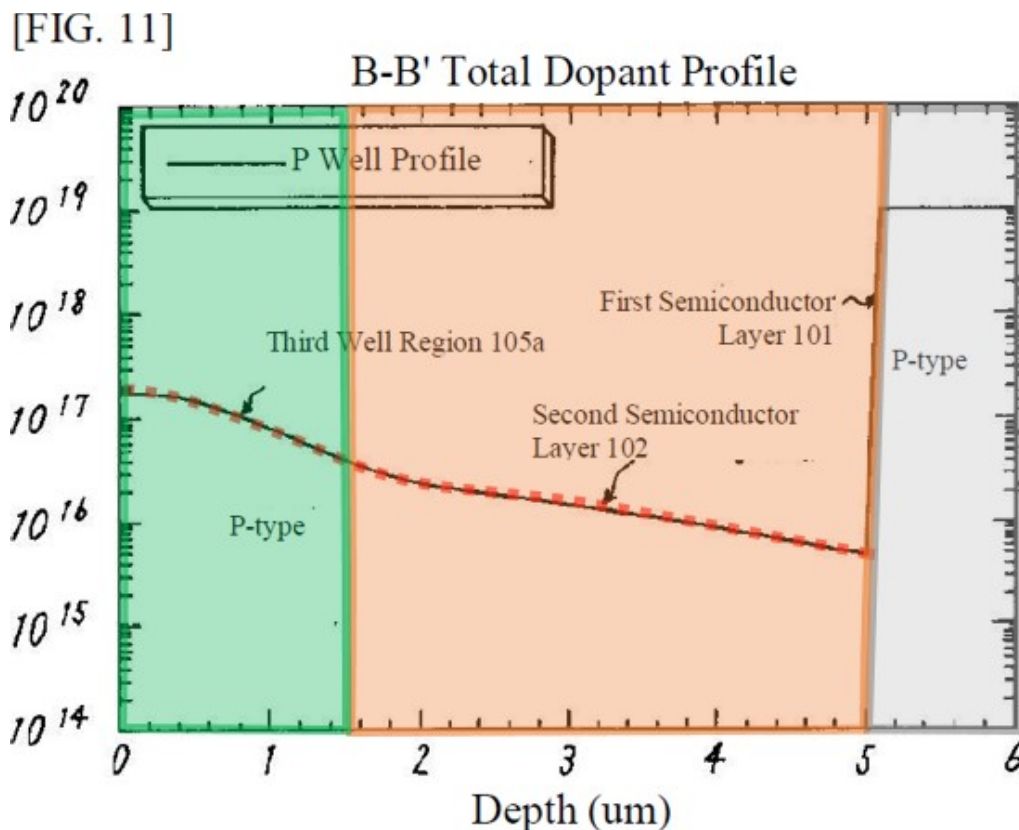
Ex.1042, FIG. 5, [0046], [0047]. As illustrated in Figure 5, the dopant concentration of the epitaxial layer 102a, as a whole, is between 1×10^{16} and $1 \times 10^{18}/\text{cm}^3$. *Id.*, [0047]. At this time, the dopant concentration of boron (B) is depicted by the solid line B indicated in Figure 9 below. *Id.*; Ex.1003, ¶146.



Ex.1042, FIG. 9. As further discussed below in Section IX.B.1.g (element [7.6]), P- well regions 105a, 105b, 105c, 104a and 104b (dark green) and N-well regions 103, 106a, 106b and 106c (light green) are formed in semiconductor layer 102 resulting in the structure depicted in Figure 8 below. *Id.*, [0042], [0048]-[0050]; Ex.1003, ¶147.

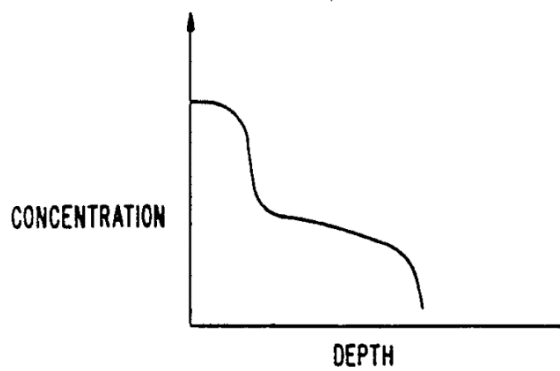


Ex.1042, FIG. 8. The dopant profile appearing in the B-B' cross-section in Figure 8 is shown in Figure 11. *Id.*, [0052]. As Figure 11 illustrates, “both the third well region 105a and the second semiconductor layer 102 are of the same conductivity type, that is, P-type, so there is no clear boundary between the third well region 105a and the second semiconductor layer 102, but rather *the dopant concentration falls off smoothly.*” *Id.*; Ex.1003, ¶147.

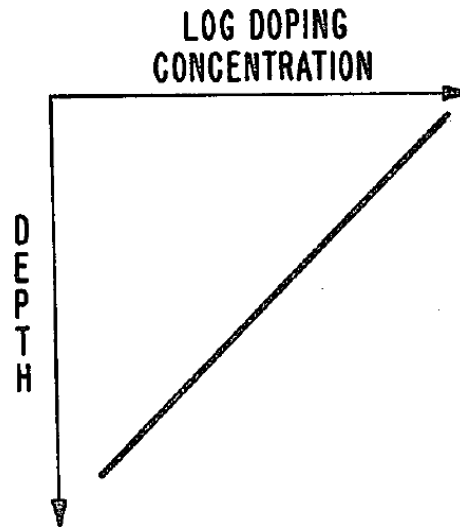


Ex.1042, FIG. 11.

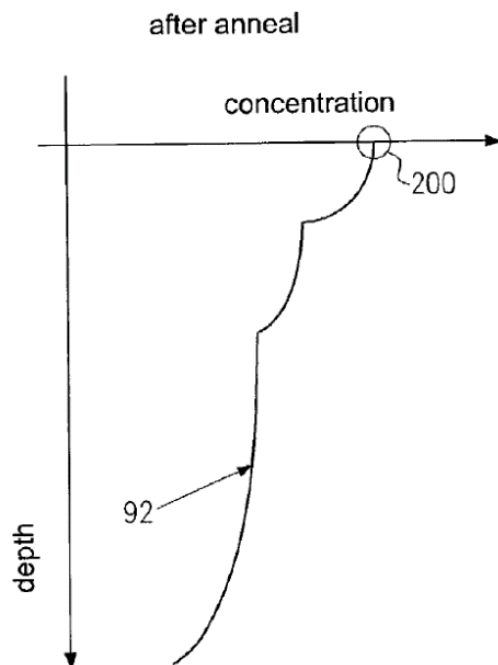
A POSITA would have understood that Onoda's *high-to-low* concentration is *gradually decreasing* across Onoda's single drift layer (second semiconductor layer 102) because it is formed through ion implantation techniques and thermal diffusion techniques. Ex.1042, [0041], [0046], [0047], FIGS. 4, 5; Ex.1003, ¶148. Indeed, a downward-sloping graded-dopant concentration formed through ion implantation and thermal diffusion was well-known in the art. Such gradients were disclosed in many prior art references, such as Payne, Kawagoe, Wiczorek and Jastrzebski, as shown below. Ex.1003, ¶¶149-152.



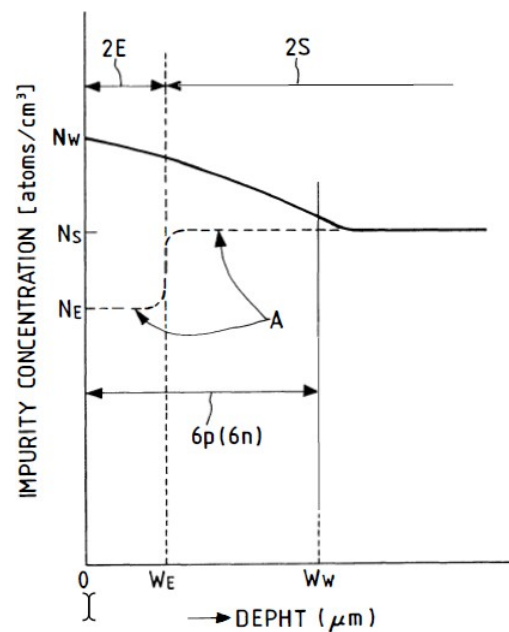
Payne, Figure 11



Jastrzebski, Figure 1b



Wieczorek, Figure 2b



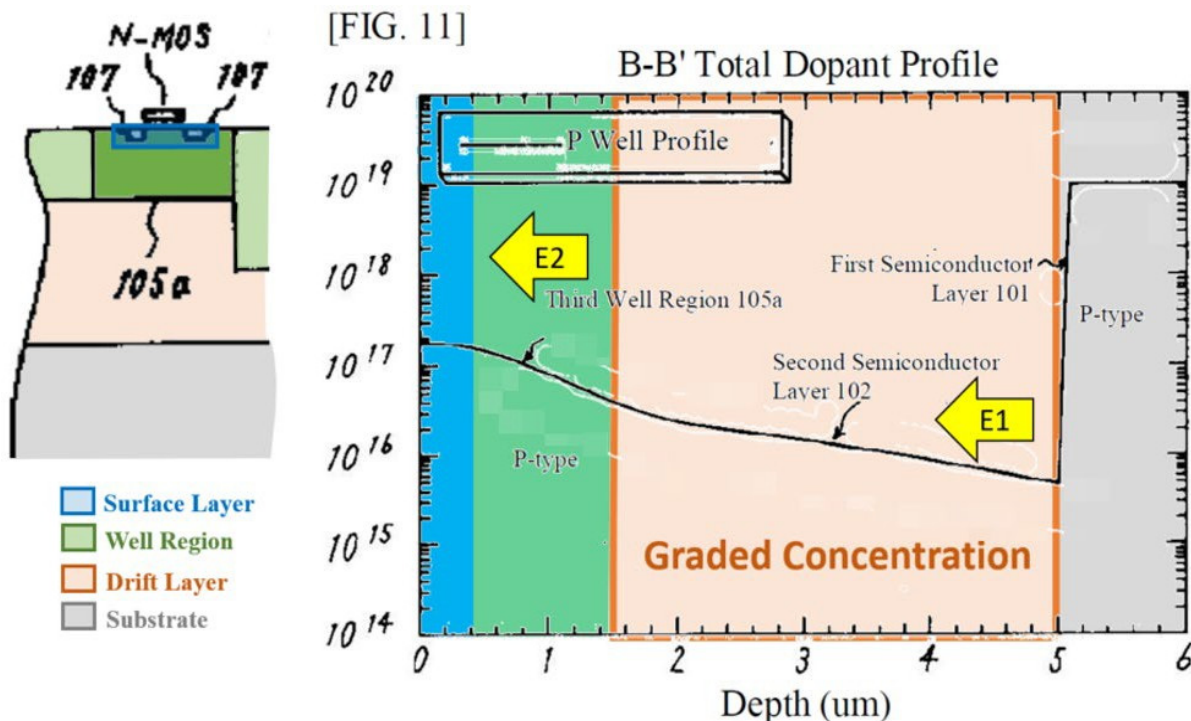
Kawagoe, Figure 17

Ex.1005, FIG. 11, 3:28-42, 4:19-39, 5:7-17; Ex.1007, FIG. 17, 15:62-16:2, 17:31-61; Ex.1038, FIG. 2b, [0008], [0010]-[0011]; Ex.1010, FIG. 1b, 5:5-27;

9:2-8. Significantly, Payne’s Figure 11 illustrates a graded-dopant profile that is downward-sloping over a *nested well structure* similar to the dopant profile of Onoda’s second semiconductor layer 102, as detailed under IX.A.1.e-f.

As discussed above with regard to element [7.4], Onoda discloses a SDL (tan) having a downward-sloping dopant concentration extending between the surface layer (blue—*i.e.*, starting at the 0 μm depth level) and the substrate (grey, starting at the 5 μm depth level). §IX.B.1.e.

First static unidirectional electric drift field to aid the movement of minority carriers – The below annotation of Onoda’s Figure 11 depicts the exemplary first static unidirectional electric drift field (“E1”) described in Section IX.A.1.f, at a depth corresponding to Onoda’s second semiconductor layer 102 (tan).



Ex.1042, FIG. 11, [0041], [0046], [0047], [0052]; Fig. 3 (excepted).

Thus, given Applicant’s repeated representations to the Patent Office and the Jastrzebski and Kamins cited art relied on by Applicant—such a downward-sloping graded-dopant concentration creates a “built-in” unidirectional electric drift field to aid the movement of minority carriers from the surface layer to the substrate. Ex.1003, ¶¶153-155; §IX.A.1.f.⁹

Such a profile is created “through ion implantation techniques and thermal diffusion techniques” and thus the profile (and any resulting electric drift field) is static—it is set once the CMOS device has been fabricated and does not change afterwards. Ex.1003, ¶156; §IX.A.1.f. As discussed in Section IX.A.1.f, Applicant described “static” similarly during prosecution of the parent ’195 Patent. Ex.1046, 318 (citing Ex.1009), 333 (same).

Accordingly, Onoda satisfies element [7.5] under PO’s plain-meaning constructions. Ex.1033. Onoda’s graded-dopant concentration is downward-sloping over the entire single drift layer (tan)—in fact, from the top of the silicon/surface

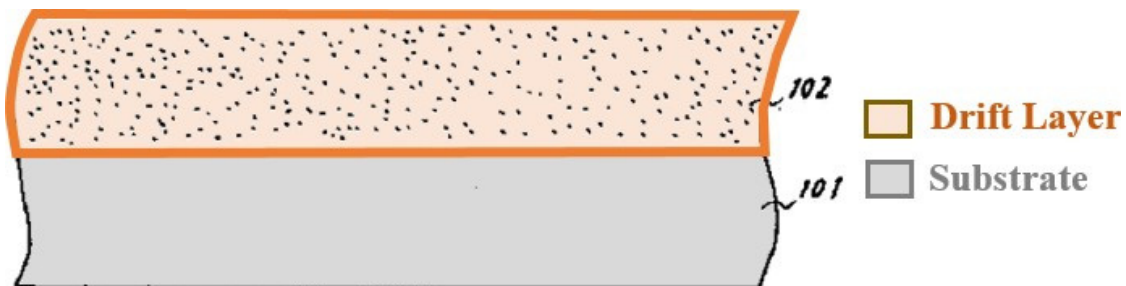
⁹ The electric fields in Figure 11 are left-facing, because the downward-sloping graded-dopant concentration is in a P-Well (rather than N-well). Nonetheless, as discussed in Section IX.A.1.f, the electric fields aid the movement of minority carriers (here, electrons in a P-well) from the surface layer to the substrate, as required. Ex.1003, ¶155.

layer (blue) to the bottom of the SDL—and thus, according to PO (and in light of Applicant’s representations to the Patent Office), creates a static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. Ex.1003, ¶157.

- g. **Element [7.6]: “at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.”**

Onoda discloses this element. Ex.1003, ¶¶158-172.

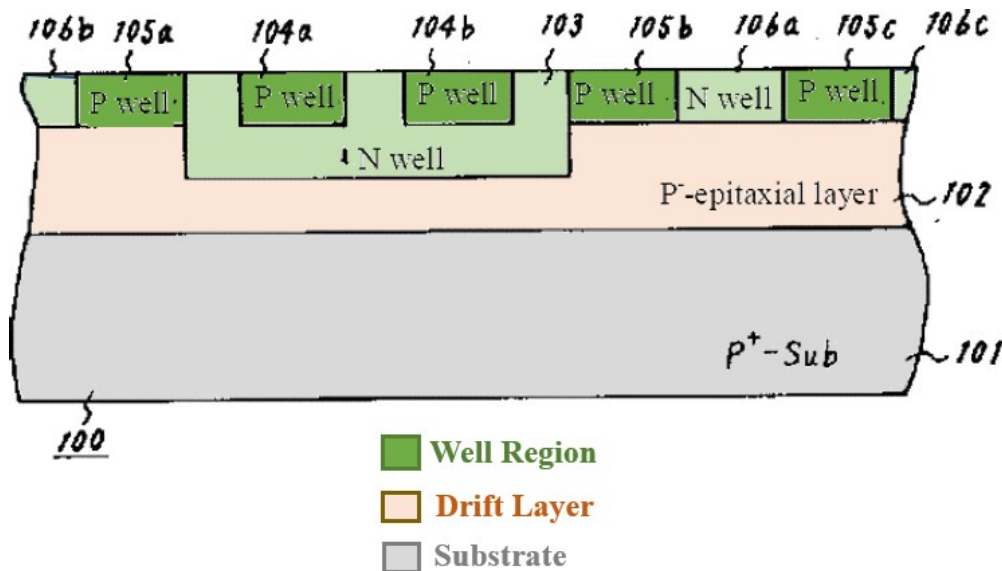
Well region disposed in said single drift layer ... having a graded concentration of dopants – As detailed above, Onoda discloses a SDL (semiconductor layer 102) (tan), as shown below. Ex.1042, [0046], [0047]; §§IX.B.1.e-f.



Ex.1042, FIG. 8; *id.*, FIGS. 2 and 3.

Each well in Onoda’s lightly doped P-type semiconductor layer 102—*e.g.*,

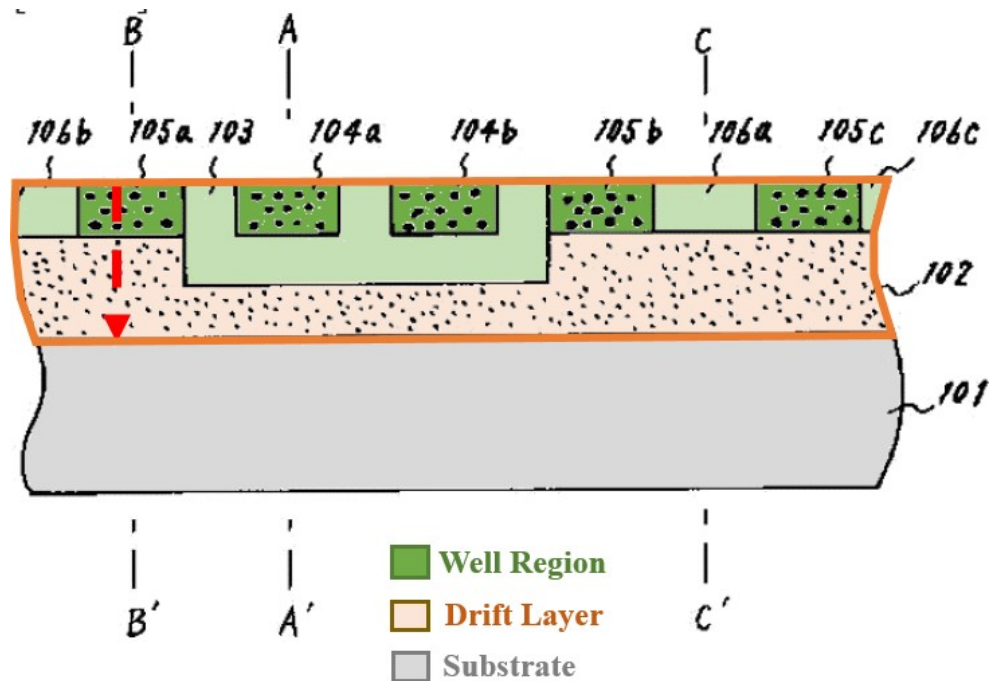
P- wells 104a, 104b, 105a, 105b, and 105c (dark green) and N-wells 103, 106a, 106b, and 106c (light green)—is an example of a well region disposed in a single drift layer (tan). Ex.1042, [0041], [0042], [0046]-[0049]; Ex.1003, ¶¶159-160.



Ex.1042, FIG. 2.

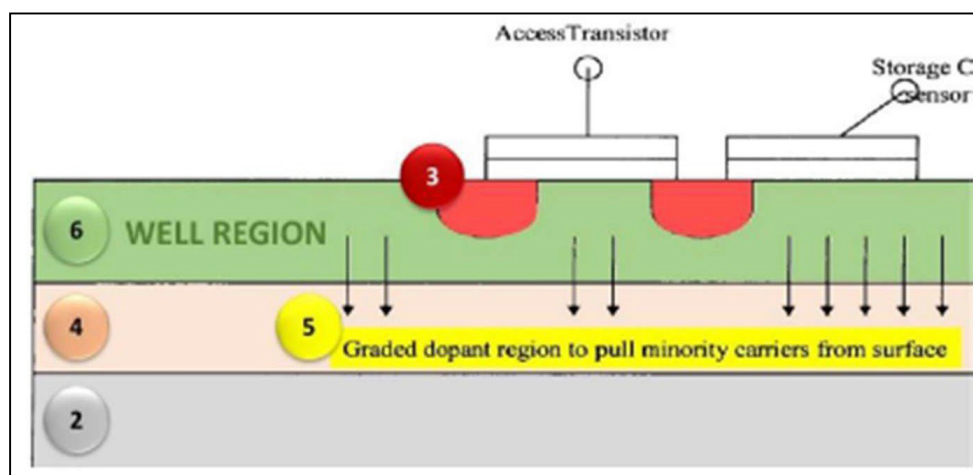
Onoda discloses the steps to form the P-wells and the N-wells in the lightly-doped semiconductor layer 102. Ex.1042, [0048]-[0050]. After forming the epitaxial second semiconductor layer 102, an N-type dopant (*e.g.*, phosphorus P) is implanted and heat treatment is carried out to form an N-type first well region 103 with a depth of about 3 μm . *Id.*, [0048]. Thereafter, a P-type dopant (*e.g.*, boron B) is implanted to form P-type implantation layers 104a, 104b and 105a through 105c, and an N-type dopant is implanted to form N-type implantation layers 106a through 106c. *Id.* Finally, after carrying out heat treatment, P-type second well regions 104a, 104b, P-type third well regions 105a through 105c, and N-type fourth well regions 106a

through 106c are formed in the second semiconductor layer 102, as illustrated in Figure 8 below. *Id.*, [0050]; Ex.1003, ¶161.



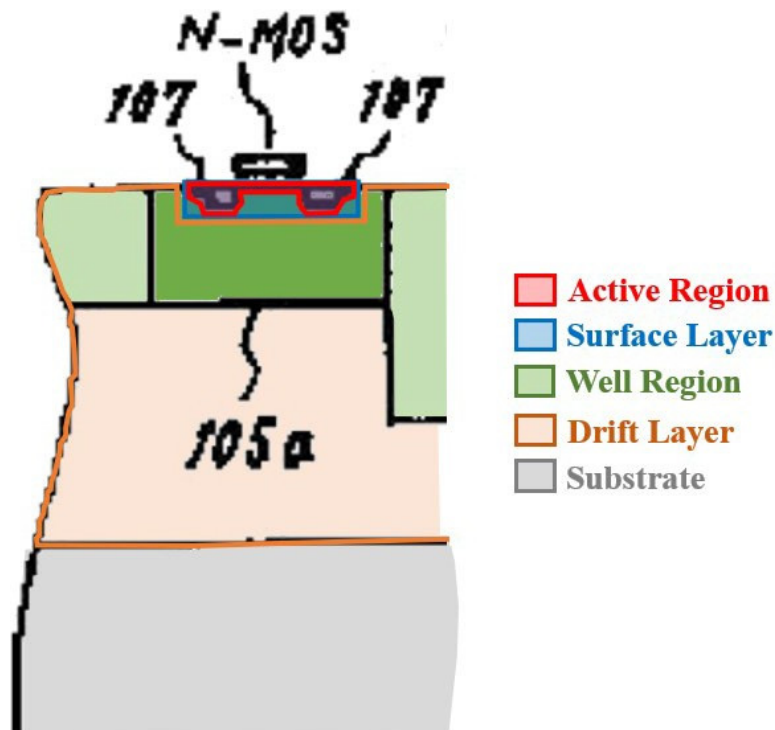
Ex.1042, FIG. 8.

Notably, Onoda satisfies element [7.6] to the same extent that Figure 5(b) of the '502 Patent, annotated by PO in its claim construction brief, meets it:

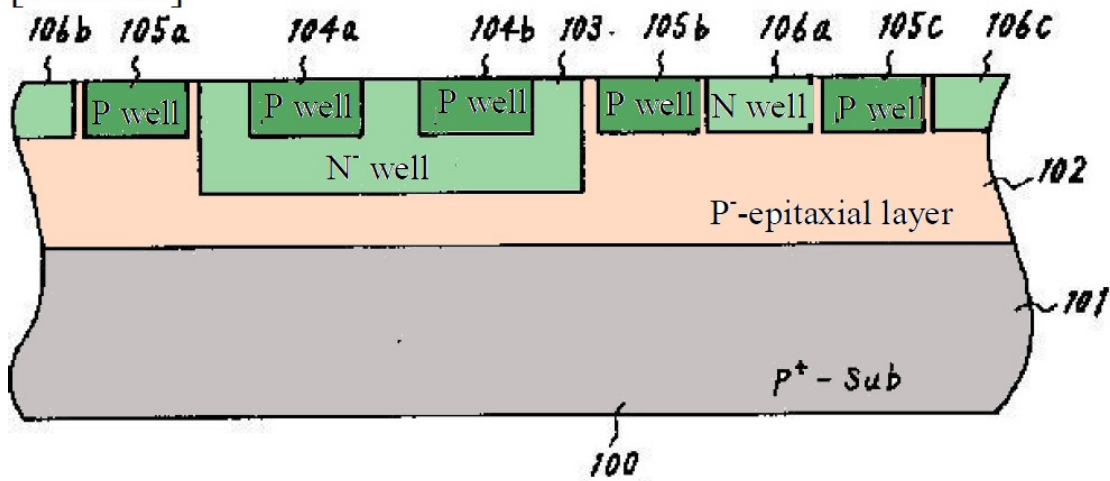


Ex.1001, FIG. 5(b); Ex.1030, 7.

To the extent PO argues that the well region must be entirely contained within the SDL, Onoda discloses that too. Figure 3 (excerpted below) shows that the well regions (*e.g.*, 105a) are entirely contained within the drift layer *See, e.g.*, Ex.1042, FIGS. 2 and 3.

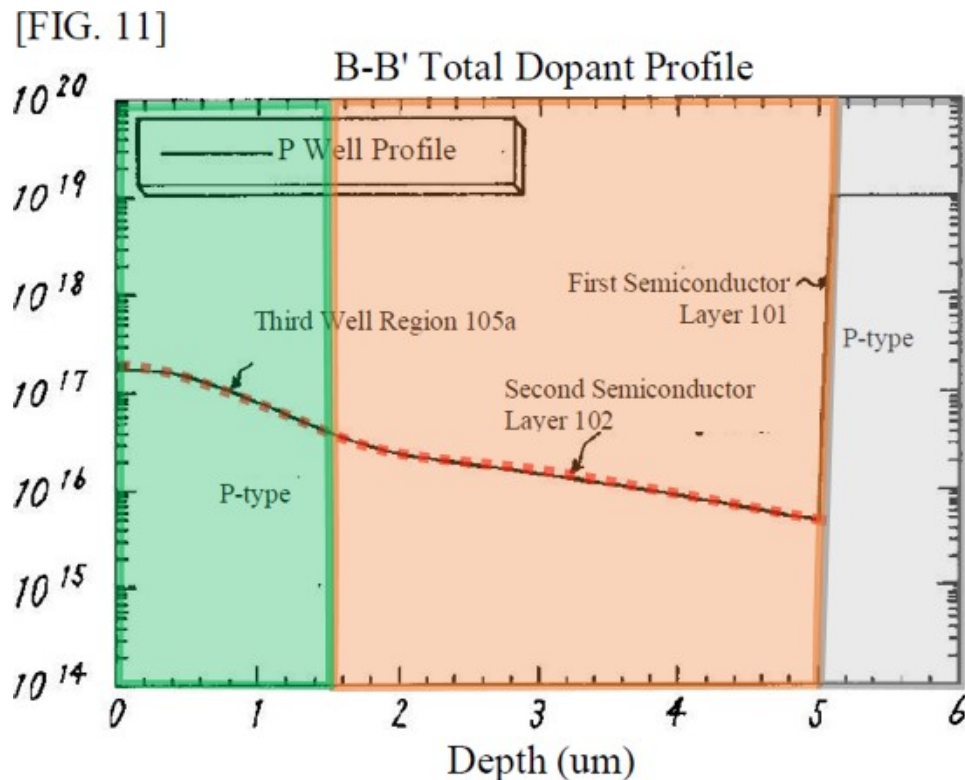


Ex.1042, Fig. 3 (excerpted, annotated). Furthermore, whereas Onoda's Figure 3 shows well regions in contact with one another, Onoda's Figure 13 shows an alternate structure "wherein the first well region 103, third well region 105, and fourth well region 106 are separated from each other, that is, wherein the second semiconductor layer 102"—*i.e.*, the drift layer—"is interposed between the well



Ex.1042, Fig. 13 (annotated). This likewise shows the well regions are entirely contained within the SDL. Ex.1003, ¶162.

The dopant profile appearing in the B-B' cross-section in Figure 8 (above) is shown in Figure 11 (below). As depicted therein, “a third well region 105a is formed down to a depth of about 1.5 μm from the surface of the second semiconductor layer 102, and the second semiconductor layer 102 is interposed from the bottom surface of the third well region 105a down to the surface of the first semiconductor layer 101.” Ex.1042, [0052]. “[B]oth the third well region 105a and the second semiconductor layer 102 are of the same conductivity type, that is, P-type, so there is no clear boundary between the third well region 105a and the second semiconductor layer 102, but rather the dopant concentration falls off smoothly.” *Id.*; Ex.1003, ¶¶163-169.



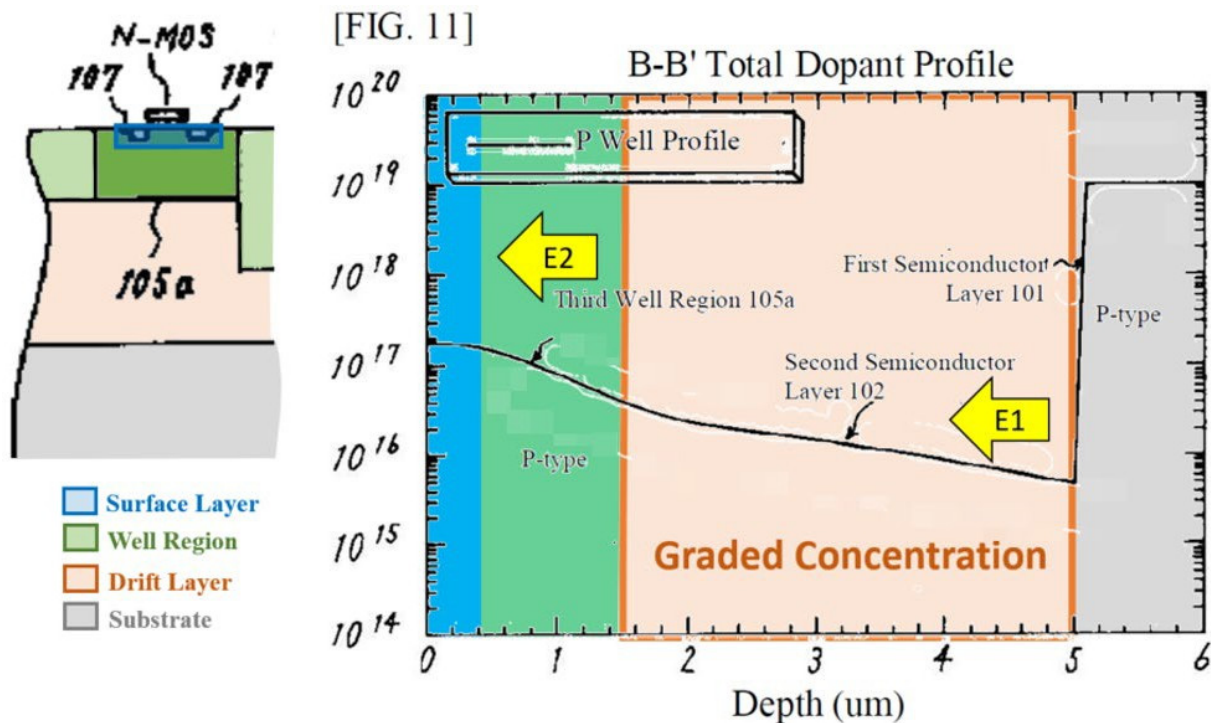
Ex.1042, FIG. 11.

Further, as also detailed above with respect to element [7.4], Onoda's structure has a downward-sloping graded-dopant concentration extending between the surface layer and the substrate, such that well region 105a (green) also has a downward-sloping graded-dopant concentration. Ex.1042, [0052]; Ex.1003, ¶168; §IX.B.1.e. Onoda discloses that in Embodiment 1, "the first through fourth well regions are all formed through thermal diffusion, and thus the dopant profiles thereof are profiles that approximate *Gaussian distributions with the concentrations at maxima near the surface.*" Ex.1042, [0053].

Accordingly, Onoda satisfies element [7.6] under PO's construction that the term "well region" means "a doped region that surrounds the active region of a

semiconductor device.” Ex.1033. As shown in Onoda’s Figures 2 and 3, the exemplary well region (green) is a doped region that surrounds both the surface layer (blue) and the active region therein. Ex.1003, ¶169; §IX.B.1.d.

Second static unidirectional electric drift field to aid the movement of minority carriers – The below annotation of Onoda’s Figure 11 depicts the exemplary first static unidirectional electric drift field (“E1”) described in Section IX.A.1.f, at a depth corresponding to Onoda’s well (tan), and an exemplary second static unidirectional electric drift field (“E2”), at a depth corresponding to Onoda’s second semiconductor layer 102 (green) (exemplary well region disposed in the single drift layer).



Ex.1042, FIG. 3 (excerpted, annotated) FIG. 11 (annotated). Moreover, E1 and E2 are illustrated as electric fields having different magnitudes, to reflect the different local slopes (gradients) of the dopant profile. Ex.1003, ¶170; Ex.1022, [0071] (“the vertical ϵ -field is established by the rate of change in the graded dopant concentration, *i.e.*, the greater the rate of change ... the greater the intensity of the ϵ - field.”). Further, Onoda’s graded-dopant profile, including the profile in the well region, is set once the device has been fabricated and does not change, making the profile (and any resulting electric field) static, as described in §IX.B.1.f.

Further, based on Applicant’s repeated representations during prosecution of the parent ’195 Patent , and according to the Jastrzebski and Kamins prior art relied on by Applicant during the prosecution, and PO’s statements in its claim construction brief, the downward-sloping graded-dopant concentration in each of these well regions creates a (second) static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. *Id.*; §IX.A.1.f.

In light of the above, Onoda satisfies element [7.6] under PO’s plain-meaning construction of “to aid the movement of minority carriers.” Ex.1033. As shown in Figure 11 above, Onoda’s graded-dopant concentration is downward-sloping over the entire well region, and thus, according to PO (and also in light of Applicant’s

representations to the Patent Office, discussed in §IX.A.1.f), it creates a static unidirectional electric drift field that aids the movement of minority carriers downward from the surface layer to the substrate. Ex.1003 ¶¶171-172.

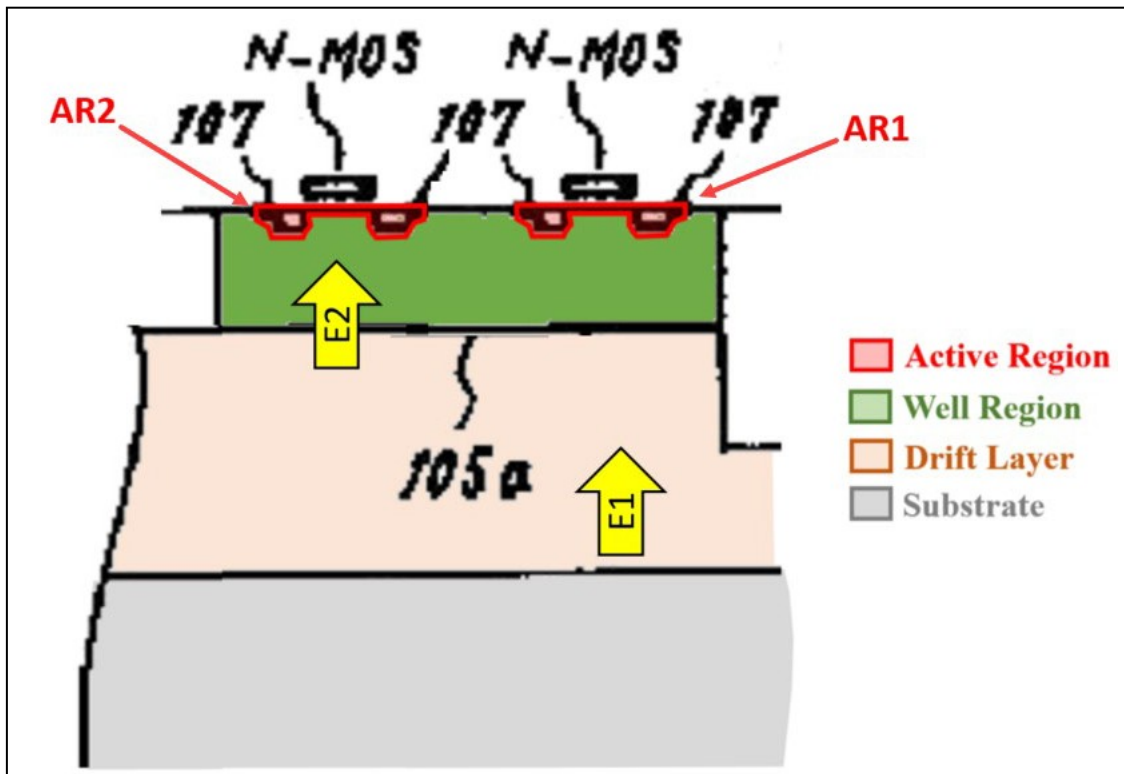
2. Dependent Claim 8: “The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.”

Onoda discloses this element. Ex.1003, ¶¶173-176.

As discussed in Sections IX.B.1.e-f, second semiconductor layer 102 (SDL)(tan) generates a first static unidirectional electric field E1 (yellow) that aids the movement of carriers that are in, or originate from, active region AR1 (red) above it. Ex.1003, ¶174. As discussed above in Section IX.B.1.d, Figure 3 from Onoda illustrates active regions containing NMOS transistors with source/drain regions in a doped P-well 105a, 105b and 105c, and PMOS transistors with source/drain regions in a doped N-well 106a, 106b, and 106c. Ex.1042, FIG. 3, [0042], [0055], [0044].

While Onoda’s Figure 3 illustrates a single NMOS transistor formed in P-well 105a, Onoda expressly discloses that the “P-type third well region [is] formed in the surface of the second semiconductor layer,” and that “at least *some N-channel MOS transistors of the plurality of the N-channel MOS* transistors that structure the peripheral circuitry are *formed in the third well region.*” Ex. 1042, [0009]; *see also*

id., [0054] (referring to “the plurality of MOS transistors that are formed in” third well region 105a (among other regions)). To illustrate these express teachings, Dr. Banerjee has prepared Figure 3M below, which extends the P-Well 105a in Onoda’s Figure 3 past to the left and shows two NMOS transistors, each with its active region indicated in red—AR2 (left), AR2 (right)—formed in the P-Well 105a (green). Ex.1003, ¶175. The P-well region generates a second static unidirectional field E2 (yellow) that aids movements of carriers that are in, originate from, active region AR2 (red) above it. For this mapping, the surface layer of claim 7 includes both active regions AR1 and AR2. §IX.B.1d; Ex.1003, ¶175.



Ex. 1042, FIG. 3M. Dr. Banerjee explains that Figure 3M not only reflects

the teachings of Onoda, but also reflects standard practice in CMOS layout and fabrication. Ex.1003, ¶175. Other prior art references confirm this. Ex.1054 (Maziasz), 27 (“Each cell consists of two horizontal diffusion rows for pMOS and nMOS transistors. This implies that single p- and n-wells can be used.”), Figure 2.3(b); Ex.1049 (Yamada), 6:51-53 (“diffusion layers [(active regions)] 60 and 61 [of] NMOS transistors” formed in “a common p-well 43” as shown in Figures 5-6).

Electric fields E1 and E2 are adapted to the grading of dopants in second semiconductor layer 102 (SDL) (tan) and P-type well region 105a (well region) (green), respectively, because the direction of electric fields E1 and E2 (*i.e.*, toward the surface or away from the surface) is dependent on the local slope of the graded dopant profile according to Applicant’s repeated representations during prosecution of the parent ’195 Patent, the Jastrzebski and Kamins prior art relied on by Applicant during its prosecution, and PO’s statements in its claim construction brief as discussed in §IX.A.1.f (including fn.8). Additionally, the magnitude of electric fields E1 and E2 also depends on the local grading of dopants. §IX.B.1.g; Ex.1022, [0071]; Ex.1003, ¶176.

3. Dependent Claim 11: “The semiconductor device of claim 7 wherein the semiconductor device is a flash memory device.”

Onoda discloses this element. When discussing the first embodiment, Onoda discloses a “configuration of a *flash memory* . . . to which this first embodiment is

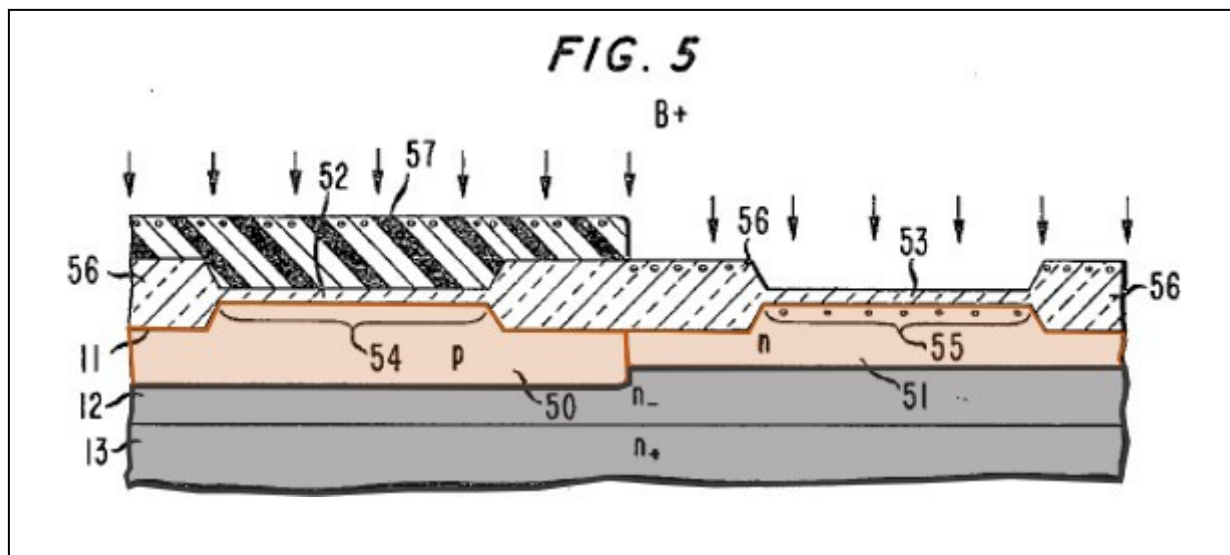
applied.” Ex.1042, [0029], [0041] (“semiconductor substrate 100 applied in this first embodiment in order to form *flash memory*”), [0046] (“A method of manufacturing a flash memory structured in this way, and, . . . a method for manufacturing a semiconductor substrate 100 that is applied to *a flash memory*, will be explained . . .”). Ex.1003, ¶177.

C. Ground IV

1. Dependent Claim 8: “The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.”

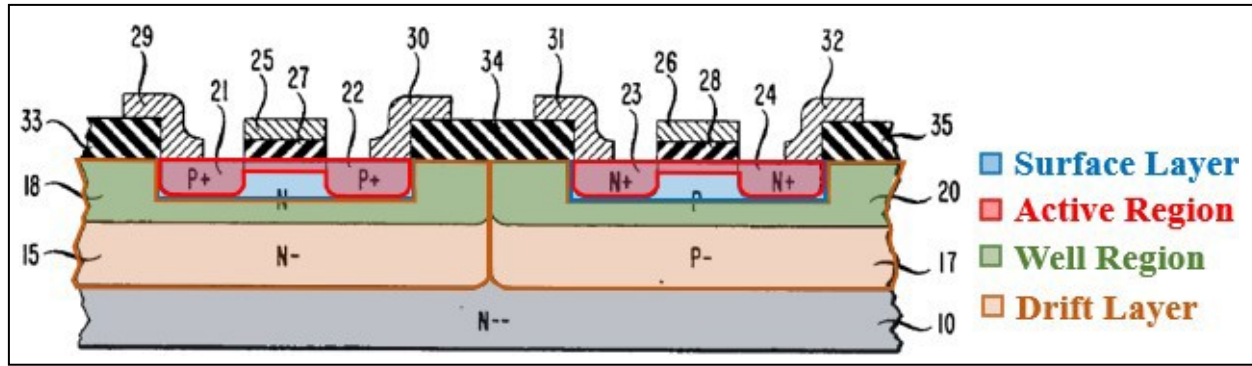
Payne discloses or renders obvious claim 7. §IX.A.1. Payne in combination with Parrillo (“Payne-Parrillo”) renders obvious the additional limitation of claim 8. Ex.1003, ¶¶178-192. Parrillo and Payne are contemporaneous patents that share a common inventor (Richard S. Payne). Ex.1025; Ex.1005. Both patents were originally assigned to AT&T Bell Labs. *Id.*

Parrillo is directed to “twin-tub” (twin well) CMOS semiconductor devices. Ex.1025, 1:13-20, 2:22-25 (“[T]he invention is a twin-tub complementary CMOS integrated circuit in which the n-tubs and p-tubs are contiguous with one another with no spacing between.”). Parrillo’s Figure 5 below illustrates contiguous p-tub (p-well) 50 (left, tan) and n-tub (n-well) 51 (right, tan).



Ex.1025, FIG. 5. Parrillo explains that each tub (well) of its “twin-tub” CMOS device contains “one or more transistors.” *Id.*, 3:22-25 (“The device may, for example, be a VLSI circuit in which case there would be a large number of tubs of each type, each of which might contain *one or more transistors*.”). Indeed, a VLSI device contains a very large number of transistors. *Id.*, 1:13-20, 3:34-38 (“a VLSI circuit employ[s] a large number of p-channel and n-channel transistors.”).

Payne is directed to improving “twin-tub” (twin-well) CMOS technology similar to that described in Parrillo by adding a shallow well (“surface region”) (green) in each deep well (“tub”) (tan) of a twin-tub CMOS device, as illustrated in Payne’s Figure 10 below. Ex.1005, 1:5-14, 1:59-2:28, 6:20-21; *id.*, 1:15-50; §§IX.A.1.e-g; Ex.1003, ¶180. Payne teaches that this nested well structure improves packing density. *Id.*, Abstract, 1:51-54, 6:17-19, 6:57-59.



Ex.1005, FIG. 10. A POSITA would have been motivated to apply Payne’s improved CMOS technology to a known twin-tub CMOS semiconductor device that has individual tubs containing multiple transistors, such as that described by Parrillo, to achieve high packing density as taught by Payne. Ex.1003, ¶181. Doing so would have resulted in forming Payne’s nested well structure in the tubs to reduce the spacing between active regions of adjacent transistors. *Id.*; Ex.1005, Abstract, 1:51-54, 6:17-19, 6:57-59. There would have been a reasonable expectation of success because the Payne and Parrillo patents are closely related (as discussed above) and Payne shows that a POSITA knew how to use Payne’s CMOS technology to improve a twin-tub CMOS device similar to that described by Parrillo. Ex.1005, 6:20-21 (Payne’s technology “is designed primarily for twin-tub structures”); Ex.1003, ¶¶182-183. This combination of Payne and Parrillo would have merely amounted to (1) use of a known technique (Payne’s improved twin-tub CMOS technology) to improve similar devices (known twin-tub CMOS devices with individual tubs having multiple transistors) in the same way (to increase packing density) and (2) a

simple substitution of one known element (Parrillo's twin-tub CMOS technology) with another (Payne's improved twin-tub CMOS technology) to fabricate a known twin-tub CMOS device with individual tubs having multiple transistors.

While Payne's Figure 10 illustrates a single transistor formed in each tub, Payne expressly discloses that "the figures show fabrication of a device which is typically part of an integrated circuit including many other [transistor] devices." Ex.1005, 2:53-55, 6:17-19, 6:57-59. And given the jagged edges to the left and right of Payne's Figure 10, Payne is at least suggestive that its illustrated tubs contain multiple transistors just like Parrillo describes. Ex.1025, 3:22-25. To illustrate this, Dr. Banerjee has prepared Figure 10M below, which extends Payne's Figure 10 past its left jagged edge and shows two PMOS transistors, each with its active region 21/22 (red), formed in the nested n-well structure (left) that consists of n-tub 15 (tan) and shallow n-well 18 (green) disposed in it. Ex.1003, ¶¶184-185. As detailed in §§IX.A.1.e-g, tub 15 is an exemplary SDL. §§IX.A.1.e-g.

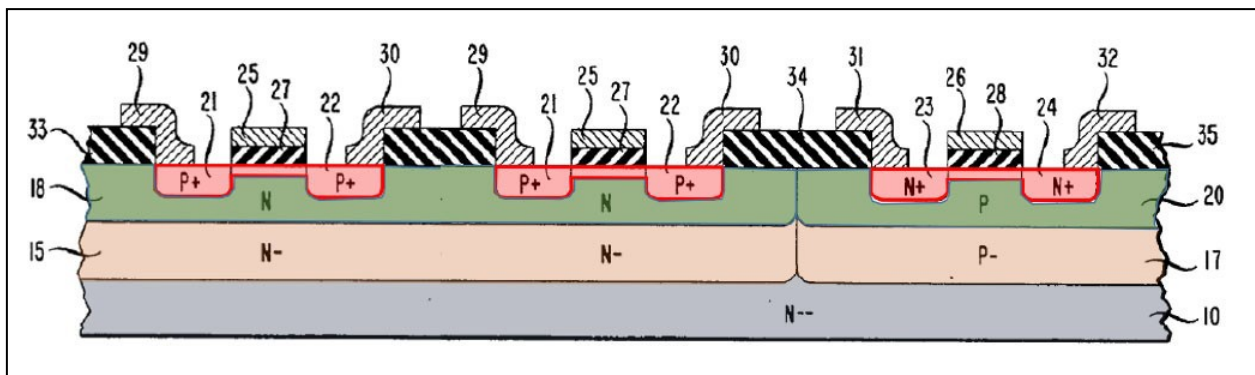
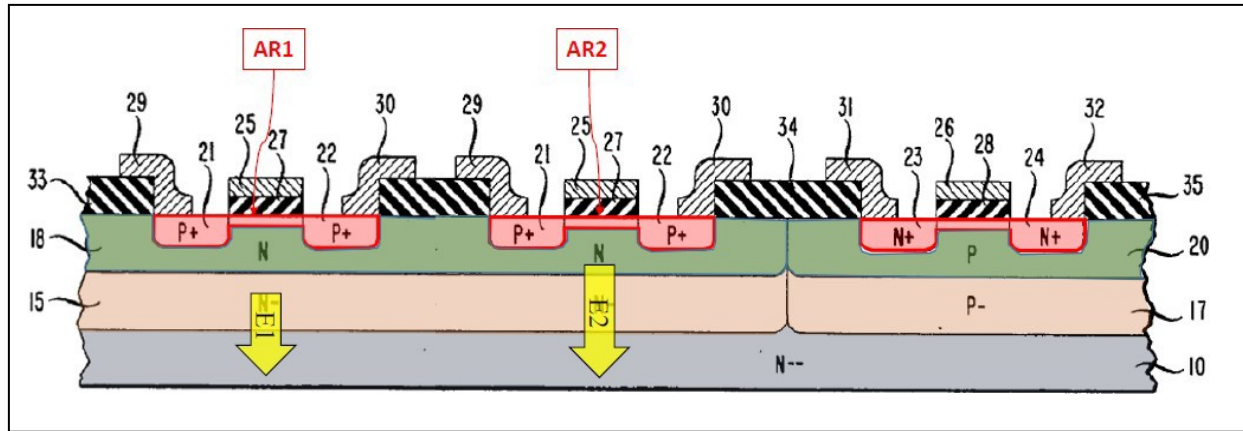


FIG. 10M. Dr. Banerjee explains that Figure 10M not only reflects the teachings of Payne and Parrillo, it also reflects standard practice in CMOS layout and fabrication. Ex.1003, ¶¶213-217. Other prior art references confirm this. *Id.*; Ex.1054 (Maziasz), 27 (“Each cell consists of two horizontal diffusion rows for pMOS and nMOS transistors. This implies that single p- and n-wells can be used.”), Figure 2.3(b); Ex.1049 (Yamada), 6:51-53 (“diffusion layers [(active regions)] 60 and 61 [of] NMOS transistors” formed in “a common p-well 43” as shown in Figures 5-6).

Figure 10M, reproduced below, makes clear that Payne-Parrillo satisfies claim 8. Ex.1003, ¶¶185-190. The figure shows that, as discussed in §IX.A.1.f, tub 15 (SDL) (tan) generates a first static unidirectional electric field E1 (yellow) that aids movements of carriers that are in, or originate from, active region AR1 (red) above it. Ex.1005, 1:60-68, 5:21-29; §IX.A.1.f; Ex.1013, 431; §§IX.A.1.d-g. Likewise, as discussed in §IX.A.1.g, well region 18 (green) generates a second static unidirectional electric field E2 (yellow) that aids movements of carriers that are in, or originate from, active region AR2 (red) above it. *Id.* For this mapping, the surface layer of claim 7 includes both active regions AR1 and AR2. Ex.1003, ¶¶185-190.



Ex.1005, FIG. 10. Electric fields E1 and E2 are adapted to the grading of dopants in tub 15 (SDL) (tan) and well region 18 (green), respectively, because the direction of electric fields E1 and E2 (*i.e.*, toward the surface or away from the surface) is dependent on the local slope of the graded-dopant profile according to Applicant's repeated representations during prosecution of the parent '195 Patent, the Jastrzebski and Kamins prior art relied on by Applicant during its prosecution, and PO's statements in its claim construction brief as discussed in §IX.A.1.f (including fn.8). Additionally, the magnitude of electric fields E1 and E2 also depends on the local grading of dopants. §IX.A.1.g; Ex.1022, [0071]; Ex.1003, ¶¶191-192.

D. Ground V

Payne in combination with Wolf ("Payne-Wolf") renders claims 9-11 obvious. Ex.1003, ¶¶193-208. Payne is directed to CMOS devices. Ex.1005, 1:5-10, 1:51-54, 6:57-59. Wolf is a well-known textbook that teaches fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on

CMOS. *See generally* Ex.1008A; *id.*, Chapter 16 (“CMOS Process Integration”); Ex.1003, ¶193. Wolf also published over 20 years after Payne was filed. Exs.1014-15. A POSITA would have therefore understood and expected that the teachings of Wolf would apply to Payne, and would have looked to Wolf for advances in CMOS technology and additional process details to the extent not covered in Payne. *Id.*

1. Dependent Claim 9: The semiconductor device of claim 7 wherein the semiconductor device is a central processing unit (CPU)."

Payne renders obvious claim 7. §IX.A.1. Payne-Wolf renders obvious the additional limitation of claim 9. Ex.1003, ¶¶195-199.

Twin-well CMOS technology was, by the early 2000s, “the dominant CMOS technology in IC production.” Ex.1008D, 181. It was also known to fabricate microprocessors (CPUs) using CMOS technology to achieve the benefits of “lower power-dissipation” in such devices. Ex.1008B, 368-370; Ex.1032, 1334 (see “microcomputer”); Ex.1003, ¶195.

Rabaey confirms this. Ex.1050, 180 (“The [CMOS] inverter is truly the nucleus of all digital [logic] designs” and, together with other “[logic] gates such as NAND, NOR, or XOR ... form the building blocks for modules such as multipliers and processors.”), 37 (“Modern [CMOS] processes are increasingly using a dual- well [(twin-well)] approach that uses both n- and p-wells ...”), 383-84, FIG. 8-6 (showing Intel Pentium processor “designed in a 0.18µm CMOS

technology.”). Sze also confirms this, describing a system-on-a-chip that includes CMOS “*logic IC (e.g., CPU)*” fabricated using twin-well CMOS technology. Ex.1051, 525-26, FIGS. 37-38; Ex.1003, ¶196.

Payne teaches an improvement on “twin tub” (twin-well) CMOS technology to reduce separation “between source and drain regions of adjacent [transistor] devices” and thus increase packing density of CMOS semiconductor devices. Ex.1005, Abstract, 1:5-8, 1:51-68, 6:17-21, 6:57-59, 1:9-50; §IX.A.

It would have been obvious to fabricate known CPUs using Payne’s improved twin-well CMOS technology for the benefit of increased packing density. Ex.1003, ¶¶197-199. Additionally, using Payne’s technology to form CPUs would have merely amounted to (1) use of a known technique (Payne’s improved twin-well CMOS process) to improve similar devices (known CPU designs) in the same way (to increase packing density) and (2) a simple substitution of one known element (CMOS technology for prior art CPUs) with another (Payne’s improved CMOS technology). *Id.* There would have been a reasonable expectation of success with predictable results because Payne’s twin-well CMOS process was a known improvement over conventional twin-well CMOS process and would have been used for its intended purpose in manufacturing known CPUs, designed for implementation using CMOS technology. *Id.*

2. Dependent Claim 10: “The semiconductor device of claim 7 wherein the semiconductor device is a DRAM device.”

Payne renders obvious claim 7. §IX.A.1. Payne-Wolf renders obvious the additional limitation of claim 10. Ex.1003, ¶¶200-203.

Twin-well CMOS technology was, by the early 2000s, “the dominant CMOS technology in IC production.” Ex.1008D, 181. It was also known to fabricate DRAM devices for “the advantages of cost per bit, device density, and flexibility of use (i.e., both read and write operations are possible) [which] have made DRAMs the most widely used form of semiconductor memory to date,” and to do so using CMOS technology to take advantage of “lower power dissipation [] and smaller soft error rates.” Ex.1008B, 587, 596-597; Ex.1003, ¶200.

Payne teaches an improvement on “twin tub” (twin-well) CMOS technology to reduce separation “between source and drain regions of adjacent [transistor] devices” and thus increase packing density of CMOS semiconductor devices. Ex.1005, Abstract, 1:5-8, 1:51-68, 6:17-21, 6:57-59, 1:9-50; §IX.A; Ex.1003, ¶201.

It would have been obvious to fabricate known DRAM devices using Payne’s improved twin-well CMOS technology for the benefit of increased packing density. Ex.1003, ¶¶201-203. Additionally, using Payne’s technology to form DRAMs would have merely amounted to (1) use of a known technique (Payne’s improved twin-well CMOS process) to improve similar devices (known DRAM designs) in

the same way (to increase packing density) and (2) a simple substitution of one known element (CMOS technology contemplated by Wolf for DRAM) with another (Payne's improved CMOS technology). *Id.* There would have been a reasonable expectation of success with predictable results because Payne's improved CMOS process was an improvement over conventional twin-well CMOS process and would have been used for its intended purpose in manufacturing a known DRAM designed for implementation using CMOS technology. *Id.*

3. Dependent Claim 11: “The semiconductor device of claim 7 wherein the semiconductor device is a flash memory device.”

Payne renders obvious claim 7. §IX.A.1. Payne-Wolf renders obvious the additional limitation of claim 11. Ex.1003, ¶¶204-208.

Twin-well CMOS technology was, by the early 2000s, “the dominant CMOS technology in IC production.” Ex.1008D, 181; Ex.1003, ¶204. It was also known to fabricate semiconductor flash memory devices to achieve the benefits of “high density [], small-die size, lower cost, and hot-electron writability of EPROMs, together with the easy erasability, on-board reprogrammability, and electron-tunneling erasure features of EEPROMs,” and to do so using CMOS technology for “lower power-dissipation.” Ex.1008B, 632-634; Ex.1008A, 808-810; Ex.1003, ¶204. Indeed, flash memory devices commonly used CMOS technology. Ex.1008B, 633-635 (describing known “CMOS flash-EEPROM” devices); Ex.1007, 22:16-17

(flash EEPROM is flash memory), 22:10-23:2, FIG. 28 (peripheral flash memory circuit with CMOS transistors); Ex.1003, ¶205.

Payne teaches an improvement on “twin tub” (twin-well) CMOS technology to reduce separation “between source and drain regions of adjacent [transistor] devices” and thus increase packing density of CMOS semiconductor devices. Ex.1005, Abstract, 1:5-8, 1:51-68, 6:17-21, 6:57-59, 1:9-50; §IX.A.

It would have been obvious to fabricate known flash memory devices using Payne’s improved twin-well CMOS technology for the benefit of increased packing density. Ex.1003, ¶¶206-208. Additionally, using Payne’s technology to form flash memory would have merely amounted to (1) use of a known technique (Payne’s improved twin-well CMOS process) to improve similar devices (known CMOS flash memory designs) in the same way (to increase packing density) and (2) a simple substitution of one known element (CMOS technology for prior art flash memory) with another (Payne’s improved CMOS technology). *Id.* There would have been a reasonable expectation of success with predictable results because Payne’s improved CMOS process was an improvement over conventional twin-well CMOS process and would have been used for its intended purpose in manufacturing a known flash memory designed for implementation using CMOS technology. *Id.*

E. Ground VI

1. Dependent Claim 9: The semiconductor device of claim 7 wherein the semiconductor device is a central processing unit (CPU)."

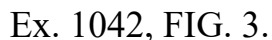
Onoda anticipates or else renders obvious claim 7. §IXB.1. Onoda-Wolf renders obvious the additional limitation of claim 9. Ex.1003, ¶209. As discussed in Section IX.D.1, Wolf discloses microprocessors (CPUs) using CMOS technology. Ex.1008B, 368-370; Ex.1032, 1334 (see "microcomputer"); Ex.1003, ¶¶210-216. As discussed further in Section IX.E.3, a POSITA would have been motivated to combine Onoda with Wolf with a reasonable expectation of success.

2. Dependent Claim 10: "The semiconductor device of claim 7 wherein the semiconductor device is a DRAM device."

Onoda anticipates or else renders obvious claim 7. §IXB.1. Onoda-Wolf renders obvious the additional limitation of claim 10. Ex.1003, ¶217. As discussed in Section IX.D.2, Wolf discloses DRAM devices using CMOS technology. Ex.1008B, 587, 596-597; Ex.1003, ¶218. As discussed further in Section IX.E.3, a POSITA would have been motivated to combine Onoda with Wolf with a reasonable expectation of success.

3. Motivation to combine Onoda and Wolf

According to Wolf, a well-known textbook on semiconductor fabrication, a CMOS device, by definition, has "N-channel MOS [(NMOS)] transistor[s]" and "P-



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Onoda's process for making improved devices containing NMOS and PMOS to Wolf's CPU and DRAM devices using CMOS technology for the benefit of improved latch-up resistance, punch-through breakdown voltage, and junction breakdown voltage. *Id.*

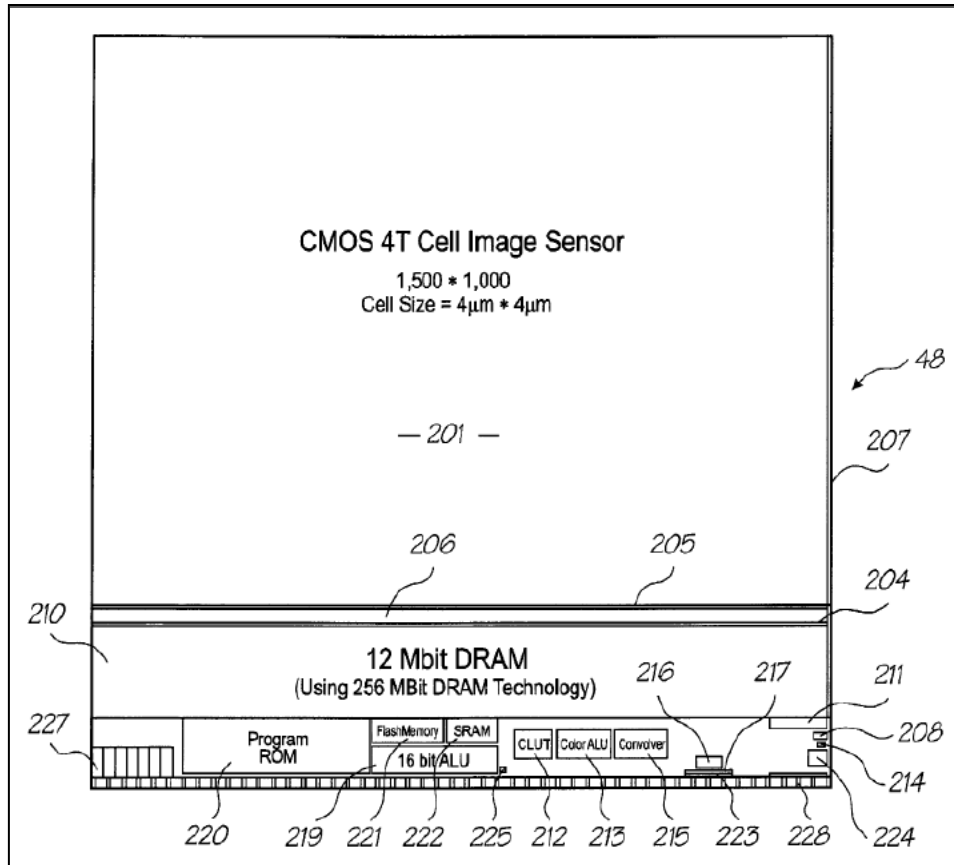
Using Onoda's technology to form CPUs and DRAMs would have merely amounted to (1) use of a known technique (Onoda's process to improve latch-up resistance, punch-through breakdown voltage, and junction voltage) to improve similar devices (known CPU and DRAM designs) in the same way (to make semiconductor devices containing NMOS and PMOS) and (2) a simple substitution of one known element (CMOS technology in prior art CPUs and DRAMs) with another (Onoda's technology with improvement to NMOS and PMOS). *Id.*, ¶221. There would have been a reasonable expectation of success with predictable results because Onoda's process regarding NMOS and PMOS was a known improvement over conventional CMOS process and would have been used for its intended purpose in manufacturing known CPU and DRAM devices using CMOS technology. *Id.*

F. GROUND VII

1. Dependent Claim 12: "The semiconductor device of claim 7 wherein the semiconductor device is an image sensor device."

Payne renders obvious claim 7. §IX.A.1. Payne-Silverbrook renders obvious the additional limitation of claim 12. Ex.1003, ¶¶222-224.

Payne teaches an improvement on “twin tub” (twin-well) CMOS technology to reduce separation “between source and drain regions of adjacent [transistor] devices” and thus increase packing density of CMOS semiconductor devices. Ex.1005, Abstract, 1:5-8, 1:51-68, 6:17-21, 6:57-59, 1:9-50; §IX.A. Silverbrook discloses a CMOS image sensor device. Ex.1047, 6:41-13:39. An example of such an image sensor device from Silverbrook (called “Image Capture and Processing Chip (ICP)”) is pictured below.



Ex.1047, FIG. 15. Silverbrook’s ICP includes “CMOS logic, a CMOS image sensor, DRAM, and analog circuitry.” *Id.*, 6:56-57; Ex.1003, ¶223.

It would have been obvious to fabricate known CMOS logic or CMOS image

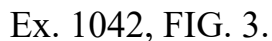
sensors in Silverbrook's ICP using Payne's improved twin-well CMOS technology for the benefit of increased packing density. Ex.1003, ¶224. Additionally, using Payne's technology to form CMOS logic or CMOS image sensors would have merely amounted to (1) use of a known technique (Payne's improved twin-well CMOS process) to improve similar devices (known image sensor device designs) in the same way (to increase packing density) and (2) a simple substitution of one known element (CMOS technology for prior art image sensors, as disclosed in Silverbrook) with another (Payne's improved CMOS technology). *Id.* There would have been a reasonable expectation of success with predictable results because Payne's twin-well CMOS process was a known improvement over conventional twin-well CMOS process and would have been used for its intended purpose in manufacturing known image sensors, designed for implementation using CMOS technology. *Id.*

G. GROUND VIII

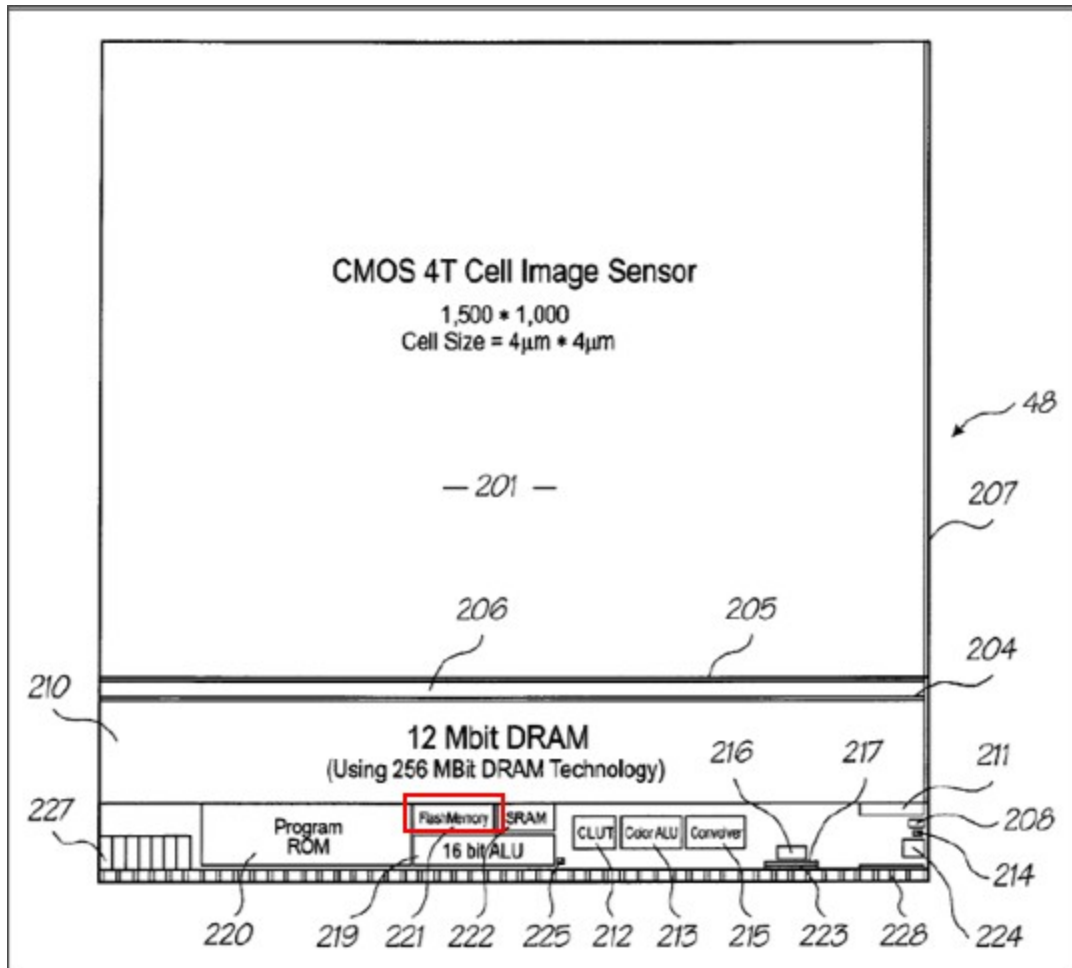
1. Dependent Claim 12: "The semiconductor device of claim 7 wherein the semiconductor device is an image sensor device."

Onoda anticipates or else renders obvious claim 7. §IXB.1. Onoda-Silverbrook renders obvious the additional limitation of claim 12. Ex.1003, ¶¶225-230.

Onoda discloses N-channel MOS (NMOS) transistors and P-channel MOS



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Ex.1047, FIG. 15; Ex.1003, ¶227.

It would have been obvious to use Onoda's flash memory as the flash memory used in Silverbrook's ICP. Onoda teaches that "[a] flash memory that is structured as described [in Onoda] has advantages," Ex. 1042, [0085], resulting from "reducing the tendency for latch-up and for punch-through" and "increasing the junction breakdown voltage." *Id.*, [0018]-[0028]. Because Silverbrook does not include any details about the fabrication of the flash memory, a POSITA would have been motivated to implement the flash memory manufacturing process disclosed in

Onoda, given its disclosed advantages. Further, a POSITA would have had a reasonable expectation of success in doing so because a flash memory is a common type of storage medium that can be used in various electronic devices. The flash memory is part of Silverbrook's image sensor device (*i.e.*, ICP), and therefore the use of Onoda's flash memory in Silverbrook's ICP meets the added limitation of claim 12. Ex.1003, ¶228.

Besides the flash memory, a POSITA would have been motivated to use Onoda's manufacturing process to make the CMOS logic or CMOS image sensor in Silverbrook's ICP. A CMOS device, by definition, has "N-channel MOS [(NMOS)] transistor[s]" and "P-channel MOS [(PMOS)] transistors." Ex.1008A, 807-09; *see also* Ex.1008B, 368 ("Complementary MOS (CMOS) is so-named because it uses both p- and n-type (complementary) MOS transistors in its circuits."). Though Onoda does not explicitly refer to a CMOS device, a POSITA would have recognized from Onoda's disclosure that its devices are CMOS devices. Ex.1003, ¶229. But regardless of whether Onoda's devices are CMOS, a POSITA would have been motivated to apply Onoda's process for making improved devices containing NMOS and PMOS to Silverbrook's CMOS logic or CMOS image sensors for the benefit of improved latch-up resistance, punch-through breakdown voltage, and junction breakdown voltage. *Id.*

Using Onoda's technology to form CMOS logic or CMOS image sensors

would have merely amounted to (1) use of a known technique (Onoda’s process to improve latch-up resistance, punch-through breakdown voltage, and junction voltage) to improve similar devices (known image sensor device designs) in the same way (to make semiconductor devices containing NMOS and PMOS) and (2) a simple substitution of one known element (CMOS technology for prior art image sensors, as disclosed in Silverbrook) with another (Onoda’s technology with improvement to NMOS and PMOS). *Id.*, ¶230. There would have been a reasonable expectation of success with predictable results because Onoda’s process regarding NMOS and PMOS was a known improvement over conventional CMOS process and would have been used for its intended purpose in manufacturing known image sensors, designed for implementation using CMOS technology. *Id.*

X. THE BOARD SHOULD INSTITUTE IPR

The Board should decline to exercise its discretion to deny institution for several reasons.

A. 35 U.S.C. § 314(a)

In *Apple Inc. v. Fintiv, Inc.*, the Board enumerated six factors that it will assess in determining whether to exercise discretion to deny institution under §314(a) based on co-pending litigation. IPR2020-00019, Paper 11 at 2-3 (PTAB “precedential” Mar. 20, 2020). The USPTO issued updated discretionary denial guidance in view of the *Fintiv* factors and confirmed that “the PTAB will not

discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB.”

See June 21, 2022 Memorandum to Members of the PTAB, 3 (available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf). Here,

Petitioner has eliminated any risk of duplicated effort by voluntarily presenting a *Sotera* stipulation to Patent Owner. EX1101; *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020). For at least this reason, and considering the compelling merits of the above-detailed Grounds, discretionarily denial is unwarranted and would be unjust.

B. 35 U.S.C. § 325(d)

The Board should likewise not deny institution under §325(d) because neither prong of the two-part *Advanced Bionics* framework is satisfied. See *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019- 01469, Paper No. 6 at 8 (P.T.A.B. Feb. 13, 2020) (precedential). Under that framework, in evaluating discretionary denial arguments under §325(d), the Board looks to “(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied,

whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Id.*

In applying this test, the PTAB considers the “*Becton, Dickinson*” factors.¹⁰ Among these are “the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection,” *Becton, Dickinson*, Paper No. 8 at 17-18; *see also Edwards Life Sciences Corp. v. Colibri Heartinvalve, LLC*, IPR2020-01649, Paper No. 8 at 20-21 (P.T.A.B. Mar. 26 2021) (declining to exercise discretionary denial where prior art references were not substantively considered during prosecution). Here, none of the ground references (Payne, Onoda, Wolf, and Parrillo) is cited art, and the arguments presented herein were not considered during prosecution of the ’502 Patent.

Payne and Onoda are not cumulative with the Rhodes cited art – In its POPR to the terminated IPR2022-00290, PO argued that Payne is cumulative with Rhodes on the alleged ground that the nested well structure of Payne is nothing more than a single well formed with multiple implants. Ex.1016, 25-41. This is incorrect.

First, Figure 2 of Onoda expressly discloses forming P-type well regions (105a through 105c) and N-type well regions (103, 106a through 106c) in a lightly-

¹⁰ *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (Dec. 15, 2017) (precedential as to § III.C.5, first paragraph) (“*Becton, Dickinson*”).

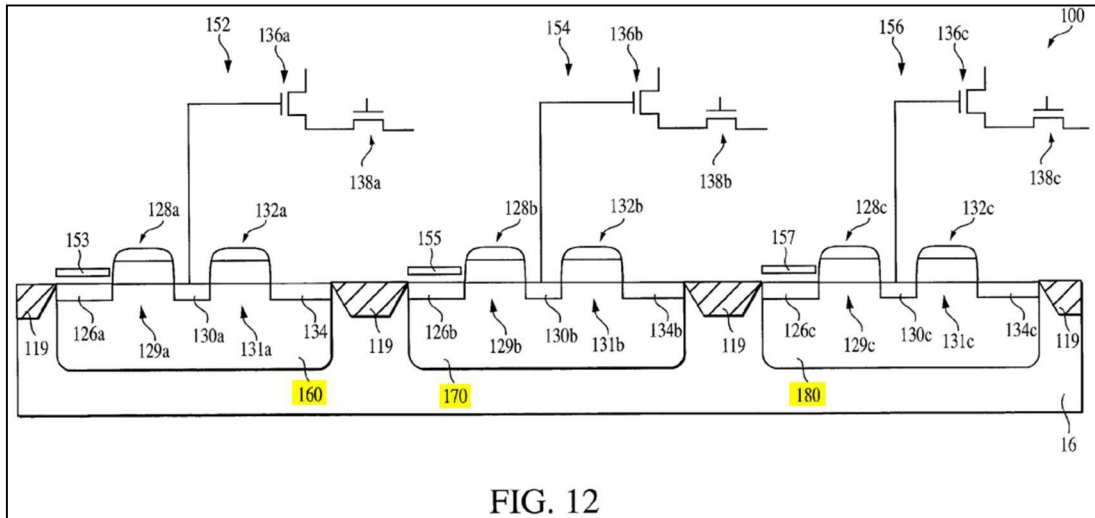
doped semiconductor layer 102 that is formed through epitaxial deposition. Ex.1042, FIG. 2. Thus, Onoda's well regions and the semiconductor layer 102 are formed through processes that are distinct from those disclosed in Rhodes. Ex.1003, ¶¶231-232.

Second, Payne's nested-well structure, in which shallow wells are formed in deeper wells with *separate* implants *and* annealing steps, differentiates Payne from Rhodes which does not teach a nested-well structure. Ex.1003, ¶¶233-234. As Payne describes and illustrates in Figures 2 and 5-9, the deep wells ("tub regions") of Payne's nested well structure are formed first, using their own specific masks, ion implantation and thermal drive-in process steps. Ex.1005, 3:17-4:30. The shallow wells ("surface regions") are then separately formed, using different masks, ion implantation and thermal drive-in process steps. Ex.1005, 4:31-5:17, 5:44-55. Payne's separately formed deep and shallow wells, such as wells 15 and 18, are not a single well formed using multiple implants. *Id.*

Third, a POSITA would have understood Payne's tub and surface regions to constitute distinct wells. Ex.1003, ¶¶235-236. That understanding is consistent with Sakai, which uses separate implants and annealing steps to form each well of its nested well structure and uses the term "well" to refer to distinct wells. Ex.1006, 5:56-6:4, 6:24-28, 6:52-58, FIGS. 10A, 10B.

In contrast to Payne, Rhodes teaches a twin-well architecture with side-by-

side wells 160/170/180 (indicated in highlight below) that Payne and Sakai seek to improve upon with their nested-well structure. Ex.1011, [0064]; Ex.1005, 1:24-68; Ex.1006, 1:6-2:39.



Ex.1011, FIG. 12, [0064]. Rhodes does not mention or suggest (in paragraph [0064] or otherwise) forming a nested-well structure, and thus does not teach a “well region disposed in [a] single drift layer.” Ex.1003, ¶¶237-238. This was the reason the Examiner allowed the claims to issue over Rhodes (and other art, including Kamins and Jastrzebski). Ex.1046, 346. Nowhere in the prosecution did the Applicant or Examiner discuss nested well structures, as Payne discloses. Thus, there is no support for PO’s argument in the POPR that “it is reasonable to infer that the Examiner agreed with the argument Patent Owner makes explicitly herein that a multiple-implant well does not disclose a well region disposed in a single drift layer.” Ex.1016, 27; Ex.1003, ¶¶240-242.

PO also implied in its POPR that the Applicant overcame Rhodes-based

rejections during prosecution of the parent '195 Patent by adding the “drift layer” limitation to the pending claims. Ex.1016, 22-24. This is incorrect. Applicant overcame Rhodes-based rejections on the basis that Rhodes is a “CMOS imaging device,” and by amending claims to include a “graded dopant concentration in the ... active channel regions” (a limitation that was later removed). Ex.1046, 94-96. The “drift layer” limitation was added much later in the process after several intervening rejections. There is no indication the Examiner specifically considered Rhodes in relation to the “drift layer” limitation, let alone the “well region disposed in said single drift layer” limitation. Ex.1003, ¶239.

C. Prior Terminated Petitions Do No Warrant Denying Institution

The instant Petition is Petitioner’s first petition challenging claims of the ’502 Patent. Petitioner is not a related company to those who have previously challenged the ’502 Patent. None of the prior challenges to the ’502 Patent reached an institution decision. In addition, Petitioner is a defendant in the District Court Case, and Petitioner would potentially be severely prejudiced if this Petition is not instituted. *Apple Inc. v. Uniloc 2017 LLC*, IPR2019-01667, Paper No. 7, 11-12 (P.T.A.B. Apr. 21, 2020). In light of the foregoing, *General Plastic* factors weigh strongly against discretionary denial. *Xilinx, Inc. v. Arbor Global Strategies, LLC*, IPR2020-01568, Paper No. 12 at 10 (P.T.A.B. Mar. 5, 2021).

Petition for *Inter Partes* Review of U.S. Patent No. 9,190,502

Respectfully submitted,

Dated April 10, 2024

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter partes* Review totals 13,027 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated April 10, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on April 10, 2024, a complete and entire copy of this Petition for *Inter partes* Review, Power of Attorney, and all supporting exhibits were provided by Express Mail, to the Patent Owner, by serving the correspondence address of record as follows:

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