PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : H04B 1/00, 7/00, G06F 7/00 H04B 14/04

A1

(11) International Publication Number: WO 90/06633

(43) International Publication Date: 14 June 1990 (14.06.90)

(21) International Application Number: PCT/US89/05579

(22) International Filing Date: 8 December 1989 (08.12.89)

(30) Priority data:

283,425	9 December 1988 (09.12.88)	US
282,819	9 December 1988 (09.12.88)	US
283,534	9 December 1988 (09.12.88)	US
282,402	9 December 1988 (09.12.88)	US
282,008	9 December 1988 (09.12.88)	US
283,427	9 December 1988 (09.12.88)	US
282,406	9 December 1988 (09.12.88)	US
283,140	9 December 1988 (09.12.88)	US
282,417	9 December 1988 (09.12.88)	US
283,428	9 December 1988 (09.12.88)	US
283,554	9 December 1988 (09.12.88)	US
283,426	9 December 1988 (09.12.88)	US
282,792	9 December 1988 (09.12.88)	US
283,549	9 December 1988 (09.12.88)	US
282,410	9 December 1988 (09.12.88)	US

(60) Parent Applications or Grants
(63) Related by Continuation

US	283,425 (CIP)
Filed on	9 December 1988 (09.12.88)
US	282,819 (CIP)
Filed on	9 December 1988 (09.12.88)
US	283,534 (CIP)
Filed on	9 December 1988 (09.12.88)
US	282,402 (CIP)
Filed on	9 December 1988 (09.12.88)
US	282,008 (CIP)
Filed on	9 December 1988 (09.12.88)
US	283,427 (CIP)
Filed on	9 December 1988 (09.12.88)
US	282,406 (CIP)
Filed on	9 December 1988 (09.12.88)
US	283,140 (CIP)
Filed on	9 December 1988 (09.12.88)
US	282,417 (CIP)
Filed on	9 December 1988 (09.12.88)
US	283,428 (CIP)
Filed on	9 December 1988 (09.12.88)
US	283,554 (CIP)
Filed on	9 December 1988 (09.12.88)
US	283,426 (CIP)
Filed on	9 December 1988 (09.12.88)
US	282,792 (CIP)
Filed on	9 December 1988 (09.12.88)
US	283,549 (CIP)
Filed on	9 December 1988 (09.12.88)
US	282,410 (CIP)
Filed on	9 December 1988 (09.12.88)

(71) Applicant *(for all designated States except US)*: DALLAS SEMICONDUCTOR CORPORATION [US/US]; 4350 Beltwood Parkway South, Dallas, TX 75244 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)* : LEE, Robert, D. [US/US]; 916 Linwood, Denton, TX 76201 (US). DIAS, Donald, R. [US/US]; 2217 Via del Norte, Carrollton, TX 75006 (US). MOUNGER, Robert, W. [US/US]; 4280 Trinity Mills Road, 143507, Dallas, TX 75252 (US). BOLAN, Michael, L. [US/US]; 6214 Misty Trail, Dallas, TX 75248 (US). HEPTIG, John, Patrick [US/US]; 7000 Treehaven, Fort Worth, TX 76116 (US). KURKOWSKI, Hal [US/US]; 4208 West Creek Drive, Dallas, TX 75252 (US). KLUGHART, Kevin, M. [US/US]; 3721 Spring Valley Road, 143131, Dallas, TX 75244 (US).

(74) Agent: GROOVER, Robert, III; Worsham, Forsythe, Sampels & Wooldridge, 2001 Bryan Tower, Suite 3200, Dallas, TX 75201 (US).

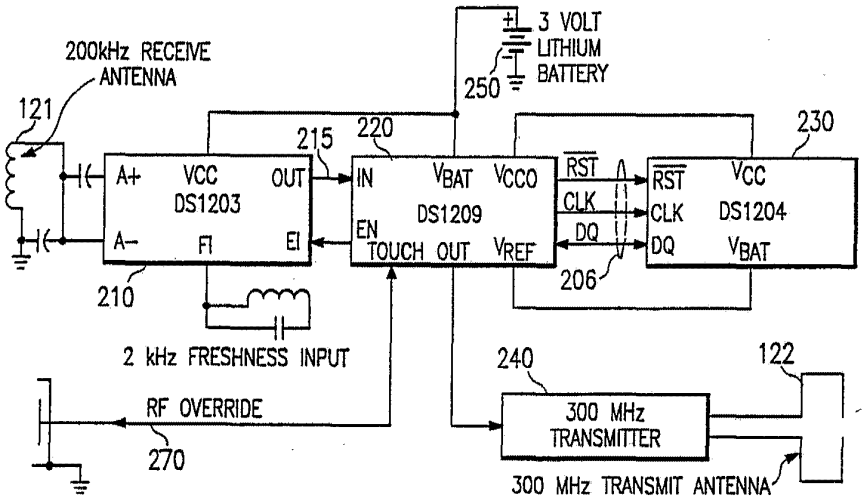
(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), ES (European patent), FR (European patent), GB (European patent), IT (European patent), JP, KR, LU (European patent), NL (European patent), SE (European patent), US.

Published
With international search report.

(54) Title: MICROPOWERED RF DATA MODULES

(57) Abstract

A low-power wireless data communication system, in which base stations (110) can automatically interface to batter-powered portable data modules (210) as they are brought within range. In the data modules (210), each receive antenna (121) is directly connected to a gain-controlled comparator (420A, 420B). Bandpass filtering (448) is accomplished economically by use of simple digital circuits. The two-level digital output from the comparator (420A, 420B) is fed (through an intersymbol detector, a counter, and a ripple-through magnitude comparator) to a state machine (552), which decodes the resulting digital waveform to a conventional serial-bus format. The internal data bus (701D) provides an interface to memory chips (262) and (optionally) to other chips, such as an electronic key. The decoder chip (220) also provides a secondary power supply to the other chips (230), and modulates the power supply (250) to assist detection of transitions on the reset-bar line of the serial bus (206). The modules (230) use widely different frequencies for read and write operations. (Transmissions by the base station (110) use a pulse-width modulation scheme where the most commonly used signals correspond to the shortest pulse. A "read" command is encoded as the same pulse width as one of the two write commands). In addition, a pair of touch contacts (270) can be used to override the RF link. Error-checking (Fig. 7E) is performed on incoming commands before memory access (260) is permitted. "Freshness seal" logic (510) prevents any battery drain until the module is initially turned on (by placing it in a strong field).



GOOGLE EXHIBIT 1008

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	ES	Spain	MG	Madagascar
AU	Australia	FI	Finland	ML	Mali
BB	Barbados	FR	France	MR	Mauritania
BE	Belgium	GA	Gabon	MW	Malawi
BF	Burkina Fasso	GB	United Kingdom	NL	Netherlands
BG	Bulgaria	HU	Hungary	NO	Norway
BJ	Benin	IT	Italy	RO	Romania
BR	Brazil	JP	Japan	SD	Sudan
CA	Canada	KP	Democratic People's Republic of Korea	SE	Sweden
CF	Central African Republic			SN	Senegal
CG	Congo	KR	Republic of Korea	SU	Soviet Union
CH	Switzerland	LI	Liechtenstein	TD	Chad
CM	Cameroon	LK	Sri Lanka	TG	Togo
DE	Germany, Federal Republic of	LU	Luxembourg	US	United States of America
DK	Denmark	MC	Monaco		

MICROPOWERED RF DATA MODULES

BACKGROUND AND SUMMARY OF THE INVENTION

The present invention relates to wireless data interface systems, and to portable data modules for use within such a system, and to power-efficient integrated circuits.

Systems which can provide short-range wireless data communication between a base station and a portable low-power module have recently been the subject of development efforts by a number of groups. Such systems can be extremely useful in many contexts, such as control of personnel access to secure facilities, medical monitoring of inpatients, automated livestock management, automated manufacturing generally, inventory control, theft control, and others described below.

There are many uses for low-powered RF receivers, in such systems and elsewhere. Due to the legal constraints of spectrum allocation, many short-range data links must use extremely small RF signal levels. Moreover, in many cases the transceivers used for such communication must operate with minimal power drain, including minimal standby power.

It is very difficult to satisfy the objectives of low power consumption while also providing adequate sensitivity and noise rejection.

However, such a system is subject to many constraints. If the portability of the portable stations is to be maximized, the battery weight must be small. This means that the power consumption of the portable module - in active or in standby mode - must be exceedingly low. Moreover, many possible applications are highly cost-sensitive.

In most applications, rechargeable batteries are not suitable for a power supply. Rechargeable batteries not only impose a user burden (to perform recharging), but also tend to have electrical characteristics which may be dependent on the discharge/recharge history of the particular battery. Many possible applications cannot tolerate such uncertainty, and require a degree of reliability which demands a very conservative approach to power supply design and rating.

Greater noise immunity can be achieved by using high transmitter power, by by using large, highly directional, and/or highly resonant antennas (which provide "antenna gain"), or by using narrow-bandwidth filtering (or more sophisticated signal processing operations) in the receiver (which provide "processing gain"). However, due to the constraints on the total power budget in a portable data module, and due to the legal constraints mentioned above, higher transmitter power is often not an option. Moreover, directional antennas are also impractical for many systems. Moreover, processing gain is also not free: processing gain is most easily achieved by precise knowledge of the characteristics of the expected signal, and/or by extensive computing operations on the recovered signal. Precise knowledge of signal characteristics tends to require precise knowledge of time and/or frequency, and maintaining this knowledge also consumes power. Thus, adding processing gain into a portable data module not only increases the capital cost, but also places an additional burden on the power budget. Thus, while successive engineering improvements can provide some increase in noise immunity, the room for improvement is inherently limited.

The result of these constraints is a severe squeeze on the system designer: sensitivity must not be too low, and the immunity to electrical noise must be good, and the power consumption must be very low. Such systems may sometimes need to operate in high-noise environments, and such environments may completely block the communications channels. In a micropowered system, where the transmitter powers may be of the order of a few milliWatts to a few Watts, noise sources may sometimes provide an RF power level, at the receiver, within the reception band, which is comparable to the power level provided by the transmitter. For example, in manufacturing environments, extremely high broad-band noise levels may be generated by arc welding (or arc furnaces), by plasma deposition processes, by large motors, or by digitally controlled actuators. In such applications, it would obviously be undesirable for the wireless data link to shut down when an extended period of high noise occurs. For another example, in a military system which controls entry to secured-access facilities, it would obviously be unacceptable for the access control system to shut whenever a high level of electrical noise occurred, e.g. due to high-powered radar or communications activities. Therefore, for system "robustness," it is highly desirable that such systems should be able to operate under high-noise conditions.

In many such applications, the size and weight of the portable module is an extremely sensitive issue. A module which is merely transportable will not suffice. For example, pagers and portable radios have often had weights of 10 ounces or more, and volumes of 10 cubic inches or more. If modules of this size were used (for example) for patient identification in a hospitals, the patients would unload such cumbersome objects as quickly as possible, by any means possible. Similarly, in many applications such large modules could not be used for inventory control, since there would be no convenient place to put them, and they would easily be damaged (or personnel would learn to bypass them).

The need to conserve power actually implies several separate constraints: the consumption requirements of both the active and the

standby mode must be separately minimized, and the issues to be considered are somewhat different.

The most difficult issues are presented by the standby mode. The portable module cannot afford the power to continually broadcast a beacon, but, even if the base station module broadcasts a beacon to ascertain the possible presence of receiver modules, the power requirements of listening for such a beacon are large.

Suppose, for example, that a portable data module, with non-rechargeable batteries, is desired to have a lifetime of at least 10 years, and to be able to perform at least 1,000,000 data transactions during its lifetime. (This is an extremely aggressive set of specifications, and is believed to be far beyond the capabilities of any system presently available.) Suppose further that the available battery energy is 2000 Joules (1 milliAmpere for 190 hours at 3 Volts). Then the power dissipation in the standby mode must be no more than several millionths of a Watt, or all of the battery energy will be dissipated merely in waiting for the active communication transactions to begin, before the design lifetime has expired. The present application discloses several novel teachings which are directed to this aspect of power conservation.

The power efficiency requirements of battery-powered modules can be extremely stringent. For best reliability, neither battery recharging nor user detection of imminent failure should be relied on. Therefore, to reliably meet the design battery lifetime of a module, extreme care must be taken to identify and control the worst-case battery-drain scenarios.

Battery lifetime management can be particularly difficult where several complex integrated circuits are included in a battery-powered module. Where significant control interactions, or even data exchange, may occur, the demands of such transactions must also be allowed for.

Some previously proposed methods for implementing such wireless-access data systems have used passive components for RF detection, connected so that the RF power received from the base station can actually provide the necessary power to operate the remote module. Such

systems require that the RF power level at the receiver must be far higher than would be needed merely for communication.

Power conservation also affects the choice of coding scheme. The energy per bit of data successfully sent to the base station, and per bit of data correctly received from the base station, must both be minimized under the conditions actually expected (including distance from remote to base module, RF noise level, and the lengths of data streams which typically need to be handled).

A systems which provides a wireless data-transfer interface to portable data modules has the potential for great flexibility. However, the high-level organization of such a system must also be considered carefully. The communications protocols often assign the base station to be the master station. In such a typical configuration of this kind, each base station (unless passwording prevents this) can query, read, and write data to any portable module which may happen to be in range, without any independent action at the remote module.

A large system of this kind presents issues of access collision. If a large number of modules are within a base station's range, the base station may receive responses from many portable modules when it broadcasts a query signal. Each module has a "name" by which it can be addressed separately, but the use of module identifiers does not remove all problems: if a large number of modules may be present in the total system, the time for a base station to query the possible module identifiers may be large.

Modern semiconductor technology has provided solid-state memories with such low standby power requirements that a single coin-sized battery can power the memory for ten years of lifetime or more. Such memories are already commercially available. However, if a high volume of such memory could be used in a portable wireless-accessible module, the functionality of such modules could be tremendously increased. However, presently available techniques tend to lead to low maximum data rates. With the constraints discussed above, this means that, while it is easy to

accumulate a large volume of data, it is not so easy to download that data. However, for many applications it would be quite desirable to be able to perform a block "dump" of memory.

Error-check-and-correct protocols are commonly used to preserve data integrity. However, in a wireless data communication system, which inherently has a high exposure to noise, one important class of error must be carefully avoided: if a write were to be directed to the wrong location in the module's memory, data integrity would be lost, even though the error checkbits for the data stream all indicated that no error had occurred.

Multiport Memory

As is well known to those skilled in the art of computer system architectures, multiport memories are a very useful basic tool. A "multiport" memory is one in which different computer processes can independently access a common memory space, through hardware channels which are at least partly separate. Multiport memories are generally useful for flexible buffering of data transfers. For example, they can be used to pass data between two processes which are independently clocked, or clocked at different frequencies.

The most straightforward way to achieve multiport functionality is by using memory chips which actually have independent data paths to each cell. (For example, a two-port SRAM of this type would have two pairs of pass transistors in each cell, and would be connected to two wordlines (one for each of the pass transistor pairs), and would also be connected to two bitline pairs. However, this approach does not scale well as the number of ports increases.

An alternative approach to multiport memory is to use a simple memory array (e.g. single-ported or dual-ported), with memory controller logic which arbitrates access to the array. (The memory controller logic may be on a separate integrated circuit, or may be integrated with the memory cells.) In such architectures, it may sometimes be necessary for

a port to wait until access is available, but the multiport functionality can still be achieved.

Adjusting analog circuits

The closed-loop gain of an amplifer gain stage is normally adjusted using a resistor ratio. (That is, when a feedback resistor R_F is interposed in the feedback path from the output terminal to the negative input terminal of a differential amplifier, and an input resistance R_{in} is interposed between the negative input terminal signal and an incoming signal V_{in}, the voltage gain V_{out}/V_{in} will be equal to the ratio of the resistances $-R_F/R_{in}$.)

Many methods are known for trimming resistor values, to adjust the closed-loop gain of an amplifer. Such trimming methods will typically involve applying a laser beam to reduce the linewidth of a thin-film or thick-film resistor.

Closed-loop amplifier stage gain values are adjusted, in some embodiments of the invention, by selecting components which have values scaled in powers of two. For example, if the smallest available value of the feedback resistor is $R_{f,0}$, thin film (polysilicon) resistors would be provided with values of $2R_{f,0}$, $4R_{f,0}$, $8R_{f,0}$, etc. Similarly, if the smallest available value of the input resistor is $R_{in,0}$, then additional resistors would preferably be provided with values of $2R_{in,0}$, $4R_{in,0}$, $8R_{in,0}$, etc. (Note that the minimum resistor values $R_{f,0}$ and $R_{in,0}$ do not have to be equal.) This provision of selectable digital increments means a desired closed-loop gain can be "dialed in" directly, by translating a desired ratio into two binary numbers.

The presently preferred embodiment provides such digitally scaled values not only for resistors, but also for capacitors. The trimmable resistors and capacitors are adjusted to set both the center frequency and Q of a bandpass filter. The mathematical relations which define the center frequency and Q of an active RC filter as a function of the component values used are very well known to those skilled in the art.

However, the use of digitally scaled selectable components, so that the desired component values can be directly "dialed in," is believed to be new in the art.

As is well known to those skilled in the art, the value of a thin film resistor can be changed by changing the width/length ratio of a layer of a given sheet resistance, by changing the film thickness of a material of a given resistivity, by modifying the thin film layer so that it has a different sheet resistance (e.g. implanting it with a dopant), or by substituting a material with a different sheet resistance. The preferred embodiment simply uses pattern modifications, to provide a variety of width/length ratios. This idea is particularly useful where high-gain amplifer stages may be needed.

Filtering

Filtering electrical signals is one of the most basic operations in electronics. Typically filtering functions will be defined with reference to the frequency domain. For example, if a complex signal is passed through a "low-pass" filter, only those signal components which are below a certain frequency will pass through the filter. Similarly, a "bandpass" filter will pass only those signal components which are within a range of frequencies around a center frequency. (The "bandwidth" of a bandpass filter specifies how wide this range of frequencies is.) The filtering characteristics of an electrical circuit will be determined by the values and interconnections of the active and passive components used.

A filtering characteristic may be implemented in a wide variety of ways. The different possible implementations can differ in many respects. For example, where active devices are part of the filter, the power consumption of different implementations may vary. The sharpness of the boundaries between the passband and stopband may also vary. (For example, a very simple passive filter, which includes only one capacitor and one inductance in series, will typically have a slope of about 6 dB per octave at the passband edges. Thus, the wider the passband, the less

sharp the passband edges will be. For many applications a sharper slope is needed. More complex circuits can provide much sharper slopes.) Different implementations may also differ in their area requirements, sensitivity to parameter variation, passband ripple, maximum attenuation, insertion loss, practicable frequency range, etc.

Digital signal processing ("DSP") can be used to readily implement a very wide variety of filter functions. However, unless the system design already includes a microprocessor or specialized DSP unit, and digital/analog and analog/digital converters, a substantial amount of hardware must be added before DSP techniques can be used. Moreover, DSP is likely to consume relatively large amounts of power, and may generate significant amounts of electrical noise.

Battery-backed Microprocessor

In addition, microprocessors which can operate on extremely low power are also now available. An important example is the DS5000, available from Dallas Semiconductor Corporation, Dallas, Texas. (This chip, and its description in the data books of Dallas Semiconductor Corporation, are hereby incorporated by reference.) This microprocessor can operate with very low power consumption in active and standby modes. The power consumption is so small that this microprocessor can be used in an extremely compact module powered by a very small lithium battery, and still have good operating lifetime.

Such microprocessors can be useful in a very wide variety of applications, and it would be very useful to be able to make use of them in a portable wireless data module. The present invention provides a system architecture, for a "smart" portable wireless module, in which a large volume of memory space is shared by a microprocessor (or other complex chip) and by the demands of wireless access.

It should be noted that microprocessors are not the only type of integrated circuit which the present invention helps to integrate into a

portable data module. Different chips (and/or multiple chips) can be used. For example, display drivers can also be connected to memory through a high-data-rate internal bus. For another example, customized signal processing chips, adapted to functions such as speaker identification, can also be used. More exotic chip types, such as neural networks or cellular automata, can also be used (in suitably low-power versions).

It should also be noted that the disclosed novel memory controller is not applicable only to portable modules, nor even to low-power applications generally. The innovative teachings herein can provide improved access arbitration between serial and parallel ports, wherever a multiport interface to serial and parallel ports is used. Thus, for example, this controller architecture could also be used in much higher-data-rate environments.

Error-check-and-correct protocols are commonly used to preserve data integrity. However, in a wireless data communication system, which inherently has a high exposure to noise, one important class of error must be carefully avoided: if a write were to be directed to the wrong location in the module's memory, data integrity would be lost, even though the error checkbits for the data stream all indicated that no error had occurred.

The presently preferred embodiment provides an architecture wherein a substantial amount of random-access memory (RAM) is included in the remote module. This presents data-integrity problems which are quite different from those presented by the more common use of a small amount of memory: if an error occurred in the address field, during a write to the RAM, data could be lost. To ensure data integrity, a serial access protocol is used to control wireless accesses. Since the data rate of wireless access is rather slow, a special command is added to this protocol to accelerate access arbitration between wireless accesses to memory and the higher-bandwidth internal accesses.

As described in detail below, the memory controller chip of the presently preferred embodiment provides dual-port access to single-port

memory, where one of the two ports is serial and one is parallel. In the presently preferred embodiment, an arbitration byte is used to avoid conflicts between the two ports. (Some bits of the arbitration byte can be written only by the serial port, and some bits can be written only by the parallel port.) In the presently preferred embodiment, the serial port always has priority for access to the memory. Normally, in a multiport memory organization of this kind, the serial port would read, write, read the arbitration byte to check for no access collision. However, due to the overhead imposed by the 56-bit access protocol used in the presently preferred embodiment, such a series of accesses would require 192 serial bits (56+8 + 56+8 + 56+8), which is slow. Instead, the present invention uses a special protocol (for this purpose only), which compresses the normal serial access protocol so that the serial port will read 8 bits (of the arbitration byte), write 8 bits, and read 8 bits, within a single access. Thus, instead of 192 bits of overhead, only 80 (56 + 8 + 8 + 8) are required.

For long lifetimes, a prime determinant of the lifetime is the power consumption when the integrated circuit is idle. For example, even a few microAmperes of standby current will exhaust a 2000-Joule battery within a ten-year lifetime. Various design techniques can be used to reduce standby current, but the system designer can readily find other uses for any excess battery capacity. (For example, other functions may be added, or longer lifetimes specified, or smaller batteries used.) Since standby power consumption is a significant factor in design lifetime, the design lifetime must normally be dated from the time when standby power consumption begins.

This is generally undesirable. The customer needs to know the lifetime from the time when he gets the part. To provide customers with this assurance, the manufacturer and distributors must therefore control the distribution chain so that the maximum time in inventory is known, and the design lifetime for the part must be reduced to allow for this maximum time in inventory. This is inconvenient.

Moreover, in some applications a long inventory time is highly desirable. For example, in military or industrial applications it might be useful to keep a stock of "field spares" on hand, very close to the actual installation, so that a failed electronic module could be rapidly replaced.

The present invention provides a way to totally inactivate (or reactivate) a sealed integrated circuit module, without using any mechanical elements which might fail, or using any electrical contacts which might burden the hermeticity of the module packaging.

The present invention provides a micropowered module containing one or more integrated circuits and a battery. The module is originally in a state of zero power consumption. When the module is to be put into use, a very strong electromagnetic field is applied at a predetermined frequency. (For example, the user can hold the module between the poles of a C-shaped solenoid which is being driven by a significant current at the appropriate frequency.) A very small and simple antenna is used to receive this energy. The output of this antenna is, in the presently preferred embodiment, connected directly to the input of MOS logic gates, so that no current flows unless the incoming signal reaches a high enough voltage to switch the MOS transistors. A preset pulse code at this frequency will be detected by subsequent logic elements, and will change the status of a stored bit which identifies whether the integrated circuit should be turned off (i.e. in "sleep" mode) or on. (While the integrated circuit is on, it may be in active or standby mode. This is determined by other logic, and is separate from the operations described.) In standby mode, the power from the battery will avoid data loss.

The lithium batteries preferably used have a very long shelf life, so that the time when the module is in sleep mode does not subtract from the design lifetime. Thus, the manufacturer can ship modules which are in sleep mode, and the customer (or distributor) can activate the modules when they are nearing use.

Only one chip in a module normally needs to have this sleep and wake capability. This chip can provide a control signal or a power supply output to the other chips accordingly.

In the presently preferred embodiment, the wireless "freshness seal" command can be used to command the module to wake up or to command it to go back to sleep. Thus, a user who foresees a long idle time for a module can cause the module to go back into a zero-power-consumption mode until needed.

The present invention is particularly advantageous in a wireless-access data module, since the module can be made totally hermetic. However, this wireless freshness seal is also advantageous in other module configurations too. The lack of external switches or contacts improves the reliability of the module. Moreover, the fact that the freshness seal switching is not readily apparent may prevent unsophisticated users from inadvertently activating it, and losing functionality or stored data.

Of course, a wide variety of engineering techniques can be used to reduce the standby power consumption of integrated circuits. However, the present invention provides a generally applicable architectural innovation, which can be used regardless of what integrated circuit types are used, and regardless of what techniques are used to reduce standby power consumption.

The present application discloses significant architectural innovations which provide improved functionality and power efficiency in a portable data module which can be used for wireless data transfer.

The disclosed innovative teachings enable a portable data module, accessible by wireless communication. The module includes an internal serial data bus, which carries data in a different coding scheme than that used on the wireless channel. The internal data bus connects receiver/decoder chips to one or more memory chips, and to other integrated circuits if desired.

The innovative architecture provides a number of advantages, including architectural flexibility (i.e. the ability to rapidly modify the

module's design to accommodate different functions). For example, it will be seen below that various alternative embodiments may optionally include a dual-port memory controller; an access control chip; a parallel data transfer connector; and various combinations of these.

A further advantage is the ability to include very complex functionality within a battery-powered portable data module. The standardized bus interface permits a very large variety of functions to be easily integrated, including such functions as one or more microprocessors.

A further advantage is the ability to select between alternative communications channels. For example, it may optionally be desirable to be able to select between quite different communications channels, where different hardware is used for different channels. In such applications, the use of the serial bus can permit various custom chips to be included in the module, and powered-up only when needed.

A further advantage is the ability to perform high-bandwidth data manipulations within the portable module. Although the bandwidth of a wireless micropower communication link is normally very limited, the internal serial bus permits a much higher data rate to be used within the module. This can be useful, for example, in applications where sophisticated cryptographic encoding or speech recognition capabilities are used.

Another way to regard the advantages of this memory chip is that it provides internal data communications which are decoupled from the design constraints of the wireless communication link. For example, in the presently preferred embodiment, pulse-width modulation is used on the send-data channel, together with a coding scheme and a data formatting protocol which provides reasonable protection against noise-induced errors. However, the cost of this protection is a fairly low data rate. The internal data bus is not as exposed to noise, and less protection can be accepted to achieve a higher data rate.

The disclosed innovative teachings enable an improved memory controller architecture. Preferably a dual-port memory controller is used,

which interfaces one or more memory chips to both a serial port and a parallel port. The local bus which runs between the controller and the memory chip is defined so that multiple controllers can be stacked together to provide multiport access. Thus, the present invention enables an expandable system in which a memory is addressable by any desired number of serial ports.

Thus, a bank of memory (or other single-port resource) can be efficiently shared by multiple serial ports, even if the shared resource is not directly compatible with serial access protocols.

The disclosed innovative teachings enable a wireless data module which has a backup communication mode. Normally data is encoded into a pair of RF channels to achieve short-range communication, but the portable module also has a pair of touch contacts, which can override the RF link, thus permitting data communication if an RF channel is jammed or if the module's battery goes bad. Preferably the touch contacts do not provide a full digital link, but are used for coded communication, at a frequency different from those used in the normal RF links. This permits isolation elements to be used, so that the touch contacts can be exposed to normal electrostatic discharge levels without destroying any key components of the module. This also permits the touch contacts to be relatively insensitive to the presence of dirt or corrosion.

The disclosed innovative teachings enable a receiver architecture which is not only advantageous in a portable wireless data module, but can also be used in a wide variety of other communications receivers where low power consumption is needed (and particularly where low standby power consumption is needed).

A micropowered RF receiver is provided, which uses a comparator (or comparators) at its input terminals. Preferably no analog gain stages are used, either before or after the comparator, and the comparator's input terminals are directly connected to an all-passive antenna circuit. This provides reasonable sensitivity, but does not consume large amounts of power in the standby mode.

A further subclass of embodiments uses feedback from pulse-counting logic to adjust the gain of the comparator(s) which receive the input.

The length of incoming pulses is measured, in a digital stage of the portable module, by a counter. When this counter reaches a count which is much longer than would be expected from any of the allowed set of symbols, it provides an overflow-indicating pulse to control logic which reduces the bias current supplied to the comparators 420 at the input to the receiver circuits, and thereby reduces the sensitivity of these comparators.

The current source in the input comparators in the receiver circuits is the primary location of standby power dissipation in the presently preferred embodiment. Therefore, the size of this current source is a significant parameter in designing the remote module: if the comparators are redesigned to draw more current, the sensitivity of the receiver circuits will be increased, but the battery lifetime will be decreased. The total charge available in the battery, and the desired design lifetime, set a limit to the current which can be drawn. The minimum current draw is defined by the desired sensitivity of the receiver: the desired minimum sensitivity will dictate a certain level of current to achieve it.

Thus, battery lifetime considerations indicate a maximum size for the current source, but do not indicate a minimum size. Therefore, in this class of embodiments, the channel width of the current source device is divided up between several devices in parallel. For example, where the maximum device width is W, this device width can be allocated into four parallel current-source devices having widths of W/15, 2W/15, 4W/15, and 8W/15. A switching transistor is placed in series with each of these current-source devices, and a four-bit down counter is used as a current-source-control counter. The four output bit lines of the current-source-control counter are each connected to one of these switching transistors, to control one of the current-source devices.

Thus, when the main counter saturates, the current-source-control counter is decremented, and the total channel width of the current sources

in the input comparators of the receiver circuits is reduced. This reduces the sensitivity of the comparators. Pulse counting continues, and if saturation occurs again the receiver sensitivity is decremented again.

A further feature of this class of embodiments is the use of a slow timer circuit to recover from saturation. A simple RC timing circuit with a long time constant (e.g. 1 to 10 seconds) is used to periodically reset the current-source-control counter. This assures that the portable module will be able to rapidly recover from saturation.

All antennas tend to have higher gain in some directions than in others. The directions where gain is maximal are referred to as "lobes," and the directions where antenna gain is zero or minimal are referred to as "nulls." The presence of antenna nulls could cause the portable module to fail to receive signals from the base station, if the portable module's orientation happens to be wrong. To avoid antenna nulls, the wireless data modules may includes two micro-antennas oriented to avoid coincident nulls. However, the RF signals cannot be directly combined, or the two antennas will simply act as one combined antenna, with a new set of possible nulls.

The presently preferred embodiment uses two separate comparators, connected to separate antenna inputs, to detect the presence of an RF signal. One of the two comparators is given preference, but, if no pulses are being detected by the primary comparator, the output of the secondary comparator is monitored. (Thus the two comparator outputs are combined in what is almost an OR relation, except that, once an incoming pulse train has been detected by one comparator, interference by the other comparator is avoided.)

Note that U.S. Patent 4,584,709 to Kneissel et al. discloses a portable radio which switches between multiple antennas until an antenna with adequate signal quality is found. The configuration disclosed in this patent uses separate tank circuits for the two antennas, with PIN diodes used to switch the tank circuits (and therefore the antennas) in and out. Timesharing is used to monitor the signals on the two antennas, to see

which is better, and the signal from the better antenna is connected to the receiver. (By contrast, the presently preferred embodiment does use timesharing in this fashion.)

The disclosed innovative teachings not only significant architectural innovations, which result in improved functionality and power efficiency in the portable data module, but also discloses a complete system architecture and coding protocol which provides substantial advantages.

The present invention provides a communications system which uses a variable-symbol-length coding scheme, such as pulse-width modulation or burst-length modulation. In the presently preferred embodiment, information is encoded (in the RF signal) as variable-duration pulses separated by quiet periods. The length of the pulses is thresholded at several levels, so that each pulse can correspond to one of several symbols. The pulse length thresholds are well separated, so that accurate reception will occur even if the receiver makes some errors in measuring the length of the pulses. (In the detection and decoding circuitry, these variable-length pulses are translated into pulse trains at the carrier frequency.)

The coding used maps the most frequently used symbols onto the shortest pulses. Since the direction of information transfer is defined by overhead bits, the <u>same</u> pulse sequence is used to encode a command of "READ" or of "WRITE 0." (Of course, similar benefits could be obtained, alternatively, by combining the "READ" command with the "WRITE 1" command.) In general, the pulse-width code of the presently preferred embodiment attempts to assign the most frequently used commands to the shortest pulses, to maximize the average baud rate. For example, in the presently preferred embodiment, the symbol for "reset" is the next-shortest symbol after the read and write symbols.

In the presently preferred embodiment, receiver circuits detect an incoming pulse-width-modulated signal, and generate digital pulse trains which are correspondingly burst-length-modulated. These variable-length bursts of constant-width pulses are counted. An intersymbol detector

watches for a minimum silence period, which would indicate that one symbol has ended and another has begun. When an intersymbol silence is detected, the counter total is thresholded against a set of predetermined boundary values, using a ripple-through magnitude comparator. A series of one-bit outputs, showing the results of these comparisons, is then provided as inputs to a state machine. The state machine translates the various pulse length possibilities and drives lines to perform the appropriate action.

The present application not only discloses significant architectural innovations which provide improved functionality and power efficiency in the portable data module, but also discloses a complete system architecture and coding protocol which provides substantial advantages.

As noted, the power consumption constraints on a portable station are exceedingly stringent. In addition to the problems of active power consumption, standby power consumption must also be reduced. That is, over the lifetime of the portable module (which should ideally be years), the portable module may be required to spend tens of thousands of hours in standby mode, where it can detect an incoming query from a base station.

This difficult constraint also has implications for the choice of frequency. Higher frequencies permit higher data rates, but may require the use of devices which have greater power consumption. For example, in embodiments (such as the first embodiment discussed below) which use op amps for RF detection, higher frequencies mean that higher-bandwidth op amps (broad-broad operational amplifiers) must be used. Such op amps tend to have higher static power consumption.

In a micropowered RF receiver, comparators can be used for RF detection if the signal levels are sufficiently high (and the frequencies are sufficiently low). However, if lower signal levels must be detected (in a micropowered direct detection circuit), then op amps are preferably used. The power level which is seen by the receiver is determined by various system parameters, including the size and configuration of the receiver

antenna, the Q of the receiver antenna circuit, the power and antenna gain of the transmitter, and the maximum distance between the transmitter and receiver. In the system described, comparators are considered to be satisfactory for a minimum detectable signal of 10 mV at 200 kHz. However, if the minimum detectable signal level is to be less than one millivolt, it is preferable to use op amps.

Thus, in the first embodiment described below, there are five different frequencies which appear at the portable module. In this example, the frequencies used include:

300 MHz: (the "read-data" frequency): This UHF frequency is used for transmission from the portable module to the base station. This frequency falls in a relatively quiet part of the spectrum, where good range can be achieved. This frequency also facilitates antenna design and placement, since a high-Q resonant antenna circuit can readily be configured to fit inside a small module.

200 kHz (the "write-data" frequency): This frequency is used for transmissions from the base station to the portable module. This frequency is low enough to permit a reasonably good power efficiency (in the receiving circuits) during data reception, while also permitting an acceptably high data rate to be achieved.

100 kHz: (the alternate "write-data" frequency): This is an alternate frequency, which can be used instead of 200 kHz for transmissions from the base station to the portable module. The portable module, in the presently preferred embodiment, also includes circuitry for receiving 100 kHz signals which are seen at a pair of electrical contacts. This provides a back-up data channel which permits a user to bypass the RF link. This can be particularly useful in factory automation or other high-noise environments. If desired, the module can be readily reconfigured so that this frequency is received by an antenna, instead of (or in addition to) the 200 kHz antenna. Due to regulatory constraints, this frequency may be available in some places where the 200 kHz is not usable.

20 kHz (the "wakeup" frequency): This frequency is used solely to initiate wake-up of the portable module. When the module is in standby mode, it monitors this frequency only. A base station broadcasts a signal on this frequency to wake-up nearby portable modules.

2 kHz (the "freshness-seal" frequency): This lowest frequency is monitored with essentially zero standby power. This is done by connecting the antenna input directly to an MOS gate (biased at ground), so that no current is drawn unless the signal is large enough to turn on the transistor, i.e. exceeds one V_T (threshold voltage). Pulse trains at this low frequency are used to switch the module out of (or into) a shutdown mode, where the module is not even monitoring the 20 kHz frequency. The signals at this lowest frequency must be of large magnitude, such as would be achieved by physically inserting the module in the slot in a toroidal coil, or between a pair of driven electrodes.

In this first embodiment, the power required to monitor the 20 kHz frequency in the standby mode is approximately two orders of magnitude less than that required to monitor the 200 kHz frequency in the active mode. Thus, the power saving achieved by this frequency allocation is very considerable.

In the second described embodiment of the receiver, only four frequencies can appear at the portable module, since the 20 kHz wakeup signal is not used.

Of course, the 2 kHz and 100 kHz frequencies are not often used, and the 200 kHz (or equivalent) and 300 MHz (or equivalent) frequencies provide the primary data channels.

Of course, the specific frequencies referred to are merely illustrative, and verbal labels are accordingly used to refer to disclosed frequencies and to other frequencies which could be substituted therefor. The specific frequencies are not at all critical, although some aspects of the relation of frequencies, and of the frequency bands used, are particularly advantageous and are believed to be novel. For example, as will be readily recognized by those of ordinary skill in the art, the specific

frequencies used in the sample embodiments described can easily be changed (to a certain degree) simply by changing the values of reactances in the disclosed circuits.

The disclosed innovative teachings provide a wireless data-interface system, where the identification field (which is 64 bits long in the presently preferred embodiment) can be parallel polled. By commanding all modules within range to respond, the base station can see the 64-bit identification fields combined in what is almost a "wired-OR" fashion. That is, if any one of the portable modules within range is pulsing (reporting a "1" bit) in a given time window, the base station will see a pulse; the base station will see the absence of a pulse only if all of the modules within range are reporting a "0" bit (not pulsing). This can be used, for example, to implement combinatorial logic functions on all (or some subfields of) the 64-bit identification field.

An example of the use of this capability is in secure facilities, for personnel access control. Suppose that every employee (or visitor or contractor) wears a badge, and that 10 bits of the identification field are used to indicate security clearance (at ten possible levels). One bit can be assigned to each level, so that each badge has only one "1" bit in this subfield. Then a base station can poll all badges in its area, and rapidly determine that there are no clearances below a certain level within range.

Disclosed innovative teachings advantageously enable a wireless data communication system, including at least one base station and at least one low-power portable module. RF assignments, protocols, and coding are chosen to permit the portable module to provide data exchanges with the base station over very short distances, at moderate baud rates, with high power efficiency in the portable modules. A connector, including a power supply input, is also provided on the portable module. Using this connector permits the data in the portable module to be read out very rapidly, even if the data has been accumulated from a long series of transactions. The power supply input means that block-dump operations can be performed as often as desired without degrading the battery

lifetime of the portable module, no matter how large the memory in the module is.

The disclosed innovative teachings provide a very simple filter circuit, which is all-digital but does not require the complex circuits and techniques used in DSP techniques. In effect, the present invention exploits the analog properties of digital circuit configurations.

It is well known that a simple digital inverter will usually have fairly sharp low-pass cutoff characteristics. That is, an analog input signal at a certain frequency, applied to a logic gate with a certain time constant, will provide a peak voltage which depends on only three factors: the peak voltage of the input signal; the RC time constant of the circuit; and the frequency of the input signal. If the frequency of the input signal is low enough, in relation to the RC time constant, the analog input signal will be able to switch the logic gate on each cycle, so that the output of the logic gate will contain a strong signal component at the input frequency.

The present invention makes use of this characteristic to provide a compact, low-power, bandpass filter. The characteristic of this filter has very sharp band edges, and essentially no ripple in the passband. Moreover, this filter configuration is relatively insensitive to parameter variation. This filter configuration is particularly advantageous at low frequencies and in low-power systems.

The presently preferred embodiment uses the time constants of the inputs to two logic gates to define the upper and lower passband edges. In the simplest example, where the passband center frequency is 2 kHz, two digital inverters are used, with cutoff frequencies which bracket the desired signal frequency (e.g. 1500 Hz and 2500 Hz). The cutoff frequency of the two digital inverters is selected by changing their RC time constants. (In practice, this is done merely by adding series resistance or shunt capacitance in the gate circuit.)

The inverter with the lower cutoff frequency has its output connected to the reset input of a counter, and the inverter with the higher cutoff frequency has its output connected to the clock input of a counter. The

counter output is monitored, to see when a certain count threshold has occurred. The result is that, at very low frequencies, the counter will be reset approximately as often as it is clocked, so it will not accumulate. At very high frequencies, the counter will not be clocked. Thus, this very simple digital circuit provides a bandpass filter, with sharp passband edges. This filter also has the advantage of very sharp rejection of 1/f noise.

Note that this circuit performs both filtering and thresholding functions: an in-band signal must be present, and must have sufficient magnitude, before any AC component will appear in the output of the logic gate.

Note also that this circuit is not linear, and will treat complex signals quite differently from simple signals. This circuit is particularly well adapted to detecting the presence or absence of an in-band signal whose energy is largely concentrated at a single frequency. This circuit is less well adapted to passing more complex in-band signals, since (in this circuit) the different frequency components may interfere with each other.

In a further optional alternative, this circuit can be used to detect the presence of in-band energy, and enable a more complex circuit to perform more complex filtering operations accordingly. In a further optional alternative, the output of this circuit can be used to provide a clock signal which is used to synchronize other circuits to the principal in-band frequency of the incoming signal.

Another feature of this circuit is that even a strong in-band signal can be blocked by low-frequency noise. However, in applications where this is a problem, a large series capacitor can be used to attenuate the lowest frequencies.

The present invention is particularly advantageous in low-power applications. Where the incoming analog signal is expected to be a strong one, it can be connected directly (i.e. without amplification) to the logic gates being used for filtering. This means that no power is consumed if the incoming signal is not able to trip either of the logic gates.

The disclosed innovative teachings provide a battery-powered module architecture which is particularly advantageous where a serial data interface is used to link two (or more) integrated circuits within the module. Among the teachings of the present invention is a battery-powered system, where a first integrated circuit provides a secondary power supply to a second integrated circuit, and also provides data signals in a serial protocol. The first integrated circuit steps down the secondary power supply when the reset-bar signal is being driven high. The second chip goes active whenever its reset-bar input exceeds its battery-voltage input.

Preferably a scaled supply voltage output is provided by a data converter chip to downstream chips (including an access control chip, in the presently preferred embodiment). The access control chip (in the presently preferred embodiment) goes active whenever its RST* input exceeds its V_{BAT} input. Since RST* can be driven only to the positive power supply level, the converter chip provides the access control with a reference voltage level which is lower than the power supply level. (However, to minimize power consumption, this reference voltage level is lowered only when necessary, i.e. when the RST* line is being driven high.) This reference voltage is connected to the V_{BAT} input of the access control chip.

A further feature is that the switching transistors are arranged in a configuration such that two transistors would have to fail before the battery could receive uncontrolled charging current. This provides improved safety.

The disclosed innovative teachings provide additional insurance against data corruption, by testing for errors in the address field before any memory write is permitted to occur. This prevents data corruption due to errors in the address field, without greatly degrading the overall data rate.

The presently preferred embodiment provides an architecture wherein a substantial amount of random-access memory (RAM) is included in the

remote module. This presents data-integrity problems which are quite different from those presented by the more common use of a small amount of memory: if an error occurred in the address field, during a write to the RAM, data could be lost. The presently preferred embodiment uses error-checking logic to implement a cyclic redundancy check. The cyclic redundancy check is used to detect errors in data transmission. It is also used to lock out access if a bit error occurs anywhere in the protocol word (which includes the memory address bits). Thus, one-bit errors cannot cause data to be written to the wrong address in memory.

Preferred System Embodiment of the Disclosed Inventions

In the presently preferred embodiment, the claimed inventions are used in the context of a wireless-accessible data module. Various features of this system context will therefore be described in great detail below. The general features of this context will now be described.

Many of the innovative teachings of the present application will initially be described in the context of an embodiment, as shown in Figure 1, wherein RF communication is established between a base station and one or more portable data modules. Each portable module can be accessed, in slave mode, by a base station 110 whenever the portable module comes within range of the base station.

A split frequency allocation is used on the RF channel. The base station transmits at a relatively low frequency (referred to herein as the "write-data" frequency), and the remote module transmits at a much higher frequency (referred to herein as the "read-data" frequency). The transmitter powers used permit communication over a very short range.

The portable data module is preferably extremely compact, and is powered by an small non-rechargeable battery. The base station is assumed not to be power-limited, but of course the innovative teachings set forth herein could also be applied to systems where some of the base stations are micropowered and/or some of the portable modules are not micropowered.

Within the remote module, each variable-length pulse in an incoming RF signal is converted into a variable-length burst of digital pulses. These bursts are decoded to derive commands and data. (The portable module operates in slave mode, so that the commands thus received govern its operation.) The portable module also contains an internal serial data bus, and memory or other devices in the portable module can be written to (or read from) over this serial bus, as commanded by the incoming RF signals.

The 3-wire serial data bus within the portable module can be used in a variety of ways. In the presently preferred embodiment, this bus is connected to an access control chip and to the converter chip. In an alternative embodiment, this bus is connected to a memory controller chip (instead of the access control chip), and, through the memory controller chip, to an SRAM. In further alternative embodiments, additional micropowered integrated circuits (such as a microprocessor or display driver) can also be connected to this bus if desired. Similarly, while the portable module preferably also contains access control logic, to provide security against unauthorized access, this can be omitted if desired.

To further conserve power, the portable module has the capability to be completely turned off or on, by wireless control. By keeping the receiver circuit turned off until the module is put into service, the battery life is conserved. In the off state (which is referred to as the "sleep" or "freshness seal" mode, as distinguished from the standby mode), the battery drain is reduced to transistor leakage currents - almost zero power (a few nanoamps). To put the module into service, the whole module is placed in a strong 2 kHz electromagnetic field. A strong coded signal at this frequency is detected by zero-standby-power circuits, with control logic to turn on or turn off all the other detection functions of the receiver.

BRIEF DESCRIPTION OF THE DRAWING

The present invention will be described with reference to the accompanying drawings, which show important sample embodiments of the invention and which are incorporated in the specification hereof by reference, wherein:

Figure 1 shows the general organization of a **wireless communication system** enabled by the present invention, wherein a base station 110 can send data to a nearby remote module 120 at a first frequency, and can receive data from the remote module 120 at a second frequency.

Figure 2A shows a block diagram of the **remote module** 120, in a first embodiment. Figures 2B and 2C show a more detailed circuit diagram of the module of Figure 2A, including discrete reactances and the VHF/UHF transmitter circuit. Figure 2D shows an alternative embodiment of the portable module portion of Figure 2A, including a large block of memory, a memory access controller, and an external connector which allows a rapid readout of the stored data.

Figure 3A is a block diagram, showing key signal connections, of the **base station** 110 shown in Figure 1.

Figure 4A shows the organization of some functions of the **receiver chip** 210 of the presently preferred embodiment. Figure 4B shows the preferred implementation of the bandpass filter used in the receiver chip 210. Figure 4C shows a second embodiment 210' of the receiver chip, which can detect lower signal levels. Figure 4D shows further details of the configuration of a single amplifier stage with constant-multiplier-scaled arrays of feedback and series resistors. Figure 4E shows further details of an active bandpass filter stage with constant-multiplier-scaled arrays of capacitors and feedback resistors. Figure 4F shows how digital automatic gain control is performed in the receiver chip, in an alternative embodiment. Figure 4G shows a further alternative embodiment, wherein digital automatic gain control is performed by using transistors to selectably switch out individual elements of a resistor ladder.

Figure 5A shows the overall organization of the **converter chip** of the presently preferred embodiment. Figure 5B shows the power switching circuit preferably used in the converter chip of Figure 5A. Figure 5C shows the control logic 550 preferably used in the converter chip of Figure 5A. Figure 5D shows an alternative embodiment of the converter chip of Figure 5A, and shows separately some additional portions of the control logic 550, as well as the input select. Figure 5E shows the timing relations used, in the presently preferred embodiment, to implement the pulse counter 530. Figure 5F shows an eight-bit digital magnitude comparator which is preferably used within the pulse width detector 530. Figure 5G shows the state diagram which is preferably implemented by the state machine 552 shown in Figure 5D.

Figure 6A is a block diagram of the **access control chip** used in the presently preferred embodiment, in its normal mode of operation. Figure 6B is a flow chart of the normal mode of operation of the access control chip of Figure 22. Figure 6C is a block diagram of the access control chip used in the presently preferred embodiment, in its program mode of operation. Figure 6D is a flow chart of the program mode of operation of the access control chip of Figure 6A.

Figure 7A shows an overall block diagram of the **memory controller chip** 260 which is used in the alternative remote module embodiment of Figure 2D. Figure 7B shows the communication protocol preferably used in the memory controller chip 260. Figure 7C shows the command structure for selectable masking of address bits in the memory controller chip 260. Figure 7D shows the format of the arbitration byte preferably used to arbitrate between the two ports which may seek access to memory, through controller 260. Figure 7E shows the logic used, in the presently preferred embodiment, to generate the cyclic redundancy check (CRC) data.

Figure 8 shows how the converter chip, in the presently preferred embodiment, controls its power-supply output line to help other chips receive data from the serial bus.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment, wherein these innovative teachings are advantageously applied to the particular problems of a wireless electronic key system. However, it should be understood that this embodiment is only one example of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others.

Application Environment

Some of the many application environments for the preferred data communications system (with RF-accessible portable data modules) will now be described. Some of the innovative teachings set forth herein are particularly advantageous in some of these application environments. Among the innovative teachings set forth herein may be systems in which novel communications capabilities are applied to a particular application.

One particularly useful class of applications of the disclosed communication system is tracking work-in-process in automated manufacturing environments. A portable data module can, for example, be attached to a product on an assembly line. As the product moves from station to station, the portable module 120 can be interrogated to let the station known what the product is, what operations must be done, what the next destination is, etc., all without physical contact. One example of this is in semiconductor manufacturing, where an RF-accessible data

module, embedded in a wafer carrier, can provide an instantly accessible detailed processing history of the wafer or lot being transported. This remotely accessible data memory provides an important tool for reconciling automated handling and transportation with highly flexible and reconfigurable workpiece routing.

Another advantageous instance of work-in-process tracking is in livestock management. By attaching RF-accessible portable modules 120 to each animal, the history of each animal can be carried with it, and automated gates can be used to select animals as desired. For example, feeding can be controlled to optimize the rate of weight gain, and animals which are off their feed can be detected very promptly.

A related class of applications is for inventory control. Note that the disclosed communication system can be used for completely automatic inventory control, since each base station can readily ascertain what portable modules 120 are in its vicinity. Similarly, base stations mounted at every entrance and exit can track all movements of inventoried goods.

In addition, the wireless system disclosed can also be used to provide a wireless link between a hand-held terminal and a host system.

Another related class of applications is for monitoring and control of machinery or other capital equipment. For example, maintenance and use records of vehicles or other machinery can be automatically maintained and remotely queried.

Another class of applications is shipping containers of various kinds, including personal luggage. The read/write capability of the system provided by the innovative teachings herein means that destinations, tare weights, contents descriptions, etc. can be readily reprogrammed, and remotely detected. Thus, handling equipment can perform automated routing, specific shipments can readily be traced, and loss and theft can be greatly reduced.

Another important class of applications is in control of access to secure facilities. A portable module 120 can be used to store extensive identification parameters for the person to whom it is assigned, including

(for example) height, weight, voice recognition parameters, or even parameters for image recognition (of fingerprints, faces, or retinas). This permits very sophisticated machine-recognition strategies to be implemented, without the data-flow bottlenecks which could occur (in a large facility) if such extensive recognition parameters were stored only in a central database. (Sampling and updating strategies would be used to assure integrity of the data in the remote modules 120 and in the central database.)

Area-specific access is also conveniently achievable. Base stations 110 can be positioned at key movement bottlenecks in a large building, so that the movements of individuals can be tracked. Thus, for example, in secure facilities, access intrusions can be detected, and movements of persons without clearance can be tracked. In hospitals, control of inpatient movements can be readily achieved. Where the present invention is used to monitor personnel movements, infrared sensors (or other such auxiliary remote sensors) can be used to detect any individual who is not carrying a functional remote module 120.

Medical applications generally are a very advantageous class of embodiments. Key parts of a patient's medical records (including, for example, recent weight and temperature data, and current medication authorizations) can be stored in a remote module 120 which is physically attached to the patient. Similarly, the source and history of specimens can be tracked by data modules.

Another class of applications is in financial instruments, such as credit cards, securities, large checks, letters of credit, or large-denomination currency. The disclosed communication system permits the convenience of bearer instruments to be provided without the untraceable diversion possibilities of conventional bearer instruments. In addition to the self-authenticating features of conventional cards or documents, the remote polling capability of the disclosed system permits convenient query for authentication, as well as remote detection of spurious items.

Overall System Architecture

The overall configuration of the system in which the presently preferred embodiment is preferably used will first be described in detail, since this system context highlights some of the advantages obtained by the present invention.

Figure 1 schematically shows a very simple system embodiment, where RF communication is established between one base station module 110 and one portable data module. However, it should be noted that the disclosed architecture can accept many base stations and many portable data modules. The base station module 110 interfaces to a host system (e.g. using a wired serial bus), and also provides an RF communications link to one or more remote modules 120. The remote modules 120 are preferably small portable units, which operate with very high power efficiency from a battery. (Units of this type are generally referred to as "micropowered.")

A split frequency allocation is used on the RF channel. The base station 110 transmits at a relatively low frequency (referred to as the "write-data" frequency), and the remote module 120 transmits at a much higher frequency (referred to as the "read-data" frequency). In the presently preferred embodiment, the read-data frequency actually falls in the VHF or UHF bands, and the write-data frequency falls within the LF (low-frequency) band.

In the presently preferred embodiment, a pulse-width modulation coding scheme is used for transmissions on the write-data frequency channel. This scheme provides good noise immunity, and the code assignments are selected to optimize the data rate (by assigning the most frequently used symbols to the shortest pulse widths). The RF transmitter is simply switched on or off, to provide binary (on or off) pulses of varying length. A simple binary amplitude shift keying scheme is used for transmissions on the read-data channel.

The RF organization is designed for very short-range communications. However, the power levels of the RF channels are very unequal. Higher

transmitter power and net receiver sensitivity are preferably located in the base station, where the power budget, and the volumetric constraints, are less limited.

Each active base station 110 can broadcast a query signal, to determine whether any portable data modules 120 are in its vicinity. If one of the remote modules 120 is within range (e.g. within 5 feet or less), it will detect the base station's query signal, and will then put out a beacon response by keying its transmitter (on the read-data frequency) with a square wave (e.g. by chopping at a 10 kHz rate). The base station scans the read-data frequency band, to detect any such beacons. Once the beacon is detected, the base station 110 can then initiate an RF communication session, and get read or write access to the data memory in the portable module 120.

One full transmission and reception cycle contains 280 bits, maximum, and is called a transaction. (The 10-year estimated battery life (for a 180 mA-hour lithium cell) allows for more than 10^8 transactions during the portable module 120's lifetime.) In these transactions, the portable module 120 is slaved to the base station 110.

In any system which permits wireless data access, problems of data security and integrity must be considered. The disclosed preferred systems include two levels of functionality for this purpose. (Of course, as further alternatives, many known methods could be adapted to serve instead.) In the presently preferred embodiment, an access control chip is used in the portable module, and this chip includes a 64-bit identification field and a 64-bit password. In an alternative embodiment, the converter chip also includes a 16-bit chip-selection-tag field, which can be used for first-level scan of possible portable modules within range. In this alternative embodiment, the access control preferably also has the capability to generate random data when access is attempted without the correct password. (Preferably this capability is not used without the 16-bit chip-selection-tag field, since otherwise access collisions could occur whenever two modules were within range of a base station.)

In the principal preferred embodiment, after the foregoing interchange has initiated communication, the base transceiver transmits a command, on the write-data frequency, requesting (normally) that the module's 64-bit identification code be returned. After this operation finishes, a 64-bit password is transmitted to "unlock" the secure memory in the access control chip, so that data can be read from it or written to it.

Two features speed up the base station's ability to identify which of the possible remote modules may be within its range. These features may be particularly useful in applications where a large number of remote modules may come within range of a given base station.

First, in the alternative embodiment just mentioned, the base station can scan over segments of the 16-bit chip-selection-tag field to rapidly identify whether a given module is nearby. This means that all possible combinations of the 16-bit chip-select field can be scanned in $8x2^2$ searches, rather than 2^{16} as would otherwise be required. (Of course, if more than one portable module is nearby simultaneously, the amount of time required to identify all modules present may well be longer than $8x2^2$ searches.)

Secondly, a further optional alternative embodiment permits parallel polling of the 64-bit identification field. By commanding all modules within range to respond, the base station can see the 64-bit identification fields combined in what is almost a "wired-OR" fashion. That is, if any one of the portable modules within range is pulsing (reporting a "1" bit) in a given time window, the base station will see a pulse; the base station will see the absence of a pulse only if all of the modules within range are reporting a "0" bit (not pulsing). This can be used, for example, to implement combinatorial logic functions on all (or some subfields of) the 64-bit identification field.

The portable data module is preferably extremely compact, and is micropowered. The base station is assumed not to be power-limited, but of course the innovative teachings set forth herein can also be applied

to systems where some of the base stations are micropowered and/or some of the portable modules are not micropowered.

In this application, it should be noted that the term "RF" is used to refer to wireless electromagnetic radiation at all sub-optical frequencies, including frequencies which fall in the ultra-low frequency (ULF) band below 3000 Hz (cycles per second). (In some literature, such low frequencies may be referred to as audio frequencies, as distinguished from radio frequencies.)

Portable Wireless Data Module

The portable data module 120 provides a miniature transportable electronic memory, together with a self contained transmitter, receiver, and power supply, which provides wireless data communication, via a base station 110, with a host computer system. The small, lightweight construction makes the device suitable for carrying in a pocket or for direct attachment to any mobile object.

Figure 2A shows an overview of the remote module 120. The RF receiver functions are segregated on a receiver chip 210. No decoding is performed by the receiver chip 210. Decoding and encoding are performed by a converter chip 220, which also controls the serial data bus 206 within the remote module 120. The receiver chip 210 receives an RF signal (from an antenna tuned to the write-data frequency), and tracks the amplitude shifts of the RF signals to output a burst of pulses (at full digital logic levels). (The duration of the digital pulse bursts at the receiver chip's output corresponds to the duration of the analog pulse seen at its input from the write-data RF channel.) Since the output of the receiver chip 210 is simply pulse bursts, the receiver chip 210 is connected to the converter chip 220 by a simple one-wire bus, with no clock or reset signals required.

The data converter chip 220 decodes the pulse bursts provided by the receiver chip 210. This converter chip translates these digital pulse bursts from the one-wire pulse-width modulation protocol to data signals on a

conventional 3-wire serial data bus 206 within the portable data module 120.

The 3-wire serial data bus 206 within the portable module can be used in a variety of ways. In the presently preferred embodiment, this bus is connected to an access control chip 230 and to the converter chip 220. (In an alternative embodiment, as seen in Figure 2D, bus 206 is also connected to a memory controller chip 260, and, through the memory controller chip 260, to SRAMs 262.) In further alternative embodiments, additional micropowered integrated circuits (such as a microprocessor or display driver) can also be included in portable module 120, and connected to bus 206, if desired. Similarly, while the portable module preferably also contains access control logic, to provide security against unauthorized access (e.g. implemented as access control chip 230), this can be omitted if desired.

To further conserve power, the portable module 120 has the capability to be completely turned off or on, by wireless control. When the receiver circuits are turned off, the power consumption is essentially zero. By keeping the receiver circuits turned off until the module is put into service, the battery life is conserved. In the off state (which is referred to as the "sleep" or "freshness seal" mode, as distinguished from the standby mode), the battery drain is reduced to transistor leakage currents - almost zero power (a few nanoamps). To put the module into service, the whole module 120 is placed in a strong 2 kHz electromagnetic field. A strong coded signal at this frequency is detected by zero-standby-power circuits in the receiver chip 210, which control logic to turn on or turn off all the other detection functions of the receiver.

The variable-duration pulses received on the write-data channel, and converted by the receiver chip 210 into variable-length bursts of digital pulses on the one-wire connection to converter chip 220, are decoded by the converter chip 220 into one of the set of possible symbols (commands). In the presently preferred embodiment, the possible command set includes:

A. Write 0 or read when active;

B. Write 1 when active;

C. Activate Reset;

D. Beacon path;

E. Return to standby.

(Even if the portable module 120 does not receive a Return-to-standby command, it will automatically return to the idle mode to conserve power after a 2 ms quiet period.) However, it should be understood that a variety of other command sets could be used instead.

These commands are interpreted by the converter chip 220 to control the three-wire serial bus 206. This bus, as is conventional, includes one line reserved for clock signals, one bidirectional data line, and one line reserved for Reset signals. Such a bus can readily be connected to serial-port memory chips, or to port pins on a DS5000 or on other microcontrollers sold by Dallas Semiconductor.

One important alternative embodiment (shown in Figure 4C, and discussed in detail below) uses a modified receiver chip 210', and a slightly different RF frequency allocation. In this embodiment, the portable data module 120 has the capability to detect quite weak RF signals (RF voltages down to about 300 microVolt). To implement this detection ability, the alternative receiver chip 210' uses op amps rather than comparators at its input. To minimize the power drain of these op amps in standby mode, a much lower frequency (e.g. ten times lower than the write-data frequency) is used solely for wakeup. Lower-power op amps, which have a lower slew rate and smaller gain-bandwidth product than would be necessary to track the signals in the write-data channel, monitor this wakeup frequency. If a wakeup signal is detected, the beacon is turned on, and the detection circuits in the write-data channel are turned on.

A touch-contact port 270 is also provided. Signals received at this port will override signals received from the antenna 121 which receives signals on the write-data frequency. Preferably this input is connected

directly to the converter chip 220, so that antenna 121 and receiver chip 210 are bypassed if this input is used. In the presently preferred embodiment, the touch contact port 270 transfers data using a carrier frequency of 100 kHz.

The port 270 provides a backup interface mode, which can be used to supplement the RF interface in (e.g.) high noise environments, or when the battery of the portable module 120 is weak. The capability to handle a 100 kHz interface also provides useful versatility, since the module can be reconfigured fairly easily to (for example) provide capability for both 100 kHz and 200 kHz RF links.

An advantage of the encoding used on the write-data channel is that it is relatively insensitive to frequency. For example, when data is being transferred over the touch-contact port 270, the exact same coding can be used as would be used for transfer over the write-data channel. The data rate will be lower, because the frequency is lower, but the state-machine decoder circuits in the converter chip 220 can still operate in the same way. Similarly, the frequency assigned to the write-data channel can easily by changed, simply by changing or varying the reactive elements in the turned circuits, but the coding scheme will still provide a good balance of data rate with noise immunity at whatever frequency is being used.

The variable-duration pulses sent by the base station 110 at the write-data frequency (200 kHz) are picked up by the write-data receive antenna 121, and are thereby seen at the comparator input terminals (A+ and A-) of the receiver chip 210. Unless the receiver chip 210 is in freshness seal mode (as described below), the receiver chip 210 will amplify the analog input pulse signals from as low as 10 mV to provide full digital level pulse-burst signals at the output pin. The receiver chip 210 does not demodulate the RF input signal, but simply amplifies its instantaneous level. Thus, the carrier is a component of the amplified digital signal, so that what is sent to the converter chip 220 is not merely a series of variable-length pulses, but a series of variable-length bursts of constant-length pulses.

In the presently preferred embodiment, two parallel tuned antenna circuits 121 are used for reception the write-data (200 kHz or equivalent) frequency, and each of the antenna circuits is separately connected to an open loop comparator. (These connections are shown in Figure 4A as input pairs A+/A- and B+/B-.)

In alternative embodiments, the tuned antenna circuit 121 at the write-data frequency is also coupled to a tuned tank circuit, and/or to a notch filter centered at half the pass frequency, to provide sharper passband characteristics.

A tuned circuit with a discrete inductance is used to receive signals at the freshness seal frequency, but no other antenna is used. (Thus, the effective antenna cross-section at this frequency is very small. This is acceptable because the freshness seal only needs to detect very strong signals.) The input to the freshness-seal-signal detection circuits is labelled as signal "FI".

The converter chip 220 is basically a state machine, which controls the serial bus 206 and determines what action is to be taken by the attached access control chip 230. The access control chip 230 receives signals from the converter chip 220 over the bus 206. These signals either write data into or read data out of the access control chip 230. The access control chip 230 includes specially partitioned memory space, which stores a 64 bit identification code and a 64-bit password. The password memory is combined with comparison logic, so that data accesses are screened for password match. Preferably the password memory (which, in this embodiment, includes 128 bits of read/write nonvolatile memory) cannot be read, and can be overwritten only by an access which includes a match with the existing password.

When the portable data module is receiving data to store in the access control chip 230, the converter chip 220 generates the CLK, RST* and data signals, in accordance with data received from the receiver chip 210. However, when the portable data module is being read, data is

transmitted back to the base station 110 via a 300 MHz transmitter which is controlled by the converter chip 220.

The portable data module is self powered by a lithium energy cell. The unit is designed to last for over ten years. The converter chip 220 and receiver chip 210 control the energy consumption and power distribution within the module.

Figures 2A-2C show a more detailed view of the portable module 120 of the presently preferred embodiment. As shown in Figure 2B, a tuned coil 121 acts as an antenna, and is connected, through an RLC filter network, to a receiver chip 210. The receiver chip 210 provides an output, at full digital levels, to a data converter chip 220. The receiver chip 210 and the data converter chip 220 are both powered from a battery 250, which in the presently preferred embodiment is a lithium battery.

In addition, an access control chip 230 is connected to the data converter chip 220 by the 3-wire serial data bus 206. The access control chip 230 can receives its power supply voltage from the data converter chip 220 either over the RST* line, or (when RST* is low), over the V_{BAT} input (which is connected to the reduced-voltage supply BATOUT of the converter chip 220).

The data converter chip 220 also provides a signal RFOUT, which controls a transmitter 240 (shown in Figure 2C).

Alternative Embodiment with Fast Data Dump

Figure 2D shows an alternative embodiment of the portable module 120 portions shown in Figure 2B. In this alternative embodiment, a memory access controller 260 is also connected to the 3-wire data bus 206 from the converter chip 220 to the access control chip 230. This memory controller, in turn, is connected to a block of memory, such as a pair of 256K SRAMs 262. (In optional alternative embodiments, the preferred memory access controller 260 can control up to 16 32Kx8 SRAMs.)

Figure 2D also shows the further alternative feature of a parallel port contact 290. (Note that this is not the same as the touch-contact port 270,

which provides serial data transfer. The parallel port 290, unlike the serial port 270, provides data transfer which is much faster than that achievable over the RF channel.) The parallel port 290 can be connected to a complementary parallel port connector, to permit a rapid dump of all the data in memory with burden on the battery 250. However, it should be noted that a parallel port contact 290 can be used without the memory controller chip 260 (especially if serial-ported memories 262 are used, or if a microprocessor is also included in the portable module). Conversely, a memory controller chip 260 can be used advantageously, even if the parallel port contact 290 is not included.

The memory controller chip 260, in the presently preferred embodiment, provides dual-ported access to a parallel memory bus 703. Access is shared between serial bus 206 and parallel bus 701 (which is connected to the connector 290 in embodiments like that of Figure 2D).

Note that parallel port 290 preferably also includes a power input, which is connected to a power supply input of the converter chip 220. When the converter chip 220 detects a voltage higher than V_{BAT} on this input, it will switch over to the higher supply voltage. This means that the rapid readout cycles will not place a burden on the battery 250.

This embodiment permits a large volume of data, collected in portable modules over a relatively long period of time, to be rapidly downloaded. Thus, the wireless communications channels can be organized for very high power efficiency, at very low data rates, since a high-data-rate read operation can always be accomplished by other means. A further advantage of this class of embodiments is that very large amounts of memory (e.g. a megabyte) can be used in a micropowered portable module, while still achieving long data-retention lifetimes. This fast data dump capability is particularly advantageous for applications (such as delivery logbooks, retail inventory, or vehicle management), where data is collected slowly in the field, and then rapidly dumped at a more central location.

Alternative Embodiment with Low-Frequency Wakeup

One important alternative embodiment uses a modified receiver chip 210', and a slightly different RF frequency allocation. In this embodiment, the portable data module 120 has the capability to detect quite weak RF signals (RF voltages down to about 300 microVolt).

To implement this detection ability, the alternative receiver chip 210' (shown in Figure 4C) uses op amps rather than comparators at its input. To minimize the power drain of these op amps in standby mode, an additional RF frequency (which is a much lower frequency, e.g. ten times lower, than the write-data frequency) is used solely for wakeup. When a base station 110 is broadcasting to find portable modules 110, it broadcasts on this wakeup frequency. In the receiver chip 210', the write-data frequency is not monitored when the module 120 is in standby mode. Instead, another pair of op amps, which have a lower slew rate and smaller gain-bandwidth product than those used to track the signals on the write-data channel, are kept active to monitor an antenna input at the wakeup frequency. Any inputs received on the wakeup frequency are decoded by a very simple thresholding scheme, like that used to decode symbols on the write-data frequency, which provides noise rejection. If a properly encoded signal is detected on the wakeup frequency, the (higher-powered) detection circuits in the write-data channel are turned on.

In the standby mode, the receiver chip 210 will draw about 1 microAmp, while amplifying incoming RF signals at the wakeup frequency (20 kHz in this example) to digital pulse bursts on one-wire bus 215. These pulse bursts are monitored by the converter chip 220, and when the proper sequence occurs the converter chip 220 provides an enable signal EN back to input EI of the receiver chip 210. After this enable signal has been received, the receiver chip 210 activate a higher-

power pair of op amps, which have a high enough slew rate and gain-bandwidth product to track signals at the write-data frequency, and which draw about 100 microAmp. The receiver chip 210 will stay enabled for as long as signals are seen at either the write-data frequency or the wakeup frequency. If neither signal is present for 2 msec, the 200 kHz receiver will automatically turn off. The 200 kHz receiver can also be turned off by a specific sequence of 20 kHz signals.

Transmitter

Figure 2C shows details of the transmitter 240. This transmitter is powered and controlled by signal RFOUT, which is provided by the data converter chip 220. When the signal RFOUT is pulled high, transistor 241 is enabled to turn on. The transistor 241, in this example, is an NPN transistor with a cutoff frequency substantially higher than the desired transmission frequency. For example, an MRF931 has been found to be satisfactory.

The various reactances shown provide feedback, so that the transistor 241 sustains oscillation. The oscillation output is connected to read-data transmit antenna 122. Antenna 122 is preferably an etched PC board trace, tuned by a discrete capacitor 242 to achieve resonance at the desired operating wavelength (which in this example about 100 centimeters). (However, it must be understood that the circuit configuration of these reactances could be rearranged in a tremendous variety of ways. Moreover, different values can be readily substituted for the specific sample values given.

It is further contemplated that frequency stabilization, using low-loss surface-acoustic-wave (SAW) devices, will become advantageous. SAW devices with reasonably low insertion losses (close to 1 dB) are now available reasonably cheaply. Such stabilization means that the base station does not have to sweep so broad a band to detect an incoming signal.

Note that Figure 2C shows a SAW filter used to provide a reactance from gate to ground, but a capacitor may be used instead if a lower insertion loss or lower Q is desired. Note also that the antenna is connected across the tank circuit: this has been found to be advantageous in such low-power applications.

Base Station 110

Figure 3A shows key blocks and key signal connection of the base station 110 of the presently preferred embodiment. A digital interface 300 interfaces to a standard RS232 bus, using data lines HOST_TXD and HOST_RXD. This digital interface permits the host computer (or a terminal) to provide an interface to the transmitter 301 and the receiver 302.

The receiver 301 is shown in several blocks, to clarify the functions performed. Antenna 112 is tuned to the read-data frequency, to receive RF signals transmitted by a portable data module 120. This antenna is connected, through a bandpass filter 320, to an RF receiver section 330. Section 330 provides outputs RFA, indicating amplitude of the RF signal, and outputs QUAD and /QUAD, which respectively correspond to the average amplitude of leading and lagging phase components.

Block 340 performs the ASK (amplitude-shift keying) and automatic frequency control (AFC) functions. The AFC operation is controlled by a feedback loop which extends through several of the components: The ASK/AFC block 340 compares the signals QUAD and /QUAD, to determine if the frequency needs to be adjusted. That is, phase error in one direction will indicate that the local oscillator is leading the incoming RF signal, and phase error in an opposite direction will mean that the local oscillator is lagging. When such a lead or lag or condition is detected, the FREQ_HIGH or FREQ_LOW lines are driven. In response to one of these signals occurring, the digital interface 300 increments or decrements a control value, which is converted by a digital/analog converter in the interface 300 to provide the signal DAC. The signal

DAC is fed back to control the local oscillator frequency and RF section 330. Thus, these connections in effect configured a phase-locked loop.

In addition, the digital interface 300 controls a 200 kHz transmitter 302. This transmitter is shown as switching (control) transistor 1710, antenna 1720 (or 111), and resonator circuit 1730.

Operation

To clarify the described relations and protocols, the steps in a sample transaction will now be described in detail. This sample transaction will be a normal read of the data in access control chip 230. Assume that the access control chip 230 has contents as follows (where each byte is represented as two hexadecimal numbers):

ID: 31 31 31 31 31 31 31 31 (hexadecimal)

Password: 01 23 45 67 89 AB CD EF (hexadecimal)

Data: 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33 33 (hexadecimal)

To access this remote module 120, the base station will have to know (from user input, or from data stored in the host computer) that the password is 01 23 45 67 89 AB CD EF. Next, the base station 110 is told (for example) to read the first portable data module it finds.

The conversation now proceeds as follows:

Step 1. The base station turns on the beacons of all keys in range. This is done by sending (on the write-data frequency) pulse group E (50 pulses)(to assure that all converter chips 220 are sent to the inactive 000 state), followed by pulse groups D(40), A(10), and B(20). Thus, the complete transmission at 200 kHz would be:

50 pulses, q, 40 pulses, q, 10 pulses, q, 20 pulses, q.

(The symbol "q" is used to indicate a quiet space of at least 50 microseconds.) After this transmission, any portable modules in range

will be in beacon mode, and will be transmitting a 300 MHz (±15 MHz) RF carrier, chopped at a 5 kHz rate.

Step 2. The base station 110 then sweeps its 100 kHz bandwidth input band pass filter 320 from 285 MHz to 315 MHz. At each step the base station 110 looks for the presence of any beacon from a portable module 120. Since any beacon will be chopped at 5 kHz (100 microsec on, 100 microsec off) the base station 110 must search each frequency range for at least 100 microseconds. (In alternative embodiments the sweep time can be decreased by increasing the beacon chopping frequency.) If no signal is present at a given step, the bandpass filter 320 is stepped to the next frequency range. If signal is present, the base station 110 records the times t_1, t_2, ... t_{10} of the next ten rising edges of 300 MHz signal. If the delays t_2-t_1, t_3-t_2, ... t_{10}-t_9 are all within 20% of each other, and both are in the range 167-250 microsec (4-6 kHz), then a portable module 120 is assumed to be present, and the base station 110 goes to step 4. If not, the band pass filter is stepped to the next frequency step.

Step 3. The base station 110 now sends out a command to initialize the portable data module 120, by sending pulse group C (30 pulses) at 200 kHz. On the first rising edge of the pulse packet, the converter chip 220 turns off the 300 MHz transmitter 240, and takes the portable module 120 out of beacon mode.

Step 4. The base station now sends a 24 bit command word to the portable module 120. This command word will be passed over the serial bus 206 to access control chip 230. For example, to initiate a normal read, the 24 bit word in hex is A00162. Since this is sent LSB first, the base station 110 transmission is as follows (where a write 0 command is represented by 10 pulses, and a write 1 is represented by 20 pulses):

10 pulses, q, 20 pulses, q, 10 pulses, q, 10 pulses, q,	2
10 pulses, q, 20 pulses, q, 20 pulses, q, 10 pulses, q,	6
20 pulses, q, 10 pulses, q, 10 pulses, q, 10 pulses, q,	1
10 pulses, q, 10 pulses, q, 10 pulses, q, 10 pulses, q,	0
10 pulses, q, 10 pulses, q, 10 pulses, q, 10 pulses, q,	0
10 pulses, q, 20 pulses, q, 10 pulses, q, 20 pulses, q,	A

Step 5. The access control chip 230 will now read out data for the next 64 clock cycles. The data read out will be that in its ID field. To read each bit, the base station 110 sends out 10 pulses, and then checks, 100 microsec later, for the presence of a 300 MHz signal. If the base station detects a 300 MHz signal at this instant, it infers that a "1" has been read out; otherwise the base station infers that a "0" has been read. This step is repeated for each of the 64 bits. Note that this readout scheme has the advantage that the timing of communication is entirely controlled by the base station. This provides additional noise margin. This also permits reliable communication even if significant clock inaccuracy exists in the micropowered portable module.

Step 6. Next (unless the base station rejects the identification data just received), the 64-bit password is sent to the portable module 120 as a series of write commands. Accordingly, the password data will be written to the access control chip 230. Step 7. The access control chip 230 will now read out 128 bits of data from its data field. After receiving this data, the base station 110 can respond appropriately. For example, the base station may report the 64 bits of identification and 128 bits of data back to its host computer. The host computer may then command the base station to initiate another transaction (such as a data write), or to reprogram the identification or password fields of the module, or to resume polling for other remote modules, or to initiate a physical action (such as unlocking a door).

Several of the alternative embodiments mentioned would also require additional steps in this transaction. For example, optionally the base station 110 may first send a "wake-up" or enable command, with a 16-bit

chip-selection-tag and one additional byte of command parameters. (In a further alternative, this may be a masked wakeup, so that the byte of command parameters will specify which fields are to be compared to the transmitted value.) However, this step is not used in the presently preferred embodiment, since the 16-bit chip-selection-tag field is not used. This wake-up or enable step may be repeated after scanning, if duty cycling is used to avoid the chance of missing a portable module which simply happened to be in the quiescent part of its duty cycle.

Receiver Chip 210

This integrated circuit in the portable data module performs the RF reception functions.

The receiver chip 210, as configured in the presently preferred embodiment, is an ultra-low-power dual comparator circuit designed to listen for signals of up to 250 kHz. Input signals as small as 10 mV peak-to-peak will be amplified to provide full digital signals, at power supply levels, at the output.

A dual comparator arrangement is used, where an alternate antenna input is used if no signal is found on the primary antenna input. By using two orthogonal antennas, the risk of nulls or dead spots are eliminated.

Note that the receiver chip 210 of the preferred embodiment can also be used advantageously in many systems other than the preferred system embodiment. For example, this integrated circuit can also be used as a front end for wireless communication links using infrared, ultrasonic, or magnetic field. The ultra-low-power features of this integrated circuit are particularly advantageous in applications where a portable module must be permanently powered by an energy source capable of lasting over ten years. The "freshness seal" logic, which provides a zero-power sleep mode, is particularly advantageous in this respect. The available duty cycle options can further reduce power consumption in special applications.

Two alternative embodiments of this chip are specifically disclosed. The first embodiment uses op amps for detection, and can detect RF

voltages as low as about 0.1 mV. The second (and preferred) embodiment uses comparators rather than op amps, but requires a significantly higher RF signal for detection.

Figure 4A shows a block diagram of the micropowered receiver chip 210. Two comparators 420 are used to amplify analog inputs. Comparator 420A receives inputs A+/A-, and comparator 420B receives inputs B+/B-. Each comparator is followed by a one-shot 422, to ensure that the digital outputs have a certain minimum duration, and to guarantee that the output state will be zero if no input is present.

When the comparators 420 are enabled, an AC input signal which exceeds 10 mV peak-to-peak will cause the comparator to change state at least twice per full cycle of the AC input signal. When the comparator output goes high, it will fire one-shot 422. This produces an output signal at full digital levels, with a certain minimum width per output pulse.

Several inputs are relevant to enablement of these comparators:

1) The comparators will not operate in any case, unless the freshness-seal logic 410 has previously been triggered (by an appropriate signal on line FI) to hold the enable line 411 high, and thereby bring the receiver chip 210 out of sleep mode.

2) A duty cycle generator 430 generates periodic duty cycle waveform, for an on/off ratio which can be programmed to be anywhere from 64/64 down to 1/64. (Whatever the ratio, the duration of the on-state is preferably at least 2 msec.) The duty cycle generator is enabled or disabled by a laser fuse 432. (For clarity, the Figure shows this fuse as a simple series connection. However, in practice, this fuse is actually used to control a gate which provides the desired logic state.)

3) An enable input (EI) can be driven by the data converter chip 220, to turn on the comparators 420 directly (if the freshness seal has been enabled). This input is particularly useful when the duty cycle feature is being used, since it permits the converter chip to override the duty cycle as soon as a data transaction begins.

4) While comparator 420A is active, it will provide digital outputs through OR gate 425, and AND gate 424 will cut off the output of comparator 420B. However, when no signal is detected at terminals A+/A- for at least three pulse periods, delay/integrator 423 will change state, enabling AND gate 424 to pass through the output from comparator 420B (and one-shot 422B).

The freshness input (FI) is used to seal or break receiver chip 210 power consumption activity. This input accepts 2 kHz pulse packets at a signal level greater than one Volt. When the seal is broken, comparators "A" and "B" continuously listen for activity at the inputs. When the seal is intact, no listening occurs and the receiver chip 210 enters a zero-power-consumption sleep mode.

Figure 4B shows details of the bandpass filter preferably used in the freshness seal logic 410. The input FI is connected to a first timing circuit 413, in which the time constant is determined by the RC time constant of a PMOS load element and a depletion capacitor. The output of this stage is connected both to a counting chain 415 and to a second timing circuit 414. The second timing circuit will add an additional time delay onto the delay of the first circuit, so that the output of the second circuit will have a lower cutoff frequency than will the output of the first timing circuit. If the second timing circuit is permitted to switch its output, it will reset the elements of the counting chain 415, and also block the outputs of the first timing circuit from clocking the counting chain 415. Counting chain 415 is combined with additional flip-flops 416 as shown, to perform the freshness-seal filtering and decoding function as described.

As shown in Figure 4A, the (optional) duty cycle generator 430 in the receiver chip 210 provides additional power savings.

Alternative Higher-Sensitivity Receiver Chip 210'

Figure 4C shows the analog portions of an alternative embodiment 210' of the receiver chip 210. This alternative embodiment does not have

as low power consumption as the primary embodiment 210, but does have much higher sensitivity.

Two chains of op amps are used. The first chain uses op amps 442 which have a relatively low slew rate, and require a relatively modest bias current. This chain monitors the 20 kHz wakeup frequency to detect wakeup signals. The second chain uses op amps 444 which have significantly higher slew rates, and correspondingly higher bias current requirements. The slew rates and reactance values of this chain are chosen to permit detection of signals at the write-data frequency, which, in the presently preferred embodiment, is 200 kHz. The first op amp chain, when active, uses 1 to 2 microamps of bias current, and the second op amp chain, when active, uses about 200 microAmps. Thus,it may be seen that a substantial power savings is achieved by shutting down the op amps 444 in the standby mode.

In Figure 4C, it should be noted that the series and feedback resistors are shown as variable resistors 448. These resistors, although not adjustable by the end user, do illustrate a further innovative teaching.

Figure 4D shows further details of the configuration of a single amplifier stage 444 with constant-multiplier-scaled arrays of feedback and series resistors. Note that the resistive elements 446' of the series resistor are scaled in powers of two, from a width/length ratio of 125 microns by 2 microns (nominal) up. The resistive elements 446' of the feedback resistor are also scaled in powers of two, but begin with dimensions of 625/2. Thus, the maximum value of the feedback resistance is five times as large as the maximum series resistance. As discussed above, this arrangement permits the resistance values to be "dialed in": once the designer has an appropriately scaled 6-bit (in this example) digital value for the resistances, he simply specifies that the fuses 446" corresponding to each "1" bit of the resistance are to be blown. In this example, the individual resistance elements 446' are polysilicon resistors, but of course a wide variety of other device technologies could be substituted.

Figure 4E shows further details of an active bandpass filter stage with constant-multiplier-scaled arrays of capacitors and feedback resistors. In this drawing, each of the individual capacitor elements 448' has equal capacitance. (In this example, the individual capacitor elements 448' is a 30 micron square polysilicon-to-polysilicon capacitor, but of course a wide variety of other device technologies could be substituted.) Note that the stage shown provides a one-pole bandpass filter function, and that selection of the values of the two capacitors 448 shown and of the feedback resistor 446 can select both the center frequency and Q of this active filter.

A bandpass filter stage is used, in combination with several op amp stages. The bandpass filter stage has a Q of about 5, with minimal gain. The individual op amp stages have respective gains of about 10, for a net total gain of about 10,000 at the center frequency.

The voltage gain V_{out}/V_{in} of the op amp stage will be equal to the ratio of the resistances $-R_F/R_{in}$, where the net resistance of the enabled elements of the feedback resistor is R_F, and the net resistance of the enabled elements of the input resistors is written as R_{in}.

The presently preferred embodiment provides such digitally scaled values not only for resistors, but also for capacitors. The trimmable resistors and capacitors are adjusted to set both the center frequency and Q of a bandpass filter. The mathematical relations which define the center frequency and Q of a bandpass filter as a function of the component values used are very well known to those skilled in the art. However, the use of digitally scaled selectable components, so that the desired component values can be directly "dialed in" is believed to be new in the art.

As is well known to those skilled in the art, the value of a thin film resistor can be changed by changing the width/length ratio of a layer of a given sheet resistance, by changing the film thickness of a material of a given resistivity, by modifying the thin film layer so that it has a different sheet resistance (e.g. implanting it with a dopant), or by substituting a

material with a different sheet resistance. The preferred embodiment simply uses pattern modifications, to provide a variety of width/length ratios.

The use of the bandpass filter in the analog input stages of the receiver chip 210' provides advantages of noise rejection. In the all-digital (and preferred) embodiment, noise rejection can optionally be increased by increasing the Q of the (passive) antenna circuit, or by using a filter function which includes poles at two closely spaced frequencies within the passband, or by other passive filtering options well known to those skilled in the art.

Converter Chip 220

This integrated circuit, in the portable data module 120, performs the function of 2-wire to 3-wire conversion. The one-wire bus 215 provides pulse bursts as inputs to converter chip 220. (This one-wire bus 215, together with the transmitter control output from the converter chip 220, may be regarded as a two-wire bidirectional bus.) Converter chip 220 decodes these pulse bursts, and drives serial bus 206 accordingly.

The converter chip 220, as configured in the presently preferred embodiment, is a low-power CMOS integrated circuit which accepts pulse packets at the input, and interprets these signals to control bidirectional data transfer on a 3 wire serial bus 206. The converter chip 220 also controls an output pin RFOUT, which is switched, when data is being read from the serial bus 206, in accordance with the data seen. This output pin is preferably used to control a simple VHF/UHF transmitter 240, but alternatively the RFOUT signal can be connected to gate a variety of transmitting devices.

Alternatively, the touch-contact port 270 can be connected, as a bidirectional interface, so that the converter chip 220 both receives 100 kHz pulse packets from port 270 (instead of from receiver chip 210), and also returns data to port 270 (instead of keying the transmitter 240).

The converter chip 220 also provides stretched clock and DQ signals. These signals facilitate synchronization to work with a microprocessor.

The detailed circuit implementation described below contains features which support various of the alternative embodiments discussed. However, it should be realized that these features can be omitted if desired, and in fact several of the disclosed features are not used in the preferred embodiment as presently practiced (although it is contemplated that it will be desirable to restore these features in future versions, at least for some applications).

In the presently preferred embodiment, a set of five commands is used, as detailed above. The pulse streams on the one-wire bus 215 (which are extracted by receiver chip 210 from the variable-length pulses on the 200 kHz RF channel, or are directly connected in from the touch-contact port 270) are counted. The count values are divided into classes by five boundary values B1, B2, B3, B4, and B5. In the presently preferred embodiment, boundary values B1-B5 are set at 5, 15, 25, 35, and 45, and the numbers of pulses sent by the base unit to transmit symbols A through E are 10, 20, 30, 40, and 50 respectively. The boundary values B1-B5 are independently selectable, by laser trimming, in the range from 0 to 255. Optionally, if noise margins allow, these numbers can be decreased to decrease transmit time. (For example, if boundary values B1-B5 are set at 3, 9, 15, 21, and 27, and the numbers of pulses sent by the base unit to transmit symbols A through E are 6, 12, 18, 24, and 30 respectively, the gross data rate would increase by two-thirds, <u>if</u> the error rate did not increase.) Alternatively, in applications where high noise is likely, these boundary values B1-B5 can be increased.

A state diagram of the converter chip 220 is shown in Figure 5G. This shows how the converter chip 220 will react to all possible pulse train sequences on the one-wire bus 215. This diagram can be explained in three divisions.

The first division is the inactive state (represented as <u>000</u>). In this state the converter chip 220 drives lines RST*, DQ, and CLK (of the

serial bus 206) low, and turns off the 300 MHz oscillator 240 (except when arriving at state 000 from Beacon state 011). Pulse classes E and F (45 pulses or more, and inactivity for 2 msec) will always send the converter chip 220 to this state. (These pulse classes are also represented as "t1500" and "t200P" in the wiring diagrams shown.)

The second division is the active state 100. In this state the converter chip 220 drives the RST* line high, pulses the CLK line, and drives data onto the DQ line (or loads data from the DQ line, depending on whether data is being read from or written to access control chip 230). The converter chip 220 will also turn on the 300 MHz transmitter 240 whenever a 1 is read out from the access control chip 230. Pulse class C (= signal t150) will always send the converter chip 220 to the active state 100.

The third division includes states 001, 010, and 011. A sequence of pulse classes DAB received by the converter chip 220 when it is in the inactive state 000 will put it into the first beacon state. In this state the converter chip 220 will pulse the 300 MHz oscillator on and off at a 5 kHz rate (laser programmable to 2.5 kHz, 10 kHz, 20 kHz, and 40 kHz). The pulsing will terminate in 200 msec or upon reaching active state 100. This beacon permits the base station's 300 MHz receiver to differentiate a valid key from background noise, when it is scanning the frequency range of 285-315 MHz looking for a key.

Once the converter chip has reached the active state 100, pulse groups A, B, and C (corresponding to internal signals t50, t100, and t150 respectively) will keep the converter chip 220 in this state. It is in this state that reading and writing of the access control chip 230 occurs. Following are the actions caused by the pulse groups A, B, and C when the converter chip 220 is in the active state 100.

A number of pulses C will cause the converter chip 220 to drive RST* low and then high, terminating any conversation with the access control chip 230 and initializing the access control chip 230 for the start of a new conversation.

A number of pulses B will keep RST* high while driving DQ and CLK so as to write a 1 to the key. The converter chip 220 will not turn on the 300 MHz transmitter, even though the access control chip 230 D0 line went high, since the converter chip 220 knows data is being written to the access control chip 230.

A number of pulses A will keep RST* high while driving DQ and CLK so as to write a 0, or read data, from the access control chip 230. The combination of the write-0 and read functions decreases circuit complexity and increases the speed of communication. In order to permit this combination of functions, the presently preferred embodiment makes the pull down strength of converter chip 220 much less than the pull up strength of access control chip 230. If the access control chip 230 is expecting to be written to, it does not drive the DQ line, so that the converter chip 220 can drive the DQ line. If the access control chip 230 is being read from, it will drive the DQ line with data while CLK is low. If a "0" is read from the access control chip 230, the waveforms are identical to those above, since the converter chip 220 and access control chip 230 both drive DQ to ground. However, if a "1" is read from the access control chip 230 the converter chip 220 and access control chip 230 will contend when CLK is low, with the access control chip 230 winning. Note that out of all three cases of Write 0, Read 0, and Read 1, the only time DQ went high while CLK was low was during the Read 1. If DQ goes high while CLK is low, the 300 MHz transmitter 240 is turned on, sending a 1 to the base station 110. The 300 MHz transmitter 240 will turn itself off after about 150 microseconds. In an alternative embodiment, the transmitter 240 will also be turned off by the fourth rising edge of the 200 kHz signal presented to the converter chip 220.

Following are descriptions of some of the pin connections and signal names used in the presently preferred embodiment of this chip:

V_{BAT}: This input is designed to be connected to a lithium battery with a voltage range between 2.5 and 4 volts. When VCCI is grounded, the converter chip 220 acts as a battery operated device, and power is supplied from the V_{BAT} pin at all times. The V_{BAT} input should be grounded if not used.

VCCI: This input is designed to be connected to a power supply with a voltage range of 4.5 to 5.5 volts. This voltage input is switched to the VCCO pin as long as VCCI is greater than V_{BAT}. However, when V_{BAT} is the greater, its voltage will be present at VCCO. When both VCCI and V_{BAT} inputs are used, the converter chip 220 is in the battery operate mode until VCCI becomes greater than V_{BAT}. VCCI should be grounded when not being used.

VCCO: This is a switched output, which will always be the greater of V_{BAT} or VCCI.

V_{REF}: This output pin represents the battery voltage input (V_{BAT}) less 0.6 Volts. It is designed to be connected to the battery input pin on the access control chip 230, or to such additional chips as a DS1207 TimeKey (TM) or DS1207 Electronic Tag.

PORT: This input/output pin provides an override for standard 2 to 3 wire converter. The port pin acts as an input pin for 100 kHz pulse packets containing both command and data input to the 3 wire serial port. Data is also output on the same pin when memory content is read via the 3 wire serial port.

STDQ: This output (stretched data) contains the same data as the serial port DQ pin. The difference is that the data output remains valid until the STCLK is transitioned high via an external source.

STCLK: This input/output (stretched clock) contains the same clock output as the serial port CLK pin. This pin differs in that an external source is required to drive the STCLK pin high after the converter chip 220 has asserted it high.

IN: This input accepts the 200 kHz pulse packets. In typical applications this pin is connected to the signal output pin of the receiver chip 210.

EN: This output pin is active high when the protocol shift register has received a command (including an appropriate match in the 16-bit chip-selection-tag field) to "wake-up." In a typical application this pin is connected to the enable pin EI of the receiver chip 210. In the embodiments where the duty cycle option of the receiver chip 210 is used for power conservation, this connection can be used to hold the receiver chip 210 on. The duty-cycle control logic (as will be discussed below) holds the receiver chip 210 active, during each active cycle, for at least long enough for the converter chip 220 to receive an enable command and activate this connection. This assures that, even in the maximum-efficiency duty cycle mode, it will be possible to detect an enable pulse and wake-up.

TRI: This input is used to tristate outputs CLK, RST*, and DQ. The TRI pin is active in high state.

DQTRI*: This input is used to tristate the DQ pin only. The DQTRI pin is active in the low state.

OUT: The OUT pin carries the data which is output from the 3 wire serial port. In a typical application this pin is used to key the RF transmitter which will send data back to a base station 110 via a 300 MHz loop.

RST*: This output signal is the reset-bar signal for the 3 wire serial bus 206. When RST* is at high level, the 3 wire port is active, and data can be written into or read from the serial bus.

CLK: This output signal is the clock signal for the 3 wire serial bus 206. This signal times data into and out of the DQ line of the 3 wire serial bus 206.

DQ: This input/output is the data input/output for the 3 wire serial port. In a typical application, RST*, CLK, and DQ connect directly to the RST*, CLK and DQ pins on the access control chip 230, memory

controller chip 260, data converter chip 220, or such other circuits as a DS1207 TimeKey (TM) or Electronic Tag.

GND: This pin is the ground pin for the converter chip 220.

Figure 5D shows a high-level overview of an alternative embodiment of the converter chip 220. This embodiment differs from the embodiment of Figure 5A in two major respects:

The alternative embodiment of Figure 5D does not have a 20 kHz input. Thus, this embodiment is suitable for embodiments where the low-frequency-wakeup protocol described above is not used.

This alternative embodiment also differs from the embodiment of Figure 5A in having the ability to enter (and awaken from) a sleep mode. A corresponding hardware difference is that this alternative embodiment has a protocol register 554.

In the organization shown in Figure 5D, the input select logic 506 selects between inputs from the data line of one-wire bus 215 and port 270. (Note that this logic can also divert the output of the beacon control logic 556 to provide an output to port 270 instead of to the transmitter 240.) The pulses from the selected input are provided to pulse counter 530, where they are deciphered into various action codes which affect the protocol shift register, the state machine, and ultimately the 3 wire serial bus 206.

When a signal is coming in over the write-data channel, the pulse packets received by the pulse counter 530 will have approximately a square-wave shape at 200 kHz, with a 50 microsec dead time after the last pulse in each packet. The pulse counter logic 530 watches for such dead time intervals, and then assesses the count value to determine what action to be taken, in accordance with the threshold values B1-B5. In addition, if the input to the pulse counter 530 is low (inactive) for longer than 2.0 msec, the converter chip 220 will time-out, reset the protocol shift register 554, and place the state machine 552 into an inactive state.

If a signal is incoming from the touch-contact port 270, the operation of the converter chip 220 is modified slightly. Due to the lower frequency

used for communication over the port 270, all time windows are doubled (except that the limit for timeout is kept at 2000 microseconds). If a read pulse packet is detected, time is allotted beyond the 100 microsec between pulse packets for the converter chip 220 to send out a one or a zero. This time is specified as a 400 microsec window. If a logic "0" is being sent, the port line will remain low for the entire window. If a logic "1" is being sent, the port line will be driven high within a maximum of 150 microsec. The port line is guaranteed to be inactive after a third 150 microsec time period.

Note that the specific circuit embodiment which will now be described does support the use of the 16-bit chip selection field, which, as mentioned above, is a desirable alternative not used in all embodiments. Those skilled in the art will readily recognize how this additional functionality can be disabled or designed out.

The pulse counter 530 will direct the interpretation of each packet of input pulses to one of two circuits. If a pulse packet of more than 44 pulses (i.e. a "50-pulse" packet) arrives at the pulse counter 530, the next 24 pulse packets are sent to the protocol shift register 554, and the state machine 552 is set inactive. (Thus, a 50-pulse packet always sets the state machine to inactive, regardless of any action which may have been occurring. This packet can be used to abort a current action/conversation.) The 24 pulse packets following a 50-pulse packet, which are routed to the protocol shift register 554, can command a normal wakeup, a masked wakeup, a read of the chip-select bits, a write of the chip-select bits, or a lock of the chip-select bits. The chip-select bits (in an incoming command) are the first 16 bits of the 24-bit protocol shift register 554. The last eight bits are the function field.

The state machine 552, which implements a state diagram as described above, receives inputs from the protocol shift register and also from the pulse counter 530. The outputs of the state machine control the three lines RST*, D/Q, and CLK of the serial bus 206. Another output of the state machine 556 also activates the beacon control logic 556, which

provides outputs to the transmitter 240 and to the multiplexer (input select logic) 506. The state machine 552 can also use the D/Q line as an input.

The D/Q and CLK lines are also connected to stretch circuit 558, which generates STDQ and STCLK signals as described above. The STCLK and STDQ pins are similar to the CLK and DQ lines: when CLK goes low, the STCLK line is also pulled low by the converter chip 220. This signal tells a monitoring device (such as a microprocessor) that the STDQ pin contains data, and that this data matches the data on the normal DQ pin. When the normal CLK goes high, however, STCLK and STDQ both remain valid. This allows time for a monitoring device to capture the data. Once the monitoring device retrieves data, the STCLK signal must be forced to a high level externally. In this manner the monitoring device will terminate the cycle, and the STDQ line will go to high impedance.

A power switching circuit 510 selects between alternative power supply inputs V_{BAT} and VCCI, to supply the internal power supply V_{DD} and a supply voltage output VCCO. This circuit also supplies a lowered supply voltage output V_{REF}, which provides power to certain downstream chips as discussed above. (The use of this reduced-voltage output means that, when the converter chip 220 drives the RST* line to full supply voltage, the downstream chips which use the V_{REF} output for their battery supply voltages will see an RST* voltage which is higher than their supply voltages.)

Figures 5A-5C show a much more detailed circuit diagram. Note that the protocol shift register 554, state machine 552, stretch circuit 558, and beacon control logic 556 are all shown implemented as control logic 550 in Figure 5A. For clarity, clock lines and miscellaneous timing logic (such as clock generators) are not separately shown.

Input buffers 502 receive incoming signals 507, 20KP (used, in alternative embodiments, to indicate that the receiver chip 210 is receiving

a signal on the wakeup frequency), DQ, DQOE, and TRIWIR. Output buffers 504 buffer output signals DQ, CLK, and EN.

Counter logic 530 receives the data from line 507 (which will usually be connected to the data line of the bus 215), and also receives the 20KP signal (which indicates when the currently incoming data was received on the wakeup frequency rather than the write-data frequency).

The incoming digital pulses are expected to have symmetrical high and low durations of about 2.5 microsec (± 20%). The minimum quiet time required for the converter chip 220 to recognize the end of one pulse packet and the beginning of another is 50 microsec. Conversely, if another pulse occurs after less than 10 microseconds of quiet, this pulse can be recognized as a continuation of the previous packet. If an idle period (with no pulses) of 2.0 msec occurs, the protocol shift register 554 will initialize and the state machine will go inactive. Quiet intervals of about 100 nsec or less may not even be noticed by the converter chip 220. Pulse packets range from 10 pulses to 50 pulses, depending on the action to be taken. If a read pulse packet is detected, data is to be read from a device connected on the 3 wire serial bus 206, and the output pin will become active high for a logic one or remain low for a zero. Time is allotted beyond the 50 microsec between pulse packets for the converter chip 220 to send out a one or a zero. This time is specified as a 225 microsec window. If a logic "1" is being sent, the out pin will be driven to high level within a maximum of 75 microsec and will remain high for a minimum of an additional 75 microsec. However, if a minimum of four 200 kHz pulses are received at the 200 kHz input, the RFOUT pin activity is terminated on the assumption that a logic one has been received and the sending unit has started the next pulse packet. The RFOUT pin is guaranteed to be inactive after a third 75 microsec time period.

When counter logic 530 detects a gap of 50 microseconds or more, which would indicates the end of a pulse packet, the counter 530 drives a data-valid line DV, compares the current count value against various

threshold values, and updates the threshold output lines 531. Note that lines 531 are not simply counter output bits, but represent the results of multiple comparison tests. As noted above, the boundary values B1-B5 are separately laser-programmable, and the lines 531 represent the separate logical results of magnitude comparisons between each of these boundary values and the count value for the latest completed pulse packet. The counter 530 also provides another output (not shown), indicating that a quiet delay long enough to cause timeout (set to 2 msec, in the presently preferred embodiment) has been detected.

Wakeup logic 520 receives the highest bit of the comparison bits 531, and also receives the signal 20KP to detect activity on the wakeup frequency. Wakeup logic 520 performs the wakeup-frequency decoding mentioned above. This capability is used in the alternative embodiment which uses the more sensitive receiver chip 210' of Figure 4C, with signalling on a lower wakeup frequency used to initiate all transactions. When the module 120 is in standby mode, signals received on the wakeup frequency are amplified by receiver chip 210, to provide pulse bursts on the one-wire bus 215. Converter chip 220 counts pulses in the pulse trains of the wakeup-frequency signal, in a manner which is analogous to its operation for pulse trains received on the write-data frequency. (However, note that, when the pulse packets are derived from a wakeup signal, the individual pulses will have a high-state duration which is equal to half the period of the RF carrier at the wakeup frequency, instead of half the period of the RF carrier at the write-data frequency.) The converter chip 220 counts these pulses, and measures them against a pulse count boundary B0. A stream which has fewer pulses than B0 is considered a "0", while greater than or equal to B0 pulses is considered a "1". The value of B0 (like that of boundary values B1-B5 discussed below) is laser trimmable from 0 to 255. If no laser trim is used, B0 will be equal to 20. In the present system, 10 pulses will be used to send a 0, and 30 pulses to send a 1 with B0 set at 20. (Optionally, if noise and error margins allow, these numbers can be decreased to decrease transmit

time.) The converter chip 220 looks at a moving window of bits received at 20 kHz as described above. When the last bit of a pattern B9 (10111001) is received, the converter chip 220 will enable the 200 kHz receiver of the receiver chip 210. When the last bit of a pattern 6D(01101101) is received, the converter chip 220 will disable the 200 kHz receiver of the receiver chip 210. If no 20 kHz or 200 kHz signal is received by the converter chip 220 for at least 2 msec, the converter chip will disable the 200 kHz receive operation.

Figure 5B shows details of the power switching circuit 510. Note that this circuit can actually accommodate two system supply voltage inputs VCCI, in addition to the battery voltage input V_{BAT}. Comparator 512A tests supply voltage input $VCCI_1$, to see whether it is greater than the battery voltage V_{BAT}. Comparator 512B tests supply voltage input $VCCI_2$, to see whether it is greater than the battery voltage V_{BAT}. The large switching transistors 513 are controlled in accordance with the logical outputs of these comparators:

If voltage $VCCI_2$ is greater than the battery voltage V_{BAT}, then the on-chip supply voltage V_{DD} and the supply voltage output VCCO will both be connected to $VCCI_2$ and disconnected from $VCCI_1$ and V_{BAT}.

If voltage $VCCI_1$ is greater than the battery voltage V_{BAT} AND voltage $VCCI_2$ is NOT greater than the battery voltage V_{BAT}, then the on-chip supply voltage V_{DD} and the supply voltage output VCCO will both be connected to $VCCI_1$ and disconnected from $VCCI_2$ and V_{BAT}.

If neither voltage $VCCI_1$ nor voltage $VCCI_2$ is greater than the battery voltage V_{BAT}, then the on-chip supply voltage V_{DD} and the supply voltage output VCCO will both be connected to V_{BAT} and disconnected from $VCCI_1$ and $VCCI_2$.

The capability to use two alternative power supply inputs, in addition to the battery voltage input, helps to allow system flexibility. Moreover, this is a desirable safety feature, since it helps to minimize the risk of cross-connection of separate power supply sources (which could cause damaging high currents), without wasting power in diode drops.

The reduced-voltage output supply V_{REF} is generated by one or two bipolar transistors 511. (The second transistor is connectable, by a laser option, to provide a Darlington pair.) As noted above, this provides a V_{REF} output which is about one diode drop (or two, depending on the laser option just mentioned) below the on-chip supply. However, to minimize power dissipation in these bipolar transistors, logic is used to condition the V_{REF} signal so that V_{REF} remains equal to V_{BAT}, unless the reset signal goes high and both the system supply voltage inputs $VCCI_1$ and $VCCI_2$ are low.

The configuration shown is also advantageous for safety reasons. In embodiments like that shown in Figure 2D, where a data cartridge can be externally powered during fast readout operations, conflicts between the two power supplies must be avoided. For example, Underwriters' Laboratory (UL) rules require that, in a system which has both a battery supply and a connection to receive external power, two elements must go bad before the battery can be directly charged by the external power supply. (This rule is intended to avoid catastrophic failure due to overcurrent and/or overvoltage in the battery.) One element which can be used to protect the battery is a substantial series resistance, e.g. 5 or 10 kilohms, in series with the battery. However, this series resistance cannot be used when the device is actually being powered by the battery. Thus, in the embodiment of Figure 5B, the control signal to switch power supply sources is first tied to the gate of the the device which switches in the battery. If VCCI is less than V_{BAT}, the battery will not be charged. If VCCI is greater than V_{BAT}, the gate of the battery-switching device will be high. If a failure occurs, so that the gate of the battery-switching device goes low, the resulting voltages will ripple through the circuit to the V_{CC}-switching device, and turn it off.

The converter chip 220, in the presently preferred embodiment, can work off of a battery supply as low as 2.5 volts. However, if an alternative supply is available, it can be connected to the $VCCI_1$ or $VCCI_2$

inputs. (To avoid disturbing the switching transistors 513, any unused supply input VCCI should preferably be grounded.)

Figure 5C shows the presently preferred embodiment of the state machine 552. Note that three outputs of the state machine control the bus 206. (Three other lines are assigned to receive signals from the serial bus 206.) The RST* pin on the serial bus 206 is driven high whenever a 30-pulse packet is received by the state machine. The RST* signal remains high until a 40- or 50-pulse packet is received, or until 2.0 msec has elapsed without activity at the 200 kHz input. The CLK pin on the converter chip 220 is normally low, and will remain low until the RST* signal goes high. When RST* goes high, and a 10- or 20-pulse packet is received by the state machine (indicating a "read from" or "write to" the 3 wire port), the CLK pin is driven low for a period of 500 nsec minimum to 1 microsec maximum. If data is being read from a device on the 3 wire serial port, it will become valid within 200 nsec of the falling edge of the clock, and remain valid until the clock returns high. This data is transferred to the RFOUT pin after a time delay of 75 microsec maximum. The output will be a high level for a logic one or remain at low level for a logic zero. If data is being written to a device on the 3 wire serial port, then data will be sent from the state machine to the DQ line on the falling edge of the clock. This data will remain valid beyond the time when the clock transitions back to the high level. The RFOUT pin remains low while data is being written to the 3 wire serial port. Note that, if multiple addressable devices are to be attached to the serial bus 206, some sort of addressing protocol will have to be added.

The state machine includes three flip-flops 560, which implement the 8-state diagram of Figure 5G. Note that inputs on lines E or F (signals t200p and t1500) reset the flip-flops 560, and all other inputs clock the flip-flops. Reset logic 562 generates an output signal on line RST* (of bus 206) under the appropriate conditions. Two one-shots are also provided, to drive pulses, under the appropriate conditions, onto lines CLK and DQ of bus 206.

Figure 5E shows the timing relations used, in the presently preferred embodiment, to implement the pulse counter 530. A rising pulse edge (of the pulses derived from the one-wire bus 215) resets the counter (at the time shown as t_{E1}), and causes a decode enable signal to go low. When the pulse burst ends (i.e. at time t_{E3} when no further rising edges have been seen for a predetermined delay time t_{DELAY} after the last rising edge time t_{E2}), the decode enable signal is again brought high. (The delay t_{DELAY} provides setup time, so that the count value, which has been valid since the rising edge of the last pulse, can ripple through the magnitude comparators.) When the next rising edge occurs, at time t_{E4}, the decode enable signal will again go low.

Figure 5F shows the magnitude comparator which is preferably used in the pulse counter 530, to rapidly threshold the pulse-count values against the preset thresholds. Note that this is a ripple-through architecture, where the highest boundary values are tested first. The small cell which is used at each stage provides both "greater than" and "equal to x" outputs. Only three stages are shown, although eight stages are used in the presently preferred embodiment (and of course more or fewer stages could be used instead).

Figure 8 shows how the converter chip, in the presently preferred embodiment, controls its power-supply output line to help other chips receive data from the serial bus. Note how the V_{REF} output is driven opposite to the RST* signal.

Alternative Embodiment: Use of Chip Selection Bits for Masked Wakeup

The logic which permits the base station 110 to identify which portable units are nearby, and to access a desired nearby portable unit, will now be described.

Normal and Masked Wakeup

The only difference between normal wakeup and masked wakeup is the number of chip-select bits which must be matched to wakeup the state machine. For example, if a function code indicates the use of all chip-select bits, then all 16 bits must be correctly matched to enable the main state machine. The following step by step procedure will illustrate normal and masked wakeup.

1. First a 50-pulse packet is sent to the IN pin which puts the state machine into an inactive state.

2. Issue a wakeup or masked wakeup command, by sending the 8 bit function code followed by the 16 chip-select bits which are proper to enable the state machine. The protocol register is always loaded by sending write zeroes (10-pulse packets) or write ones (20-pulse packets). The loaded pulse packets are compared to values stored in the 8 bit function Code Table and the previously stored 16 chip-select bits (storing the chip-select values will be covered later). When masking is being used, the first entered bits (LSBs) are the last to be masked. For example, Bits 0 and 1 will be the only bits unmasked if "mask 2-15" is selected. Pulse packets of 25 to 44 pulses are ignored when loading the protocol shift register 554. A pulse packet of greater than 45 pulses always initializes the protocol shift register 554 back to starting with the LSB and aborts any previous transaction. The state machine is also set inactive. After the first 24 bits are received and a valid wakeup is decoded, the protocol shift register 554 will no longer allow data bits to be written into it and the enable output will become active and remain active until another 50-pulse packet is received to reinitialize. Subsequent pulse packets which are received will be directed to the state machine with action taken corresponding to the number of pulses received as shown in Table 1.

3. A pulse packet train of 40-pulse packet, followed by a 20-pulse packed, followed by a 10-pulse packet enables the beacon mode of the state machine. Beacon mode turns on and off the out pin at a 5 kHz rate for 100 msec. This signal can be used (for example) to key

a transmitter, which allows a base station 110 to lock onto the transmitted beacon.

4. The converter chip 220 is now put into the active state by issuing a 30-pulse packet which takes RST* high on the 3 wire serial port. This same 30-pulse packet also turns off the beacon if it has not already timed out. With reset high a conversation can now take place between devices placed on the 3 wire port (such as Access control chips 230, memory controller chips 260, or such other circuits as a DS1207 TimeKey (TM) or Electronic Tag) from the 200 kHz input and data is returned to the sending unit via the out pin. As 200 kHz pulse packets continue to be received, the devices attached to the 3 wire port will be written and read using 10-and 20-pulse packets and reset with a 30-pulse packet. When data is read from the 3 wire port, it is always sent to the out pin for transmission back to the sending 200 kHz unit.

5. If a 200 kHz 40-pulse packet is received, the state machine will go to an inactive state but still remain alert for new 200 kHz pulse packets.

6. If no 200 kHz pulse packets are received for more than 2.0 msec, the converter chip 220 will time out, initialize the protocol shift register 554, and set the state machine back to the inactive state. The converter chip 220 now waits for new 200 kHz inputs to the protocol serial shift register which begins with a 50-pulse packet.

Reading the Chip-select Bits

The 16 bit CS value stored in the protocol shift register 554 can be determined in several ways. In fact, an exhaustive search could be implemented with a trial and error method which would eventually eliminate all but the correct bit pattern. Obviously, this method is painfully slow as 2^{16} possible combinations may need to be tried. In a similar but much more expedient manner, mask bits can be used in a successive approximation manner to determine the value of the CS bits. This procedure is accomplished by gradually increasing the size of the

unmasked chip-select fields as each set of bits are identified. However, the simplest method of determining the 16 bit CS value is to read the 16 bit value directly. The following step by step procedure will illustrate how to read the chip-select bits.

1. Wakeup the converter chip 220 using the mask-all function code. This is accomplished by sending a 50-pulse packet followed by 24 10-pulse and 20-pulse packets. In the protocol used, the least significant bits are transmitted first. The command format preferably used therefore transmits the command code for the desired action first. Thus, in this example, the first 8 pulse packets must match the mask-all function code. The next 16 packets, which are the chip-select field, may be any combination of 10- and 20-pulse packets (since the 16 CS bits are masked). Next, the beacon mode of the state machine is enabled by sending a 40-pulse packet followed by a 10-pulse packet followed by a 20-pulse packet. The beacon mode must be enabled when using an RF link with a scanning receiver, as the beacon will allow the receiver to lock on to the transmitter frequency. If the port pin is used directly or if the out pin is read directly or indirectly by a non-scanning device, this step can be omitted. Finally, if the beacon mode has been enabled, it should be disabled after receiver lock on by sending a 30-pulse packet to the IN pin.

2. Now load the converter chip 220 protocol shift register 554 with the read-CS-bits function code. This is accomplished by sending a 50-pulse packet, followed by 24 10-pulse and 20-pulse packets. Again, the first 8 pulse packets must match the read CS bits function code, but the next 16 pulse packets may be any combination of 10- and 20-pulse packets. During the 24 bit protocol shift register 554 load, pulse packets of 30 and 40 pulses are ignored. As usual, pulse packets of 50 pulses will initialize the protocol shift register 554 and set the state machine inactive.

3. If the 8 bit function code in the protocol shift register 554 is correctly matched, the next 16 bits will be read at the out pin for each 10-pulse packets (read) at the IN pin. If more than 16 read pulse packets

are sent to the IN pin in this mode, the converter chip 220 will start over again reading the CS bits, beginning with the first bit. Pulse packets of 20, 30, or 40 pulses are ignored, and 50-pulse packets will initialize the protocol shift register 554 and set the state machine inactive.

4. During the entire CS bit read operation, the state machine is disabled. All pulse packets except the 50-pulse packet are ignored. As usual, the 50-pulse packet or a time-out of 2.0 msec will initialize the protocol shift register 554 and return the state machine to inactive.

Storing the Chip-select Bits

In order to store a new value into the chip-select bits of the protocol shift register 554, it is necessary to know the existing stored value. In addition, if the lock bit is set, a new value for the chip-select bits cannot be stored unless power is removed and reapplied. The lock function is only useful in applications where power is permanently applied or removed by exception. The existing value of the CS bits should be obtained using the "Read Chip-select Bits" described earlier. After obtaining the existing chip-select values, a new value can be entered by using the step by step procedure which follows.

1. Load in the proper 24 bit pattern into the protocol shift register 554 for storing the chip-select bits. This pattern consists of 24 10-pulse and 20-pulse packets. Any 30- or 40-pulse packets will be ignored. As always, 50-pulse packets will initialize the protocol shift register 554 and set the state machine inactive.

2. If the 8 bit function code and the 16 CS bits are correct, the next 16 pulse packets will store a new CS value, overriding the old CS bits. Only 10-pulse and 20-pulse packets are accepted. Larger pulse packets are ignored, and 50-pulse packets cause the stored CS value to abort, initializing the protocol shift register 554 and return the state machine to inactive. The converter chip 220 does not lock up after 16 pulse packets are sent in this mode. If more packets are sent, the new

packets will continue to shift in, storing the last 16 packets that are received.

3. During the entire store CS bits operation, the main state machine is disabled. All pulse packets received will have no effect on the state machine except the 50-pulse packet, which will initialize the protocol shift register 554 and return the state machine to an inactive state. A time-out of 2.0 msec will have the same effect as a 50-pulse packet.

Locking the Chip-select Bits

The design of the converter chip 220 allows for both battery backup and battery operation. The device also consumes only modest amounts of power. As a result, most applications for this device are permanently powered and memory elements within the device, like the protocol shift register 554 CS bits, are nonvolatile. A special latch is provided so that upon initial power up (when battery is first connected) the nonvolatile chip-select bits can be written with a store CS function code. The CS bits can be changed as often as desired, using the store function until a lock CS function code is issued. Once sent, the value of the chip-select bits cannot be changed until power is removed (battery disconnected) from the converter chip 220. The lock CS bit can be accomplished by the following step by step procedure.

1. If the CS value is unknown, the procedure for reading the CS bits should be followed so that the value is known.

2. The 8 bit function code for locking the CS bits is then transmitted, followed by the 16 bit chip-select value, using 10- and 20-pulse packets. Only 10- and 20-pulse packets are accepted, and 30- and 40- pulse packets are ignored. A 50-pulse packet will cause the lock CS bits to abort, initializing the protocol shift register 554 and returning the state machine to the inactive state.

3. Once the 24 bit protocol shift register 554 is loaded with an exact match for the CS bits and the lock CS function code, the latch is set automatically and no further action is required.

4. The only way the latch can be reset is to remove power (the battery) from the device. During the lock-CS operation the main state machine is disabled, so that all pulse packets have no effect on the state machine. As usual, a 50-pulse packet or a time-out of 2.0 msec will initialize the protocol shift register 554 and return the state machine to inactive.

Digital AGC Feedback

The presently preferred embodiment does not include any automatic gain control circuits (AGC) stages, although these are frequently used, and recognized as being useful, in RF communication systems. Normally AGC is implemented using analog amplification stages, which are controlled by feedback to reduce their gain when large incoming signals are overloading subsequent circuits. As noted above, the micropowered receiver circuits of the presently preferred embodiment do not use any analog amplification, since such circuits tend to consume power.

However, an alternative embodiment, shown in Figure 4F, uses a digitally controlled automatic gain control, which does not consume any additional power. This is very advantageous, since it reduces the risk of short-range RF communications being disrupted in high-noise environments, or in environments where a remote module can hear multiple base stations.

In the primary preferred embodiment, when the counter 530 receives an extremely long pulse train it simply saturates at its maximum count value (255 in this embodiment). However, in this alternative embodiment, the counter 530 provides an overflow-indicating pulse to a current-source-control counter 470. This current-source-control counter provides control signals to a split current source in the comparators 420 at the input to the receiver circuits.

The current source in the input comparators in the receiver circuits is the primary location of standby power dissipation in the presently preferred embodiment. Therefore, the size of this current source is a

critical parameter in designing the remote module: if the comparators are redesigned to draw more current, the sensitivity of the receiver circuits will be increased, but the battery lifetime will be decreased. Thus, in the presently preferred embodiment (using a 190 mA-hour battery), the current sources have been designed for the maximum current draw which can reliably be accommodated by the battery lifetime. (As mentioned above, this current draw is a few microAmps total.) In the presently preferred embodiment, these current sources are conventionally configured using a CMOS current mirror circuit which controls an NMOS driver (current source) device.

These considerations indicate a maximum size for the current source, but do not indicate a minimum size. Therefore, in this alternative embodiment, the channel width of the current source device is divided up between several devices in parallel. For example, where the maximum device width is W, this device width can be allocated into four parallel current-source devices 461 having widths of W/15, 2W/15, 4W/15, and 8W/15. (Alternatively, of course, the total width can be divided up differently, to achieve whatever relation between digital control input and the analog sensitivity is desired.)

Thus, this embodiment provides a significantly different current source for the comparators 420. The individual driver elements are each driven by the voltage output of a current-mirror circuit 465, just as the single driver element is in the current source of the primary embodiment. A switching transistor 463 is placed in series with each of these current-source devices 461, and a four-bit down counter 470 is used as the current-source-control counter. The four output bit lines 472 of the current-source-control counter 470 are each connected to one of these switching transistors, to control one of the current-source devices. In the presently preferred embodiment, the current source device sizes are chosen so that the maximum current into the comparator is about 1.5 microAmps.

The effect of this is that the multiplier, defined by the ratio of the current-source device to the pull-down device in the current mirror, will be changed (as is well known to those skilled in the art of MOS circuit design) as the separate branches of the current-source device are switched in or out. For example, if the input side of the current mirror receives a current of one microAmpere, and drives this current through an NMOS device which is 5 microns wide and has its gate tied to its drain, the gate of this device can be connected to control the gate of a following NMOS device (with the same threshold voltage, gate oxide thickness, etc.), which will provide a current source. (The amount of current from this current source will be equal to the current on the input side of the current mirror, multiplied by the ratio of the widths of the two devices.) Therefore, in this example, the voltage from the input side of the current mirror can be used to control as many NMOS devices in parallel as desired. Each of these NMOS devices will source a current (into sufficiently low impedance) of 1 microAmpere times its width (in microns) divided by 5.

Thus, when the main counter saturates, the current-source-control counter is decremented, and the total channel width of the current sources in the input comparators 420 of the receiver circuits is reduced. This reduces the sensitivity of the comparators. Pulse counting continues, and if saturation occurs again the receiver sensitivity is decremented again.

A further feature of this embodiment is the use of a slow timer circuit to recover from saturation. A simple RC timing circuit 474 with a long time constant (e.g. 1 to 10 seconds) is used to periodically reset the current-source-control counter. This assures that the portable module will be able to rapidly recover from saturation.

Note that this embodiment requires at least one additional control line between the circuits which are now on the converter chip 220 and the circuits which are now on the receiver chip 210. This line can be added into these chip designs if needed, or alternatively the receiver and converter chips can be combined.

In a further modification of this alternative embodiment, two stages of gain reduction are used when saturation occurs. First, as just discussed, the receiver gain is decremented whenever the pulse counter saturates. However, after such decrement operations have reduced the gain so that the system is not overwhelmingly saturated, an additional small decrement is performed to optimize reception.

This can be implemented, for example, by using an additional threshold bit, to show when counter values exceed some intermediate value. This intermediate value would be chosen to reveal saturation problems - for example, it might be set slightly higher than the length which would be seen if the intersymbol separation for the longest legal two-symbol sequence were missed.

A further alternative way to implement the digital AGC function is using transistors to selectably switch out individual elements of a resistor ladder. In this further alternative embodiment, a constant current source is used for the comparator, instead of the adjustable current source just described. Gain control is performed by dynamically scaling the RF input voltage, using a digital feedback circuit as described above. For example, in the preferred version of this embodiment, the input A+ would not be connected directly to the + input of the comparator 420A, but instead would be connected through a high-impedance resistor ladder to the - input of the comparator 420A. A third terminal on this resistor ladder (i.e. a "wiper" terminal) would be connected to the + input of the comparator 420A. The counter outputs would be connected to control transistors which switch the individual elements of the resistor ladder in or out. (Preferably two resistor arrays would be used, one between the A+ input and the + terminal of the comparator, and one between the comparator's + and - terminals. The digital inputs would each be connected to two pass transistors.) This embodiment is illustrated in Figure 4G. Note that the values of the resistor elements are scaled in multiples of 1.5, rather than in multiples of two. Preferably the total value

of the resistance between A+ and A- is large enough not to greatly degrade the Q of the circuit; for example, a resistance

The embodiment of Figure 4G may be advantageous in providing a wider range of gain control. Since the gain of the comparator varies as the square root of the bias current, the current sources might have to be scaled over a wider range than is practical to achieve the desired sensitivity range.

These two embodiments of automatic gain control can also be combined. For example, some bits of the counter output can be routed to switch a resistor array to scale the input voltage, while other bits of the counter output (for example, the most significant bits) are routed to switch the current input to the comparator as discussed above.

Access Control Chip 230

This integrated circuit, in the portable data module, implements addressing and security controls.

The access control chip 230, in the presently preferred embodiment, is a miniature security system which stores 64 bits of user definable identification code and a 64 bit password which protects 128 bits of read/write nonvolatile memory. This security subsystem enables the access control chip 230 to act, in effect, as an electronic key. The 64-bit identification code and the password are programmed into the access control chip 230 via a special program mode operation. After programming, the access control chip 230 follows a special procedure with a serial format to retrieve or update data.

Interface cost to a microprocessor is minimized by on-chip circuitry which permits data transfer with only three signals: CLK (clock), RST* (reset complemented), and DQ (data input or output).

Low pin count and a guided entry for a mating receptacle overcomes mechanical problems normally encountered with conventional integrated circuit packaging, making the device transportable and user insertable.

Operation - Normal Mode

The access control chip 230 has two modes of operation: the normal mode and the program mode. The block diagram (Figure 6A) illustrates the main elements of the access control chip 230 when used in the normal mode. To initiate data transfer with the access control chip 230, RST* is taken high and 24 bits are loaded into the command register on each low to high transition of the CLK input. The command register must match the exact bit pattern which defines normal operation for read or write or communications is ignored. If the command register is loaded properly, communications are allowed to continue. The next 64 cycles to the access control chip 230 are read. Data is clocked out of the access control chip 230 on the high to low transition of the clock from the identification memory. Next, 64 write cycles must be written to the compare register. These 64 bits must match the exact pattern stored in the security match memory. If a match is not found, access to additional information is denied. Instead, random data is output for the next 128 cycles when reading data. If write cycles are being executed, the write cycles are ignored. If a match is found, access is permitted to a 128-bit read/write nonvolatile memory. Figure 6B is a flow chart of the normal mode sequence.

Program Mode

The block diagram of Figure 6C illustrates the main elements of the access control chip 230 when used in the program mode. Note that, preferably, any change of password will cause the data memory to be wiped. This enhances data security.

To initiate the program mode, RST* is driven high and 24 bits are loaded into the command register on each low to high transition of the CLK input. The command register must match the exact pattern which defines program operation. If an exact match is not found, the remainder of the program cycle is ignored. If the command register is properly loaded, the entire RAM (all 256 bits) is pulsed to all zeros. The next 128

bits received are written to the identification memory and the password memory. Figure 6D is a flow chart of program mode operation.

Command Word

Each data transfer for the normal and program mode begins with a three byte command word. As defined, the first byte of the command word specifies whether the 128 bit nonvolatile memory will be written into or read. If any of the bits of the first byte of the command word fails to meet the exact pattern of read or write, the data transfer will be aborted.

For example, in the presently preferred embodiment, the 8 bit pattern for read is "01100010" (binary). The pattern for write is "10011101" (binary). The first two bits of the second byte of the command word specify whether the data transfer to follow is a program or normal cycle. The bit pattern for program is 0 in bit 0 and 1 in bit 1. The program mode can be selected only when the first byte of the command word specifies a write. If the program mode is specified and the first byte of the command word does not specify a write, data transfer will be aborted. The bit pattern which selects the normal mode of operation is 1 in bit 0 and 0 in bit 1. The other two possible combinations for the first two bits of byte 2 will cause data transfer to abort.

The remaining 6 bits of byte 2 and the first 7 bits of byte 3 form unique patterns, which allow multiple access control chips 230 to reside on a common bus. As such, each respective code pattern must be written exactly for a given device, or data transfer will abort. The bit pattern as defined by the user must be written exactly or data transfer will abort. The last bit of byte 3 of the command word must be written to logic 1 or data transfer will abort.

Reset and Clock Control

All data transfers are initiated by driving the RST* input high. The RST* input serves three functions. First, it turns on control logic which allows access to the command register for the command sequence. Second, the RST* signal provides a power source for the cycle to follow. To meet this requirement, a drive source for RST* of 2 mA at 3 Volts is required. However, if the V_{CC} pin is connected to a 5 Volt supply which is within nominal limits, then RST* is not used as a source of power. In this case, input levels will revert to normal inputs with a drive current requirement of 500 microA. Third, the RST* signal provides a method of terminating data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, the data must be valid during the rising edge of a clock cycle. Command bits and data bits are input on the rising edge of the clock and data bits are output on the falling edge of the clock. All data transfer terminates if the RST* pin is low and the DQ pin goes to a high impedance state. When data transfer to the access control chip 230 is terminated using RST*, the transition of RST* must occur while the clock is at high level, to avoid disturbing the last bit of data.

Dual Port Memory Controller 260

Figure 2D shows how the memory controller chip 260 is used in an alternative embodiment of the portable module 120. However, the memory controller chip has capabilities which can be useful in a wide variety of embodiments, including system embodiments which are not closely analogous to that shown in Figure 2D. The architecture and operation of this integrated circuit will now be described in detail.

The memory controller 260 is a dual-port memory controller, which permits three-wire serial port to interface to a bank of one or more byte wide static RAMs 262, yet maintains the existing byte wide port. Memory address space, in the presently preferred embodiment, of up to 512K can be addressed directly. (Therefore, a single controller 260, in the presently

preferred embodiment, can provide dual-port interface to a bank of 512 kbytes of memory, e.g. 16 32K-by-8 SRAMs.) Arbitration between the serial and byte wide port is accomplished either by handshaking or by using predictable idle time as an access window. The serial port requires a six byte protocol to set up memory transfers. Cyclic Redundancy Check circuitry is included to monitor serial data transmission for error.

Of course, the disclosed architecture can readily be modified for use with by-9, by-4, by-16, or other memory organization if desired. If a wider memory organization than that built into the controller 260 is needed - e.g., in this example, if a by-16 organization is needed rather than by-8 - the parallel ports of multiple controllers can easily be parallelled. In this case the serial port access would need to be multiplexed over the multiple controllers (either by additional controllers or otherwise), but the parallel system port could simply be split.

Pin Descriptions

The presently preferred embodiment will be described with reference to the following pin and signal designations:

RST*: This pin provides a selection signal input to the serial port 705 (at serial port buffer 706). (In the presently preferred system embodiment, the serial port 705 is connected to the serial data bus 206 in portable module 120.) When RST* is low, all communications to the serial port are inhibited. When high, data is clocked into or out of the serial port.

CLK: The clock input signal is used to input or extract data from the three-wire serial port 705. A clock cycle is defined as a falling edge followed by a rising edge on this line. During read cycles, data is driven out onto the bus 206 after a falling edge. During write cycles, data is latched into the port on the rising edge.

DQ: This is the bidirectional data signal for the 3 wire serial port 705. Valid data will be read from the DQ line, while RST* is high,

on the low to high transition of the CLK signal, if the data is stable on the DQ line with the proper setup and hold times.

DQE: The DQE output signal is active (high level) whenever the 3 wire serial port buffer 706 is driving the DQ line. Therefore, this pin will be high whenever data is being read from the controller 260. Otherwise it will be low, and the DQ line will be an input to the controller 260. (This can be implemented by using the DQE line to command the other DQ drivers on the bus to go to a high-impedance state.)

$A0_{Sys}$-$A18_{Sys}$: These are the lines of system address bus 701A. These 18-bit addresses can specify one of 2^{19} (524,288, frequently written as "512K") locations for access.

$A0_{RAM}$-$A18_{RAM}$: Addresses supplied to RAM, on RAM address bus 703A. These signals allow access to up to 512K bytes of RAM controlled by the memory controller 260. The addresses are either derived from the system address bus ($A0_{Sys}$-$A18_{Sys}$), or from the protocol and internal binary counter provided by the 3 wire serial port and associated timing circuits.

$D0_{Sys}$-$D7_{Sys}$: These are the lines of system data bus 701D. This bidirectional bus is used to carry data to and from the parallel system bus and RAM.

$D0_{RAM}$-$D7_{RAM}$: Data supplied to or read from RAM 262 on RAM data bus 703D. During write mode, this data is either derived from the system data bus ($D0_{Sys}$-$D7_{Sys}$) or from the protocol and data stream provided by the 3 wire serial port and associated timing circuits.

The system control lines 701C provide control inputs CE_{Sys}* (chip enable), OE_{Sys}* (output enable (read))(for transfer of data from RAM to the parallel system bus), and WE_{Sys}* (write enable). If the system parallel port 701 has access to RAM 262, these control lines will be translated into the corresponding signals CE_{RAM}*, OE_{RAM}*, and WE_{RAM}* on RAM control lines 703C. If the serial port 705 has access, these control signals will be derived from a 56-bit protocol provided by the 3 wire serial port and associated timing circuits.

V_{CC}: +5 Volt power for the memory controller 260 (2 pins).

GND: Ground for the memory controller 260 (2 pins).

Operation

The block diagram of Figure 7A illustrates the main elements of the memory controller 260. The memory controller 260 performs two major functions: serial to parallel conversion (in converter 720), and access arbitration between the two ports (the serial port and the parallel port). Access is arbitrated, between serial port 705 and byte-wide parallel port 701, by address multiplexer 740 and data multiplexer 760. Arbitration is preferably controlled by signals from the 3 wire to byte wide converter 720. The 3 wire serial port 705, has priority in accessing the RAM. Accesses through the parallel port 701 are expected to "steer around" accesses through the serial port 705.

Interface to System (Parallel) Bus

If the RST* reset signal for the 3 wire serial port 705 is low (active), the byte wide parallel port 701 has immediate access to RAM 262. The system-derived control signals (CE_{Sys}*, OE_{Sys}*, and WE_{Sys}*) are buffered by the control signal buffer 702C and passed through by control line multiplexer 710, to provide CE_{RAM}*, OE_{RAM}*, and WE_{RAM}* respectively, which are connected directly to the control inputs of memory chip(s) 262. The byte wide parallel bus addresses ($A0_{Sys}$-$A18_{Sys}$) and control signals (CE_{Sys}*, OE_{Sys}*, and WE_{Sys}*) are buffered by the control signal buffer

702C, and passed through by the control line multiplexer 710 to provide outputs $A0_{RAM}$-$A18_{RAM}$, CE_{RAM}*, OE_{RAM}*, and WE_{RAM}* respectively, which are connected directly to the RAM memory chip(s) 262. The data input/output signals ($D0_{Sys}$-$D7_{Sys}$) are internally buffered and sent to RAM on the data input/output signals $D0_{RAM}$-$D7_{RAM}$. The buffering is designed to handle bidirectional data transfer. Data will be written from the byte wide parallel bus to RAM when CE_{Sys}* and WE_{Sys}* inputs are both active (low). The OE_{Sys}* signal is a "don't care" signal during a write cycle. Data is read from RAM via the byte wide parallel port when CE_{Sys}* and OE_{Sys}* signals are both low and WE_{Sys}* is high.

Interface to Three-Wire Serial Bus

If the RST* signal at the serial port 705 is high, the 3 wire to bytewide converter 720 takes control of the RAM, by switching the control/address/data multiplexers 710, 740, and 760. The converter 720 follows a 56-bit protocol, which is written serially from port 705, to determine the action required and also the starting address location in the RAM to be used. The last 8 bits of the 56 bit protocol give the value of a cyclic redundancy check byte (CRC). A correct value for this byte provides assurance that all bits of the 56-bit protocol have been received correctly. If the 56 bits of protocol have not been received correctly, further action will be aborted. The CRC check byte can detect up to three single bit errors within the 56 bit protocol, and can also be used on incoming and outgoing serial data streams to check the integrity of data being read or written.

Command Set for Interface to Serial Bus

In the presently preferred embodiment, the serial bus protocol can cause the memory controller 260 to perform any of the following eight actions:

Protocol Commands

1. Burst read
2. Burst write
3. Read protocol select bits
4. Write protocol select bits
5. Burst read masking portions of the protocol select bits
6. Read CRC register
7. Set the address arbitration byte location
8. Poll arbitration byte for status and control

The organization of the 56 bit protocol is shown in Figure 7B. As defined, the first byte of protocol determines whether the action which is to occur involves a read or write. A read function is defined by the binary pattern 11101000. This pattern, therefore, applies to commands 1, 3, 5, and 6 of Table 1. A write function is defined by the binary pattern 00010111. This pattern, therefore, applies to commands 2, 4, 7 and 8 of Table 1. Any other pattern which is entered into the read/write field will cause further action to terminate. (This provides further protection against transmission errors in the overhead bits.) Additional differentiation as to which read or write command is determined by the last five bits of the third byte of the protocol called the control field.

The control field bits, in the presently preferred embodiment, are as follows.

Control Field

Bits:	Command
00110	Burst read
10001	Burst write
00011	Read CRC register
10110	Set arbitration byte address to 00000 or 3FFFF
01001	Poll arbitration byte for access to RAM
00101	Read protocol select bits
01110	Write protocol select bits
11XXX	Burst read masking portions of the select bits

These commands are interpreted as follows:

A burst read uses a 19 bit address field (which includes the second and third bytes plus bits 0, 1, and 2 of the fourth byte) of the protocol to determine the starting address of information to be read from RAM. The byte of data resident in that location is loaded into the eight-bit shift register within the memory controller 260. The byte of data is then transferred from the shift register to the 3 wire bus by driving the DQ line on the falling edge of the next eight clocks with the LSB first.

A burst write uses the same 19 bit address field to determine the starting address of information to be written into RAM. Data is shifted from the DQ line of the 3 wire bus into an eight bit shift register within the memory controller 260 on the next eight rising clock edges. After a byte is loaded, the data is written into the RAM location immediately after the rising edge of the eighth clock.

Burst reads and writes will continue on a byte by byte basis, automatically incrementing the selected address by one location for each successive byte. Termination of a current operation will occur at any time when RST* is taken low. However, once a byte of data has been loaded into the shift register, the ongoing write cycle will be allowed to finish, even if RST* goes low during RAM write. This prevents corrupted data from being written into the RAM. If a full byte of data has not been

loaded into the shift register when RST* goes low, no writing occurs. Reads can be terminated at any point, since there is no potential for corruption of data.

The read CRC command provides a method for checking the integrity of data sent over the 3 wire bus. The CRC byte resides in the last byte (Byte 6) of the protocol. The eight bit CRC byte not only operates on the protocol bits as they are written in, but also on all data that is written or read from RAM. After a burst read or write has finished and RST* has gone low, the final value of the CRC is stored in the memory controller 260. If a read CRC register command is issued, the stored CRC value is driven onto the D/Q line by the first eight clock cycles after the protocol is received. The CRC value generated by the memory controller 260 should match exactly with the value generated in the host system which is transmitting or receiving data on the other end of the 3 wire bus. If it does not, data has been corrupted and retransmission should occur.

It should be noted that the CRC for a previous transaction can only be obtained if a read CRC command is issued immediately after RST* goes low to reset the memory controller 260, then high to accept a read CRC command. If any other sequence is followed, an intermediate CRC will be generated and stored whenever RST* goes low again, destroying the CRC value of interest.

In any two port system there is a potential for access collisions. To solve this problem, an arbitration byte is provided so that the serial and parallel ports of the memory controller 260 can determine the status of the other port. A special byte in RAM address space is reserved to allow for handshaking between the two ports. This arbitration byte has a special attribute in that it is simultaneously accessible by both ports. Two commands are used by the 3 wire serial port protocol to manage the arbitration byte. First, since this byte will create a hole in RAM address space for the parallel byte wide port, a command is added to move the arbitration byte to either address location "00000" or address location

"3FFFF". When setting the arbitration byte address location, the correct read/write field and command field must be entered, along with a value for bit A0 of the address field. (A 0 moves the arbitration byte to 00000, and a 1 moves it to 3FFFF.) It is important to note that the arbitration byte is located in the parallel memory location assigned by the serial port using the appropriate commands. However, the physical byte of RAM is located within the memory controller 260. The existence of this physical byte is transparent to the bytewide parallel port and looks like normal RAM space with some write restriction. However, the serial port can still address the actual RAM location at either 00000 or 3FFFF in addition to accessing the arbitration byte. The second command used by the 3 wire serial port provides for polling of the arbitration byte to determine the status of the parallel port. In addition, the arbitration byte can be set to indicate to the parallel port at the serial port is taking over the RAM.

The second command protocol allows the serial port to do a compressed read-write-read operation, which causes the arbitration byte to be read by the first eight clocks following the protocol. The next eight clocks cause data to be written into the arbitration byte, and the last eight clock cycles allow for a second read of the data for verification. These 24 cycles are initiated by entering the 56 bit protocol only once. The protocol pattern entered is a write function in the read/write field (00010111), and the correct control field.

Two other commands are used to access the select bits in the protocol. Once the select bits are set to binary values, they must be matched exactly when protocol is sent by further activity is prevented. The bits allow for 65,536 different binary combinations. Therefore, many memory controllers can be connected on the same serial bus, and only the appropriate device will respond. To write the select bits, a write cycle in the read/write field is required along with the appropriate command in the command field. To read the select bits, a read cycle in the read/write field is required along with the appropriate command in the command field. The arrangement of reading and writing select bits allows the user

to have a large number of memory controllers in use and uniquely identify each. A read can occur successfully without knowing the select bits but a write cannot occur without matching the current select field.

A third command, masking specific select bits, provides a means for determining the identify of specific memory controllers in the presence of many memory controllers. A read in the read/write field and a "11000" in the command field will execute a burst (masked) read. This operation ignores all select bits, to permit a base station 110 to quickly determine the presence of any memory controllers. With the detection of at least one device, a search can begin by masking all but a single pair of memory controller select bits. A read in the read/write field and a "11001" in the command field will unmask the first two LSBs of byte 4 of the select bits (Figure 7C). With these two select bits unmasked, only an exact match of four possible combinations (00,01,10,11) of these two select bits will now allow access through the 3 wire port to RAM. Therefore, repeating the unmasking of the first two bits of the select field up to four times will give the binary value of these select bits. Having determined the first two select bits, the next two select bits can be unmasked, and the process of matching one of four combinations can proceed as before. In fact, repetition of unmasking select bit pairs will yield an exact match of 65,536 possible memory controllers in no more than 32 attempts.

Arbitration

As mentioned earlier, one byte of RAM has been reserved for arbitration between the 3 wire port and the bytewide parallel bus. The location of this byte within the memory map will be at address 00000 or at address 3FFFF (as determined by the protocol input from the 3 wire serial port).

The arbitration byte has special restrictions and disciplines so that the 3 wire serial bus and the bytewide parallel bus are never in contention for RAM access. The format of this byte, in the presently preferred embodiment, is shown in Figure 7D. In this embodiment, the serial port

705 can read the whole arbitration byte, but can only write bits S2-SO. The parallel port 701 can read the whole byte, but can only write bits P1-P0. An internal counter controls count bits C2-C0, which cannot be written by either port.

To access memory, in this scheme, the ports read the status bits, and write the bits over which they have control. If the serial port wants to access RAM, it polls the arbitration byte until bit P1 equals zero (indicating that the parallel port is not engaged in access). When P1 equals zero, the serial port then writes a one into bit S2. After writing bit S2, the serial port then reads the arbitration byte again, to confirm that P1=0 and S2=1. This operation must be executed with the protocol for the compressed read-write-read sequence which minimizes overhead. The 3 wire serial port should always abort any attempt to access RAM if P1 equals one. When the 3 wire serial port completes any transfer of data to or from RAM, Bit S2 should be written back to zero so that the bytewide parallel port will know that the 3 wire serial port is not using the RAM. The bytewide serial bus can gain access to RAM by polling the arbitration byte until S2 bit equals zero. When S2 equals zero, the bytewide parallel port then writes a one into bit P1. A read cycle verifying that S2 equals zero and P1 equals one confirms that the bytewide parallel port has access to RAM. The bytewide parallel port can then read or write RAM as required. When the entire transaction is complete, the bytewide parallel port should write the P1 bit to zero, signalling the 3 wire serial port that the RAM is not in use. The bits B0, S1, and S0 can be defined by the user definition to pass additional arbitration information making possible more elaborate handshaking schemes between two ports. Some typical uses for these bits could be an indication that a port desires access to RAM, or the amount of RAM.

An alternative method of arbitration can also be followed. In this alternative method, arbitration is accomplished by use of the count bits CO-C2. Due to the overhead protocol used for accesses on the serial bus 705, the serial port cannot read or write from RAM more often than once

in every eight clock cycles. Moreover, the internal counter (which is updated whenever another byte is loaded into the internal serial buffer) is organized so that it is certain that serial port accesses will only occur when the counter transitions from a "111" state to a "000" state. The serial port has access on these clock cycles, and the parallel port has access at all other times, regardless of the arbitration byte status bits. Since the 3 wire port always reads or writes at the ends of a byte (when bits C0-C2 are all equal to 1), the software which controls the bytewide parallel bus is never allowed to access the bytewide RAM bus at these times (when the count bits are all ones). The parallel port can determine the minimum time left before the 3 wire serial port will access the memory, by reading the count bits and the minimum clock cycle applied to the 3 wire clock input. Essentially the 3 wire serial port is given priority on access to RAM, and the bytewide parallel port determines when it can access the RAM to avoid colliding with the 3 wire serial port.

CRC Generation

The cyclic redundancy check byte is generated, within the controller 260, by a conventional configuration. In the presently preferred embodiment, as shown in Figure 7E, this logic includes an eight bit shift register, four exclusive-OR gates, and two sets of transmission gates. The transmission gates are connected so that the CRC Generator monitors the data stream from the DQ pin, and continually updates its internal parameters, without disrupting the serial data flow. The reset signal (RST*) must be high while the CRC Generator is being used, since an inactive state will disable the eight bit shift registers.

A CRC Generator for serial port communications can be constructed as described above to satisfy the memory controller CRC requirements. However, another approach is to generate the CRC using software.

Analysis of Power Efficiency

The portable module is a low power device capable of operating on one battery for ten years. The power dissipation of the portable module falls into two main categories: DC listening (or quiescent) power dissipation, and transient transaction power dissipation. "DC listening power dissipation" refers to the current used by receiver chip 210 to continuously monitor for the presence of a signal delivered to it by the receiving antenna network. The input comparator of receiver chip 210 operates with a current of 1.5 microA. In ten years this will consume a charge of:

$$Q_{DC} = 10 \text{ yr} \times 365 \text{ day/year} \times 24 \text{ hr/day} \times 0.0015 \text{ mA}$$
$$= 131.4 \text{ mA-hr} = 471 \text{ Coulombs (C)}.$$

This charge is the majority of the 190 mA-hr that the battery used in the presently preferred system embodiment can supply. The 58.6 mA-hr that is left can be used for data transfers to and from the portable module - referred to above as transient transaction power dissipation. The charge used by the portable module in data transfers is listed below.

Some charge is used by receiver chip 210 and converter chip 220 in amplifying and interpreting pulse packets. This charge is referred to below as $CVF_{210+220}$ and refers to the charge used to move the voltage on the capacitances in the chip. The total of the charge consumption of the two chips has been measured to be 25 pC/input pulse.

The oscillator in converter chip 220 that provides the 5 kHz modulation of the 300 MHz transmitter burns 20 microA when active. The converter chip 220, in the presently preferred embodiment, actually divides down an 80 kHz oscillator output to 5 kHz. A contemplated improvement will replace the 80 kHz oscillator with a 20 kHz oscillator, reducing the current by a factor of four to 5 microA.

The 300 MHz transmitter burns 120 microA when on.

As with receiver chip 210 and converter chip 220, there is charge used to move the capacitances in access control chip 230. This is referred to as CVF_{230} in the table below, and has a value of 25 pC/bit.

The RAM in access control chip 230 burns 500 microA when it is active. Converter chip 220 activates the RAM for 500 nsec when it accesses access control chip 230. This causes a charge consumption of 500 nsec x 500 microA = 250 pC/bit when the RAM is accessed. In a contemplated revision, the RAM sensing scheme will be redesigned to reduce this value to 25 pC/bit.

Whenever the RST* pin of access control chip 230 is high, access control chip 230 will sink 250 microA from it. (In a contemplated revision of access control chip 230 this value will be reduced to zero.)

Charge consumption components of portable module

Component	Present Design	Contemplated Revision
$CVF_{210+220}$	25 pC/input pulse	25 pC/input pulse
Beacon oscillator	20 microA	5 microA
300 MHz transmit	120 microA	120 microA
CVF_{230}	25 pC/bit	25 pC/bit
$RAM\text{-}acc_{230}$	250 pC/bit	25 pC/bit
$standby_{230}$	250 microA	0 microA.

To show how to use the component values in this table, a calculation of the charge used in a typical transaction follows. The transaction analyzed will consist of the following steps:

1) Wake up module 1
2) Send beacon protocol
3) Scan for beacon
4) Turn off beacon
5) Send protocol for access control chip 230
6) Data transaction with ID, password, and memory fields
7) Put module 1 to sleep.

After a calculation of charge used at each step, a table will summarize the results.

Step 1: Wake up module 1

To wake up module 1, 24 bits (16 bits of chip select and 8 bits of command) must be sent to converter chip 220. Assuming the data sent is 50% "1" bits and 50% "0" bits, and that the pulse packet sizes are 10 and 20 for a 0 and a 1 respectively this results in a charge consumption of:

$$Q = (12 \times 10 + 12 \times 20)\text{pulses} \times 25 \text{ pC/pulse}$$
$$= 9 \text{ nC.}$$

Step 2: Send beacon protocol

The beacon is enabled (turned on) by sending pulse packets of length 50, 40, 10, and 20. This results in a charge consumption of:

$$Q = (50 + 40 + 10 + 20) \text{ pulses} \times 25 \text{ pC/pulse}$$
$$= 3 \text{ nC.}$$

Step 3: Scan for beacon

In the present embodiment of the converter chip 220, 20 microA is burned when the beacon oscillator is running. The 300 MHz transmitter will burn 120 microA at a 50% duty cycle for an average current burn of 60 microA. Converter chip 220 and the 300 MHz transmitter thus burn a total of 80 microA when the beacon is operating. The scan time for module 1 will be estimated in this example to be that required to take 25 steps of 40 kHz each with a dwell time of 0.3 msec per step. This time is 25 x 0.3 msec = 7.5 msec. Thus the charge consumed is:

$$Q = 7.5 \text{ msec} \times 80 \text{ microA}$$
$$= 600 \text{ nC.}$$

In a contemplated modification of the converter chip, the beacon oscillator current will be reduced from 20 microA to 5 microA. When added to the 60 microA of transmitter current this gives a total current drain of 65 microA. Also, it is planned to increase the beacon frequency to 20 kHz. This reduces the dwell time at each frequency step to be 0.3 msec/4 = 0.075 msec and speeds up the scan by a factor of four. The bandwidth of the receiver is also planned to be increased, thus decreasing

the number of steps required. However, for this example the number of steps will be kept at 25. This results in a scan time of 25 x 0.075 msec = 1.875 msec which results in an improved charge consumption of:

Q = 1.875 msec x 65 microA
= 122 nC.

Step 4: Turn off beacon

Turning off the beacon requires sending a pulse packet of length 30. This causes a charge consumption of:

Q = 30 pulses x 25 pC/pulse
= 0.75 nC.

Step 5: Send access control protocol

The access control protocol is 24 bits long. Assuming a 50% density of "1" bits, as in step 1, receiver chip 210 and converter chip 220 will consume 9 nC as in step 1. In addition, access control chip 230 will consume 25pC/bit (RAM is not activated) and the RST* line being high will burn 250 microA for the length of the transmission. Assuming a 5 kHz data rate, the transmission will last 24 x 0.2msec = 4.8 msec. The total charge consumption will be:

Q = 9 nC + (24 bits x 25 pC/bit) + (250 microA x 4.8 msec)
= 9 nC + 0.6 nC + 1200 nC
= 1209.6 nC.

In a contemplated modification, access control chip 230 will not draw current from the RST* line, thereby removing the 250 microA x 4.8 msec component of charge above. The new design's total charge consumption will be:

Q = 9 nC + 0.6 nC
= 9.6 nC.

Step 6: Data transaction with access control chip 230

The combined number of bits sent to/from these fields is 256. Assuming a 50% 1's density, and the use of 10 and 20 pulses for a 0 and a 1 respectively, receiver chip 210 and converter chip 220 will consume 128 x (10 + 20) x 25 pC = 96 nC. Access control chip 230 will consume 256 x 25 pC = 6.4 nC of CVF charge and 256 x 250 pC = 64 nC of RAM access charge. The RST* line will cause a current burn of 250 microA for 256 x 0.2 msec (at an assumed 5 kHz data rate) = 12,800 nC. The combined length of the ID and memory fields is 192 bits. Assuming a 50% 1's density and that the 300 MHz transmitter is on for 200 microsec per bit, this results in a charge consumption by the 300 MHz transmitter of 192 x 50% x 200 microsec x 120 microA = 2304 nC. Thus the total charge consumption is:

$$Q = 96\text{ nC} + 6.4\text{ nC} + 64\text{ nC} + 12{,}800\text{ nC} + 2304\text{ nC}$$
$$= 15{,}270.4\text{ nC}.$$

In a contemplated modification, access control chip 230 will reduce the RAM access charge to 256 x 25pC = 6.4 nC from 64 nC. Access control chip 230 will reduce the 12,800 nC of RST* charge consumption to 0 nC. This will improve the total charge consumption to:

$$Q = 96\text{ nC} + 6.4\text{ nC} + 6.4\text{ nC} + 0\text{ nC} + 2304\text{ nC}$$
$$= 2{,}412.8\text{ nC}.$$

Step 7: Put module 1 to sleep

This is a 24 bit protocol sent to converter chip 220 which results in a charge consumption equal to that in step 1:

$$Q = 9\text{ nC}.$$

The results of these calculations are as follows:

Thus, the total charge used in the example transaction is 17,101.7 nC, using the present design, and 2,566.1 nC using the new design. This transaction is merely an example, which shows how the total charge consumption of a transaction can be calculated. Moreover, this calculation

Charge consumption of example transaction

Step	Present Design	Contemplated Design
Wake up module	9 nC	9 nC
Send beacon prot	3 nC	3 nC
Scan for beacon	600 nC	122 nC
Turn off beacon	0.75 nC	0.75 nC
Send access control bits	1209.6 nC	9.6 nC
Data transaction	15270.4 nC	2412.8 nC
Module to sleep	9 nC	9 nC
Total	17101.7 nC	2566.1 nC

gives some indication of the number of transactions, of this type, that could be performed within the available battery lifetime.

Of the 190 mA-hr in the battery, 58.6 mA-hr is available for transactions. Dividing the charge used per transaction into 58.6 mA-hr yields 12.3 million transactions for the present portable module (and 82.2 million transactions with modifications as set out above). By far the largest charge consumer in the present design is the RST* current to access control chip 230 in standby mode, followed by the use of the 300 MHz transmitter to send data. Thus, a rough (but conservative) worst case estimate would be at least one million worst case transactions out of the portable module. This is 100,000 transactions per year, or 274 transactions per day.

Further Modifications and Variations

It will be recognized by those skilled in the art that the innovative concepts disclosed in the present application can be applied in a wide variety of contexts. Moreover, the preferred implementation can be modified in a tremendous variety of ways. Accordingly, it should be understood that the modifications and variations suggested below and above are merely illustrative. These examples may help to show some of the scope of the inventive concepts, but these examples do not nearly exhaust the full scope of variations in the disclosed novel concepts.

Of course, the particular frequencies used for communication can be widely modified and varied. For example, the write-data frequency is

preferably 200 kHz (as described) for North American applications; but for European applications, this frequency is preferably set to about 132 kHz instead.

However, it should be noted that many of the disclosed innovative teachings are not even dependent on the use of RF communications channels. For one example, an optical (infrared) link could be directly substituted for the 200 kHz RF link from the base station 110 to the portable module 120. For example, to accomplish this, a sending interface could use a solid-state LED (driven by an output of the converter chip), in place of the transmitter circuit and antenna described. The receiving interface could use a photodiode (covered by an appropriate filter), in place of the antenna, receiver chip, and converter chip described. Similarly, ultrasonic or microwave channels could also be readily substituted, particularly in the channel from the base station 110 to the portable module 120.

Note that some (but not all) of the foregoing teachings suggest that particular frequency relations may be more desirable than others. For example, it is advantageous (but not strictly necessary) to make the read-data frequency so high that a very compact antenna can present a high impedance with good efficiency. Similarly, it is also advantageous (but not strictly necessary) to make the write-data frequency so low that the clock period of digital circuits (in the low-power technology selected for use) is much less than half the period of the write-data signal. (For example, in the presently preferred embodiment, the period of the write-data frequency is about 50 times as long as the clock period of the low-power CMOS digital circuits used in the converter chip 220.) Even if these preferred relations are observed, the frequencies used can still be varied tremendously.

However, it should be noted that many of the disclosed innovative teachings are not even dependent on the use of RF communications channels. For one example, an optical (infrared) link could be directly substituted for the 200 kHz RF link from the base station 110 to the

portable module 120. Ultrasonic or microwave channels could also be readily substituted, particularly in the channel from the base station 110 to the portable module 120.

Additional signal processing can also be used in the base station 110. For example, AGC circuitry could be added to the RF receivers, to improve the signal-to-noise ratio over the expected range of signal strengths.

For another example, where use in crowded environments is expected, it may be advantageous to include time windowing in the base station's polling logic, so that the base station could exclude responses from remote modules 120 outside a certain radius (regardless of RF signal strength differences).

For another example, where many base stations are expected to be sharing a small area, time-domain multiplexing can be used to allocate time slots among the base stations.

Another class of modifications relates to the power source for the micropowered remote module. The presently preferred embodiment uses a nonrechargeable lithium battery; but alternatively a variety of other power sources can be used, including a combination of rechargeable and nonrechargeable batteries, or batteries combined with a solar-powered or RF-powered additional power input, etc. The power-switching abilities of the disclosed integrated circuits make such multiple-source power architectures particularly convenient.

Additional signal processing can also be used in the base station 110. For example, AGC circuitry could be added to the RF receivers, to improve the signal-to-noise ratio over the expected range of signal strengths.

For another example, where use in crowded environments is expected, it may be advantageous to include time windowing in the base station's polling logic, so that the base station could exclude responses from remote modules 120 outside a certain radius (regardless of RF signal strength differences).

For another example, where many base stations are expected to be sharing a small area, time-domain multiplexing can be used to allocate time slots among the base stations.

The disclosed innovative teachings can also be applied to implement more complex filter functions. For example, by using combinations of bandpass filters like those of the principal preferred embodiment, circuits can readily be configured to detect signals with energy either in band A or in band B; or to detect only signals with energy in both band A and band B.

Moreover, more complex logic gates can optionally be used instead of the two inverters of the presently preferred embodiment. For example, by substituting an AND gate for an inverter, a joint-timing relationship can be implemented, where one signal is gated by another. Similarly, by substituting XOR gates, a different combined relationship can be imposed.

It should also be recognized that the power and data links described are not by any means limited to the specific chips described, nor even to the general area of communications modules. For example, the disclosed architecture could also be adapted to a wireless data communication module which included other integrated circuits, such as a microprocessor, display driver, and/or more memory. For another example, the disclosed architecture could also be adapted to other module functions, such as a calculator which included a microprocessor and a digital signal processing chip.

Of course, the 56-bit access protocol could be widely varied, or other signalling schemes could even be used instead.

Another class of modifications relates to the power source for the micropowered remote module. The presently preferred embodiment uses a nonrechargeable lithium battery; but alternatively a variety of other power sources can be used, including a combination of rechargeable and nonrechargeable batteries, or batteries combined with a solar-powered or RF-powered additional power input, etc. The power-switching abilities of

the disclosed integrated circuits make such multiple-source power architectures particularly convenient.

As will be recognized by those skilled in the art, the innovative concepts described in the present application can be modified and varied over a tremendous range of applications, and accordingly their scope is not limited except by the allowed claims.

CLAIMS

What is claimed is:

1. A communication system, comprising:

at least one base station and at least one remote module, each comprising at least one RF transmitter and at least one RF receiver, and each connected to mutually communicate using a pulse code modulation protocol;

wherein said remote module is battery-powered, and comprises

an antenna,

a serial data bus internal to said portable module,

plural integrated circuits, mutually connected through said serial data bus and which are connected and programmed to receive and decode RF signals from said base station, and

memory which is read/write accessible over said serial data bus.

2. A micropowered wireless data module, comprising:

a power source;

a serial data bus internal to said portable module;

plural integrated circuits mutually connected through said serial data bus, ones of said integrated circuits being connected and programmed to receive and decode RF signals, said plural integrated circuits including

memory which is read/write accessible over said serial data bus, and

access control circuitry, connected to provide password protection for access to said memory with respect to a user-changeable password;

a sending interface, which is connected to perform wireless data transmission in accordance with signals on said serial data bus;

a receiving interface, which is connected to receive wireless data transmissions and to control said serial data bus and to drive command and data signals on said serial data bus accordingly;

wherein said receiving interface unit provides translation from a duration-modulated code to the data format of said serial data bus.

3. A low-power RF receiver, comprising:

a battery;

at least one antenna circuit, tuned to at least one predetermined reception frequency;

at least one comparator, having a pair of inputs directly connected to receive a low-level analog signal at said predetermined frequency from said antenna circuit;

at least one digital logic stage, connected to be driven by the output of said comparator and provide a full digital output corresponding to the voltage received at said comparator ;

said comparator and said logic stage being connected to be powered by said battery.

4. A wireless data module, comprising:

an RF receiver and antenna, capable of RF reception at a first frequency;

an RF transmitter and antenna, capable of RF transmission at a second frequency which is different from said first frequency;

a memory connected to selectably store data received through said receiver, and to selectably read data for transmission by said transmitter, to provide two-way data communication using said first and second frequencies; and

conductive signal contacts, connected to said transmitter and receiver in such relation that said memory can also selectably store data received through said contacts in an RF signal, and can selectably read data for RF transmission through said contacts, to provide two-way data communication through said contacts, using substantially the same protocols as are used in said wireless data communication.

5. A multiport memory system, comprising:

a plurality of multiport memory controller chips, each comprising

a parallel port interface;

a parallel memory interface, separate from said parallel port; and

a serial port interface, comprising circuits connected and programmed to receive bit streams in a predetermined serial format, including a predetermined protocol for overhead bits, and to provide corresponding outputs to said memory interface in a parallel output;

one or more integrated circuit memories, connected to said parallel memory interface of one of said controller chips;

wherein said memory interface of at least one of said controller chips is directly connected to said parallel port interface of another of said controller chips;

whereby said respective serial ports of multiple ones of said controller chips share multiport access to said memory interface of one of said controller chips.

6. A method for data communication, in a system which includes one or more base stations each including a wireless transmitter and receiver, and one or more remote modules each including a wireless transmitter and receiver, comprising the steps of:

a) from one of said base stations: broadcasting a query signal;

b) in one of said micropowered portable modules which is within range of said query signal: receiving said query signal, and transmitting a beacon in response thereto;

c) in said base station: receiving said beacon, and transmitting a command to said module to read out data, and thereafter transmitting a series of read-data symbols;

d) in said module: transmitting, in synchrony with said series of read-data symbols, a series of signals which each indicate the value of one bit of data;

e) in said base station, if a write transaction is desired: transmitting a command to said module to write in data, and thereafter transmitting a series of write-data symbols of first and second types;

f) in said module, if a write transaction is desired: receiving and decoding said series of write-data symbols, to define a sequence of bits, and storing said sequence of bits;

wherein said read-data symbol is substantially the same as one of said write-data symbols.

7. A portable wireless-accessible data module, comprising:

receiver circuits capable of receiving electromagnetic radiation at a first frequency;

a transmitter capable of transmitting electromagnetic radiation at a second frequency; and

coding and data handling circuits connected so that the module can carry on data communications at low RF power levels, on said first and second frequencies, with another station while in proximity thereto;

wherein said receiver circuits comprise

a first amplifier

which has a bandwidth wide enough to track signals at said first frequency and

which is connected to receive signals at said first frequency, and

a second amplifier

which is connected to receive signals at a third frequency which is much lower than said first frequency, and

which has a bandwidth which is not wide enough to track signals at said first frequency, but is high enough to track signals at said third frequency;

and wherein said remote module, when not sending or receiving data, monitors said third frequency substantially continuously, but does not monitor said first frequency continuously;

and wherein said remote module, when not monitoring said first frequency, does not begin to monitor said first frequency until a predetermined coded command is received on said third frequency.

8. A wireless communication system, comprising:

at least one base station, and multiple remote modules, each comprising at least one RF transmitter and at least one RF receiver;

wherein said base station comprises

a first transmitter capable of operation at a first frequency, and

a second receiver capable of operation at a second frequency

and wherein said remote module comprises

a first receiver capable of operation at said first frequency, and

a second transmitter capable of operation at said first frequency;

and said transmitters and receivers are connected so that said base station and said remote module can carry on data communications on said first and second frequencies, but only while in mutual proximity;

wherein said base station can broadcast a polling command to ascertain what remote modules are in proximity at a given moment;

and wherein ones of said modules, if in proximity to said base station, respond to said polling command with a response which includes an identification field;

and wherein at least a subfield of said identification contains bit positions which are individually, and not combinatorially or numerically, assigned to correspond to respective subclasses of said remote modules;

and wherein said base station contains logic to decode responses to said polling command, and to determine the presence of multiple ones of said subclasses of said modules, if ones of said subclasses simultaneously respond to said polling command.

9. A communications receiver, comprising:

front end circuits, which receive wireless incoming signals and provide, as corresponding digital outputs, variable-length bursts of constant-width pulses;

counter logic, which counts the pulses in said bursts, and recognizes the end of a burst when a predetermined minimum silence period occurs;

thresholding logic, which compares values accumulated by said counter logic against a set of multiple boundary values, to provide a set of signals indicating the results of said comparisons;

a state machine, which translates said set of signals into output signals to selectively drive appropriate output lines in accordance with the encoded signal received.

10. A wireless-accessible portable data module, comprising:

a battery;

communication interface circuits, powered by said battery, including

an RF receiver capable of operation at a first frequency, and

an RF transmitter capable of operation at a second frequency;

a data access pathway comprising

coding logic, and

at least 2^{14} bits of solid-state memory;

a data connector; and

a multiport memory controller which arbitrates access to said memory between said data connector and said interface circuits;

said module also being connected to receive a power supply input through said data connector;

whereby, when a connection is made to said parallel port of a respective remote module, data can be rapidly downloaded from said memory without burdening said battery.

11. An integrated bandpass filter circuit, for providing a passband with predetermined upper and lower passband edge frequencies, comprising:

a first digital circuit which has an input and an output, said output responding with low-pass frequency-domain response characteristics, which include a sharp cutoff at approximately the lower passband edge frequency, to signals applied at the input thereof;

a second digital circuit which has an input and an output, said output responding with low-pass frequency-domain response characteristics, which include a sharp cutoff at approximately the upper passband edge frequency, to signals applied at the input thereof;

a third digital circuit which implements a counter function, and which comprises input connections including at least

a first input having functionality analogous to a conventional counter's reset input, and

a second input having functionality analogous to a conventional counter's clock input;

wherein the output of said first digital circuit is connected to drive said first input of said third circuit, and the output of said second digital circuit is connected to drive said second input of said third circuit;

whereby the output of said third digital circuit provides said bandpass filter function.

12. An integrated circuit, comprising:

a connection for receiving a primary power supply input;

a connection for receiving a secondary power supply input;

a connection for receiving a ground voltage;

a connection for providing a power supply output, and circuitry which is configured to connect said power supply output to whichever of said power supply inputs is more different from said ground voltage;

connections for a reset line, a clock line, and at least one data line of a serial bus, and circuitry which is configured to provide outgoing data transfer over said serial bus;

a connection for providing a reference voltage output, and circuitry which is configured to switch said reference voltage output so that

when said reset line connection is driven to a first state thereof, said reference voltage output is driven to a respective first state thereof;

and when said reset line connection is driven to a second state thereof, said reference voltage output is driven to a respective second state thereof;

wherein said second state of said reset line connection has a greater voltage to ground than does said first state of said reset line connection,

and wherein said second state of said reference voltage output has a smaller voltage to ground than does said first state of said reference voltage output.

13. A wireless data module, comprising:

a battery;

memory;

a memory controller chip, including

a parallel port interface;

a memory interface, separate from said parallel port; and

a serial port interface, comprising circuits connected and programmed to receive bit streams in a predetermined serial format, including a predetermined protocol for overhead bits, and to provide corresponding outputs to said memory interface in a parallel output;

an arbitration register which is accessible in a memory address space which is common to memory accessible through said memory interface, and which contains arbitration bits indicating which port is performing memory access through said memory interface, some of said arbitration bits being read-accessible through said serial port, but write-accessible only through said parallel port, and others of said arbitration bits being read-accessible through said parallel port, but write-accessible only through said serial port;

wherein said serial access protocol normally requires separate access cycles for read accesses and for write accesses to memory space, but also includes a special command which permits said serial port to sequentially read, write, and read ones of said arbitration bits within a single access cycle;

a complex integrated circuit, having a parallel port interface which is connected to said parallel port interface of said controller chip;

wireless interface circuitry, comprising elements connected to receive and to transmit wireless signals, and having a serial data interface which is connected to said serial port interface of said controller chip.

14. An integrated circuit, comprising:

input contacts connectable to an antenna;

a battery terminal, for connection to a battery;

enable logic, connected to said input contacts, comprising insulated gate field effect transistors which are connected to turn on only when the antenna provides a voltage greater than the threshold voltage of said transistors; and

other circuits which have significant standby power consumption requirements and which are selectably connected to said battery terminal;

wherein said enable logic is connected to selectively disable said other circuits, and does not permit said other circuits to operate until said enable logic has detected a strong electromagnetically radiated signal at a predetermined low frequency.

15. The system of Claim 1, wherein said remote module comprises at least one integrated circuit memory.

16. The system of Claim 1, wherein said remote module comprises at least one integrated circuit which implements access control restrictions.

17. The system of Claim 1, wherein the total set of symbols transmitted by said base station includes

a first symbol which encodes a write command for a first data bit state, and which also, during read mode, provides timing for reading one bit of data;

a second symbol which encodes a write command for a second data bit state;

a third symbol which encodes a reset command; and

a fourth symbol which encodes a command to turn on a wireless beacon;

wherein said first, second, third, and fourth symbols each have respectively different durations;

and wherein said first and second symbols each have a duration less than that of either of said third and fourth symbols.

18. The system of Claim 1, wherein said remote module is hand-portable.

19. The system of Claim 8, wherein at least some ones of said bits of said subfield are specifically assigned to individual ones of said remote modules.

20. The system of Claim 8, wherein some number N of said bit positions of said identification are combinatorially assigned to 2^N of said remote modules, and N is greater than two.

21. The system of Claim 1, wherein at least one of said remote modules comprises an access control chip, which is connected to said serial data bus and which is connected to provide password protection for said memory.

22. The system of Claim 1, wherein at least one of said remote modules comprises a microprocessor.

23. The method of Claim 6, wherein said beacon is chopped at a predetermined frequency.

24. The method of Claim 6, wherein each transaction of said steps a) b) c) and d) includes only a predetermined fixed total number of symbols.

25. The method of Claim 6, further comprising the additional steps, after said step c) and before said step e), of

g) in said base station: transmitting a chip-select signal;

h) in said module: comparing said chip-select signal with an internally stored value;

i) in said module: transmitting an identification signal, if said chip-select signal matches said internally stored value;

j) in said base station: transmitting a password; and

k) in said module: comparing said password with an internally stored value.

26. The method of Claim 6, further comprising the additional steps, after said step c) and before said step e), of

g) in said base station: transmitting a chip-select signal;

h) in said module: comparing said chip-select signal with an internally stored value;

i) in said module: transmitting an identification signal, if said chip-select signal matches said internally stored value;

j) in said base station: transmitting a password; and

k) in said module: comparing said password with an internally stored value, and generating false data if said password does not match said internally stored value.

27. The method of Claim 6, wherein the total set of symbols transmitted by said base station includes

a first symbol which encodes a write command for a first data bit state, and which also, during read mode, provides timing for reading one bit of data;

a second symbol which encodes a write command for a second data bit state;

a third symbol which encodes a reset command; and

a fourth symbol which encodes a command to turn on a wireless beacon;

wherein said first, second, third, and fourth symbols each have respectively different durations, and wherein said first and second

symbols each have a duration less than that of either of said third and fourth symbols.

28. The method of Claim 9, wherein, during said step b), said base station scans a narrow-band band pass filter across a range of frequencies in which said beacon is expected to fall.

29. The method of Claim 9, wherein the range of said query signal is approximately 5 feet or less.

30. The module of Claim 2, further comprising an access control chip, which is connected to said serial data bus and which is connected to provide password protection for said memory.

31. The module of Claim 4, further comprising an access control chip, which is connected to said serial data bus and which is connected to provide password protection for said memory.

32. The module of Claim 2, wherein said remote module further comprises a microprocessor, which is connected to have access to said memory over said serial data bus.

33. The module of Claim 2, wherein said remote module weighs less than 10 ounces and has a total volume of less than 10 cubic inches.

34. The module of Claim 2, further comprising a memory controller chip, which is connected to provide an interface between an array of memory cells and said serial data bus.

35. The module of Claim 7, wherein said data access pathway can receive data through said contacts at a frequency which is different from said first frequency and which falls in a frequency range of about one-

third of said first frequency to three times said first frequency, and wherein said data access pathway can send data through said contacts using a carrier frequency which is different from said first frequency and which falls in a frequency range of about one-third of said second frequency to three times said second frequency.

36. The module of Claim 7, wherein said data access pathway can receive data through said contacts at a third frequency which is different from said first frequency, and wherein said data access pathway can send data through said contacts using, as a carrier frequency, a fourth frequency which is different from said second frequency.

37. The module of Claim 4, wherein said first and second frequencies are much less than 100 GHz.

38. The module of Claim 4, wherein said first frequency is less than 1 MHz, and said second frequency is greater than 30 MHz.

39. The module of Claim 13, wherein said check value provided by said error-checking logic is also tested at the end of data transfers.

40. The module of Claim 13, wherein said error-checking logic is included in said memory controller.

41. The module of Claim 13, wherein said memory controller contains a protocol register which stores incoming commands while said check value is being tested.

42. The module of Claim 13, wherein said wireless interface circuitry is configured to receive infrared signals.

43. The module of Claim 13, wherein said wireless interface circuitry is configured to receive ultrasonic signals.

44. The module of Claim 10, wherein said battery is non-rechargeable.

45. The receiver of Claim 3, wherein said full digital output is at the same frequency as said low-level analog signal.

46. The receiver of Claim 3, wherein said low-level analog signal has a frequency below 10 MHz.

47. The receiver of Claim 3, wherein said low-level analog signal has a frequency below 1 MHz.

48. The receiver of Claim 3, wherein said comparator receives a standby current which is regulated by a current source, and wherein said current source comprises multiple current-source devices in parallel, and switching transistors which are connected in series with individual ones of said current-source devices, to enable or disable ones of said current-source devices; and further comprising current-source-control logic, connected to control said switching transistors, and thereby enable or disable ones of said current-source devices, in accordance with signal detection characteristics seen at a later stage.

49. The receiver of Claim 3, wherein said comparator receives a standby current which is regulated by a current source, and wherein said current source comprises multiple current-source devices in parallel, and switching transistors which are connected in series with individual ones of said current-source devices, to enable or disable ones of said current-source devices; and further comprising current-source-control logic, connected to control said switching transistors, and thereby enable or disable ones of said current-source devices, in accordance with signal

detection characteristics seen at a later stage; and wherein the widest of said current-source devices is at least four times as wide as the narrowest of said current-source devices.

50. The receiver of Claim 3, comprising at least two of said antenna circuits, both tuned to a predetermined reception frequency; and at least two of said comparators, each having a respective pair of inputs directly connected to receive a low-level analog signal at said predetermined frequency from a respective one of said antenna circuits.

51. The integrated circuit of Claim 11, wherein said third digital circuit is a counter.

52. The integrated circuit of Claim 11, wherein said first logic gate is an inverter.

53. The integrated circuit of Claim 11, wherein said first logic gate is a NAND gate.

54. The integrated circuit of Claim 11, wherein said first and second digital circuits are inverters, and wherein said first digital circuit comprises a resistor connected in series with the output of said first digital circuit.

55. The integrated circuit of Claim 12, further comprising a connection for an additional serial data input, separate from said serial bus.

56. The integrated circuit of Claim 12, further comprising a connection for keying a wireless transmitter.

57. The integrated circuit of Claim 14, wherein said other circuits include wireless interface circuits.

58. The integrated circuit of Claim 14, wherein said enable logic does not permit said other circuits to operate until said enable logic has detected a strong electromagnetically radiated signal with a predetermined coded pattern at said predetermined low frequency.

59. The integrated circuit of Claim 14, wherein said enable logic can also command said other circuits to cease operation if enable logic has detected a strong electromagnetically radiated signal with a predetermined coded pattern at said predetermined low frequency.

60. The integrated circuit of Claim 14, wherein the output of said enable logic is connected to change the state of at least one bit of nonvolatile memory, and said nonvolatile memory bit controls logic gates in said other circuits.

61. The integrated circuit of Claim 14, further comprising a filter circuit which blocks the output of said enable logic unless energy near said predetermined low frequency is much stronger than energy at other frequencies.

62. The integrated circuit of Claim 14, wherein said predetermined low frequency is below 3000 Hz.

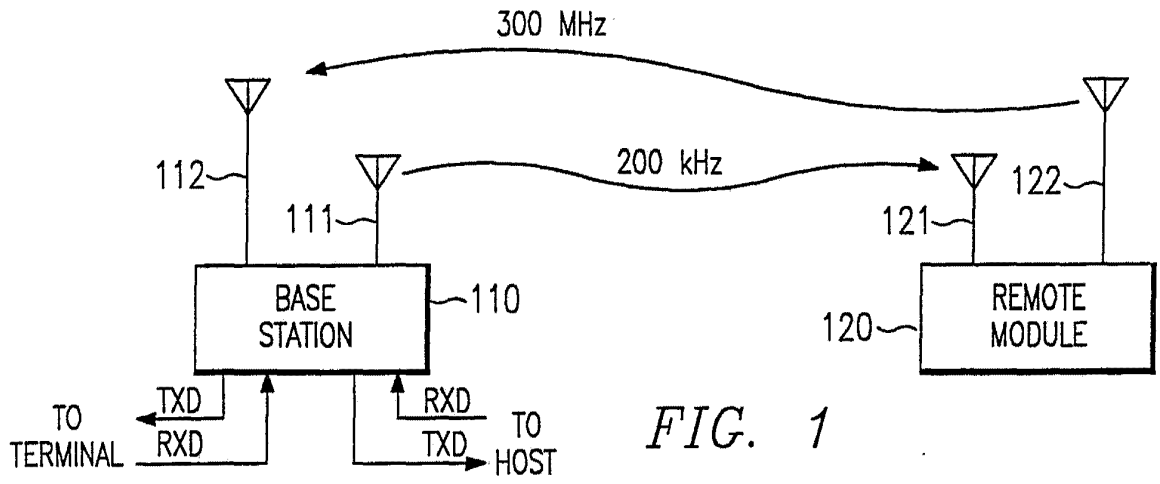


FIG. 1

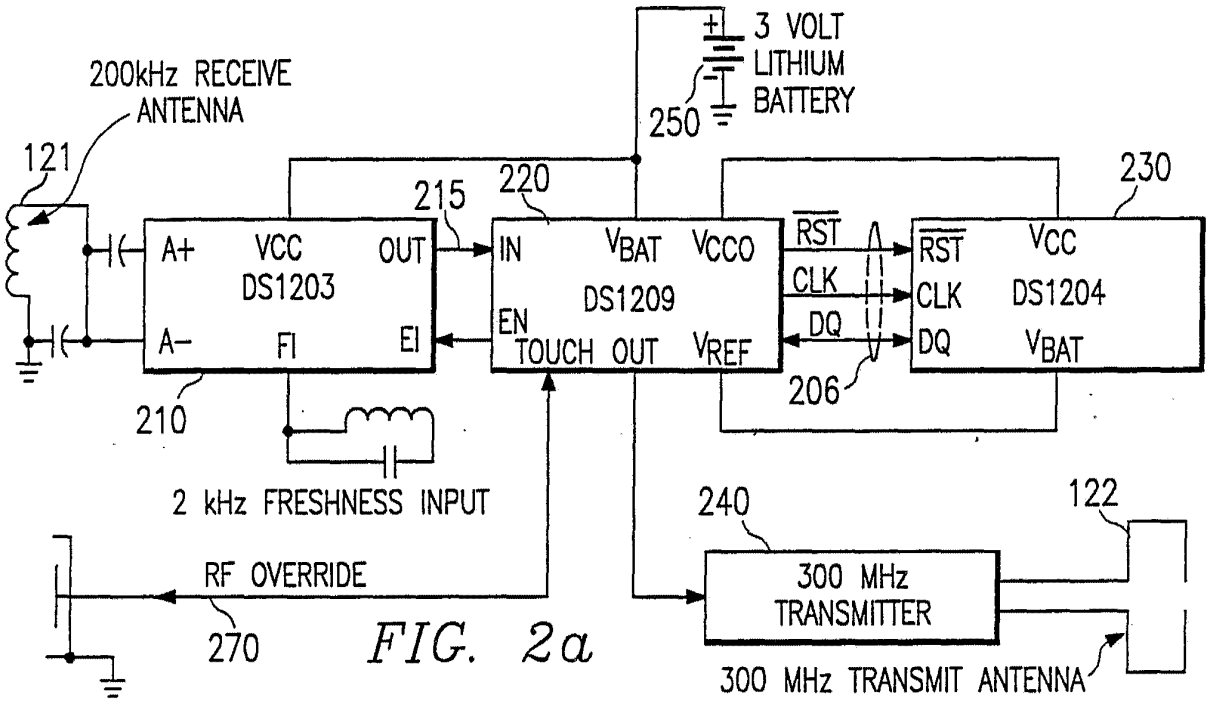


FIG. 2a

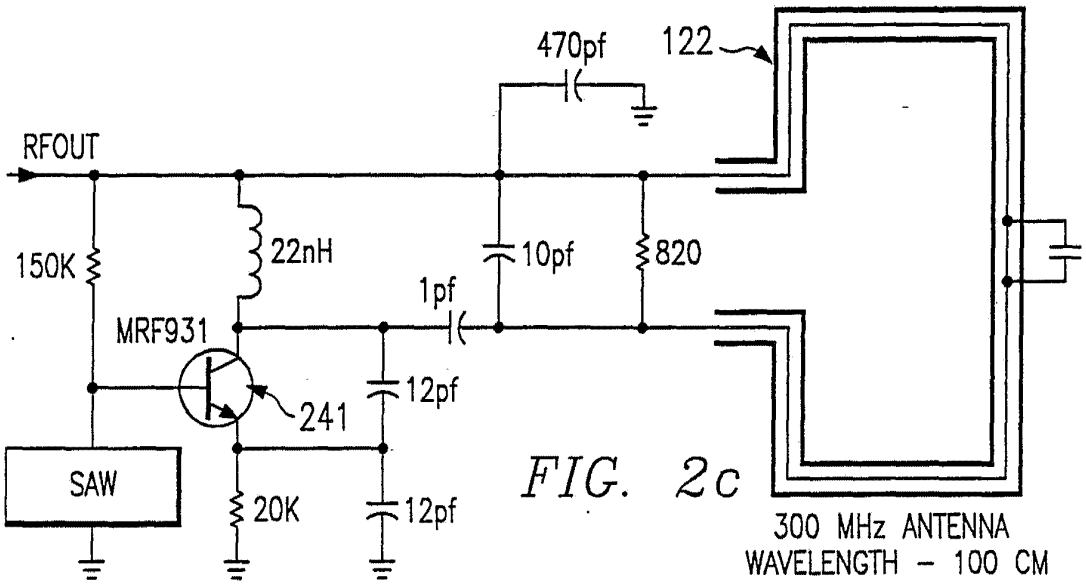


FIG. 2c

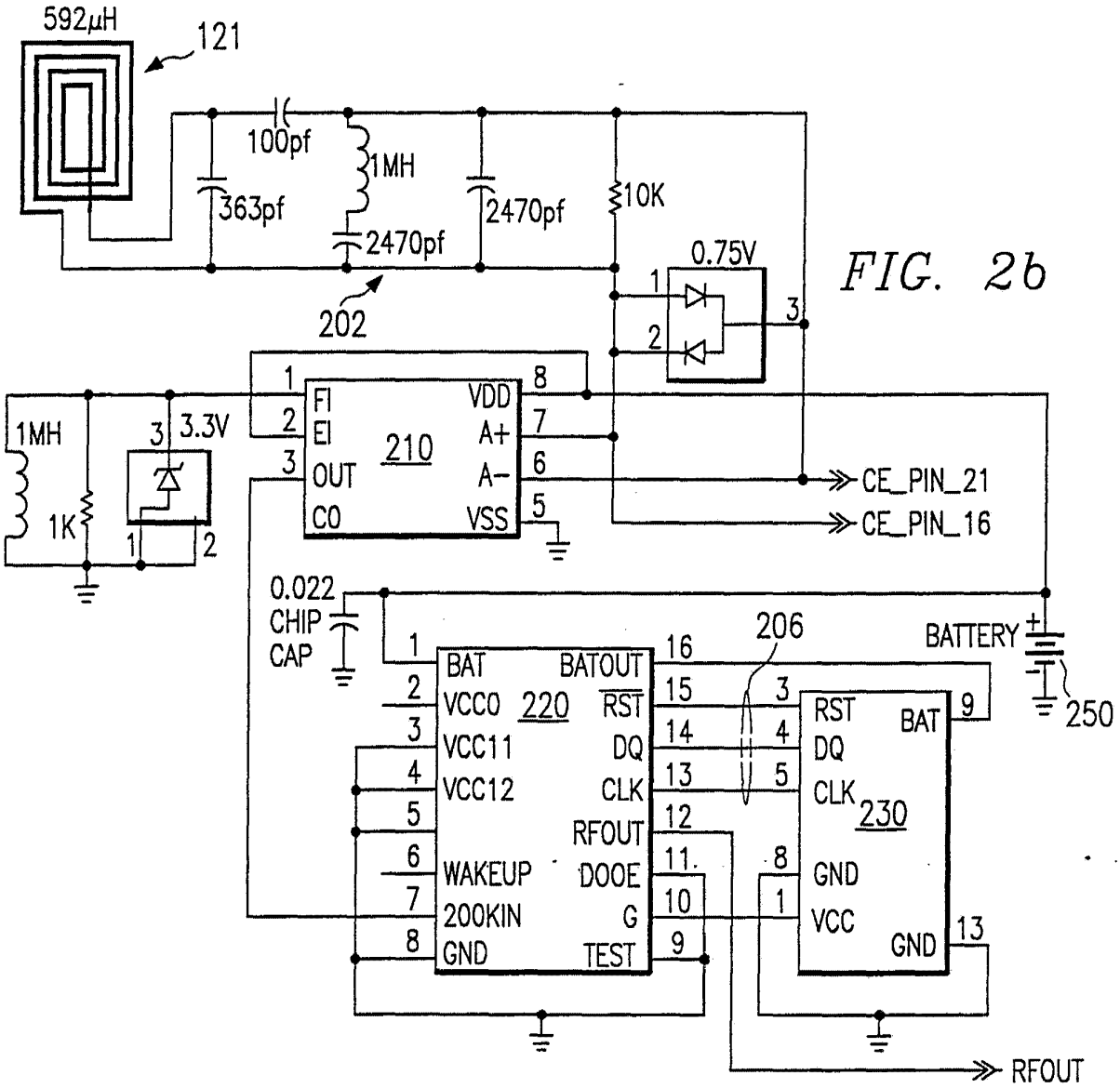

592μH
121
100pf
1MH
363pf
2470pf
2470pf
10K
0.75V
202
1MH
3.3V
1K
FI
EI
OUT
CO
210
VDD
A+
A−
VSS
CE_PIN_21
CE_PIN_16
0.022
CHIP
CAP
BAT
VCC0
VCC11
VCC12
WAKEUP
200KIN
GND
220
BATOUT
RST
DQ
CLK
RFOUT
DOOE
G
TEST
206
BATTERY
250
RST
DQ
CLK
BAT
230
GND
VCC
GND
RFOUT

FIG. 2b

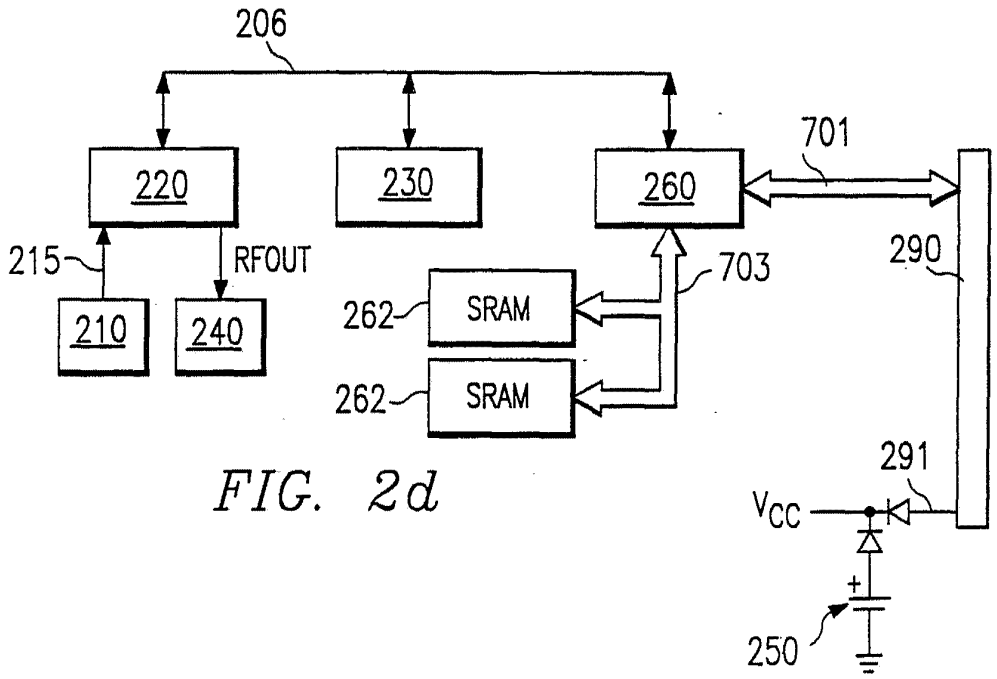

206
220
230
260
701
215
RFOUT
210
240
262
SRAM
262
SRAM
703
290
291
Vcc
250

FIG. 2d

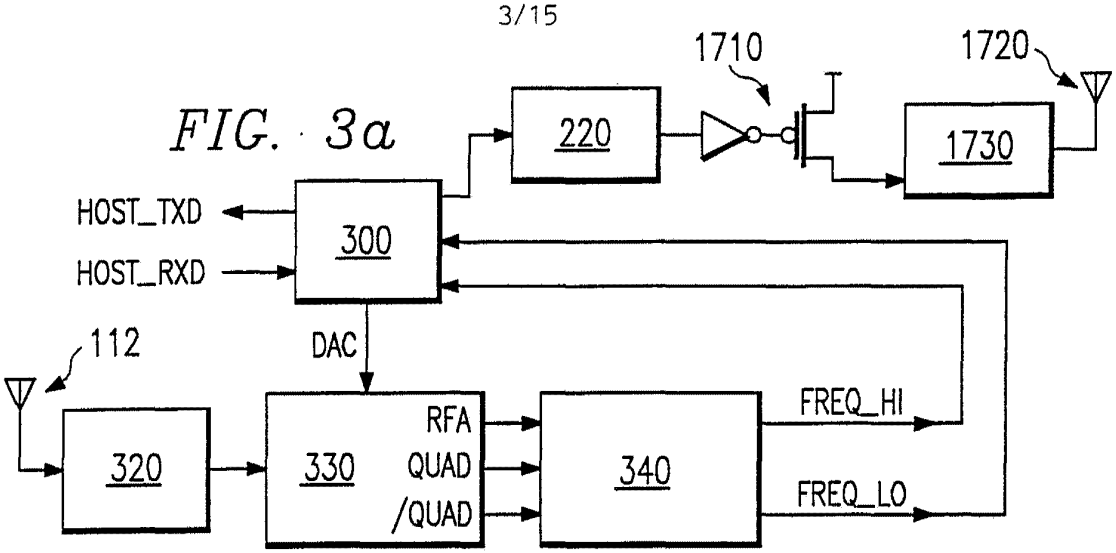


FIG. 3a

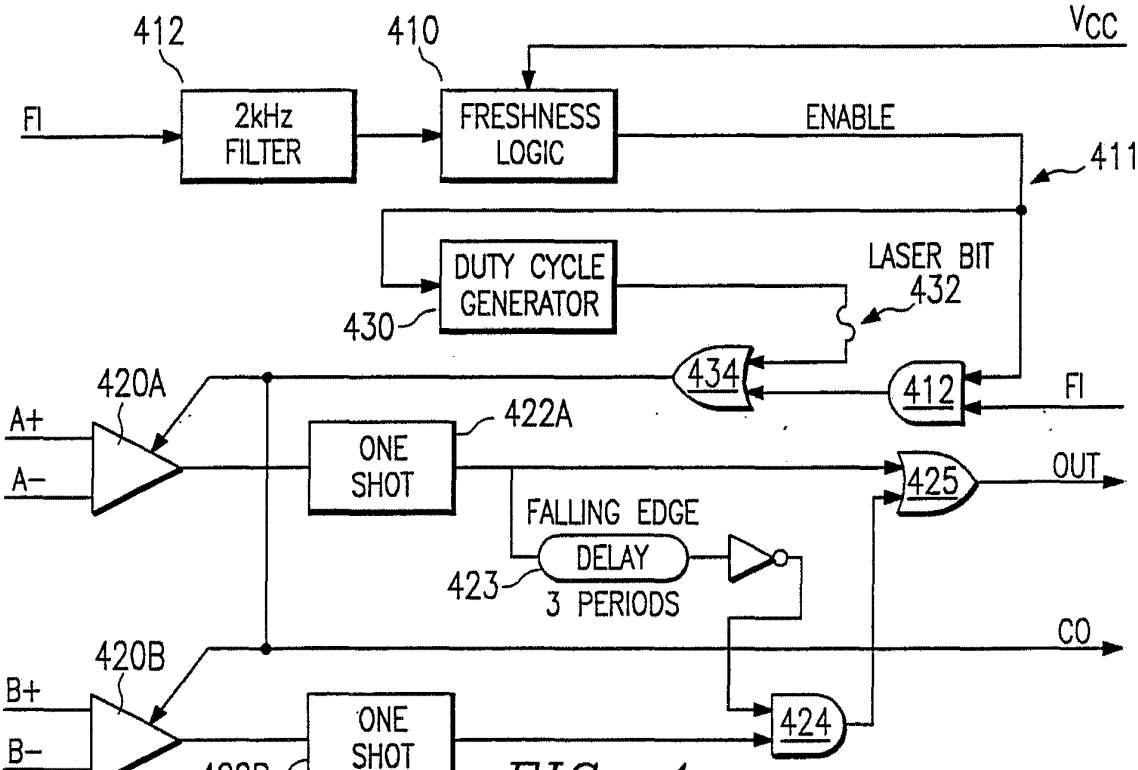


FIG. 4a

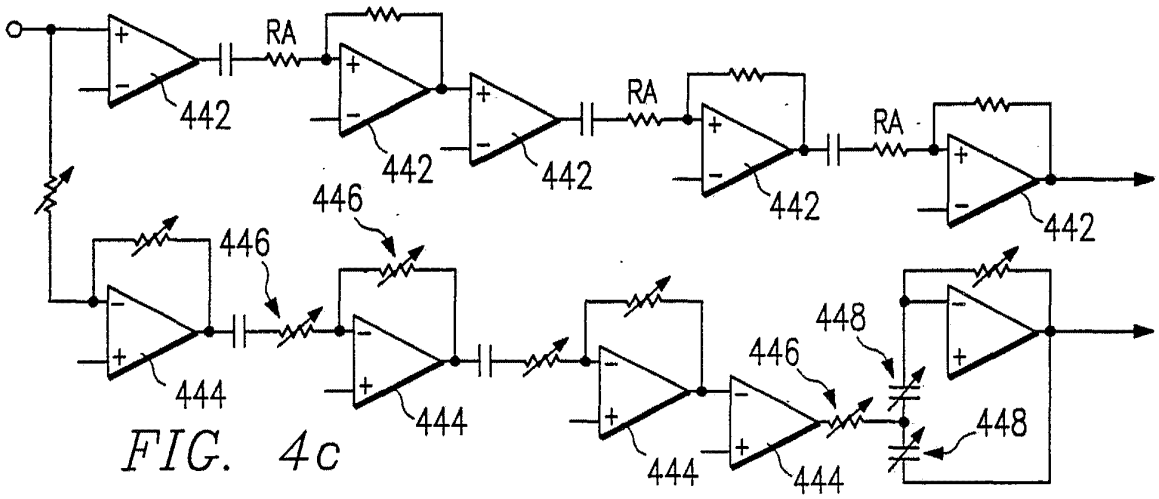


FIG. 4c

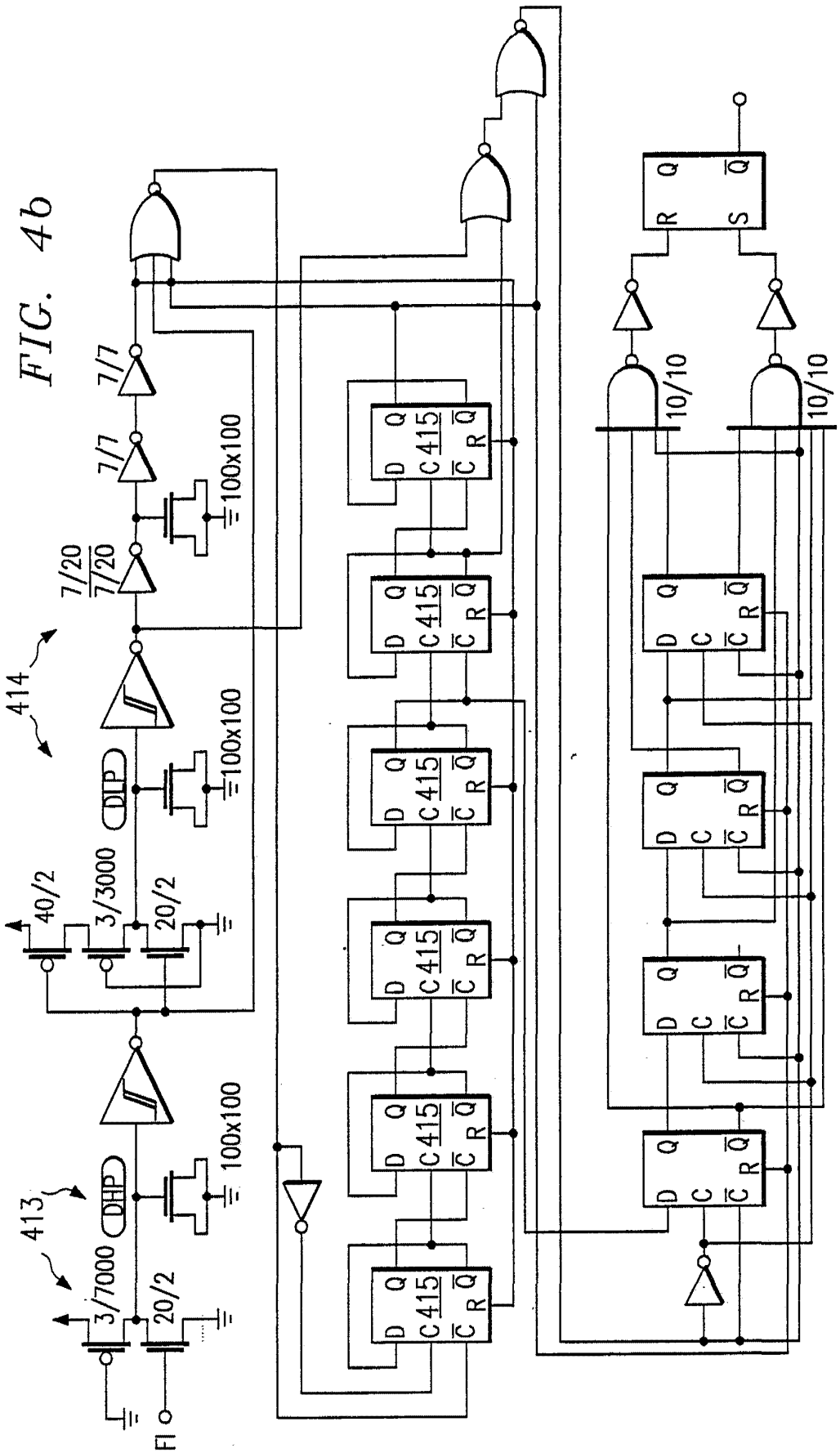

413
414
3/7000
20/2
DHP
100x100
40/2
3/3000
20/2
DLP
100x100
7/20
7/20
7/7
7/7
100x100
415
10/10
10/10
FI

FIG. 4b

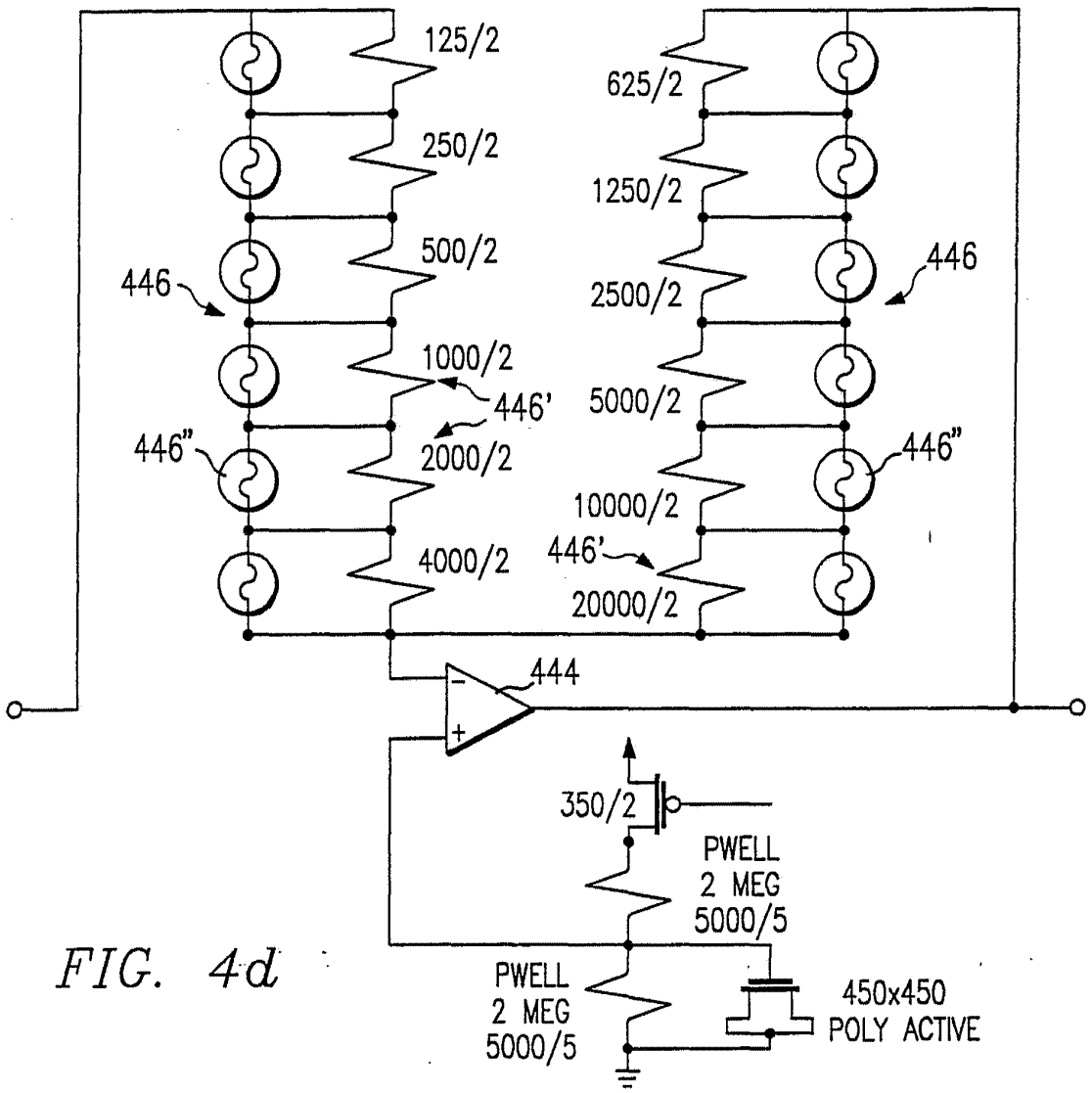

125/2
250/2
500/2
1000/2
2000/2
4000/2
625/2
1250/2
2500/2
5000/2
10000/2
20000/2
446
446'
446"
444
350/2
PWELL
2 MEG
5000/5
PWELL
2 MEG
5000/5
450x450
POLY ACTIVE

FIG. 4d

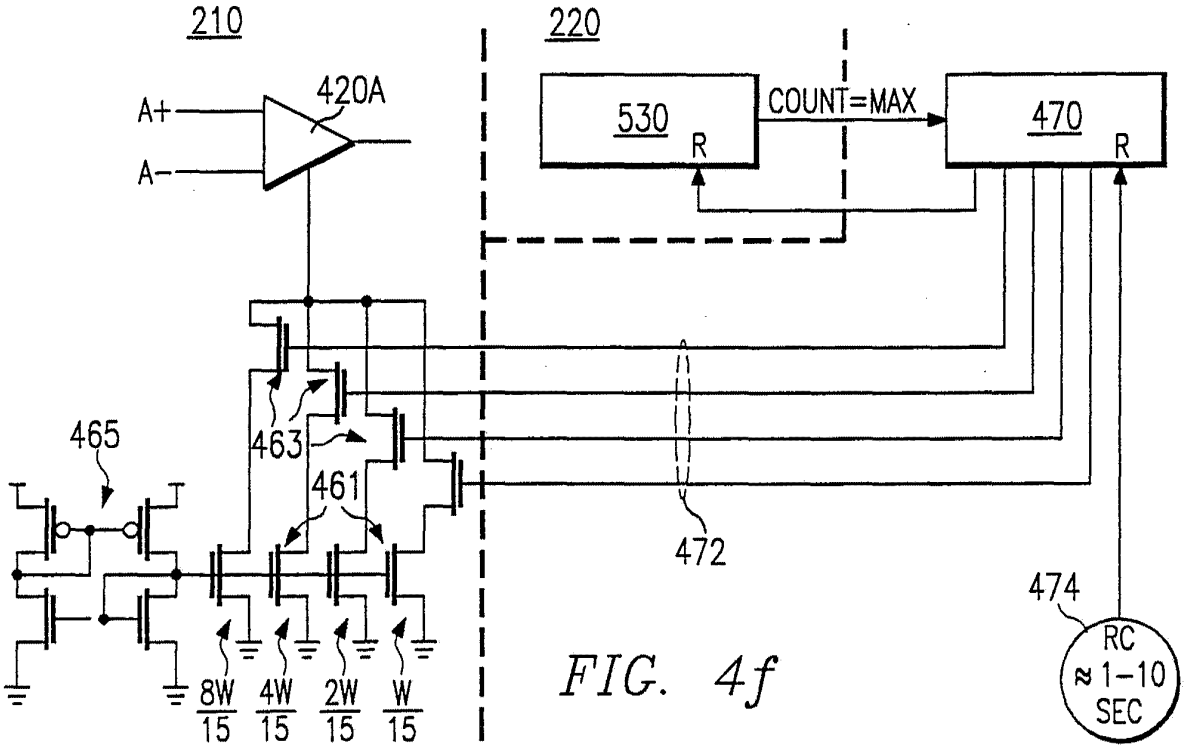

210
220
A+
A-
420A
530
R
COUNT=MAX
470
R
465
463
461
472
474
RC
≈ 1-10
SEC
8W/15
4W/15
2W/15
W/15

FIG. 4f

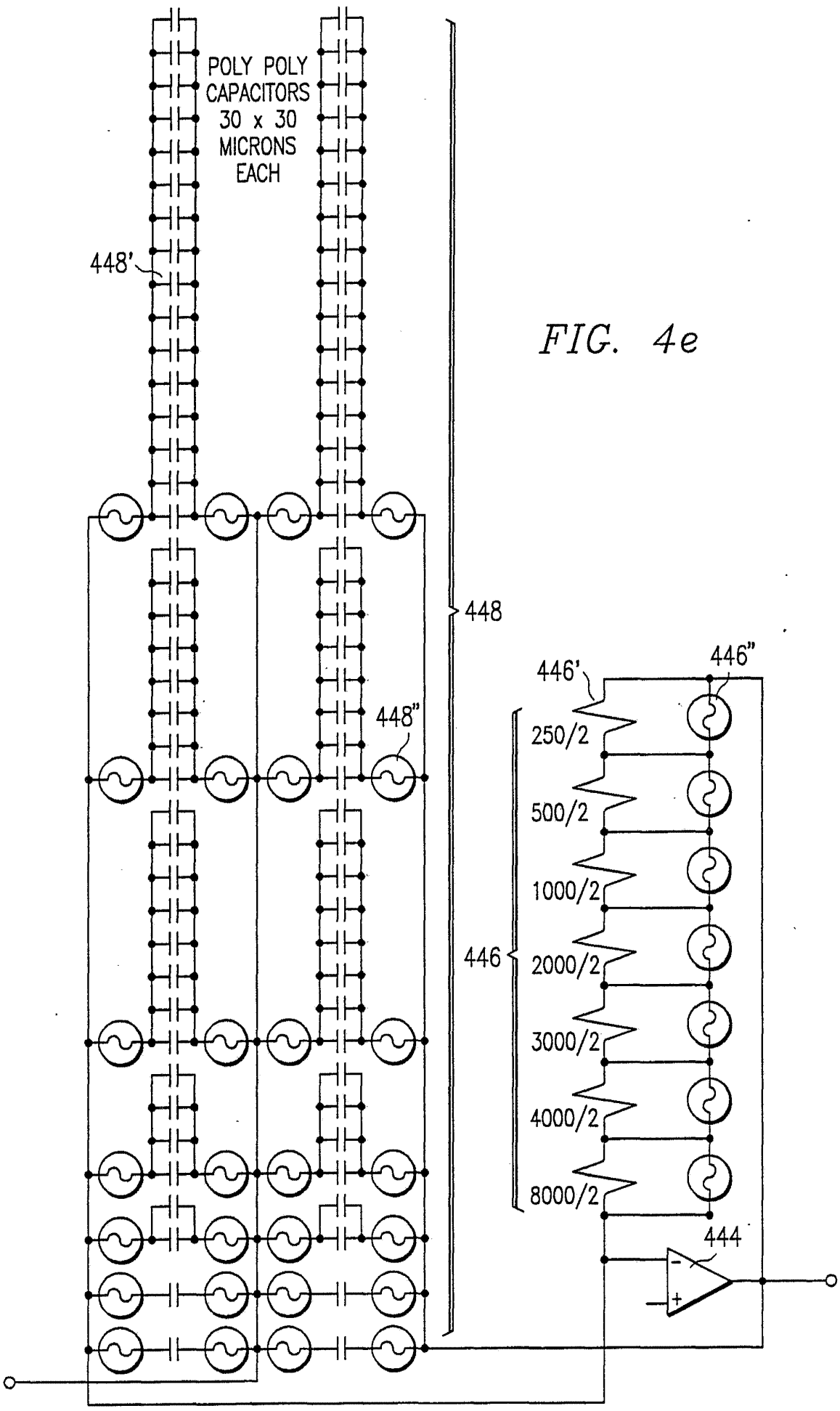

POLY POLY
CAPACITORS
30 x 30
MICRONS
EACH
448'
448
448"
446'
446"
250/2
500/2
1000/2
2000/2
3000/2
4000/2
8000/2
446
444

FIG. 4e

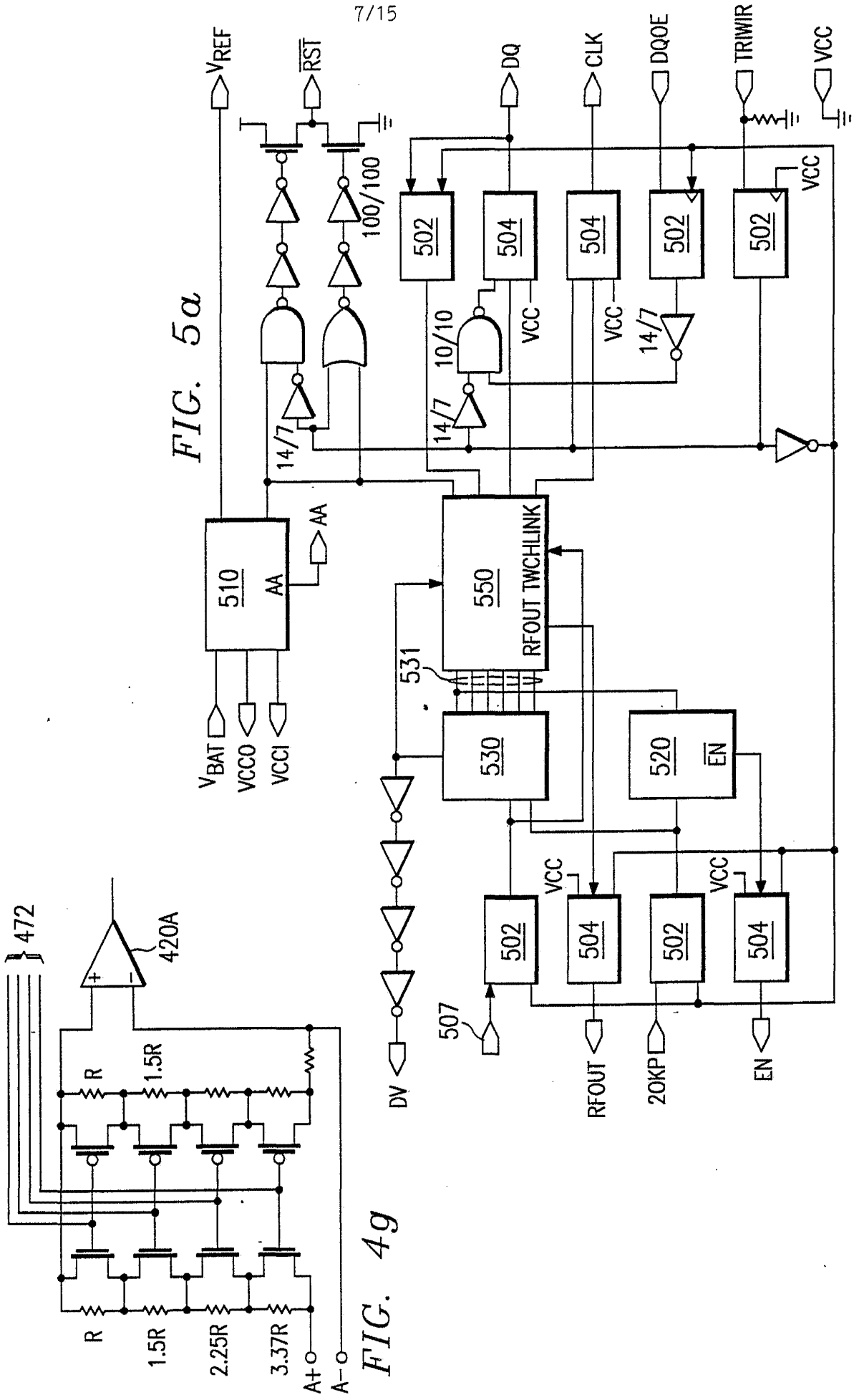

VREF
RST
DQ
CLK
DQOE
TRIWIR
VCC
100/100
502
504
504
502
502
VCC
10/10
VCC
VCC
14/7
14/7
14/7
510
AA
AA
550
RFOUT TWCHLINK
531
VBAT
VCCO
VCCI
530
520
EN
VCC
VCC
502
504
502
504
507
DV
RFOUT
20KP
EN
472
420A
R
1.5R
R
1.5R
2.25R
3.37R
A+
A−

FIG. 5a

FIG. 4g

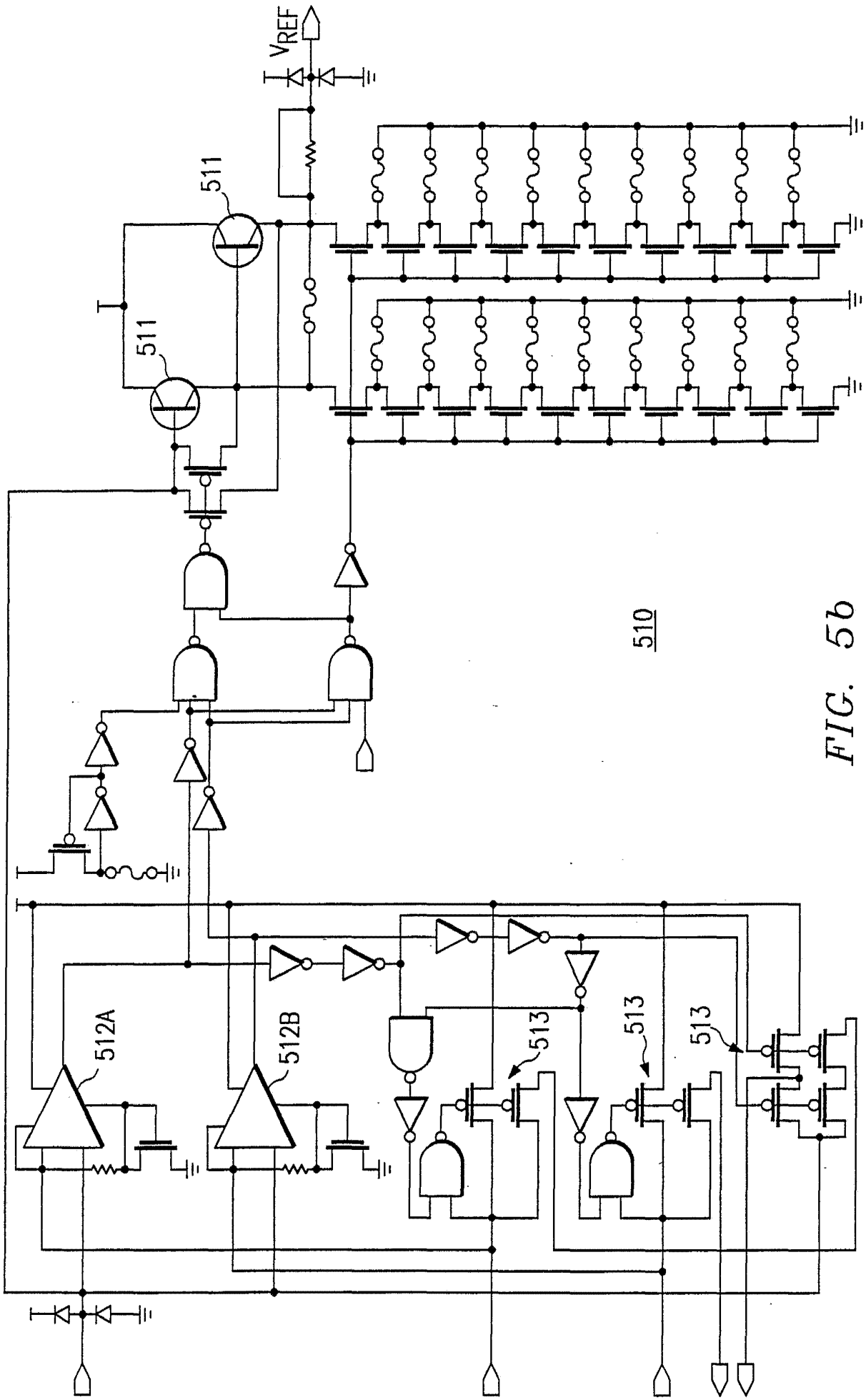


FIG. 5b

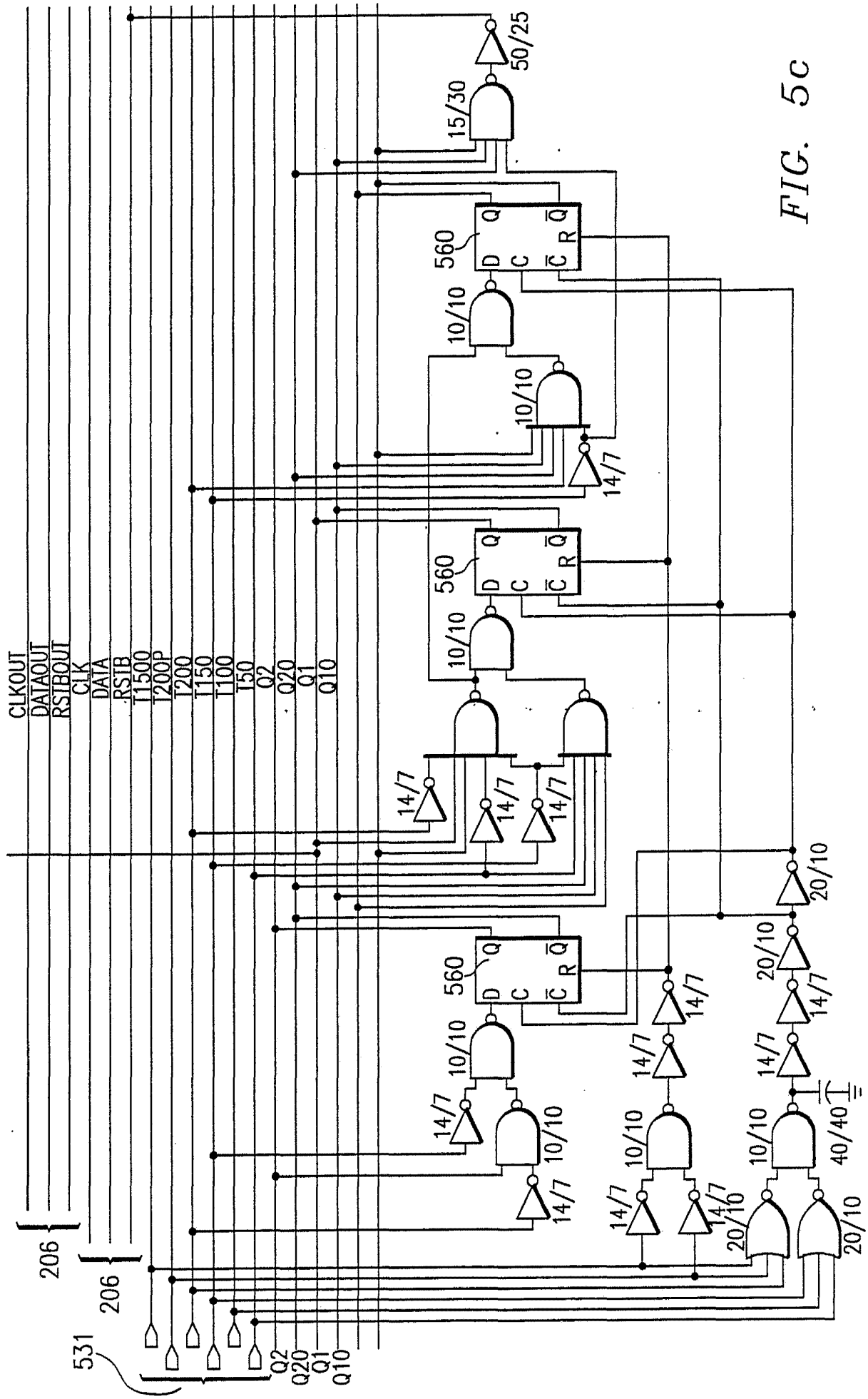

CLKOUT
DATAOUT
RSTBOUT
CLK
DATA
RSTB
T1500
T200P
T200
T150
T100
T50
Q2
Q20
Q1
Q10
206
206
531
Q2
Q20
Q1
Q10
50/25
15/30
560
10/10
14/7
20/10
40/40

FIG. 5c

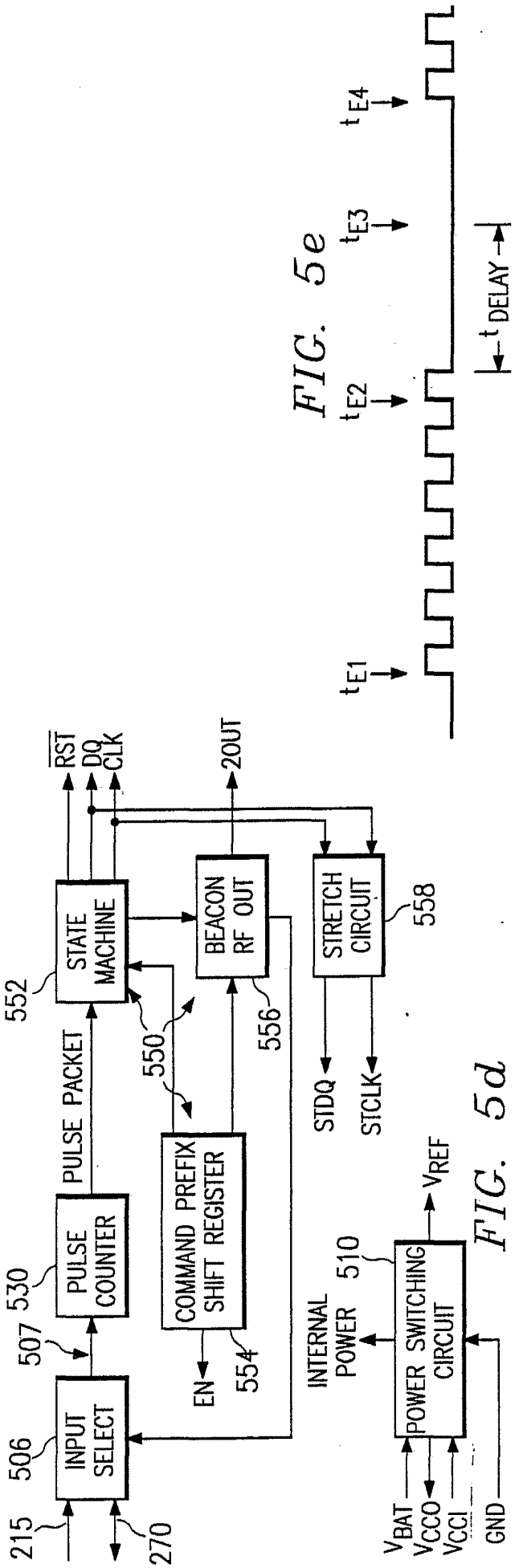


FIG. 5d

FIG. 5e

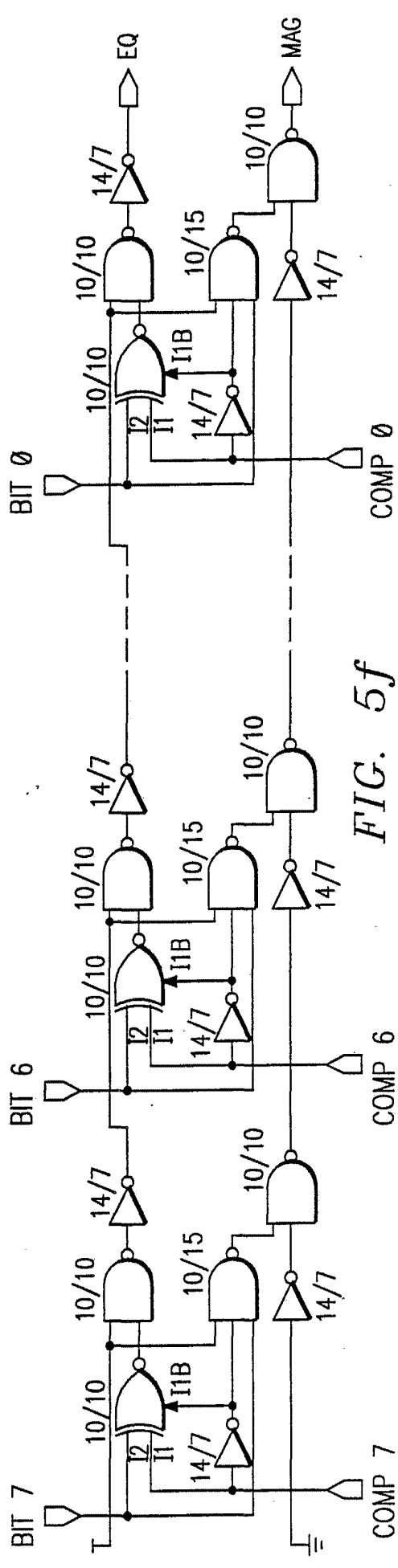


FIG. 5f

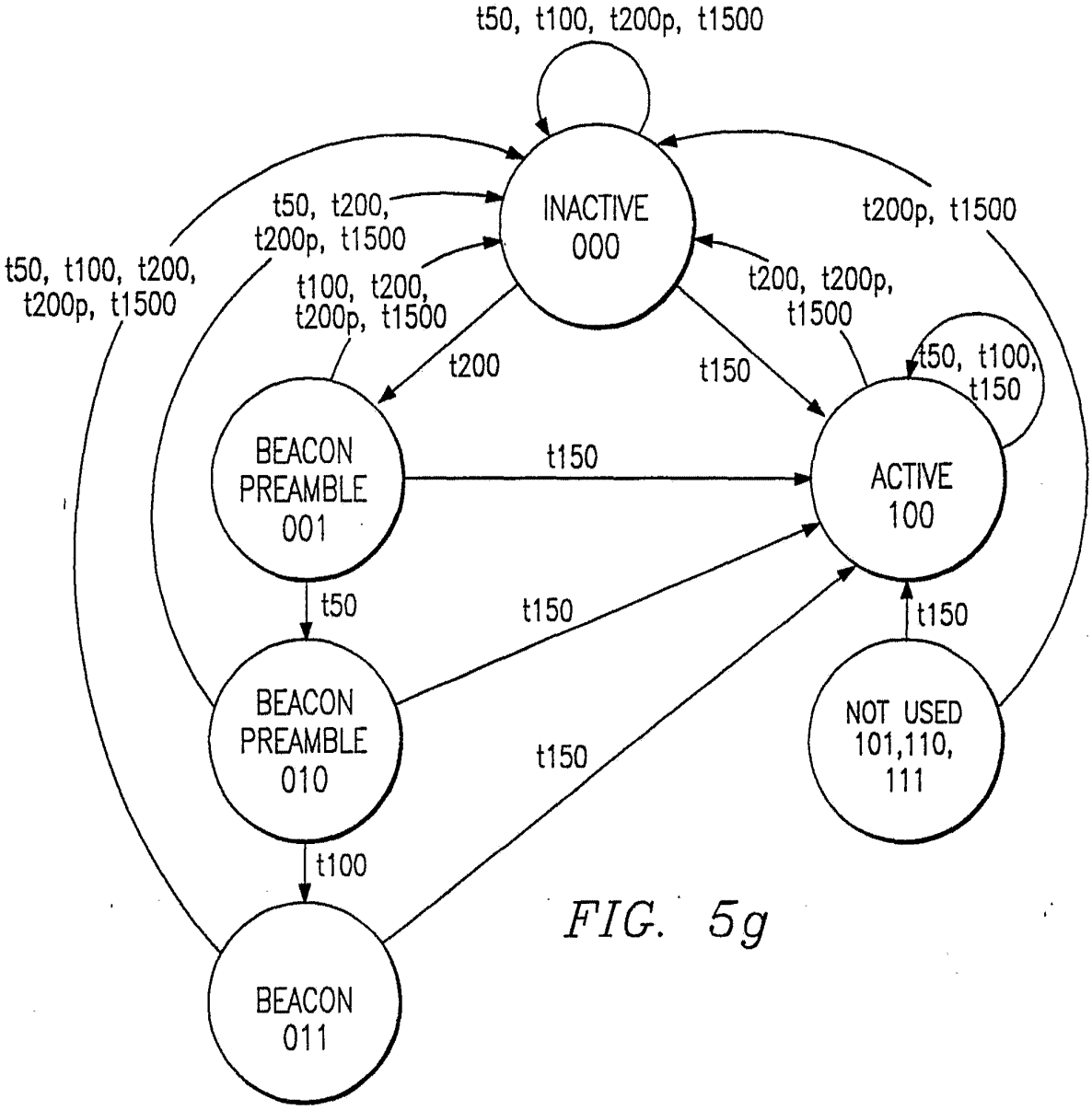

t50, t100, t200p, t1500
INACTIVE
000
t50, t200,
t200p, t1500
t200p, t1500
t50, t100, t200,
t200p, t1500
t100, t200,
t200p, t1500
t200, t200p,
t1500
t200
t150
t50, t100,
t150
BEACON
PREAMBLE
001
t150
ACTIVE
100
t50
t150
t150
BEACON
PREAMBLE
010
t150
NOT USED
101,110,
111
t100
BEACON
011

FIG. 5g

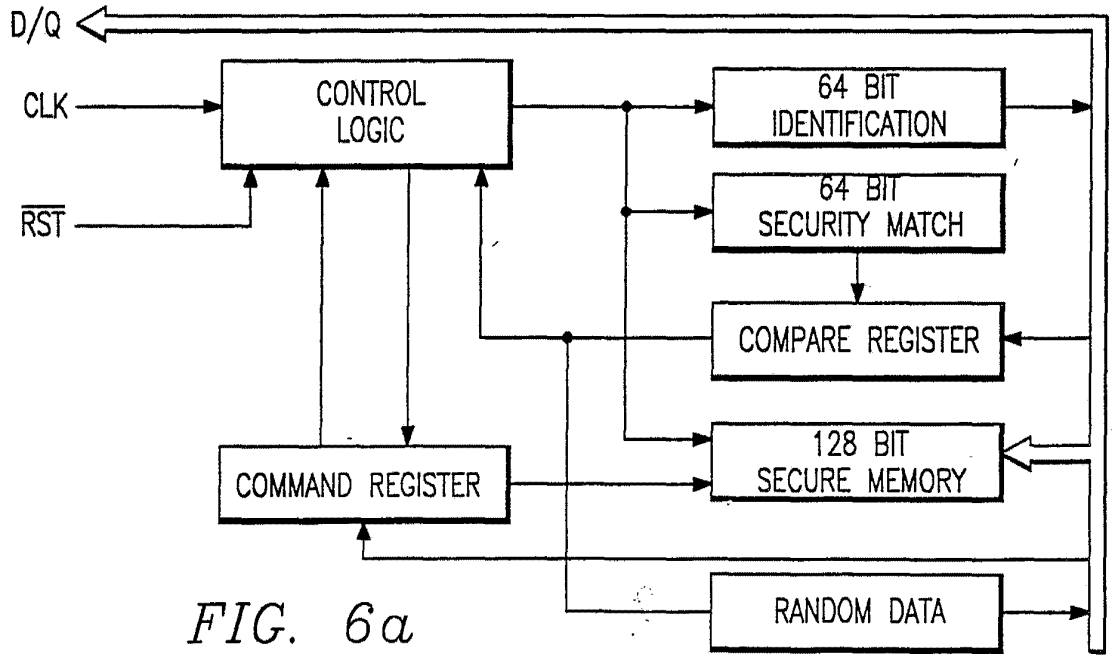

D/Q
CLK
RST
CONTROL
LOGIC
64 BIT
IDENTIFICATION
64 BIT
SECURITY MATCH
COMPARE REGISTER
128 BIT
SECURE MEMORY
COMMAND REGISTER
RANDOM DATA

FIG. 6a

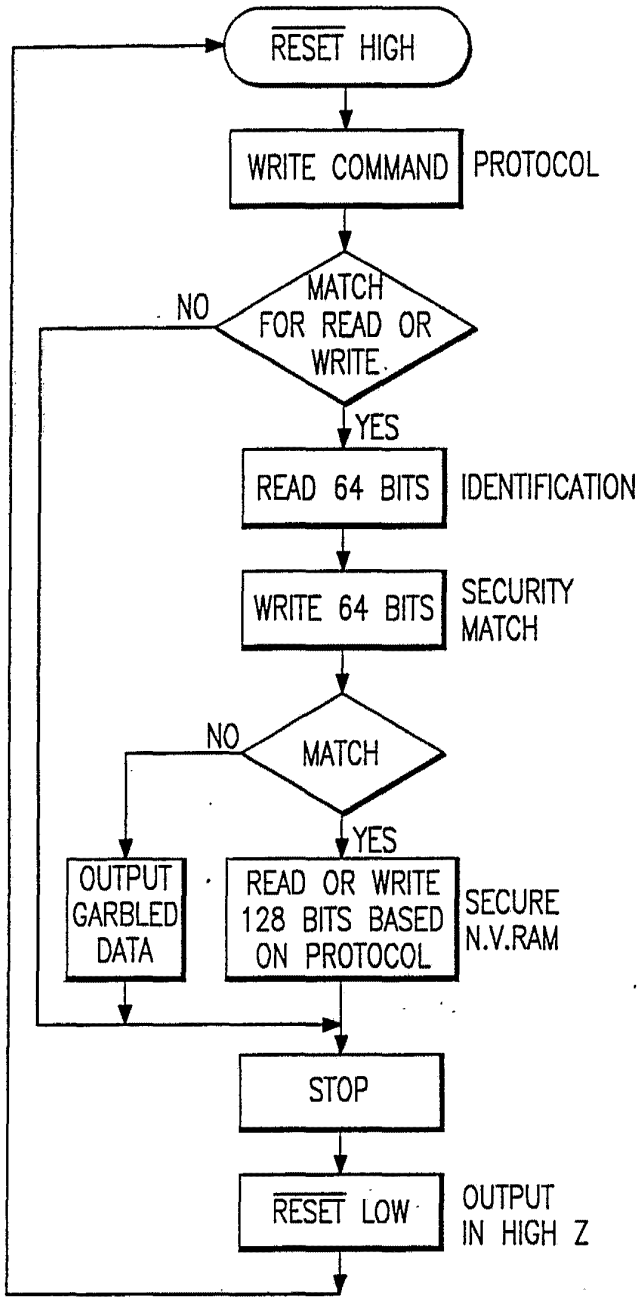


FIG. 6b

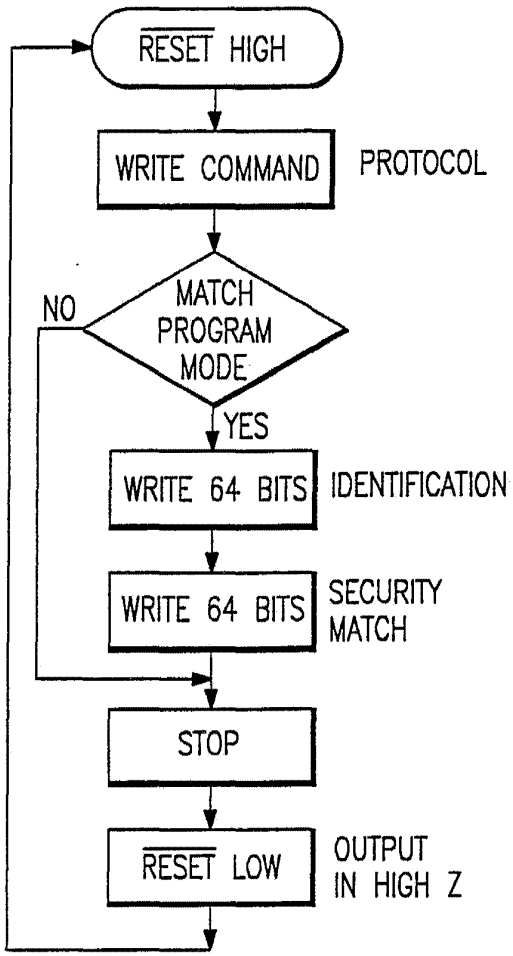


FIG. 6d

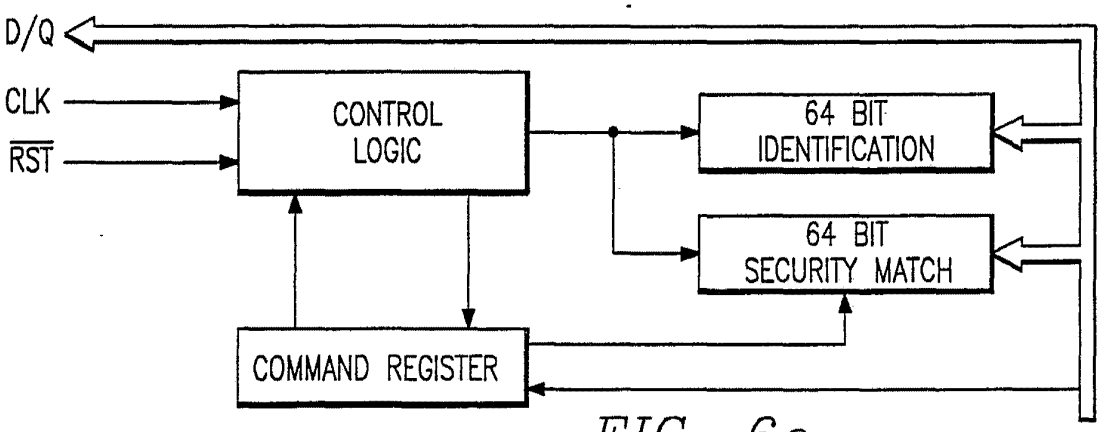


FIG. 6c

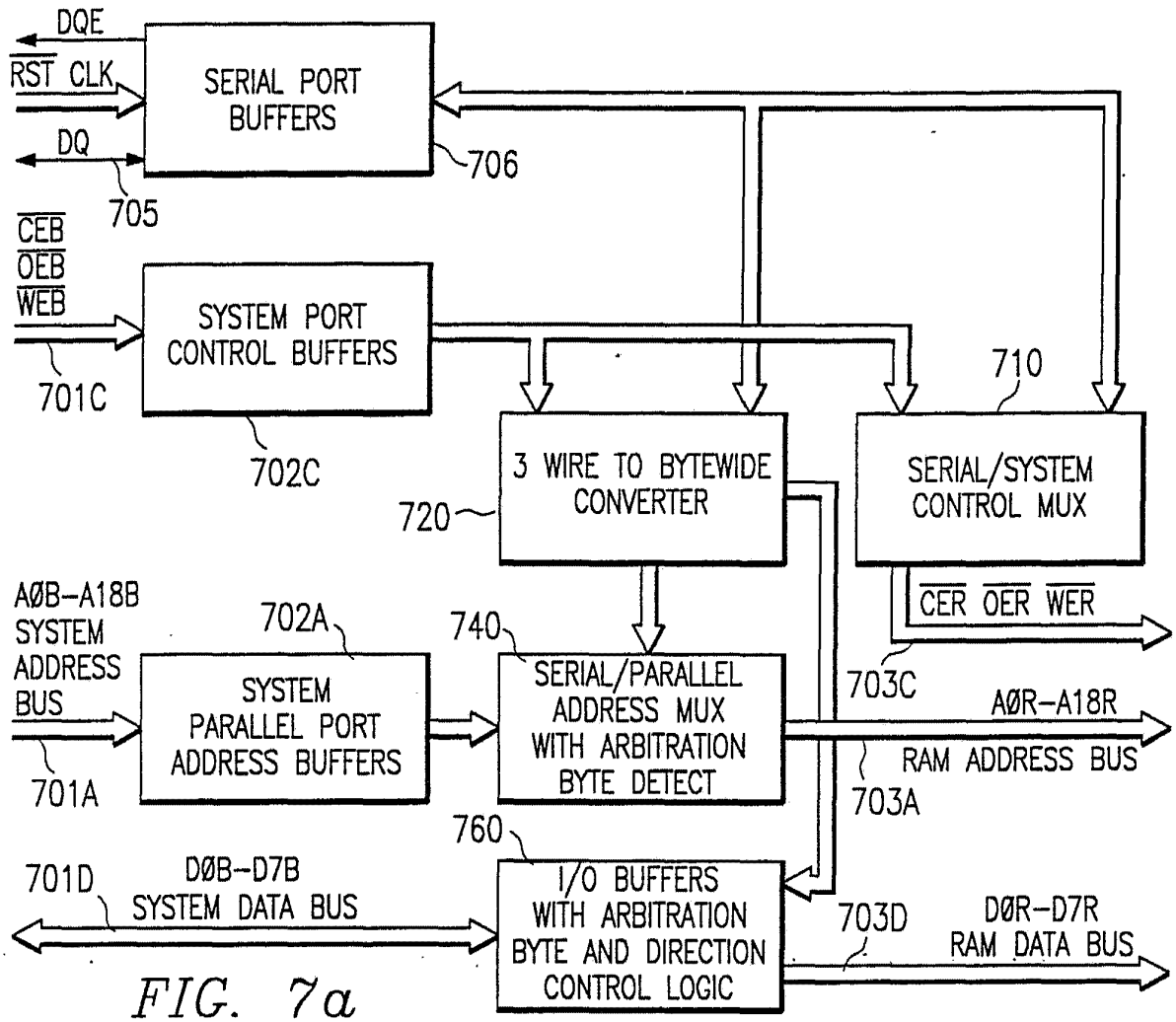

DQE
RST CLK
DQ
SERIAL PORT BUFFERS
706
705
CEB
OEB
WEB
SYSTEM PORT CONTROL BUFFERS
701C
702C
710
3 WIRE TO BYTEWIDE CONVERTER
720
SERIAL/SYSTEM CONTROL MUX
CER OER WER
703C
AØB–A18B SYSTEM ADDRESS BUS
702A
740
SYSTEM PARALLEL PORT ADDRESS BUFFERS
SERIAL/PARALLEL ADDRESS MUX WITH ARBITRATION BYTE DETECT
AØR–A18R
RAM ADDRESS BUS
703A
701A
760
701D
DØB–D7B SYSTEM DATA BUS
I/O BUFFERS WITH ARBITRATION BYTE AND DIRECTION CONTROL LOGIC
703D
DØR–D7R RAM DATA BUS

FIG. 7a

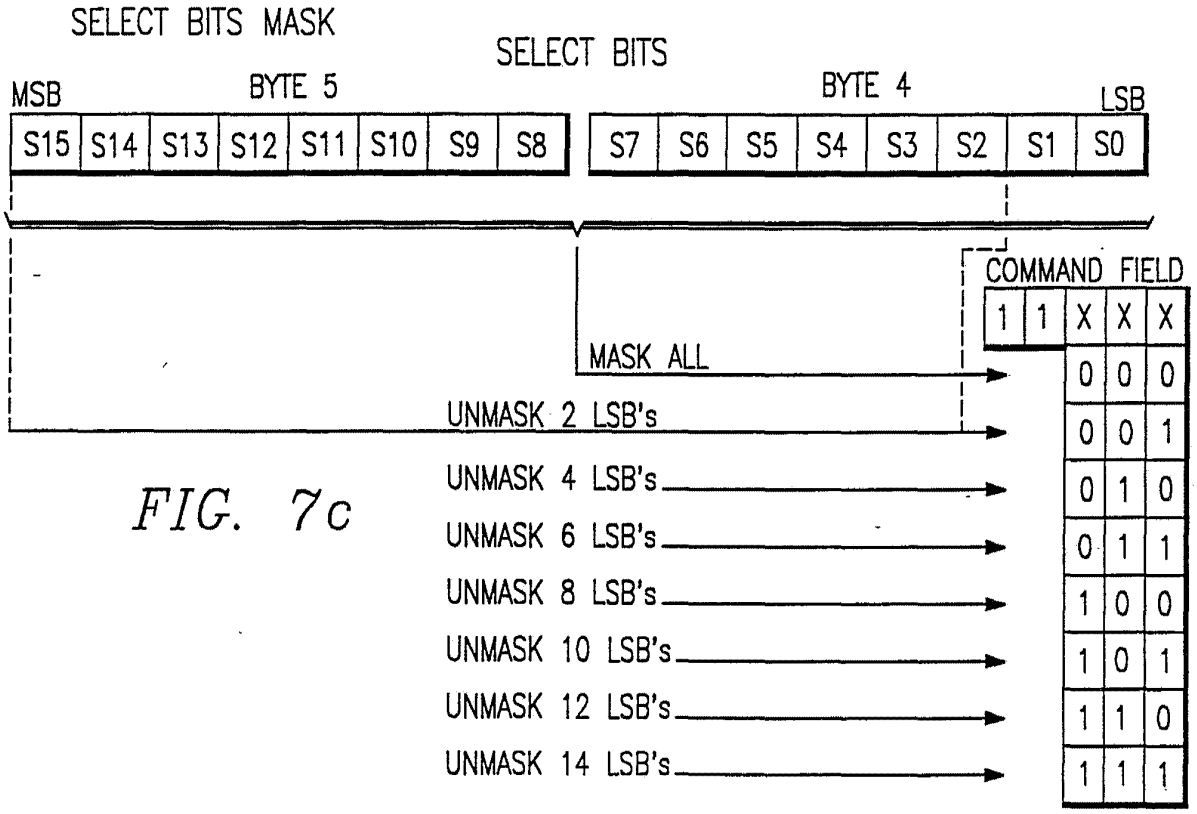

SELECT BITS MASK
SELECT BITS
MSB
BYTE 5
BYTE 4
LSB
S15 S14 S13 S12 S11 S10 S9 S8
S7 S6 S5 S4 S3 S2 S1 S0
COMMAND FIELD
1 1 X X X
MASK ALL
0 0 0
UNMASK 2 LSB's
0 0 1
UNMASK 4 LSB's
0 1 0
UNMASK 6 LSB's
0 1 1
UNMASK 8 LSB's
1 0 0
UNMASK 10 LSB's
1 0 1
UNMASK 12 LSB's
1 1 0
UNMASK 14 LSB's
1 1 1

FIG. 7c

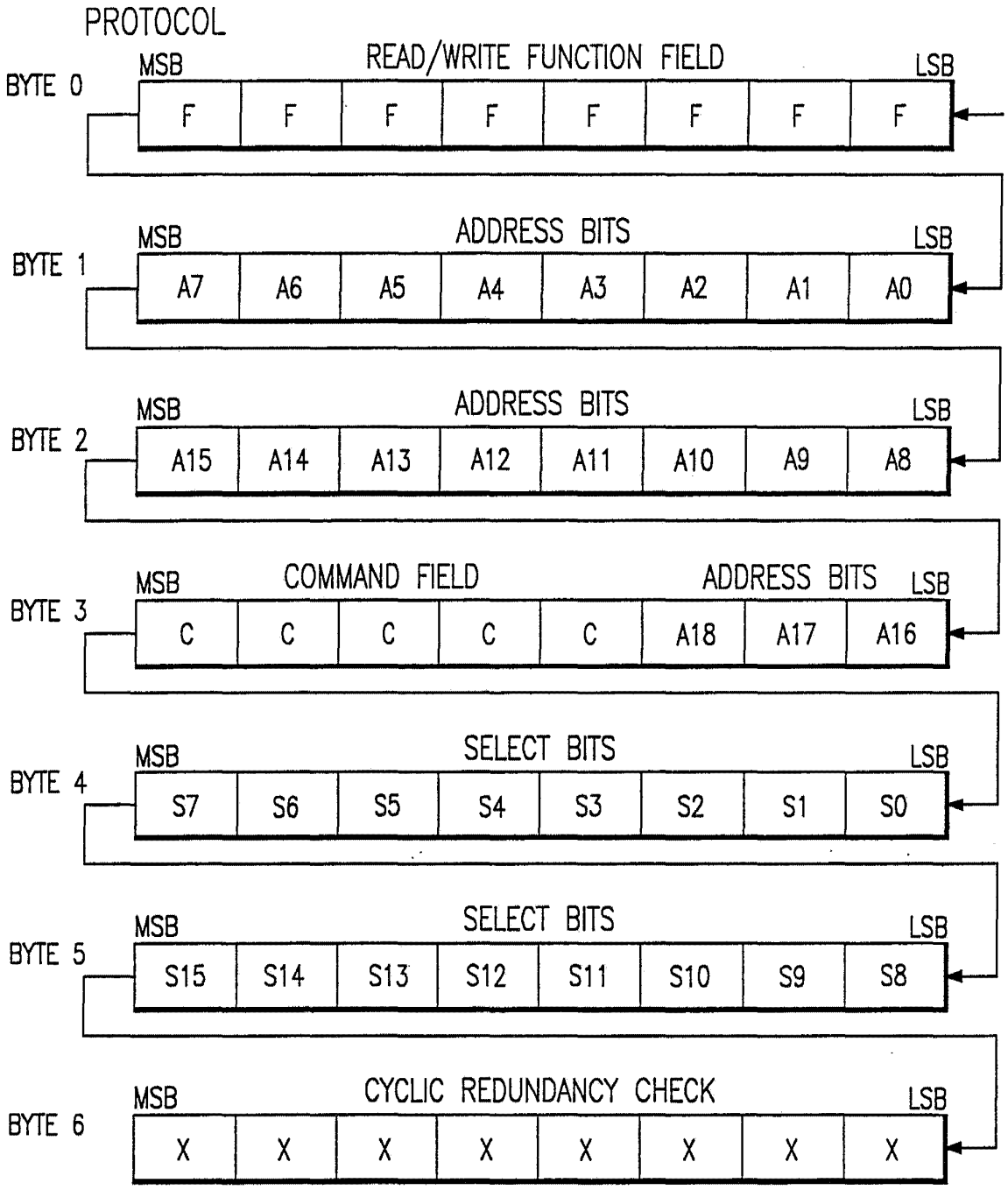

PROTOCOL
BYTE 0
MSB
READ/WRITE FUNCTION FIELD
LSB
F F F F F F F F
BYTE 1
MSB
ADDRESS BITS
LSB
A7 A6 A5 A4 A3 A2 A1 A0
BYTE 2
MSB
ADDRESS BITS
LSB
A15 A14 A13 A12 A11 A10 A9 A8
BYTE 3
MSB
COMMAND FIELD
ADDRESS BITS
LSB
C C C C C A18 A17 A16
BYTE 4
MSB
SELECT BITS
LSB
S7 S6 S5 S4 S3 S2 S1 S0
BYTE 5
MSB
SELECT BITS
LSB
S15 S14 S13 S12 S11 S10 S9 S8
BYTE 6
MSB
CYCLIC REDUNDANCY CHECK
LSB
X X X X X X X X

FIG. 7b

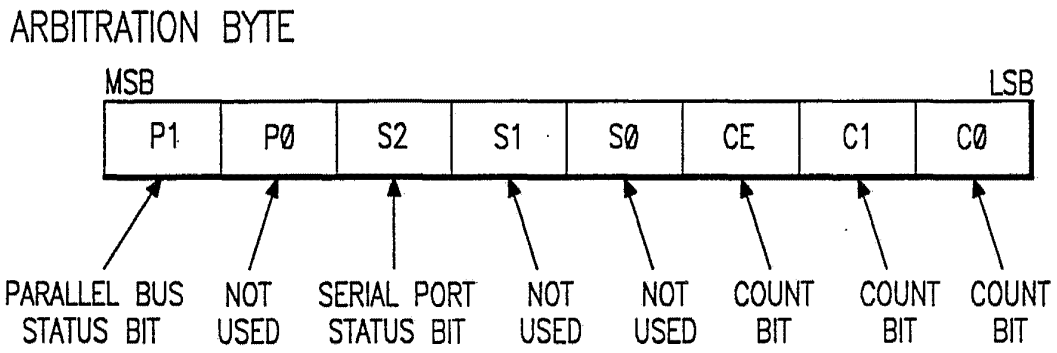

ARBITRATION BYTE
MSB
LSB
P1 PØ S2 S1 SØ CE C1 CØ
PARALLEL BUS STATUS BIT
NOT USED
SERIAL PORT STATUS BIT
NOT USED
NOT USED
COUNT BIT
COUNT BIT
COUNT BIT

FIG. 7d

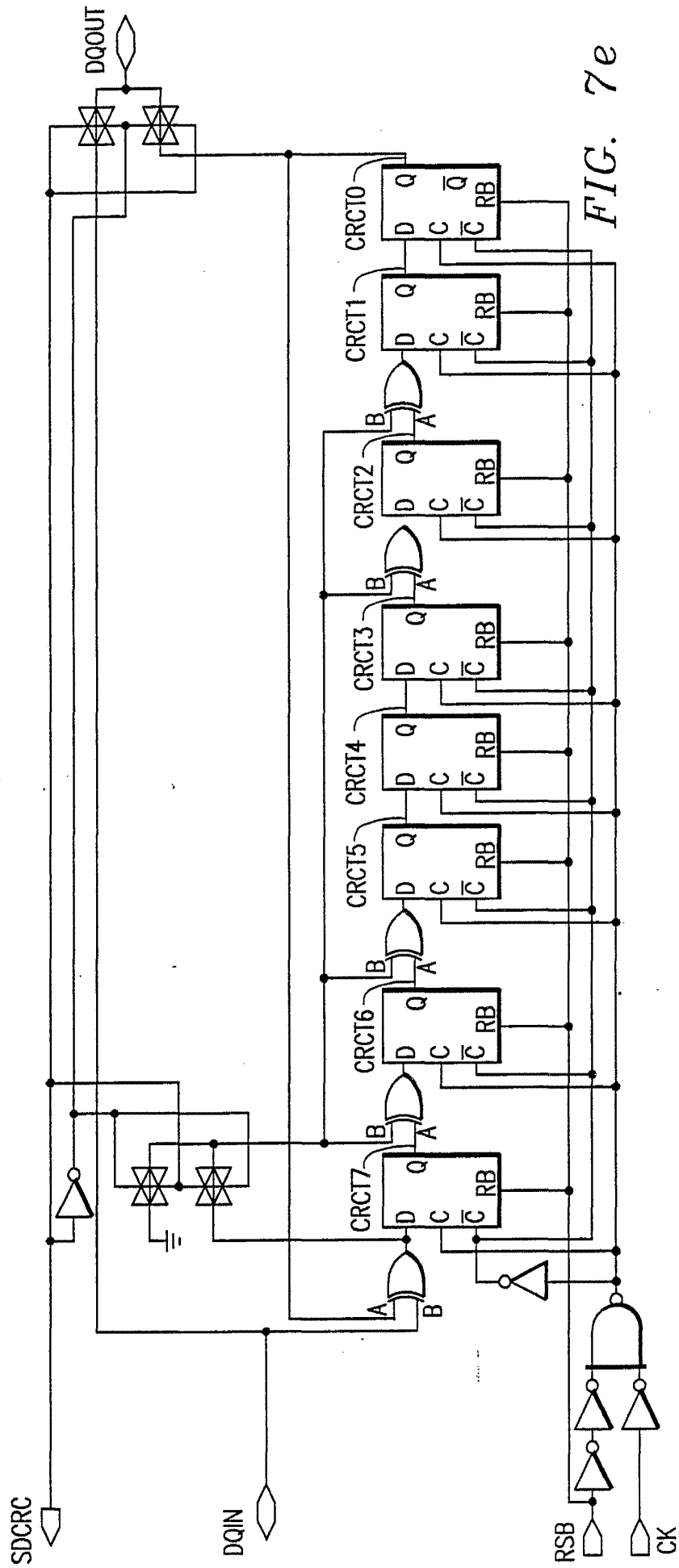

DQOUT
CRCT0
CRCT1
CRCT2
CRCT3
CRCT4
CRCT5
CRCT6
CRCT7
D
Q
C
RB
A
B
SDCRC
DQIN
RSB
CK

FIG. 7e

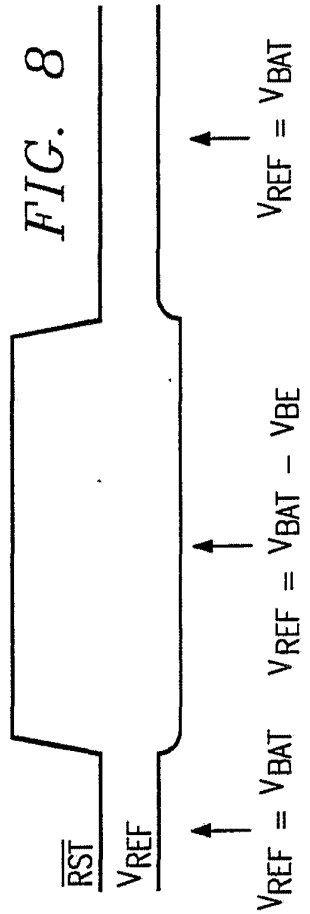

RST
VREF
VREF = VBAT
VREF = VBAT − VBE
VREF = VBAT

FIG. 8

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US89/05579

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT CL[5] H04B 1/00, 7/00; G06F 7/00; H04B 14/04

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
US	375/22, 25; 455/33,53,54,56,89,127,343; 370/95.2 379/61,62,93; 364/200,900; 340/825.44,825.47 340/825.54,825.5 825.52

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	US,A, 4,403,342 (BORRAS et al) 06 September 1983 See Figure 3	1,2,15-18,21 22,30 and 32-34
A	US,A, 4,132,950 (COCHRAN et al) 02 JANUARY 1979	1,2,15-18,21 22,30 and 32-34
A	US,A, 4,691,202 (DENNE et al) 01 September 1987	3 and 45-50
A	US,A, 4,129,855 (RODRIAN) 12 December 1978	3 and 45-50
Y,P	US,A, 4,839,642 (BATZ et al) 13 June 1989. See Column 3, lines 40-54 and Column 4, lines 12-27	4,31,37 and 38
Y	US,A, 4,752,949 (Steinbeck et al) 21 June 1988 See Column 13, lines 9-22	4,31,37 and 38

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
18 February 1990	14 MAR 1990
International Searching Authority	**Signature of Authorized Officer**
ISA/US	STEPHEN CHIN

Form PCT/ISA/210 (second sheet) (Rev.11-87)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
A	US,A, 3,962,553 (LINDER et al) 08 June 1976	7 and 36
A	US,A, 3,937,882 (BINGHAM) 10 February 1976	7 and 36
A	US,A, 4,153,877 (FATHAUER et al) 08 May 1979	7 and 36
A	US,A, 4,672,685 (PHILLIPS et al) 09 June 1987	7 and 36
A	US,A, 4,680,583 (GROVER) 14 July 1987	8,19 and 20
A	US,A, 4,689,619 (O'BRIEN, JR.) 25 August 1987	8,19 and 20
X	US,A, 4,300,236 (GILMOUR) 10 November 1981 See Fig. 2; Column 3, lines 9-46	9,28 and 29
Y	US,A, 4,599,745 (BARAN et al) 08 July 1986 See Fig. 29 and Columns 3-4	10 and 44
Y,P	US,A, 4,835,372 (GOMBRICH et al) 30 May 1989 See Column 24, lines 1-36	10 and 44
Y	US,A, 4,691,313 (IWATA) 01 September 1987 See Figs. 1 and 3	10 and 44
Y	US,A, 4,578,653 (HOWELL) 25 March 1986 See Fig. 4	11 and 51-54
X	US,A, 4,583,195 (DANIELS et al) 15 April 1986 See Figs. 2,3A and 3B	12,55 and 56
A	US,A, 4,409,495 (ENOMOTO et al) 11 October 1983	14 and 57-62
A	US,A, 4,788,456 (URMAN et al) 29 November 1988	14 and 57-62

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

A,P	US,A, 4,851,834 (STOCKEBRAND et al) 25 July 1989	5,13,34,35 and 39-43
A	US,A, 4,394,726 (KOHL) 19 July 1983	5,13,34,35 and 39-43
A	US,A, 4,654,788 (BOUDREAU et al) 31 March 1987	5,14,35 and 57-62
A	US,A, 4,247,908 (LOCKHART, JR. et al) 27 January 1981	6 and 23-27
A	US,A, 4,433,387 (DYER et al) 21 February 1984	6 and 23-27

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers , because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers , because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

3. ☐ Claim numbers_____, because they are dependent claims not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☒ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [2]

This International Searching Authority found multiple inventions in this international application as follows:

SEE ATTACHED PAPER

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application. Telephone practice

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.

ATTACHMENT TO FORM PCT/ISA/210, PART VI. 1.

1. Claims 1, 2, 15-18, 21, 30 and 32-34 are drawn to PCM communucation system; ckass 375 subclass 25.

2. Claims 3, 45-50 are drawn ti kiw power R.F. receiver; class 340 subclass 825.34.

3. Claims 4, 31, 37 and 38 are drawn to wireless data module with memory and conductive signal contacts; class 340 subclass 825.54.

4. Claims 5 and 35 are drawn to multiport memory system; 364 subclass 900.

5. Claims 6, 8, 19, 20 and 23-27 are drawn to a communication system having a base station and a plurality of remote stations; class 455 subclass 54.

6. Claims 7 and 36 are drawn to portable wireless transceiver; class 455 subclass 89.

7. Claims 9, 28 and 29 are drawn to a communication receiver; class 375 subclass 22.

8. Claims 10, 44 are drawn to a communication receiver; class 455 subclass 54.

9. Claims 11, 51-54 are drawn to a integrated bandpass filter; class 328 subclass 167.

10. Claims 12, 55 and 56 are drawn to power supply intercept circuit; class 455 subclass 127.

11. Claims 13 and 39-43 are drawn to multiport memory system; class 364 subclass 900.

12. Claims 14 and 57-62 are drawn to integrated circuit receiver; class 343 subclass 701.