

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00788
U.S. Patent No. 10,658,378
Issue Date: May 19, 2020

Title: THROUGH ARRAY CONTACT (TAC) FOR
THREE-DIMENSIONAL MEMORY DEVICES

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,658,378
PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42**

	<u>Page</u>
I. INTRODUCTION	1
II. REQUIREMENTS FOR INTER PARTES REVIEW	3
A. Grounds for Standing (37 C.F.R. §42.104(a))	3
B. Notice of Lead and Backup Counsel and Service Information (37 C.F.R. §§42.8(b)(3-4), 41.10(a))	3
C. Notice of Real-Parties-in-Interest (37 C.F.R. §42.8(b)(1)).....	5
D. Notice of Related Matters (37 C.F.R. §42.8(b)(2)).....	5
E. Fee for <i>Inter Partes</i> Review	6
F. Proof of Service.....	6
III. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§42.104(B))	6
IV. INSTITUTION SHOULD BE GRANTED.....	7
A. There Are No Grounds for a § 314 Discretionary Denial.....	7
1. Possibility of a Stay	7
2. Proximity of the Court’s Trial Date	8
3. Investment in the Parallel Proceeding	8
4. Issue Overlap.....	9
5. Party Overlap	9
6. Other Circumstances	9
B. Denial Under Section 325(d) Would Be Inappropriate	9
V. THE 378 PATENT	15
A. Technology Background	15
B. The 378 Patent.....	22
C. Prosecution History	23
VI. DESCRIPTION OF THE PRIOR ART	24
A. Toyama	24
B. Mushiga	26
C. Makala	26

VII.	CLAIM CONSTRUCTION	27
VIII.	LEVEL OF SKILL IN THE ART	27
IX.	GROUND 1: TOYAMA IN VIEW OF THE KNOWLEDGE OF A POSITA	28
A.	Claim 15:	28
1.	[15.PRE] “A three-dimensional (3D) memory device, comprising:”	28
2.	[15.A] “a substrate with an isolation structure;”	28
3.	[15.B] “an alternating conductor/dielectric layer stack disposed on the substrate;”	36
4.	[15.C] “a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;”	38
5.	[15.D] “channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;”	55
6.	[15.E] “a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;”	59
7.	[15.F] “a word line contact disposed on the conductor layer of the each level;”	62
8.	[15.G] “local contacts disposed on the channel structures and the slit structures; and”	63
9.	[15.H] “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.”	66
B.	Claim 16:	70
1.	[16] “The 3D memory device of claim 15, wherein the dielectric structure abuts a sidewall of each TAC of the TACs.”	70

C.	Claim 17:	72
1.	[17] “The 3D memory device of claim 15, wherein the dielectric structure comprises a through array contact region of the 3D memory device.”	72
D.	Claim 19:	75
1.	[19] “The 3D memory device of claim 15, wherein the dielectric material comprises silicon oxide.”	75
E.	Claim 20:	76
1.	[20] “The 3D memory device of claim 15, wherein the TACs comprise a conductive material.”	76
X.	GROUND 2: MUSHIGA IN VIEW OF THE KNOWLEDGE OF A POSITA	77
A.	Claim 15:	77
1.	[15.PRE] “A three-dimensional (3D) memory device, comprising:”	77
2.	[15.A] “a substrate with an isolation structure;”	78
3.	[15.B] “an alternating conductor/dielectric layer stack disposed on the substrate;”	80
4.	[15.C] “a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;”	81
5.	[15.D] “channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;”	86
6.	[15.E] “a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;”	91
7.	[15.F] “a word line contact disposed on the conductor layer of the each level;”	92

8.	[15.G] “local contacts disposed on the channel structures and the slit structures; and”	94
9.	[15.H] “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.”	98
B.	Claim 16:	99
1.	[16] “The 3D memory device of claim 15, wherein the dielectric structure abuts a sidewall of each TAC of the TACs.”	99
C.	Claim 17:	100
1.	[17] “The 3D memory device of claim 15, wherein the dielectric structure comprises a through array contact region of the 3D memory device.”	100
D.	Claim 19:	101
1.	[19] “The 3D memory device of claim 15, wherein the dielectric material comprises silicon oxide.”	101
E.	Claim 20:	102
1.	[20] “The 3D memory device of claim 15, wherein the TACs comprise a conductive material.”	102
XI.	GROUND 3: MUSHIGA AND MAKALA IN VIEW OF THE KNOWLEDGE OF A POSITA.....	102
A.	Claim 15	102
B.	Claims 16-17 and 19-20	105
XII.	SECONDARY CONSIDERATIONS	106
XIII.	CONCLUSION.....	106
	Dated: April 30, 2024 /Jeremy Jason Lang/	106

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>ABS Glob., Inc. v. Cytonome/St, LLC</i> , 84 F.4th 1034 (Fed. Cir. 2023)	68
<i>Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH</i> , IPR2019-01469, Paper 6 (PTAB February 13, 2020)	9, 10
<i>Agrizap, Inc. v. Woodstream Corp.</i> , 520 F.3d 1337 (Fed. Cir. 2008)	48
<i>Apple Inc. v. Fintiv, Inc.</i> , Case No. IPR2020-00019, Paper No. 11 (PTAB Mar. 20, 2020)	7, 8
<i>Becton, Dickinson, and Co. v. B. Braun Melsungen AG</i> , IPR2017-01586, Paper 8 (Dec. 15, 2017).....	10, 11, 13
<i>KCJ Corp. v. Kinetic Concepts, Inc.</i> , 223 F.3d 1351 (Fed. Cir. 2000)	41
<i>Retractable Techs., Inc. v. Becton, Dickinson & Co.</i> , 653 F.3d 1296 (Fed. Cir. 2011)	47
<i>Samsung Bioepis Co. Ltd. v. Alexion Pharmaceuticals, Inc.</i> , IPR2023-01070, Paper 9 (PTAB Dec. 19, 2023)	10
<i>Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC</i> , IPR2019-01393, Paper 24 (PTAB June 16, 2020)	7, 8, 9
<i>Yangtze Memory Technologies Co., Ltd. v. Micron Technology, Inc. & Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL (N.D. Cal., filed Nov. 9, 2023)	5
Statutes	
35 U.S.C. §§ 102	24, 26, 27

Other Authorities

37 C.F.R. §42.8 3

37 C.F.R. §42.10 3, 5

37 C.F.R. §42.15 6

37 C.F.R. §42.104 3

LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 10,658,378 to Tao et al.
1002	File History of U.S. Patent No. 10,658,378 to Tao et al.
1003	Declaration of Dr. Jack C. Lee (“Lee”)
1004	<i>Curriculum Vitae</i> of Dr. Jack C. Lee
1005	U.S. Patent Publ. No. 2017/0179026 A1 (“Toyama”)
1006	U.S. Patent No. 10,354,980 (“Mushiga”)
1007	U.S. Patent No. 10,262,945 (“Makala”)
1008	Minute Order, Dkt. No. 42, dated February 22, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1009	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1010	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1011	CN109075169A Office Action, dated November 14, 2019
1012	Certified Translation of CN109075169A Office Action, dated November 14, 2019
1013	CN109075169A Reexamination Decision, dated November 25, 2021
1014	Certified Translation of CN109075169A Reexamination Decision, dated November 25, 2021
1015	Michelsoni, “3D Flash Memories” (2016)

Petition for *Inter Partes* Review of U.S. Patent No. 10,658,378

Exhibit	Description
1016	Aritome, “NAND Flash Memory Technologies” (2016)
1017	U.S. Patent No. 9,620,512 to Nishikawa et al.
1018	U.S. Patent Publ. No. 2016/0056188 A1 to Lee et al.
1019	U.S. Patent No. 9,293,348 to Lai et al.
1020	U.S. Patent No. 10,103,169 to Ge et al.
1021	U.S. Patent No. 8,697,519 to Jee et al.
1022	Excerpts from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)

Petitioner Micron Technology, Inc. (“Micron” or “Petitioner”) respectfully requests *Inter Partes* Review (“IPR”) of claims 15-17 and 19-20 (“the Challenged Claims”) of U.S. Patent Number 10,658,378 (the “378 Patent”). There is more than a reasonable likelihood that Petitioner will prevail with respect to at least one claim.

I. INTRODUCTION

The 378 Patent’s title is “Through Array Contact (TAC) for Three-Dimensional Memory Devices.” As its title suggests, the 378 Patent relates to a three-dimensional (3D) NAND memory device with “through array contacts” (“TACs”). TACs are electrical connections that extend through the device’s memory array and may, for example, connect the memory array to a peripheral device located underneath the memory array.

Most elements of the Challenged Claims are conventional for 3D NAND memory devices, which existed long before the 378 Patent’s priority date. And the alleged point of novelty—the TACs—were not, in fact, new. Two primary references discussed in this Petition—Toyama and Mushiga—disclose and/or render obvious the “through array contacts” and all other elements of the Challenged Claims. The Petition combines a third reference, Makala, with Mushiga as an alternative ground.

The Applicant did not disclose to the Examiner, nor did the Examiner cite, Mushiga or Makala. Mushiga alone and in combination with Makala render all

Challenged Claims obvious, and the Board should grant institution for that reason alone.

After the Chinese Patent Office rejected all claims of the Chinese counterpart to the 378 Patent as unpatentable in view of Toyama, Patent Owner cited Toyama to the U.S. Examiner. However, despite the Chinese Patent Office rejecting a claim materially identical to the independent claim challenged in this Petition, Patent Owner did *not* provide the U.S. Examiner with the Chinese rejection that specifically mapped Toyama to that claim. Perhaps due to Patent Owner's omission of the bases for the Chinese rejection, the Examiner never discussed or relied on Toyama in any rejection, overlooking that Toyama teaches or renders obvious all elements of the Challenged Claims. Confirming this, after Patent Owner appealed the Chinese rejection, a three-member panel of the Chinese Patent Office affirmed that all claims are unpatentable over Toyama. That the U.S. Examiner overlooked material teachings in Toyama provides a further reason for the Board to institute trial here.

In sum, because the Challenged Claims encompass prior art 3D NAND memory devices, and are nothing more than a routine, predictable combination of known elements, Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable as obvious under Section 103.

II. REQUIREMENTS FOR INTER PARTES REVIEW

A. Grounds for Standing (37 C.F.R. §42.104(a))

Petitioner certifies that the 378 Patent is available for IPR and that no law bars Petitioner from requesting IPR of the Challenged Claims of the 378 Patent on the grounds identified herein.

B. Notice of Lead and Backup Counsel and Service Information (37 C.F.R. §§42.8(b)(3-4), 41.10(a))

Pursuant to 37 C.F.R. §§42.8(b)(3-4) and 41.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

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Petitioner consents to service by electronic mail at the following addresses: PTABDocketJL2@orrick.com, P52PTABDocket@orrick.com, PTABDocketJ3B3@orrick.com, T61PTABDocket@orrick.com, PTABDocketP2S7@orrick.com, and micron-ymtc_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner attaches a Power of Attorney.

C. Notice of Real-Parties-in-Interest (37 C.F.R. §42.8(b)(1))

Petitioner Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real-parties in interest.

D. Notice of Related Matters (37 C.F.R. §42.8(b)(2))

According to USPTO assignment records, the 378 Patent is currently assigned to Yangtze Memory Technologies, Co., Ltd. (“YMTC” or “Patent Owner”). YMTC has asserted the 378 Patent and U.S. Patent Nos. 10,861,872, 10,868,031, 10,937,806, 10,950,623, 11,468,957, 11,501,822, and 11,600,342 in a co-pending litigation, *Yangtze Memory Technologies Co., Ltd. v. Micron Technology, Inc. & Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed Nov. 9, 2023) (“Co-Pending Litigation”).

In addition to this Petition, Petitioner is filing petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation: Petition for *Inter Partes* Review of U.S. Patent No. 10,861,872, IPR2024-00789, Petition for *Inter Partes* Review of U.S. Patent No. 10,868,031, IPR2024-00790, Petition for *Inter Partes*

Review of U.S. Patent No. 10,937,806, IPR2024-00791, Petition for *Inter Partes* Review of U.S. Patent No. 10,950,623, IPR2024-00794, Petition for *Inter Partes* Review of U.S. Patent No. 11,468,957, IPR2024-00792, Petition for *Inter Partes* Review of U.S. Patent No. 11,501,822, IPR2024-00795 and Petition for *Inter Partes* Review of U.S. Patent No. 11,600,342, IPR2024-00793.

E. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. §42.15(a), and any other required fees, to Deposit Account No. 15-0665.

F. Proof of Service

Petitioner has attached proof of service of this Petition on the Patent Owner at the correspondence addresses of record for the 378 Patent.

III. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§42.104(B))

This Petition assumes that the '378 Patent's earliest-listed priority date of May 3, 2018 is the priority date (the "Priority Date").

Petitioner relies on the following references: (1) U.S. Pat. Pub. No. 2017/0179026 (Ex. 1005, "Toyama"); (2) U.S. Pat. No. 10,354,980 (Ex. 1006, "Mushiga"); and (3) U.S. Pat. No. 10,262,945 (Ex. 1007, "Makala").

Petitioner challenges the claims on the following grounds:

Ground 1: Claims 15-17 and 19-20 would have been obvious over Toyama in view of the knowledge of a person of ordinary skill in the art ("POSITA");

Ground 2: Claims 15-17 and 19-20 would have been obvious over Mushiga in view of the knowledge of a POSITA; and

Ground 3: Claims 15-17 and 19-20 would have been obvious over Mushiga and Makala in view of the knowledge of a POSITA.

The Declaration of Dr. Jack C. Lee (Ex. 1003, “Lee”) supports these grounds.

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There Are No Grounds for a § 314 Discretionary Denial

Petitioner submits that it presents a compelling case here: the claims of the 378 Patent are unambiguously unpatentable, and thus the Board should not discretionarily deny in view of the parallel district court case. 6/21/22 Interim Procedure, 2, 4-5.

Petitioner also notes the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”).

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking*

LLC, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) (“*Sand Revolution*”); *Fintiv* at 12 (similar).

2. Proximity of the Court’s Trial Date

The district court entered a scheduling order which set a trial date of December 1, 2025. *See* Ex. 1008. If IPR proceedings are instituted, they should be completed well before the scheduled trial date. *See also* Ex. 1009 (statistics indicating 48.9 month average time-to-trial in district). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

To date, the parties and Court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings, no substantive progress has been made. The parties are months away from completing the exchange of infringement and invalidity contentions and have not taken any depositions. Fact discovery is in its infancy. No claim construction positions have been exchanged, no claim construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution* at 11.

The Board also has explained institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv* at 11. Against 8 patents, Petitioner did

so, filing approximately 5 ½ months after being served with the original complaint and 3 months after the filing of an amended complaint. *See* Ex. 1010. This also weighs strongly in favor of institution.

4. Issue Overlap

Given the early stage of the parallel proceeding, it is not yet possible to determine the amount of overlap. Moreover, should the Board institute, Micron stipulates it will not advance in District Court any invalidity grounds advanced in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found such stipulations weigh in favor of institution. *Sand Revolution* at 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

6. Other Circumstances

The Petition has significant substantive merit, including understandable prior art the Patent Office did not previously consider. Thus, this factor also weighs in favor of institution.

B. Denial Under Section 325(d) Would Be Inappropriate

The *Advanced Bionics* framework weighs against section 325(d) denial. The grounds in the Petition rely on three primary references: Mushiga, Makala, and

Toyama. Neither the Examiner nor the patentee cited or discussed Mushiga or Makala during prosecution. Although Patent Owner cited Toyama, the fact that neither Mushiga nor Makala was cited, and the fact that they render the claims obvious independent of Toyama, means the Board should not invoke section 325(d), and need not reach Part II. *Samsung Bioepis Co. Ltd. v. Alexion Pharmaceuticals, Inc.*, IPR2023-01070, Paper 9 (PTAB Dec. 19, 2023), at 61 (Board proceeds to Part II only if Office considered “all of the references relied on by Petitioner”). Regardless, at Part II, the record demonstrates the Examiner erred by overlooking Toyama’s disclosures and failing to reject the claims in light of Toyama.

“[I]f the record of the Office’s previous consideration of the art is not well developed or silent, then a petitioner may show the Office erred by overlooking something persuasive.” *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (PTAB February 13, 2020), at 10 (precedential).

The record here is silent as to what, if any, substantive consideration the Examiner gave Toyama. As an initial matter, the Examiner never discussed Toyama or its teachings. *Becton, Dickinson, and Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (Dec. 15, 2017), at 22-23 (factor (c)).

What’s more, Patent Owner’s conduct during prosecution may have prevented the Examiner from appreciating Toyama’s significance. During prosecution, the

Examiner issued an Office Action rejecting the then pending independent claims as obvious over two references, Nishikawa and Lee. However, the Examiner indicated dependent claim 17 was allowable over these references. Claim 17 recited structures that, as this Petition explains, were commonplace in prior art 3D NAND memory devices and well-known to a POSITA: *a staircase structure, a word line contact, and a local contact disposed on each channel structure and slit structure.*¹ Section V.A; *Becton, Dickinson*, at 25-28 (factor (f)). The Examiner only allowed now-challenged independent claim 15 after Patent Owner rewrote it to incorporate the limitations of original claim 17.

After the Office Action, but before Patent Owner's response to it, the Chinese Patent Office rejected all claims of the corresponding Chinese patent application as unpatentable over Toyama.² Ex. 1012 (Certified Translation of CN109075169A Office Action, dated November 14, 2019), 3-10. The Chinese Patent Office's rejection explained how specific elements of Toyama taught the claim limitations.

¹ All red italicized text in this Petition is a quotation of the 378 Patent's claim language.

² Both the Chinese patent application and the application that issued as the 378 Patent claim priority to, and are national stage applications of, PCT App. No. PCT/CN2018/085421.

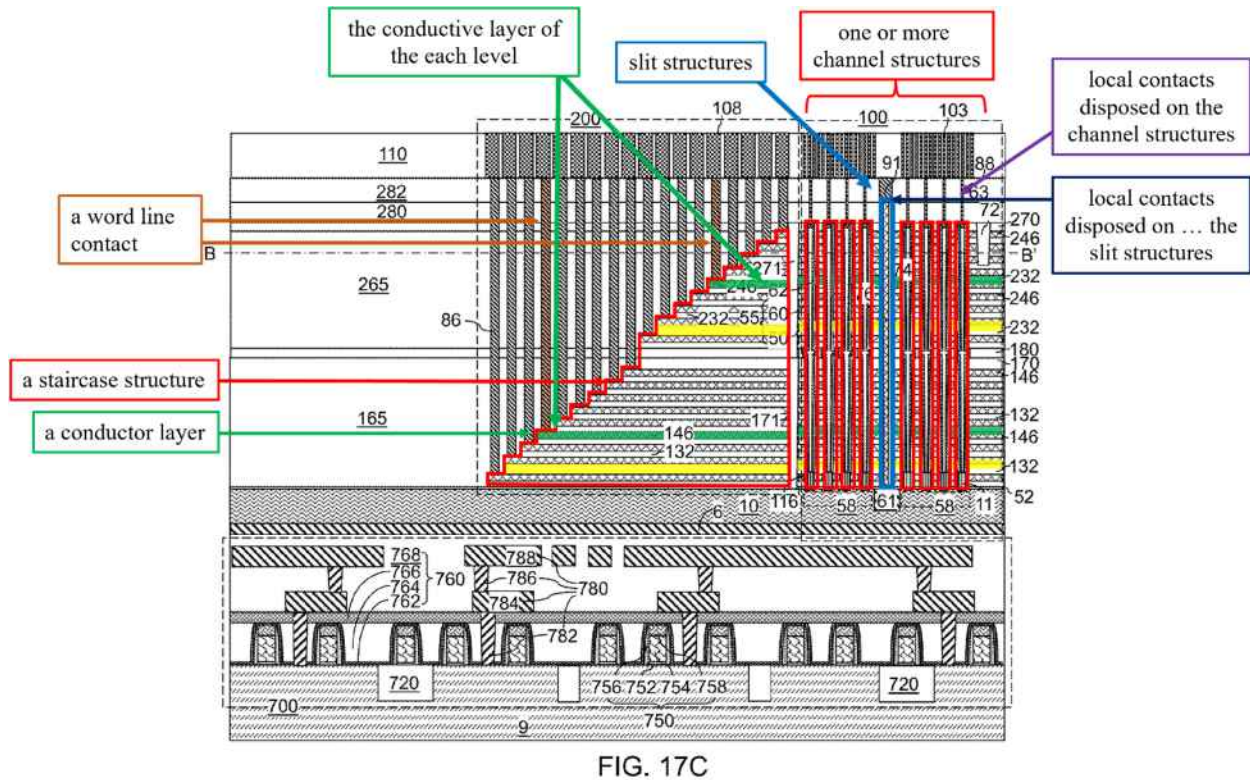
Id. One of the claims rejected by the Chinese Patent Office, claim 29, is materially identical to original U.S. claim 17.³

Thus, at the time Patent Owner secured issuance by rewriting original claim 17 into independent form, it knew the Chinese Patent Office had rejected a materially identical claim in view of a reference the U.S. Examiner was not aware of when he indicated claim 17's allowability. Despite this, Patent Owner never notified the Examiner of the rejection or provided the Examiner with the Chinese Patent Office's written rejection or its reasoning. Patent Owner's failure to disclose the Chinese Patent Office's reasoning—including the specific relied-upon elements of Toyama—may have been especially material because of Toyama's length (the reference spans 143 figures and 178 pages). In essence, Patent Owner only gave the Examiner a haystack (i.e., Toyama) despite also knowing the location of the needle (i.e., the specific elements of Toyama identified by the Chinese Patent Office).

³ Both claims depend on materially identical independent claims (claims 28 of the Chinese application, and original claim 16 of the U.S. application). And both claims recite a *staircase structure* (“a ladder structure,” in the English translation of the Chinese claim), a *word line contact*, and *local contacts disposed on the channel structures and the slit structures* (“local contacts disposed on each channel structure and crevice structure,” in the English translation of the Chinese claim).

The Petition demonstrates the Examiner erred by overlooking specific teachings in Toyama. *Becton, Dickinson*, at 24-25 (factor (e)). As noted above, the Examiner only allowed the Challenged Claims of the 378 Patent after the applicant rewrote them to incorporate the limitations of original claim 17. As illustrated below, Toyama teaches each of these limitations:

1. *a staircase structure disposed in the alternating conductor/dielectric layer stack* (Toyama’s “alternating stack (132, 146, 232, 246)”), *wherein the staircase structure comprises levels with each level having a conductor layer thereon* (Toyama’s “electrically conductive layers (146, 246)”);
2. *a word line contact* (“word line contact via structures 86”) *disposed on each conductor layer of the staircase structure* (Toyama’s “first and second conductive material layers (146, 246)”; and
3. *a local contact* (“drain contact via structures 88”) *disposed on each channel structure* (“memory stack structures 55”), and *a local contact* (“source connection via structures 91”) *disposed on each slit structure* (“laterally-elongated contact via structures 76”):



Toyama, Figure 17C; *see generally* Part VIII.⁴

The Chinese prosecution history confirms Toyama's merit as an invalidating reference. After the Chinese Examiner maintained the rejection of all claims in view of Toyama, Patent Owner appealed. On appeal, a three-judge panel of the Chinese Patent Office affirmed the Chinese Examiner's rejection of all claims of a related Chinese patent application as unpatentable over Toyama. Ex. 1014 (Certified Translation of CN109075169A Reexamination Decision, dated November 25,

⁴ Toyama's fourth exemplary structure (also relied upon in this Petition) also discloses the same elements.

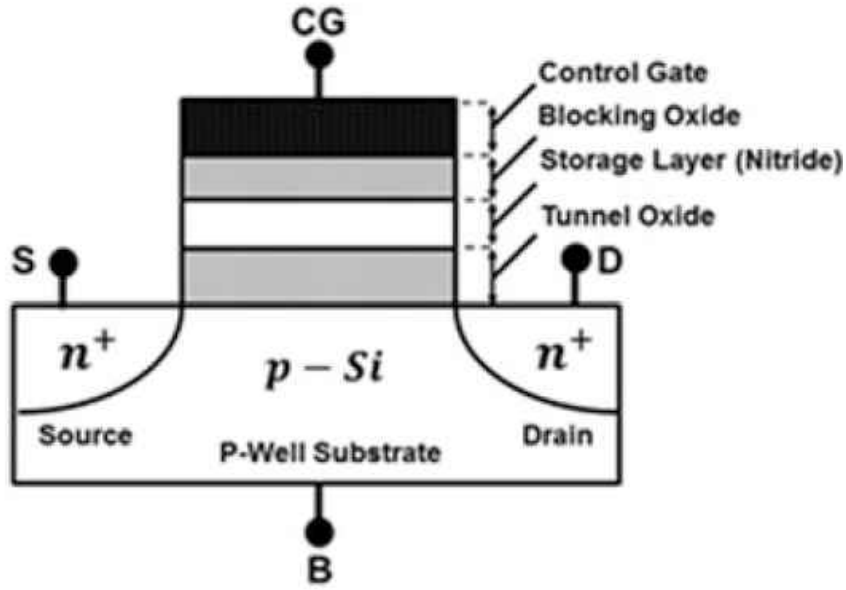
2021). Notably, the Chinese Patent Office cited to the exact same structures identified in this Petition as disclosing the elements of Chinese claim 29 (i.e., original U.S. claim 17). *Id.*, 6, 14. To date, Patent Owner has been unable to obtain a patent in its native China corresponding to the 378 Patent. And also to date, PO has not disclosed this important information to the Patent Office in any continuation of the '378 Patent.

Because the U.S. Examiner never considered Mushiga and Makala, and overlooked specific teachings in Toyama that disclose what the U.S. Examiner considered as the point of novelty (the elements of original claim 17), the Board should not exercise its discretion under section 325(d) to deny institution.

V. THE 378 PATENT

A. Technology Background

The 378 Patent relates to three-dimensional (3D) NAND flash memory. “NAND” flash memory is a particular type of flash memory where cells form a structure similar to that of a NAND (not-AND) logic gate. Lee, ¶¶ 40-42; Ex. 1015, 14. At the core of a NAND flash memory is a “memory cell,” which stores information as electrical charge. Lee ¶ 41. One example of a memory cell as shown below:



Ex. 1015, 41. In a memory cell, current flows from the “drain” of the device to the “source” of the device, which is connected to ground (e.g., the negative terminal of a power connection). *Id.*, 150 (“[T]he Source Line ... plays the role of the ‘local ground’ for each memory cell.”); Lee, ¶ 41. A flash memory controller reads from or writes to a memory cell by applying a voltage to that cell’s “control gate,” labeled as “CG” in the above figures. *Id.*, ¶ 43.

Initially, a NAND flash memory was “planar,” that is, two-dimensional (2D). Lee, ¶ 44. In 2D NAND flash memory, all memory cells lie on a 2D plane (*i.e.*, the x-y plane) on the surface of a memory chip as shown below:

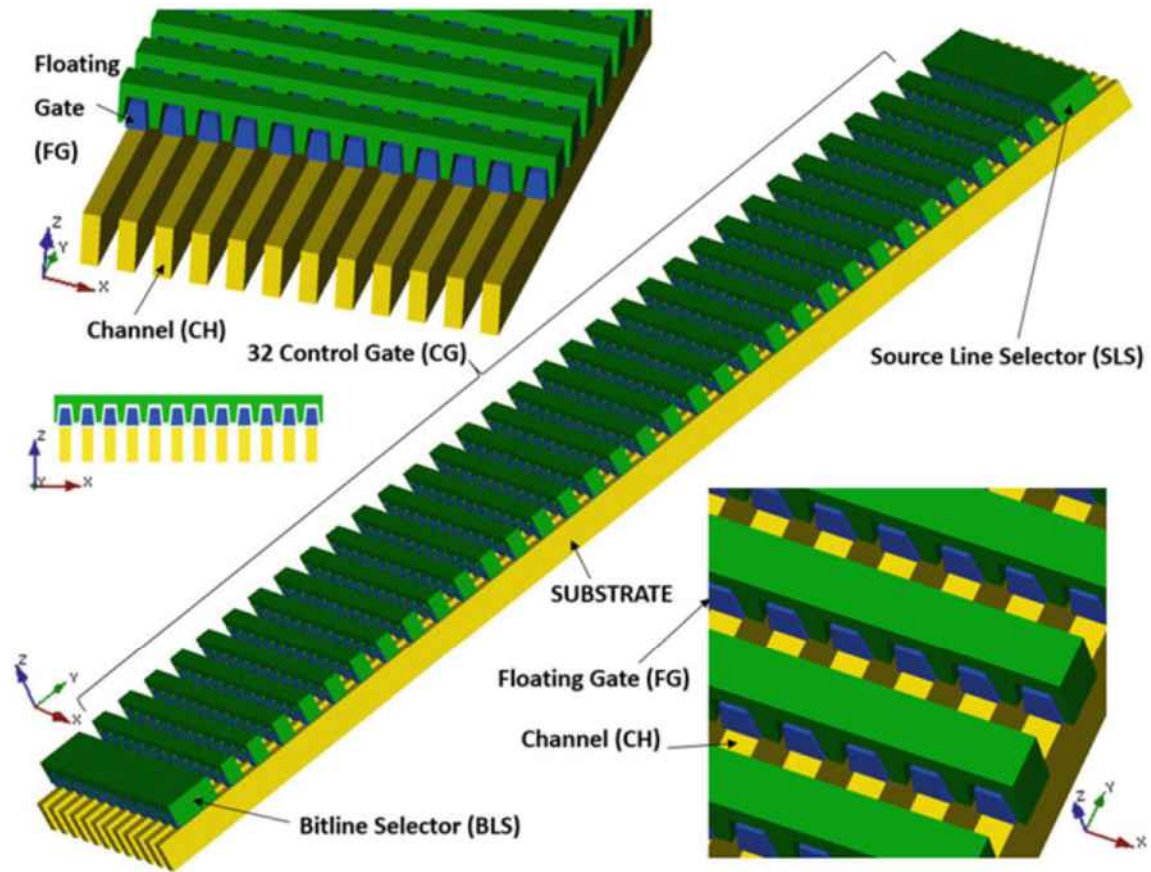


Fig. 3.9 Bird's-eye view of a planar NAND string

Ex. 1015, at 86.

Well before the priority date of the 378 Patent, Petitioner and others had developed techniques for manufacturing 3D NAND flash memory. Lee, ¶¶ 54-57. In a 3D NAND flash memory, memory cells exist in vertical, cylindrical NAND flash “strings”:

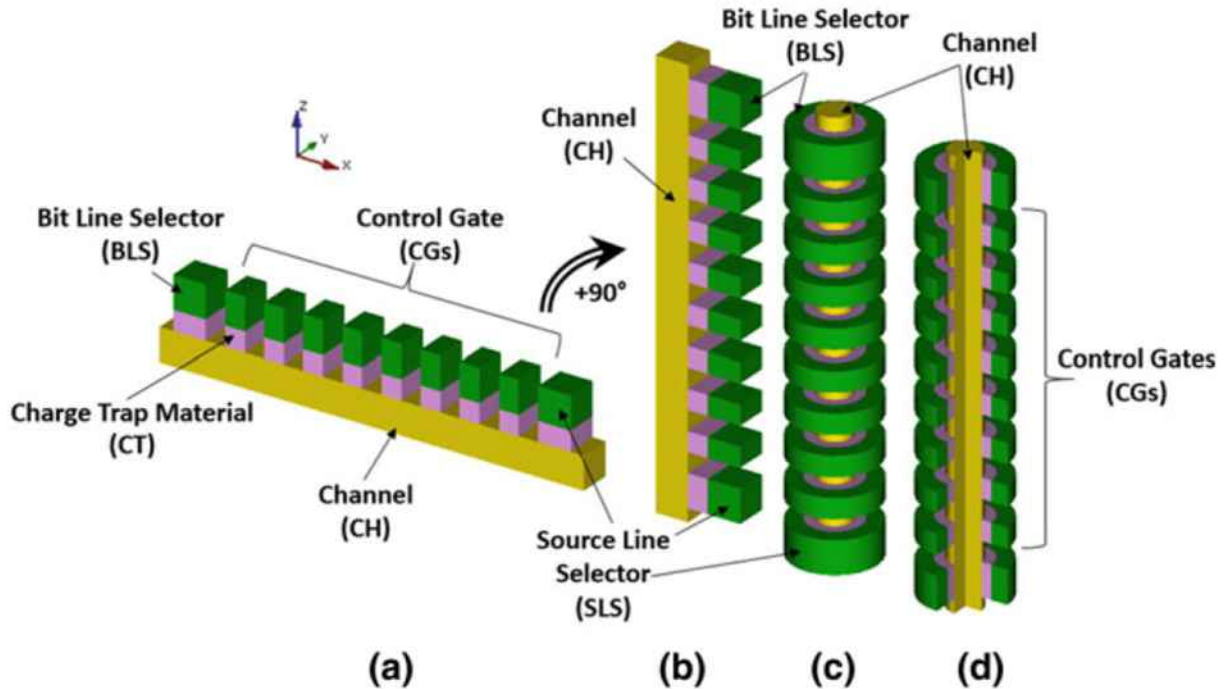


Fig. 4.1 NAND Flash string with horizontal gate and vertical channel: **a** planar, **b** planar rotated by 90°, **c** vertical channel with cylindrical shape and **d** its cross section

Ex. 1015, at 102; Lee, ¶¶ 45-48. As labeled in Figure 4.1, above, each NAND string includes a “cylindrical channel.” EX1015, 58; Lee, ¶¶ 45-48.

A number of architectures for constructing a memory device out of NAND strings were known in the art. For example, in the well-known BiCS (Bit Cost Scalable) architecture, various “contacts,” that is, electrical connections, are on top of the memory array. These include source line contacts (for providing a ground connection to the memory cells):

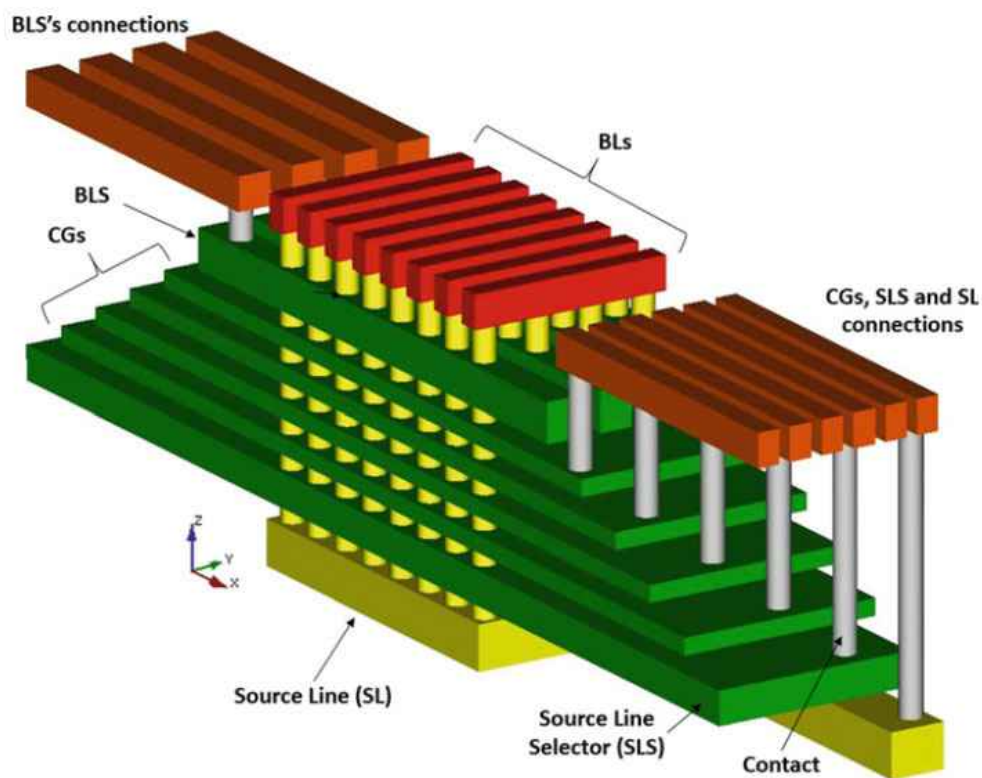


Fig. 4.13 Top bird's eye view of BiCS with gate connections

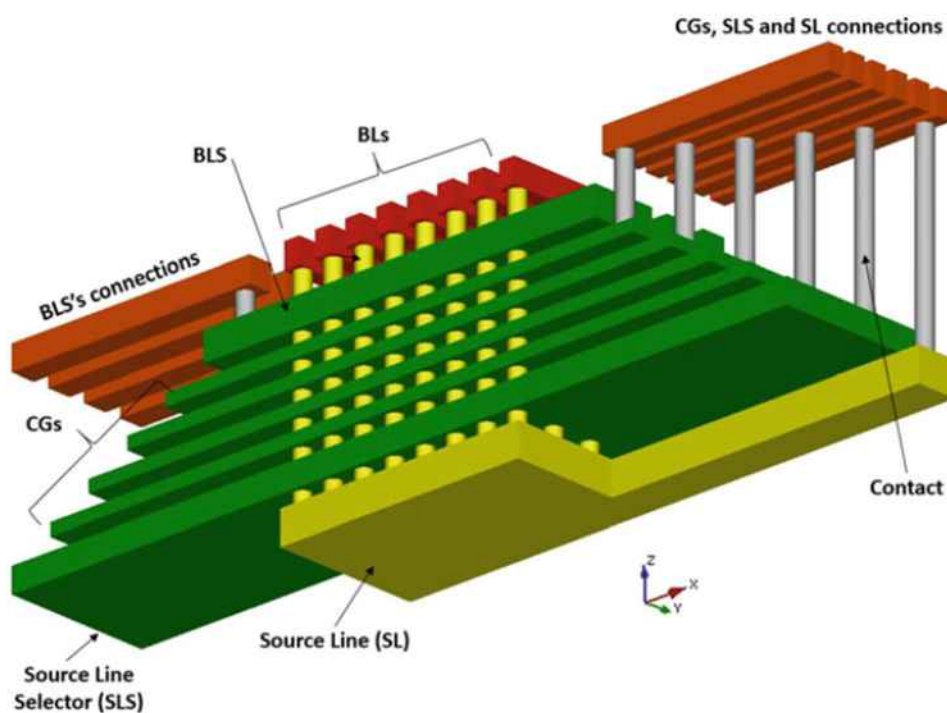


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

Ex. 1015, 109-110; Lee, ¶¶ 49-50. The memory cells' control gates form a staircase structure as shown below:

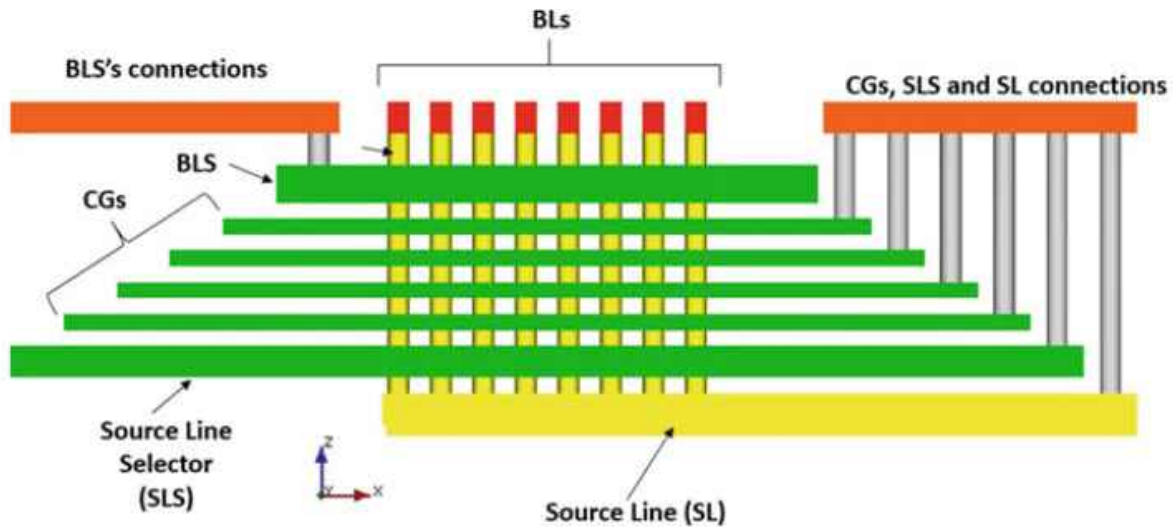


Fig. 4.12 Vertical cross section of BiCS with gate connections

Ex. 1015, 109 (green control gates forming a staircase). Each control gate delivers a control signal to a number of memory cells at the same horizontal level in the 3D NAND memory device. Lee, ¶¶ 50-51. The memory cells that a single control gate controls are together a “word,” and the control gate is a “word line.” Ex. 1016, 41. Reflecting this, the grey columns contacting the top surface of the control gates (shown above in green) are “word line contacts.” Lee, ¶ 51.

Various modifications to the BiCS structure were known, including the use of slit structures to serve as source line contacts for the NAND strings:

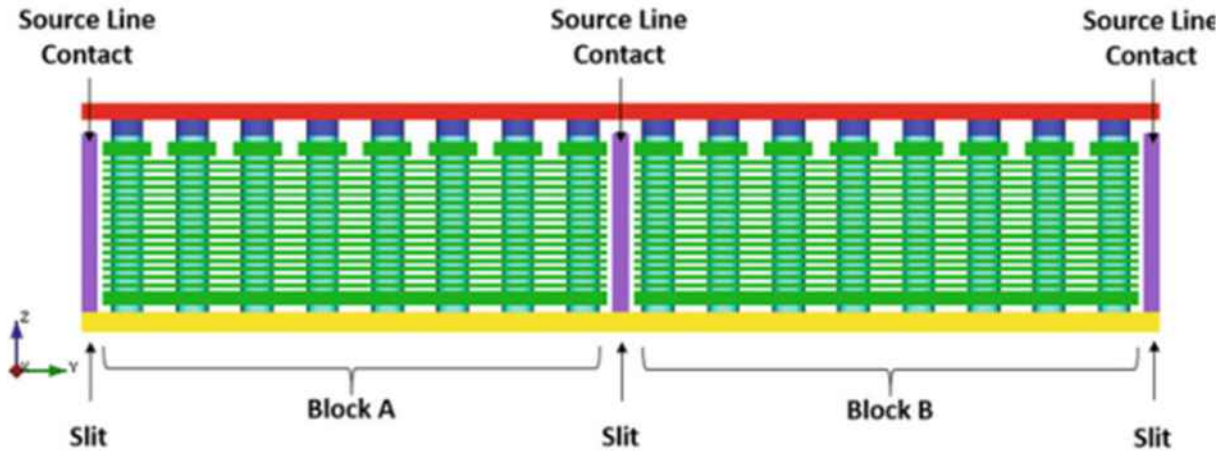


Fig. 6.8 Side view of Fig. 6.7

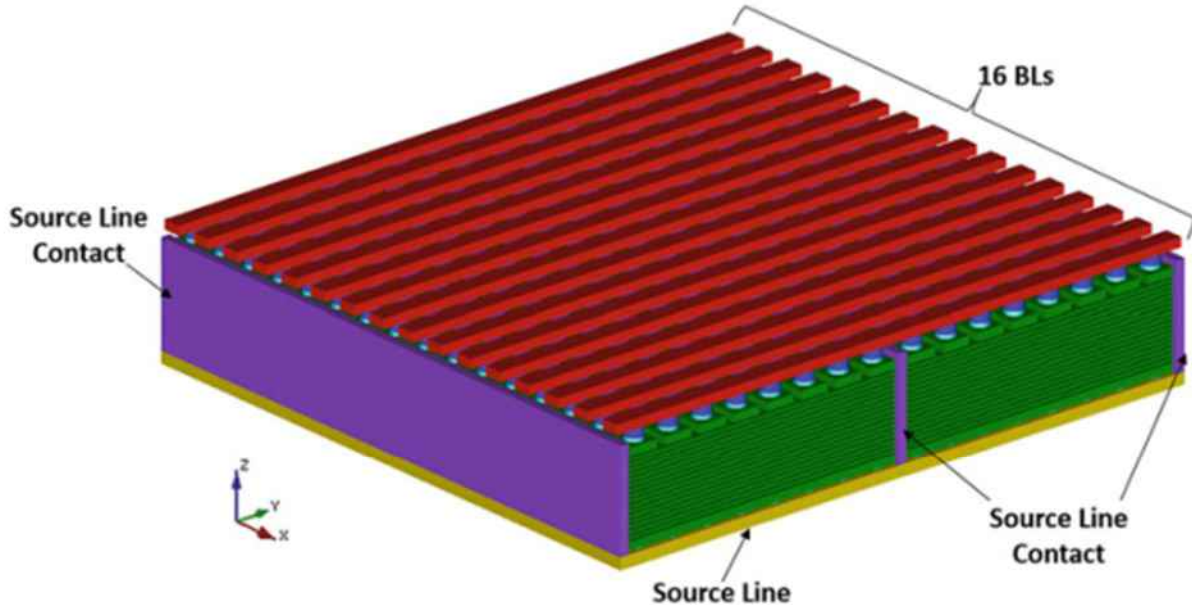


Fig. 6.7 Array slits

Ex. 1015, 185.

In each of the above figures, there are various gaps between the depicted structures. In a real 3D NAND memory device, these gaps are not merely empty space, but instead filled with an insulating material (also known as a “dielectric”).

Lee, ¶¶ 52-53. One purpose of the dielectric is to prevent electrical signals from one

conductive structure from interfering with the electrical signals in other structures.

Id., ¶ 53. Another purpose of the dielectric is as structural support to prevent the conductive structures from collapsing. *Id.*.

In sum, techniques for manufacturing 3D NAND memory devices were well-known in the art before the 378 Patent's priority date. Lee, ¶¶ 54-57.

B. The 378 Patent

The 378 Patent describes a "3D memory device 200" that, by and large, has a structure similar to the well-known and conventional BiCS architecture described above:

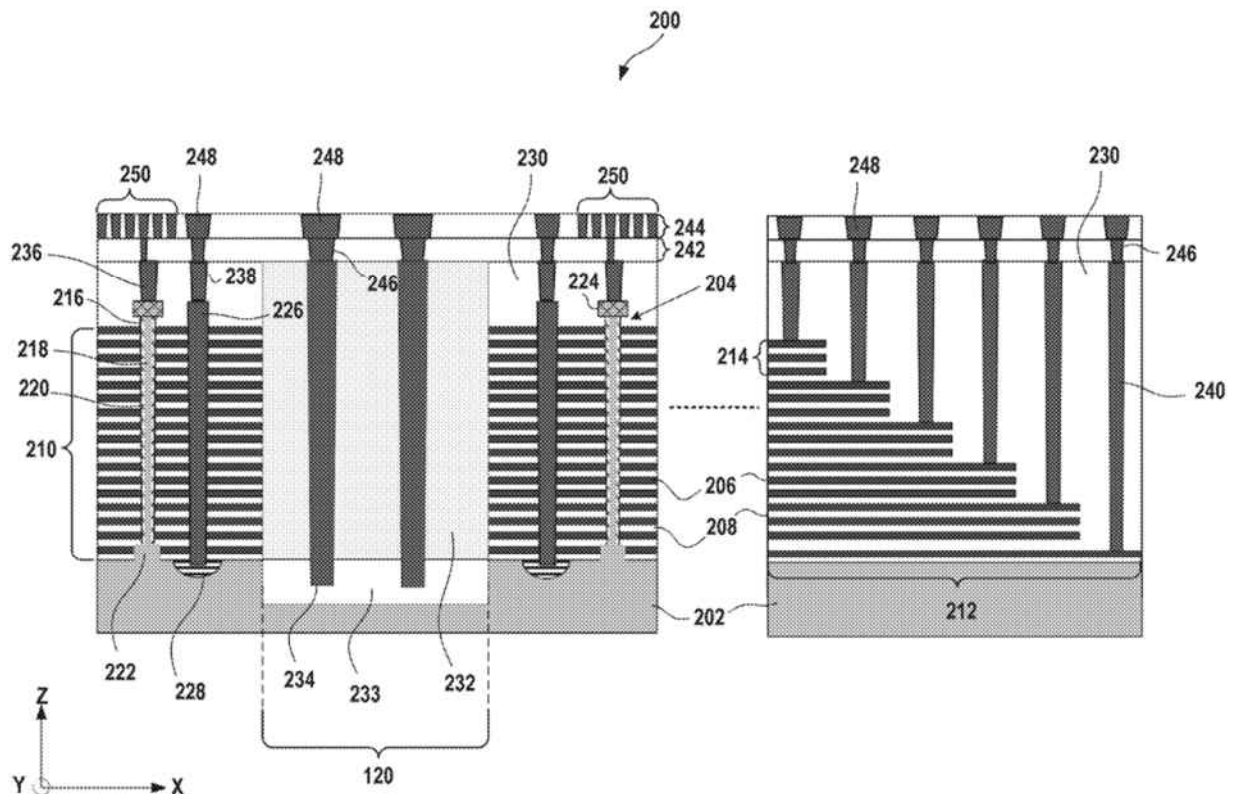


FIG. 2

Ex. 1001, Fig. 2.

As reflected in the 378 Patent's title, the alleged point of novelty is a 3D memory device with "vertical interconnects between [a] stacked array device" (e.g., "3D memory device 200") and "a peripheral device," "thereby reducing metal levels and shrinking die size." Ex. 1001, 5:32-59. The 378 Patent refers to these vertical interconnects as "through array contacts" ("TACs"). *Id.*, 1:51-55.

"In some embodiments, TACs 234 can provide electrical connections between 3D memory device 200 and the peripheral device (e.g., on a CMOS chip; not shown in FIG. 2)." Ex. 1001, 11:3-9. "Each TAC 234 can extend through the entire thickness of dielectric structure 232 and extend through at least a portion of STI structure 233 in a substrate 202." *Id.*, 10:67-11:2.

C. Prosecution History

During prosecution of the 378 Patent, the Examiner rejected the then-pending independent claims as obvious in view of U.S. Pat. No. 9,620,512 ("Nishikawa," Ex. 1017) and U.S. Pat. Pub. No. 2016/0056188 ("the 188 Publication," Ex. 1018). Ex. 1002, 530. However, the Examiner indicated dependent claim 17 was allowable over these references. *Id.*, 536. Claim 17 recited structures that, as explained in Section V.A, were well-known in the art: *a staircase structure, a word line contact, and a local contact disposed on each channel structure and slit structure*. *Id.*, 110. The Examiner only allowed the claim Petitioner now challenges, independent claim

15, after Patent Owner rewrote it to recite the limitations of then-claim 17. *Id.*, 110, 567.

The references this Petition relies on are not cumulative of those the Examiner discussed. During prosecution, the Examiner found Nishikawa did not disclose the claimed *through array contacts*, instead relying on the 188 Publication. But the 188 Publication does not even relate to memory, let alone a 3D NAND memory device. Ex. 1018, Abstract. Instead, the 188 Publication describes an image sensor. *Id.* By contrast, the primary references in this Petition (Toyama and Mushiga) both disclose or render obvious *all* claim elements, including the *through array contacts*. See Lee, ¶¶ 65-68.

VI. DESCRIPTION OF THE PRIOR ART

A. Toyama

Toyama has a filing date of September 19, 2016, a publication date of June 22, 2017, and claims a priority date of December 22, 2015. Toyama is prior art to the 378 Patent under 35 U.S.C. §§ 102(a)(1) and 102(a)(2).

Toyama's title is "Through-Memory-Level Via Structures For A Three-Dimensional Memory Device." Toyama discloses the conventional features of a 3D memory device claimed by the 378 Patent, including an alternating conductor/dielectric layer stack, memory channel structures extending through the alternating stack, word line contacts disposed on the staircase structure, a slit

structure, and local contacts. *E.g.*, Toyama, Figure 17A-F (showing these components). And, like the 378 Patent, Toyama discloses 3D NAND memory devices with the electrical connections (“through-memory-level via structures” in Toyama’s parlance) that extend through the memory array to provide a connection to “peripheral” devices. *Id.*, [0164] (discussing “peripheral device region 700” located underneath the “memory-level assembly”).

Toyama discloses four “exemplary structures,” each of which is an embodiment of Toyama’s invention. Each of Toyama’s exemplary structures incorporates the teachings of previously described exemplary structures. Toyama, [0261] (second exemplary structure), [0277] (third exemplary structure), [0310] (fourth exemplary structure). Toyama also discloses a number of “modifications” to its “exemplary structures,” which also incorporate the teachings of previously described embodiments. *Id.*, [0332] (second modification of fourth exemplary structure).

The Petition’s discussion of the Challenged Claims focuses on two of Toyama’s embodiments: (1) the “second modification of the fourth exemplary structure,” illustrated in Figures 44A-B to 49 (hereinafter, “Second Modification”); and (2) the “first exemplary structure,” illustrated in Figures 1A-B to 17A-F. As this Petition explains in further detail below, both of these embodiments independently discloses, or renders obvious, all limitations of claim 15.

B. Mushiga

Mushiga has a filing date of March 22, 2018, and was issued on July 16, 2019. Mushiga is prior art under at least 35 U.S.C. §102(a)(2).

Mushiga's title is "Three-Dimensional Memory Device Containing Bonded Chip Assembly with Through-Substrate Via Structures and Method of Making the Same." Mushiga discloses the conventional features of a 3D memory device claimed by the 378 Patent, including an alternating conductor/dielectric layer stack, memory channel structures extending through the alternating stack, word line contacts disposed on the staircase structure, a slit structure, and local contacts. Mushiga, Figure 11. And, like the 378 Patent, Mushiga discloses 3D NAND memory devices with the electrical connections ("through-substrate via structures" in Mushiga's parlance) that extend through the memory array to provide a connection to "peripheral" devices. *Id.*, 5:31-57.

C. Makala

Makala has a filing date of April 28, 2017, was issued on April 16, 2019, and claims a priority date of November 28, 2016. Makala is prior art under at least 35 U.S.C. § 102(a)(2).

Like the 378 Patent, Makala discloses a 3D memory device and discloses such a device's conventional elements, including an alternating conductor/dielectric layer stack, memory channel structures extending through the alternating stack, word line

contacts disposed on the staircase structure, a slit structure, and local contacts. Makala, Figure 16. This Petition relies on Makala primarily for its disclosure of *local contacts disposed on the slit structures* (“source connection via structures 91”), which the Petition uses to buttress Mushiga’s disclosure.

VII. CLAIM CONSTRUCTION

For purposes of this petition, Petitioner submits the terms of the 378 Patent’s claims do not require further construction and should receive their plain and ordinary meaning. Lee, ¶¶ 70-73.

VIII. LEVEL OF SKILL IN THE ART

A POSITA in the field of the ’378 patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). Lee ¶¶ 36-37. This POSITA would also have been aware of and generally knowledgeable about semiconductor manufacturing and 3D NAND’s structure, its component parts, how it operates, and how it is controlled. *Id.*

IX. GROUND 1: TOYAMA IN VIEW OF THE KNOWLEDGE OF A POSITA

A. Claim 15:

1. [15.PRE] “A three-dimensional (3D) memory device, comprising:”

To the extent the preamble is limiting, Toyama discloses *a three-dimensional (3D) memory device*. Indeed, the first sentence of Toyama’s detailed description states that “the present disclosure is directed to three-dimensional non-volatile memory devices, such as vertical NAND strings and other three-dimensional devices, and methods of making the same.” Toyama, [0156]; Lee ¶ 91.

2. [15.A] “a substrate with an isolation structure;”

a. [15.A.i] “a substrate”

Toyama discloses, or at least renders obvious, a *substrate*.

As an initial matter, the 378 Patent defines a “substrate” as “a material onto which subsequent material layers are added, or otherwise ‘disposed.’” Ex. 1001, 4:41-43. The 378 Patent further notes that “[a] substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow.” *Id.*, 5:4-6. Reflecting this, the 378 Patent embraces embodiments in which “the array device and a peripheral device are formed on different substrates.” *Id.*, 5:40-45.

Toyama’s “planar semiconductor material layer” 10 is a *substrate*.

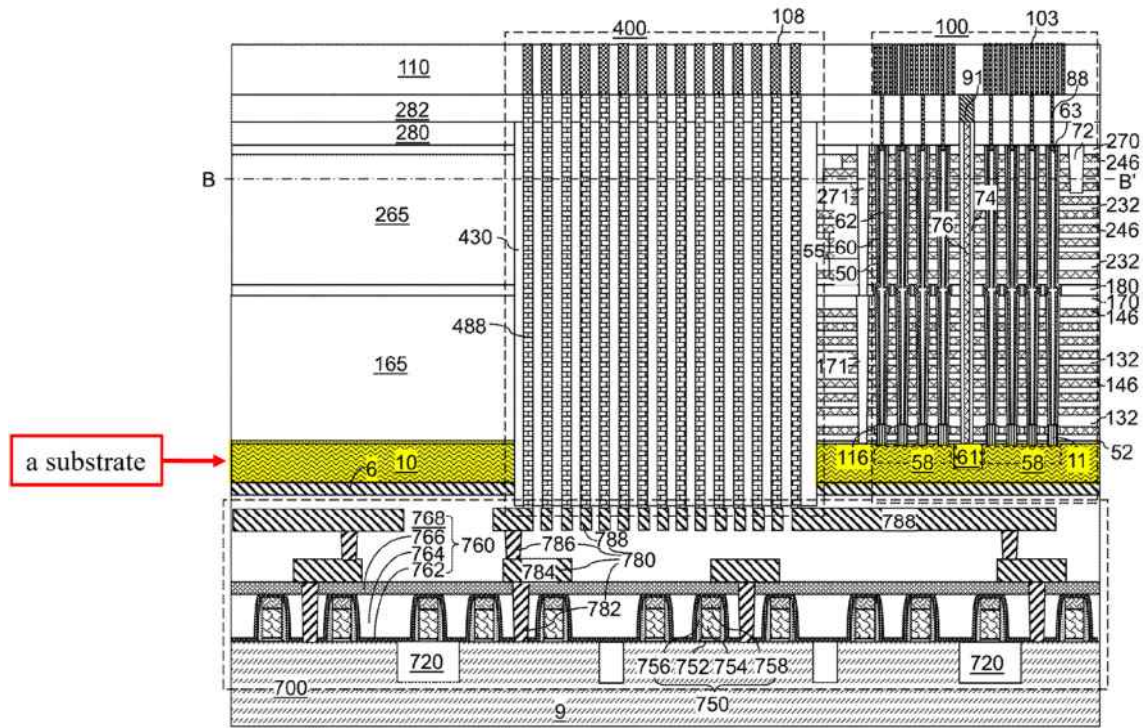


FIG. 17A

Toyama, Figure 17A. Figures 2 through 17A-E of Toyama illustrate how materials are disposed on “planar semiconductor material layer 10.” For example, Toyama notes that “[a]n alternating plurality of the first insulating layers 132 and first sacrificial material layers 142 [are] formed over the planar semiconductor material layer 10.” *Id.*, [0173]. And Toyama explains that “at least one retro-stepped dielectric material portion (165, 265) can be formed over the staircase regions on the at least one alternating stack (132, 142, 232, 242).” *Id.*, [0196]. Because Toyama’s “planar semiconductor material layer 10” is a material onto which subsequent material layers are added or otherwise disposed, it is *a substrate*.

Although the citations above are for Toyama’s “first exemplary structure,” Toyama’s fourth exemplary structure also include a “planar semiconductor material

layer 10,” and thus teach this limitation for the same reason. *See, e.g.,* Toyama, Figure 49 (Second Modification); Lee, ¶¶ 93-94.

b. [15.A.ii] “... with an isolation structure”

Both Toyama’s Second Modification and Toyama’s first exemplary structure teach this limitation.

i. Second Modification

Toyama’s description of its Second Modification starts after the alternating stack has already been formed. *See* Toyama, Figure 44A. Toyama explains that the alternating stack can be formed as described for any of the prior structures. Toyama states, for example, “[t]he second modification of the fourth exemplary structure can be formed concurrently with the formation of any of the first, second, and third exemplary structures or modifications thereof.” *Id.*, [0332]. Toyama further states the “alternating stack of insulating layers (132, 232) and dielectric spacer layers (which can be the sacrificial material layers (142, 242)) can be formed over the semiconductor substrate 9 as in previously described embodiments.” *Id.*

A POSITA would have understood Toyama’s Second Modification would use the process described in the context of the third exemplary structure for creating “opening 151” and filling it with an insulating material. Toyama, [0277] (“The optional planar conductive material layer 6 and the planar semiconductor material layer 10 may be patterned to form an opening 151 extending through these layers to

the underlying insulating layer 760. The opening 151 ... may be filled with another insulating material layer (e.g., a silicon oxide or doped silicate glass) 760.”); Lee, ¶¶ 99-100. A POSITA would therefore have understood that, in the context of Toyama’s Second Modification, the insulating material layer that fills “opening 151” is *an isolation structure*:

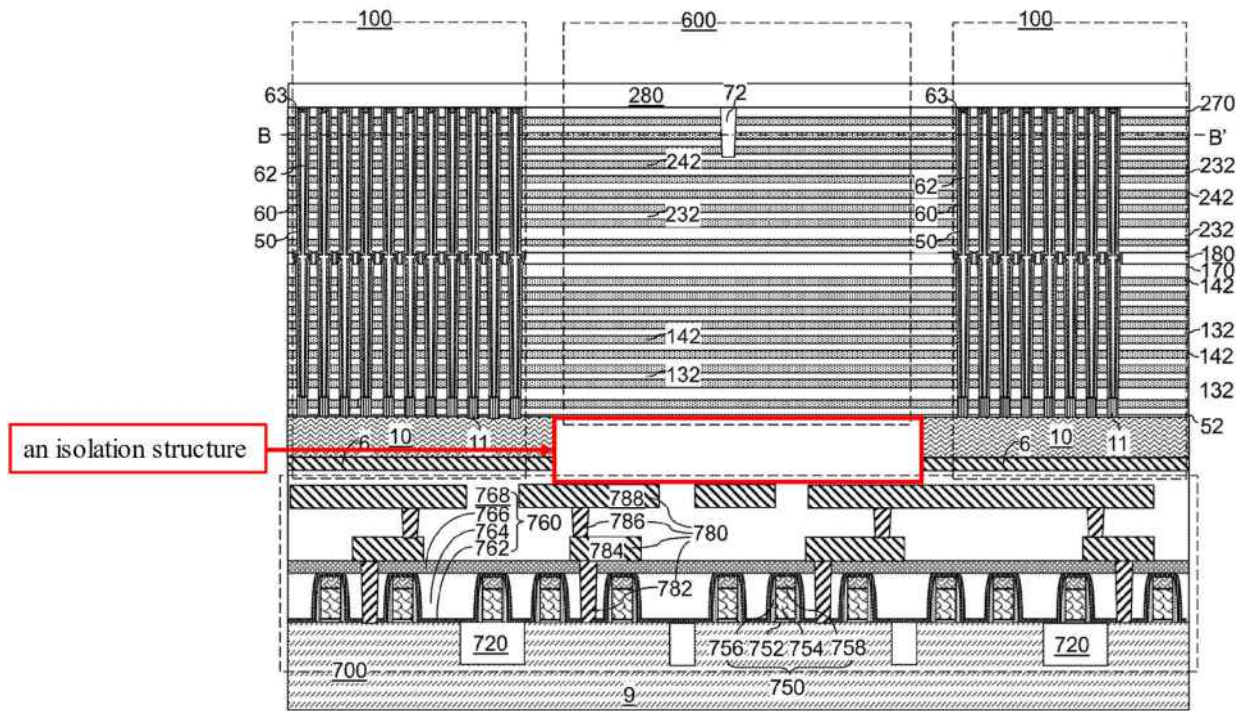


FIG. 44A

Toyama, Figure 44A. Thus, Toyama’s Second Modification teaches *a substrate* (“planar semiconductor material layer 10”) *with an isolation structure* (the insulating material layer that fills “opening 151”).

ii. First exemplary structure

In the context of Toyama’s first exemplary structure, the lower part of Toyama’s “dielectric fill material portion 430” is *an isolation structure*. Figures

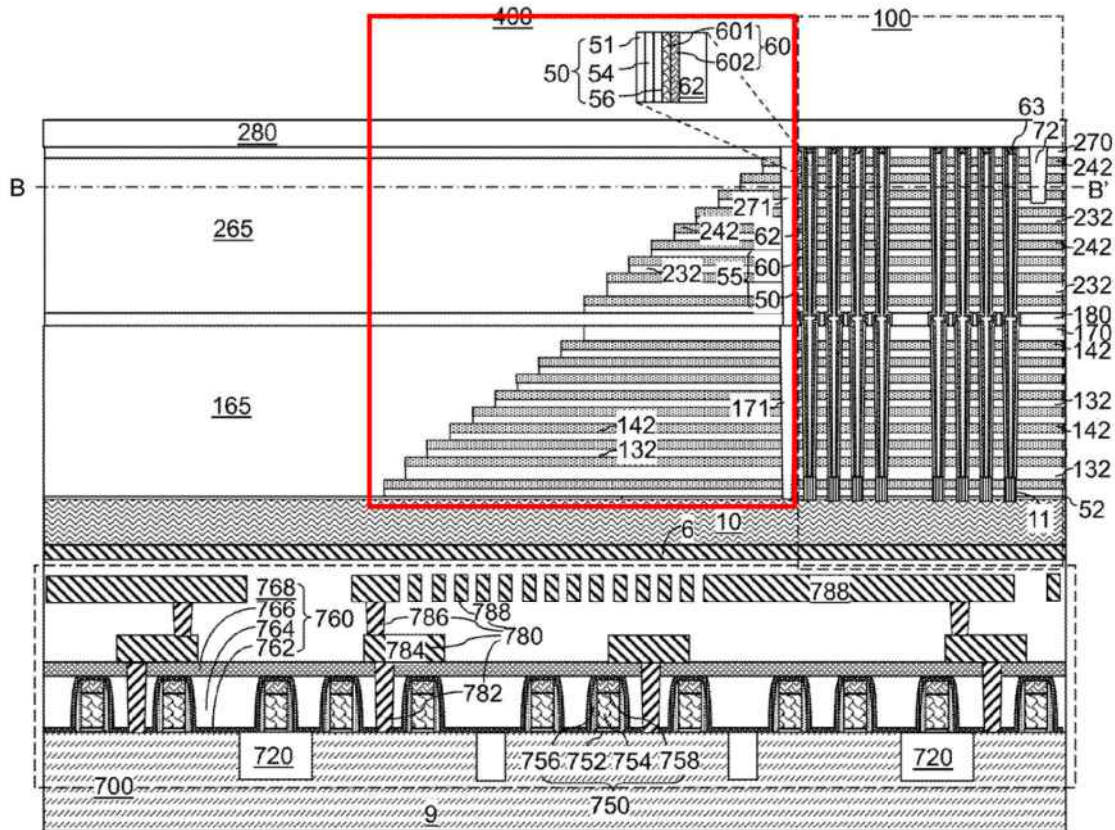
Petition for *Inter Partes* Review of U.S. Patent No. 10,658,378

FIG. 10A

Toyama, Figure 10A, [0192]-[0194]. The next step removes these layers, resulting in “through-memory-level opening 769”:

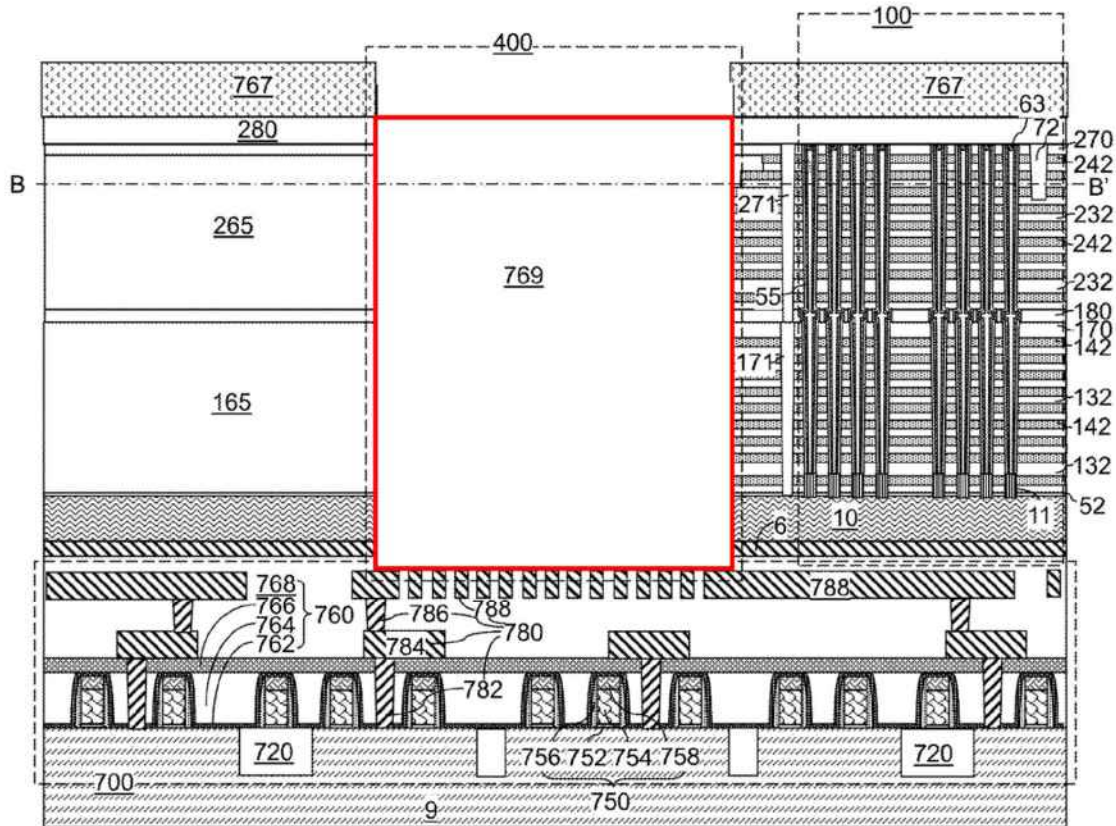


FIG. 11A

Id., Figure 11A; [0213]. The next step fills “opening 769” with a dielectric to form “dielectric fill material portion 430”:

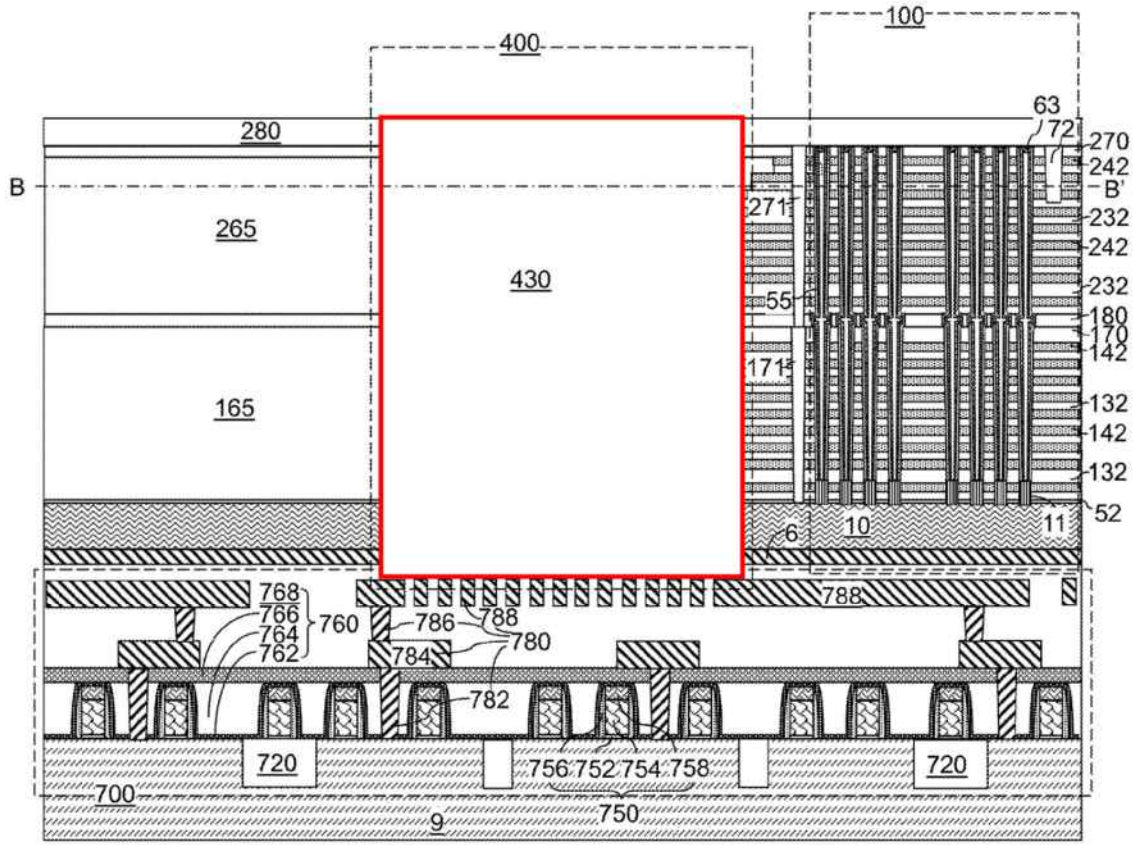


FIG. 12A

Id., Figure 12A; [0216]. The lower part of “dielectric fill material portion 430”—the portion level with and below the top of the “planar semiconductor material layer 10,” shown below—is *an isolation structure*:

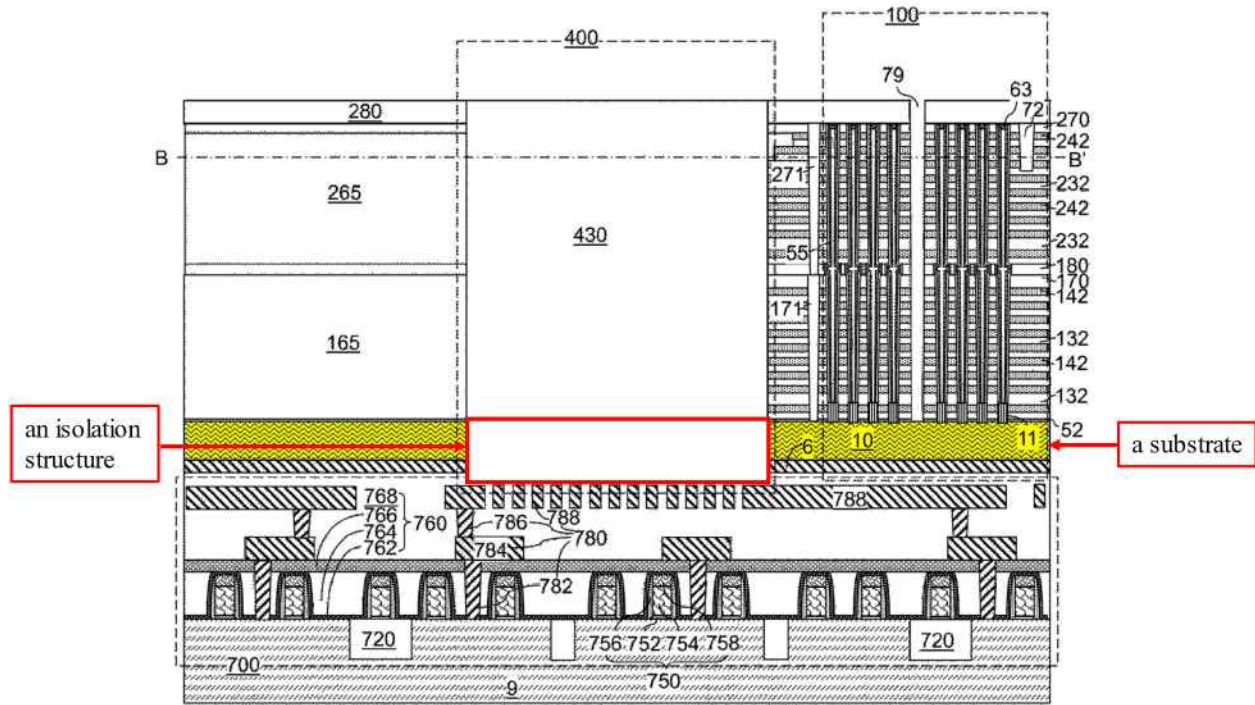


FIG. 13A

Id., Figure 13A. Toyama discloses that “dielectric fill material portion 430 includes a dielectric material such as undoped silicate glass (e.g., silicon oxide.)” *Id.*, [0216]. A POSITA would have understood that “dielectric fill material portion 430” is *an isolation structure* because it electrically isolates electrical conductors from each other and from electrical interference from the *substrate* (“planar semiconductor material layer 10”). Lee, ¶ 102.

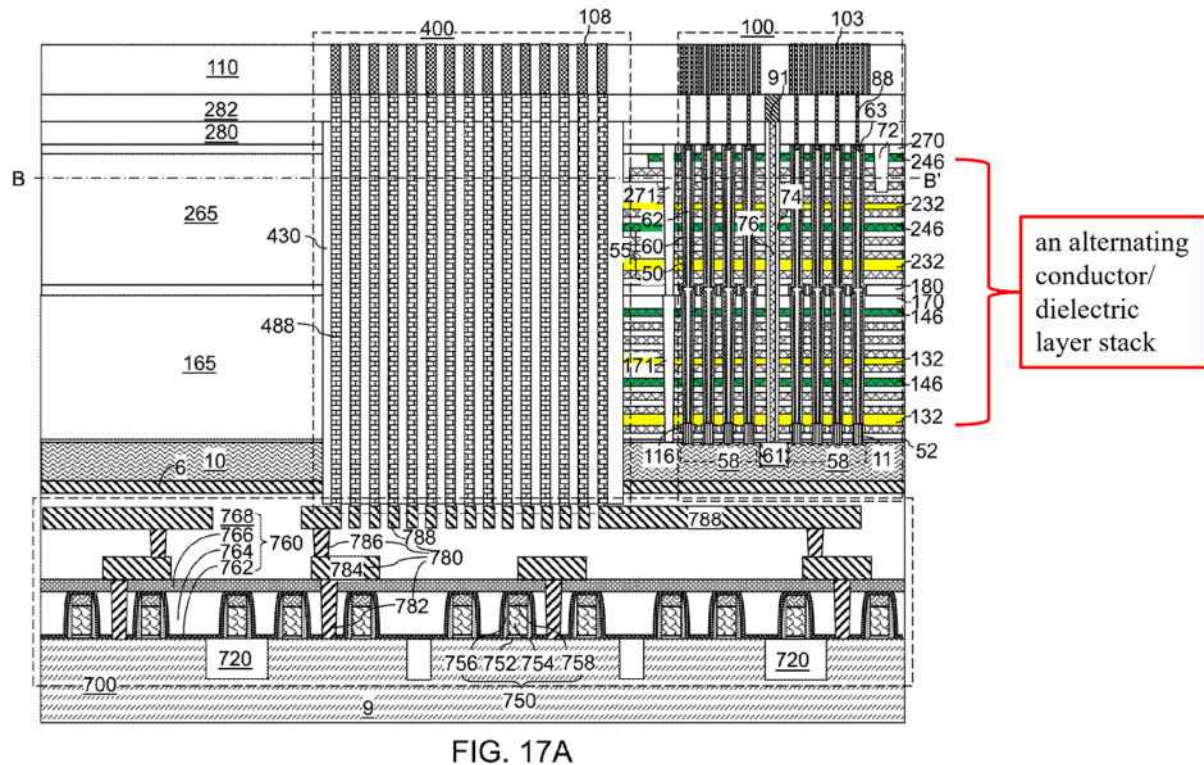
Toyama’s *substrate* (“planar semiconductor material layer 10”) is *with its isolation structure* (lower part of “dielectric fill material portion 430”). Indeed, Toyama’s *isolation structure* (lower part of “dielectric fill material portion 430”) *is formed by removing and is surrounded by substrate* (“planar semiconductor material layer 10”). Toyama, Figures 10A-12B (forming “opening 769” in “layer

10,” then filling the opening to form “portion 430”); Lee, ¶ 103. What’s more, the isolation structure is within the substrate and isolates portions of the substrate from one another. Lee, ¶ 103.

Toyama’s first exemplary structure thus discloses *a substrate* (“planar semiconductor material layer 10”) *with an isolation structure* (lower portion of “dielectric fill material portion 430”).

3. [15.B] “an alternating conductor/dielectric layer stack disposed on the substrate;”

Toyama’s “alternating stack (132, 146, 232, 246)” (shown below) is *an alternating conductor/dielectric layer stack disposed on the substrate*:



Toyama, Figure 17A; Lee, ¶ 106. Toyama explains its “alternating stack” comprises “first and second conductive material layers (146, 246),” (representative layers of which Petitioner highlights in green above) “first insulating layers 132,” and “second insulating layers 232” (representative layers of which Petitioner highlights in yellow above). Toyama, [0172], [0190], [0228], [0232].

Toyama’s “alternating stack” is *disposed on the semiconductor substrate*. Lee, ¶ 107. As an initial matter, the 378 Patent instructs that the term “on” “should be interpreted in the broadest manner such that ‘on’ not only means ‘directly on’ something but also includes the meaning of ‘on’ something with an intermediate feature or a layer therebetween.” Ex. 1001, 4:20-25. As noted for limitation [15.A],

above, Toyama's "planar semiconductor material layer 10" is a *semiconductor substrate*. Toyama, [0170]-[0171]. As shown in Figure 17A, above, Toyama's alternating stack is *disposed on* (above) "planar semiconductor material layer 10."

Although the citations above are for Toyama's "first exemplary structure," Toyama's Second Modification also teaches this limitation for the same reasons. *See, e.g.*, Toyama, Figure 49 (Second Modification), [0337] ("An alternating stack (132, 146, 232, 246) of insulating layers ([1]32, 232) and electrically conductive layers (146, 246) is thus formed."); Lee, ¶ 108.

4. **[15.C] "a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;"**

Toyama's Second Modification and Toyama's first exemplary structure teach this limitation.

a. Second Modification

i. [15.C.i] “a dielectric structure on the isolation structure”

In Toyama’s Second Modification, shown below,⁵ “insulating liners 674” are *a dielectric structure*:

⁵ In a clear typographical error, Figure 49 labels its alternating conductor/dielectric layer stack as elements 132, 142, 232, 242. Elements 142, 242 are “sacrificial material layers” which, in a process step prior to Figure 49, were removed and replaced with “electrically conductive layers (146, 246).” Toyama, [0337], [0340]. That is also reflected in the figures, which depict how the sacrificial material layers (shaded in gray, as in Figure 45A) are replaced by electrically conductive layers (cross-hatched, as in Figure 46A).

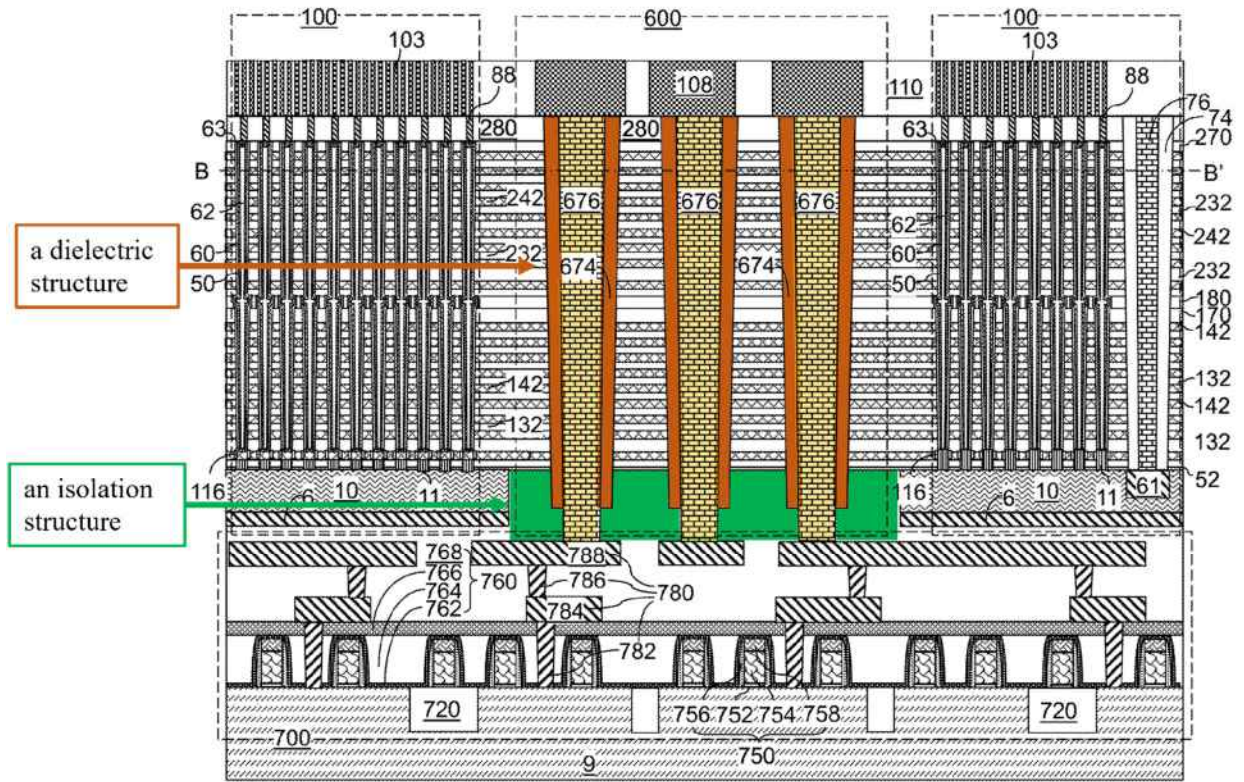


FIG. 49

Toyama, Figure 49.

As an initial matter, “insulating liners 674” are *dielectric*. Toyama forms “insulating liners 674” by depositing “a conformal insulating material layer” in “through-memory-level openings 679.”⁶ Toyama, [0338]-[0340]. Insulating liner 674 may be a “dielectric material.” *Id.*, [0233] (“[a]n insulating spacer 74 including

⁶ Although paragraph 338 of Toyama refers to “through-memory-level openings 689,” that appears to be a typographical error. All of the relevant figures (*e.g.*, Figures 47A-B to 49) and the other textual description refer to the elements as “through-memory-level openings 679.”

a dielectric material”), [0381] (“insulating liner 674 having a same material composition and a same thickness as the insulating spacer 74”); Lee, ¶ 111. The claims do not require a “single-material” dielectric structure. Ex. 1001, 5:50-59 (contemplating a “single-material” dielectric structure only “[i]n some embodiments”). Regardless, Toyama contemplates that “insulating liners 674” are made of a single material (e.g., silicon oxide). Section IX.D.1 (claim 19).

What’s more, the “insulating liners 674” are collectively a *structure*. As explained above, they are constructed together. Ex. 1022, 5 (Merriam-Webster’s definition of “structure” as “something (such as a building) that is constructed”). And all of the “liners 674” have the same function of insulating and electrically isolating the *through array contacts* (“through-memory-level via structures 676”) as they pass through the *alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246).”⁷

⁷ If Patent Owner argues “insulating liners 674” are multiple structures and not collectively a single structure, that would be incorrect for the reasons above. And, in any event, it would be irrelevant. The Federal Circuit has “repeatedly emphasized that an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more’ in open-ended claims containing the transitional phrase ‘comprising.’” *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000).

A POSITA would thus have understood “insulating liners 674” are individually and collectively *a dielectric structure*. Lee, ¶¶ 110-114.

As explained above with reference to limitation [15.A], Toyama’s Second Modification contemplates forming *the isolation structure* (the insulating material layer filling “opening 151”) using the process described for the third exemplary structure. Section **Error! Reference source not found.**, above.

Toyama further teaches the *dielectric structure* (“insulating liners 674”) is *on* the *isolation structure* (the insulating material layer filling “opening 151”) because “insulating liners 674” are on the isolation structure. Ex. 1001, 4:20-29 (defining “on”).

ii. [15.C.ii] “a dielectric structure ... extending vertically through the alternating conductor/dielectric layer stack”

As noted immediately above, Toyama’s “insulating liners 674” are individually and collectively *a dielectric structure*. And, as noted above with reference to limitation [15.B], Toyama’s “alternating stack (132, 146, 232, 246)” is *the alternating conductor/dielectric layer stack*. Section IX.A.3. Thus, as shown in the figure below, Toyama discloses *a dielectric structure* (“insulating liners 674”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack 132, 146, 232, 246”):

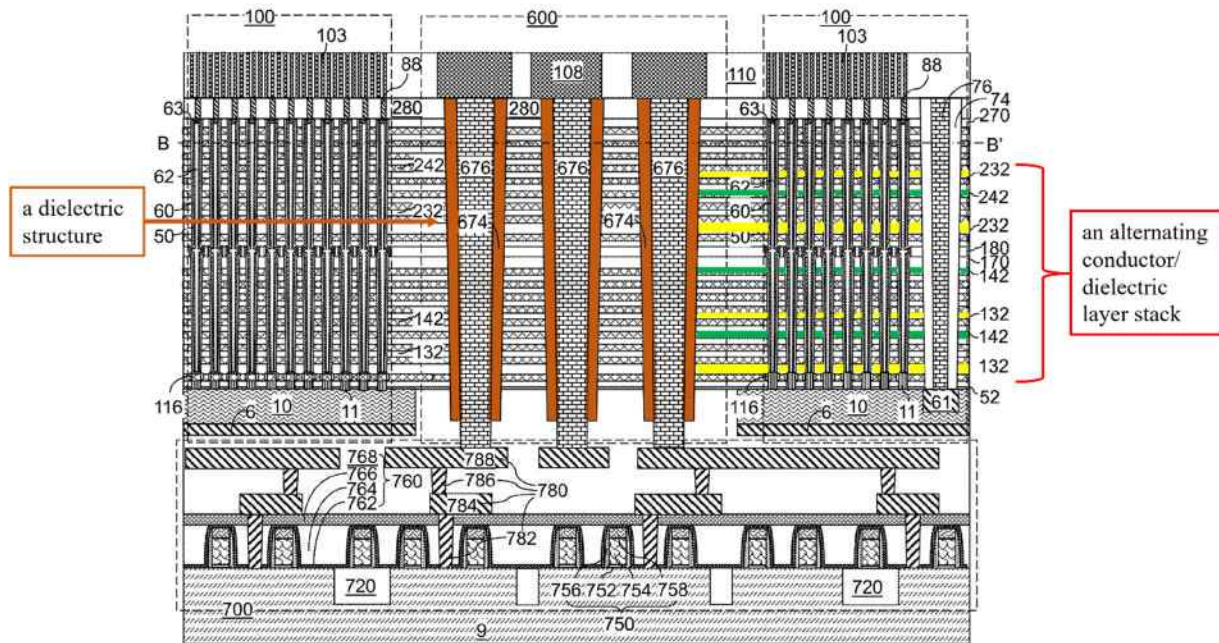


FIG. 49

Toyama, Figure 49;⁸ Lee, ¶ 115.

- iii. [15.C.iii] “a dielectric structure ... wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure”

As illustrated below, Toyama discloses *a dielectric structure* (“insulating liners 674”) *wherein the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”) *abuts a sidewall surface of the dielectric structure* (a sidewall surface of “insulating liner 674”):

⁸ As noted in footnote 5, above, labels 142 and 242 are properly understood to refer to “conductive material layers (146, 246).”

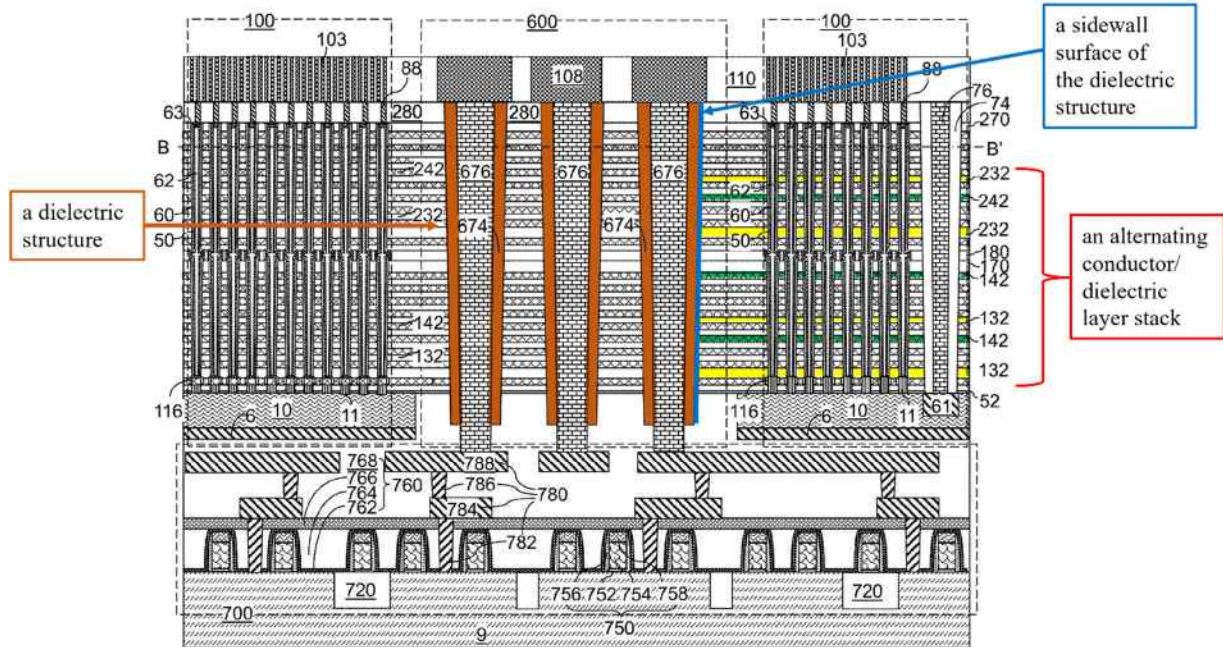


FIG. 49

Toyama, Figure 49;⁹ Lee, ¶ 116.

iv. [15.C.iv] “... wherein ... the dielectric structure is formed of a dielectric material”

As noted above, Toyama’s “insulating liners 674” are individually and collectively *a dielectric structure*. As noted above for limitation [15.C.i], each of these elements comprises a dielectric material. Section IX.A.4.a.i. Toyama thus discloses *a dielectric structure* (“insulating liners 674”) *wherein the dielectric structure is formed of a dielectric material*. Lee, ¶ 117.

⁹ As noted in footnote 5, above, labels 142 and 242 are properly understood to refer to “conductive material layers (146, 246).”

b. First exemplary structure

i. [15.C.i] “a dielectric structure on the isolation structure”

In Toyama’s first exemplary structure, shown below, the upper part of “dielectric fill material portion 430” is a *dielectric structure*:

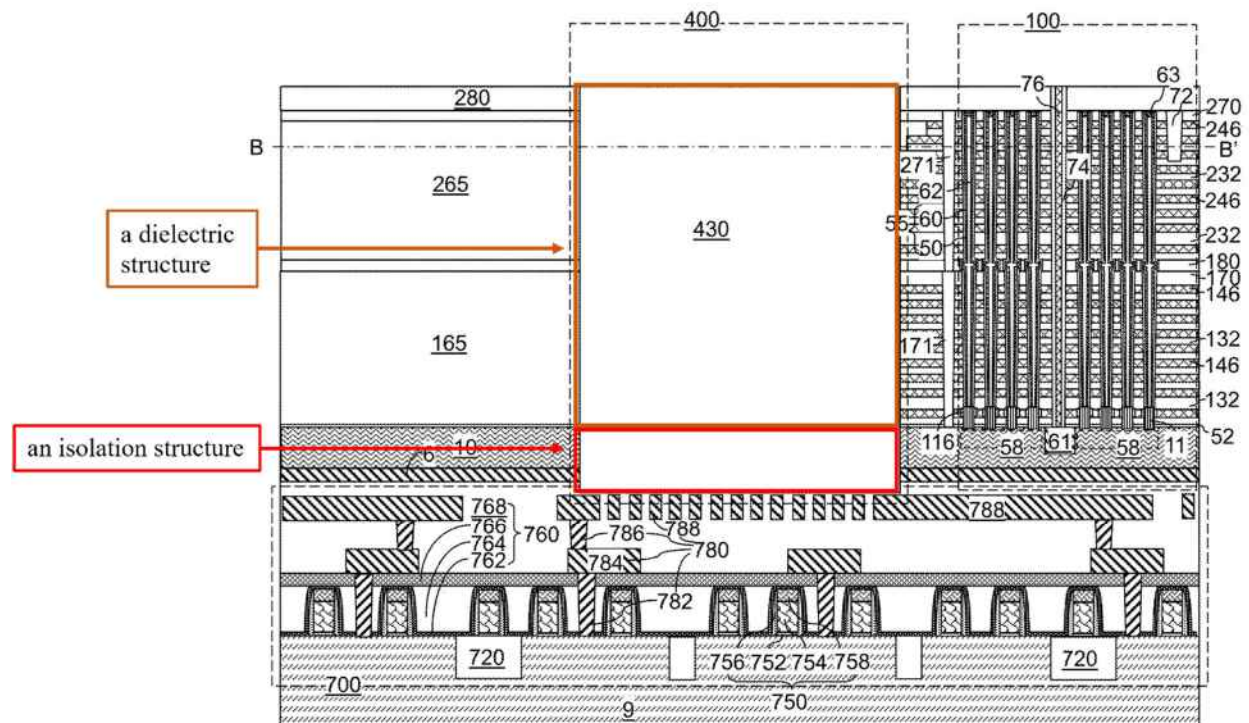


FIG. 15A

Toyama, Figure 15A. Toyama explains that “a dielectric fill material portion 430 is formed within each through-memory-level opening 769, for example, by deposition of a dielectric fill material.” *Id.*, [0216]. The upper part of “dielectric fill material portion 430” is a *dielectric structure* because it is composed of “a dielectric fill material.” *Id.*; Lee, ¶ 118.

As explained above with reference to claim limitation [15.A], in the context of Toyama's first exemplary structure, *the isolation structure* is the portion of "dielectric fill material portion 430" at and below the top surface of semiconductor substrate 10. *See* Section IX.A.2.b.ii, *above*. The portion of dielectric fill material 430 above the upper surface of substrate 10 is *a dielectric structure*. Toyama thus discloses the first exemplary structure's *dielectric structure* (upper part of "dielectric fill material portion 430") is *on the isolation structure* (lower portion of "dielectric fill material portion 430").

If Patent Owner were to contend the claim excludes forming the *isolation structure* and the *dielectric structure* during the same process step, that would be incorrect. Nothing in the language of the claim requires forming the structures in different steps or of different materials, nor is there a clear disavowal of such in the specification. On the contrary, the 378 Patent's disclosure expressly broadens "isolation structure" beyond the disclosed embodiment. Ex. 1001, 10:34-35 ("STI structure 233 is exemplary and not limiting. As such, other isolation structures can be used."). The purpose of the 378 Patent's "dielectric structure" is to electrically insulate a "through array contact" as it extends through the "alternating conductor/dielectric layer stack." *Id.*, 11:12-14; Lee, ¶ 120. The purpose of the 378 Patent's "isolation structure" is to electrically insulate a "through array contact" as

it extends through the “substrate.” The upper and lower portions, respectively, of Toyama’s “dielectric fill material portion 430” equally serve these purposes. *Id.*

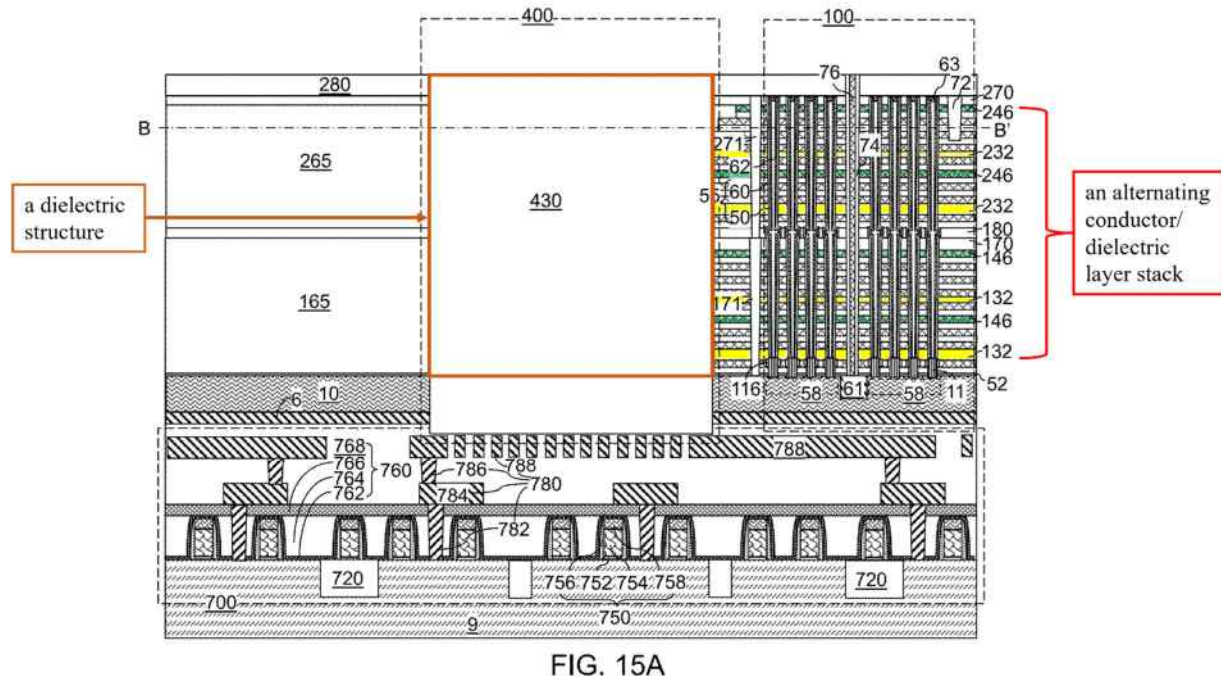
This case is analogous to *Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1303 (Fed. Cir. 2011), in which the Court held different parts of the same structure can meet distinct claim elements. As in *Retractable*, the intrinsic record here “lacks the clarity required to exclude from the scope of the claims [an isolation structure] and [a dielectric structure] that form distinct portions of a single structure.” *Id.* at 1304. And here, as in *Retractable*, each distinct part of the unitary structure (here, the upper and lower parts of “dielectric fill material portion 430”) fulfills the structural and functional requirements of the respective claim element (here, *dielectric* and *isolation structures*, respectively).

Even if the claims require forming *the isolation structure* separately from *the dielectric structure*, the first exemplary structure’s disclosure nevertheless renders the claims obvious. The use of isolation structures on a substrate to electrically isolate components was well known and commonplace by the priority date. Lee, ¶ 121. What’s more, Toyama itself contemplates forming the *isolation structure* and *dielectric structure* separately. Indeed, Toyama’s third exemplary structure teaches how to do so. Section **Error! Reference source not found.** In the context of Toyama’s first exemplary structure, forming the *isolation structure* and the *dielectric structure* separately would be no more than the mere substitution of a

known process (forming an isolation structure in “opening 151” before forming the dielectric structure, as in Toyama’s third exemplary structure) for another process (forming the isolation and dielectric structures at the same time, as in Toyama’s first exemplary structure) to obtain predictable results (the insulating material layer filling “opening 151” electrically isolates the conductors embedded within). Lee, ¶ 121; *Agrizap, Inc. v. Woodstream Corp.*, 520 F.3d 1337 (Fed. Cir. 2008).

ii. [15.C.ii] “a dielectric structure ... extending vertically through the alternating conductor/dielectric layer stack”

As noted immediately above, the upper part of Toyama’s “dielectric fill material portion 430” is *a dielectric structure*. And, as noted above with reference to limitation [15.B], Toyama’s “alternating stack (132, 146, 232, 246)” is *the alternating conductor/dielectric layer stack*. Section IX.A.3. Thus, as shown in the figure below, Toyama discloses *a dielectric structure* (upper part of “dielectric fill material portion 430”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack 132, 146, 232, 246”):



Toyama, Figure 15A; Lee, ¶¶ 122-123.

Indeed, Toyama's first exemplary structure discloses this limitation in materially the same way as one of the 378 Patent's embodiments. The 378 Patent discloses an embodiment in which the dielectric structure 124 borders three regions that include an alternating conductor/dielectric layer stack: above and below by staircase (i.e., word line) regions 140, and to the right-hand side by a NAND string region 110:

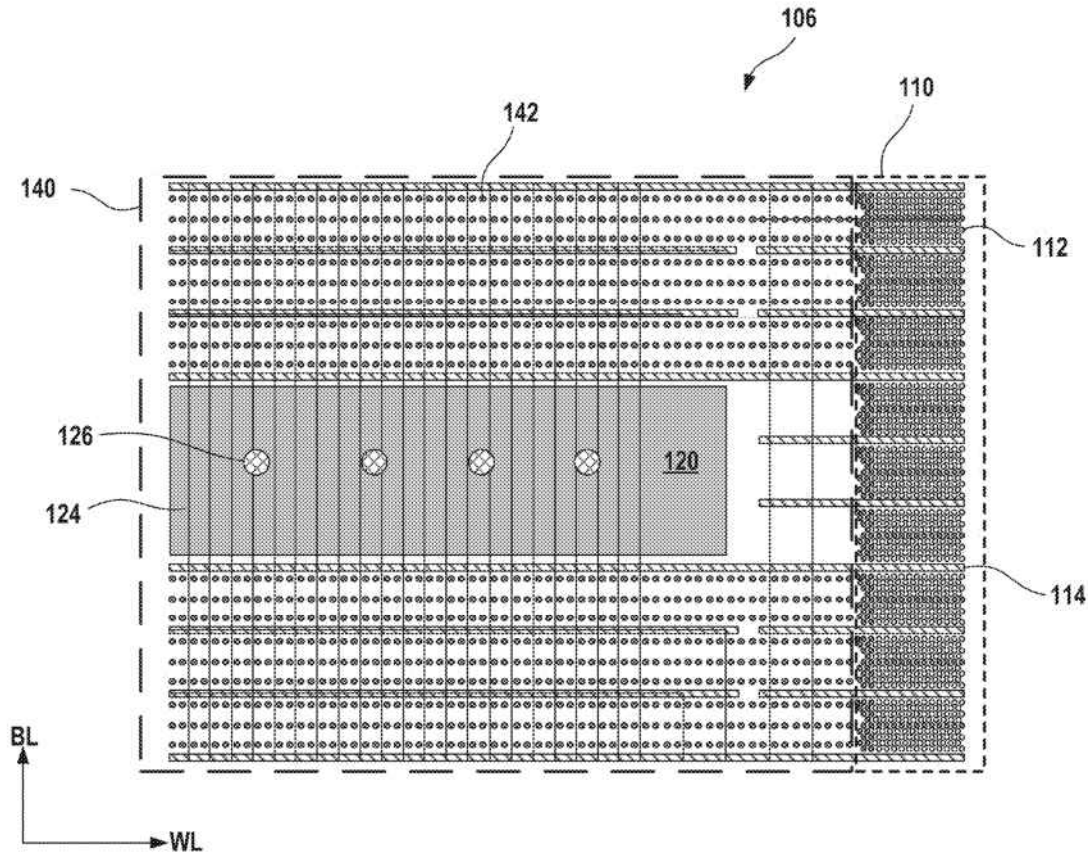


FIG. 1C

Ex. 1001, Figure 1C. Similarly, in Toyama’s first exemplary structure, the *dielectric structure* (“dielectric fill material portion 430”) borders three regions including an alternating conductor/dielectric layer stack: above and below by staircase regions (“word line contact via region 200”) and to the right-hand side by a NAND string region (“memory array region 100”):

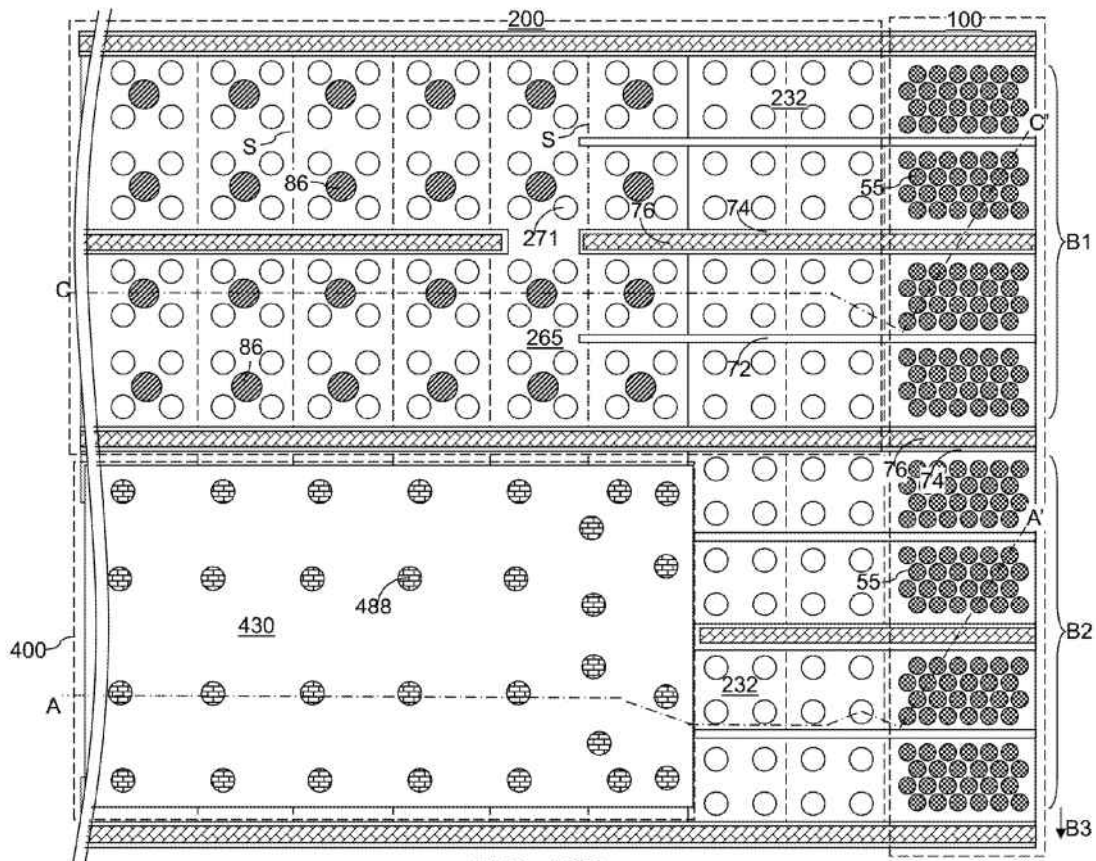


FIG. 16B

Toyama, Figure 16B; Lee, ¶ 124.

What's more, Toyama and the 378 Patent form the *dielectric structure* ("dielectric fill material portion 430" and "dielectric layer 702," respectively) in the same way. Toyama forms "dielectric fill material portion 430" like the 378 Patent forms "dielectric layer 702," by removing part of the dielectric stack before replacing the dielectric stack's sacrificial layers with electrically conductive layers. Specifically, the 378 Patent removes part of "dielectric stack 400" to form "opening 600":

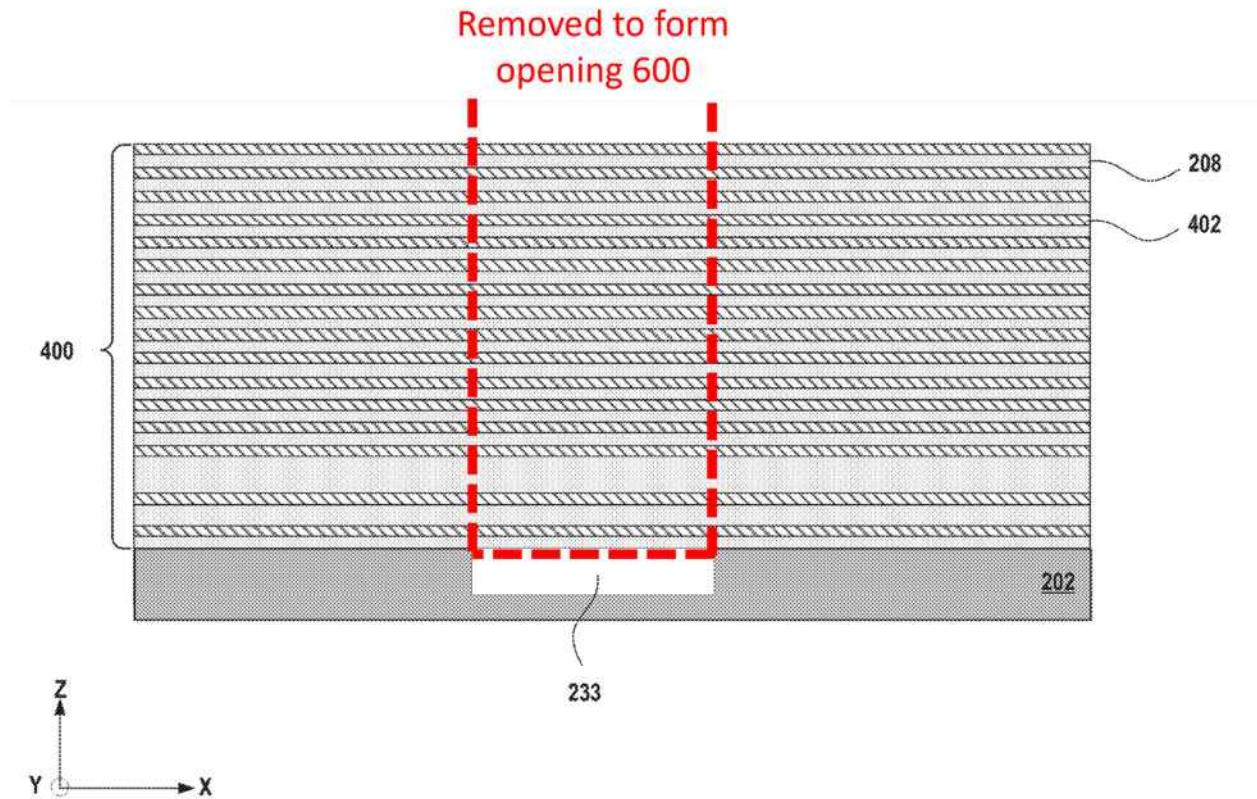


FIG. 4

Ex. 1001, Figure 4, 15:12-14. The 378 Patent then fills “opening 600” with the dielectric structure (“dielectric layer 702”). *Id.*, 15:42-44.

Similarly, Toyama’s first exemplary structure removes “insulating layers” 132, 232 and “sacrificial material layers” 142, 242 to form “opening 769”:

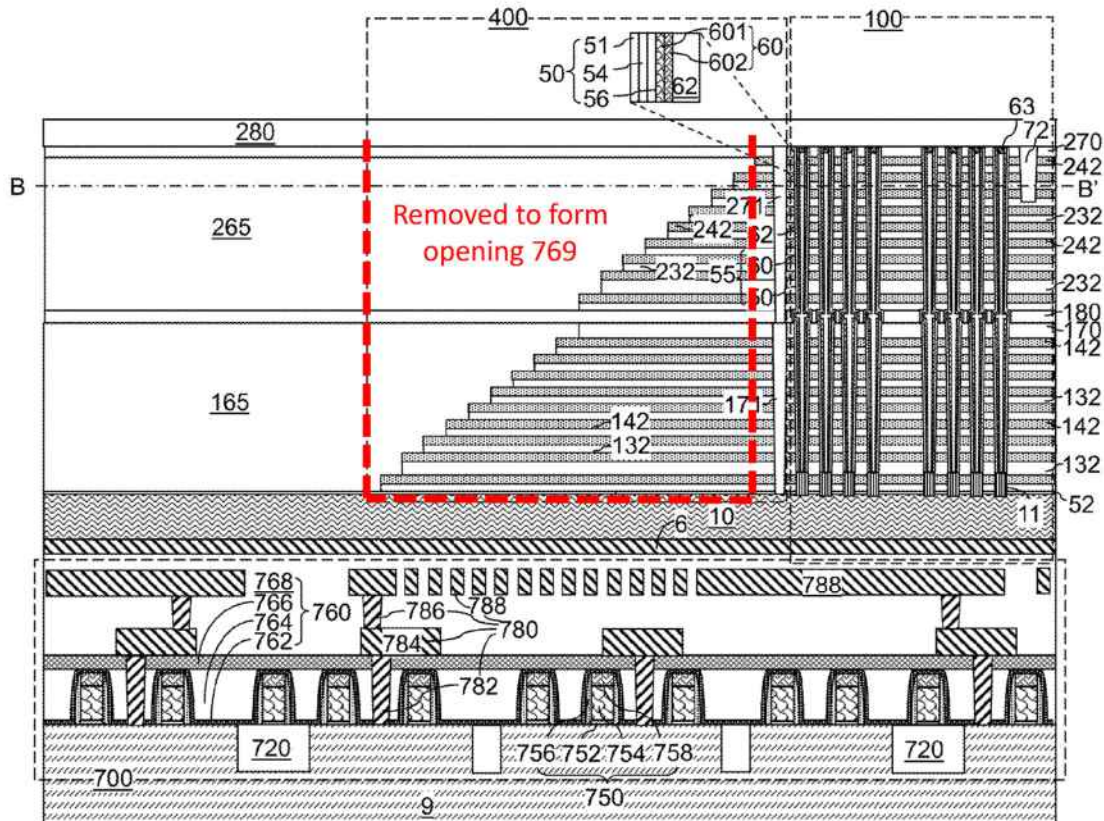


FIG. 10A

Toyama, Figure 10A, [0173], [0189]. Toyama then fills “opening 769” with the dielectric structure (“dielectric fill material portion 430”).

Toyama’s first exemplary structure thus discloses this limitation. Lee, ¶¶ 122-126.

- iii. [15.C.iii] “A dielectric structure ... wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure”

As illustrated below, Toyama discloses *a dielectric structure* (upper part of “dielectric fill material portion 430”) *wherein the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”) *abuts* (touches) *a sidewall*

surface of the dielectric structure (sidewall of upper part of “dielectric fill material portion 430”):

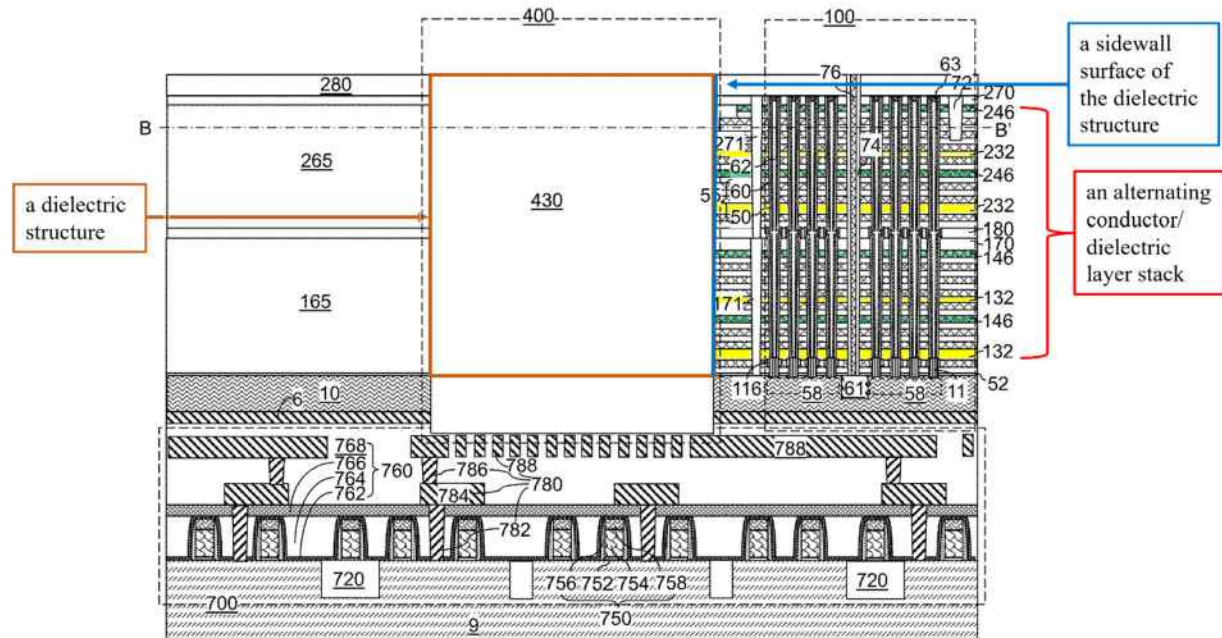


FIG. 15A

Toyama, Figure 15A; Lee, ¶ 127.

iv. [15.C.iv] “... wherein ... the dielectric structure is formed of a dielectric material”

As noted above, the upper part of Toyama’s “dielectric fill material portion 430” is *a dielectric structure*. Toyama discloses “dielectric fill material portion 430 is formed ... for example, by deposition of a dielectric fill material.” Toyama, [0216]. Toyama thus discloses *a dielectric structure* (upper part of “dielectric fill material portion 430”) *wherein the dielectric structure is formed of a dielectric material* (the “dielectric fill material” that forms “dielectric fill material portion 430”). Lee, ¶ 128].

55 vertically extending through the at least one alternating stack (132, 146, 232, 246).” Toyama, [0232].

Although the claim language does not impose any additional functional or structural requirements for the *channel structures*, Toyama’s “memory stack structures 55” perform the same function and are composed of the same components as the 378 Patent’s channel structures. Like the 378 Patent’s channel structures, Toyama’s “memory stack structures 55” serve as the device’s memory elements. Ex. 1001, 14:4-31 (“channel structure” includes a “memory film”); Toyama, [0388] (“The memory stack structures 55 can comprise memory elements of a vertical NAND device.”); Lee, ¶ 131. The 378 Patent’s “channel structures” and Toyama’s memory stack structures 55” are also composed of the same components. Ex. 1001, 9:1-6 (“[c]hannel structure 216 is filled with semiconductor materials (e.g., as a semiconductor channel 218) and dielectric materials (e.g., as a memory film 220)”); Toyama, [0210] (“[e]ach of the memory stack structures 55 comprises a memory film 50 and a vertical semiconductor channel 60”).

Although the citations above are for Toyama’s “first exemplary structure,” Toyama’s Second Modification also teaches this limitation for the same reason. *See, e.g.,* Toyama, Figure 49 (showing “memory stack structures 55”); Lee, ¶ 132.

b. “slit structures extending vertically through the alternating conductor/dielectric layer stack”

As shown below, Toyama teaches *slit structures* (“laterally-elongated contact via structures 76”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”):

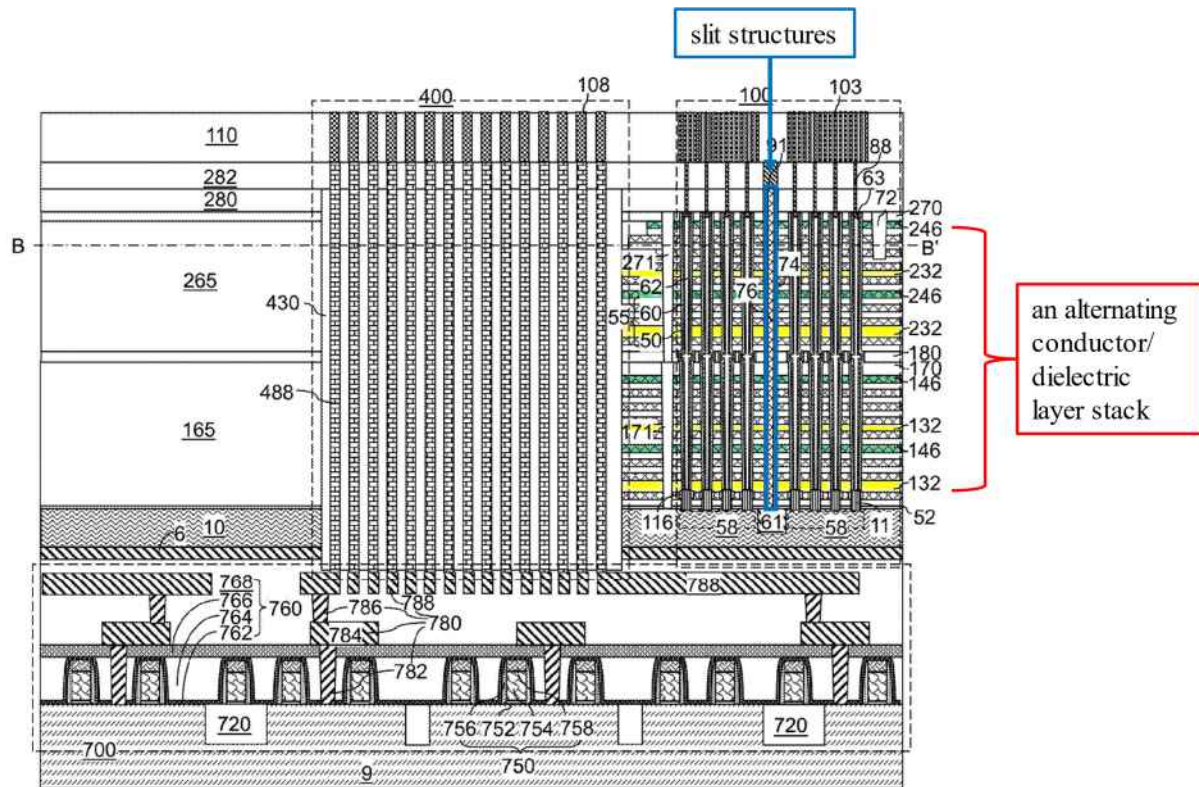
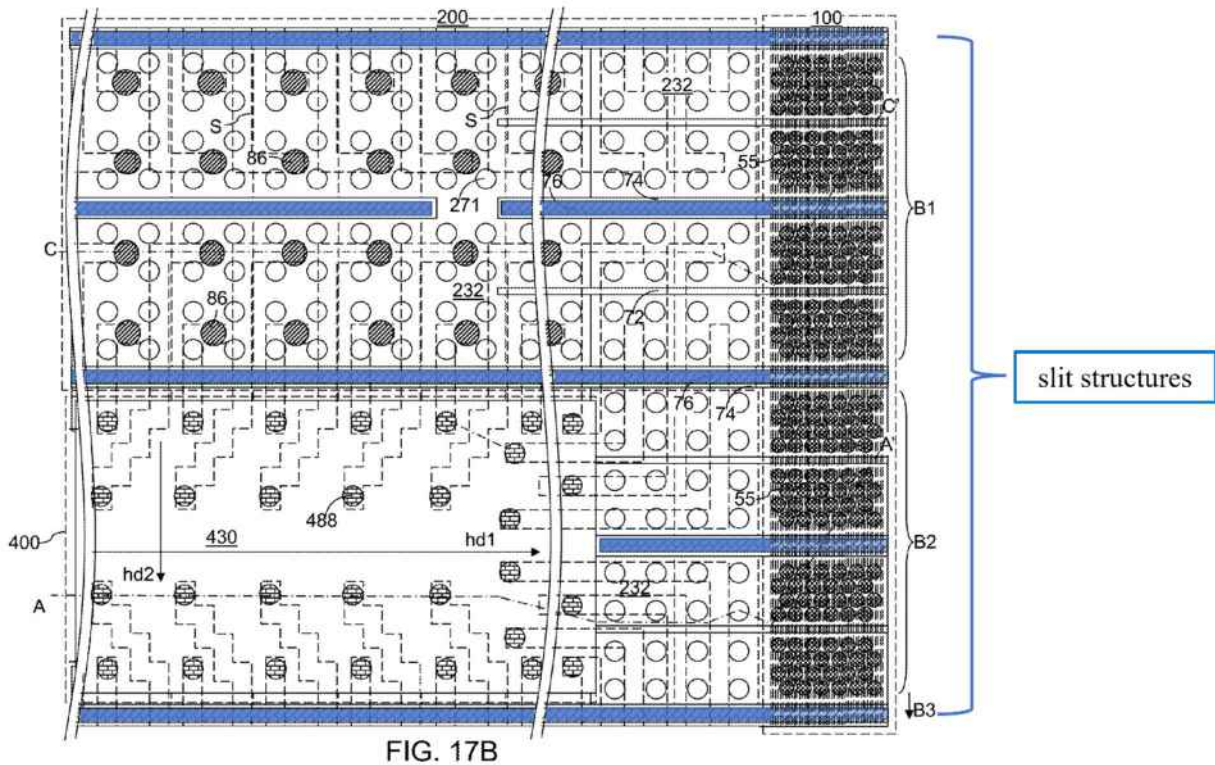


FIG. 17A

Toyama, Figure 17A; Lee, ¶ 133. Toyama also depicts its *slit structures* (“laterally-elongated contact via structures 76”) in a top view:



Toyama, Figure 17B; Lee, ¶¶ 133-134.

Although Toyama and the 378 Patent’s claim use slightly different terminology, each of “laterally-elongated contact via structures 76” is *a slit structure* as claimed. Lee, ¶ 133. As an initial matter, the plain meaning of “slit” is of a laterally-elongated structure. *Id.*; Ex. 1022, 4 (Merriam-Webster’s definition of “slit” as “a long narrow cut or opening”). Toyama, Figure 17B (showing structure 76 has a slit shape). And, as shown in Figure 17A, above, Toyama discloses “laterally-elongated contact via structure 76” *extending vertically in the alternating layer stack* (“alternating stack (132, 146, 232, 246)”). Thus, Toyama’s “laterally-elongated contact via structures 76” meets the plain language of the claims.

Although the claims do not place any functional limitation on the “slit structure,” Toyama’s “laterally-elongated contact via structures 76” serves the same function as the 378 Patent’s “slit structures.” Lee, ¶ 135. In the 378 Patent, each “slit structure 226 acts as a source contact for NAND strings 204.” Ex. 1001, 9:63-67. Similarly, each of Toyama’s “laterally-elongated contact via structures 76” serves as a “source connection.” Toyama, [0241]. The 378 Patent’s “[s]lit structures 226 ... extend along the y-axis to separate alternating conductor/dielectric stack 210 into multiple blocks.” Ex. 1001, 9:52-54. Similarly, “laterally-elongated contact via structures 76 laterally extend along the first horizontal direction ... and laterally divide the at least one alternating stack ... into a plurality of laterally spaced-apart blocks.” Toyama, [0237].

Although the citations above are for Toyama’s “first exemplary structure,” Toyama’s Second Modification also includes “laterally-elongated contact via structures 76” and teaches this limitation for the same reasons as discussed above. *See, e.g.*, Toyama, Figure 49; Lee, ¶ 136.

6. [15.E] “a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;”

As shown below, Toyama teaches *a staircase structure* (“staircase regions”) *disposed in the alternating conductor/dielectric layer stack* (“alternating stack (132,

146, 232, 246)”), *wherein the staircase structure comprises levels with each level having a conductor layer* (“electrically conductive layers 146, 246”) *thereon*:

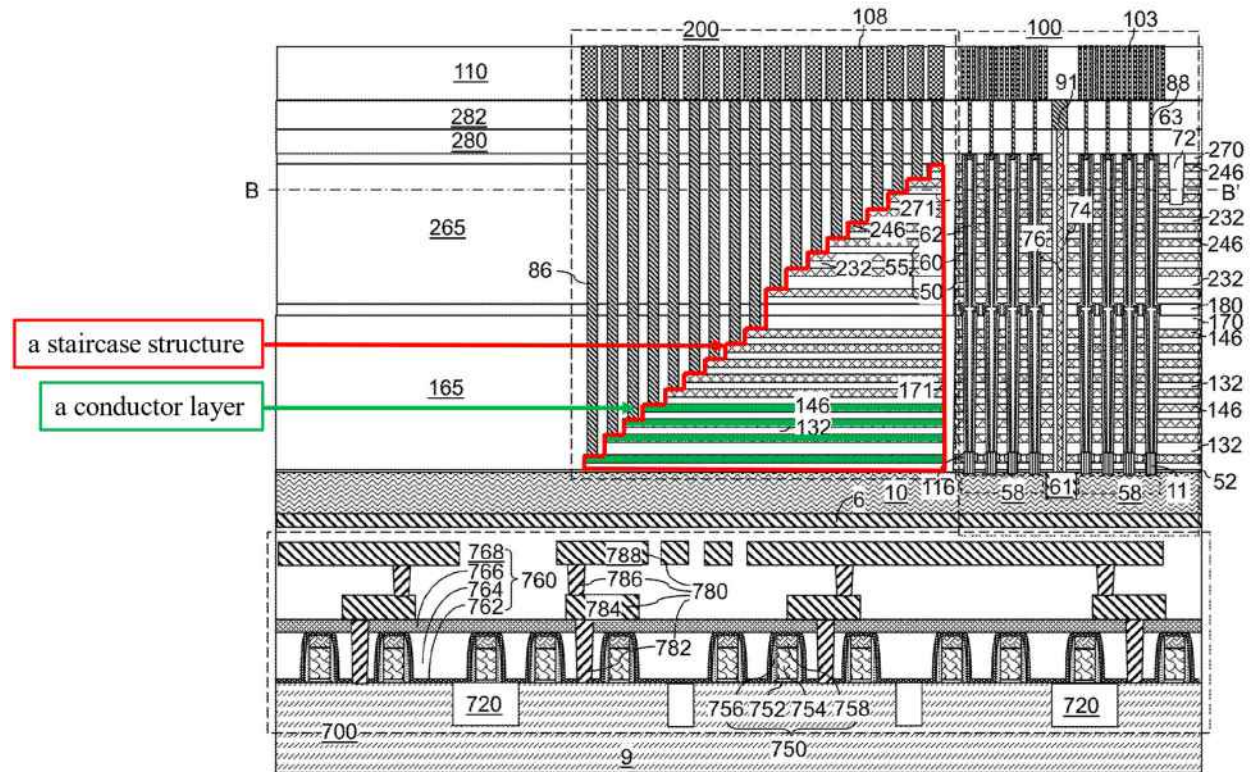


FIG. 17C

Toyama, Figure 17C; Lee, ¶ 137. Toyama explains: “[t]he at least one alternating stack (132, 146, 232, 246) comprises staircase regions that include terraces in which each underlying electrically conductive layer (146, 246) extends farther along the first horizontal direction hd1 than any overlying electrically conductive layer (146, 246).” Toyama, [0232].

Although the citations above are for Toyama’s “first exemplary structure,” a POSITA would have understood Toyama’s Second Modification also teaches this limitation. Lee, ¶ 138. In describing the fourth exemplary structure, Toyama notes

“word line contact via structures [86] can be formed as in the first through third embodiments.” Toyama, [0322]. As Toyama shows for the first embodiment, “word line contact via structures 86” are in contact with the electrically conductive layers (146, 246) in the “staircase regions.” Toyama, Figure 17C, [0243]. A POSITA would therefore have understood Toyama’s fourth exemplary structure (and modifications thereof) to include *a staircase structure* (“staircase regions”). Lee, ¶ 138.

At the very least, a POSITA would have found it obvious to implement a staircase structure (“staircase regions”) in Toyama’s Second Modification. A POSITA would have known that for the memory device to be functional, there must be some way of conveying signals to the “electrically conductive layers (146, 246)” because these layers serve as the word lines of the memory stack structures. Toyama, [0323]; Lee, ¶ 139. A POSITA would have found it obvious to use *a staircase structure* (“staircase regions”) to enable Toyama’s “word line contact via structures 86” to contact each of the device’s “electrically conductive layers (146, 246),” which in turn serve as the memory stack structures’ word lines. Toyama, [0323]; Lee, ¶ 139.

7. [15.F] “a word line contact disposed on the conductor layer of the each level;”

As shown below, Toyama discloses *a word line contact* (“word line contact via structures 86”) *disposed on the conductor layer of the each level* (“electrically conductive layers (146, 246)”):

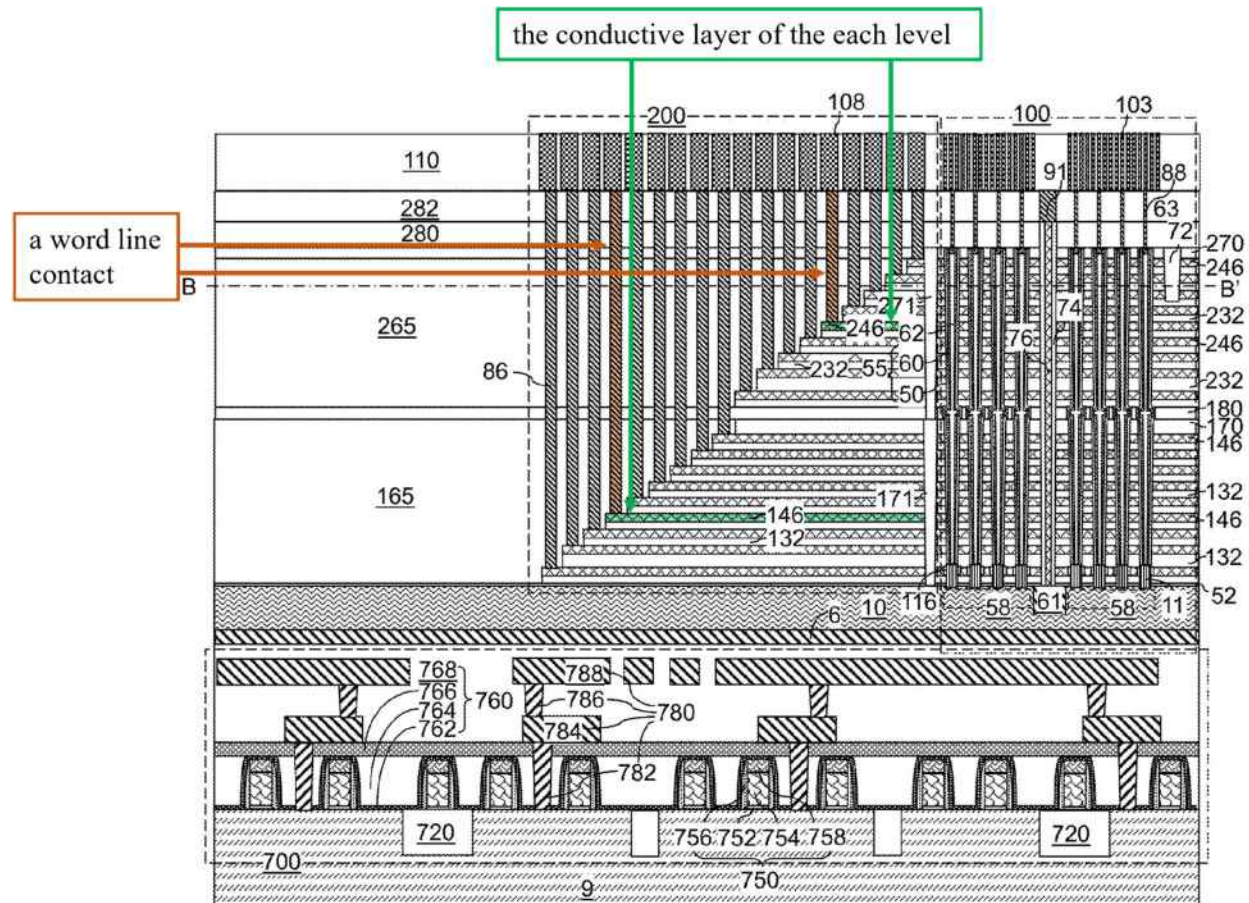


FIG. 17C

Toyama, Figure 17C; *id.*, [0260] (“[W]ord line contact via structures 86 ... can contact respective portions of electrically conductive layers (146, 246)”); Lee, ¶ 140.

Although the citations above are for Toyama’s “first exemplary structure,” Toyama’s Second Modification also teaches this limitation for the same reason. In

describing the fourth exemplary structure, Toyama notes that the *word line contacts* (“word line contact via structures”) “can be formed as in the first through third embodiments.” Toyama, [0322]. At the very least, a POSITA would have found it obvious to convey signals to electrically conductive layers (146, 246) using “word line contact via structures” on “staircase regions” for the reasons described above. Section IX.A.6 (limitation [15.E]). Lee, ¶¶ 141-142.

8. [15.G] “local contacts disposed on the channel structures and the slit structures; and”

As an initial matter, the 378 Patent states that “[i]n some embodiments, 3D memory device 200 includes a plurality of ‘local contacts.’” Ex. 1001, 11:16-17. “The contacts are referred to herein as ‘local contacts’ because they are in direct contact with the memory array structures, and further because they are formed within dielectric layer 230.” *Id.*, 11:20-24.

a. First exemplary structure

Toyama discloses *local contacts* (“drain contact via structures 88”) *disposed on* (in contact with and extending above) *the channel structures* (“memory stack structures 55”), and *local contacts* (“source connection via structures 91”) *disposed on* (in contact with and extending above) *the slit structures* (“laterally-elongated contact via structures 76”):

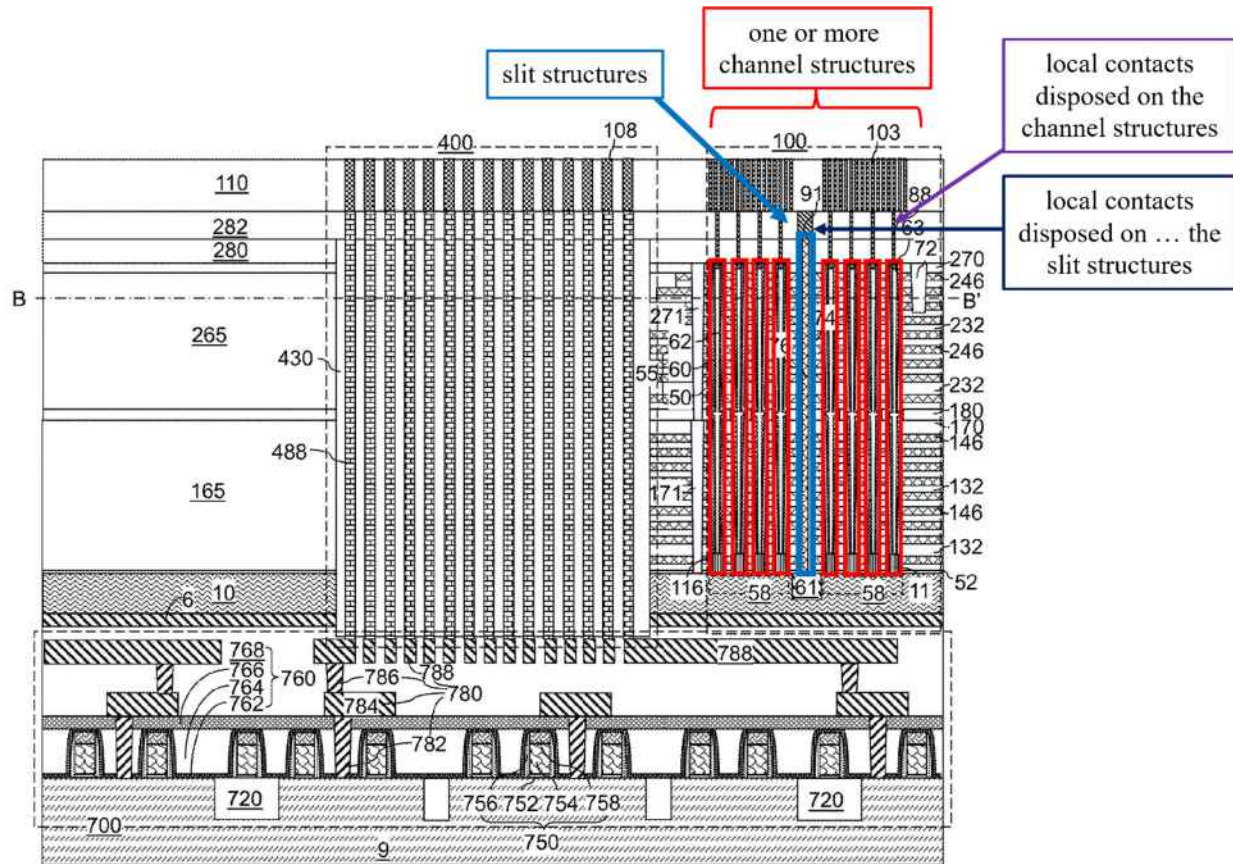


FIG. 17A

Toyama, Figure 17A; *id.*, [0251] (“The bit lines 103 are formed over the memory-level assembly, and are electrically coupled to nodes (e.g., drain regions 63) of the memory stack structures 55 by the drain contact via structures 88.”); *id.*, [0241] (“A source connection via structure 91 can extend through the contact level dielectric layers (280, 282) to provide electrical connection to the laterally-elongated contact via structures 76.”); Lee, ¶ 144.

b. Second Modification

Although the citations above are for Toyama's "first exemplary structure," Toyama's Second Modification also teaches (or, at the very least renders obvious) this limitation.

Toyama's Second Modification discloses *local contacts* ("drain contact via structures 88") *disposed on the channel structures* ("memory stack structures 55") for the reasons explained above for the first exemplary structure. Toyama, Figure 49, [0342] ("drain contact via structures 88 ... can be formed as in the first through third embodiments"); Lee, ¶¶ 145-148.

Toyama does not expressly disclose *local contacts* ("source connection via structures 91") *disposed on the slit structures* ("laterally-elongated contact via structures 76") in the context of the Second Modification, likely because of where the cross section of Figure 49 is taken. Lee, ¶ 146. However, a POSITA would have understood the Second Modification to include *local contacts disposed on the slit structures* ("source connection via structures 91"). Indeed, in describing the Second Modification, Toyama notes "the metal interconnect structures can include ... source connection line structures (not shown)." Toyama, [0342]. As expressly described in the first exemplary structure, "source connection line structures 101 ... contact the source connection via structures 91 to provide electrically conductive paths for biasing the source region 61 through the laterally-elongated contact via structures

76.” Toyama, [0250]. A POSITA would have understood the Second Modification, which expressly includes “source connection line structures,” “source region 61,” and “laterally elongated contact via structure 76,” would also include “source connection via structures.” Lee, ¶¶ 146-147].

At the very least, a POSITA would have found the use of *local contacts disposed on the slit structures* (“source connection via structures 91”) obvious. A POSITA would have understood “laterally-elongated contact via structures 76” serve as source lines for “source regions 61.” Toyama, [0382]; Lee, ¶ 148. And a POSITA would have understood that for “via structures 76” to serve their purpose, they would connect to a higher-level source connection. *Id.* Given that other of Toyama’s embodiments (from which the Second Modification derives) expressly disclose “source connection via structures 91” for this purpose, a POSITA would have been motivated to implement “source connection via structures 91” in the Second Modification, and would have had a reasonable expectation of success in doing so. *Id.*

9. [15.H] “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.”

a. Second Modification

In Toyama’s Second Modification, “through-memory-level via structures 676” are *through array contacts*:

FIG. 49

As noted above with reference to limitations [15.C] and [15.A.ii], respectively, in the Second Modification, “insulating liners 674” are individually and collectively *the dielectric structure*, and the insulating material layer filling “opening 151” is *the isolation structure*. Sections **Error! Reference source not found., Error! Reference source not found..**

discloses *through array contacts* (“through-memory-level via structures 676”) *extending vertically through the dielectric* (“insulating liners 674”) *and isolation* (the insulating material layer filling “opening 151”) *structures*. Toyama, [0340]-[0342]; Lee, ¶¶ 149-151.¹⁰

b. First exemplary structure

In Toyama’s first exemplary structure, “through-memory-level via structures 488” are *through array contacts (TACs)*:

¹⁰ As explained above, the claim term *a dielectric structure* is properly understood to include one *or more* dielectric structures. Section IX.A.4.a.i (limitation [15.C]). Accordingly, the claim encompasses embodiments in which each *through array contact* extends vertically through a different *dielectric structure*. *ABS Glob., Inc. v. Cytonome/St, LLC*, 84 F.4th 1034, 1040 (Fed. Cir. 2023) (“The reference-back ‘the’ language takes its meaning from the meaning of the antecedent, so if ‘a sample stream’ has a plural-allowing meaning, so does the reference-back ‘the sample stream’ phrase.”).

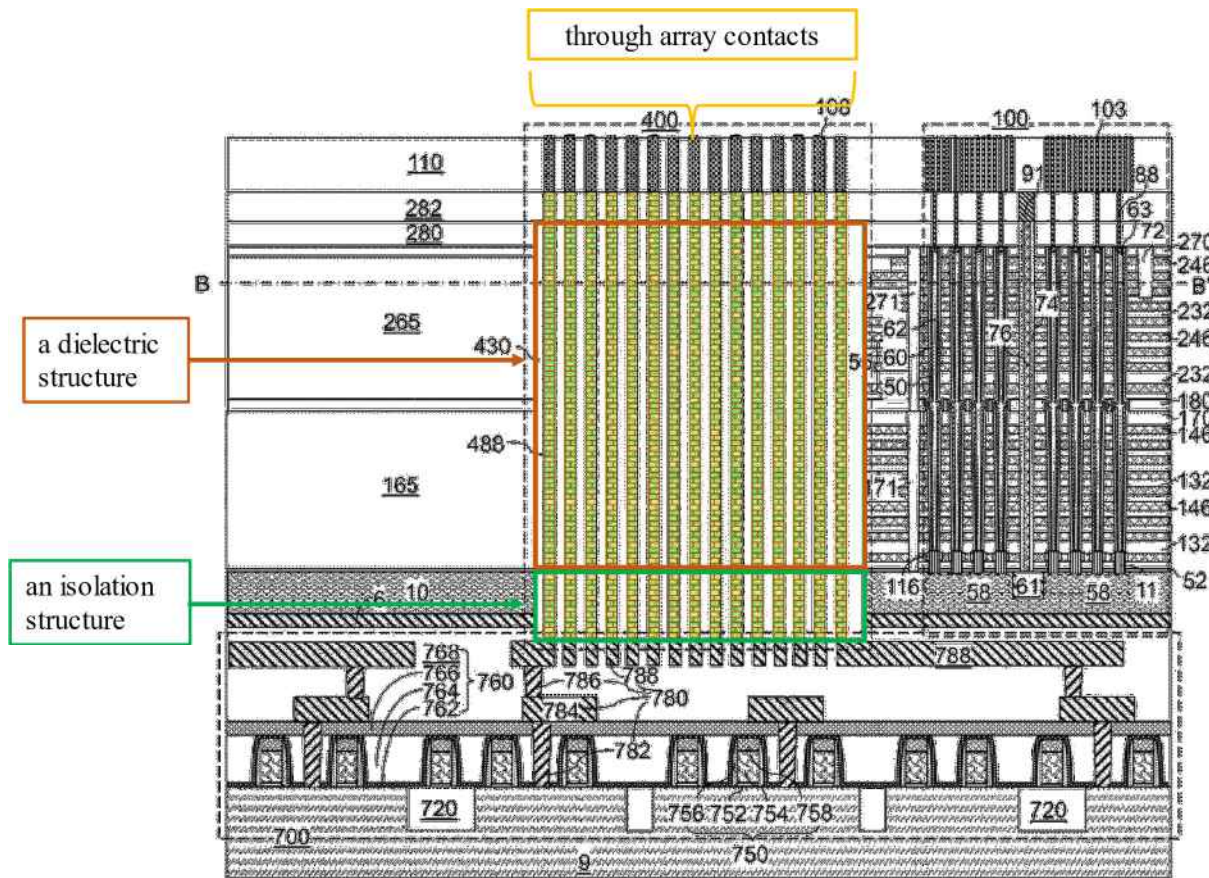


FIG. 17A

Toyama, Figure 17A; *id.*, [0239]; Lee, ¶ 152.

As noted above with reference to limitations [15.C] and [15.A.ii], respectively, in Toyama’s first exemplary structure the upper part of “dielectric fill material portion 430” is *the dielectric structure*, and the lower part of Toyama’s “dielectric fill material portion 430” is *the isolation structure*. Sections IX.A.4.b IX.A.4.a.

Toyama’s first exemplary structure thus discloses *through array contacts* (“through-memory-level via structures 488”) *extending vertically through the dielectric* (upper part of “dielectric fill material portion 430”) *and isolation* (lower

part of “dielectric fill material portion 430”) *structures*. Toyama, [0239]; Lee ¶¶ 152-154.

B. Claim 16:

1. [16] “The 3D memory device of claim 15, wherein the dielectric structure abuts a sidewall of each TAC of the TACs.”

Toyama’s Second Modification, and Toyama’s first exemplary structure, both teach this limitation.

a. Second Modification

In the context of its Second Modification, Toyama teaches *the dielectric structure* (“insulating liners 674”) *abuts a sidewall of each TAC of the TACs* (a sidewall of each of the “through-memory-level via structures 676”):

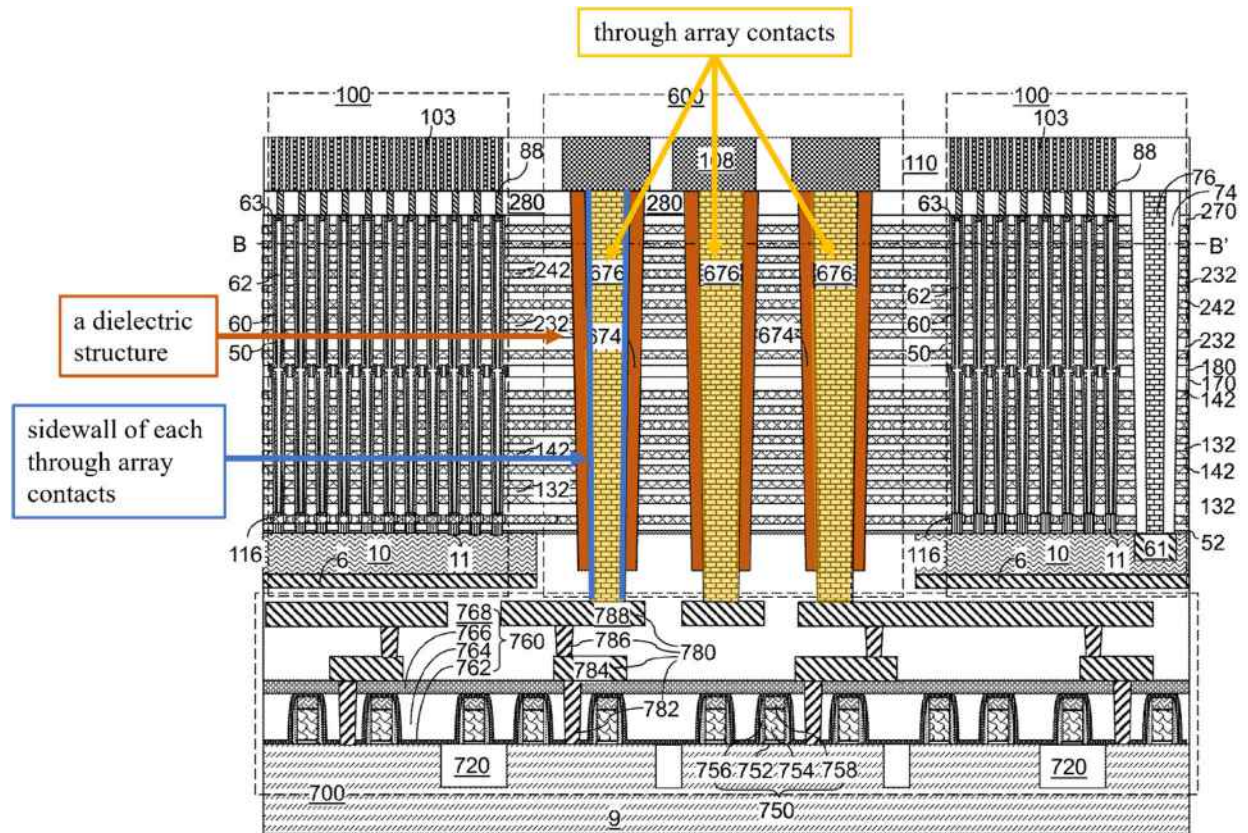


FIG. 49

Toyama, Figure 49; Lee, ¶ 156.

b. First exemplary structure

In the context of its first exemplary structure, Toyama teaches *the dielectric structure* (upper part of “dielectric fill material portion 430”) *abuts a sidewall of each TAC of the TACs* (sidewall surface of “through-memory-level via structures 488”):

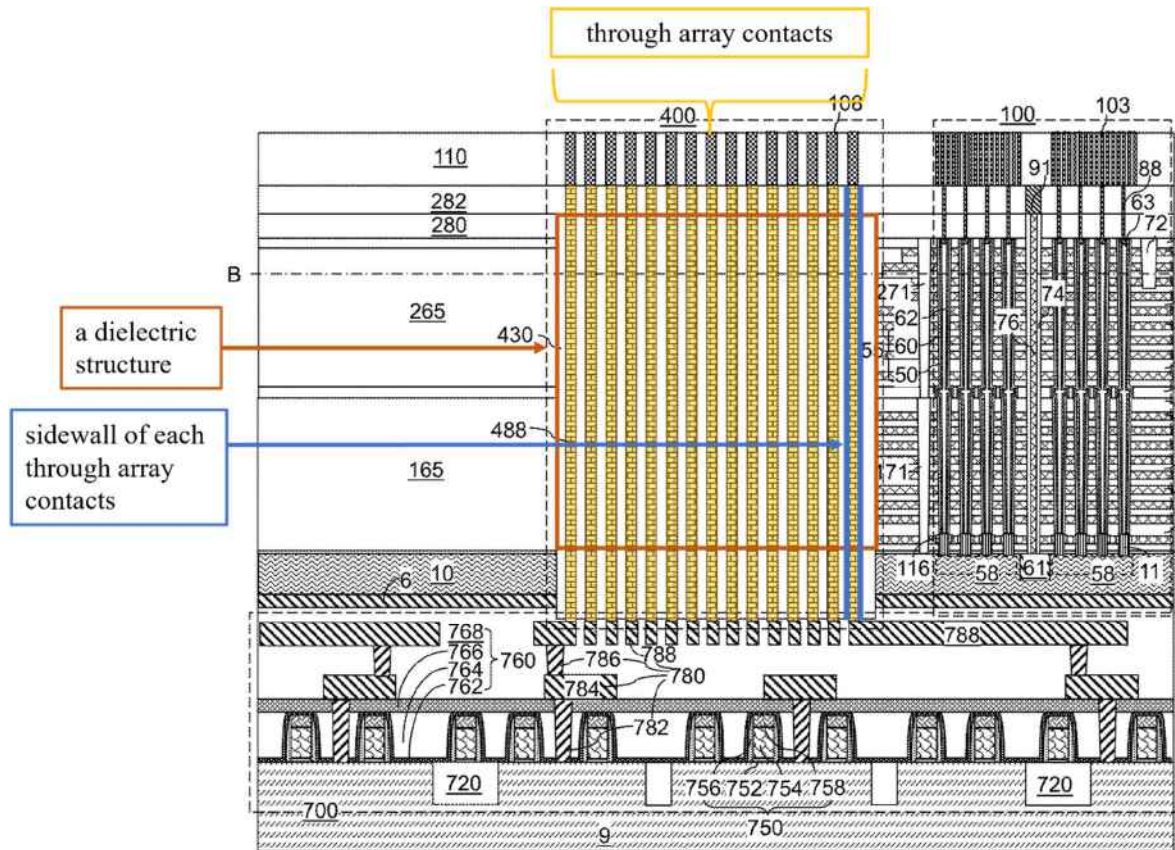


FIG. 17A

Toyama, Figure 17A; Lee, ¶ 157.

C. Claim 17:

1. [17] “The 3D memory device of claim 15, wherein the dielectric structure comprises a through array contact region of the 3D memory device.”

As an initial matter, the 378 Patent broadly defines *through array contact region*, noting that it “can have a rectangle or square shape” but that “these shapes are not limiting and dielectric structure 232 can have any shape according to a design layout,” and that “multiple dielectric structures ... are possible across [the]

substrate.” Ex. 1001, 10:49-56. Toyama’s Second Modification, and Toyama’s first exemplary structure, both teach this limitation. Lee, ¶¶ 158-161.

a. Second Modification

Toyama discloses *the dielectric structure* (“insulating liners 674”) *comprises a through array contact region of the 3D memory device* (part of “through-memory-level via region 600”):

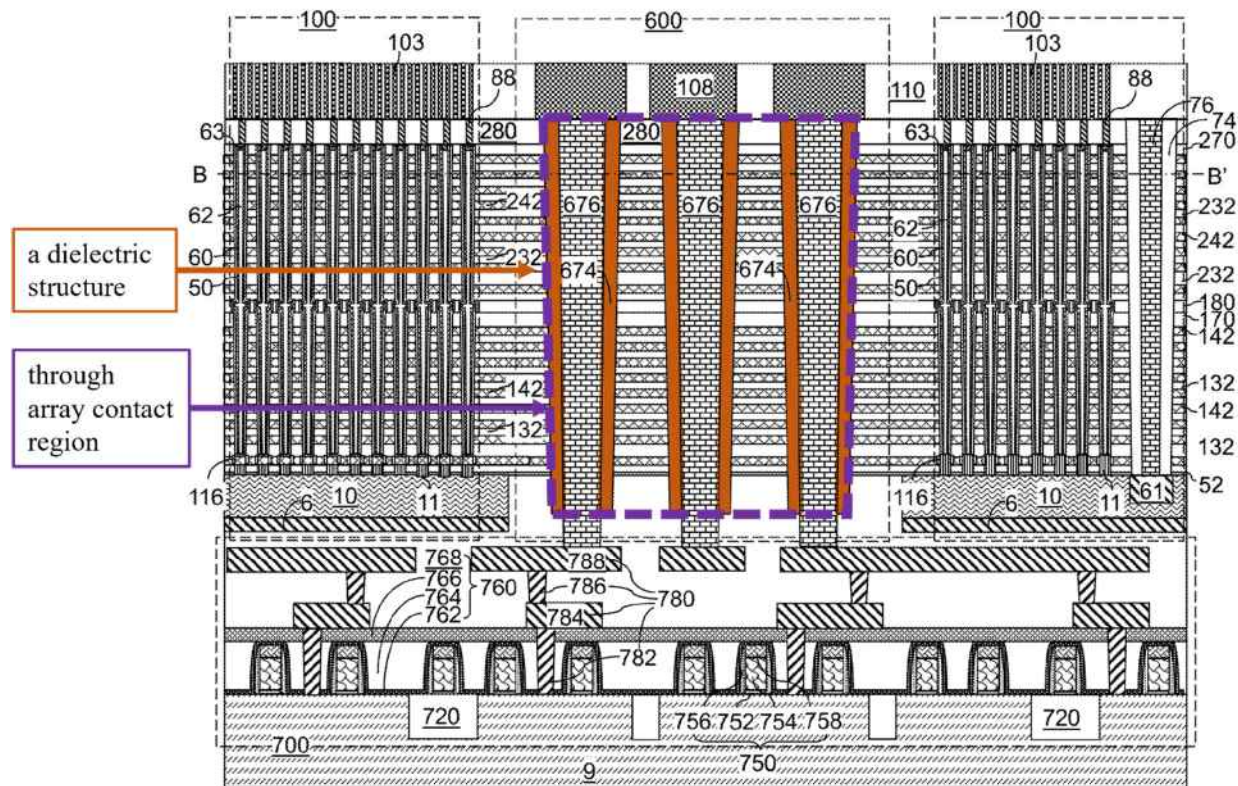


FIG. 49

Toyama, Figure 49; *id.*, [0333], [340], [352]; Lee, ¶¶ 159-160. As “[i]n some embodiments” of the 378 Patent, the “dielectric structure ... defines the boundaries, the shape, and the size of [the] TAC region.” Ex. 1001, 10:21-23. Thus, the part of the dielectric structure (“insulating liners 674”) through which the *through array*

D. Claim 19:

1. [19] **“The 3D memory device of claim 15, wherein the dielectric material comprises silicon oxide.”**

Toyama’s Second Modification and Toyama’s first exemplary structure teach this limitation.

a. Second Modification

As noted above for limitation [15.C.iv], in the Second Modification, “insulating liners 674” are *a dielectric structure*, and the material from which “insulating liners 674” are made is *a dielectric material*.

Toyama contemplates that “insulating liner 674” comprises silicon oxide. Specifically, Toyama notes “insulating liner 674” may “hav[e] a same material composition ... as the insulating spacer 74.” Toyama, [0381]. Toyama describes “spacer 74,” in turn, as including “an insulating material such as silicon oxide.” *Id.*, [0234].

Thus, Toyama teaches *the dielectric material* (a material out of which “insulating liners 674” are made) *comprises silicon oxide*.

To the extent Toyama does not expressly disclose this limitation, it would have been obvious to a POSITA. By its very terms, “insulating liner 674” is insulating, and a POSITA would have known silicon oxide to be a commonplace and suitable insulating material from which “insulating liner 674” could be made. Ex. 1019 (U.S. Pat. No. 9,293,348), 2:61-65 (“dielectric structure” may comprise an

“oxide” such as “silicon oxide”); Ex. 1020 (U.S. Pat. No. 8,598,643), Figs. 11-12, 3:1-8 (discussing “formation of a conformal silicon oxide liner” in 3D-NAND); Ex. 1021 (U.S. Pat. No. 8,697,519), 7:30-40 (“the liner insulating layer may include a silicon oxide layer”); Lee, ¶¶ 163-164.

b. First exemplary structure

As noted above for limitation [15.C.iv], in Toyama’s first exemplary structure, *the dielectric material* is the “dielectric fill material” that forms “dielectric fill material portion 430.” Section A.4.b.iv.

Toyama further notes “dielectric fill material portion 430 includes a dielectric material such as undoped silicate glass (e.g., silicon oxide), doped silicate glass, or a spin-on glass (SOG).” Toyama, [0216].

Toyama thus teaches *the dielectric material* (“dielectric fill material” that forms “dielectric fill material portion 430”) *comprises silicon oxide*. Lee, ¶ 165.

E. Claim 20:

- 1. [20] “The 3D memory device of claim 15, wherein the TACs comprise a conductive material.”**

Toyama’s Second Modification and Toyama’s first exemplary structure teach this limitation.

a. Second Modification

As noted above for limitation [15.H], in the Second Modification, the “through-memory-level via structures 676” are *through array contacts (TACs)*. Section IX.A.9.a.

Toyama teaches *the TACs* (“through-memory-level structures 676”) *comprise a conductive material*. Toyama, [0341] (“Each remaining portion of the ... conductive material in a through-memory-level opening 679 constitutes a through-memory-level via structure 676.”); Lee, ¶ 167.

b. First exemplary structure

As noted above for limitation [15.H], in Toyama’s first exemplary structure the “through-memory-level via structures 488” are *through array contacts (TACs)*. Sections IX.A.9.a.

Toyama teaches *the TACs* (“through-memory-level structures 488”) *comprise a conductive material*. Toyama, [0244] (“through-memory-level via structures 488 may be formed ... [by] depositing a conductive material”); Lee, ¶ 168.

X. GROUND 2: MUSHIGA IN VIEW OF THE KNOWLEDGE OF A POSITA

A. Claim 15:

1. [15.PRE] “A three-dimensional (3D) memory device, comprising:”

To the extent the preamble is limiting, Mushiga discloses *a three-dimensional (3D) memory device*. Mushiga, 6:24-29 (“The embodiments of the disclosure can

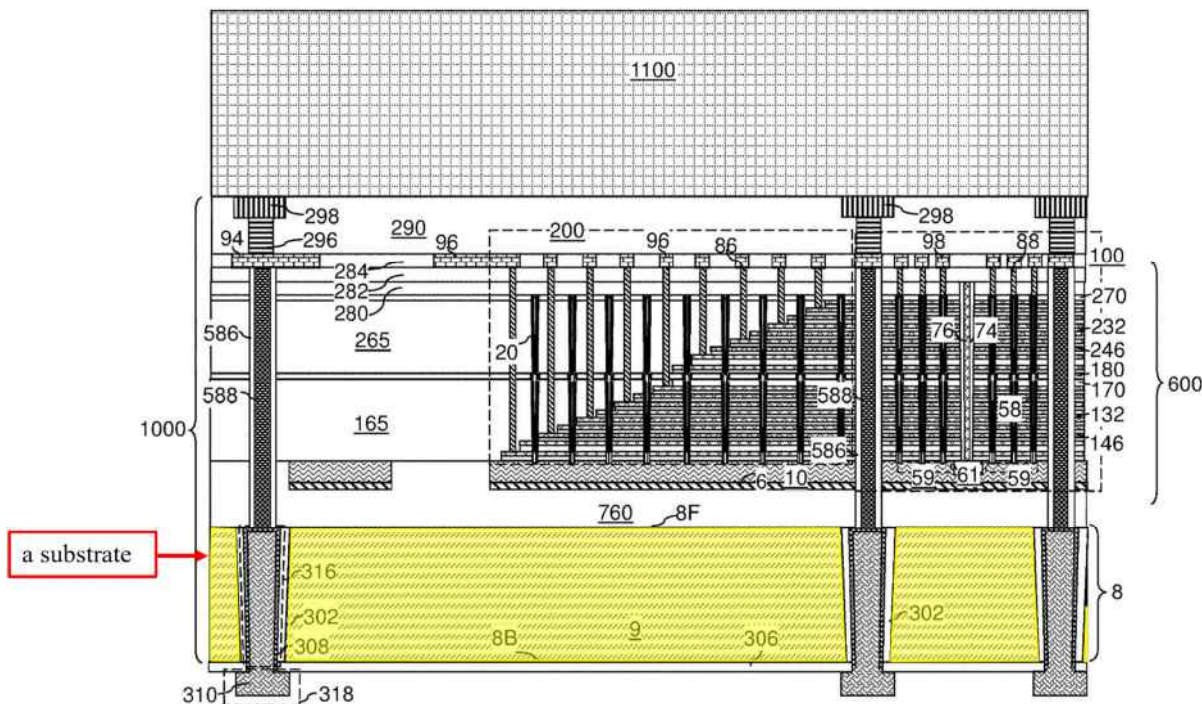
be employed to form various structures including ... three-dimensional monolithic memory array devices.”); Lee, ¶ 170.

2. [15.A] “a substrate with an isolation structure;”

a. [15.A.i] “a substrate”

Mushiga discloses *a substrate*.

As an initial matter, the 378 Patent defines a “substrate” as “a material onto which subsequent material layers are added, or otherwise ‘disposed.’” Ex. 1001, 4:41-43. Because Mushiga’s “first semiconductor substrate 8” is a material onto which subsequent material layers are added, or otherwise disposed, it is *a substrate*:



Mushiga, Figure 11; 9:8-14 (“insulating material layer 760” formed over substrate); 8:62-64 (“first semiconductor devices 600” formed over substrate); Lee, ¶ 172.

Mushiga’s *substrate* (“first semiconductor substrate 8”) is *with* its *isolation structure* (elements 302, 306). Indeed, Mushiga’s *isolation structure* (elements 302, 306) is formed by removing portions of the substrate and is subsequently formed within the *substrate* (“first semiconductor substrate 8”). Lee, ¶¶ 173-174.

3. [15.B] “an alternating conductor/dielectric layer stack disposed on the substrate;”

As shown below, Mushiga’s “alternating stack of insulating layers (132, 232) and electrically conductive layers (146, 246)” is *an alternating conductor/dielectric layer stack disposed on the substrate* (“semiconductor substrate 9”):

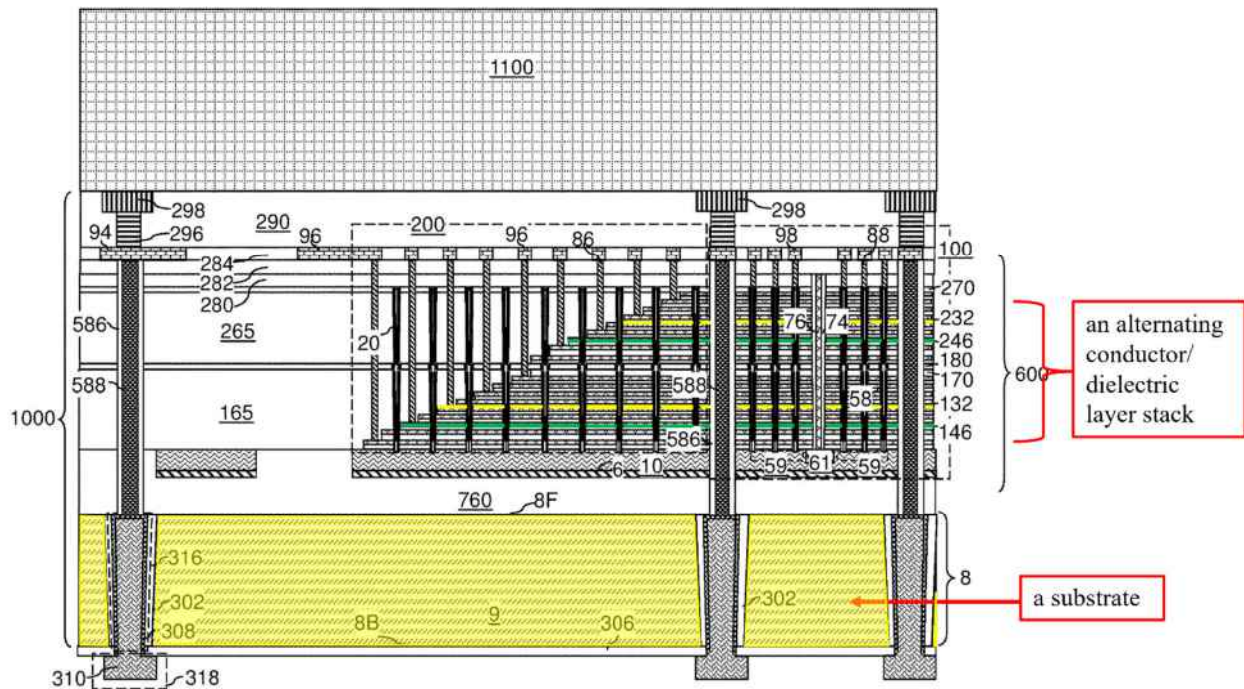


FIG. 11

Mushiga, Figure 11; 8:67-9:2; Lee, ¶ 175. Recall the 378 Patent instructs that the term “on” “should be interpreted in the broadest manner such that ‘on’ not only

means ‘directly on’ something but also includes the meaning of ‘on’ something with an intermediate feature or a layer therebetween.” Ex. 1001, 4:20-25.

4. **[15.C] “a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;”**

- a. **[15.C.i] “a dielectric structure on the isolation structure”**

As shown below, Mushiga’s “insulating material layer 760,” “first retro-stepped dielectric material portion 165,” “inter-tier dielectric layer 180,” “second retro-stepped dielectric material portion 265,” and “insulating spacer 586” are, collectively, *a dielectric structure*:

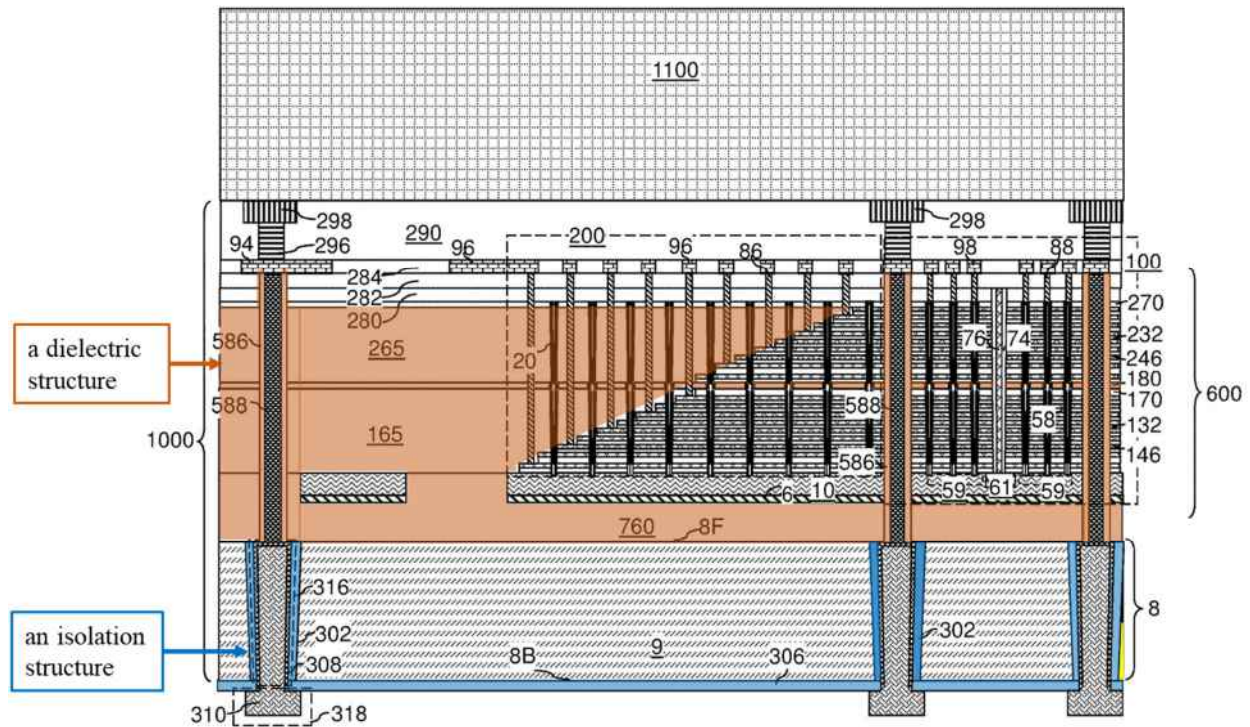


FIG. 11

Mushiga, Figure 11; Lee, ¶ 177.

The components indicated are *a dielectric structure* because each of the components consists of an insulating material because Mushiga discloses that insulating material layer 760 includes a dielectric material such as silicon oxide. Mushiga, 9:8-10, 15:13-32. Retro-stepped dielectric material portions 165, 265 are similarly made from a dielectric material. *Id.*, 9:22-23, 9:38-39; Lee, ¶ 178. And a POSITA would have understood that “insulating spacer 586,” being insulating, would also consist of a dielectric material, e.g., because Mushiga discloses various insulating liners are made of silicon oxide. Mushiga, 11:64-66; Lee, ¶ 178. And because these components together are something “that is constructed,” they are a

structure. Ex. 1022, 5 (Merriam-Webster definition of “structure” as “something ([such] as a building) that is constructed”); Lee, ¶ 179.

The 378 Patent instructs that the term “on” “should be interpreted in the broadest manner such that ‘on’ not only means ‘directly on’ something but also ... ‘on’ something with an intermediate feature or a layer therebetween.” Ex. 1001, 4:20-29; Lee, ¶ 180. As illustrated above, at least one element of Mushiga’s *dielectric structure* (namely, “insulating material layer 760”) is directly on the *isolation structure* (elements 302, 306). Thus, Mushiga’s *dielectric structure* (elements 760, 165, 180, 265, 586) is **on** its *isolation structure* (elements 302, 306).

b. [15.C.ii] “a dielectric structure ... extending vertically through the alternating conductor/dielectric layer stack”

As noted immediately above, Mushiga’s elements 760, 165, 180, 265, and 586 are, collectively, *a dielectric structure*. And, as noted above with reference to limitation [15.B], Mushiga’s “alternating stack” is the alternating conductor/dielectric layer stack (132, 146, 232, 246). Section X.A.3. Thus, as shown in the figure below, Mushiga discloses *a dielectric structure* (elements 760, 165, 180, 265, 586) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack” 132, 146, 232, 246):

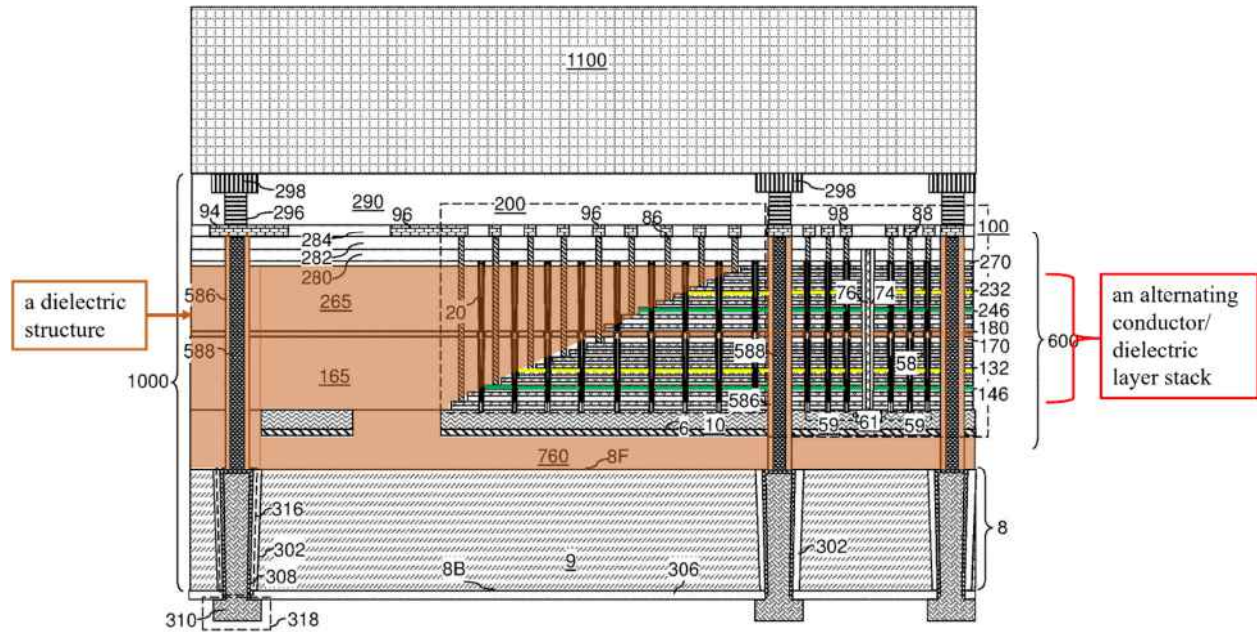


FIG. 11

Mushiga, Figure 11; Lee, ¶ 181.

- c. [15.C.iii] “a dielectric structure ... wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure”

As illustrated below, Mushiga teaches this limitation:

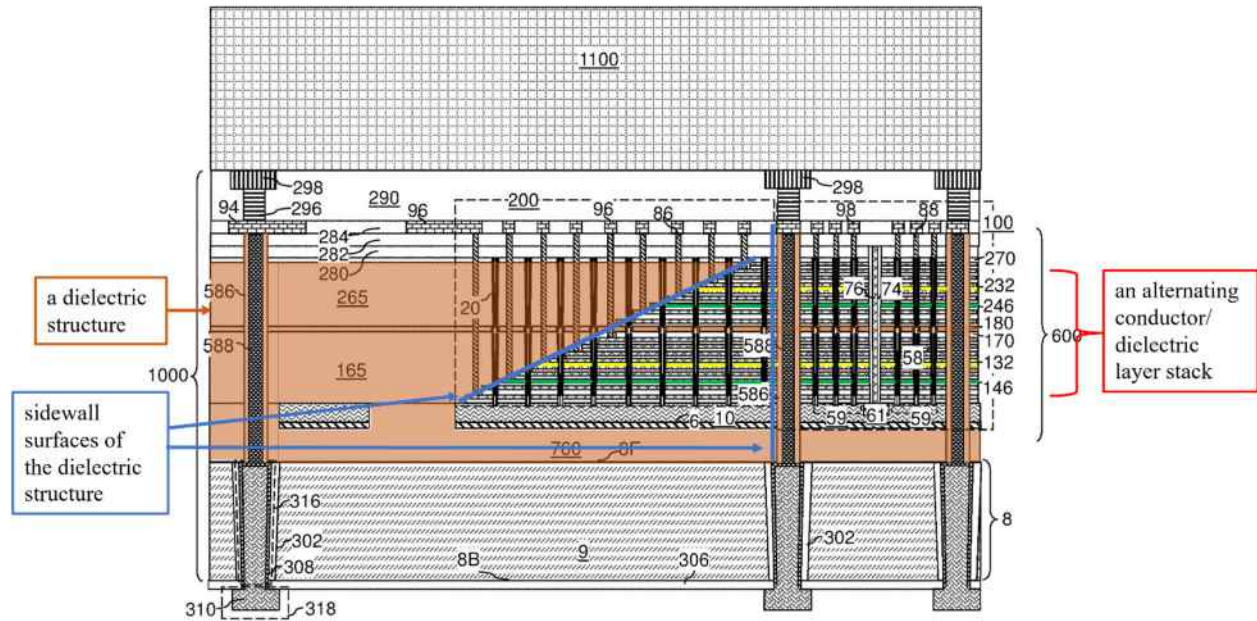


FIG. 11

Mushiga, Figure 11; Lee, ¶ 182. Figure 11, above, depicts two sidewall surfaces that meet this limitation: (1) where “retro-stepped dielectric material portions” (165, 265) meet the alternating stack; and (2) where “insulating spacer 586” meets the alternating stack. Thus, Mushiga discloses *a dielectric structure* (elements 760, 165, 180, 265, 586) *wherein the alternating conductor/dielectric layer stack* (“alternating stack” 132, 146, 232, 246) *abuts a sidewall surface of the dielectric structure* (where “retro-stepped dielectric material portion” 165, 265 meet the alternating stack *and/or* where “insulating spacer 586” meets the alternating stack).

d. [15.C.iv] “... wherein ... the dielectric structure is formed of a dielectric material”

As was well known in the art, an electrically insulating material in semiconductors typically refers to a dielectric material. Lee, ¶ 183; Ex. 1022, 3

(Merriam-Webster definition of “dielectric” as “a nonconductor of direct electric current”). As noted above for limitation [15.C.i], each component of Mushiga’s *dielectric structure* (elements 760, 165, 180, 265, 586) *is formed of a dielectric material, e.g., silicon oxide*. Section X.A.4.a, above. Thus, Mushiga teaches this limitation.

To the extent Mushiga does not expressly disclose that element 586 (or elements 760, 165, 180, 265) is formed of a dielectric material, it would have been obvious to a POSITA to form that element from a dielectric material, such as silicon oxide, because Mushiga expressly discloses each of these elements is insulating and/or dielectric. Section X.D.1, below; Lee, ¶ 184.

5. [15.D] “channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;”
 - a. [15.D.i] “channel structures ... extending vertically through the alternating conductor/dielectric layer stack”

As shown below, Mushiga discloses *channel structures* (“memory stack structures 58”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack” 132, 146, 232, 246):

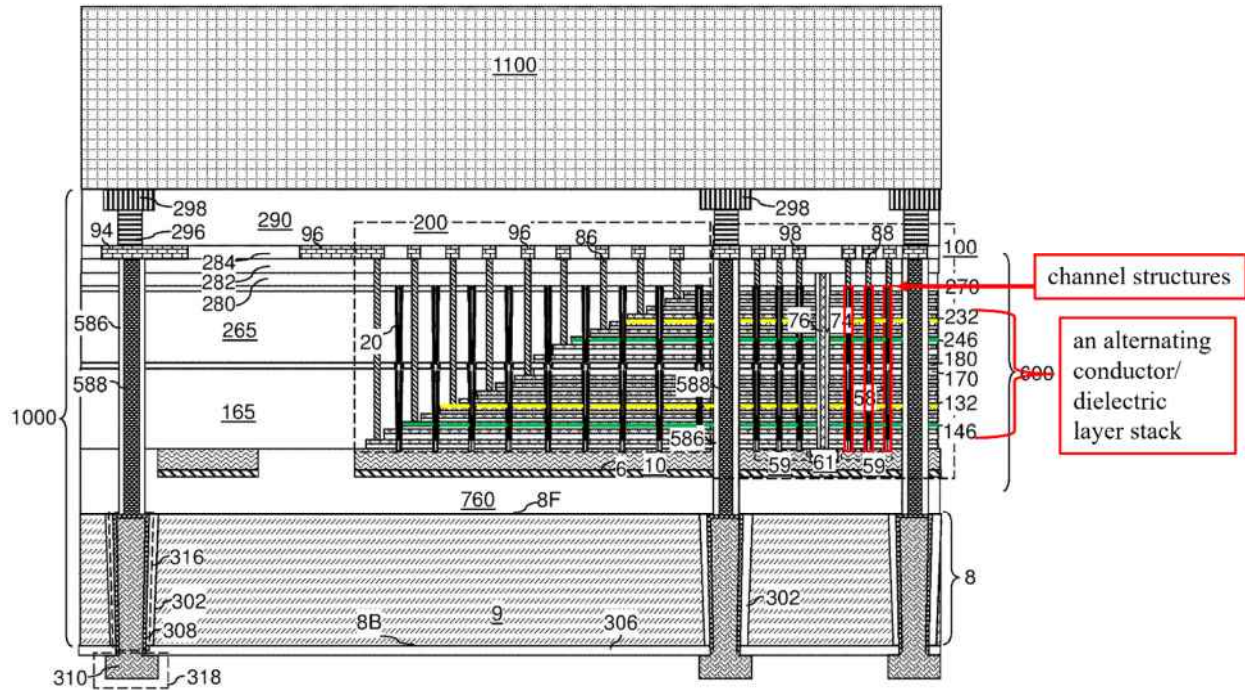


FIG. 11

Mushiga, Figure 11; *id.*, 9:2-5; Lee, ¶ 186.

Indeed, Mushiga’s “memory stack structures 58” perform the same function and are composed of the same components as the 378 Patent’s “channel structures.” Like the 378 Patent’s channel structures, Mushiga’s “memory stack structures 58” serve as the device’s memory elements. Ex. 1001, 14:4-31 (“channel structure” includes a “memory film”); Mushiga, 9:2-4 (“memory stack structures 58 includ[e] a respective vertical stack of memory elements”); Lee, ¶ 187. The 378 Patent’s “channel structures” and Mushiga’s “memory stack structures 58” are also composed of the same components. “Channel structure 216 is filled with semiconductor materials (e.g., as a semiconductor channel 218) and dielectric materials (e.g., as a memory film 220).” Ex. 1001, 9:1-6. Similarly, Mushiga

explains “[e]ach of the memory stack structures 58 ... can include, from outside to inside, a blocking dielectric layer, a charge storage layer, a tunneling dielectric layer, and a vertical semiconductor channel.” Mushiga, 9:53-57.

b. [15.D.ii] “slit structures extending vertically through the alternating conductor/dielectric layer stack”

As shown below, Mushiga teaches *slit structures* (“backside contact via structures 76”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack” 132, 146, 232, 246):

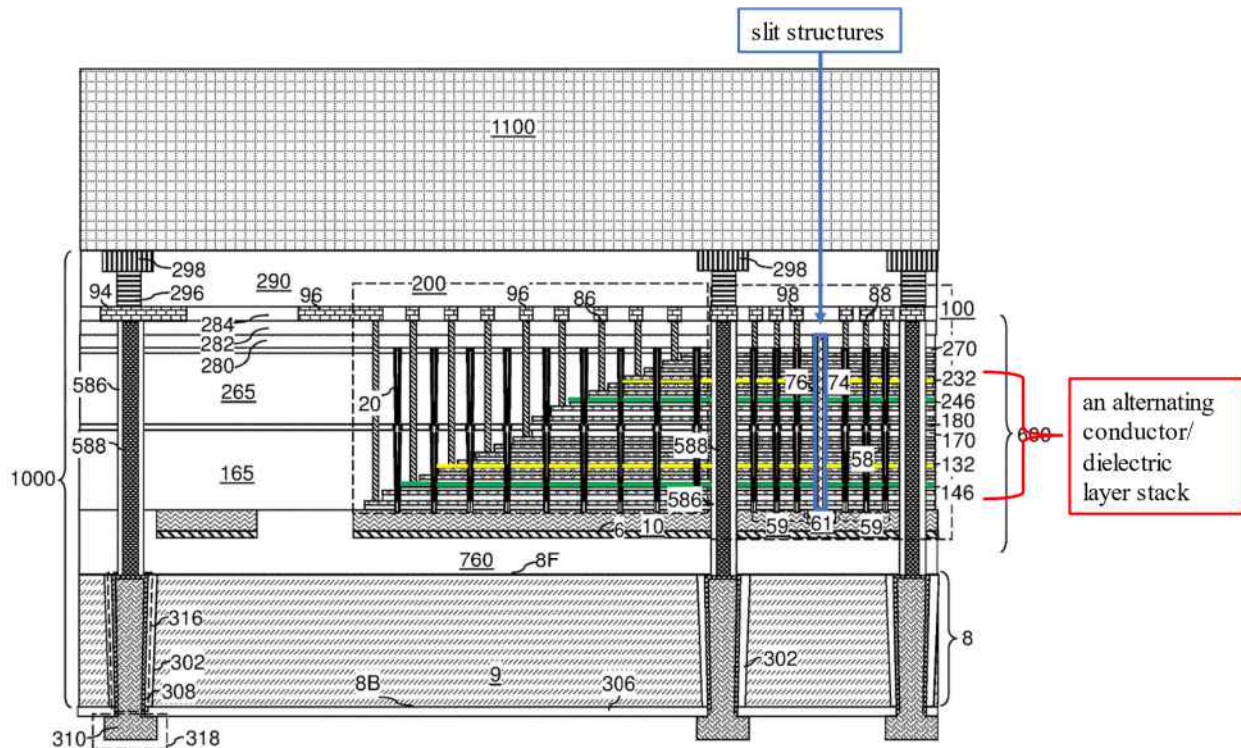


FIG. 11

Mushiga, Figure 11; Lee, ¶ 188.

Although Mushiga and the claim use slightly different terminology, each of the “backside contact via structures 76” is *a slit structure*. Lee, ¶ 189. Mushiga

forms the “backside contact via structures 76” by first creating “backside trenches” through the alternating stack, and subsequently forming “[a]n insulating spacer 74” and “a backside contact via structure 76” within “each backside trench.” Mushiga, 10:1-18. Consistent with the plain meaning of “trench,” which refers to a long and narrow cut in a surface, a POSITA would have understood each of the “backside trenches” was a long and narrow cut in the alternating stack down to the substrate. Lee, ¶ 190. And a POSITA would have understood that, as a result, each “backside contact via structures 76” was a long and narrow structure—that is, *a slit structure*. Ex. 1022, 4 (Merriam-Webster definition of “slit” as “a long narrow cut or opening”); Lee, ¶ 190.

To the extent the claim limits the process for creating the *slit structures*, a POSITA would have recognized that both the 378 Patent’s “slit structures 114,” and Mushiga’s “backside contact via structures 76,” are made in the same way. The first step in the formation of both structures is the etching of an opening through the alternating stack. Ex. 1001, 16:12-14 (etching “alternating dielectric stack” to form “slit openings”); Mushiga, 10:2-5 (etching “alternating stack” to form “[b]ackside trenches”); Lee, ¶ 191. The next step in the formation of both structures is the replacement of the sacrificial layers in the stack with electrically conductive layers. *Compare* Ex. 1001, 16:23-30 (“second dielectric layers” in stack “are replaced with conductor layers”) *with* Mushiga, 10:5-10 (“first and second sacrificial material

layers ... can be replaced with first ... and second electrically conductive layers”); Lee, ¶ 191. The final step in the formation of both structures is to form the slit structure itself. Ex. 1001, 16:57-66 (“slit openings can be filled with a conductor material ... to form slit structures,” and “a dielectric layer ... can be deposited [between the slit structure and the conductor layers]”); Mushiga, 10:16-18 (“[a]n insulating spacer 74 and a backside contact via structure 76 can be formed within each backside trench”); Lee, ¶ 191.

To the extent the claim limits the function of the *slit structures*, the function of Mushiga’s “backside contact via structures 76” is the same as the 378 Patent’s “slit structures 114”—both structures serve as the source contact for the NAND memory string. Ex. 1001, 6:25-27 (“some slit structures [] can function as the common source contact for an array ... strings”), 17:3-6 (“slit structure 226 can function as a source contact that is electrically connected to NAND string 204 through doped region 228 of substrate 202”); Mushiga, 10:16-18 (“backside contact via structures 76 ... provide electrical contact to source region 61.”); Lee, ¶ 192.

That the process by which Mushiga’s “backside contact via structure 76” and the function it performs in the device are both identical to the 378 Patent’s “slit structure” further confirm that “backside contact via structure 76” is *a slit structure*. Lee, ¶¶ 191-193.

6. [15.E] “a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;”

As shown below, Mushiga teaches *a staircase structure* (“stepped surfaces”) *disposed in the alternating conductor/dielectric layer stack* (“alternating stack” 132, 146, 232, 246), *wherein the staircase structure* (“stepped surfaces”) *comprises levels with each level having a conductor layer* (“electrically conductive layers (146, 246)”) thereon:

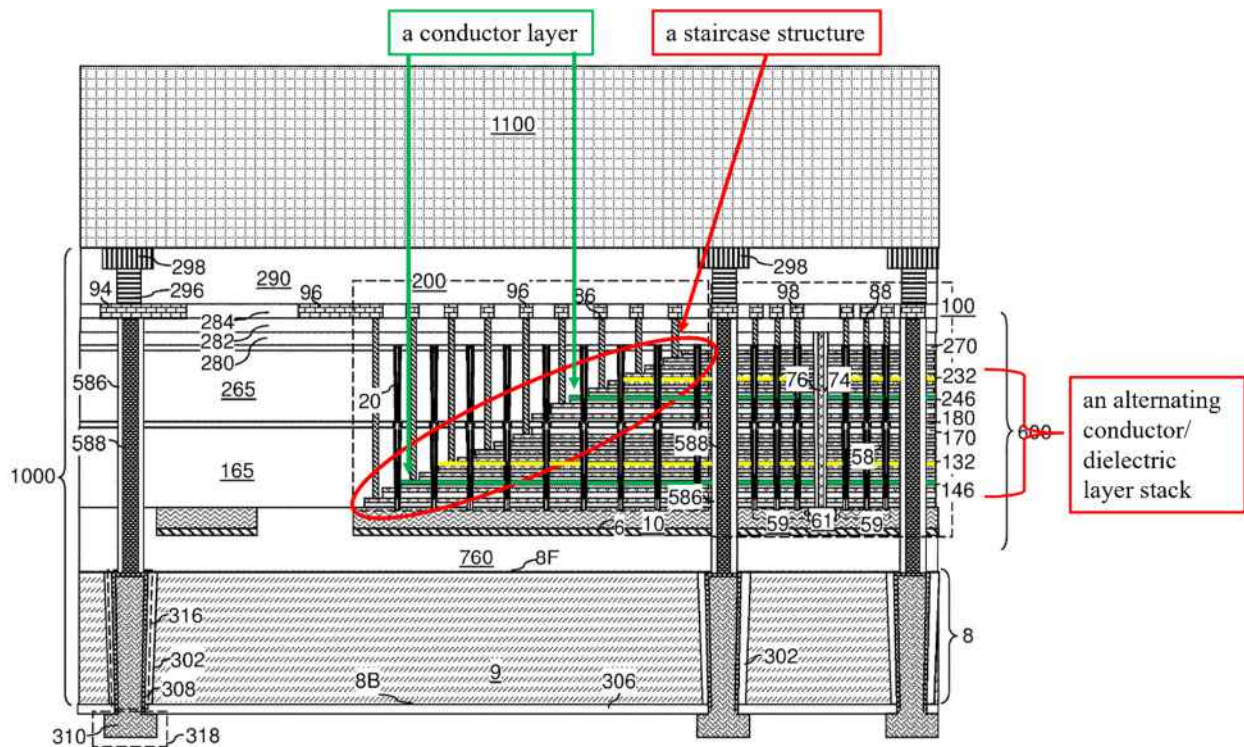


FIG. 11

Mushiga, Figure 11; Lee, ¶ 194. Mushiga explains that “[a]t least one alternating stack of insulating layers and sacrificial material layers can be formed with stepped surfaces,” that is, *a staircase structure*. Mushiga, 9:15-17. Once the sacrificial

material layers are replaced with electrically conductive layers (*id.*, 10:5-10), *the staircase structure* (“stepped surfaces”) *comprises levels with each level having a conductor layer* (“electrically conductive layers (146, 246)”). As shown above, staircase contacts extend down to a gate layer and makes contact with a gate layer, i.e., a *level* of the *staircase structure*. Although only representative conductive layers are highlighted above, a POSITA would have understood that each level has a conductive layer because each memory cell needs to be accessed by a wordline. Lee, ¶¶ 194-195.

7. [15.F] “a word line contact disposed on the conductor layer of the each level;”

As shown below, Mushiga discloses *a word line contact* (“word line contact via structures 86”) *disposed on* (in contact with and extending above) *the conductor layer of the each level* (“electrically conductive layers (146, 246)”):

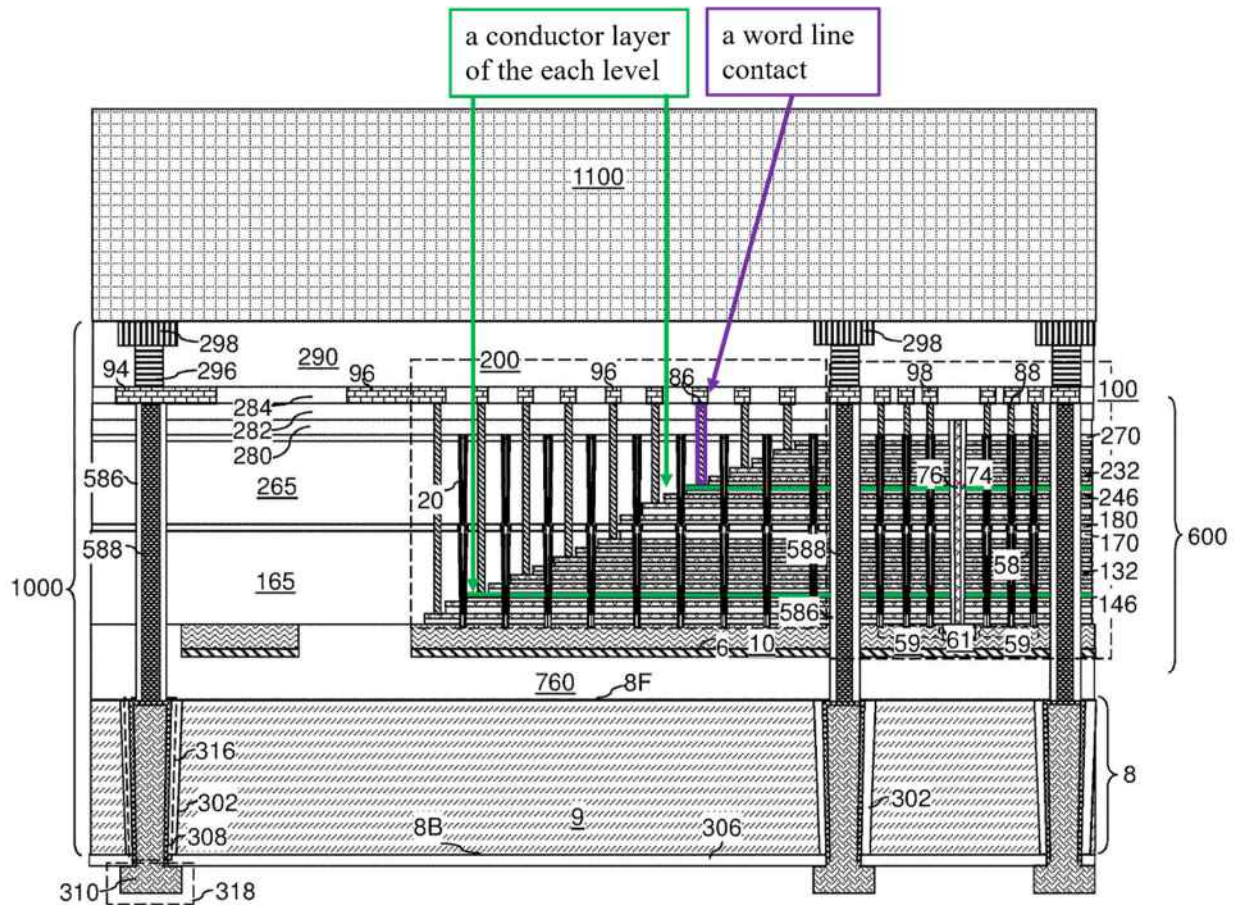


FIG. 11

Mushiga, Figure 11; *id.*, 10:21-27 (“The contact via structures can include ... word line contact via structures 86 contacting a top surface of the respective one of the first and second electrically conductive layers (146, 246).”); Lee, ¶ 196. In other words, there is a word line contact for *each level*. *Id.*

8. [15.G] “local contacts disposed on the channel structures and the slit structures; and”

a. [15.G.i] “local contacts disposed on the channel structures”

As shown below, Mushiga discloses *local contacts* (“drain contact via structures 88”) *disposed on* (in contact with and extending above) *the channel structures* (“memory stack structures 58”):

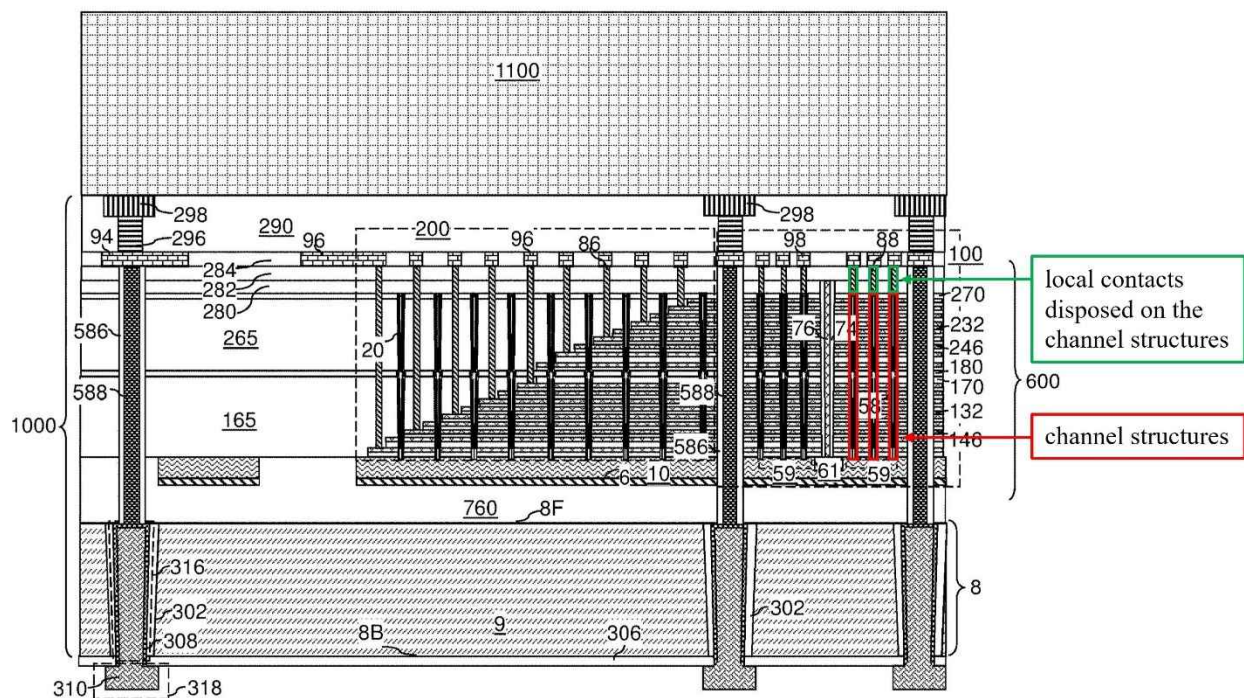


FIG. 11

Mushiga, Figure 11; *id.*, 10:21-27 (“[D]rain contact via structures 88 ... provide electrical contact to the drain regions located in an upper portion of each memory stack structure 58.”); Lee, ¶ 198.

b. [15.G.ii] “local contacts disposed on ... the slit structures”

As noted for limitation [15.D.ii], above, Mushiga’s “backside contact via structures 76” are *slit structures*. Mushiga does not expressly disclose *local contacts* on *the slit structures* (“backside contact via structures 76”), but a POSITA would have understood Mushiga to do so. Lee, ¶¶ 199-203.

Mushiga notes “backside contact via structures 76” serve as the source connection for “memory stack structures 58.” Mushiga, 10:16-18 (“backside contact via structure 76 ... provide electrical contact to source region 61.”).

The function of a source connection in a three-dimensional memory device would have been well known to a POSITA. Lee, ¶¶ 200-201. In 3D NAND memory devices, as in electronic devices generally, electric current flows from a higher voltage to lower voltage, such as ground. *Id.* More specifically, in 3D NAND memory devices, current flows from the “drain” of the device to the “source” of the device, which is connected to ground.¹¹ Ex. 1015, 150 (“the Source Line ... plays the role of the ‘local ground’ for each memory cell.”); Lee ¶ 201.

¹¹ A full discussion of the terms “drain” and “source” is beyond the scope of the present Petition, but a POSITA would have understood that the drain and source of a memory stack structure would need to be connected to an appropriate voltage source and ground, respectively. Lee, ¶¶ 200-201.

By the filing date of the 378 Patent, a POSITA would have known that a “source line” is used to provide a source connection to the memory stacks in a 3D NAND memory device. For example, in the well-known BiCS architecture, a “source line” (abbreviated “SL”) is disposed in the substrate underneath the memory stack:

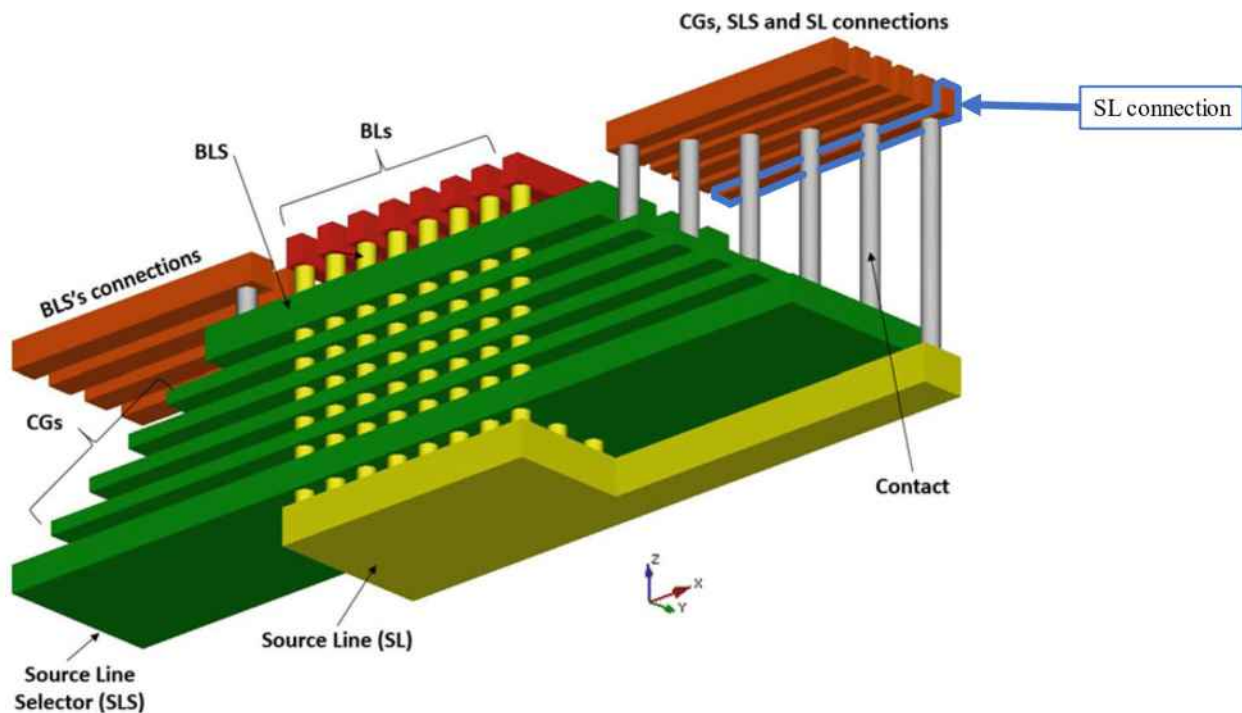


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

Ex. 1015, 110 (Figure 4.14); Ex. 1016, 275, 288; Lee, ¶ 201. The “source line,” in turn, connects to a source line *contact* that extends vertically to a source line *connection*. The source line connection, which carries a ground signal to the source line contact, is in the 378 Patent’s parlance *a local contact*. Lee, ¶ 202. Thus, a POSITA would have known of *local contacts* (source line connections) that provide a source connection to a 3D memory array. *Id.*

It would have been useful and obvious to use *local contacts* (source line connections) *disposed on the slit structures* (“backside contact via structures 76”) to connect “backside contact via structures 76” to a top-level source connection. Lee, ¶ 203 As noted above, Mushiga’s “backside contact via structures 76” serve as the source connection for “memory stack structures 58.” Mushiga, 10:10-18. But without some link to a source connection, Mushiga’s “backside contact via structures 76” would be electrically non-functional. Thus, a POSITA would have understood, or at least found it obvious, that Mushiga’s NAND memory device include *local contacts* (source line connections) *disposed on* (in contact with and extending above) *the slit structures* (“backside contact via structures 76”). *Id.*

To the extent that PO argues Mushiga does not disclose source line connections *disposed on the slit structures* (“backside contact via structures 76”), PO would be incorrect (see above), but it would at the very least have been obvious in view of the knowledge of a POSITA. As described above, a POSITA would have known source line connections could be used to connect “backside contact via structures 76” to the device’s top-level source connection. And it would have been desirable to do so as to enable Mushiga’s “backside contact via structures 76” to serve their express purpose of being source connections. Mushiga, 10:17-18; Lee, ¶ 203. The use of *local contacts* (source line connections) *disposed on the slit structures* (“backside contact via structures 76”) thus represents no more than the

use of a known element (source line connections) to improve a similar device (Mushiga's 3D memory device) in the same way (provide an electrical link to the top-level source connection). *Id.*

9. [15.H] “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.”

Mushiga discloses *through array contacts (TACs)* (the combination of each “through-memory-level via structure 588” and its adjoining “through-substrate via structure 316”) *extending vertically through the dielectric structure* (elements 760, 165, 180, 265, 586) *and the isolation structure* (elements 302, 306):

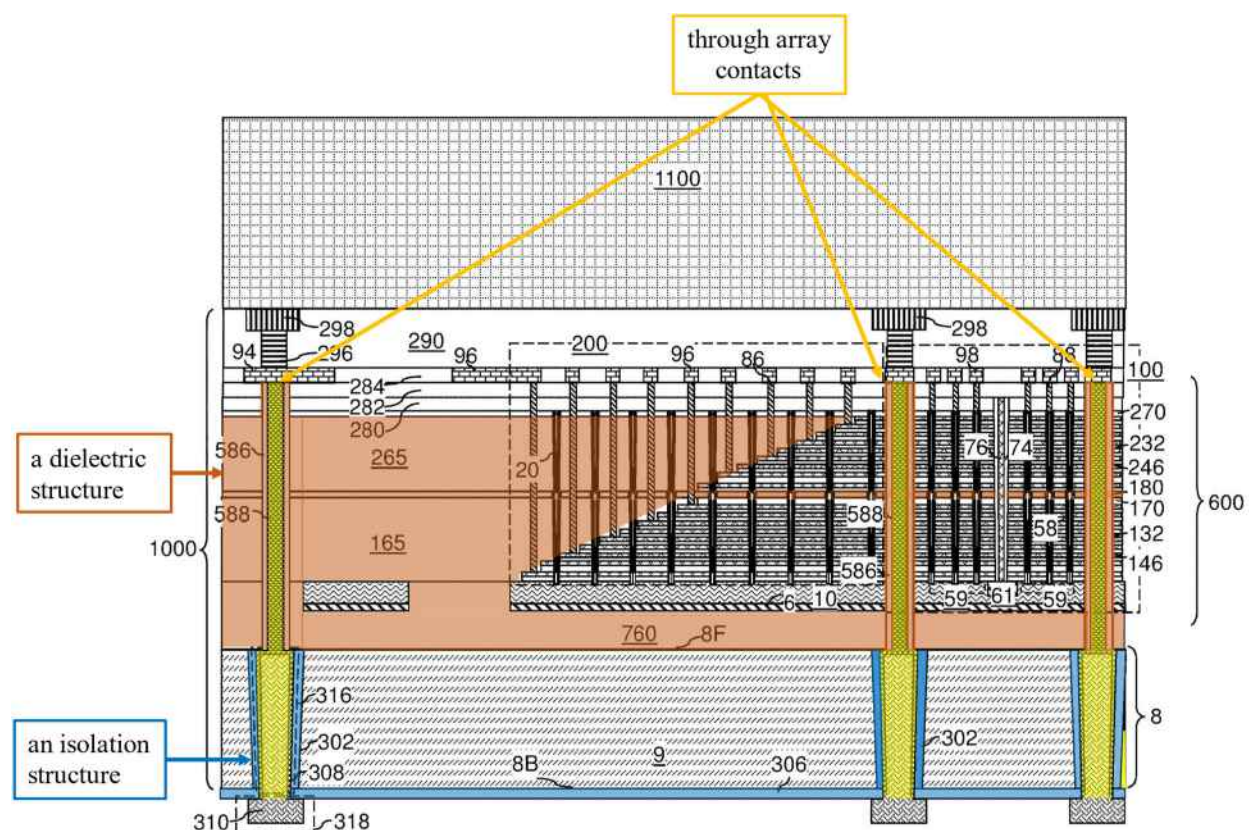


FIG. 11

Mushiga, Figure 11; *id.*, 10:31-57; Lee, ¶ 204.

B. Claim 16:

1. [16] “The 3D memory device of claim 15, wherein the dielectric structure abuts a sidewall of each TAC of the TACs.”

Mushiga Fig. 11 discloses *the dielectric structure* (elements 760, 165, 180, 265, 586) *abuts a sidewall of each TAC of the TACs* (a sidewall of each of the “through-memory-level via structures 588”):

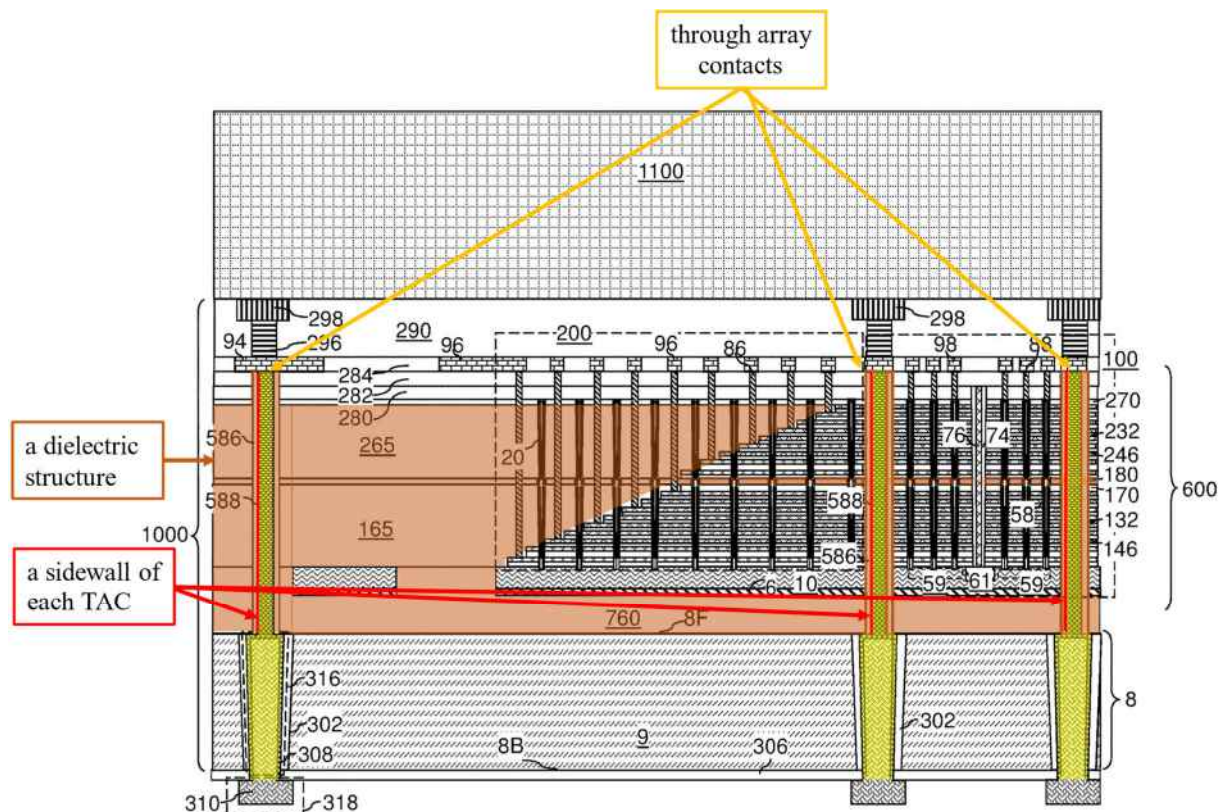


FIG. 11

Mushiga, Figure 11; *id.*, 10:31-57; Lee, ¶ 205.

C. Claim 17:

1. [17] “The 3D memory device of claim 15, wherein the dielectric structure comprises a through array contact region of the 3D memory device.”

As shown below, Mushiga discloses *the dielectric structure* (elements 760, 165, 180, 265, 586) *comprises a through array contact region of the 3D memory device*:

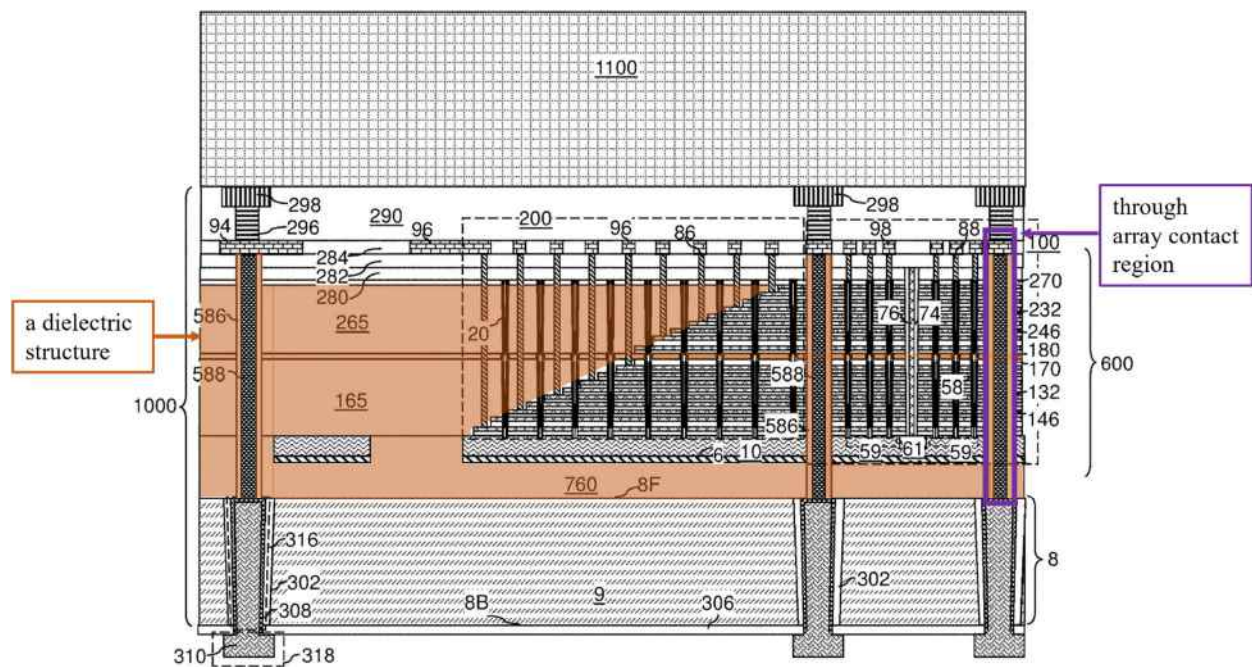


FIG. 11

Mushiga, Figure 11; *id.*, 10:31-57; Lee, ¶ 206. Mushiga’s dielectric structure (elements 760, 165, 180, 265, 586) *comprises a through array contact region of the 3D memory device* because that is the area through which part of each TAC (“through-memory-level via structure 588”) extends through the dielectric structure (elements 760, 165, 180, 265, 586).

D. Claim 19:

1. [19] “The 3D memory device of claim 15, wherein the dielectric material comprises silicon oxide.”

As explained above, Mushiga’s *dielectric structure* comprises elements 760, 165, 180, 265, and 586. Mushiga expressly states one element of its dielectric structure, “insulating material layer 760,” may consist of silicon oxide. *E.g.*, Mushiga, 9:8-10. Mushiga thus teaches this limitation.

If the claim requires that all elements of the dielectric structure comprises silicon oxide (it does not), Mushiga nevertheless renders the claim obvious. Aside from “insulating material layer 760,” Mushiga does not expressly disclose that the other elements of its dielectric structure (elements 165, 180, 265, 586) are formed of silicon oxide. However, forming these elements out of silicon oxide would have been obvious to a POSITA. At the 378 Patent’s priority date, and for many decades prior, silicon oxide was known to be a dielectric and insulating material. Lee, ¶ 208. Indeed, Mushiga notes “silicon oxide” is “an electrically insulating material.” Mushiga, 8:8-10. As noted for limitation [15.C.i], above, Mushiga describes each of elements 165, 180, 265, and 586 as being “insulating” or “dielectric.” Section X.A.4.a. Thus, it would have been obvious to a POSITA to use silicon oxide to construct each of elements 165, 180, 265, and 586. Ex. 1019 (U.S. Pat. No. 9,293,348), 2:61-65; Ex. 1020 (U.S. Pat. No. 10,103,169, Figs. 11-12, 3:1-8

(discussing “formation of a conformal silicon oxide liner” in 3D-NAND); Ex. 1021 (U.S. Pat. No. 8,697,519), 7:30-40; Lee, ¶¶ 207-208.

E. Claim 20:

1. [20] “The 3D memory device of claim 15, wherein the TACs comprise a conductive material.”

Mushiga discloses this limitation. Mushiga explains: “At least one conductive material, such as a combination of a metallic liner and a metal fill material (e.g., tungsten) can be deposited in remaining volumes of the through-memory-level via cavities to form through-memory-level via structures 588.” Mushiga, 10:42-46. “The first through-substrate via structure 316 includes vertically extending portions of the metallic liner 308L and the metal fill material layer 310L that are embedded within the first semiconductor substrate 8 and the backside insulating layer 306.” *Id.*, 13:25-29. As was well known in the art, metal is a conductive material. Mushiga thus teaches that multiple components of *the TACs* (“through-memory-level via structure 588” and “through-substrate via structure 316”) each *comprise a conductive material*. Lee, ¶ 209.

XI. GROUND 3: MUSHIGA AND MAKALA IN VIEW OF THE KNOWLEDGE OF A POSITA

A. Claim 15

This Ground relies solely on Mushiga’s disclosure for all limitations of claim 15 except limitation [15.G.ii], *local contacts disposed on the slit structures*. See

generally Part X, above; Lee, ¶¶ 210-219. For the reasons below, Mushiga and Makala in view of the knowledge of a POSITA also disclose limitation [15.G.ii].

Makala discloses a “three-dimensional memory device” nearly identical to Mushiga’s “first semiconductor devices 600.” Lee, ¶ 211.

- Just as Mushiga discloses *an alternating conductor/dielectric layer stack* (“alternating stack of insulating layers (132, 232) and electrically conductive layers (146, 246)”), so too does Makala (“alternating stack (132, 146, 232, 246)”). Makala, 32:8-30; Lee, ¶ 211.
- Just as Mushiga discloses *channel structures* (“memory stack structures 58”), so too does Makala (“memory stack structures 55”). Makala, 29:4-8; Lee, ¶ 212.
- Just as Mushiga discloses *a staircase structure* (“stepped surfaces”), so too does Makala (“stepped surfaces”). Makala, 19:35-38, 22:48-53; Lee, ¶ 213.
- Just as Mushiga discloses *a word line contact* (“word line contact via structures 86”), so too does Makala (“word line contact via structures 86”). Makala, 33:47-49; Lee, ¶ 214.
- Just as Mushiga discloses *slit structures* (“backside contact via structures 76”), so does Makala (“laterally-elongated contact via structures 76”). Makala, 32:53-33:3; Lee, ¶ 215.

Makala discloses *local contacts* (“source connection via structures 91”) *disposed on* (in contact with and extending above) *the slit structures* (“laterally elongated contact via structures 76”):

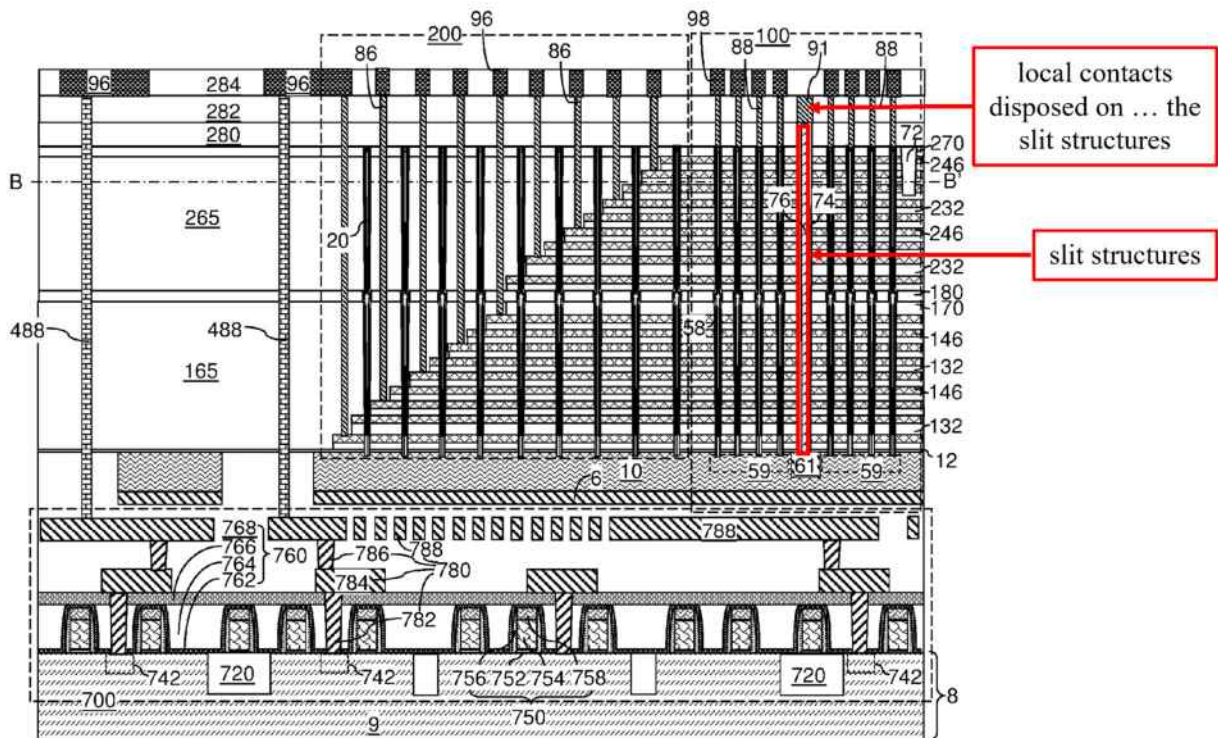


FIG. 16

Makala, Figure 16; Lee, ¶ 216. “Additional line level metal interconnect structures that are not expressly illustrated can include source connection line structures that contact the source connection via structures 91 to provide electrically conductive paths for biasing the source region 61 through the laterally-elongated contact via structures 76.” Makala, 34:27-33; *see also id.*, 33:40-42.

It would have been obvious to integrate Makala’s teaching of “source connection via structures 91” with Mushiga’s memory device. Mushiga’s “backside

contact via structures 76,” like Makala’s “laterally-elongated contact via structures 76,” serve as the source connection for the memory stack. Mushiga, 10:16-18; Lee, ¶ 218. While Mushiga implies how its “via structures 76” receive their source connection, Makala expressly teaches: its “via structures 76” connect to “source connection via structures 91,” which in turn are connected to “source connection line structures.” Makala, 34:27-33.

A POSITA would have been motivated to incorporate these teachings from Makala because a POSITA would have understood that, to be electrically operative, Mushiga’s “via structures 76” would need to be connected to a source line. Lee, ¶ 219. Makala’s “source connection via structures 91” expressly provide for doing so. And a POSITA would have had a reasonable expectation of success in integrating Makala’s teaching of “source connection via structures 91” with Mushiga’s device because, as discussed above, Makala’s three-dimensional memory device” is nearly identical to Mushiga’s “first semiconductor devices 600.” *Id.*

B. Claims 16-17 and 19-20

Mushiga and Makala in view of the knowledge of a POSITA renders obvious claims 16-17 and 19-20 the reasons explained above in Sections X.B-X.E. Lee, ¶ 220.

XII. SECONDARY CONSIDERATIONS

There is no evidence in the prosecution history of this or any related application or patent that any arguments regarding secondary considerations exist.

XIII. CONCLUSION

Petitioner respectfully requests that the Board enter a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: April 30, 2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,823 words.

Dated: April 30, 2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on April 30, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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