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Bibliographic data: CN105826323 (A) — 2016-08-03**Memory element and making method thereof****Inventor(s):** LAI SHENGZHI; CHEN WEICHEN ± (赖升志; 陈威臣)**Applicant(s):** MACRONIX INT CO LTD ± (旺宏电子股份有限公司)**Classification:** - international: **H01L27/115**
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The invention discloses a memory element and a making method thereof. The memory element comprises a first conductive strip, a first storage layer, a first conductive column, a first dielectric layer, and a first conductive plug. The first conductive strip extends along a first direction. The first storage layer extends along a second direction, is adjacent to the first conductive strip, and overlaps with the first conductive strip to define a first storage area on the first storage layer. The first conductive column extends along the second direction, and is adjacent to and overlaps with the first storage area. The first dielectric layer extends along the second direction, and is adjacent to the first conductive strip, the first storage layer and the first conductive column. The first conductive plug extends along the second direction, at least partially overlaps with the first conductive strip, and is electrically isolated from the first conductive strip, the first storage layer and the first conductive column through the first dielectric layer.

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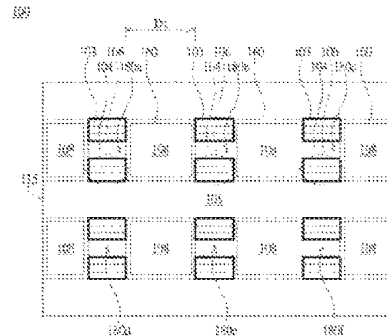
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(54) 发明名称

存储器元件及其制作方法

(57) 摘要

本发明公开了一种存储器元件及其制作方法,该存储器元件包括:第一导电条带、第一存储层、第一导电柱状体、第一介电层以及第一导电插塞。第一导电条带沿第一方向延伸。第一存储层沿第二方向延伸,并邻接第一导电条带,且与第一导电条带重叠,而在第一存储层上定义出第一存储区。第一导电柱状体沿第二方向延伸,邻接且与第一存储区重叠。第一介电层沿第二方向延伸,并邻接第一导电条带、第一存储层和第一导电柱状体。第一导电插塞,沿第二方向延伸,并与第一导电条带至少部分重叠,且通过第一介电层而与第一导电条带、第一存储层和第一导电柱状体电性隔离。



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1. 一种存储器元件,包括:
 - 第一导电条带,沿一第一方向延伸;
 - 第一存储层,沿一第二方向延伸,与该第一导电条带重叠,并在该第一存储层与该第一导电条带的重叠处定义出一第一存储区;
 - 第一导电柱状体,沿该第二方向延伸,并邻接该第一存储层,且与该第一存储区重叠;
 - 第一介电层,沿该第二方向延伸,并邻接该第一导电条带、该第一存储层和该第一导电柱状体;以及
 - 第一导电插塞,沿该第二方向延伸,并与该第一导电条带至少部分重叠,且通过该第一介电层而与该第一导电条带、该第一存储层和该第一导电柱状体电性隔离。
2. 根据权利要求 1 所述的存储器元件,更包括:
 - 第二介电层,沿该第二方向延伸,并邻接该第一导电条带、该第一存储层和该第一导电柱状体,且使该第一导电柱状体位于该第一介电层与该第二介电层之间;以及
 - 第二导电插塞,沿该第二方向延伸,并通过该第二介电层与该第一导电条带、该第一存储层和该第一导电柱状体电性隔离。
3. 根据权利要求 2 所述的存储器元件,更包括:
 - 第二存储层,沿该第二方向延伸,并与该第一导电条带重叠,而在该第二存储层与该第一导电条带重叠处定义出一第二存储区,且该第二存储区和该第一存储区之间,具有平行该第一方向的一距离;以及
 - 第二导电柱状体,沿该第二方向延伸,并邻接且与该第二存储区重叠;其中,该第一导电插塞与该第二导电柱状体之间是通过该第一介电层电性隔离。
4. 根据权利要求 3 所述的存储器元件,更包括:
 - 第二导电条带,沿该第一方向延伸,并与该第一存储层和该第二存储层重叠,分别定义出一第三存储区和一第四存储区,且该第一导电柱状体和该第二导电柱状体分别与该第三存储区和该第四存储区重叠;以及
 - 绝缘层,沿该第一方向延伸,并且位于该第一导电条带与该第二导电条带之间。
5. 根据权利要求 4 所述的存储器元件,更包括:
 - 第一字线,沿一第三方向延伸,并与该第一导电柱状体电性接触;以及
 - 第二字线,沿该第三方向延伸,并与该第二导电柱状体电性接触;
 - 其中,该第一导电插塞位于该第一字线和该第二字线之间,且与该第一字线和该第二字线电性隔离。
6. 根据权利要求 5 所述的存储器元件,更包括:
 - 第一介电插塞,位于该第一导电插塞上,并与该第一介电层和该第一导电插塞接触;
 - 以及
 - 第二介电插塞,位于该第二导电插塞上,并与该第二介电层和该第二导电插塞接触。
7. 根据权利要求 5 所述的存储器元件,更包括:
 - 多个脊状多层叠层 (ridged-shaped multi-layer stacks) 位于一基材上,沿着该第一方向延伸,其中每一这些脊状多层叠层,都包括一部分的该第一导电条带、该绝缘层和该第二导电条带;

该第一存储层和该第二存储层,分别位于这些脊状多层叠层所定义的一沟槽 (trench) 中,并且覆盖于该沟槽的一侧壁;

该第一导电柱状体和该第二导电柱状体,位于这些沟槽之中,分别覆盖这些第一存储层和该第二存储层;以及

该第一字线和该第二字线,位于这些脊状多层叠层的顶部。

8. 根据权利要求 1 所述的存储器元件,更包括:

一第二存储层,沿该第二方向延伸,与该第一导电条带重叠,而在该第二存储层与该第一导电条带重叠处定义出一有源区;以及

一第二导电柱状体,沿该第二方向延伸,并与该有源区重叠,且与一串行选择线 (String Select Line, SSL) 连接。

9. 根据权利要求 1 所述的存储器元件,更包括:

一第二存储层,沿该第二方向延伸,与该第一导电条带重叠,而在该第二存储层与该第一导电条带重叠处定义出一有源区;以及

一第二导电柱状体,沿该第二方向延伸,并与该有源区重叠,且与一接地选择线 (Ground Select Line, GSL) 连接。

10. 一种存储器元件的制作方法,包括:

于一基材上形成一多层叠层结构 (multi-layer stack);

图案化该多层叠层结构,以形成多个脊状多层叠层;其中,每一这些脊状多层叠层至少包括一导电条带沿着一第一方向延伸;

于这些脊状多层叠层之间的至少一沟槽的一底部和侧壁上形成一存储材料层;

于这些脊状多层叠层上形成一导电材料层,并填满该沟槽;

图案化该导电材料层和该存储材料层,以于该沟槽之中形成多个通孔,将一部分该基材以及该导电条带暴露于外;其中,图案化的该导电材料层包括至少一导电柱状体,位于该沟槽中;图案化的该存储材料层包括至少一存储层,位于该沟槽中;且在该存储层与该导电条带重叠处定义出一存储区;

于这些通孔的侧壁以及暴露于外的该基材上形成一介电层;

形成多个导电插塞,分别部分地填充这些通孔,并且使这些导电插塞至少与该导电条带部分重叠;

于这些导电插塞上形成多个介电插塞,以填满这些通孔;以及

再图案化该导电材料层,以于这些脊状多层叠层的顶部形成至少一字线,沿一第三方向延伸,并且与该导电柱状体电性接触。

存储器元件及其制作方法

技术领域

[0001] 本发明是有关于一种非易失性存储器元件及其制作方法。特别是有关于一种立体 (Three-Dimension, 3D) 非易失性存储器元件及其制作方法。

背景技术

[0002] 传统非易失性存储器 (non-volatile memory) 元件, 例如 NAND 闪存元件, 一般会使用单晶硅或多晶硅材质的导电条带 (stripe) 来串接位于位线与源极线之间的多个存储单元。而为了降低存储单元之间的串接电阻 (series resistance), 通常会对串连存储单元之间的单晶硅或多晶硅导电条带进行离子注入掺杂。然而, 在制作具有三维多层存储器阵列的 NAND 闪存元件时, 由于多晶硅或单晶外延硅导电条带会与多个介电层叠层形成一多层叠结构, 存储单元则位于多层叠结构的垂直面上; 要在存储单元之间的多晶硅导电条带中注入离子掺杂, 不仅会使工艺步骤复杂化, 增加工艺的热预算 (thermal budget), 且离子掺杂的扩散控制不易, 容易会干扰存储器元件的读取、编程及擦除 (program/erase), 进而导致元件失效。

[0003] 因此, 有需要提供一种更先进的存储器元件及其制作方法, 以改善已知技术所面临的问题。

发明内容

[0004] 根据本说明书的一实施例, 提供一种存储器元件, 其包括: 第一导电条带、第一存储层、第一导电柱状体、第一介电层以及第一导电插塞。第一导电条带沿第一方向延伸。第一存储层沿第二方向延伸, 并与第一导电条带重叠, 而在第一存储层与第一导电条带重叠处定义出第一存储区。第一导电柱状体沿第二方向延伸, 并邻接第一存储层且与第一存储区重叠。第一介电层沿第二方向延伸, 并邻接第一导电条带、第一存储层和第一导电柱状体。第一导电插塞, 沿第二方向延伸, 并与第一导电条带至少部分重叠, 且通过第一介电层而与第一导电条带、第一存储层和第一导电柱状体电性隔离。

[0005] 根据本说明书的另一实施例, 提供一种存储器元件的制作方法, 包括下述步骤: 首先在基材的表面上形成多层叠层 (multi-layer stack) 结构。再图案化多层叠层结构, 以形成多个脊状多层叠层 (ridge-shaped stacks), 使每一个脊状多层叠层至少包括一个沿着第一方向延伸的导电条带。然后, 于这些脊状多层叠层间的至少一个沟槽的底部和侧壁上形成存储材料层。再于这些脊状多层叠层上形成导电材料层, 并填满沟槽。接着, 图案化导电材料层和存储材料层, 以于沟槽之中形成多个通孔, 藉以将一部分的基材和导电条带暴露于外。其中, 图案化的存储材料层至少包括一个位于沟槽中的存储层; 图案化的导电材料层至少包括一个位于沟槽中的导电柱状体, 且在此存储层与导电条带重叠处定义出一存储区。之后, 于通孔的侧壁以及暴露于外的基材上形成介电层。再形成多个导电插塞, 分别部分地填充这些通孔, 并且使导电插塞至少与导电条带部分重叠。后续, 于这些导电插塞上形成多个介电插塞, 以填满这些通孔。然后, 再次图案化导电材料层, 以于脊状多层叠层的

顶部形成至少一条字线,沿第三方向延伸,并且与导电柱状体电性接触。

[0006] 根据上述实施例,本发明是在提供一种立体存储器元件及其制作方法。立体存储器元件至少包括多个阶层;每个阶层包含多个存储单元,并通过沿第一方向延伸的导电条带加以串连。每一个存储单元都包括沿第二方向延伸的存储层和导电柱状体。其中,存储层邻接导电条带,且在与导电条带重叠的位置,定义出存储区。导电柱状体邻接存储层,且与存储区重叠。相邻两存储单元的导电柱状体之间具有一个平行导电柱状体的导电插塞,与串接两存储单元的导电条带至少部分重叠,并且通过介电层将导电插塞分别与相邻两存储单元以及导电条带电性隔离。

[0007] 由于导电插塞与介电层的配置方式,使导电插塞具有浮置栅的功能,当立体存储器元件进行操作时,导电插塞会因导电柱状体导通而具有一感应电压,可在串连相邻两存储单元的导电条带中形成反转层,有助于降低两存储单元之间的串接电阻。因此,不需对串连相邻两存储单元的导电条带进行离子注入掺杂,即可降低存储单元之间的串接电阻。同时可解决已知技术因为采用离子注入掺杂工艺所导致的工艺步骤繁复、热预算增加及干扰存储器元件读取、编程及擦除的问题。

附图说明

[0008] 为了对本发明的上述实施例及其他目的、特征和优点能更明显易懂,特举数个较佳实施例,并配合所附图式,作详细说明如下:

[0009] 图 1A 是根据本发明的一实施例所绘示的多层叠层结构的结构透视图;

[0010] 图 1B 是根据图 1A 所绘示的多层叠层结构的结构上视图;

[0011] 图 2A 是绘示对图 1A 的多层叠层结构进行图案化工艺之后的结构透视图;

[0012] 图 2B 是根据图 2A 所绘示的结构上视图;

[0013] 图 3A 是绘示依序在图 2A 的结构上形成存储材料层和导电材料层之后的结构透视图;

[0014] 图 3B 是根据图 3A 所绘示的结构上视图;

[0015] 图 4A 是绘示对图 3B 的导电材料层和存储材料层进行图案化之后的结构上视图;

[0016] 图 4B 是沿着图 4A 的切线 S41 所绘示的部分结构透视图;

[0017] 图 4C 是沿着图 4A 的切线 S42 所绘示的部分结构透视图;

[0018] 图 5A 是绘示在图 4B 的结构中形成介电层之后的结构上视图;

[0019] 图 5B 是沿着图 5A 的切线 S51 所绘示的部分结构透视图;

[0020] 图 5C 是沿着图 5A 的切线 S52 所绘示的部分结构透视图;

[0021] 图 6A 是绘示在图 5A 的结构中形成多个导电插塞之后的结构上视图;

[0022] 图 6B 是沿着图 6A 的切线 S61 所绘示的部分结构透视图;

[0023] 图 6C 是沿着图 6A 的切线 S62 所绘示的部分结构透视图;

[0024] 图 7A 是绘示在图 6A 的结构中形成多个介电插塞之后的结构上视图;

[0025] 图 7B 是沿着图 7A 的切线 S71 所绘示的部分结构透视图;

[0026] 图 7C 是沿着图 7A 的切线 S72 所绘示的部分结构透视图;

[0027] 图 8A 是绘示在图 7A 的结构中形成多条字线之后的结构上视图;

[0028] 图 8B 是沿着图 8A 的切线 S81 所绘示的部分结构透视图;

[0029] 图 8C 是沿着图 8A 的切线 S82 所绘示的部分结构透视图；

[0030] 图 9 是沿着立体存储器元件的 X-Y 截面所绘示的部分阶层结构剖面示意图。

[0031] 【符号说明】

[0032] 100:立体存储器元件 101:基材

[0033] 102:通孔 103:存储层

[0034] 104:导电柱状体 105:导电条带

[0035] 106:存储区 108:导电插塞

[0036] 109:介电插塞 110:多层叠层结构

[0037] 110a:沟槽 110b:脊状多层叠层

[0038] 110c:沟槽的侧壁 111-118:导电层

[0039] 121-128:绝缘层 130:图案化硬掩模层

[0040] 130a:沟槽开口 140:存储材料层

[0041] 150:导电材料层 160:介电层

[0042] 170:字线 180a-180f:存储单元

[0043] S51、S52、S61 S62、S71、S72、S81、S82、S91 和 S92:切线

具体实施方式

[0044] 本发明提供一种立体存储器元件及其制作方法,可在不需对串连两相邻存储单元的导电条带进行离子注入掺杂的情况下,降低存储单元之间的串接电阻。为了对本发明的上述实施例及其他目的、特征和优点能更明显易懂,下文特举数立体存储器元件及其制作方法作为较佳实施例,并配合所附图式作详细说明。

[0045] 但必须注意的是,这些特定的实施案例与方法,并非用以限定本发明。本发明仍可采用其他特征、元件、方法及参数来加以实施。较佳实施例的提出,仅是用以例示本发明的技术特征,并非用以限定本发明的权利要求范围。该技术领域中具有通常知识者,可根据以下说明书的描述,在不脱离本发明的精神范围内,作均等的修饰与变化。在不同实施例与图式之中,相同的元件,将以相同的元件符号加以表示。

[0046] 制作立体存储器元件 100 的方法,包括下述步骤:首先在基材 101 的表面上形成多层叠层结构 (multi-layer stack) 110。请参照图 1A 和图 1B,图 1A 是根据本发明的一实施例所绘示的多层叠层结构 110 的结构透视图。图 1B 是根据图 1A 所绘示的多层叠层结构 110 的结构上视图。在本发明的一些实施例中,多层叠层结构 110 是形成于基材 101 上。多层叠层结构 110 包括多个导电层 111-118 以及多个绝缘层 121-128。在本实施例中,绝缘层 121-128 与导电层 111-118 是沿着图 1A 所绘示的 Z 轴方向,在基材 101 上彼此交错叠层,使导电层 111 位于多层叠层结构 110 的底层,而绝缘层 128 位于多层叠层结构 110 的顶层。

[0047] 导电层 111-118 可以由导电半导体材料,例如掺杂有磷或锶的 n 型多晶硅,或 n 型外延单晶硅,所构成。此外,导电层 111-118 也可以由掺杂有硼的 p 型多晶硅或 p 型外延单晶硅所构成。另一方面,导电层 111-118 也可以由无掺杂的半导体材料,例如无掺杂的多晶硅或外延单晶硅,所构成。在本实施例中,导电层 111-118 是由无掺杂多晶硅所构成。无掺杂多晶硅的晶粒尺寸 (grain size),较佳可以实质介于 400 纳米 (nm) 到 600 纳米之间;无掺杂多晶硅的片电阻 (sheet resistance) 可以实质介于 10^7ohm/square 到 10^{11}ohm/square

之间。导电层 111-118 每一者的厚度可以实质介于 5 纳米到 40 纳米之间。

[0048] 绝缘层 121-128 可以由介电材料,例如硅氧化物 (oxide)、硅氮化物 (nitride)、硅氮氧化物 (oxynitride)、硅酸盐 (silicate) 或其他材料,所构成。每一绝缘层 121-128 的厚度可以实质介于 10 纳米到 50 纳米之间。在本发明的一些实施例中,导电层 111-118 和绝缘层 121-128 可通过,例如低压化学气相沉积 (Low Pressure Chemical Vapor Deposition, LPCVD) 工艺,制作而成。

[0049] 接着,对多层叠层结构 110 进行一图案化工艺,以形成多个脊状多层叠层 110b。请参照图 2A 和图 2B,图 2A 是绘示对图 1A 的多层叠层结构 110 进行图案化工艺之后的结构透视图。图 2B 是根据图 2A 所绘示的结构上视图。在本发明的一些实施例中,多层叠层结构 110 的图案化工艺,包括先在多层叠层结构 110 顶部形成一图案化硬掩模层 130。在本实施例中,图案化硬掩模层 130 是形成于绝缘层 128 的顶部表面。其中,图案化硬掩模层 130 包括多个沿着 Z 轴方向向下延伸的沟槽开口 130a。这些沟槽开口 130a 的长轴沿着 X 轴方向延伸,并将一部份的绝缘层 128 的顶部表面暴露于外。

[0050] 在本发明的一些实施例中,图案化硬掩模层 130 可以是一种通过化学气相沉积 (Chemical Vapor Deposition, CVD) 工艺,在多层叠层结构 110 的顶部表面所形成的先进图案化膜 (Advanced Patterning Film, APF)。这些沟槽开口 130a,则是通过光刻 (photolithography) 工艺来移除一部分的先进图案化膜所形成。在本实施例中,每一沟槽开口 130a 都具有相同尺寸,且每一沟槽开口 130a 皆为长方孔型式 (但不以此为限)。

[0051] 然后,以图案化硬掩模层 130 为刻蚀掩模,通过非等向刻蚀工艺 (anisotropic etching process),例如反应离子刻蚀 (Reactive Ion Etching, RIE) 工艺,对多层叠层结构 110 进行刻蚀。藉以在多层叠层结构之中形成沿着 Z 轴方向延伸的沟槽 110a,将多层叠层结构 110 分割成多个脊状多层叠层 110b,并将基材 101 的部分区域经由沟槽 110a 曝露于外。在本实施例中,每一脊状多层叠层 110b 都包含一部份条状的导电层 111-118,可作为串连立体存储器元件 100 中位于同一脊状多层叠层 110b 的同一阶层的多个存储单元的导电条带 105。

[0052] 接着,请参照图 3A 和图 3B,图 3A 是绘示依序在图 2A 的结构上形成存储材料层 140 和导电材料层 150 之后的结构透视图。图 3B 是根据图 3A 所绘示的结构上视图。在本发明的一些实施例中,存储材料层 140 可以通过低压化学气相沉积工艺所制作而成。存储层 140 可以由包含氧化硅 (silicon oxide) 层、氮化硅 (silicon nitride) 层和氧化硅层的复合层 (即,ONO 层) 所构成。在本实施例中,存储材料层 140 覆盖位于脊状叠层 110 的顶部以及沟槽 110a 的底部 (即被沟槽 110a 暴露于外的基材 101) 和侧壁 110c 上。

[0053] 在形成存储层 140 之后,再于这些脊状多层叠层 110b 上形成导电材料层 150,覆盖存储材料层 140,并填满沟槽 110a。在本发明的一些实施例中,可以通过低压化学气相沉积工艺来制作导电材料层 150。构成导电材料层 150 的材质,可以包含掺杂有磷或砷的 n 型多晶硅 (或 n 型外延单晶硅)、掺杂有硼的 p 型多晶硅 (或 p 型外延单晶硅)、无掺杂的多晶硅、金属硅化物 (silicides),例如硅化钛 (TiSi)、硅化钴 (CoSi) 或硅锗 (SiGe)、氧化物半导体 (oxide semiconductors),例如氧化镓锌 (InZnO) 或氧化铟镓锌 (InGaZnO)、金属,例如铝 (Al)、铜 (Cu)、钨 (W)、钛 (Ti)、钴 (Co)、镍 (Ni)、氮化钛 (TiN)、氮化钽 (TaN) 或氮化钽铝 (TaAlN),或两种或多种上述材质的组合物所构成。

[0054] 接着,图案化导电材料层 150 和存储材料层 140,于沟槽 110a 之中形成多个通孔 102,藉以将一部分的基材 101 和导电条带 105 暴露于外,并分别在图案化的导电材料层 150 以及图案化的存储材料层 140 之中,定义出多个存储层 103 和多个导电柱状体 104。请参照图 4A、图 4B 和图 4C,图 4A 是绘示对图 3B 的导电材料层 150 和存储材料层 140 进行图案化之后的结构上视图。图 4B 是沿着图 4A 的切线 S41 所绘示的部分结构透视图。图 4C 是沿着图 4A 的切线 S42 所绘示的部分结构透视图。

[0055] 在本发明的一些实施例中,通孔 102 是通过非等向刻蚀工艺,例如反应离子刻蚀工艺,移除位于沟槽 110a 之中的一部分导电材料层 150 以及一部分存储材料层 140 所形成,使一部分的导电条带 105 由通孔 102 的侧壁暴露于外;而被余留在沟槽 110a 之中的一部分导电材料层 150 和存储材料层 140,则可分别形成多个沿着 Z 轴方向延伸的条状存储层 103 和多个导电柱状体 104。

[0056] 在本实施例中,每一个存储层 103 与多个位于沟槽 110a 侧壁上,但未被通孔 102 所暴露的一部分导电条带 105 邻接;并且在每一个存储层 103 与每一个导电条带 105 重叠的位置,定义出一个存储区 106。每一个导电柱状体 104 邻接一个存储层 103,并与相对应的存储层 103 的存储区 106 重叠。其中,与同一个存储区 106 重叠的存储层 103、导电条带 105 和导电柱状体 104,三者可构成一个存储单元。而由多个存储层 103、导电条带 105 和导电柱状体 104 所共同定义出来的多个存储单元,可构成立体存储器元件 100 的存储器阵列。

[0057] 但在本发明的另一些实施例中,位于存储器阵列外围的导电条带 105 与存储层 103 重叠所共同定义出的存储区 106,可以作为立体存储器元件 100 的串行选择晶体管或接地选择晶体管(未绘示)的有源区,而与该有源区重叠的对应导电柱状体 104,则与串行的选择线(String Select Line, SSL)或接地选择线(Ground Select Line, GSL)(未绘示)连接。

[0058] 之后,于通孔 102 的侧壁(包含经由通孔 110a 暴露于外的导电条带 105)以及即经由通孔 110a 暴露于外的基材 101 上形成介电层 160。请参照图 5A、图 5B 和图 5C,图 5A 是绘示在图 4A 的结构中形成介电层 160 之后的结构上视图。图 5B 是沿着图 5A 的切线 S51 所绘示的部分结构透视图。图 5C 是沿着图 5A 的切线 S52 所绘示的部分结构透视图。

[0059] 介电层 160 可以通过低压化学气相沉积工艺制作而成。构成介电层 160 的材料,可以和构成绝缘层 121-128 的材料相同。在本发明的一些实施例之中,介电层 160 可以是由包含硅氧化物、硅氮化物、硅氮氧化物、硅酸盐或上述组合的介电材料所构成。在本实施例之中,构成介电层 160 的材料可以包括氧化硅。另外,介电层 160 较佳的厚度介于 3nm 至 10nm 之间。

[0060] 之后,再形成多个导电插塞 108,部分地填充于每一个通孔 102 之中,并且使每一个导电插塞 108 至少与每一个被相对应的通孔 102 暴露于外的导电条带 105 部分重叠。请参照图 6A、图 6B 和图 6C,图 6A 是绘示在图 5A 的结构中形成多个导电插塞 108 之后的结构上视图。图 6B 是沿着图 6A 的切线 S61 所绘示的部分结构透视图。图 6C 是沿着图 6A 的切线 S62 所绘示的部分结构透视图。在本实施例中,为了确保每一个导电插塞 108 至少与每一个导电条带 105 部分重叠,每一个导电插塞 108 必须填充相对应的通孔 102,直到高过最顶层的导电条带 105 的底部。换言之,导电插塞 108 的高度,由基材 101 起算,必须高过导电层 118 的顶部。

[0061] 后续,于这些导电插塞 108 上形成多个介电插塞 109,以填满这些通孔 102,并且与位于通孔 102 侧壁上的介电层 160 连接。请参照图 7A、图 7B 和图 7C,图 7A 是绘示在图 6A 的结构中形成多个介电插塞 109 之后的结构上视图。图 7B 是沿着图 7A 的切线 S71 所绘示的部分结构透视图。图 7C 是沿着图 7A 的切线 S72 所绘示的部分结构透视图。在本发明的一些实施例中,介电插塞 109 可以通过低压化学气相沉积工艺制作而成。构成介电插塞 109 的材料,可以和构成介电层 160 的材料相同。在本发明的一些实施例之中,介电插塞 109 可以由包含硅氧化物、硅氮化物、硅氮氧化物、硅酸盐或上述组合的介电材料所构成。在本实施例之中,构成介电插塞 109 的材料可以包括氧化硅。

[0062] 然后,对位于脊状多层叠层 110b 上方的导电材料层 150 进行再一次的图案化工艺,以于脊状多层叠层 110b 的顶部形成多条字线 170,沿第 Y 轴方向延伸,并且与导电柱状体 104 电性接触。请参照图 8A、图 8B 和图 8C,图 8A 是绘示在图 8A 的结构中形成多条字线 170 之后的结构上视图。图 8B 是沿着图 8A 的切线 S81 所绘示的部分结构透视图。图 8C 是沿着图 8A 的切线 S82 所绘示的部分结构透视图。在本发明的一些实施例之中,多条字线 170 形成于脊状多层叠层 110b 的顶部上;且每一条字线 170 分别与多个导电柱状体 104 电性接触。其中,两相邻的字线 170 之间配置一个导电插塞 108,且导电插塞 108 通过介电层 160 和介电插塞 109 与两相邻的字线 170 电性隔离。

[0063] 后续,再通过一连串后段工艺完成立体存储器元件 100 的制备。立体存储器元件 100 的存储器阵列中,至少包括多个形成于导电层 111-118 上的阶层结构。例如请参照图 9,图 9 是沿着立体存储器元件 100 的 X-Y 截面所绘示的部分阶层结构剖面示意图。在本实施例中,图 9 所绘示的阶层结构是位于导电层 115 上。其中,每一个阶层结构包含多个存储单元,例如存储单元 180a、180b、180c、180d、180e 和 180f;且这些存储单元 180a、180b、180c、180d、180e 和 180f,都经由图案化导电层 115 所形成的导电条带 105 沿 X 轴方向延伸而彼此串接。

[0064] 这些存储单元 180a、180b、180c、180d、180e 和 180f 的每一者都包括一存储层 103 和一导电柱状体 104。其中,存储层 103 沿 Z 轴(垂直 X-Y 平面)方向延伸,并邻接导电条带 105,且在与导电条带 105 重叠的位置,定义出存储区 106。导电柱状体 104 也沿 Z 轴方向延伸,并邻接存储层 103,且与存储区 106 重叠。

[0065] 两相邻的存储单元,例如存储单元 180a 和 180b 之间具有平行 X 轴方向的一段距离 D1。且二者之间配置有一介电层 160 以及一导电插塞 108。其中,介电层 160 沿 Z 轴方向延伸,并分别邻接相邻两相存储单元 180a 和 180b 的导电条带 105、存储层 103 和导电柱状体 104。导电插塞 108 沿 Z 轴方向延伸,并与沿 X 方向延伸,用来串接相邻两相存储单元 180a 和 180b 的一部分导电条带 105 至少部分重叠。介电层 160 夹设于导电插塞 108 与两相存储单元 180a 和 180b 的导电条带 105、存储层 103 和导电柱状体 104 三者之间,使导电插塞 108 可通过介电层 160 而与两相邻存储单元 180a 和 180b 的导电条带 105、存储层 103 和导电柱状体 104 电性隔离。由于,导电插塞 108 与导电条带 105 彼此电性隔离,且至少有一部分相互重叠。因此导电插塞 108 可作为导电条带 105 的浮置栅。当立体存储器元件 100 进行读取或编程操作时,导电插塞 108 会因导电柱状体 104 导通而具有感应电压,可在串连两相邻存储单元 180a 和 180b 的导电条带 105 中形成反转层,有助于而降低存储单元 180a 和 180b 之间的串接电阻。

[0066] 另外值得注意的是,形成于相邻导电层,例如位于导电层 115 下方的导电层 114 上的阶层结构也包含与图 9 所绘示的相同结构。其中,存储单元 180a 中沿 Z 轴方向延伸的存储器层 103 和导电柱状体 104 也会和位于导电层 114 上的导电条带 105 彼此邻接并重叠,进而定义出另一个包含存储区 106 的存储单元(未绘示)。由于,两个存储单元之间被绝缘层 124(未绘示)阻隔,因此二者之间在平行 Z 轴的方向具有一段距离(未绘示)。

[0067] 根据上述实施例,本发明是在提供一种立体存储器元件及其制作方法。立体存储器元件至少包括多个阶层;每个阶层包含多个存储单元,并通过沿第一方向延伸的导电条带加以串连。每一个存储单元都包括沿第二方向延伸的存储层和导电柱状体。其中,存储层邻接导电条带,且在与导电条带重叠的位置,定义出存储区。导电柱状体邻接存储层,且与存储区重叠。相邻两存储单元的导电柱状体之间具有一个平行导电柱状体的导电插塞,与串接两存储单元的导电条带至少部分重叠,并且通过介电层将导电插塞分别与相邻两存储单元以及导电条带电性隔离。

[0068] 由于导电插塞与介电层的配置方式,使导电插塞具有浮置栅的功能,当立体存储器元件进行操作时,导电插塞会因导电柱状体导通而具有一感应电压,可在串连相邻两存储单元的导电条带中形成反转层,有助于降低两存储单元之间的串接电阻。因此,不需对串连相邻两存储单元的导电条带进行离子注入掺杂,即可降低存储单元之间的串接电阻。同时可解决已知技术因为采用离子注入掺杂工艺所导致的工艺步骤繁复、热预算增加及干扰存储器元件读取、编程及擦除的问题。

[0069] 虽然本发明已以较佳实施例揭露如上,然其并非用以限定本发明。本发明所属技术领域中具有通常知识者,在不脱离本发明的精神和范围内,当可作各种的更动与润饰。因此,本发明的保护范围当视随附的权利要求范围所界定的为准。

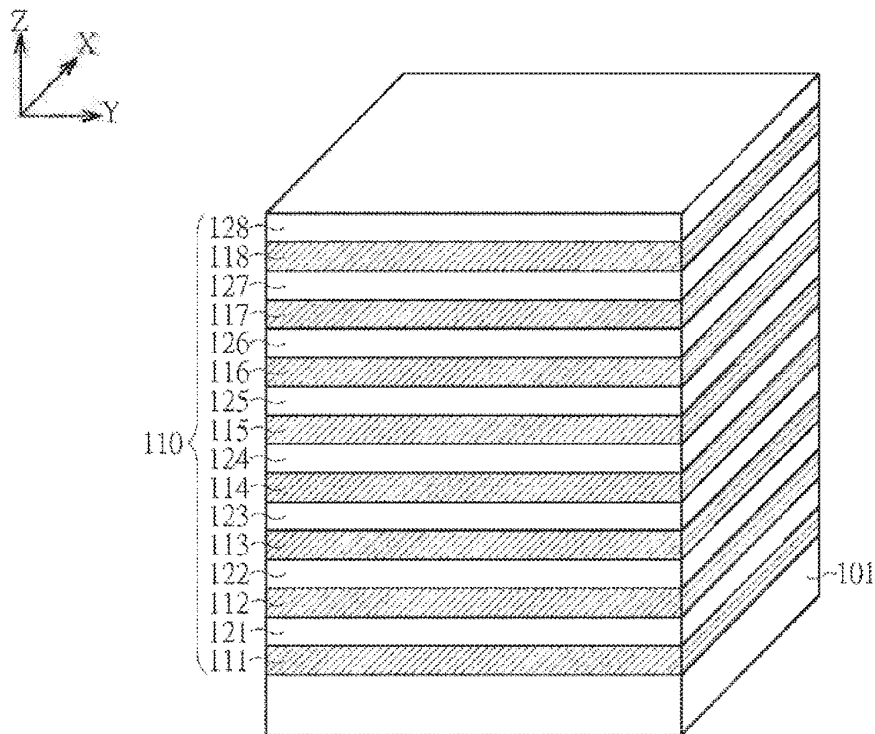


图 1A

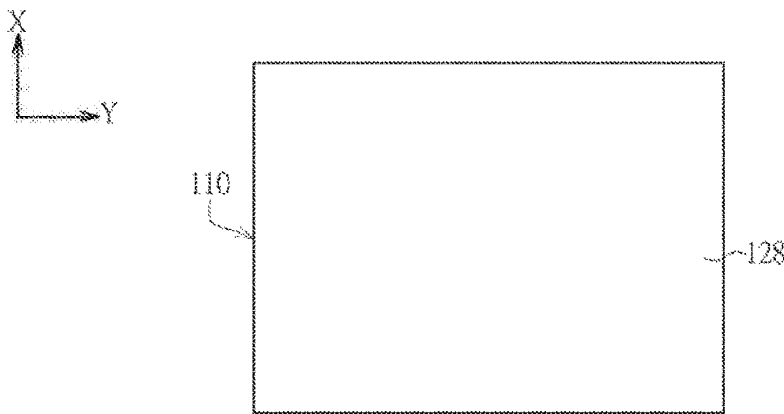


图 1B

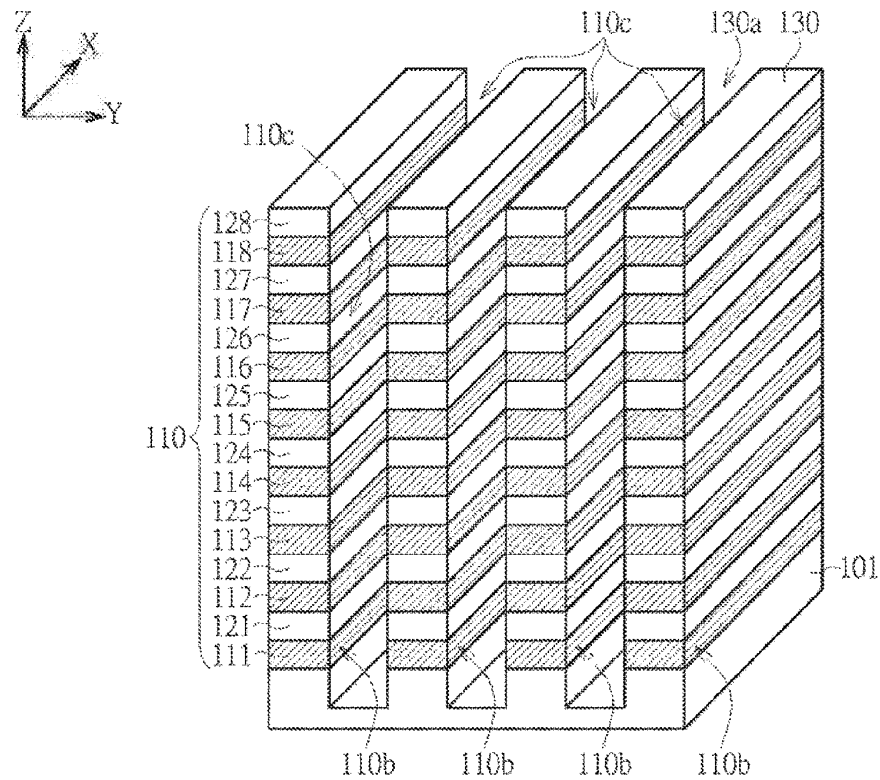


图 2A

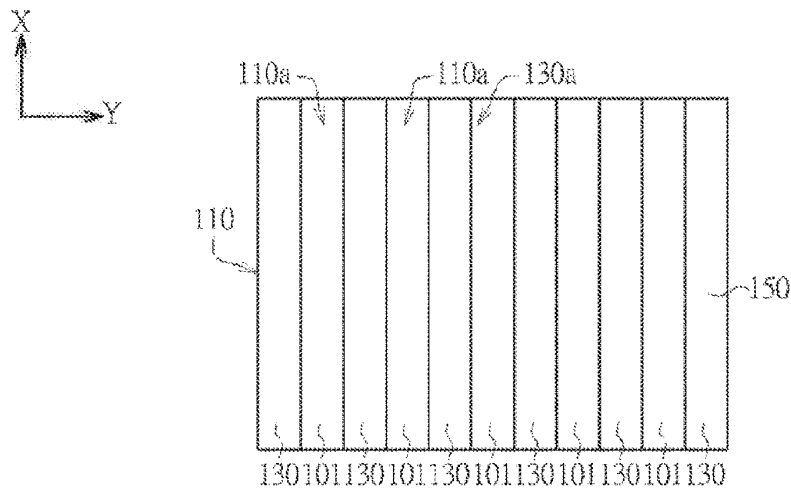


图 2B

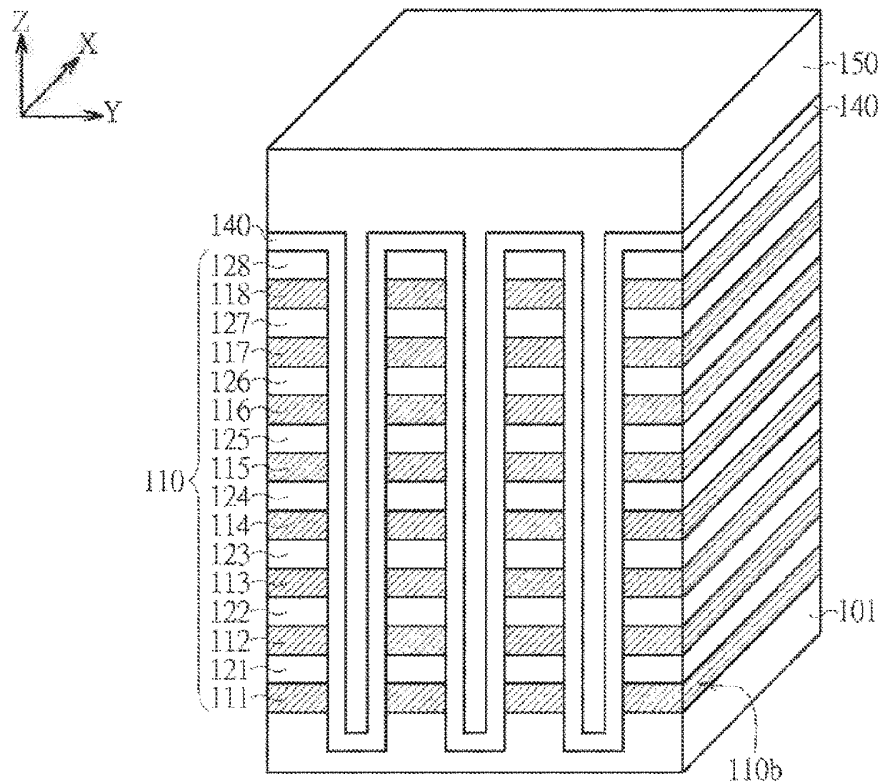


图 3A

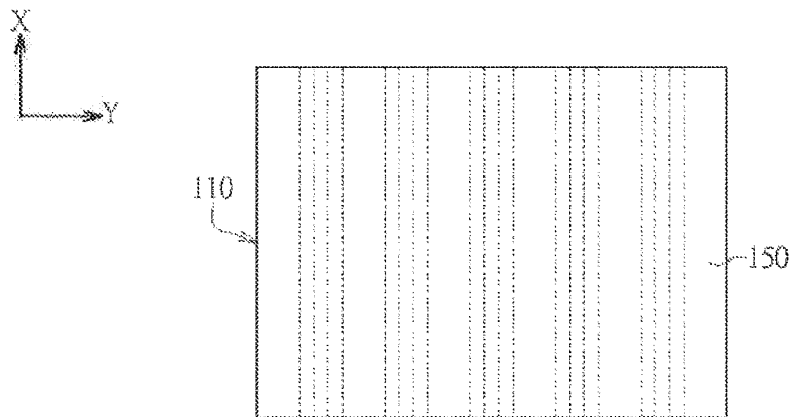


图 3B

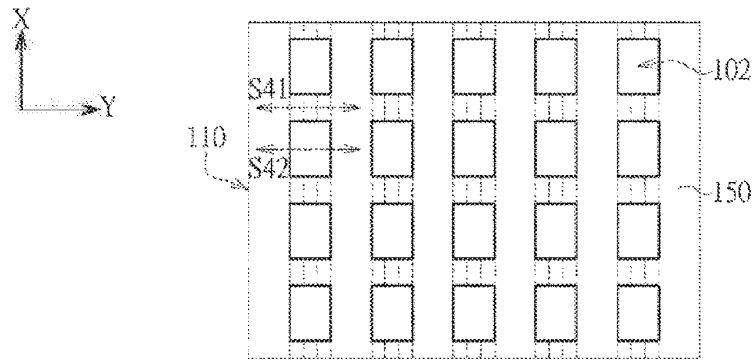


图 4A

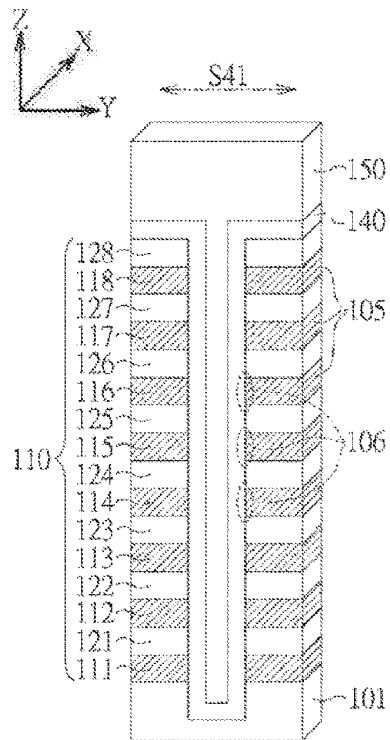


图 4B

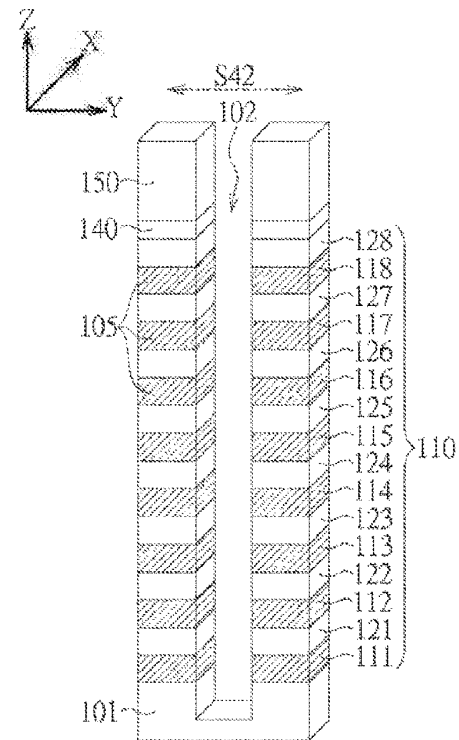


图 4C

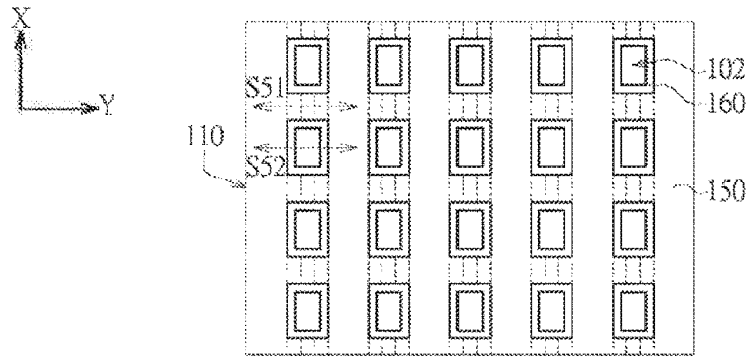


图 5A

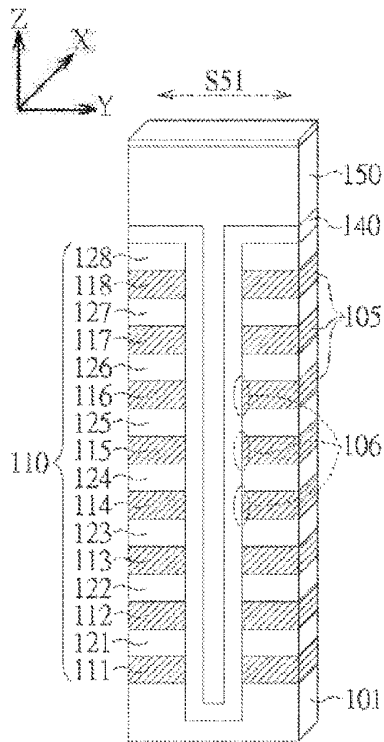


图 5B

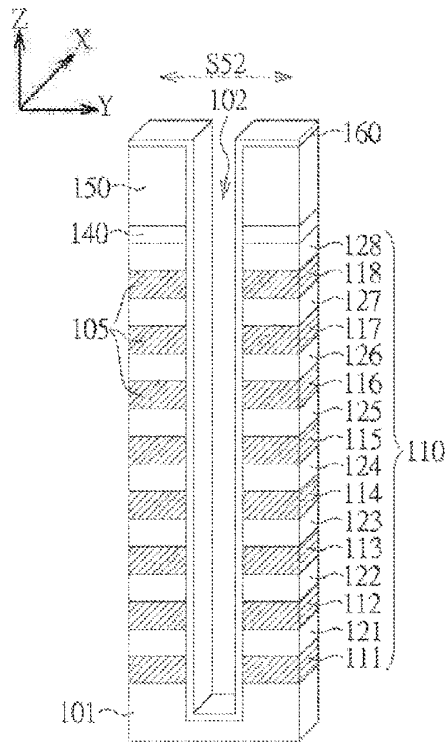


图 5C

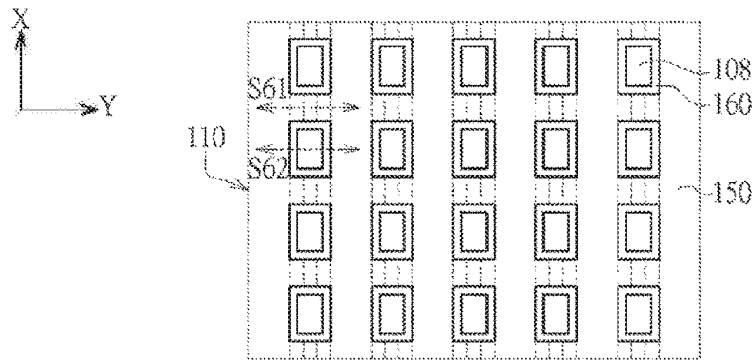


图 6A

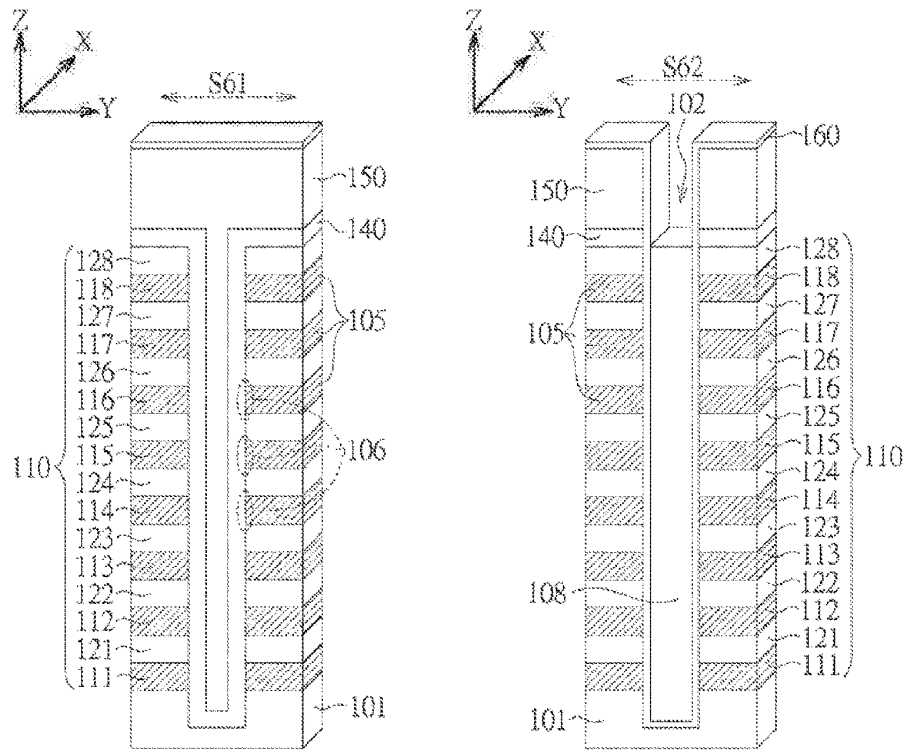


图 6B

图 6C

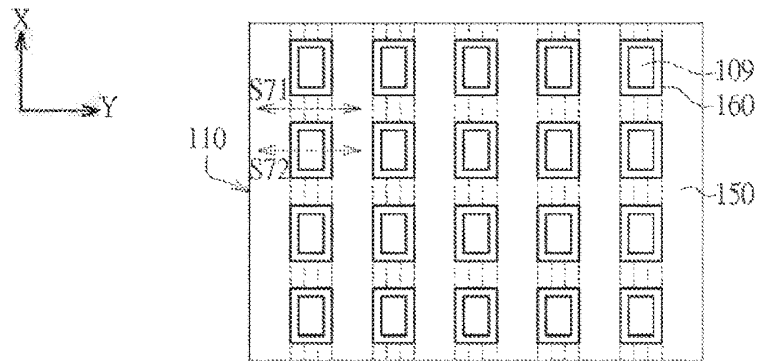


图 7A

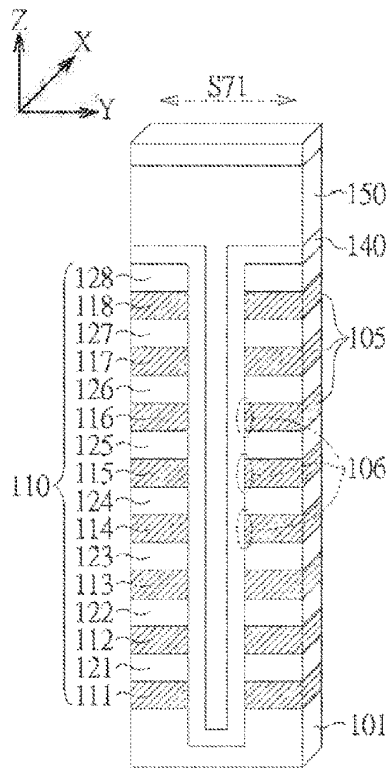


图 7B

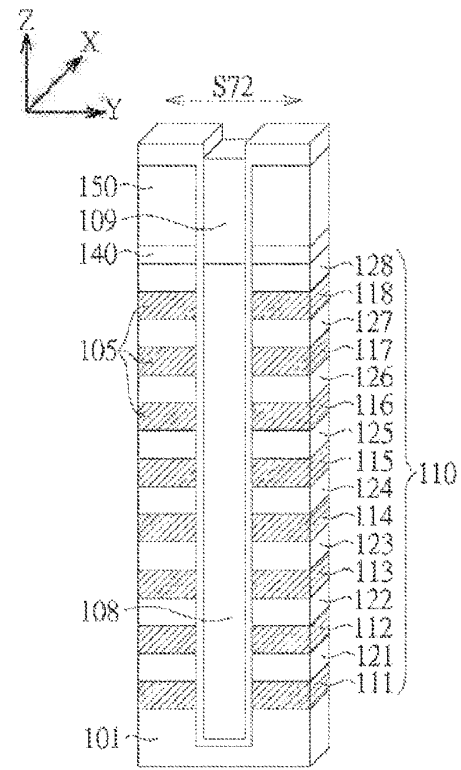


图 7C

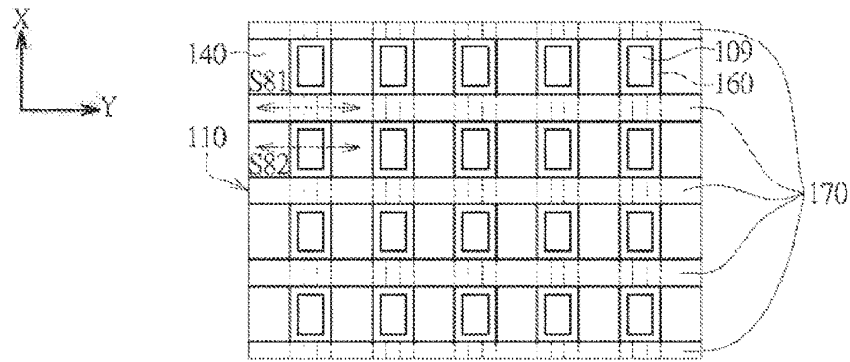


图 8A

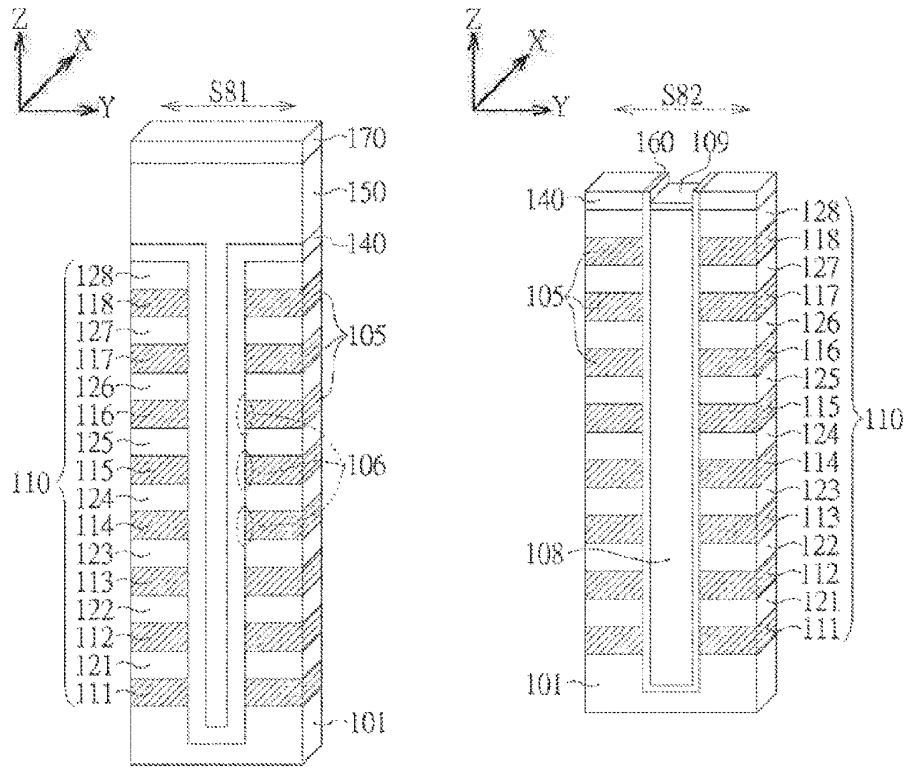


图 8B

图 8C

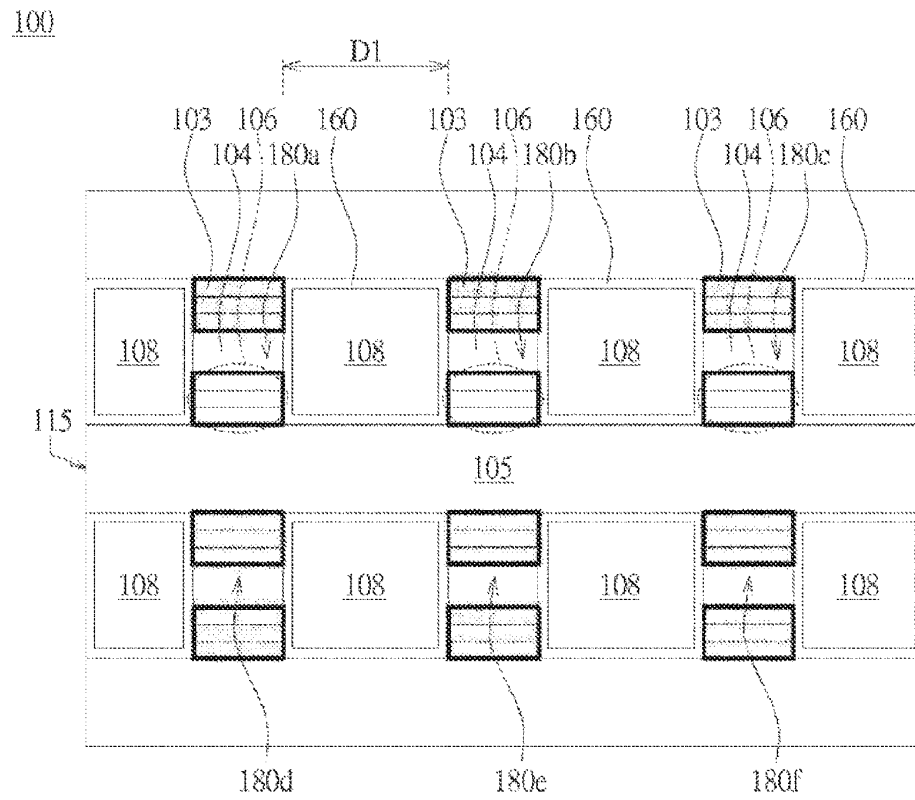


图 9



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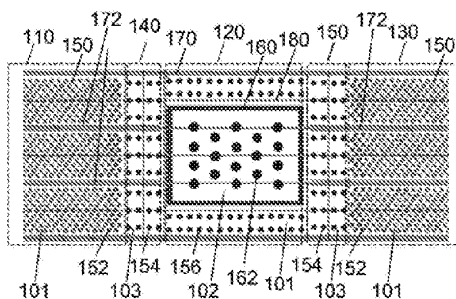
权利要求书3页 说明书10页 附图6页

(54)发明名称

一种3D NAND存储器件及其制造方法、封装
方法

(57)摘要

本发明提供了一种3D NAND存储器件及其制造方法、封装方法,通过绝缘环将环内和环外的堆叠层隔离开,绝缘环内仍为氧化物层和氮化物层的堆叠,绝缘环外为氧化物层和金属层的堆叠,绝缘环内的氧化物层和氮化物层的堆叠易于贯通接触孔的形成,而绝缘环外金属层保证了存储阵列字线的电连接,这种结构的贯通接触孔便于实现存储器件同CMOS芯片的连接,且易于同现有的工艺集成,特别是当堆叠层的厚度不断增加后,无需刻蚀金属堆叠来形成贯通接触孔,利于工艺的实现在集成度的不断提高。



1. 一种3D NAND存储器件,其特征在于,包括:

基底;

所述基底上的堆叠层,所述堆叠层包括沿字线方向依次排布的第一区域、第二区域和第三区域;其中,

所述第二区域位于所述第一区域和第三区域之间,所述第二区域中形成有贯通的绝缘环,所述绝缘环内的堆叠层为相互间隔堆叠的氧化物层和氮化物层,所述绝缘环内的堆叠层中形成有贯通接触孔;

所述绝缘环外的第二区域以及第一区域、第三区域的堆叠层为相互间隔堆叠的氧化物层和金属层,堆叠层中的顶层金属层为顶层选择栅,所述第一区域和第三区域中形成有用于形成存储器件的沟道孔;

设置在绝缘环外的栅线缝隙。

2. 根据权利要求1所述的存储器件,其特征在于,所述堆叠层还包括位于所述第一区域和第二区域之间的第四区域,以及位于所述第二区域和第三区域之间的第五区域,所述第四区域和第五区域的堆叠层为相互间隔堆叠的氧化物层和金属层且上两层金属层为顶层金属层阶梯结构;

第一区域、第四区域以及第三区域、第五区域的堆叠层中设置有沿字线方向延伸至所述绝缘环的一对相互平行栅线缝隙,沿与栅线缝隙垂直的方向所述绝缘环的边界至少延伸到一对相互平行的栅线缝隙之外的区域;

通过所述顶层金属层阶梯结构将所述绝缘环两侧的平行的栅线缝隙之间的所述第一区域和第三区域的顶层选择栅电连接。

3. 根据权利要求1所述的存储器件,其特征在于,第一区域以及第三区域的堆叠层中设置有沿字线方向延伸至所述绝缘环的一对相互平行栅线缝隙,沿与栅线缝隙垂直的方向所述绝缘环的边界至少延伸到一对相互平行的栅线缝隙之外的区域;所述第一区域和第三区域的外侧为堆叠层的阶梯结构,通过所述堆叠层的阶梯结构将所述绝缘环两侧的平行的栅线缝隙之间的所述第一区域和第三区域的顶层选择栅电连接。

4. 根据权利要求1所述的存储器件,其特征在于,所述绝缘环设置于相互平行的相邻的栅线缝隙之间的第二区域中,所述相互平行的相邻的栅线缝隙连续贯穿第一区域、第二区域和第三区域。

5. 根据权利要求1所述的存储器件,其特征在于,所述绝缘环设置于相互平行的相邻的栅线缝隙之间,所述相互平行的相邻的栅线缝隙穿过第一区域、第二区域和第三区域,且至少有一条栅线缝隙在第二区域处具有间断区。

6. 根据权利要求1所述的存储器件其特征在于,所述绝缘环之外的第二区域的堆叠层中形成有伪沟道孔。

7. 根据权利要求1-6中任一项所述的存储器件,其特征在于,所述基底为第一衬底,所述第一衬底的背面设置有贯通第一衬底且与贯通接触孔连接的第一互联结构。

8. 根据权利要求7所述的存储器件,其特征在于,还包括第二衬底,第二衬底中形成了CMOS器件电路以及键合层,所述第二衬底的键合层朝向第一衬底的正面,所述键合层将所述第一衬底和第二衬底粘合。

9. 根据权利要求8所述的存储器件,其特征在于,在对应于存储区域的第一衬底的背面

上形成有第一互联结构的衬垫。

10. 根据权利要求1-6中任一项所述的存储器件, 其特征在于, 所述基底包括第三衬底及第三衬底之上的外延衬底, 第三衬底中形成了CMOS器件电路以及第二互联结构, 所述贯通接触孔进一步贯穿外延衬底至第三衬底中的第二互联结构。

11. 一种3D NAND存储器件的制造方法, 其特征在于, 包括:

提供基底;

在所述基底上形成堆叠层, 所述堆叠层包括沿字线方向依次排布的第一区域、第二区域和第三区域, 所述堆叠层为相互间隔堆叠的氧化物层和氮化物层;

在所述堆叠层的两侧形成堆叠层的阶梯结构;

分别在所述第一区域、第三区域的堆叠层中形成沟道孔以及在所述第二区域的堆叠层中形成贯通的绝缘环;

形成栅线缝隙, 通过所述栅线缝隙将绝缘环之外的堆叠层中的氮化物层替换为金属层, 同时, 栅线缝隙中填满金属层, 堆叠层中的顶层金属层为顶层选择栅;

在绝缘环内的堆叠层中形成贯通接触孔。

12. 根据权利要求11所述的制造方法, 其特征在于, 所述堆叠层还包括位于所述第一区域和第二区域之间的第四区域, 以及位于所述第二区域和第三区域之间的第五区域; 第一区域、第四区域以及第三区域、第五区域的堆叠层中设置有沿字线方向延伸至所述绝缘环的一对相互平行栅线缝隙, 沿与栅线缝隙垂直的方向所述绝缘环的边界至少延伸到一对相互平行的栅线缝隙之外的区域; 则,

在所述堆叠层的两侧形成堆叠层的阶梯结构的同时, 还包括:

将第四区域和第五区域的堆叠层中的上两层氧化物层和氮化物层靠近绝缘环的一侧形成阶梯结构; 则,

在通过所述栅线缝隙将绝缘环之外的堆叠层中的氮化物层替换为金属层的步骤中, 在第四区域和第五区域形成顶层金属层阶梯结构, 通过所述顶层金属层阶梯结构将所述绝缘环两侧的平行的栅线缝隙之间的所述第一区域和第三区域的顶层选择栅电连接。

13. 根据权利要求11所述的制造方法, 其特征在于, 第一区域以及第三区域的堆叠层中设置有沿字线方向延伸至所述绝缘环的一对相互平行栅线缝隙, 沿与栅线缝隙垂直的方向所述绝缘环的边界至少延伸到一对相互平行的栅线缝隙之外的区域; 所述第一区域和第三区域的外侧为堆叠层的阶梯结构, 通过所述堆叠层的阶梯结构将所述绝缘环两侧的平行的栅线缝隙之间的所述第一区域和第三区域的顶层选择栅电连接。

14. 根据权利要求11所述的制造方法, 其特征在于, 所述绝缘环设置于相互平行的相邻的栅线缝隙之间的第二区域中, 所述相互平行的相邻的栅线缝隙连续贯穿第一区域、第二区域和第三区域。

15. 根据权利要求11所述的制造方法, 其特征在于, 所述绝缘环设置于相互平行的相邻的栅线缝隙之间, 所述相互平行的相邻的栅线缝隙穿过第一区域、第二区域和第三区域, 且至少有一条栅线缝隙在第二区域处具有间断区。

16. 根据权利要求11所述的制造方法, 其特征在于, 在所述第一区域、第三区域的堆叠层中形成沟道孔的步骤中, 还包括:

在所述绝缘环之外的第二区域的堆叠层中形成伪沟道孔。

17. 根据权利要求16所述的制造方法, 其特征在于, 分别在所述第一区域、第三区域的堆叠层中形成沟道孔以及在所述第二区域的堆叠层中形成贯通的绝缘环的步骤包括:

同时, 在第一区域、第三区域的堆叠中形成沟道通孔以及在第二区域的堆叠层中形成通孔环以及通孔环之外的第二区域的堆叠层中形成伪沟道通孔, 并分别进行沟道通孔、伪沟道通孔及通孔环的填充, 以分别形成沟道孔、伪沟道通孔和绝缘环。

18. 根据权利要求11-17中任一项所述的制造方法, 其特征在于, 所述基底为第一衬底, 还包括:

从所述第一衬底的背面形成贯通第一衬底且与贯通接触孔连接的第一互联结构。

19. 根据权利要求11-17中任一项所述的制造方法, 其特征在于, 所述基底包括第三衬底和第三衬底上的外延衬底, 与绝缘环内的区域对应的外延衬底的区域设置有开口, 开口中填充有介质材料, 第三衬底中形成了CMOS器件电路以及第二互联结构, 形成贯通接触孔的步骤包括: 形成贯穿绝缘环内的堆叠层以及外延衬底开口中的介质材料直至第三衬底中的互联结构的贯通接触孔。

20. 一种3D NAND存储器件结构的封装方法, 其特征在于, 包括:

提供如权利要求1-6中任一项所述的3D NAND存储器件, 基底为第一衬底;

提供第二衬底, 第二衬底中形成了CMOS器件电路以及键合层;

将所述第二衬底的键合层朝向第一衬底的正面, 通过所述键合层将所述第一衬底和第二衬底粘合。

21. 根据权利要求20所述的封装方法, 其特征在于, 还包括:

在所述第一衬底的背面形成贯通第一衬底且与贯通接触孔连接的第一互联结构。

22. 根据权利要求21所述的制造方法, 其特征在于, 还包括:

在对应于存储区域的第一衬底的背面上形成第一互联结构的衬垫。

一种3D NAND存储器件及其制造方法、封装方法

技术领域

[0001] 本发明涉及闪存存储器领域,尤其涉及一种3D NAND存储器件及其制造方法、封装方法。

背景技术

[0002] NAND闪存是一种比硬盘驱动器更好的存储设备,随着人们追求功耗低、质量轻和性能佳的非易失存储产品,在电子产品中得到了广泛的应用。目前,平面结构的NAND闪存已近实际扩展的极限,为了进一步的提高存储容量,降低每比特的存储成本,提出了3D结构的NAND存储器。

[0003] 在3D NAND存储器结构中,采用垂直堆叠多层数据存储单元的方式,实现堆叠式的3D NAND存储器结构,然而,其他的电路例如解码器(decoder)、页缓冲(page buffer)和锁存器(latch)等,这些外围电路都是CMOS器件形成的,CMOS器件的工艺无法与3D NAND器件集成在一起,目前,是分别采用不同的工艺形成3D NAND存储器阵列和外围电路,再通过穿过3D NAND存储器阵列的通孔将二者电连接在一起。3D NAND存储器阵列中的堆叠主要采用0POP结构,即多晶硅(poly)和氧化物(oxide)依次层叠的结构,随着存储容量需求的不断提高,0POP结构堆叠的层数不断增多,这对通孔的形成提出很大的挑战。

发明内容

[0004] 有鉴于此,本发明的第一方面提供了一种3D NAND存储器件,在存储阵列内设置贯通接触孔,便于同CMOS芯片的连接,且易于集成。

[0005] 为解决上述问题,本发明实施例提供了一种3D NAND存储器件,包括:

[0006] 基底;

[0007] 所述基底上的堆叠层,所述堆叠层包括沿字线方向依次排布的第一区域、第二区域和第三区域;其中,

[0008] 所述第二区域位于所述第一区域和第三区域之间,所述第二区域中形成有贯通的绝缘环,所述绝缘环内的堆叠层为相互间隔堆叠的氧化物层和氮化物层,所述绝缘环内的堆叠层中形成有贯通接触孔;

[0009] 所述绝缘环外的第二区域以及第一区域、第三区域的堆叠层为相互间隔堆叠的氧化物层和金属层,堆叠层中的顶层金属层为顶层选择栅,所述第一区域和第三区域中形成有用于形成存储器件的沟道孔;

[0010] 设置在绝缘环外的栅线缝隙。

[0011] 可选地,所述堆叠层还包括位于所述第一区域和第二区域之间的第四区域,以及位于所述第二区域和第三区域之间的第五区域,所述第四区域和第五区域的堆叠层为相互间隔堆叠的氧化物层和金属层且上两层金属层为顶层金属层阶梯结构;

[0012] 第一区域、第四区域以及第三区域、第五区域的堆叠层中设置有沿字线方向延伸至所述绝缘环的一对相互平行栅线缝隙,沿与栅线缝隙垂直的方向所述绝缘环的边界至少

延伸到一对相互平行的栅线缝隙之外的区域；

[0013] 通过所述顶层金属层阶梯结构将所述绝缘环两侧的平行的栅线缝隙之间的所述第一区域和第三区域的顶层选择栅电连接。

[0014] 可选地，第一区域以及第三区域的堆叠层中设置有沿字线方向延伸至所述绝缘环的一对相互平行栅线缝隙，沿与栅线缝隙垂直的方向所述绝缘环的边界至少延伸到一对相互平行的栅线缝隙之外的区域；所述第一区域和第三区域的外侧为堆叠层的阶梯结构，通过所述堆叠层的阶梯结构将所述绝缘环两侧的平行的栅线缝隙之间的所述第一区域和第三区域的顶层选择栅电连接。

[0015] 可选地，所述绝缘环设置于相互平行的相邻的栅线缝隙之间的第二区域中，所述相互平行的相邻的栅线缝隙连续贯穿第一区域、第二区域和第三区域。

[0016] 可选地，所述绝缘环设置于相互平行的相邻的栅线缝隙之间，所述相互平行的相邻的栅线缝隙穿过第一区域、第二区域和第三区域，且至少有一条栅线缝隙在第二区域处具有间断区。

[0017] 可选地，所述绝缘环之外的第二区域的堆叠层中形成有伪沟道孔。

[0018] 可选地，所述基底为第一衬底，所述第一衬底的背面设置有贯通第一衬底且与贯通接触孔连接的第一互联结构。

[0019] 可选地，还包括第二衬底，第二衬底中形成了CMOS器件电路以及键合层，所述第二衬底的键合层朝向第一衬底的正面，所述键合层将所述第一衬底和第二衬底粘合。

[0020] 可选地，在对应于存储区域的第一衬底的背面上形成有第一互联结构的衬垫。

[0021] 可选地，所述基底包括第三衬底及第三衬底之上的外延衬底，第三衬底中形成了CMOS器件电路以及第二互联结构，所述贯通接触孔进一步贯穿外延衬底至第三衬底中的第二互联结构。

[0022] 此外，本发明还提供了一种3D NAND存储器件的制造方法，包括：

[0023] 提供基底；

[0024] 在所述基底上形成堆叠层，所述堆叠层包括沿字线方向依次排布的第一区域、第二区域和第三区域，所述堆叠层为相互间隔堆叠的氧化物层和氮化物层；

[0025] 在所述堆叠层的两侧形成堆叠层的阶梯结构；

[0026] 分别在所述第一区域、第三区域的堆叠层中形成沟道孔以及在所述第二区域的堆叠层中形成贯通的绝缘环；

[0027] 形成栅线缝隙，通过所述栅线缝隙将绝缘环之外的堆叠层中的氮化物层置换为金属层，同时，栅线缝隙中填满金属层，堆叠层中的顶层金属层为顶层选择栅；

[0028] 在绝缘环内的堆叠层中形成贯通接触孔。

[0029] 可选地，所述堆叠层还包括位于所述第一区域和第二区域之间的第四区域，以及位于所述第二区域和第三区域之间的第五区域；第一区域、第四区域以及第三区域、第五区域的堆叠层中设置有沿字线方向延伸至所述绝缘环的一对相互平行栅线缝隙，沿与栅线缝隙垂直的方向所述绝缘环的边界至少延伸到一对相互平行的栅线缝隙之外的区域；则，

[0030] 在所述堆叠层的两侧形成堆叠层的阶梯结构的同时，还包括：

[0031] 将第四区域和第五区域的堆叠层中的上两层氧化物层和氮化物层靠近绝缘环的一侧形成阶梯结构；则，

[0032] 在通过所述栅线缝隙将绝缘环之外的堆叠层中的氮化物层替换为金属层的步骤中,在第四区域和第五区域形成顶层金属层阶梯结构,通过所述顶层金属层阶梯结构将所述绝缘环两侧的平行的栅线缝隙之间的所述第一区域和第三区域的顶层选择栅电连接。

[0033] 可选地,第一区域以及第三区域的堆叠层中设置有沿字线方向延伸至所述绝缘环的一对相互平行栅线缝隙,沿与栅线缝隙垂直的方向所述绝缘环的边界至少延伸到一对相互平行的栅线缝隙之外的区域;所述第一区域和第三区域的外侧为堆叠层的阶梯结构,通过所述堆叠层的阶梯结构将所述绝缘环两侧的平行的栅线缝隙之间的所述第一区域和第三区域的顶层选择栅电连接。

[0034] 可选地,所述绝缘环设置于相互平行的相邻的栅线缝隙之间的第二区域中,所述相互平行的相邻的栅线缝隙连续贯穿第一区域、第二区域和第三区域。

[0035] 可选地,所述绝缘环设置于相互平行的相邻的栅线缝隙之间,所述相互平行的相邻的栅线缝隙穿过第一区域、第二区域和第三区域,且至少有一条栅线缝隙在第二区域处具有间断区。

[0036] 可选地,在所述第一区域、第三区域的堆叠层中形成沟道孔的步骤中,还包括:

[0037] 在所述绝缘环之外的第二区域的堆叠层中形成伪沟道孔。

[0038] 可选地,分别在所述第一区域、第三区域的堆叠层中形成沟道孔以及在所述第二区域的堆叠层中形成贯通的绝缘环的步骤包括:

[0039] 同时在第一区域、第三区域的堆叠中形成沟道通孔以及在第二区域的堆叠层中形成通孔环以及通孔环之外的第二区域的堆叠层中形成伪沟道通孔,并分别进行沟道通孔、伪沟道通孔及通孔环的填充,以分别形成沟道孔、伪沟道通孔和绝缘环。

[0040] 可选地,所述基底为第一衬底,还包括:

[0041] 从所述第一衬底的背面形成贯通第一衬底且与贯通接触孔连接的第一互联结构。

[0042] 可选地,所述基底包括第二衬底和第三衬底上的外延衬底,与绝缘环内的区域对应的外延衬底的区域设置有开口,开口中填充有介质材料,第三衬底中形成了CMOS器件电路以及第二互联结构,形成贯通接触孔的步骤包括:形成贯穿绝缘环内的堆叠层以及外延衬底开口中的介质材料直至第三衬底中的互联结构的贯通接触孔。

[0043] 此外,本发明又提供了一种3D NAND存储器件结构的封装方法,包括:

[0044] 提供上述任一的3D NAND存储器件,基底为第一衬底;

[0045] 提供第二衬底,第二衬底中形成了CMOS器件电路以及键合层;

[0046] 将所述第二衬底的键合层朝向第一衬底的正面,通过所述键合层将所述第一衬底和第二衬底粘合。

[0047] 可选地,还包括:

[0048] 在所述第一衬底的背面形成贯通第一衬底且与贯通接触孔连接的第一互联结构。

[0049] 可选地,还包括:

[0050] 在对应于存储区域的第一衬底的背面上形成第一互联结构的衬垫。

[0051] 根据本发明实施例提供的3D NAND存储器件及其制造方法、封装方法,第一区域和第三区域为用于形成存储阵列的区域,在第二区域中设置了绝缘环,通过绝缘环将环内和环外的堆叠层隔离开,绝缘环内仍为氧化物层和氮化物层的堆叠,绝缘环外为氧化物层和金属层的堆叠,绝缘环内的氧化物层和氮化物层的堆叠易于贯通接触孔的形成,而绝缘环

外金属层保证了存储阵列字线的电连接,这种结构的贯通接触孔便于实现存储器件同CMOS芯片的连接,且易于同现有的工艺集成,特别是当堆叠层的厚度不断增加后,无需刻蚀金属堆叠来形成贯通接触孔,利于工艺的实现和集成度的不断提高。

附图说明

[0052] 图1示出了根据本发明实施例一的3D NAND存储器件的俯视结构示意图;
[0053] 图2示出了根据本发明实施例二的3D NAND存储器件的俯视结构示意图;
[0054] 图3示出了根据本发明实施例三的3D NAND存储器件的俯视结构示意图;
[0055] 图4示出了根据本发明实施例四的3D NAND存储器件的俯视结构示意图;
[0056] 图5示出了根据本发明实施例五的3D NAND存储器件的剖视结构示意图;
[0057] 图6示出了根据本发明实施例六的3D NAND存储器件的剖视结构示意图;
[0058] 图7示出了根据本发明实施例的3D NAND存储器件的制造方法流程图;
[0059] 图8-图10示出了根据本发明实施例的3D NAND存储器件的封装方法的制造过程中的结构示意图。

具体实施方式

[0060] 为使本发明的上述目的、特征和优点能够更加明显易懂,下面结合附图对本发明的具体实施方式做详细的说明。

[0061] 在下面的描述中阐述了很多具体细节以便于充分理解本发明,但是本发明还可以采用其他不同于在此描述的其它方式来实施,本领域技术人员可以在不违背本发明内涵的情况下做类似推广,因此本发明不受下面公开的具体实施例的限制。

[0062] 其次,本发明结合示意图进行详细描述,在详述本发明实施例时,为便于说明,表示器件结构的剖面图会不依一般比例作局部放大,而且所述示意图只是示例,其在此不应限制本发明保护的范围。此外,在实际制作中应包含长度、宽度及深度的三维空间尺寸。另外,以下描述的第一特征在第二特征之“上”的结构可以包括第一和第二特征形成为直接接触的实施例,也可以包括另外的特征形成在第一和第二特征之间的实施例,这样第一和第二特征可能不是直接接触。

[0063] 参考图1-6所示,本发明实施例提供了一种3D NAND存储器件,包括:

[0064] 基底;

[0065] 所述基底上的堆叠层,所述堆叠层包括沿字线方向依次排布的第一区域110、第二区域120和第三区域130;其中,

[0066] 所述第二区域120位于所述第一区域110和第三区域130之间,所述第二区域120中形成有贯通的绝缘环160,所述绝缘环160内的堆叠层102为相互间隔堆叠的氧化物层1021和氮化物层1022,所述绝缘环160内的堆叠层102中形成有贯通接触孔162;所述绝缘环160外的第二区域120以及第一区域110、第三区域130的堆叠层101为相互间隔堆叠的氧化物层1011和金属层1012,堆叠层中的顶层金属层为顶层选择栅1013,所述第一区域110和第三区域130中形成有用于形成存储器件的沟道孔150;设置在绝缘环外的栅线缝隙170。

[0067] 在3D NAND存储器件中,堆叠层的层数决定了垂直方向上的存储单元的个数,堆叠层的层数例如可以为32层、64层等,堆叠层的层数越多,越能提高集成度,堆叠层的最外侧

为阶梯结构,堆叠层中最上层的金属层为顶层选择栅,堆叠层中的金属层为字线,通过最外侧的阶梯结构将字线引出。

[0068] 在本发明实施例中,第一区域110、第二区域120和第三区域130是沿字线(word line)方向依次排布的,在字线方向上这三个区域具有基本一致的边界,他们的堆叠层具有相同的层数,绝缘环内、外的堆叠层的材料不同。其中,第一区域110、第三区域130及绝缘环160外的第二区域120的堆叠层为氧化物层与金属层间隔堆叠而成,金属层例如为W,氧化物层例如为oxide,第一区域110、第三区域130是用于形成实际存储数据的存储阵列的区域,其堆叠层中形成有用于形成存储器件的沟道孔150,这些沟道孔150之上会继续设置有与其连接的位线和/或其他的互联线,沟道孔150中包括有电荷存储层和沟道层,电荷存储层例如可以为Oxide-Nitrid-Oxide的结构,沟道层例如可以为多晶硅。

[0069] 栅线缝隙170设置在绝缘环160之外的堆叠层中,在存储区内栅线缝隙170的方向同字线方向是一直的,栅线缝隙170贯穿到存储堆叠层的底部到基底上,栅线缝隙170的侧壁为氧化物层、填充材料为金属,例如W,其下下形成有掺杂区,在制造过程中,栅线缝隙170用于堆叠层中金属层的替换,形成之后,栅线缝隙170一方面将整个存储区分割为多个块存储区和指存储区,另一方面起到共源(common source)的作用。通常在指存储区的中部设置有顶层选择栅切线(Top Select Gate Cut)180,将指存储区的顶层选择栅分割为两部分,顶层选择栅切线通常由氧化物材料形成,该选择栅切线可以不穿过绝缘环及绝缘环内的区域。

[0070] 绝缘环160内的堆叠层为氧化物层与氮化物层的堆叠,为用于形成贯通接触孔162的区域,贯通接触孔162至少贯通了堆叠层,贯通接触孔162用于与另一具有CMOS电路的芯片电连接,CMOS电路芯片主要包括了3D NAND存储器件的阵列芯片所需的电路,例如页缓存(page buffer)、解码器(decoder)、锁存(latches)以及外围电路等,贯通接触孔162例如可以由Ti/TiN和W来形成。

[0071] 由于在第二区域120中设置了绝缘环160,通过绝缘环160将环内和环外的堆叠层隔离开,绝缘环160内为氧化物层和氮化物层的堆叠层,绝缘环160外,包括绝缘环160外的第二区域120以及第一区域110、第三区域130的堆叠层都为氧化物层和金属层的堆叠,绝缘环160内的氧化物层和氮化物层的堆叠易于贯通接触孔162的形成,而绝缘环外堆叠层中的金属层保证了存储阵列字线的电连接,这种结构的贯通接触孔便于实现存储器件同CMOS芯片的连接,且易于同现有的工艺集成,特别是当堆叠层的厚度不断增加后,无需刻蚀金属堆叠来形成贯通接触孔,利于工艺的集成和集成度的不断提高。

[0072] 为了更好地理解本发明,以下将结合具体的实施例进行详细的说明。在下述实施例一至实施例四中,以一个块存储区为例进行说明,每两条栅线缝隙之间为一个指存储区,在块存储区中有三个指存储区,可以理解的是,此处仅为示例,根据不同的设计,可以是不同设置的存储区。

[0073] 实施例一

[0074] 在该实施例中,参考图1所示,第二区域120设置在块(block)存储区中,块存储区由栅线缝隙170间隔开,栅线缝隙170的方向为字线方向,栅线缝隙之间相互平行,一对栅线缝隙170之间为指(finger)存储区。在图2所示的具体实施例中,栅线缝隙将一个块存储区分隔为三个指存储区,根据不同的设计需求,可以分隔为2个或更多个的指存储区。

[0075] 参考图5所示,栅线缝隙170贯穿到堆叠层的底部,栅线缝隙170的侧壁为氧化物层、填充材料为金属,例如W,其下下形成有掺杂区,栅线缝隙170一方面隔断指存储区,另一方面起到共源(common source)的作用。通常在指存储区的中部设置有顶层选择栅切线(Top Select Gate Cut)180,将指存储区的顶层选择栅分割为两部分,顶层选择栅切线180通常由氧化物材料形成。

[0076] 在该实施例中,所述第一区域110和第三区域130的堆叠层中形成有相互平行的栅线缝隙170,沿与栅线缝隙垂直的方向所述绝缘环160的边界至少延伸到一对相互平行的栅线缝隙170之外的区域,这样,绝缘环160将这对相互平行的栅线缝隙170之间的第一区域110和第三区域130的堆叠层中的金属层被完全阻断,也就是说,绝缘环160两侧的指存储区中顶层选择栅无法通过堆叠层中的顶层金属层连通。

[0077] 为此,在该实施例中,在所述第一区域110和第二区域120之间设置有第四区域140,以及在所述第二区域120和第三区域130之间设置有第五区域150,同时,所述第四区域140和第五区域150的堆叠层中的上两层金属层为阶梯结构,第一区域110、第四区域140以及第三区域130、第五区域150的堆叠层中设置有沿字线方向延伸至所述绝缘环160的一对相互平行栅线缝隙172,也就是说,此时,栅线缝隙172延伸到绝缘环处,同时,所述第四区域140和第五区域150的堆叠层中的上两层金属层为阶梯结构,为了便于描述,记做顶层金属层阶梯结构,该阶梯结构可以为单侧阶梯,这样,通过所述顶层金属层阶梯结构将所述绝缘环两侧的平行的栅线缝隙之间的所述第一区域和第三区域的顶层选择栅电连接,例如可以在阶梯结构上设置一层或多层互联层将两侧的选择栅电连接起来。

[0078] 同第一区域和第三区域,所述第四区域140和第五区域150的堆叠层为相互间隔堆叠的氧化物层和金属层,所述第四区域140和第五区域150的堆叠层的层数同第一区域的堆叠层的层数。

[0079] 在该实施例中,为了便于工艺的优化和集成,在第一区域110靠近第四区域140的边缘部分、第三区域110靠近第五区域150的边缘部分的堆叠层中形成有伪沟道孔152,第四区域140和第五区域150的堆叠层中形成有伪沟道孔154,以及绝缘环160外的第二区域的堆叠层中也形成有伪沟道孔156,这些伪沟道孔152、154、156可以与形成存储单元的沟道孔150一同形成,而后续并不在这些伪沟道孔上形成位线及互联线,他们并不用于真正的存储。

[0080] 该实施例中,可以形成尺寸较大的绝缘环,适用于形成较多数量的贯通接触孔,且可以通过顶层金属层阶梯结构实现第一区域和第三区域的顶层选择栅的连接,因此,根据设计的需要,可以在一个块存储区中设置一个或多个第二区域。

[0081] 实施例二

[0082] 在该实施例中,将描述与实施例一不同的部分,相同部分将不再赘述。

[0083] 参考图2所示,所述第一区域110和第三区域130的堆叠层中形成有延伸至绝缘环160的相互平行的一对栅线缝隙172,沿与栅线缝隙垂直的方向所述绝缘环160的边界至少延伸到一对相互平行的栅线缝隙170之外的区域,这样,绝缘环160将这对相互平行的栅线缝隙172之间的第一区域110和第三区域130的堆叠层中的金属层被完全阻断,也就是说,绝缘环160两侧的指存储区中顶层选择栅无法通过堆叠层中的顶层金属层连通。

[0084] 在该实施例中,所述第一区域110和第三区域130的外侧为堆叠层的阶梯结构(图

未示出),通过所述堆叠层的阶梯结构将所述绝缘环两侧的平行的栅线缝隙之间的所述第一区域110和第三区域130的顶层选择栅电连接。也就是说,可以利用3D NAND器件中本身就固有的堆叠层两侧的阶梯结构,该实施例适用于X-DEC(字线解码)的设计为交错(zigzag)的设计,这样,不用于字线解码的一侧的阶梯结构可以用于上述的第一区域110和第三区域130的顶层选择栅电连接。对于该实施例,在一个块存储区中可以设置一个第二区域。

[0085] 此外,同实施例一,为了便于工艺的优化和集成,也可以在第一区域110和第三区域110靠近第二区域120的边缘部分的堆叠层中设置伪沟道孔152,以及绝缘环160外的第二区域的堆叠层中设置伪沟道孔156,这些伪沟道孔并不用于形成存储单元。

[0086] 实施例三

[0087] 参考图3所示,在该实施例中,栅线缝隙170连续贯穿第一区域110、第二区域120和第三区域130,将所述绝缘环160设置于相互平行的栅线缝隙170之间的第二区域120中,也就是说绝缘环160没有完全占据第二区域。这样,绝缘环160之外的第二区域120的堆叠层中的顶层金属将第一区域和第二区域的顶层选择栅连接起来,绝缘环160两侧的第一区域和第二区域的顶层选择栅不会被绝缘环阻断。

[0088] 这样,可以在每个指存储区中设置一个绝缘环,且无需额外的结构来弥补阻断造成的影响,也可以根据设计的需要,在一个块存储区的指存储中设置一个或多个第二区域,设计灵活且简单易行。

[0089] 此外,同实施例一,为了便于工艺的优化和集成,也可以在第一区域110和第三区域110靠近第二区域120的边缘部分的堆叠层中设置伪沟道孔152,以及绝缘环160外的第二区域的堆叠层中设置伪沟道孔156,这些伪沟道孔并不用于形成存储单元。

[0090] 实施例四

[0091] 参考图4所示,在该实施例中,所述绝缘环160设置于相互平行的相邻的栅线缝隙之间,所述栅线缝隙170、172穿过第一区域110、第二区域120和第三区域130,且至少有一条栅线缝隙172在第二区域120处具有间断区171。

[0092] 在该实施例中,穿过第一区域110、第二区域120和第三区域130的栅线缝隙可以是连续贯穿这三个区域,也可以是连续穿过第一区域110和第二区域120、连续穿过第三区域130和第二区域120但在第二区域120处具有间断区171,参考图4所示,一条栅线缝隙170可以为连续贯穿、另一条栅线缝隙172为有间断的贯穿,也可以为两条栅线缝隙均为有间断的贯穿。

[0093] 同实施例三,绝缘环160没有完全占据第二区域,这样,绝缘环160之外的第二区域120的堆叠层中的顶层金属将第一区域和第二区域的顶层选择栅连接起来,绝缘环160两侧的第一区域和第二区域的顶层选择栅不会被绝缘环阻断。

[0094] 这样,在具体应用中,如图4所示,可以将块存储区内的栅线缝隙172都设置为有间断的贯穿,块存储区之间的栅线缝隙170设置为连续的贯穿,通过块存储区内的栅线缝隙172的间断区171将整个块存储区的字线连接起来了。这种方式无需额外的结构就可以实现顶层选择栅以及字线的连接,结构简单且易于实现,集成度更高。

[0095] 此外,同实施例一,为了便于工艺的优化和集成,也可以在第一区域110和第三区域110靠近第二区域120的边缘部分的堆叠层中设置伪沟道孔152,以及绝缘环160外的第二区域的堆叠层中设置伪沟道孔156,这些伪沟道孔并不用于形成存储单元。

[0096] 实施例五

[0097] 对于本发明实施例,存储器件设置于基底之上,该基底至少起到支撑的作用,在一些实施例中,参考图5所示,基底为第一衬底100,第一衬底100可以为半导体衬底,例如可以为Si衬底、Ge衬底、SiGe衬底、SOI(绝缘体上硅,Silicon On Insulator)或GOI(绝缘体上锗,Germanium On Insulator)、三五族化合物及二四族化合物半导体等。

[0098] 对于直接在衬底上形成上述存储器件的实施例,如图5所示,可以从第一衬底100的背面设置贯通第一衬底100且与贯通接触孔162连接的第一互联结构190,该第一互联结构190可以包括一层或多层过孔、金属层,通过第一衬底背面第一互联结构190将贯通接触孔162引出,以进一步与CMOS电路的第二衬底实现电连接。

[0099] 具体的,键合层将所述第一衬底和第二衬底粘合,实现两个芯片的电连接,在第二衬底中已经形成了CMOS器件电路以及键合层,所述第二衬底的键合层朝向第一衬底的正面,所述键合层将所述第一衬底和第二衬底粘合。

[0100] 进一步地,由于采用了背面引出贯通接触孔的方式,可以在对应于存储区域的第一衬底的背面上形成第一互联结构的衬垫。由于是在第一衬底的存储区域的背面形成了衬垫,不同于常规方法,无需在第一衬底的存储区域的周边形成衬垫,可以进一步缩小器件的尺寸,提高集成度。

[0101] 实施例六

[0102] 在另一些实施例中,参考图6所示,所述基底包括第三衬底300及第三衬底300之上的外延衬底400,第三衬底300中形成了CMOS器件电路(图未示出)以及第二互联结构302,所述贯通接触孔162进一步贯穿外延衬底400至第三衬底300中的第二互联结构302。

[0103] 在所述第三衬底300中已经形成了CMOS器件电路以及互联结构,该第二互联结构可以包括接触、一层或多层过孔、金属层,进而在第三衬底之上通过淀积的方式形成外延衬底400,外延衬底进一步用于上述存储器件的形成,该外延衬底100可以为单层或叠层结构,例如可以为单晶硅、多晶硅或多晶硅与金属层的叠层。进一步地,可以在与绝缘环内的区域对应的外延衬底的区域中设置开口402,以便于贯通接触孔162贯通至第二互联结构302。

[0104] 以上对本发明实施例的3D NAND存储器件进行了详细的描述,此外,本发明还提供了上述存储器件的制造方法。

[0105] 参考图7所示,在步骤S01,提供基底。

[0106] 在一些实施例中,所述基底可以为第一衬底100,参考图5所示。

[0107] 在另一些实施例中,参考图6所示,所述基底可以包括第三衬底300和第三衬底300之上的外延衬底400,第三衬底300中形成了CMOS器件电路以及第二互联结构302。

[0108] S02,在所述基底上形成堆叠层,所述堆叠层包括沿字线方向依次排布的第一区域、第二区域和第三区域,所述堆叠层为相互间隔堆叠的氧化物层和氮化物层(图未示出)。

[0109] 可以采用合适的淀积方法依次堆叠氧化物层和氮化物层来形成堆叠层,堆叠层的层数根据垂直方向所需形成的存储单元的个数来确定。

[0110] S03,在所述堆叠层的两侧形成堆叠层的阶梯结构(图未示出)。

[0111] 可以采用多次刻蚀的方法,在堆叠层的两侧形成阶梯结构,阶梯结构的阶梯面暴露出氮化物层,该氮化物层在后续的步骤中将被替换为金属层,以用于字线或其他金属层的连接。

[0112] 在一些实施例中,参考图1所示,所述堆叠层还包括位于所述第一区域110和第二区域120之间的第四区域140,以及位于所述第二区域120和第三区域130之间的第五区域150,在形成阶梯结构的同时,例如在形成堆叠层的较浅的阶梯的同时,还进行如下步骤:

[0113] 将第四区域140和第五区域150的堆叠层中的上两层氧化物层和氮化物层靠近绝缘环的一侧形成阶梯结构。

[0114] S04,分别在所述第一区域、第三区域的堆叠层中形成沟道孔以及在所述第二区域的堆叠层中形成贯通的绝缘环。

[0115] 参考图1及图5所示,在优选的实施例中,可以通过以下步骤来实现:

[0116] 同时在第一区域110、第三区域130的堆叠层101中形成沟道通孔以及在第二区域120的堆叠层101中形成通孔环以及通孔环之外的第二区域的堆叠层中形成伪沟道通孔,并分别进行沟道通孔、伪沟道通孔及通孔环的填充,以分别形成沟道孔150、伪沟道通孔152、156和绝缘环160。其中,绝缘环的材料可以为介质材料,例如可以为氧化物、氮化物或他们的组合。沟道通孔和伪沟道通孔可以同时形成,可以依次形成oxide-nitride-oxide的电荷捕获层和多晶硅填充层。

[0117] 这样,可以在形成沟道孔的同时形成绝缘环160,简化工艺步骤。当然,在其他实施例中,可以采用其他方法来形成绝缘环160,例如在形成沟道孔之前或者之后来形成绝缘环。

[0118] S05,形成栅线缝隙170,通过所述栅线缝隙170将绝缘环之外的堆叠层中的氮化物层置换为金属层1012,同时,栅线缝隙中填满金属层,堆叠层中的顶层金属层为顶层选择栅。

[0119] 在不同的实施例中,根据不同的设置需求,设置栅线缝隙的结构以及与绝缘环的相对位置。

[0120] 在该步骤中,由于绝缘环的阻挡作用,绝缘环内堆叠层中的氮化物层并不会被去除和替换,而通过栅线缝隙绝缘环外的堆叠层中的氮化物层将会被去除并替换,优选地,替换的金属层可以为W。

[0121] 在一些实施例中,参考图1所示,所述堆叠层还包括位于所述第一区域110和第二区域120之间的第四区域140,以及位于所述第二区域120和第三区域130之间的第五区域150,所述第四区域140和第五区域150的堆叠层为相互间隔堆叠的氧化物层和金属层且上两层金属层为顶层金属层阶梯结构;第一区域110、第四区域140以及第三区域130、第五区域150的堆叠层中设置有沿字线方向延伸至所述绝缘环的一对相互平行栅线缝隙172,沿与栅线缝隙垂直的方向所述绝缘环160的边界至少延伸到一对相互平行的栅线缝隙172之外的区域。这样,在通过所述栅线缝隙172将绝缘环160之外的堆叠层中的氮化物层置换为金属层后,在第四区域和第五区域形成顶层金属层阶梯结构,通过所述顶层金属层阶梯结构将所述绝缘环两侧的平行的栅线缝隙之间的所述第一区域和第三区域的顶层选择栅电连接。

[0122] 在另一些实施例中,参考图2所示,第一区域110以及第三区域130的堆叠层中设置有沿字线方向延伸至所述绝缘环的一对相互平行栅线缝隙172,沿与栅线缝隙垂直的方向所述绝缘环的边界至少延伸到一对相互平行的栅线缝隙172之外的区域;所述第一区域110和第三区域130的外侧为堆叠层的阶梯结构,通过所述堆叠层的阶梯结构将所述绝缘环两

侧的平行的栅线缝隙之间的所述第一区域和第三区域的顶层选择栅电连接。

[0123] 在另一些实施例中,参考图3所示,所述绝缘环设置于相互平行的相邻的栅线缝隙170之间的第二区域120中,所述相互平行的相邻的栅线缝隙170连续贯穿第一区域110、第二区域120和第三区域130。

[0124] 在又一些实施例中,参考图4所示,所述绝缘环设置于相互平行的相邻的栅线缝隙170、172之间,所述相互平行的相邻的栅线缝隙穿过第一区域110、第二区域120和第三区域130,且至少有一条栅线缝隙172在第二区域120处具有间断区171。

[0125] S06,在绝缘环内160的堆叠层102中形成贯通接触孔162。

[0126] 绝缘环160内的堆叠层为氧化物层与氮化物层的叠层,可以通过刻蚀技术刻蚀绝缘环内的堆叠层,直至暴露堆叠层下的区域,进而,进行金属材料的填充,例如W,来形成贯通接触孔。

[0127] 在一些实施例中,参考图6所示,所述基底包括第三衬底300和第三衬底300上的外延衬底400,与绝缘环内160的区域对应的外延衬底的区域设置有开口402,开口402中填充有介质材料,第三衬底300中形成了CMOS器件电路以及第二互联结构302,形成贯通接触孔的步骤包括:形成贯穿绝缘环内的堆叠层以及外延衬底开口中的介质材料直至第三衬底中的互联结构302的贯通接触孔162。

[0128] 在一些实施例中,参考图5所示,所述基底为第一衬底100,还可以包括:

[0129] 从所述第一衬底100的背面形成贯通第一衬底100且与贯通接触孔160连接的第一互联结构190。

[0130] 此外,本发明还提供了一种3D NAND存储器件结构的封装方法,参考图8-10所示,包括:

[0131] 提供第一衬底100,第一衬底100上形成有上述实施例中任一的3D NAND存储器件;

[0132] 提供第二衬底200,第二衬底200中形成了CMOS器件电路以及键合层220;

[0133] 将所述第二衬底200的键合层220朝向第一衬底100的正面,通过所述键合层将所述第一衬底100和第二衬底200粘合。

[0134] 此步骤中,第一衬底100的互连结构230与第二衬底的互联结构210需要相对应设置,以实现二者的互联。

[0135] 进一步地,还包括:

[0136] 在所述第一衬底100的背面形成贯通第一衬底100且与贯通接触孔162连接的第一互联结构190。

[0137] 可以依次通过减薄第一衬底100、抛光第一衬底100以及形成互联结构等步骤来进行贯通接触孔的背连接。

[0138] 进一步地,在对应于存储区域的第一衬底的背面上形成第一互联结构的衬垫(图未示出)。

[0139] 虽然本发明披露如上,但本发明并非限定于此。任何本领域技术人员,在不脱离本发明的精神和范围内,均可作各种更动与修改,因此本发明的保护范围应当以权利要求所限定的范围为准。

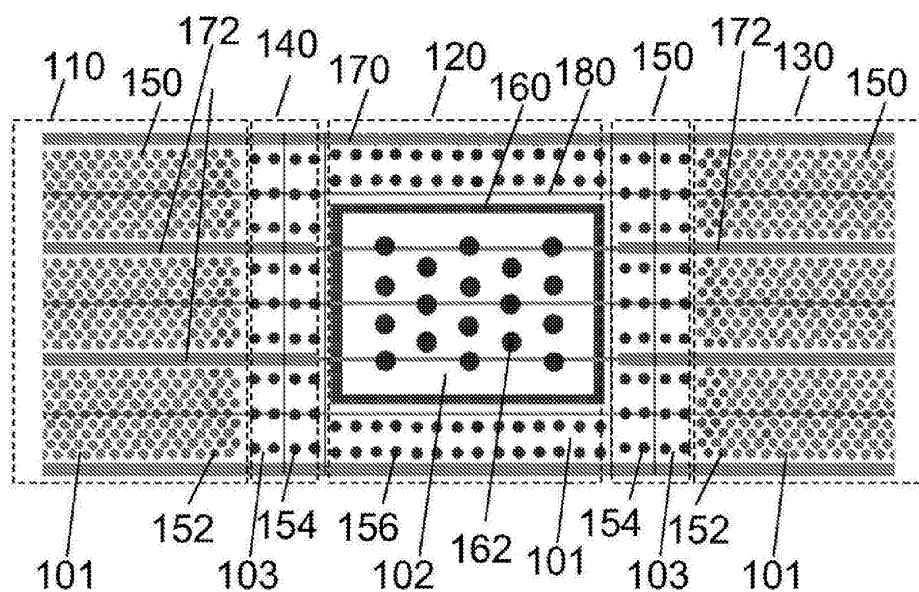


图1

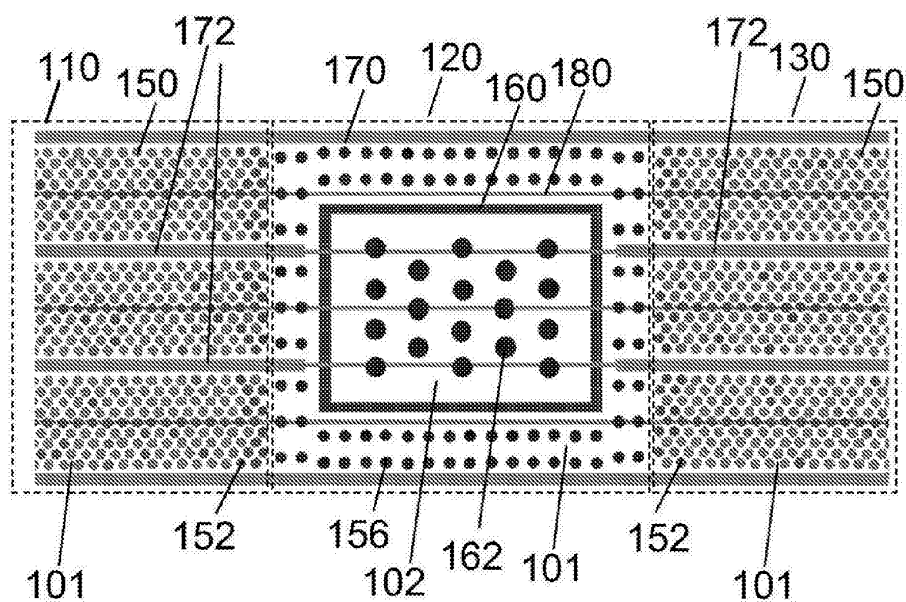


图2

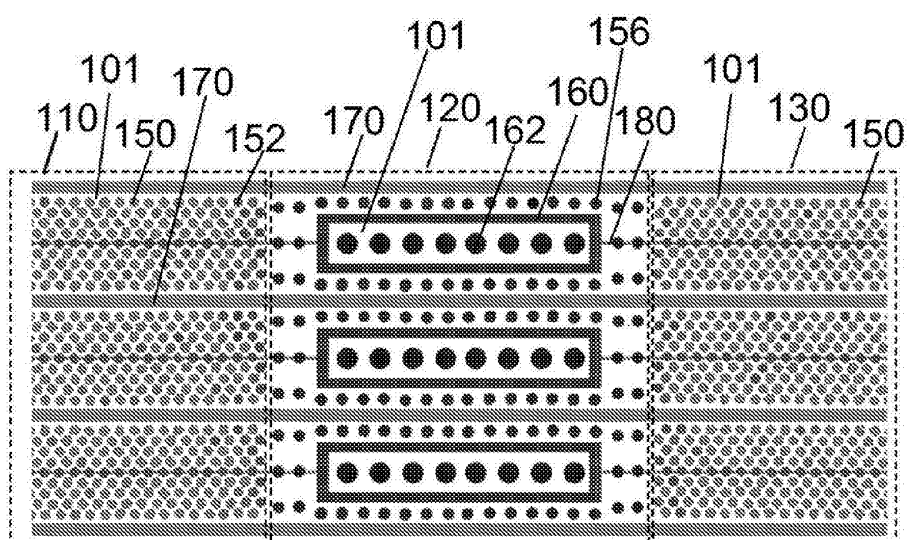


图3

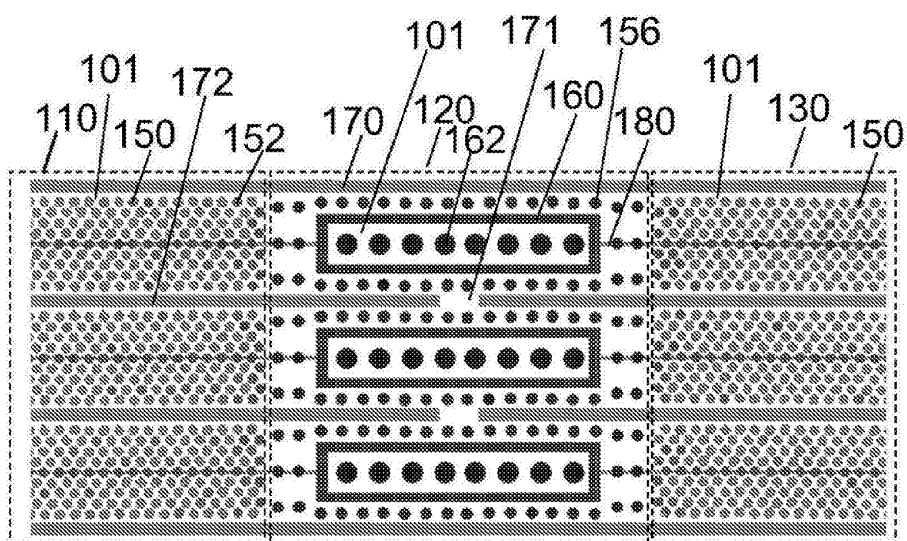


图4

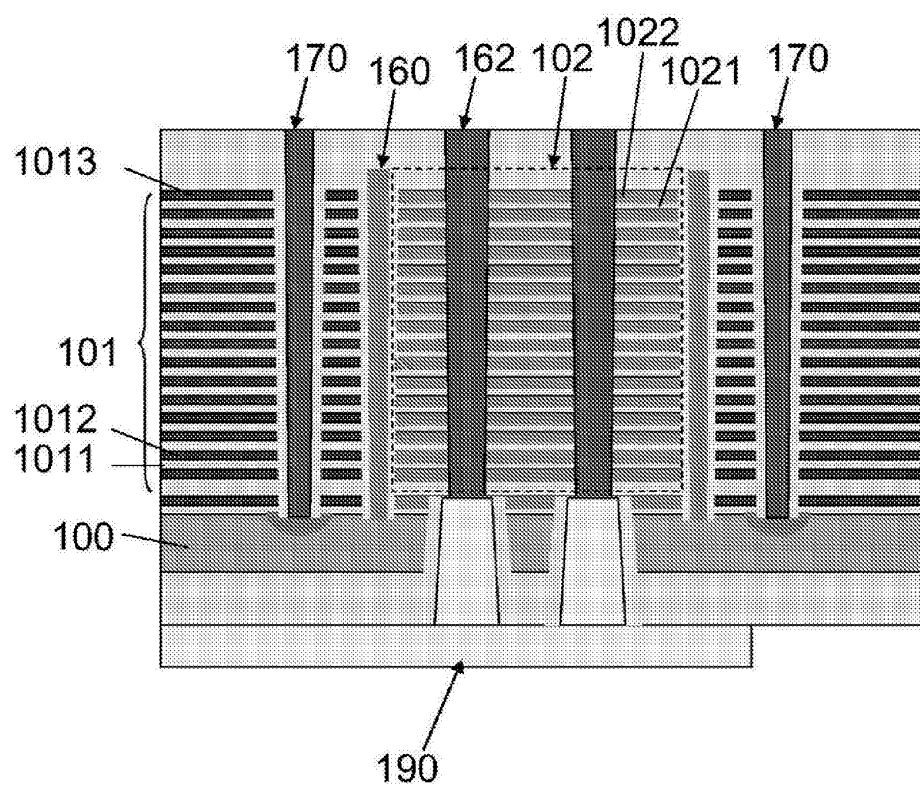


图5

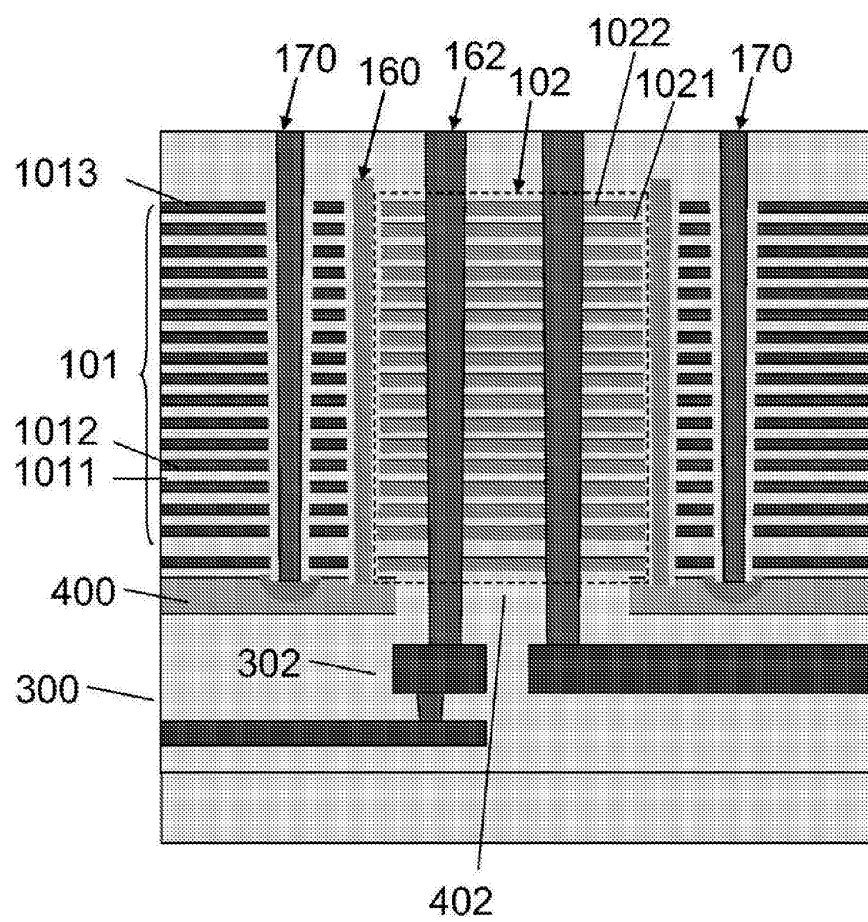


图6

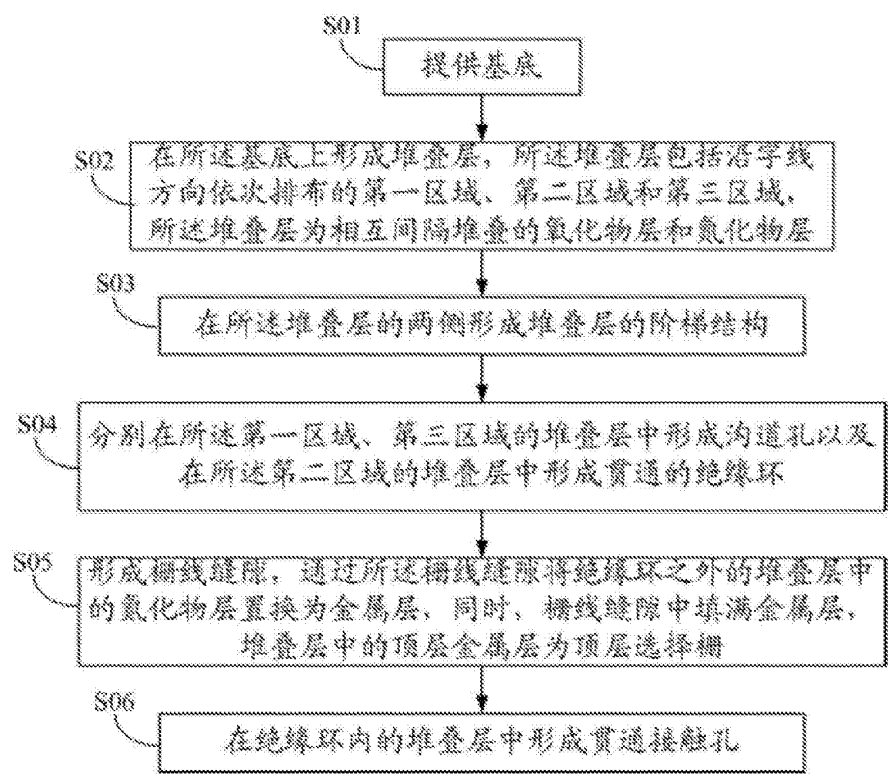


图7

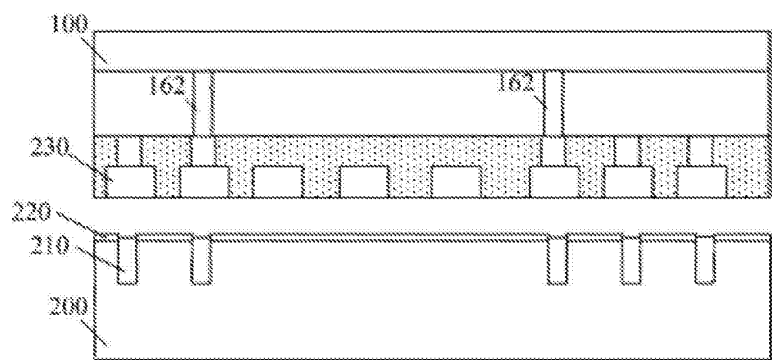


图8

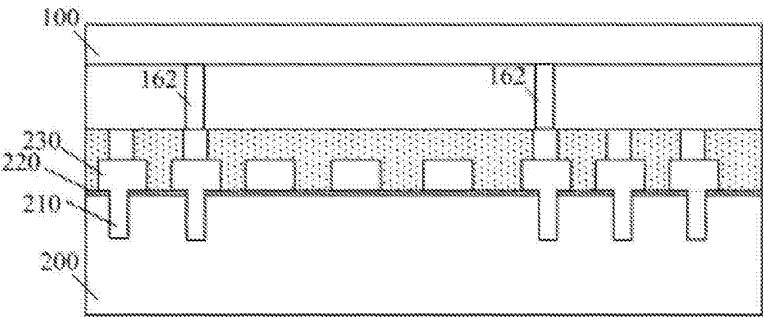


图9

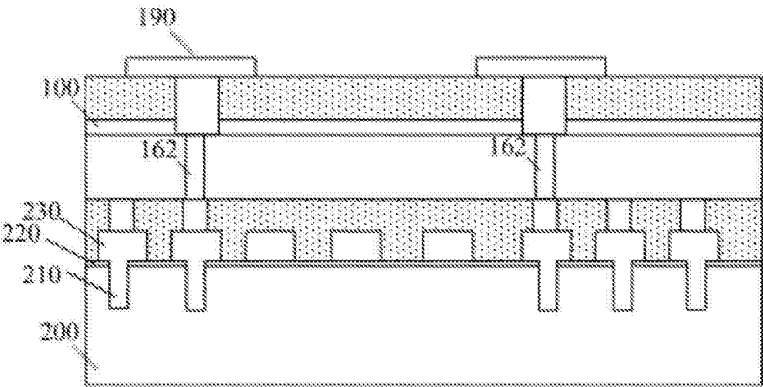


图10



Espacenet

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3D NAND memory device and manufacturing method therefor

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Classification: - **international:** H01L27/11519; H01L27/11551; H01L27/11565;
H01L27/11578
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Application number: CN201710135329 20170308 Global Dossier

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Abstract of CN106920794 (A)

The invention provides a 3D NAND memory device. The memory device comprises a substrate, a first memory region, a sub step region, run-through contact holes, and grid line gaps, wherein the first memory region is arranged on the substrate; the first memory region comprises a word line stacking layer and channel holes in the word line stacking layer; the side wall of the word line stacking layer adopts a step structure; the sub step region is arranged in the step structure; the sub step region is a stacked layer of an oxide layer and a nitride layer; the sub step region extends to the edge of the step structure in a word line direction; an insulating layer is arranged on the side wall, connected with the step structure, of the sub step region; the run-through contact holes are formed in the sub step region; and the grid line gaps are formed in the step structure outside the sub step region. By virtue of the run-through contact holes with the structure, connection between the memory device and a CMOS chip can be realized conveniently, and the memory device can be integrated with the existing process easily; particularly, when the thickness of the stacking layer is constantly increased, a step of etching metal stacking to form the run-through contact holes is not

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needed, so that realization of the process and constant improvement of the integration degree can be facilitated.

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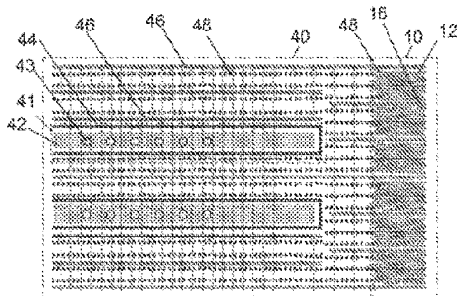
权利要求书2页 说明书9页 附图5页

(54)发明名称

一种3D NAND存储器件及其制造方法

(57)摘要

本发明提供了一种3D NAND存储器件,包括:基底;基底上的第一存储区,第一存储区包括字线堆叠层以及字线堆叠层中的沟道孔,字线堆叠层的侧壁为阶梯结构;在阶梯结构中具有子阶梯区域,子阶梯区域为氧化物层和氮化物层的叠层,子阶梯区域沿字线方向延伸至阶梯结构的边缘,在子阶梯区域与阶梯结构相接的侧壁上设置有绝缘层;在子阶梯区域中设置有贯通接触孔;子阶梯区域之外的阶梯结构中的栅线缝隙。这种结构的贯通接触孔便于实现存储器件同CMOS芯片的连接,且易于同现有的工艺集成,特别是当堆叠层的厚度不断增加后,无需刻蚀金属堆叠层形成贯通接触孔,利于工艺的实现和集成度的不断提高。



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1. 一种3D NAND存储器件,其特征在于,包括:

基底;

基底上的第一存储区,第一存储区包括字线堆叠层以及字线堆叠层中的沟道孔,字线堆叠层的侧壁为阶梯结构;

在阶梯结构中具有子阶梯区域,子阶梯区域为氧化物层和氮化物层的叠层,子阶梯区域沿字线方向延伸至阶梯结构的边缘,在子阶梯区域与阶梯结构相接的侧壁上设置有绝缘层;

在子阶梯区域中设置有贯通接触孔;

子阶梯区域之外的阶梯结构中的栅线缝隙。

2. 根据权利要求1所述的存储器件,其特征在于,子阶梯区域之外的阶梯结构中形成有伪沟道孔。

3. 根据权利要求1所述的存储器件,其特征在于,阶梯结构的栅线缝隙非等间距设置,子阶梯区域设置于间距较大的栅线缝隙之间,以使得子阶梯区域与栅线缝隙之间的空间用于互联结构的形成。

4. 根据权利要求1所述的存储器件,其特征在于,子阶梯区域设置于阶梯结构的对应块区域的栅线缝隙之间,另一侧的阶梯结构的相应的区域用于互联结构的形成。

5. 根据权利要求1-4中任一项所述的存储器件,其特征在于,还包括通孔形成区和第二存储区,第一存储区、通孔形成区和第二存储区沿位线依次排布,第二存储区包括字线堆叠层以及字线堆叠层中的沟道孔;通孔形成区包括氧化物层和氮化物层的通孔堆叠层、贯穿通孔堆叠层的贯通接触孔以及通孔堆叠层的侧壁上的绝缘层;第一存储区和第二存储区中沿字线方向的栅线缝隙。

6. 根据权利要求5所述的存储器件,其特征在于,第一存储区和第二存储区包括:

块堆叠层,所述块堆叠层包括沿字线方向依次排布的第一区域、第二区域和第三区域;其中,

所述第二区域位于所述第一区域和第三区域之间,所述第二区域中形成有贯通的绝缘环,所述绝缘环内的块堆叠层为相互间隔堆叠的氧化物层和氮化物层,贯穿所述绝缘环内的块堆叠层的贯通接触孔;所述绝缘环外的第二区域以及第一区域、第三区域的块堆叠层为相互间隔堆叠的氧化物层和金属层,顶层的所述金属层为顶层选择栅,所述第一区域和第三区域中形成有沟道孔,第一区域和第三区域中的块堆叠层为字线堆叠层;绝缘环外的堆叠层中的栅线缝隙。

7. 根据权利要求6所述的存储器件,其特征在于,所述绝缘环设置于相邻的栅线缝隙之间,所述相邻的栅线缝隙穿过第一区域、第二区域和第三区域,且至少有一条栅线缝隙在第二区域处具有间断区。

8. 根据权利要求1-5中任一项所述的存储器件,其特征在于,所述基底包括第一衬底及第一衬底之上的外延衬底,第一衬底中形成了CMOS器件电路以及第一互联结构,所述贯通接触孔进一步贯穿外延衬底至第一衬底中的第一互联结构。

9. 一种3D NAND存储器件的形成方法,其特征在于,包括:

提供基底;

在基底上形成氧化物层与氮化物层相互间隔的堆叠层,堆叠层具有第一存储区;

在所述堆叠层的两侧形成堆叠层的阶梯结构；

在第一存储区的堆叠层中形成沟道孔以及在阶梯结构中沿字线方向形成延伸至阶梯结构的边缘的绝缘层，绝缘层呈开口的条形图案，开口朝向阶梯结构边缘，绝缘层内的区域为子阶梯区域；

形成栅线缝隙，通过栅线缝隙将第一存储区和绝缘层之外的阶梯结构中的氮化物层置换为金属层，同时，在栅线缝隙中填满金属层；

在子阶梯区域中形成贯通接触孔。

10. 根据权利要求9所述的制造方法，其特征在于，在第一存储区的堆叠层中形成沟道孔以及在阶梯结构中沿字线方向形成延伸至阶梯结构的边缘的绝缘层的步骤包括：

在第一存储区的堆叠层中形成通孔，同时，在阶梯结构中沿字线方向形成延伸至阶梯结构边缘的沟槽，沟槽为呈开口的条形图案，开口朝向阶梯结构边缘，分别进行通孔和沟槽的填充，以分别形成沟道孔和绝缘层。

11. 根据权利要求9或10所述的制造方法，其特征在于，所述基底包括第一衬底及第一衬底之上的外延衬底，第一衬底中形成了CMOS器件电路以及第一互联结构；在基底上形成氧化物层与氮化物层相互间隔的堆叠层之前，还包括：

在外延衬底上形成开口，所述开口对应于子阶梯区域的区域，开口中填充有介质材料；则，

在子阶梯区域中形成贯通接触孔的步骤包括：

在子阶梯区域中形成贯穿子阶梯区域和开口至第一互联结构的贯通接触孔。

一种3D NAND存储器件及其制造方法

技术领域

[0001] 本发明涉及闪存存储器领域,尤其涉及一种3D NAND存储器件及其制造方法。

背景技术

[0002] NAND闪存是一种比硬盘驱动器更好的存储设备,随着人们追求功耗低、质量轻和性能佳的非易失存储产品,在电子产品中得到了广泛的应用。目前,平面结构的NAND闪存已近实际扩展的极限,为了进一步的提高存储容量,降低每比特的存储成本,提出了3D结构的NAND存储器。

[0003] 在3D NAND存储器结构中,采用垂直堆叠多层数据存储单元的方式,实现堆叠式的3DNAND存储器结构,然而,其他的电路例如解码器(decoder)、页缓冲(page buffer)和锁存器(latch)等,这些外围电路都是CMOS器件形成的,CMOS器件的工艺无法与3D NAND器件集成在一起,目前,是分别采用不同的工艺形成3D NAND存储器阵列和外围电路,再通过穿过3D NAND存储器阵列的通孔将二者电连接在一起。3D NAND存储器阵列中的堆叠主要采用OPOP结构,即多晶硅(poly)和氧化物(oxide)依次层叠的结构,随着存储容量需求的不断提高,OPOP结构堆叠的层数不断增多,这对通孔的形成提出很大的挑战。

发明内容

[0004] 有鉴于此,本发明的第一方面提供了一种3D NAND存储器件,在存储阵列内设置贯通接触孔,便于同CMOS芯片的连接,且易于集成。

[0005] 为解决上述问题,本发明实施例提供了一种3D NAND存储器件,包括:

[0006] 基底;

[0007] 基底上的第一存储区,第一存储区包括字线堆叠层以及字线堆叠层中的沟道孔,字线堆叠层的侧壁为阶梯结构;

[0008] 在阶梯结构中具有子阶梯区域,子阶梯区域为氧化物层和氮化物层的叠层,子阶梯区域沿字线方向延伸至阶梯结构的边缘,在子阶梯区域与阶梯结构相接的侧壁上设置有绝缘层;

[0009] 在子阶梯区域中设置有贯通接触孔;

[0010] 子阶梯区域之外的阶梯结构中的栅线缝隙。

[0011] 可选地,子阶梯区域之外的阶梯结构中形成有伪沟道孔。

[0012] 可选地,阶梯结构的栅线缝隙非等间距设置,子阶梯区域设置于间距较大的栅线缝隙之间,以使得子阶梯区域与栅线缝隙之间的空间用于互联结构的形成。

[0013] 可选地,子阶梯区域设置于阶梯结构的对应块区域的栅线缝隙之间,另一侧的阶梯结构的相应的区域用于互联结构的形成。

[0014] 可选地,还包括通孔形成区和第二存储区,第一存储区、通孔形成区和第二存储区沿位线依次排布,第二存储区包括字线堆叠层以及字线堆叠层中的沟道孔;通孔形成区包括氧化物层和氮化物层的通孔堆叠层、贯穿通孔堆叠层的贯通接触孔以及通孔堆叠层的侧

壁上的绝缘层;第一存储区和第二存储区中沿字线方向的栅线缝隙。

[0015] 可选地,第一存储区和第二存储区包括:

[0016] 块堆叠层,所述块堆叠层包括沿字线方向依次排布的第一区域、第二区域和第三区域;其中,

[0017] 所述第二区域位于所述第一区域和第三区域之间,所述第二区域中形成有贯通的绝缘环,所述绝缘环内的块堆叠层为相互间隔堆叠的氧化物层和氮化物层,贯穿所述绝缘环内的块堆叠层的贯通接触孔;所述绝缘环外的第二区域以及第一区域、第三区域的块堆叠层为相互间隔堆叠的氧化物层和金属层,顶层的所述金属层为顶层选择栅,所述第一区域和第三区域中形成有沟道孔,第一区域和第三区域中的块堆叠层为字线堆叠层;绝缘环外的堆叠层中的栅线缝隙。

[0018] 可选地,所述绝缘环设置于相邻的栅线缝隙之间,所述相邻的栅线缝隙穿过第一区域、第二区域和第三区域,且至少有一条栅线缝隙在第二区域处具有间断区。

[0019] 可选地,所述基底包括第一衬底及第一衬底之上的外延衬底,第一衬底中形成了CMOS器件电路以及第一互联结构,所述贯通接触孔进一步贯穿外延衬底至第一衬底中的第一互联结构。

[0020] 此外,本发明还提供一种3D NAND存储器件的形成方法,包括:

[0021] 提供基底;

[0022] 在基底上形成氧化物层与氮化物层相互间隔的堆叠层,堆叠层具有第一存储区;

[0023] 在所述堆叠层的两侧形成堆叠层的阶梯结构;

[0024] 在第一存储区的堆叠层中形成沟道孔以及在阶梯结构中沿字线方向形成延伸至阶梯结构的边缘的绝缘层,绝缘层呈开口的条形图案,开口朝向阶梯结构边缘,绝缘层内的区域为子阶梯区域;

[0025] 形成栅线缝隙,通过栅线缝隙将第一存储区和绝缘层之外的阶梯结构中的氮化物层置换为金属层,同时,在栅线缝隙中填满金属层;

[0026] 在子阶梯区域中形成贯通接触孔。

[0027] 可选地,在第一存储区的堆叠层中形成沟道孔以及在阶梯结构中沿字线方向形成延伸至阶梯结构的边缘的绝缘层的步骤包括:

[0028] 在第一存储区的堆叠层中形成通孔,同时,在阶梯结构中沿字线方向形成延伸至阶梯结构边缘的沟槽,沟槽为呈开口的条形图案,开口朝向阶梯结构边缘,分别进行通孔和沟槽的填充,以分别形成沟道孔和绝缘层。

[0029] 可选地,所述基底包括第一衬底及第一衬底之上的外延衬底,第一衬底中形成了CMOS器件电路以及第一互联结构;在基底上形成氧化物层与氮化物层相互间隔的堆叠层之前,还包括:

[0030] 在外延衬底上形成开口,所述开口对应于子阶梯区域的区域,开口中填充有介质材料;则,

[0031] 在子阶梯区域中形成贯通接触孔的步骤包括:

[0032] 在子阶梯区域中形成贯穿了阶梯区域和开口至第一互联结构的贯通接触孔。

[0033] 根据本发明实施例提供的3D NAND存储器件及其制造方法,在阶梯结构中设置了绝缘层,通过绝缘层将子阶梯区域和阶梯结构隔离开,绝缘层内仍为氧化物层和氮化物层

的堆叠,从而易于贯通接触孔的形成,这种结构的贯通接触孔便于实现存储器件同CMOS芯片的连接,且易于同现有的工艺集成,特别是当堆叠层的厚度不断增加后,无需刻蚀金属堆叠来形成贯通接触孔,利于工艺的实现和集成度的不断提高。

附图说明

- [0034] 图1示出了根据本发明实施例的3D NAND存储器件芯片的俯视示意图;
- [0035] 图2示出了根据本发明实施例一的3D NAND存储器件的俯视结构示意图;
- [0036] 图3示出了根据本发明实施例二的3D NAND存储器件的俯视结构示意图;
- [0037] 图4示出了根据本发明实施例三的3D NAND存储器件的俯视结构示意图;
- [0038] 图5示出了根据本发明实施例四的3D NAND存储器件的俯视结构示意图;
- [0039] 图6示出了根据本发明实施例五的3D NAND存储器件的剖视结构示意图;
- [0040] 图7示出了根据本发明实施例的3D NAND存储器件的制造方法流程图。

具体实施方式

[0041] 为使本发明的上述目的、特征和优点能够更加明显易懂,下面结合附图对本发明的具体实施方式做详细的说明。

[0042] 在下面的描述中阐述了很多具体细节以便于充分理解本发明,但是本发明还可以采用其他不同于在此描述的其它方式来实施,本领域技术人员可以在不违背本发明内涵的情况下做类似推广,因此本发明不受下面公开的具体实施例的限制。

[0043] 其次,本发明结合示意图进行详细描述,在详述本发明实施例时,为便于说明,表示器件结构的剖面图会不依一般比例作局部放大,而且所述示意图只是示例,其在此不应限制本发明保护的范围。此外,在实际制作中应包含长度、宽度及深度的三维空间尺寸。另外,以下描述的第一特征在第二特征之“上”的结构可以包括第一和第二特征形成为直接接触的实施例,也可以包括另外的特征形成在第一和第二特征之间的实施例,这样第一和第二特征可能不是直接接触。

[0044] 参考图1至图3所示,本发明提出了一种3D NAND存储器件,包括:

[0045] 基底;

[0046] 基底上的第一存储区10,第一存储区10包括字线堆叠层以及字线堆叠层中的沟道孔,字线堆叠层的侧壁为阶梯结构40;

[0047] 在阶梯结构40中具有子阶梯区域41,子阶梯区域41中的字线部分为氮化物层,子阶梯区域41沿字线方向延伸至阶梯结构的边缘,在子阶梯区域41与阶梯结构40相接的侧壁上设置有绝缘层44;

[0048] 在子阶梯区域42中设置有贯通接触孔43;

[0049] 子阶梯区域41之外的阶梯结构40中的栅线缝隙46。

[0050] 在本发明实施例中,存储区为用于形成存储单元的区域,根据不同的设计,存储区可以为一个或多个的块(block)存储区。

[0051] 在3D NAND存储器件中,堆叠层的层数决定了垂直方向上的存储单元的个数,堆叠层的层数例如可以为32层、64层等,堆叠层的层数越多,越能提高集成度,堆叠层可以为多晶硅层和氧化物层交替的叠层,也可以为金属层和氧化物层交替的叠层,堆叠层中最上

层为顶层选择栅,堆叠层中的金属层或多晶硅层为字线。堆叠层的两侧为阶梯结构,阶梯结构为通过堆叠层形成的结构,具有与堆叠层相同的材料层,通过阶梯结构可以将字线引出。

[0052] 3D NAND存储器的存储区形成在堆叠层中,本发明实施例中,堆叠层为氧化物层和金属层的堆叠层,金属层例如为W,氧化物层例如为oxide,在堆叠层中形成有沟道孔12,沟道孔12包括有电荷存储层和沟道层,电荷存储层例如可以为Oxide-Nitrid-Oxide的结构,沟道层例如可以为多晶硅,这样,每一层金属层与沟道孔接触的地方就形成一个存储单元,多层金属层和多个沟道孔构成了3D的存储阵列,为了便于描述和与通孔形成区的堆叠层相区别,将包含金属层的堆叠层记做存储堆叠层。

[0053] 在第一存储区10中设置有栅线缝隙16,栅线缝隙16的方向同字线方向是一致的,栅线缝隙16贯穿到存储堆叠层的底部到基底上,栅线缝隙16的侧壁为氧化物层、填充材料为金属,例如W,其下下形成有掺杂区,在制造过程中,栅线缝隙16用于堆叠层中金属层的替换,形成之后,栅线缝隙16一方面将整个存储区分割为多个块存储区和指存储区,另一方面起到共源(common source)的作用。通常在指存储区的中部设置有顶层选择栅切线(Top Select Gate Cut),将指存储区的顶层选择栅分割为两部分,顶层选择栅切线通常由氧化物材料形成。同样地,在阶梯结构40中也设置有栅线缝隙46,该栅线缝隙46贯穿阶梯结构40到基底上,在制造过程中,栅线缝隙16用于阶梯结构中金属层的替换。

[0054] 子阶梯区域41为阶梯结构40中的部分区域,子阶梯区域41沿字线方向延伸至阶梯结构40的边缘,其仍为阶梯型的结构,与阶梯结构具有相同的结构,在子阶梯区域41与阶梯结构40相接的侧壁上设置有绝缘层44,也就是说,通过绝缘层44将阶梯结构40和子阶梯区域41分隔开来,这样,在通过栅线缝隙46将阶梯结构40中的氮化物层进行替换时,子阶梯区域41中的氮化物层仍然保留。绝缘层44为介质材料,可以为单层或多层结构,例如可以为氧化物、氮化物等或他们的组合。

[0055] 贯通接触孔43形成了阶梯区域41中,贯通接触孔43至少贯通了整个阶梯结构至基底,用于与另一具有CMOS电路的芯片电连接,CMOS电路芯片主要包括了3D NAND存储器件的阵列芯片所需的电路,例如页缓存(page buffer)、解码器(decoder)、锁存(latches)以及外围电路等,贯通接触孔43例如可以由Ti/TiN和W来形成。

[0056] 由于在阶梯结构中设置了绝缘层,通过绝缘层将子阶梯区域和阶梯结构隔离开,绝缘层内仍为氧化物层和氮化物层的堆叠,从而易于贯通接触孔的形成,这种结构的贯通接触孔便于实现存储器件同CMOS芯片的连接,且易于同现有的工艺集成,特别是当堆叠层的厚度不断增加后,无需刻蚀金属堆叠来形成贯通接触孔,利于工艺的实现和集成度的不断提高。

[0057] 为了工艺的优化和集成,可以在阶梯结构40上,以及第一存储区10靠近阶梯结构的区域,形成了伪沟道孔48,这些伪沟道孔48可以与形成存储单元的沟道孔12一同形成,而后续并不在这些伪沟道孔上形成位线及互联线,他们并不用于真正的存储。

[0058] 为了更好地理解本发明实施例的技术方案,以下将结合具体的实施例进行详细的说明。

[0059] 实施例一

[0060] 参考图1所示,为本发明一个实施例的3D NAND存储器件芯片的俯视图示意图,在该具体的实施例中,存储器芯片包含了4个片(plate)存储区,在每个片(plate)存储区中包含

了多个块(block)存储区。可以理解的是,此处仅为示例,根据不同的设计,可以具有其他的设计排布方式,本发明并不限于此。

[0061] 参考图2所示,为图1中部分区域40的局部放大图,该图示中示出了阶梯结构和部分的第一存储区,在第一存储区10中,一个块被栅线缝隙分成三部分,每一对栅线缝隙之间为一个指(finger)存储区,第一存储区为3D NAND存储单元的阵列区域,可以包含有一个或多个的块存储区。

[0062] 在该实施例中,阶梯结构40的栅线缝隙46非等间距设置,子阶梯区域41设置于间距较大的栅线缝隙46之间,以使得子阶梯区域41与栅线缝隙46之间的空间用于互联结构的形成。

[0063] 在该实施例中,子阶梯区域41设置在了栅线缝隙之间,通常地,这个区域为一个指存储区的宽度,在设置子阶梯区域之后,可能会存在难以从阶梯将字线引出的问题,为此,将阶梯结构40的栅线缝隙46设置为非等间隔的间距,在一个块区域内,使得某个栅线缝隙之间的间隔更大些,这样,在设置子阶梯区域之后,在子阶梯区域41与栅线缝隙46之间还能存在一些空间,以用于互联结构的形成。

[0064] 实施例二

[0065] 在该实施例中,将描述与实施例一不同的部分,相同部分将不再赘述。

[0066] 参考图3所示,为图1中部分区域40的局部放大图,该图示中示出了阶梯结构和部分的第一存储区,在第一存储区10中,一个块被栅线缝隙分成三部分,每一对栅线缝隙之间为一个指(finger)存储区,第一存储区为3D NAND存储单元的阵列区域,可以包含有一个或多个的块存储区。

[0067] 子阶梯区域41设置于阶梯结构40的对应块区域的栅线缝隙之间,另一侧的阶梯结构(图未示出)的相应的区域用于互联结构的形成。也就是说,子阶梯区域41占据了第一存储区10的一个块区域所对应的阶梯结构区域,这样,可以形成较大面积的了阶梯区域,以供形成贯通接触孔43,却无法再用作字线的引出,而在阶梯结构40的另一侧也为同样的结构,在相应的区域,即在同一个块区域另一侧的阶梯结构的区域上形成该块区域的字线的引出,这种情况适用于X-DEC(字线解码)的设计为交错(zigzag)的设计。

[0068] 实施例三

[0069] 此外,还可以在位线方向上设置贯通接触孔的区域,以用于与CMOS电路芯片的连接,参考图1和图4所示,图4为图1中区域11的局部放大图,在第一存储区10和第二存储区30之间设置有通孔形成区20,第一存储区10、通孔形成区20和第二存储区30沿位线依次排布,同第一存储区10,第二存储区20包括字线堆叠层以及字线堆叠层中的沟道孔12;通孔形成区20包括氧化物层和氮化物层的通孔堆叠层24、贯穿通孔堆叠层24的贯通接触孔26以及通孔堆叠层的侧壁上的绝缘层22;第一存储区10和第二存储区20中沿字线方向的栅线缝隙16。

[0070] 同第一存储区10,第二存储区20为字线方向上的另一用于形成存储单元的阵列的区域,第二存储区20也设置栅线缝隙16。

[0071] 通孔形成区20设置在第一存储区10和第二存储区30之间,通孔形成区20中的堆叠层为氧化物层和氮化物层的堆叠,为了便于描述,记做通孔堆叠层24,通孔堆叠层24与存储堆叠层具有相同的层数,通孔堆叠层24的侧壁上为绝缘层22,这样,通过绝缘层22将通孔堆叠层24与存储堆叠层间隔开,在通过栅线缝隙16将存储区的堆叠进行替换时,通孔形成区

20内通孔堆叠层24仍保留。绝缘层22为介质材料,可以为单层或多层结构,例如可以为氧化物、氮化物等或他们的组合。

[0072] 在通孔堆叠层24中形成有贯通接触孔26,贯通接触孔26至少贯通了通孔堆叠层26,贯通接触孔26用于与另一具有CMOS电路的芯片电连接。

[0073] 此外,考虑到工艺的优化,参考图4所示,在第一存储区10和第二存储区20中靠近通孔形成区20的部分为伪存储区14。在该具体的实施例中,伪存储区14为一个指存储区,与实际的存储阵列的区域一样,伪存储区14包括相同的存储堆叠层以及存储堆叠层中的沟道孔,区别在于,伪存储区14并不进行后续的位线及互联线的形成,他们并不用于真正的存储。

[0074] 在该实施例中,通过绝缘层将存储区和贯通接触孔区域隔离开来,绝缘层内氧化物层和氮化物层的堆叠,而存储区域为形成存储单元的存储堆叠层,氧化物层和氮化物层的堆叠易于贯通接触孔的形成,这种结构的贯通接触孔便于实现存储器件同CMOS芯片的连接,且易于同现有的工艺集成,特别是当堆叠层的厚度不断增加后,无需刻蚀金属堆叠层来形成贯通接触孔,利于工艺的实现和集成度的不断提高。

[0075] 实施例四

[0076] 进一步的,还可以在第二存储区30内也进一步设置贯通接触孔,以下将详细描述第二存储区30及其中的贯通接触孔的结构,以下仅描述与上述实施例不同的部分,相同部分不再赘述。

[0077] 参考图1和图5所示,图5为图1中区域21的局部放大图,图6为一个实施例的剖面结构示意图,所述第二存储区30包括:

[0078] 块堆叠层,所述块堆叠层包括沿字线方向依次排布的第一区域110、第二区域120和第三区域130;其中,

[0079] 所述第二区域120位于所述第一区域110和第三区域130之间,所述第二区域120中形成有贯通的绝缘环160,所述绝缘环160内的块堆叠层102为相互间隔堆叠的氧化物层和氮化物层,贯穿所述绝缘环内的块堆叠层102的贯通接触孔162;

[0080] 所述绝缘环160外的第二区域120域以及第一区域110、第三区域130的块堆叠层为相互间隔堆叠的氧化物层和金属层,顶层的所述金属层为顶层选择栅,所述第一区域110和第三区域130中形成有沟道孔150,第一区域110和第三区域130中的块堆叠层为存储堆叠层;

[0081] 栅线缝隙170、172设置在绝缘环160外的块堆叠层中。

[0082] 在本发明实施例中,第一区域110、第二区域120和第三区域130在一个块存储区中,它们沿字线(word line)方向依次排布的,他们的堆叠层具有相同的层数,绝缘环内、外的堆叠层的材料不同。

[0083] 绝缘环160内的块堆叠层为氧化物层与氮化物层的堆叠,为用于形成贯通接触孔162的区域,贯通接触孔162至少贯通了块堆叠层,贯通接触孔162用于与另一具有CMOS电路的芯片电连接,贯通接触孔162例如可以由Ti/TiN和W来形成。

[0084] 由于在第二区域120中设置了绝缘环160,通过绝缘环160将环内和环外的块堆叠层隔离开,绝缘环160内为氧化物层和氮化物层的块堆叠层,绝缘环160外,包括绝缘环160外的第二区域120以及第一区域110、第三区域130的块堆叠层都为氧化物层和金属层的堆叠,绝缘环160内的氧化物层和氮化物层的堆叠易于贯通接触孔162的形成,而绝缘环外的

块堆叠层中的金属层保证了存储阵列字线的电连接,这种结构的贯通接触孔便于实现存储器件同CMOS芯片的连接,且易于同现有的工艺集成,特别是当堆叠层的厚度不断增加后,无需刻蚀金属堆叠层来形成贯通接触孔,利于工艺的实现和集成度的不断提高。

[0085] 可以根据具体的设计需要,在合适的位置来设置绝缘环,在一个优选的实施例中,参考图5所示,所述绝缘环160设置于相互平行的相邻的栅线缝隙之间,所述栅线缝隙170、172穿过第一区域110、第二区域120和第三区域130,且至少有一条栅线缝隙172在第二区域120处具有间断区171。

[0086] 在该实施例中,穿过第一区域110、第二区域120和第三区域130的栅线缝隙可以是连续贯穿这三个区域,也可以是连续穿过第一区域110和第二区域120、连续穿过第三区域130和第二区域120但在第二区域120处具有间断区171,参考图6所示,一条栅线缝隙170可以为连续贯穿、另一条栅线缝隙172为有间断的贯穿,也可以为两条栅线缝隙均为有间断的贯穿。

[0087] 在该优选实施例中,绝缘环160没有完全占据第二区域,这样,绝缘环160之外的第二区域120的块堆叠层中的顶层金属将第一区域和第二区域的顶层选择栅连接起来,绝缘环160两侧的第一区域和第二区域的顶层选择栅不会被绝缘环阻断。

[0088] 这样,在具体应用中,如图5所示,可以将块存储区内的栅线缝隙172都设置为有间断的贯穿,块存储区之间的栅线缝隙170设置为连续的贯穿,通过块存储区内的栅线缝隙172的间断区171将整个块存储区的字线连接起来了。这种方式无需额外的结构就可以实现顶层选择栅以及字线的连接,结构简单且易于实现,集成度更高。

[0089] 此外,为了便于工艺的优化,也可以在第一区域110和第三区域110靠近第二区域120的边缘部分的块堆叠层中设置伪沟道孔152,以及绝缘环160外的第二区域的块堆叠层中设置伪沟道孔156,这些伪沟道孔并不用于形成存储单元。

[0090] 实施例五

[0091] 对于本发明实施例,存储器件设置于基底之上,该基底至少起到支撑的作用,可以根据具体的设计来选择基底的结构,在一些实施例中,参考图6所示,所述基底包括第一衬底300及第一衬底300之上的外延衬底400,第一衬底300中形成了CMOS器件电路(图未示出)以及第一互联结构302,贯通接触孔进一步贯穿外延衬底400至第一衬底300中的第一互联结构302,贯通接触孔可以是上述实施例中的阶梯结构形成的、存储区中形成的或存储区之间形成的贯通接触孔中的一种或几种。

[0092] 在所述第一衬底300中已经形成了CMOS器件电路以及互联结构,该第一互联结构可以包括接触、一层或多层过孔、金属层,进而在第一衬底之上通过淀积的方式形成外延衬底400,外延衬底进一步用于上述存储器件的形成,该外延衬底400可以为单层或叠层结构,例如可以为单晶硅、多晶硅或多晶硅与金属层的叠层。进一步地,可以在与绝缘环内的区域对应的外延衬底的区域中设置开口402,以便于一种或多种贯通接触孔贯通至第一互联结构302。

[0093] 以上对本发明实施例的3D NAND存储器件进行了详细的描述,此外,本发明还提供了上述存储器件的制造方法。

[0094] 参考图7所示,在步骤S01,提供基底。

[0095] 在本发明实施例中,所述基底至少起到支撑作用,进一步地,还可以作为器件形成

的部件,例如可以为半导体衬底,进一步还可以已包括形成了器件电路的衬底。

[0096] 在一些实施例中,参考图6所示,所述基底可以包括第一衬底300和第一衬底300上的外延衬底400,第一衬底300中形成了CMOS器件电路以及第一互联结构302。该外延衬底400可以为单层或叠层结构,例如可以为单晶硅、多晶硅或多晶硅与金属层的叠层。

[0097] 为了便于后续集成贯通接触孔,参考图1-7,还进行了以下步骤:

[0098] 在外延衬底400上形成开口402,所述开口对应于字阶梯区域41的区域,开口中填充有介质材料,进一步地,开口还对应于第一存储区和第二存储区的绝缘环160内的区域,或者还对应于第一存储区和第二存储区之间的通孔形成区20。

[0099] 在步骤S02,在基底上形成氧化物层与氮化物层相互间隔的堆叠层,堆叠层具有第一存储区。

[0100] 可以采用合适的淀积方法依次堆叠氧化物层和氮化物层来形成堆叠层,堆叠层的层数根据垂直方向所需形成的存储单元的个数来确定。堆叠层中可以存在多个存储区,在本实施例中,可以至少具有沿字线方向排布的第一存储区10、通孔形成区20和第二存储区30。

[0101] 在步骤S03,在所述堆叠层的两侧形成堆叠层的阶梯结构。

[0102] 可以采用多次刻蚀的方法,在堆叠层的两侧形成阶梯结构,阶梯结构的阶梯面暴露出氮化物层,该氮化物层在后续的步骤中将被替换为金属层,以用于字线或其他金属层的连接。

[0103] 在步骤S04,在第一存储区10的堆叠层中形成沟道孔48以及在阶梯结构40中沿字线方向形成延伸至阶梯结构的边缘的绝缘层44,绝缘层44呈开口的条形图案,开口朝向阶梯结构40边缘,绝缘层内的区域为子阶梯区域41。

[0104] 在优选的实施例中,可以通过以下步骤来实现:

[0105] 在第一存储区的堆叠层中形成通孔,同时,在阶梯结构中沿字线方向形成延伸至阶梯结构边缘的沟槽,沟槽为呈开口的条形图案,开口朝向阶梯结构边缘,分别进行通孔和沟槽的填充,以分别形成沟道孔和绝缘层。这样,可以在形成沟道孔的同时形成绝缘层,简化工艺步骤。

[0106] 在该步骤中,参考图2-3,还可以同时在通孔形成区的堆叠层中形成沿字线方向延伸的绝缘层44,参考图4,以及第一存储区和第二存储区的在第二区域120的堆叠层中形成绝缘环160。同该优选的实施例,绝缘环及绝缘层的可以在沟道孔形成时进行,以简化工艺步骤,提高工艺集成度。该步骤中形成的沟道孔可以包括实际形成器件的沟道孔以及伪沟道孔,二者在结构上可以没有区别,伪沟道孔并不在后续工艺中形成位线等互联线。

[0107] 在步骤S05,形成栅线缝隙,通过栅线缝隙将第一存储区和绝缘层之外的阶梯结构中的氮化物层置换为金属层,同时,在栅线缝隙中填满金属层。

[0108] 在该步骤中,通过栅线缝隙将堆叠层中的氮化物层去除,进而填充进金属材料,如W等,形成金属层,作为字线,而由于绝缘层和绝缘环的隔离作用,子阶梯区域、通孔形成区和绝缘环内的堆叠层没有被去除和替换,仍然为氮化物和氧化物的堆叠,便于进行贯通接触孔的形成。

[0109] 根据不同的设置需求,可以在步骤S04和步骤S05中,通过不同的掩膜图案,形成不同结构的子阶梯结构的绝缘层和栅线缝隙,以及存储区内的栅线缝隙和绝缘环结构,参见

实施例一和实施例二、实施例四的描述,以满足不同的需求。

[0110] S06,形成贯通接触孔。

[0111] 绝缘层和绝缘环内的堆叠层为氧化物层与氮化物层的叠层,可以通过刻蚀技术刻蚀绝缘环内的堆叠层,直至暴露堆叠层下的区域,进而,进行金属材料的填充,例如W,来形成贯通接触孔。

[0112] 在一些实施例中,参考图6所示,所述基底包括第一衬底300和第一衬底300上的外延衬底400,外延衬底400中设置有开口,开口可以对应于阶梯区域、通孔形成区以及第一存储区和第二存储区中的绝缘环内的区域,开口中填充有介质材料,第一衬底中形成了CMOS器件电路以及第二互联结构,形成贯通接触孔的步骤包括:贯穿氮化物层和氧化物层的堆叠以及外延衬底开口中的介质材料直至第一衬底中的互联结构,以形成贯通接触孔,可以包括子阶梯区域中的贯通接触孔、通孔形成区内的贯通接触孔和绝缘环内的贯通接触孔。

[0113] 虽然本发明披露如上,但本发明并非限定于此。任何本领域技术人员,在不脱离本发明的精神和范围内,均可作各种更动与修改,因此本发明的保护范围应当以权利要求所限定的范围为准。

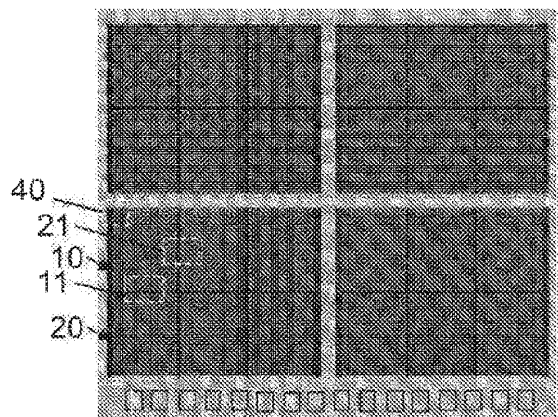


图1

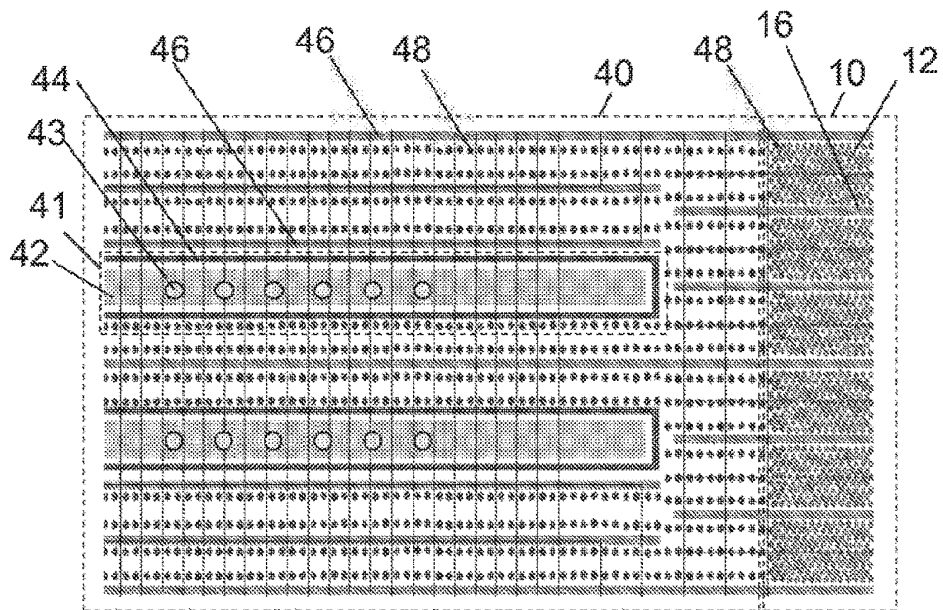


图2

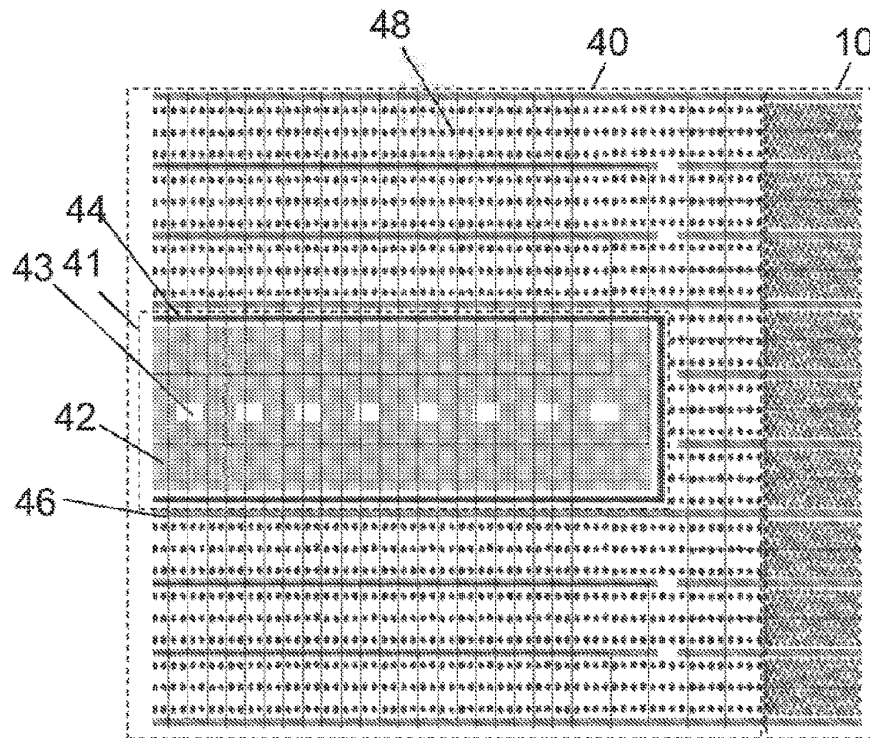


图3

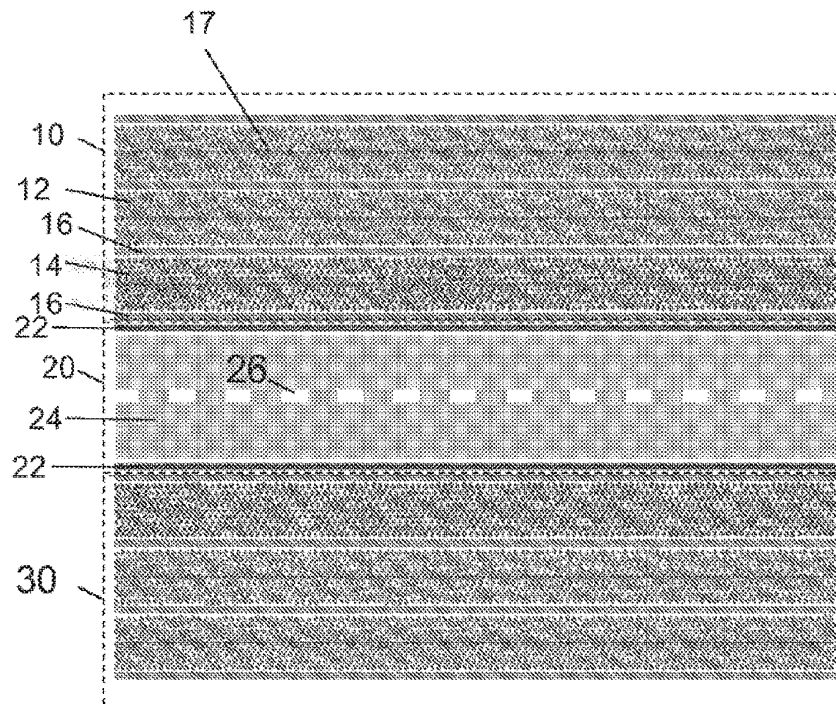


图4

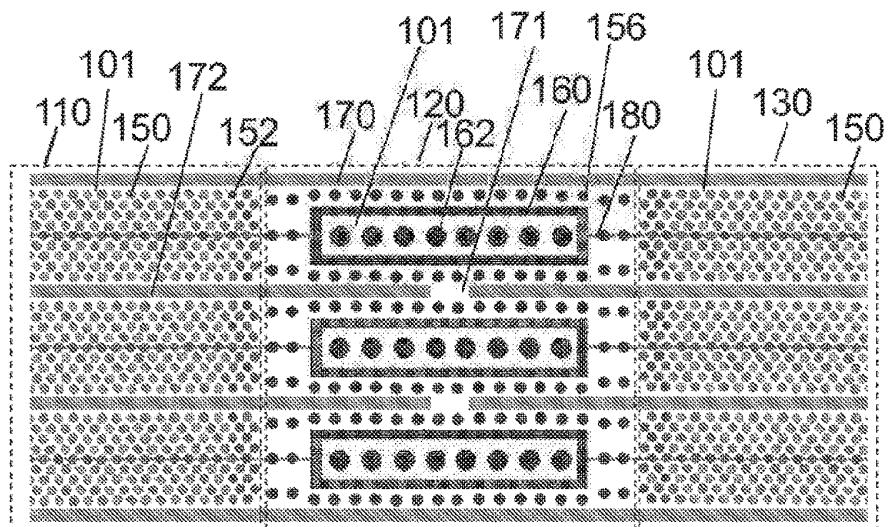


图5

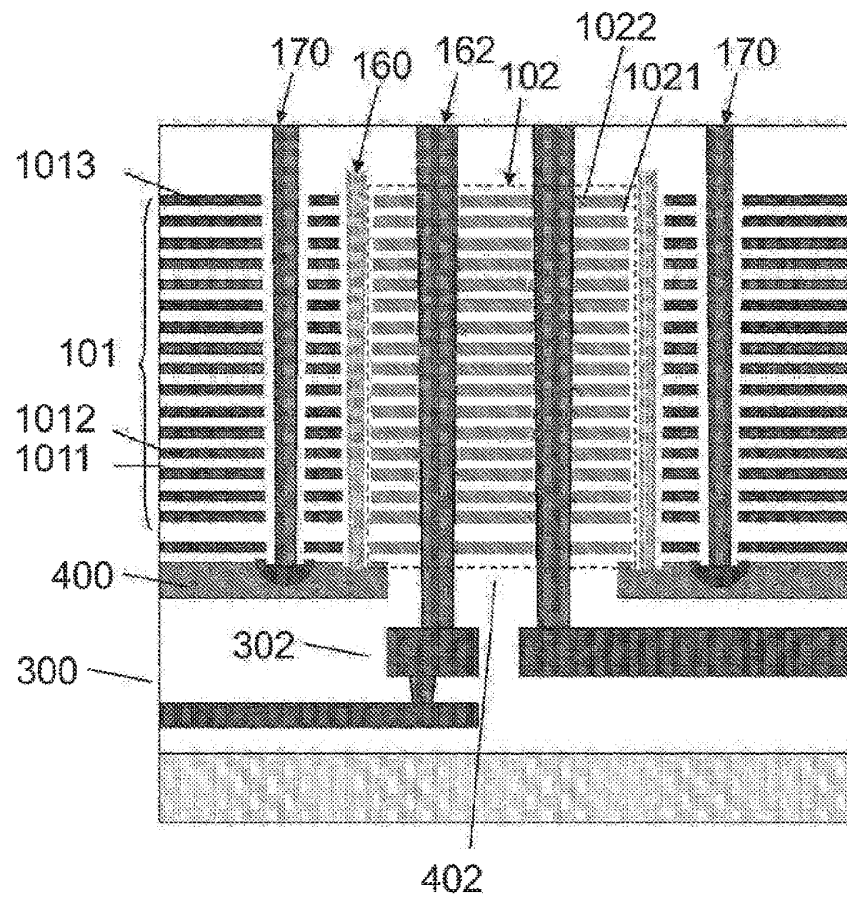


图6

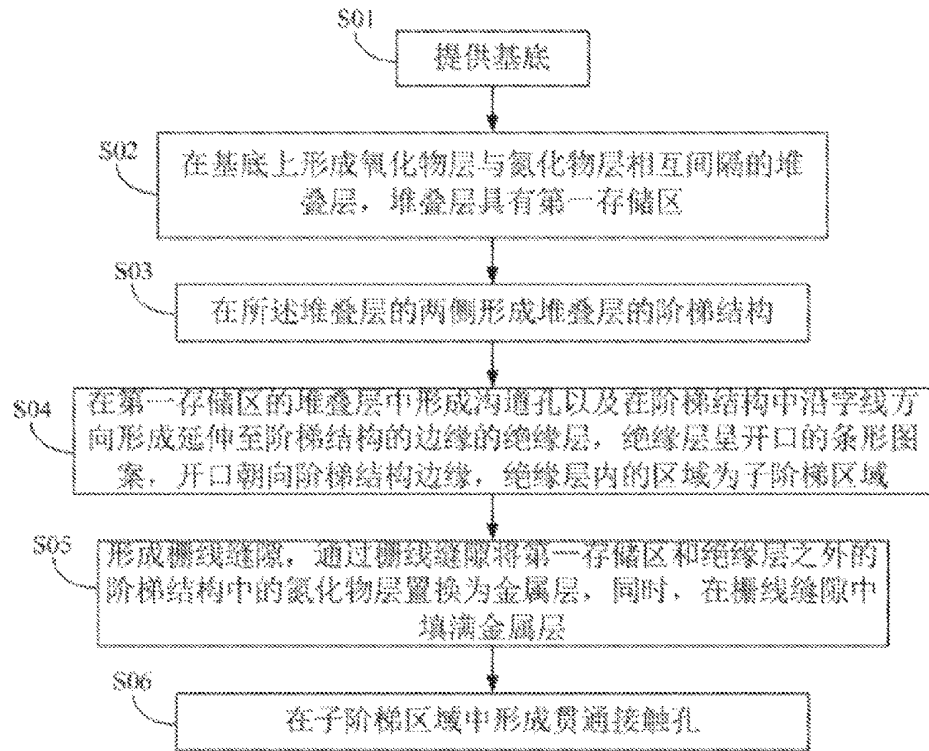


图7



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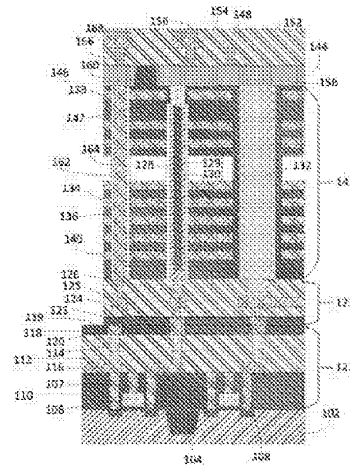
权利要求书3页 说明书12页 附图13页

(54)发明名称

NAND存储器及其制备方法

(57)摘要

本发明公开了一种NAND存储器,包括:等级层堆栈、NAND串、共源触点和源端导电层;所述等级层堆栈包括由导体层和绝缘层交替堆叠形成的导体/绝缘体叠层;所述NAND串和所述共源触点在垂直于所述等级层堆栈中的导体层或绝缘层的第一方向上延伸贯穿所述等级层堆栈;所述源端导电层覆盖所述等级层堆栈,并与所述NAND串第一端和所述共源触点的第一端接触,所述NAND串和所述共源触点通过所述源端导电层形成电性连接;所述源端导电层的导电区由金属、金属合金和金属硅化物中的一种或多种的组合构成。本发明旨在提高器件的操作速度以及外围器件对存储块的源端的驱动能力。



1. 一种NAND存储器, 其特征在于, 包括: 等级层堆栈、NAND串、共源触点和源端导电层; 所述等级层堆栈包括由导体层和绝缘层交替堆叠形成的导体/绝缘体叠层; 所述NAND串和所述共源触点在垂直于所述等级层堆栈中的导体层或绝缘层的第一方向上延伸贯穿所述等级层堆栈; 所述源端导电层覆盖所述等级层堆栈, 并与所述NAND串的第一端和所述共源触点的第一端接触, 所述NAND串和所述共源触点通过所述源端导电层形成电性连接; 所述源端导电层的导电区由金属、金属合金和金属硅化物中的一种或多种的组合构成。

2. 如权利要求1所述的NAND存储器, 其特征在于, 所述金属由铜、钴、镍、钛和钨中的一种或多种的组合构成。

3. 如权利要求1所述的NAND存储器, 其特征在于, 所述金属合金为铜、钴、镍、钛和钨中的至少两种金属构成的合金中的一种或多种的组合。

4. 如权利要求1所述的NAND存储器, 其特征在于, 所述金属硅化物由硅化钴、硅化镍、硅化钛和硅化钨中的一种或多种的组合构成。

5. 如权利要求1至4中任一项所述的NAND存储器, 其特征在于, 在所述NAND串和所述源端导电层间形成有硅外延层, 所述NAND串通过所述硅外延层与所述源端导电层形成电性连接。

6. 如权利要求1至4中任一项所述的NAND存储器, 其特征在于, 所述源端导电层具有多个导电区和隔离区, 所述多个导电区之间通过所述隔离区绝缘, 所述NAND串和所述共源触点通过所述多个导电区中的第一部分导电区实现电性连接。

7. 如权利要求6所述的NAND存储器, 其特征在于, 所述存储器还包括在所述第一方向上延伸贯穿所述等级层堆栈的贯穿阵列触点, 所述贯穿阵列触点与所述多个导电区中的第二部分导电区接触。

8. 如权利要求7所述的NAND存储器, 其特征在于, 所述存储器还包括第一互联层, 所述第一互联层具有第一导体层, 所述NAND串的第一端通过所述多个导电区中的第一部分导电区与所述第一导体层实现电性连接。

9. 如权利要求7所述的NAND存储器, 其特征在于, 所述存储器还包括第一互联层, 所述第一互联层具有第二导体层, 所述贯穿阵列触点通过所述多个导电区中的第二部分导电区与所述第二导体层实现电性连接。

10. 如权利要求1至4中任一项所述的NAND存储器, 其特征在于, 所述存储器还包括外围器件, 形成在所述NAND串的第二端和所述共源触点的第二端。

11. 如权利要求10所述的NAND存储器, 其特征在于, 所述存储器还包括与所述外围器件接触的第二互联层, 所述第二互联层包含一个或多个绝缘层, 以及形成在该一个或多个绝缘层中的一个或多个导体层。

12. 如权利要求11所述的NAND存储器, 其特征在于, 所述存储器还包括与所述NAND串的第二端和所述共源触点的第二端接触的第三互联层, 所述第三互联层包含一个或多个绝缘层, 以及形成在该一个或多个绝缘层中的一个或多个导体层。

13. 如权利要求12所述的NAND存储器, 其特征在于, 所述第二互联层和所述第三互联层间形成有粘结界面, 所述外围器件与所述NAND串和所述共源触点通过所述第二互联层和所述第三互联层形成电性连接。

14. 一种NAND存储器的制备方法, 其特征在于, 包括如下步骤:

在第一硅基板上形成等级层堆栈；

形成垂直贯穿等级层堆栈的NAND串和共源触点；

将第一硅基板替换为源端导电层；所述源端导电层与所述NAND串的第一端和所述共源触点的第一端接触，所述NAND串和所述共源触点通过所述源端导电层形成电性连接；所述源端导电层由金属、金属合金和金属硅化物中的一种或多种的组合构成。

15. 如权利要求14所述的NAND存储器的制备方法，其特征在于，所述将第一硅基板替换为源端导电层的步骤进一步包括：

去除第一硅基板；

在原来第一硅基板的位置形成源端导电层。

16. 如权利要求15所述的NAND存储器的制备方法，其特征在于，所述去除第一硅基板的步骤具体为：首先减薄第一硅基板，然后再去除减薄后的第一硅基板。

17. 如权利要求14所述的NAND存储器的制备方法，其特征在于，所述将第一硅基板替换为源端导电层的步骤进一步包括：

在第一硅基板上形成金属层；

使第一硅基板中的硅与金属层中的金属合金化形成金属硅化物，得到源端导电层。

18. 如权利要求17所述的NAND存储器的制备方法，其特征在于，所述在第一硅基板上形成金属层的步骤包括：首先减薄第一硅基板，然后在减薄后的第一硅基板上形成金属层。

19. 如权利要求18所述的NAND存储器的制备方法，其特征在于，所述在第一硅基板上形成金属层的步骤具体为：在第一硅基板与等级层堆栈接触的一端形成有由绝缘材料构成的隔离区，减薄第一硅基板，直至第一硅基板的隔离区露出，在减薄后的第一硅基板上形成金属层。

20. 如权利要求14至19中任一项所述的NAND存储器的制备方法，其特征在于，所述方法还包括：去除选定区域中的源端导电层材料，在源端导电层上形成隔离区图案，向隔离区图案中填充绝缘材料，在源端导电层中形成隔离区。

21. 如权利要求14至19中任一项所述的NAND存储器的制备方法，其特征在于，所述方法还包括：

在第二硅基板上形成外围器件；

使所述外围器件形成在所述NAND串的第二端和所述共源触点的第二端。

22. 如权利要求21所述的NAND存储器的制备方法，其特征在于，所述使所述外围器件形成在所述NAND串的第二端和所述共源触点的第二端的步骤进一步包括：

在所述NAND串的第二端和所述共源触点的第二端形成第一互联层；

形成与所述外围器件接触的第二互联层；

在第一互联层和第二互联层间形成粘结界面，使所述外围器件与所述NAND串和所述共源触点通过第一互联层和第二互联层形成电性连接。

23. 如权利要求22所述的NAND存储器的制备方法，其特征在于，所述第一互联层包含一个或多个绝缘层，以及形成在该一个或多个绝缘层中的一个或多个导体层；所述第二互联层包含一个或多个绝缘层，以及形成在该一个或多个绝缘层中的一个或多个导体层。

24. 如权利要求23所述的NAND存储器的制备方法，其特征在于，所述在第一互联层和第二互联层间形成粘结界面的步骤进一步包括：使第一互联层中的绝缘层和第二互联层中的

绝缘层形成化学键合,和/或使第一互联层中的导体层和第二互联层中的导体层进行物理互扩散。

NAND存储器及其制备方法

技术领域

[0001] 本发明涉及一种NAND存储器及其制备方法,尤其涉及一种形成3D NAND闪存的NAND存储器及其制备方法。

背景技术

[0002] 随着对高度集成电子装置的持续重视,对以更高的速度和更低的功率运行并具有增大的器件密度的半导体存储器件存在持续的需求。为达到这一目的,已经发展了具有更小尺寸的器件和具有以水平和垂直阵列布置的晶体管单元的多层器件。3D NAND是业界所研发的一种新兴的闪存类型,通过垂直堆叠多层数据存储单元来解决2D或者平面NAND闪存带来的限制,其具备卓越的精度,支持在更小的空间内容纳更高的存储容量,可打造出存储容量比同类NAND技术高达数倍的存储设备,进而有效降低成本和能耗,能全面满足众多消费类移动设备和要求最严苛的企业部署的需求。

[0003] 现有的3D NAND存储器中,利用源极选择门控制硅基板上源端通道的导通与关断,进而将电流由NAND串传导至共源触点。上述结构存在如下问题:1、通过源极选择门控制源端通道的导通与关断,源端通道从关断到导通需要一定的时间,且受源极选择门控制导通的源端通道的电阻较大,导致器件的操作速度下降;2、受源极选择门控制导通的源端通道的电阻较大,由于整个存储块共享一个下选择栅,外围CMOS器件驱动整个存储块的源端难度较大。

发明内容

[0004] 本发明提供了一种NAND存储器及其制备方法,旨在提高器件的操作速度以及外围器件对存储块的源端的驱动能力。

[0005] 按照本发明的一个方面,提供了一种NAND存储器,包括:等级层堆栈、NAND串、共源触点和源端导电层;所述等级层堆栈包括由导体层和绝缘层交替堆叠形成的导体/绝缘体叠层;所述NAND串和所述共源触点在垂直于所述等级层堆栈中的导体层或绝缘层的第一方向上延伸贯穿所述等级层堆栈;所述源端导电层覆盖所述等级层堆栈,并与所述NAND串的第一端和所述共源触点的第一端接触,所述NAND串和所述共源触点通过所述源端导电层形成电性连接;所述源端导电层的导电区由金属、金属合金和金属硅化物中的一种或多种的组合构成。

[0006] 优选地,所述金属由铜、钴、镍、钛和钨中的一种或多种的组合构成。

[0007] 优选地,所述金属合金为铜、钴、镍、钛和钨中的至少两种金属构成的合金中的一种或多种的组合。

[0008] 优选地,所述金属硅化物由硅化钴、硅化镍、硅化钛和硅化钨中的一种或多种的组合构成。

[0009] 优选地,在所述NAND串和所述源端导电层间形成有硅外延层,所述NAND串通过所述硅外延层与所述源端导电层形成电性连接。

[0010] 优选地,所述源端导电层具有多个导电区和隔离区,所述多个导电区之间通过所述隔离区绝缘,所述NAND串和所述共源触点通过所述多个导电区中的第一部分导电区实现电性连接。

[0011] 优选地,所述存储器还包括在所述第一方向上延伸贯穿所述等级层堆栈的贯穿阵列触点,所述贯穿阵列触点与所述多个导电区中的第二部分导电区接触。

[0012] 优选地,所述存储器还包括第一互联层,所述第一互联层具有第一导体层,所述NAND串的第一端通过所述多个导电区中的第一部分导电区与所述第一导体层实现电性连接。

[0013] 优选地,所述存储器还包括第一互联层,所述第一互联层具有第二导体层,所述贯穿阵列触点通过所述多个导电区中的第二部分导电区与所述第二导体层实现电性连接。

[0014] 优选地,所述存储器还包括外围器件,形成在所述NAND串的第二端和所述共源触点的第二端。

[0015] 优选地,所述存储器还包括与所述外围器件接触的第二互联层,所述第二互联层包含一个或多个绝缘层,以及形成在该一个或多个绝缘层中的一个或多个导体层。

[0016] 优选地,所述存储器还包括与所述NAND串的第二端和所述共源触点的第二端接触的第三互联层,所述第三互联层包含一个或多个绝缘层,以及形成在该一个或多个绝缘层中的一个或多个导体层。

[0017] 优选地,所述第二互联层和所述第三互联层间形成有粘结界面,所述外围器件与所述NAND串和所述共源触点通过所述第二互联层和所述第三互联层形成电性连接。

[0018] 按照本发明的另一方面,提供了一种NAND存储器的制备方法,包括如下步骤:

[0019] 在第一硅基板上形成等级层堆栈;

[0020] 形成垂直贯穿等级层堆栈的NAND串和共源触点;

[0021] 将第一硅基板替换为源端导电层;所述源端导电层与所述NAND串的第一端和所述共源触点的第一端接触,所述NAND串和所述共源触点通过所述源端导电层形成电性连接;所述源端导电层由金属、金属合金和金属硅化物中的一种或多种的组合构成。

[0022] 优选地,所述将第一硅基板替换为源端导电层的步骤进一步包括:

[0023] 去除第一硅基板;

[0024] 在原来第一硅基板的位置形成源端导电层。

[0025] 优选地,所述去除第一硅基板的步骤具体为:首先减薄第一硅基板,然后再去除减薄后的第一硅基板。

[0026] 优选地,所述将第一硅基板替换为源端导电层的步骤进一步包括:

[0027] 在第一硅基板上形成金属层;

[0028] 使第一硅基板中的硅与金属层中的金属合金化形成金属硅化物,得到源端导电层。

[0029] 优选地,所述在第一硅基板上形成金属层的步骤包括:首先减薄第一硅基板,然后在减薄后的第一硅基板上形成金属层。

[0030] 优选地,所述在第一硅基板上形成金属层的步骤具体为:在第一硅基板与等级层堆栈接触的一端形成有由绝缘材料构成的隔离区,减薄第一硅基板,直至第一硅基板的隔离区露出,在减薄后的第一硅基板上形成金属层。

- [0031] 优选地,所述方法还包括:去除选定区域中的源端导电层材料,在源端导电层上形成隔离区图案,向隔离区图案中填充绝缘材料,在源端导电层中形成隔离区。
- [0032] 优选地,所述方法还包括:
- [0033] 在第二硅基板上形成外围器件;
- [0034] 使所述外围器件形成在所述NAND串的第二端和所述共源触点的第二端。
- [0035] 优选地,所述使所述外围器件形成在所述NAND串的第二端和所述共源触点的第二端的步骤进一步包括:
- [0036] 在所述NAND串的第二端和所述共源触点的第二端形成第一互联层;
- [0037] 形成与所述外围器件接触的第二互联层;
- [0038] 在第一互联层和第二互联层间形成粘结界面,使所述外围器件与所述NAND串和所述共源触点通过第一互联层和第二互联层形成电性连接。
- [0039] 优选地,所述第一互联层包含一个或多个绝缘层,以及形成在该一个或多个绝缘层中的一个或多个导体层;所述第二互联层包含一个或多个绝缘层,以及形成在该一个或多个绝缘层中的一个或多个导体层。
- [0040] 优选地,所述在第一互联层和第二互联层间形成粘结界面的步骤进一步包括:使第一互联层中的绝缘层和第二互联层中的绝缘层形成化学键合,和/或使第一互联层中的导体层和第二互联层中的导体层进行物理互扩散。
- [0041] 与现有技术相比,本发明具有以下有益效果:
- [0042] (1) 用高电导率的源端导电层代替硅基板上的源端通道,实现共源触点与NAND串的连接,由于高电导率的源端导电层的存在,共源触点与硅外延层间具有良好的导电性,有利于提高器件的操作速度;
- [0043] (2) 高电导率的源端导电层材料可以为金属、金属合金和金属硅化物中的一种或多种的组合,也可以为其它高电导率材料。可以根据设计需要,对高电导率的源端导电层进行图形化,得到合适的源端导电层结构以驱动单个存储块、多个存储块、或存储块的部分;
- [0044] (3) 共源触点与硅外延层直接通过高电导率的源端导电层连接,源极选择门在擦除模式下可以利用栅诱导漏电流驱动导电;
- [0045] (4) 由于源端导电层具有高电导率,其除了用于实现共源触点与NAND串的连接之外,还可以被用作额外导电层,并可根据实际电路设计需要对源端导电层进行图形化,以实现额外的走线功能。

附图说明

- [0046] 通过阅读下文优选实施方式的详细描述,各种其他的优点和益处对于本领域普通技术人员将变得清楚明了。附图仅用于示出优选实施方式的目的,而并不认为是对本发明的限制。而且在整个附图中,用相同的参考符号表示相同的部件。在附图中:
- [0047] 图1是根据本发明实施方式的NAND存储器的结构示意图;
- [0048] 图2A-2D是根据本发明实施方式的NAND存储器的外围器件和外围互联层的制备步骤示意图;
- [0049] 图3A-3D是根据本发明实施方式的NAND存储器的阵列器件和阵列互联层的制备步骤示意图;

[0050] 图4A-4D是根据本发明实施方式的阵列器件与外围器件粘结得到NAND存储器的制备步骤示意图；

[0051] 图5是形成外围器件和外围互联层的示例方法500的流程图；

[0052] 图6是形成阵列器件和阵列互联层的示例方法600的流程图；

[0053] 图7是结合阵列器件和外围器件的示例方法700的流程图。

具体实施方式

[0054] 下文将参照附图更充分地描述本发明的实施例，本发明的优选实施例在附图中示出。然而，本发明可以以不同的方式实施，而不应被解释为仅限于此处所述的实施例。在整个说明书中相同的附图标记始终指代相同的元件。

[0055] 应当理解，虽然这里可使用术语第一、第二等描述各种元件，但这些元件不应受限于这些术语。这些术语用于使一个元件区别于另一个元件。例如，第一元件可以称为第二元件，类似地，第二元件可以称为第一元件，而不背离本发明的范围。如此处所用的，术语“和/或”包括一个或多个所列相关项目的任意及所有组合。

[0056] 应当理解，当称一个元件在另一元件“上”、“连接到”或“耦合到”另一元件时，它可以直接在另一元件上或者连接到或耦合到另一元件，或者还可以存在插入的元件。相反，当称一个元件“直接在”另一元件上或者“直接连接到”或“直接耦合到”另一元件时，不存在插入的元件。其他的用于描述元件之间关系的词语应当以类似的方式解释（例如，“在...之间”相对于“直接在...之间”、“相邻”相对于“直接相邻”等）。这里当称一个元件在另一元件上时，它可以在另一元件上或下，直接耦合到另一元件，或者可以存在插入的元件，或者元件可以通过空隙或间隙分隔开。

[0057] 这里所用的术语仅仅是为了描述特定实施例，并非要限制本发明。如此处所用的，除非上下文另有明确表述，否则单数形式“一”和“该”均同时旨在包括复数形式。还应当理解，术语“包括”、“包括”、“包括”和/或“包括”，当在此处使用时，指定了所述特征、整体、步骤、操作、元件和/或组件的存在，但并不排除一个或多个其他的特征、整体、步骤、操作、元件、组件和/或其组合的存在或添加。

[0058] 本发明一个实施例的NAND存储器的结构示意图如图1所示。包括一个第一硅基板102。在一些实施例中，第一硅基板102可由单晶硅制成。在一些实施例中，第一硅基板102可由其他合适的材料制成，例如但不限于，硅锗、锗或绝缘体上硅薄膜（SOI）。外围器件形成在第一硅基板102上。所述外围器件包括多个晶体管106。在一些实施例中，第一硅基板102上形成有隔离区104和掺杂区108。外围互联层122覆盖晶体管106以进行电信号传导。外围互联层122包括一个或多个层间绝缘层，例如绝缘层110、112和118。外围互联层122进一步包括层间绝缘层中的一个或多个触点，例如触点107和触点114，以及一个或多个互联导体层，例如层116和120。触点和互联导体层由导电材料制成，可以为钨、钴、铜、铝和金属硅化物中的一种或多种的组合，也可以为其他合适的材料。层间绝缘层由绝缘材料制成，可以为氧化硅、氮化硅、氮氧化硅和掺杂氧化硅中的一种或多种的组合，也可以为其他合适的材料。

[0059] 阵列器件形成在外围器件之上。阵列器件包括多个NAND串130，其延伸贯穿等级层堆栈142。在一些实施例中，等级层堆栈142包括由多个交替堆叠的导体层134和绝缘层136构成的导体/绝缘体叠层。在一些实施例中，等级层堆栈142还包括导体/绝缘体叠层之外的

导体层和/或绝缘层。在一些实施例中,等级层堆栈142中的导体/绝缘体叠层之外的导体层与导体/绝缘体叠层内的导体层由不同的材料制成和/或具有不同的厚度。在一些实施例中,等级层堆栈142中的导体/绝缘体叠层之外的绝缘层与导体/绝缘体叠层内的绝缘层由不同的材料制成和/或具有不同的厚度。

[0060] 在一些实施例中,等级层堆栈142中一些位置的导体/绝缘体叠层与另一些位置的导体/绝缘体叠层由不同的材料制成和/或具有不同的厚度,例如,等级层堆栈中一些位置的导体/绝缘体叠层中的绝缘层的厚度为5-40nm,导体层的厚度为5-40nm;另一些位置的导体/绝缘体叠层中的绝缘层的厚度为10-40nm,导体层的厚度为10-40nm;又一些位置的导体/绝缘体叠层中的绝缘层的厚度为50-200nm,导体层的厚度为5-40nm。

[0061] 在一些实施例中,导体层由导电材料制成,可以为钨、钴、铜、铝、掺杂硅和金属硅化物中的一种或多种的组合,也可以为其他合适的材料。绝缘层由绝缘材料制成,可以为氧化硅、氮化硅和氮氧化硅中的一种或多种的组合,也可以为其他合适的材料。

[0062] NAND串130包括半导体通道层128和介质层129。在一些实施例中,半导体通道层128由非晶硅、多晶硅或单晶硅制成。在一些实施例中,介质层129包括隧道层、存储单元层和阻隔层。在一些实施例中,所述隧道层包括绝缘材料,包括但不限于氧化硅、氮化硅或氮氧化硅,或者上述材料的组合。在一些实施例中,隧道层的厚度为5-15nm,半导体通道中的电子或空穴可以通过这层隧道层隧穿至NAND串的存储单元层中。在一些实施例中,存储单元层可以用于存储操作NAND的电荷,存储单元层中的电荷的存储或是移除决定了半导体通道的开关状态。存储单元层的材料包括但不限于氮化硅、氮氧化硅或硅,或者以上材料的组合。在一些实施例中,存储单元层的厚度为3-15nm。在一些实施例中,阻隔层材料为氧化硅、氮化硅或高介电常数绝缘材料,或者多种以上材料的组合。例如一个氧化硅层或一个包含氧化硅/氮化硅/氧化硅(ONO)三层的厚度为4-15nm的复合层。在一些实施例中,阻隔层可以进一步包括一个高K介电层(例如厚度为1-5nm的氧化铝)。

[0063] 在一些实施例中,等级层堆栈142中的导体层用作多个NAND串的选择门或字线。在一些实施例中,等级层堆栈142中的导体层134用作NAND串的字线。在一些实施例中,等级层堆栈142中的形成在NAND串的一端的导体层138用作NAND串的源极选择门。在一些实施例中,等级层堆栈142中的形成在NAND串的另一端的导体层140用作NAND串的漏极选择门。

[0064] 阵列器件进一步包括一个或多个共源触点132,其延伸贯穿等级层堆栈142。在一些实施例中,共源触点132由导电材料制成,可以为钨、钴、铜、铝和金属硅化物中的一种或多种的组合,也可以为其他合适的导电材料。在一些实施例中,共源触点132和等级层堆栈142间形成有绝缘层以达到隔离目的。

[0065] 在一些实施例中,阵列器件进一步包括覆盖等级层堆栈142的源端导电层144。在一些实施例中,共源触点132和NAND串130均与源端导电层144接触。在一些实施例中,源端导电层144的导电区由高电导率材料构成,其导电性能不受源极选择门控制,并使得共源触点132与NAND串130能够形成良好的电性连接。在一些实施例中,源端导电层144的导电区由金属、金属合金和金属硅化物中的一种或多种的组合构成,也可以由其他高电导率材料构成。在一些实施例中,构成源端导电层144的导电区的金属由铜、钴、镍、钛和钨中的一种或多种的组合构成,也可以为其他合适的金属材料。在一些实施例中,构成源端导电层144的导电区的金属合金为铜、钴、镍、钛和钨中的至少两种金属构成的合金中的一种或多种的组

合(例如,所述金属合金可以为钛镍合金,也可以为钛镍合金和钛钨合金的组合),也可以为其他合适的金属合金材料。在一些实施例中,构成源端导电层144的导电区的金属硅化物由硅化钴、硅化镍、硅化钛和硅化钨中的一种或多种的组合构成,也可以由其他合适的金属硅化物材料构成。

[0066] 在一些实施例中,源端导电层144具有多个导电区(例如导电区158和导电区160)和隔离区(例如隔离区146),多个导电区之间通过隔离区绝缘。在一些实施例中,采用光刻和干法/湿法刻蚀工艺去除选定区域中的导电层材料,形成隔离区图案,并向隔离区图案中填充绝缘材料形成隔离区146,与此相对应地,形成被隔离区146绝缘的多个导电区158和160。在一些实施例中,采用热生长和/或薄膜淀积工艺形成隔离区146。在一些实施例中,隔离区146的材料为氧化硅、氮化硅、氮氧化硅和掺杂氧化硅中的一种或多种的组合,也可以为其他合适的材料。在一些实施例中,NAND串130和共源触点132通过导电区158实现电性连接。在一些实施例中,根据设计需要,在源端导电层144中形成不同的隔离区图案,以得到合适的源端导电层结构,驱动单个存储块、多个存储块、或存储块的部分。

[0067] 阵列器件进一步包括一个或多个贯穿阵列触点162,其延伸贯穿等级层堆栈142。在一些实施例中,通过湿法/干法刻蚀工艺形成贯穿等级层堆栈142的开口后,用导体材料填充所述开口,形成贯穿阵列触点162。在一些实施例中,贯穿阵列触点162和等级层堆栈142间形成有绝缘层164以达到隔离目的。在一些实施例中,贯穿阵列触点162包含导电材料,所述导电材料包括但不限于钨、钴、铜、铝、掺杂硅、硅化物或以上材料的组合。在一些实施例中,可以采用ALD、CVD、PVD和/或其他合适的方法使导体材料或者其他材料填充所述开口。

[0068] 在一些实施例中,根据设计需要,在源端导电层144中形成不同的隔离区图案,以得到合适的源端导电层结构,使源端导电层在连接共源触点与NAND串之外,实现其他的电性连接功能。在一些实施例中,贯穿阵列触点162与导电区160接触,有助于实现贯穿阵列触点162与互联层的电性连接。

[0069] 在一些实施例中,阵列器件进一步包括形成在NAND串130和源端导电层144间的硅外延层147,NAND串130通过硅外延层147与源端导电层144形成电性连接。

[0070] 阵列器件和外围互联层122间形成有阵列互联层123。在一些实施例中,阵列互联层123包括一个或多个绝缘层(例如绝缘层125和绝缘层121)。阵列互联层123进一步包括绝缘层中的一个或多个位线触点126,以及一个或多个导体层(例如层124)。所述导体层可以由导电材料制成,具体可以由钨、钴、铜、铝和金属硅化物中的一种或多种的组合构成,也可以由其他合适的材料构成。所述绝缘层由绝缘材料制成,具体可以由氧化硅、氮化硅和高介电常数绝缘材料中的一种或多种的组合构成,也可以由其他合适的材料构成。

[0071] 粘结界面119形成在外围互联层122的绝缘层118和阵列互联层123的绝缘层121之间。在一些实施例中,粘结界面119也可以形成在导体层124和导体层120之间。在一些实施例中,绝缘层118是氮化硅层而绝缘层121是氧化硅层。在一些实施例中,绝缘层118是氧化硅层而绝缘层121是氮化硅层。

[0072] 在一些实施例中,位线触点126与NAND串130接触,进而可通过位线触点独立寻址每个NAND串。

[0073] 在一些实施例中,阵列器件进一步包括后段制程互联层。在一些实施例中,后段制

程互联层包括一个或多个后段制程绝缘层(例如绝缘层152)。后段制程互联层进一步包括后段制程导体层(例如导体层148、154、166和168)和后段制程衬垫层(例如衬垫层156)。所述后段制程互联层在所述NAND存储器和外部电路之间传送电信号。在一些实施例中,后段制程导体层和衬垫层均由导电材料制成,具体可以由钨、钴、铜、铝和金属硅化物中的一种或多种的组合构成,或者由其他合适的材料构成。在一些实施例中,后段制程绝缘层由绝缘材料制成,具体可以由氧化硅、氮化硅和高介电常数绝缘材料中的一种或多种的组合构成,或者由其他合适的材料构成。

[0074] 在一些实施例中,源端导电层144可以作为后段制程互联层的一部分。在一些实施例中,导电区158连接除NAND中130和共源触点132外的其他结构,例如导体层148,实现NAND存储器和其他电路(例如后段互联层154等)的电性连接。在一些实施例中,导电区160连接导体层166,实现贯穿阵列触点162和其他电路(例如后段互联层168)的电性连接。在一些实施例中,贯穿阵列触点162将电信号从外围器件传输到后段互联层或衬垫层。

[0075] 图2A-2D是根据本发明实施方式的NAND存储器的外围器件和外围互联层的制备步骤示意图;图5是形成外围器件和外围互联层的示例方法500的流程图。

[0076] 示例方法500开始于操作502,如图5所示,即在第一硅基板上形成外围器件。如图2A所示,首先提供了第一硅基板202,用以形成外围器件。在一些实施例中,外围器件包括多个晶体管器件204。所述多个晶体管器件204形成在第一硅基板202上。在一些实施例中,形成晶体管器件204包括多个步骤,包括但不限于光刻、干法/湿法刻蚀、薄膜沉淀、热生长、注入、化学机械平坦化(CMP)、和/或以上的组合。在一些实施例中,掺杂区208也形成在第一硅基板202上。在一些实施例中,隔离区206也形成在第一硅基板202上。

[0077] 示例方法500继续于操作504,如图5所示,在外围器件上形成一个或多个绝缘层和导体层。所述一个或多个绝缘层和导体层是外围互联层的一部分,能够传输外围器件的电信号。如图2B所示,第一层绝缘层210形成在第一硅基板202上,接触层209形成并电性连接外围器件。如图2C所示,第二绝缘层216形成在第一绝缘层210上。在一些实施例中,第二绝缘层216可以是多个层的组合并且由独立步骤形成。在一些实施例中,导体层212、接触层209和导体层214由导电材料制成。形成导体层和接触层的工艺可以使用薄膜沉淀工艺,包括但不限于化学气相沉积法(CVD)、物理气相沉积法(PVD)、或原子层沉积法(ALD)和电镀工艺。形成导体层和接触层的工艺也可以使用光刻、化学机械平坦化、干法/湿法刻蚀。形成绝缘层的工艺可以使用薄膜沉淀工艺,包括但不限于化学气相沉积法(CVD)、物理气相沉积法(PVD)、或原子层沉积法(ALD)。

[0078] 示例方法500继续于操作506,如图5所示,形成外围互联层的一个顶部绝缘层和一个顶部导体层。如图2D所示,第三绝缘层218形成在第二绝缘层216上,导体层220形成在第三绝缘层218内。如此形成了外围互联层222。形成导体层的工艺可以使用薄膜沉淀工艺,包括但不限于化学气相沉积法(CVD)、物理气相沉积法(PVD)、或原子层沉积法(ALD)和电镀工艺。形成导体层的工艺也可以使用光刻、化学机械平坦化、干法/湿法刻蚀。形成绝缘层的工艺可以使用薄膜沉淀工艺,包括但不限于化学气相沉积法(CVD)、物理气相沉积法(PVD)、或原子层沉积法(ALD)。

[0079] 图3A-3D是根据本发明实施方式的NAND存储器的阵列器件和阵列互联层的制备步骤示意图;图6是形成阵列器件和阵列互联层示例方法600的流程图。

[0080] 示例方法600开始于操作602,如图6所示,在第二硅基板上形成隔离区。如图3A所示,第二硅基板302用于形成阵列器件。在一些实施例中,第二硅基板302可由单晶硅制成。在一些实施例中,第二硅基板302可由其他合适的材料制成,例如但不限于,硅锗、锗或绝缘体上硅薄膜(SOI)。在一些实施例中,隔离区304形成在第二硅基板302上。在一些实施例中,形成隔离区304的工艺可以采用热生长和/或薄膜沉淀。在一些实施例中,光刻和干法/湿法刻蚀工艺可用于形成隔离区图案。

[0081] 示例方法600继续于操作604,如图6所示,在第二硅基板上形成等级层堆栈。在一些实施例中,等级层堆栈306包括由多个交替堆叠的第一绝缘层308和第二绝缘层310构成的绝缘层对。在一些实施例中,等级层堆栈306还包括绝缘层对之外的一层或多层绝缘层。在一些实施例中,等级层堆栈306中的绝缘层对之外的绝缘层与绝缘层对内的绝缘层由不同的材料制成和/或具有不同的厚度。在一些实施例中,等级层堆栈306中一些位置的绝缘层对与另一些位置的绝缘层对由不同的材料制成和/或具有不同的厚度,例如,等级层堆栈中一些位置的绝缘层对中的第一绝缘层的厚度为5-40nm,第二绝缘层的厚度为5-40nm;另一些位置的绝缘层对中的第一绝缘层的厚度为10-40nm,第二绝缘层的厚度为10-40nm;又一些位置的绝缘层对中的第一绝缘层的厚度为50-200nm,第二绝缘层的厚度为5-40nm。在一些实施例中,等级层堆栈306中的绝缘层材料为氮化硅、氧化硅和氮氧化硅中的一种或多种的组合。在一些实施例中,第一绝缘层308为氮化硅层,第二绝缘层310为氧化硅层。在一些实施例中,形成等级层堆栈306的工艺可以使用薄膜沉淀工艺,包括但不限于化学气相沉积法(CVD)、物理气相沉积法(PVD)、或原子层沉积法(ALD)。

[0082] 示例方法600继续于操作606,如图6所示,在第二硅基板上形成多个阵列器件的NAND串。如图3C所示,多个NAND串318形成在第二硅基板302上。在一些实施例中,等级层堆栈306的绝缘层对中的第一绝缘层308可以替换为导体层,从而在等级层堆栈314中形成多个导体/绝缘体层对。在一些实施例中,使用导体层替换第一绝缘层308的工艺可以采用选择第二绝缘层310上湿法刻蚀第一绝缘层308,然后将导体层填入结构中。在一些实施例中,填充导体层可以采用CVD、ALD和其他合适的方法。在一些实施例中,导体层由导电材料制成,包括但不限于钨、钴、铜、铝和/或金属硅化物。

[0083] 在一些实施例中,等级层堆栈314中的导体层用作多个NAND串的选择门或字线。在一些实施例中,等级层堆栈314中的导体层316用作NAND串的字线。在一些实施例中,等级层堆栈314中的形成在NAND串的一端的导体层328用作NAND串的源极选择门。在一些实施例中,等级层堆栈314中的形成在NAND串的另一端的导体层330用作NAND串的漏极选择门。

[0084] 在一些实施例中,对等级层堆栈306顶部的一个或多个绝缘层对进行图形化后,再将图形化的绝缘层对中的第一绝缘层替换为导体层,形成漏极选择门。在一些实施例中,在等级层堆栈306顶部形成一层导电层,对该导电层进行图形化,形成漏极选择门。在一些实施例中,导电层材料为钨、钴、铜、铝、掺杂硅和金属硅化物中的一种或多种的组合,也可以为其他合适的材料。在一些实施例中,导电层的厚度为5-40nm。在一些实施例中,形成导电层的工艺可以使用薄膜沉淀工艺,包括但不限于化学气相沉积法(CVD)、物理气相沉积法(PVD)、或原子层沉积法(ALD)。在一些实施例中,可以采用光刻和干法/湿法刻蚀工艺对导电层进行图形化。

[0085] 在一些实施例中,形成NAND串进一步包括形成半导体通道320,其在竖直方向延伸

并穿过所述等级层堆栈314。在一些实施例中,形成NAND串进一步包括介质层322,其位于半导体通道320和多个导体/绝缘层对之间。在一些实施例中,介质层322是多个层的组合,包括但不限于隧道层、存储单元层、和阻隔层。在一些实施例中,所述隧道层包括绝缘材料,包括但不限于氧化硅、氮化硅、氮氧化硅或上述材料的组合。在一些实施例中,隧道层的厚度为5-15nm,半导体通道中的电子或空穴可以通过这层隧道层隧穿至NAND串的存储单元层中。在一些实施例中,存储单元层可以用于存储操作NAND的电荷。存储单元层的材料包括但不限于氮化硅、氮氧化硅、或氧化硅和氮化硅的组合、或上述材料的组合。在一些实施例中,存储单元层的厚度为3-15nm。在一些实施例中,阻隔层材料为氧化硅、氮化硅或高介电常数绝缘材料,或者多种以上材料的组合。例如一个氧化硅层或一个包含氧化硅/氮化硅/氧化硅(ONO)三层的厚度为4-15nm的复合层。在一些实施例中,所述阻隔层可以进一步包括一个高K介电层(例如厚度为1-5nm的氧化铝)。在一些实施例中,形成介质层322可以采用ALD、CVD、PVD和其他合适的方法。

[0086] 在一些实施例中,形成NAND串进一步包括形成在所述NAND串一端的外延层。如图3C所示,外延层326形成在NAND串318和第二硅基板302之间。在一些实施例中,外延层326是硅层,其与第二硅基板302直接接触并且从第二硅基板302上外延生长。在一些实施例中,外延层326进一步被掺杂到期望的掺杂水平。

[0087] 在一些实施例中,操作606进一步包括形成一个或多个共源触点。如图3C所示,垂直延伸并贯穿等级层堆栈314的共源触点324形成在第二硅基板302上。在一些实施例中,共源触点324的一端直接接触第二硅基板302。在一些实施例中,共源触点324通过第二硅基板302连接多个NAND串318。在一些实施例中,通过源极选择门328控制外延层326的开关状态。在一些实施例中,共源触点324由导电材料制成,包括但不限于钨、钴、铜、铝、掺杂硅、硅化物或以上材料的组合。在一些实施例中,形成共源触点324可以通过使用干法/湿法刻蚀工艺来形成垂直贯穿等级层堆栈314的开口,然后将导体材料或者其他材料例如绝缘材料填充所述开口。所述填充材料可以采用ALD、CVD、PVD和其他合适的方法。

[0088] 示例方法600继续于操作608,如图6所示,在多个NAND串上形成阵列互联层。如图3D所示,阵列互联层338形成在多个NAND串318上。阵列互联层用于传输NAND串和其他电路之间的电信号。在一些实施例中,形成阵列互联层338包括形成绝缘层334,然后形成多个位线触点335,其在绝缘层334中并与NAND串318接触。在一些实施例中,绝缘层334是一层或多层绝缘材料,例如氧化硅、氮化硅、氮氧化硅或者其组合。在一些实施例中,位线触点335的形成过程为:首先在绝缘层334中形成开口,然后使用导体材料或绝缘材料填充所述开口。在一些实施例中,制造位线触点335的导体材料包括但不限于钨、钴、铜、铝、掺杂硅、硅化物或以上材料的组合。在一些实施例中,使用导体材料或者其他材料填充所述开口可以采用ALD、CVD、PVD和/或其他合适的方法。

[0089] 在一些实施例中,形成阵列互联层338进一步包括形成其他导电层,例如形成在绝缘层334中的导体层340和导体接触层344。在一些实施例中,具有一个或多个导体层340和/或导体接触层344。在一些实施例中,制造导体层340和导体接触层344的导体材料包括但不限于钨、钴、铜、铝、掺杂硅、硅化物或以上材料的组合。形成导体层和导体接触层的工艺可以采用公知的后段制程方法。

[0090] 在一些实施例中,形成阵列互联层338进一步包括形成顶部导电层342和顶部绝缘

层336。在一些实施例中,制造顶部导电层342的导体材料包括但不限于钨、钴、铜、铝、掺杂硅、硅化物或以上材料的组合。在一些实施例中,制造顶部绝缘层336的绝缘材料包括但不限于氧化硅、氮化硅、氮氧化硅、或上述材料的组合。

[0091] 图4A-4D是根据本发明实施方式的结合上述阵列器件和外围器件的步骤示意图;图7是结合上述阵列器件和外围器件的示例方法700的流程图。

[0092] 示例性方法700开始于操作702,如图7所示,将第二硅基板上的阵列器件上下倒置从而使得阵列互联层位于第二硅基板下方,并将阵列互联层和外围互联层对齐。如图4A所示,阵列互联层338被置于第二硅基板302下方。在一些实施例中,对齐阵列互联层338和外围互联层222的方法为对齐阵列互联层338的导体层342和外围互联层222的导体层220。如此,当阵列器件和外围器件结合时导体层342与220接触。

[0093] 示例性方法700继续于操作704,如图7所示,结合阵列互联层和外围互联层。如图4A所示,阵列互联层338和外围互联层222结合并形成粘结界面403。在一些实施例中,在两个互联层结合之前或结合时,处理工艺可用于加强阵列互联层338和外围互联层222之间的结合力。在一些实施例中,绝缘层336为氧化硅层,绝缘层218为氮化硅层。在一些实施例中,绝缘层336为氮化硅层,绝缘层218为氧化硅层。在一些实施例中,结合处理包括等离子体处理工艺和/或湿法化学处理工艺,处理阵列互联层的表面和外围互联层的表面以在两个绝缘层336和218之间形成化学结合。在一些实施例中,结合处理为热处理工艺,在一些实施例中,热处理的操作温度是250℃到600℃。在一些实施例中,热处理工艺使得导体层342和220之间产生互扩散。由此,导体层342和220在结合处理后相互混合。在一些实施例中,导体层342和220都由铜制成。

[0094] 示例性方法700继续于操作706,如图7所示,在等级层堆栈上形成源端导电层。

[0095] 在本发明的一个实施例中,操作706具体为:去除等级层堆栈上的第二硅基板后,在等级层堆栈上形成源端导电层,并在源端导电层中形成隔离区。

[0096] 在一些实施例中,去除第二硅基板302,并在等级层堆栈314上形成源端导电层405,如图4B1所示。在一些实施例中,源端导电层405由高电导率材料构成,其导电性能不受源极选择门控制,并使得共源触点324与NAND串318能够形成良好的电性连接。在一些实施例中,源端导电层405由金属、金属合金和金属硅化物中的一种或多种的组合构成,也可以由其他高电导率材料构成。在一些实施例中,构成源端导电层405的金属由铜、钴、镍、钛和钨中的一种或多种的组合构成,也可以为其他合适的金属材料。在一些实施例中,构成源端导电层405的金属合金为铜、钴、镍、钛和钨中的至少两种金属构成的合金中的一种或多种的组合(例如,所述金属合金可以为钛镍合金,也可以为钛镍合金和钛钨合金的组合),也可以为其他合适的金属合金材料。在一些实施例中,构成源端导电层405的金属硅化物由硅化钴、硅化镍、硅化钛和硅化钨中的一种或多种的组合构成,也可以为其他合适的金属硅化物材料。

[0097] 在一些实施例中,源端导电层405的厚度介于20nm到50μm之间。在一些实施例中,源端导电层405的厚度介于200nm到5000nm之间。在一些实施例中,形成源端导电层的工艺可以使用薄膜沉淀工艺,包括但不限于化学气相沉积法(CVD)、物理气相沉积法(PVD)、或原子层沉积法(ALD)。

[0098] 在一些实施例中,一次全部去除第二硅基板302。在一些实施例中,首先减薄第二

硅基板302,然后再去除减薄后的第二硅基板。在一些实施例中,减薄第二硅基板302,直至第二硅基板302中的隔离区304露出。在一些实施例中,去除第二硅基板302的工艺包括但不限于晶圆研磨、干法刻蚀、湿法刻蚀或化学机械抛光或上述工艺的组合。

[0099] 在一些实施例中,图形化源端导电层,在源端导电层中形成隔离区。如图4C1所示,一个或多个隔离区407形成在源端导电层405上。在一些实施例中,采用光刻和干法/湿法刻蚀工艺去除选定区域中的源端导电层材料,形成隔离区图案,并向隔离区图案中填充绝缘材料形成隔离区407。在一些实施例中,形成隔离区407的工艺可以采用热生长和/或薄膜淀积工艺。在一些实施例中,隔离区407的材料为氧化硅、氮化硅、氮氧化硅和掺杂氧化硅中的一种或多种的组合,也可以为其他合适的材料。在一些实施例中,根据实际设计需要,在源端导电层405中形成不同的隔离区图案,以得到合适的源端导电层结构,驱动单个存储块、多个存储块、或存储块的部分。在一些实施例中,根据实际设计需要,在源端导电层405中形成不同的隔离区图案,以得到合适的源端导电层结构,使源端导电层在连接共源触点与NAND串之外,实现其他的电性连接功能。

[0100] 在本发明的另一个实施例中,操作706具体为:在第二硅基板上形成金属层,使第二硅基板中的硅与金属层中的金属合金化形成金属硅化物,得到源端导电层。

[0101] 如图4B2所示,在一些实施例中,减薄第二硅基板302,直至第二硅基板302中的隔离区304露出,得到减薄后的硅基板417。在一些实施例中,减薄第二硅基板302的工艺包括但不限于晶圆研磨、干法刻蚀、湿法刻蚀或化学机械抛光或上述工艺的组合。在一些实施例中,在减薄后的硅基板417上形成金属层419。在一些实施例中,金属层材料是钴、镍、钛和钨中的一种或几种的组合,或者是其它合适的金属材料。所述金属层应该具有足够的厚度,以满足后续反应需要。可以使用薄膜沉淀工艺形成金属层419,包括但不限于化学气相沉积法(CVD)、物理气相沉积法(PVD)、或原子层沉积法(ALD)和/或其他合适的方法。

[0102] 在一些实施例中,可以使用退火或其它合适的工艺使减薄后的硅基板417中的硅与金属层419中的金属合金化形成金属硅化物,得到源端导电层421,源端导电层421中具有隔离区304,最后去除源端导电层421上残留的金属层,如图4C2所示。具体地,使金属层419中的金属进入减薄后的硅基板417中形成金属硅化物。源端导电层421中的金属硅化物根据金属层419所含金属的不同而有所不同,如果金属层419采用钴、镍、钛或钨,则源端导电层421中的金属硅化物相应地为硅化钴、硅化镍、硅化钛或硅化钨。在一些实施例中,源端导电层421的金属硅化物具有高电导率,其导电性能不受源极选择门控制,并使得共源触点324与NAND串318能够形成良好的电性连接。

[0103] 在一些实施例中,在第二硅基板302上形成的隔离区304不能满足对源端导电层421的设计需要,因此,上述操作706进一步包括:图形化源端导电层421,在源端导电层421中形成新的隔离区(图中未示出)。在一些实施例中,在第二硅基板302上形成的隔离区304能满足对源端导电层421的设计需要,因此,不需要对形成的源端导电层421再进行图形化操作。此外,对于上述操作706,第二硅基板302上的隔离区304不是必须的,即,在一些实施例中,形成的第二硅基板302上不存在隔离区304,因此,上述操作706进一步包括:图形化源端导电层421,在源端导电层421中形成隔离区(图中未示出)。

[0104] 在一些实施例中,采用光刻和干法/湿法刻蚀工艺去除选定区域中的源端导电层材料,形成隔离区图案,并向隔离区图案中填充绝缘材料形成隔离区。在一些实施例中,形

成隔离区的工艺可以采用热生长和/或薄膜淀积工艺。在一些实施例中,形成的隔离区的材料为氧化硅、氮化硅、氮氧化硅和掺杂氧化硅中的一种或多种的组合,也可以为其他合适的材料。在一些实施例中,根据实际设计需要,在源端导电层421中形成不同的隔离区图案,以得到合适的源端导电层结构,驱动单个存储块、多个存储块、或存储块的部分。在一些实施例中,根据实际设计需要,在源端导电层421中形成不同的隔离区图案,以得到合适的源端导电层结构,使源端导电层在连接共源触点与NAND串之外,实现其他的电性连接功能。

[0105] 示例性方法700继续于操作708,如图7所示,在源端导电层上形成后段制程互联层和衬垫层。如图4D所示,在源端导电层405/421上形成后段制程互联层和衬垫层415。在一些实施例中,后段制程互联层包括一个或多个绝缘层409、一个或多个触点411和一个或多个导体层413。在一些实施例中,绝缘层409是多个绝缘层的组合,所述多个绝缘层可以通过独立的步骤制作。在一些实施例中,触点411、导体层413和衬垫层415可由导电材料制成,包括但不限于钨、钴、铜、铝、掺杂硅、硅化物或以上材料的组合。在一些实施例中,制造绝缘层409的绝缘材料包括但不限于氧化硅、氮化硅、氮氧化硅、或上述材料的组合。在一些实施例中,绝缘层409可进一步包括高K绝缘材料。在一些实施例中,衬垫层415与外部电路连接以在结合的阵列/外围器件和外部电路之间传递电信号。在一些实施例中,后端制程互联层(例如触点411)与源端导电层直接或间接电性连接。

[0106] 应当指出,上述形成NAND存储器的方法,以及形成NAND存储器的方法中包含的形成外围器件和外围互联层的方法、形成阵列器件和阵列互联层的方法、以及结合阵列器件和外围器件的方法均为示例性的,并不应当用来形成对本发明的限制,可以根据实际需要调整上述方法中的步骤内容和/或顺序,以获得相同或相似的技术效果。例如,形成外围器件和外围互联层的步骤与形成阵列器件和阵列互联层的步骤是相互独立的,二者没有先后顺序,也就是说,也可以先形成阵列器件和阵列互联层,再形成外围器件和外围互联层。此外,在等级层堆栈上形成源端导电层的步骤不一定要在结合阵列器件和外围器件时完成,也可以在形成阵列器件和阵列互联层时完成。在一些实施方式中,在第二硅基板上形成多个阵列器件的NAND串后,在原来第二硅基板的位置形成源端导电层,然后再在多个NAND串上形成阵列互联层。在一些实施方式中,在第二硅基板上形成多个阵列器件的NAND串,以及在多个NAND串上形成阵列互联层后,再在原来第二硅基板的位置形成源端导电层,然后再结合阵列器件和外围器件。此外,也可以在其他合适的时候形成源端导电层,以实现共源触点和NAND串的电性连接。与此相对应地,上述形成源端导电层的方法也应为示例性的,也可以采用其他合适的方法形成源端导电层。

[0107] 本发明用高电导率的源端导电层代替硅基板上的源端通道,实现共源触点与NAND串的连接,源极选择门只需要控制硅外延层的通断,使得对硅外延层的控制不再受到对源端通道的控制的干扰,并能进一步提高器件的操作速度以及外围器件对存储块的源端的驱动能力。

[0108] 以上所述,仅为本发明较佳的具体实施方式,但本发明的保护范围并不局限于此,任何熟悉本技术领域的技术人员在本发明揭露的技术范围内,可轻易想到的变化或替换,都应涵盖在本发明的保护范围之内。因此,本发明的保护范围应以所述权利要求的保护范围为准。

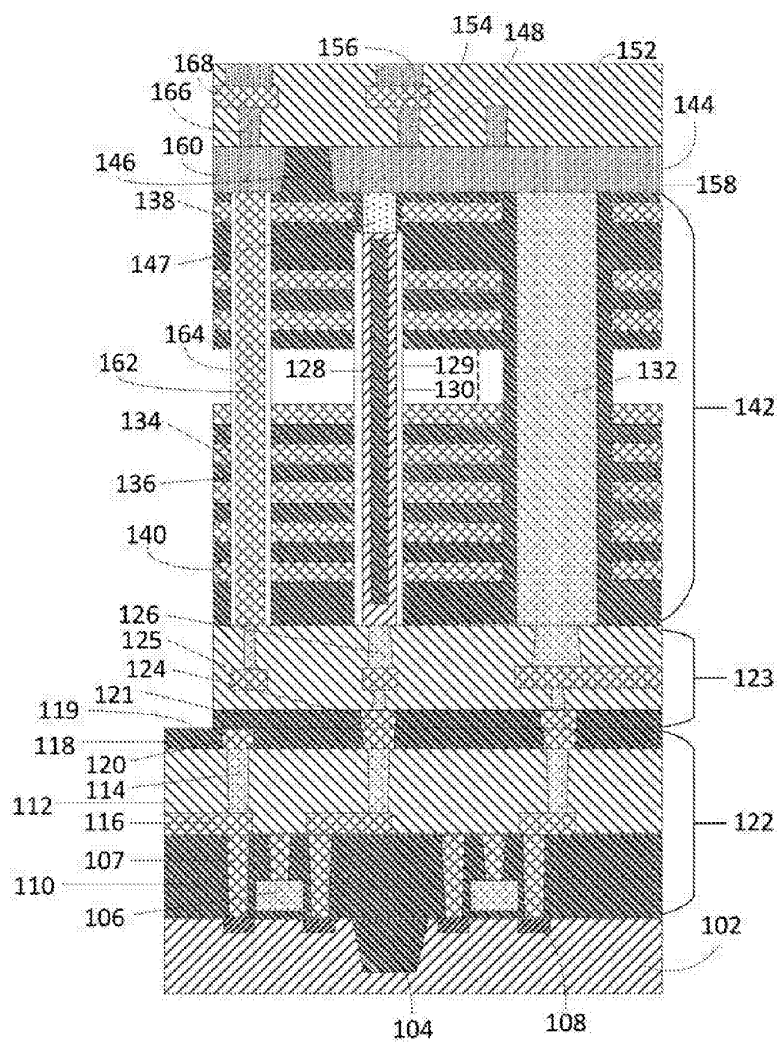


图1

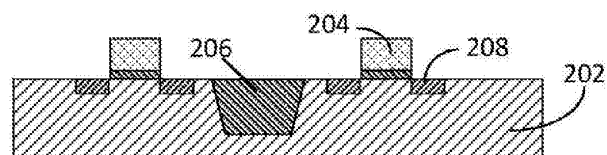


图2A

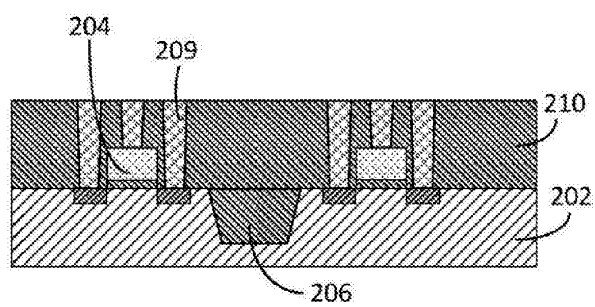


图2B

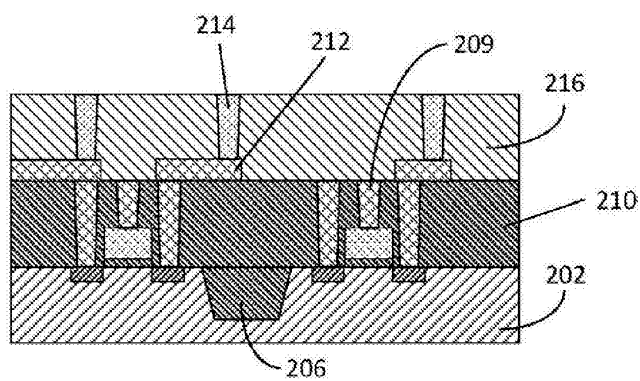


图2C

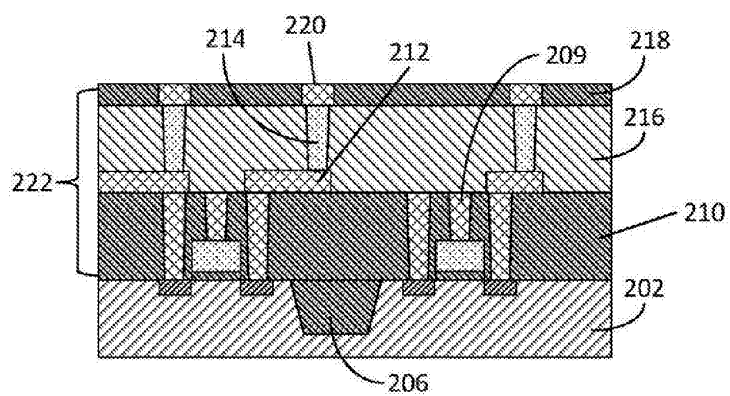


图2D

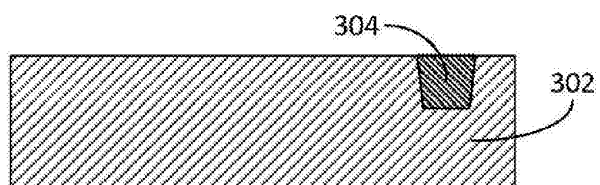


图3A

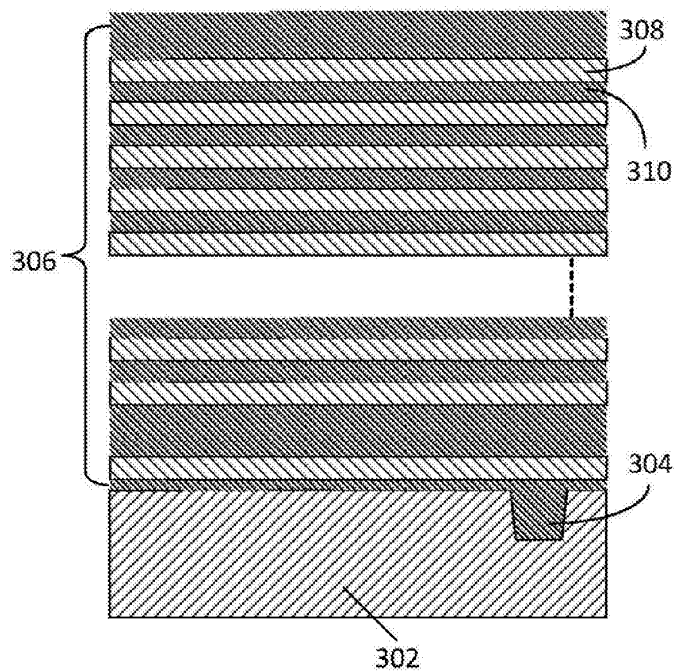


图3B

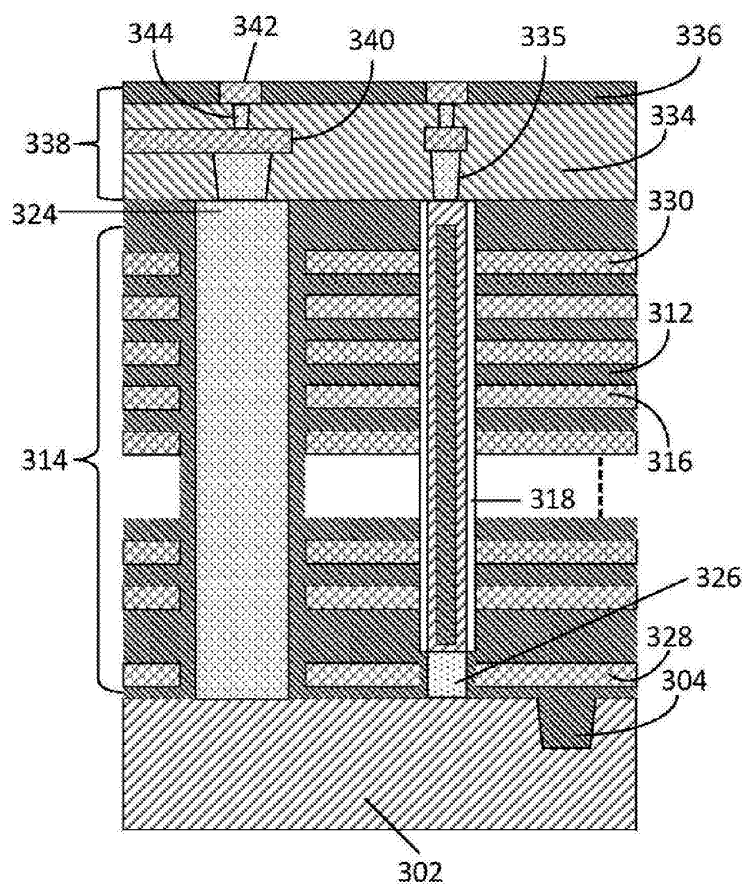


图3D

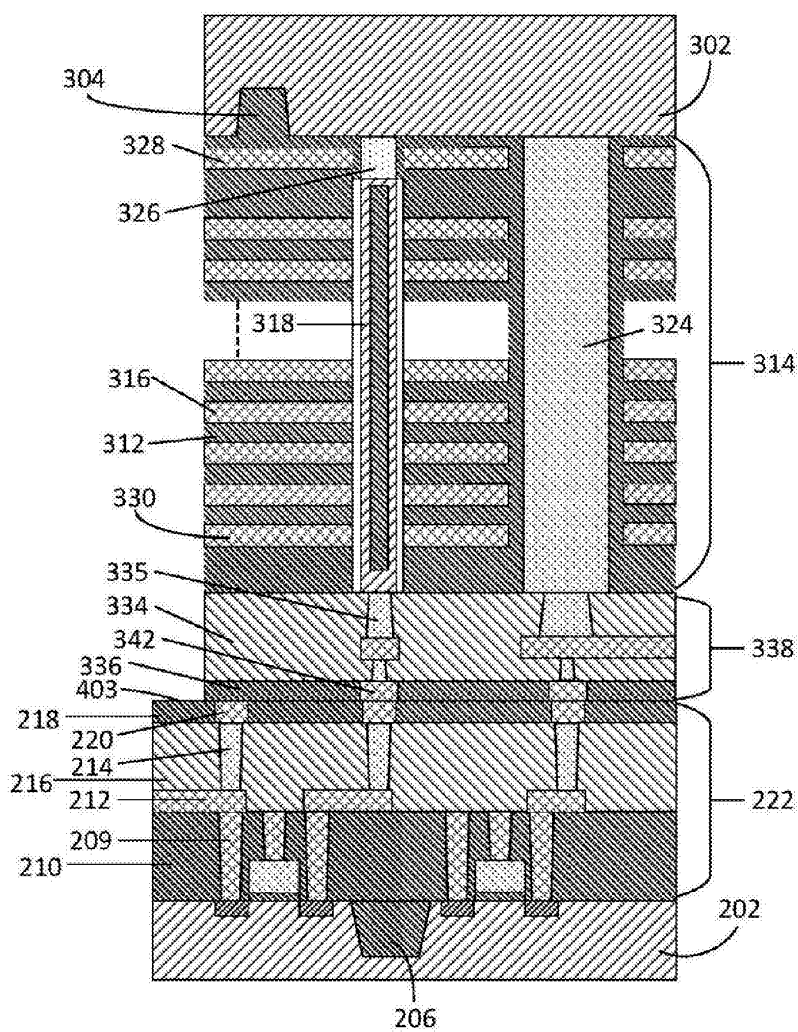


图4A

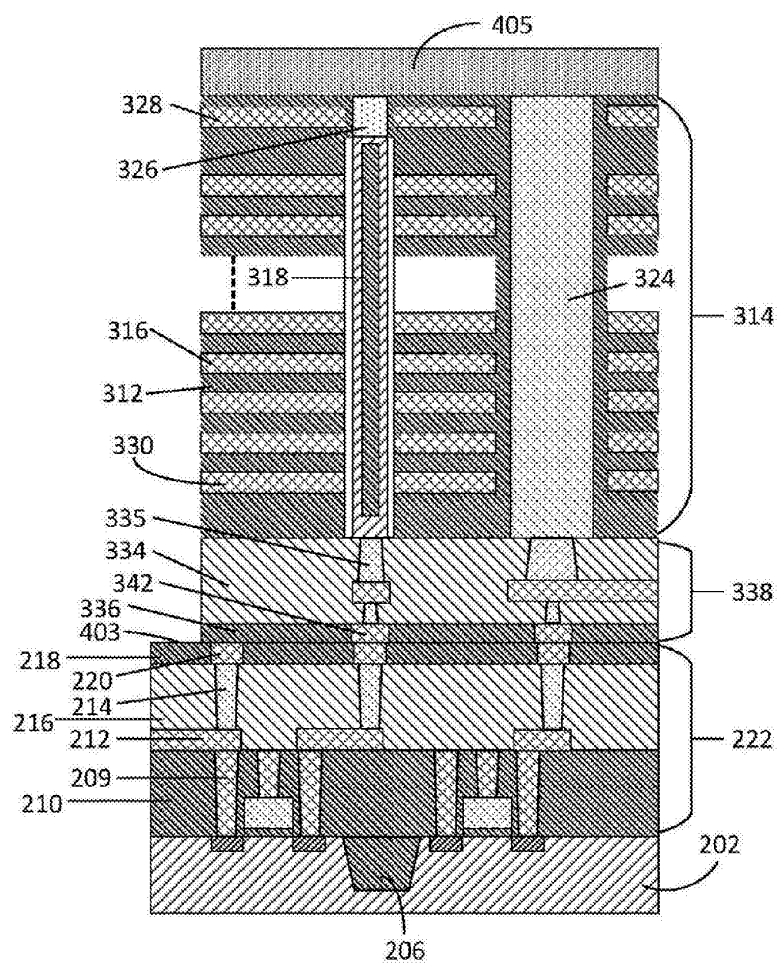


图4B1

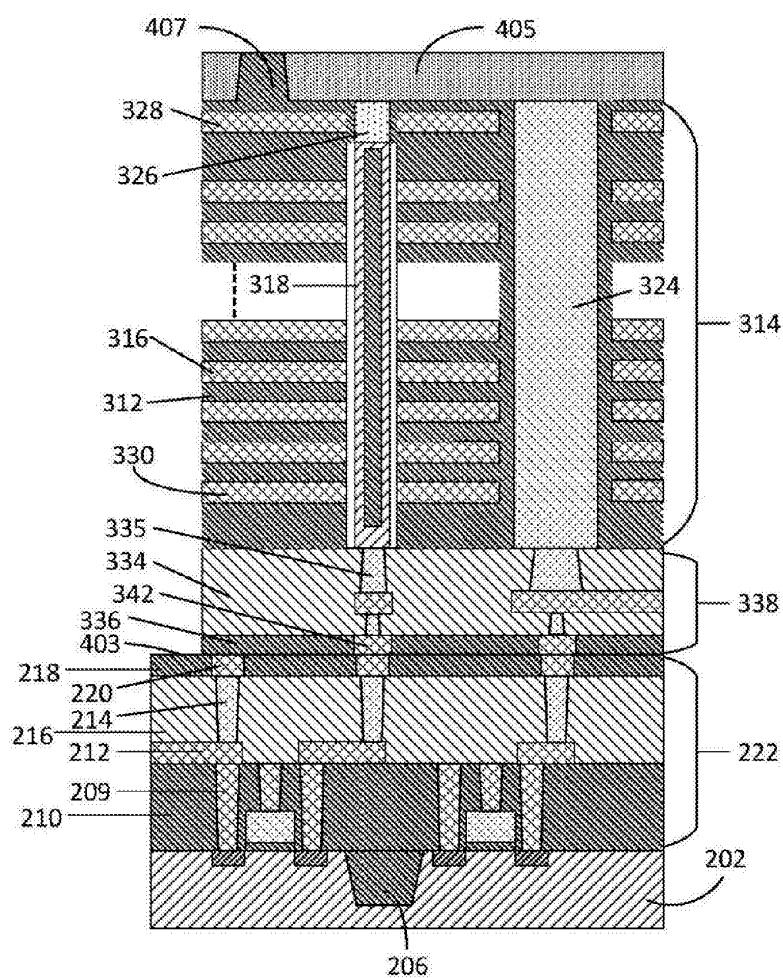


图4C1

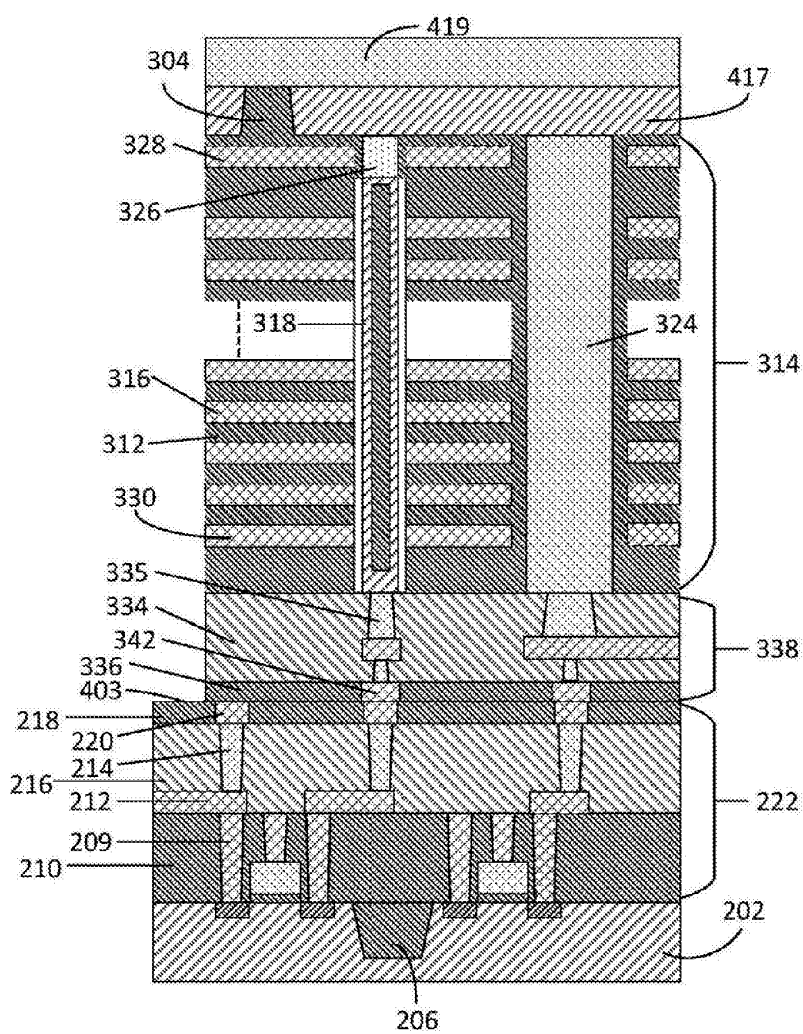


图4B2

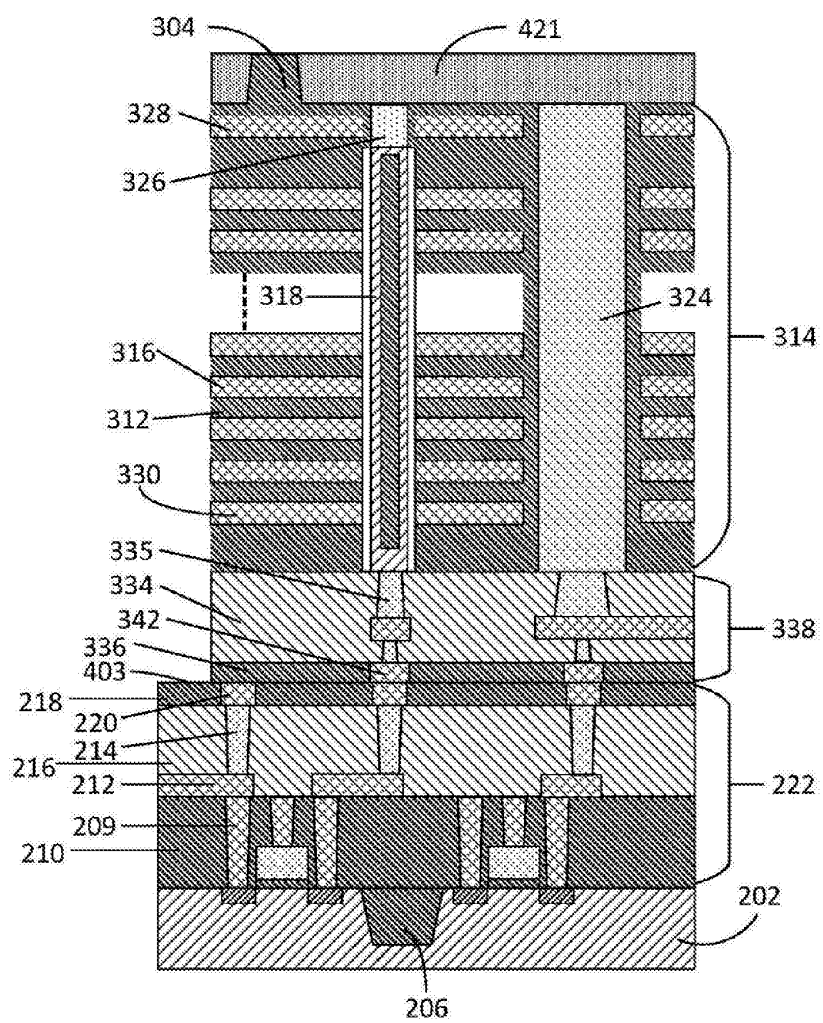


图4C2

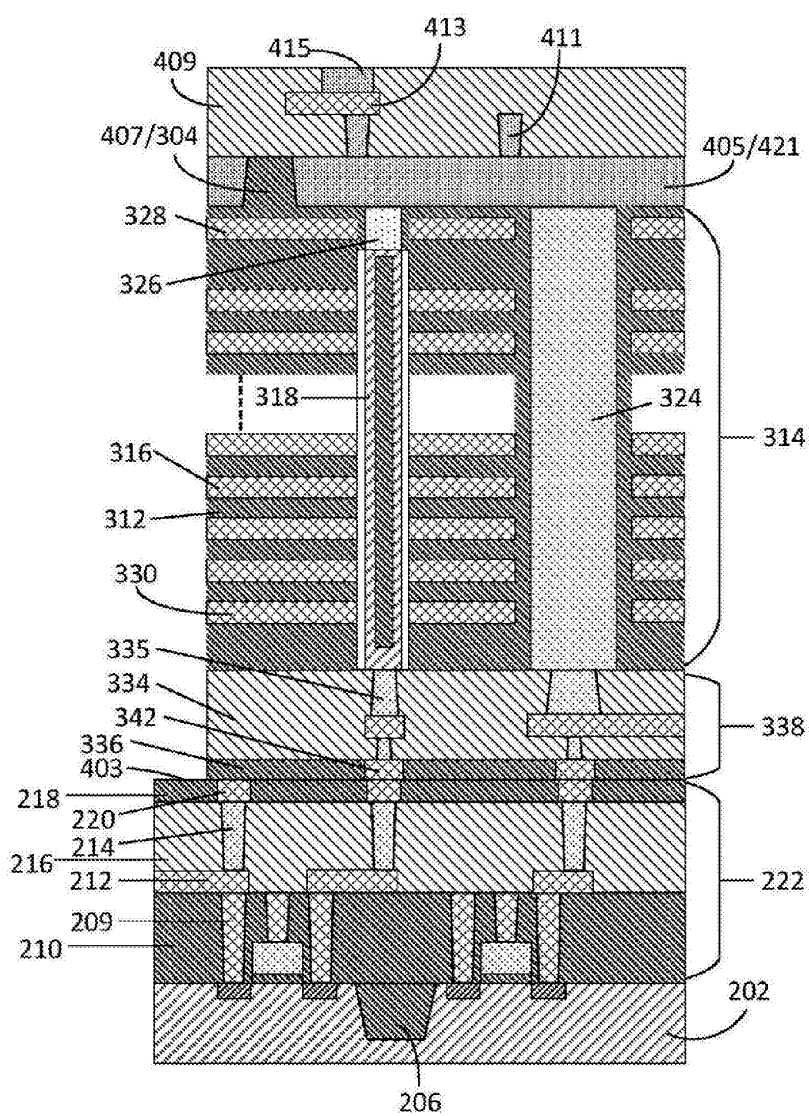


图4D

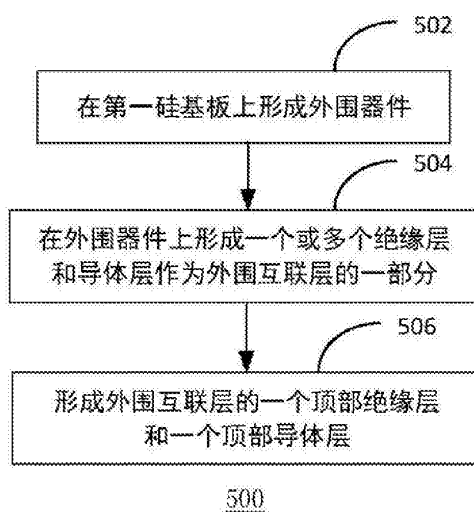


图5

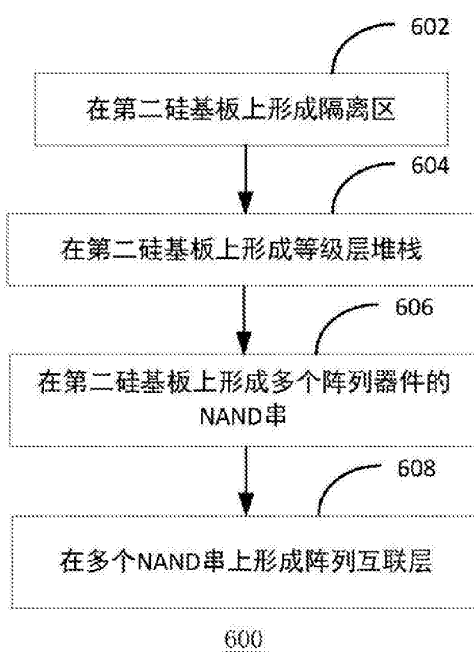


图6

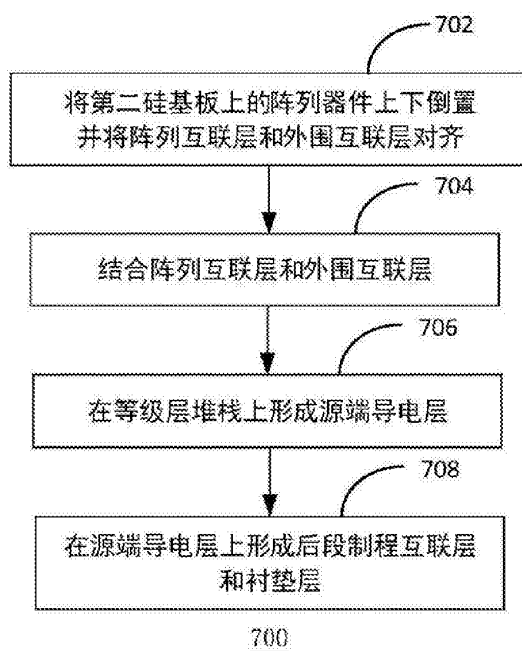


图7

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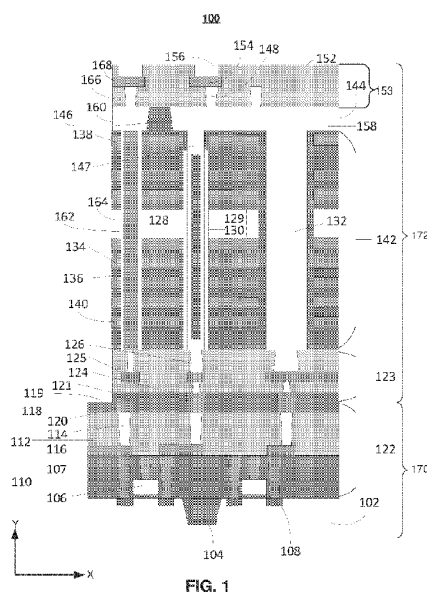
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(54) **Title:** SOURCE STRUCTURE OF THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME



(57) **Abstract:** Source structure of a three-dimensional (3D) memory device and method for forming the source structure of the 3D memory device are disclosed. In an example, a NAND memory device includes a substrate (102), an alternating conductor/dielectric stack (142), a NAND string (130), a source conductor layer (144), and a source contact (132). The alternating conductor/dielectric stack (142) includes a plurality of conductor/dielectric pairs above the substrate (102). The NAND string (130) extends vertically through the alternating conductor/dielectric stack (142). The source conductor layer (144) is above the alternating conductor/dielectric stack (142) and is in contact with an end of the NAND string (130). The source contact (132) includes an end in contact with the source conductor layer (144). The NAND string (130) is electrically connected to the source contact (132) by the source conductor layer (144). The source conductor layer (144) includes one or more conduction regions each including one or more of a metal, a metal alloy, and a metal silicide.

[Continued on next page]

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SOURCE STRUCTURE OF THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to Chinese Patent Application No. 201711236924.1 filed on November 30, 2017, which is incorporated herein by reference in its entirety.

BACKGROUND

[0002] Embodiments of the present disclosure relate to three-dimensional (3D) memory devices and fabrication methods thereof.

[0003] Planar memory cells are scaled to smaller sizes by improving process technology, circuit design, programming algorithm, and fabrication process. However, as feature sizes of the memory cells approach a lower limit, planar process and fabrication techniques become challenging and costly. As a result, memory density for planar memory cells approaches an upper limit.

[0004] A 3D memory architecture can address the density limitation in planar memory cells. The 3D memory architecture includes a memory array and peripheral devices for controlling signals to and from the memory array.

BRIEF SUMMARY

[0005] Embodiments of 3D memory architectures and fabrication methods thereof are disclosed herein.

[0006] According to some embodiments of the present disclosure, a NAND memory device includes a substrate, an alternating conductor/dielectric stack, a NAND string, a source conductor layer, and a source contact. The alternating conductor/dielectric stack includes a plurality of conductor/dielectric pairs above the substrate. The NAND string extends vertically through the alternating conductor/dielectric stack. The source conductor layer is above the alternating conductor/dielectric stack and is in contact with a first end of the NAND string. The source contact includes a first end in contact with the

source conductor layer. The NAND string is electrically connected to the source contact by the source conductor layer.

[0007] In some embodiments, the source conductor layer includes one or more conduction regions each including a metal, a metal alloy, and/or a metal silicide. The metal can include copper, cobalt, nickel, titanium, and/or tungsten. The metal alloy can include an alloy of at least two of copper, cobalt, nickel, titanium, and tungsten. The metal silicide can include copper silicide, cobalt silicide, nickel silicide, titanium silicide, and/or tungsten silicide.

[0008] In some embodiments, the NAND memory device includes an epitaxial silicon layer between the NAND string and the source conductor layer. The NAND string can be electrically connected to the source conductor layer by the epitaxial silicon layer. The source conductor layer can include a plurality of conduction regions and one or more isolation regions electrically isolating the plurality of conduction regions. The NAND string can be electrically connected to the source contact by a first conduction region of the plurality of conduction regions.

[0009] In some embodiments, the NAND memory device includes a through array contact (TAC) extending vertically through the alternating conductor/dielectric stack. The TAC can be in contact with a second conduction region of the plurality of conduction regions.

[0010] In some embodiments, the NAND memory device includes a first interconnect layer (e.g., a back-end-of-line (BEOL) interconnect layer). The first interconnect layer can include a first contact and a second contact. The NAND string can be electrically connected to the first contact by the first conduction region. The TAC can be electrically connected to the second contact by the second conduction region.

[0011] In some embodiments, the NAND memory device includes a peripheral device between the substrate and the NAND string. The NAND memory device can also include a second interconnect layer (e.g., a peripheral interconnect layer) above and in contact with the peripheral device. The second interconnect layer can include one or more conductor layers in one or more dielectric layers. The NAND memory device can further include a third interconnect layer (e.g., an array interconnect layer) in contact with a second end of the NAND string and a second end of the source contact. The third

interconnect layer can include one or more conductor layers in one or more dielectric layers.

[0012] In some embodiments, the NAND memory device includes a bonding interface between the second interconnect layer and the third interconnect layer. The peripheral device can be electrically connected to the NAND string by the second interconnect layer and the third interconnect layer.

[0013] According to some embodiments of the present disclosure, a method for forming a NAND memory device is disclosed. An alternating conductor/dielectric stack is formed on a first substrate. A NAND string and a source contact both extending vertically through the alternating conductor/dielectric stack are formed. The first substrate is replaced with a source conductor layer, so that the source conductor layer is in contact with a first end of the NAND string and a first end of the source contact, and the NAND string is electrically connected to the source contact by the source conductor layer. In some embodiments, the source conductor layer includes one or more conduction regions each including a metal, a metal alloy, and/or a metal silicide.

[0014] In some embodiments, to replace the first substrate with the source conductor layer, the first substrate is removed, and the source conductor layer is formed at the original location of the first substrate. To remove the first substrate, the first substrate can be thinned, and the thinned first substrate can be removed.

[0015] In some embodiments, to replace the first substrate with the source conductor layer, a metal layer is formed on the first substrate, and a metal silicide layer is formed based on a reaction between silicon in the first substrate and a metal in the metal layer. To form the metal layer, the first substrate can be thinned, and the metal layer can be formed on the thinned first substrate. To form the metal layer, an isolation region can be formed at a first surface of the first substrate that is in contact with the alternating conductor/dielectric stack, and the first substrate can be thinned from a second surface of the first substrate to expose the isolation region. In some embodiments, one or more isolation regions are formed in the source conductor layer after the first substrate has been replaced with the source conductor layer.

[0016] In some embodiments, a peripheral device can be formed on a second substrate. The NAND string and the peripheral device can be joined, so that the NAND string is between the first substrate and the peripheral device. To join the NAND string and the

peripheral device, a first interconnect layer in contact with a second end of the NAND string and a second end of the source contact can be formed, a second interconnect layer in contact with the peripheral device can be formed, and a bonding interface can be formed between the first interconnect layer and the second interconnect layer, so that the peripheral device can be electrically connected to the NAND string by the first interconnect layer and the second interconnect layer. The first interconnect layer can include one or more conductor layers in one or more dielectric layers. The second interconnect layer can include one or more conductor layers in one or more dielectric layers.

[0017] In some embodiments, to form the bonding interface between the first interconnect layer and the second interconnect layer, chemical bonds are formed between one of the dielectric layers in the first interconnect layer and one of the dielectric layers in the second interconnect layer, and/or physical inter-diffusion is caused between one of the conductor layers in the first interconnect layer and one of the conductor layers in the second interconnect layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.

[0019] FIG. 1 illustrates a cross-section of a 3D memory device, according to some embodiments.

[0020] FIGs. 2A–2D illustrate an exemplary fabrication process for forming a peripheral device and a peripheral interconnect layer, according to some embodiments.

[0021] FIGs. 3A–3D illustrate an exemplary fabrication process for forming an array device and an array interconnect layer, according to some embodiments.

[0022] FIG. 4 illustrates an exemplary fabrication process for joining an array device and a peripheral device, according to some embodiments.

[0023] FIGs. 5A–5B illustrate an exemplary fabrication process for forming a source conductor layer, according to some embodiments.

- [0024] FIGs. 6A–6B illustrate another exemplary fabrication process for forming a source conductor layer, according to some embodiments.
- [0025] FIG. 7 illustrates an exemplary fabrication process for forming a BEOL interconnect layer on a source conductor layer, according to some embodiments.
- [0026] FIG. 8 is a flowchart of an exemplary method for forming a peripheral device and a peripheral interconnect layer, according to some embodiments.
- [0027] FIG. 9 is a flowchart of an exemplary method for forming an array device and an array interconnect layer, according to some embodiments.
- [0028] FIG. 10 is a flowchart of an exemplary method for forming a 3D memory device with an array device and a peripheral device, according to some embodiments.
- [0029] FIG. 11 is a flowchart of an exemplary method for forming a source conductor layer, according to some embodiments.
- [0030] FIG. 12 is a flowchart of another exemplary method for forming a source conductor layer, according to some embodiments.
- [0031] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

- [0032] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.
- [0033] It is noted that references in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” “some embodiments,” etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent

art to effect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0034] In general, terminology may be understood at least in part from usage in context. For example, the term “one or more” as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as “a,” “an,” or “the,” again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term “based on” may be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0035] It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something but also includes the meaning of “on” something with an intermediate feature or a layer therebetween, and that “above” or “over” not only means the meaning of “above” or “over” something but can also include the meaning it is “above” or “over” something with no intermediate feature or layer therebetween (i.e., directly on something).

[0036] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0037] As used herein, the term “substrate” refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0038] As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which contacts, interconnect lines, and/or vias are formed) and one or more dielectric layers.

[0039] As used herein, the term “nominal/nominally” refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term “about” indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term “about” can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., $\pm 10\%$, $\pm 20\%$, or $\pm 30\%$ of the value).

[0040] As used herein, the term “3D memory device” refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as “memory strings,” such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term “vertical/vertically” means nominally perpendicular to the lateral surface of a substrate.

[0041] In some 3D memory devices, a source selective gate controls the on/off state of a doped silicon channel formed in the substrate of the 3D memory device. The operation speed of the source selective gate depends on the conductance of the silicon channel, which can be limited as silicon is a semiconductor material. Further, as the entire block of

memory cells can share a single source selective gate, the load to drive the array common source of the memory block can be challenging for the peripheral device.

[0042] Various embodiments in accordance with the present disclosure provide a 3D memory device with a source conductor layer in place of the silicon channel in the substrate used by other 3D memory devices. By replacing silicon with conductive materials (e.g., metal, metal alloy, and/or metal silicide) that form the source conductor layer disclosed herein, the resistance of the source side (e.g., between the common source contact and the NAND strings) of the 3D memory device can be reduced, thereby increasing the device operation speed. In some embodiments, the conduction mechanism for erase operation of the source selective gate can become driven by gate-induced drain leakage (GIDL).

[0043] Moreover, compared with silicon substrate, the source conductor layer disclosed herein can be more easily patterned into any suitable layout (e.g., with different isolation regions) for driving a single memory block, multiple memory blocks, or a portion of a memory block as desired, which can enhance the driving capability of the peripheral device for the memory array. Due to its conductive nature, the source conductor layer disclosed herein can be patterned and used as an interconnect layer (e.g., part of the BEOL interconnect).

[0044] FIG. 1 illustrates a cross-section of an exemplary 3D memory device 100 according to some embodiments of the present disclosure. 3D memory device 100 can include a substrate 102, which can include silicon (e.g., single crystalline silicon), silicon germanium (SiGe), gallium arsenide (GaAs), germanium (Ge), silicon on insulator (SOI) or any other suitable materials.

[0045] 3D memory device 100 can include a peripheral device on substrate 102. The peripheral device can be formed “on” substrate 102, in which the entirety or part of the peripheral device is formed in substrate 102 (e.g., below the top surface of substrate 102) and/or directly on substrate 102. The peripheral device can include a plurality of transistors 106 formed on substrate 102. An isolation region 104 and a doped region 108 (e.g., a source region or a drain region of transistor 106) can be formed in substrate 102 as well.

[0046] In some embodiments, the peripheral device can include any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of 3D

memory device 100. For example, the peripheral device can include one or more of a page buffer, a decoder (e.g., a row decoder and a column decoder), a sense amplifier, a driver, a charge pump, a current or voltage reference, or any active or passive components of the circuits (e.g., transistors, diodes, resistors, or capacitors). In some embodiments, the peripheral device is formed on substrate 102 using complementary metal-oxide-semiconductor (CMOS) technology (also known as a “CMOS chip”).

[0047] 3D memory device 100 can include a peripheral interconnect layer 122 above transistors 106 to transfer electrical signals to and from transistors 106. Peripheral interconnect layer 122 can include one or more contacts, such as a contact 107 and a contact 114, and one or more conductor layers, such as a conductor layer 116 and a conductor layer 120, each including one or more interconnect lines and/or vias. As used herein, the term “contact” can broadly include any suitable types of interconnects, such as middle-end-of-line (MEOL) interconnects and BEOL interconnects, including vertical interconnect accesses (e.g., vias) and lateral lines (e.g., interconnect lines). Peripheral interconnect layer 122 can further include one or more interlayer dielectric (ILD) layers, such as dielectric layers 110, 112, and 118. That is, peripheral interconnect layer 122 can include conductor layers 116 and 120 in dielectric layers 112 and 118. The contact and conductor layers in peripheral interconnect layer 122 can include conductor materials including, but not limited to, tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), silicides, or any combination thereof. The dielectric layers in peripheral interconnect layer 122 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, doped silicon oxide, or any combination thereof.

[0048] 3D memory device 100 can include a memory array device above the peripheral device. It is noted that x and y axes are added in FIG. 1 to further illustrate the spatial relationship of the components in 3D memory device 100. Substrate 102 includes two lateral surfaces (e.g., a top surface and a bottom surface) extending laterally in the x-direction (the lateral direction or width direction). As used herein, whether one component (e.g., a layer or a device) is “on,” “above,” or “below” another component (e.g., a layer or a device) of a semiconductor device (e.g., 3D memory device 100) is determined relative to the substrate of the semiconductor device (e.g., substrate 102) in the y-direction (the vertical direction or thickness direction) when the substrate is

positioned in the lowest plane of the semiconductor device in the y-direction. The same notion for describing spatial relationship is applied throughout the present disclosure.

[0049] In some embodiments, 3D memory device 100 is a NAND Flash memory device in which memory cells are provided in the form of an array of NAND strings 130 extending vertically above substrate 102. The array device can include a plurality of NAND strings 130 that extend through a plurality of conductor layer 134 and dielectric layer 136 pairs. The plurality of conductor/dielectric layer pairs are also referred to herein as an “alternating conductor/dielectric stack” 142. Conductor layers 134 and dielectric layers 136 in alternating conductor/dielectric stack 142 alternate in the vertical direction. In other words, except the ones at the top or bottom of alternating conductor/dielectric stack 142, each conductor layer 134 can be adjoined by two dielectric layers 136 on both sides, and each dielectric layer 136 can be adjoined by two conductor layers 134 on both sides. Conductor layers 134 can each have the same thickness or have different thicknesses. Similarly, dielectric layers 136 can each have the same thickness or have different thicknesses. For example, for a first plurality of conductor/dielectric pairs in alternating conductor/dielectric stack 142, the thickness of each conductor layer 134 and dielectric layer 136 can be between about 5 nm and about 40 nm (e.g., between 5 nm and 40 nm). For a second plurality of conductor/dielectric pairs in alternating conductor/dielectric stack 142, the thickness of each conductor layer 134 and dielectric layer 136 can be between about 10 nm and about 40 nm (e.g., between 10 nm and 40 nm). For a third plurality of conductor/dielectric pairs in alternating conductor/dielectric stack 142, the thickness of each conductor layer 134 can be between about 5 nm and about 40 nm (e.g., between 5 nm and 40 nm), and the thickness of each dielectric layer 136 can be between about 50 nm and about 200 nm (e.g., between 50 nm and 200 nm).

[0050] In some embodiments, alternating conductor/dielectric stack 142 includes more conductor layers or more dielectric layers with different materials and/or thicknesses than the conductor/dielectric layer pair. Conductor layers 134 can include conductor materials including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. Dielectric layers 136 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.

[0051] As shown in FIG. 1, each NAND string 130 can include a semiconductor channel 128 and a dielectric layer 129 (also known as “memory film”). In some embodiments,

semiconductor channel 128 includes silicon, such as amorphous silicon, polysilicon, or single crystalline silicon. In some embodiments, dielectric layer 129 is a composite layer including a tunneling layer, a storage layer (also known as “charge trap/storage layer”), and a blocking layer. Each NAND string 130 can have a cylinder shape (e.g., a pillar shape). Semiconductor channel 128, the tunneling layer, the storage layer, and the blocking layer are arranged along a direction from the center toward the outer surface of the pillar in this order, according to some embodiments. The tunneling layer can include silicon oxide, silicon nitride, or any combination thereof. The thickness of the tunneling layer (e.g., in the radial direction of Each NAND string 130) can be between about 5 nm and about 15 nm (e.g., between 5 nm and 15 nm). The storage layer can include silicon nitride, silicon oxynitride, silicon, or any combination thereof. The thickness of the storage layer (e.g., in the radial direction of Each NAND string 130) can be between about 3 nm and about 15 nm (e.g., between 3 nm and 15 nm). The blocking layer can include silicon oxide, silicon nitride, high dielectric constant (high-k) dielectrics, or any combination thereof. In one example, the blocking layer can include a composite layer of silicon oxide/silicon nitride/silicon oxide (ONO) with a thickness between about 4 nm and about 15 nm (e.g., between 4 nm and 15 nm). In another example, the blocking layer can include a high-k dielectric layer, such as an aluminum oxide (Al_2O_3) layer with a thickness between about 1 nm and about 5 nm (e.g., between 1 nm and 5 nm).

[0052] In some embodiments, NAND strings 130 include a plurality of control gates (each being part of a word line) for NAND strings 130. Each conductor layer 134 in alternating conductor/dielectric stack 142 can act as a control gate for each memory cell of NAND string 130. As shown in FIG. 1, NAND string 130 can include a selective gate 138 (e.g., a source selective gate) at an upper end of NAND string 130. NAND string 130 can include another selective gate 140 (e.g., a drain selective gate) at a lower end of NAND string 130. As used herein, the “upper end” of a component (e.g., NAND string 130) is the end further away from substrate 102 in the y-direction, and the “lower end” of the component (e.g., NAND string 130) is the end closer to substrate 102 in the y-direction. As shown in FIG. 1, for each NAND string 130, source selective gate 138 can be above drain selective gate 140. In some embodiments, selective gate 138 and selective gate 140 include conductor materials including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof.

[0053] In some embodiments, 3D memory device 100 includes a source conductor layer 144 above alternating conductor/dielectric stack 142. The bottom surface of source conductor layer 144 can contact an upper end of NAND string 130. Source conductor layer 144 can include one or more conduction regions (e.g., conduction regions 158 and 160) and one or more isolation regions (e.g., isolation region 146) that electrically isolate the conduction regions. Different from a semiconductor layer (e.g., a doped silicon channel), the conductance of conduction regions 158 and 160 is independent from source selective gate 138 because conduction regions 158 and 160 include conductive materials. Source conductor layer 144 thus can provide an electrical connection between one or more NAND strings 130 and a source contact 132 (e.g., acting as the common source contact of all NAND strings 130 in a memory block of 3D memory device 100) with lower resistance compared with other 3D memory devices in which a semiconductor channel is used for electrically connecting the NAND strings and the common source contact.

[0054] Conduction regions 158 and 160 can include conductive materials that have a higher electrical conductivity than a semiconductor material, such as silicon (e.g., amorphous silicon, single crystalline silicon, or polysilicon—either doped or undoped). In some embodiments, conduction regions 158 and 160 each has an electrical conductivity of at least about 1×10^4 S/m at about 20°C, such as at least 1×10^4 S/m at 20°C. In some embodiments, conduction regions 158 and 160 each has an electrical conductivity of between about 1×10^4 S/m and about 1×10^8 S/m at about 20°C, such as between 1×10^4 S/m and 1×10^8 S/m at 20°C (e.g., 1×10^4 S/m, 1×10^5 S/m, 5×10^5 S/m, 1×10^6 S/m, 2×10^6 S/m, 3×10^6 S/m, 4×10^6 S/m, 5×10^6 S/m, 6×10^6 S/m, 7×10^6 S/m, 8×10^6 S/m, 9×10^6 S/m, 1×10^7 S/m, 2×10^7 S/m, 3×10^7 S/m, 4×10^7 S/m, 5×10^7 S/m, 6×10^7 S/m, 7×10^7 S/m, 8×10^7 S/m, 9×10^7 S/m, 1×10^8 S/m, any range bounded on the lower end by any of these values, or in any range defined by any two of these values, at 20°C). The conductive materials in conduction regions 158 and 160 can include, but are not limited to, metals, metal alloys, and metal silicides. In some embodiments, conduction regions 158 and 160 each includes one or more metals, such as copper (Cu), cobalt (Co), nickel (Ni), titanium (Ti), and tungsten (W). The metals can also include any other suitable metals, such as silver (Ag), aluminum (Al), gold (Au), platinum (Pt), etc. In some embodiments, conduction regions 158 and 160 each includes one or more metal alloys, each of which is an alloy of at least

two of Cu, Co, Ni, Ti, and W (e.g., TiNi alloy or a combination of TiNi alloy and TiW alloy), or any other suitable metal alloys of, for example, Ag, Al, Au, Pt, iron (Fe), chromium (Cr), etc. In some embodiments, conduction regions 158 and 160 each includes one or more metal silicides, such as copper silicide, cobalt silicide, nickel silicide, titanium silicide, and tungsten silicide. The metal silicides can also include any other suitable metal silicides, such as silver silicide, aluminum silicide, gold silicide, platinum silicide, etc.

[0055] Source conductor layer 144 can be patterned to form any suitable layout with different numbers of conduction regions and isolation regions in different arrangements. The different layouts of conduction regions and isolation regions in source conductor layer 144 can be used to drive the memory array in various configurations, such as an array of NAND strings in a single memory block, in multiple memory blocks, or in a portion of a memory block (e.g., one or more memory fingers). To accommodate the various configurations of the memory array to be driven by source conductor layer 144, in some embodiments, source conductor layer 144 is in a trench shape or in a plate shape in a plan view, so that the conduction regions (e.g., conduction region 158) can contact an array of NAND strings 130. In some embodiments, at least one conduction region (e.g., conduction region 160) in source conductor layer 144 is not in contact with NAND string 130 (e.g., being electrically isolated from conduction region 158 by isolation region 146). Conduction region 160 can be in contact with any suitable contact in the array device to provide electrical connections between the array device and/or peripheral device to the upper level interconnects (e.g., BEOL interconnects). That is, source conductor layer 144 can be patterned to form any suitable layout to function as part of the BEOL interconnects.

[0056] In some embodiments, isolation region 146 extends across the entire thickness of source conductor layer 144 to electrically isolate conduction region 158 and conduction region 160. Isolation region 146 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, doped silicon oxide, any other suitable dielectric materials, or any combination thereof. Patterning process (e.g., photolithography and dry/wet etch) can be used for patterning isolation region 146 in source conductor layer 144. Isolation region 146 then can be formed by thermal growth and/or thin film deposition of the dielectric materials in the patterned region. The layout of multiple conduction regions (e.g., conduction regions 158 and 160) can be defined by

the formation of the isolation regions (e.g., isolation region 146) in source conductor layer 144.

[0057] In some embodiments, NAND string 130 further includes an epitaxial layer 147 on an upper end of semiconductor channel 128 of NAND string 130. Epitaxial layer 147 can include a semiconductor material, such as silicon. Epitaxial layer 147 can be epitaxially grown from a semiconductor layer (e.g., a silicon substrate). For example, epitaxial layer 147 can be a single crystalline silicon layer epitaxially grown from a silicon substrate (e.g., prior to be removed and replaced with source conductor layer 144 in 3D memory device 100). For each NAND string 130, epitaxial layer 147 is referred to herein as an “epitaxial plug.” Epitaxial plug 147 at the upper end of NAND string 130 can contact both conduction region 158 of source conductor layer 144 and semiconductor channel 128 of NAND string 130, thereby providing electrical connections between NAND string 130 and source conductor layer 144. Epitaxial plug 147 can extend vertically through the partial or entire thickness of source selective gate 138 and can function as the channel that can be controlled by source selective gate 138 at the upper end of NAND string 130. Source selective gate 138 can control the conductance of epitaxial plug 147. On the other hand, as conduction region 158 of source conductor layer 144 above source selective gate 138 includes conductive materials, source selective gate 138 cannot control the conductance of conduction region 158. Thus, the control of the source side of NAND string 130 can be performed solely on epitaxial layer 147. In some embodiments, the thickness of source selective gate 138 and the thickness of epitaxial layer 147 can each be tuned. For example, the thickness of source selective gate 138 can be between about 5 nm and about 100 nm (e.g., between 5 nm and 100 nm), and the thickness of epitaxial layer 147 can be between about 1 nm and about 100 nm (e.g., between 1 nm and 100 nm).

[0058] In some embodiments, the array device further includes a source contact 132 that extends vertically through alternating conductor/dielectric stack 142. As shown in FIG. 1, an upper end of source contact 132 can contact conduction region 158 of source conductor layer 144 and can electrically connect to NAND string 130 by conduction region 158 of source conductor layer 144. In some embodiments, multiple NAND strings (e.g., an array of NAND strings of a single memory block, multiple memory blocks, or a portion of a memory block) can be electrically connected to source contact 132 by source

conductor layer 144. Source contact 132 can thus be referred to as a “common source contact” of the multiple NAND strings. Source contact 132 can include conductor materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof. To electrically insulate source contact 132 from surrounding conductor layers 134 in alternating conductor/dielectric stack 142, a dielectric layer with any suitable dielectric materials can be between source contact 132 and alternating conductor/dielectric stack 142.

[0059] In some embodiments, the array device further includes a through array contact (TAC) 162 that extends vertically through alternating conductor/dielectric stack 142. TAC 162 can extend through the entire thickness of alternating conductor/dielectric stack 142, (e.g., all the conductor/dielectric pairs in the vertical direction). An upper end of TAC 162 can contact conduction region 160 in source conductor layer 144. TAC 162 can carry electrical signals from the peripheral device to a BEOL contact layer 166, a BEOL conductor layer 168, and a pad layer 156 by conduction region 160. TAC 162 can include a vertical opening through alternating conductor/dielectric stack 142 (e.g., formed by dry/wet etch process) filled with conductor materials. In some embodiments, a dielectric layer 164 is between TAC 162 and alternating conductor/dielectric stack 142 for electrical insulation purposes. TAC 162 can include conductor materials including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. The opening of TAC 162 can be filled with conductor materials by ALD, CVD, PVD, electroplating, any other suitable processes, or any combination thereof.

[0060] As shown in FIG. 1, 3D memory device 100 can include an array interconnect layer 123 above and in contact with peripheral interconnect layer 122. Array interconnect layer 123 can include bit line contacts 126, one or more conductor layers (e.g., a conductor layer 124), and one or more dielectric layers (e.g., dielectric layers 121 and 125). Each bit line contact 126 can contact the lower end of a corresponding NAND string 130 to individually address corresponding NAND string 130. The conductor layers can include conductor materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof. The dielectric layers can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, low-k dielectrics, or any combination thereof.

[0061] A bonding interface 119 can be formed between dielectric layer 118 of peripheral interconnect layer 122 and dielectric layer 121 of array interconnect layer 123. Bonding interface 119 can also be formed between conductor layer 124 of array interconnect layer 123 and conductor layer 120 of peripheral interconnect layer 122. Each of dielectric layer 118 and dielectric layer 121 can include silicon nitride or silicon oxide.

[0062] In some embodiments, a first semiconductor structure 170 is bonded to a second semiconductor structure 172 at bonding interface 119. First semiconductor structure 170 can include substrate 102, one or more peripheral devices on substrate 102, and peripheral interconnect layer 122. Second semiconductor structure 172 can include source conductor layer 144, array interconnect layer 123, alternating conductor/dielectric stack 142 having a plurality of conductor/dielectric layer pairs, and NAND string 130. First semiconductor structure 170 can include the elements shown below bonding interface 119 in FIG. 1, while second semiconductor structure 172 can include the elements shown above bonding interface 119 in FIG. 1. Peripheral interconnect layer 122 can include conductor layer 120, which contacts conductor layer 124 of array interconnect layer 123 at bonding interface 119. Peripheral interconnect layer 122 can also include dielectric layer 118, which contacts dielectric layer 121 of array interconnect layer 123 at bonding interface 119.

[0063] As shown in FIG. 1, 3D memory device 100 can further include a BEOL interconnect layer 153 above source conductor layer 144. In some embodiments, BEOL interconnect layer 153 includes conductor layers 154 and 168, contact layers 148 and 166, one or more dielectric layers (e.g., a dielectric layer 152), and one or more pad layers (e.g., pad layer 156). BEOL interconnect layer 153 can transfer electrical signals between 3D memory device 100 and external circuits. The conductor layers, contact layers, and pad layers (e.g., including bonding pads) in BEOL interconnect layer 153 can include conductor materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof. The dielectric layers in BEOL interconnect layer 153 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, low-k dielectrics, or any combination thereof.

[0064] BEOL interconnect layer 153 can be electrically connected to the peripheral device. Specifically, contact layer 166 of BEOL interconnect layer 153 can contact conduction region 160 of source conductor layer 144 at the top surface of source conductor layer 144. The upper end of TAC 162 can contact conduction region 160 of

source conductor layer 144 at the bottom surface of source conductor layer 144. The lower end of TAC 162 can contact a contact in array interconnect layer 123.

[0065] In some embodiments, BEOL interconnect layer 153 includes source conductor layer 144 as well. For example, conduction region 158 of source conductor layer 144, in conjunction with contact layer 148, can electrically connect the array device (e.g., NAND string 130 and source contact 132) with other circuits (e.g., BEOL conductor layer 154 and pad layer 156). Similarly, conduction region 160 of source conductor layer 144, in conjunction with contact layer 166, TAC 162, array interconnect layer 123 and peripheral interconnect layer 122, can electrically connect the peripheral device (e.g., transistors 106) with other circuits (e.g., BEOL conductor layer 168 and pad layer 156). In some embodiments, as part of BEOL interconnect layer 153, source conductor layer 144 can be patterned to form any suitable layout for the conduction regions based on the desired interconnect configuration of the array device and peripheral device.

[0066] FIGs. 2A-2D illustrate an exemplary fabrication process for forming a peripheral device and a peripheral interconnect layer. FIG. 8 is a flowchart of an exemplary method 800 for forming a peripheral device and a peripheral interconnect layer. An example of the peripheral device and peripheral interconnect layer depicted in FIGs. 2A-2D and FIG. 8 is the peripheral device (e.g., transistors 106) and peripheral interconnect layer 122 depicted in FIG. 1. It should be understood that the operations shown in method 800 are not exhaustive and that other operations can be performed as well before, after, or between any of the illustrated operations.

[0067] Referring to FIG. 8, method 800 starts at operation 802, in which a peripheral device is formed on a first substrate. The first substrate can be a silicon substrate. As illustrated in FIG. 2A, a peripheral device is formed on a first silicon substrate 202. The peripheral device can include a plurality of transistors 204 formed on first silicon substrate 202. Transistors 204 can be formed by a plurality of processing steps including, but not limited to, photolithography, dry/wet etch, thin film deposition, thermal growth, implantation, chemical mechanical polishing (CMP), or any combination thereof. In some embodiments, doped regions 208 are formed in first silicon substrate 202, which function, for example, as source regions and/or drain regions of transistors 204. In some embodiments, an isolation region 206 is also formed in first silicon substrate 202.

[0068] Method 800 proceeds to operation 804, as illustrated in FIG. 8, in which one or more dielectric layers and conductor layers are formed above the peripheral device. As illustrated in FIG. 2B, a first dielectric layer 210 can be formed on first silicon substrate 202. First dielectric layer 210 can include a contact layer 209, including MEOL contacts, to make electrical connections with the peripheral device (e.g., transistors 204).

[0069] As illustrated in FIG. 2C, a second dielectric layer 216 is formed on first dielectric layer 210. In some embodiments, second dielectric layer 216 is a combination of multiple layers formed in separate steps. For example, second dielectric layer 216 can include a conductor layer 212 and a contact layer 214. The conductor layers (e.g., conductor layer 212) and contact layers (e.g., contact layers 209 and 214) can include conductor materials deposited by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, electroplating, electroless plating, or any combination thereof. Fabrication processes to form the conductor layers and contact layers can also include photolithography, CMP, wet/dry etch, or any combination thereof. The dielectric layers (e.g., dielectric layers 210 and 216) can include dielectric materials deposited by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, or any combination thereof.

[0070] Method 800 proceeds to operation 806, as illustrated in FIG. 8, in which a top dielectric layer and a top conductor layer of a peripheral interconnect layer are formed. The dielectric layers and conductor layers formed at operations 804 and 806 can be collectively referred to as an “interconnect layer” (e.g., the peripheral interconnect layer). Each of the dielectric layers and conductor layers can be a portion of the peripheral interconnect layer that transfers electrical signals to and from the peripheral device. As illustrated in FIG. 2D, a third dielectric layer (the top dielectric layer) 218 is formed on second dielectric layer 216, and a top conductor layer 220 is formed in third dielectric layer 218. As a result, a peripheral interconnect layer 222 is formed. The conductor layers (e.g., conductor layer 220) can include conductor materials deposited by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, electroplating, electroless plating, or any combination thereof. Fabrication processes to form the conductor layer and contact layers can also include photolithography, CMP, wet/dry etch, or any combination thereof. The dielectric layers (e.g., dielectric layer 218) can include

dielectric materials deposited by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, or any combination thereof.

[0071] FIGs. 3A-3D illustrate an exemplary fabrication process for forming an array device and an array interconnect layer. FIG. 9 is a flowchart of an exemplary method 900 for forming an array device and an array interconnect layer. An example of the array device and array interconnect layer depicted in FIGs. 3A-3D and FIG. 9 is the array device (e.g., NAND string 130) and array interconnect layer 123 depicted in FIG. 1. It should be understood that the operations shown in method 900 are not exhaustive and that other operations can be performed as well before, after, or between any of the illustrated operations.

[0072] Referring to FIG. 9, method 900 starts at operation 902, in which an isolation region is formed in a second substrate. The second substrate can be a silicon substrate, such as a second silicon substrate 302 in FIG. 3A. An array device can be formed on second silicon substrate 302. In some embodiments, an isolation region 304 is formed in second silicon substrate 302. Isolation region 304 can be formed by thermal growth and/or thin film deposition. Patterning process (e.g., photolithography and dry/wet etch) can be used for patterning isolation region 304 in second silicon substrate 302.

[0073] Method 900 proceeds to operation 904, as illustrated in FIG. 9, in which a plurality of dielectric layer pairs (also referred to herein as an “alternating dielectric stack”) are formed on the second substrate. As illustrated in FIG. 3B, a plurality of first dielectric layer 308 and second dielectric layer 310 pairs are formed on second silicon substrate 302. The plurality of dielectric pairs can form an alternating dielectric stack 306. Alternating dielectric stack 306 can include an alternating stack of a first dielectric layer 308 and a second dielectric layer 310 that is different from first dielectric layer 308. In some embodiments, each dielectric layer pair includes a layer of silicon nitride and a layer of silicon oxide. In some embodiments, there are more layers than the dielectric layer pairs made of different materials and/or with different thicknesses in alternating dielectric stack 306. In some embodiments, first dielectric layers 308 can each have the same thickness or have different thicknesses. Similarly, second dielectric layers 310 can each have the same thickness or have different thicknesses. In one example, for a first plurality of dielectric pairs in alternating dielectric stack 306, the thickness of each first dielectric layer 308 and second dielectric layer 310 can be between about 5 nm and about

40 nm (e.g., between 5 nm and 40 nm). For a second plurality of dielectric pairs in alternating dielectric stack 306, the thickness of each first dielectric layer 308 and second dielectric layer 310 can be between about 10 nm and about 40 nm (e.g., between 10 nm and 40 nm). For a third plurality of dielectric pairs in alternating dielectric stack 306, the thickness of each first dielectric layer 308 can be between about 5 nm and about 40 nm (e.g., between 5 nm and 40 nm), and the thickness of each second dielectric layer 310 can be between about 50 nm and about 200 nm (e.g., between 50 nm and 200 nm). Alternating dielectric stack 306 can be formed by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, or any combination thereof. In some embodiments, alternating dielectric stack 306 can be replaced by a plurality of conductor/dielectric layer pairs, i.e., an alternating stack of a conductor layer (e.g., polysilicon) and a dielectric layer (e.g., silicon oxide).

[0074] Method 900 proceeds to operation 906, as illustrated in FIG. 9, in which a plurality of NAND strings of the array device are formed on the second substrate. As illustrated in FIG. 3C, NAND string 318 is formed on second silicon substrate 302. Each first dielectric layer 308 of alternating dielectric stack 306 can be replaced by a conductor layer 316, thereby forming a plurality of conductor/dielectric layer pairs in an alternating conductor/dielectric stack 314. The replacement of first dielectric layers 308 with conductor layers 316 can be performed by wet etching first dielectric layers 308 selective to second dielectric layers 310 and filling the structure with conductor layers 316. The thickness of each conductor layer 316 can be between about 5 nm and about 40 nm (e.g., between 5 nm and 40 nm). Conductor layers 316 can include conductor materials including, but not limited to, W, Co, Cu, Al, doped silicon, polysilicon, silicides, or any combination thereof. Conductor layers 316 can be filled by thin film deposition processes, such as CVD, ALD, any other suitable process, or any combination thereof.

[0075] In some embodiments, conductor layers 316 in alternating conductor/dielectric stack 314 are used to form the selective gates and word lines for NAND string 318. At least some of conductor layers 316 in alternating dielectric stack 306 (e.g., except the top and bottom conductor layers 316) can each be used as a word line for NAND string 318. As illustrated in FIG. 3C, the top conductor layer (the uppermost conductor layer) and the bottom conductor layer (the lowermost conductor layer) in alternating conductor/dielectric stack 314 can each be patterned to form a drain selective gate 330

and a source selective gate 328, respectively, for NAND string 318. In some embodiments, one or more pairs of first dielectric layer 308 and second dielectric layer 310 at the upper end of alternating dielectric stack 306 are patterned, and first dielectric layer 308 in the top patterned dielectric layer pairs can be replaced with a corresponding conductor layer 316, thereby forming drain selective gate 330. In some embodiments, an additional conductor layer is formed on top of alternating conductor/dielectric stack 314 and is patterned to form the drain selective gate for NAND string 318.

[0076] In some embodiments, fabrication processes to form NAND string 318 further include forming a semiconductor channel 320 that extends vertically through alternating conductor/dielectric stack 314. In some embodiments, fabrication processes to form NAND string 318 further include forming a dielectric layer 322 between semiconductor channel 320 and the plurality of conductor/dielectric layer pairs in alternating conductor/dielectric stack 314. Dielectric layer 322 can be a composite dielectric layer, such as a combination of multiple dielectric layers including, but not limited to, a tunneling layer, a storage layer, and a blocking layer.

[0077] The tunneling layer can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. Electrons or holes from the semiconductor channel can tunnel to a storage layer of NAND string 318 through the tunneling layer. The thickness of the tunneling layer (e.g., in the radial direction of NAND string 318) can be between about 5 nm and about 15 nm (e.g., between 5 nm and 15 nm). The storage layer can include materials for storing charge for memory operation. The storage layer materials include, but are not limited to, silicon nitride, silicon oxynitride, a combination of silicon oxide and silicon nitride, or any combination thereof. The thickness of the storage layer (e.g., in the radial direction of NAND string 318) can be between about 3 nm and about 15 nm (e.g., between 3 nm and 15 nm). The blocking layer can include dielectric materials including, but not limited to, silicon oxide or a combination of silicon oxide/silicon nitride/silicon oxide (ONO) with a thickness between about 4 nm and about 15 nm (e.g., between 4 nm and 15 nm). The blocking layer can further include a high-k dielectric layer, such as a Al_2O_3 layer with a thickness between about 1 nm and about 5 nm (e.g., between 1 nm and 5 nm). Dielectric layer 322 can be formed by processes such as ALD, CVD, PVD, any other suitable processes, or any combination thereof.

[0078] In some embodiments, fabrication processes to form NAND string 318 further include forming an epitaxial layer 326 at an end of NAND string 318. As illustrated in FIG. 3C, epitaxial layer 326 can be formed at a lower end of NAND string 318 as an epitaxial plug. Epitaxial layer 326 can be a silicon layer in contact with and epitaxially grown from second silicon substrate 302 and can be implanted to a desired doping level.

[0079] In some embodiments, operation 906 further includes forming one or more source contacts (e.g., a common source contact). As illustrated in FIG. 3C, a source contact 324 that extends vertically through alternating conductor/dielectric stack 314 can be formed on second silicon substrate 302. Source contact 324 can have an end in contact with second silicon substrate 302. In some embodiments, source contact 324 can be electrically connected to multiple NAND strings 318 by second silicon substrate 302. Selective gate 328 can be formed at the lower end of NAND string 318 to turn on and turn off epitaxial layer 326 as a switch. In some embodiments, epitaxial layer 326 extends vertically through the partial or entire thickness of selective gate 328. Source contact 324 can include conductor materials including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. Source contact 324 can be formed by a dry/wet etch process to form a vertical opening through alternating conductor/dielectric stack 314, followed by a fill process to fill the opening with conductor materials and other materials (e.g., dielectric materials.) The opening can be filled by ALD, CVD, PVD, electroplating, any other suitable processes, or any combination thereof.

[0080] Method 900 proceeds to operation 908, as illustrated in FIG. 9, in which an array interconnect layer is formed above the plurality of NAND strings. The array interconnect layer can transfer electrical signals between the NAND strings and other parts of the 3D memory device, such as the peripheral device. As illustrated in FIG. 3D, an array interconnect layer 338 is formed above NAND string 318. In some embodiments, fabrication processes to form array interconnect layer 338 include forming a dielectric layer 334, followed by forming a bit line contact 335 in contact with NAND string 318 in dielectric layer 334. Dielectric layer 334 can include one or more layers of dielectric materials such as silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. Bit line contact 335 can be formed by forming an opening in dielectric layer 334, followed by filling the opening with conductor materials and dielectric materials. Bit line contact 335 can include conductor materials including, but not limited to, W, Co, Cu, Al,

doped silicon, silicides, or any combination thereof. The opening of bit line contact 335 can be filled with conductor materials and dielectric materials by ALD, CVD, PVD, any other suitable processes, or any combination thereof.

[0081] In some embodiments, fabrication processes to form array interconnect layer 338 further include forming one or more conductor layers (e.g., a conductor layer 340) and one or more contact layers (e.g., contact layer 344) in dielectric layer 334. Conductor layer 340 and contact layer 344 can include conductor materials including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. Conductor layer 340 and conductor contact layer 344 can be formed by any suitable known BEOL methods.

[0082] In some embodiments, fabrication processes to form array interconnect layer 338 further include forming a top conductor layer 342 and a top dielectric layer 336. Top conductor layer 342 can include conductor materials including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. Dielectric layer 336 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.

[0083] FIG. 4 illustrates an exemplary fabrication process for joining an array device and a peripheral device. FIGs. 5A–5B and FIGs. 6A–6B illustrate various exemplary fabrication processes for forming a source conductor layer. FIG. 7 illustrates an exemplary fabrication process for forming a BEOL interconnect layer on a source conductor layer. FIG. 10 is a flowchart for an exemplary method 1000 for forming a 3D memory device with an array device and a peripheral device. An example of the 3D memory device and the source conductor layer depicted in FIGs. 4–7 is 3D memory device 100 and source conductor layer 144 depicted in FIG. 1. It should be understood that the operations shown in method 1000 are not exhaustive and that other operations can be performed as well before, after, or between any of the illustrated operations.

[0084] Referring to FIG. 10, method 1000 starts at operation 1002, in which the array device (and the array interconnect layer) is positioned below the second substrate (e.g., by flipping the second substrate upside down), and the array interconnect layer is aligned with the peripheral interconnect layer. As illustrated in FIG. 4, array interconnect layer 338 can be placed below second silicon substrate 302. In some embodiments, aligning array interconnect layer 338 with peripheral interconnect layer 222 is performed by

aligning conductor layer 342 of array interconnect layer 338 with conductor layer 220 of peripheral interconnect layer 222. As a result, conductor layer 342 can contact conductor layer 220 when the array device is joined with the peripheral device.

[0085] Method 1000 proceeds to operation 1004, as illustrated in FIG. 10, in which the array interconnect layer is joined with the peripheral interconnect layer. The array interconnect layer can be joined with the peripheral interconnect layer by flip-chip bonding the first and second substrates. In some embodiments, the array interconnect layer and the peripheral interconnect layer are joined by hybrid bonding of the first substrate and the second substrate in a face-to-face manner, such that the array interconnect layer is above and in contact with the peripheral interconnect layer in the resulting 3D memory device. Hybrid bonding (also known as “metal/dielectric hybrid bonding”) can be a direct bonding technology (e.g., forming bonding between surfaces without using intermediate layers, such as solder or adhesives), which obtains metal-metal bonding and dielectric-dielectric bonding simultaneously. As illustrated in FIG. 4, array interconnect layer 338 can be joined with peripheral interconnect layer 222, thereby forming a bonding interface 403.

[0086] A treatment process can be used to enhance the bonding strength between array interconnect layer 338 and peripheral interconnect layer 222 before or during the joining process of the two interconnect layers. In some embodiments, each of dielectric layer 336 and dielectric layer 218 includes silicon oxide or silicon nitride. In some embodiments, the treatment process includes a plasma treatment that treats the surfaces of array interconnect layer 338 and peripheral interconnect layer 222 so that the surfaces of the two interconnect layers form chemical bonds between dielectric layer 336 and dielectric layer 218. In some embodiments, the treatment process includes a wet process that treats the surfaces of array interconnect layer 338 and peripheral interconnect layer 222 so that the surfaces of the two interconnect layers form chemical bonds to enhance the bonding strength between two dielectric layers 336 and 218. In some embodiments, the treatment process includes a thermal process that can be performed at a temperature from about 250°C to about 600°C (e.g., from 250°C to 600°C). The thermal process can cause inter-diffusion between conductor layer 342 and conductor layer 220. As a result, conductor layer 342 can be inter-mixed with conductor layer 220 after the joining process. Conductor layer 342 and conductor layer 220 can each include Cu.

[0087] Method 1000 proceeds to operation 1006, as illustrated in FIG. 10, in which a source conductor layer is formed above the NAND strings. The second substrate on which the alternating conductor/dielectric stack (and the NAND strings therein) is formed can be removed after the joining process, and the source conductor layer can be formed on the alternating conductor/dielectric stack (and the NAND strings therein). That is, the source conductor layer can replace the second substrate after the joining process by being formed at the original location of the second substrate (e.g., on the alternating conductor/dielectric stack). In some embodiments, the source conductor layer can be patterned to form one or more isolation regions.

[0088] As illustrated in FIG. 5A, in some embodiments, second silicon substrate 302 (as shown in FIG. 4) has been removed, and a source conductor layer 405 is formed on alternating conductor/dielectric stack 314. In other words, source conductor layer 405 can replace second silicon substrate 302 at the original location of second silicon substrate 302. Source conductor layer 405 can include conductive materials, so that the conductance of source conductor layer 405 cannot be affected by source selective gate 328 below source conductor layer 405. The conductive materials in source conductor layer 405 can provide electrical connections between source contact 324 and NAND string 318. The conductive materials in source conductor layer 405 can include, but is not limited to, metals, metal alloys, and metal silicides. In some embodiments, source conductor layer 405 includes one or more metals, such as Cu, Co, Ni, Ti, W, or any other suitable metals. In some embodiments, source conductor layer 405 includes one or more metal alloys, each of which is an alloy of at least two of Cu, Co, Ni, Ti, W (e.g., TiNi alloy or a combination of TiNi alloy and TiW alloy), or any other suitable metal alloys. In some embodiments, source conductor layer 405 includes one or more metal silicides, such as copper silicide, cobalt silicide, nickel silicide, titanium silicide, tungsten silicide, or any other suitable metal silicides.

[0089] In some embodiments, source conductor layer 405 has a thickness between about 20 nm and about 50 μm , such as between 20 nm and 50 μm (e.g., 20 nm, 30 nm, 40 nm, 50 nm, 60 nm, 70 nm, 80 nm, 90 nm, 100 nm, 110 nm, 120 nm, 130 nm, 140 nm, 150 nm, 160 nm, 170 nm, 180 nm, 190 nm, 200 nm, 500 nm, 1 μm , 5 μm , 10 μm , 15 μm , 20 μm , 25 μm , 30 μm , 35 μm , 40 μm , 45 μm , 50 μm , any range bounded on the lower end by any of these values, or in any range defined by any two of these values). In some

embodiments, source conductor layer 405 has a thickness between about 200 nm and about 5 μm , such as between 200 nm and 5 μm (e.g., 200 nm, 300 nm, 400 nm, 500 nm, 600 nm, 700 nm, 800 nm, 900 nm, 1 μm , 2 μm , 3 μm , 4 μm , 5 μm , any range bounded on the lower end by any of these values, or in any range defined by any two of these values). Source conductor layer 405 can be formed by one or more thin film deposition processes including, but not limited to, CVD, PVD, and ALD.

[0090] FIG. 11 is a flowchart of an exemplary method for forming the source conductor layer. It should be understood that the operations shown in method 1100 are not exhaustive and that other operations can be performed as well as before, after, or between any of the illustrated operations. Referring to FIG. 11, method 1100 starts at operation 1102, in which the second substrate is thinned. For example, second silicon substrate 302 (in FIG. 4) can be thinned to become a thinned silicon substrate. In some embodiments, second silicon substrate 302 can be thinned from the top surface (opposite to the bottom surface that is in contact with alternating conductor/dielectric stack 314) until isolation region 304 is exposed. That is, the thickness of the thinned second substrate can be the same as that of the isolation region formed in the second substrate.

[0091] Method 1100 proceeds to operation 1104, as illustrated in FIG. 11, in which the thinned second substrate is removed. The thinned second substrate can be removed by grinding, wet/dry etching, CMP, or any combination thereof. It is understood that in some embodiments, operation 1102 can be skipped, and the second substrate (e.g., second silicon substrate 302 in FIG. 4) can be removed in a single process without being thinned first.

[0092] Method 1100 proceeds to operation 1106, as illustrated in FIG. 11, in which a source conductor layer is formed at the original location of the second substrate that has been removed. As illustrated in FIG. 5A, source conductor layer 405 can be formed on alternating conductor/dielectric stack 314, so that the bottom surface of source conductor layer 405 can be in contact with the top dielectric layer of alternating conductor/dielectric stack 314 as well as the upper end of NAND string 318 (e.g., epitaxial layer 326) and the upper end of source contact 324.

[0093] Method 1100 proceeds to operation 1108, as illustrated in FIG. 11, in which the source conductor layer is patterned. In some embodiments, the source conductor layer is patterned to form one or more isolation regions. The remaining conductive materials in

the source conductor layer can become conduction regions electrically isolated by the isolation regions. As illustrated in FIG. 5B, an isolation region 407 can be formed in source conductor layer 405. Isolation region 407 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, doped silicon oxide, any other suitable dielectric materials, or any combination thereof. Patterning process (e.g., photolithography and dry/wet etch) can be used for patterning isolation region 407 in source conductor layer 405. Isolation region 407 can then be formed by thermal growth and/or thin film deposition of dielectric materials in the patterned region. Source conductor layer 405 can be patterned to form any suitable layout with different numbers of conduction regions and isolation regions in different arrangements. The different layouts of conduction regions and isolation regions in source conductor layer 405 can be used to drive the memory array in various configurations, such as an array of NAND strings in a single memory block, in multiple memory blocks, or in a portion of a memory block (e.g., one or more memory fingers). The conduction regions formed in source conductor layer 405 can provide additional electrical connections—besides electrical connections between NAND string 318 and source contact 324—such as electrical connections between the peripheral device and the BEOL interconnects and between the array device and the BEOL interconnects.

[0094] FIG. 12 is a flowchart of another exemplary method for forming the source conductor layer. It should be understood that the operations shown in method 1200 are not exhaustive and that other operations can be performed as well as before, after, or between any of the illustrated operations. Referring to FIG. 12, method 1200 starts at operation 1202, in which the second substrate is thinned. For example, second silicon substrate 302 (in FIG. 4) can be thinned to become a thinned second silicon substrate 417 (in FIG. 6A). In some embodiments, second silicon substrate 302 can be thinned from its upper side (opposite to its bottom side on which NAND string 318 is formed) until isolation region 304 is exposed. That is, the thickness of thinned second silicon substrate 417 can be the same as that of isolation region 304 formed in second silicon substrate 302. The second substrate can be thinned by grinding, wet/dry etching, CMP, or any combination thereof.

[0095] Method 1200 proceeds to operation 1204, as illustrated in FIG. 12, in which a metal layer is formed on the thinned second substrate. As illustrated in FIG. 6A, a metal

layer 419 can be formed on the upper side of thinned second silicon substrate 417. Metal layer 419 can include Co, Ni, Ti, W, any other suitable metal that can form metal silicides, or any combination thereof. Metal layer 419 can be formed by one or more thin film deposition processes including, but not limited to, CVD, PVD, ALD, or any combination thereof. In some embodiments, the thickness of metal layer 419 is at least about 2 nm (e.g., at least 2 nm), such as between about 2 nm and about 500 nm (e.g., between 2 nm and 500 nm). The thickness of metal layer 419 can be thick enough for the subsequent silicidation process.

[0096] Method 1200 proceeds to operation 1206, as illustrated in FIG. 12, in which a metal silicide layer is formed. The metal silicide layer can be formed based on a reaction of silicon in the thinned second substrate and metal in the metal layer. As illustrated in FIG. 6B, a source conductor layer 421 can be a metal silicide layer formed by the silicidation process based on the reaction of thinned second silicon substrate 417 and metal layer 419. The metal silicide layer can be formed by a thermal treatment (e.g., annealing, sintering, or any other suitable process), resulting in the formation of metal-silicon alloy (silicide). The annealing process can include, for example, rapid thermal annealing (RTA) and laser annealing. The dielectric materials in isolation region 304 cannot react with metal in metal layer 419. Thus, isolation region 304 can remain in source conductor layer 421. In some embodiments, the unreacted portion of metal layer 419 after the silicidation process can be removed from source conductor layer 421. The removal of the unreacted portion of metal layer 419 can be performed by a wet etch process, a dry etch process, or any other suitable process.

[0097] The metal silicide materials in source conductor layer 421 can depend on the metal materials in metal layer 419. For example, if metal layer 419 includes Co, Ni, Ti, or W, then source conductor layer 421 includes cobalt silicide, nickel silicide, titanium silicide, or tungsten silicide, respectively. In some embodiments, the metal silicide materials in source conductor layer 421 are conductive materials with an electrical conductivity that is high enough so that the conduction of source conductor layer 421 cannot be affected by source selective gate 328, and source conductor layer 421 can electrically connect NAND string 318 and source contact 324. In some embodiments, the electrical conductivity of the metal silicide materials in source conductor layer 421 is at least about 1×10^4 S/m at about 20°C (e.g., at least 1×10^4 S/m at 20°C), such as between

about 1×10^4 S/m and about 1×10^7 S/m at about 20°C (e.g., between 1×10^4 S/m and 1×10^7 S/m at 20°C).

[0098] As illustrated in FIG. 6B, isolation region 304 formed prior to the formation of source conductor layer 421 can remain in source conductor layer 421, while the conduction regions electrically isolated by isolation region 304 include the metal silicides formed by the silicidation process. That is, in some embodiments, the conduction regions and isolation regions in source conductor layer 421 can be patterned prior to the formation of the metal silicide layer (e.g., operation 902 in method 900). In some embodiments, additional patterning is performed after the formation of the metal silicide layer (i.e., by patterning source conductor layer 421 directly) to form additional isolation regions (not shown in FIG. 6B). For example, method 1200 proceeds to operation 1208, as illustrated in FIG. 12, in which the metal silicide layer is patterned to form isolation regions and conduction regions electrically isolated by the isolation region. It is understood that in some embodiments, the isolation regions in the second substrate (e.g., isolation region 304) may not be necessary, and the isolation regions in source conductor layer 421 can be formed by patterning source conductor layer 421 after the silicidation process.

[0099] Patterning process (e.g., photolithography and dry/wet etch) can be used for patterning source conductor layer 421 after the formation of the metal silicide layer. Isolation regions then can be formed by thermal growth and/or thin film deposition of dielectric materials in the patterned region. Isolation regions can include dielectric materials, such as silicon oxide, silicon nitride, silicon oxynitride, doped silicon oxide, any other suitable dielectric materials, or any combination thereof. The layout of multiple conduction regions can be defined after the formation of the isolation regions in source conductor layer 421. The different layouts of conduction regions and isolation regions in source conductor layer 421 can be used to drive the memory array in various configurations, such as an array of NAND strings in a single memory block, in multiple memory blocks, or in a portion of a memory block (e.g., one or more memory fingers). The conduction regions formed in source conductor layer 421 can provide additional electrical connections besides between NAND string 318 and source contact 324, such as between the peripheral device and the BEOL interconnects and between the array device and the BEOL interconnects.

[0100] Referring back to FIG. 10, method 1000 proceeds to operation 1008, in which a BEOL interconnect layer is formed above the source conductor layer. As illustrated in FIG. 7, a BEOL interconnect layer 702 is formed above source conductor layer 405/421. BEOL interconnect layer 702 can include a dielectric layer 409, one or more contact layers 411, one or more conductor layers 413, and a pad layer 415. Dielectric layer 409 can be a combination of multiple dielectric layers formed at separate process steps. Contact layer 411, conductor layer 413, and pad layer 415 can include conductor materials including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. Dielectric layer 409 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, low-k dielectrics, or any combination thereof. In some embodiments, pad layer 415 is electrically connected to external circuits or devices to transfer electrical signals between the joined array/peripheral device and the external circuits or devices. In some embodiments, BEOL interconnect layer 702 (e.g., contact layer 411) is electrically connected to source conductor layer 405/421 (e.g., in contact with the top surface of a conduction region of source conductor layer 405/421).

[0101] It is to be understood that in some embodiments, the order of forming the array device/array interconnect layer and forming the peripheral device/peripheral interconnect layer can be modified, or the fabrication of the array device/array interconnect layer and the fabrication of the peripheral device/peripheral interconnect layer can be performed in parallel. Also, the order of forming the source conductor layer on the alternating conductor/dielectric stack and joining the array device and the peripheral device can be modified, according to some embodiments. In some embodiments, the source conductor layer is formed on the alternating conductor/dielectric stack prior to the joining of the array device and the peripheral device. In one example, after forming the NAND strings on the second substrate, the source conductor layer can be first formed to replace the second substrate, and then the array interconnect layer can be formed. In another example, after forming the NAND strings on the second substrate, the array interconnect layer can be formed first, and then the source conductor layer can be formed to replace the second substrate. In general, the timing of forming the source conductor layer is not limited and can occur in any suitable timing during the fabrication process of the 3D memory device (e.g., 3D memory device 100) disclosed herein.

- [0102] Various embodiments in accordance with the present disclosure provide a 3D memory device with a source conductor layer in place of the silicon channel in the substrate used by other 3D memory devices. By replacing silicon with conductive materials (e.g., metal, metal alloy, and/or metal silicide) that form the source conductor layer disclosed herein, the resistance of the source side (e.g., between the common source contact and the NAND strings) of the 3D memory device can be reduced, thereby increasing the device operation speed. In some embodiments, the conduction mechanism for erase operation of the source selective gate can become driven by gate-induced drain leakage (GIDL).
- [0103] Moreover, compared with silicon substrate, the source conductor layer disclosed herein can be more easily patterned into any suitable layout (e.g., with different isolation regions) for driving a single memory block, multiple memory blocks, or a portion of a memory block as desired, which can enhance the driving capability of the peripheral device for the memory array. Due to its conductive nature, the source conductor layer disclosed herein can be patterned and used as an interconnect layer (e.g., part of the BEOL interconnect).
- [0104] In some embodiments, a NAND memory device includes a substrate, an alternating conductor/dielectric stack, a NAND string, a source conductor layer, and a source contact. The alternating conductor/dielectric stack includes a plurality of conductor/dielectric pairs above the substrate. The NAND string extends vertically through the alternating conductor/dielectric stack. The source conductor layer is above the alternating conductor/dielectric stack and is in contact with a first end of the NAND string. The source contact includes a first end in contact with the source conductor layer. The NAND string is electrically connected to the source contact by the source conductor layer.
- [0105] In some embodiments, a 3D memory device includes a substrate, a peripheral device on the substrate, a plurality of memory strings each extending vertically above the peripheral device, and a source conductor layer above the plurality of memory strings. An upper end of each of the plurality of memory strings is in contact with a first surface of the source conductor layer.
- [0106] In some embodiments, a method for forming a NAND memory device is disclosed. An alternating conductor/dielectric stack is formed on a first substrate. A NAND string and a source contact both extending vertically through the alternating conductor/dielectric

stack are formed. The first substrate is replaced with a source conductor layer, so that the source conductor layer is in contact with a first end of the NAND string and a first end of the source contact, and the NAND string is electrically connected to the source contact by the source conductor layer.

[0107] In some embodiments, a method for forming a 3D memory device is disclosed. An alternating conductor/dielectric stack is formed on a first substrate. A plurality of memory strings extending vertically through the alternating conductor/dielectric stack are formed, so that a first end of each of the plurality of memory strings is in contact with a first surface of the first substrate. The first substrate is removed. A source conductor layer is formed, so that the first end of each of the plurality of memory strings is in contact with a first surface of the source conductor layer.

[0108] In some embodiments, a method for forming a 3D memory device is disclosed. An alternating conductor/dielectric stack is formed on a first substrate. A plurality of memory strings extending vertically through the alternating conductor/dielectric stack are formed on a first side of the first substrate. The first substrate is thinned from a second side of the first substrate. A metal layer is formed on the second side of the thinned first substrate. A source conductor layer is formed based on a reaction between at least part of the metal layer and the thinned first substrate.

[0109] The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.

[0110] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can

be defined so long as the specified functions and relationships thereof are appropriately performed.

[0111] The Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0112] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A NAND memory device, comprising:
 - a substrate;
 - an alternating conductor/dielectric stack comprising a plurality of conductor/dielectric pairs above the substrate;
 - a NAND string extending vertically through the alternating conductor/dielectric stack;
 - a source conductor layer above the alternating conductor/dielectric stack and in contact with a first end of the NAND string; and
 - a source contact comprising a first end in contact with the source conductor layer, wherein the NAND string is electrically connected to the source contact by the source conductor layer.
2. The NAND memory device of claim 1, wherein the source conductor layer comprises one or more conduction regions each comprising one or more of a metal, a metal alloy, and a metal silicide.
3. The NAND memory device of claim 2, wherein the metal comprises one or more of copper, cobalt, nickel, titanium, and tungsten.
4. The NAND memory device of claim 2, wherein the metal alloy comprises an alloy of at least two of copper, cobalt, nickel, titanium, and tungsten.
5. The NAND memory device of claim 2, wherein the metal silicide comprises one or more of copper silicide, cobalt silicide, nickel silicide, titanium silicide, and tungsten silicide.
6. The NAND memory device of any one of claims 1-5, further comprising an epitaxial silicon layer between the NAND string and the source conductor layer, wherein the NAND string is electrically connected to the source conductor layer by the epitaxial silicon layer.
7. The NAND memory device of any one of claims 1-6, wherein:

the source conductor layer comprises a plurality of conduction regions and one or more isolation regions electrically isolating the plurality of conduction regions; and

the NAND string is electrically connected to the source contact by a first conduction region of the plurality of conduction regions.

8. The NAND memory device of claim 7, further comprising a through array contact (TAC) extending vertically through the alternating conductor/dielectric stack, wherein the TAC is in contact with a second conduction region of the plurality of conduction regions.

9. The NAND memory device of claim 7 or 8, further comprising a first interconnect layer comprising a first contact, wherein the NAND string is electrically connected to the first contact by the first conduction region.

10. The NAND memory device of claim 8, further comprising a first interconnect layer comprising a second contact, wherein the TAC is electrically connected to the second contact by the second conduction region.

11. The NAND memory device of any one of claims 1-10, further comprising a peripheral device between the substrate and the NAND string.

12. The NAND memory device of claim 11, further comprising a second interconnect layer above and in contact with the peripheral device, wherein the second interconnect layer comprises one or more conductor layers in one or more dielectric layers.

13. The NAND memory device of claim 12, further comprising a third interconnect layer in contact with a second end of the NAND string and a second end of the source contact, wherein the third interconnect layer comprises one or more conductor layers in one or more dielectric layers.

14. The NAND memory device of claim 13, further comprising a bonding interface between the second interconnect layer and the third interconnect layer, wherein the peripheral

device is electrically connected to the NAND string by the second interconnect layer and the third interconnect layer.

15. A method for forming a NAND memory device, comprising:
forming an alternating conductor/dielectric stack on a first substrate;
forming a NAND string and a source contact both extending vertically through the alternating conductor/dielectric stack; and
replacing the first substrate with a source conductor layer, so that the source conductor layer is in contact with a first end of the NAND string and a first end of the source contact, and the NAND string is electrically connected to the source contact by the source conductor layer.

16. The method of claim 15, wherein the source conductor layer comprises one or more conduction regions each comprising one or more of a metal, a metal alloy, and a metal silicide.

17. The method of claim 15 or 16, wherein replacing the first substrate with a source conductor layer comprises:
removing the first substrate; and
forming the source conductor layer at an original location of the first substrate.

18. The method of claim 17, wherein removing the first substrate comprises:
thinning the first substrate; and
removing the thinned first substrate.

19. The method of claim 15, wherein replacing the first substrate with a source conductor layer comprises:
forming a metal layer on the first substrate; and
forming a metal silicide layer based on a reaction between silicon in the first substrate and a metal in the metal layer.

20. The method of claim 19, wherein forming a metal layer comprises:
thinning the first substrate; and

forming the metal layer on the thinned first substrate.

21. The method of claim 20, wherein forming a metal layer further comprises:
forming an isolation region at a first surface of the first substrate that is in contact with the alternating conductor/dielectric stack; and
thinning the first substrate from a second surface of the first substrate to expose the isolation region.

22. The method of any one of claims 15-21, further comprising forming one or more isolation regions in the source conductor layer.

23. The method of any one of claims 15-22, further comprising:
forming a peripheral device on a second substrate; and
joining the NAND string and the peripheral device, so that the NAND string is between the first substrate and the peripheral device.

24. The method of claim 23, wherein joining the NAND string and the peripheral device comprises:
forming a first interconnect layer in contact with a second end of the NAND string and a second end of the source contact;
forming a second interconnect layer in contact with the peripheral device; and
forming a bonding interface between the first interconnect layer and the second interconnect layer, so that the peripheral device is electrically connected to the NAND string by the first interconnect layer and the second interconnect layer.

25. The method of claim 24, wherein:
forming a first interconnect layer comprises forming one or more conductor layers in one or more dielectric layers; and
forming a second interconnect layer comprises forming one or more conductor layers in one or more dielectric layers.

26. The method of claim 25, wherein forming a bonding interface comprises one or more of (i) forming chemical bonds between one of the dielectric layers in the first interconnect layer and one of the dielectric layers in the second interconnect layer, and (ii) causing physical inter-diffusion between one of the conductor layers in the first interconnect layer and one of the conductor layers in the second interconnect layer.

27. A three-dimensional (3D) memory device, comprising:
a substrate;
a peripheral device on the substrate;
a plurality of memory strings each extending vertically above the peripheral device; and
a source conductor layer above the plurality of memory strings, wherein an upper end of each of the plurality of memory strings is in contact with a first surface of the source conductor layer.

28. The 3D memory device of claim 27, wherein the source conductor layer comprises a conduction region with an electrical conductivity of at least about 1×10^4 S/m at about 20°C.

29. The 3D memory device of claim 27, wherein the source conductor layer comprises a conduction region comprising one or more of a metal, a metal alloy, and a metal silicide.

30. The 3D memory device of any one of claims 27-29, wherein each of the plurality of memory strings comprises an epitaxial plug at the upper end of the memory string.

31. The 3D memory device of claim 30, wherein the epitaxial plug comprises a single crystalline silicon.

32. The 3D memory device of claim 30 or 31, wherein each of the plurality of memory strings comprises a selective gate configured to control a conductance of a corresponding epitaxial plug.

33. The 3D memory device of claim 32, wherein a conductance of the source conductor layer is independent from the selective gate.

34. The 3D memory device of any one of claims 27-33, further comprising a first interconnect layer on a second surface of the source conductor layer.

35. The 3D memory device of claim 34, further comprising:
an alternating conductor/dielectric stack above the peripheral device, wherein each of the plurality of memory strings extends vertically through the alternating conductor/dielectric stack;
and
a second interconnect layer between the peripheral device and the alternating conductor/dielectric stack.

36. The 3D memory device of claim 35, wherein the source conductor layer comprises a first conduction region, a second conduction region, and an isolation region electrically isolating the first conduction region and the second conduction region.

37. The 3D memory device of claim 36, wherein each of the plurality of memory strings is in contact with the first conduction region of the source conductor layer.

38. The 3D memory device of claim 36 or 37, further comprising a first contact extending vertically through the alternating conductor/dielectric stack and in contact with the first conduction region of the source conductor layer.

39. The 3D memory device of any one of claims 36-38, wherein the first interconnect layer comprises a second contact in contact with the second conduction region of the source conductor layer.

40. The 3D memory device of claim 39, further comprising a third contact extending vertically through the alternating conductor/dielectric stack and in contact with the second conduction region and the second interconnect layer at a respective end, so that the first interconnect layer is electrically connected to the second interconnect layer.

41. The 3D memory device of any one of claims 27-40, wherein the source conductor layer is in a trench shape or a plate shape in a plan view.

42. A method for forming a three-dimensional (3D) memory device, comprising:
forming an alternating conductor/dielectric stack on a first substrate;
forming a plurality of memory strings extending vertically through the alternating conductor/dielectric stack, so that a first end of each of the plurality of memory strings is in contact with a first surface of the first substrate;
removing the first substrate; and
forming a source conductor layer, so that the first end of each of the plurality of memory strings is in contact with a first surface of the source conductor layer.

43. The method of claim 42, further comprising forming a first interconnect layer on a second surface of the source conductor layer.

44. The method of claim 42 or 43, further comprising patterning the source conductor layer to form an isolation region in the source conductor layer.

45. The method of any one of claims 42-44, further comprising:
forming a second interconnect layer above the plurality of memory strings on the first substrate;
forming, on a second substrate, a peripheral device;
forming a third interconnect layer above the peripheral device on the second substrate;
and
bonding the first substrate and the second substrate, so that the second interconnect layer is above and in contact with the third interconnect layer.

46. A method for forming a three-dimensional (3D) memory device, comprising:
forming an alternating conductor/dielectric stack on a first substrate;
forming, on a first side of the first substrate, a plurality of memory strings extending vertically through the alternating conductor/dielectric stack;

thinning the first substrate from a second side of the first substrate;
forming, on the second side of the thinned first substrate, a metal layer; and
forming a source conductor layer based on a reaction between at least part of the metal layer and the thinned first substrate.

47. The method of claim 46, further comprising patterning the first substrate to form an isolation region in the first substrate, wherein the isolation region remains in the source conductor layer.

48. The method of claim 46, further comprising patterning the source conductor layer to form an isolation region in the source conductor layer.

49. The method of any one of claims 46-48, wherein the first substrate comprises silicon, and the source conductor layer comprises a metal silicide.

50. The method of any one of claims 46-49, further comprising:
forming a first interconnect layer above the plurality of memory strings on the first substrate;
forming, on a second substrate, a peripheral device;
forming a second interconnect layer above the peripheral device, on the second substrate,;
and
bonding the first substrate and the second substrate, so that the first interconnect layer is above and in contact with the second interconnect layer.

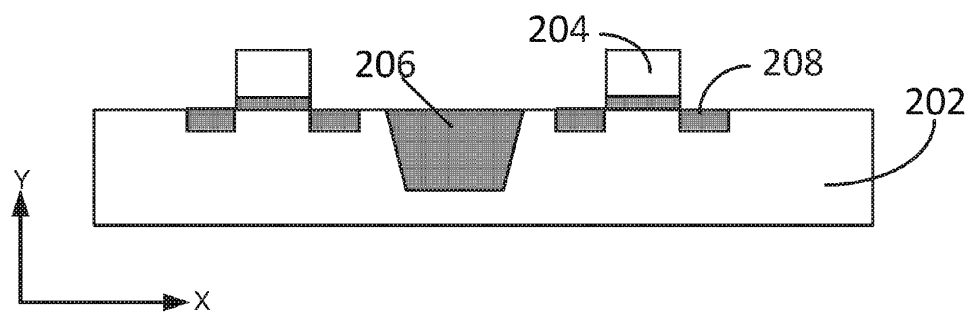


FIG. 2A

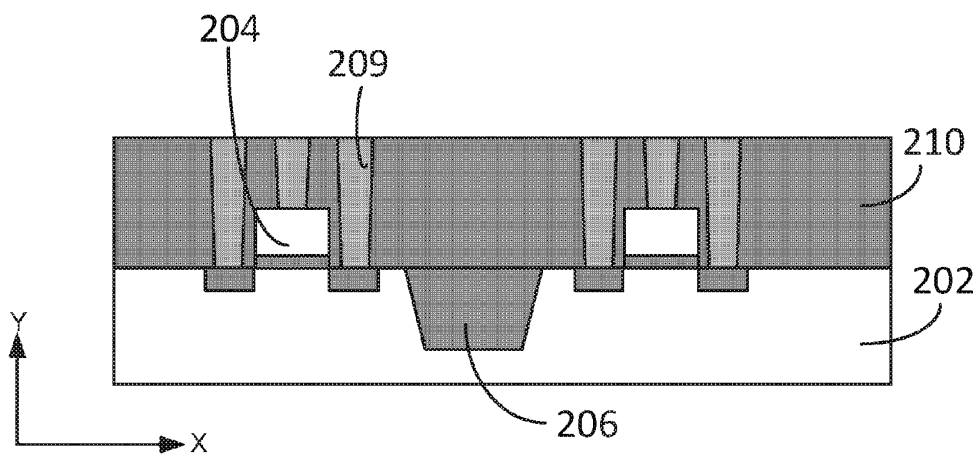


FIG. 2B

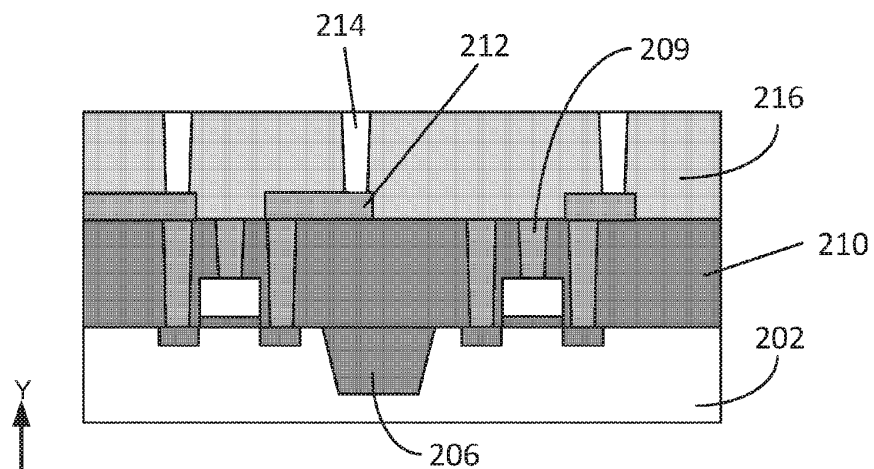


FIG. 2C

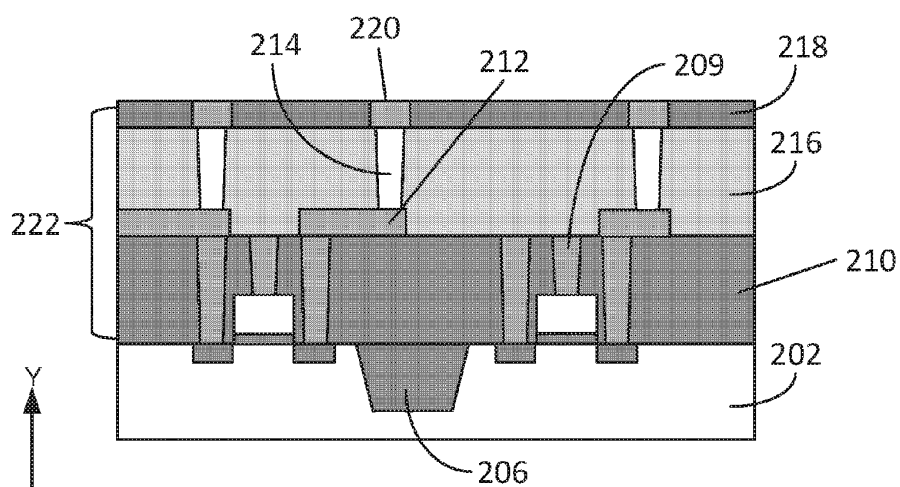


FIG. 2D

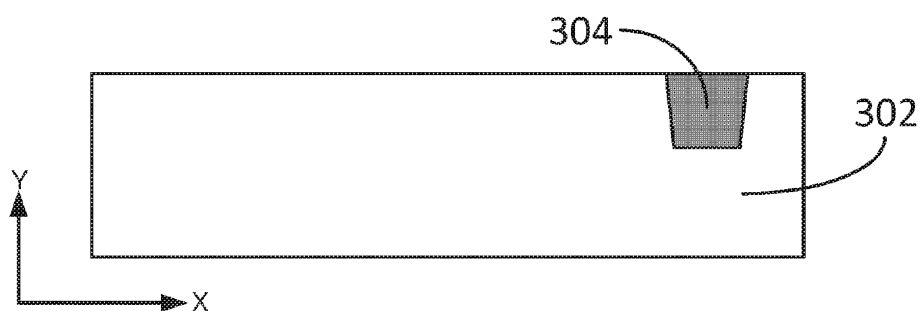


FIG. 3A

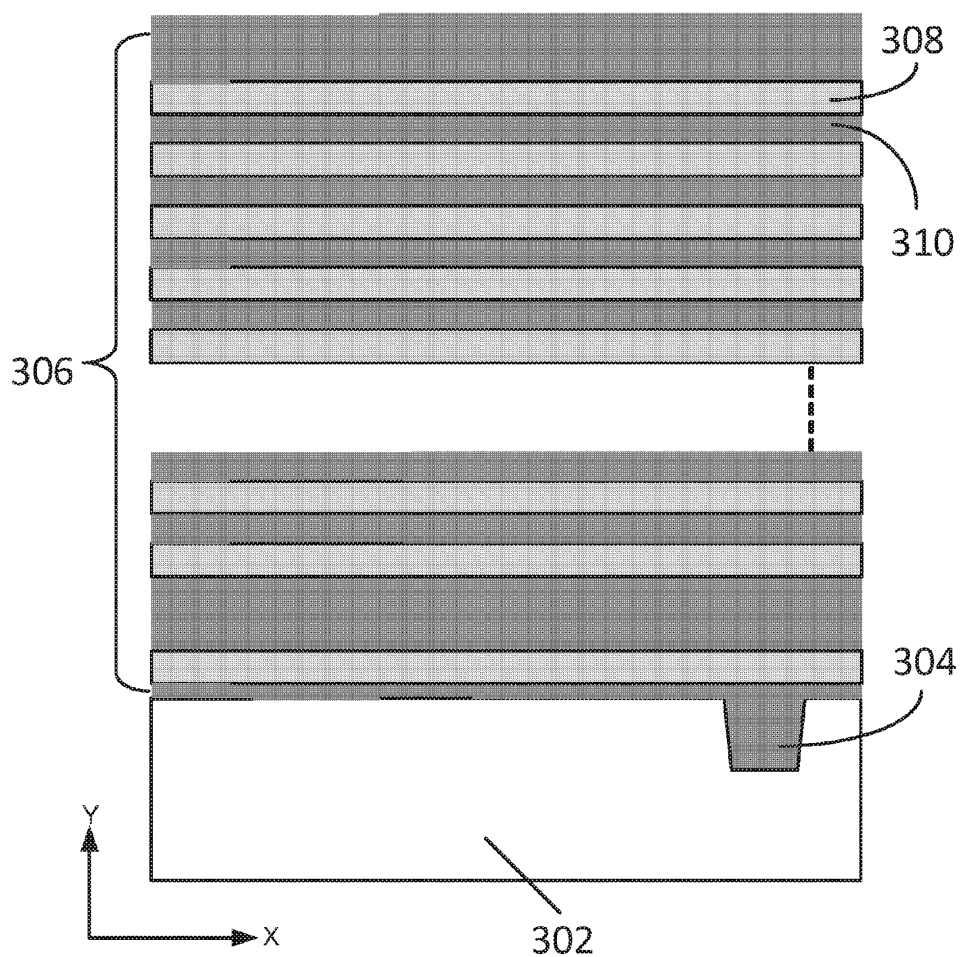


FIG. 3B

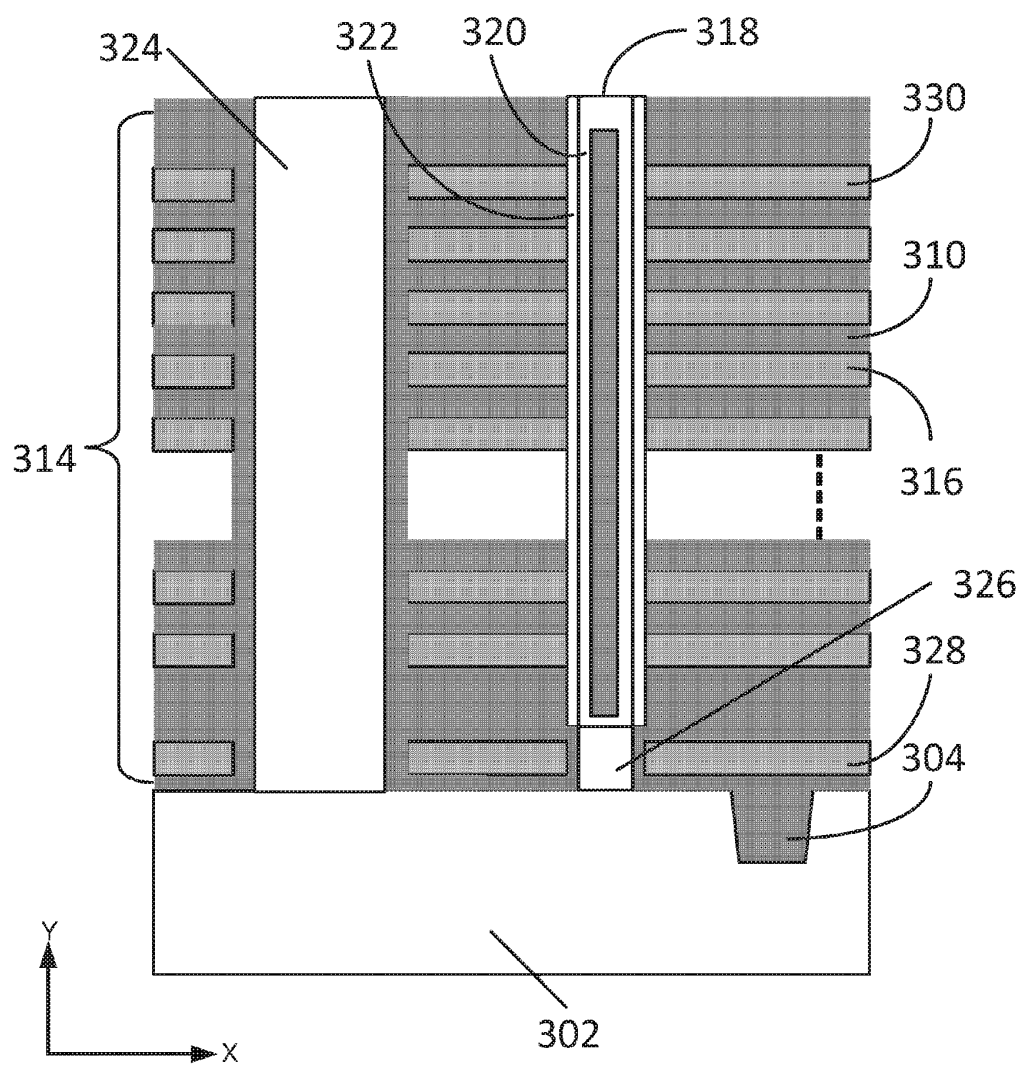


FIG. 3C

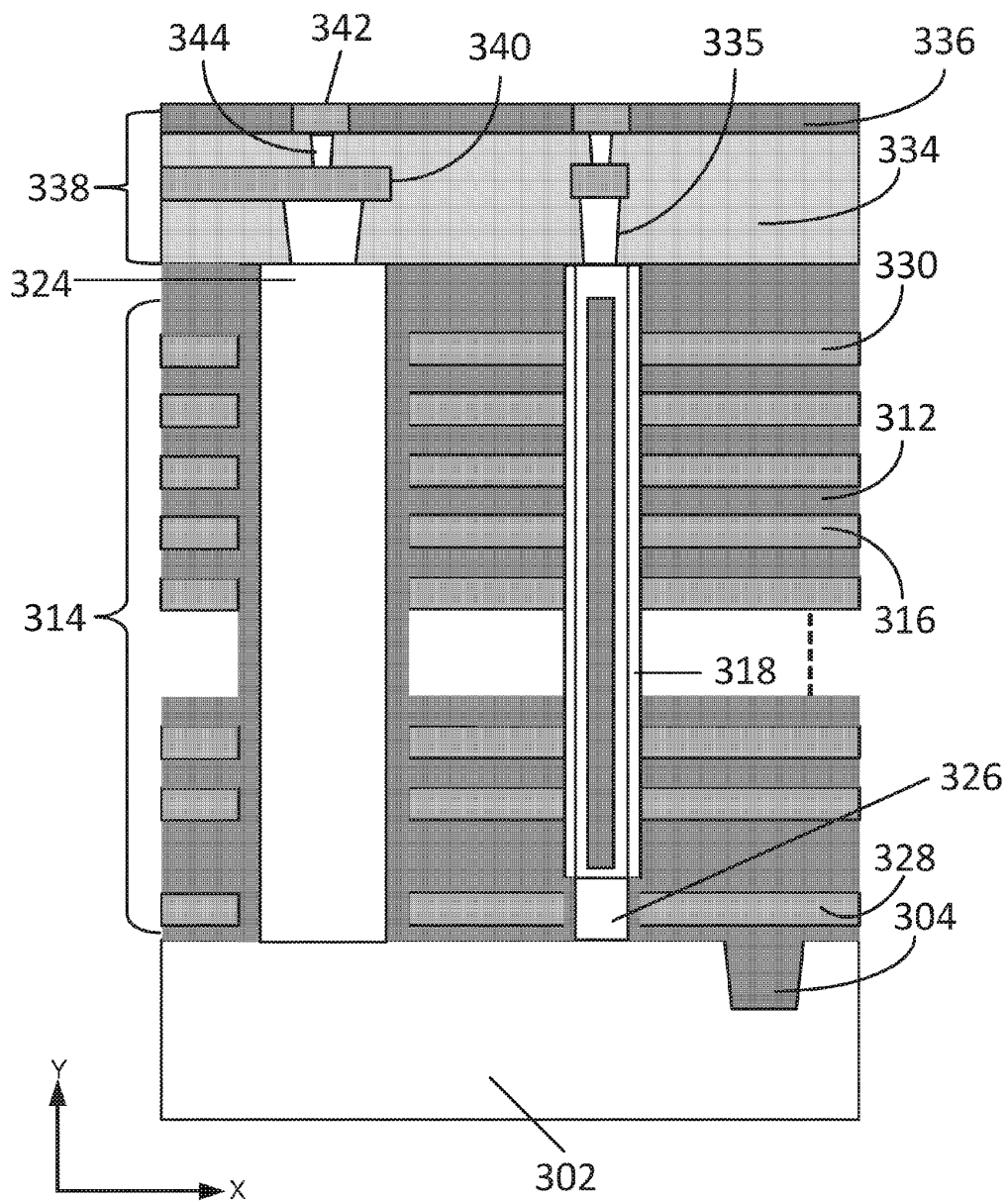


FIG. 3D

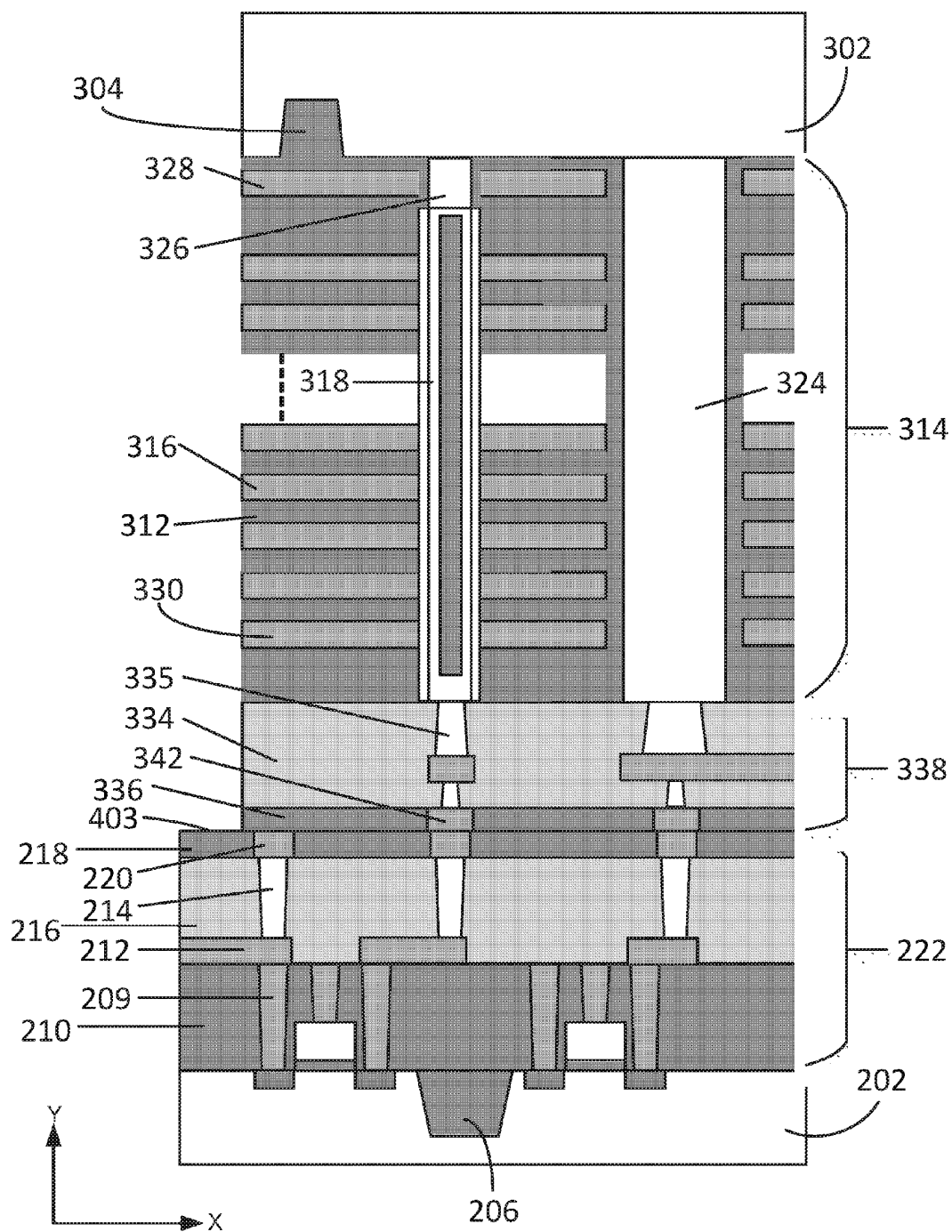


FIG. 4

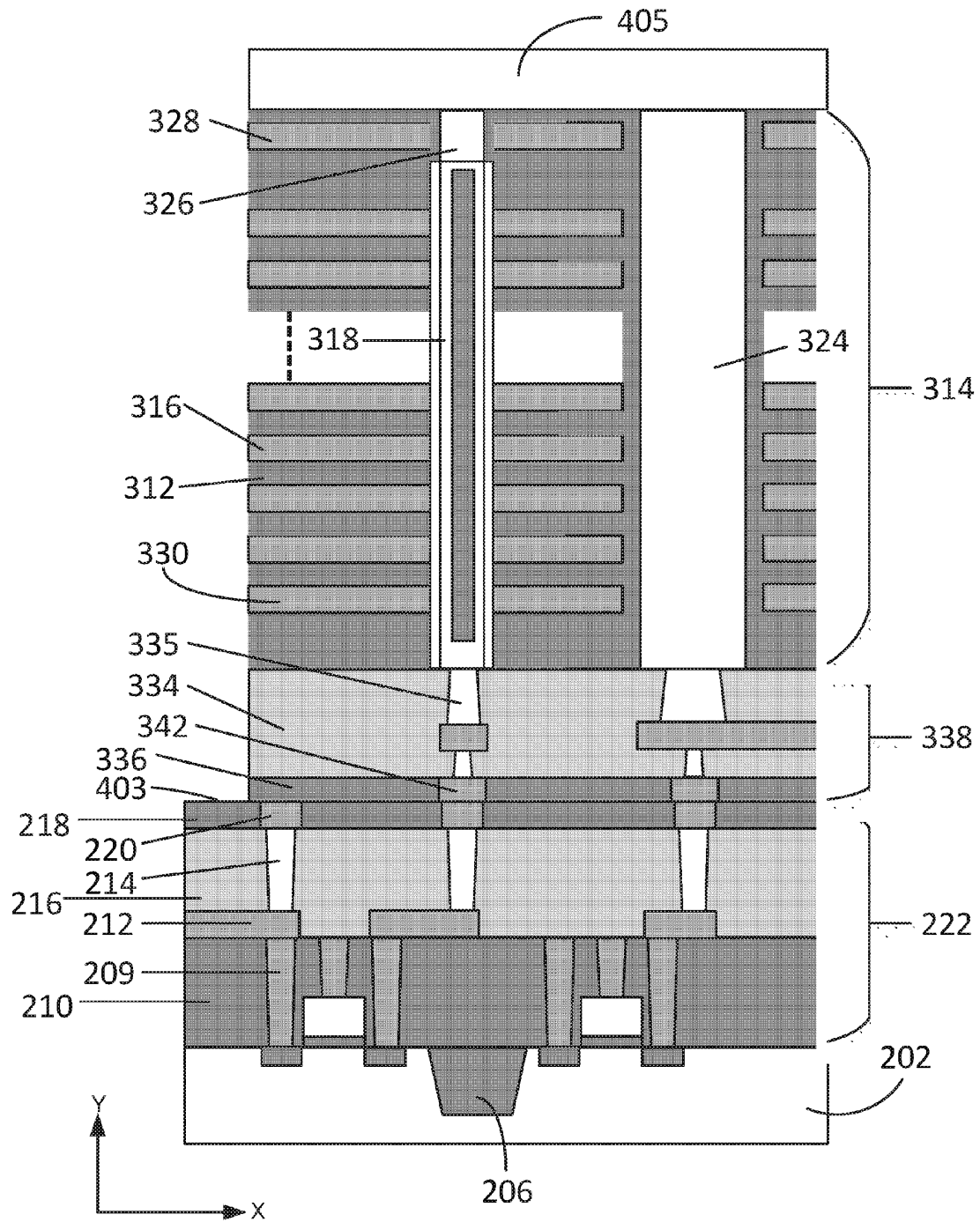


FIG. 5A

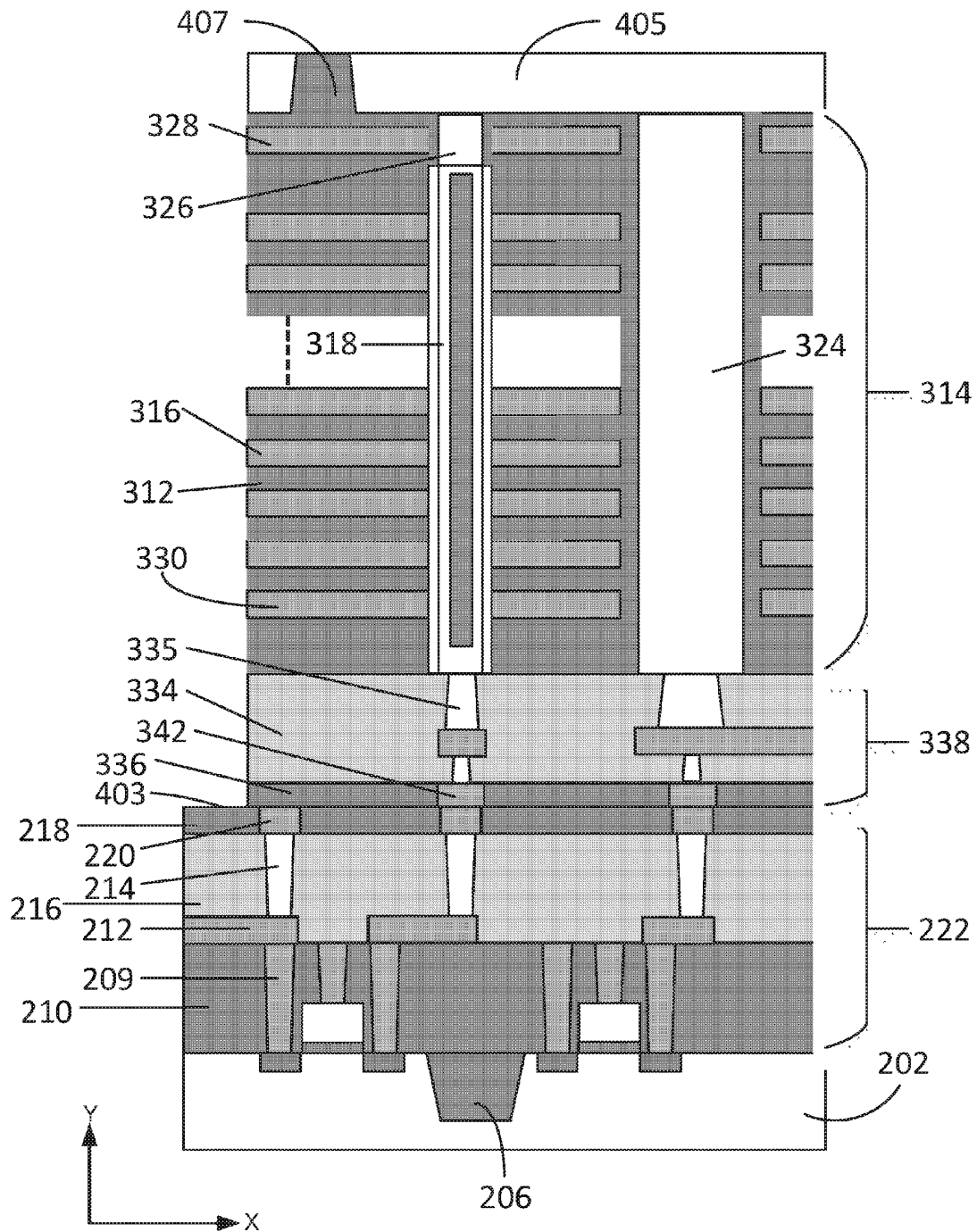


FIG. 5B

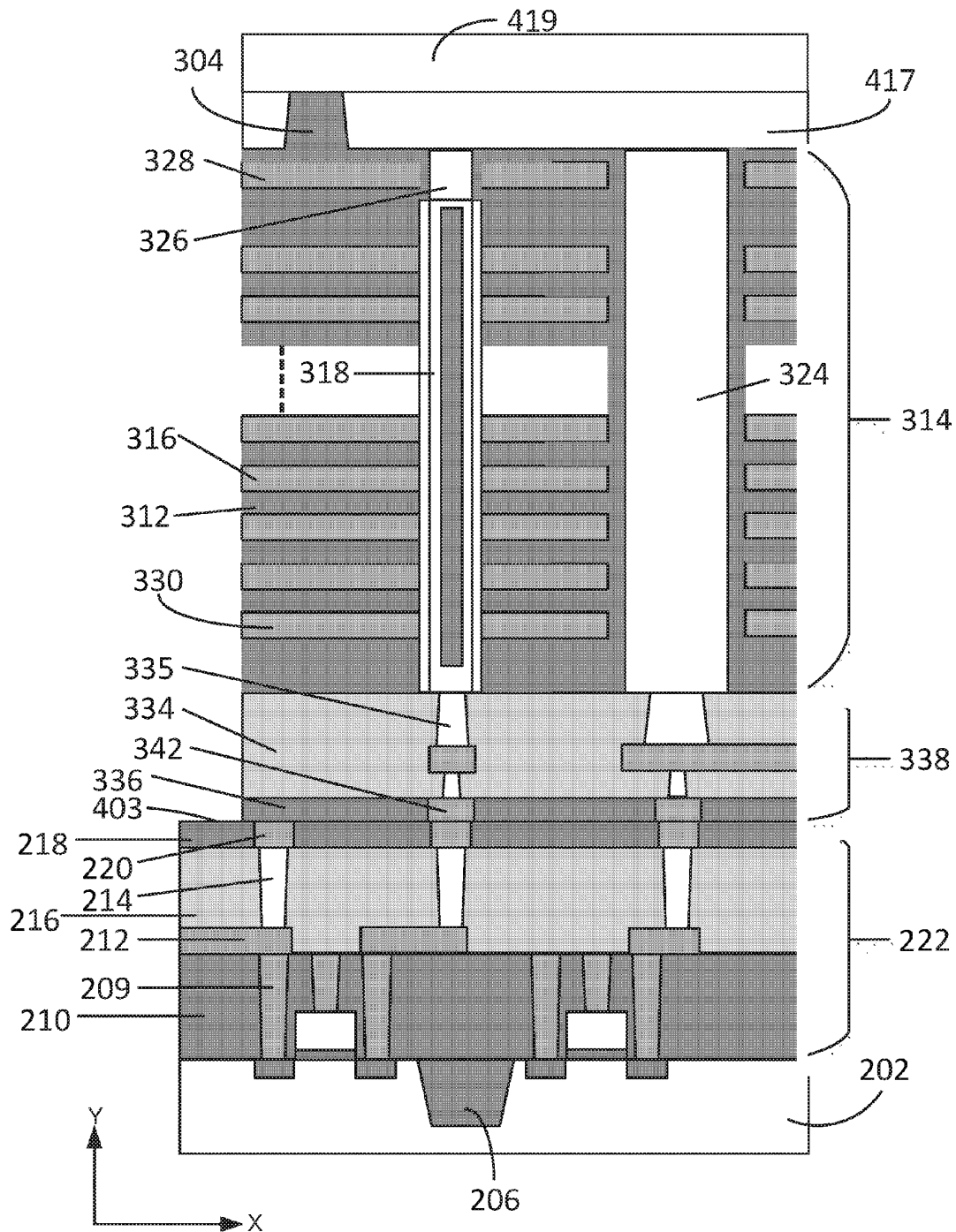


FIG. 6A

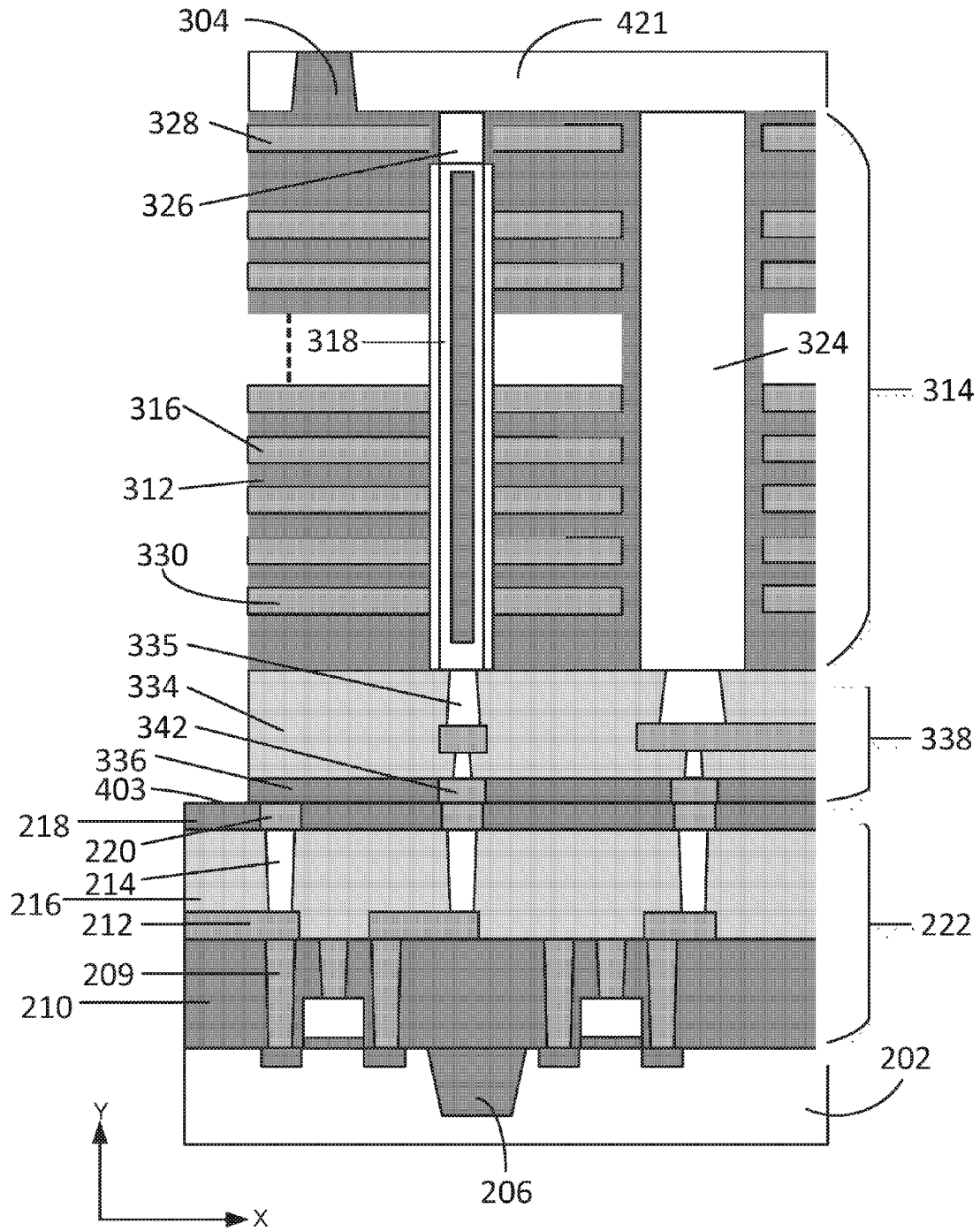


FIG. 6B

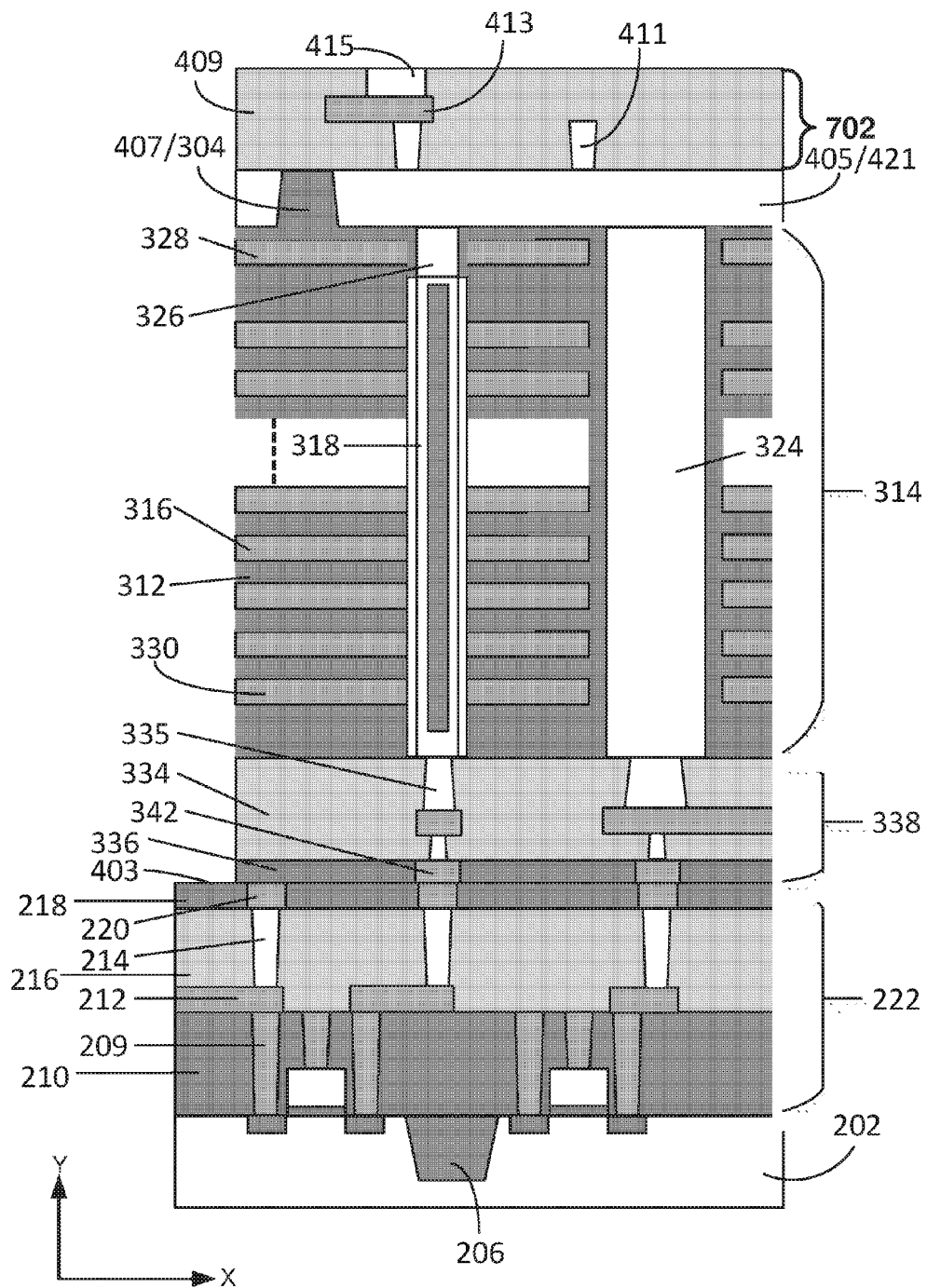
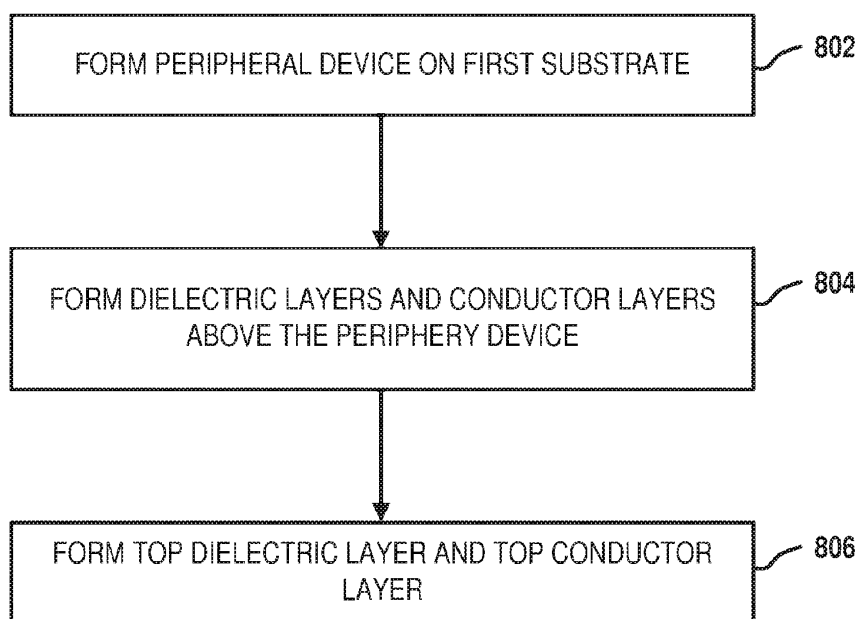
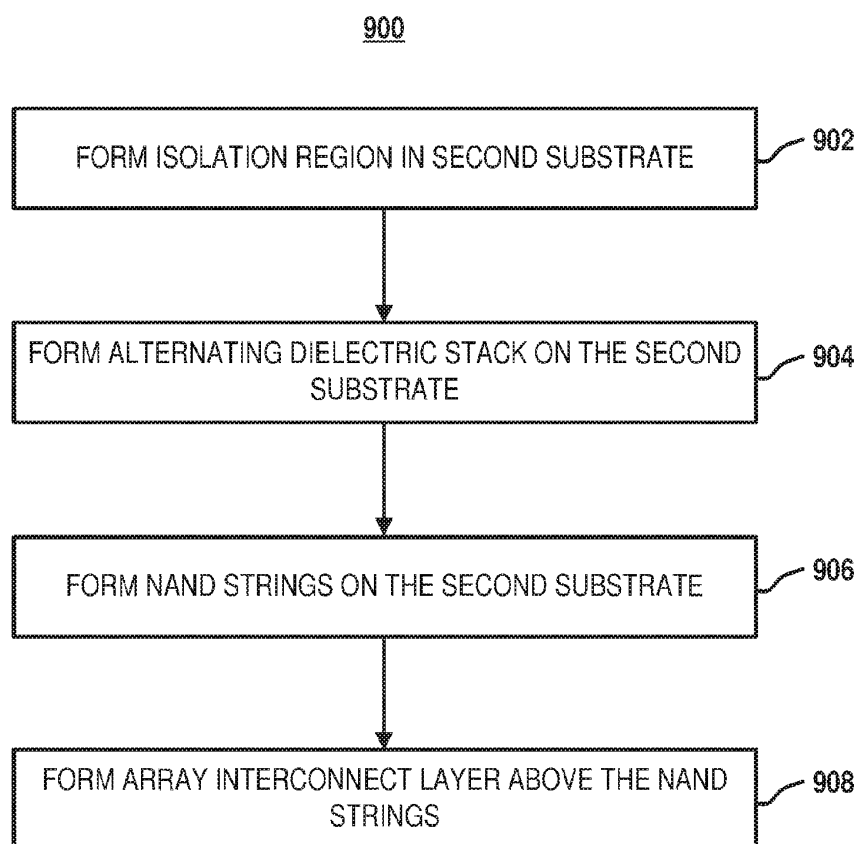
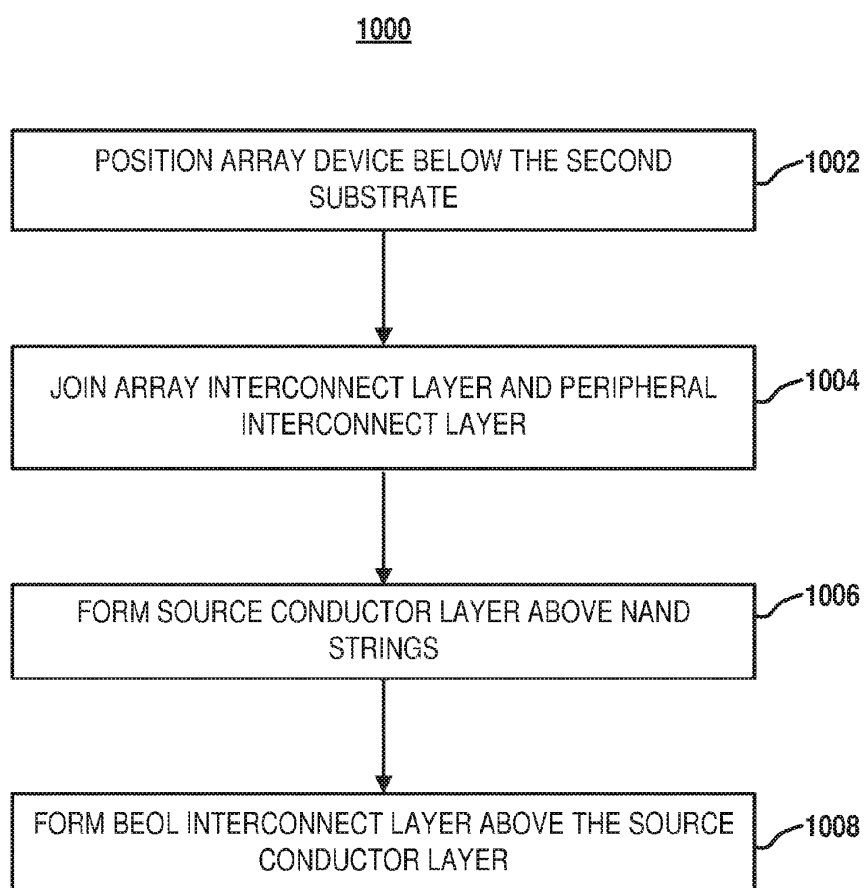
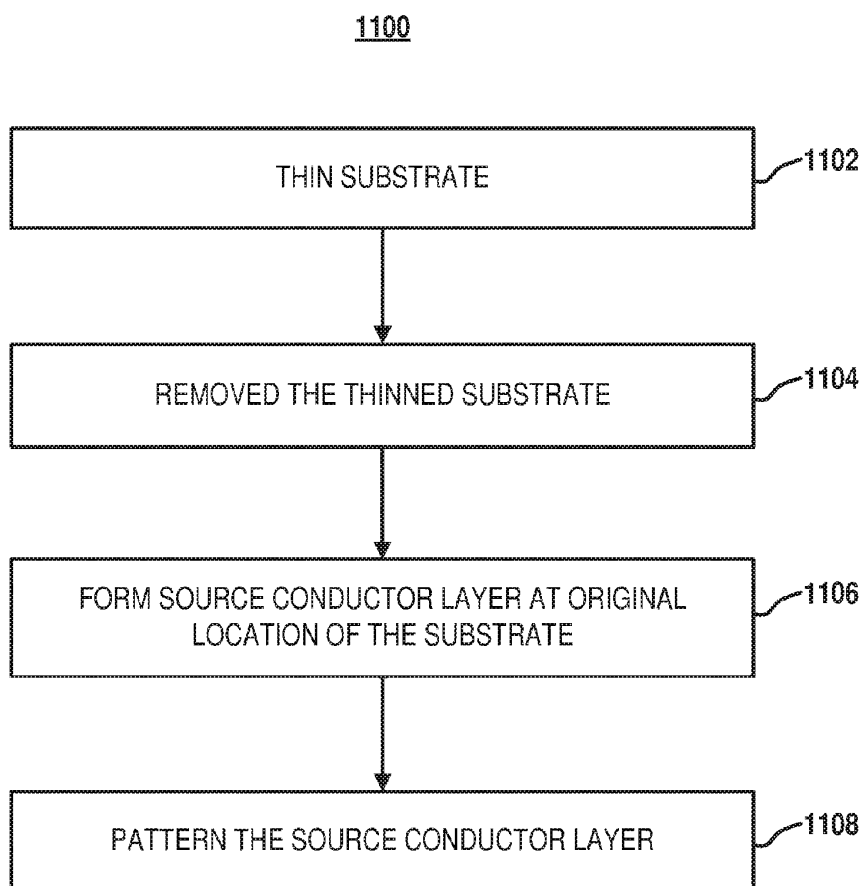


FIG. 7

800**FIG. 8**

**FIG. 9**

**FIG. 10**

**FIG. 11**

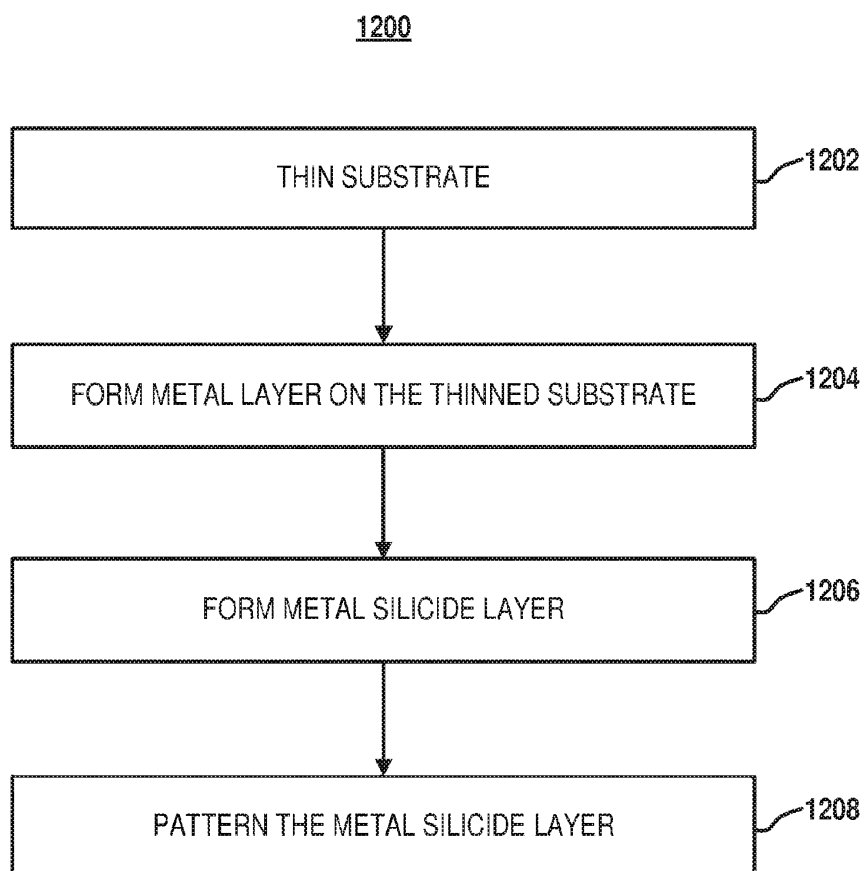


FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2018/077767

A. CLASSIFICATION OF SUBJECT MATTER		
H01L 27/11582(2017.01)i; H01L 27/1157(2017.01)i		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H01L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
CNPAT,EPODOC,WPL,CNKI,IEEE;semiconductor, substrate, chip, silicon, peripher+, logic, surround+, combin+, adjoin+, bond +, joint+, 3D, dimension+, NAND, conductor, dielectric, stack, string		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2016079164 A1 (KABUSHIKI KAISHA TOSHIBA) 17 March 2016 (2016-03-17) description, paragraphs [0020]-[0113], figures 3-10	1-50
A	US 2016204117 A1 (SANISK TECHNOLOGIES INC.) 14 July 2016 (2016-07-14) the whole document	1-50
A	CN 103730470 A (MACRONIX INTERNATIONAL CO., LTD.) 16 April 2014 (2014-04-16) the whole document	1-50
A	CN 102034829 A (SAMSUNG ELECTRONICS CO., LTD.) 27 April 2011 (2011-04-27) the whole document	1-50
A	CN 103681687 A (SAMSUNG ELECTRONICS CO., LTD.) 26 March 2014 (2014-03-26) the whole document	1-50
☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
27 July 2018		29 August 2018
Name and mailing address of the ISA/CN		Authorized officer
STATE INTELLECTUAL PROPERTY OFFICE OF THE P.R.CHINA 6, Xitucheng Rd., Jimeu Bridge, Haidian District, Beijing 100088 China		WU,Yuanyuan
Facsimile No. (86-10)62019451		Telephone No. 86-(10)-53961351

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2018/077767

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2016079164	A1	17 March 2016	US	2017103994	A1	13 April 2017
				JP	2016062901	A	25 April 2016
US	2016204117	A1	14 July 2016	None			
CN	103730470	A	16 April 2014	None			
CN	102034829	A	27 April 2011	DE	102010037434	A1	31 March 2011
				US	2011073866	A1	31 March 2011
				KR	20110034816	A	06 April 2011
				TW	201138070	A	01 November 2011
				JP	2011077521	A	14 April 2011
CN	103681687	A	26 March 2014	US	2017133400	A1	11 May 2017
				JP	2014057067	A	27 March 2014
				US	2014070302	A1	13 March 2014
				US	2015311214	A1	29 October 2015
				KR	20140100333	A	14 August 2014
				KR	20140100332	A	14 August 2014
				KR	20140033983	A	19 March 2014

Form PCT/ISA/210 (patent family annex) (January 2015)

PATENT COOPERATION TREATY

PCT

From the INTERNATIONAL SEARCHING AUTHORITY

To:
100013
10th Floor, Tower C, Beijing Global Trade Center, 36 North Third Ring Road East, Dongcheng District, Beijing, China
NTD UNIVATION INTELLECTUAL PROPERTY AGENCY LTD.

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Date of mailing (day/month/year)
30. Jan. 2019 (30. 01. 2019)

Applicant's or agent's file reference
P2018TC490

FOR FURTHER ACTION
See paragraphs 1 and 4 below

International application No.
PCT/CN2018/085421

International filing date (day/month/year)
03. May. 2018 (03. 05. 2018)

Applicant

Yangtze Memory Technologies Co., Ltd.

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:

The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

How? Directly to the International Bureau of WIPO preferably through ePCT or on paper to, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 - 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ With regard to any protest against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. Reminders

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. These comments will be made available to the public after international publication. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established.

Shortly after the expiration of 18 months from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within 19 months from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase until 30 months from the priority date (in some Offices even later); otherwise, the applicant must, within 20 months from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices. In respect of other designated Offices, the time limit of 30 months (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the PCT Applicant's Guide, National Chapters.

Within 22 months from the priority date, the applicant may request that a supplementary international search be carried out by a different International Searching Authority that offers this service (Rule 45bis.1). The procedure for requesting supplementary international search is described in the PCT Applicant's Guide, International Phase, paragraphs 8.006-8.032.

National Intellectual Property Administration, PRC (ISA/CN)
6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088
Facsimile No. (86-10) 62019451

Authorized officer
ZHOU Zhongtang
Telephone No.: 86-10-53961222

Form PCT/ISA/220 (July 2017)



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PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
100013
10th Floor, Tower C, Beijing Global Trade Center, 36 North Third Ring Road East, Dongcheng District, Beijing, China NTD UNIVATION INTELLECTUAL PROPERTY AGENCY LTD.

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43 *bis* 1)

Date of mailing(<i>day/month/year</i>)	
30 Jan. 2019 (30. 01. 2019)	
Applicant's or agent's file reference	
P2018TC490	
FOR FURTHER ACTION	
See paragraph 2 below	
International application No.	International filing date(<i>day/month/year</i>)
PCT/CN2018/085421	03. May. 2018 (03. 05. 2018)
Priority date (<i>day/month/year</i>)	
International Patent Classification (IPC) or both national classification and IPC	
H01L 27/11565 (2017. 01) i	
Applicant	
Yangtze Memory Technologies Co., Ltd.	
1. This opinion contains indications relating to the following items: ☒ Box No. I Basis of the opinion ☐ Box No. II Priority ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability ☐ Box No. IV Lack of unity of invention ☒ Box No. V Reasoned statement under Rule 43<i>bis</i> 1(a)(i) with regard to novelty, inventive step or industrial applicability, citations and explanations supporting such statement ☐ Box No. VI Certain documents cited ☐ Box No. VII Certain defects in the international application ☐ Box No. VIII Certain observations on the international application 2. FURTHER ACTION If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1<i>bis</i>(b) that written opinions of this International Searching Authority will not be so considered. If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later. For further options, see Form PCT/ISA/220. 3. For further details, see notes to Form PCT/ISA/220.	
Name and mailing address of the ISA/CN	Date of completion of this opinion
National Intellectual Property Administration, PRC	24. Jan. 2019 (24. 01. 2019)
6, Xitucheng Rd., Jimeu Bridge, Haidian District, Beijing 100088, China	Authorized officer
Facsimile No. (86---10) 62019451	ZHOU, Zhongtang
	Telephone No. 86-(10) 62019451

Form PCT/ISA/237 (cover sheet) (January 2015)



WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CN2018/085421

0036

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:
☒ the international application in the language in which it was filed.
☐ a translation of the international application into..... which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91(Rule 43bis.1(b))
3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:
 - a. ☐ forming part of the international application as filed:
☐ in the form of an Annex C/ST.25 text file.
☐ on paper or in the form of an image file.
 - b. ☐ furnished together with the international application under PCT Rule 13ter.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.
 - c. ☐ furnished subsequent to the international filing date for the purposes of international search only:
☐ in the form of an Annex C/ST.25 text file (Rule 13ter.1(a))
☐ on paper or in the form of an image file (Rule 13ter.1(b) and Administrative Instructions, Section 713).
4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Form PCT/ISA/237 (cover sheet) (January 2015)



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WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CN2018/086421

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement:

Novelty (N)	Claims <u>2, 11-27, 32</u>	YES
	Claims <u>1, 3-10, 28-31</u>	NO
Inventive step (IS)	Claims <u>12-27</u>	YES
	Claims <u>1, 11, 28, 32</u>	NO
Industrial applicability (IA)	Claims <u>1-32</u>	YES
	Claims <u>None</u>	NO

2. Citations and explanations

Document:

DI: CN106910746 A 30 June 2017 (30.06.2017).

1. Novelty / Inventive step

DI discloses a 3D memory device and a method for forming the device (description, paragraphs [0074]-[0085], [0096]-[0137], Figures. 1-2, 5-7). The device, comprising: a semiconductor substrate 400 with an isolation structure 402; an alternating conductor 1012/dielectric 1011 layer stack 101 disposed on the semiconductor substrate 400; a dielectric structure (160, 102) on the isolation region 402 of the substrate 400 and extending vertically through the stack 101, wherein the stack 101 abuts a sidewall surface of the dielectric structure (160, 102) which is formed of a dielectric material; one or more TACs 162 extending vertically through the dielectric structure (160, 102) and the isolation region 402; and one or more channel structures 150 extending vertically through the stack 101.

The method, comprising: forming the isolation structure 402 on the substrate 400 (S01); disposing an alternating dielectric layer stack on the substrate 400, the alternating dielectric layer stack comprising pairs of a first dielectric layer and a second dielectric layer different from the first dielectric layer (S02); forming a channel structure 170 extending vertically in the alternating dielectric layer stack (S04).

Claims 1, 28 lack novelty and an inventive step in the sense of PCT 33(2) and PCT 33(3).

Claims 12, 21 differ from DI in the features of forming TAC respectively. The problems solved by the above features are how to improve integration of the 3D memory. The above features are neither common method nor disclosed by the prior art. Claims 12-27 are novel and involve an inventive step in the sense of PCT 33(2) and PCT 33(3).

The additional features of claims 3-10, 29-31 are disclosed by DI (description,

Form PCT/ISA/237 (cover sheet) (January 2015)



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paragraphs [0074] - [0085], Figures 5-6). Partial of the additional features of claims 2, 32 are disclosed by D1 (description, paragraphs [0074] - [0085], Figures 5-6), rest of them are common practice for a person skilled in the art. The additional features of claim 11 are common practice for a person skilled in the art.

Claims 3, 5-10, 29-31 lack novelty and an inventive step in the sense of PCT 33(2) and PCT 33(3). Claims 2, 11, 32 are novel in the sense of PCT 33(2) but do not involve an inventive step in the sense of PCT 33(3).

Claim 4 lacks novelty and an inventive step in the sense of PCT 33(2) and PCT 33(3) when citing claim 1 lacks novelty and an inventive step in the sense of PCT 33(2) and PCT 33(3); Claim 4 is novel in the sense of PCT 33(2) but does not involve an inventive step in the sense of PCT 33(3) when citing claim 5 is novel in the sense of PCT 33(2) but does not involve an inventive step in the sense of PCT 33(3).

III. Industrial applicability

Claims 1-32 are industrial applicable in the sense of PCT 33(4).



PATENT COOPERATION TREATY
PCT

INTERNATIONAL SEARCH REPORT
(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference P2018TC490	FOR FURTHER ACTION see Form PCT/ISA/220 as well as, where applicable, item 5 below.	
International application No. PCT/CN2018/085421	International filing date (day/month/year) 03 May 2018 (03. 05. 2018)	(Earliest) Priority date (day/month/year)
Applicant Yangtze Memory Technologies Co., Ltd.		
This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau. This international search report consists of a total of <u>4</u> sheets. ☐ It is also accompanied by a copy of each prior art document cited in this report.		
1. Basis of the report a. With regard to the language , the international search was carried out on the basis of: ☒ the international application in the language in which it was filed ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)) b. ☐ This international search report has been established taking into account the rectification of an obvious mistake authorized by or notified to this Authority under Rule 91 (Rule 43.6bis(a)). c. ☐ With regard to any nucleotide and/or amino acid sequence disclosed in the international application, see Box No. I. 2. ☐ Certain claims were found unsearchable (see Box No. II) 3. ☐ Unity of invention is lacking (see Box No. III) 4. With regard to the title , ☒ the text is approved as submitted by the applicant. ☐ the text has been established by this Authority to read as follows: 5. With regard to the abstract , ☒ the text is approved as submitted by the applicant. ☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority. 6. With regard to the drawings , a. The figure of the drawings to be published with the abstract is Figure No. 13 ☒ as suggested by the applicant ☐ as selected by this Authority, because the applicant failed to suggest a figure ☐ as selected by this Authority, because this figure better characterizes the invention b. ☐ none of the figures is to be published with the abstract		

Form PCT/ISA/210(first sheet) January 2015)



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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2018/085421

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/11565(2017.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, IEEE, WPI: Yangtze Memory, CHANGJIANG MEMORY, TAC, through, array, contact+, connect+, three, dimension, 3D, memory, channel, slit, hole, trench, open+, window+, fill+, form+, deposit+, insulat+, isolate+, dielectric, silicon, oxide, nitride, step, staircase, conduct+, metal, plug, etch+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 106910746A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 30 Jun.2017(30.06.2017) description, paragraphs [0074]-[0085], [0096]-[0137], Figures 1-2, 5-7	1-11, 28-32
X	CN 106920794A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 04 Jul.2017(04.07.2017) description, paragraphs [0077]-[0112], Figures 5-7	1-11, 28-32
A	US 8247895B2 (IBM CORPORATION) 21 Aug.2012(21.08.2012) the whole document	1-32
A	CN 105826323A (MACRONIX INT CO., LTD.) 03 Aug.2016(03.08.2016) the whole document	1-32

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

International application No.
PCT/CN2018/095421

* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance, the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family
Date of the actual completion of the international search	Date of mailing of the international search report
03 Jan. 2019(03. 01. 2019)	30 Jan. 2019(30. 01. 2019)
Name and mailing address of the ISA/CN National Intellectual Property Administration, PRC 6, Xitucheng Rd., Jimen Bridge, Haifan District, Beijing 100088, China Facsimile No.(86-10)62019451	Authorized officer ZHOU, Zhongtang
	Telephone No.: 86-(10) 53961222



INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2018/085421

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN106910746A	30.06.2017	TW201834221A	16.09.2018
		WO2018161859A1	13.09.2018
		CN106910746B	19.06.2018
CN106920794A	04.07.2017	CN106920794B	30.11.2018
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Form PCT/ISA/210(patent family annex) (January 2015)



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Electronic Acknowledgement Receipt	
EFS ID:	36564326
Application Number:	16047182
International Application Number:	
Confirmation Number:	7800
Title of Invention:	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES
First Named Inventor/Applicant Name:	Qian TAO
Customer Number:	26111
Filer:	Donald J. Featherstone/Laney Flanagan
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0190001
Receipt Date:	12-JUL-2019
Filing Date:	27-JUL-2018
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Application Type:	Utility under 35 USC 111(a)

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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	019_IDS_CoverLetter.pdf	20934	no	1
			89410e050024ded849a1fdb35f2c6c0ac8f7d8ab		
Warnings:					

Information:					
2	Transmittal Letter	019_IDS_Pleading.pdf	30231	no	7
			067e6c84999937bd5355f4477ab3a618f030dbf4		
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	019_SB08.pdf	48091	no	3
			01dd70b96dc0188fa3265253697764a1c891b13d		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
4	Foreign Reference	FP1.pdf	843060	no	55
			6a4fc9e4f008afbfbba4d902a2ce096050b0986e7		
Warnings:					
Information:					
5	Foreign Reference	FP2.pdf	663603	no	54
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Information:					
6	Foreign Reference	FP3.pdf	764846	no	48
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Warnings:					
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7	Foreign Reference	FP4.pdf	2917452	no	73
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Warnings:					
Information:					
8	Foreign Reference	FP5.pdf	560617	no	20
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Warnings:					
Information:					

9	Foreign Reference	FP6.pdf	416773	no	20
			5519136a4f33d11782702c468583443c3c1681a9		
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Information:					
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Warnings:					
Information:					
11	Foreign Reference	FP8.pdf	913874	no	29
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12	Foreign Reference	FP9.pdf	739165	no	62
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13	Non Patent Literature	NPL1.pdf	289598	no	9
			29ed65cade20c25d543e49be9a9fac8831c2cbd7		
Warnings:					
Information:					
Total Files Size (in bytes):			8930030		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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July 12, 2019

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 7800
Art Unit 2812
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Application No. 16/047,182; Filing Date: July 27, 2018
For: **THROUGH ARRAY CONTACT (TAC) FOR THREE-
DIMENSIONAL MEMORY DEVICES**
Inventors: TAO *et al.*
Our Ref: 4123.0190001

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Information Disclosure Statement;
2. Form PTO/SB/08a (2 sheets) listing 15 documents (**US1-US8** and **FP1-FP9**);
3. Form PTO/SB/08b (1 sheet) listing 1 document (**NPL1**); and
4. Copies of cited documents (**FP1-FP9** and **NPL1**).

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/Y-G/lef
Enclosures

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: TAO *et al.*

Confirmation No.: 7800

Applicant: Yangtze Memory Technologies
Co., Ltd.

Art Unit: 2812

Application No.: 16/047,182

Examiner: CHOI, CALVIN Y

Filing Date: July 27, 2018

Atty. Docket: 4123.0190001

Title: **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY
DEVICES**

Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on accompanying IDS Forms PTO/SB/08a and PTO/SB/08b equivalent are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

- ☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement: (i) was first cited in any communication from a patent office in a counterpart¹ foreign or international application or from the Office; and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of this information disclosure statement; OR (ii) is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of the information disclosure statement.
- ☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action

¹ The term counterpart foreign patent application means that a claim for priority has been made in either the U.S. application or a foreign application based on the other, or that the disclosures of the U.S. and foreign patent applications are substantively identical (e.g., an application filed in the European Patent Office claiming the same U.K. priority as claimed in the U.S. application).

after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.

- ☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.
- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.
37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement.
37 C.F.R. § 1.97(e)(2).
- ☐ c. Attached is our PTO-2038 Credit Card Payment Form in the amount of \$240.00 in payment of the fee under 37 C.F.R. § 1.17(p).
- ☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or

Atty. Dkt. No. 4123.0190001

Notice of Allowance, but on or before payment of the Issue Fee. Enclosed find our PTO-2038 Credit Card Payment Form in the amount of \$240.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☒ 5. The patent family for one or more foreign language documents submitted herewith includes a United States patent, and other patent, in the English language. Copies of both the particular foreign patent(s) or published foreign patent applications cited in the foreign patent office communication, and that are not already of record in this application, are enclosed. Copies of the related United States or other English language patent or published application from the family list, if not already of record, are listed on the accompanying SB/08A form. For the purposes of a statement under 37 CFR 1.97(e)(1), the United States or

Atty. Dkt. No. 4123.0190001

other English language patent or published application are to be construed as being cited by the foreign patent office. MPEP 609.04(b)(V).

- ☐ 6. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. MPEP 609.04(a)(III).

- ☒ 7. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).

Document **US4** (2019/0057974 A1) is submitted herewith as the English-language counterpart of document **FP6** (CN 106910746 A).

Document **US6** (9,530,789 B2) is submitted herewith as the English-language counterpart of document **FP4** (CN 105047668 A).

Document **US7** (9,595,531 B2) is submitted herewith as the English-language counterpart of document **FP2** (TW 201606388 A).

Document **US8** (9,595,667 B2) is submitted herewith as the English-language counterpart of document **FP1** (TW 201419449 A).

Document **FP9** (WO 2019/104896 A1) is submitted herewith as the English-language counterpart of document **FP8** (CN 107887395 A).

- ☒ 8. Copies of documents **FP1-FP9** and **NPL1** are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of the U.S. patent application publications and patents cited as documents **US1-US8** on the attached IDS Forms are submitted.

Atty. Dkt. No. 4123.0190001

- ☐ 9. Copies of the _____ documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. _____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).
- ☐ 10. It is expected that the examiner will review the prosecution and cited art in the parent Application No(s). _____, in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.
- ☐ 11. In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from the co-pending U.S. Patent Application No. _____, filed _____, as documents _____ to _____. The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

Atty. Dkt. No. 4123.0190001

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
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Date: July 12, 2019

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Atty. Dkt. No. 4123.0190001



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/047,182	07/27/2018	Qian TAO	4123.0190001	7800
26111	7590	08/22/2019		
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER CHOI, CALVIN Y	
			ART UNIT	PAPER NUMBER
			2812	
			NOTIFICATION DATE	DELIVERY MODE
			08/22/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

e-office@sternekessler.com

DETAILED ACTION

1. This Office Action is in response to the application filed on 27 July 2018.

Notice of Pre-AIA or AIA Status

2. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Rejections - 35 USC § 103

3. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.
4. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

5. **Claim(s) 1, 3-16, and 18-20 is/are rejected under 35 U.S.C. 103 as being unpatentable over Nishikawa et al. (US 9,620,512 B1; hereinafter *Nishikawa*) in view of Lee et al. (US 2016/0056188 A1; hereinafter *Lee*).**

6. **In regards to claim 1, *Nishikawa* teaches a three-dimensional (3D) memory device, comprising:**
- a semiconductor substrate (9/10) (col. 6/lns. 7-8);
 - an alternating layer stack (32/46) disposed on the semiconductor substrate (col. 7/lns. 11-55; col. 23/lns. 55-62);
 - a dielectric structure (64) (e.g. figs. 4-5) on an isolation region (120) (col. 6/lns. 7-8) of the substrate and extending vertically through the alternating layer stack (figs. 4-5), wherein the

alternating layer stack abuts a sidewall surface of the dielectric structure (e.g. at the left side of (64)) and the dielectric structure is formed of a dielectric material; and

- one or more channel structures (11) extending vertically through the alternating layer stack (col. 9/lns. 47-49).

7. *Nishikawa* appears to be silent as to, but does not preclude, the elements of one or more through array contacts (TACs) extending vertically through the dielectric structure and the isolation region. *Lee* teaches the elements of: one or more through array contacts (TACs) (83) extending vertically through the dielectric structure and the isolation region [0067]. It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the device taught by *Nishikawa* with the aforementioned elements taught by *Lee* to have an image sensor having a higher resolution (*Lee* [0005]).

8. **In regards to claim 3**, the combination of *Nishikawa* and *Lee* teaches the device discussed above in addressing claim 1. *Lee* further teaches the elements wherein the dielectric structure (83B) abuts a sidewall surface of the TACs (83) [0067]. It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the device taught by *Nishikawa* with the aforementioned elements taught by *Lee* to have an image sensor having a higher resolution (*Lee* [0005]).

9. **In regards to claim 4**, the combination of *Nishikawa* and *Lee* teaches the device discussed above in addressing claim 1. *Nishikawa* further teaches the elements wherein the 3D memory device is a NAND 3D memory device (col. 1/lns. 64-66).

10. **In regards to claim 5**, the combination of *Nishikawa* and *Lee* teaches the device discussed above in addressing claim 1. *Nishikawa* further teaches the elements wherein the alternating layer stack comprises alternating pairs of a dielectric (32) (col. 7/lns. 11-55) and a conductor layer (46) (col. 23/lns. 55-62).

11. In regards to claim 6, the combination of *Nishikawa* and *Lee* teaches the device discussed above in addressing claim 1. *Nishikawa* further teaches the elements wherein the dielectric material is silicon oxide (col. 17/lns. 30-39).

12. In regards to claim 7, the combination of *Nishikawa* and *Lee* teaches the device discussed above in addressing claim 1. *Nishikawa* further teaches the elements wherein the dielectric structure comprises an oxide (col. 17/lns. 30-39).

13. In regards to claim 8, the combination of *Nishikawa* and *Lee* teaches the device discussed above in addressing claim 1. *Lee* further teaches the elements wherein the dielectric structure defines a through array contact region (83) within the 3D memory device [0067]. It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the device taught by *Nishikawa* with the aforementioned elements taught by *Lee* to have an image sensor having a higher resolution (*Lee* [0005]).

14. In regards to claim 9, the combination of *Nishikawa* and *Lee* teaches the device discussed above in addressing claim 1. *Lee* further teaches the elements wherein the dielectric structure has a footprint equal to or smaller than the isolation region (fig. 7B: e.g. (53) is thinner than (50) and is part of (53)). It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the device taught by *Nishikawa* with the aforementioned elements taught by *Lee* to have an image sensor having a higher resolution (*Lee* [0005]).

15. In regards to claim 10, *Nishikawa* teaches a method for forming a 3D memory device, the method comprising:

- forming an isolation structure (120) (col. 6/lns. 7-8) on a substrate (9/10) (col. 6/lns. 7-8);

- disposing an alternating dielectric layer stack (32/42) on the substrate, the alternating dielectric layer stack comprising pairs of a first dielectric layer (32) and a second dielectric layer (42) different from the first dielectric layer (col. 7/lns. 11-55);
- forming a channel structure (11) extending (e.g. partially) vertically in the alternating dielectric layer stack (col. 9/lns. 47-49); and
- forming an opening (179) in the alternating dielectric layer stack, wherein the opening exposes the isolation structure (col. 19/lns. 13-22).

16. *Nishikawa* appears to be silent as to, but does not preclude, the steps of filling the opening with a dielectric layer to form a dielectric structure as a through array contact (TAC) region of the 3D memory device; removing portions of the dielectric structure and the isolation structure until the substrate is exposed to form a TAC opening that vertically extends through the dielectric structure and the isolation structure; and filling the TAC opening with a conductor to form a TAC structure in the TAC region, wherein the TAC structure is in contact with the substrate. *Lee* teaches the steps of:

- filling the opening (85T/50T) [0084] with a dielectric layer (851/51) [0085-0086] to form a dielectric structure as a through array contact (TAC) region of the 3D memory device (figs. 8);
- removing portions (81H/52T) [0086] of the dielectric structure and the isolation structure until the substrate (35) [0033] is exposed to form a TAC opening that vertically extends through the dielectric structure and the isolation structure (fig. 8D); and
- filling the TAC opening with a conductor to form a TAC structure (83) in the TAC region, wherein the TAC structure is in contact with the substrate [0067].

17. It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the method taught by *Nishikawa* with the aforementioned steps taught by *Lee* to have an image sensor having a higher resolution (*Lee* [0005]).

18. In regards to claim 11, the combination of *Nishikawa* and *Lee* teaches the method discussed above in addressing claim 10. *Nishikawa* further teaches the steps wherein before forming the TAC opening the method further comprises: forming slit openings (479) (col. 19/lns. 13-22) extending vertically in the alternating dielectric layer stack, wherein the slit openings expose a doped region (61) of the substrate (col. 19/lns. 46-53); replacing the second dielectric layer (42) (col. 7/lns. 11-55) through the one or more slit openings with a conductor layer (46) to convert the alternating dielectric layer stack to an alternating dielectric/conductor layer stack (col. 23/lns. 55-62); and filling the one or more slit openings with a conductor (46L) to form one or more slit structures extending vertically in the alternating dielectric/conductor layer stack (col. 23/lns. 55-62).

19. In regards to claim 12, the combination of *Nishikawa* and *Lee* teaches the method discussed above in addressing claim 10. *Nishikawa* further teaches the steps wherein before forming the channel structure performing a trim-etch process to form a staircase structure in the alternating dielectric layer stack (e.g. fig. 4).

20. In regards to claim 13, the combination of *Nishikawa* and *Lee* teaches the method discussed above in addressing claim 10. *Lee* further teaches the steps wherein filling the opening with the dielectric layer (51) comprises depositing the dielectric layer with a chemical vapor deposition, a plasma-enhanced chemical vapor deposition, or a physical vapor deposition process ([0059]; fig. 8). It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the method taught by *Nishikawa* with the aforementioned steps taught by *Lee* to have an image sensor having a higher resolution (*Lee* [0005]).

21. In regards to claim 14, the combination of *Nishikawa* and *Lee* teaches the method discussed above in addressing claim 10. *Lee* further teaches the steps wherein filling the opening with the dielectric layer (51) comprises forming an oxide ([0039]; fig. 8). It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the method taught

by *Nishikawa* with the aforementioned steps taught by *Lee* to have an image sensor having a higher resolution (*Lee* [0005]).

22. In regards to claim 15, the combination of *Nishikawa* and *Lee* teaches the method discussed above in addressing claim 10. *Nishikawa* further teaches the steps wherein the first dielectric layer (32) (col. 7/lns. 17-29) comprises an oxide and the second dielectric layer (42) (col. 7/lns. 52-55) comprises a nitride.

23. In regards to claim 16, *Nishikawa* teaches a three-dimensional (3D) memory device, comprising:

- a substrate (9/10) (col. 6/lns. 7-8) with an isolation structure (120) (col. 6/lns. 7-8);
- an alternating conductor/dielectric layer (46/32) stack disposed on the substrate (col. 23/lns. 55-62; col. 7/lns. 11-55);
- a dielectric structure (64) (figs. 4-5) on the isolation structure (120) (col. 6/lns. 7-8) and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material (figs. 4-5: e.g. at the left side of (64)); and
- channel structures (11) extending (e.g. partially) vertically through the alternating conductor/dielectric layer stack (col. 9/lns. 47-49).

24. *Nishikawa* appears to be silent as to, but does not preclude, the elements of through array contacts (TAC) extending vertically through the dielectric and the isolation structures. *Lee* teaches the elements of through array contacts (TAC) (83) extending vertically through the dielectric and the isolation structures [0067]. It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the device taught by *Nishikawa* with the aforementioned elements taught by *Lee* to have an image sensor having a higher resolution (*Lee* [0005]).

25. In regards to claim 18, the combination of *Nishikawa* and *Lee* teaches the device discussed above in addressing claim 16. *Lee* further teaches the elements wherein the dielectric structure (83B) abuts a sidewall surface of the TACs (83) [0067]. It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the device taught by *Nishikawa* with the aforementioned elements taught by *Lee* to have an image sensor having a higher resolution (*Lee* [0005]).

26. In regards to claim 19, the combination of *Nishikawa* and *Lee* teaches the device discussed above in addressing claim 16. *Lee* further teaches the elements wherein the dielectric structure comprises a through array contact region (83) of the 3D memory device [0067]. It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the device taught by *Nishikawa* with the aforementioned elements taught by *Lee* to have an image sensor having a higher resolution (*Lee* [0005]).

27. In regards to claim 20, the combination of *Nishikawa* and *Lee* teaches the device discussed above in addressing claim 16. *Nishikawa* further teaches the elements further comprising: an etch stop plug (62) interposed between each local contact (63) and each channel structure (602/11); and an epitaxial layer disposed between each channel structure and the substrate (figs. 2).

Allowable Subject Matter

28. Claims 2 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CALVIN Y CHOI whose telephone number is (571)270-7882. The examiner can normally be reached on M-F 9-5.

30. Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

31. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CALVIN Y. CHOI
Primary Examiner
Art Unit 2812

/CALVIN Y CHOI/
Primary Examiner, Art Unit 2812

Notice of References Cited	Application/Control No. 16/047,182		Applicant(s)/Patent Under Reexamination TAO et al.	
	Examiner CALVIN Y CHOI		Art Unit 2812	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-9620512-B1	04-2017	Nishikawa; Masatoshi	H01L27/11524	1/1
*	B	US-20160056188-A1	02-2016	Lee; Yun-Ki	H01L27/1463	257/446
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	E					
	F					
	G					
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	I					
	J					
	K					
	L					
	M					

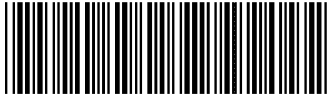
FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 16/047,182	Applicant(s)/Patent Under Reexamination TAO et al.
	Examiner CALVIN Y CHOI	Art Unit 2812

CPC - Searched*		
Symbol	Date	Examiner
H01L27/11524,11529,11582,11551-11556,11565,1157.cpc. or H01L21/76802,76831,76877.cpc. or H01L23/5226.cpc. - with date and text.		

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
257	314 - with date and text.		

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
H01L27/11524,11529,11582,11551-11556,11565,1157.cpc. or H01L21/76802,76831,76877.cpc. or H01L23/5226.cpc. - with date and text.	08/13/2019	CYC
257/314 - with date and text.	08/13/2019	CYC
Inventor, assignee, and text search using EAST - please refer to search history.	08/13/2019	CYC

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/CALVIN Y CHOI/ Primary Examiner, Art Unit 2812	
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2094	(Yangtze Memory Technologies).as. or TAO-Qian.in. or HU-Yushi.in. or LU-Zhenyu.in. or XIAO-Li-Hong.in. or DAI-Xiaowang.in. or ZHOU-Yu-Ting.in. or TANG-Zhao-Hui.in. or GUO-Mei-Lan.in. or TANG-ZhiWu.in. or WEI-Qinxiang.in. or XU-Qianbing.in. or LIU-Sha-Sha.in. or SUN-Jian-Hua.in. or WANG-Enbo.in.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/13 17:48
S2	87756	257/314.ccls. or H01L27/11524,11529,11582,11551-11556,11565,1157.cpc. or H01L21/76802,76831,76877.cpc. or H01L23/5226.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/13 17:51
S3	306	S1 and S2	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/13 17:51
S4	0	S1 and S2 and through\$1array\$1contact	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/13 17:51
S5	0	S2 and through\$1array\$1contact	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/13 17:51
S6	0	through\$1array\$1contact	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/13 17:51
S7	57	S3 and ((through\$1via) or (through near2 contact))	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/13 17:52
S8	36	S3 and ((through\$1via) or (through near2 contact)) and isolat\$5	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/13 18:17

S9	2	S3 and ((through\$1via) or (through near2 contact)) and isolat\$5 with substrate with stack	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/13 18:18
S10	200	S2 and ((through\$1via) or (through near2 contact)) and isolat\$5 with substrate with stack	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/13 18:31
S11	46	S2 and ((through\$1via) or (through near2 contact)) and isolat\$5 with substrate with stack with channel	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/13 18:31
S13	34	S2 and ((through\$1via) or (through near2 contact)) and isolat\$5 with substrate with stack with channel with (vertical\$4 or perpendicular\$4 or orthogonal\$4)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/13 18:32
S15	3904	through near2 array near2 (contact or electrode or plug)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/15 10:44
S16	62	through near2 array near2 (contact or electrode or plug) same (sti or isolat\$4)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/15 10:45
S17	14	through near2 array near2 (contact or electrode or plug) same (sti or isolat\$4) same substrate	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/15 10:45
S18	29	through near2 array near2 (contact or electrode or plug) same2 (sti or isolat\$4) same substrate	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/15 10:47
S19	9	through near2 array near2 (contact or electrode or plug) same2 (sti or isolat\$4) same substrate and memory	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/15 10:49
S20	32	through near2 array near2 (contact or electrode or plug) same (sti or isolat\$4) and memory	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/15 10:49

EAST Search History

S21	77	through near2 array near2 (contact or electrode or plug or via) same (sti or isolat\$4) and memory	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2019/08/15 10:49
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EAST Search History (I nterference)

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Bibliographic Data

Application No: 16/047,182

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged: /CALVIN Y CHOI/

Examiner's Signature

Initials

Title:

THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
07/27/2018	257	2812	4123.0190001
RULE			

APPLICANTS

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

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Sha Sha LIU Wuhan, CHINA

Jian Hua SUN Wuhan, CHINA

Enbo WANG Wuhan, CHINA

CONTINUING DATA

This application is a CON of PCT/CN2018/085421 05/03/2018

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

09/05/2018

STATE OR COUNTRY

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1100 NEW YORK AVENUE, N.W.

WASHINGTON, DC 20005

UNITED STATES

FILING FEE RECEIVED

\$2,080

PTO/SB/08a (07-09)

Approved for use through 11/30/2020, OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known	
		Application Number	16/047,182
		Filing Date	07-27-2018
		First Named Inventor	Qian TAO
		Art Unit	2812
		Examiner Name	CHOI, CALVIN Y
Sheet 1 of 2	Attorney Docket Number	4123.0190001	

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	US1	US- 2016/0071861 A1	03-10-2016	Serov et al.	
	US2	US- 2017/0186758 A1	06-29-2017	Lee et al.	
	US3	US- 2017/0358593 A1	12-14-2017	Yu et al.	
	US4	US- 2019/0057974 A1	02-21-2019	Lu et al.	
	US5	US- 8,247,895 B2	08-21-2012	Haensch et al.	
	US6	US- 9,530,789 B2	12-27-2016	Lee et al.	
	US7	US- 9,595,531 B2	03-14-2017	Zhu et al.	
	US8	US- 9,595,667 B2	03-14-2017	Pio	
		US-			
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
	FP1	TW 201419449 A	05-16-2014	MICRON TECHNOLOGY INC		
	FP2	TW 201606388 A	02-16-2016	INTEL CORP		
	FP3	TW 201721921 A	06-16-2017	MACRONIX INT CO LTD		✓
	FP4	CN 105047668 A	11-11-2015	SAMSUNG ELECTRONICS CO LTD		
	FP5	CN 105826323 A	08-03-2016	MACRONIX INT CO LTD		✓
	FP6	CN 106910746 A	06-30-2017	YANGTZE MEMORY TECH CO LTD		

Examiner Signature	Date Considered
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Application Number	16/047,182
Filing Date	07-27-2018
First Named Inventor	Qian TAO
Art Unit	2812
Examiner Name	CHOI, CALVIN Y
Attorney Docket Number	4123.0190001

Examiner Signature	Date Considered
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Micron Ex. 1002, p. 546
Micron v. YMTC
IPR2024-00788

PTO/SB/08b (07-09)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	16/047,182
				Filing Date	07-27-2018
				First Named Inventor	Qian TAO
				Art Unit	2812
				Examiner Name	CHOI, CALVIN Y
Sheet	1	of	1	Attorney Docket Number	4123.0190001

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Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	NPL1	International Search Report and Written Opinion of the International Searching Authority directed to related International Patent Application No. PCT/CN2018/085421, mailed January 20, 2019; 9 pages.	

Examiner Signature	/CALVIN Y CHOI/	Date Considered	08/19/2019
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/047,182	07/27/2018	Qian TAO	4123.0190001

CONFIRMATION NO. 7800

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

PUBLICATION NOTICE



OC000000112484886

Title:THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

Publication No.US-2019-0341399-A1

Publication Date:11/07/2019

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The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: TAO *et al.*

Applicant: Yangtze Memory Technologies
Co., Ltd.

Application No.: 16/047,182

Filing Date: July 27, 2018

Confirmation No.: 7800

Art Unit: 2812

Examiner: CHOI, Calvin Y.

Atty. Docket: 4123.0190001

Title: **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY
DEVICES**

First Supplemental Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on accompanying IDS Form PTO/SB/08a equivalent is a document that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed the publication date on the attached IDS Form based on information presently available to the undersigned. However, the listed publication date should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

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Applicant has checked the appropriate boxes below.

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- ☐ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.
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Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
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- ☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but on or before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of \$240.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

Atty. Dkt. No. 4123.0190001

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☐ 5. The patent family for one or more foreign language documents submitted herewith includes a United States patent, and other patent, in the English language. Copies of both the particular foreign patent(s) or published foreign patent applications cited in the foreign patent office communication, and that are not already of record in this application, are enclosed. Copies of the related United States or other English language patent or published application from the family list, if not already of record, are listed on the accompanying SB/08A form. For the purposes of a statement under 37 CFR 1.97(e)(1), the United States or other English language patent or published application are to be construed as being cited by the foreign patent office. MPEP 609.04(b)(V).

Atty. Dkt. No. 4123.0190001

- ☐ 6. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. MPEP 609.04(a)(III).
- ☐ 7. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).
- ☒ 8. In accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copy of the U.S. patent application publication cited as document **US1** on the attached IDS Form is submitted.
- ☐ 9. Copies of the _____ documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. _____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).
- ☐ 10. It is expected that the examiner will review the prosecution and cited art in the parent Application No(s). _____ in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.
- ☐ 11. In accordance with the Federal Circuit decision in *Dayco Prods., Inc. v. Total Containment, Inc.* 329 F.3d 1358 (Fed. Cir. 2003), Applicants submit herewith Office Actions from the co-pending U.S. Patent Application No. _____, filed _____, as documents _____ to _____. The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the

Atty. Dkt. No. 4123.0190001

present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Form, and indicate in the official file wrapper of this patent application that the document has been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: December 3, 2019

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

14176276_1

Atty. Dkt. No. 4123.0190001

Electronic Patent Application Fee Transmittal				
Application Number:		16047182		
Filing Date:		27-Jul-2018		
Title of Invention:		THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		
First Named Inventor/Applicant Name:		Qian TAO		
Filer:		Donald J. Featherstone/Laney Flanagan		
Attorney Docket Number:		4123.0190001		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
Total in USD (\$)				240

Electronic Acknowledgement Receipt	
EFS ID:	37907360
Application Number:	16047182
International Application Number:	
Confirmation Number:	7800
Title of Invention:	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES
First Named Inventor/Applicant Name:	Qian TAO
Customer Number:	26111
Filer:	Donald J. Featherstone/Laney Flanagan
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0190001
Receipt Date:	03-DEC-2019
Filing Date:	27-JUL-2018
Time Stamp:	09:35:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 240
RAM confirmation Number	E2019B3036089564
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		4123019_Bundle.pdf	72938	yes	8
			98a99e6b7be1c58c48c2451705043e8f0ae4c657		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Miscellaneous Incoming Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	7	
	Information Disclosure Statement (IDS) Form (SB08)		8	8	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30515	no	2
			dd9fbeb5c6a196a1b2de3412f19b1e66d0bb262a		
Warnings:					
Information:					
Total Files Size (in bytes):			103453		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DONALD J. FEATHERSTONE
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December 3, 2019

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 7800
Art Unit 2812
Attn: Mail Stop Amendment

Re: U.S. Utility Patent Application
Application No. 16/047,182; Filing Date: July 27, 2018
For: **THROUGH ARRAY CONTACT (TAC) FOR THREE-
DIMENSIONAL MEMORY DEVICES**
Inventors: TAO *et al.*
Our Ref: 4123.0190001

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Online Credit Card Payment Authorization in the amount of \$240.00 in payment of the fee under 37 C.F.R. § 1.17(p);
2. First Supplemental Information Disclosure Statement;
3. Form PTO/SB/08a (1 sheet) listing 1 document (**US1**);

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/lef
Enclosures

14176284_1

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P 202.371.2500 | F 202.371.2540 | sternekessler.com

Micron Ex. 1002, p. 561
Micron v. YMTC
IPR2024-00788

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 16/047,182		Filing Date 07/27/2018		☐ To be Mailed	
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED - PART I									
FOR		(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA			RATE (\$)		FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A			N/A			
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A			N/A			
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A			N/A			
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*			x \$100 =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*			x \$460 =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL			
APPLICATION AS AMENDED - PART II									
AMENDMENT	12/23/2019	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x \$100 =		0	
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	x \$460 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		0	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =			
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE			
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/CHRISTINE MOLLISH/			
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".									
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: TAO *et al.*

Applicant: Yangtze Memory Technologies Co., Ltd.

Application No.: 16/047,182

Filing Date: July 27, 2018

Confirmation No.: 7800

Art Unit: 2812

Examiner: CHOI, Calvin Y.

Atty. Docket: 4123.0190001

Title: **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES**

Amendment and Reply Under 37 C.F.R. § 1.111

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Office Action dated August 22, 2019, Applicant submits the following Amendment and Remarks.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A three-dimensional (3D) memory device, comprising:
a semiconductor substrate;
an alternating layer stack disposed on the semiconductor substrate;
a dielectric structure on an isolation region of the substrate and extending vertically through the alternating layer stack, wherein the alternating layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;
one or more through array contacts (TACs) extending vertically through the dielectric structure and the isolation region; ~~[[and]]~~
one or more channel structures extending vertically through the alternating layer stack;
an epitaxial layer between the one or more channel structures and the semiconductor substrate;
an etch stop plug on each of the one or more channel structures;
a staircase structure in the alternating layer;
slit structures extending vertically in the alternating layer stack; and
one or more contact layers on the one or more TACs, the one or more channel structures, and the slit structures.
2. (Cancelled)
3. (Original) The 3D memory device of claim 1, wherein the dielectric structure abuts a sidewall surface of the TACs.
4. (Previously Presented) The 3D memory device claim 1, wherein the 3D memory device is a NAND 3D memory device.
5. (Original) The 3D memory device of claim 1, wherein the alternating layer stack comprises alternating pairs of a dielectric and a conductor layer.

Atty. Dkt. No. 4123.0190001

6. (Previously Presented) The 3D memory device of claim 1, wherein the dielectric material is silicon oxide.
7. (Previously Presented) The 3D memory device of claim 1, wherein the dielectric structure comprises an oxide.
8. (Original) The 3D memory device of claim 1, wherein the dielectric structure defines a through array contact region within the 3D memory device.
9. (Original) The 3D memory device of claim 1, wherein the dielectric structure has a footprint equal to or smaller than the isolation region.
10. (Currently Amended) A method for forming a 3D memory device, the method comprising:
 - forming an isolation structure on a substrate;
 - disposing an alternating dielectric layer stack on the substrate, the alternating dielectric layer stack comprising pairs of a first dielectric layer and a second dielectric layer different from the first dielectric layer;
 - disposing a staircase structure in the alternating dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;
 - forming a channel structure extending vertically in the alternating dielectric layer stack;
 - disposing a word line contact on the conductor layer of the each level of the staircase structure;
 - forming one or more slit structures extending vertically in the alternating dielectric layer stack;
 - forming an opening in the alternating dielectric layer stack, wherein the opening exposes the isolation structure;
 - filling the opening with a dielectric layer to form a dielectric structure as a through array contact (TAC) region of the 3D memory device;

removing portions of the dielectric structure and the isolation structure until the substrate is exposed to form a TAC opening that vertically extends through the dielectric structure and the isolation structure; [[and]]

filling the TAC opening with a conductor to form a TAC structure in the TAC region, wherein the TAC structure is in contact with the substrate; and

disposing a local contact on the channel structure, the one or more slit structures, and the TAC structure.

11. (Currently Amended) The method of claim 10, wherein the forming one or more slit structures before forming the TAC opening the method further comprises:

forming slit openings extending vertically in the alternating dielectric layer stack, wherein the slit openings expose a doped region of the substrate;

replacing the second dielectric layer through the one or more slit openings with [[a]] the conductor layer to convert the alternating dielectric layer stack to an alternating dielectric/conductor layer stack; and

filling the one or more slit openings with a conductor ~~to form one or more slit structures extending vertically in the alternating dielectric/conductor layer stack.~~

12. (Currently Amended) The method of claim 10, wherein ~~before forming the channel structure~~ the disposing the staircase structure comprises performing a trim-etch process to form a staircase structure in the alternating dielectric layer stack before forming the channel structure.

13. (Original) The method of claim 10, wherein filling the opening with the dielectric layer comprises depositing the dielectric layer with a chemical vapor deposition, a plasma-enhanced chemical vapor deposition, or a physical vapor deposition process.

14. (Original) The method of claim 10, wherein filling the opening with the dielectric layer comprises forming an oxide.

15. (Original) The method of claim 10, wherein the first dielectric layer comprises an oxide and the second dielectric layer comprises a nitride.

16. (Currently Amended) A three-dimensional (3D) memory device, comprising:
a substrate with an isolation structure;
an alternating conductor/dielectric layer stack disposed on the substrate;
a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;

a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

a word line contact disposed on the conductor layer of the each level;

local contacts disposed on the channel structures and the slit structures; and

through array contacts ([[TAC]]TACs) extending vertically through the dielectric and the isolation structures.

17. (Cancelled)

18. (Currently Amended) The 3D memory device of claim 16, wherein the dielectric structure abuts a sidewall of [[the]] each TAC of the TACs.

19. (Original) The 3D memory device of claim 16, wherein the dielectric structure comprises a through array contact region of the 3D memory device.

20. (Currently Amended) The 3D memory device of claim 16, further comprising:
an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures; and

an epitaxial layer disposed between ~~[[each]] the channel structure~~ structures and the substrate.

21. (New) The 3D memory device of claim 16, wherein the dielectric material comprises silicon oxide.

22. (New) The 3D memory device of claim 16, wherein the TACs comprise a conductive material.

Remarks

Upon entry of the foregoing amendment, claims 1, 3-16, and 18-22 are pending in the application, with claims 1, 10, and 16 being the independent claims. Claims 1, 10-12, 16, 18, and 20 are sought to be amended. Claims 2 and 17 are sought to be cancelled without prejudice to or disclaimer of the subject matter therein. New claims 21 and 22 are sought to be added. Exemplary support for the amended claims can be found, *inter alia*, in ¶¶ [0039] and [0061] and Fig. 2 of the originally-filed application. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding rejections and that they be withdrawn. Throughout the arguments, Applicant reminds the Examiner that the claims are given their broadest reasonable meaning in view of the specification, and any paraphrasing of the claim features is not to be interpreted as reading any features into, or characterizing of, the claims.

Rejections under 35 U.S.C. § 103

Claims 1, 3-16, and 18-20 are rejected under 35 U.S.C. § 103 as allegedly being unpatentable over U.S. Patent No. 9,620,512 B1 to Nishikawa *et al.* ("Nishikawa") in view of U.S. Patent Application Publication No. 2016/0056188 A1 to Lee *et al.* ("Lee"). Applicant respectfully traverses the rejections.

Claims 1, 3-9, 16, and 18-20

Without acquiescing to the propriety of the rejection, independent claims 1 and 16 have been amended to incorporate the allowable subject matter recited in claims 2 and 17, respectively. Further, dependent claims 3-9 and 18-20 are also patentable at least because they recite all of the features of independent claims 1 and 16 from which they depend, as well as for their additional distinguishing features. Accordingly, Applicant respectfully requests the Examiner to reconsider and withdraw the rejections under 35 U.S.C. § 103 and to pass claims 1, 3-9, 16, and 18-20 to allowance.

Claims 10-15

Without acquiescing to the propriety of the rejection, independent claim 10 has been amended to recite features that further distinguish from Nishikawa and Lee. For example, claim 10 recites, *inter alia*,

disposing a staircase structure in the alternating dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon...

disposing a word line contact on the conductor layer of the each level of the staircase structure;

forming one or more slit structures extending vertically in the alternating dielectric layer stack...

disposing a local contact on the channel structure, the one or more slit structures, and the TAC structures.

Nishikawa does not disclose these distinguishing features. For example, Nishikawa is completely silent regarding at least “a local contact on the channel structure, the one or more slit structures, and the TAC structures.” Lee does not cure the deficiencies of Nishikawa. Further, dependent claims 11-15 are also patentable at least because they recite all of the features of independent claim 10 from which they depend, as well as for their additional distinguishing features. Accordingly, Applicant respectfully requests the Examiner to reconsider and withdraw the rejections under 35 U.S.C. §103 and to pass claims 10-15 to allowance.

Allowable Subject Matter

Applicant thanks the Examiner for indicating the allowability of claims 2 and 17 if they were rewritten in independent form including all limitations of the base claim and any intervening claims. Applicant has amended claims 1 and 16 to respectively recite features of claims 2 and 17.

New Claims 21 and 22

New claims 21 and 22 have been added. At least based on their dependencies from claim 16, claims 21 and 22 are distinguishable over the applied reference for the reasons above, as well as for their own distinguishing features. Accordingly, Applicant respectfully requests that claims 21 and 22 be passed to allowance.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 12/23/19 _____

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Washington, D.C. 20005-3934
(202) 371-2600

13800788_1.docx

Electronic Patent Application Fee Transmittal				
Application Number:		16047182		
Filing Date:		27-Jul-2018		
Title of Invention:		THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		
First Named Inventor/Applicant Name:		Qian TAO		
Filer:		Donald J. Featherstone/Catherine Saunders		
Attorney Docket Number:		4123.0190001		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description		Fee Code	Quantity	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 1 month with \$0 paid	1251	1	200	200
Miscellaneous:				
Total in USD (\$)				200

Electronic Acknowledgement Receipt	
EFS ID:	38116967
Application Number:	16047182
International Application Number:	
Confirmation Number:	7800
Title of Invention:	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES
First Named Inventor/Applicant Name:	Qian TAO
Customer Number:	26111
Filer:	Donald J. Featherstone/Catherine Saunders
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0190001
Receipt Date:	23-DEC-2019
Filing Date:	27-JUL-2018
Time Stamp:	12:41:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 200
RAM confirmation Number	E2019BMC42063771
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Filing-Bundle-4123-0190001. PDF	530674	yes	11
			55f6dc275384c5d83b5310401cff3dee3ba9c05e		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Miscellaneous Incoming Letter		1	1	
	Extension of Time		2	2	
	Amendment/Req. Reconsideration-After Non-Final Reject		3	3	
	Claims		4	8	
	Applicant Arguments/Remarks Made in an Amendment		9	11	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30988	no	2
			38edd7d7c86163f8703198def03d71ef7cd0d24c		
Warnings:					
Information:					
Total Files Size (in bytes):			561662		

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

December 23, 2019

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 7800
Art Unit 2812
Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 16/047,182; Filing Date: July 27, 2018
For: **THROUGH ARRAY CONTACT (TAC) FOR THREE-
DIMENSIONAL MEMORY DEVICES**
Inventors: TAO *et al.*
Our Ref: 4123.0190001

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Online Credit Card Payment Authorization for \$200.00 to cover extension of time fee due;
2. Petition for Extension of Time Under 37 C.F.R. § 1.136(a); and
3. Amendment and Reply Under 37 C.F.R. § 1.111.

The above-listed documents are filed electronically.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036. If extensions of time under 37 C.F.R. § 1.136 other than those otherwise provided for herewith are required to prevent abandonment of the present patent application, then such extensions of time are hereby petitioned, and any fees therefor are hereby authorized to be charged to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/Y-G/cms
Enclosure

13800669_1.docx

Sterne, Kessler, Goldstein & Fox P.L.L.C. | 1100 New York Avenue, NW | Washington, D.C. 20005
P 202.371.2600 | F 202.371.2540 | sternekessler.com

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)		Docket Number (Optional) 4123.0190001		
Application Number 16/047,182	Filed July 27, 2018			
For THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES				
Art Unit 2812	Examiner CHOI, Calvin Y.			
This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application. The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):				
	<u>Fee</u>	<u>Small Entity Fee</u>	<u>Micro Entity Fee</u>	
☒ One month (37 CFR 1.17(a)(1))	\$200	\$100	\$50	\$ <u>200.00</u>
☐ Two months (37 CFR 1.17(a)(2))	\$600	\$300	\$150	\$ _____
☐ Three months (37 CFR 1.17(a)(3))	\$1,400	\$700	\$350	\$ _____
☐ Four months (37 CFR 1.17(a)(4))	\$2,200	\$1,100	\$550	\$ _____
☐ Five months (37 CFR 1.17(a)(5))	\$3,000	\$1,500	\$750	\$ _____
☐ Applicant asserts small entity status. See 37 CFR 1.27.				
☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.				
☐ A check in the amount of the fee is enclosed.				
☐ Payment by credit card. Form PTO-2038 is attached.				
☐ The Director has already been authorized to charge fees in this application to a Deposit Account.				
☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number <u>19-0036</u>				
☒ Payment made via EFS-Web.				
WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.				
I am the				
☐ applicant/inventor.				
☐ assignee of record of the entire interest. See 37 CFR 3.71. 37 CFR 3.73(b) statement is enclosed (Form PTO/SB/96).				
☒ attorney or agent of record. Registration number <u>33,876</u>				
☐ attorney or agent acting under 37 CFR 1.34. Registration number _____				
<u>/Donald J. Featherstone/</u>		<u>12/23/19</u>		
Signature		Date		
<u>Donald J. Featherstone</u>		<u>(202) 371-2600</u>		
Typed or printed name		Telephone Number		
NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below.				
☒ * Total of <u>1 (one)</u> forms are submitted.				

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

26111 7590 01/13/2020
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
CHOI, CALVIN Y	
ART UNIT	PAPER NUMBER

2812

DATE MAILED: 01/13/2020

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/047,182	07/27/2018	Qian TAO	4123.0190001	7800

TITLE OF INVENTION: THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	04/13/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 01/13/2020
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/047,182	07/27/2018	Qian TAO	4123.0190001	7800

TITLE OF INVENTION: THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	04/13/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOI, CALVIN Y	2812	257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/047,182	07/27/2018	Qian TAO	4123.0190001	7800
26111 7590 01/13/2020 STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER CHOI, CALVIN Y	
			ART UNIT 2812	PAPER NUMBER
DATE MAILED: 01/13/2020				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/047,182	Applicant(s) TAO et al.	
	Examiner CALVIN Y CHOI	Art Unit 2812	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the Remarks and Amendments filed on 23 December 2019.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1,3-16 and 18-22. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____. 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
--	--

/CALVIN Y CHOI/
Primary Examiner, Art Unit 2812

DETAILED ACTION

1. This Office Action is in response to the Remarks and Amendments filed on 23 December 2019.

Notice of Pre-AIA or AIA Status

2. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Allowable Subject Matter

3. **Claims 1, 3-16, and 18-22 are allowed.**

4. The following is an examiner's statement of reasons for allowance: independent claims 1, 10, and 16 are allowable because the closest prior art does not appear to disclose, alone or in combination, the steps and the elements resulting from the steps of: forming an isolation structure on a substrate; disposing an alternating dielectric layer stack on the substrate, the alternating dielectric layer stack comprising pairs of a first dielectric layer and a second dielectric layer different from the first dielectric layer; disposing a staircase structure in the alternating dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon; forming a channel structure extending vertically in the alternating dielectric layer stack; disposing a word line contact on the conductor layer of the each level of the staircase structure; forming one or more slit structures extending vertically in the alternating dielectric layer stack; forming an opening in the alternating dielectric layer stack, wherein the opening exposes the isolation structure; filling the opening with a dielectric layer to form a dielectric structure as a through array contact (TAC) region of the 3D memory device; removing portions of the dielectric structure and the isolation structure until the substrate is exposed to form a TAC opening that vertically extends through the dielectric structure and the isolation structure; and filling the TAC opening with a conductor to form a TAC structure in the TAC region, wherein the TAC structure is in contact with the substrate; and disposing a local contact on the channel structure, the one or more slit structures, and the TAC structure. Specifically, the aforementioned

limitations appear to be material to the inventive concept of the application at hand to have a fabrication technique that can more easily produce memory cells that have smaller individual sizes and a higher density of features at a lower cost.

5. The dependent claims of the application at hand are allowable because they respectively depend, directly or indirectly, from the allowable independent claims of the application at hand.

Therefore, the dependent claims incorporate the allowable limitations of the independent claims.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CALVIN YCHOI whose telephone number is (571)270-7882. The examiner can normally be reached on M-F 9-5.

8. Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic

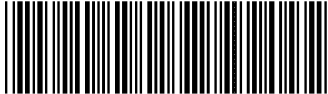
Application/Control Number:16/047,182
Art Unit:2812

Page4

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CALVIN Y. CHOI
Primary Examiner
Art Unit 2812

/CALVIN Y CHOI/
Primary Examiner, Art Unit 2812

Issue Classification 	Application/Control No. 16/047,182	Applicant(s)/Patent Under Reexamination TAO et al.
	Examiner CALVIN Y CHOI	Art Unit 2812

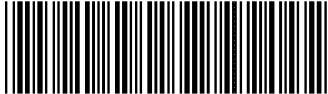
CPC						
Symbol					Type	Version
H01L	/	27	/	11582	F	2013-01-01
H01L	/	21	/	76802	I	2013-01-01
H01L	/	21	/	76831	I	2013-01-01
H01L	/	21	/	76877	I	2013-01-01
H01L	/	23	/	5226	I	2013-01-01
H01L	/	27	/	11565	I	2013-01-01
H01L	/	27	/	1157	I	2013-01-01

CPC Combination Sets							
Symbol				Type	Set	Ranking	Version
	/		/				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/CALVIN Y CHOI/	02 January 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	9	2

U.S. Patent and Trademark Office

Part of Paper No.: 20200102

Issue Classification 	Application/Control No. 16/047,182	Applicant(s)/Patent Under Reexamination TAO et al.
	Examiner CALVIN Y CHOI	Art Unit 2812

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L		29	76
NON-CLAIMED			

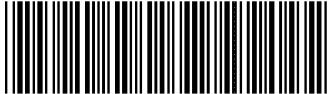
US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/CALVIN Y CHOI/ Primary Examiner, Art Unit 2812	02 January 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	9	2

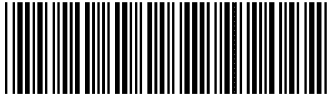
U.S. Patent and Trademark Office

Part of Paper No.: 20200102

Issue Classification 	Application/Control No. 16/047,182	Applicant(s)/Patent Under Reexamination TAO et al.
	Examiner CALVIN Y CHOI	Art Unit 2812

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	9	10	17	19										
	2	10	11	18	20										
2	3	11	12	19	21										
3	4	12	13	20	22										
4	5	13	14												
5	6	14	15												
6	7	15	16												
7	8		17												
8	9	16	18												

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/CALVIN Y CHOI/	02 January 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	9	2

<i>Search Notes</i> 	Application/Control No. 16/047,182	Applicant(s)/Patent Under Reexamination TAO et al.
	Examiner CALVIN Y CHOI	Art Unit 2812

CPC - Searched*		
Symbol	Date	Examiner
H01L27/11524,11529,11582,11551-11556,11565,1157.cpc. or H01L21/76802,76831,76877.cpc. or H01L23/5226.cpc. - with date and text.	08/13/2019	CYC

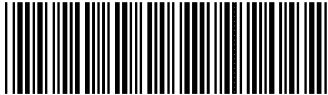
CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
257	314 - with date and text.	08/13/2019	CYC

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
H01L27/11524,11529,11582,11551-11556,11565,1157.cpc. or H01L21/76802,76831,76877.cpc. or H01L23/5226.cpc. - with date and text.	08/13/2019	CYC
257/314 - with date and text.	08/13/2019	CYC
Inventor, assignee, and text search using EAST - please refer to search history.	08/13/2019	CYC
Updated text search using EAST - please refer to updated search history.	01/02/2020	CYC

/CALVIN Y CHOI/ Primary Examiner, Art Unit 2812	
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<i>Search Notes</i> 	Application/Control No. 16/047,182	Applicant(s)/Patent Under Reexamination TAO et al.
	Examiner CALVIN Y CHOI	Art Unit 2812

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	H01L27/11524,11529,11582,11551-11556,11565,1157.cpc. or H01L21/76802,76831,76877.cpc. or H01L23/5226.cpc. - with date and text.	01/02/2020	CYC
257	314 - with date and text.	01/02/2020	CYC

/CALVIN Y CHOI/ Primary Examiner, Art Unit 2812	
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EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	9	("20170179026" "20160071861" "20170186758" "20170358593" "20190057974" "8247895" "9530789" "9595531" "9595667").PN.	US-PGPUB; USPAT	ADJ	ON	2020/01/02 11:48

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	42256	257/314.ccls. or H01L27/11524,11529,11582,11551-11556,11565,1157.cpc. or H01L21/76802,76831,76877.cpc. or H01L23/5226.cpc.	US-PGPUB; USPAT	ADJ	ON	2020/01/02 11:10
L2	4	through near2 array near2 (contact or electrode or plug or via) same (sti or isolat\$4) and memory and (stepped or stairway)	US-PGPUB; USPAT	ADJ	ON	2020/01/02 11:15
L3	4	L1 and L2	US-PGPUB; USPAT	ADJ	ON	2020/01/02 11:16

1/ 2/ 2020 11:49:13 AM

C:\Users\cchoi2\Documents\EAST\Workspaces\16047182 - Tao et al.wsp

PTO/SB/08a (07-09)

Approved for use through 11/30/2020. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known	
		Application Number	16/047,182
		Filing Date	07-27-2018
		First Named Inventor	Qian TAO
		Art Unit	2812
		Examiner Name	CHOI, CALVIN Y
Sheet 1	of 1	Attorney Docket Number	4123.0190001

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	US1	US- 2017/0179026 A1	06-22-2017	Toyama et al.	
		US-			
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		US-			

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				

Examiner Signature	/CALVIN Y CHOI/	Date Considered	01/02/2020
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.Y.C/

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

April 13, 2020

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 7800
Mail Stop Issue Fee

Re: Allowed U.S. Utility Patent Application
Appl. No. 16/047,182; Filed: July 27, 2018
For: **THROUGH ARRAY CONTACT (TAC) FOR THREE-
DIMENSIONAL MEMORY DEVICES**
Inventors: TAO *et al.*
Our Ref: 4123.0190001

Commissioner:

In response to the **Notice of Allowance and Fee(s) Due** dated January 13, 2020, the following documents are transmitted for appropriate action by the U.S. Patent and Trademark Office:

1. Online Credit Card Payment Authorization for \$1,000.00 to cover Issue Fee due;
2. Issue Fee Transmittal (Form PTOL-85); and
3. Comments on Statement of Reasons for Allowance.

The above-listed documents are filed electronically.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/Y-G/cms
Enclosures

14455740_1.docx

Sterne, Kessler, Goldstein & Fox P.L.L.C. | 1100 New York Avenue, NW | Washington, D.C. 20005

P 202.371.2500 | F 202.371.2540 | sternekessler.com

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 01/13/2020
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/047,182	07/27/2018	Qian TAO	4123.0190001	7800

TITLE OF INVENTION: THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	04/13/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOI, CALVIN Y	2812	257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Sterne, Kessler, Goldstein & Fox P.L.L.C.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Yangtze Memory Technologies Co., Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Wuhan, CHINA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 19-0036

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Donald J. Featherstone/

Date 4/13/2020

Typed or printed name Donald J. Featherstone

Registration No. 33,876

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: TAO *et al.*

Applicant: Yangtze Memory Technologies Co., Ltd.

Application No.: 16/047,182

Filing Date: July 27, 2018

Confirmation No.: 7800

Art Unit: 2812

Examiner: CHOI, Calvin Y.

Atty. Docket: 4123.0190001

Title: **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES**

Comments on Statement of Reasons for Allowance

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Mail Stop: Issue Fee

Commissioner:

Applicant thanks the Examiner for indicating the allowability of claims 1, 3-16, and 18-22 in the Notice of Allowance dated January 13, 2020.

Applicant notes the Examiner's Statement of Reasons for Allowance presented on page 2 of the Notice of Allowance. Applicant reserves the right to demonstrate claims 1, 3-16, and 18-22 are allowable over the art made of record for further reasons related to any of their recited features.

Applicant further contends that reservation of this right does not give rise to any implication regarding whether the Applicant agrees with or acquiesces in the reasoning provided by the Examiner.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 4/13/2020

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
14455723_1.docx

Electronic Patent Application Fee Transmittal				
Application Number:		16047182		
Filing Date:		27-Jul-2018		
Title of Invention:		THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		
First Named Inventor/Applicant Name:		Qian TAO		
Filer:		Donald J. Featherstone/Catherine Saunders		
Attorney Docket Number:		4123.0190001		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1000

Electronic Acknowledgement Receipt	
EFS ID:	39136499
Application Number:	16047182
International Application Number:	
Confirmation Number:	7800
Title of Invention:	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES
First Named Inventor/Applicant Name:	Qian TAO
Customer Number:	26111
Filer:	Donald J. Featherstone/Catherine Saunders
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0190001
Receipt Date:	13-APR-2020
Filing Date:	27-JUL-2018
Time Stamp:	16:08:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1000
RAM confirmation Number	E20204CG09506234
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Filing-Bundle-4123-0190001.pdf	961639	yes	3
			6db3af2aa9057eff0714d6058c55696330dfa07		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Miscellaneous Incoming Letter		1	1	
	Issue Fee Payment (PTO-85B)		2	2	
	Post Allowance Communication - Incoming		3	3	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30416	no	2
			0cdfd43ee5eeee8c4687b90cf841c16bef7317a9		
Warnings:					
Information:					
Total Files Size (in bytes):			992055		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/047,182	05/19/2020	10658378	4123.0190001	7800

26111 7590 04/29/2020
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Qian TAO, Wuhan, CHINA;
Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA
Yushi HU, Wuhan, CHINA;
Zhenyu LU, Wuhan, CHINA;
Li Hong XIAO, Wuhan, CHINA;
Xiaowang DAI, Wuhan, CHINA;
Yu Ting ZHOU, Wuhan, CHINA;
Zhao Hui TANG, Wuhan, CHINA;
Mei Lan GUO, Wuhan, CHINA;
ZhiWu TANG, Wuhan, CHINA;
Qinxiang WEI, Wuhan, CHINA;
Qianbing XU, Wuhan, CHINA;
Sha Sha LIU, Wuhan, CHINA;

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IR103 (Rev. 10/09)

Micron Ex. 1002, p. 602
Micron v. YMTC
IPR2024-00788