

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00788
U.S. Patent No. 10,658,378
Issue Date: May 19, 2020

Title: THROUGH ARRAY CONTACT (TAC) FOR
THREE-DIMENSIONAL MEMORY DEVICES

DECLARATION OF DR. JACK C. LEE

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I, Dr. Jack C. Lee, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in claims 15-17 and 19-20 of U.S. Patent No. 10,658,378, which I refer to herein as the ’378 patent.

3. My opinions and the bases for my opinions are set forth below.

4. I am being compensated at my standard consulting rate of \$680 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. BACKGROUND AND EXPERT QUALIFICATIONS

5. My curriculum vitae (“CV”) is attached hereto as Ex. 1004 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and NAND memory technology.

6. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley (“UC Berkeley”).

7. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

8. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers (“IEEE”) International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

9. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin (“UT Austin”). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. This includes classes relating to, among other things, 3D NAND technology. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professorship in Engineering in the

Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

10. My current research and teaching interests include semiconductor devices, semiconductor memory applications (including non-volatile memory), fabrication processes, silicon-on-insulator technologies, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display technologies, photovoltaic and solar cell technologies, high-K gate dielectrics and electrode, and alternative channel materials. I routinely encounter and address topics relating to NAND flash memory, and more specifically 3D NAND flash memory, in my research. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

11. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 books and book chapters on semiconductor technologies. Many of these relate to the structure and operation of memory devices, including non-volatile memory such as NAND flash memory and 3D NAND flash memory. I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g., inventor recognition and best paper awards.

12. In 2002, I became an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices.” I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

13. I have served in various technology consulting and business advisor roles. For example, I have taught short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

III. ASSIGNMENT AND MATERIALS CONSIDERED

14. I have been asked to provide analysis and explain the subject matter of the '378 patent, including the state of the art when the application underlying the '378 patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '378 patent including how that art relates to claims 15-17 and 19-20 (which I refer to as the “challenged claims”) of the '378 patent and to provide my opinions regarding whether that art invalidates the challenged claims.

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15. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the challenged claims of the '378 patent. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part that any claim complies with the requirements of any other applicable rule.

16. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the '378 patent.

17. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, and my experience. I have also reviewed and considered the '378 patent (Ex. 1001), its prosecution history (Ex. 1002), and the following additional materials:

Exhibit	Description
1005	U.S. Patent Publ. No. 2017/0179026 A1 (“Toyama”)
1006	U.S. Patent No. 10,354,980 (“Mushiga”)
1007	U.S. Patent No. 10,262,945 (“Makala”)
1011	CN109075169A Office Action, dated November 14, 2019
1012	Certified Translation of CN109075169A Office Action, dated November 14, 2019

Exhibit	Description
1013	CN109075169A Reexamination Decision, dated November 25, 2021
1014	Certified Translation of CN109075169A Reexamination Decision, dated November 25, 2021
1015	Micheloni, “3D Flash Memories” (2016)
1016	Aritome, “NAND Flash Memory Technologies” (2016)
1017	U.S. Patent No. 9,620,512 to Nishikawa et al.
1018	U.S. Patent Publ. No. 2016/0056188 A1 to Lee et al.
1019	U.S. Patent No. 9,293,348 to Lai et al.
1020	U.S. Patent No. 10,169,169 to Ge et al.
1021	U.S. Patent No. 8,697,519 to Jee et al.
1022	Excerpts from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)

IV. UNDERSTANDING OF THE LAW

18. I am not an attorney, but have been instructed in and applied the law as described in this section.

19. I understand that the first step in comparing a challenged claim to the prior art is for the claim to be properly construed. I address how a person of ordinary skill in the art (POSITA) would have understood the challenged claims of the alleged invention in Section VIII below.

20. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a POSITA of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

21. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there must be some reason or motivation for a POSITA to combine the prior art references to arrive at the claimed subject matter.

22. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a POSITA at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

23. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine. The motivation linking two or more prior art references can also come from other sources, including, for instance, economic or market demand or the common sense of a POSITA at the time of the invention.

24. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

25. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

26. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield

predictable results. Thus, where all the elements of a claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

27. Additionally, I understand that a patent is likely to be invalid for obviousness if a POSITA can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

28. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

29. I also understand that a POSITA must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

30. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial

expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

31. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a “nexus,” between any such secondary indicia and the claimed invention.

32. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

33. I provide my opinions in this declaration based on the guidelines set forth above.

V. LEVEL OF SKILL IN THE ART

34. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

35. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have

been further informed and understand that a person of ordinary skill in the art (POSITA) is also a person of ordinary creativity.

36. In my opinion, a POSITA in the field of the '378 patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

37. In my opinion, this POSITA would also have been aware of and generally knowledgeable about semiconductor manufacturing and 3D NAND's structure, its component parts, how it operates, and how it is controlled.

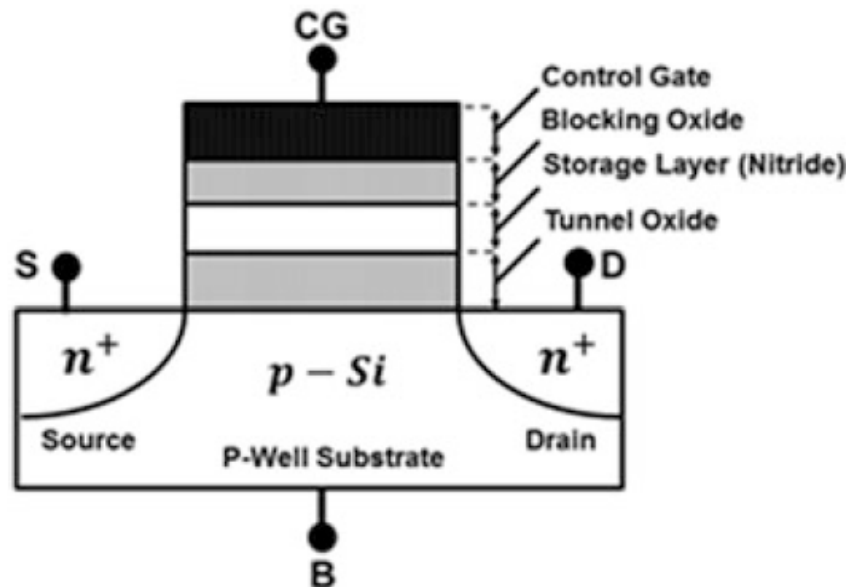
38. In view of my educational background and decades of experience working with semiconductor memory—including non-volatile 3D NAND flash memory—I was a person of more than the ordinary level of skill in the art as of May 2018. In forming my opinion, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed taking into account the perspective of an ordinarily skilled artisan.

VI. TECHNOLOGY BACKGROUND AND STATE OF THE ART

39. I have been asked to provide a brief overview of the technology relevant to the '378 patent and the state of the art when the '378 priority application was filed.

40. The '378 patent (and the prior art I discuss herein) relate to three-dimensional (3D) NAND flash memory. “Flash memory” has been known for many decades and is a type of memory that stores information even when power is removed (*viz.*, when the device is turned off).

41. At the heart of flash memory is the “memory cell,” which stores information as electrical charge. An example memory cell is below:



Ex. 1015, 41. In a memory cell, current flows from the “drain” of the device to the “source” of the device, which is typically connected to a low voltage, such as ground. *Id.*, 150 (“[T]he Source Line ... plays the role of the ‘local ground’ for each memory cell.”).

42. The acronym “NAND” refers to a “not-AND” logic gate, and NAND flash memory is a particular type of flash memory where the memory cells form a

structure similar to that of a NAND gate. Ex. 1015, at 14. The other most common type of flash memory is NOR flash, but NAND offers a higher integration density and occupies a larger market than NOR flash.

43. A NAND flash memory device, like most flash memory devices, has an associated memory controller that controls the read, write, and erase operations on a memory cell by applying a voltage to that cell's "control gate," labeled as "CG" in the above figures. Ex. 1015, 41.

44. For many years, a NAND flash memory was "planar," that is, two-dimensional (2D). In 2D NAND flash memory, all memory cells lie on a 2D plane (*i.e.*, the x-y plane) on the surface of a memory chip as shown below:

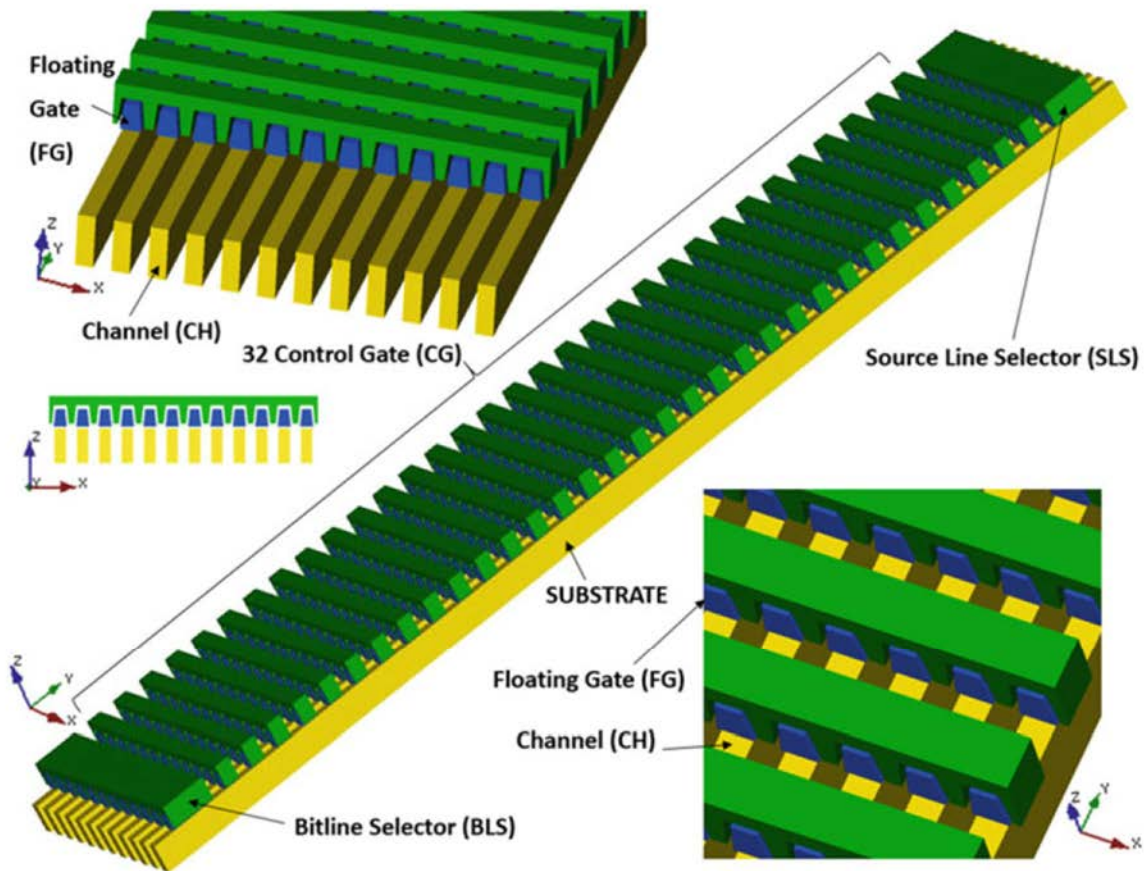


Fig. 3.9 Bird's-eye view of a planar NAND string

Ex. 1015, at 86.

45. To boost data storage densities and reduce cost per gigabit, the art developed so-called “three-dimensional (3D) NAND flash cells” starting in about 2006. Ex. 1016, 292. Unlike planar 2D NAND flash memory, in 3D NAND flash memory the memory cells are arranged in vertical, cylindrical NAND flash columns, often referred to as “memory strings.” Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block and turning

the 2D NAND string on its side, resulting in a 3D structure with a vertical channel.

The following image provides an example:

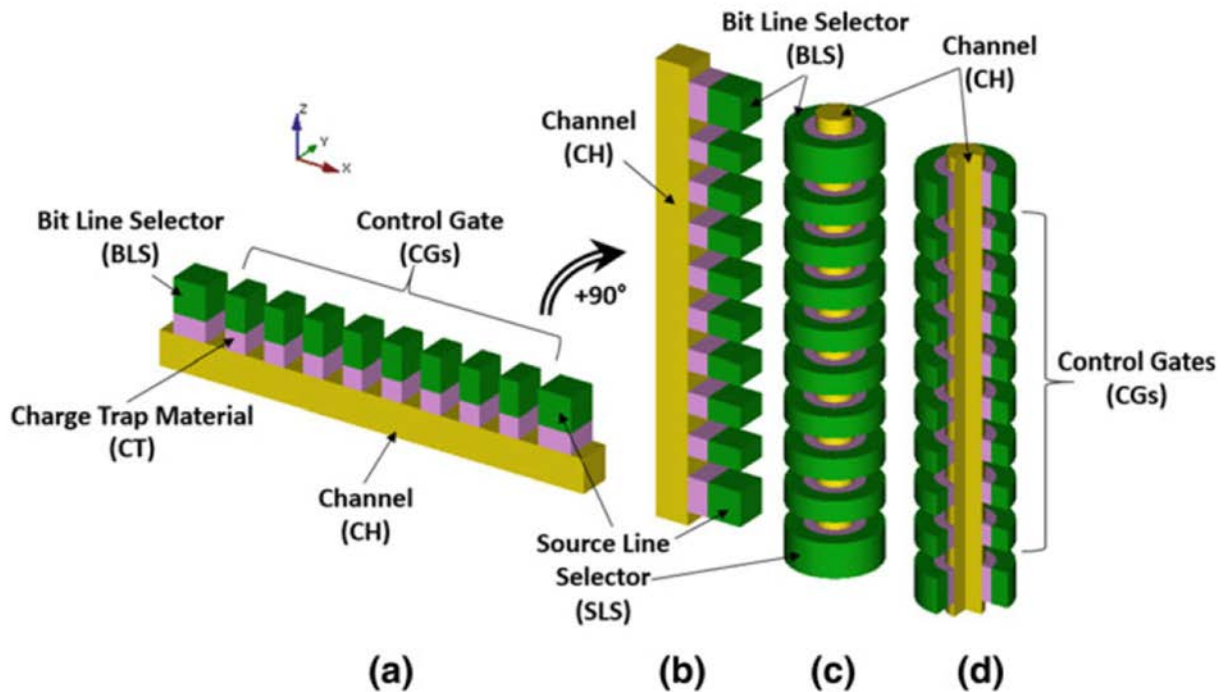


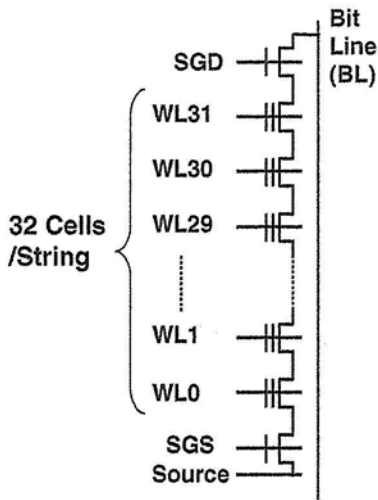
Fig. 4.1 NAND Flash string with horizontal gate and vertical channel: **a** planar, **b** planar rotated by 90°, **c** vertical channel with cylindrical shape and **d** its cross section

Ex. 1015, 102. As labeled in Figure 4.1, above, each NAND string includes a “cylindrical channel.” *Id.*, 58. The concept of a “channel” was well-known in semiconductor devices and refers to a thin and layer of charge that is formed between the source and drain of a transistor when a voltage is applied to the gate. The “channel” is highly conductive and allows current to easily flow between the source and drain. The “cylindrical channel” in 3D NAND devices also provides the means for current to flow in a memory string.

46. Multiple of such vertical channels are then repeated in a three-dimensional array. Ex. 1016, 296.

47. As can be seen above, the NAND flash memory “strings” each contain multiple cells “connected in series.” Ex. 1016, 38. The source of one cell is connected to the drain of the next one. Depending on the technology, typically a string consists of 32 to 128 NAND cells.

48. Each end of a string is terminated with a “select transistor.” One is often called the “SGD” (drain-end select gate transistor) and the other one is often called “SGS” (source-end select gate transistor). The “SGD connects” at the string’s drain side “to isolate it from the bit line (BL).” Ex. 1016, 38. Hence, the SGD is also known as the “bit line select transistor” or the “upper select gate.” The SGS connects at the string’s source side “to isolate it from a source line (SL).” *Id.* Since the source line is commonly connected to the ground terminal, SGS is also known as the “ground select transistor” or the “lower select gate.” Word lines are connected to each memory cell control gate. *Id.*, 38-39. A schematic representation of a memory string is shown below:



Ex. 1016, 39.

49. Various architectures for constructing 3D NAND flash memory were known in the art. One such example is the well-known BiCS (Bit Cost Scalable) architecture, where various “contacts” (electrical connections) are formed on top of the memory array. Below are two illustrations of the BiCS architecture show top and bottom perspective views.

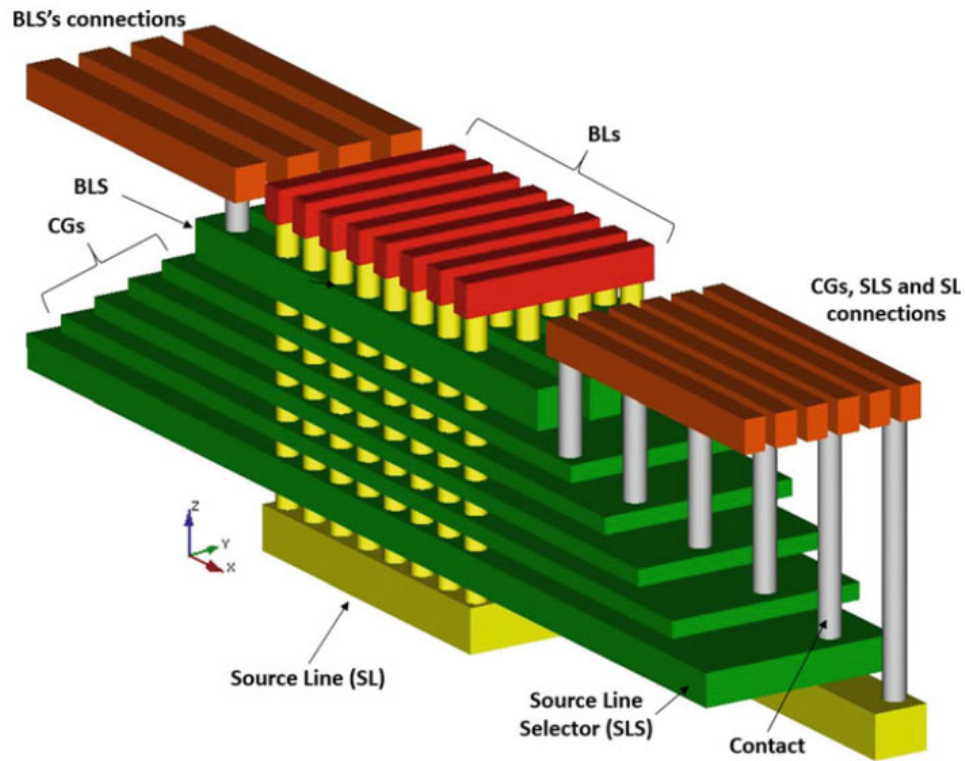


Fig. 4.13 Top bird's eye view of BiCS with gate connections

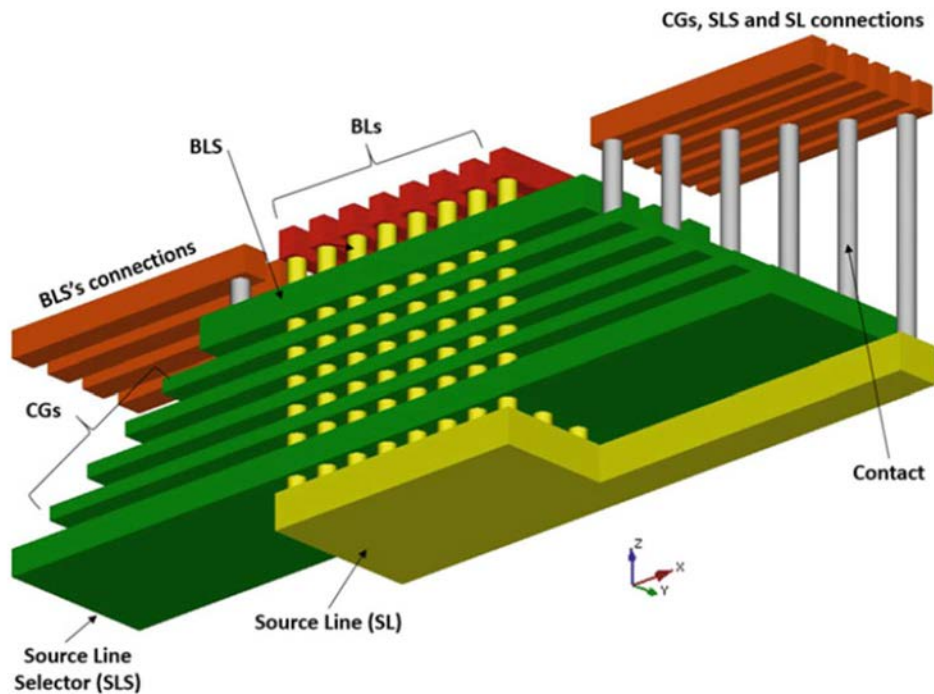


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

Ex. 1015, 109-110. As is traditional in MOSFET transistors, the “source” terminal connects to a low voltage, such as ground. The same holds true in 3D NAND design, and the BiCS architecture includes source line contacts for providing a low voltage (*e.g.*, ground) connection to the memory strings. This is shown in yellow in the figures above.

50. The individual memory cells in a memory string are accessed by word lines that typically extend horizontally and connect to a control gate for a given cell on each memory string. On the periphery of the 3D NAND device, the word lines form a staircase structure, where each subsequent word line protrudes a short distance beyond the word line above it, like a staircase, as shown below in green.

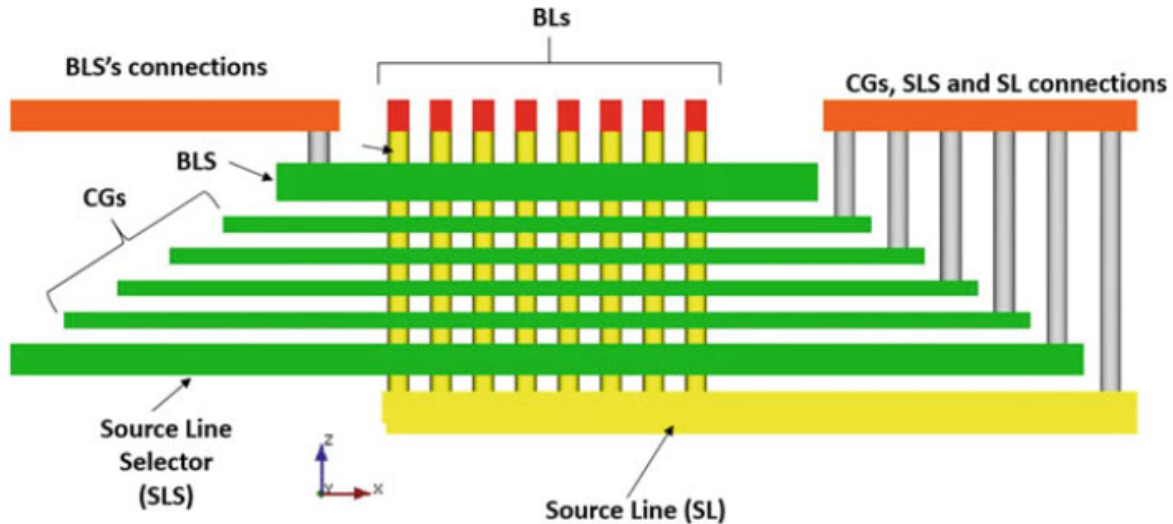


Fig. 4.12 Vertical cross section of BiCS with gate connections

Ex. 1015, 109 (green control gates forming a staircase). As noted, each word line delivers a control signal to a number of memory cells at the same horizontal level in the 3D NAND memory device.

51. The collection of memory cells controlled by a common signal together constitute a “word,” and the control gate is a “word line.” *Id.*; Ex. 1016, 41. The grey columns in the figure above, often referred to as “local contacts,” show how the word lines can be controlled by signals on the top surface of the 3D NAND device. In the context of 3D NAND chips, “local contacts” refer to the electrical connections made within the memory device to link various components such as the word lines and source lines. In facts, local contacts are also often referred to as “vias,” which have been widely known and used in all sorts of semiconductor devices for many decades. These vias create vertical electrical connections between the different

layers within the 3D NAND stack. They are integral to the architecture of semiconductor devices generally, including 3D NAND technology where they enable the functional linkage of stacked memory cells across multiple layers. Note that these local contacts can be of various lengths – some long and some very short. For example, the local contacts (the grey columns in the figure above) that connect to the word lines located near the top of the memory stack are very short while the grey column that connect to the source line is much longer. Where local contacts are connecting an existing vertical structure, such as a memory string or slit, the local contacts tend to be relative short. I note in this regard that the '378 patent gives examples of long local contacts (*e.g.*, an entire TAC) and short local contacts (*e.g.*, atop channel structures and slits). See Ex. 1001, 11:16-30.

52. A variety of modifications to the BiCS architecture were known, including the use of slit structures to serve as source line contacts for the NAND strings. Exemplary slit structures are shown in purple below. These particular slit structures function as contacts for connecting to the source (which may be shared by some, or all, memory strings) located on the bottom of the 3D NAND device.

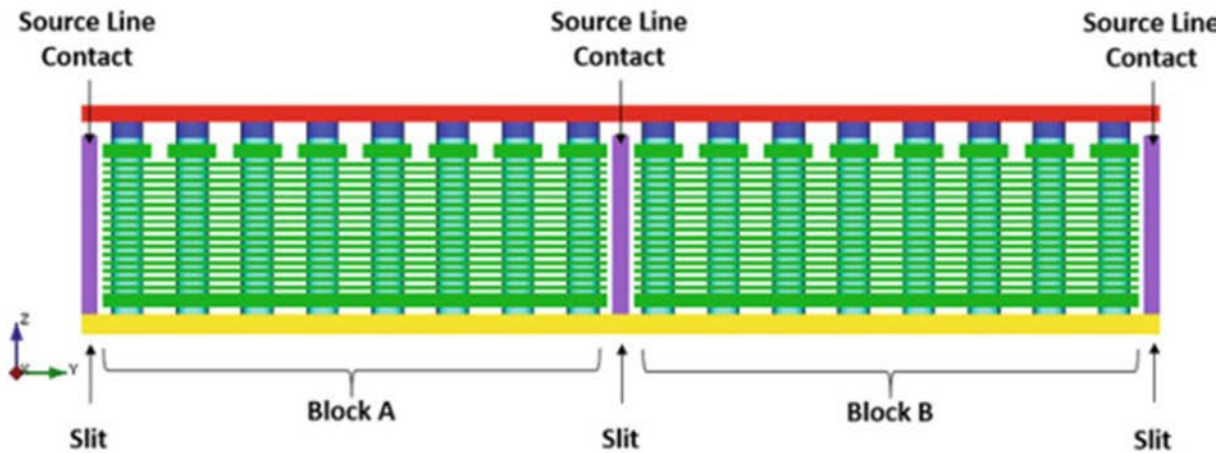


Fig. 6.8 Side view of Fig. 6.7

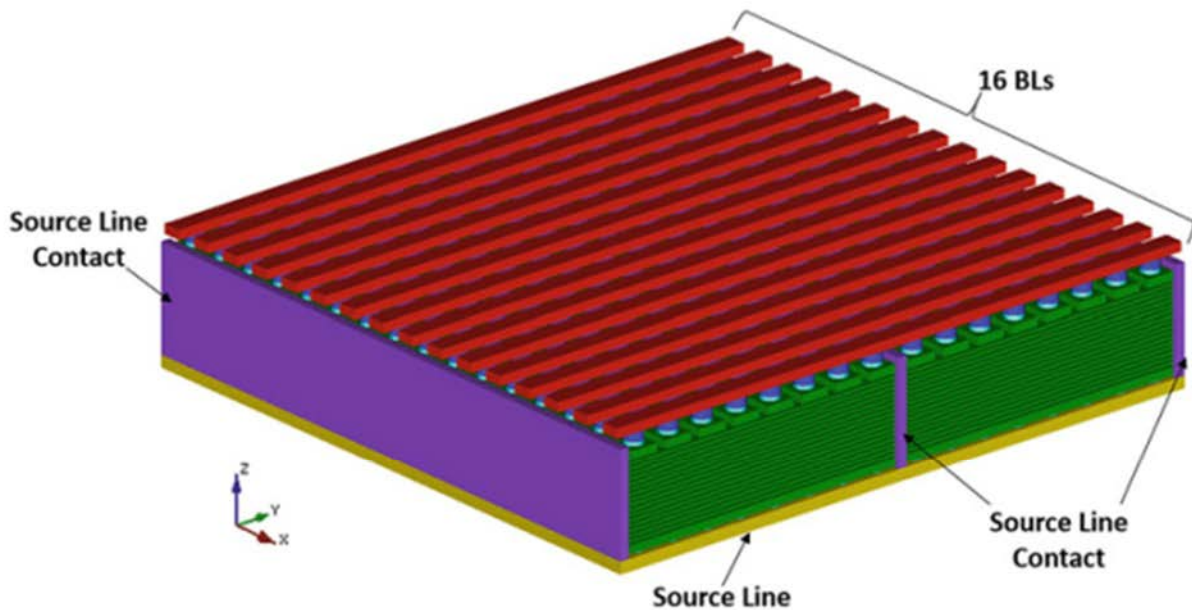


Fig. 6.7 Array slits

Ex. 1015, 185.

53. In both figures above, gaps are shown between the various structures. In actual 3D NAND memory devices, these “gaps” are not empty space; rather, they are filled with insulating material (known as “dielectric” material). Among other

things, dielectrics serve to isolate electrical signals and prevent one conductive structure from interfering with another other. Another function performed by the dielectric is mechanical support to prevent the other structures from collapsing.

54. Well before the effective filing date of the '378 patent, companies (including Micron) had developed various techniques for manufacturing 3D NAND flash memory, many of which leveraged fabrication principles and materials that had been in use generally in the semiconductor manufacturing industry for decades.

55. The fabrication of 3D NAND memory chips involves etching techniques to construct vertical, high-density storage architectures. These etching processes, fundamental to semiconductor manufacturing, have been well established prior to 2018 but have been adapted for 3D NAND. Here are just a few examples of etching processes used for 3D NAND. Channel hole etching which typically makes use of a dry etching process, e.g., deep reactive ion etching (DRIE) to create vertical channels through the NAND stack. DRIE was developed in the mid-1990s, allows for etching with high aspect ratios, essential for the vertical structures in 3D NAND. Staircase etching involves sequential etching steps to create a staircase-like structure for accessing word lines across each memory layer. This process leverages standard lithographic and etching techniques known long before 2018, adapted to create the precise, repetitive structures needed for multi-layer access. Hard-mask etching process, well-known long before 2018, involves depositing a durable

material like nitrides which is then patterned using photolithography to serve as a mask. The hard mask protects underlying layers during subsequent etching. Selective etching is used to remove specific materials without damaging others by using different chemistries in plasma to target certain layers of materials, again was well-known long before 2018. Spacer etching which involves depositing and then partially removing the material developed to define narrow, uniform spacers (gaps) for cell isolation. Spacer etching processes was developed for lightly-doped drain (LDD) MOSFETs back in the 1980's and adapted for 3D NAND manufacturing process. Each of these processes originates from fundamental techniques known in semiconductor manufacturing well before 2018, adapted for the advanced architecture of 3D NAND.

56. Stacking multiple chips, also known as 3D integration, was just one of many advancements in semiconductor technology that have happened over the years. The concept of 3D integration should not be confused with 3D NAND. Although 3D integration has application to 3D NAND chips, the concept of vertically stacking multiple dies/chips predates 3D NAND by many years and has been used extensively in a variety of chip technologies. This method significantly enhances device performance and functionality while conserving space, addressing the limitations faced by traditional planar scaling methods. Naturally, when stacking multiple dies on top of one another, via structures (also called through-silicon vias

(TSVs) or through-array contacts (TACs)) were implemented to provide connections between different chips in the stack. The concept of TACs predates 2018 and was developed to meet the growing demands for increased functionality and higher performance without expanding the chip's footprint. These vertical connections are essential for shortening the path electrical signals must travel compared to traditional methods like wire bonding or flip-chip techniques. By reducing the length of interconnects, TACs enhance signal speed and reduce power consumption. Before 2018, the semiconductor industry recognized the potential of through-array contacts to mitigate the slowing pace of enhancements afforded by Moore's Law due to physical and economic limits.

57. In summary, techniques for manufacturing 3D NAND memory devices were well-known in the art before the '378 patent's effective filing date.

VII. THE '378 PATENT

A. Effective Filing Date

58. I understand that the application leading to the '378 patent was filed on July 27, 2018.

59. Based on my review of the '378 patent, I note that it also references a PCT application on its face, which was filed May 3, 2018.

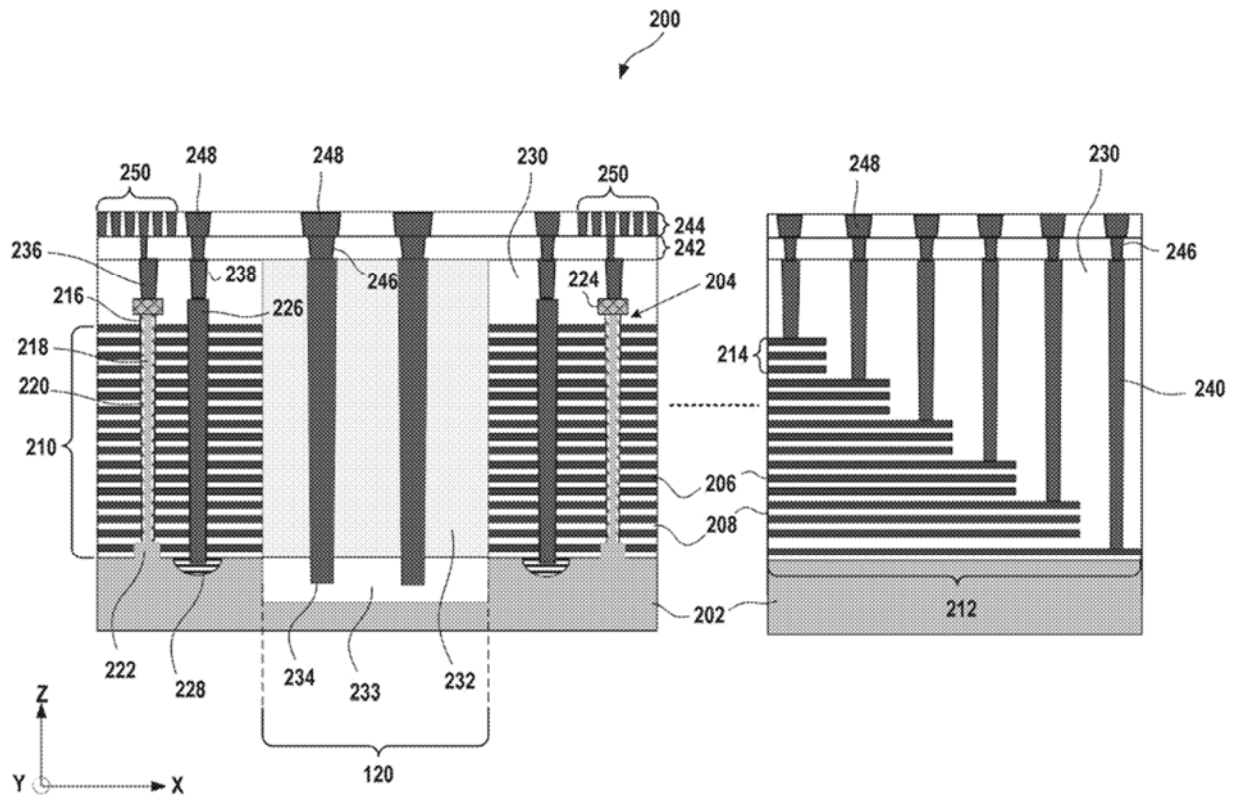
60. For purposes of this declaration, I have been asked to assume that May 3, 2018 is the effective filing date of the '378 patent. My opinions in this declaration

were formed from the perspective of a POSITA as of May 3, 2018, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the '378 patent and the prior art.

B. Overview

61. The '378 patent relates to “three-dimensional (3D) memory devices.” Ex. 1001, 1:13-16. The title of the '378 Patent is “Through Array Contact (TAC) For Three-Dimensional Memory Devices.” In particular, the specification describes and illustrates various “[e]mbodiments of interconnect structures of a three-dimensional (3D) memory device and method[s] for forming the interconnect structures.” *Id.*, Abstract.

62. To begin, as seen in Fig. 2 of the '378 patent below, the specification describes and illustrates a “3D memory device 200” with an overall 3D NAND architecture similar to that of the conventional BiCS architecture (*e.g.*, vertical memory strings, staircase region for word line access, etc.) that I discussed previously in the Technology Background.



Ex. 1001, Fig. 2.

63. The alleged point of novelty in the '378 patent is a 3D memory device containing “vertical interconnects” that are located between a “stacked array device” (such as “3D memory device 200”) and a “peripheral device.” Ex. 1001, 5:32-59. In other words, the TACs may provide connections between separately fabricated chips (e.g., a memory chip and a controller chip) that are physically stacked on top of each other to form an overall 3D NAND memory device. *Id.*, 11:5-9. The '378 patent refers to these vertical interconnects as “through array contacts” (“TACs”). *Id.*, 1:51-55; *see also id.*, Title (“Through Array Contact (TAC) For Three-Dimensional Memory Devices”). In Fig. 2 above, element 234 is a TAC. *Id.*, 10:57-

59. According to the specification, “[t]he interconnect structures allow contacts to various memory array structures (e.g., NAND strings, gate line slits, word lines, etc.) to be fabricated in a limited number of steps (e.g., in a single step or in two steps), thereby reducing the process complexity and manufacturing cost.” *Id.*, 5:35-40. The cross-sectional profile of the TACs resembles that of a via and tapers slightly from top to bottom, as is common with semiconductor etch processes, which have long been well-known to POSITAs.

64. “In some embodiments, TACs 234 can provide electrical connections between 3D memory device 200 and the peripheral device (e.g., on a CMOS chip; not shown in FIG. 2).” Ex. 1001, 11:3-9. “Each TAC 234 can extend through the entire thickness of dielectric structure 232 and extend through at least a portion of STI structure 233 in a substrate 202.” *Id.*, 10:67-11:2. Given that the TACs may “provide electrical connections,” it is unsurprising that the specification teaches that “[e]ach TAC 234 is filled with conductor materials, including, but not limited to, W, Co, Cu, Al, doped Si, silicides, or any combination thereof.” *Id.*, 11:9-12. All of these materials were well-known to POSITAs for their conductive properties and had been used long before the ’378 patent.

C. Prosecution History

65. As noted above, I have reviewed the ’378 patent’s file history. I focus my discussion of the file history as it relates to the challenged claims. In this regard,

the file history is quite short. In particular, in the first Office Action, the Examiner indicated that then-pending dependent claim 17 would be allowable if rewritten in independent form. Ex. 1002, 536. The Applicant did just this. *Id.*, 570 (“Applicant thanks the Examiner for indicating the allowability of claims 2 and 17 if they were rewritten in independent form including all limitations of the base claim and any intervening claims. Applicant has amended claims 1 and 16 to respectively recite features of claims 2 and 17.”). Thus, the limitations of claim 17 were incorporated into independent claim 16, which was subsequently renumbered to be independent claim 15 in the as-issued ’378 patent. *Id.*, 590 (showing renumbering). Challenged claims 16-17 and 19-20 all depend from independent claim 15. Thus, all challenged claims resulted from a First Action allowance.

66. The limitations of dependent claim 17 that were incorporated into the independent claim to obtain allowance were: *a staircase structure ..., a word line contact disposed on each conductor layer of the staircase structure*, and *a local contact disposed on each channel structure and slit structure*. Ex. 1002, 110. As I discuss in the Technology Background, these three elements were all well-known to POSITAs and conventional in 3D NAND devices by 2018.

67. I note that other claims in the ’378 application (none of which I analyze in this declaration) were rejected by the Examiner as obvious in view of U.S. Pat.

No. 9,620,512 (“Nishikawa,” Ex. 1017) combined with U.S. Pat. Publ. No. 2016/0056188 (“the 188 Publication,” Ex. 1018). Ex. 1002, 530.

68. The prior art references I discuss in this declaration are not cumulative of those that the Examiner discussed. I note that U.S. Pub. 2017/0179026 (Ex. 1005, “Toyama”) was cited in an IDS, but was not used as the basis for a rejection or otherwise discussed by the Examiner in the file history. And neither Mushiga nor Makala was cited or discussed by the Examiner or the applicant during prosecution at all. And with respect to Nishikawa, the Examiner found that it did **not** disclose *through array contacts*, instead relying on the 188 Publication. Ex. 1002, 531 (“Nishikawa appears to be silent as to, but does not preclude, the elements of one or more through array contacts (TACs) extending vertically through the dielectric structure and the isolation region. [The 188 Publication] teaches the elements of: one or more through array contacts (TACs) (83) extending vertically through the dielectric structure and the isolation region [0067]. It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the device taught by Nishikawa with the aforementioned elements taught by [the 188 Publication]”). But the 188 Publication is titled “IMAGE SENSOR HAVING SHIELDING STRUCTURE” and does not even relate to memory, let alone a 3D NAND memory device. Ex. 1018, Abstract; *see also id.*, [0028] (“Referring to FIGS. 1A to 1C, the image sensor 10A includes a pixel array PA,

peripheral circuit areas PCA, an interface areas IA, and a shielding structure 50 formed in the interface areas IA.”), [0097] (“FIG. 10A is a schematic block diagram for describing a camera system including one of the image sensors”). By contrast, the primary references in this Petition (Toyama and Mushiga) both disclose or render obvious ***all*** claim elements, including the claimed *through array contacts*.

D. Claims

69. For reference, the challenged claims (*i.e.*, claims 15-17 and 19-20) of the '378 patent are reproduced below, with identifiers added for reference:

15. A three-dimensional (3D) memory device, comprising:

[A] a substrate with an isolation structure;

[B] an alternating conductor/dielectric layer stack disposed on the substrate;

[C] a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

[D] channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;

[E] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

[F] a word line contact disposed on the conductor layer of the each level;

[G] local contacts disposed on the channel structures and the slit structures; and;

[H] through array contacts (TACs) extending vertically through the dielectric and the isolation structures.

16. The 3D memory device of claim 15, wherein the dielectric structure abuts a sidewall of each TAC of the TACs.

17. The 3D memory device of claim 15, wherein the dielectric structure comprises a through array contact region of the 3D memory device.

19. The 3D memory device of claim 15, wherein the dielectric material comprises silicon oxide.

20. The 3D memory device of claim 15, wherein the TACs comprise a conductive material.

VIII. CLAIM CONSTRUCTION

70. I am not a legal expert or an attorney and offer no opinions on the law.

I understand that claim construction is a matter of law. However, I have been

informed by counsel of the legal standards that apply to claim construction in an *inter partes* review, and I have applied them in forming my opinions. I understand that during an *inter partes* review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

71. I have been informed that the words of a claim are generally given their plain and ordinary meaning that the term or phrase would have to POSITA at the time of the invention in view of the surrounding claim language, the specification and the file history (collectively, the “intrinsic evidence” or “intrinsic record”).

72. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the “extrinsic evidence” or the “extrinsic record”), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

73. In my opinion, the challenged claims do not require further construction and can be afforded their plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration.

IX. UNPATENTABILITY ANALYSIS

74. For the reasons I explain in greater detail below, it is my opinion that as of the effective filing date of the '378 patent, claims 15-17 and 19-20 of the '378 patent are unpatentable as obvious over the prior art discussed in this declaration.

A. Overview of the Prior Art

75. The following paragraphs provide an overview of the main prior art references I discuss throughout this declaration.

1. Toyama

76. Toyama (U.S. Pub. 2017/0179026) is titled “Through-Memory-Level Via Structures for a Three-Dimensional Memory Device.” Ex. 1005. Toyama was filed September 19, 2016, and issued on June 22, 2017. *Id.* Toyama claims priority to December 22, 2015. *Id.* I am informed that Toyama is prior art under at least 35 U.S.C. §102(a)(1) and §102(a)(2).

77. Toyama is generally directed to “[a] three dimensional NAND memory device” that includes conventional 3D NAND memory features such as “an alternating stack of word lines and insulating layers located over the word line driver devices” and “a plurality of memory stack structures extending through the alternating stack.” Ex. 1005, Abstract. Toyama also discloses “through-memory-level via structures” that “extend through a through-memory-level via region located between a staircase region of the first memory block and a staircase region of another memory block.” *Id.*

78. Toyama is a lengthy reference, including 76 figures (many with sub-parts) and over 60 columns of text. Much of Toyama describes the manufacturing processes and techniques used to form the 3D NAND memory structures it

describes. I will highlight here only two of Toyama's embodiments, which are the focus of my substantive invalidity analysis. The first is Toyama's "first exemplary structure," which is depicted in Figs. 1-17, and described in the accompanying text. *See generally* Ex. 1005, [0014]-[0048], [0163]-[0260]. The second is Toyama's "second modification to fourth exemplary structure," which I refer to hereafter as Toyama's "Second Modification" for shorthand. Toyama's Second Modification is depicted in Figs. 44-49, and described in the accompanying text. *Id.*, [0093]-[0103], [0332]-[0342]. I note that other figures and text are also relevant as some of Toyama's disclosure and teachings are generally applicable to all embodiments, and certain aspects of one embodiment are simply expanded upon by other embodiments. Each of Toyama's first exemplary structure and Second Modification independently discloses, or renders obvious, all of the challenged claims for the reasons I discuss in Section IX.B.

79. ***First Exemplary Structure.*** Many of the features of Toyama's first exemplary structure (*e.g.*, alternating layers of conductor/dielectric, memory array region 100 containing memory strings that extend through the stack of alternating conductors 146, 246 and dielectrics 132, 232, a staircase structure, word line contacts 86 on the staircase structure, etc.) can be seen in the cross-sectional diagram of Fig. 17C below.

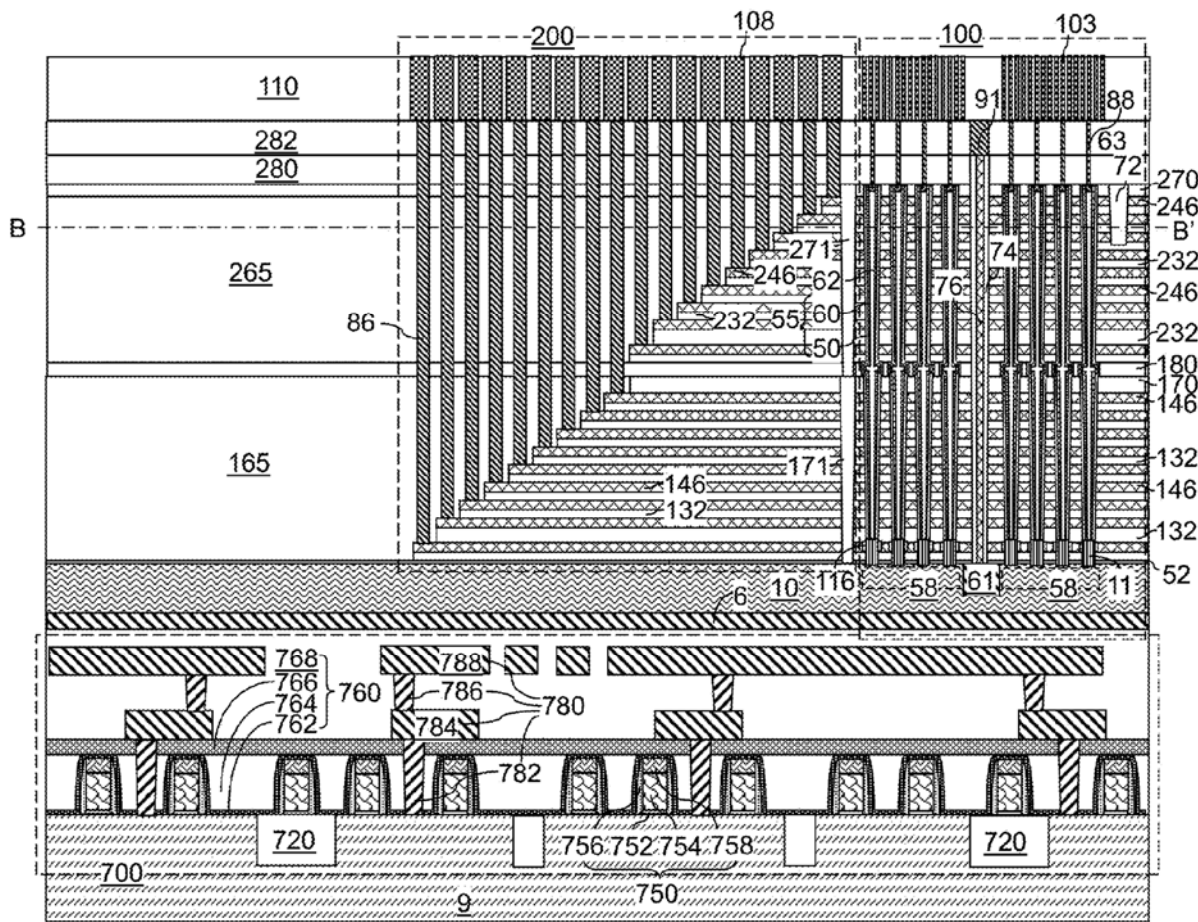


FIG. 17C

Ex. 1005, Fig. 17C.

80. And, like the '378 patent's *through array contacts*, Toyama's first exemplary embodiment discloses 3D NAND memory devices with "through-memory-level via structures," which are vias that extend through the memory array to provide electrical connection to "peripheral" devices. Ex. 1005, [0164] (discussing "peripheral device region 700" located underneath the "memory-level assembly").

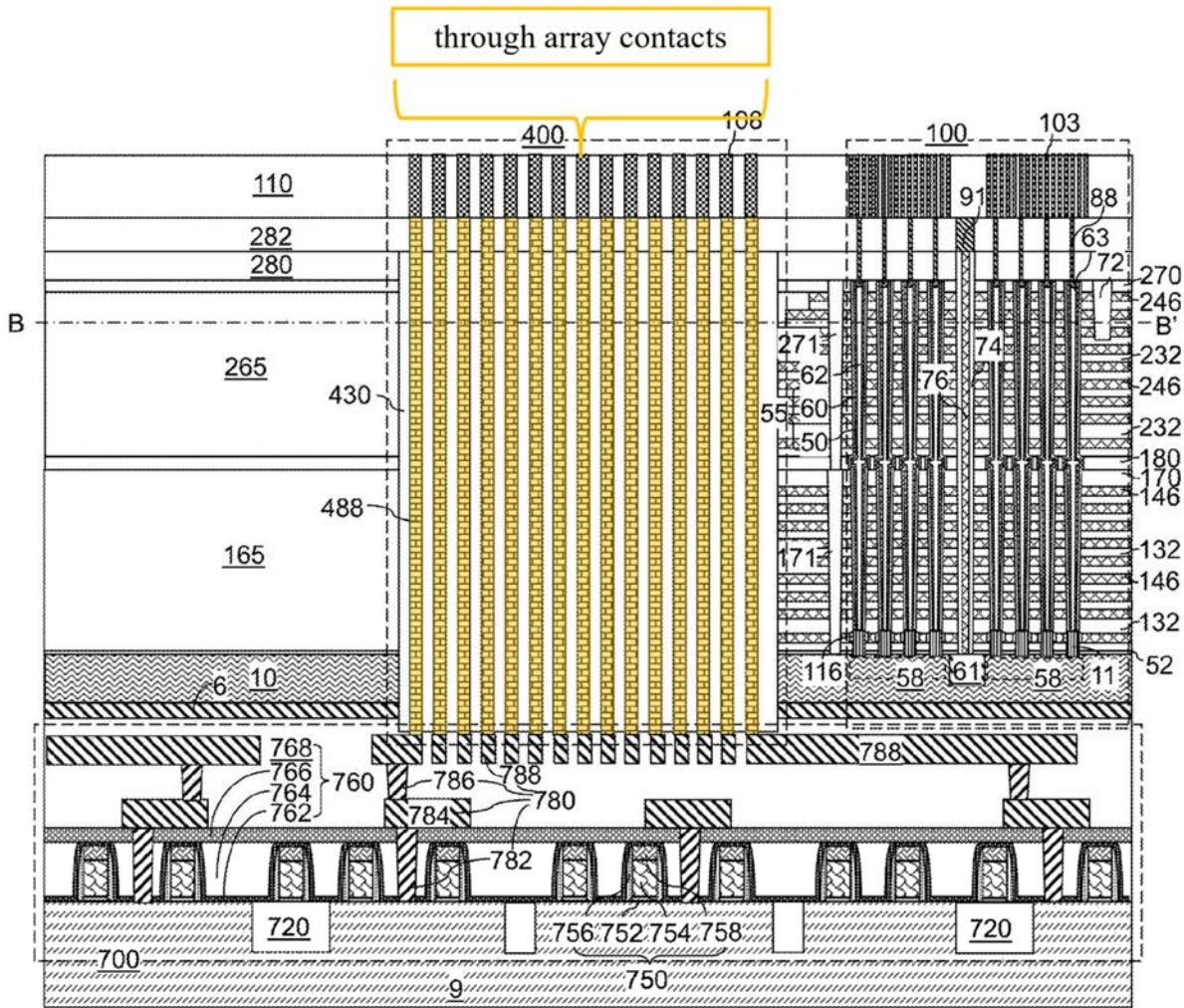


FIG. 17A

Id., Fig. 17A (annotated).

81. **Second Embodiment.** Many of the features of Toyama's Second Embodiment (*e.g.*, alternating layers of conductor/dielectric, memory array region 100 containing memory strings that extend through the stack of alternating conductors, etc.) can be seen in the cross-sectional diagram of the 3D NAND memory device in Fig. 49 below. And, like the '378 patent's *through array contacts*, Toyama's Second Embodiment discloses "through-memory-level via structures

676” (highlighted in yellow below) that extend through the memory array to provide electrical connection to “peripheral” devices. Ex. 1005, [0341], [0164] (discussing “peripheral device region 700” located underneath the “memory-level assembly”).

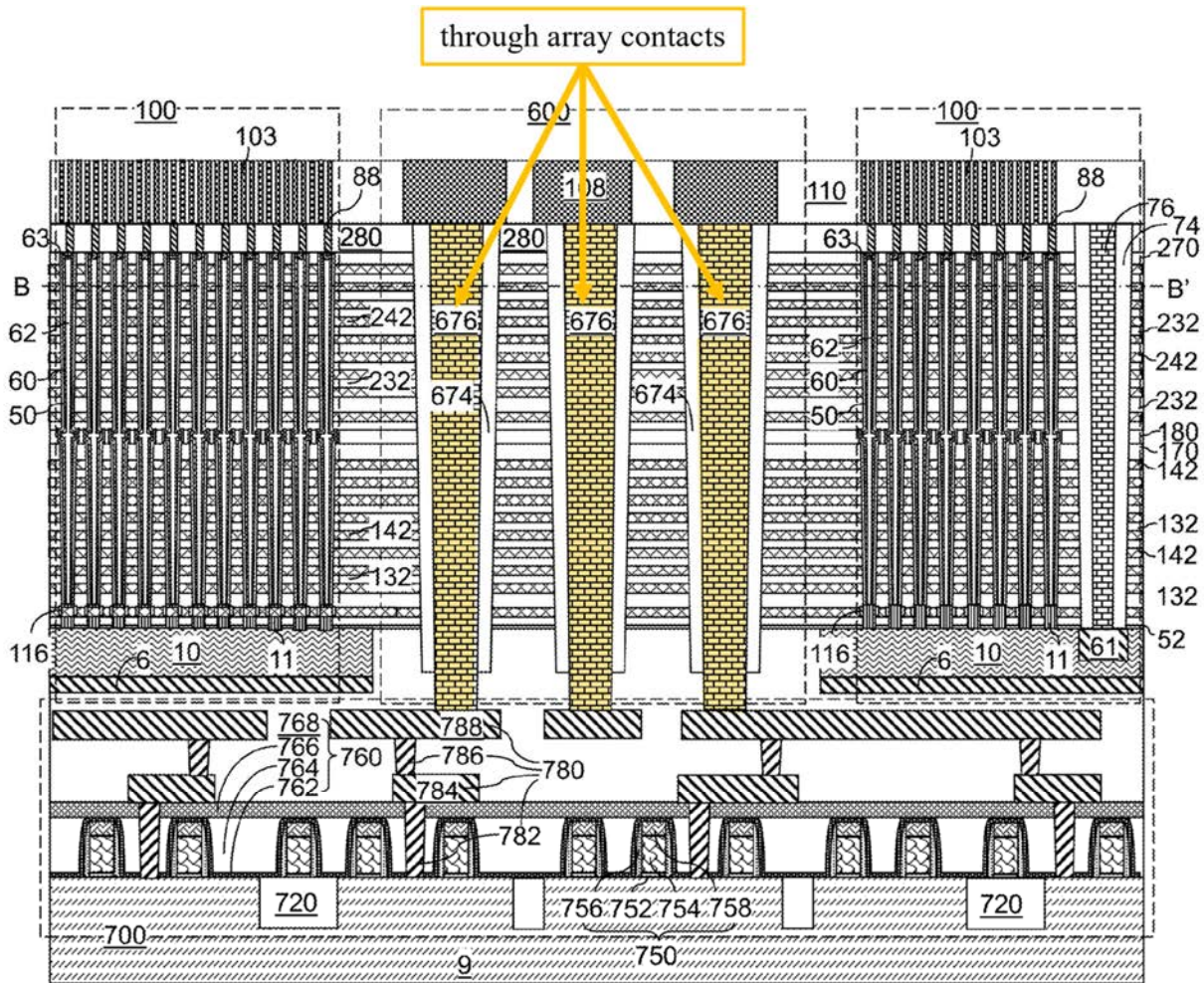


FIG. 49

Id., Fig. 49.

82. The last observation I will make here is that many of Toyama’s figures build on one another to illustrate various steps in the fabrication process (*e.g.*, one figure will show an etch step to create a cavity and the next figure will show the

cavity being filled with a dielectric or conductor). This is helpful to know, especially when initially reviewing Toyama.

2. Mushiga

83. Mushiga (U.S. Pat. No. 10,354,980) is titled “Three-Dimensional Memory Device Containing Bonded Chip Assembly with Through-Substrate Via Structures and Method of Making the Same.” Ex. 1006. Mushiga was filed March 22, 2018, and issued on July 16, 2019. *Id.* I am informed that Mushiga is prior art under at least 35 U.S.C. §102(a)(2).

84. As illustrated in Fig. 11 below, Mushiga discloses conventional features of 3D NAND memory devices, including alternating layers of conductor/dielectric, memory strings that extending through the stack of alternating conductors/dielectrics, a staircase structure, word line contacts on the staircase structure, slit structures, and various local contacts.

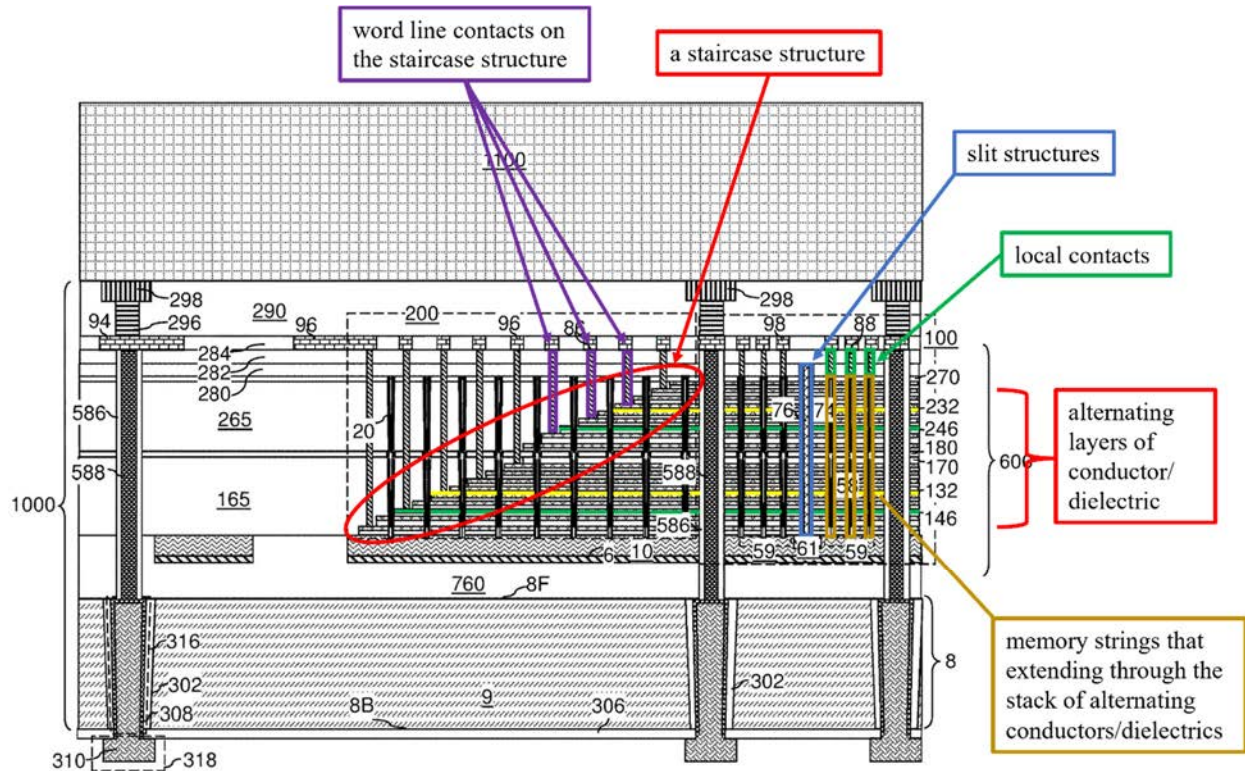


FIG. 11

Ex. 1006, Fig. 11.

85. Mushiga is also concerned with bonding together multiple semiconductor chips. Ex. 1006, Abstract. “The multiple semiconductor chips include a logic chip and multiple memory chips.” *Id.* In other words, Mushiga discloses stacking multiple chips on top of one another and bonding them together to form a singular memory device with greater memory capacity. Mushiga calls this a “chip assembly structure.” *Id.* 5:49. In at least some instances, the logic chip (*e.g.*, a memory controller) is located on the bottom of the stack of chips. *Id.*, 5:51-54. Because the logic chip (also called a “peripheral” circuit in Mushiga) needs to access all of the overlying 3D NAND memory chips, Mushiga discloses electrical

connections (which it calls “through-substrate via structures”) that go all the way through the memory chips. *Id.*, 5:31-57. Mushiga’s “through-substrate via structures” are the claimed TACs (the alleged point-of-novelty) in the ’378 patent.

3. Makala

86. Makala (U.S. Pat. No. 10,262,945) is titled “Three-Dimensional Array Device Having a Metal Containing Barrier and Method of Making Thereof.” Ex. 1007. Makala was filed on April 28, 2017 and issued April 16, 2019. *Id.* Makala claims priority to November 28, 2016. *Id.* I am informed that Makala is prior art under at least 35 U.S.C. § 102(a)(2).

87. As reflected in its title, Makala is directed to 3D memory structures and related manufacturing methods. Many of the conventional 3D memory characteristics and structures (*e.g.*, staircase region, memory strings, etc.) are disclosed in Makala, as can be seen in Makala Fig. 16 below.

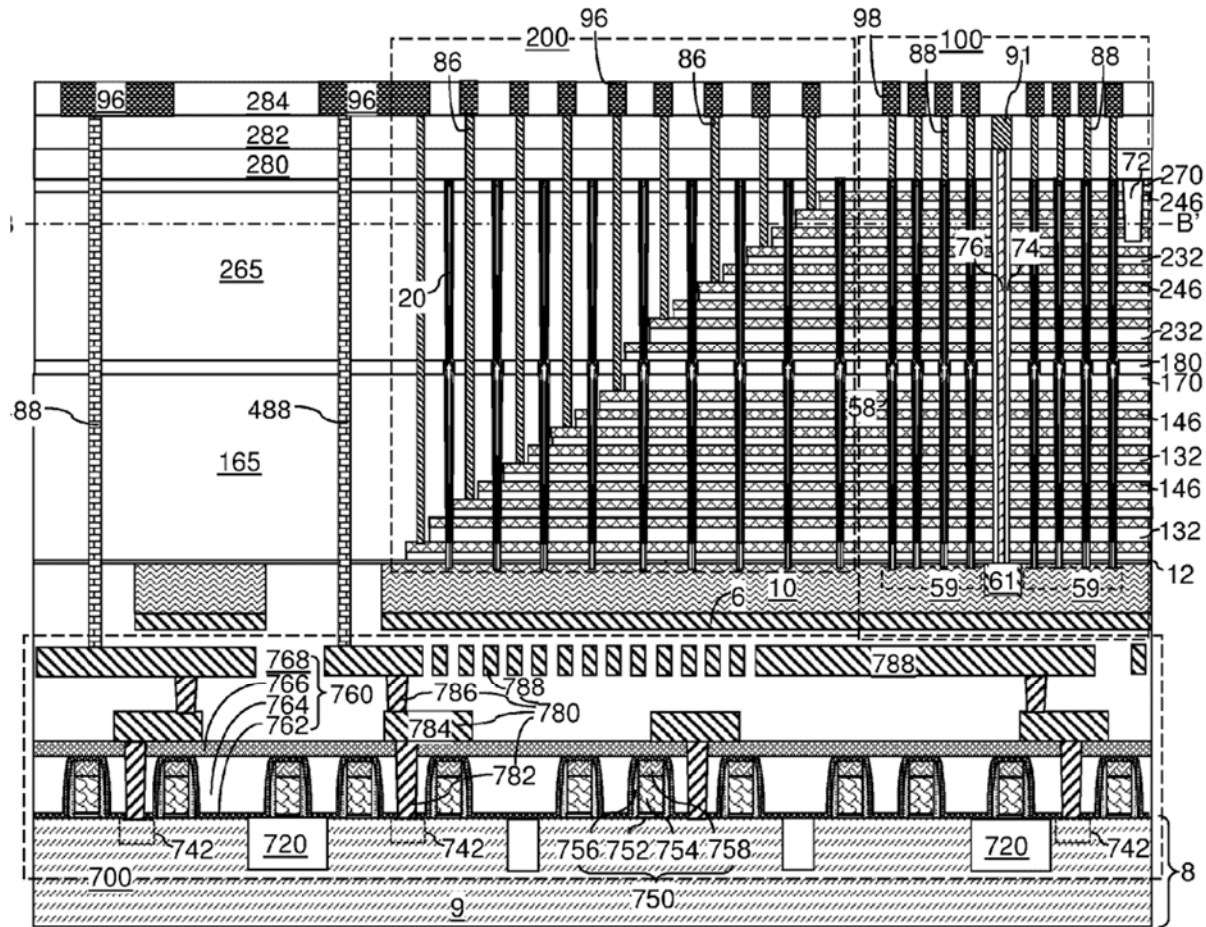


FIG. 16

Ex. 1007, Fig. 16.

88. Indeed, Fig. 16 illustrates a 3D memory device with conventional elements such as alternating conductor/dielectric layer stack, memory channel structures extending through the alternating stack, word line contacts disposed on the staircase structure, a slit structure, and local contacts.

89. The primary reason I discuss Makala (which is only used as a secondary reference in combination with Mushiga) in Section IX.D.1 is for Makala's disclosure

of *local contacts disposed on the slit structures*. As such, I call attention here to Makala's "source connection via structures 91." Makala explains that "[a] source connection via structure 91 can extend through the contact level dielectric layers (280, 282) to provide electrical connection to the laterally-elongated contact via structures 76." Ex. 1007, 33:40-43. Thus, source connection via structures 91 are the claimed *local contacts disposed on the slit structures*.

B. Ground 1: Toyama in View of the Knowledge of a POSITA

90. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Toyama's "second modification of the fourth exemplary structure" (which I refer to as Toyama's "Second Modification" for shorthand) and its first exemplary structure each independently render claims 15-17 and 19-20 of the '378 patent obvious. I note at the outset that Toyama's Second Modification and its first exemplary structure share some commonalities and I sometimes analyze them together where appropriate (*e.g.*, where Toyama contains general disclosure that applies equally to both embodiments), but frequently provide sub-headings for each and analyze them separately.

1. Claim 15

[15.Pre] "A three-dimensional (3D) memory device, comprising:"

91. I offer no opinion on whether the preamble is or is not limiting. However, if the preamble is considered to be a limitation, my opinion is that Toyama

discloses it. Indeed, the first sentence of Toyama’s detailed description states that “the present disclosure is directed to three-dimensional non-volatile memory devices, such as vertical NAND strings and other three-dimensional devices, and methods of making the same.” Ex. 1005, [0156]. This disclosure applies to both Toyama’s first exemplary embodiment and its Second Embodiment.

[15.A] “a substrate with an isolation structure;”

92. For ease of analysis, I separate this limitation into two sub-parts.

[15.A.i] “a substrate”

93. Toyama’s first exemplary structure and Second Embodiment both have a *substrate*. As a preliminary point, the ’378 patent explains that a “substrate” is “a material onto which subsequent material layers are added, or otherwise ‘disposed.’” Ex. 1001, 4:41-43. The ’378 patent further states that “[a] substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow.” *Id.*, 5:4-6. This is reflected in certain embodiments in the ’378 specification in which “the array device and a peripheral device are formed on different substrates.” *Id.*, 5:40-45.

i. First Exemplary Structure

94. In Toyama’s first exemplary structure, the *substrate* is the “planar semiconductor material layer” 10, highlighted in Fig. 17A below. *See, e.g.*, Ex. 1005, [0169]-[0170].

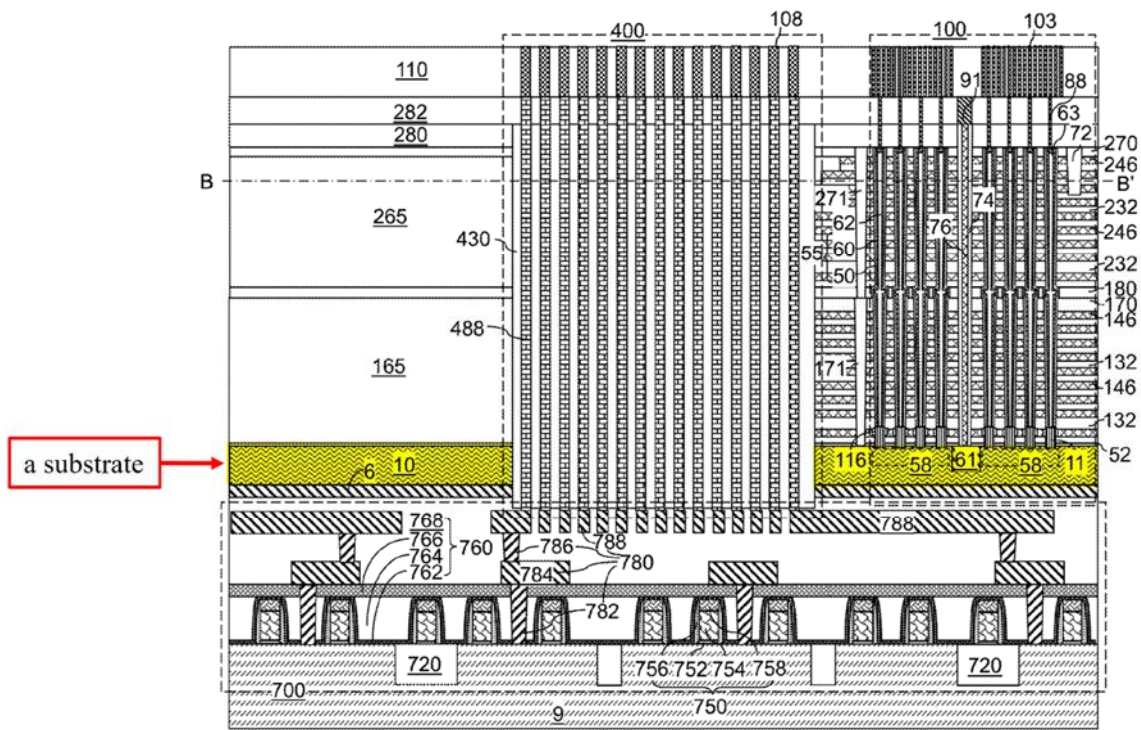


FIG. 17A

Id., Fig. 17A (annotated). Toyama Figs. 2 through 17 depict how various layers are disposed on top of “planar semiconductor material layer 10.” As one example, Toyama notes that “[a]n alternating plurality of the first insulating layers 132 and first sacrificial material layers 142 [are] formed over the planar semiconductor material layer 10.” *Id.*, [0173]. As another example, Toyama explains that “at least one retro-stepped dielectric material portion (165, 265) can be formed over the staircase regions on the at least one alternating stack (132, 142, 232, 242).” *Id.*, [0196]. Because the “planar semiconductor material layer 10” in Toyama is a material onto which other materials and layers are added, it is *a substrate*.

ii. Second Modification

95. Although the cites above are for Toyama's "first exemplary structure," Toyama's Second Embodiment likewise includes a "planar semiconductor material layer 10" as shown in Fig. 49 below, and thus teaches this limitation for the same reason.

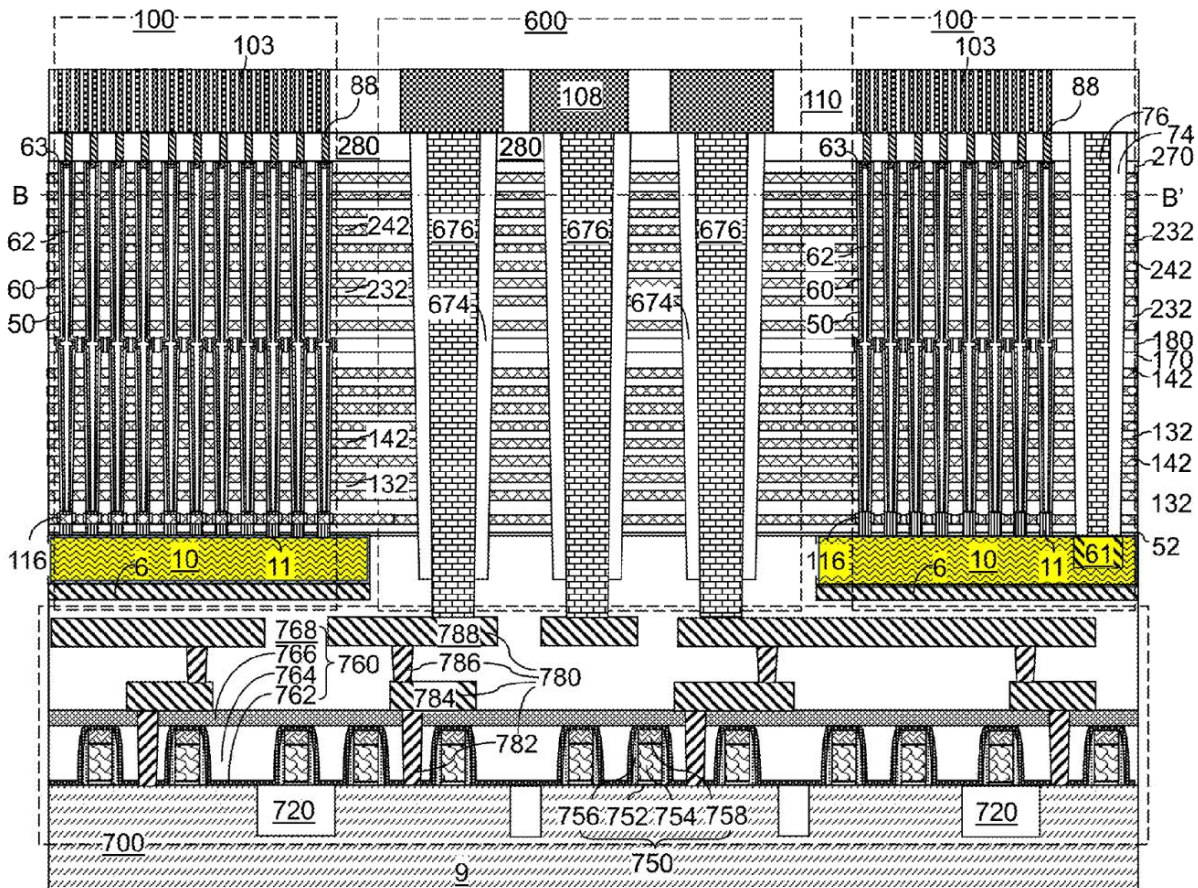


FIG. 49

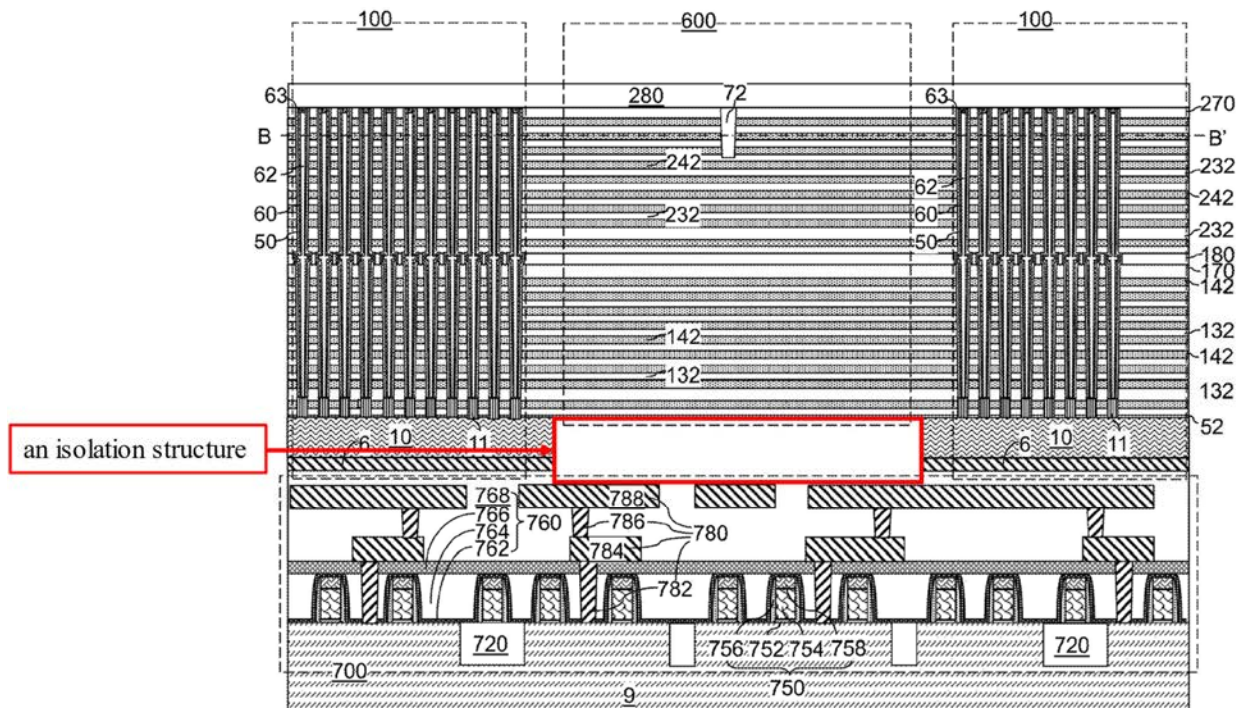
Ex. 1005, Fig. 49 (annotated).

[15.A.ii] “... with an isolation structure”

96. Both Toyama’s Second Modification and Toyama’s first exemplary structure teach this limitation.

i. Second Modification

97. Toyama’s *isolation structure* in the Second Modification is shown in Fig. 44A below.



Ex. 1005, Fig. 44A (annotated).

98. Toyama describes its Second Modification starting after the alternating stack of conductors/insulators has already been formed. See Ex. 1005, Fig. 44A. Toyama states that the “alternating stack of insulating layers (132, 232) and

dielectric spacer layers (which can be the sacrificial material layers (142, 242)) can be formed over the semiconductor substrate 9 as in previously described embodiments.” *Id.*, [0332]. Toyama further states that its Second Modification “can be formed concurrently with the formation of any of the first, second, and third exemplary structures or modifications thereof.” *Id.*, [0332].

99. A POSITA would have thus understood that Toyama’s Second Modification would use the process described for the third exemplary structure to create “opening 151” and fill it with an insulating material. Ex. 1005, [0277] (“The optional planar conductive material layer 6 and the planar semiconductor material layer 10 may be patterned to form an opening 151 extending through these layers to the underlying insulating layer 760. The opening 151 ... may be filled with another insulating material layer (e.g., a silicon oxide or doped silicate glass) 760.”). The “opening 151” is illustrated in Toyama Fig. 24A below.

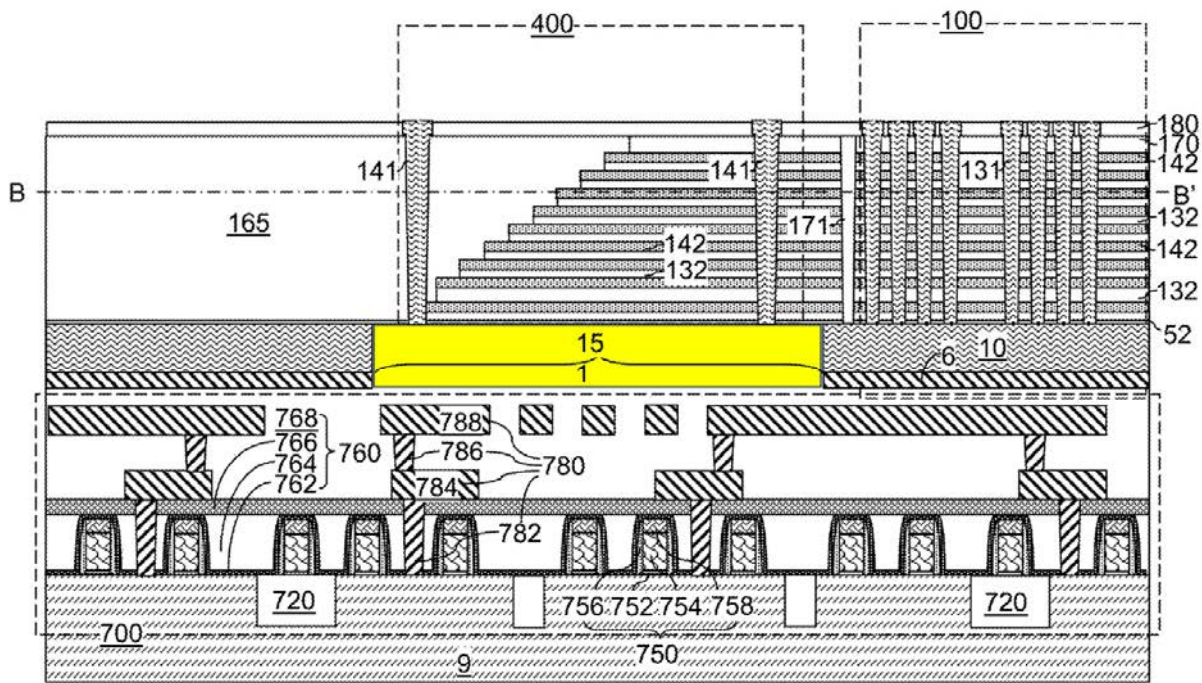


FIG. 24A

Id., Fig. 24A (annotated).

100. A POSITA would therefore have understood that, in the context of Toyama's Second Modification, the insulating material layer that fills "opening 151" is *an isolation structure*. Claim element [15.A] requires not only a *substrate* and an *isolation structure*, but *a substrate with an isolation structure*. That Toyama's *substrate* ("planar semiconductor material layer 10") is *with* its *isolation structure* (the insulating material layer that fills "opening 151") is apparent because Toyama's *isolation structure* (the insulating material layer that fills "opening 151") is formed by removing portions of the substrate and is subsequently formed within the *substrate* ("planar semiconductor material layer 10"). Accordingly, Toyama's

Second Modification teaches *a substrate* (“planar semiconductor material layer 10”) *with an isolation structure* (the insulating material layer that fills “opening 151”).

ii. First Exemplary Structure

101. For Toyama’s first exemplary structure, the lower part of Toyama’s “dielectric fill material portion 430” is *an isolation structure*. See, e.g., Ex. 1005, [0216]. Figs. 10A-12A show the formation of this structure. To begin, “through-memory-level via region 400” includes the staircase structure of layers 132, 142, 232, 242:

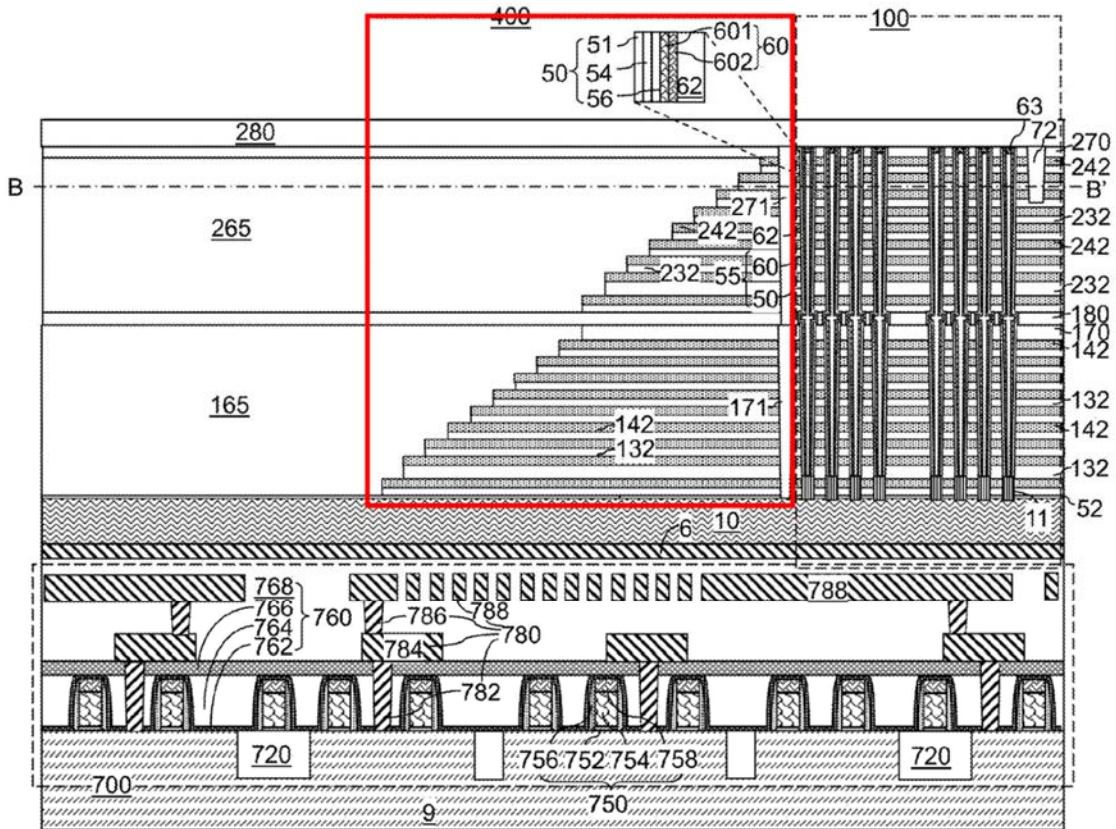


FIG. 10A

Id., Fig. 10A (annotated), [0192]-[0194]. These layers are removed, resulting in “through-memory-level opening 769”:

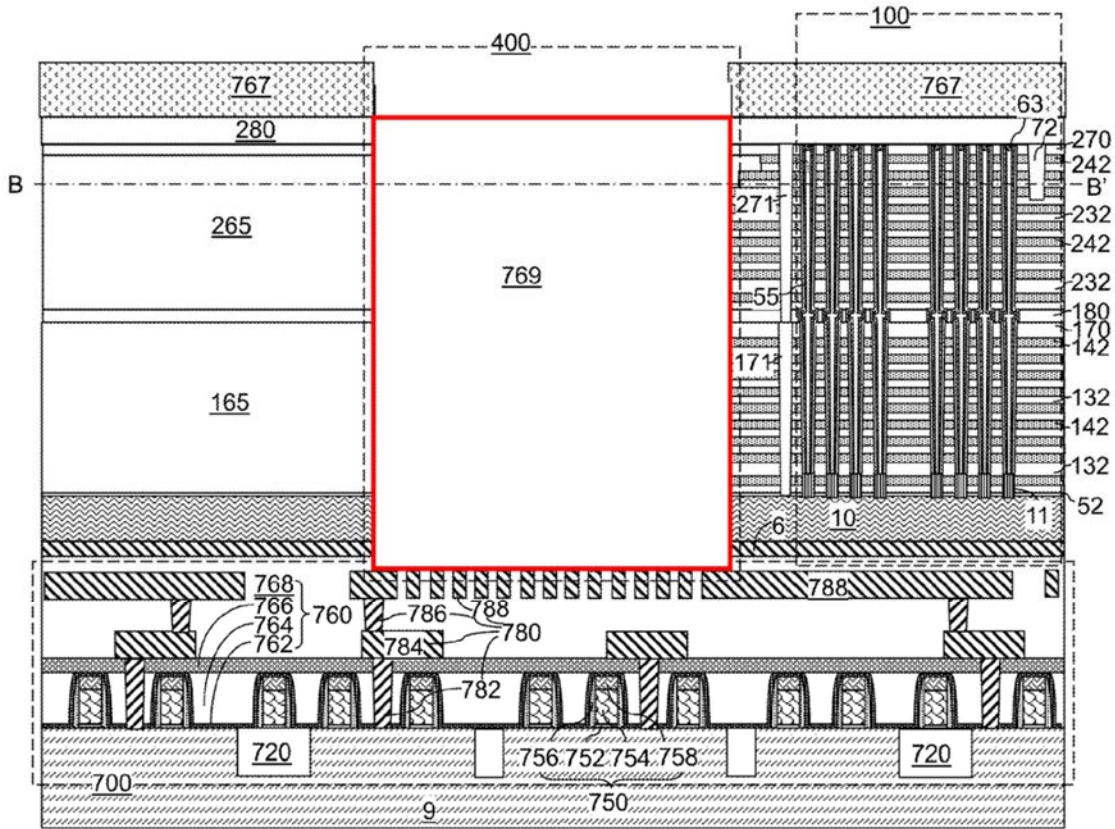


FIG. 11A

Id., Fig. 11A (annotated); [0213]. Next, “opening 769” is filled with a dielectric to form “dielectric fill material portion 430”:

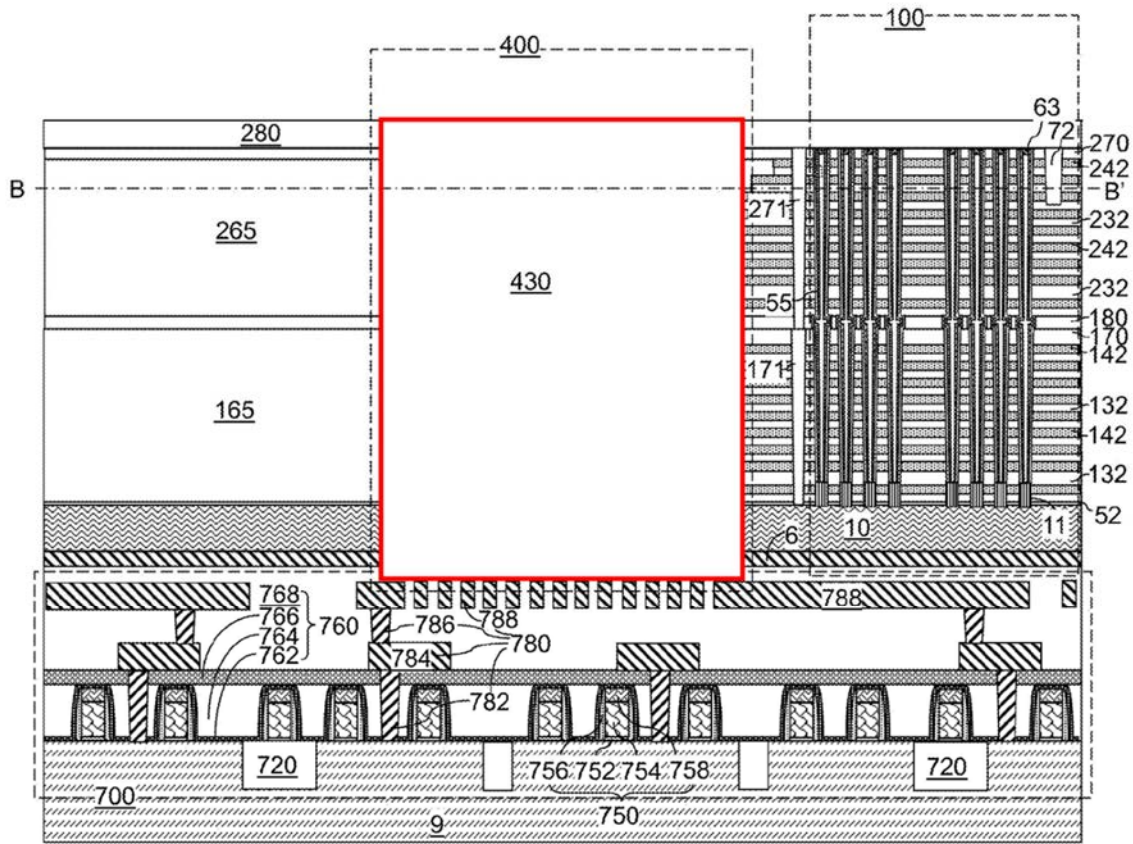
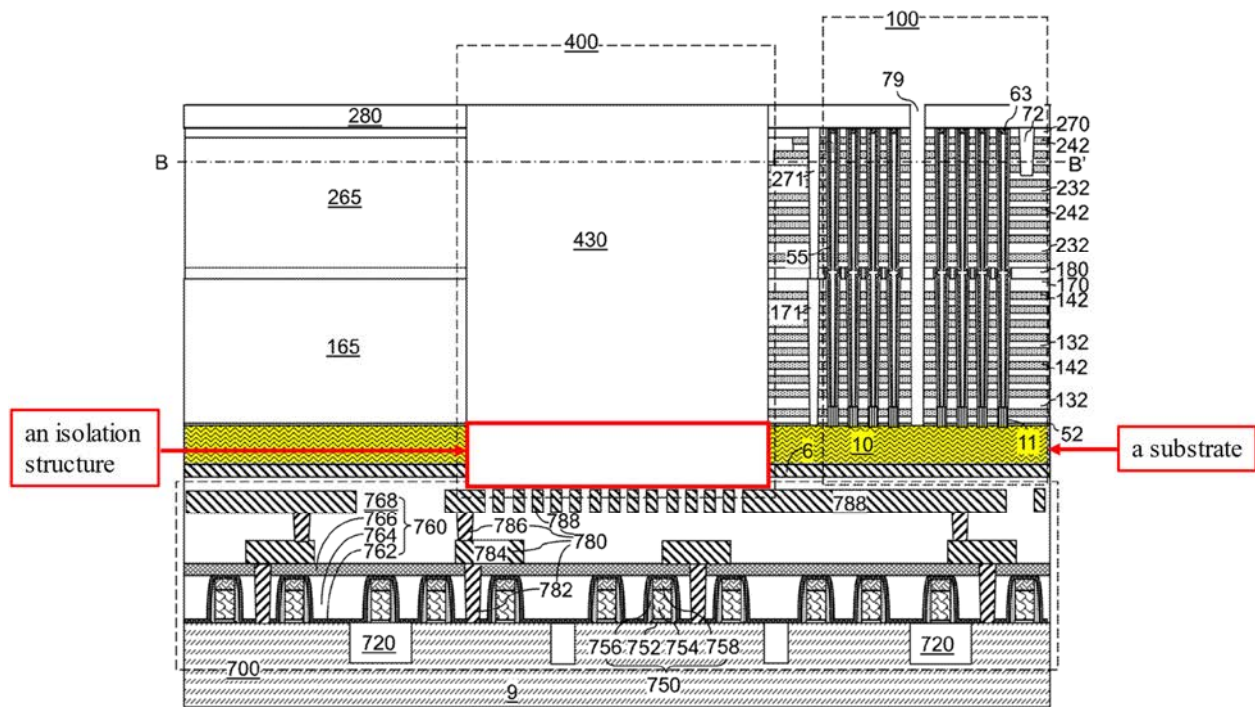


FIG. 12A

Id., Fig. 12A (annotated); [0216]. The lower portion of “dielectric fill material portion 430” (*viz.*, the portion level with and below the top of “planar semiconductor material layer 10”) is the claimed *isolation structure*, as shown below:



Id., Fig. 13A (annotated).

102. Toyama discloses that its “dielectric fill material portion 430 includes a dielectric material such as undoped silicate glass (e.g., silicon oxide.)” Ex. 1005, [0216]. A POSITA would have understood that “dielectric fill material portion 430” is *an isolation structure* because it electrically isolates conductors from each other and from electrical interference from the *substrate* (“planar semiconductor material layer 10”).

103. Toyama’s *substrate* (“planar semiconductor material layer 10”) is *with* its *isolation structure* (lower part of “dielectric fill material portion 430”) because it is formed by removing a portion of, and is surrounded by, the *substrate* (“planar

semiconductor material layer 10”). Ex. 1005, Figs. 10A-12B (forming “opening 769” in “layer 10,” then filling the opening to form “portion 430”). Indeed, Toyama’s isolation structure is within the substrate and isolates portions of the substrate from one another.

104. In summary, Toyama’s first exemplary structure discloses *a substrate* (“planar semiconductor material layer 10”) *with an isolation structure* (lower portion of “dielectric fill material portion 430”).

[15.B] “an alternating conductor/dielectric layer stack disposed on the substrate;”

105. Toyama’s first exemplary structure and Second Embodiment each disclose this limitation. As a preliminary matter that applies to both, the ’378 patent teaches that the term “‘on’ not only means ‘directly on’ something but also includes the meaning of ‘on’ something with an intermediate feature or a layer therebetween.” Ex. 1001, 4:20-25.

ii. First Exemplary Structure

106. As can be seen in Fig. 17A below, Toyama’s “alternating stack (132, 146, 232, 246)” is the claimed *alternating conductor/dielectric layer stack disposed on the substrate*. I note that only some of the alternating conductors (green) and dielectric (yellow) layers are highlighted to avoid cluttering the figure.

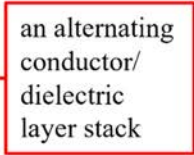


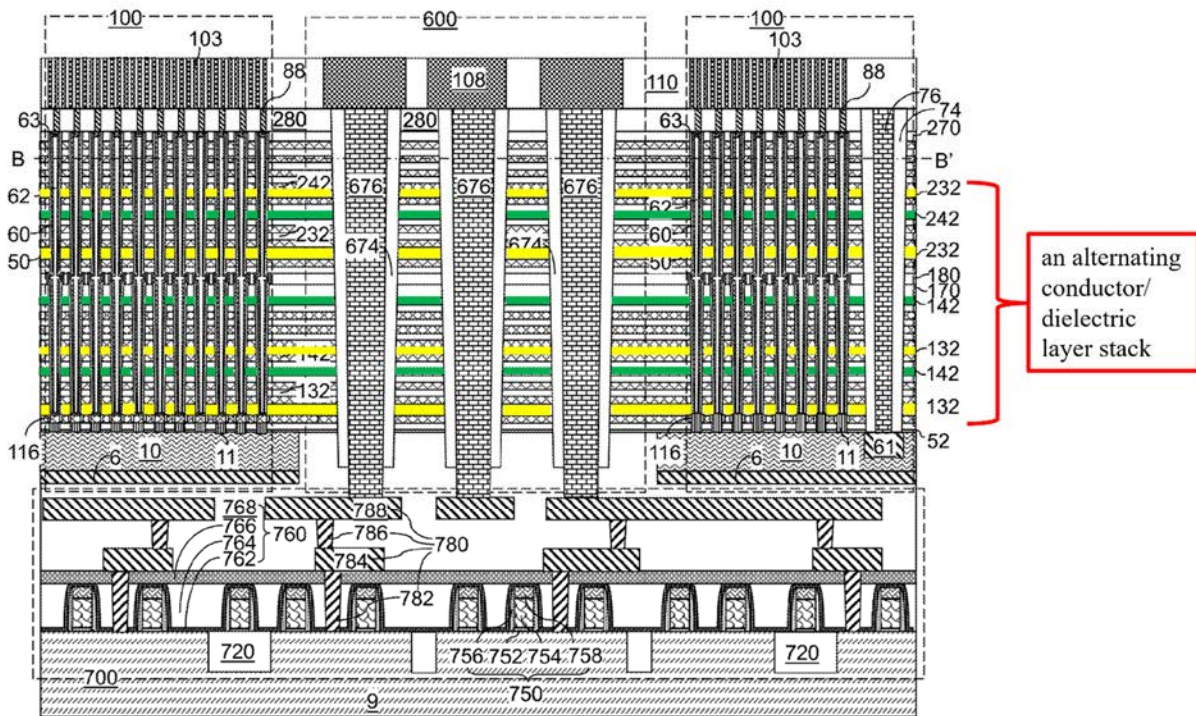
FIG. 17A

Ex. 1005, Fig. 17A (annotated). Toyama “alternating stack” comprises “first and second conductive material layers (146, 246),” “first insulating layers 132,” and “second insulating layers 232.” *Id.*, [0172], [0190], [0228], [0232].

107. Toyama’s “alternating stack” is *disposed on the semiconductor substrate*, per the broad meaning of “on” set forth in the ’378 patent itself. As noted for limitation [15.A], above, Toyama’s “planar semiconductor material layer 10” is a *semiconductor substrate*. Ex. 1005, [0170]-[0171]. As shown in Fig. 17A, above, Toyama’s alternating stack is *disposed on* (above) “planar semiconductor material layer 10.”

ii. Second Modification

108. While the discussion above is for Toyama's "first exemplary structure," Toyama's Second Modification also teaches this limitation (as can be seen in Fig. 49 below) for the same reasons.



See, e.g., Ex. 1005, Fig. 49, [0337] ("An alternating stack (132, 146, 232, 246) of insulating layers ([1]32, 232) and electrically conductive layers (146, 246) is thus formed."). In what amounts to a clear typographical error, Fig. 49 labels its alternating conductor/dielectric layer stack as elements 132, 142, 232, 242. Elements 142, 242 are "sacrificial material layers" which, in a process step prior to Fig. 49, were removed and replaced with "electrically conductive layers (146, 246)."

Id., [0337], [0340]. That is also reflected in the figures, which depict how the sacrificial material layers (shaded in gray, as in Fig. 45A) are replaced by electrically conductive layers (cross-hatched, as in Fig. 46A).

[15.C] “[i] a dielectric structure on the isolation structure and [ii] extending vertically through the alternating conductor/dielectric layer stack, [iii] wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and [iv] the dielectric structure is formed of a dielectric material;”

109. For ease of analysis, I separate this limitation into four sub-parts labelled [i]-[iv] and address how Toyama’s first exemplary structure and Second Embodiment teach each one in turn.

i. Second Modification

[15.C.i] “a dielectric structure on the isolation structure”

110. The “insulating liners 674” in Toyama’s Second Modification, shown below in Fig. 49, are the claimed *dielectric structure*. Ex. 1005, [0340].

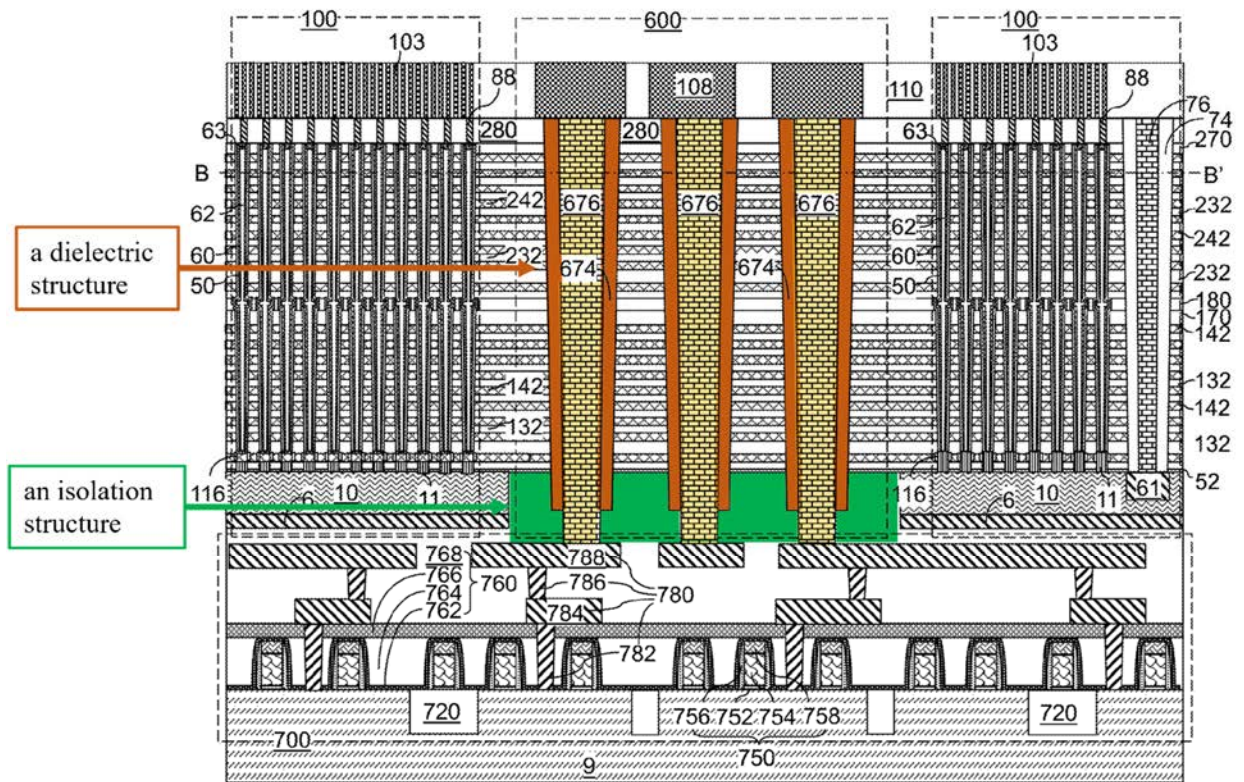


FIG. 49

Id., Fig. 49 (annotated).

111. The “insulating liners 674” are *dielectric*. Toyama forms “insulating liners 674” by depositing “a conformal insulating material layer” in “through-memory-level openings 679.”¹ Ex. 1005, [0338]-[0340]. Toyama discloses that

¹ I note that Toyama [0338] refers to “through-memory-level openings 689,” but that appears to be a typographical error. All of the relevant figures (*e.g.*, Figs. 47A-B to 49) and the other textual description refer to the elements as “through-memory-level openings 679.”

insulating liner 674 may be a “dielectric material.” *Id.*, [0233] (“[a]n insulating spacer 74 including a dielectric material”), [0381] (“insulating liner 674 having a same material composition and a same thickness as the insulating spacer 74”).

112. The challenged claims do not recite, or otherwise require, a “single-material” dielectric structure. This is confirmed by the ’378 patent which contemplates a “single-material” dielectric structure only “[i]n some embodiments.” Ex. 1001, 5:50-59. Regardless, Toyama contemplates that its “insulating liners 674” are made of a single material (e.g., silicon oxide). See claim 19 analysis.

113. Toyama’s “insulating liners 674” are, individually and collectively, a *structure*, which is not an art-specific term and is given its plain and ordinary meaning. See Ex. 1022, 5 (Merriam-Webster’s definition of “structure” as “something (such as a building) that is constructed”). As explained above, they are constructed together, and all have the same function of insulating and electrically isolating the *through array contacts* (“through-memory-level via structures 676”) as they pass through the *alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246).” A POSITA would thus have understood that “insulating liners 674” are individually and collectively *a dielectric structure*.

114. As explained above for element [15.A], Toyama’s Second Modification contemplates forming *the isolation structure* (the insulating material layer that fills “opening 151”) using the process described for the third exemplary structure.

Toyama further teaches that the *dielectric structure* (“insulating liners 674”) is *on* the *isolation structure* (the insulating material layer that fills “opening 151”) because “insulating liners 674” make contact with and extend above the isolation structure. Ex. 1001, 4:20-29 (defining “on”).

[15.C.ii] “a dielectric structure ... extending vertically through the alternating conductor/dielectric layer stack”

115. As I discuss in the section above, Toyama’s “insulating liners 674” are individually and collectively the claimed *dielectric structure*. And, as I noted above with reference to claim element [15.B], Toyama’s “alternating stack (132, 146, 232, 246)” is *the alternating conductor/dielectric layer stack*. Accordingly, as shown in Fig 49 below, Toyama discloses *a dielectric structure* (“insulating liners 674”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack 132, 146, 232, 246”).

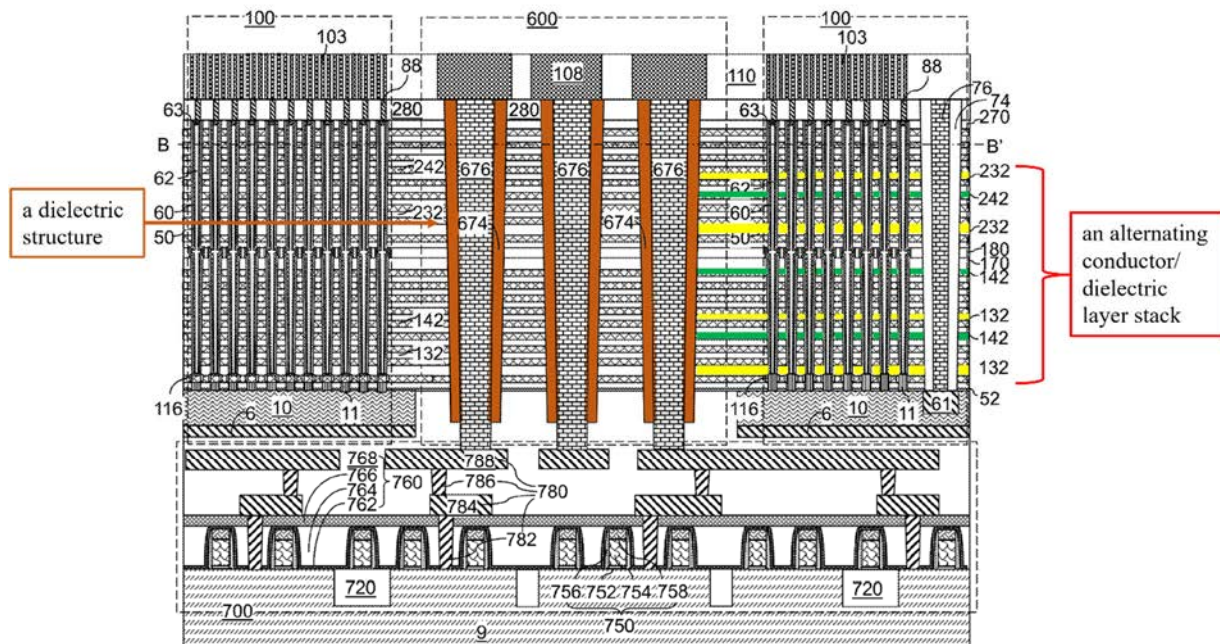


FIG. 49

Ex. 1005, Fig. 49 (annotated). As I noted previously, labels 142 and 242 are properly understood to refer to conductive material layers (146, 246).

[15.C.iii] “a dielectric structure ... wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure”

116. As highlighted below in Fig. 49, Toyama discloses *a dielectric structure* (“insulating liners 674”) *wherein the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”) *abuts a sidewall surface of the dielectric structure* (a sidewall surface of “insulating liner 674”):

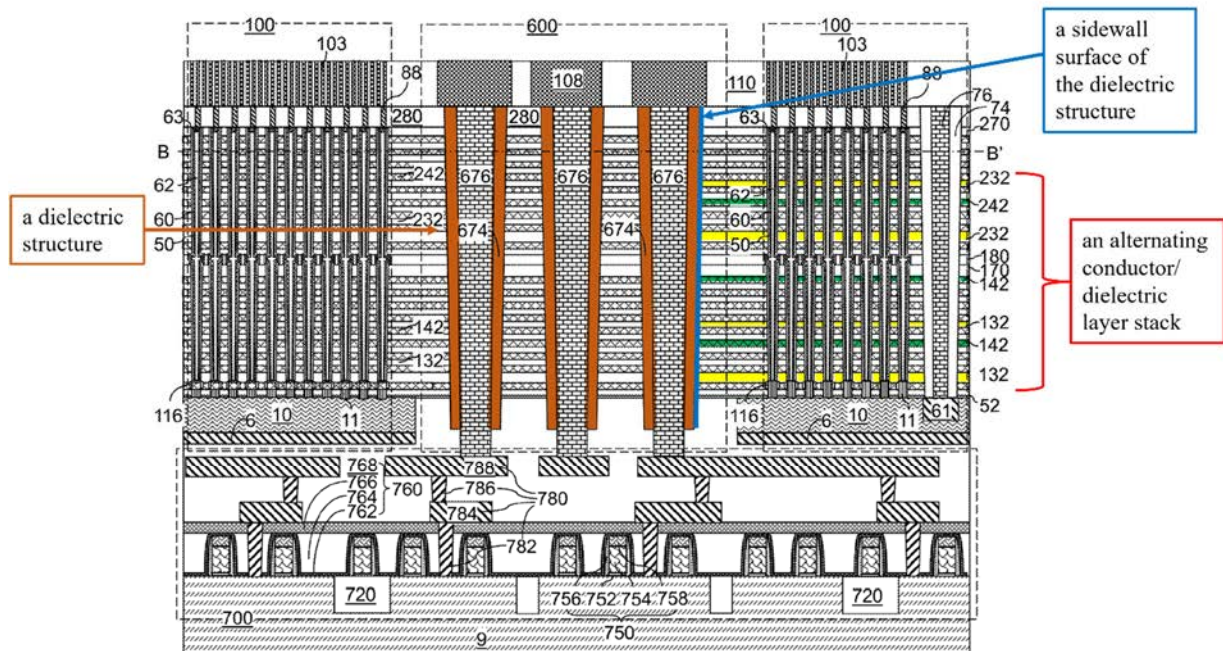


FIG. 49

Ex. 1005, Fig. 49 (annotated). As I noted previously, labels 142 and 242 are properly understood to refer to conductive material layers (146, 246).

[15.C.iv] “... wherein ... the dielectric structure is formed of a dielectric material”

117. As I discussed above, Toyama’s “insulating liners 674” are individually and collectively the claimed *dielectric structure*. And, as I discussed for element [15.C.i], each of these elements is a dielectric material. Toyama thus discloses *a dielectric structure* (“insulating liners 674”) *wherein the dielectric structure is formed of a dielectric material*.

b. First Exemplary Structure

[15.C.i] “a dielectric structure on the isolation structure”

118. I discussed in connection with claim element [15.A] that *the isolation structure* is the portion of “dielectric fill material portion 430” at and below the top surface of semiconductor substrate 10. As shown below in Fig. 15A, in Toyama’s first exemplary structure the upper part of “dielectric fill material portion 430” (viz., above the top of substrate 10) is the claimed *dielectric structure*:

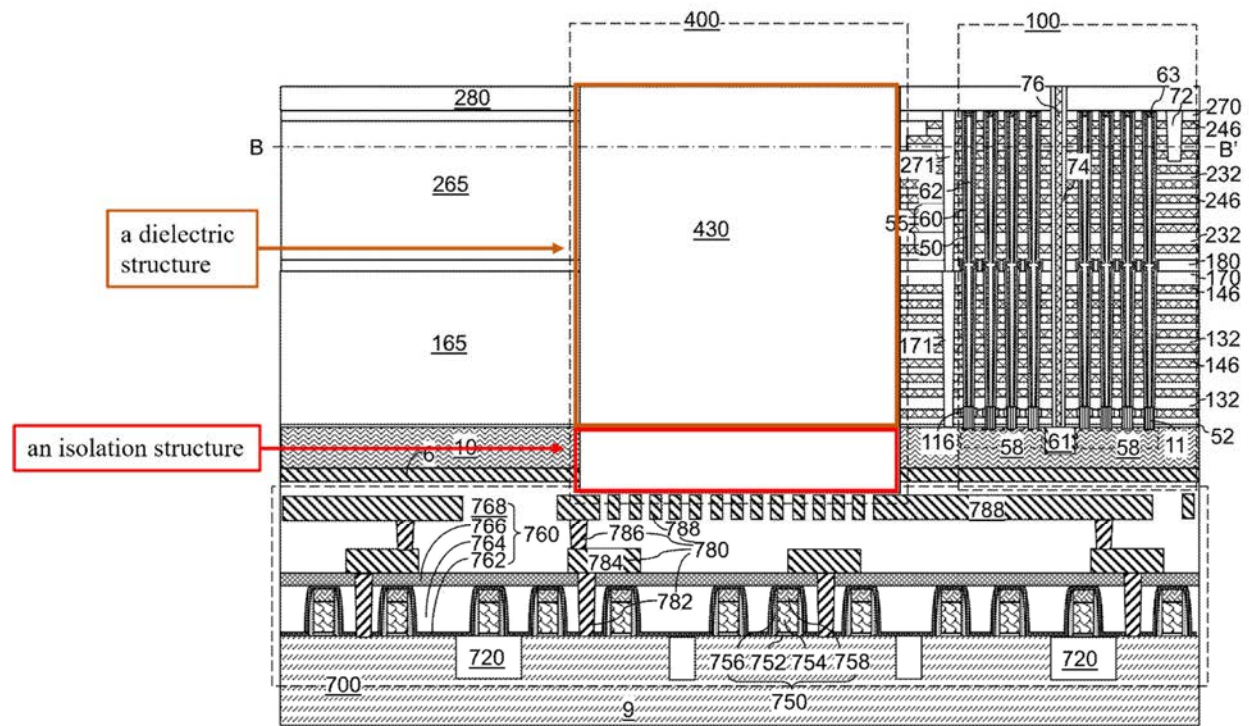


FIG. 15A

Ex. 1005, Fig. 15A (annotated). Toyama explains that “a dielectric fill material portion 430 is formed within each through-memory-level opening 769, for example, by deposition of a dielectric fill material.” *Id.*, [0216]. Thus, the upper section of

the “dielectric fill material portion 430” is *a dielectric structure* because it is composed of “a dielectric fill material.” *Id.*

119. Recall that Toyama’s isolation structure is the portion of “dielectric fill material portion 430” at or below the top of substrate 10. Toyama discloses that the first exemplary structure’s *dielectric structure* (upper part of “dielectric fill material portion 430”) is *on the isolation structure* (lower portion of “dielectric fill material portion 430”).

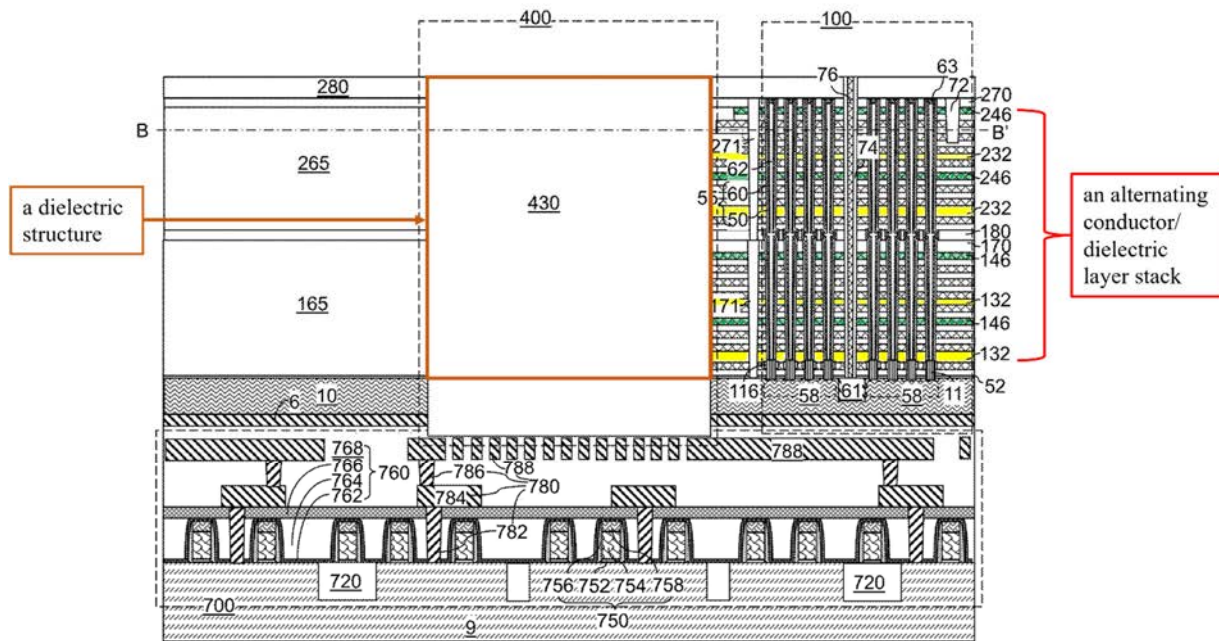
120. I note that nothing in the claim requires forming the *dielectric structure* and *isolation structure* in different steps or from different materials, nor does the specification prohibit or disavow this. On the contrary, the ’378 specification broadens “isolation structure” beyond the disclosed embodiment when it states that “STI structure 233 is exemplary and not limiting. As such, other isolation structures can be used.” Ex. 1001, 10:34-35. The purpose of the “dielectric structure” in the ’378 patent is to electrically insulate a “through array contact” as it extends through the alternating conductor/dielectric layer stack. *Id.*, 11:12-14. The purpose of the “isolation structure” in the ’378 patent is to electrically insulate a “through array contact” as it extends through the “substrate.” The upper and lower portions of Toyama’s “dielectric fill material portion 430,” respectively, fulfill these same purposes. Moreover, the language of claim element [15.A], which recites *a substrate with an isolation structure*, supports my opinion. This claim language suggests that

only the portion of an isolation structure that is *with* the *substrate* is the claimed *isolation structure*. By extension, a portion of a dielectric structure (such as the upper portion of dielectric 430 in Toyama), that is located above the level of the substrate is properly considered *a dielectric structure on the isolation structure* (because the upper bound of the claimed *isolation structure* is determined by reference to the substrate).

121. Even if the claim language did require separately forming *the isolation structure* and *the dielectric structure* (which it does not), Toyama's first exemplary structure nevertheless renders the claim element obvious. Using isolation structures on a substrate to electrically isolate components was well-known and commonplace prior to the effective filing date of the '378 patent priority date. Indeed, Toyama's third exemplary structure teaches just that, as I described in connection with element [15.A.ii] for Toyama's Second Embodiment. As it relates to Toyama's first exemplary structure, forming the *isolation structure* and the *dielectric structure* separately would be no more than the mere substitution of a known process (forming an isolation structure in "opening 151" before forming the dielectric structure, as in Toyama's third exemplary structure) for another process (forming the isolation and dielectric structures at the same time, as in Toyama's first exemplary structure) to obtain predictable results (the insulating material layer that fills "opening 151" electrically isolates the conductors embedded within).

[15.C.ii.] “a dielectric structure ... extending vertically through the alternating conductor/dielectric layer stack”

122. As I discussed in the previous section, the upper part of Toyama’s “dielectric fill material portion 430” is the claimed *dielectric structure*. And, as I discussed in connection with element [15.B], Toyama’s “alternating stack (132, 146, 232, 246)” is *the alternating conductor/dielectric layer stack*. Accordingly, as shown in Fig.15A below, Toyama discloses *a dielectric structure* (upper part of “dielectric fill material portion 430”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack 132, 146, 232, 246”):



Ex. 1005, Fig. 15A (annotated).

123. I note here that Toyama’s first exemplary structure satisfies this limitation in substantially the same way as one of the embodiments in the ’378

patent. In particular, the '378 specification shows an embodiment where dielectric structure 124 is surrounded on three sides by an alternating conductor/dielectric layer stack. This can be seen in Fig. 1C below, which is a top view of a 3D NAND device (with memory region 110 on the right and staircase region on the left):

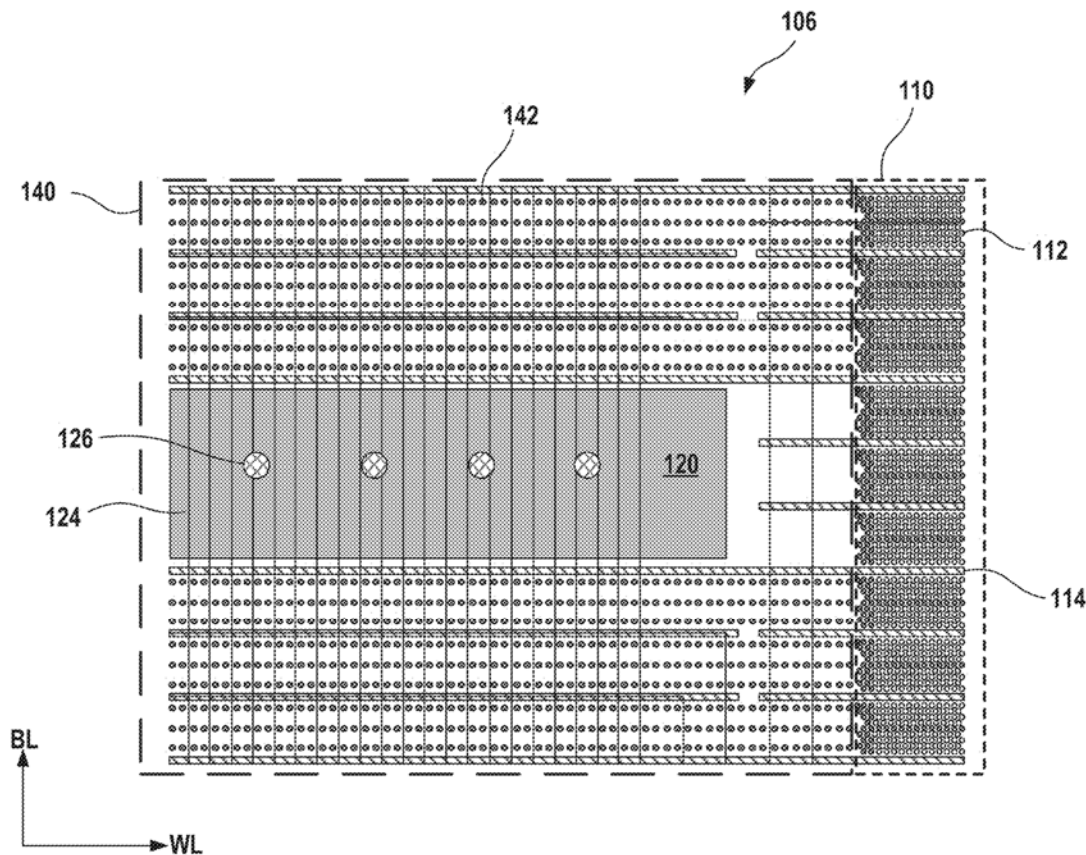
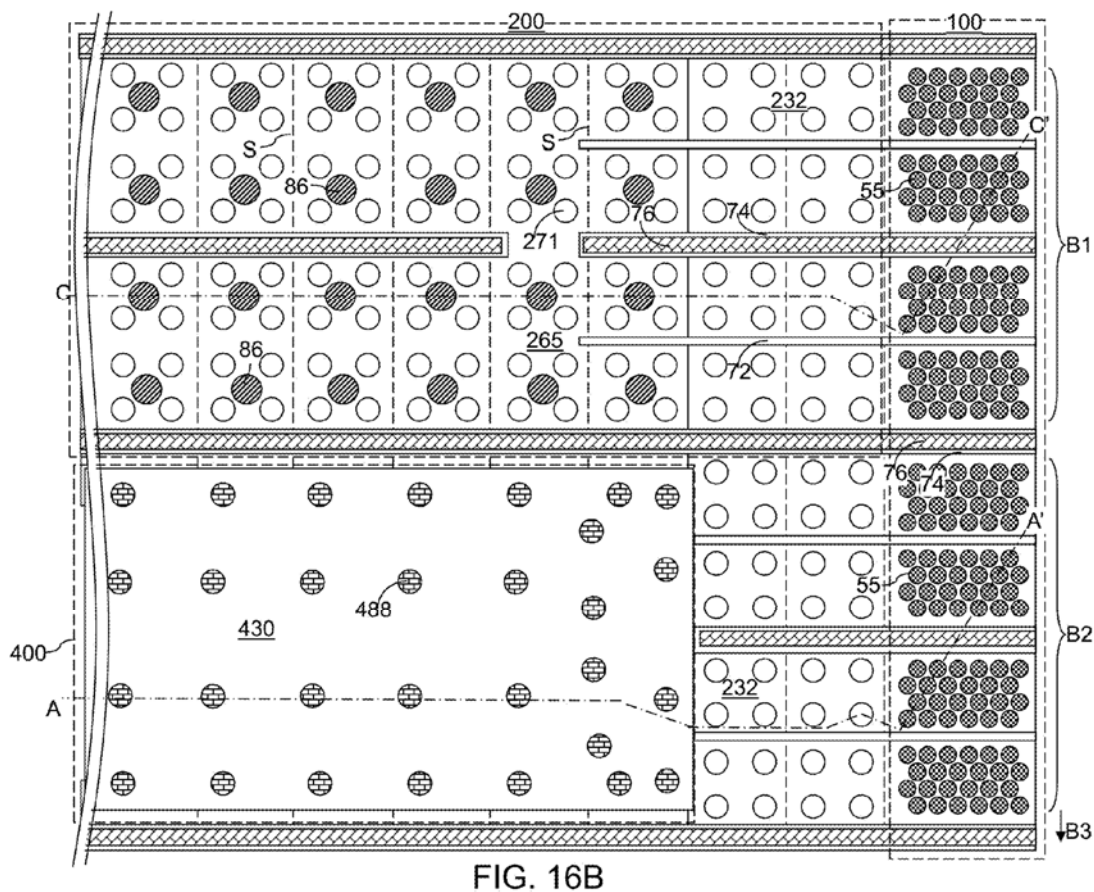


FIG. 1C

Ex. 1001, Fig. 1C.

124. Toyama's first exemplary structure is similar: the *dielectric structure* ("dielectric fill material portion 430") borders three regions including an alternating conductor/dielectric layer stack. This is shown in Toyama Fig. 16B below, which is

a top view of a 3D NAND device (with “memory array region 100” on the right and staircase regions (“word line contact via region 200”) on the left). Although not illustrated in Fig. 16B, I note that region 200 extends on the bottom of the figure as well.



Ex. 1005, Fig. 16B.

125. Toyama forms its *dielectric structure* (“dielectric fill material portion 430”) in the same way as the ’378 patent forms its dielectric layer 702. The “dielectric fill material portion 430” in Toyama and “dielectric layer 702” in the ’378 specification are both formed by removing part of the dielectric stack before

replacing the sacrificial layers with electrically conductive layers. In particular, the '378 patent removes part of “dielectric stack 400” to form “opening 600”:

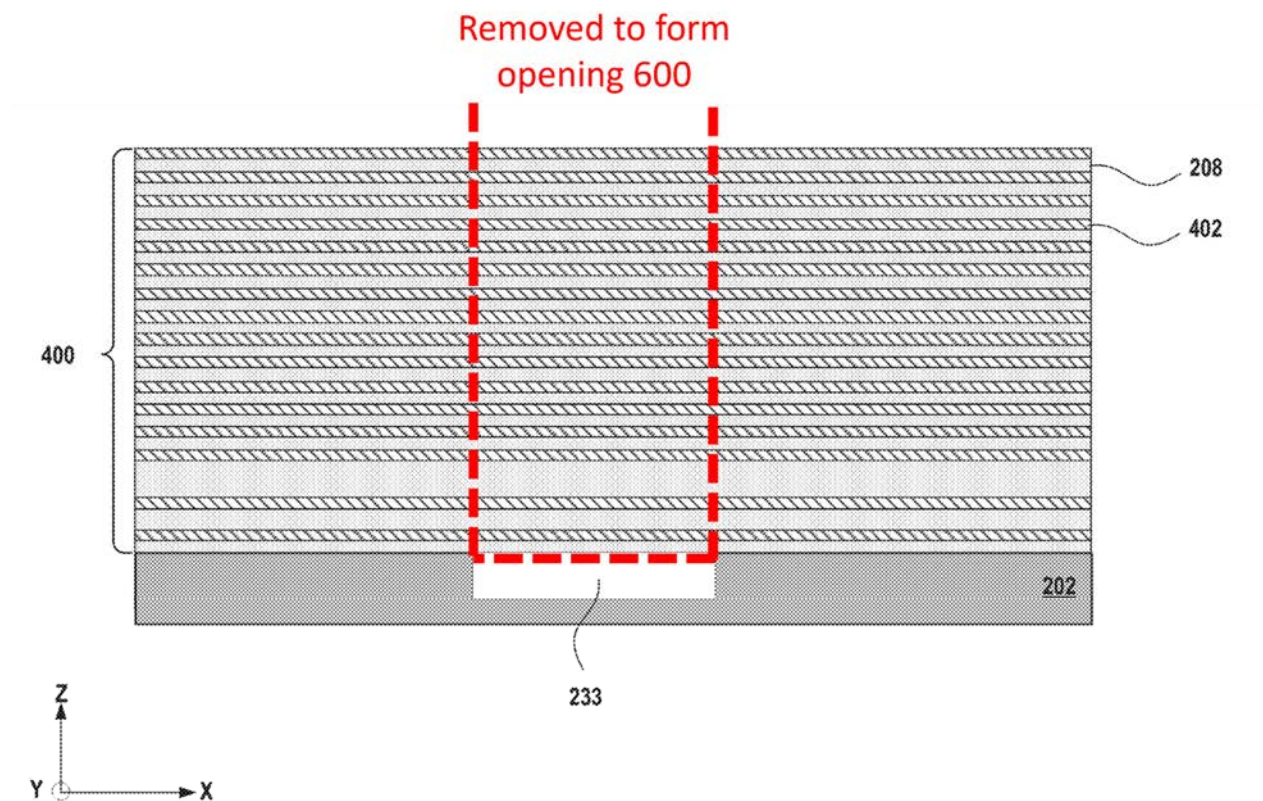


FIG. 4

Ex. 1001, Fig. 4 (annotated); *see also id.*, Fig. 6, 15:12-14. The '378 patent then fills “opening 600” with “dielectric layer 702.” *Id.*, 15:42-44.

126. In like manner, Toyama’s first exemplary structure removes “insulating layers” 132, 232 and “sacrificial material layers” 142, 242 to form “opening 769,” as shown below in Fig. 10A:

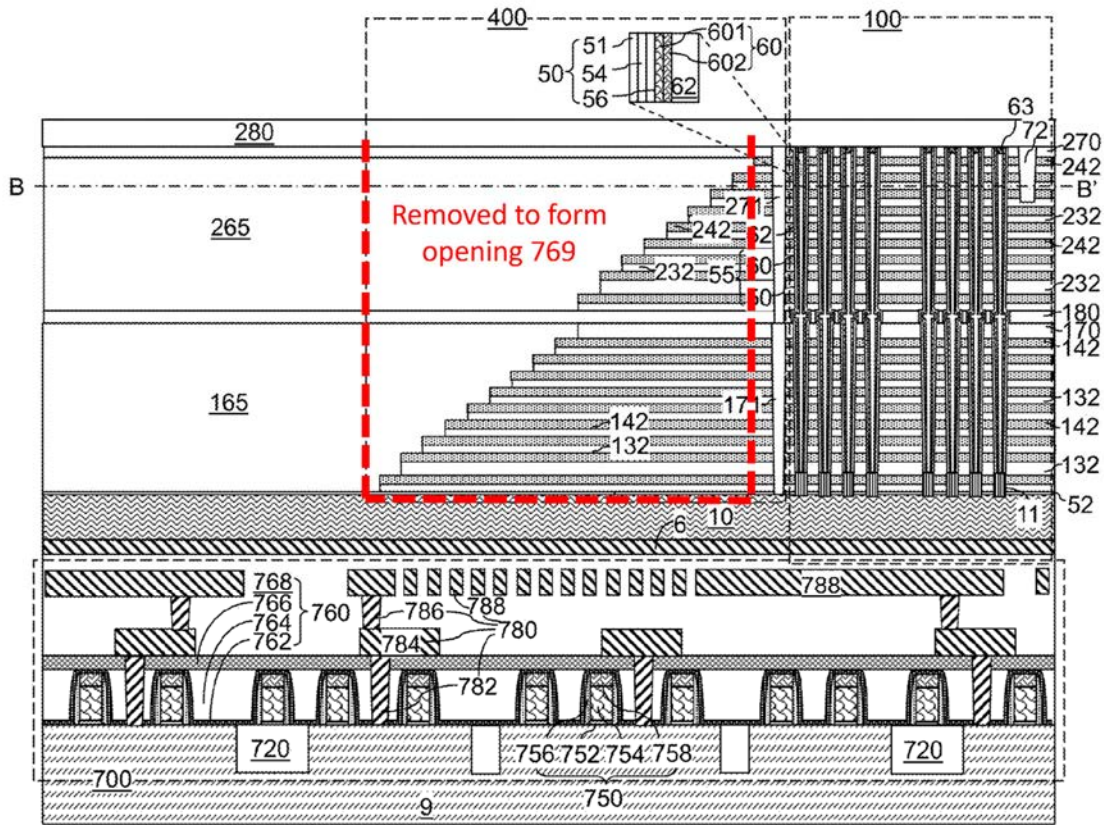
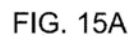


FIG. 10A

Ex. 1005, Fig. 10A (annotated), [0173], [0189]. Toyama then fills “opening 769” with “dielectric fill material portion 430.” Thus, Toyama’s first exemplary structure discloses this limitation.

[15.C.iii] “A dielectric structure ... wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure”

127. As highlighted in Fig. 15A below, Toyama discloses *a dielectric structure* (upper part of “dielectric fill material portion 430” in brown) *wherein the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”



[15.C.iv] “... wherein ... the dielectric structure is formed of a dielectric material”

Micron Ex. 1003, p. 75
Micron v. YMTC
IPR2024-00788

[15.D] “channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;”

129. For ease of analysis, I separate this limitation into two sub-parts.

Toyama’s first exemplary structure and Second Embodiment disclose each sub-part.

[15.D.i] “channel structures ... extending vertically through the alternating conductor/dielectric layer stack”

i. First Exemplary Structure

130. In Toyama’s first exemplary structure, the “memory stack structures 55” are the claimed *channel structures*, and they *extend[] vertically through the alternating layer stack* (“alternating stack (132, 146, 232, 246)”) as shown in red in Fig. 17A below:

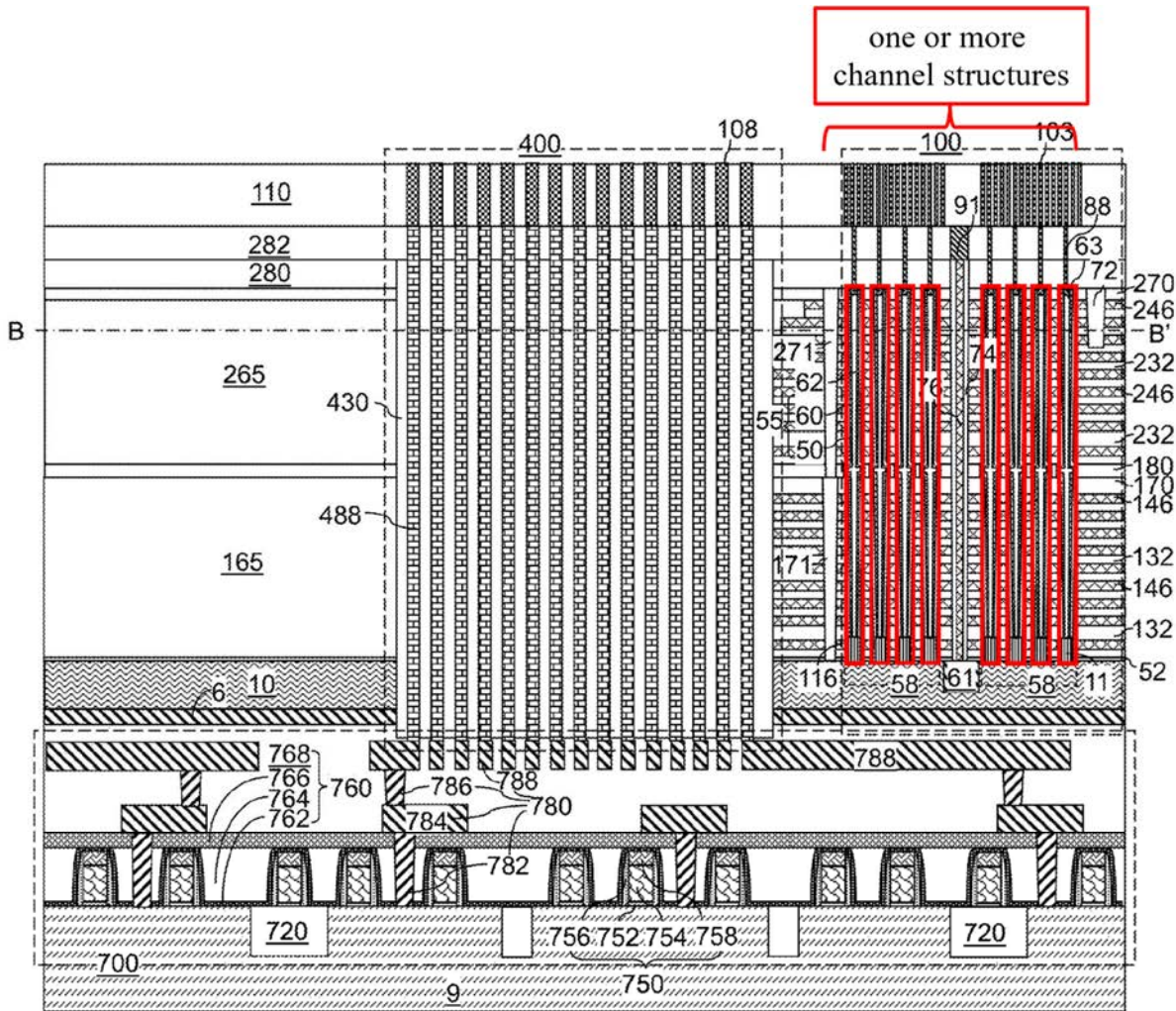


FIG. 17A

Ex. 1005, Fig. 17A (annotated). Toyama describes its “memory stack structures 55 vertically extending through the at least one alternating stack (132, 146, 232, 246).” *Id.*, [0232].

131. Even though the claim element places no other functional or structural requirements on the claimed *channel structures*, I note that Toyama’s “memory stack structures 55” perform the same function and are composed of the same

components as the channel structures in the '378 patent. With respect to function, both serves as memory elements. *Compare* Ex. 1001, 14:4-31 (“channel structure” includes a “memory film”) *with* Ex. 1005, [0388] (“The memory stack structures 55 can comprise memory elements of a vertical NAND device.”). And both are constructed from the same components. *Compare* Ex. 1001, 9:1-6 (“[c]hannel structure 216 is filled with semiconductor materials (e.g., as a semiconductor channel 218) and dielectric materials (e.g., as a memory film 220)”) *with* Ex. 1005, [0210] (“[e]ach of the memory stack structures 55 comprises a memory film 50 and a vertical semiconductor channel 60”). This supports my opinion that Toyama’s first exemplary structure discloses *channel structures* (“memory stack structures 55”) *extending vertically through the alternating layer stack* (“alternating stack (132, 146, 232, 246)”).

ii. Second Modification

132. Although the discussion above relates to Toyama’s first exemplary structure, it is equally applicable to Toyama’s Second Modification which meets this limitation for the same reasons. As shown below in Toyama Fig. 49, the *channel structures* (“memory stack structures 55”) *extend[]vertically through the alternating layer stack* (“alternating stack (132, 146, 232, 246)”).

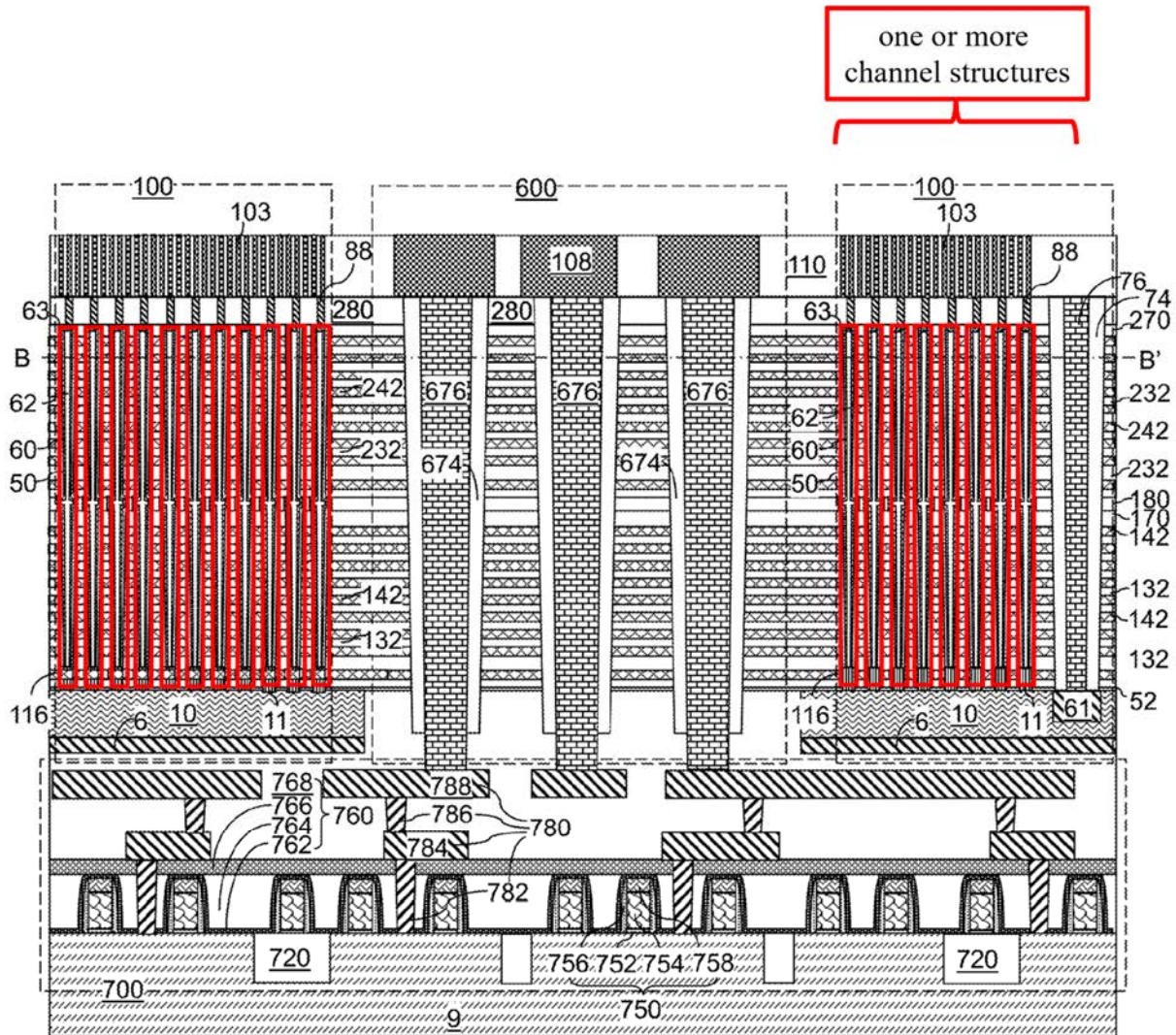


FIG. 49

Ex. 1005, Fig. 49 (showing “memory stack structures 55”).

[15.D.ii] “slit structures extending vertically through the alternating conductor/dielectric layer stack”

i. First Exemplary Structure

133. The claimed *slit structures* in Toyama’s first exemplary structure are the “laterally-elongated contact via structures 76,” and they *extend[] vertically*

through the alternating conductor/dielectric layer stack (“alternating stack (132, 146, 232, 246)”) as shown in Fig. 17A below:

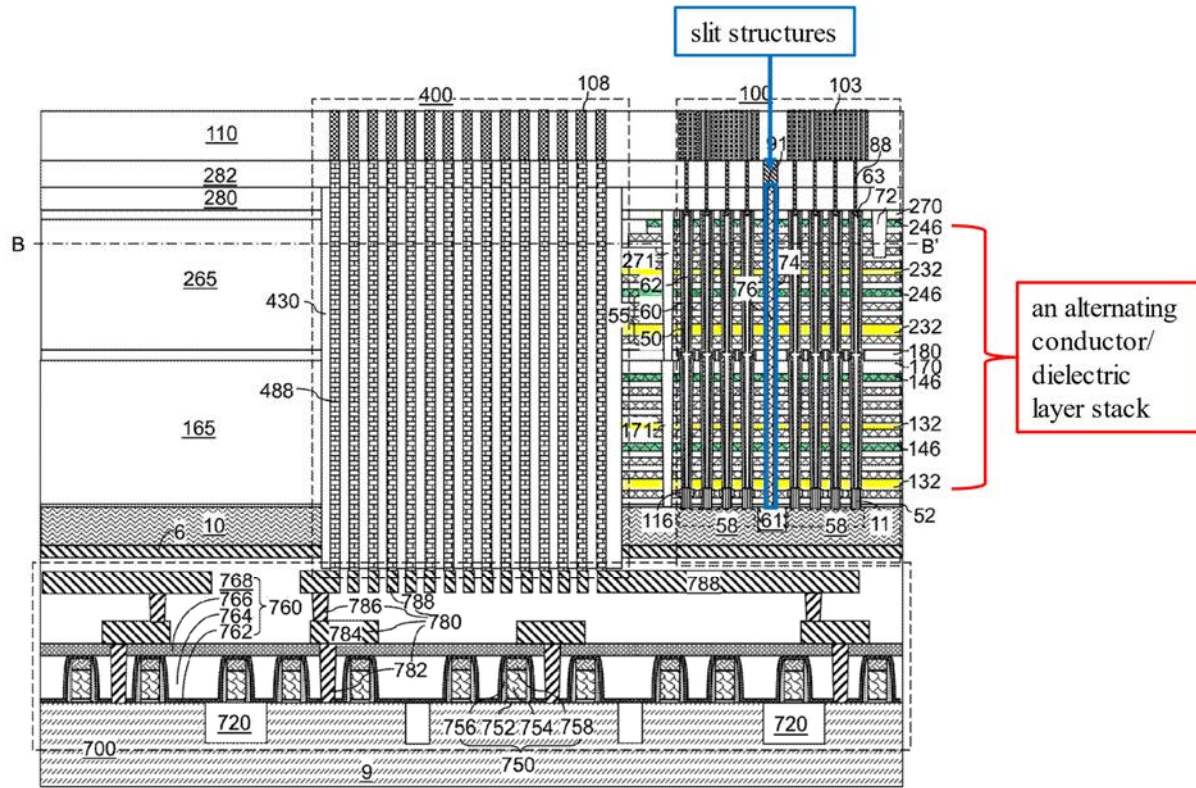
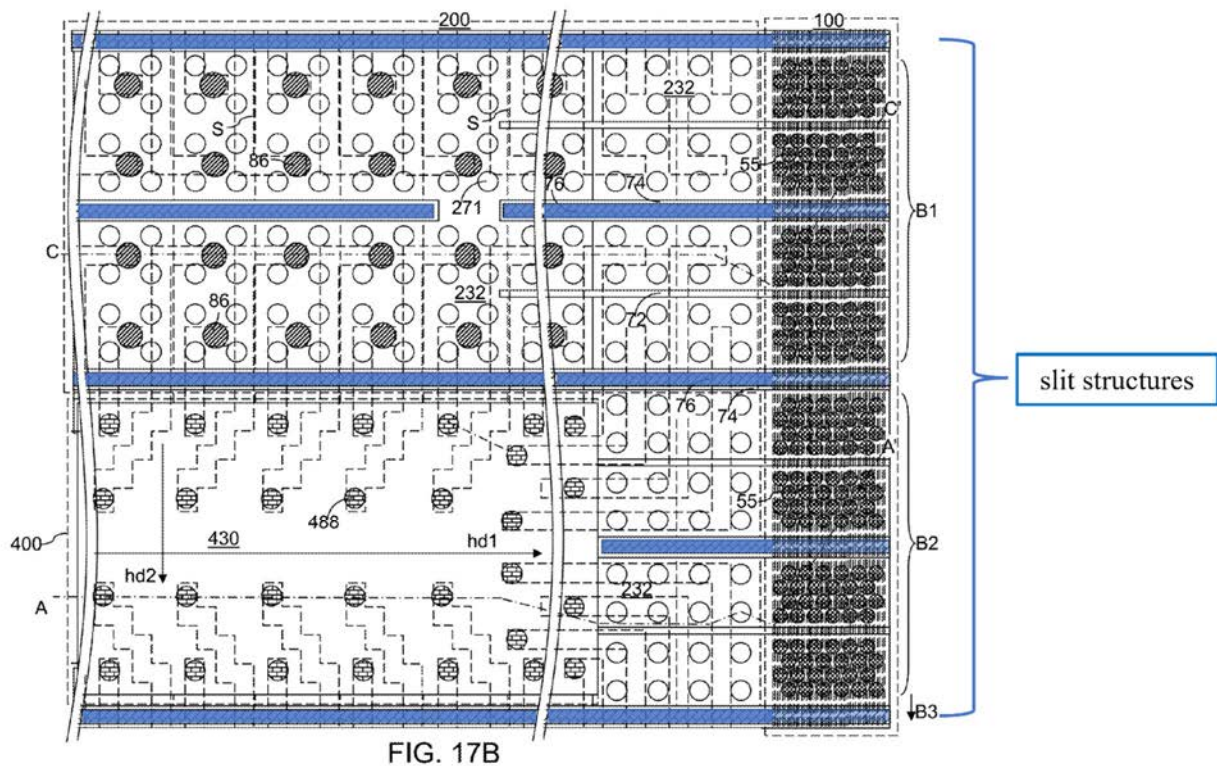


FIG. 17A

Ex. 1005, Fig. 17A (annotated). The lateral elongated shape of the “laterally-elongated contact via structures 76” *slit structures* is most easily observed in the top view of Fig. 17B:



Id., Fig. 17B (annotated). It is of no import that Toyama refers to the claimed *slit structures* as “laterally-elongated contact via structures 76.” Indeed, the plain meaning of “slit” is a laterally-elongated structure. See Ex. 1022, 4 (Merriam-Webster’s definition of “slit” as “a long narrow cut or opening”).

134. And, as can be seen in Toyama Fig. 17A above, Toyama “laterally-elongated contact via structure 76” *extend[s] vertically in the alternating layer stack* (“alternating stack (132, 146, 232, 246)”), as required by the claim.

135. Even though the claim places no functional limitation on the “slit structure,” Toyama’s “laterally-elongated contact via structures 76” perform the same function as the ’378 patent’s “slit structures.” The ’378 specification explains

that each “slit structure 226 acts as a source contact for NAND strings 204.” Ex. 1001, 9:63-67. Likewise, Toyama’s “laterally-elongated contact via structures 76” serves as “source connection[s].” Ex. 1005, [0241]. And the *slit structures* in Toyama and the ’378 patent both define memory “blocks” in their respective 3D memory arrays. *Compare* Ex. 1001, 9:52-54 (“[s]lit structures 226 ... extend along the y-axis to separate alternating conductor/dielectric stack 210 into multiple blocks.”) *with* Ex. 1005, [0237] (“laterally-elongated contact via structures 76 laterally extend along the first horizontal direction ... and laterally divide the at least one alternating stack ... into a plurality of laterally spaced-apart blocks.”). This reinforces my opinion that Toyama’s first exemplary embodiment meets the claim language.

ii. Second Modification

136. Although the discussion above relates to Toyama’s first exemplary structure, it applies equally to Toyama’s Second Modification and meets this limitation for the same reasons. As shown below in Fig. 49, Toyama’s “laterally-elongated contact via structures 76” are the claimed *slit structures* and they *extend[] vertically through the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”).

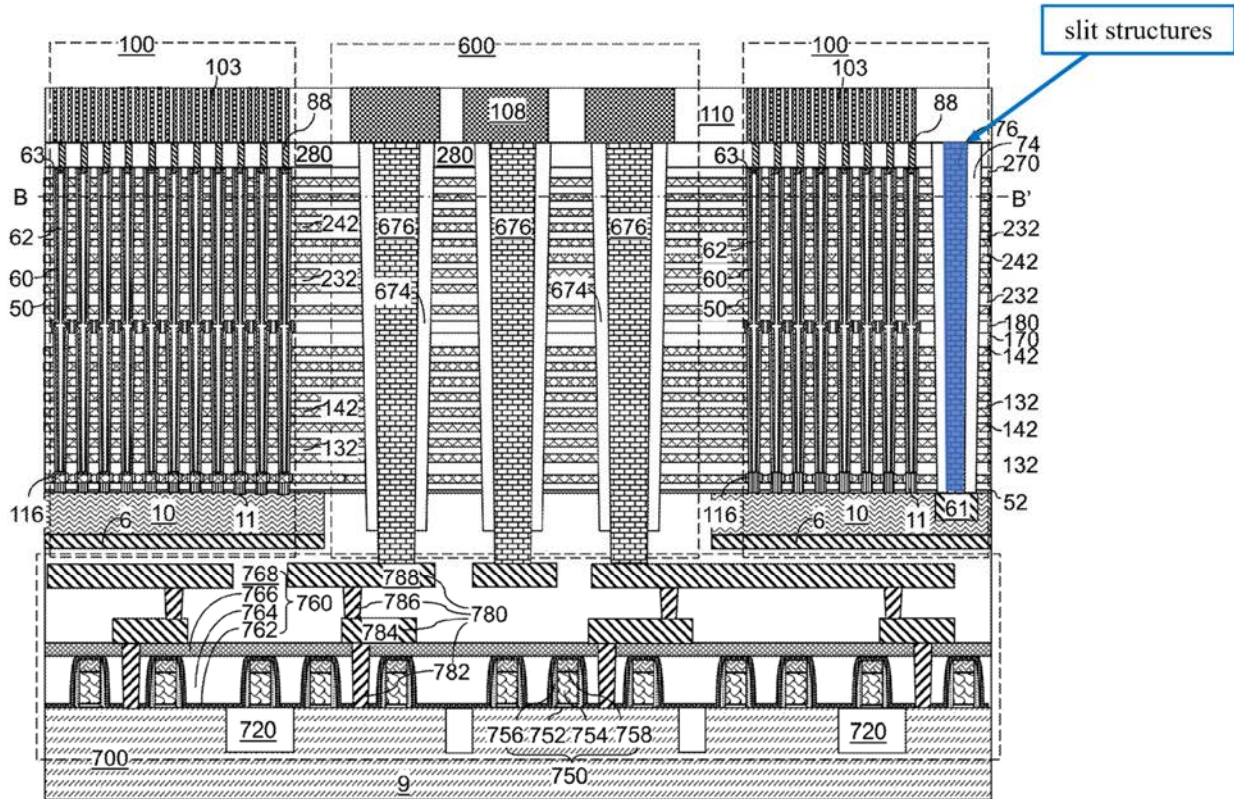


FIG. 49

Ex. 1005, Fig. 49 (annotated) (showing “laterally-elongated contact via structures 76”). In this regard, it is important not to mistake the structure 676 (in the middle of the figure) for the “laterally-elongated contact via structures 76” (on the right hand side of the figure).

[15.E] “a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;”

i. First Exemplary Structure

137. The “staircase region” highlighted in Toyama Fig. 17C below is *a staircase structure* that is *disposed in the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”). Moreover, *the staircase structure*

(“staircase region”) *comprises levels with each level having a conductor layer*
(“electrically conductive layers 146, 246”) *thereon*:

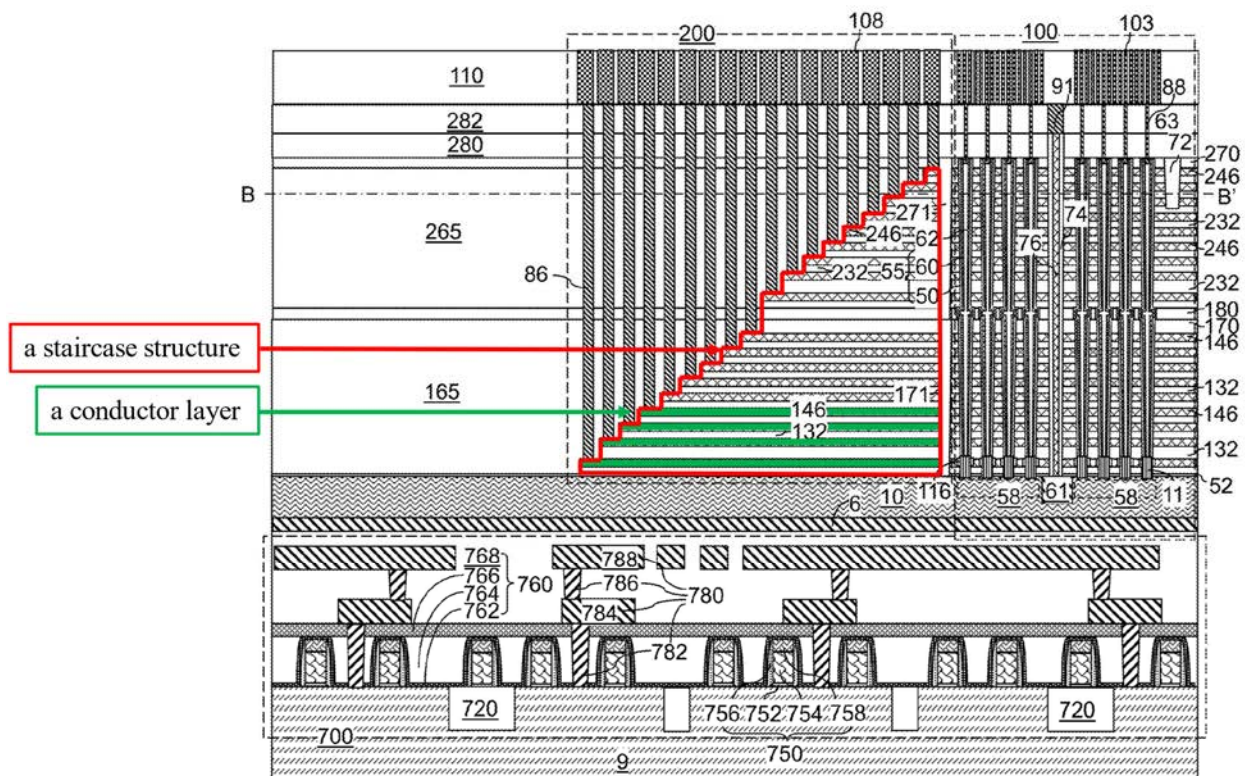


FIG. 17C

Ex. 1005, Fig. 17C (annotated). Toyama explains that “[t]he at least one alternating stack (132, 146, 232, 246) comprises staircase regions that include terraces in which each underlying electrically conductive layer (146, 246) extends farther along the first horizontal direction hd1 than any overlying electrically conductive layer (146, 246).” *Id.*, [0232].

ii. Second Modification

138. While the discussion above was in the context of Toyama's first exemplary structure, a POSITA would have understood that Toyama's Second Modification also teaches this limitation for substantially the same reasons. With respect to Toyama's fourth exemplary structure (to which the Second Modification pertains), Toyama notes that "word line contact via structures [86] can be formed as in the first through third embodiments." Ex. 1005, [0322]. Recall that the word line contacts are in Toyama's staircase region. *See id.*, Fig. 17C, [0243]. Thus, although not explicitly depicted in Figs. 44-49, a POSITA would therefore have understood that Toyama's fourth exemplary structure (and modifications thereof including the Second Modification) includes *a staircase structure* ("staircase regions").

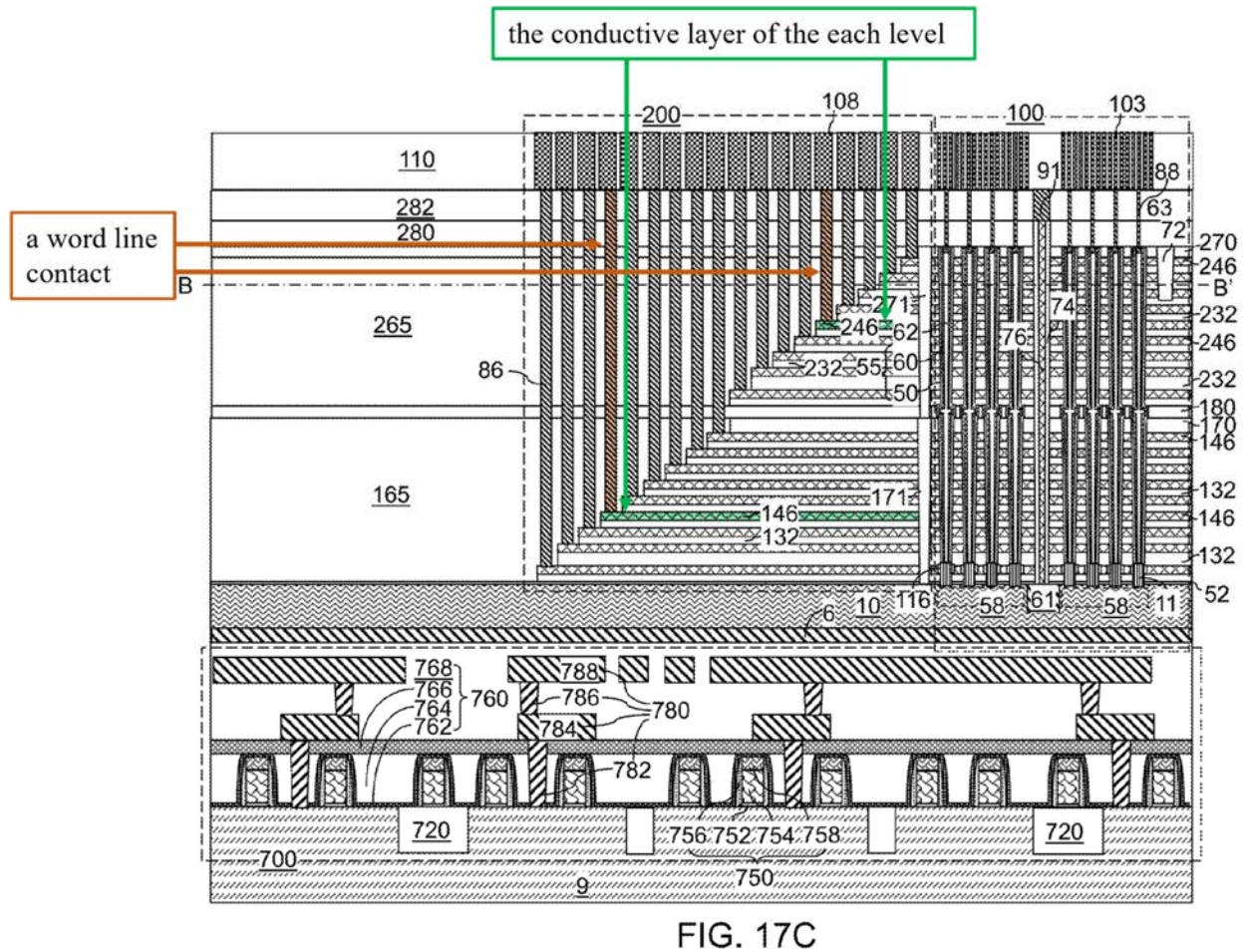
139. At a minimum, it would have been obvious to a POSITA to use a staircase structure ("staircase regions") in Toyama's Second Modification. For the memory device to be functional, a POSITA would have understood that there needed to be some way to transmit signals to the "electrically conductive layers (146, 246)," because these layers serve as the word lines for accessing (*e.g.*, reading, writing, and erasing) the memory elements in the channel structures. Ex. 1005, [0323]. And it would have been obvious to a POSITA to use the well-known *staircase structure* ("staircase regions") architecture to provide access to Toyama's word lines. Not only is this true in view of the knowledge of a POSITA, but also in view of the

teachings in Toyama itself regarding its first, second, and third exemplary structures, from which the Second Modification derives. *See, e.g., id.*, Fig. 17C.

[15.F] “a word line contact disposed on the conductor layer of the each level;”

i. First Exemplary Structure

140. As shown below, Toyama discloses *a word line contact* (“word line contact via structures 86”) *disposed on the conductor layer of the each level* (“electrically conductive layers (146, 246)”). Note that only representative examples are highlighted to avoid cluttering the image.



Ex. 1005, Fig. 17C (annotated); *id.*, [0260] (“[W]ord line contact via structures 86 ... can contact respective portions of electrically conductive layers (146, 246)”).

ii. Second Modification

141. While the discussion above was in the context of Toyama’s first exemplary structure, a POSITA would have understood that Toyama’s Second Modification also teaches this limitation for substantially the same reasons. Toyama notes that the *word line contacts* (“word line contact via structures”) in its fourth exemplary structure (of which the Second Modification is a part) “can be formed as

in the first through third embodiments.” Ex. 1005, [0322]. Thus, my analysis for the first exemplary structure applies equally here.

142. At a minimum, a POSITA would have found it obvious to transmit signals to electrically conductive layers (146, 246) in the “staircase regions” using “word line contact via structures” for the reasons I explained relative to claim element [15.E].

[15.G] “local contacts disposed on the channel structures and the slit structures; and”

143. Toyama’s first exemplary structure and its Second Modification each disclose this element. Before turning to my analysis, I first note that the ’378 patent teaches that “[i]n some embodiments, 3D memory device 200 includes a plurality of ‘local contacts.’” Ex. 1001, 11:16-17. “The contacts are referred to herein as ‘local contacts’ because they are in direct contact with the memory array structures, and further because they are formed within dielectric layer 230.” *Id.*, 11:20-24.

i. First Exemplary Structure

144. The “drain contact via structures 88” in Toyama’s first exemplary structure are the claimed *local contacts*, that are *disposed on* (in contact with and extending above) *the channel structures* (“memory stack structures 55”), and Toyama’s “source connection via structures 91” are the *local contacts* that are *disposed on* (in contact with and extending above) *the slit structures* (“laterally-elongated contact via structures 76”), as shown in Fig. 17A below:

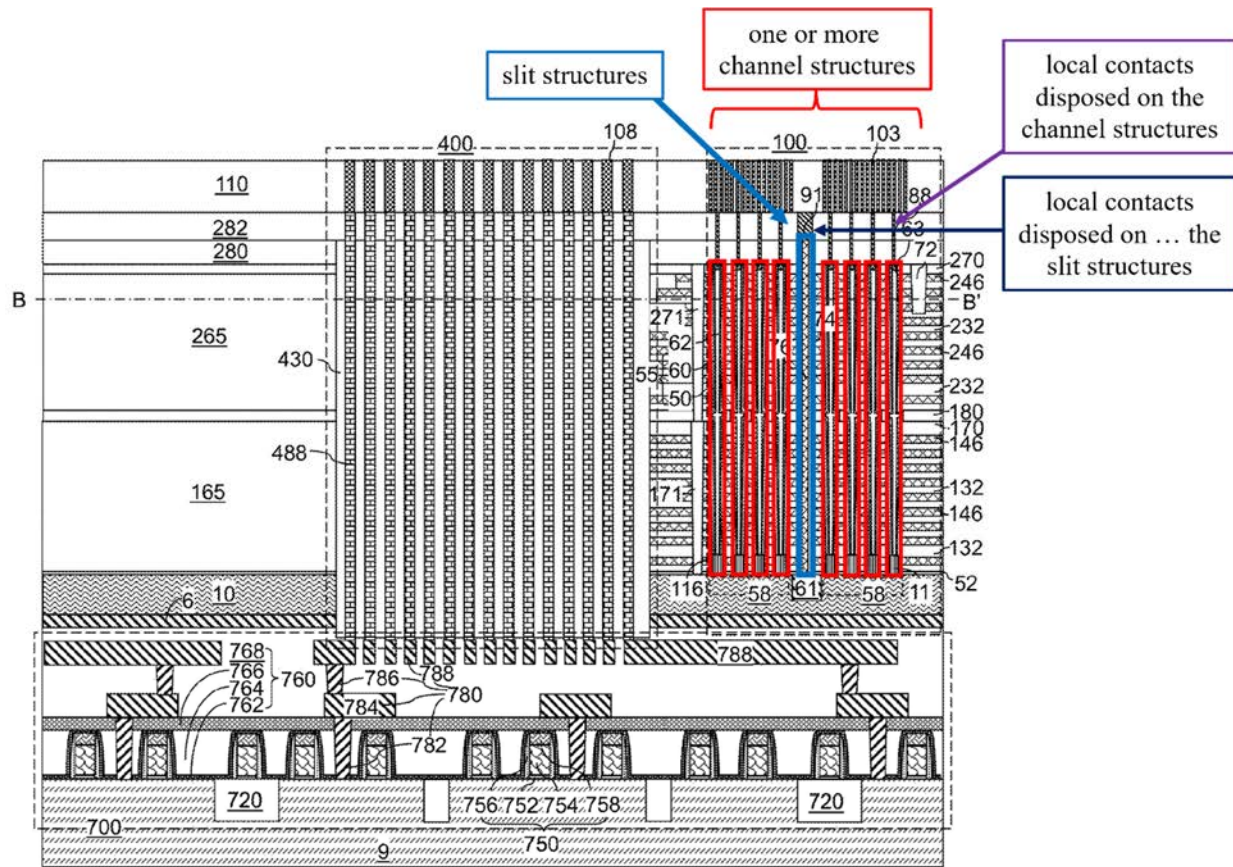


FIG. 17A

Ex. 1005, Fig. 17A (annotated); *id.*, [0251] (“The bit lines 103 are formed over the memory-level assembly, and are electrically coupled to nodes (e.g., drain regions 63) of the memory stack structures 55 by the drain contact via structures 88.”); *id.*, [0241] (“A source connection via structure 91 can extend through the contact level dielectric layers (280, 282) to provide electrical connection to the laterally-elongated contact via structures 76.”).

ii. Second Modification

145. Although the discussion above was in the context of Toyama’s first exemplary structure, Toyama’s Second Modification also teaches (or, at the very

least renders obvious) this limitation for substantially the same reasons. Toyama's "drain contact via structures 88" in the Second Modification are the *local contacts* that are *disposed on the channel structures* ("memory stack structures 55"). Ex. 1005, Fig. 49, [0342] ("drain contact via structures 88 ... can be formed as in the first through third embodiments").

146. Toyama Fig. 49 (showing the cross-section of the Second Modification) does not expressly illustrate that "source connection via structures 91" are used to connect to "laterally-elongated contact via structures 76," but a POSITA would have understood the Second Modification to include *local contacts disposed on the slit structures* ("source connection via structures 91"). The fact that Fig. 49 does not show any connection to Toyama's "laterally-elongated contact via structures 76" appears to merely be an artifact of where the cross-section was taken. Indeed, in describing the Second Modification, Toyama notes that "the metal interconnect structures can include ... source connection line structures (not shown)." Ex. 1005, [0342]. Because Toyama's *slit structures* are "**laterally-elongated** contact via structures 76," they extend some length in the horizontal direction. As such, there is no need to have a single, continuous local contact that spans the entire length of the slit. Rather, a POSITA would have understood that periodic/intermittent local contacts would suffice. This explains why a particular cross-section (such as Fig.

49) does not illustrate the local contacts. But taking a cross-section at a different location would reveal such contacts.

147. As Toyama's expressly states in connection with its first exemplary structure, "source connection line structures 101 ... contact the source connection via structures 91 to provide electrically conductive paths for biasing the source region 61 through the laterally-elongated contact via structures 76." Ex. 1005, [0250]. A POSITA would thus have understood that the Second Modification, which expressly includes "source connection line structures," "source region 61," and "laterally elongated contact via structure 76," also includes "source connection via structures." Thus, Toyama discloses *local contacts* ("source connection via structures 91") *disposed on the slit structures* ("laterally-elongated contact via structures 76") in the context of the Second Modification.

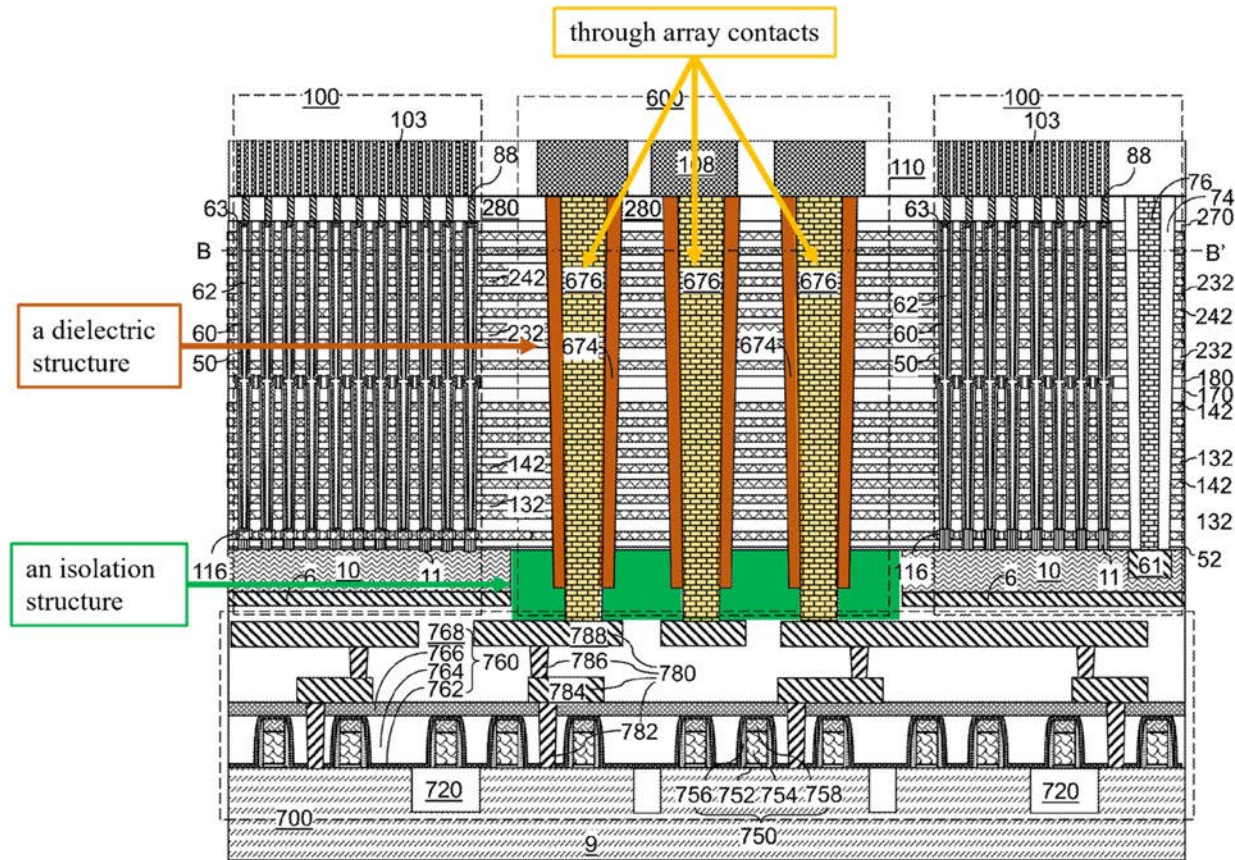
148. At a minimum, it would have been obvious to a POSITA to use *local contacts* ("source connection via structures 91") *disposed on the slit structures* ("laterally elongated contact via structure 76"). To begin, a POSITA would have understood that "laterally-elongated contact via structures 76" function as the source lines for "source regions 61" in Toyama's Second Modification. Ex. 1005, [0382]. And a POSITA would have further known that "via structures 76" require a higher-level source connection to serve their purpose. Given Toyama's express disclosure in other embodiments of "source connection via structures 91" for the same purpose,

a POSITA would have been motivated to implement “source connection via structures 91” in the Second Modification (which is largely derivative of Toyama’s first, second, and third exemplary structures). Similarly, given Toyama’s express disclosure in other embodiments of using “source connection via structures 91” for the same purpose, a POSITA would have had a reasonable expectation of success in using the same (or substantially identical) manufacturing steps (which as discussed in Section VI were very well-known) to create local contacts on Toyama’s slit structures in its Second Embodiment. This is even more the case because Toyama’s Second Embodiment is largely derivative of Toyama’s first, second, and third embodiments, which expressly disclose local contacts on slit structures..

[15.H] “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.”

i. Second Modification

149. In Toyama’s Second Modification, the “through-memory-level via structures 676” are the claimed *through array contacts*. And, as can be seen in Fig. 49 below, *they extend[]vertically through the dielectric and the isolation structures* (respectively shown in red and green below).



Ex. 1005, Fig. 49 (annotated); [0341]-[0342].

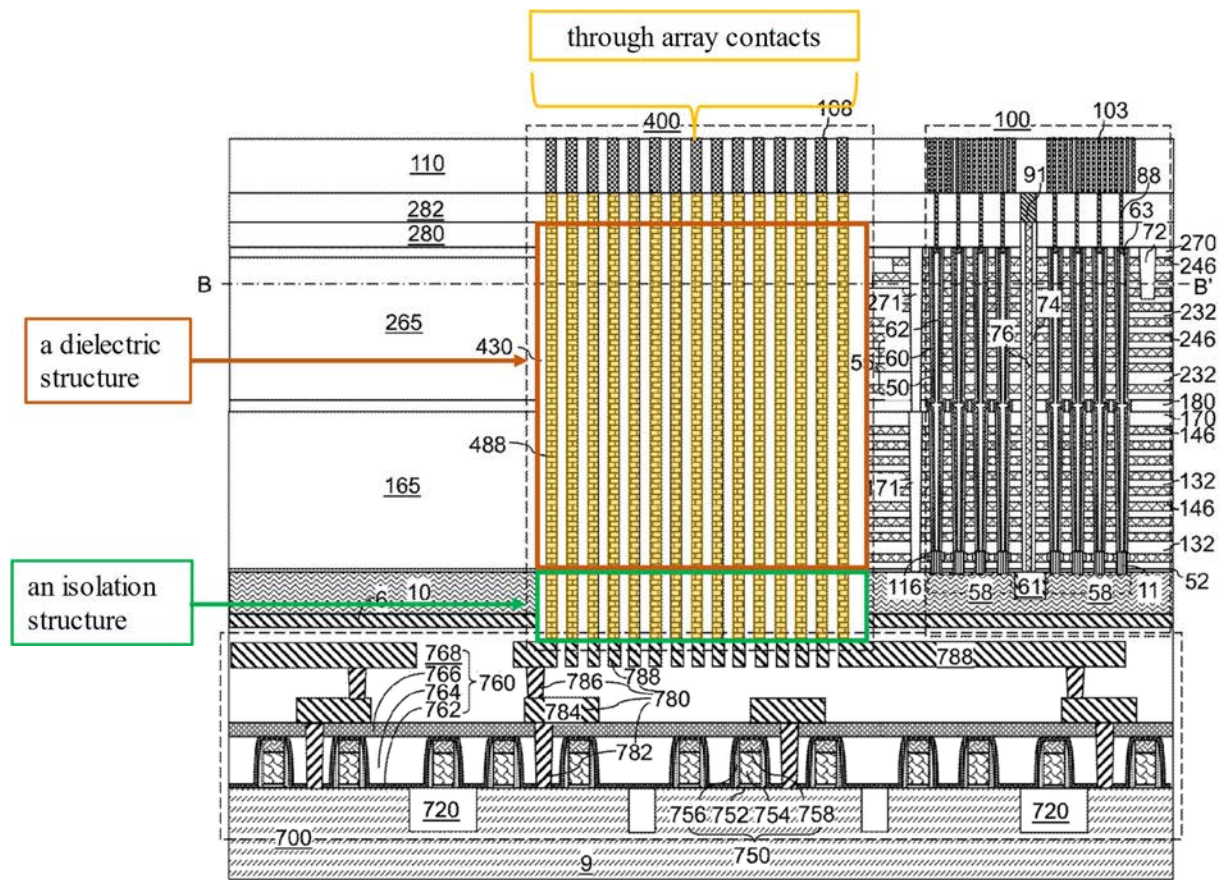
150. As discussed for claim element [15.C], “insulating liners 674” are individually and collectively *the dielectric structure* in Toyama’s Second Modification. And as discussed for claim element [15.A.ii], the insulating material layer that fills “opening 151” is *the isolation structure* in Toyama’s Second Modification.

151. Like water that travels *through* a hose or a pipe that extends *through* a wall, Toyama’s “through-memory-level via structures 676” extend *through* “insulating liners 674,” and the insulating material layer that fills “opening 151.”

Thus, Toyama discloses *through array contacts* (“through-memory-level via structures 676”) *extending vertically through the dielectric* (“insulating liners 674”) *and isolation* (the insulating material layer that fills “opening 151”) *structures*. Ex. 1005, [0340]-[0342].

ii. First Exemplary Structure

152. In Toyama’s first exemplary structure, “through-memory-level via structures 488” are the *through array contacts (TACs)*, as shown in Fig. 17A below.



Ex. 1005, Fig. 17A (annotated); *id.*, [0239].

153. As I discussed for element [15.C], in Toyama’s first exemplary structure the upper part of “dielectric fill material portion 430” is *the dielectric structure*. And as I discussed for element [15.A.ii], the lower part of Toyama’s “dielectric fill material portion 430” is *the isolation structure* in Toyama’s first exemplary structure.

154. Accordingly, Toyama’s first exemplary structure discloses *through array contacts* (“through-memory-level via structures 488”) *extending vertically through the dielectric* (upper part of “dielectric fill material portion 430”) *and isolation* (lower part of “dielectric fill material portion 430”) *structures*. Ex. 1005, [0239].

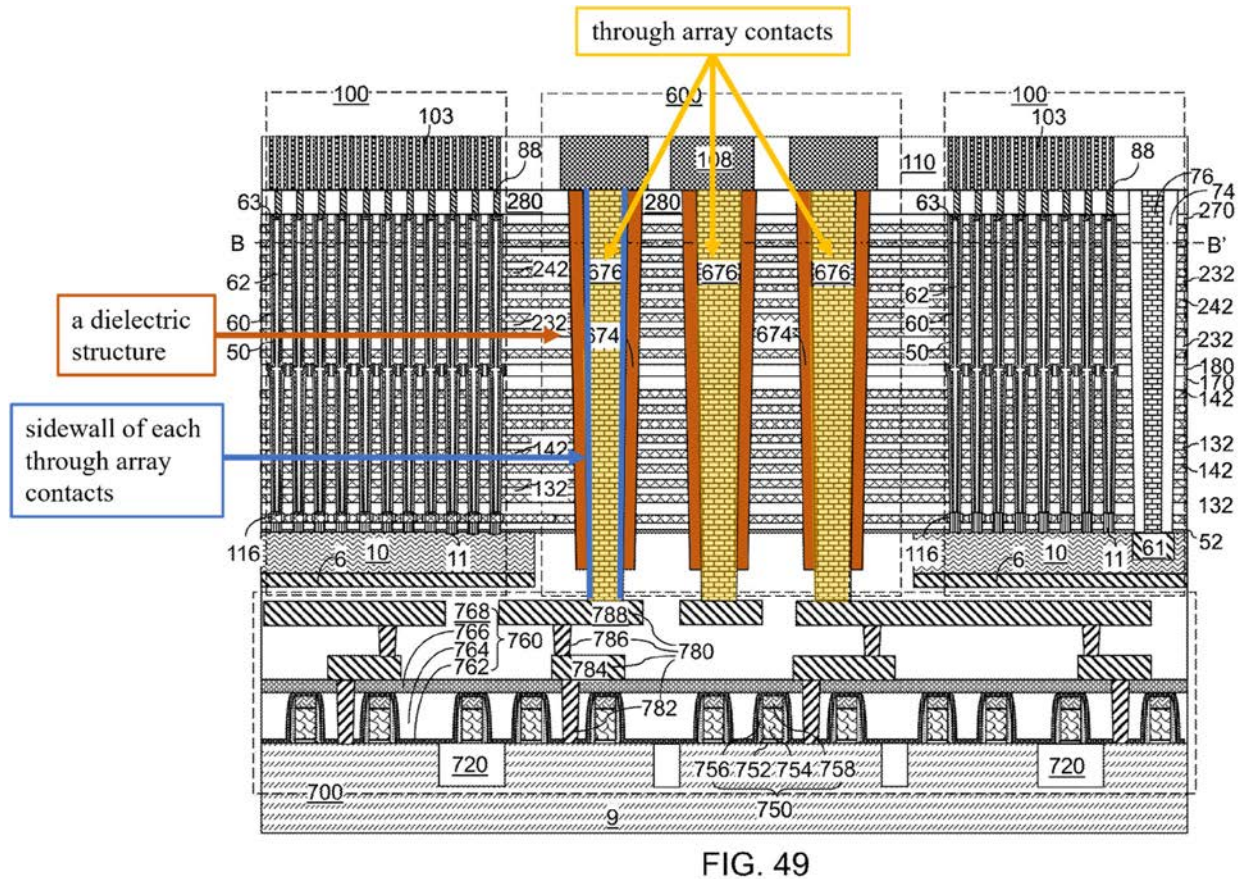
2. Claim 16

[16] “The 3D memory device of claim 15, wherein the dielectric structure abuts a sidewall of each TAC of the TACs.”

155. Toyama’s Second Modification and Toyama’s first exemplary structure both teach this limitation.

a. Second Modification

156. As shown in Toyama Fig. 49 below, *the dielectric structure* (“insulating liners 674”) in Toyama’s Second Modification *abuts a sidewall of each TAC of the TACs* (a sidewall of each of the “through-memory-level via structures 676”):



Ex. 1005, Fig. 49 (annotated).

b. First exemplary structure

157. As shown in Fig. 17A below, *the dielectric structure* (upper part of “dielectric fill material portion 430”) in Toyama’s first exemplary structure *abuts a sidewall of each TAC of the TACs* (sidewall surface of “through-memory-level via structures 488”):

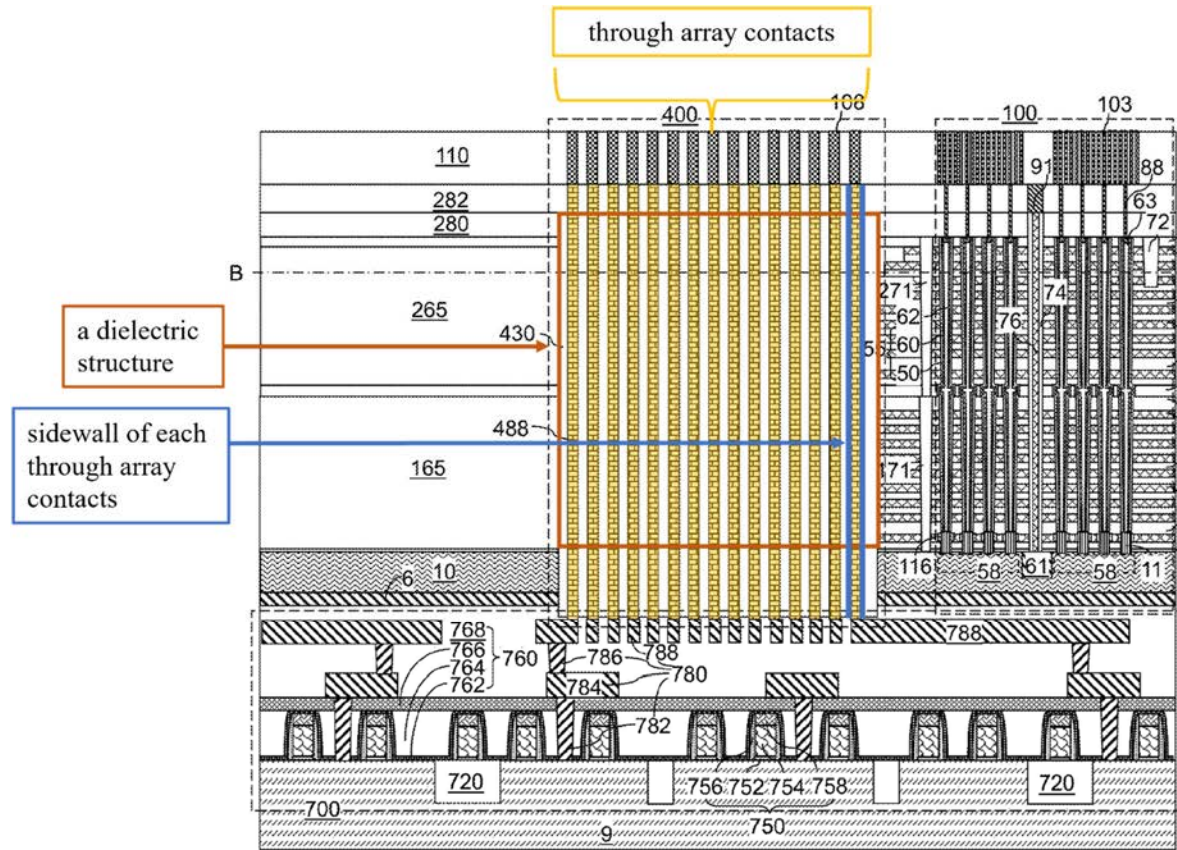


FIG. 17A

Ex. 1005, Fig. 17A (annotated).

3. Claim 17

[17] “The 3D memory device of claim 15, wherein the dielectric structure comprises a *through array contact region* of the 3D memory device.”

158. Toyama’s Second Modification and Toyama’s first exemplary structure both meet this requirement. One preliminary matter that applies to both embodiments is that the ’378 patent broadly characterizes the *through array contact region*. Ex. 1001, 10:49-56. The ’378 specification says it “can have a rectangle or square shape,” but these are only examples. *Id.* The ’378 specification goes on to

say that “these shapes are not limiting and dielectric structure 232 can have any shape according to a design layout,” and that “multiple dielectric structures ... are possible across [the] substrate.” *Id.* This is consistent with the plain and ordinary meaning of region, which does not denote any particular shape.

a. Second Modification

159. The claimed *through array contact region* in Toyama Second Modification is highlighted in Fig. 49 below. As a reminder, Toyama’s *dielectric structure* is formed by “insulating liners 674” as I discussed for claim element [15.C]. Toyama’s *through array contact region* that *comprises a through array contact region of the 3D memory device* is a part of “through-memory-level via region 600” as shown below:

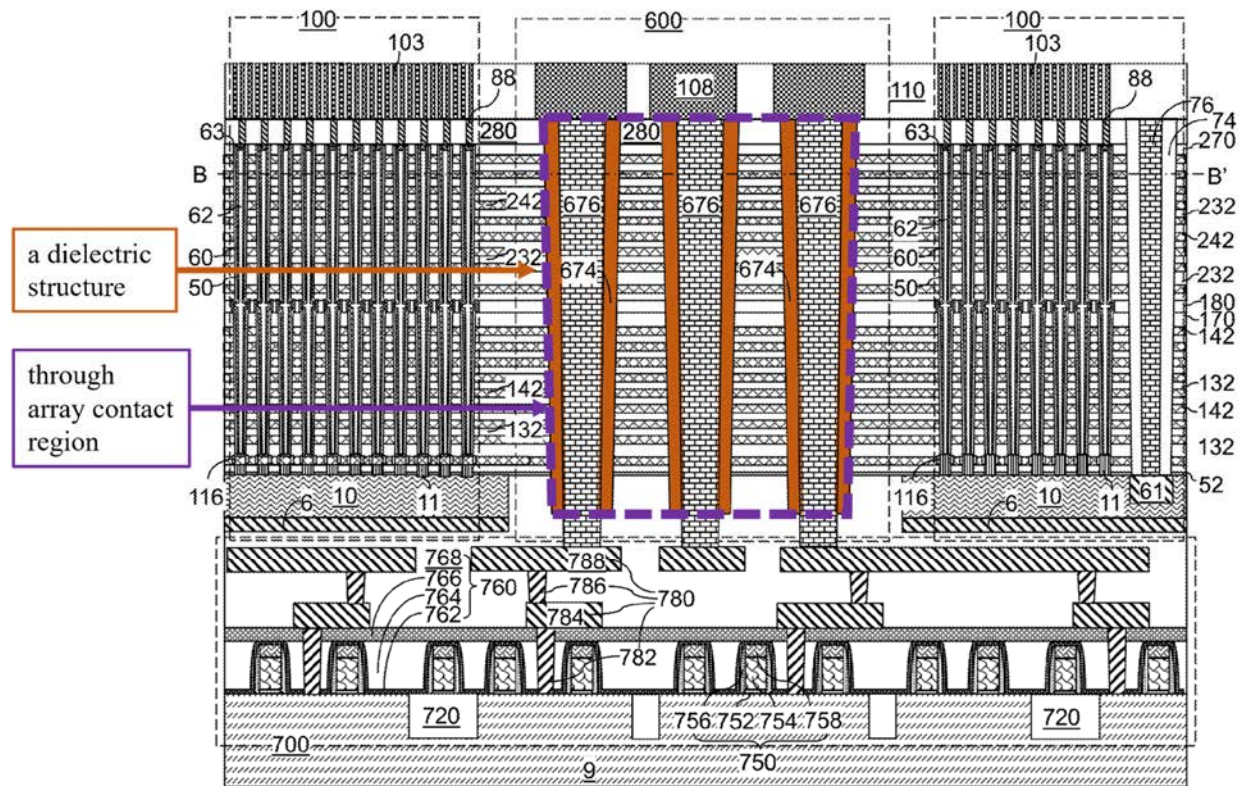


FIG. 49

Ex. 1005, Fig. 49 (annotated); *id.*, [0333], [340], [0352].

160. “In some embodiments” of the ’378 specification, the “dielectric structure ... defines the boundaries, the shape, and the size of [the] TAC region.”

Ex. 1001, 10:21-23. According to this teaching, the portion of the *dielectric structure* (“insulating liners 674”) through which the *through array contacts* (“through-memory-level via structures 676”) pass constitutes a *through array contact region*. In this manner, the *through array contacts* (“through-memory-level via structures 676”) are electrically isolated by the *dielectric structure* (“insulating liners 674”).

b. First exemplary structure

161. The claimed *through array contact region* in Toyama’s first exemplary structure is highlighted in Fig. 17A below. As a reminder, Toyama’s *dielectric structure* is “dielectric fill material portion 430” as I discussed for claim element [15.C]. The upper part of Toyama’s “portion 430” highlighted below that is part of “through-memory-level via region 400” *comprises a through array contact region of the 3D memory device* and thus satisfies claim 17.

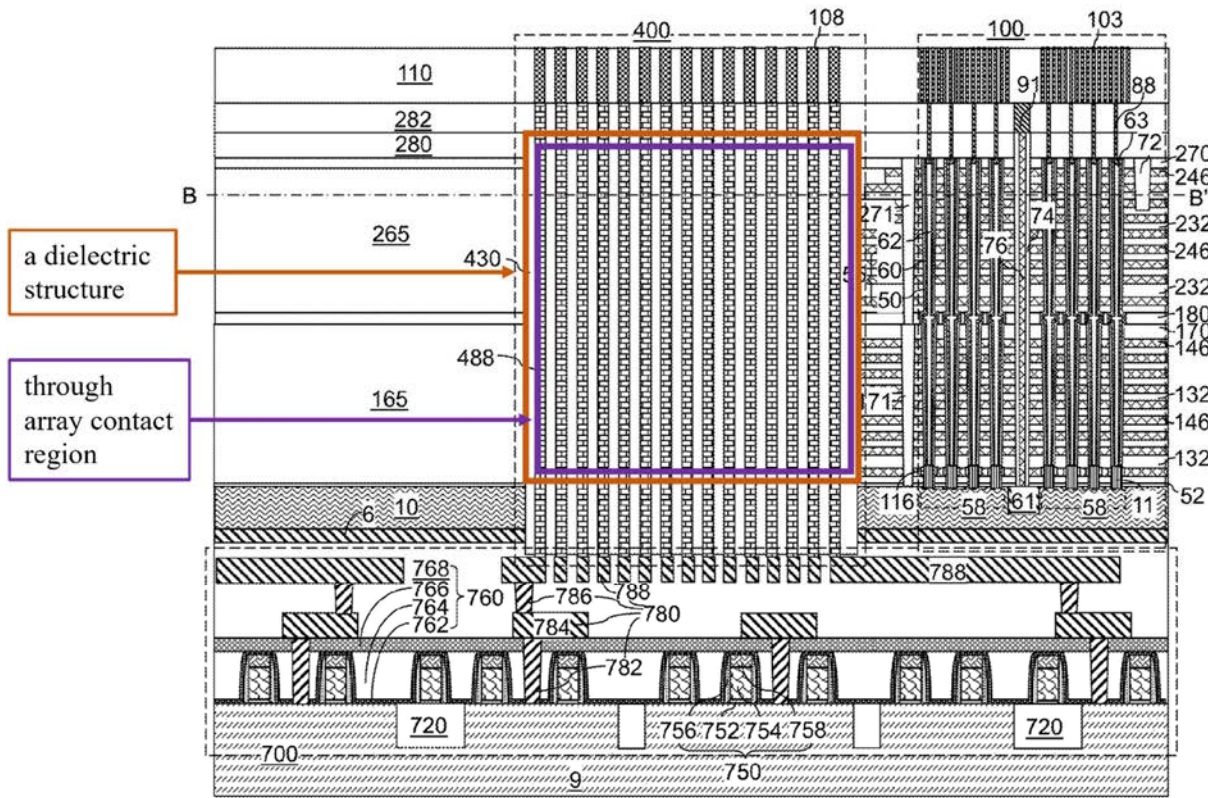


FIG. 17A

Ex. 1005, Fig. 17A (annotated); [0165]-[0167].

4. Claim 19

[19] “The 3D memory device of claim 15, wherein the dielectric material comprises silicon oxide.”

162. Toyama’s Second Modification and Toyama’s first exemplary structure meet this requirement.

a. Second Modification

163. As a reminder, in Toyama’s Second Modification the claimed *dielectric structure* is “insulating liner[] 674.” See limitation [15.C.iv] discussion. Toyama contemplates that the *dielectric material* from which the dielectric structure (“insulating liner 674”) is made comprises silicon oxide. In particular, Toyama discloses that “insulating liner 674” may “hav[e] a same material composition ... as the insulating spacer 74.” Ex. 1005, [0381]. The “insulating spacer 74” in Toyama is described as including “an insulating material such as silicon oxide.” *Id.*, [0234]. Accordingly, Toyama teaches that *the dielectric material* (a material out of which “insulating liners 674” are made) *comprises silicon oxide*.

164. At a minimum, it would have been obvious to a POSITA that Toyama’s insulating liners 674 comprised silicon oxide. As its name reflects, Toyama’s “insulating liner 674” is insulating. The properties of silicon oxide were well-characterized and had been studied extensively. It was well-known to POSITAs that silicon oxide was a suitable insulating material from which an insulating liner could be made and it was commonly used for that purpose. This knowledge is reflected in

numerous references, including: Ex. 1019 (U.S. Pat. No. 9,293,348), 2:61-65 (“dielectric structure” may comprise an “oxide” such as “silicon oxide”); Ex. 1020 (U.S. Pat. No. 10,103,169), Figs. 11-12, 3:1-8 and 21:1-61 (discussing “formation of a conformal silicon oxide liner” in 3D-NAND memory devices”); Ex. 1021 (U.S. Pat. No. 8,697,519), 7:30-40 (“the liner insulating layer may include a silicon oxide layer”). Because silicon oxide had been used extensively in semiconductor manufacturing, a POSITA would have had more than a reasonable expectation of success in using it for Toyama’s insulating liners 674. Thus, a POSITA would have found it obvious to use silicon oxide as the *dielectric material* in Toyama’s insulating liners 674.

b. First exemplary structure

165. As a reminder, in Toyama’s first exemplary structure *the dielectric material* is the “dielectric fill material” that forms “dielectric fill material portion 430.” See limitation [15.C.iv] discussion. Toyama discloses that “dielectric fill material portion 430 includes a dielectric material such as undoped silicate glass (e.g., *silicon oxide*), doped silicate glass, or a spin-on glass (SOG).” Ex. 1005, [0216] (emphasis added).

5. **Claim 20**

[20] “The 3D memory device of claim 15, wherein the TACs comprise a conductive material.”

166. Toyama’s Second Modification and Toyama’s first exemplary structure meet this requirement.

a. Second Modification

167. As a reminder, in Toyama’s Second Modification, the “through-memory-level via structures 676” are *through array contacts (TACs)*. See limitation [15.H] discussion. Toyama teaches its *TACs* (“through-memory-level structures 676”) *comprise a conductive material*. For example, Toyama discloses that “[e]ach remaining portion of the ... *conductive material* in a through-memory-level opening 679 constitutes a through-memory-level via structure 676.” Ex. 1005, [0341] (emphasis added).

b. First exemplary structure

168. As a reminder, in Toyama’s first exemplary structure the “through-memory-level via structures 488” are *through array contacts (TACs)*. See limitation [15.H] discussion. Toyama teaches that its *TACs* (“through-memory-level structures 488”) *comprise a conductive material*. For example, Toyama states that “through-memory-level via structures 488 may be formed ... [by] depositing a conductive material.” Ex. 1005, [0244].

C. Ground 2: Mushiga in View of the Knowledge of a POSITA

169. In my opinion, Mushiga in view of a POSITA's knowledge renders claims 15-17 and 19-20 obvious. Fig. 11 of Mushiga is useful for illustrating many of the elements of the challenged claims and I use Fig. 11 to show the mapping where possible for consistency. I note at the outset, however, that Mushiga's "first exemplary structure" encompasses all of Figs. 1-13. So, too, does my analysis and opinions since Figs. 1-13 show different steps in the manufacturing process and many of the structures I rely on are shown in multiple figures with the same reference numerals.

1. Claim 15

[15.Pre] "A three-dimensional (3D) memory device, comprising:"

170. I offer no opinion on whether the preamble is or is not limiting. However, if the preamble is considered to be a limitation, my opinion is that Mushiga discloses *a three-dimensional (3D) memory device*. For example, Mushiga expressly recites that "[t]he embodiments of the disclosure can be employed to form various structures including ... three-dimensional monolithic memory array devices." Ex. 1006, 6:24-29.

[15.A] "a substrate with an isolation structure;"

171. For ease of analysis, I separate this limitation into two sub-parts.

[15.A.i] “a substrate”

172. To begin, Mushiga discloses *a substrate*. A substrate, as defined in the '378 specification is “a material onto which subsequent material layers are added, or otherwise ‘disposed.’” Ex. 1001, 4:41-43. This is consistent with the plain and ordinary meaning of that term to a POSITA. Mushiga discloses a “first semiconductor substrate 8” onto which other layers are added. Ex. 1006, 7:34-38; *see also id.*, 7:40-8:5 (discussing formation of additional layers on substrate). Thus, Mushiga discloses *a substrate*, which is highlighted in Fig. 11 below.

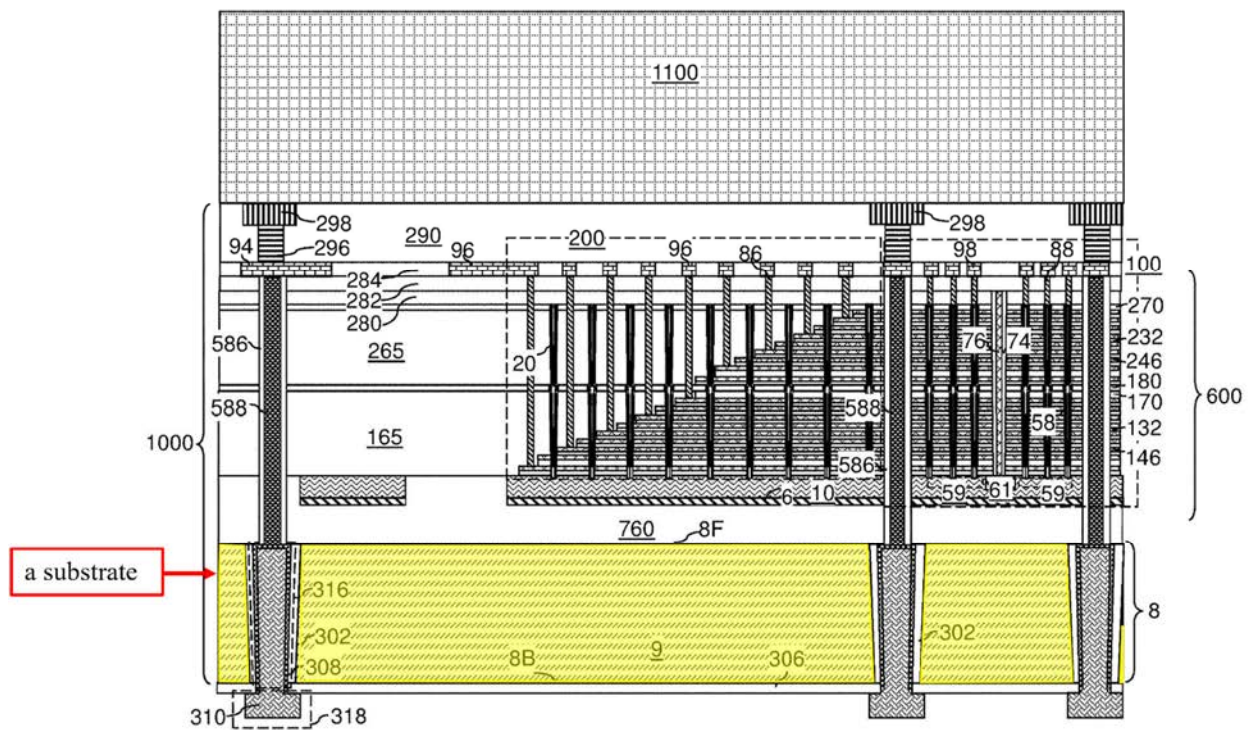


FIG. 11

Id., Fig. 11 (annotated); 9:8-14 (“insulating material layer 760” formed over substrate); 8:62-64 (“first semiconductor devices 600” formed over substrate).

[15.A.ii] “... with an isolation structure”

173. The “insulating material liners 302” and “backside insulating layer 306” in Mushiga (shown in blue below) collectively form the claimed *isolation structure*.

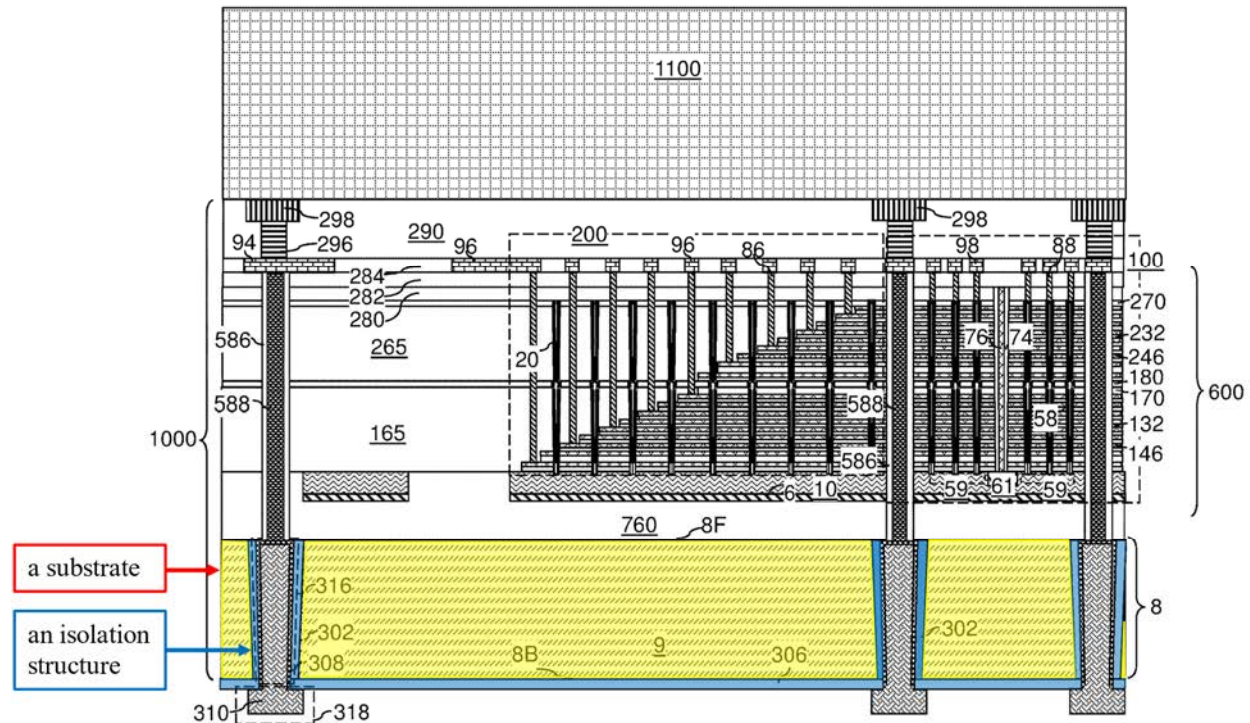


FIG. 11

Ex. 1006, Fig. 11 (annotated). Mushiga’s “insulating material liners 302” and “backside insulating layer 306” are, by their very definitions, insulators. A POSITA would have understood that they serve to isolate various conductive components from electrical interference from the substrate. *Id.*, 14:4-12 (“The first integrated through-substrate via and pad structures (318, 316) ... are electrically isolated from

the first semiconductor substrate 8 by a respective tubular insulating spacer 302 and by a backside insulating layer 306”).

174. Claim element [15.A] requires not only a *substrate* and an *isolation structure*, but *a substrate with an isolation structure*. That Mushiga’s *substrate* (“first semiconductor substrate 8”) is *with* its *isolation structure* (elements 302, 306) is apparent because Mushiga’s *isolation structure* (elements 302, 306) is formed by removing portions of the substrate and is subsequently formed within the *substrate* (“semiconductor substrate 9”). Ex. 1006, Figs. 1B and 2, 8:6-10 (“Referring to FIG. 2, an insulating material liner layer 302L and a sacrificial material layer 303L are sequentially formed in the via openings 301. The insulating material liner layer 302L includes an electrically insulating material such as silicon oxide.”). Mushiga Fig. 9 also illustrates the insulating layer 306 being added. Thus, Mushiga discloses element [15.A].

[15.B] “an alternating conductor/dielectric layer stack disposed on the substrate;”

175. Mushiga discloses element [15.B]. As shown below, Mushiga’s “alternating stack of insulating layers (132, 232) and electrically conductive layers (146, 246)” is *an alternating conductor/dielectric layer stack disposed on the substrate* (“semiconductor substrate 9”):

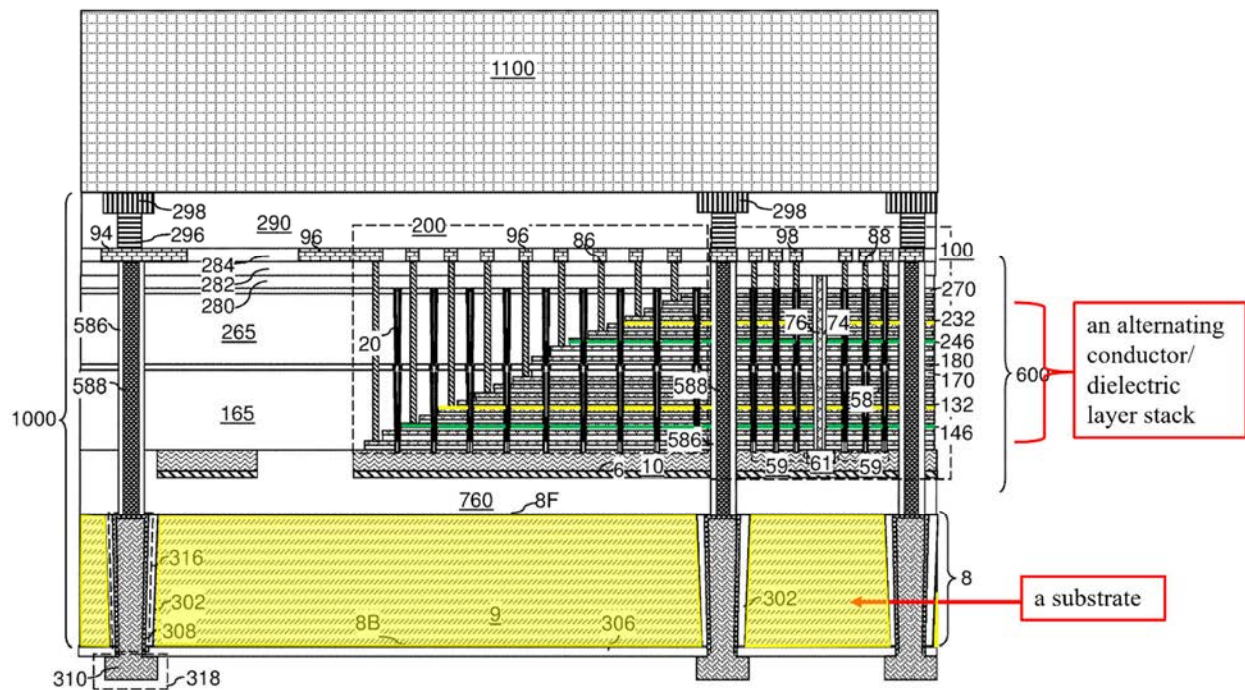


FIG. 11

Ex. 1006, Fig. 11; 8:67-9:2. I note that with respect to the use of the term *on* in this claim element, the '378 specification specifically states that “on” “should be interpreted in the broadest manner such that ‘on’ not only means ‘directly on’ something but also includes the meaning of ‘on’ something with an intermediate feature or a layer therebetween.” Ex. 1001, 4:20-25. Thus, it is of no import whether the alternating conductor/dielectric layers in Mushiga are in direct contact with the substrate 8.

[15.C] “[i] a dielectric structure on the isolation structure and [ii] extending vertically through the alternating conductor/dielectric layer stack, [iii] wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and [iv] the dielectric structure is formed of a dielectric material;”

176. For ease of analysis, I separate this limitation into four sub-parts labelled [i]-[iv] and address how Mushiga satisfies each one in turn.

[15.C.i] “a dielectric structure on the isolation structure”

177. Mushiga discloses this element. Mushiga’s *dielectric structure* is highlighted in orange in Fig. 11 below. It comprises five parts: 760, 165, 180, 265, and 586. At the bottom of the *dielectric structure* is “[a]n insulating material layer 760 including an insulating material such as silicon oxide can be formed over the first substrate semiconductor layer 9.” Ex. 1006, 9:8-10. Above layer 760 is layer 165 (“A first retro-stepped dielectric material portion 165 can be formed on the first stepped surfaces.”). *Id.*, 9:22-24. Next is “inter-tier dielectric layer 180 ... formed above the first alternating stack and the first retro-stepped dielectric material portion 165.” *Id.*, 9:23-25. On top of that is “[a] second retro-stepped dielectric material portion 265.” *Id.*, 9:38-43. Spanning all of these is “an insulating spacer 586 having a tubular configuration at a periphery of each through-memory-level via cavity.” *Id.*, 10:38-43.

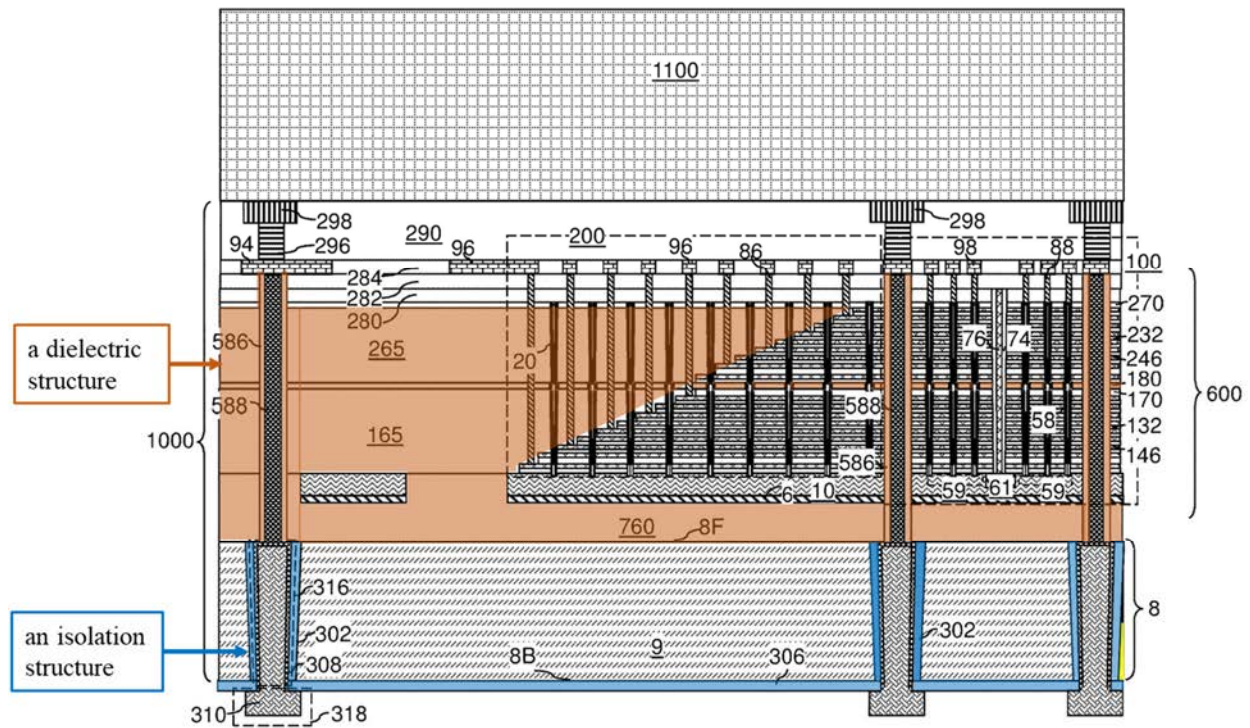


FIG. 11

Id., Fig. 11 (annotated).

178. These indicated layers are *a dielectric structure* because each consists of an insulating material (i.e., a dielectric material). Mushiga teaches that its insulating material layer 760 includes a dielectric material such as silicon oxide. Ex. 1006, 9:8-10, 15:13-32. And both retro-stepped dielectric material portions 165, 265 are similarly made from a dielectric material. *Id.*, 9:22-23, 9:38-39. “[I]nter-tier dielectric layer 180” is, by its own name, a dielectric. Finally, “insulating spacer 586 having” is formed of an “insulating spacer material layer” that is “conformally deposited and anisotropically etched.” *Id.*, 10:38-43. A POSITA would have understood that “insulating spacer 586” was a dielectric material because dielectrics

are commonly made from insulators and Mushiga discloses that various insulating liners are made of silicon oxide. *Id.*, 11:64-66.

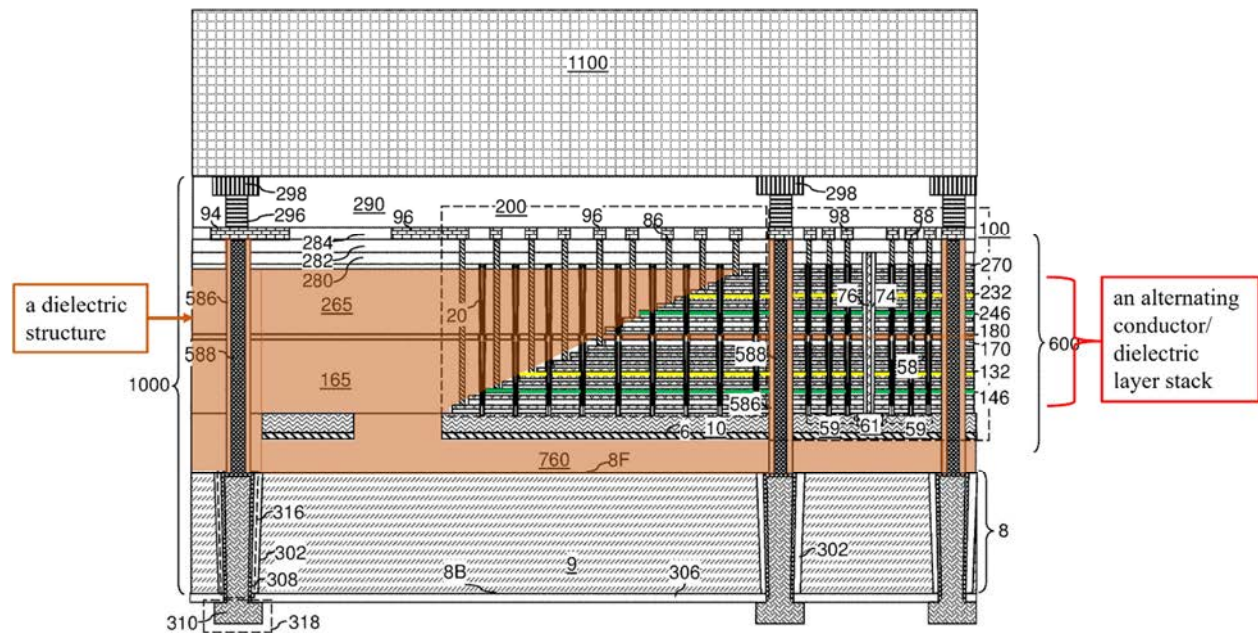
179. Because components 760, 165, 180, 265, and 586 together are something “that is constructed,” they constitute a structure. Ex. 1022, 5 (Merriam-Webster definition of “structure” as “something ([such] as a building) that is constructed”).

180. The '378 patent says the word “on” “should be interpreted in the broadest manner such that ‘on’ not only means ‘directly on’ something but also ... ‘on’ something with an intermediate feature or a layer therebetween.” Ex. 1001, 4:20-29. As shown in Fig. 11 above, “insulating material layer 760” is directly on Mushiga’s *isolation structure* (elements 302, 306). Thus, Mushiga’s *dielectric structure* (elements 760, 165, 180, 265, 586) is **on** its *isolation structure* (elements 302, 306). Moreover, Mushiga’s layers 165, 180, 265, and 586 are also **on** (viz. above) elements 302, 306 even though there may be “an intermediate feature or a layer therebetween.” *Id.*

[15.C.ii] “a dielectric structure ... extending vertically through the alternating conductor/dielectric layer stack”

181. As I just discussed, Mushiga’s elements 760, 165, 180, 265, and 586 together form the claimed *dielectric structure*. And Mushiga’s “alternating stack” is the alternating conductor/dielectric layers (132, 146, 232, 246) as discussed for

element [15.B]. As is apparent in Mushiga Fig. 11 below, Mushiga's *dielectric structure* (elements 760, 165, 180, 265, 586) *extend[s] vertically through the alternating conductor/dielectric layer stack* ("alternating stack" 132, 146, 232, 246):



Ex. 1006, Fig. 11 (annotated).

[15.C.iii] “a dielectric structure ... wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure”

182. Mushiga satisfies this requirement in two ways. Both can be seen in Fig. 11 below. The first is where the “retro-stepped dielectric material portions” 165, 265 are in contact with the alternating conductor/dielectric stack. And the second is where the “insulating spacer 586” meets the alternating stack. Thus, Mushiga discloses *a dielectric structure* (elements 760, 165, 180, 265, 586) *wherein the alternating conductor/dielectric layer stack* (“alternating stack” 132, 146, 232,

246) *abuts a sidewall surface of the dielectric structure* ((1) where “retro-stepped dielectric material portion” 165, 265 meet the alternating stack; and (2) where “insulating spacer 586” meets the alternating stack).

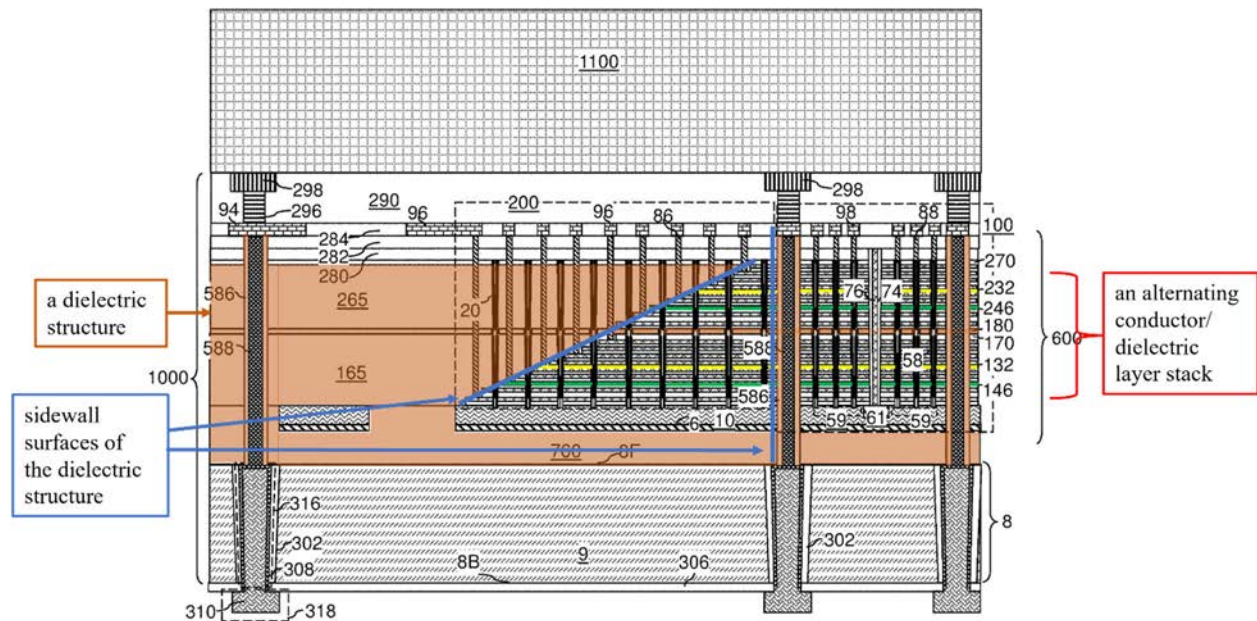


FIG. 11

Ex. 1006, Fig. 11 (annotated).

[15.C.iv] “... wherein ... the dielectric structure is formed of a dielectric material”

183. Mushiga satisfies this requirement. It was well-known in the art that an electrically insulating material in semiconductors refers to a dielectric material. Even non-technical dictionaries reflect the same. *See, e.g.*, Ex. 1022, 3 (Merriam-Webster definition of “dielectric” as “a nonconductor of direct electric current”). As noted above for limitation [15.C.i], each component of Mushiga’s *dielectric structure* (elements 760, 165, 180, 265, 586) *is formed of a dielectric material*, e.g.,

silicon oxide. For example, Mushiga teaches that its insulating material layer 760 includes a dielectric material such as silicon oxide. Ex. 1006, 9:8-10, 15:13-32. And both retro-stepped dielectric material portions 165, 265 are similarly made from a dielectric material. *Id.*, 9:22-23, 9:38-39. “[I]nter-tier dielectric layer 180” is, by its own name, a dielectric. Finally, “insulating spacer 586 having” is formed of an “insulating spacer material layer” that is “conformally deposited and anisotropically etched.” *Id.*, 10:38-43. A POSITA would have understood that “insulating spacer 586” was a dielectric material because it is an insulator and Mushiga discloses that various insulating liners are made of silicon oxide. *Id.*, 11:64-66. Thus, Mushiga teaches this limitation.

184. To the extent that Mushiga does not expressly disclose that any of elements 760, 165, 180, 265, 586 is formed of a dielectric material, it would have been obvious to a POSITA to form that element from a dielectric material, such as silicon oxide, because Mushiga expressly discloses that each of these elements is insulating and/or dielectric. See analysis for claim 19 for further discussion of the obviousness of using silicon oxide for the *dielectric material*.

[15.D] “channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;”

185. For ease of analysis, I separate this limitation into two sub-parts and address each.

[15.D.i] “channel structures ... extending vertically through the alternating conductor/dielectric layer stack”

186. Mushiga satisfies this requirement. Mushiga’s *channel structures* are “memory stack structures 58.” Ex. 1006, 8:67-9:5, 9:50-53 (“A series of processing steps can be sequentially performed 50 to simultaneously form a memory stack structure 58 within each inter-tier memory opening ...”). Mushiga’s “memory stack structures 58” *extend[]vertically through the alternating conductor/dielectric layer stack* (“alternating stack” 132, 146, 232, 246) as shown in Fig. 11 below:

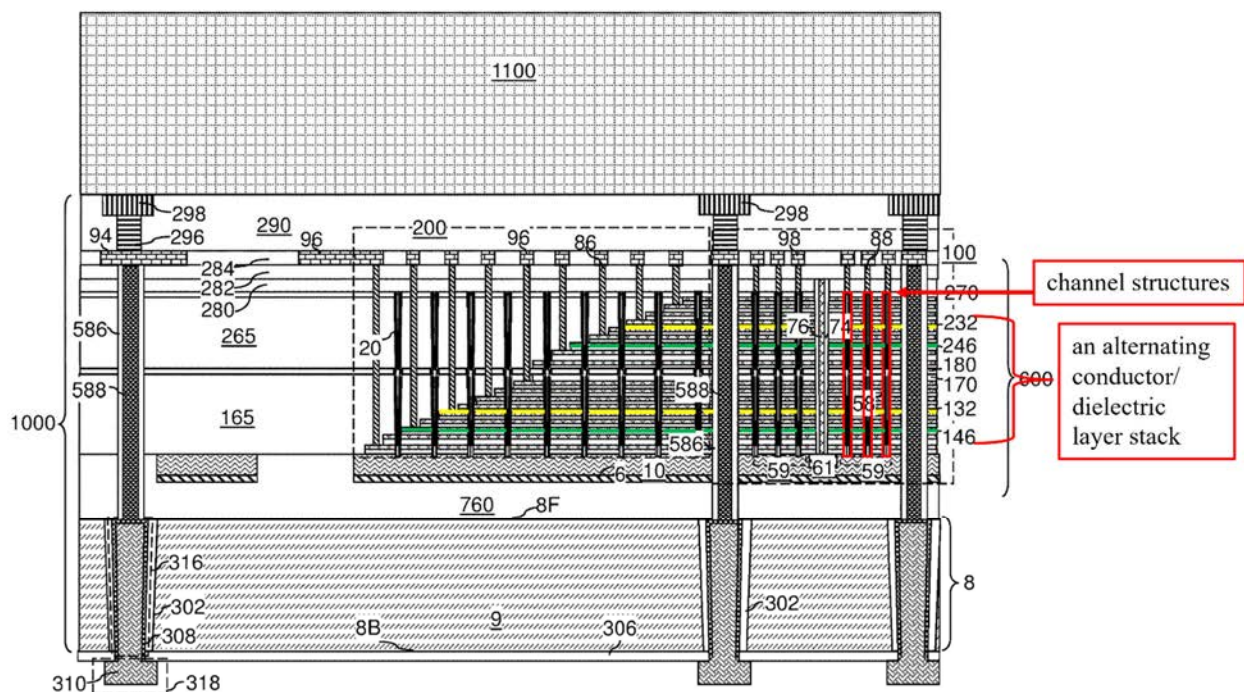


FIG. 11

Id., Fig. 11 (annotated).

187. Moreover, Mushiga’s “memory stack structures 58” are vertical memory strings that perform the same function and are composed of the same

components as the “channel structures” described in the ’378 patent. *See* Ex. 1001, 14:4-31; Ex. 1006, 9:2-4 (“memory stack structures 58 includ[e] a respective vertical stack of memory elements”). In both the ’378 patent and Mushiga, the memory strings are where the data is stored. The ’378 patent’s “channel structures” and Mushiga’s “memory stack structures 58” are also formed of the same components. “Channel structure 216” in the ’378 patent “is filled with semiconductor materials (e.g., as a semiconductor channel 218) and dielectric materials (e.g., as a memory film 220).” Ex. 1001, 9:1-6. Likewise, Mushiga explains that “[e]ach of the memory stack structures 58 ... can include, from outside to inside, a blocking dielectric layer, a charge storage layer, a tunneling dielectric layer, and a vertical semiconductor channel.” Ex. 1006, 9:53-57.

[15.D.ii] “slit structures extending vertically through the alternating conductor/dielectric layer stack”

188. Mushiga satisfies this requirement. The *slit structures* in Mushiga are the “backside contact via structures 76.” Ex. 1006, 10:16-18 (“An insulating spacer 74 and a ***backside contact via structure 76*** can be formed within each backside trench to provide electrical contact to the source regions 61.”) (emphasis added). Mushiga’s “backside contact via structure[s] 76” *extend[] vertically through the alternating conductor/dielectric layer stack* (“alternating stack” 132, 146, 232, 246) as shown in Fig. 11 below:

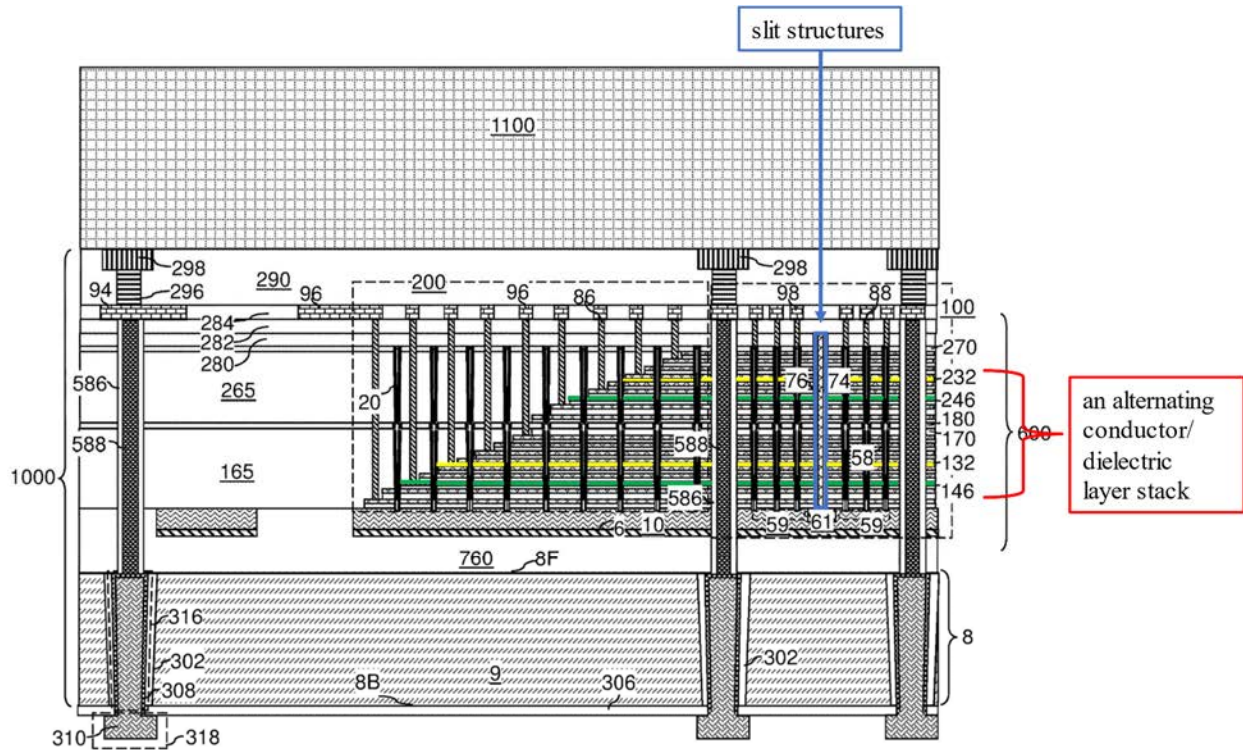


FIG. 11

Id., Fig. 11 (annotated).

189. It is of no import that Mushiga uses slightly different terminology (*viz.*, “backside contact via structures 76”) than the claim to describe its *slit structure*. Mushiga “backside contact via structures 76” are formed by first creating “backside trenches” through the stack of conductors/insulators, and subsequently forming “[a]n insulating spacer 74” and “a backside contact via structure 76” within “each backside trench.” Ex. 1006, 10:1-18.

190. A POSITA would have understood that Mushiga’s “backside trenches” were long, narrow cuts in the alternating stack that extended downward to the substrate. This is consistent with the plain meaning of “trench,” which refers to a

long/narrow groove. See Ex. 1022, 4 (Merriam-Webster definition of “slit” as “a long narrow cut or opening”). And a POSITA would also have understood that the “backside contact via structures 76” formed therein were long and narrow structures—viz., *a slit structure*.

191. Even if the claim limited the process for creating the claimed *slit structures* (which it does not), a POSITA would have recognized that Mushiga’s “backside contact via structures 76” and the ’378 patent’s “slit structures 114” were made in the same way. First, both begin by etching an opening through the alternating stack. Ex. 1001, 16:12-14 (etching “alternating dielectric stack” to form “slit openings”); Ex. 1006, 10:2-5 (etching “alternating stack” to form “[b]ackside trenches”). Next, both replace the sacrificial layers in their respective stacks with electrically conductive layers to form the alternating stack. Compare Ex. 1001, 16:23-30 (“second dielectric layers” in stack “are replaced with conductor layers”) with Ex. 1006, 10:5-10 (“first and second sacrificial material layers ... can be replaced with first ... and second electrically conductive layers”). And the last step in the formation of both structures is to form the slit structure itself. Ex. 1001, 16:57-66 (“slit openings can be filled with a conductor material ... to form slit structures,” and “a dielectric layer ... can be deposited [between the slit structure and the conductor layers]”); Ex. 1006, 10:16-18 (“[a]n insulating spacer 74 and a backside contact via structure 76 can be formed within each backside trench”).

192. If the claim limits the function of the claimed *slit structures* (which it does not), the function of Mushiga’s “backside contact via structures 76” and the ’378 patent’s “slit structures 114” is the same: both structures are the source contact for the memory strings. *Compare* Ex. 1001, 6:25-27 (“some slit structures [] can function as the common source contact for an array ... strings”), 17:3-6 (“slit structure 226 can function as a source contact that is electrically connected to NAND string 204 through doped region 228 of substrate 202”); Ex. 1006, 10:16-18 (“backside contact via structures 76 ... provide electrical contact to source region 61.”).

193. While neither the process for making, nor the function of, the *slit structure* is claimed, the fact that Mushiga’s “backside contact via structure 76” is formed in the same way and performs the same function described in the ’378 specification reinforces my opinion that Mushiga’s “backside contact via structure 76” is *a slit structure*.

[15.E] “a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;”

194. Mushiga satisfies this element. As the name implies, a *staircase structure* has the profile of a staircase. This distinctive profile is apparent in Mushiga Fig. 11 below, which Mushiga calls “stepped surfaces.” Ex. 1006, 9:15-17.

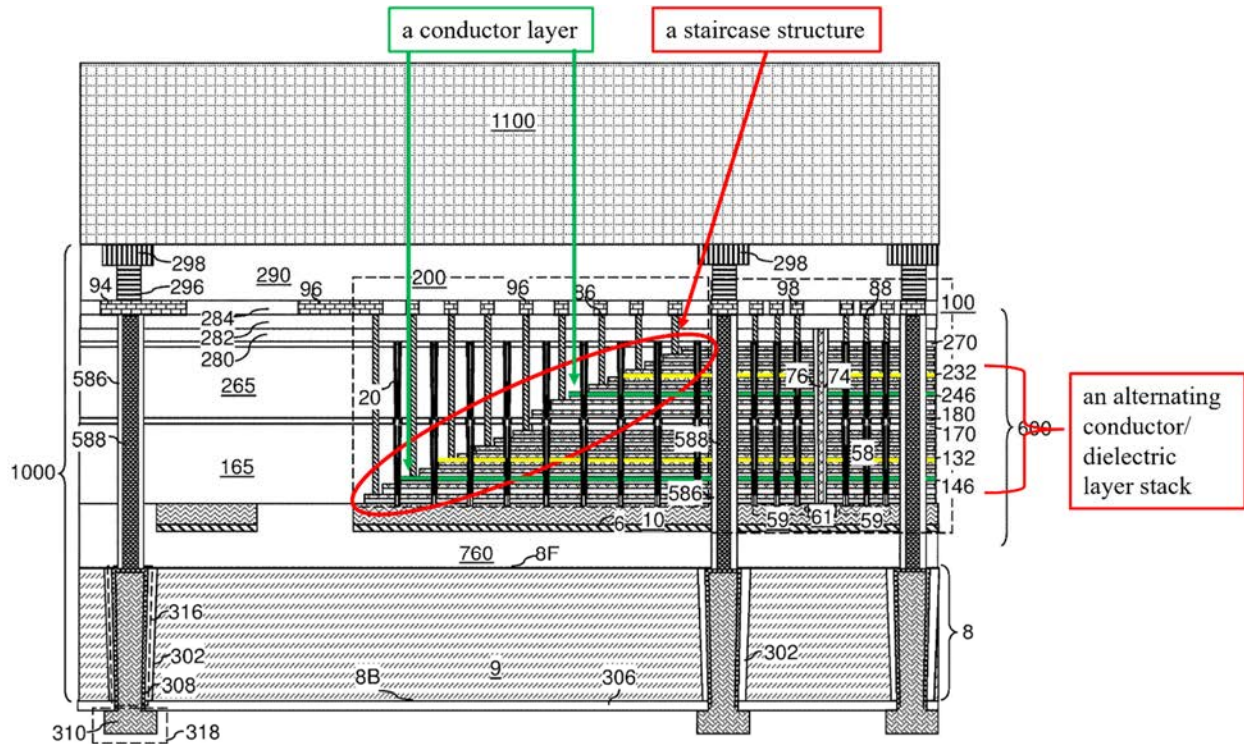


FIG. 11

Id., Fig. 11 (annotated).

195. Mushiga further discloses that its *staircase structure* (“stepped surfaces”) is *disposed in the alternating conductor/dielectric layer stack* (“alternating stack” 132, 146, 232, 246). This is also shown in Fig. 11 above. Mushiga expressly teaches that “[a]t least one alternating stack of insulating layers and sacrificial material layers can be formed with stepped surfaces.” Ex. 1006, 9:15-17. Once the sacrificial material layers are replaced with electrically conductive layers (*id.*, 10:5-10), *the staircase structure* (“stepped surfaces”) is *disposed in the alternating conductor/dielectric layer stack* (“alternating stack” 132, 146, 232, 246) and *comprises levels with each level having a conductor layer* (“electrically

conductive layers (146, 246)"). As can be seen in Fig. 11 above, the staircase contacts extend down to a gate layer and make contact with a gate layer, i.e., a *level* of the *staircase structure*. In the figure above, only representative conductive layers are highlighted to avoid cluttering the image. However, a POSITA would have understood that each level has a conductive layer because it is necessary for each memory cell to be accessible by a wordline control voltage. The vertical contacts are what provide the connections to the horizontal wordlines.

[15.F] "a word line contact disposed on the conductor layer of the each level;"

196. Mushiga discloses this element. Exemplary conductor layers are highlighted in green below in Mushiga Fig. 11. The figure shows *a word line contact* ("word line contact via structures 86," in purple) *disposed on* (in contact with and extending above) *the conductor layer of the each level* ("electrically conductive layers (146, 246)"). I note that not all conductor layers and word line contacts are highlighted in the figure. This was done to avoid making the figure hard to read, but each conductor layer does have a word line contact.

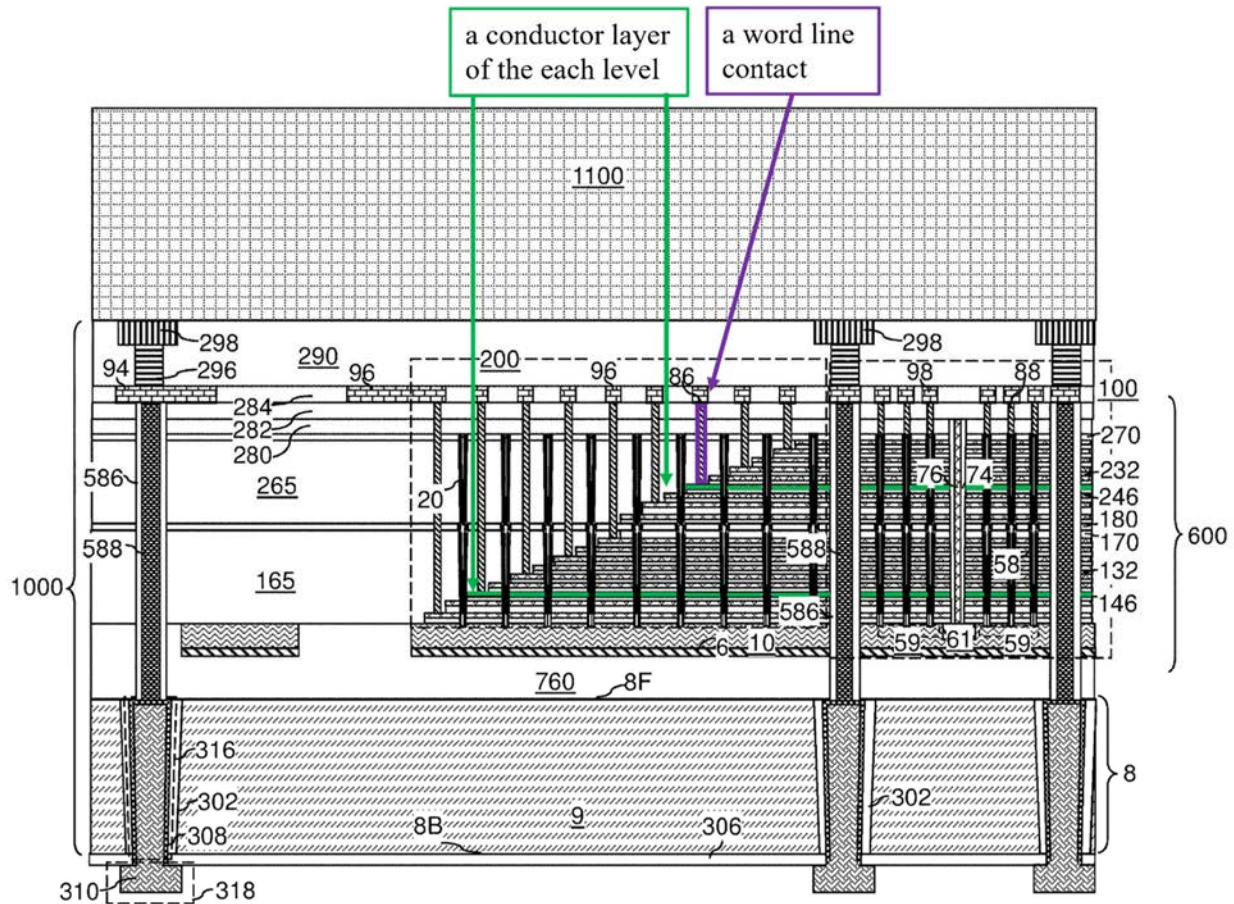


FIG. 11

Ex. 1006, Fig. 11 (annotated); *id.*, 10:21-27 (“The contact via structures can include ... word line contact via structures 86 contacting a top surface of the respective one of the first and second electrically conductive layers (146, 246).”). In other words, there is a word line contact for *each level*. *Id.* As I noted for the previous claim element, a POSITA would have understood that each level has a conductive layer has a wordline contact so that every memory cell can be accessed by a respective wordline. Moreover, it is necessary to be able to apply a pass voltage to each cell (other than the target cell being read which receives a read voltage) in a

memory string to be able to read a target memory cell. It is the wordline contacts that apply the pass voltage (and read) voltages.

[15.G] “local contacts disposed on the channel structures and the slit structures; and”

197. For ease of analysis, I separate this limitation into two sub-parts.

[15.G.i] “local contacts disposed on the channel structures”

198. Mushiga satisfies this requirement. Mushiga’s “drain contact via structures 88” are the claimed *local contacts*. Ex. 1006, 10:21-24 (“The contact via structures can include, for example, drain contact via structures 88 that provide electrical contact to the drain regions located in an upper portion of each memory stack structure”). As shown in Fig. 11 below, Mushiga’s “drain contact via structures 88” are *disposed on* (in contact with and extending above) *the channel structures* (“memory stack structures 58”).

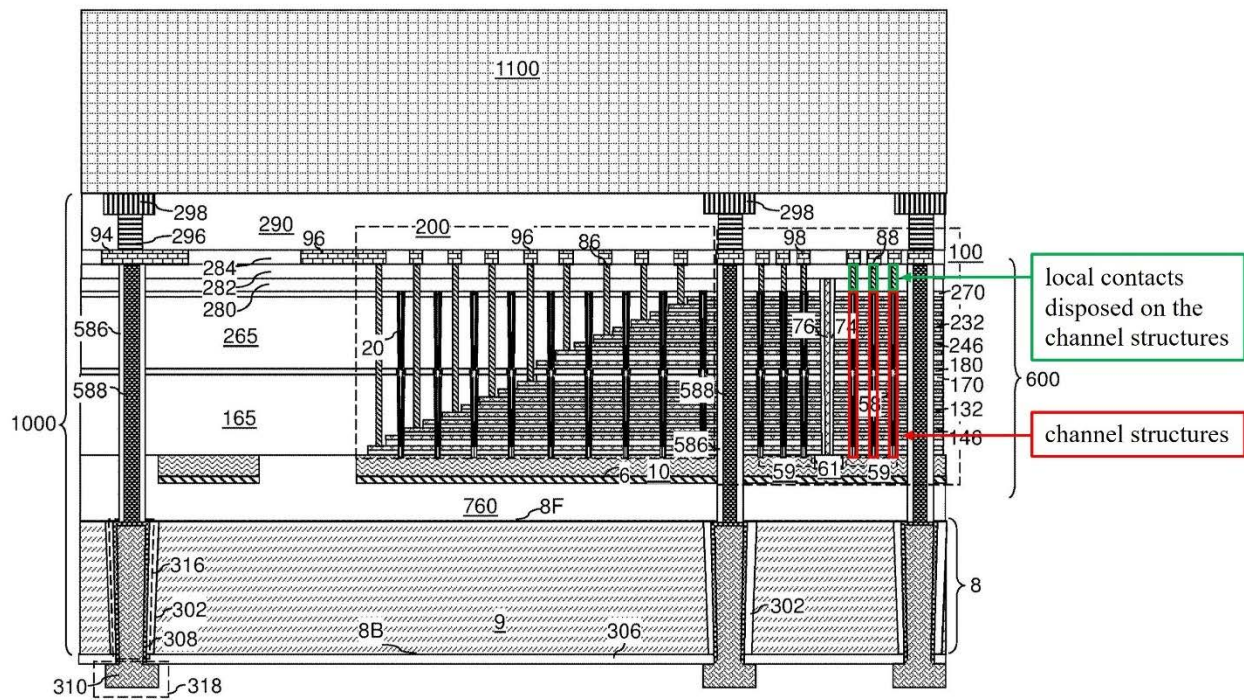


FIG. 11

Ex. 1006, Fig. 11; *id.*, 10:21-27.

[15.G.ii] “local contacts disposed on ... the slit structures”

199. A POSITA would understand that Mushiga has *local contacts disposed on ... the slit structures*, or at least renders such a limitation obvious. To begin, as I discussed in connection with claim limitation [15.D.ii], Mushiga’s “backside contact via structures 76” are the claimed *slit structures*. Mushiga does not expressly disclose *local contacts* on *the slit structures* (“backside contact via structures 76”), but a POSITA would have understood Mushiga to have such *local contacts*. As described for sub-element [15.G.i] above, Mushiga does expressly disclose “contact via structures 88” for the memory strings. A POSITA would have understood that

similar contact via structures would be used in Mushiga to make electrical connections to the slit structures (“backside contact via structures 76”).

200. Mushiga discloses that the “backside contact via structures 76” serve as the source connection for “memory stack structures 58.” Ex. 1006, 10:16-18 (“backside contact via structure 76 ... provide electrical contact to source region 61.”). A POSITA would have been well aware of the function a source connection plays in a 3D memory device—viz., to establish an electrical connection to a low voltage, such as ground. This is true not only in 3D NAND memory devices, but in electronic devices generally. The source and drain terminals in MOSFET transistors are identified by the direction the current flows, which is always higher voltage to lower voltage. I emphasize that the direction of *current* flow is determinative. This is important to keep in mind because electrons are negatively charged and thus flow in the *opposite* direction of current in n-channel MOSFETs. The terminal with higher voltage is called the “drain,” and the lower voltage terminal is called the “source.” The same is true in 3D NAND memory devices, where current flows from the “drain” of a memory string to the “source,” which is typically connected to a low voltage, such as ground. See Ex. 1015, 150 (“the Source Line ... plays the role of the ‘local ground’ for each memory cell.”).

201. A POSITA would have known that a “source line” provides a source connection to the memory stack of a 3D NAND memory device, as can be seen in

the well-known BiCS architecture, where a “source line” (abbreviated “SL”) is located beneath the memory stack:

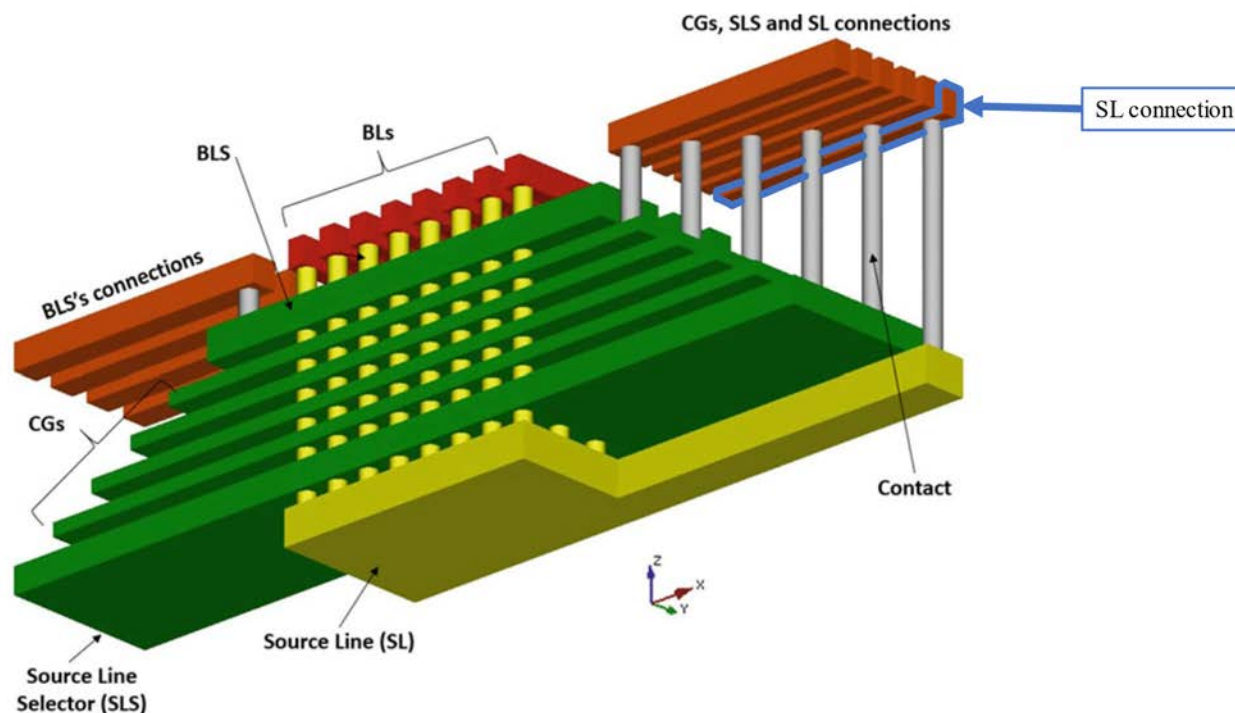


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

Ex. 1015, 110 (Figure 4.14); *see also* Ex. 1016, 275, 288. The “source line” is connected to a vertical source line *contact* (farthest right contact shown in gray above) that extends upward to a source line *connection* (shown in red). The source line connection carries a low voltage (*viz.*, ground) to the source line contact and is, in the terminology of the '378 patent, a *local contact*. Thus, a POSITA would have known that *local contacts* (source line connections) provide a source connection to the memory strings of a 3D memory array.

202. Given a POSITA's knowledge and Mushiga express disclosure of "drain contact via structures 88" for accessing the memory string drain, a POSITA would have understood, or at least found it obvious, that similar *local contact* structures would provide an electrical connection to Mushiga's slit structures ("backside contact via structures 76") so a low voltage, such as ground, could be applied to the memory string source. This would allow a top-level source connection, as shown in the BiCS architecture above. For the same reasons discussed in connection with claim element [15.G] for Toyama's Second Modification (*viz.*, because the local contact does not necessarily extend across the entire surface area of the slit structure), a cross-section taken at a given location in Mushiga may not reveal the presence of a *local contact* on a slit structure. But, a POSITA would understand that taking a cross-section at the appropriate location would show the presence of Mushiga's *local contacts*.

203. Thus, a POSITA would have understood, or at least found it obvious, that Mushiga's NAND memory device includes *local contacts* (source line connections) *disposed on* (in contact with and extending above) *the slit structures* ("backside contact via structures 76"). Moreover, given that Mushiga's "backside contact via structures 76" are intended to serve as source connections and the pillars already extend vertically upward to the top of the memory strings where the local drain contacts for the memory strings are located, it would have been obvious and

desirable to locate the local source contacts for the *slit structures* (“backside contact via structures 76”) on top of (*disposed on*) the *slit structures* as required by the claim. Indeed, this is the most natural location for them given the architecture of Mushiga’s memory device (Ex. 1006, Fig. 11, 10:17-18) and would have been trivial to implement from a manufacturing perspective, leading a POSITA to have more than a reasonable expectation of success in so doing. Thus, the use of *local contacts* (source line connections) *disposed on* (in contact with and extending above) *the slit structures* (“backside contact via structures 76”) is nothing more than the use of a known element (source line connections) to improve a similar device (Mushiga’s 3D memory device) in the same way (provide an electrical link to the top-level source connection).

[15.H] “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.”

204. Mushiga discloses this element. Mushiga’s “through-memory-level via structure[s] 588,” together with their adjoining “through-substrate via structure 316,” are the claimed *through array contacts (TACs)*. Ex. 1006, 10:42-46, 13:3-7. The combination of each “through-memory-level via structure 588” and its corresponding “through-substrate via structure 316” *extend[] vertically through the dielectric structure* (elements 760, 165, 180, 265, 586) *and the isolation structure* (elements 302, 306) as shown in Fig. 11 below.

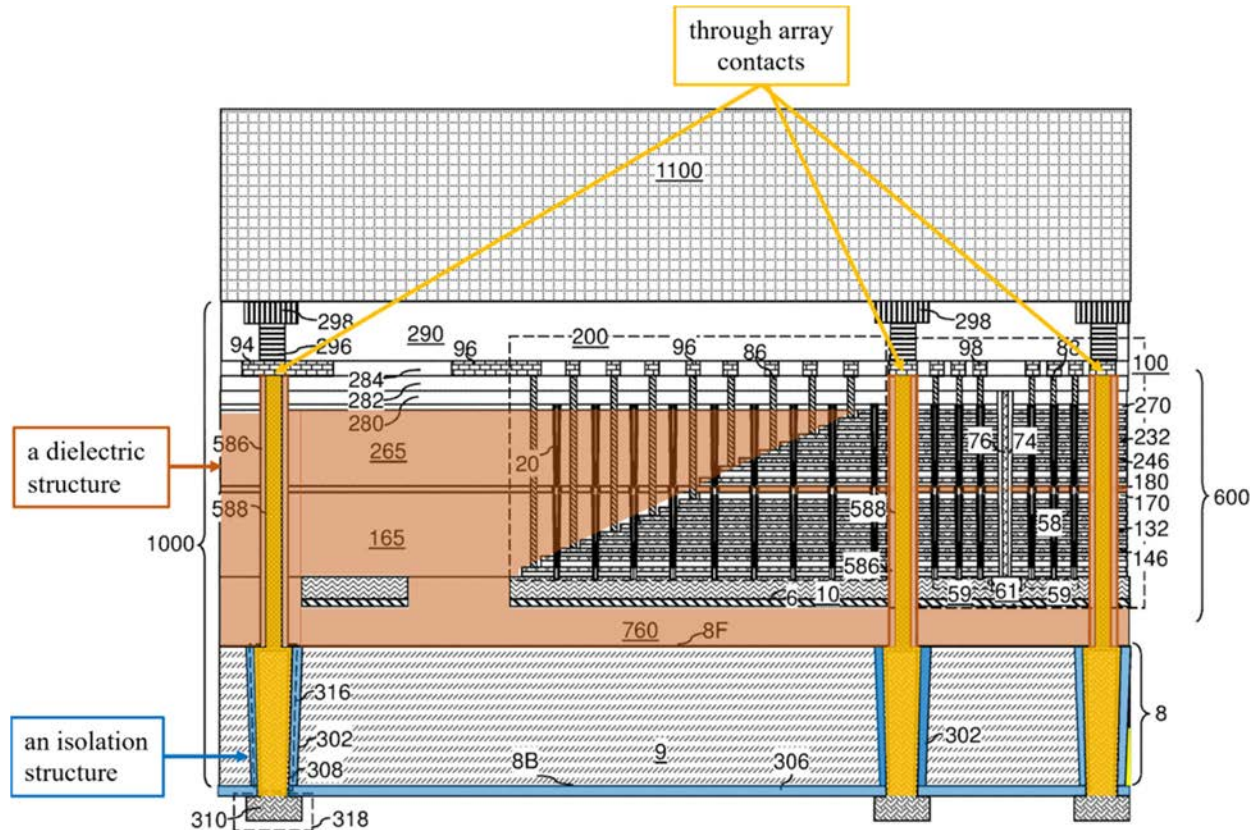


FIG. 11

Id., Fig. 11; *id.*, 10:31-57.

2. Claim 16

[16] “The 3D memory device of claim 15, wherein the dielectric structure abuts a sidewall of each TAC of the TACs.”

205. Mushiga discloses claim 16. In particular, Mushiga discloses that its *dielectric structure* (elements 760, 165, 180, 265, 586) *abuts a sidewall of each TAC of the TACs* (a sidewall of each of the “through-memory-level via structures 588”) as shown in Fig. 11 below:

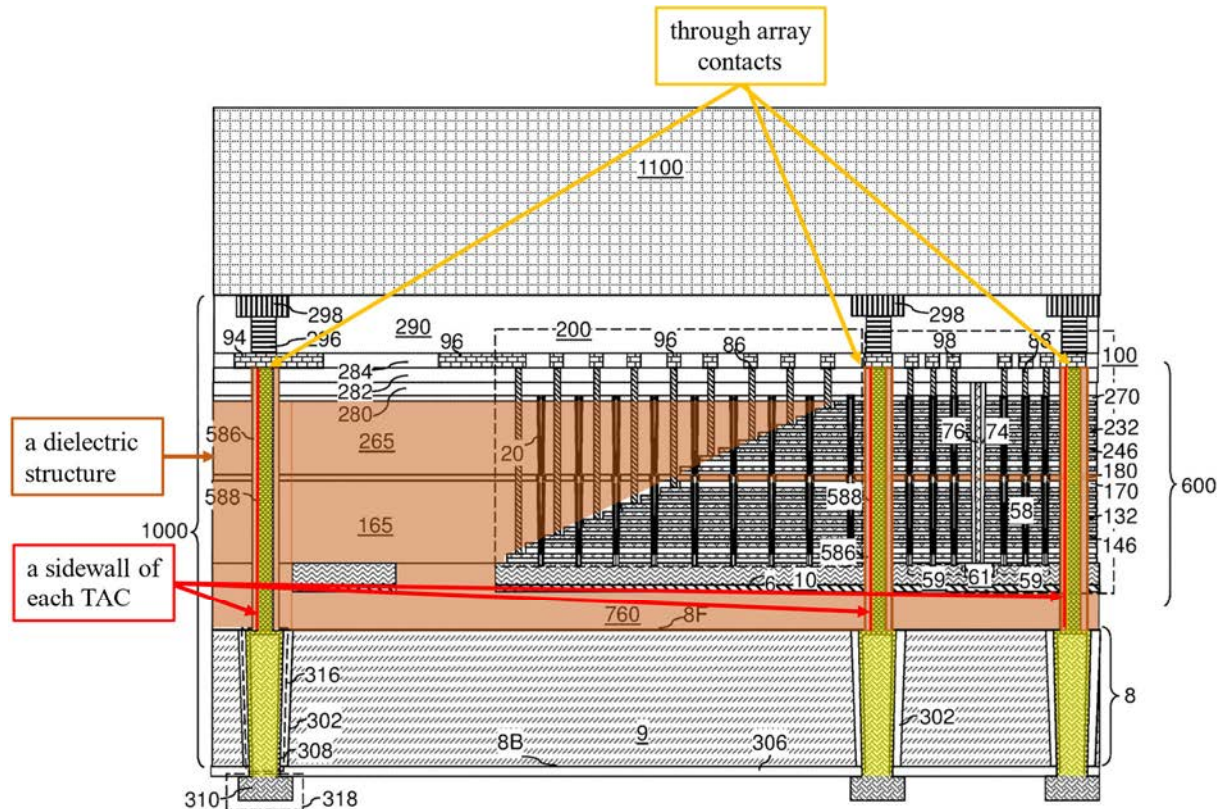


FIG. 11

Ex. 1006, Fig. 11 (annotated); *id.*, 10:31-57.

3. Claim 17

[17] “The 3D memory device of claim 15, wherein the dielectric structure comprises a through array contact region of the 3D memory device.”

206. Mushiga discloses that its *dielectric structure* (elements 760, 165, 180, 265, 586) *comprises a through array contact region of the 3D memory device* as shown below in Fig. 11 with the through array contact region identified in purple:

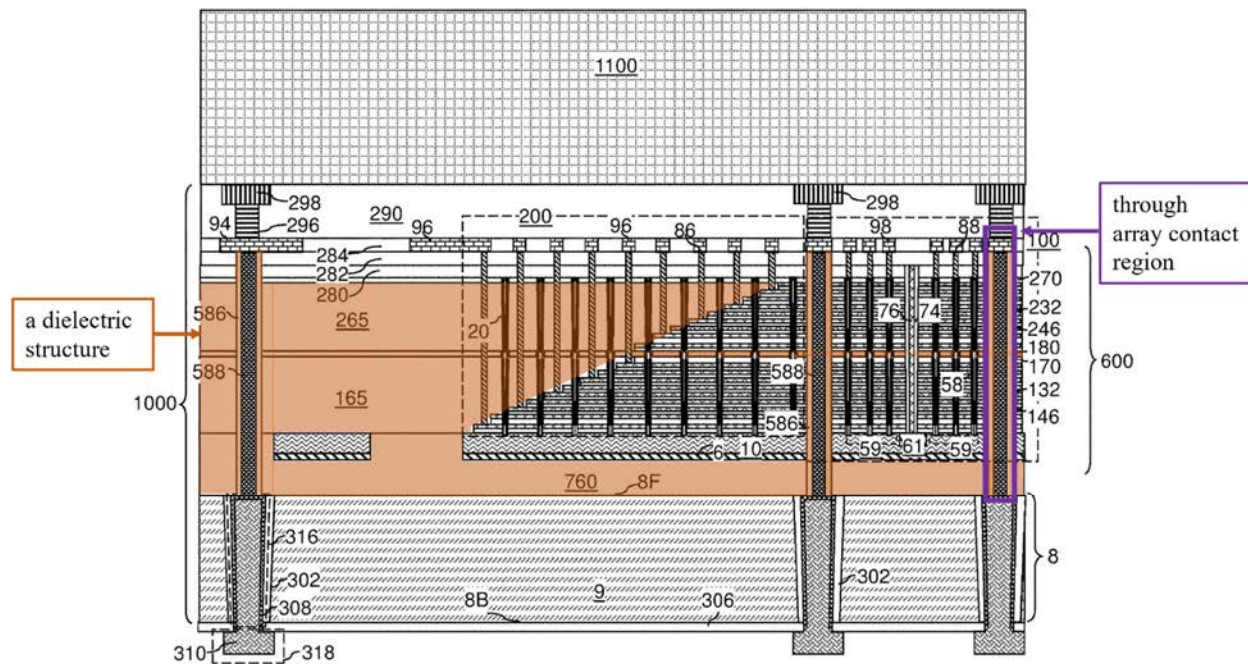


FIG. 11

Ex. 1006, Fig. 11 (annotated); *id.*, 10:31-57. The dielectric structure in Mushiga (elements 760, 165, 180, 265, 586) *comprises a through array contact region of the 3D memory device* because it forms a region through which part of each TAC (“through-memory-level via structure 588”) extends. Thus, Mushiga satisfies claim 17.

4. Claim 19

[19] “The 3D memory device of claim 15, wherein the dielectric material comprises silicon oxide.”

207. As a reminder, elements 760, 165, 180, 265, and 586 in Mushiga comprise the claimed *dielectric structure*. See element [15.C]. Mushiga expressly discloses that one element of its dielectric structure, “insulating material layer 760,”

may consist of silicon oxide. *E.g.*, Ex. 1006, 9:8-10. Mushiga thus teaches this limitation.

208. Even if claim 19 required (which it does not) that all elements of the *dielectric structure* comprise silicon oxide, Mushiga still renders the claim obvious. Even though Mushiga discloses that “insulating material layer 760” may be silicon oxide, Mushiga does not expressly state whether the other elements of its dielectric structure (elements 165, 180, 265, 586) comprise silicon oxide. However, a POSITA would have been motivated to use silicon dioxide because it was and is one of the best-known and most widely used dielectric materials in semiconductor manufacturing, and forming these elements out of silicon oxide would have been obvious to a POSITA. Indeed, for many decades prior to the effective filing date of the '378 patent, silicon oxide was extensively used as an insulating material because of its dielectric properties. *See* Ex. 1019 (U.S. Pat. No. 9,293,348), 2:61-65; Ex. 1020 (U.S. Pat. No. 10,103,169), Figs. 11-12, 3:1-8 and 21:1-61 (discussing “formation of a conformal silicon oxide liner” in 3D-NAND memory devices”); Ex. 1021 (U.S. Pat. No. 8,697,519), 7:30-40. Moreover, Mushiga notes that “silicon oxide” is “an electrically insulating material.” Ex. 1006, 8:8-10. And as discussed for limitation [15.C.i], Mushiga describes each of elements 165, 180, 265, and 586 as being “insulating” or “dielectric.” Thus, it would have been obvious to a POSITA to use silicon oxide to construct each of elements 165, 180, 265, and 586. And

because silicon dioxide is one of the most universally accepted and commonly used dielectrics in semiconductor manufacturing, a POSITA would have had a reasonable expectation of success in using it as the dielectric material in the dielectric layers for which Mushiga does not expressly identify a specific dielectric material.

5. Claim 20

[20] “The 3D memory device of claim 15, wherein the TACs comprise a conductive material.”

209. Mushiga discloses claim 20. For example, Mushiga states that “[a]t least one conductive material, such as a combination of a metallic liner and a metal fill material (e.g., tungsten) can be deposited in remaining volumes of the through-memory-level via cavities to form through-memory-level via structures 588.” Ex. 1006, 10:42-46; *see also id.*, 13:25-29 (“The first through-substrate via structure 316 includes vertically extending portions of the metallic liner 308L and the metal fill material layer 310L that are embedded within the first semiconductor substrate 8 and the backside insulating layer 306.”). As was well-known to POSITAs, metal is a conductive material. Mushiga thus teaches that multiple components of *the TACs* (“through-memory-level via structure 588” and “through-substrate via structure 316”) each *comprise a conductive material*.

D. Ground 3: Mushiga Combined with Makala and the Knowledge of a POSITA

1. Claim 15

210. Ground 3 is the same as Ground 2, except that Ground 3 additionally relies on Makala's disclosure for claim limitation [15.G.ii], *local contacts disposed on the slit structures*. See generally Part **Error! Reference source not found..C**, above. As I discuss below, Mushiga and Makala in view of a POSITA's knowledge also discloses limitation [15.G.ii].

211. Makala discloses a "three-dimensional memory device" strikingly similar to Mushiga's "first semiconductor devices 600." For example, Makala discloses an "alternating stack (132, 146, 232, 246)" of insulating and conducting layers (Ex. 1007, 32:8-30) just like Mushiga's "alternating stack of insulating layers (132, 232) and electrically conductive layers (146, 246)" (Ex. 1006, 8:67-9:2, Fig. 11).

212. As another example, Makala discloses *channel structures* just like Mushiga. Compare Ex. 1007, 29:4-8 ("The memory stack structure 55 is a combination of a semiconductor channel, a tunneling dielectric layer, a plurality of memory elements as embodied as portions of the charge storage layer 54, and an optional blocking dielectric layer 52.") with Ex. 1006, 9:2-4 ("memory stack structures 58 includ[e] a respective vertical stack of memory elements"), 9:53-57 ("Each of the memory stack structures 58 ... can include, from outside to inside, a

blocking dielectric layer, a charge storage layer, a tunneling dielectric layer, and a vertical semiconductor channel.”) Ex. 1006, 9:53-57.

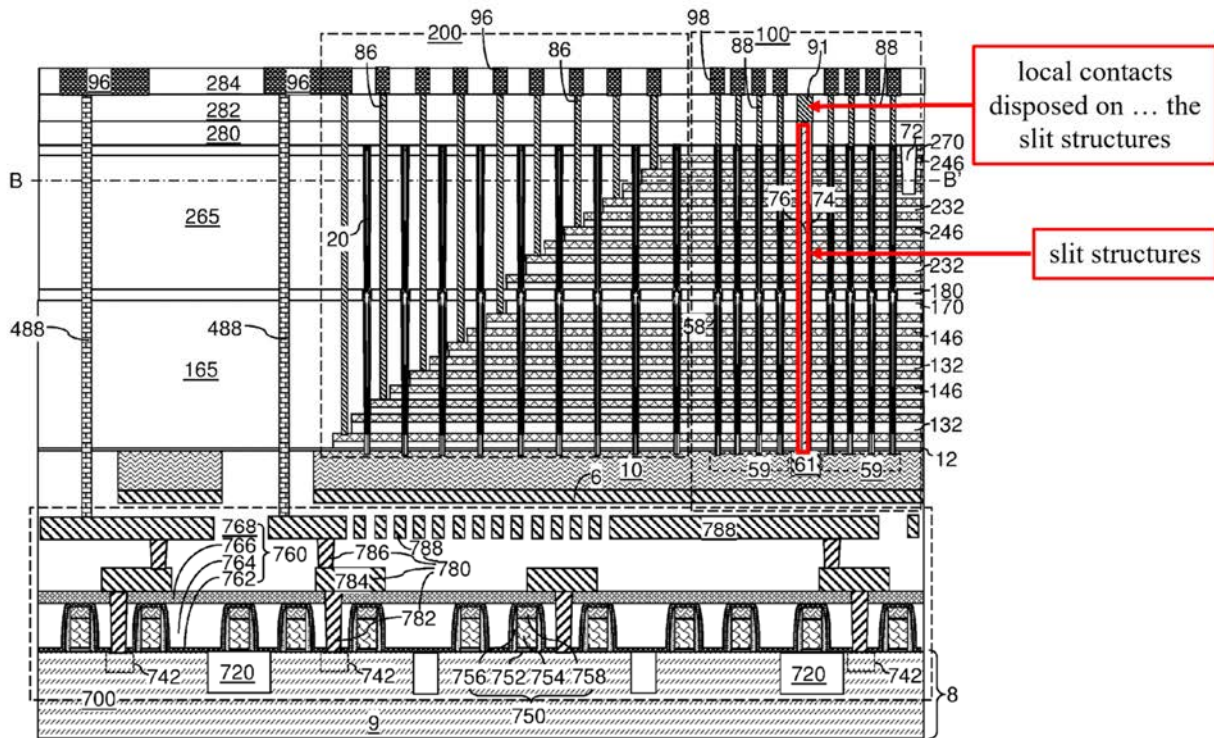
213. As a third similarity, Makala discloses *a staircase structure* substantially identical to Mushiga. *Compare* Ex. 1007, 19:35-38 (describing “first stepped surfaces in the word line contact via region 200”), 22:48-53 (describing “[s]econd stepped surfaces in the second stepped area can be formed in the word line contact via region 200”) with Ex. 1006, 9:15-17 (“At least one alternating stack of insulating layers and sacrificial material layers can be formed with stepped surfaces”).

214. As a fourth example of the architectural similarities, Makala discloses *a word line contact* similar to Mushiga. *Compare* Makala’s “word line contact via structures 86” (Ex. 1007, 33:47-49) with Mushiga’s “word line contact via structures 86”) (Ex. 1006, 10:21-27).

215. The last example I will highlight is that both Makala and Mushiga disclose similar *slit structures*. *Compare* Ex. 1007, 32:53-33:3 (“laterally-elongated contact via structures 76”) with Ex. 1006, 10:1-18 (“backside contact via structures 76”).

216. At this point, I now discuss Makala’s disclosure of *local contacts* (“source connection via structures 91”) *disposed on* (in contact with and extending above) *the slit structures* (“laterally elongated contact via structures 76”). The

analysis is straightforward. Makala Fig. 16 below illustrates a source connection via structure 91 (*local contact*) that is in contact with and located on top of (i.e., *disposed on*) the laterally elongated contact via structure 76 (*slit structure*).



Ex. 1007, Fig. 16 (annotated).

217. The claim requires plural *local contacts* and *slit structures*, but Makala expressly discloses that “[a]dditional line level metal interconnect structures that are not expressly illustrated can include source connection line structures that contact the source connection via structures 91 to provide electrically conductive paths for biasing the source region 61 through the laterally-elongated contact via structures 76.” Ex. 1007, 34:27-33; *see also id.*, 33:40-42.

218. A POSITA would have found it obvious to integrate Makala's teaching of "source connection via structures 91" with Mushiga's memory device. In particular, Mushiga's "backside contact via structures 76" (Ex. 1006, 10:16-18) serve as the source connection for the memory stack, like Makala's "laterally-elongated contact via structures 76." Whereas Mushiga only implies how its "via structures 76" connect to their source, Makala expressly teaches that its "via structures 76" connect to "source connection via structures 91." Ex. 1007, 34:27-33. Thus, Makala simply provides express disclosure for a common and straightforward way of electrically connecting *slit structures*. Makala's teaching is directly applicable to Mushiga.

219. A POSITA would have been motivated to incorporate Makala's teachings about *local contacts* because a POSITA would have understood that, to be electrically operative, Mushiga's "via structures 76" would need to be electrically connected to a source line. And Makala's "source connection via structures 91" expressly provide for just that. Applying Makala's teaching requires nothing more than conventional semiconductor processing techniques (*e.g.*, depositing a conductor such as metal and stand etch steps) that have been known for decades. Thus, a POSITA would have had a reasonable expectation of success in integrating Makala's teaching of "source connection via structures 91" with Mushiga's device

because, as I discussed above, Makala’s three-dimensional memory device” is nearly the same as Mushiga’s “first semiconductor devices 600.”

2. Claims 16-17 and 19-20

220. I do not rely on Makala for any limitations in claims 16-17 or 19-20 (other than element [15.G.ii] in underlying base claim 15). Thus, Mushiga and Makala in view of a POSITA’s knowledge renders obvious claims 16-17 and 19-20 for the same reasons discussed in Sections IX.C.2-IX.C.5.

E. Secondary Considerations of Non-Obviousness

221. Based on my review of the ’378 patent’s file history, I note that no secondary considerations of non-obviousness were identified in connection with the patent’s claims. Nor am I otherwise aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like relating to the ’378 patent. Instead, as discussed above, it is my opinion that the subject matter embraced by the challenged claims was known in and obvious over the prior art.

Petition for *Inter Partes* Review of U.S. Patent No. 10,658,378
Declaration of Dr. Jack C. Lee

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: April 30, 2024

Location: Austin TX

Signature: 
DR. JACK C. LEE