

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case No.: IPR2024-00788
U.S. Patent No. 10,658,378

**PATENT OWNER'S PRELIMINARY RESPONSE
UNDER 37 C.F.R. § 42.107**

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LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	Micron 4-2 Claim Construction Disclosure
Ex. 2002	YMTC 4-2 Claim Construction Disclosure

LIST OF ABBREVIATIONS

Abbreviation	Term
'378	U.S. Pat. No. 10,658,378
'378FH	File History of U.S. Pat. No. 10,658,378
Challenged Claims	Ex. 1001, Claims 15-17, 19-20
Office	U.S. Patent and Trademark Office
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,658,378 (IPR2024-00788, Paper 1)
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner or PO	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Toyama	U.S. Patent Publication No. 2017/0179026
Mushiga	U.S. Patent No. 10,354,980
Makala	U.S. Patent No. 10,262,945

Pursuant to § 42.107,¹ Patent Owner submits this Preliminary Response to the above-captioned Petition, which should be denied in its entirety based on Petitioner's failure to show a reasonable likelihood of prevailing on any asserted ground as to any Challenged Claim.

I. INTRODUCTION

U.S. Patent No. 10,658,378 ("the '378," Ex. 1001) is directed to a novel three-dimensional (3D) memory device having through array contacts and methods related to manufacturing such a device. As memory cells are scaled down and the density of memory cells increases, it becomes challenging to collect and route signals to the peripheral circuitry efficiently. The '378 provides a solution by forming through array contacts (TACs) in a dedicated region where they provide vertical interconnects to the peripheral devices. '378, 1:20-32, 2:19-21, 5:46-50, 11:3-9, 19:55-60.

Fabrication of 3D NAND memory devices generally involves stacks of alternating dielectric and conductive layers, through which vertical structures, such as channels and vias, are formed. '378, 1:38-55. The prior art at the time of filing

¹ All emphasis and color annotations herein are added, and all statutory and regulatory citations are to either 35 U.S.C. or 37 C.F.R., as the context indicates, unless otherwise stated.

of the '378 formed vertical vias within the alternating dielectric and conductive layers, which “increases the fabrication cost.” ’378, 10:59-66, 18:27-33. The '378 simplifies the fabrication process of these through array contacts by forming them in a dedicated dielectric structure. ’378, 18:27-33. The '378 thereby avoids the issues in prior art such as using a complex and costly etching process due to having to etch through alternating dielectric and conductive layers. ’378, 5:35-39, 10:59-66, 18:27-41, 20:9-16. The '378 further utilizes an isolation structure (*e.g.*, a “shallow trench isolation”) in the substrate on which the dielectric structure is placed and through which the lower portions of the TACs extend. ’378, 10:30-33, 21:17-25.

The '378 introduced a 3D memory device in which TACs “extend vertically through” the “dielectric structure” and the “isolation structure,” and methods of manufacturing such a device. ’378, Abstract, 10:57-59, 21:17-25. The claimed invention recites “a substrate with an isolation structure,” a “dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack,” and “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.” *See* ’378, Claim 15. As a result, the claimed invention avoids the issues arising from forming TACs through alternating dielectric/conductor stacks and “simplif[ies] the fabrication process and reduce[s] the fabrication cost.” ’378, 18:36-41.

As an initial matter, the Board should exercise its discretion to deny institution under § 325(d) because the same art (Toyama) was expressly considered during prosecution, Petitioner's other art (Mushiga and Makala) are substantially the same as Toyama, and Petitioner has not shown Examiner error.

In addition, institution should be denied because the Petition fails to establish a reasonable likelihood of prevailing with respect to the Challenged Claims. Petitioner does not assert that any of the cited references anticipates the Challenged Claims. Instead, Petitioner raises obviousness based on a mix of contradictory assertions, faulty analysis, and conclusory testimony from its expert.

Petitioner's Ground 1 relies on the "Toyama" reference (Ex. 1005) for each limitation of the Challenged Claims, but Petitioner fails to show that Toyama discloses each and every limitation of claim 15 (the sole challenged independent claim). In particular, Toyama does not disclose or render obvious "a substrate with an isolation structure," "a dielectric structure on the isolation structure," and "through array contacts (TACs) extending vertically through the dielectric and the isolation structures" as required by the Challenged Claims. Petitioner's arguments for obviousness are founded on faulty mappings that, for example, improperly attempt to divide Toyama's unitary elements to show multiple claim elements that have a claimed spatial relationship and perform unique functions, or attempt to group together physically separated elements in Toyama to meet claim requirements that

must be met by a single claimed structure in the '378 under binding Federal Circuit law.

Petitioner's Ground 2 relies on the "Mushiga" reference (Ex. 1006) for each limitation of the Challenged Claims, but Petitioner fails to show that Mushiga discloses or renders obvious at least the limitations reciting "a substrate with an isolation structure," "a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material," and "through array contacts (TACs) extending vertically through the dielectric and the isolation structures." Petitioner's arguments for obviousness are subject to the same failings as Toyama, and are again founded on faulty mappings that, for example, inconsistently include or exclude features of Mushiga's device based on hindsight.

Petitioner's Ground 3 applies certain teachings of the "Makala" reference (Ex. 1007) to Mushiga but only as to a particular requirement of claim 15. Specifically, Petitioner does not raise any new arguments as to the aforementioned limitations and instead relies on its Ground 2 arguments (Pet. 102). Therefore, Petitioner's arguments fail for at least the reasons provided regarding Petitioner's Ground 2.

Because each prior art, individually or combined, fails to disclose or render obvious at least one limitation of the Challenged Claims, the Board should deny institution.

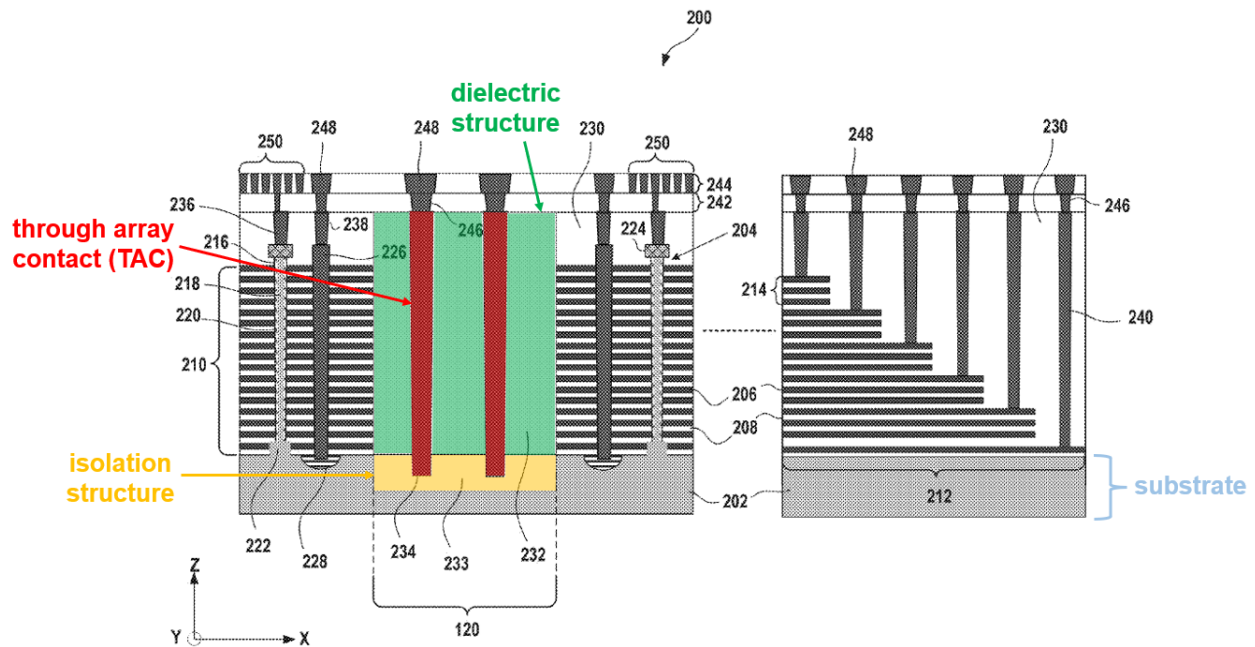
II. THE CLAIMED INVENTION OF THE '378 PATENT

The claimed invention of the '378 is directed to a “three-dimensional (3D) memory device” and related methods that addresses issues arising from the fabrication techniques known in the prior art and as a result, “simplif[ies] the fabrication process and reduce[s] the fabrication cost.” '378, Abstract, 18:36-41.

Specifically, the '378 is directed to an improved 3D memory device and methods for forming such a device in which “through array contacts (TACs)” “extend vertically through” the “dielectric structure” and the “isolation structure.” Ex. '378, Abstract, 10:57-59, 21:17-25. 3D memory devices in the prior art at the time of filing of the '378 involved through array vias that form connections between various components of the device in order to reduce the size and increase density. '378, 1:20-32. These vias were placed within the alternating dielectric and conductive layers, which required a complex etching process and “increase[d] the fabrication cost.” '378, 10:59-66.

The novel device and methods the '378 teaches and recites in the claims is characterized by “a **substrate** with an **isolation structure**” and **TACs** that “extend vertically through” the “**dielectric structure**” and the “**isolation structure**.” '378,

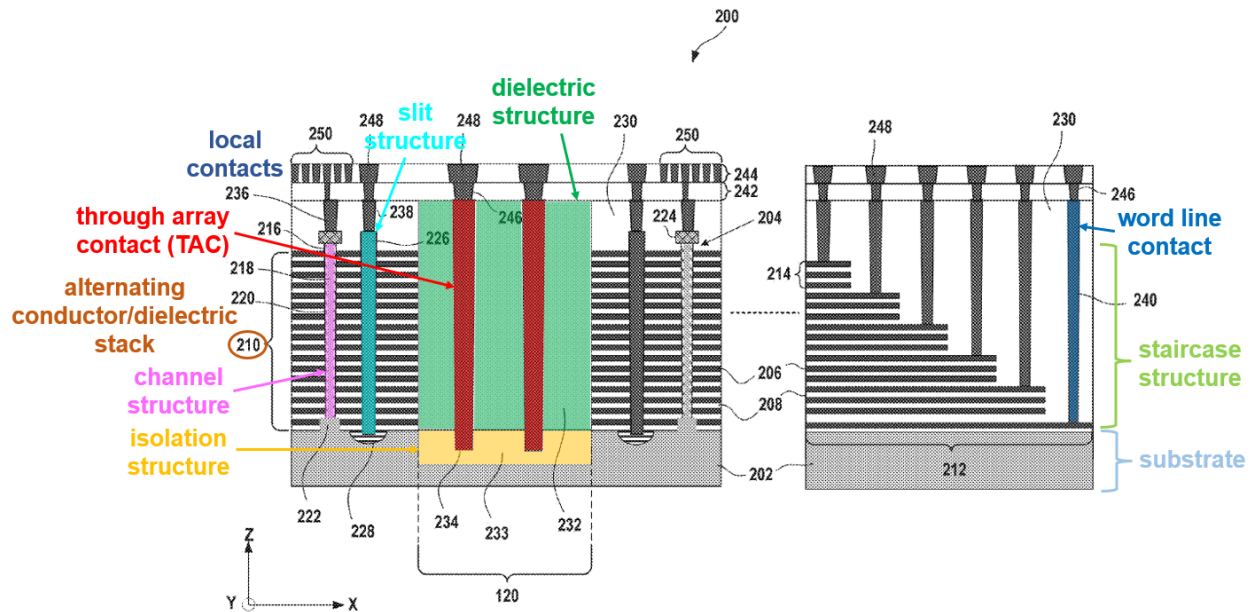
Abstract, 10:57-59, 21:17-25, Claim 15. This novel configuration of elements allows for easier and less costly manufacture of 3D memory devices. '378, 5:55-59, 18:27-33, 20:29-37.



'378, Fig. 2 (annotated).

A representative embodiment of the '378's memory device includes: (1) "substrate 202" with "isolation structure 233" ('378, 10:30-35, 22:27-38); (2) "alternating conductor/dielectric layer stack 210" ('378, 8:17-25); (3) "dielectric structure 232" on "isolation structure 233" ('378, 10:18-29); (4) "channel structures 216" and "slit structures 226" extending vertically through "alternating conductor/dielectric layer stack 210" ('378, 9:1-6, 10:1-6); (5) "staircase structure 212" ('378, 8:48-55); (6) "word line contacts 240" (11:24-26); (7) "local contacts" on "channel structures 216" and "slit structures 226"

(11:24-26); and (8) “**TACs 234**” extending vertically through “**dielectric structure 232**” and “**isolation structure 233**” (’378, 10:57-59, 20:45-48). A cross-section view of the memory device is below.



’378, Fig. 2 (annotated).

The only independent claim of the Challenged Claims, claim 15, is directed to aspects of the above-described invention:

[15.pre] A three-dimensional (3D) memory device, comprising:

[15.a] a substrate with an isolation structure;

[15.b] an alternating conductor/dielectric layer stack disposed on the substrate;

[15.c] a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer

stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

[15.d] channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;

[15.e] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

[15.f] a word line contact disposed on the conductor layer of the each level;

[15.g] local contacts disposed on the channel structures and the slit structures; and

[15.h] through array contacts (TACs) extending vertically through the dielectric and the isolation structures.

III. FILE HISTORY

The claims of the '378 remain patentable over the prior art for at least the same reason identified during prosecution. As discussed further below in § VII, the prior art does not disclose or render obvious, *inter alia*, the '378 claim elements “a substrate with an isolation structure,” “a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of

the dielectric structure and the dielectric structure is formed of a dielectric material,” and “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.” Claims directed to these limitations were allowed after thorough prosecution and consideration of numerous prior art references.

The '378 was filed on July 27, 2018. After a preliminary amendment Applicant filed to remove multiple claim dependency and correct a typographical error, the application included 3 independent claims (pending claims 1, 10, and 16) and 17 dependent claims (pending claims 2-9 which depend from claim 1, claims 11-15 which depend from claim 10, and claim 17-20 which depend from claim 16). Ex. 1002, 105-111 (12/06/2018 Preliminary Amendment).

In a non-final office action, the Examiner rejected pending claims 1, 3-16, and 18-20 under 35 U.S.C. 103 as being allegedly obvious over U.S. Patent 9,620,512 (“Nishikawa”) in view of U.S. Patent Publication No. 2016/0056188 (“Lee”), but found that pending claims 2 and 17 “would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.” Ex. 1002, 529-537 (08/22/2019 Office Action).

Applicant followed the Examiner’s suggestion “[w]ithout acquiescing to the propriety of the rejection” and rewrote pending claims 2 and 17 in independent form. Applicant also amended pending claim 10 “[w]ithout acquiescing to the propriety of the rejection” to “recite features that further distinguish it from Nishikawa and Lee.”

Having placed the independent claims in allowable form, Applicant requested that their respective dependent claims also be allowed. Applicant further added two new claims that depend from pending claim 16. Ex. 1002, 563-571 (12/23/2019 Amendment and Reply). The Examiner subsequently allowed all pending claims. Ex. 1002, 579-586 (01/13/2020 Notice of Allowance). The '378 issued on May 19, 2020 with twenty claims, including the renumbered independent claims 1, 9, and 15. Ex. 1002, 602 (04/29/2020 Issue Notification).

After the first office action and before Applicant's response, Applicant filed an information disclosure statement (IDS) that notified the Examiner of U.S. Patent Publication No. 2017/0179026 ("Toyama"). Ex. 1002, 555 (12/03/2019 Information Disclosure Statement). The Examiner considered Toyama and explicitly cited it as a "reference[] considered." Ex. 1002, 593 (01/13/2020 List of References Cited by Applicant and Considered by Examiner). Petitioner's assertion that "Patent Owner only gave Examiner a haystack" is belied by the fact that Applicant submitted an IDS solely to cite Toyama, which was then explicitly considered by the Examiner. Moreover, the '378 was issued with only sixteen references (nine U.S. patent documents and six foreign patent documents) one of which is Toyama. '378, (56). Thus, the Examiner duly considered Toyama, but found it lacking.

IV. CLAIM CONSTRUCTION

The Board construes claim terms “using the same claim construction standard that would be used to construe the claim in a civil action.” § 42.100(b). Under this standard, claim terms are “generally given their ordinary and customary meaning” to a person of ordinary skill in the art. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). A POSITA ascertains the meaning of the claims based on the claim language, specification, prosecution history, and relevant extrinsic evidence, although the claims and patent specification are the primary sources for construing claims. *Id.*, 1314-16.

The Petition asserts that “the terms of the ’378 Patent’s claims do not require further construction and can be afforded their plain and ordinary meaning.” Pet. 27. Patent Owner proposes a construction for the claim term “through array contact (TAC)” according to its plain and ordinary meaning, as explained further below. Patent Owner reserves the right to modify its proposed construction and to raise further claim construction issues if the Board institutes IPR, and to raise claim construction issues in the underlying district court proceedings.

The parties recently exchanged proposed claim constructions in the parallel district court proceeding. Exs. 2001 (“Micron 4-2 Claim Construction Disclosure”); 2002 (“YMTC 4-2 Claim Construction Disclosure”). With the exception of the term “through array contact (TAC),” the claim construction disputes in district court do

not impact the issues raised in this Preliminary Response. For the term “through array contact (TAC),” Patent Owner presents the same construction in both proceedings. Ex. 2002 at 7-8.

A. “through array contact (TAC)” (Claims 15-17)

The term “through array contact (TAC)” is a limitation of all Challenged Claims because it occurs in claim 15, which is the only independent claim among the Challenged Claims of the ’378 Patent. It is further recited in claims 16-17.

The term “through array contact (TAC)” should be construed according to its plain and ordinary meaning which is “a contact that goes through an array.” This construction is both consistent with the plain and ordinary meaning of the term and is supported by the intrinsic evidence. For example, the TACs in the ’378 go through an array of channel structures (*see* Ex. 1001, Figs. 1A-B, showing TACs 126 going through “memory array structures” including “channel structures 122”) or an array of word line contacts (*see* Ex. 1001, Fig. 1C, showing TACs 126 going through “an array of WL contacts 142”). Ex. 1001, 6:11-7:4.

V. BACKGROUND OF THE ASSERTED PRIOR ART

A. U.S. Patent Publication No. 2017/0179026 (“Toyama”) (Ex. 1005)

Petitioner does not contend that Toyama anticipates the Challenged Claims, and instead argues only that it renders obvious the Challenged Claims in view of the knowledge of a POSITA. Pet. 6, 28-77.

Toyama teaches a 3D NAND memory device with four exemplary structures and their modifications. Ex. 1005, [0004]. Only two of these exemplary structures are relied on by Petitioner: (1) “the ‘first exemplary structure,’ illustrated in Figures 1A-B to 17A-F,” and (2) “the ‘second modification of the fourth exemplary structure,’ illustrated in Figures 44A-B to 49.” Pet. 25.

Toyama’s first exemplary structure includes, among other elements: “**semiconductor substrate 9**” (Ex. 1005, [0163]); “**planar semiconductor material layer 10**” (Ex. 1005, [0170]); “**alternating stack (132, 146, 232, 246)**” (Ex. 1005, [0232]); “**channels**” (Ex. 1005, [0211]); “**laterally-elongated contact via structures 76**” (Ex. 1005, [0236]); “**drain contact via structures 88**” (Ex. 1005, [0241]); “**source connection via structures 91**” (Ex. 1005, [0250]); “**dielectric fill material portion 430**” (Ex. 1005, [0216]); and “**through-memory-level via structures 488**” (Ex. 1005, [0244]). A cross-section view of Toyama’s first exemplary structure is below.

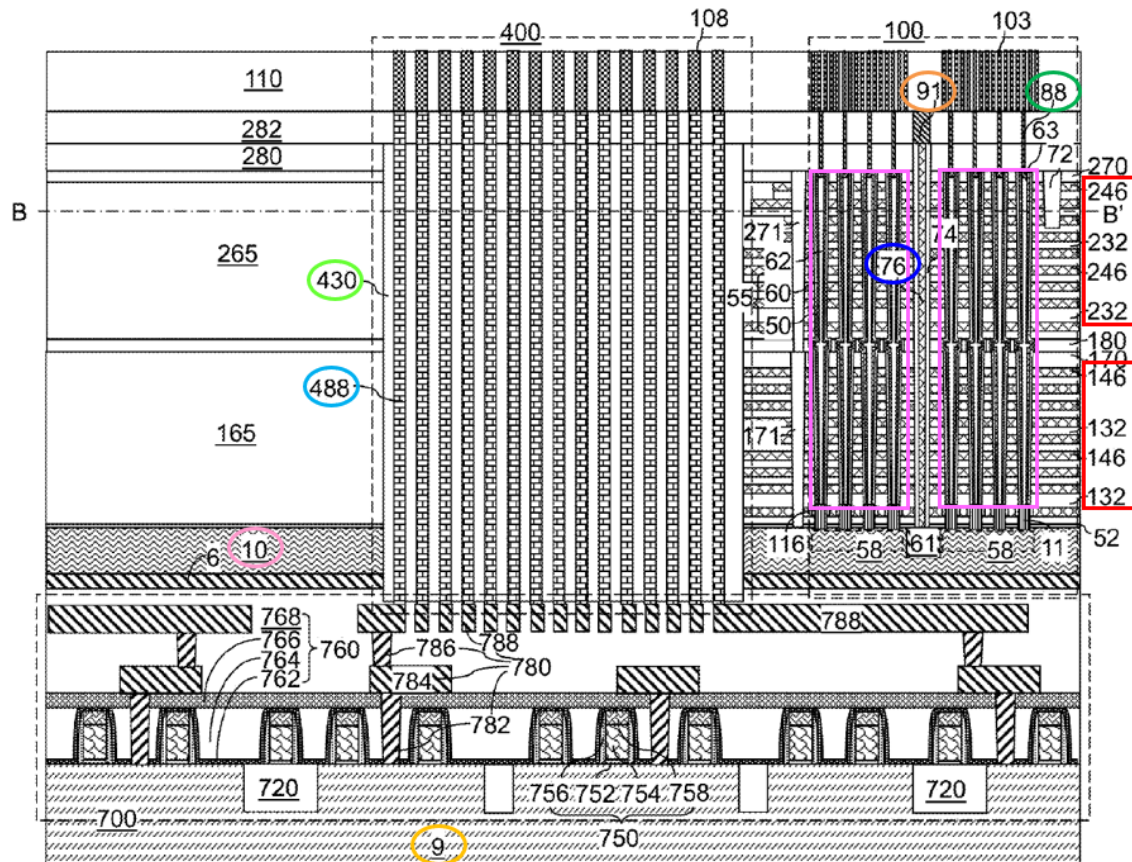


FIG. 17A

Ex. 1005, Fig. 17A (annotated).

In Toyama's first exemplary structure, **dielectric fill material portion 430** forms a hole in **planar semiconductor material layer 10**, which allows **through-memory-level via structures 488** to form vertical interconnects. Toyama's **planar semiconductor material layer 10** lacks the claimed isolation structure. While Toyama's **semiconductor substrate 9** seems to comprise "shallow trench isolation structures 720," they do not host **through-memory-level via structures 488** or similar via structures.

Toyama's second modification of the fourth exemplary structure includes, among other elements: “**semiconductor substrate 9**” (Ex. 1005, [0163]); “**planar semiconductor material layer 10**” (Ex. 1005, [0170]); “**alternating stack (132, 146, 232, 246)**” (Ex. 1005, [0232]); “**channels**” (Ex. 1005, [0211]); “**laterally-elongated contact via structures 76**” (Ex. 1005, [0236]); “**drain contact via structures 88**” (Ex. 1005, [0241]); “**insulating liners 674**” (Ex. 1005, [0340]); and “**through-memory-level via structure 676**” (Ex. 1005, [0341]). A cross-section view of Toyama's second modification of the fourth exemplary structure is below.

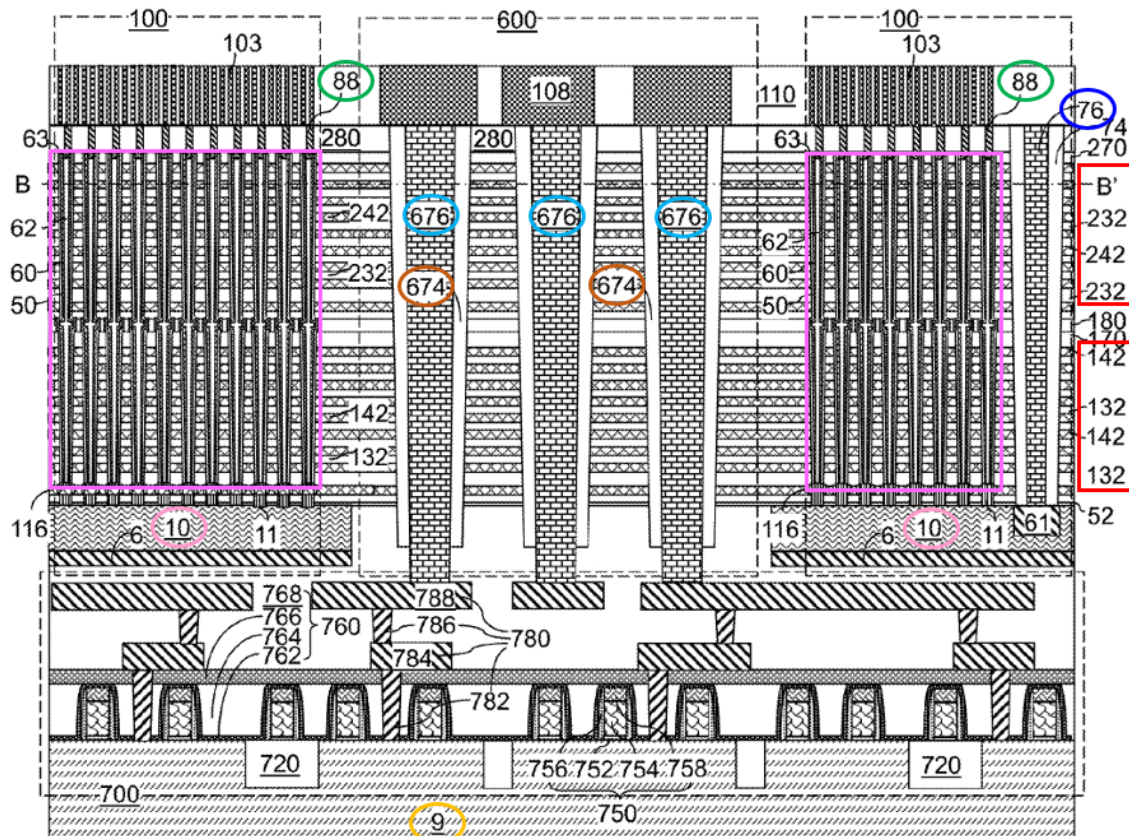


FIG. 49

Ex. 1005, Fig. 49 (annotated).²

In Toyama's second modification of the fourth exemplary structure, Toyama's **planar semiconductor material layer 10** again lacks an isolation structure. In addition, **through-memory-level via structures 676** are not formed through a dielectric structure; instead, they are formed through **alternating stack (132, 146, 232, 246)** and as a result, they require separate **insulating liners 674** around each individual **through-memory-level via structure 676**.

B. U.S. Patent No. 10,354,980 ("Mushiga") (Ex. 1006)

Petitioner does not contend that Mushiga anticipates the Challenged Claims, and instead argues only that it renders obvious the Challenged Claims in view of the knowledge of a POSITA, alone or in combination with Makala. Pet. 7, 77-105.

Mushiga also teaches a 3D NAND memory device similar to Toyama's. Ex. 1006, 5:31-43. Mushiga's memory device includes, among other elements: "**first**

² Petitioner states: "In a clear typographical error, Figure 49 labels its alternating conductor/dielectric layer stack as elements 132, 142, 232, 242. Elements 142, 242 are 'sacrificial material layers' which, in a process step prior to Figure 49, were removed and replaced with 'electrically conductive layers (146, 246).' Toyama, [0337], [0340]." Pet. 39. Patent Owner does not challenge this assertion for purposes of the POPR.

substrate semiconductor layer 9” (Ex. 1006, 7:34-44); “semiconductor material layer 10” (Ex. 1006, 9:8-14); “alternating stack (132, 146, 232, 246)” (Ex. 1006, 10:31-38); “channels” (Ex. 1006, 9:50-67); “backside contact via structures 76” (Ex. 1006, 10:1-18); “drain contact via structures 88” (Ex. 1006, 10:19-30); “insulating spacers 586” (Ex. 1006, 10:31-46); and “through-memory-level via structure 588” (Ex. 1006, 10:42-57). A cross-section view of Mushiga’s device is below.

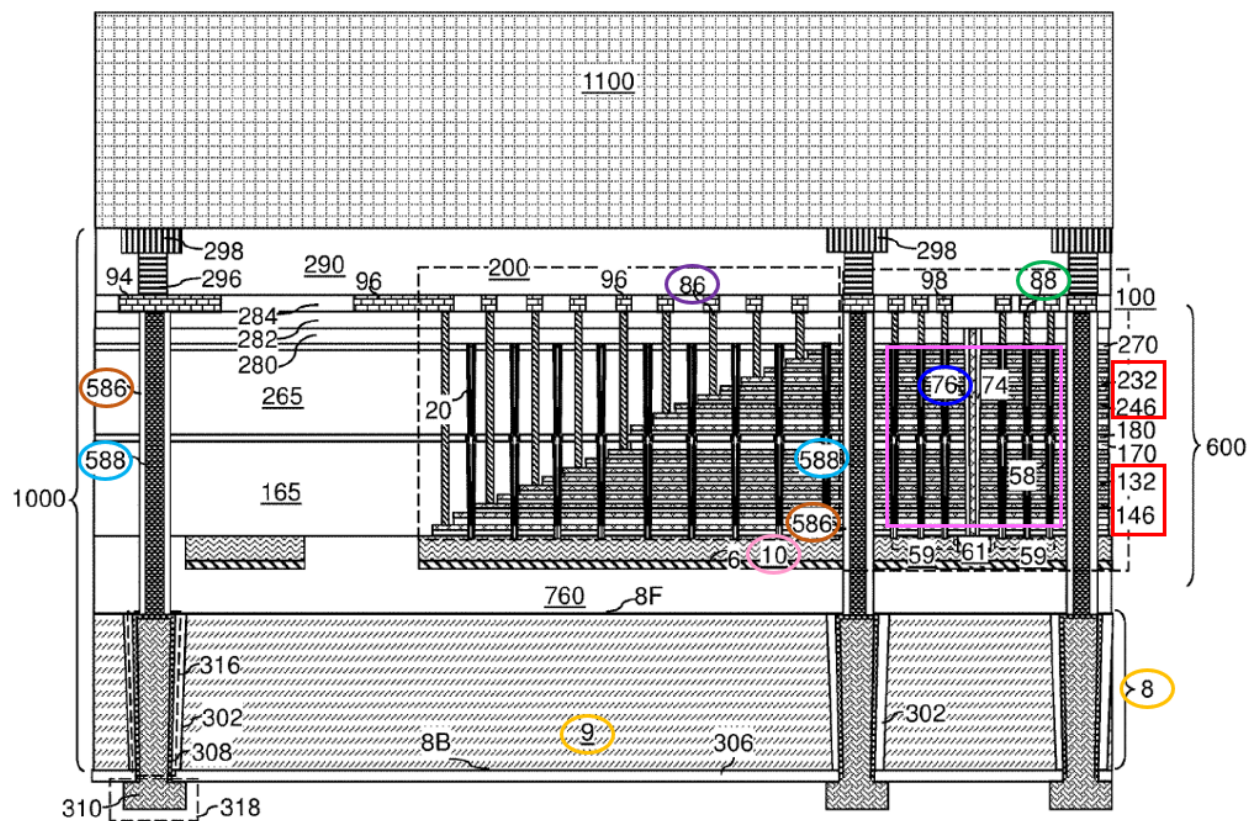


FIG. 11

Ex. 1006, Fig. 11 (annotated).

Mushiga's **semiconductor material layer 10** and **substrate semiconductor layer 9** lack the claimed isolation structure. In addition, in Mushiga, some **through-memory-level via structures 588** are placed outside the array, such as the one on the left in Fig. 11 above. For the ones placed inside the array, there is no dielectric structure in a dedicated region for forming **through-memory-level via structures 588**; instead, they are formed through **alternating stack (132, 146, 232, 246)** and as a result, they require separate **insulating spacers 586** around each individual **through-memory-level via structure 588**.

C. U.S. Patent No. 10,262,945 (“Makala”) (Ex. 1007)

Petitioner does not contend that Makala anticipates the Challenged Claims, and instead argues only that it renders obvious the Challenged Claims in view of the knowledge of a POSITA in combination with Mushiga. Pet. 7, 102-105.

Makala teaches a 3D NAND memory device similar to Mushiga's and Toyama's. Ex. 1007, 3:29-41. Makala's memory device includes, among other elements: “**substrate semiconductor layer 9**” (Ex. 1007, 4:53-61); “**planar semiconductor material layer 10**” (Ex. 1007, 17:10-40); “**alternating stack (132, 146, 232, 246)**” (Ex. 1007, 32:8-30); “**channels**” (Ex. 1007, 24:25-43); “**backside contact via structures 76**” (Ex. 1007, 33:4-29); “**drain contact via structures 88**” (Ex. 1007, 33:37-43); “**source connection via structures 91**” (Ex. 1007,

Ex. 1007, Fig. 16 (annotated).

Petitioner relies on Makala only for its disclosure of **source connection via structures 91**, although they are also disclosed by Toyama.

VI. THE BOARD SHOULD EXERCISE ITS DISCRETION UNDER § 325(D) TO DENY INSTITUTION

The Board has statutory discretion to deny *inter partes* review when the petition relies on the same or substantially the same prior art or arguments that were previously presented to the Office. *See* 35 U.S.C. §325(d). The two-part

framework established in *Advanced Bionics* considers (A) whether the same or substantially the same art was previously presented to the Office or whether the same or substantially the same arguments were previously presented to the Office, and (B) if either condition is satisfied in the first part, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of the challenged claims. See *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Pap. 6 at *8-9 (precedential) (“If a condition in the first part of the framework is satisfied and the petitioner fails to make a showing of material error, the Director generally will exercise discretion not to institute inter partes review.”). The PTAB has used the six factors set forth in *Becton, Dickinson* to evaluate the two-part *Advanced Bionics* framework. *Advanced Bionics*, IPR2019-01469, Pap. 6 at *7, n.8 citing *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Pap. 8 (Dec. 15, 2017) (precedential as to §III.C.5, first paragraph). *Becton, Dickson* factors (a) “the similarities and material differences between the asserted art and the prior art involved during examination,” (b) “the cumulative nature of the asserted art and the prior art evaluated during examination,” and (d) “the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art” relate to the first part of the *Advanced Bionics* framework (whether the art or arguments presented in the

Petition are the same or substantially the same as those previously presented to the Office). *Becton, Dickson* factors (c) “the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection,” (e) “whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art,” and (f) “the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments” relate to the second part of the framework (whether the petitioner has demonstrated a material error by the Office in its prior consideration of the prior art or arguments).

Applying the *Advanced Bionics* framework to this proceeding, the Board should exercise its discretion and deny institution because, as discussed below, (A) with respect to Ground 1 (Toyama), Petitioner relies on the same art that was previously presented to the Office, (B) with respect to Grounds 2 (Mushiga) and 3 (Mushiga in view of Makala), Petitioner relies on art that is substantially the same as Toyama, and (C) Petitioner fails to demonstrate that the Office erred in a manner material to the patentability of the Challenged Claims.

A. Ground 1 Relies on the Same Prior Art That Was Previously Presented to the Office

In Ground 1, Petitioner relies solely on Toyama. As discussed in § III, Toyama was presented to the Examiner in an information disclosure statement (IDS) containing only a single reference. Ex. 1002, 555 (12/03/2019 Information

Disclosure Statement). The Examiner considered Toyama and explicitly signed the IDS to indicate that Toyama was a “reference[] considered.” Ex. 1002, 593 (01/13/2020 List of References Cited by Applicant and Considered by Examiner). Therefore, the reference was previously presented to the Office for purposes of § 325(d). *See, e.g., Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 7-8 (precedential) (“Previously presented art includes ... art provided to the Office by an applicant, such as on an Information Disclosure Statement (IDS), in the prosecution history of the challenged patent.”). Petitioner argues that the record is silent as to what, if any, substantive consideration the Examiner gave Toyama (Pet. 10), but as explained above, the Examiner expressly confirmed that Toyama was considered, and this is not a situation where the reference was presented along with hundreds of other references. Again, Toyama was the **only** reference cited in the IDS, which was reviewed and signed by the Examiner.

B. Grounds 2 and 3 Rely on Prior Art Substantially the Same as What Was Previously Presented to the Office

In Ground 2, Petitioner relies solely on Mushiga. Mushiga discloses a 3D memory device just like Toyama, and does not include any feature relevant to the '378 invention, which is also not found in Toyama. Mushiga was filed by the same applicant as Toyama (SanDisk Technologies, LLC) within two years of Toyama's filing.

The '378 claims require, *inter alia*, “a **substrate** with an **isolation structure**” (Limitation [15.a]), “a **dielectric structure** on the **isolation structure**” (Limitation [15.c.i]), and “through array contacts (**TACs**) extending vertically through” both structures (Limitation [15.h]).

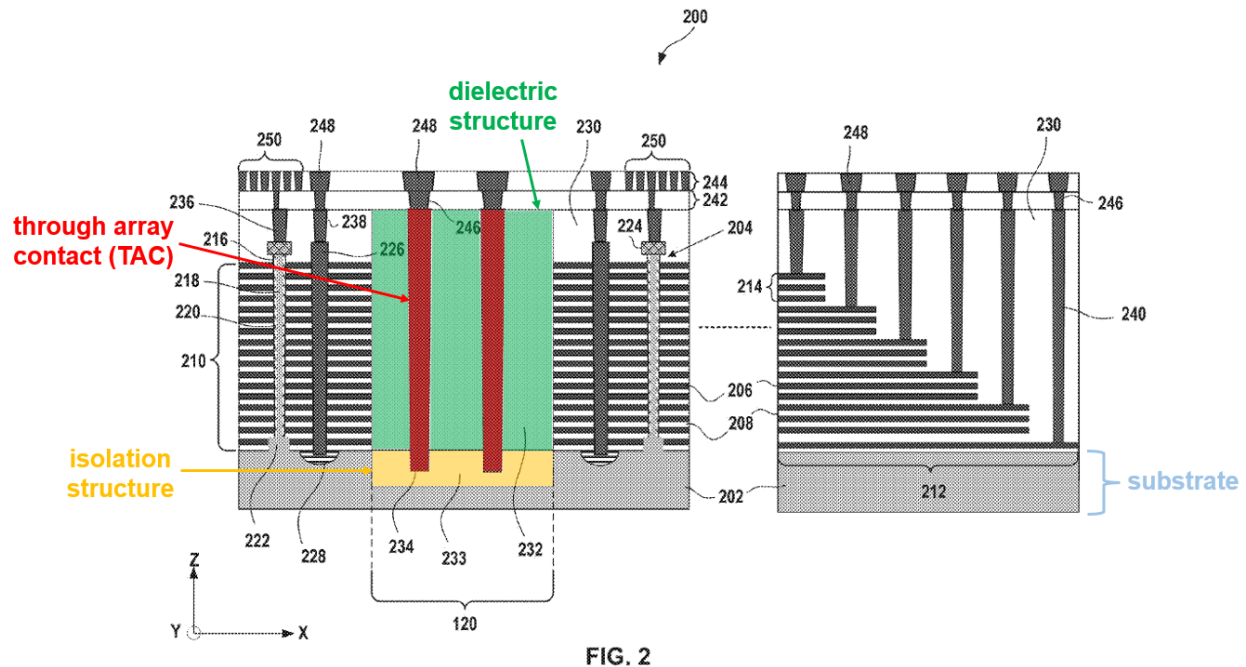


FIG. 2

'378, Fig. 2 (annotated).

Mushiga fails to satisfy these requirements in the same way as Toyama. As seen in the exemplary figures from Toyama and Mushiga below, and as explained further in § VII.B, Mushiga does nothing to cure the deficiencies of Toyama with respect to a **substrate** with an **isolation structure**, a **dielectric structure** on the **isolation structure**, and **TACs** that extend vertically through both structures.

For example, Toyama's Figure 49 and Mushiga's Figure 11 both lack a substrate with an isolation structure, a dielectric structure on the isolation

structure, and TACs that extend vertically through both structures. For Toyama's Figure 49, the alleged substrate does not have an isolation structure and, unable to point to a dielectric structure through which multiple TACs extend vertically, Petitioner relies on the alleged TACs' liners (element 674). Even if these liners could be a dielectric structure, they are not on an isolation structure and there is no one liner through which all of the TACs extend vertically.

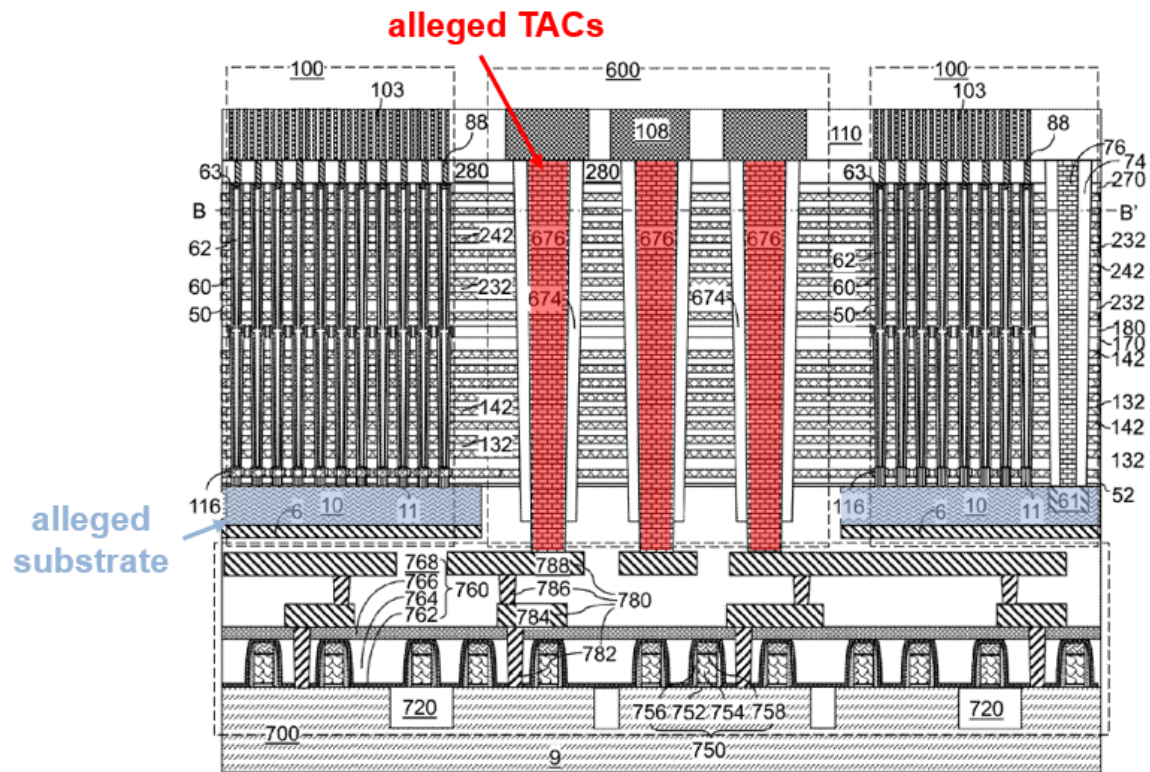


FIG. 49

Ex. 1005, Fig. 49 (annotated); *see also* Pet. 30-31, 39-42, 66-68.

Similarly for Mushiga's Figure 11, the alleged substrate does not have an isolation structure and, unable to point to a dielectric structure through which multiple TACs extends vertically, Petitioner relies on the alleged TACs' liners

(element 586). Even if these liners could be a **dielectric structure**, they are not on an **isolation structure** and there is no one liner through which all of the **TACs** extend vertically.

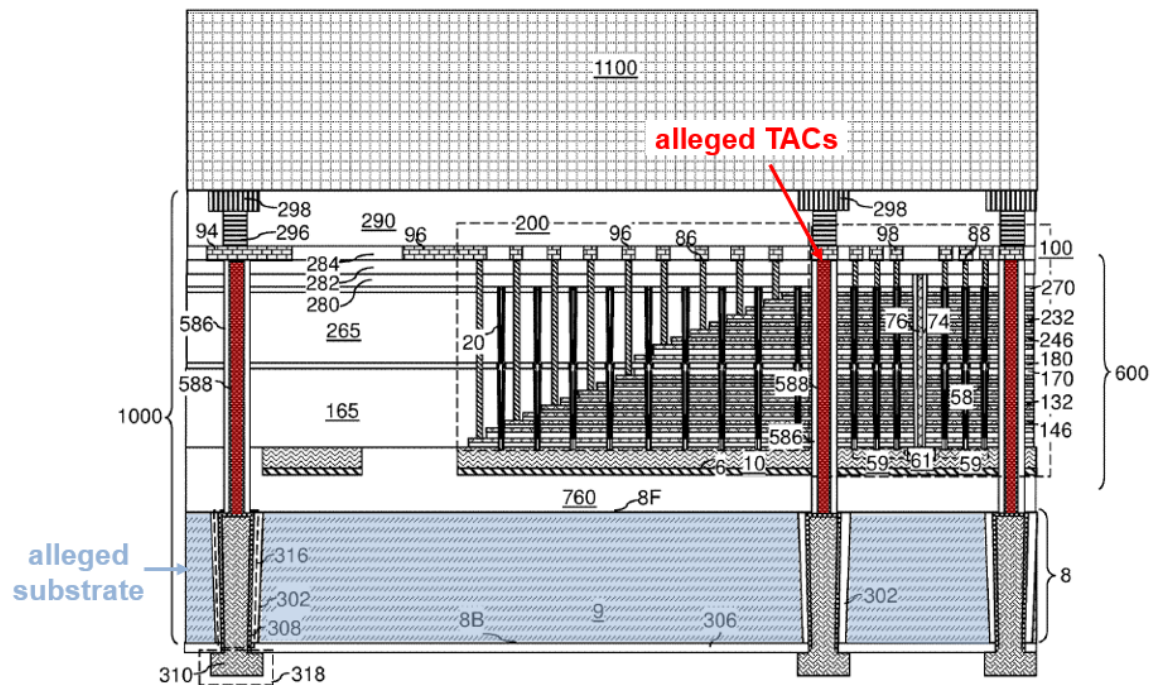


FIG. 11

Ex. 1006, Fig. 11 (annotated); *see also* Pet. 78-86, 98.

In addition, the components in Mushiga have counterparts in Toyama. The table is color coded to match Mushiga's annotated Fig. 11 below, which depicts all the features Petitioner relies on.

'378 claim limitation mapped to by Petitioner in Ground 2	Mushiga feature mapped in Ground 2	Corresponding Toyama feature
substrate	“first semiconductor substrate 8” or	“semiconductor substrate 9”

'378 claim limitation mapped to by Petitioner in Ground 2	Mushiga feature mapped in Ground 2	Corresponding Toyama feature
	“semiconductor substrate 9”	
isolation structure	“insulating material liners 302”	n/a
	“backside insulating layer 306”	n/a
alternating conductor/dielectric layer stack	“alternating stack of insulating layers (132, 232) and electrically conductive layers (146, 246)”	“alternating stack of insulating layers (132, 232) and electrically conductive layers (146, 246)”
dielectric structure	“insulating material layer 760”	“lower level dielectric layer 760”
	“first retro-stepped dielectric material portion 165”	“first-tier retro-stepped dielectric material portion 165”
	“inter-tier dielectric layer 180”	“inter-tier dielectric layer 180”
	“second retro-stepped dielectric material portion 265”	“second-tier retro-stepped dielectric material portion 265”
	“insulating spacer 586”	“insulating liner 674”
channel structure	“memory stack structure 58”	“memory stack structure 55”
slit structure	“backside contact via structures 76”	“laterally-elongated contact via structure 76”
staircase structure	“stepped surfaces”	“stepped surfaces”
word line contact	“word line contact via structure 86”	“word line contact via structure 86”
local contact	“drain contact via structure 88”	“drain contact via structure 88”

'378 claim limitation mapped to by Petitioner in Ground 2	Mushiga feature mapped in Ground 2	Corresponding Toyama feature
through array contact (TAC)	“through-memory-level via structure 588”	“through-memory-level via structure 588” or “through-memory-level via structure 676”
	“first through-substrate via structures 316”	n/a

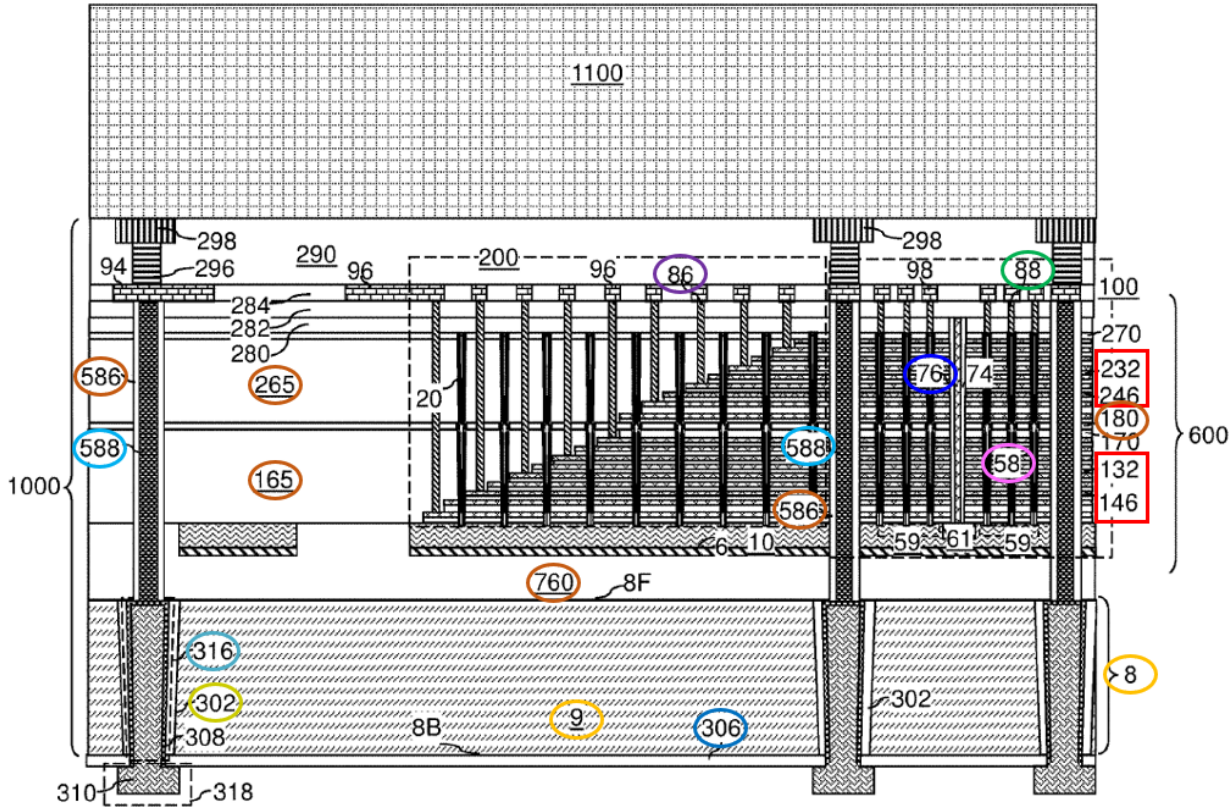


FIG. 11

Ex. 1006, Fig. 11 (annotated). Toyama’s corresponding elements are depicted in the representative annotated figures below.

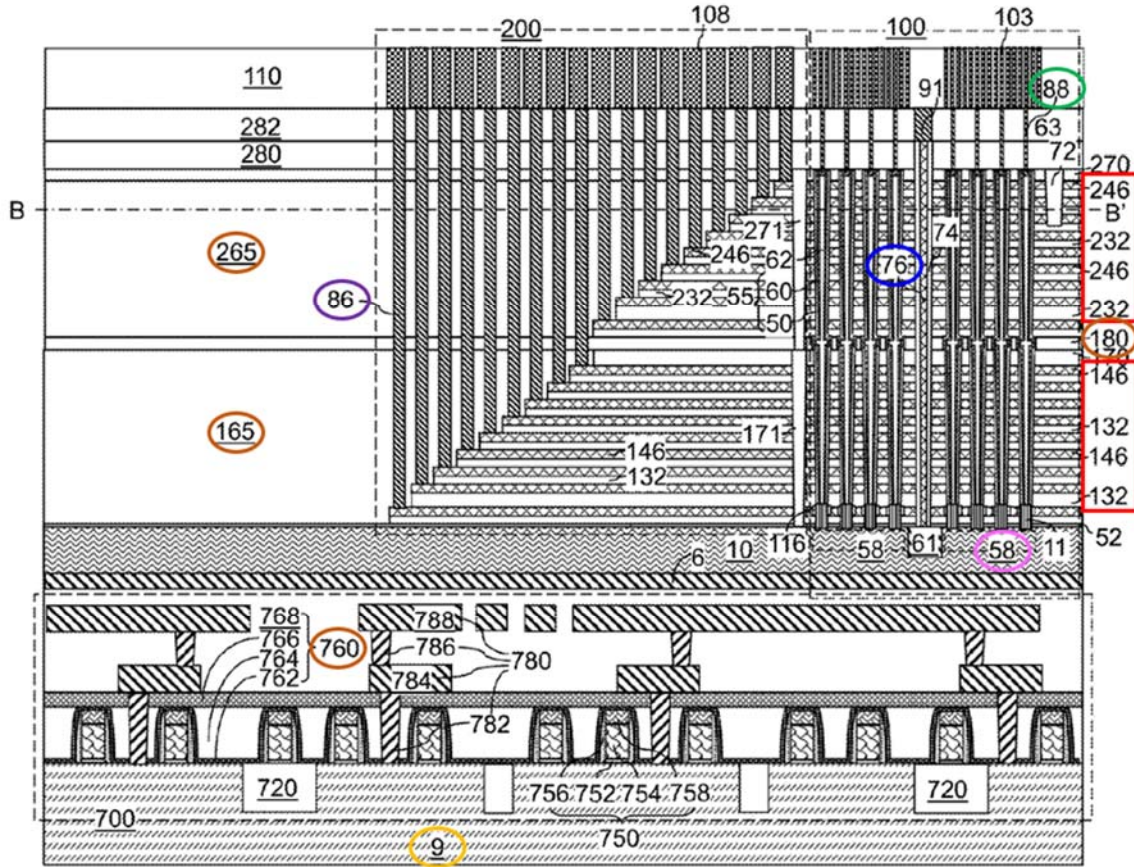


FIG. 17C

Ex. 1005, Fig. 17C (annotated).

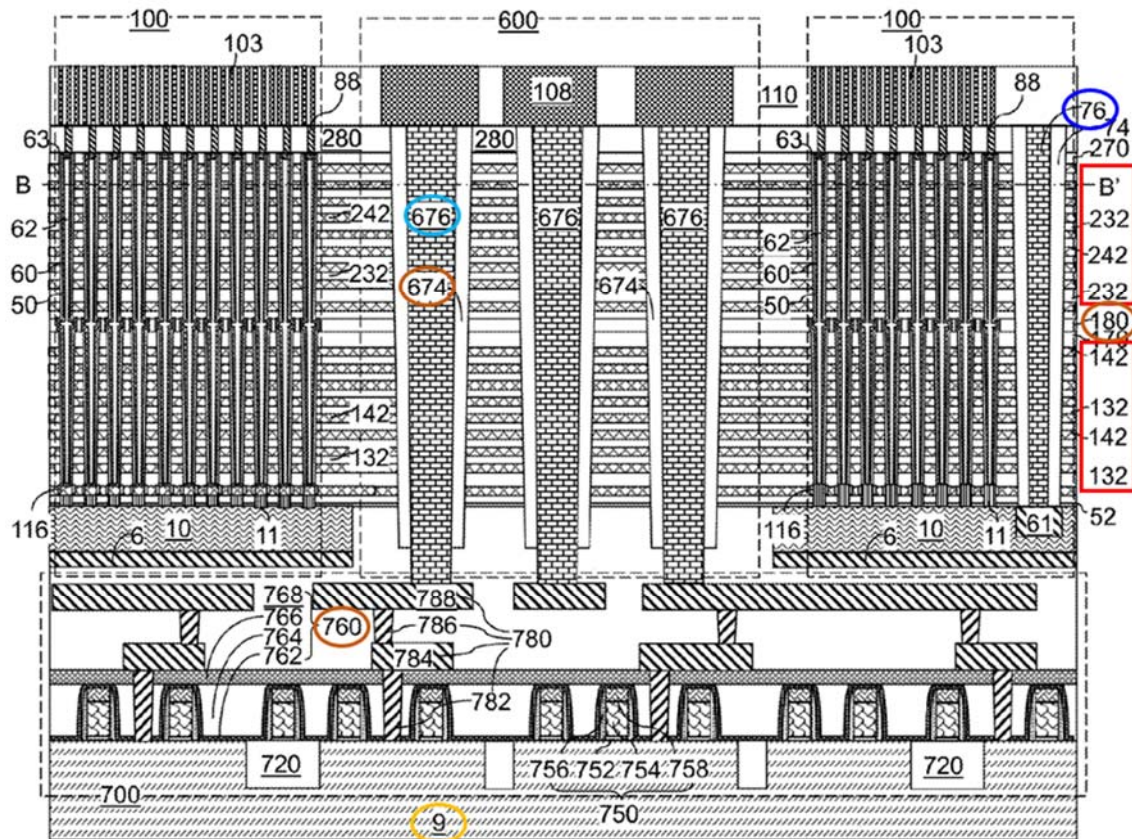


FIG. 49

Ex. 1005, Fig. 49 (annotated).³

As seen from the table and figures, the overlap of features between Mushiga and Toyama is substantially the same in all material respects. The only features Petitioner relies on in Mushiga that Toyama lacks are “insulating material liners 302,” “backside insulating layer 306,” and “first through-substrate via structures 316.” These features are present in Mushiga because Mushiga adds “first through-

³ In Toyama’s Fig. 49, elements 142, 242 should have been labeled 146, 246 for “electrically conductive layers.” See also footnote 2.

substrate via structures 316” to its “through-memory-level via structures 588” and has them extend through both “semiconductor material layer 10” and “semiconductor substrate 9,” as opposed to only “semiconductor material layer 10” in Toyama. However, this difference is not relevant to the Challenged Claims, and does nothing to cure the deficiencies of Toyama (as explained above and in further detail in § VII.B). As a result, these additions do not differentiate Mushiga from Toyama.

It is routine for corporations such as SanDisk to file patent applications as they make improvements over existing technologies, and the few additional features in Mushiga do not differentiate from Toyama, because they do not relate to the invention claimed in '378, despite Petitioner's erroneous mappings. Petitioner also does not argue that Mushiga is not cumulative over Toyama. Pet. 23-24. Therefore, the Board should find that Mushiga is substantially the same as Toyama.

In Ground 3, Petitioner relies on Mushiga in view of Makala. Makala discloses a 3D memory device just like Toyama, and does not include any element relevant to the '378 invention that is not also found in Toyama. Makala was filed by the same applicant as Toyama (SanDisk Technologies, LLC) within one year of Toyama's filing, and shares an inventor with Toyama (James Kai).

Petitioner relies on Makala only for its disclosure of “source connection via

structures 91,” which it maps to the claimed “local contacts disposed on [...] the slit structures.” Pet. 102-105. However, Toyama also teaches the same feature (“source connection via structures 91”) that Petitioner relies on in Ground 1. Pet. 63-64. Thus, Makala is not used by Petitioner to put forth an original argument, but only as a back-up reference, which teaches identical features to those in Toyama. Petitioner also does not argue that Makala is not cumulative over Toyama. Pet. 23-24. Therefore, the Board should find that Makala is substantially the same as Toyama.

C. The Office Did Not Err in a Manner Material to Patentability of the Challenged Claims

Petitioner has not shown that the Examiner erred in its consideration of Toyama during prosecution, and its arguments are contradicted by the record.

As an initial matter, Petitioner’s substantive arguments for Examiner error are focused **only** on elements from pending claim 17 that were incorporated into the pending independent claim 16 by Applicant in the December 23, 2019 Reply to Office Action. Pet. 13-14; Ex. 1002, 567. But those particular limitations were incorporated into the pending independent claim 16 following rejections based on different references than Toyama. Thus, Petitioner has no basis for limiting its § 325(d) analysis of Toyama to those particular limitations. Indeed, as explained below and in § VII.A, there are other limitations that are missing from Toyama,

which Petitioner fails to discuss in its § 325(d) analysis. Thus, Petitioner has not met its burden of showing Examiner error.

Indeed, the Examiner did not err as Toyama discloses the fabrication technique that the '378 criticizes and improves upon. For example, a key feature of the '378 that is missing from Toyama is that the TACs are formed in a dielectric structure that is formed on an isolation structure of a substrate. This configuration results in a less complex and less costly fabrication technique. '378, 5:35-39, 10:59-66, 18:27-41, 20:9-16.

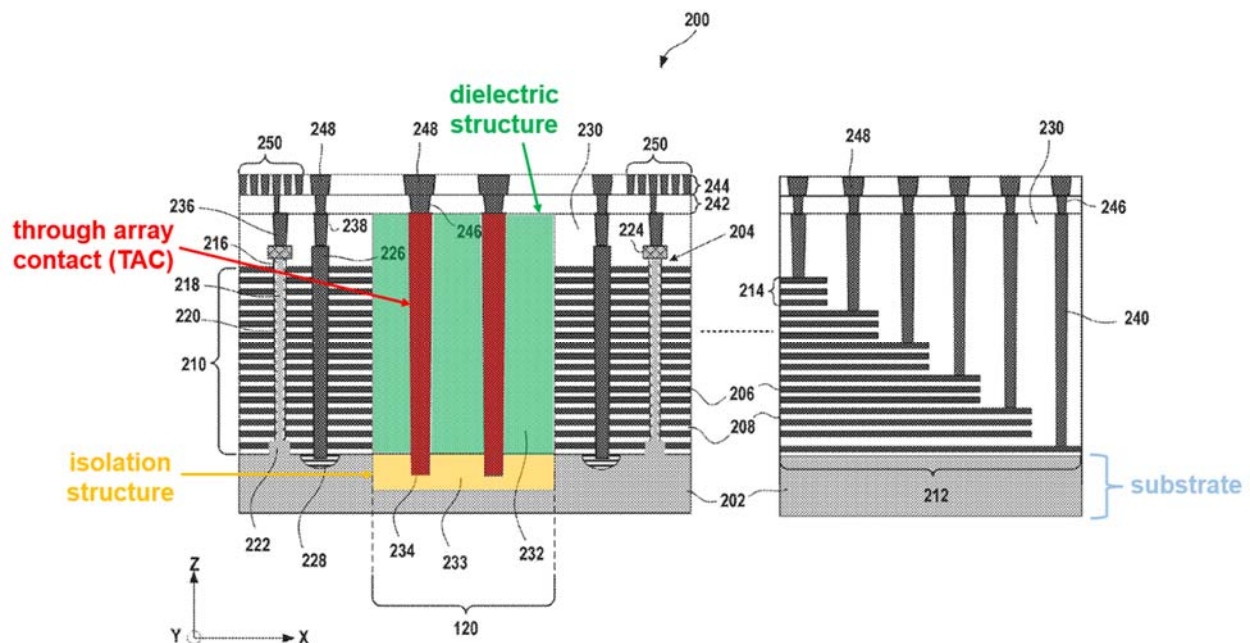


FIG. 2

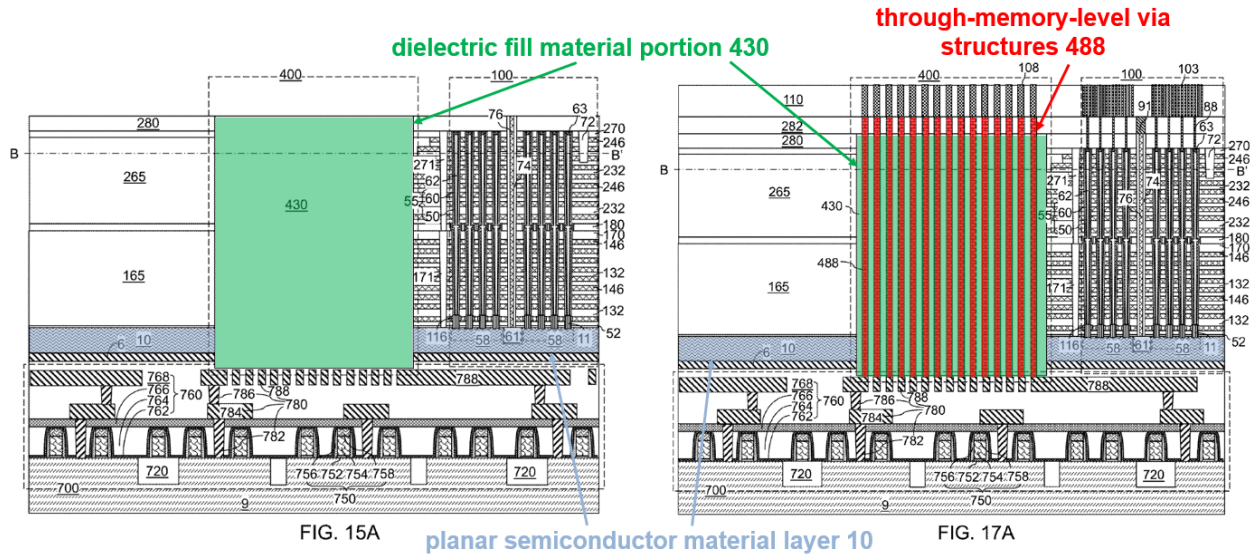
'378, Fig. 2 (annotated).

The prior art at the time of filing of the '378 formed vertical vias (such as TACs) within the alternating dielectric and conductive layers, which “increase[d] the fabrication cost.” '378, 10:59-66, 18:27-33. The '378 simplifies the

fabrication process of TACs by forming them in a dedicated dielectric structure that is on an isolation structure of the substrate. By having an isolation structure in the substrate onto which the dielectric structure is placed, the dielectric structure can be formed with ease using various patterning techniques, and the TACs can be formed via a significantly simplified process. '378, 10:30-33, 18:27-33, 21:17-25.

Toyama discloses a few embodiments, but none of them teaches the structure claimed in the '378. Regarding the placement of “through-memory-level via structures,” Petitioner relies on Toyama’s following teachings:

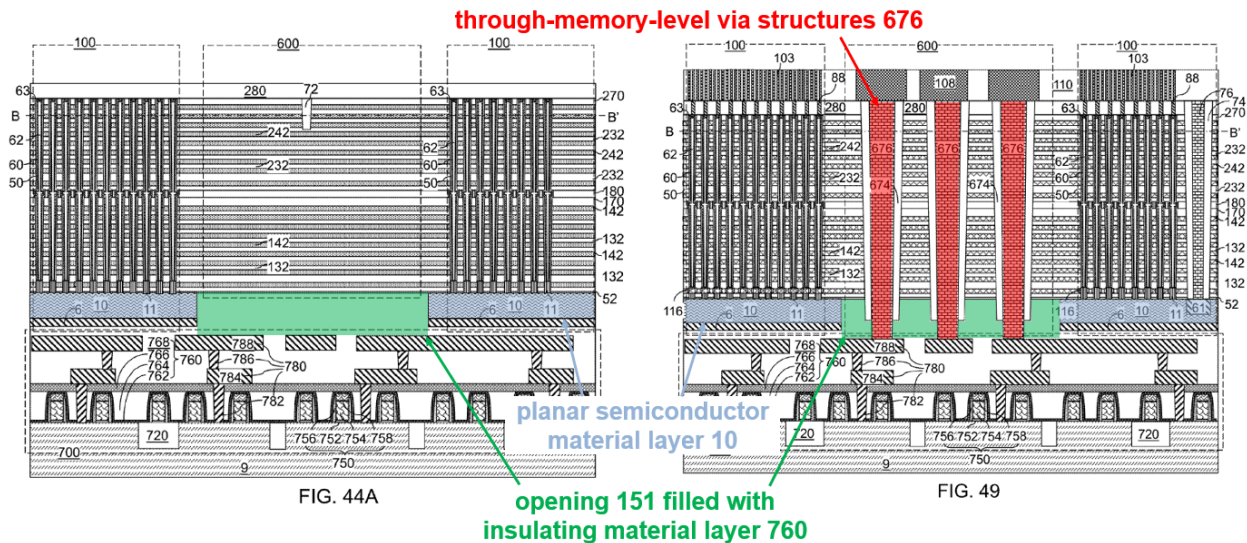
- 1) Placing “through-memory-level via structures 488” in “dielectric fill material portion 430” as in the “first exemplary structure” (Ex. 1005, Fig. 17A) is relied upon by Petitioner in Ground 1. As further explained in § VII.A.1, this structure lacks a substrate with an isolation structure and a dielectric structure on the isolation structure as claimed. Rather, the dielectric fill material extends above and below Petitioner’s alleged substrate (element 10) and is not both the claimed “isolation structure” that is part of the substrate and the claimed “dielectric structure” on top of the isolation structure—contrary to Petitioner’s allegations.



Ex. 1005, Figs. 15A, 17A (annotated).

- 2) Placing “through-memory-level via structures 676” through an alternating stack of dielectric and conductive materials as in the second modification of the fourth exemplary structure (Ex. 1005, Fig. 49) is also relied upon in Ground 1. As explained further in § VII.A.2, this embodiment also lacks a substrate with an isolation structure and a dielectric structure on the isolation structure through which multiple TACs extend as claimed. Rather, the insulating material layer extends below and is not part of Petitioner’s alleged substrate (element 10). Moreover, there is no single dielectric structure through which multiple TACs extend—even the liners of the via structures on which Petitioner relies do not constitute a dielectric structure through which multiple TACs must extend. Rather, forming

the TACs through an alternating stack of dielectric and conductive materials is exactly what the '378 aimed to avoid due to its complexity. '378, 5:35-39, 10:59-66, 18:27-41, 20:9-16.



As summarized above and discussed further in §§VII.B-C, these same deficiencies apply to Mushiga and Makala (Grounds 2-3).

Finally, Petitioner argues that a rejection by the Chinese Patent Office in a proceeding involving a foreign counterpart is evidence of the U.S. Examiner “overlooking” Toyama’s teachings (Pet. 2, 11-12), but Petitioner’s analysis is faulty and conclusory. First, Petitioner ignores that the Chinese Patent Office found that each of the independent claims (and by extension, all claims) in the Chinese application in fact had “distinguishing features” from Toyama, but only found them unpatentable by applying a legal standard different from the U.S. patent law (i.e., they did not “possess creativity” as prescribed in Chinese law).

Exs. 1012, 1014. In fact, the distinguishing features recognized by the Chinese Patent Office relate to having TACs that extend through a dielectric structure that is on an isolation structure of a substrate. *Id.* Second, Petitioner’s analysis is conclusory and, tellingly, makes no attempt to discuss the substance or applicability of the Chinese Patent Office’s analysis to the U.S. examination. Instead, Petitioner simply speculates that the Examiner must have overlooked Toyama’s teachings. All the evidence in the record points to the opposite: that Toyama’s teachings lack key inventive features of the ’378 application, and the Examiner recognized this fact.

Therefore, the Office did not err in a manner material to patentability of the Challenged Claims. The Board should exercise its discretion under §325(d) and deny institution.

**VII. PETITIONER FAILS TO ESTABLISH A REASONABLE
LIKELIHOOD THAT IT WOULD PREVAIL WITH RESPECT TO
THE CHALLENGED CLAIMS**

Petitioner fails to establish a reasonable likelihood that it would prevail with respect to the Challenged Claims because Petitioner has failed to show that prior art discloses or renders obvious the limitations of the Challenged Claims relating to “a substrate with an isolation structure,” “a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall

surface of the dielectric structure and the dielectric structure is formed of a dielectric material,” and “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.” As explained below, Petitioner cites two primary references—Toyama and Mushiga—and asserts that they each individually show these features. Each of Petitioner’s arguments fails.

Ground 1 relies on Toyama alone, but Toyama does not disclose or render obvious the aforementioned “isolation structure” limitations. Petitioner improperly attempts to either divide a single structure into two distinct structures, or patch together physically separated elements, in an attempt to recreate the ’378’s contiguous dielectric structure. And Petitioner’s obviousness arguments are conclusory and purely based on hindsight.

Ground 2 relies on Mushiga alone, but Mushiga similarly does not disclose or render obvious the aforementioned “isolation structure” limitations. In fact, Mushiga is substantially the same as Toyama, aside from a few additional features that are not relevant to the invention of the ’378. Petitioner’s reliance on Mushiga ignores clear descriptions and depictions from the ’378 and maps irrelevant elements. And Petitioner once again raises obviousness arguments that are conclusory and purely based on hindsight.

Ground 3 is based on the combination of Mushiga and Makala, but relies on the same Mushiga disclosures as Ground 2 for the claim 15 limitations at issue (see Pet. 102-105), and thus fails at least for the same reasons Ground 2 fails.

Therefore, Petitioner's assertions as to claim 15, the only independent claim among the Challenged Claims, and thus all challenges claims fail with respect to all the grounds proposed by Petitioner.

A. Ground 1: Petitioner Fails to Show That Any of Toyama's Embodiments Discloses or Renders Obvious Limitations [15.a], [15.c.i], and [15.h]

Petitioner fails to show that any of Toyama's embodiments discloses or renders obvious three separate limitations of the Challenged Claims. In Ground 1, Petitioner relies on two of Toyama's embodiments: (1) "the 'first exemplary structure,' illustrated in Figures 1A-B to 17A-F," and (2) "the 'second modification of the fourth exemplary structure,' illustrated in Figures 44A-B to 49 (hereinafter, 'Second Modification')," and asserts that these embodiments independently render obvious the Challenged Claims. Pet. 25. Hereinafter, for convenience, Petitioner's Ground 1 arguments regarding Toyama's First Exemplary Structure are referred to as Ground 1A and Petitioner's Ground 1 arguments regarding Toyama's Second Modification (of the fourth exemplary structure) are referred to as Ground 1B.

1. Ground 1A: Petitioner Fails to Show That Toyama’s First Exemplary Structure Discloses or Renders Obvious Limitations [15.a], [15.c.i], and [15.h]

In Ground 1A, Petitioner relies on Toyama’s First Exemplary Structure as allegedly rendering obvious all Challenged Claims (Pet. 28-77), but Petitioner fails to show that Toyama’s First Exemplary Structure discloses or renders obvious three separate claim limitations: [15.a] (“***a substrate with an isolation structure***”), [15.c.i] (“***a dielectric structure on the isolation structure***”), and [15.h] (“***through array contacts (TACs) extending vertically through the dielectric and the isolation structures***”).

(a) Petitioner Fails to Show That Toyama’s First Exemplary Structure Discloses or Renders Obvious “a Substrate With an Isolation Structure” (Limitation [15.a])

Toyama’s First Exemplary Structure does not disclose or render obvious “***a substrate with an isolation structure***” as required by limitation [15.a] because the feature of Toyama that Petitioner maps to the “isolation structure” is, at most, located in the region of a cut through the alleged substrate, and is not part of the substrate as required by the Challenged Claims.

The ’378 claim 15 requires “a substrate ***with*** an isolation structure,” meaning that the isolation structure is part of the substrate. For example, the ’378 describes and depicts the isolation structure, which is the structure in the isolation region, as being part of the substrate. Ex. 1001, 12:54-66 (“According to some embodiments,

substrate 202 includes isolation regions or structures, like STI structure 233 shown in FIG. 4.”), 20:38-42 (“In some embodiments, a 3D memory device includes a semiconductor substrate, an alternating layer stack disposed on the semiconductor substrate, and a dielectric structure, extending vertically through the alternating layer stack, on **an isolation region of the substrate**”) (emphasis added), Figs. 2, 4-13.

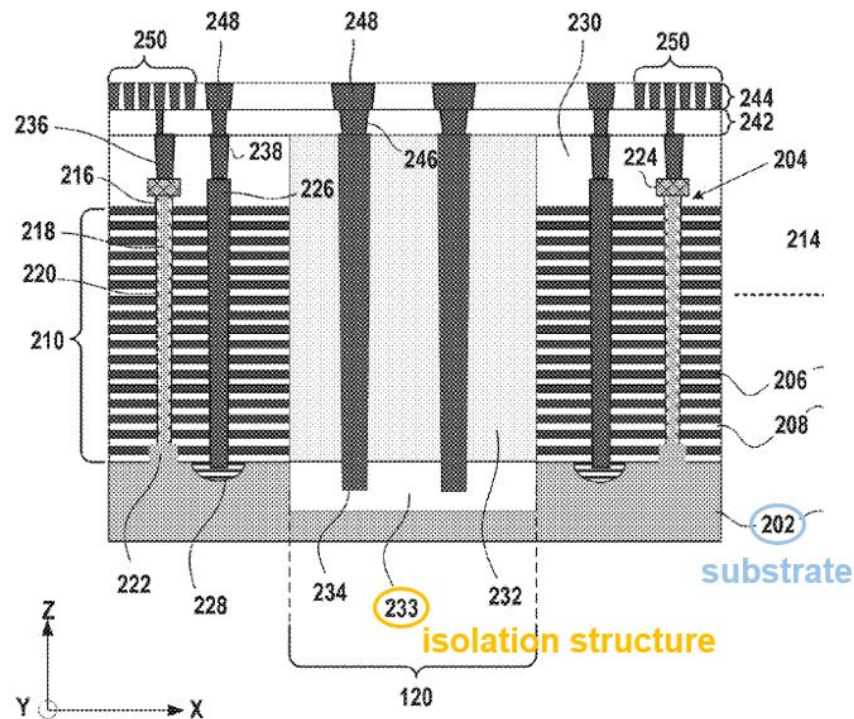
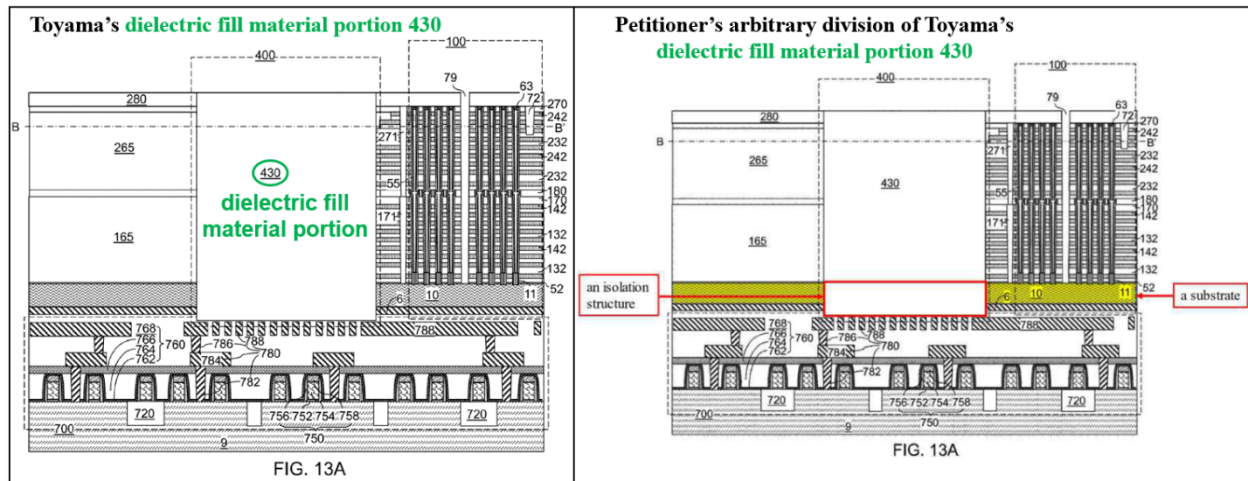


FIG. 2

Ex. 1001, Fig. 2 (annotated and excerpted). For example, the '378 depicts a shallow region in the upper portion of the substrate (see Fig. 2, above). An example of the isolation structure in the '378 is “shallow trench isolation (STI).” Ex. 1001, 10:30-43, 12:64-13:3, 14:46-15:32.

Toyama’s First Exemplary Structure includes “dielectric fill material portion 430,” which Petitioner arbitrarily and misleadingly divides into two parts, one of which it then erroneously maps to the isolation structure of the ’378. Pet. 33-35.



Ex. 1005, Fig. 13A (left image annotated by Patent Owner; right image showing Petitioner’s annotation at Pet. 35, with top heading added by Patent Owner). There is no basis for Petitioner’s arbitrary division of Toyama’s “dielectric fill material portion 430”—Toyama provides no such teaching.

Even with Petitioner’s arbitrary division, the alleged isolation structure (lower part of “dielectric fill material portion 430”) is not part of the alleged substrate (“planar semiconductor material layer 10”).⁴

⁴ For the purposes of this POPR, Patent Owner does not dispute Petitioner’s mapping of the claimed “substrate” to Toyama’s “planar semiconductor material layer 10” in Ground 1A.

Petitioner argues that the claimed relationship is satisfied because “Toyama’s isolation structure [...] *is formed by removing and is surrounded by* substrate [...]” and “the isolation structure is within the substrate and isolates portions of the substrate from one another” (Pet. 35-36 (emphasis original) (citing Ex. 1003, ¶ 103 which repeats the same language)), but its arguments are misplaced.

As a preliminary matter, Petitioner’s assertion that Toyama’s First Exemplary Structure’s alleged isolation structure “is surrounded by” its alleged substrate is unfounded. Toyama’s relevant figures (Figs. 1A-B to 17A-F) do not depict that dielectric fill material portion “430” is surrounded by other regions. As can be seen below, 430 is shown to extend all the way to the left.

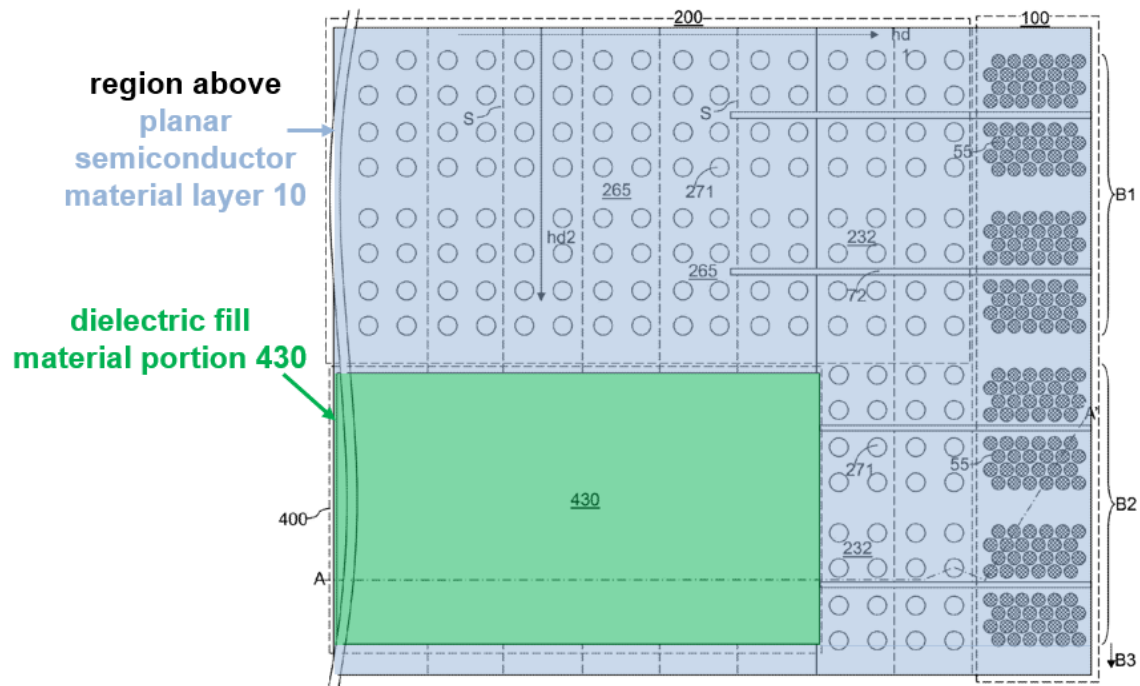
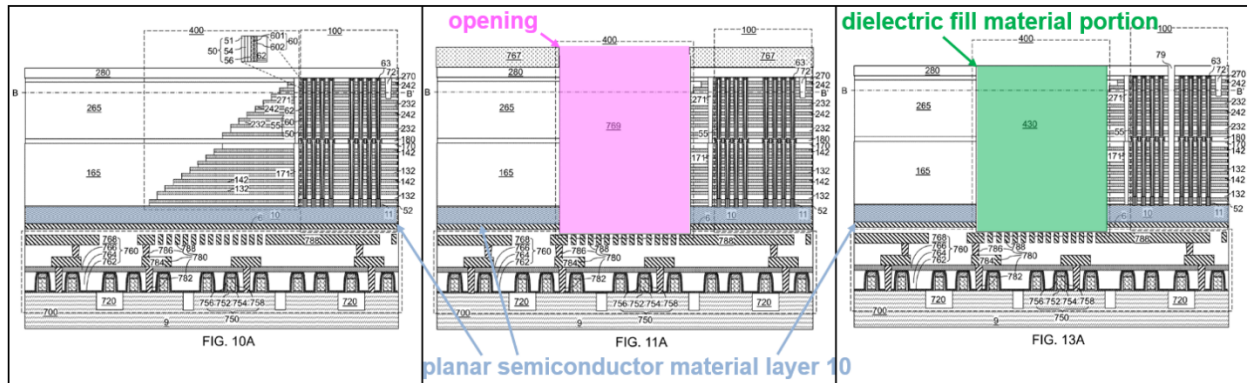


FIG. 12B

Ex. 1005, Fig. 12B (annotated). Even if the alleged isolation structure were surrounded by the alleged substrate, that would not make it a part of the substrate, just as two structures that are merely adjacent would not meet this requirement.

The fact that the opening is formed by removing the alleged substrate ((Pet. 35-36) does not support Petitioner's argument because after the substrate is removed there is no longer any portion of the alleged substrate in the relevant region. To further illustrate this, unlike the substrate of '378, which spans the horizontal area of the memory device and "onto which subsequent material layers are added, or otherwise 'disposed'" (Ex. 1001, 4:41-43), Toyama's "planar semiconductor material layer 10" is completely removed in the relevant region, and is **replaced** by "opening 769." Ex. 1005, [0213]-[0215], Figs. 12A, 13A. After this step, there is simply no substrate in the region labeled "400." Ex. 1005, Fig. 14A. As illustrated below, by forming "opening 769," Toyama creates a region outside and merely abutting the alleged substrate ("planar semiconductor material layer 10"). It is in this newly opened space, where the alleged substrate has been entirely removed, that "dielectric fill material portion 430" is added. Thus, there is no alleged substrate "with" that dielectric fill material.



Ex. 1005, Figs. 10A, 11A, 13A (annotated). Moreover, these steps relate to the manufacturing process, not the final structure, and the Challenged Claims are apparatus claims.

Finally, Petitioner’s assertion that “the isolation structure [...] isolates portions of the substrate from one another” is false. As seen in Toyama’s Fig. 12B above, its alleged substrate is not divided into isolated portions; *i.e.* it remains connected.

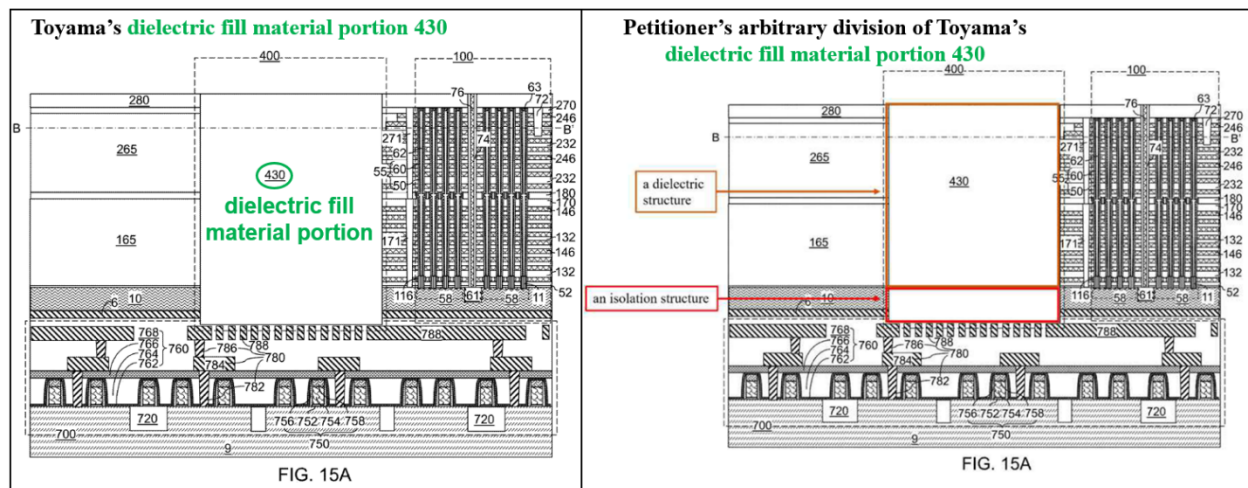
For all of these reasons, Toyama’s First Exemplary Structure does not disclose or render obvious “***a substrate with an isolation structure***” as required by limitation [15.a].

(b) Petitioner Fails to Show That Toyama’s First Exemplary Structure Discloses or Renders Obvious “a Dielectric Structure on the Isolation Structure” (Limitation [15.c.i])

Toyama’s First Exemplary Structure does not disclose or render obvious “***a dielectric structure on the isolation structure***” as required by limitation [15.c.i] because Petitioner arbitrarily and improperly divides Toyama’s single dielectric

structure into two regions and maps different regions to two separate features of the Challenged Claims: the “dielectric structure” and the “isolation structure.”

Toyama’s First Exemplary Structure includes “dielectric fill material portion 430,” which, as illustrated below, Petitioner arbitrarily divides into two parts which it then maps to the separate dielectric structure and isolation structure of the ’378. Pet. 33-35, 45.



Ex. 1005, Fig. 15A (left image annotated by Patent Owner; right image annotated by Petitioner at Pet. 45, with top heading added by Patent Owner).

As an initial matter, for all the reasons explained in § VII.A.1.a, Toyama’s First Exemplary Structure does not disclose or render obvious the isolation structure, and as a result, it does not disclose or render obvious a dielectric structure on the isolation structure.

Further, as explained above, in the ’378, the isolation structure is part of the substrate. The dielectric structure is a separate structure on the isolation structure.

In contrast, in Toyama, the “fill material portion 430” is a single integral structure. There are not two structures in Toyama and thus, necessarily, there is no dielectric structure that is “on” an isolation structure as required by the Challenged Claims. Petitioner asserts that the specification would not preclude the two structures from being formed during the same process step. Pet. 46. However, the issue is not how the device is made, it is whether it has both a dielectric structure **and** an isolation structure. The ’378 consistently claims, describes, and depicts the isolation structure and the dielectric structure to be separate structures with a specific spatial relationship. Ex. 1001, 10:30-43, Fig. 2-13. For example, the dielectric structure is “formed so that it is aligned to or covers at least a portion of” the isolation structure (Ex. 1001, 10:30-33); the dielectric structure is “in contact with” the isolation structure (Ex. 1001, 10:35-36); and the dielectric structure “can cover only portion of” the isolation structure (Ex. 1001, 10:42-43). The fact that the ’378 allows for “other isolation structures” than “STI structure” (Ex. 1001, 10:34-35; Pet. 46) does not mean that a single “dielectric fill material portion” can be arbitrarily divided to purportedly create both the claimed “dielectric structure” and the claimed “isolation structure,” or the claimed spatial relationship that is absent from Toyama.

To support its division, Petitioner argues that the function of the isolation structure is limited to electrically insulating the TACs (Pet. 46-47), but this argument

ignores the claims, which recite two structures with a claimed spatial relationship and do not limit the isolation structure to that single function.

Petitioner next cites *Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1303 (Fed. Cir. 2011) to argue that “different parts of the same structure can meet distinct claim elements” (Pet. 47), but this case is inapposite. Petitioner quotes from the following sentence (replacing “a needle holder” with “an isolation structure” and “a retainer member” with “a dielectric structure”): “Ultimately, the inventor’s statement, on its own, lacks the clarity required to exclude from the scope of the claims a needle holder and a retainer member that form distinct portions of a single structure.” 653 F.3d at 1303; Pet. 47. In *Retractable Techs.*, the Federal Circuit cited clear claim language conveying that “retainer member” can be part of “needle holder,” and a passage from the specification that suggested that they “could be formed as an integral structure in the first instance.” 653 F.3d at 1303. None of that evidence applies here, and Petitioner has cited none. Moreover, retainer member and needle holder of *Retractable Techs.* were “distinct” portions (*id.*), whereas there are no “distinct” portions of the dielectric fill material portion of Toyama absent Petitioner’s arbitrary and hindsight-based annotations.

Finally, Petitioner asserts that Toyama’s First Exemplary Structure renders the claims obvious because a different embodiment teaches forming an isolation structure in “opening 151” before forming a dielectric structure (Pet. 47-48 (citing

Ex. 1003, ¶ 121)), but the structure formed in Toyama’s “opening 151” is not the claimed isolation structure for the same reasons explained in § VI.A.1.a, *supra* (First Exemplary Structure), and § VI.A.2.a, *infra* (Second Modification). And when the other embodiment is used, it lacks additional limitations as discussed in § VI.A.2.a, *infra* (Second Modification).

Thus, Toyama’s First Exemplary Structure does not disclose or render obvious “*a dielectric structure on the isolation structure*” as required by limitation [15.c.i].

(c) Petitioner Fails to Show That Toyama’s First Exemplary Structure Discloses or Renders Obvious “TACs Extending Vertically Through the Dielectric and the Isolation Structures” (Limitation [15.h])

Toyama’s First Exemplary Structure does not disclose or render obvious “*through array contacts (TACs) extending vertically through the dielectric and the isolation structures*” as required by limitation [15.h] because, for all the reasons explained in §§ VI.A.1.a-b, Toyama’s First Exemplary Structure does not disclose or render obvious the isolation structure or a dielectric structure on the isolation structure.

2. Ground 1B: Petitioner Fails to Show That Toyama’s Second Modification Discloses or Renders Obvious Limitations [15.a], [15.c.i], and [15.h]

In Ground 1B, Petitioner relies on Toyama’s Second Modification (of the fourth exemplary structure) as allegedly rendering obvious all Challenged Claims

(Pet. 28-77), but Petitioner fails to show that Toyama’s Second Modification discloses or renders obvious three separate claim limitations: [15.a] (“***a substrate with an isolation structure***”), [15.c.i] (“***a dielectric structure on the isolation structure***”), and [15.h] (“***through array contacts (TACs) extending vertically through the dielectric and the Isolation structures***”).

(a) Petitioner Fails to Show That Toyama’s Second Modification Discloses or Renders Obvious “a Substrate With an Isolation Structure” (Limitation [15.a])

Toyama’s Second Modification does not disclose or render obvious “***a substrate with an isolation structure***” as required by limitation [15.a] because—just like with Toyama’s First Exemplary Structure—the feature of Toyama that Petitioner maps to the “isolation structure” is, at most, located in the region of a cut through the alleged substrate, and is not part of the substrate as required by the Challenged Claims.

As discussed in § VII.A.1.a, the ’378 claim 15 requires “a substrate” to be “***with*** an isolation structure,” meaning that the isolation structure is part of the substrate. As discussed above, the ’378 also describes and depicts the isolation structure as being part of the substrate.

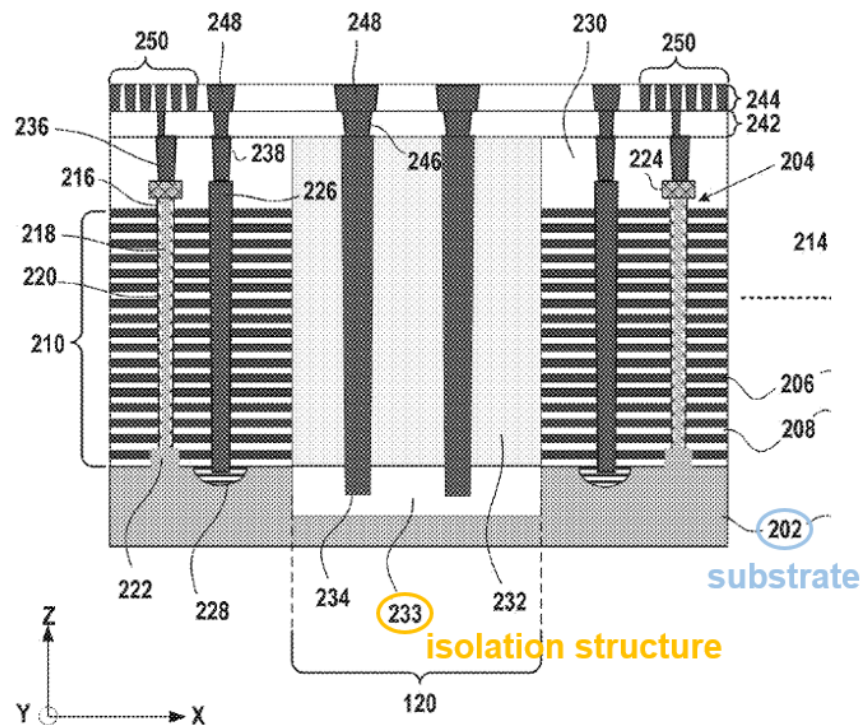


FIG. 2

Ex. 1001, Fig. 2 (annotated and excerpted); *see also* Ex. 1001, 12:54-66, 20:38-42, Figs. 4-13.

Toyama’s Second Modification includes “opening 151” which “may be filled with another insulating material layer [...] 760,” which Petitioner erroneously maps to the isolation structure of the ’378. Pet. 30-31. For the same reasons discussed in § VII.A.1.a, Petitioner’s alleged isolation structure (“opening 151” filled with “insulating material layer 760”) in Toyama’s Second Modification’s is not part of

the alleged substrate (“planar semiconductor material layer 10”).⁵ Specifically, contrary to Petitioner’s misplaced arguments about how the device is made, as illustrated below, the alleged substrate is completely removed in the relevant region, thereby creating a region outside and merely abutting the alleged substrate, and the “insulating material layer 760” is added in that through-opening.

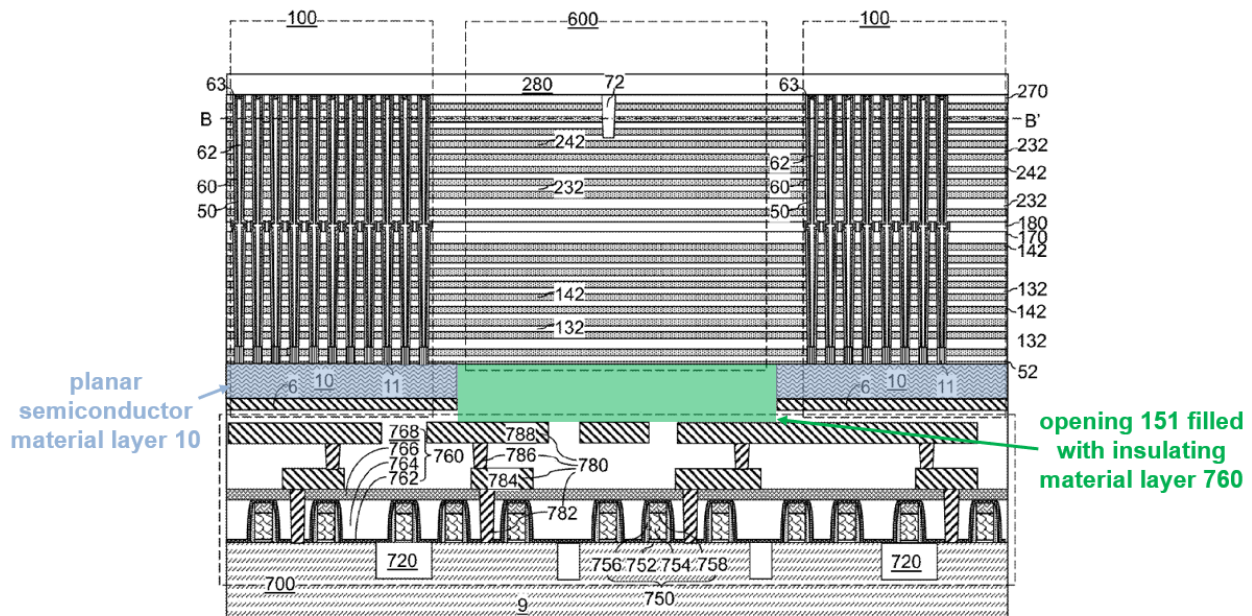


FIG. 44A

Ex. 1005, Fig. 44A (annotated). Thus, there is no alleged substrate “with” that “insulating material layer 760.” In the context of Toyama’s Second Modification, Petitioner never addresses the relationship between two claim limitations, *i.e.*, that

⁵ For the purposes of this POPR, Patent Owner does not dispute Petitioner’s mapping of the claimed “substrate” to Toyama’s “planar semiconductor material layer 10” in Ground 1B.

“a substrate” must be “**with**” “an isolation structure” and simply asserts that it is shown. Pet. 31.

Petitioner’s additional arguments relevant to this limitation made in the context of Toyama’s First Exemplary Structure (Pet. 35-36) fail for the same reasons discussed in § VI.A.1.a above.

Therefore, Petitioner has failed to show that Toyama’s Second Modification discloses or renders obvious limitation [15.a].

(b) Petitioner Fails to Show That Toyama’s Second Modification Discloses or Renders Obvious “a Dielectric Structure on the Isolation Structure” (Limitation [15.c.i])

Toyama’s Second Modification does not disclose or render obvious “**a dielectric structure on the isolation structure**” as required by limitation [15.c.i]. For all the reasons explained in § VI.A.2.a, Toyama’s Second Modification does not disclose or render obvious an isolation structure. As a result, Toyama’s Second Modification does not disclose or render obvious a dielectric structure on the isolation structure.

(c) Petitioner Fails to Show That Toyama’s Second Modification Discloses or Renders Obvious “TACs Extending Vertically Through the Dielectric and the Isolation Structures” (Limitation [15.h])

Toyama’s Second Modification does not disclose or render obvious “**through array contacts (TACs) extending vertically through the dielectric and the isolation**

structures” as required by limitation [15.h] because Toyama’s alleged TACs do not extend through the same structure (the claimed “dielectric structure”).

As an initial matter, for all the reasons explained in §§ VII.A.2.a-b, Toyama’s Second Modification does not disclose or render obvious an isolation structure or a dielectric structure on the isolation structure. As a result, Toyama’s Second Modification does not disclose or render obvious “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.”

In addition, Toyama’s TAC’s do not extend through the same “dielectric structure.” Petitioner maps “insulating liners 674” of “through-memory-level via structures 676” to the “dielectric structure” of the ’378. Pet. 39-42. However, the ’378 claim 15 requires “through array contacts (TACs) **[plural]** extending vertically through the dielectric and the isolation structures.” Even assuming a liner of a TAC can constitute a dielectric structure through which the TAC extends, in Toyama’s Second Modification, only a single “through-memory-level via structure 676” extends through a given “insulating liner 674.” Realizing this problem, Petitioner attempts to map multiple insulating liners 674 to a single “dielectric structure.” Pet. 41.

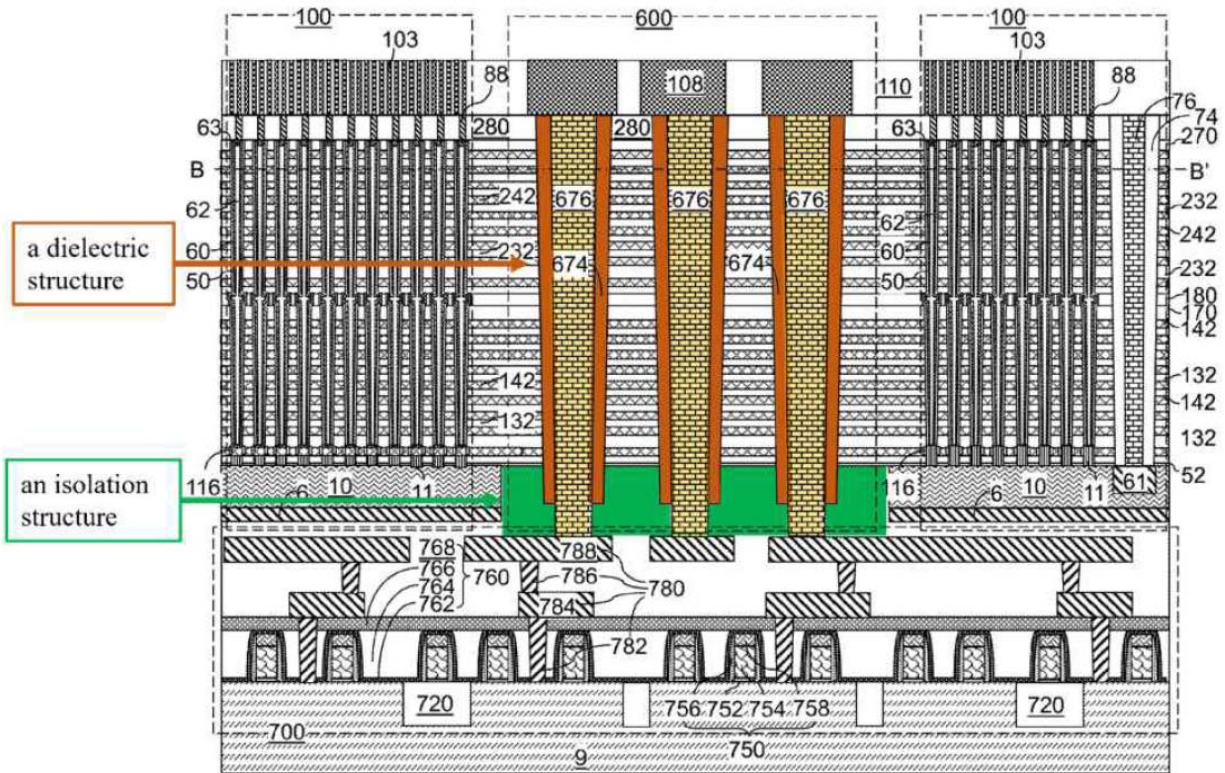


FIG. 49

Ex. 1005, Fig. 49 (annotated by Petitioner at Pet. 40).

In its attempt to map multiple separate liners to a single structure, Petitioner misinterprets the Federal Circuit decision *KCJ Corp. v. Kinetic Concepts* in which the Court found that “an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more’ in open-ended claims containing the transitional phrase ‘comprising.’” *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000). This principle merely means that in a memory structure that reads on the claims there could be more than one dielectric structures in the memory structure, and does **not** mean that more than one dielectric structures can be combined together for any claimed requirements imposed on the claimed “dielectric structure”

(singular). Indeed, the Federal Circuit has made clear that multiple occurrences of a claim element cannot be used satisfy a limitation that must be satisfied by a single occurrence of the element. *Finjan LLC v. SonicWall, Inc.*, 84 F.4th 963, 974-975 (Fed. Cir. 2023) (“‘[T]he indefinite article a means one or more in open-ended claims containing the transitional phrase comprising.’ But that is a separate issue from whether the claims require the same component to perform multiple functions or satisfy multiple limitations of a claim. ... Claim 1 of the ARB Patent requires that the same computer perform each of the claimed steps [...] Even if an infringing system can use ‘one or more computers,’ the plain language of the claims requires at least one of those computers to perform all the functions listed in the claims of the ARB Patent.”) (internal citations omitted). Here, the claim requires that a single “dielectric structure” must have multiple “through array contacts (TACs) extend[] vertically through” it, which any of Toyama’s “insulating liner 674” fails to show.

Therefore, Petitioner has failed to show that Toyama’s Second Modification discloses or renders obvious limitation [15.h].

B. Ground 2: Petitioner Fails to Show That Mushiga Discloses or Renders Obvious Limitations [15.a], [15.c], and [15.h]

Petitioner fails to show that Mushiga discloses or renders obvious multiple independent limitations of the Challenged Claims. In Ground 2, Petitioner relies on Mushiga as allegedly rendering obvious all Challenged Claims (Pet. 77-102), but Petitioner fails to show that Mushiga discloses or renders obvious three separate

claim limitations: [15.a] (“***a substrate with an isolation structure***”), [15.c] (“***a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material***”), and [15.h] (“***through array contacts (TACs) extending vertically through the dielectric and the isolation structures***”).

1. Petitioner Fails to Show That Mushiga Discloses or Renders Obvious “a Substrate With an Isolation Structure” (Limitation [15.a])

Mushiga does not disclose or render obvious “***a substrate with an isolation structure***” as required by limitation [15.a] because—just as with Toyama’s structures—the feature of Mushiga that Petitioner maps to the “isolation structure” is, at most, located in the region of a cut through the alleged substrate, and is not part of the substrate as required by the Challenged Claims.

As discussed in § VII.A.1.a, the ’378 claim 15 requires “a substrate” to be “***with*** an isolation structure,” meaning that the isolation structure is part of the substrate, and the ’378 consistently describes and depicts the isolation structure as being part of the substrate.

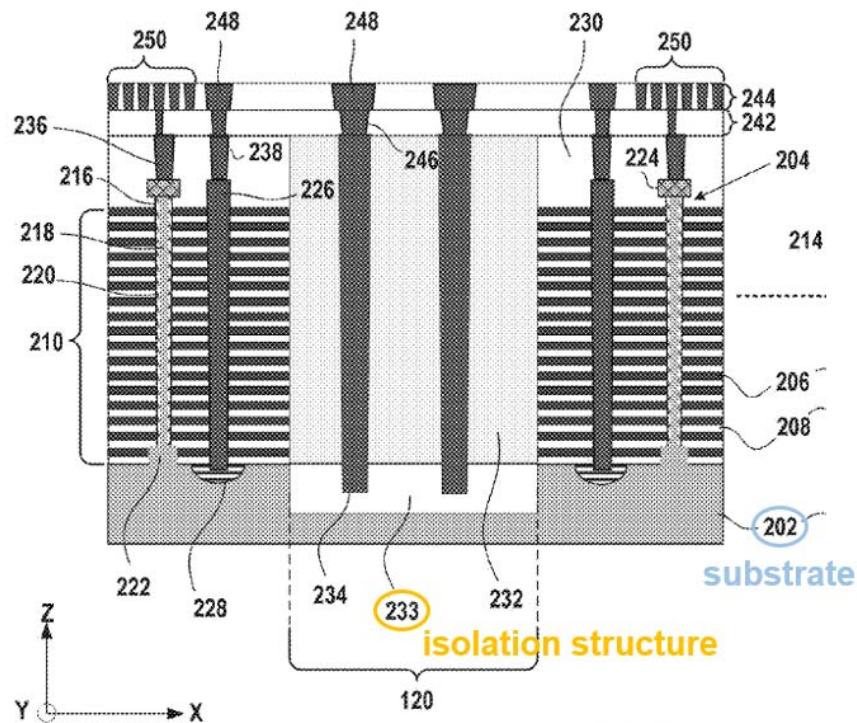


FIG. 2

Ex. 1001, Fig. 2 (annotated and excerpted); *see also* Ex. 1001, 12:54-66, 20:38-42, Figs. 4-13.

Mushiga includes “backside insulating layer 306,” which Petitioner combines with “insulating material liners 302” and erroneously maps to the isolation structure of the ’378. Pet. 79-80.

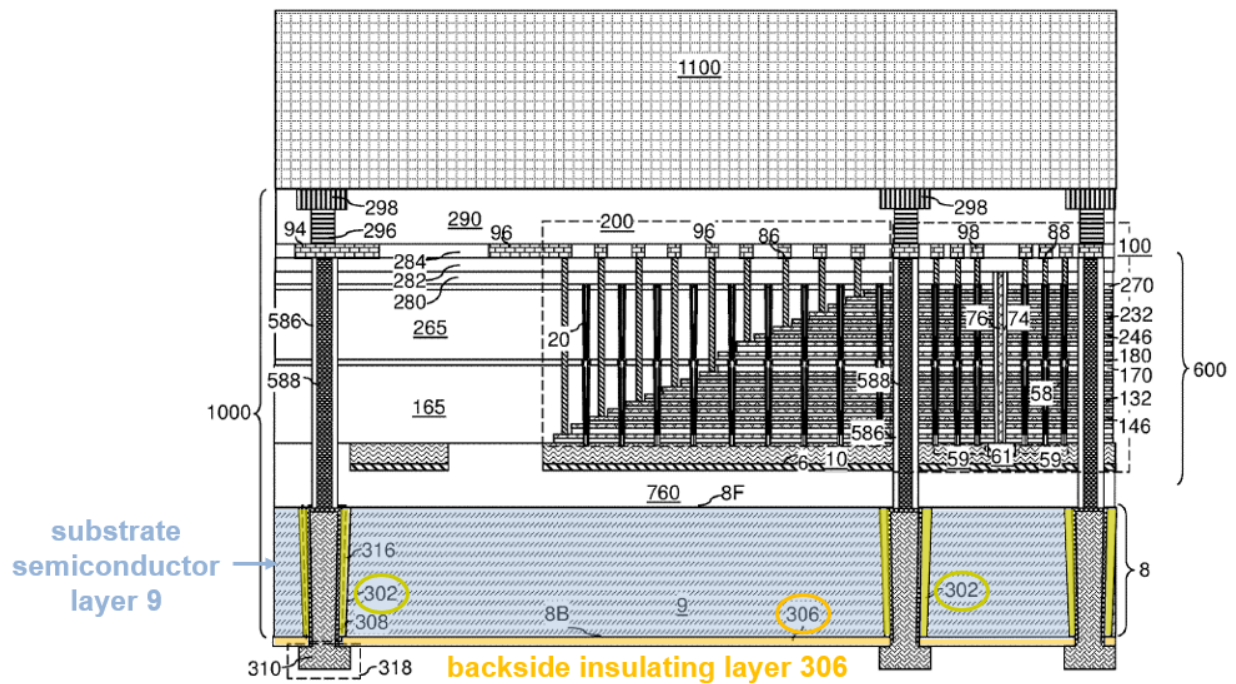


FIG. 11

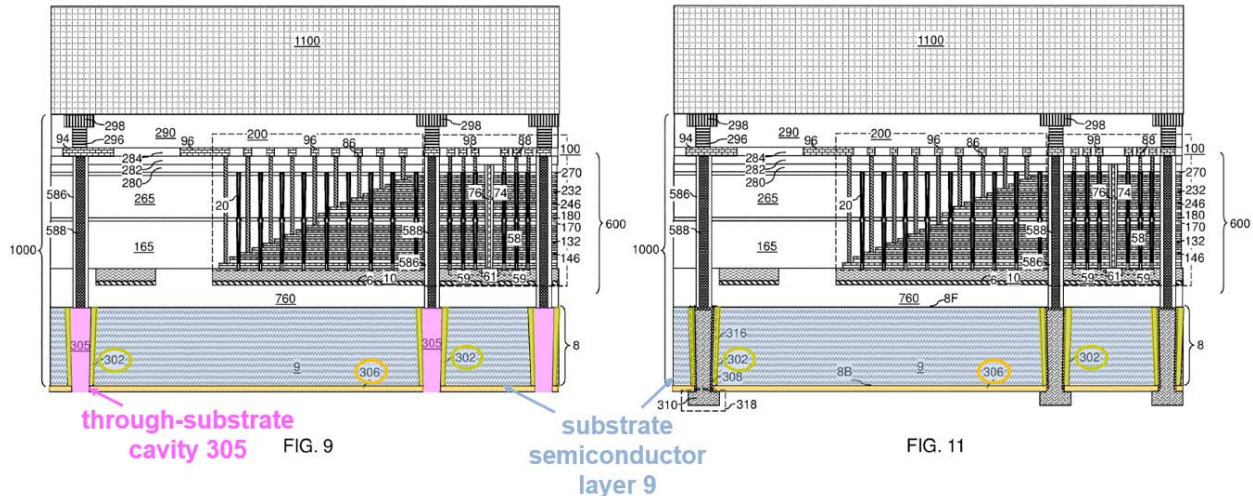
Ex. 1006, Fig. 11 (annotated). Petitioner identifies “**substrate semiconductor layer 9**” as the alleged substrate.⁶

Setting aside whether the backside insulating layer 306 and the insulating material liners 302 can be combined to be the purported isolation structure and whether the insulating material liners 302 are part of the purported substrate, the combination still fails to meet the claims.

⁶ For the purposes of this POPR, Patent Owner does not dispute Petitioner’s mapping of the claimed “substrate” to Mushiga’s “substrate semiconductor layer 9” in Ground 2.

For the same reasons discussed in § VII.A.1.a, at least a portion of Petitioner’s alleged isolation structure (“insulating material liners 302”) in Mushiga is not part of the alleged substrate (“substrate semiconductor layer 9”). “Insulating material liners 302” is an insulating liner filling a cut through the alleged substrate—i.e., the same spatial relationship at issue in Grounds 1A and 1B (Toyama). For the same reasons discussed in § VII.A.1.a, Petitioner’s alleged isolation structure (“insulating material liners 302”) in Mushiga is not part of the alleged substrate (“substrate semiconductor layer 9”).

In an attempt to address the required relationship between two claim terms, *i.e.*, that “a substrate” must be “**with**” “an isolation structure,” Petitioner argues that “Mushiga’s isolation structure [...] **is formed by removing portions of the** substrate [...]” (Pet. 79-80 (citing Ex. 1003, ¶ 173-174) (emphasis added)), but this argument fails for the same reasons discussed in § VII.A.1.a. As illustrated below, and again contrary to Petitioner’s misplaced arguments regarding how the devices are made, the alleged substrate is completely removed in the relevant region, thereby creating regions outside and merely abutting the alleged substrate (“**through-substrate cavities 305**”), and the “**insulating material liners 302**” is in those through-openings.



Ex. 1006, Figs. 9, 11 (annotated). After the substrate is removed, there is no longer any portion of the alleged substrate in the relevant region. Moreover, these steps relate to the manufacturing process, not the final structure, and the Challenged Claims are apparatus claims.

Therefore, Petitioner has failed to show that Mushiga discloses or renders obvious “*a substrate with an isolation structure*” as required by limitation [15.a].

2. Petitioner Fails to Show That Mushiga Discloses or Renders Obvious “a Dielectric Structure on the Isolation Structure and Extending Vertically through the Alternating Conductor/Dielectric Layer Stack” (Limitation [15.c])

Mushiga does not disclose or render obvious “*a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack*” as required by limitation [15.c] because the only alleged “dielectric structure” that extends though the stack is not also “on the isolation structure.”

As an initial matter, for all the reasons explained in § VII.B.1, Mushiga does not disclose or render obvious an isolation structure. As a result, Mushiga also does not disclose or render obvious a dielectric structure on the isolation structure.

Petitioner's mapping for this element also fails because the alleged "dielectric structure" is not both "extending vertically through the alternating conductor/dielectric layer stack" (mapped to "alternating stack (132, 146, 232, 246)") and "on the isolation structure." Petitioner maps "insulating material layer 760," "first retro-stepped dielectric material portion 165," "inter-tier dielectric layer 180," "second retro-stepped dielectric material portion 265," and "insulating spacer 586" collectively to the "dielectric structure" of the '378. Pet. 81-83.

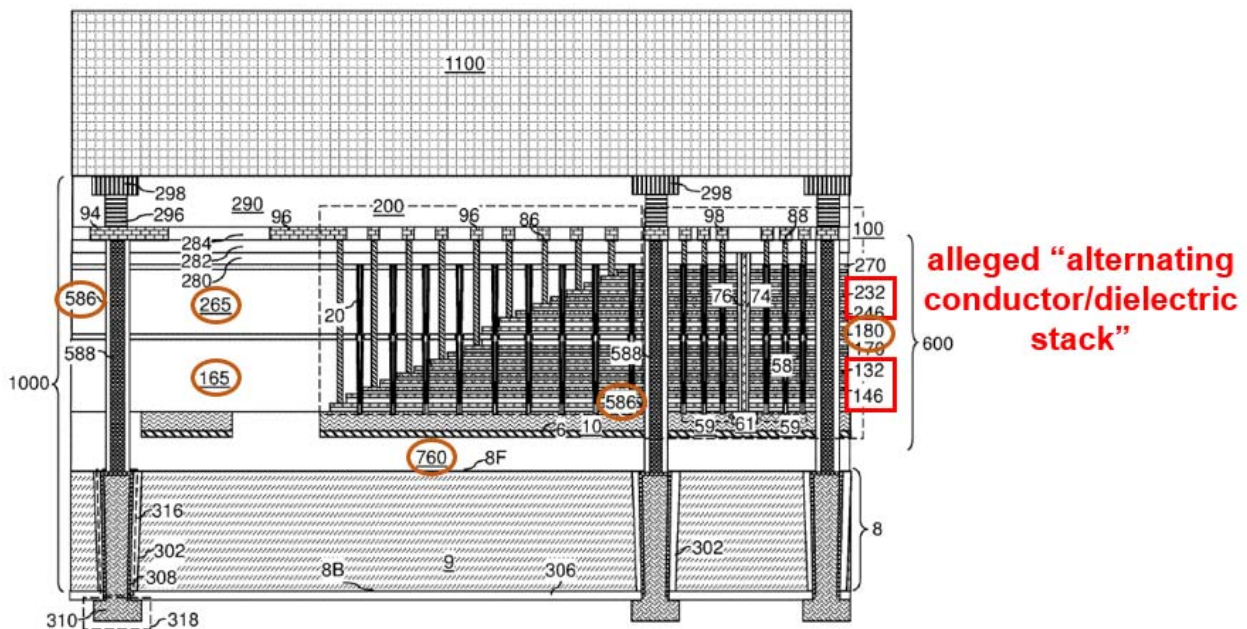


FIG. 11

Ex. 1006, Fig. 11 (annotated).

Among these elements, only the “insulating spacers 586” is even arguably **“extending vertically through the alternating conductor/dielectric layer stack”** as required by Limitation [15.c]. As can be seen in the above figure, the other features are either outside the alternating stack altogether or, in the case of “inter-tier dielectric layer 180,” it makes a horizontal cut across the alternating stack instead of extending vertically through the stack.

While “insulating spacers 586” arguably extend through the alleged alternating conductor/dielectric layer stack, they are not **“a dielectric structure on the isolation structure”** as required by the Challenged Claims (even assuming, *arguendo*, that Petitioner has identified an isolation structure).

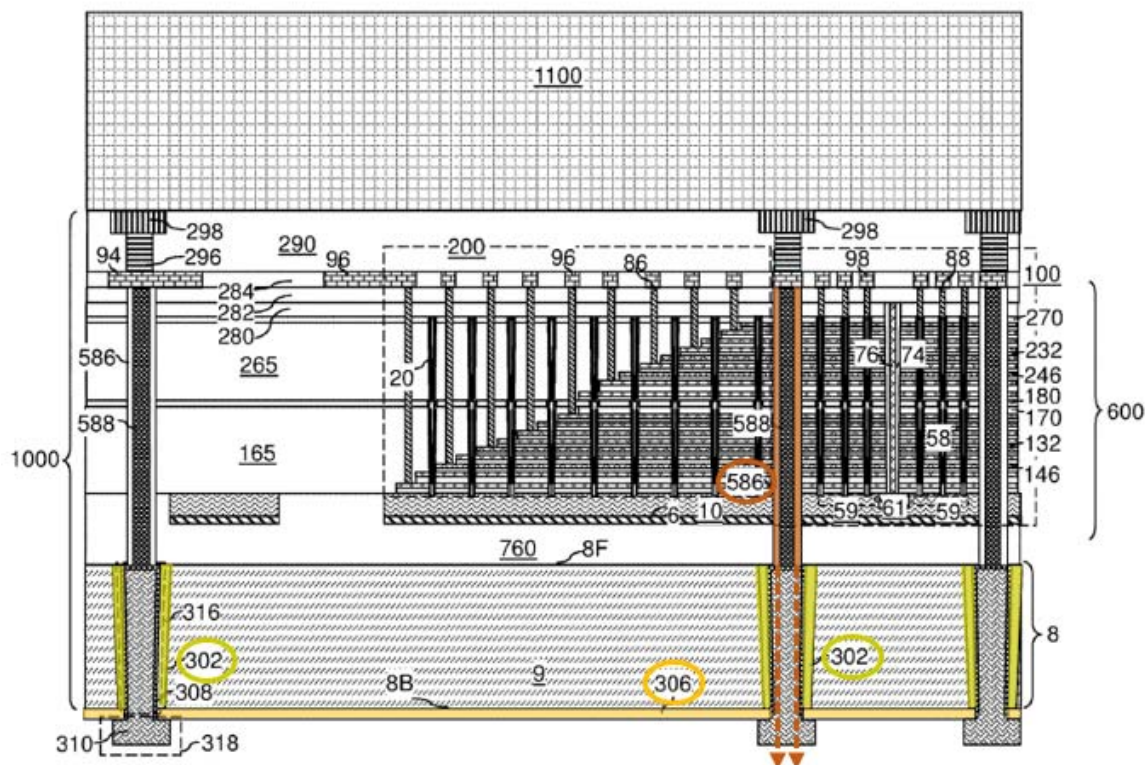
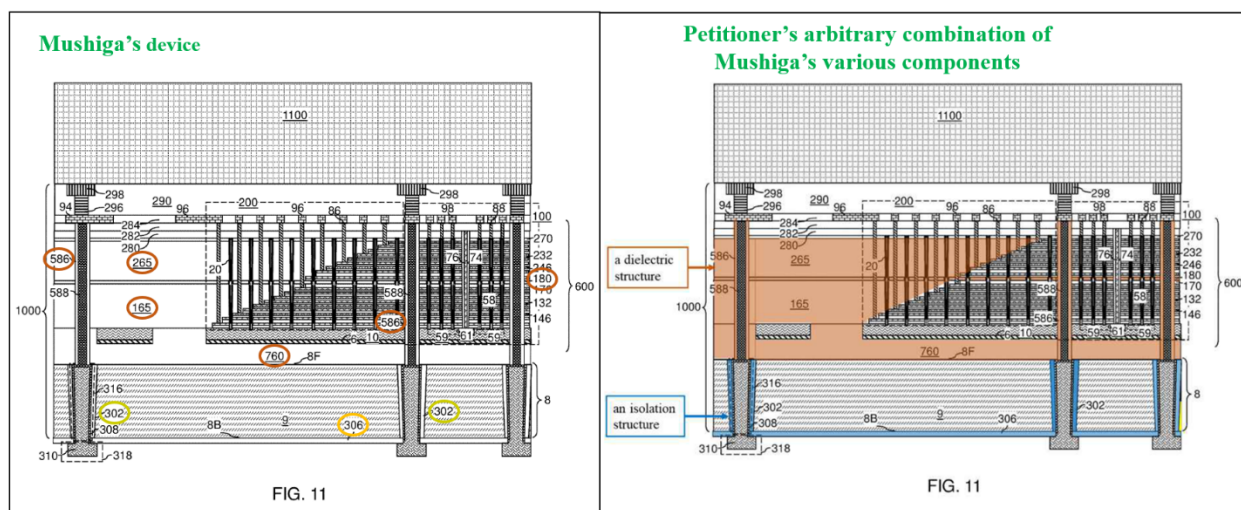


FIG. 11

Ex. 1006, Fig. 11 (annotated). As shown in the figure, **insulating spacers 586** are not “on” Petitioner’s alleged isolation structure—**backside insulating layer 306** and **insulating material liners 302**.

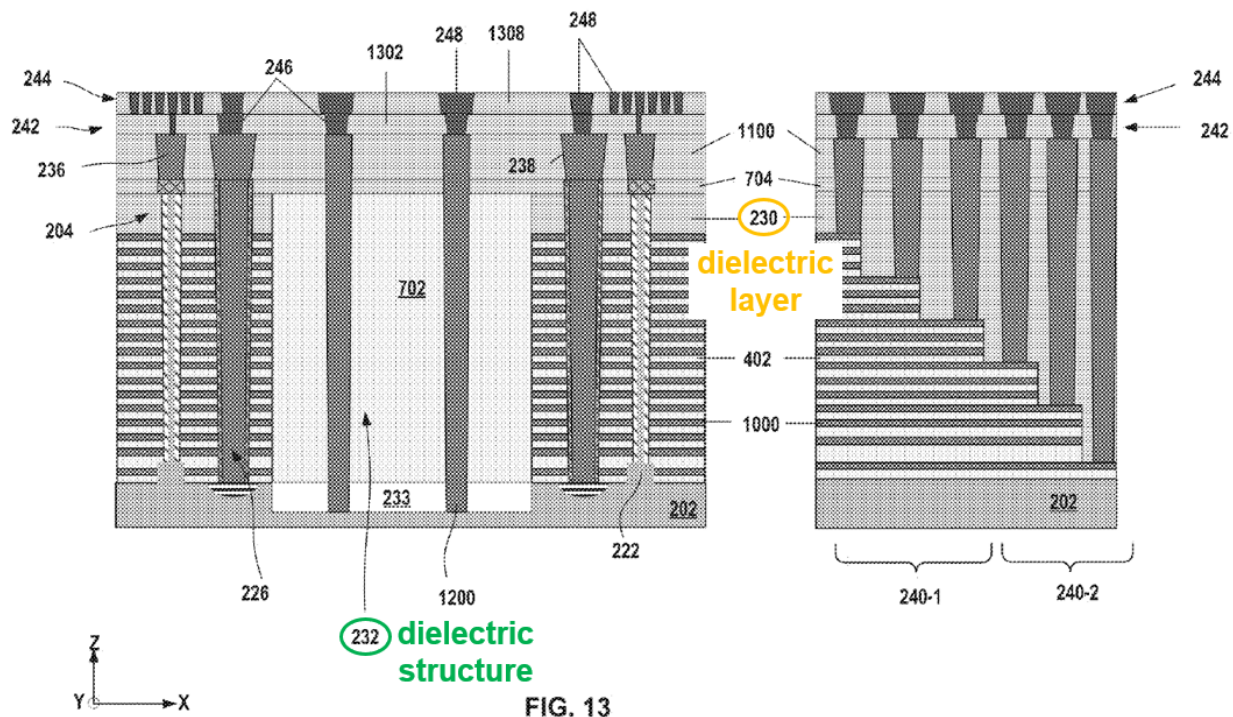
Additionally, “insulating spacer 586” fails to meet the claim limitation **“through array contacts (TACs) [plural] extending vertically through the dielectric and the isolation structures”** [15.h] in the same way as Toyama’s “insulating liner 674.” See § VII.A.2.c, *supra*.

Realizing that “insulating spacer 586” fails to satisfy all the requirements of the claimed “dielectric structure,” Petitioner attempts to combine the spacer with multiple other dielectric regions (Pet. 81-84), but its grouping has no discernable logic and does not cure the issue. The elements Petitioner combines each have distinct locations and roles compared to the ’378’s dielectric structure.



Ex. 1006, Fig. 11 (left image annotated by Patent Owner; right image annotated by Petitioner at Pet. 82, with top heading added by Patent Owner).

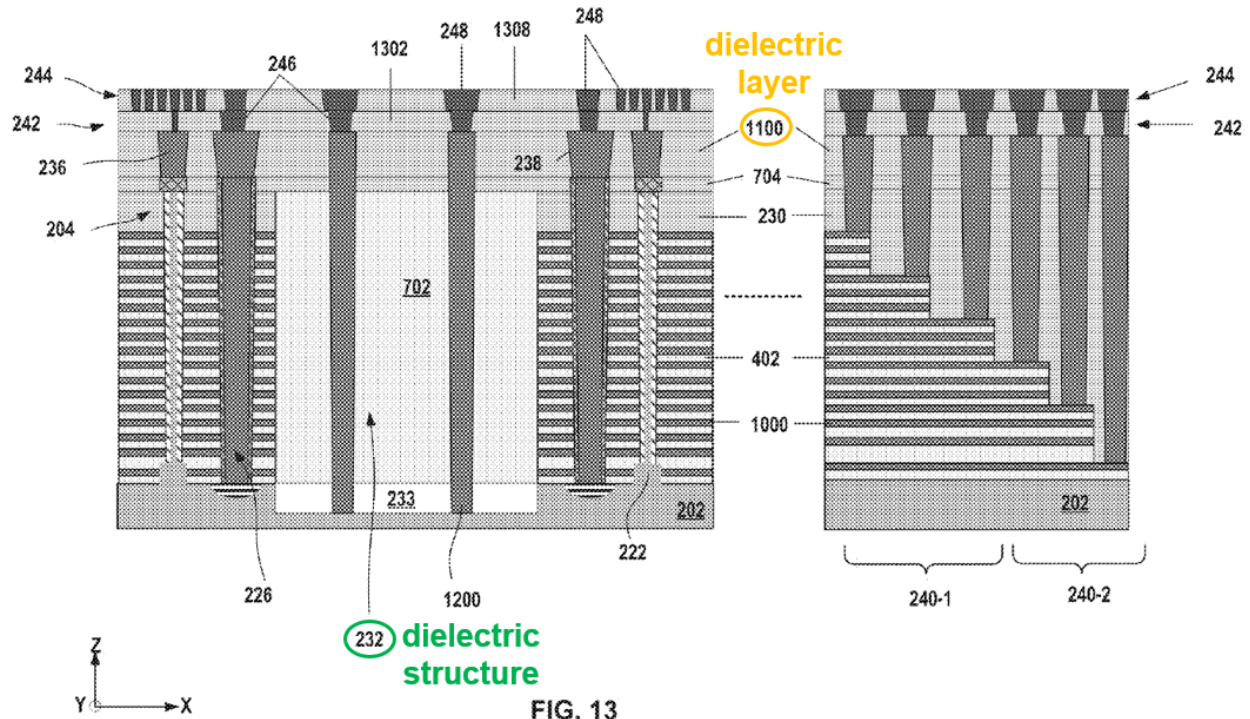
For example, Mushiga's "first retro-stepped dielectric material portion 165" and "second retro-stepped dielectric material portion 265" in combination are nothing more than the dielectric material that covers the stair steps (Ex. 1006, 9:22-26, 9:38-39), which the '378 identifies as "dielectric layer 230" (separate from the '378's "dielectric layer 702" that is on the isolation structure and extending vertically through the stack).



Ex. 1001, Fig. 13 (annotated).

Similarly, Mushiga's "insulating material layer 760" is a dielectric material layer that separates Mushiga's alleged substrate ("semiconductor layer 9") from "semiconductor material layer 10." Ex. 1006, 9:8-12. Thus, Mushiga's "insulating material layer 760" is akin to the '378's "dielectric layer 1100" shown below, which

is above and spans the full area of the alternating stack (and is separate from the '378's “dielectric layer 702” that is on the isolation structure and extending vertically through the stack).



Ex. 1001, Fig. 13 (annotated).

In its purported combination of adjacent dielectric elements, Petitioner also inconsistently omitted other adjacent dielectric elements that, if included, would have hurt its claim mapping. For example, as shown below in Mushiga's Fig. 11, the red annotated dielectric features were not included.

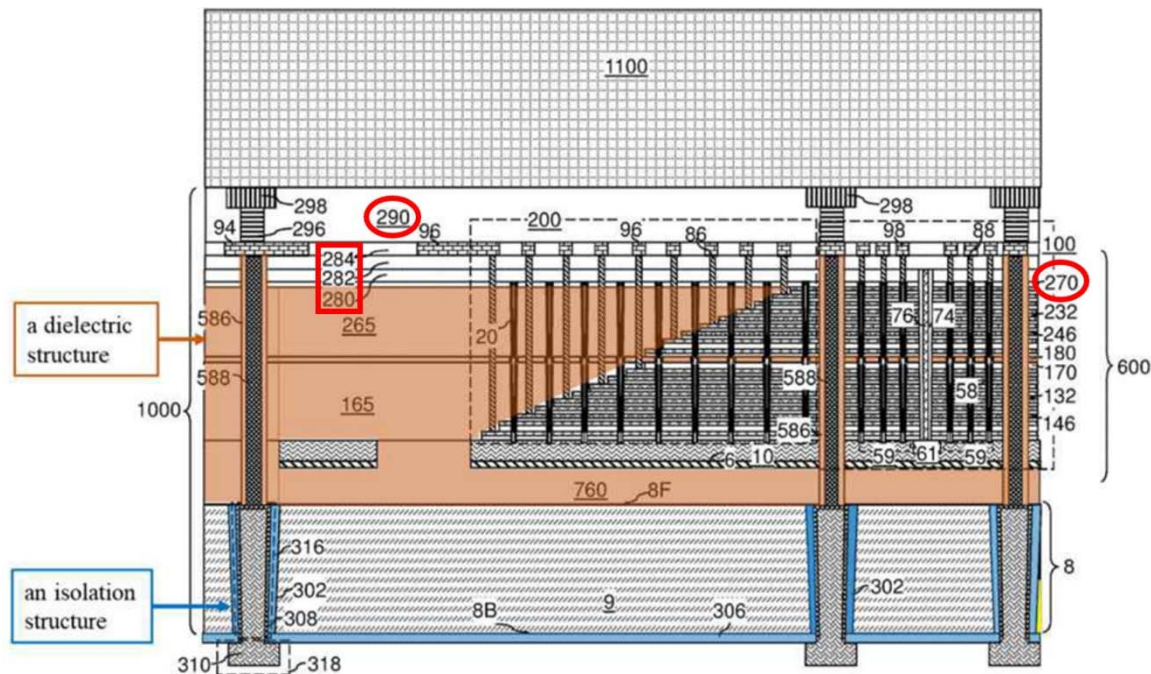


FIG. 11

Ex. 1006, Fig. 11 (annotated by Petitioner at Pet. 82, with red annotations added by Patent Owner). By Petitioner's logic of coloring in as one structure different dielectric features that are merely adjacent, Petitioner also should have included layers 270 ("second insulating cap layer 270"), 280 ("first contact level dielectric layer 280"), 282 ("second contact level dielectric layer 282"), 284 ("line level dielectric layer 284"), and 290 ("additional interconnect level dielectric layers 290"). This would have led to a situation in which Mushiga's through-memory level vias 588 (the alleged TACs) do not extend through the alleged dielectric structure as required by the Challenged Claims, as they would terminate within the dielectric structure (between layers 282 and 284). Petitioner's choices of which dielectric features to include and which to exclude in its mapping of Mushiga to the claimed

dielectric structure is inconsistent and originate purely from hindsight, rather than a teaching in the cited art or the knowledge of a POSITA.

Therefore, Petitioner has failed to show that Mushiga discloses or renders obvious limitation [15.c].

3. Petitioner Fails to Show That Mushiga Discloses or Renders Obvious “TACs Extending Vertically Through the Dielectric and the Isolation Structures” (Limitation [15.h])

Mushiga does not disclose or render obvious “*through array contacts (TACs) extending vertically through the dielectric and the isolation structures*” as required by limitation [15.h] because, for all the reasons explained in §§ VII.B.1-2, Mushiga does not disclose or render obvious the isolation structure or a dielectric structure on the isolation structure.

Additionally, “insulating spacer 586” fails to meet this limitation in the same way as Toyama’s “insulating liner 674.” *See* § VII.A.2.c, *supra*. For example, Mushiga’s alleged TACs do not extend through the same “dielectric structure” because each TAC has a separate, unconnected insulating spacer 586, which Petitioner improperly combines for the alleged “dielectric structure.” *See* Pet. 98. As discussed in § VII.A.2.c, multiple occurrences of a claim element cannot be used satisfy a limitation that must be satisfied by a single occurrence of the element. *Finjan*, 84 F.4th at 974-975.

C. Ground 3: Petitioner Fails to Show That Mushiga in view of Makala Discloses or Renders Obvious Limitations [15.a], [15.c], and [15.h]

Petitioner fails to show that Mushiga in view of Makala discloses or renders obvious limitations [15.a], [15.c], and [15.h] for the same reasons discussed above for Ground 2. In Ground 3, Petitioner relies on Mushiga in view of Makala as allegedly rendering obvious claims 15-17 and 19-20 of the '378. However, the Petition does not raise any new arguments as to limitations [15.a], [15.c], and [15.h]. Rather, the Petitioner applies Makala's teaching to Mushiga only for limitation [15.g.ii] ("local contacts disposed on ... the slit structures") and "relies solely on Mushiga" for all other limitations. Pet. 102-103. As explained in § VII.B, Petitioner fails in Ground 2 to show that limitations [15.a], [15.c], and [15.h] are disclosed or rendered obvious, and since no additional arguments are introduced regarding these limitations, Petitioner also fails in Ground 3.

Accordingly, the Board should find that Petitioner has failed to meet its burden of showing Mushiga in view of Makala discloses or renders obvious limitations [15.a], [15.c], and [15.h] in Ground 3.

VIII. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board deny institution.

Dated: August 12, 2024

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word-processing system's word count, the brief contains 10,863 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

Dated: August 12, 2024

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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