UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

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Case No.: IPR2024-00788
U.S. Patent No. 10,658,378

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# PATENT OWNER'S RESPONSE UNDER 37 C.F.R. § 42.120

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## LIST OF EXHIBITS

| Exhibit | Description |
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| Ex. 2001 | Micron 4-2 Claim Construction Disclosure |
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| Ex. 2003 | Micron's Preliminary Claim Constructions |
| Ex. 2004 | YMTC's Proposed Claim Constructions |
| Ex. 2005 | February 10, 2025, Declaration of Dr. Yang ("Yang") |
| Ex. 2006 | Decision Granting Institution of *Inter Partes Review* of U.S. Patent No. 10,937,806 (IPR2024-00791, Paper 11) |
| Ex. 2007 | Deposition Transcript of Dr. Lee |

## LIST OF ABBREVIATIONS

| Abbreviation | Term |
|---|---|
| ’378 | U.S. Pat. No. 10,658,378 |
| ’378FH | File History of U.S. Pat. No. 10,658,378 |
| Challenged Claims | Ex. 1001, Claims 15-17, 19-20 |
| Office | U.S. Patent and Trademark Office |
| Petition or Pet. | Petition for *Inter Partes* Review of U.S. Patent No. 10,658,378 (IPR2024-00788, Paper 1) |
| Parallel district court litigation | *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.*, NDCA-3-23-cv-05792 (N.D. Cal.) |
| Patent Owner or PO | Yangtze Memory Technologies Co. Ltd. |
| Petitioner | Micron Technology, Inc. |
| POSITA | Person of ordinary skill in the art |
| Toyama | U.S. Patent Publication No. 2017/0179026 |
| Mushiga | U.S. Patent No. 10,354,980 |
| Makala | U.S. Patent No. 10,262,945 |

# I. INTRODUCTION

The references in Petitioner's Grounds fail to disclose or render obvious the Challenged Claims of U.S. Patent No. 10,658,378 ("'378," Ex. 1001). For example, the art fails to disclose or render obvious at least three separate limitations of claim 15—the sole challenged independent claim from which the other challenged claims depend: [15.a] ("a substrate with an isolation structure"), [15.c.i] ("a dielectric structure on the isolation structure"), and [15.h] ("through array contacts (TACs) extending vertically through the dielectric and the isolation structures"). In addition, Petitioner fails to show that the art discloses or renders obvious claim 17, which further requires "the dielectric structure comprises a through array contact region of the 3D memory device."

The '378 is directed to a novel three-dimensional (3D) memory device having through array contacts and methods related to manufacturing such a device. As memory cells are scaled down and the density of memory cells increases, it becomes challenging to collect and route signals to the peripheral circuitry efficiently. The '378 provides a solution by forming through array contacts (TACs) in a dedicated region where they provide vertical interconnects to the peripheral devices. '378, 1:20-32, 2:19-21, 5:46-50, 11:3-9, 19:55-60.

Fabrication of 3D NAND memory devices generally involves stacks of alternating dielectric and conductive layers, through which vertical structures, such

as channels and vias, are formed. ’378, 1:38-55. The prior art at the time of filing of the ’378 formed vertical vias within the alternating dielectric and conductive layers, which “increases the fabrication cost.” ’378, 10:59-66, 18:27-33. The ’378 simplifies the fabrication process of these TACs by forming them in a dedicated dielectric structure. ’378, 18:27-33. The ’378 thereby avoids the issues in the prior art such as using a complex and costly etching process due to having to etch through alternating dielectric and conductive layers for individual TACs. ’378, 5:35-39, 10:59-66, 18:27-41, 20:9-16. The ’378 further uses an isolation structure (*e.g.*, a “shallow trench isolation”) in the substrate on which the dielectric structure is placed and through which the lower portions of the TACs extend. ’378, 10:30-33, 21:17-25.

The ’378 introduced a 3D memory device in which TACs “extend vertically through” the “dielectric structure” and the “isolation structure,” and methods of manufacturing such a device. ’378, Abstract, 10:57-59, 21:17-25. The claimed invention recites “a substrate with an isolation structure,” a “dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack,” and “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.” *See* ’378, Claim 15. As a result, the claimed invention avoids the issues arising from forming TACs

through alternating dielectric/conductor stacks and "simplif[ies] the fabrication process and reduce[s] the fabrication cost." '378, 18:36-41.

The Petition fails to establish that any of the Challenged Claims is disclosed or rendered obvious. Specifically, Petitioner sets forth the following obviousness grounds challenging '378 independent claim 15 and its dependent claims 16-17, 19-20:

Ground 1A: Toyama's (Ex. 1005) "First Exemplary Structure;"

Ground 1B: Toyama's "second modification of the fourth exemplary structure" ("Second Modification");

Ground 2: Mushiga (Ex. 1006); and

Ground 3: Mushiga in view of Makala (Ex. 1007).

Petitioner does not assert that any of the cited references anticipates the Challenged Claims, and instead raises obviousness based on a mix of contradictory assertions, faulty analysis, and pure hindsight.

Petitioner's Ground 1A relies on Toyama's First Exemplary Structure, but the First Exemplary Structure does not teach, for example, "a substrate with an isolation structure" as required by limitation [15.a] because the feature of Toyama that Petitioner maps to the "isolation structure" is, at most, located in the region of a cut through the alleged substrate, and is not "part of" the substrate as required under the proper construction of this term. In addition, Toyama's First Exemplary Structure

does not disclose or render obvious "a dielectric structure on the isolation structure" as required by limitation [15.c.i] because Petitioner arbitrarily and improperly divides Toyama's single dielectric structure into two regions and maps different regions to two separate features of the Challenged Claims: the "dielectric structure" and the "isolation structure."

Petitioner's Ground 1B relies on Toyama's Second Modification, but the Second Modification does not teach, for example, "a substrate with an isolation structure" as required by limitation [15.a] for the same reasons as for Toyama's First Exemplary Structure. In addition, Toyama's Second Modification does not disclose or render obvious "through array contacts (TACs) extending vertically through the dielectric and the isolation structures" as required by limitation [15.h] because Toyama's alleged TACs do not extend through the same structure (the claimed "dielectric structure").

Petitioner's Ground 2 relies on Mushiga for each limitation of the Challenged Claims, but Petitioner fails to show that Mushiga discloses or renders obvious, for example, "a substrate with an isolation structure" as required by limitation [15.a] for similar reasons as for Toyama. In addition, Mushiga does not disclose or render obvious "a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack" as required by limitation [15.c] because the only alleged "dielectric structure" that extends though the stack

is not also "on the isolation structure," and Mushiga does not disclose or render obvious "through array contacts (TACs) extending vertically through the dielectric and the isolation structures" as required by limitation [15.h] because Mushiga's alleged TACs do not extend through the same structure (the claimed "dielectric structure"). Petitioner's arguments are again founded on faulty mappings that, for example, inconsistently include or exclude features of Mushiga's device based on hindsight.

Petitioner's Ground 3 applies certain teachings of Makala to Mushiga but only as to a particular requirement of claim 15. Specifically, Petitioner does not raise any new arguments as to the aforementioned limitations and instead relies on its Ground 2 arguments (Pet. 102). Therefore, Petitioner's arguments fail for at least the reasons provided regarding Petitioner's Ground 2.

Finally, all of Petitioner's grounds fail to disclose or render obvious the additional requirement of claim 17 that "the dielectric structure comprises a through array contact region of the 3D memory device" because the alleged TAC region of each ground is not within or defined by the alleged dielectric structure as required under the proper construction of this term.

Because each prior art, individually or combined, fails to disclose or render obvious any of the Challenged Claims, the Board should find in favor of Patent Owner and uphold the validity of all Challenged Claims.[1]

## II. THE CLAIMED INVENTION OF THE '378 PATENT

The claimed invention of the '378 is directed to a "three-dimensional (3D) memory device" and related methods that address issues arising from the fabrication techniques known in the prior art and "simplif[y] the fabrication process and reduce[s] the fabrication cost." '378, Abstract, 18:36-41. Yang, ¶31.

Specifically, the '378 is directed to an improved 3D memory device and methods for forming such a device in which "through array contacts (TACs)" "extend vertically through" the "dielectric structure" and the "isolation structure." Ex. '378, Abstract, 10:57-59, 21:17-25. 3D memory devices in the prior art at the time of filing of the '378 involved through array vias that form connections between various components of the device to reduce size and increase density. '378, 1:20-32. These vias were placed within the alternating dielectric and conductive layers,

[1] This Patent Owner Response is supported by the declaration of Dr. Yang. *See* Ex. 2005 ("Yang"), ¶¶1-30. All emphasis and color annotations have been added unless otherwise noted.

which required a complex etching process and "increase[d] the fabrication cost." '378, 10:59-66. Yang, ¶32.

The novel device the '378 teaches and recites in the Challenged Claims is characterized by "a **substrate** with an **isolation structure**" and **TACs** that "extend vertically through" the "**dielectric structure**" and the "**isolation structure**." '378, Abstract, 10:57-59, 21:17-25, Claim 15. This novel configuration of elements allows for easier and less costly manufacture of 3D memory devices. '378, 5:55-59, 18:27-33, 20:29-37.

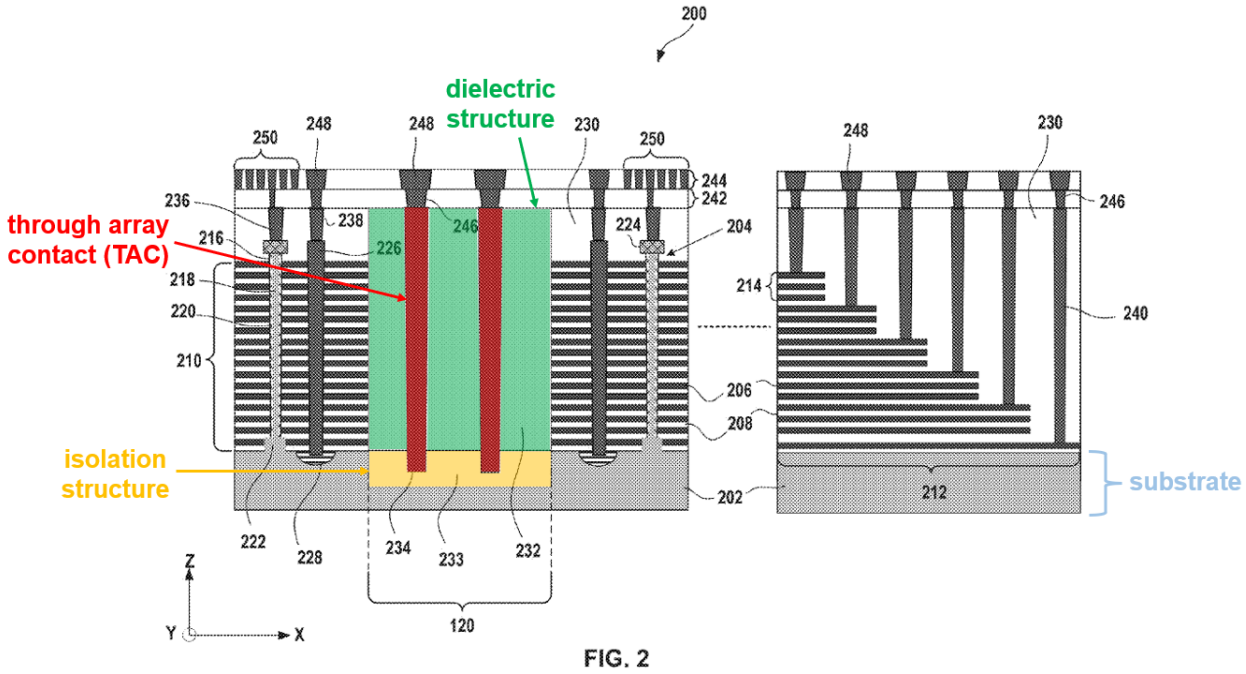



FIG. 2

'378, Fig. 2 (annotated). Yang, ¶33.

A representative embodiment of the '378's memory device includes: (1) "**substrate 202**" with "**isolation structure 233**" ('378, 10:30-35, 22:27-38); (2) "**alternating conductor/dielectric layer stack 210**" ('378, 8:17-25); (3)

"**dielectric structure 232**" on "**isolation structure 233**" ('378, 10:18-29); (4) "**channel structures 216**" and "**slit structures 226**" extending vertically through "**alternating conductor/dielectric layer stack 210**" ('378, 9:1-6, 10:1-6); (5) "**staircase structure 212**" ('378, 8:48-55); (6) "**word line contacts 240**" (11:24-26); (7) "**local contacts**" on "**channel structures 216**" and "**slit structures 226**" (11:24-26); and (8) "**TACs 234**" extending vertically through "**dielectric structure 232**" and "**isolation structure 233**" ('378, 10:57-59, 20:45-48). A cross-section view of the memory device is below.

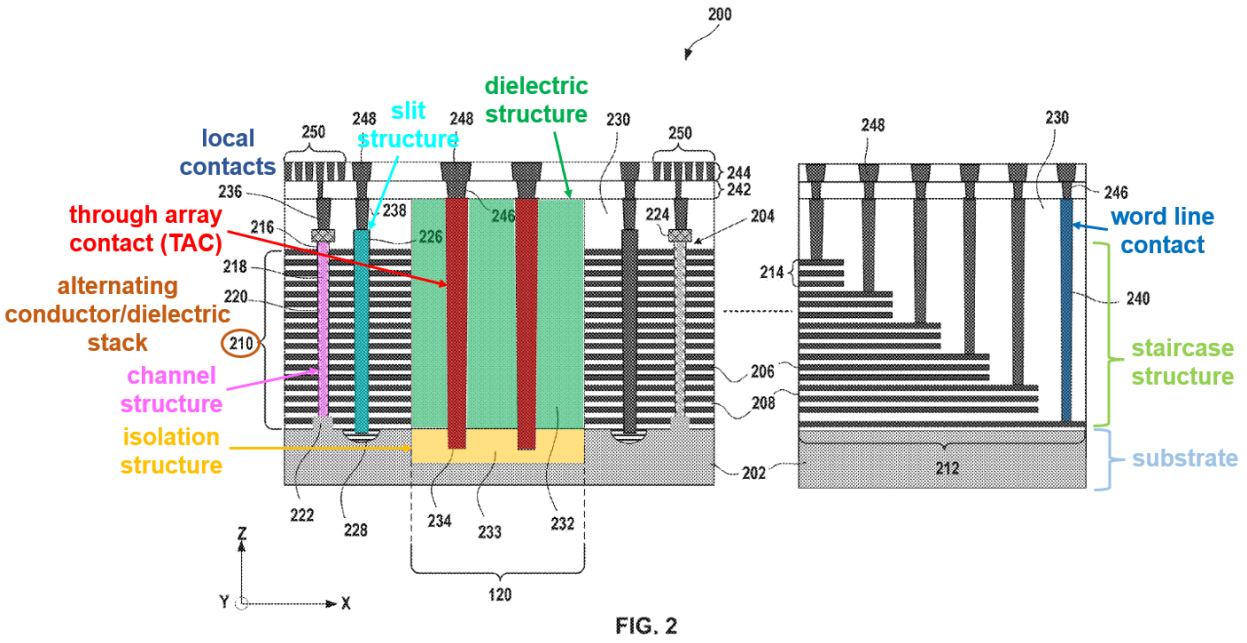


FIG. 2

'378, Fig. 2 (annotated). Yang, ¶¶34-35.

The only independent claim of the Challenged Claims, claim 15, is directed to aspects of the above-described invention:

[15.pre] A three-dimensional (3D) memory device, comprising:

[15.a] a substrate with an isolation structure;

[15.b] an alternating conductor/dielectric layer stack disposed on the substrate;

[15.c] a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

[15.d] channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;

[15.e] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

[15.f] a word line contact disposed on the conductor layer of the each level;

[15.g] local contacts disposed on the channel structures and the slit structures; and

[15.h] through array contacts (TACs) extending vertically through the dielectric and the isolation structures.

## III. FILE HISTORY

The claims of the ’378 remain patentable over the prior art for at least the same reason identified during prosecution. As discussed further below in §§VI-IX, the prior art does not disclose or render obvious, *inter alia*, the ’378 claim elements “a substrate with an isolation structure,” “a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material,” and “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.” Claims directed to these limitations were allowed after thorough prosecution and consideration of numerous prior art references.

The ’378 was filed on July 27, 2018. After a preliminary amendment where Applicant removed multiple claim dependency and corrected a typographical error, the application included 3 independent claims (pending claims 1, 10, and 16) and 17 dependent claims (pending claims 2-9 which depended from claim 1, claims 11-15 which depended from claim 10, and claim 17-20 which depended from claim 16). Ex. 1002, 105-111 (12/06/2018 Preliminary Amendment). Yang, ¶36.

In a non-final office action, the Examiner rejected pending claims 1, 3-16, and 18-20 under 35 U.S.C. §103 as being allegedly obvious over U.S. Patent 9,620,512

("Nishikawa") in view of U.S. Patent Publication No. 2016/0056188 ("Lee"), but found that pending claims 2 and 17 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." Ex. 1002, 529-537 (08/22/2019 Office Action). Yang, ¶37.

Applicant followed the Examiner's suggestion "[w]ithout acquiescing to the propriety of the rejection" and rewrote pending claims 2 and 17 in independent form. Applicant also amended pending claim 10 "[w]ithout acquiescing to the propriety of the rejection" to "recite features that further distinguish it from Nishikawa and Lee." Ex. 1002, 569 (12/23/2019 Amendment and Reply). Having placed the independent claims in allowable form, Applicant requested that their respective dependent claims also be allowed. Applicant further added two new claims that depend from pending claim 16. Ex. 1002, 563-571 (12/23/2019 Amendment and Reply). The Examiner subsequently allowed all pending claims. Ex. 1002, 579-586 (01/13/2020 Notice of Allowance). The '378 issued on May 19, 2020 with twenty claims, including the renumbered independent claims 1, 9, and 15. Ex. 1002, 602 (04/29/2020 Issue Notification). Yang, ¶38.

After the first office action and before Applicant's response, Applicant filed an information disclosure statement (IDS) that notified the Examiner of U.S. Patent Publication No. 2017/0179026 ("Toyama"). Ex. 1002, 555 (12/03/2019 Information Disclosure Statement). The Examiner considered Toyama and explicitly cited it as

a "reference[] considered." Ex. 1002, 593 (01/13/2020 List of References Cited by Applicant and Considered by Examiner). Petitioner's assertion that "Patent Owner only gave Examiner a haystack" (Pet. 12) is belied by the fact that Applicant submitted an IDS solely to cite Toyama, which was then explicitly considered by the Examiner. Moreover, the '378 was issued with only sixteen references (nine U.S. patent documents and six foreign patent documents) one of which is Toyama. '378, (56). Thus, the Examiner duly considered Toyama, but found it lacking as should the Board here. Yang, ¶39.

## IV. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this proceeding only, Patent Owner does not object to the definition of a person of ordinary skill in the art ("POSITA") proffered by Petitioner and adopted by the Board at institution. Pet. 27. The Challenged Claims are valid regardless of the precise definition used for a POSITA. Yang, ¶¶40-44.

## V. CLAIM CONSTRUCTION

Other than the terms identified below, Patent Owner submits that constructions of the claim terms are not necessary to assess whether the prior art reads on the Challenged Claims for the purposes of the *inter partes* review. Patent Owner, however, reserves the right to modify or elaborate on its proposed constructions and to raise further claim construction issues in the parallel district court proceedings. Yang, ¶45.

The parties recently exchanged proposed claim constructions in the parallel district court proceeding. Exs. 2003-2004. Aside from the terms identified below, the claim construction disputes in district court do not impact the issues raised in this Response.

**A. "a dielectric structure on the isolation structure" (Claim 15)**

The term "on" should be construed to mean "above" in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction. As confirmed by the '378, the term does not permit reorienting the direction of the "on" spatial relationship to encompass any relative position. Yang, ¶46.

Both in the claims and specification, the term "on" is used to indicate a specific spatial relationship between the isolation structure and substrate, or the dielectric structure and the isolation structure, in which the former structure is above the latter. The claims consistently use the term "on" to refer to above (e.g., "a dielectric structure on the isolation structure" as recited in claim 15) and use the different term "abut" to refer to the lateral direction (e.g., "the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure" as recited in claim 15). Yang, ¶47.

The specification expressly defines the term:

> As used herein, whether one component (e.g., a layer or a device) is ***"on,"*** "above," or "below" ***another component*** (e.g., a layer or a device) ***of a semiconductor device*** (e.g., 3D memory device 200) ***is determined relative to substrate 202 in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction***.

'378, 7:37-43. The specification likewise describes and shows the dielectric structure as above the isolation structure (and the isolation structure as above the substrate). For example, Figure 2 shows the dielectric structure above the isolation structure:

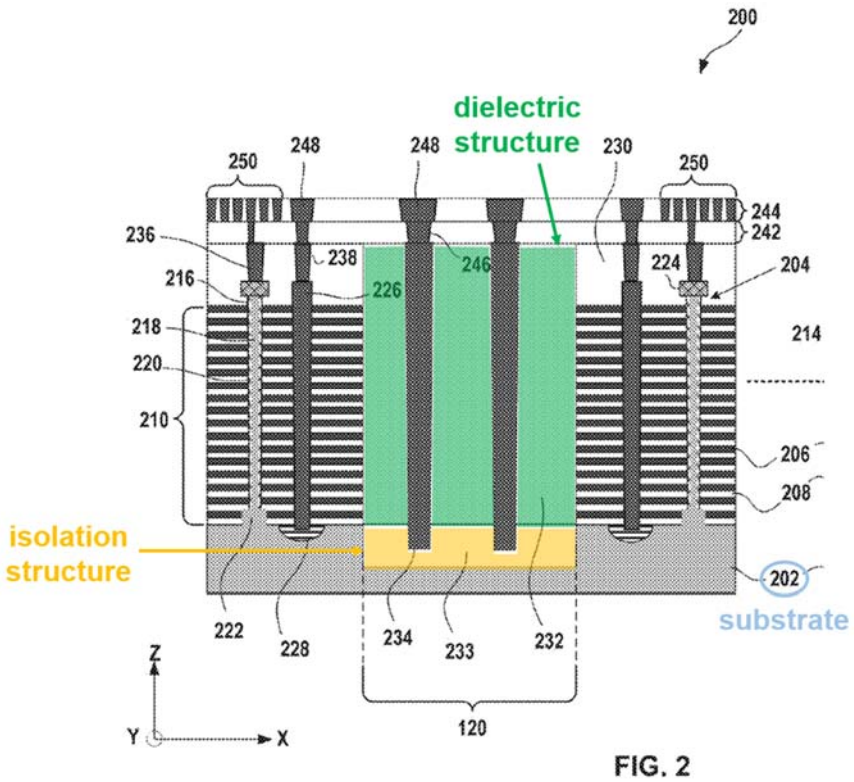



FIG. 2

'378, Fig. 2 (annotated and excerpted); *see also* '378, 10:37-38 ("…STI structure 233 is formed on a top portion of substrate 202…"), 12:66-67 ("STI structure 233 in

FIG. 4 can be formed on a top portion of substrate 202."), 20:40-42 ("…a dielectric structure, extending vertically through the alternating layer stack, on an isolation region of the substrate"), Figs. 4-13. Yang, ¶48.

Patent Owner's construction is also consistent with the vertically-oriented description of the '378's claimed "three-dimensional (3D) memory device." The "three-dimensional (3D) memory device" of the claim is described as "refer[ring] to a semiconductor device with vertically-oriented strings of memory cell transistors (referred to herein as "memory strings," such as NAND strings) ***on*** a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate." '378, 5:24-29. The patent explains that "the term 'vertical/vertically' means nominally perpendicular to the lateral surface of a substrate." *Id.*, 5:29-31; *see also* Ex. 2007 (Depo. Tr. of Dr. Lee (Petitioner's expert)), 64:5-12 ("'Vertically' means 90 degree with respect to the orientation of the substrate."). Therefore, in the context of the '378, a component being on another component requires the former to be vertically above the latter, where the vertical direction is the direction perpendicular to the substrate. Yang, ¶49.

In contrast, the '378 uses the terms "abut" and "on the side" to indicate a horizontal spatial relationship. For example, the alternating dielectric/conductor stack "abuts" a sidewall of the dielectric structure. '378, 20:42-45. While "on the side" includes the word "on" and refers to a horizontal spatial relationship, the term

"on" by itself is never used to indicate a lateral or other relationship besides above. Yang, ¶50.

Patent Owner respectfully disagrees with the Board's preliminary conclusion in its Decision to Institute ("DI") that the device may be reoriented for purposes of determining whether an alleged isolation structure is on the substrate. The Board cites disclosures from the '378 and preliminarily concludes that "a structure will be considered to be on the substrate even if it is not on the substrate in the displayed orientation so long as it is on the substrate in any possible rotation." DI, 12-13 (citing '378, 4:34-40). The cited passage states:

> The spatially relative terms are intended to encompass ***different orientations of the device in use or operation*** in addition to the orientation depicted in the figures. ***The apparatus may be otherwise oriented*** (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

'378, 4:34-40. Yang, ¶51.

This passage merely ensures that the orientation of ***the entire device*** ("***the apparatus***") may be rotated "***in use or operation***" while remaining within the scope of the claims—it does not change the claimed relative spatial relationships between the components within the device. This is also consistent with how the vertical direction is used within the '378 as the direction perpendicular to the substrate. For example, if the entire vertically-oriented memory device shown in Fig. 2 were

rotated 90 degrees, the dielectric structure is still above the isolation structure, and the isolation structure is still above the substrate, because the vertically-oriented direction has been rotated by 90 degrees along with the substrate. As this example illustrates, ***the device itself has not changed, and the same isolation structure is still "on" the substrate***. The word "on" is "interpreted accordingly" to account for the rotation and the vertically-oriented direction of the whole 3D memory cell device. Yang, ¶52.

The disclosure does not imply that any two components can have any relative spatial configuration and still be "on" each other, as the Board's interpretation would allow—that interpretation would be so broad as to render the term "on" superfluous. *See Wasica Fin. GmbH v. Cont'l Automotive Systems, Inc.*, 853 F.3d 1272, 1288 n.10 (Fed. Cir. 2017) ("It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous."). Indeed, Petitioner's expert, Dr. Lee, conceded that this interpretation is so broad that "any layers or any structure in the device perhaps can be considered on other layers or any structures of the devices." Ex. 2007, 45:10-47:5; *see generally* Ex. 2007, 33:1-47:5. Such an interpretation would also render the patentee's choice of terms such as "on" or "abut" meaningless. Yang, ¶53.

Furthermore, this interpretation would contradict the specification's consistent use of "on" to describe the spatial position of relevant structures in the

vertically-oriented direction of the 3D memory cell device, as discussed above. Spatial terms such as "on" are crucial in properly describing how a memory device is fabricated and how the various components are configured spatially. The specification describes the invention so that all the components are spatially placed and configured correctly to have a functional device. Yang, ¶54.

Petitioner's expert, Dr. Lee, has taken inconsistent positions when it comes to spatial terms. On the one hand, Dr. Lee purports to agree with the Board's conclusion that spatial terms like "on" can be ignored by random reoriented; on the other hand, he interprets several other spatial terms with definitive orientations. For example, Dr. Lee explains that a "side wall" of a dielectric structure is not just any surface of the dielectric structure, but must be one specific surface that is defined by its spatial geometry. *See* Ex. 2007, 62:13-63:7 ("[T]he side wall is between structure 210 and insulating layer 232 as the side wall, that is the side wall surface of the dielectric structure"). Similarly, Dr. Lee explains that "vertically" in the claims "means 90 degree[s] with respect to the orientation of the substrate." *Id*. 64:5-12. If Dr. Lee followed his own approach in defining these spatial terms, he would not have interpreted the term "on" to mean any reorientation. Yang, ¶55.

Thus, the term "on" should be construed as "above" in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction. The term does not permit reorienting the

direction of the "on" spatial relationship to encompass any relative position. Yang, ¶56.

### B. "a substrate with an isolation structure" (Claim 15)

The term "a substrate with an isolation structure" should be construed as requiring that ***the isolation structure is "part of" the substrate***. Yang, ¶57.

The '378 claims support the construction that the isolation structure is "part of" the substrate. Rather than listing the "isolation structure" as its own claim limitation, the "isolation structure" is introduced only in reference to the recited substrate. Specifically, claim 15 recites "a substrate with an isolation structure." Yang, ¶58.

The '378 specification also supports the construction that the isolation structure is "part of" the substrate. The '378 consistently depicts the isolation structure as a region in the upper portion of the substrate, for example as shown in Figure 2:

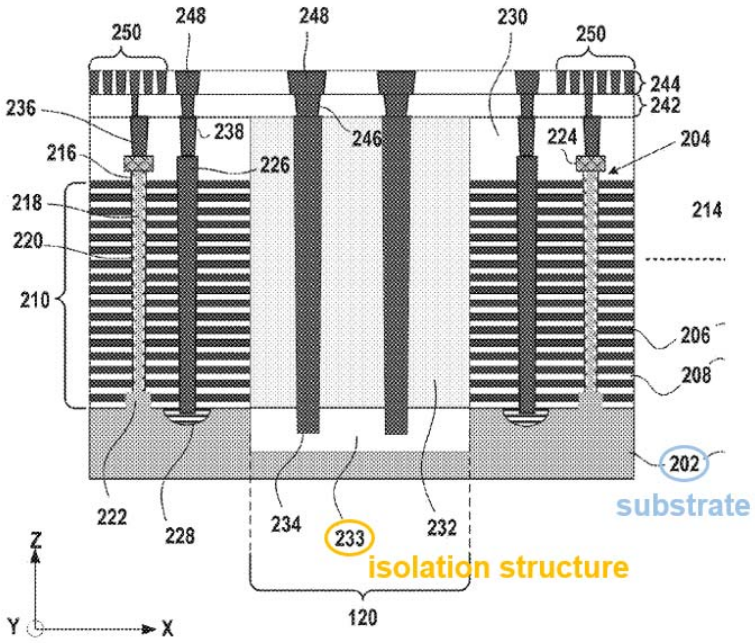



FIG. 2

’378, Fig. 2 (annotated and excerpted); *see also* ’378, Figs. 4-13. Specifically, the ’378 depicts a shallow region in the upper portion of the substrate (see Fig. 2, above). An example of the isolation structure in the ’378 is “shallow trench isolation (STI).” ’378, 10:30-43, 12:64-13:3, 14:46-15:32. Yang, ¶59.

The ’378 consistently describes the isolation structure as part of the substrate. *See* ’378, 12:54-66 (“According to some embodiments, ***substrate 202 includes isolation regions or structures***, like STI structure 233 shown in FIG. 4.”), 20:38-42 (“In some embodiments, a 3D memory device includes a semiconductor substrate, an alternating layer stack disposed on the semiconductor substrate, and a dielectric structure, extending vertically through the alternating layer stack, on ***an isolation region of the substrate***”), 21:7-13 (“In some embodiments a method for forming 3D

memory device includes forming ***an isolation structure on a substrate***, disposing an alternating dielectric layer stack on the substrate, where the alternating dielectric layer stack includes pairs of a first dielectric layer and a second dielectric layer different from the first dielectric layer."), 21:64 ("an isolation region in the substrate"), 22:27-28 ("In some embodiments, a 3D memory device includes ***a substrate with an isolation structure***"). Yang, ¶60.

The Board agreed in its Institution Decision that the isolation structure is part of the substrate (DI, 12-13), but took the preliminary position that an isolation structure could be located in any position relative to the substrate. The Board's statements are contrary to the '378 specification, which does not support an interpretation that "any "additional layers or structures added or disposed" on the substrate "could be considered part of, or 'with' the substrate," where "a layer is disposed on the substrate if it is on the substrate in any orientation, including by rotation of the device." DI, 12-13. Yang, ¶61.

***First***, the Board's preliminary interpretation that "part of" includes structures that are merely "on" the substrate is inconsistent with the claim language, which specifically invokes the term "with" (i.e., part of) rather than "on." Indeed, the Board's interpretation would lead to the absurd result that any components or layers positioned "on" the substrate would become "part of" the substrate such that the entire memory device would be subsumed by this unreasonably broad interpretation.

For example, the alternating conductor/dielectric layer stack is disposed "on" the substrate ('378, Abstract, 22:27-29), which under the Board's interpretation, would somehow become a ***part of*** the substrate. Yang, ¶62. Essentially, the Board's interpretation would render this claim term superfluous, which is "highly disfavored." *See Wasica*, 853 F.3d at 1288.

The Board quotes a passage from the specification stating that an "STI structure 233 is formed on a top portion of substrate 202 and filled with a dielectric material" (DI, 12 (citing '378, 10:30)), but in the context of this discussion, "on a top portion of the substrate" is referring to removing a part of the substrate, which is then "filled with a dielectric material," so as to form the "STI structure" "on a top portion of the substrate." '378, 10:30-44. Thus, this teaching of the specification supports the claim's recitation of "with" (i.e., part of) instead of "on," consistent with the other portions of the specification discussed above. Nothing in the specification suggests that the STI structure is merely "on" the substrate. Yang, ¶63.

***Second***, even if the "with" relationship encompassed the "on" relationship as preliminarily concluded by the Board (it does not), "on" means "above" in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction, and the '378 does not permit reorienting the direction of the "on" spatial relationship to encompass any relative position. *See* §V.B. Yang, ¶64.

Thus, the term "a substrate with an isolation structure" should be construed as requiring that the isolation structure is "part of" the substrate. The term does not encompass structures that are merely positioned "on" the substrate, and even if did, that would not permit reorienting the direction of the "on" spatial relationship to encompass any relative position. Yang, ¶65.

### C. "the dielectric and the isolation structures" (Claim 15)

The phrase "the dielectric and the isolation structures" in "through array contacts (TACs) extending vertically through the dielectric and the isolation structures" should be construed, consistent with its antecedent terms, as "the dielectric structure and the isolation structure." In other words, the term refers back to the same "dielectric structure" and the same "isolation structure" recited earlier in the claim. Yang, ¶66.

The phrase "the dielectric and the isolation structures" in [15.h] has its antecedent basis in "a dielectric structure" and "an isolation structure" from [15.a] and [15.c], confirming that the phrase is simply shorthand for "the dielectric structure" and "the isolation structure." There are no other terms in the claim, aside from "a dielectric structure" and "an isolation structure," that could provide the necessary antecedent basis for "the dielectric and the isolation structures." Yang, ¶67.

The claim language is plural ("structures") because it refers to both the isolation structure and the dielectric structure ("the dielectric and the isolation structures"), not because the term may be referring to multiple dielectric structures or multiple isolation structures. An example of the claimed configuration is shown in Fig. 2 of the '378.

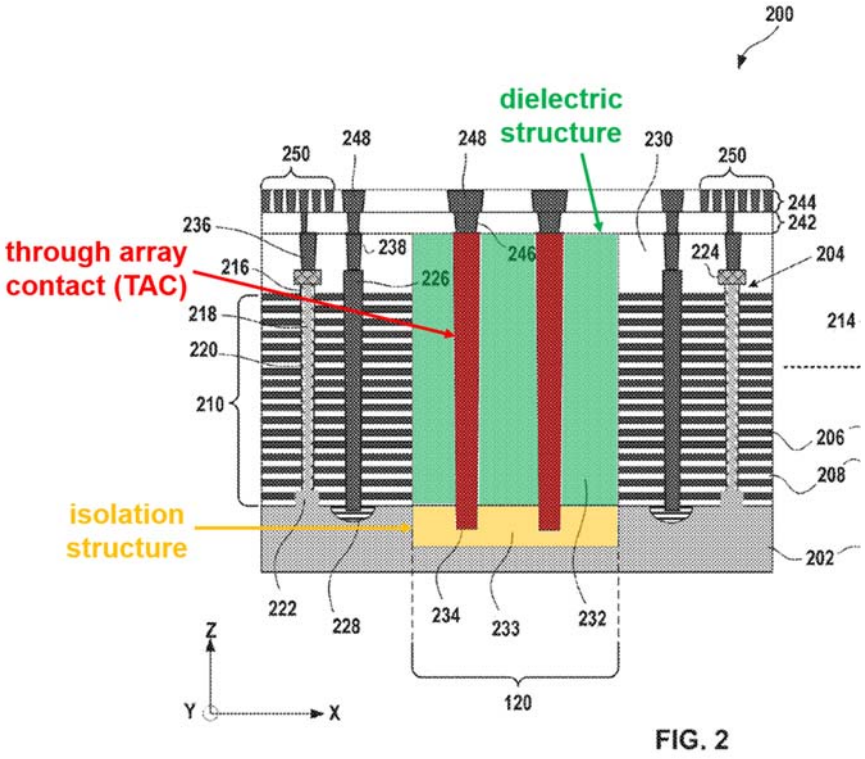



FIG. 2

'378, Fig. 2 (annotated and excerpted). As shown in the figure, a plurality of TACs extend through the same dielectric structure and the same isolation structure. Yang, ¶68.

While the claims do not preclude multiple dielectric structures or multiple isolation structures, the limitation "through array contacts (TACs) extending vertically through the dielectric and the isolation structures" requires that the

plurality of TACs extend through at least one particular dielectric structure and one particular isolation structure—i.e., the previously recited dielectric structure and isolation structure—regardless of whether additional dielectric structure or isolation structures are also present in the device. Yang, ¶69.

Patent Owner respectfully submits that the Board's preliminary analysis in its Institution Decision misinterprets the claim language. The DI states:

> Limitation [15.H] requires TACs (multiple) extending through "the dielectric and the isolation structures" (multiple). Being plural, the phrase "the dielectric and the isolation structures" is not limited to a single dielectric and a single isolation structure; it may include multiple dielectric structures and/or multiple isolation structures.

DI, 23. As discussed above, the claims and specification support construing this term as referring to the same specific dielectric structure and isolation structure previously recited in the claim, rather than multiple dielectric structures and/or multiple isolation structures. For example, the claims would not encompass each of the TACs extending through different dielectric structures instead of the same dielectric structure. Yang, ¶70.

The Board's reliance on "a single TAC extending through a single respective dielectric structure" (DI, 23 (citing '378, 21:17–25)) is misplaced. The cited passage states:

> The method also includes filling the opening with a dielectric layer to form a dielectric structure as a TAC region of the 3D memory device, removing portions of the dielectric structure and the isolation structure until the substrate is exposed to form a TAC opening that vertically extends through the dielectric structure and the isolation structure, and filling the TAC opening with a conductor to form a TAC structure in the TAC region, wherein the TAC structure is in contact with the substrate.

'378, 21:17–25. This passage describes the formation of a single TAC, not a plurality of TACs that extend through the dielectric structure and the isolation structure as claimed. The cited passage does not support an interpretation that each TAC in a group of TACs may extend through separate, discontinuous dielectric structures. As discussed above, the specification consistently describes and depicts the ***plurality of TACs*** as extending through the same dielectric structure. Regardless, even if the Board's interpretation of this passage were correct (respectfully, it is not), a claim need not be construed to encompass all disclosed embodiments. As explained, claim 15 is directed to a plurality of TACs that extend through a dielectric structure, for example as shown in Fig. 2 of the '378. Yang, ¶71.

Under the correct interpretation of "the dielectric and isolation structures" as "the dielectric structure and the isolation structure," limitation [15.h] requires that multiple TACs extend through a single dielectric structure. The Federal Circuit has made clear that even if the claims cover "one or more" of an element, there must still

be at least one instance of the element, e.g., in the accused system or the prior art, that meets all the requirements of the claim for that element. *See Finjan LLC v. SonicWall, Inc.*, 84 F.4th 963, 974-975 (Fed. Cir. 2023) ("Even if an infringing system can use 'one or more computers,' the plain language of the claims requires at least one of those computers to perform all the functions listed in the claims of the ARB Patent."). Here, the claim requires that a single "dielectric structure" must have multiple "through array contacts (TACs) extending vertically through" it. Yang, ¶72.

### D. "the dielectric structure comprises a through array contact region of the 3D memory device" (Claim 17)

The term "through array contact region" in the limitation "the dielectric structure comprises a through array contact region of the 3D memory device" should be construed as "a region that is within or defined by the dielectric structure and which includes the through array contacts extending through the dielectric structure." Thus, because the dielectric structure extends through the alternating conductor/dielectric layer stack (independent claim 15), and the through array contact region ("TAC region") is within or defined by the dielectric structure, the TAC region cannot include the alternating conductor/dielectric layer stack. This interpretation is supported by the claims and specification. Yang, ¶73.

Claim 17 recites that "the dielectric structure comprises a through array contact region," which indicates that the TAC region is nested within the dielectric

structure, or at most is coextensive with the dielectric structure. *See CIAS, Inc. v. All. Gaming Corp.*, 504 F.3d 1356, 1360 (Fed. Cir. 2007) ("In the patent claim context the term 'comprising' is well understood to mean 'including but not limited to.'"). If the TAC region extended beyond the dielectric structure, then the TAC region would comprise the dielectric structure instead of the other way around. Yang, ¶74.

In addition, Patent Owner's construction—which provides a limit to the scope of the claimed region—is the only one that gives meaning to the term "through array contact region" in the claims. Independent claim 15, from which claim 17 depends, already requires TACs to extend through the dielectric structure, and thus "through array contact region" must have some additional meaning, which Patent Owner's construction provides. Yang, ¶75.

The '378 discloses a few embodiments of a TAC region, and in all of them the TAC region is within or defined by the dielectric structure and includes the TACs and the dielectric structure through which they extend. '378, 6:11-16 ("In some embodiments, TAC region 120 is between two TSG staircase regions 130 in the WL direction of the 3D memory device. ***TAC region 120 can be defined by a single-material dielectric structure 124. Multiple TAC structures 126 can be formed within TAC region 120 in dielectric structure 124.***") (emphasis added), 10:21-24 ("In some embodiments, ***dielectric structure 232 defines the boundaries, the shape,***

***and the size of TAC region 120*** (e.g., shown in FIGS. 1A-1C).”), Figs. 1A-1C, 2; *see also* ’378, 5:60-7:4.

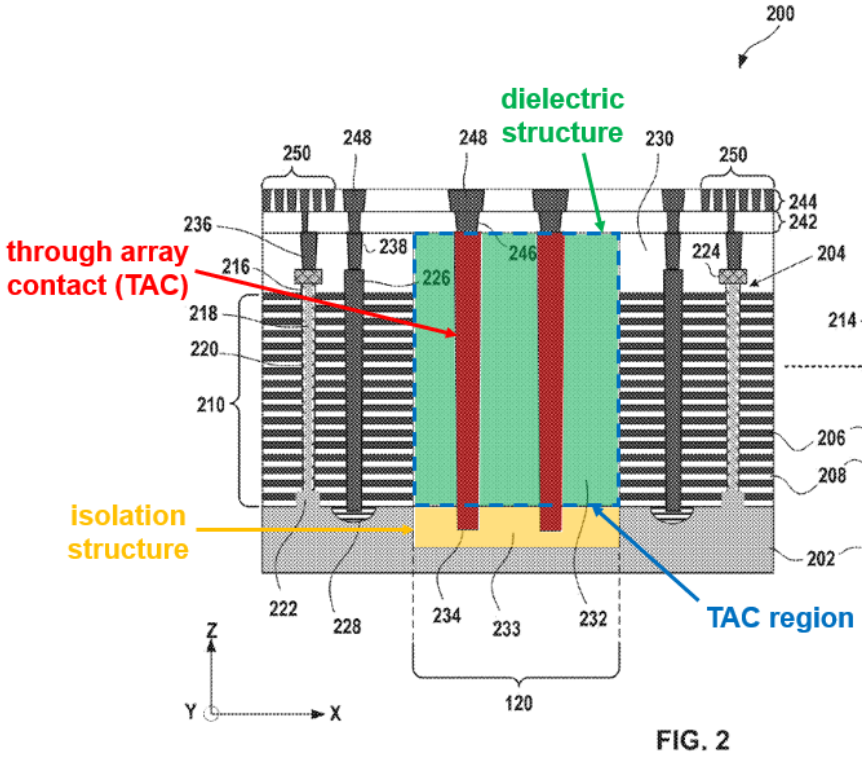



FIG. 2

’378, Fig. 2 (annotated and excerpted). In addition, in every embodiment of ’378, the dielectric structure includes only TACs extending through it and does not include, for example, the alternating conductor/dielectric layer stack. Yang, ¶76.

Thus, the term “through array contact region” in “the dielectric structure comprises a through array contact region of the 3D memory device” should be construed as “a region that is within or defined by the dielectric structure and which includes the through array contacts extending through the dielectric structure.” The TAC region does not include the alternating conductor/dielectric layer stack. Yang, ¶77.

## VI. BACKGROUND OF THE ASSERTED PRIOR ART[2]

### A. U.S. Patent Publication No. 2017/0179026 ("Toyama") (Ex. 1005)

Petitioner does not contend that Toyama anticipates the Challenged Claims, and instead argues only that it renders obvious the Challenged Claims in view of the knowledge of a POSITA. Pet. 6, 28-77. Yang, ¶78.

Toyama teaches a 3D NAND memory device with four exemplary structures and their modifications. Ex. 1005, [0004]. Only two of these exemplary structures are relied on by Petitioner: (1) "the 'first exemplary structure,' illustrated in Figures 1A-B to 17A-F," and (2) "the 'second modification of the fourth exemplary structure,' illustrated in Figures 44A-B to 49." Pet. 25. Yang, ¶79.

Toyama's first exemplary structure includes, among other elements: "**semiconductor substrate 9**" (Ex. 1005, [0163]); "**planar semiconductor material layer 10**" (Ex. 1005, [0170]); "**alternating stack (132, 146, 232, 246)**" (Ex. 1005, [0232]); "**channels**" (Ex. 1005, [0211]); "**laterally-elongated contact via structures 76**" (Ex. 1005, [0236]); "**drain contact via structures 88**" (Ex. 1005, [0241]); "**source connection via structures 91**" (Ex. 1005, [0250]); "**dielectric fill material portion 430**" (Ex. 1005, [0216]); and "**through-memory-level via**

[2] For the purposes of the present IPR proceeding only, Patent Owner does not contest that the Toyama, Mushiga, and Makala references qualify as prior art to the '378.

**structures 488**" (Ex. 1005, [0244]). A cross-section view of Toyama's first exemplary structure is below.

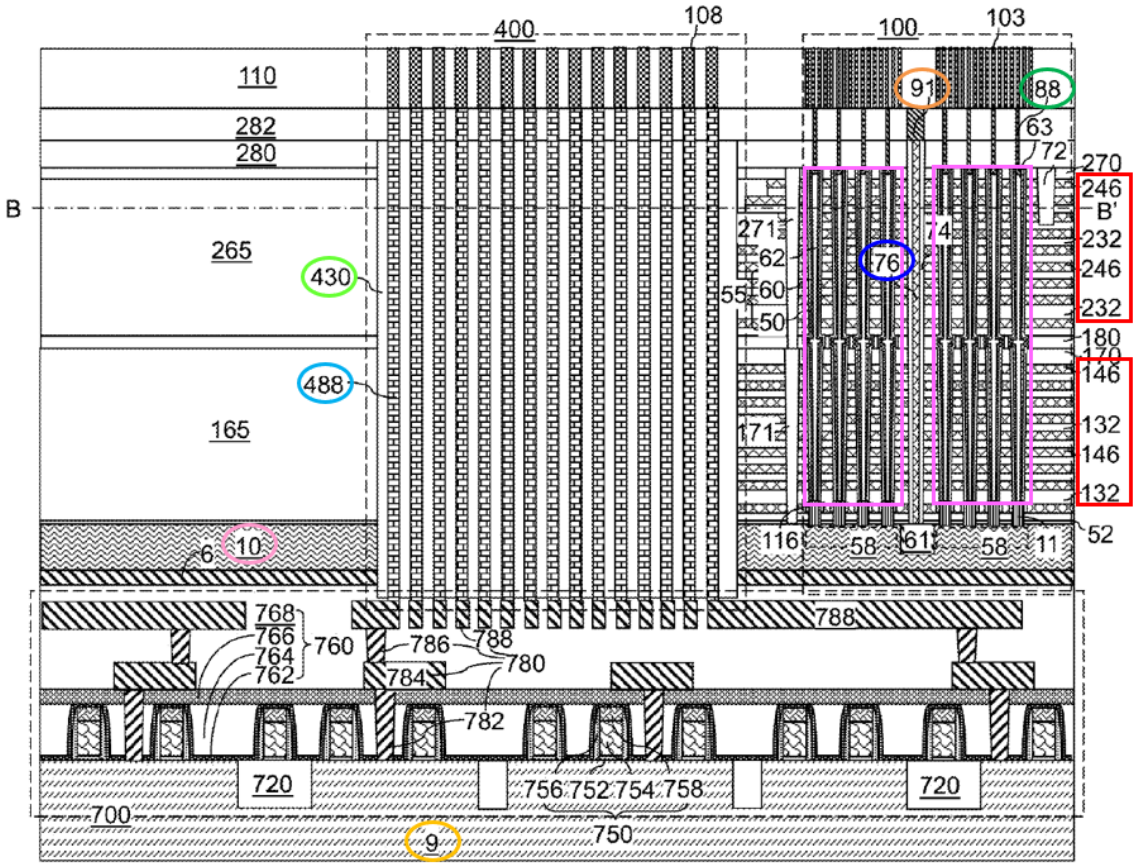



FIG. 17A

Ex. 1005, Fig. 17A (annotated). Yang, ¶80.

In Toyama's first exemplary structure, **dielectric fill material portion 430** forms a hole in **planar semiconductor material layer 10**, which allows **through-memory-level via structures 488** to form vertical interconnects. Toyama's **planar semiconductor material layer 10** lacks the claimed isolation structure. While Toyama's **semiconductor substrate 9** seems to comprise "shallow trench isolation

structures 720," they do not host **through-memory-level via structures 488** or similar via structures. Yang, ¶81.

Toyama's second modification of the fourth exemplary structure includes, among other elements: "**semiconductor substrate 9**" (Ex. 1005, [0163]); "**planar semiconductor material layer 10**" (Ex. 1005, [0170]); "**alternating stack (132, 146, 232, 246)**" (Ex. 1005, [0232]); "**channels**" (Ex. 1005, [0211]); "**laterally-elongated contact via structures 76**" (Ex. 1005, [0236]); "**drain contact via structures 88**" (Ex. 1005, [0241]); "**insulating liners 674**" (Ex. 1005, [0340]); and "**through-memory-level via structure 676**" (Ex. 1005, [0341]). A cross-section view of Toyama's second modification of the fourth exemplary structure is below.

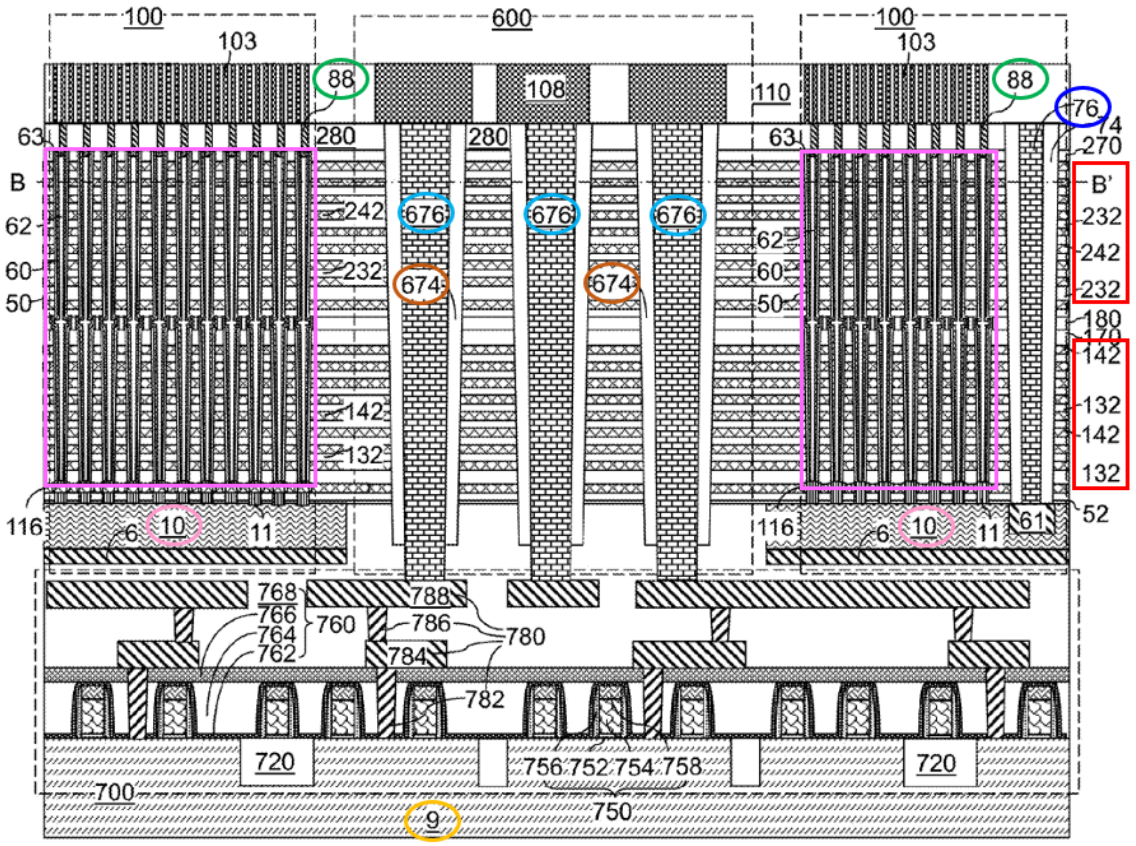



FIG. 49

Ex. 1005, Fig. 49 (annotated).[3] Yang, ¶82.

[3] Petitioner states: "In a clear typographical error, Figure 49 labels its alternating conductor/dielectric layer stack as elements 132, 142, 232, 242. Elements 142, 242 are 'sacrificial material layers' which, in a process step prior to Figure 49, were removed and replaced with 'electrically conductive layers (146, 246).' Toyama, [0337], [0340]." Pet. 39. Patent Owner does not challenge this assertion for purposes of the POR.

In Toyama's second modification of the fourth exemplary structure, Toyama's **planar semiconductor material layer 10** again lacks an isolation structure. In addition, **through-memory-level via structures 676** are not formed through a dielectric structure; instead, they are formed through **alternating stack (132, 146, 232, 246)** and as a result, they require separate **insulating liners 674** around each individual **through-memory-level via structure 676**. Yang, ¶83.

**B. U.S. Patent No. 10,354,980 ("Mushiga") (Ex. 1006)**

Petitioner does not contend that Mushiga anticipates the Challenged Claims, and instead argues only that it renders obvious the Challenged Claims in view of the knowledge of a POSITA, alone or in combination with Makala. Pet. 7, 77-105. Yang, ¶84.

Mushiga's 3D NAND memory device includes, among other elements: "**first substrate semiconductor layer 9**" (Ex. 1006, 7:34-44); "**semiconductor material layer 10**" (Ex. 1006, 9:8-14); "**alternating stack (132, 146, 232, 246)**" (Ex. 1006, 10:31-38); "**channels**" (Ex. 1006, 9:50-67); "**backside contact via structures 76**" (Ex. 1006, 10:1-18); "**drain contact via structures 88**" (Ex. 1006, 10:19-30); "**insulating spacers 586**" (Ex. 1006, 10:31-46); and "**through-memory-level via structure 588**" (Ex. 1006, 10:42-57). A cross-section view of Mushiga's device is below.

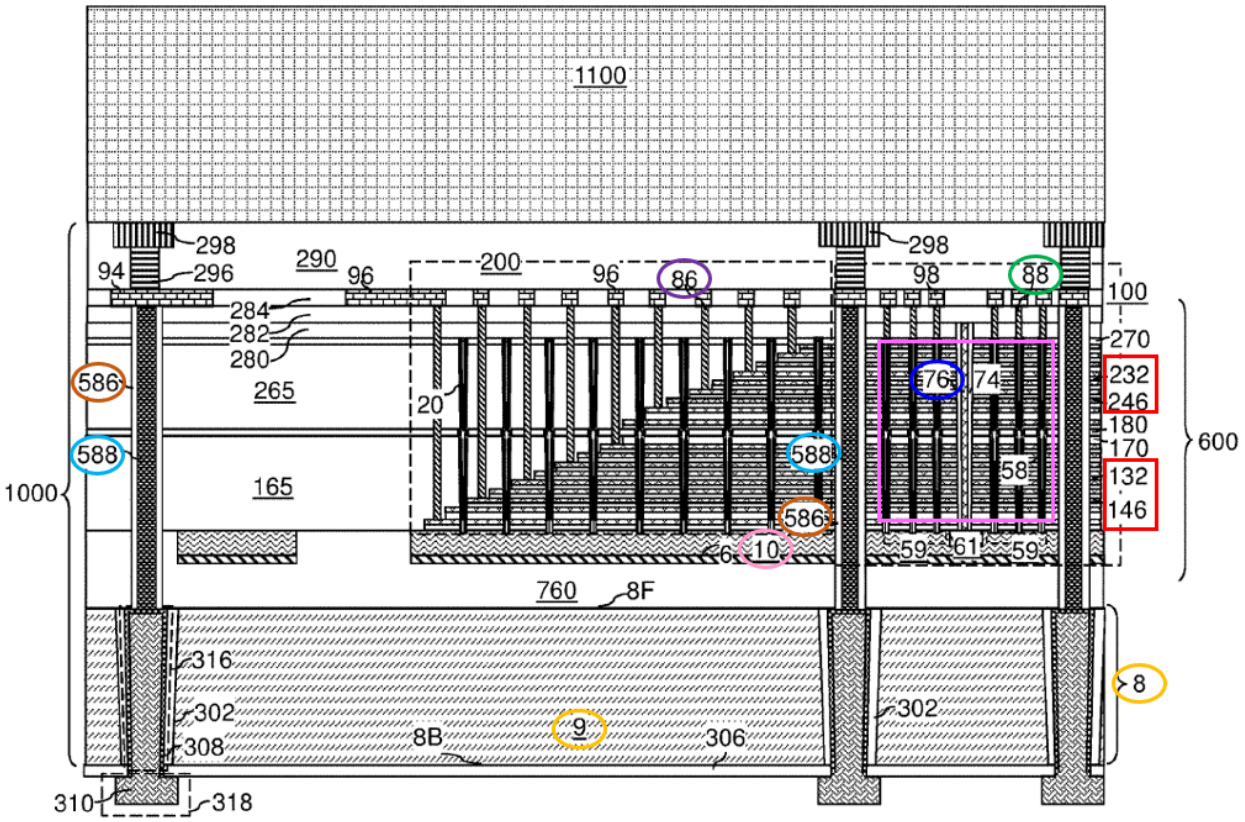



FIG. 11

Ex. 1006, Fig. 11 (annotated). Yang, ¶85.

Mushiga's **semiconductor material layer 10** and **substrate semiconductor layer 9** lack the claimed isolation structure. In addition, in Mushiga, some **through-memory-level via structures 588** are placed outside the array, such as the one on the left in Fig. 11 above. For the ones placed inside the array, there is no dielectric structure in a dedicated region for forming **through-memory-level via structures 588**; instead, they are formed through **alternating stack (132, 146, 232, 246)** and as a result, they require separate **insulating spacers 586** around each individual **through-memory-level via structure 588**. Yang, ¶86.

### C. U.S. Patent No. 10,262,945 ("Makala") (Ex. 1007)

Petitioner does not contend that Makala anticipates the Challenged Claims, and instead argues only that it renders obvious the Challenged Claims in view of the knowledge of a POSITA in combination with Mushiga. Pet. 7, 102-105. Yang, ¶87.

Makala's 3D NAND memory device includes, among other elements: "**substrate semiconductor layer 9**" (Ex. 1007, 4:53-61); "**planar semiconductor material layer 10**" (Ex. 1007, 17:10-40); "**alternating stack (132, 146, 232, 246)**" (Ex. 1007, 32:8-30); "**channels**" (Ex. 1007, 24:25-43); "**backside contact via structures 76**" (Ex. 1007, 33:4-29); "**drain contact via structures 88**" (Ex. 1007, 33:37-43); "**source connection via structures 91**" (Ex. 1007, 34:27-34); and "**through-memory-level via structure 488**" (Ex. 1007, 34:12-16). A cross-section view of Makala's device is below.

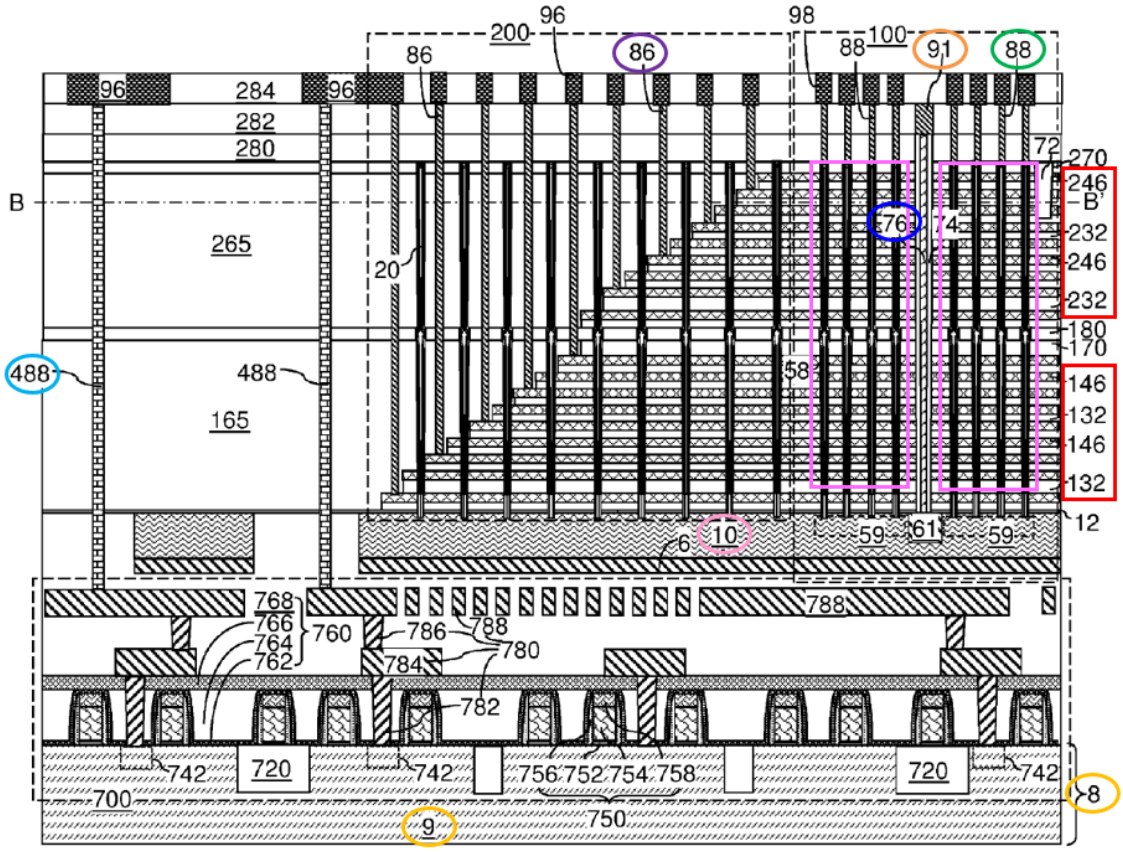



FIG. 16

Ex. 1007, Fig. 16 (annotated). Yang, ¶88.

Petitioner relies on Makala only for its disclosure of **source connection via structures 91**. The teachings of Makala are not relevant to any issues raised in this POR. Yang, ¶89.

## VII. GROUND 1A: TOYAMA'S FIRST EXEMPLARY STRUCTURE DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 15-17 AND 19-20

In Ground 1A, Petitioner relies on Toyama's First Exemplary Structure as allegedly rendering obvious all Challenged Claims (Pet. 28-77), but Petitioner fails to show that Toyama's First Exemplary Structure discloses or renders obvious three

separate limitations of claim 15, which is the sole challenged independent claim from which the other challenged claims depend: [15.a] ("***a substrate with an isolation structure***"); [15.c.i] ("***a dielectric structure on the isolation structure***"); and [15.h] ("***through array contacts (TACs) extending vertically through the dielectric and the isolation structures***"). In addition, Petitioner fails to show that Toyama's First Exemplary Structure discloses or renders obvious claim 17, which further requires "***the dielectric structure comprises a through array contact region of the 3D memory device***." Yang, ¶90.

### A. Independent Claim 15: Toyama's First Exemplary Structure Does Not Disclose or Render Obvious Limitations [15.a], [15.c.i], and [15.h]

#### 1. Petitioner Fails to Show That Toyama's First Exemplary Structure Discloses or Renders Obvious "a substrate with an isolation structure" (Limitation [15.a])

Toyama's First Exemplary Structure does not disclose or render obvious "***a substrate with an isolation structure***" as required by limitation [15.a] because the feature of Toyama that Petitioner maps to the "isolation structure" is, at most, located in the region of a cut through the alleged substrate, and is not "part of" the substrate as required under the proper construction of this term. Yang, ¶91.

As discussed in §V.B, '378 claim 15 requires "a substrate ***with*** an isolation structure," which means that the isolation structure is ***part of*** the substrate. This construction of the term does not encompass a structure that is merely next to or

abutting the substrate. And as further discussed in §V.B, even if the term "with" is construed as encompassing "on," the term "on" means "above" in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction, and the patent does not permit reorienting the direction of the "on" spatial relationship to encompass any relative position between components. Yang, ¶92.

Toyama's First Exemplary Structure includes "dielectric fill material portion 430," which Petitioner divides into two parts, one of which it then maps to the isolation structure of the '378. Pet. 33-35.

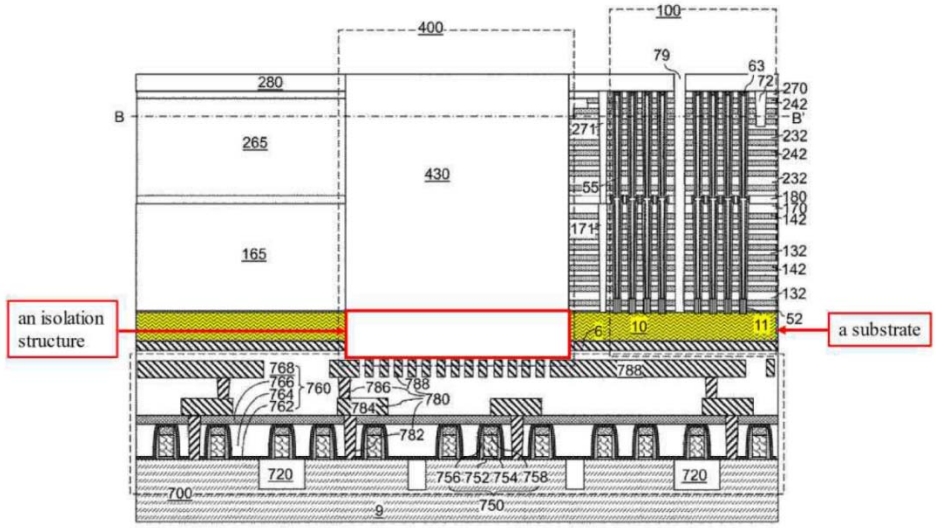



FIG. 13A

Ex. 1005, Fig. 13A (annotated by Petitioner at Pet. 35). Yang, ¶93.

Petitioner's alleged isolation structure (lower part of "dielectric fill material portion 430") is not part of the alleged substrate ("planar semiconductor material

layer 10").[4] Petitioner argues that the claimed relationship is satisfied because "Toyama's isolation structure … ***is formed by removing and is surrounded by*** [the] substrate" and "the isolation structure is within the substrate and isolates portions of the substrate from one another" (Pet. 35-36 (emphasis original) (citing Ex. 1003 ¶103)), but Petitioner's arguments are misplaced. Yang, ¶94.

As a preliminary matter, Petitioner's assertion that Toyama's First Exemplary Structure's alleged isolation structure "is surrounded by" its alleged substrate is unfounded. Toyama's relevant figures (Figs. 1A-B to 17A-F) do not depict that dielectric fill material portion "430" is surrounded by other regions. As can be seen below, 430 is shown to extend all the way to the left.

[4] For the purposes of this POR, Patent Owner does not dispute Petitioner's mapping of the claimed "substrate" to Toyama's "planar semiconductor material layer 10" in Ground 1A.

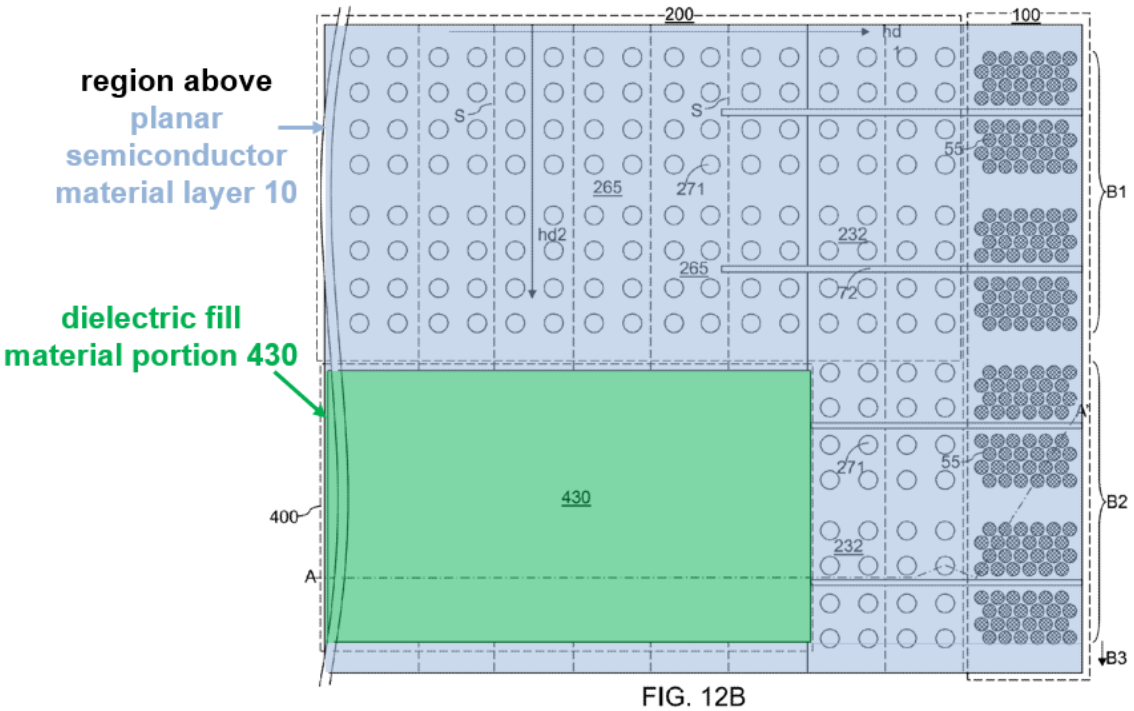
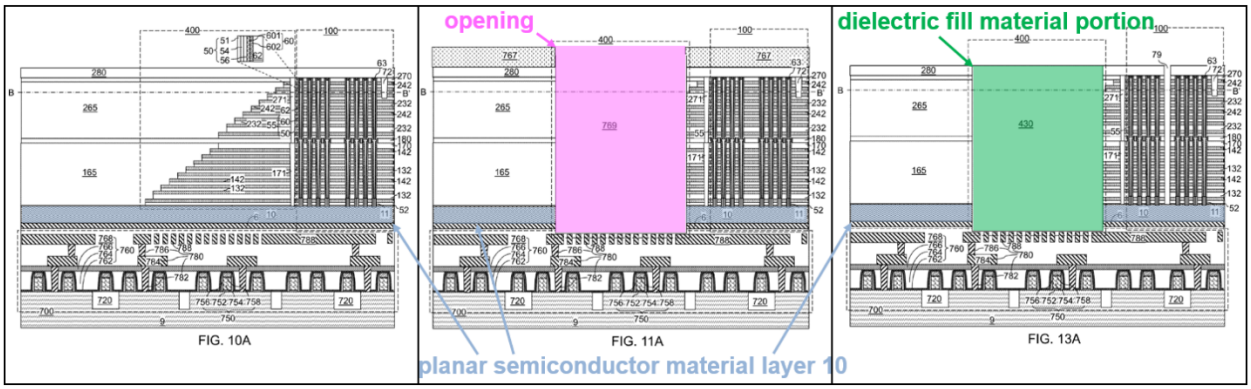



FIG. 12B

Ex. 1005, Fig. 12B (annotated). Even if the alleged isolation structure were surrounded by the alleged substrate, that would not make it a part of the substrate, just as two structures that are merely adjacent would not meet this requirement. Yang, ¶95.

The fact that the opening is formed by removing the alleged substrate (Pet. 35-36) does not support Petitioner's argument because after the substrate is removed there is no longer any portion of the alleged substrate in the relevant region. To further illustrate this, unlike the substrate of '378, which spans the horizontal area of the memory device and "onto which subsequent material layers are added, or otherwise 'disposed'" ('378, 4:41-43), Toyama's "planar semiconductor material layer 10" is completely removed in the relevant region, and is ***replaced*** by "opening

769." Ex. 1005, [0213]-[0215], Figs. 12A, 13A. After this step, there is simply no substrate in the region labeled "400." *Id.*, Fig. 14A. As illustrated below, by forming "opening 769," Toyama creates a region outside and merely abutting the alleged substrate ("planar semiconductor material layer 10"). It is in this newly opened space, where the alleged substrate has been entirely removed, that "dielectric fill material portion 430" is added. Thus, there is no alleged substrate "with" that dielectric fill material.




Ex. 1005, Figs. 10A, 11A, 13A (annotated). Moreover, these steps that Petitioner cites relate to the manufacturing process, not the final structure, and the Challenged Claims are apparatus claims. Yang, ¶96.

Finally, Petitioner's assertion that "the isolation structure […] isolates portions of the substrate from one another" is false. As seen in Toyama's Fig. 12B, the alleged substrate is not divided into isolated portions; *i.e.* it remains connected. Therefore, the alleged isolation structure does not actually isolate portions of the alleged substrate from one another.

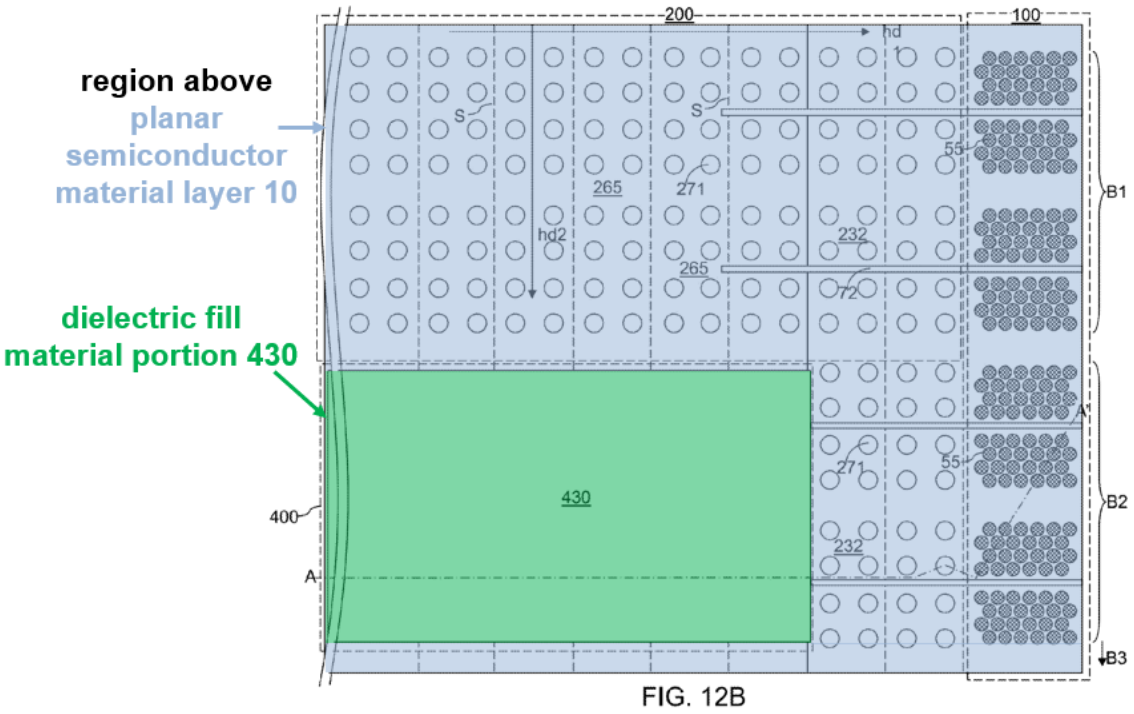



FIG. 12B

Ex. 1005, Fig. 12B (annotated). Yang, ¶97.

The Board in its Institution Decision preliminarily concluded that "on the current record for purposes of institution," the limitation "a substrate with an isolation structure" is taught by Toyama's First Exemplary Structure," but, respectfully, the conclusion was based on its incorrect construction that "an isolation structure may include a substrate having an abutting isolation structure, or an isolation structure 'formed on' the substrate, in which 'on' may be considered in any orientation of the device." DI, 15. As discussed in §V.B, this construction is incorrect—as properly construed, the limitation does not encompass an isolation structure that is merely "on" the substrate. Yang, ¶98.

Even if "a substrate with an isolation structure" encompassed an isolation structure that is merely "on" the substrate, Toyama's alleged isolation structure is not "on" the alleged substrate because it is not "above" the substrate in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction (*see* §V.A-B). The term "on" does not permit reorienting the direction of the "on" spatial relationship to encompass any relative position for the reasons discussed in §V.A-B, and so Toyama's alleged isolation structure is not "on" the alleged substrate. Specifically, dielectric fill material portion 430 (the alleged isolation structure) is not "on" the alleged substrate because there is simply no alleged substrate below the alleged isolation structure, as shown in Figure 13A. None of the dielectric fill material is above the alleged substrate. Yang, ¶99.

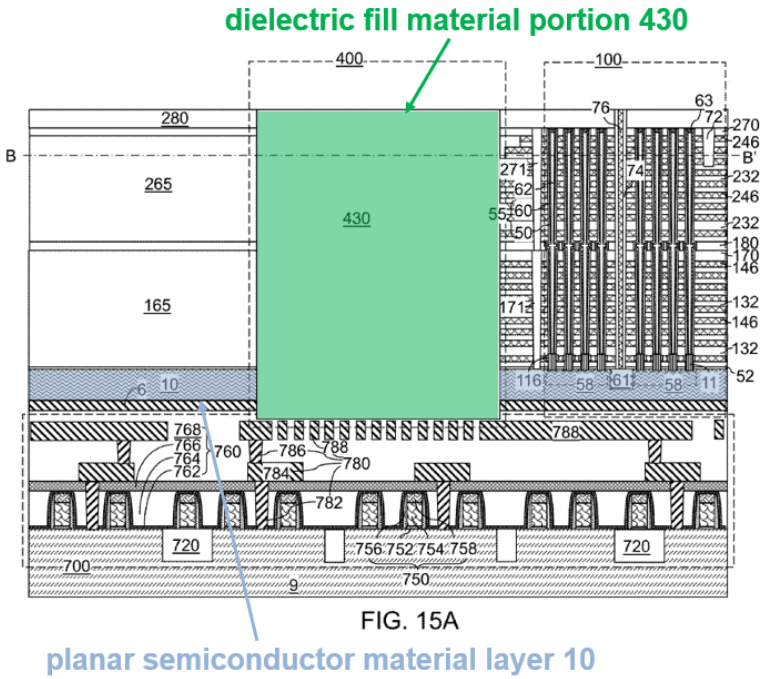



FIG. 15A

Ex. 1005, Fig. 13A (annotated).

For all of these reasons, Toyama's First Exemplary Structure does not disclose or render obvious "***a substrate with an isolation structure***" as required by limitation [15.a]. Yang, ¶100.

### 2. Petitioner Fails to Show That Toyama's First Exemplary Structure Discloses or Renders Obvious "a dielectric structure on the isolation structure" (Limitation [15.c.i])

Toyama's First Exemplary Structure does not disclose or render obvious "***a dielectric structure on the isolation structure***" as required by limitation [15.c.i] because Petitioner arbitrarily and improperly divides Toyama's single dielectric structure into two regions and maps different regions to two separate features of the

Challenged Claims: the "dielectric structure" and the "isolation structure." Yang, ¶101.

As an initial matter, for all the reasons explained in §VII.A.1, Toyama's First Exemplary Structure does not disclose or render obvious the claimed isolation structure, and as a result, it does not disclose or render obvious the claimed dielectric structure on the isolation structure. Yang, ¶102.

Further, Petitioner's only argument for this limitation is to improperly rely on the same substructure for two separate terms in the claim—the claimed dielectric structure and the claimed isolation structure. In the '378, the dielectric structure is a separate structure on the isolation structure. This is expressly recited in the claims, and is shown, for example, in Figure 2 of the '378 which illustrates the two separately claimed structures:

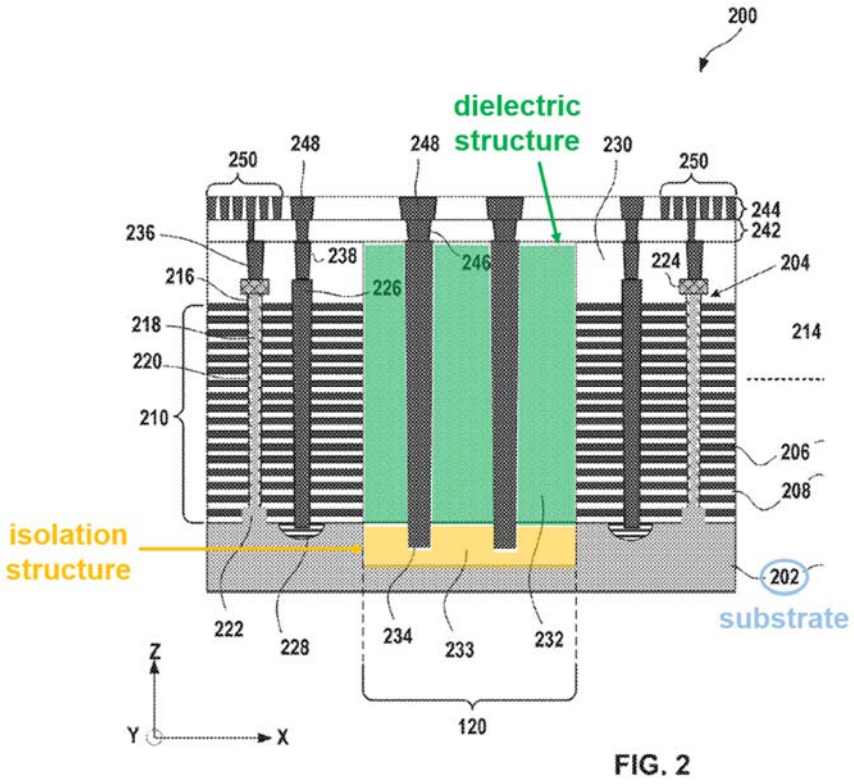
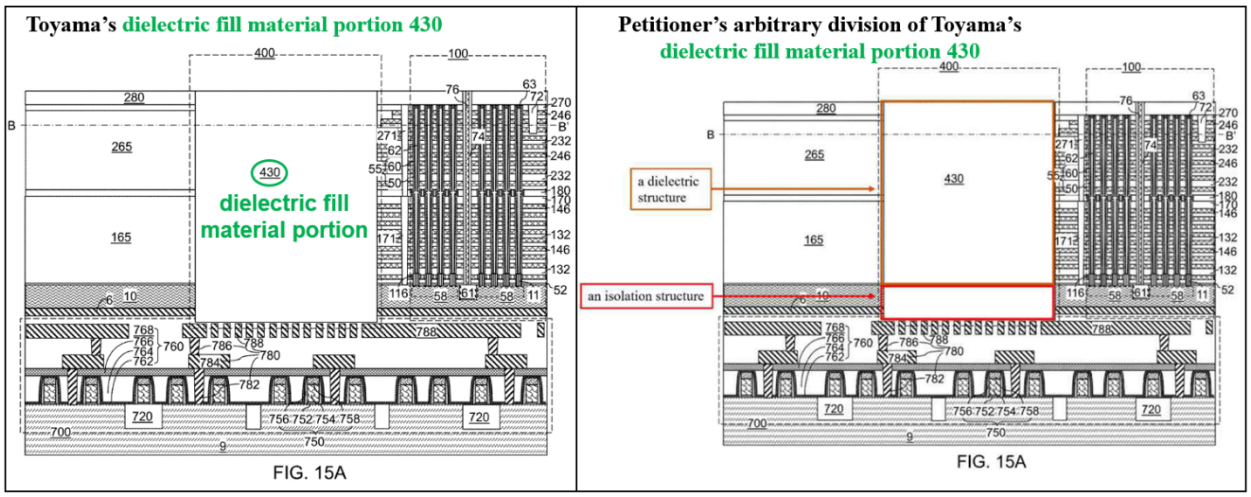



FIG. 2

’378, Fig. 2. Yang, ¶103.

In contrast, Toyama’s First Exemplary Structure includes only a single “dielectric fill material portion 430,” which, as illustrated below, Petitioner arbitrarily divides into two parts which it then maps to the separate dielectric structure and isolation structure of the ’378. Pet. 33-35, 45.




'378, Fig. 15A (left image annotated by Patent Owner; right image annotated by Petitioner at Pet. 45, with top heading added by Patent Owner). In Toyama, the "fill material portion 430" is a single integral structure. There are not two structures in Toyama and thus there is no dielectric structure that is "on" an isolation structure as required by the Challenged Claims. Yang, ¶104.

Petitioner asserts that the specification would not preclude the two structures from being formed during the same process step (Pet. 46), but the issue is not how the device is made, it is whether it has both a dielectric structure ***and*** an isolation structure with the claimed relationship—Toyama's First Exemplary Structure does not. The '378 consistently claims, describes, and depicts the isolation structure and the dielectric structure to be separate structures with a specific spatial relationship. '378, 10:30-43, Figs. 2-13. For example, the dielectric structure is "formed so that it is aligned to or covers at least a portion of" the isolation structure ('378, 10:30-33); the dielectric structure is "in contact with" the isolation structure

('378, 10:35-36); and the dielectric structure "can cover only portion of" the isolation structure ('378, 10:42-43). Thus, Patent Owner respectfully disagrees with the Board's preliminary conclusion in its Institution Decision that "[n]either the claim nor the specification of the '378 patent requires different […] separate depositions for the isolation structure and the dielectric structure thereon." DI, 20. As the above quotes exemplify, the '378 teaches forming the isolation structure in the substrate and then depositing the dielectric structure on the isolation structure, resulting in two distinct, identifiable structures. Yang, ¶105.

Petitioner argues that the function of the isolation structure is limited to electrically insulating the TACs (Pet. 46-47), but this argument ignores the claims, which are not directed to two functions of a single structure. Rather, the claims recite two structures with a claimed spatial relationship. Yang, ¶106.

The Board in its Institution Decision cites the '378 disclosures that $SiO_2$ can be used for both the isolation structure and dielectric structure (DI, 20), but even when the same material is used, the isolation structure and dielectric structure are described as two separate structures such that one structure is "in contact with" another. '378, 10:35-36. Even if the same material (e.g., $SiO_2$) were used for both the dielectric structure and the isolation structure, there are still two separately identifiable structures, in contrast to Toyama's single unitary structure. Yang, ¶107.

The fact that the ’378 allows for “other isolation structures” than “STI structure” (’378, 10:34-35; Pet. 46) is irrelevant and does not mean that a single “dielectric fill material portion” can be arbitrarily divided to purportedly create both the claimed “dielectric structure” and the claimed “isolation structure,” or the claimed spatial relationship that is absent from Toyama. Yang, ¶108.

Petitioner next cites *Retractable Techs., Inc. v. Becton, Dickinson & Co.*, 653 F.3d 1296, 1303 (Fed. Cir. 2011) to argue that “different parts of the same structure can meet distinct claim elements” (Pet. 47), but this case is inapposite. In *Retractable Techs.*, the Federal Circuit cited clear claim language conveying that “retainer member” can be part of “needle holder,” and a passage from the specification that suggested that they “could be formed as an integral structure in the first instance.” 653 F.3d at 1303. None of that evidence applies here, and Petitioner has cited none. Moreover, retainer member and needle holder of *Retractable Techs.* were “distinct” portions (*id.*), whereas there are no “distinct” portions of the dielectric fill material portion of Toyama absent Petitioner’s arbitrary and hindsight-based annotations. Yang, ¶109.

Because the isolation and dielectric structures must be two separate structures as recited in the claims, Toyama’s First Exemplary Structure does not disclose or render obvious “a dielectric structure on the isolation structure”—Petitioner’s

arbitrary division of a single structure into two parts does not teach two structures. Yang, ¶110.

Finally, Petitioner asserts that Toyama's First Exemplary Structure renders the claims obvious because a different embodiment teaches forming an isolation structure in "opening 151" before forming a dielectric structure (Pet. 47-48 (citing Ex. 1003, ¶ 121)), but the structure formed in Toyama's "opening 151" is not the claimed isolation structure which must be part of the substrate for the same reasons explained in §VII.A.1, *supra* (First Exemplary Structure), and §VIII.A.1, *infra* (Second Modification). In addition, Petitioner has not identified a motivation for making the proposed changes to the First Exemplary Structure, which are motivated purely by hindsight. Moreover, the proposed modification changes First Exemplary Structure's processing steps, which Petitioner leaves unaddressed. Pet. 47-48. Yang, ¶111.

Thus, Toyama's First Exemplary Structure does not disclose or render obvious "a dielectric structure on the isolation structure" as required by limitation [15.c.i]. Yang, ¶112.

#### 3. Petitioner Fails to Show That Toyama's First Exemplary Structure Discloses or Renders Obvious "TACs extending vertically through the dielectric and the isolation structures" (Limitation [15.h])

Toyama's First Exemplary Structure does not disclose or render obvious "***through array contacts (TACs) extending vertically through the dielectric and the***

***isolation structures***" as required by limitation [15.h] because, for all the reasons explained in §§VI.A.1-2, Toyama's First Exemplary Structure does not disclose or render obvious the claimed isolation structure or the claimed dielectric structure on the isolation structure. Yang, ¶113.

### B. Claim 17: Petitioner Fails to Show That Toyama's First Exemplary Structure Discloses or Renders Obvious "the dielectric structure comprises a through array contact region of the 3D memory device"

Toyama's First Exemplary Structure does not disclose or render obvious "***the dielectric structure comprises a through array contact region of the 3D memory device***" as required by claim 17. Yang, ¶114.

As discussed in §V.D, the limitation "the dielectric structure comprises a through array contact region of the 3D memory device" means "a region that is within or defined by the dielectric structure and which includes the through array contacts extending through the dielectric structure." For all the reasons explained in §VI.A.2, Toyama's First Exemplary Structure does not disclose or render obvious the claimed dielectric structure, and as a result, does not disclose or render obvious a through array contact region that is within or defined by the dielectric structure. Yang, ¶115.

# VIII. GROUND 1B: TOYAMA'S SECOND MODIFICATION DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 15-17 AND 19-20

In Ground 1B, Petitioner relies on Toyama's Second Modification (of the fourth exemplary structure) as allegedly rendering obvious all Challenged Claims (Pet. 28-77), but Petitioner fails to show that Toyama's Second Modification discloses or renders obvious three separate limitations of claim 15, which is the sole challenged independent claim from which the other challenged claims depend: [15.a] ("***a substrate with an isolation structure***"); [15.c.i] ("***a dielectric structure on the isolation structure***"); and [15.h] ("***through array contacts (TACs) extending vertically through the dielectric and the isolation structures***"). In addition, Petitioner fails to show that Toyama's Second Modification discloses or renders obvious claim 17, which further requires "***the dielectric structure comprises a through array contact region of the 3D memory device***." Yang, ¶116.

## A. Independent Claim 15: Toyama's Second Modification Does Not Disclose or Render Obvious Limitations [15.a], [15.c.i], and [15.h]

### 1. Petitioner Fails to Show That Toyama's Second Modification Discloses or Renders Obvious "a substrate with an isolation structure" (Limitation [15.a])

Toyama's Second Modification does not disclose or render obvious "***a substrate with an isolation structure***" as required by limitation [15.a] because—just like with Toyama's First Exemplary Structure—the feature of Toyama that Petitioner maps to the "isolation structure" is, at most, located in the region of a cut

through the alleged substrate, and is not "part of" the substrate as required by the Challenged Claims under the proper construction of this term (*see* §V.B). Yang, ¶117.

As discussed in §V.B,'378 claim 15 requires "a substrate ***with*** an isolation structure," which means that the isolation structure is ***part of*** the substrate. This construction of the term does not encompass a structure that is merely next to or abutting the substrate. And as further discussed in §V.B, even if the term "with" is construed as encompassing "on," the term "on" means "above" in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction, and the patent does not permit reorienting the direction of the "on" spatial relationship to encompass any relative position between components. Yang, ¶118.

Toyama's Second Modification includes "opening 151" that "may be filled with another insulating material layer […] 760," which Petitioner erroneously maps to the isolation structure of the '378. Pet. 30-31. For the same reasons discussed in §VI.A.1, Petitioner's alleged isolation structure ("opening 151" filled with "insulating material layer 760") in Toyama's Second Modification's is not part of

the alleged substrate ("planar semiconductor material layer 10").[5] Specifically, contrary to Petitioner's misplaced arguments about how the device is made, as illustrated below, the alleged substrate is completely removed in the relevant region, thereby creating a region outside and merely abutting the alleged substrate, and the "insulating material layer 760" is added in that through-opening.

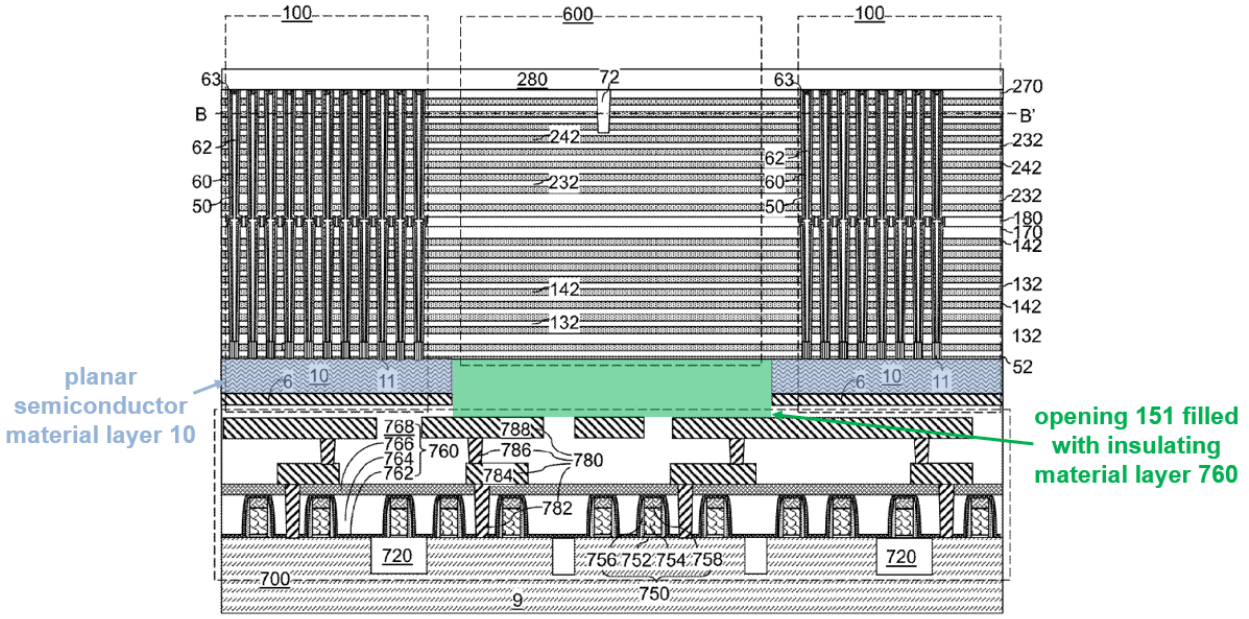



FIG. 44A

Ex. 1005, Fig. 44A (annotated). Thus, there is no alleged substrate "with" that "insulating material layer 760." In the context of Toyama's Second Modification, Petitioner never addresses the relationship between two claim limitations, *i.e.*, that

[5] For the purposes of this POR, Patent Owner does not dispute Petitioner's mapping of the claimed "substrate" to Toyama's "planar semiconductor material layer 10" in Ground 1B.

"a substrate" must be "***with***" "an isolation structure" and simply asserts that it is shown. Pet. 31. Yang, ¶119.

Petitioner's additional arguments relevant to this limitation made in the context of Toyama's First Exemplary Structure (Pet. 35-36) fail for the same reasons discussed in §VII.A.1 above. Yang, ¶120.

Therefore, Petitioner has failed to show that Toyama's Second Modification discloses or renders obvious "***a substrate with an isolation structure***" as required by limitation [15.a]. Yang, ¶121.

#### 2. Petitioner Fails to Show That Toyama's Second Modification Discloses or Renders Obvious "a dielectric structure on the isolation structure" (Limitation [15.c.i])

Toyama's Second Modification does not disclose or render obvious "***a dielectric structure on the isolation structure***" as required by limitation [15.c.i]. For all the reasons explained in § VIII.A.1, Toyama's Second Modification does not disclose or render obvious the claimed isolation structure. As a result, Toyama's Second Modification does not disclose or render obvious the claimed dielectric structure on the isolation structure. Yang, ¶122.

### 3. Petitioner Fails to Show That Toyama's Second Modification Discloses or Renders Obvious "TACs extending vertically through the dielectric and the isolation structures" (Limitation [15.h])

Toyama's Second Modification does not disclose or render obvious "***through array contacts (TACs) extending vertically through the dielectric and the isolation structures***" as required by limitation [15.h] because Toyama's alleged TACs do not extend through the same structure (the claimed "dielectric structure"). Yang, ¶123.

As an initial matter, for all the reasons explained in §§VIII.A.1-2, Toyama's Second Modification does not disclose or render obvious the claimed isolation structure or the claimed dielectric structure on the isolation structure. As a result, Toyama's Second Modification does not disclose or render obvious "through array contacts (TACs) extending vertically through the dielectric and the isolation structures." Yang, ¶124.

In addition, Toyama's TACs do not extend through the same "dielectric structure." As discussed in §V.C, the phrase "through array contacts (TACs) extending vertically through the dielectric and the isolation structures" means "through array contacts (TACs) extending vertically through the dielectric structure and the isolation structure"—i.e., through the same "a dielectric structure" recited earlier in the claim. The alleged TACs of Toyama's Second Modification fail to meet this requirement. Yang, ¶125.

Petitioner maps "insulating liners 674" of "through-memory-level via structures 676" to the "dielectric structure" of the '378 (Pet. 39-42), but this mapping relies on a separate insulating liner (i.e., a separate alleged dielectric structure) for each TAC. In other words, in Toyama's Second Modification, only a single "through-memory-level via structure 676" extends through a given "insulating liner 674." Realizing this problem, Petitioner attempts to map multiple insulating liners 674 to a single "dielectric structure." Pet. 41 (alleging that "the 'insulating liners 674' are collectively a *structure*").

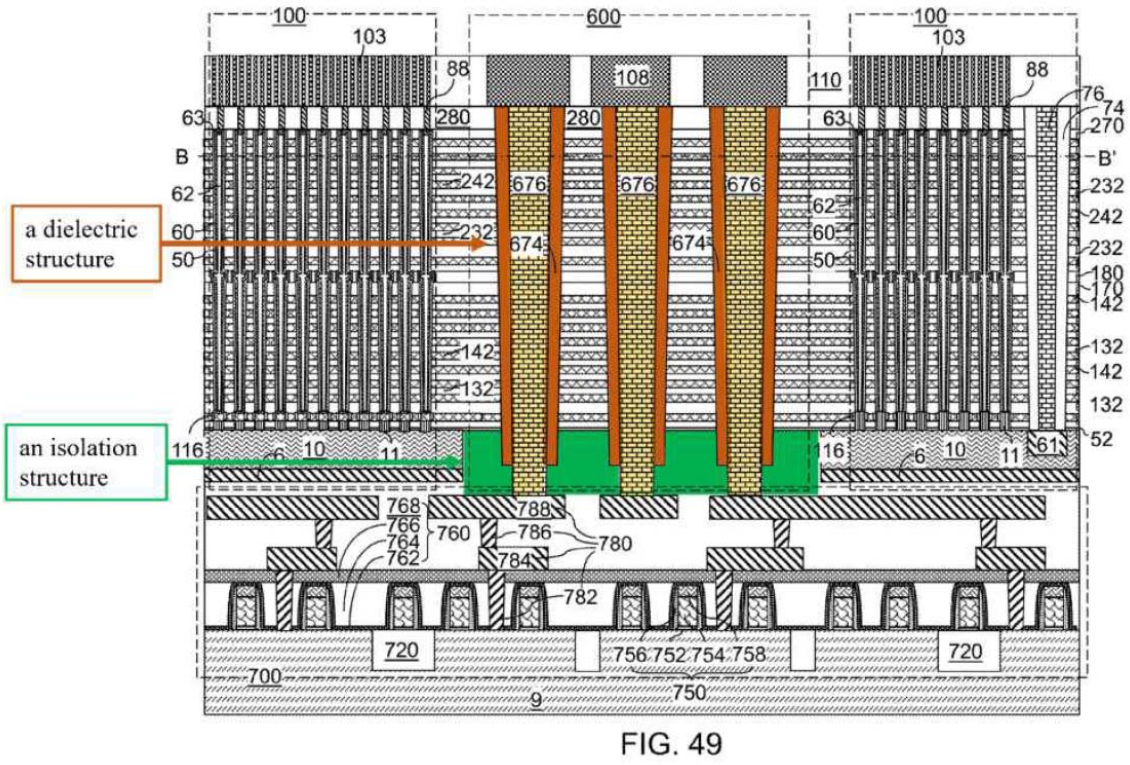



FIG. 49

Ex. 1005, Fig. 49 (annotated by Petitioner at Pet. 40). Yang, ¶126.

Petitioner's attempt to rely on separate dielectric structures as a single claimed "dielectric structure" is improper. The Federal Circuit has made clear that multiple

occurrences of a claim element cannot be used satisfy a limitation that must be satisfied by a single occurrence of the element—here, the claimed "dielectric structure." *See Finjan*, 84 F.4th at 974-975. In its subsequent decision for IPR2024-00791 (an IPR of the '806 patent, which is a continuation of the '378 patent) (Ex. 2006), the Board correctly "disagree[d] [with Petitioner's assertion] that merely because the three insulating liners are each constructed, that three constructed liners together constitute a single dielectric structure." Ex. 2006, 17. As a result, the Board found that Toyama's Second Modification does not show "a plurality of through array contacts (TACs) extending vertically through the dielectric structure" because "Petitioner has not sufficiently shown that Toyama's three insulating liners are a single dielectric structure." Ex. 2006, 17. The '378 limitation at issue here, just like the '806 limitation, requires that multiple TACs extend through a single dielectric structure, and so the Board's correct reasoning in IPR2024-00791 is equally applicable here. Yang, ¶127.

Petitioner misinterprets the Federal Circuit decision *KCJ Corp. v. Kinetic Concepts, Inc.* in which the Court found that "an indefinite article 'a' or 'an' in patent parlance carries the meaning of 'one or more' in open-ended claims containing the transitional phrase 'comprising.'" 223 F.3d 1351, 1356 (Fed. Cir. 2000). This principle merely means that in a memory structure that reads on the claims there could be more than one dielectric structure in the memory structure, and does ***not***

mean that more than one dielectric structure can be combined together for any claimed requirements imposed on the claimed "dielectric structure" (singular). Indeed, as discussed, the Federal Circuit has made clear that multiple occurrences of a claim element cannot be used satisfy a limitation that must be satisfied by a single occurrence of the element. *Finjan*, 84 F.4th at 974-975. Here, the claim, when correctly interpreted (*see* §V.C), requires that a single "dielectric structure" must have multiple "through array contacts (TACs) extend[] vertically through" it, which Toyama's "insulating liner 674" fails to show. Yang, ¶128.

Finally, in its attempt to map multiple separate liners to a single structure, Petitioner cites a dictionary to assert that because "these components together are something 'that is constructed,' they are a structure" (Pet. 31-32), but this argument conflicts with the above-discussed Federal Circuit precedent, and does not comport with the claims and specification of the '378. Yang, ¶129.

Therefore, Petitioner has failed to show that Toyama's Second Modification discloses or renders obvious "through array contacts (TACs) extending vertically through the dielectric and the isolation structures" as required by limitation [15.h]. Yang, ¶130.

### B. Claim 17: Petitioner Fails to Show That Toyama's Second Modification Discloses or Renders Obvious "the dielectric structure comprises a through array contact region of the 3D memory device"

Toyama's Second Modification does not disclose or render obvious "***the dielectric structure comprises a through array contact region of the 3D memory device***" as required by claim 17 because the alleged TAC region of Toyama's Second Modification is not within or defined by the alleged dielectric structure as required by claim 17. Yang, ¶131.

As discussed in §V.D, the limitation "the dielectric structure comprises a through array contact region of the 3D memory device" means "a region that is within or defined by the dielectric structure and which includes the through array contacts extending through the dielectric structure." As further discussed in §V.D, the TAC region does not include the alternating conductor/dielectric layer stack. Yang, ¶132.

Petitioner's alleged TAC region in Toyama's Second Modification is not within or defined by the alleged dielectric structure as required by claim 17. Instead, Petitioner's **alleged TAC region** is an arbitrarily defined region that includes **multiple alleged dielectric structures**, **TACs**, and large portions of **alternating conductor/dielectric layers**. Petitioner's mapping of the TAC region (cf. Pet. 73) is reproduced below with further annotations:

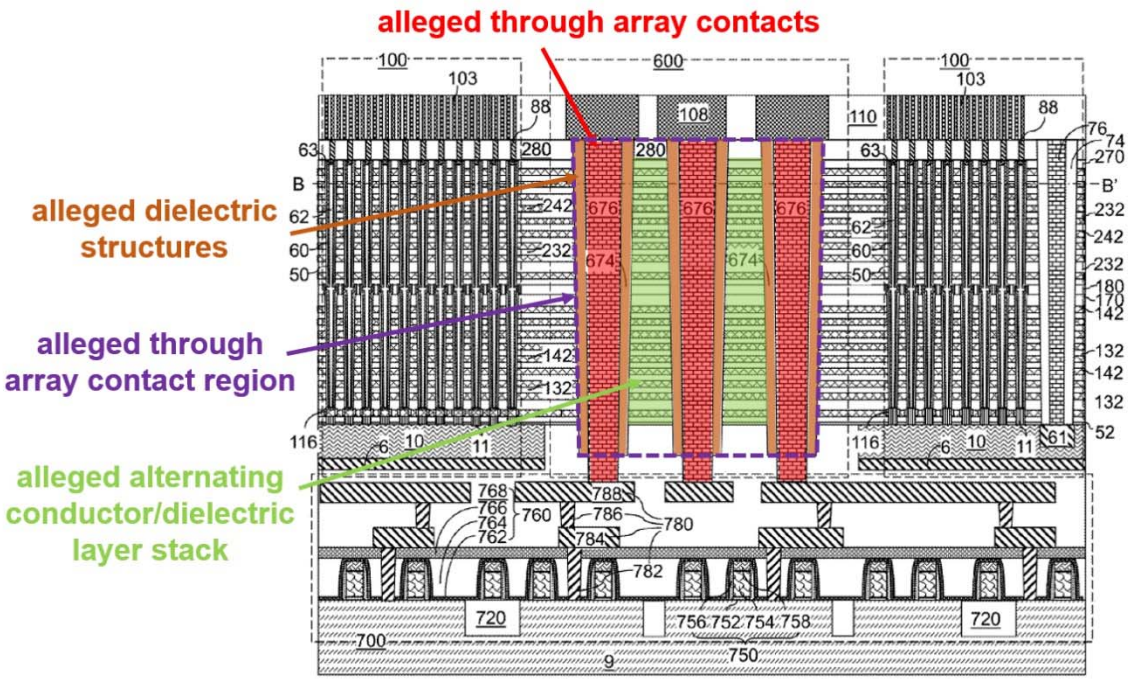



FIG. 49

Ex. 1005, Fig. 49 (annotated). Yang, ¶133.

First, Petitioner's mapping fails to meet the claim because, as shown, the alleged TAC region extends beyond the alleged structure, and thus is not within or defined by the alleged dielectric structure (*see* §V.D). In other words, because the alleged TAC region extends beyond the alleged structure, the alleged dielectric structure does not "comprise" the TAC region as required by the claim—rather, Petitioner points to an alleged TAC region that comprises a dielectric structure. Second, Petitioner's alleged TAC region includes the alternating conductor/dielectric layers, which the claim does not permit. As discussed in §V.D, because the dielectric structure extends through the alternating conductor/dielectric layer stack (independent claim 15) and the through array contact region ("TAC

region") is within or defined by the dielectric structure, the TAC region does not include the alternating conductor/dielectric layer stack. Petitioner's mapping does not address these issues. Pet. 72-74. Yang, ¶134.

Therefore, Petitioner has failed to show that Toyama's Second Modification discloses or renders obvious "the dielectric structure comprises a through array contact region of the 3D memory device" as required by claim 17. Yang, ¶135.

## IX. GROUND 2: MUSHIGA DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 15-17 AND 19-20

Petitioner fails to show that Mushiga discloses or renders obvious multiple independent limitations of the Challenged Claims. In Ground 2, Petitioner relies on Mushiga as allegedly rendering obvious all Challenged Claims (Pet. 77-102), but Petitioner fails to show that Mushiga discloses or renders obvious three separate limitations of claim 15, which is the sole challenged independent claim from which the other challenged claims depend: [15.a] ("***a substrate with an isolation structure***"); [15.c] ("***a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material***"); and [15.h] ("***through array contacts (TACs) extending vertically through the dielectric and the isolation structures***"). In addition, Petitioner fails to show that Mushiga discloses or renders obvious claim 17, which requires "***the dielectric***

***structure comprises a through array contact region of the 3D memory device***."

Yang, ¶136.

### A. Independent Claim 15: Mushiga Does Not Disclose Or Render Obvious Limitations [15.a], [15.c], and [15.h]

#### 1. Petitioner Fails to Show That Mushiga Discloses or Renders Obvious "a substrate with an isolation structure" (Limitation [15.a])

Mushiga does not disclose or render obvious "***a substrate with an isolation structure***" as required by limitation [15.a] because—just as with Toyama's structures—the feature of Mushiga that Petitioner maps to the "isolation structure" is, at most, located in the region of a cut through the alleged substrate, and is not "part of" the substrate as required by the Challenged Claims under the proper construction. Yang, ¶137.

As discussed in §V.B, '378 claim 15 requires "a substrate" to be "***with*** an isolation structure," which means that the isolation structure is ***part of*** the substrate. This construction of the term does not encompass a structure that is merely next to or abutting the substrate. And as further discussed in §V.B, even if the term "with" is construed as encompassing "on," the term "on" means "above" in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction, and the patent does not permit reorienting the direction of the "on" spatial relationship to encompass any relative position between components. Yang, ¶138.

Mushiga includes "**backside insulating layer 306**," which Petitioner combines with "**insulating material liners 302**" and erroneously maps to the isolation structure of the '378. Pet. 79-80.

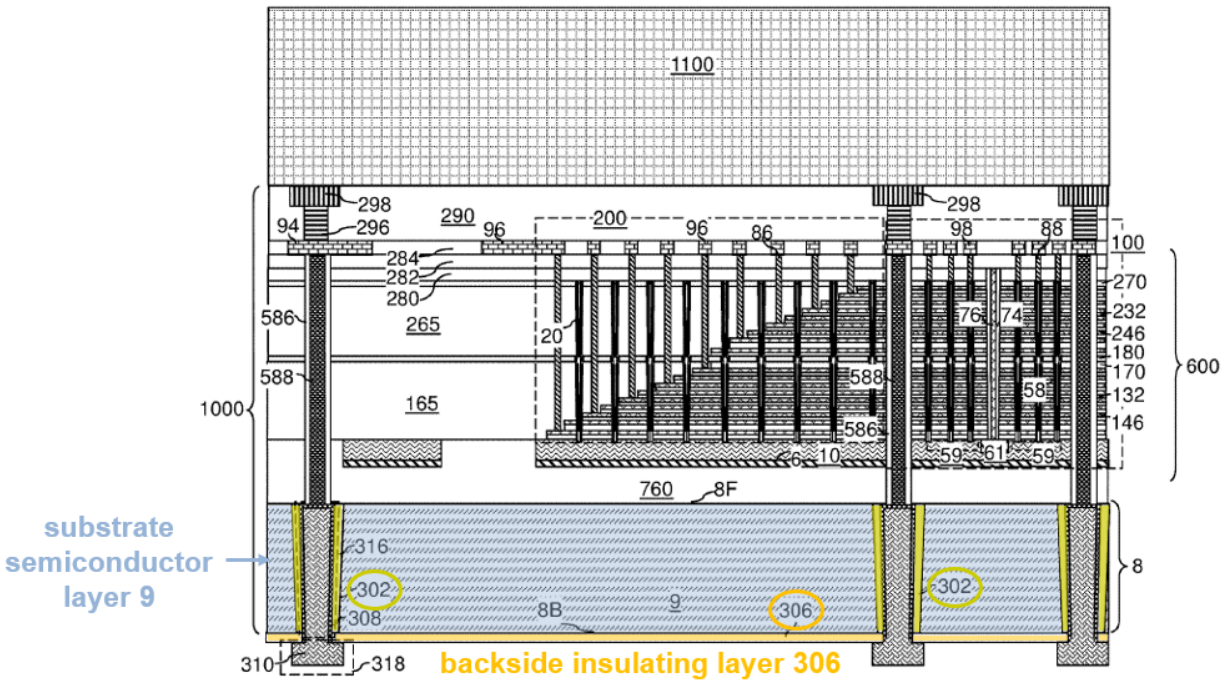



FIG. 11

Ex. 1006, Fig. 11 (annotated). Petitioner identifies "**substrate semiconductor layer 9**" as the alleged substrate.[6] Setting aside whether the backside insulating layer 306 and the insulating material liners 302 can be combined to be the purported isolation

[6] For the purposes of this POR, Patent Owner does not dispute Petitioner's mapping of the claimed "substrate" to Mushiga's "substrate semiconductor layer 9" in Ground 2.

structure and whether the insulating material liners 302 are part of the purported substrate, the combination still fails to meet the claims. Yang, ¶139.

No portion of Petitioner's alleged isolation structure is "part of" the alleged substrate as required by the claims. First, the "**insulating material liners 302**" portion of Petitioner's alleged isolation structure in Mushiga is not part of the alleged substrate ("substrate semiconductor layer 9") for the same reasons discussed in §§VI.A.1 and VII.A.1. Specifically, and again contrary to Petitioner's misplaced arguments about how the device is made, the alleged substrate is completely removed in cuts that extend through the alleged substrate, thereby creating regions that are outside and merely abutting the alleged substrate, and the "**insulating material liners 302**" is added in that through-opening.

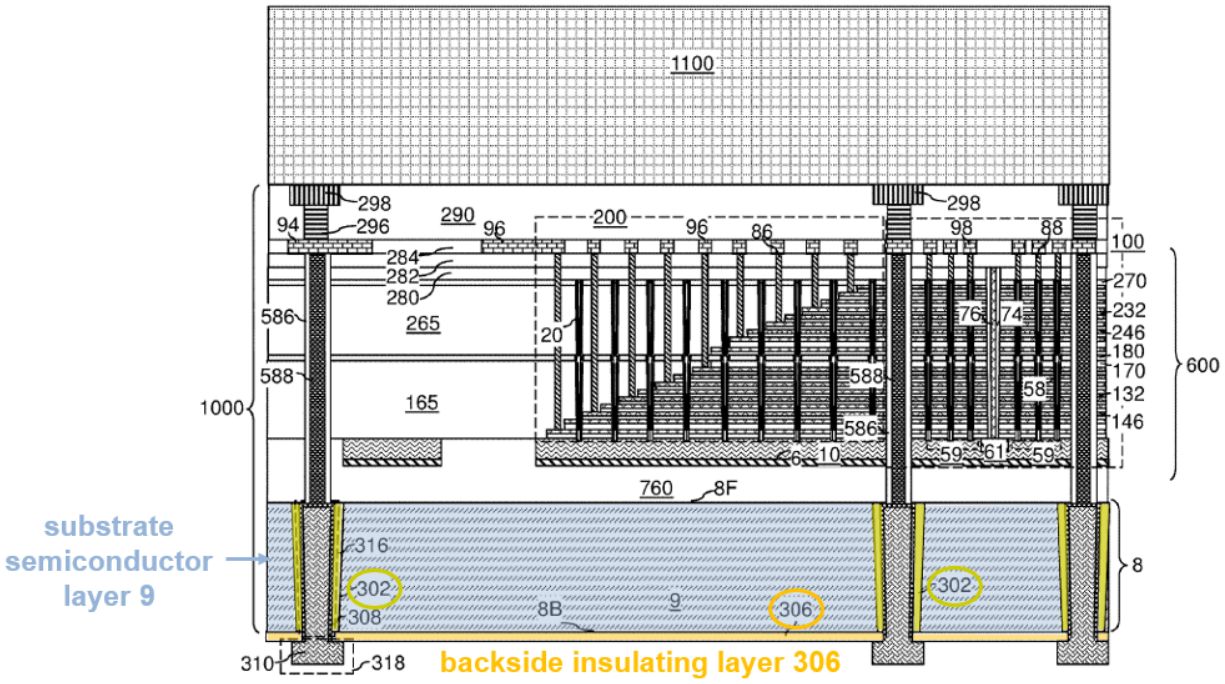
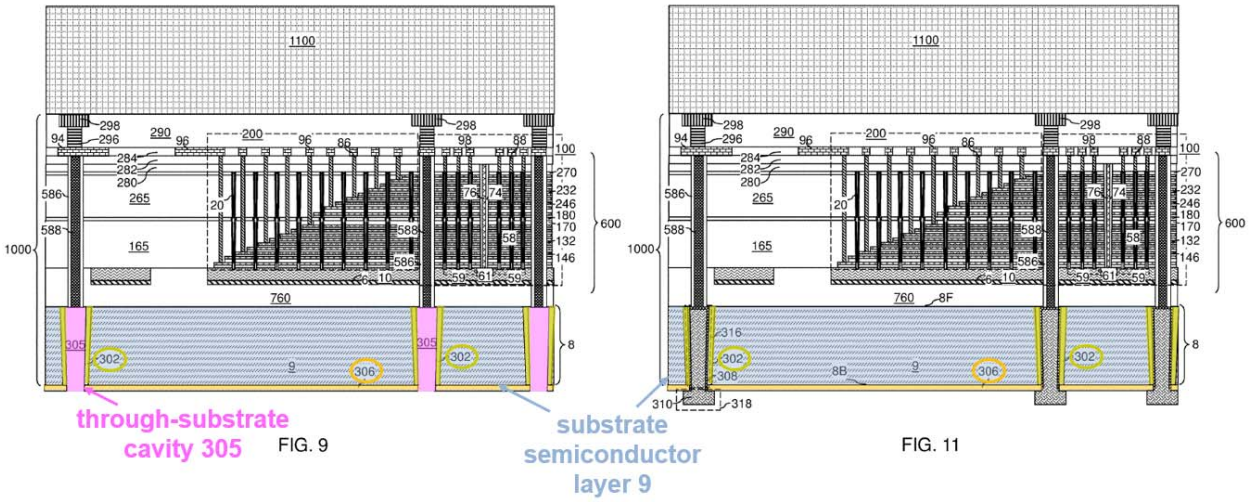



FIG. 11

Ex. 1006, Figure 11 (annotated). Thus, Mushiga teaches a similar spatial relationship to those at issue in Grounds 1A and 1B (Toyama), and Petitioner's arguments fail for the same reasons. Second, the "**backside insulating layer 306**" portion of Petitioner's alleged isolation structure in Mushiga is merely below the alleged substrate, rather than "part of" the substrate. Such a mapping fares no better than Toyama's alleged structure that is merely "on" the alleged substrate, and as discussed in §V.B, the construction "part of" does not encompass structures that are merely "on" (or in this case, "below") the alleged substrate. And even if "part of" encompassed structures that are merely "on" the substrate (it does not), "on" means "above" in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction (*see* §V.A-B). Yang, ¶140.

Attempting to address the required relationship between two claim terms, *i.e.*, that "a substrate" must be "***with***" "an isolation structure," Petitioner argues that "Mushiga's isolation structure […] ***is formed by removing portions of the*** substrate […]" (Pet. 79-80 (citing Ex. 1003, ¶ 173-174)), but this argument fails for the same reasons discussed in §VI.A.1. Specifically, as illustrated below, and again contrary to Petitioner's misplaced arguments regarding how the devices are made, the alleged substrate is completely removed in the relevant region, thereby creating regions

(**"through-substrate cavities 305"**) outside and merely abutting the alleged substrate, and the "**insulating material liners 302**" is in those through-openings.




Ex. 1006, Figs. 9, 11 (annotated). After the substrate is removed, there is no longer any portion of the alleged substrate in the relevant region. Moreover, and again similar to the discussion in §VI.A.1, Petitioner's cited processing steps relate to the manufacturing process, not the final structure, and the Challenged Claims are apparatus claims. Yang, ¶141.

Therefore, Petitioner has failed to show that Mushiga discloses or renders obvious "***a substrate with an isolation structure***" as required by limitation [15.a]. Yang, ¶142.

### 2. Petitioner Fails to Show That Mushiga Discloses or Renders Obvious "a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack" (Limitation [15.c])

Mushiga does not disclose or render obvious "***a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack***" as required by limitation [15.c] because the only alleged "dielectric structure" that extends though the stack is not also "on the isolation structure." Yang, ¶143.

As an initial matter, for all the reasons explained in §VIII.A.1, Mushiga does not disclose or render obvious the claimed isolation structure. As a result, Mushiga also does not disclose or render obvious the claimed dielectric structure on the isolation structure. Yang, ¶144.

Petitioner's mapping for this element also fails because the alleged "dielectric structure" is not both "extending vertically through the alternating conductor/dielectric layer stack" (mapped to Mushiga's "alternating stack (132, 146, 232, 246)") and "on the isolation structure." Petitioner maps "insulating material layer 760," "first retro-stepped dielectric material portion 165," "inter-tier dielectric layer 180," "second retro-stepped dielectric material portion 265," and "insulating spacer 586" collectively to the "dielectric structure" of the '378. Pet. 81-83.

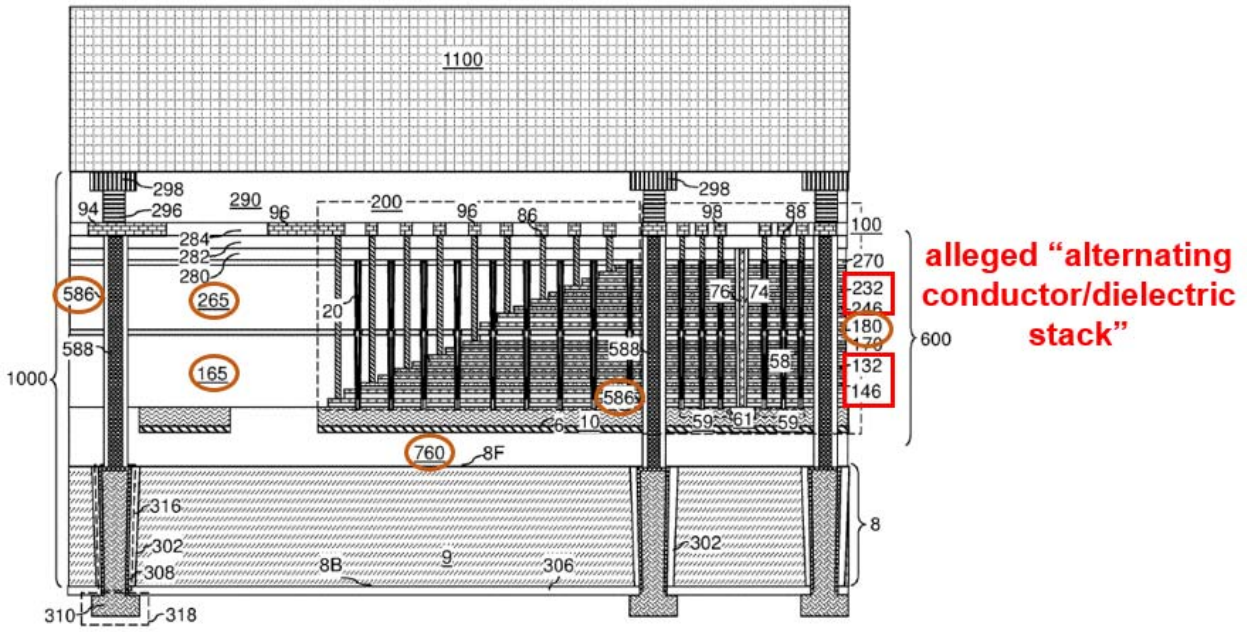



FIG. 11

Ex. 1006, Fig. 11 (annotated). Yang, ¶145.

Among these elements, only the "insulating spacers 586" is even arguably "***extending vertically through the alternating conductor/dielectric layer stack***" as required by Limitation [15.c]. As can be seen in the above figure, the other features are either outside the alternating stack altogether or, in the case of "inter-tier dielectric layer 180," it makes a horizontal cut across the alternating stack instead of extending vertically through the stack. Yang, ¶146.

While "insulating spacers 586" arguably extend through the alleged alternating conductor/dielectric layer stack, they fail to meet multiple other claim requirements. First, "insulating spacers 586" are not "***a dielectric structure on the***

***isolation structure"*** as required by the Challenged Claims (even assuming, *arguendo*, that Petitioner has identified an isolation structure).

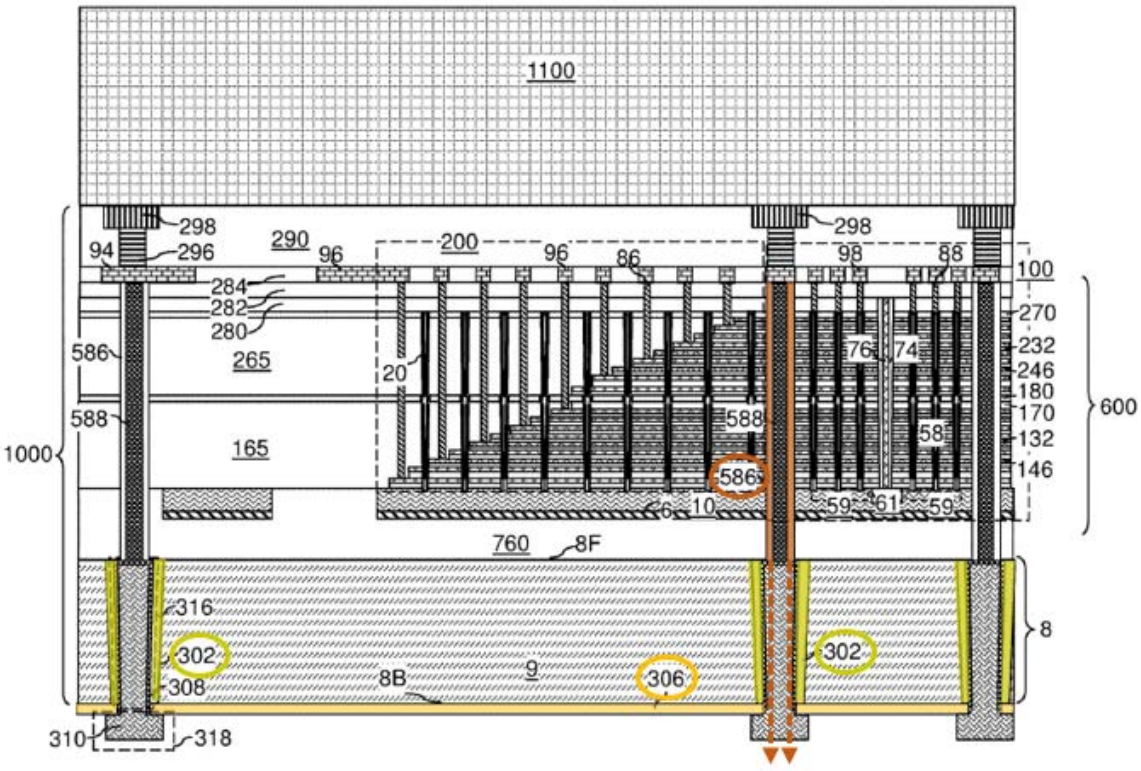


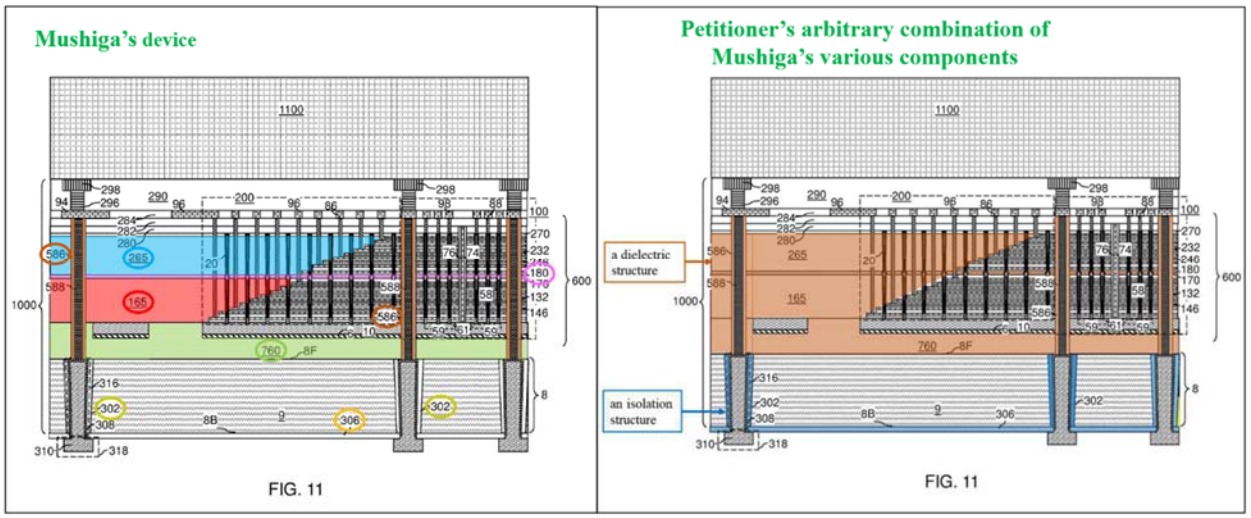

FIG. 11

Ex. 1006, Fig. 11 (annotated). As shown in the figure, **insulating spacers 586** are not "on" Petitioner's alleged isolation structure—**backside insulating layer 306** and **insulating material liners 302**—because **insulating spacers 586** are not above those structures. The annotated dashed lines show that the edge of the **insulating spacers 586**, if extended downward, do not pass through **backside insulating layer 306** or **insulating material liners 302** and thus are not above them. In the Institution Decision, the Board preliminarily found that "on" is not limited to any particular orientation (DI, 29), but as discussed in §V.A , the device may not be reoriented for

purposes of determining whether an alleged dielectric structure is on the isolation structure (when the device is reoriented, the vertical direction is reoriented and remains perpendicular to the substrate). Yang, ¶147.

Second, "insulating spacer 586" fails to meet the claim limitation "***through array contacts (TACs) [plural] extending vertically through the dielectric and the isolation structures***" [15.h] in the same way as Toyama's "insulating liner 674." *See* §VII.A.3, *supra*. Specifically, Petitioner has not shown a plurality of TACs that extend through the same insulating spacer 586 because, as shown above, each TAC extends through a separate insulating spacer. Yang, ¶148.

Realizing that "insulating spacer 586" fails to satisfy all the requirements of the claimed "dielectric structure," Petitioner attempts to combine the spacer with multiple other dielectric regions (Pet. 81-84), but its grouping has no discernable logic and does not cure the issue.



Ex. 1006, Fig. 11 (left image annotated by Patent Owner; right image annotated by Petitioner at Pet. 82, with top heading added by Patent Owner). As discussed further below, the elements Petitioner arbitrarily combines are separate structures with distinct locations and roles. Indeed, Petitioner purports to include structures that are analogous to ones described in the '378 as being separate from the claimed dielectric structure, and thus are not a single "dielectric structure" as claimed. Yang, ¶149.

For example, Mushiga's "first retro-stepped dielectric material portion 165" and "second retro-stepped dielectric material portion 265" in combination are nothing more than the dielectric material that covers the stair steps (Ex. 1006, 9:22-26, 9:38-39), which the '378 identifies as "dielectric layer 230" (separate from the '378's "dielectric layer 702" that is on the isolation structure and extending vertically through the stack).

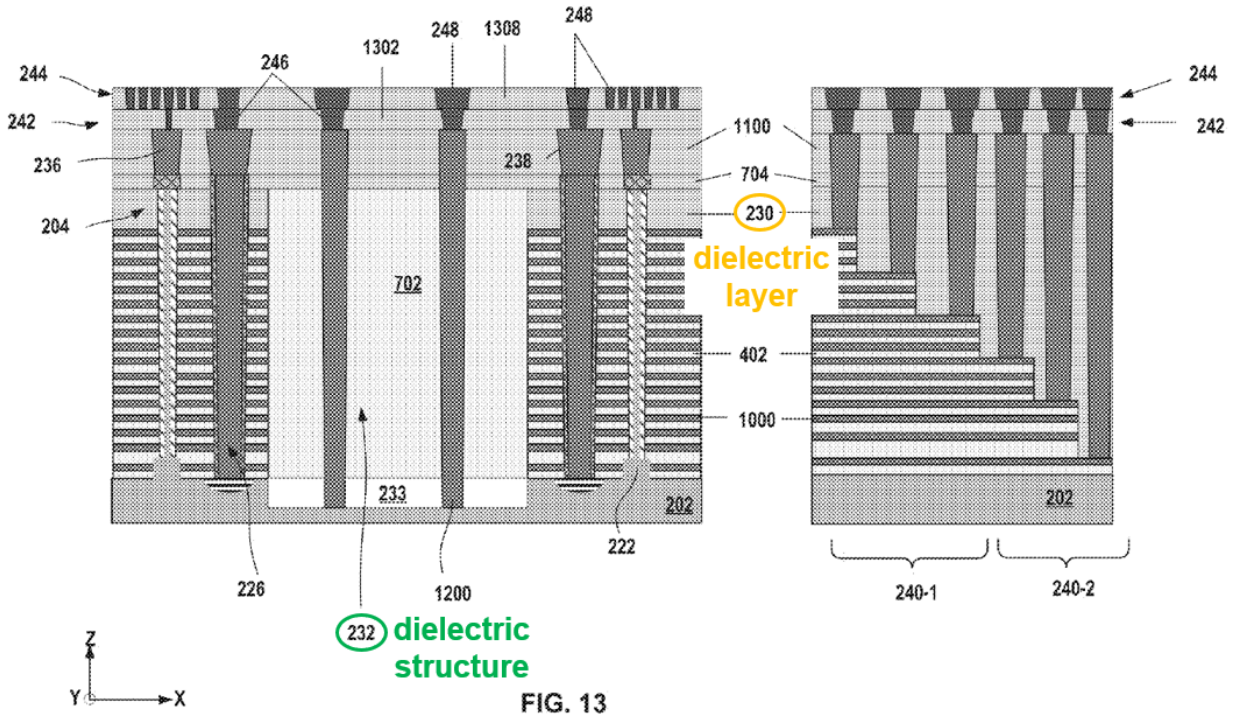



FIG. 13

’378, Fig. 13 (annotated). Yang, ¶150.

Similarly, Mushiga’s “insulating material layer 760” is a dielectric material layer that separates Mushiga’s alleged substrate (“semiconductor layer 9”) from “semiconductor material layer 10.” Ex. 1006, 9:8-12. Thus, Mushiga’s “insulating material layer 760” is akin to the ’378’s “dielectric layer 1100” shown below, which is above and spans the full area of the alternating stack (and is separate from the ’378’s “dielectric layer 702” that is on the isolation structure and extending vertically through the stack).

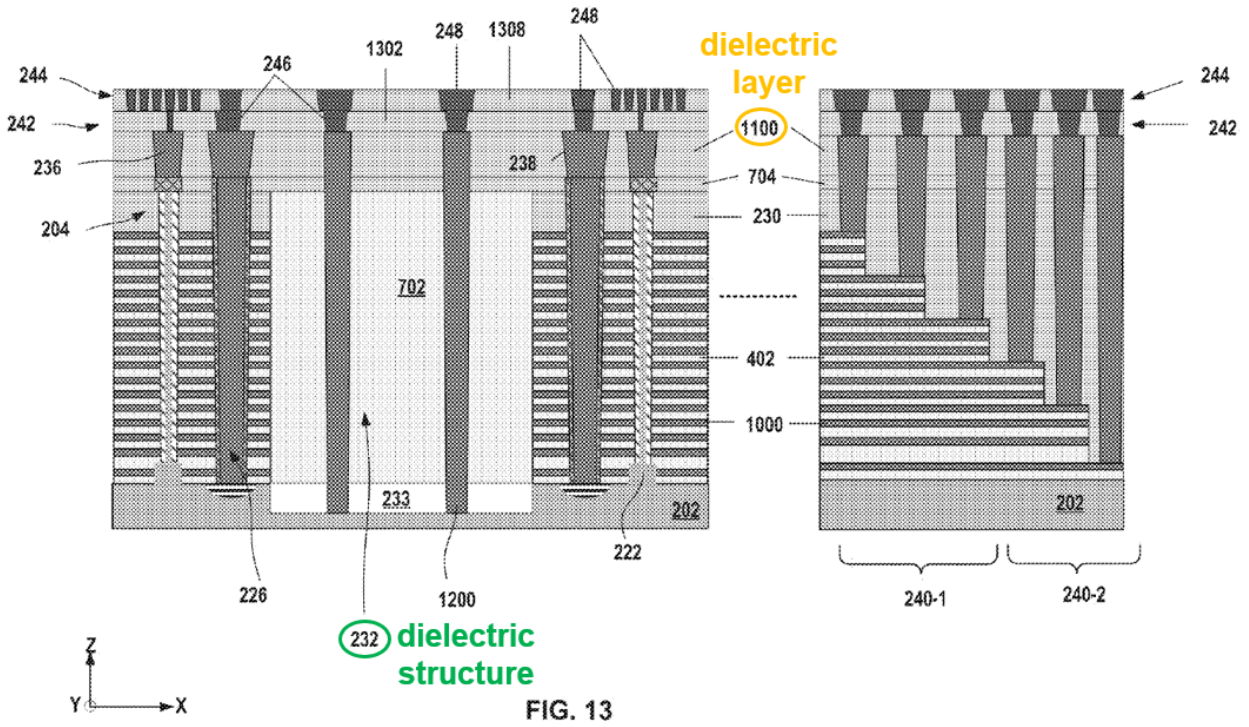



FIG. 13

’378, Fig. 13 (annotated). Yang, ¶151.

In its purported combination of adjacent dielectric elements, Petitioner also inconsistently omitted other adjacent dielectric elements that, if included, would have hurt its claim mapping. For example, as shown below in Mushiga’s Fig. 11, the red annotated dielectric features were not included.

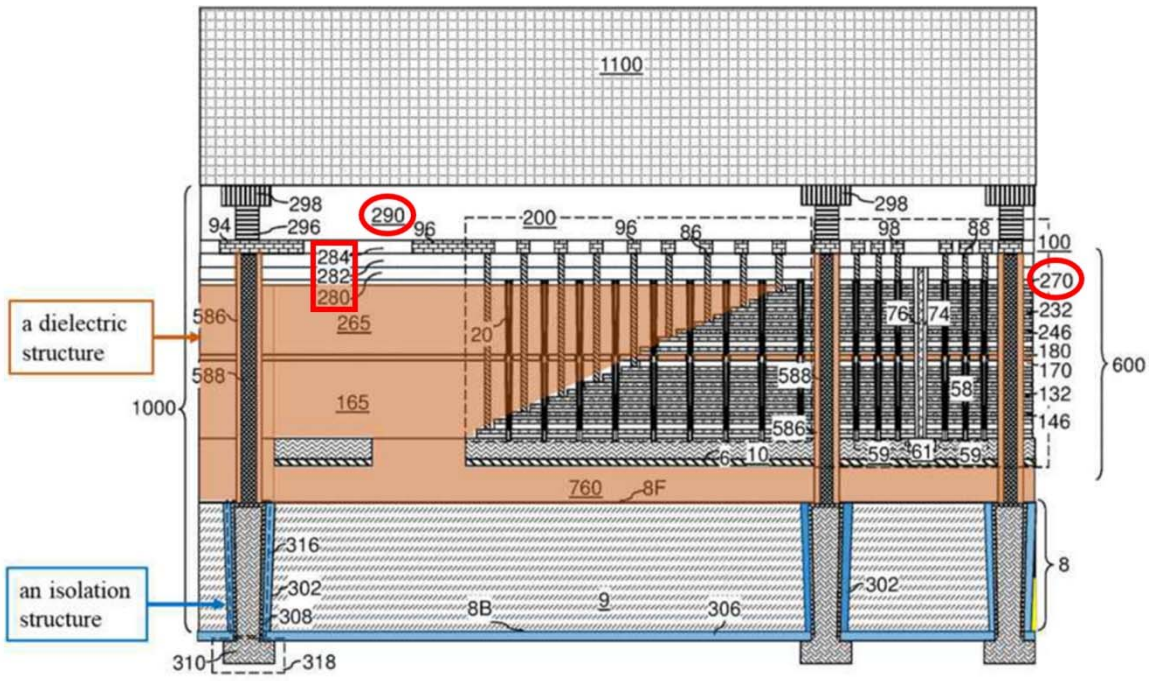



FIG. 11

Ex. 1006, Fig. 11 (annotated by Petitioner at Pet. 82, with red annotations added by Patent Owner). By Petitioner's logic of coloring in as one structure different dielectric features that are merely adjacent, Petitioner also should have included layers 270 ("second insulating cap layer 270"), 280 ("first contact level dielectric layer 280"), 282 ("second contact level dielectric layer 282"), 284 ("line level dielectric layer 284"), and 290 ("additional interconnect level dielectric layers 290"). This would have led to a situation in which Mushiga's through-memory level vias 588 (the alleged TACs) do not extend through the alleged dielectric structure as required by the Challenged Claims, as they would terminate within the dielectric structure (between layers 282 and 284). Petitioner's choices of which dielectric features to include and which to exclude in its mapping of Mushiga to the claimed

dielectric structure is inconsistent and originate purely from hindsight, rather than a teaching in the cited art or the knowledge of a POSITA. Indeed, Dr. Lee admits that there are other dielectric structures in Mushiga that he omitted, and that his process of selecting which structures to combine was guided by the claim language. Ex. 2007, 53:21-57:17. Yang, ¶152.

In the Institution Decision, the Board preliminarily found that the '378 does not preclude the claimed dielectric structure from being taught by multiple elements having different purposes (DI, 29), but this conclusion is inconsistent with the claims, which apply multiple requirements to the same "dielectric structure," regardless of whether other dielectric structures are also present in the device. *See, e.g.*, §V.C (discussing the requirement that TACs extend through the same dielectric structure). Petitioner does not sufficiently explain how these separate components can be considered a single structure (the claimed "dielectric structure"); *cf. Finjan*, 84 F.4th at 974-975 (holding that multiple occurrences of a claim element cannot be used satisfy a limitation that must be satisfied by a single occurrence of the element). Petitioner's argument that these separate components are a "structure" because "these components together are something 'that is constructed'" (Pet. 82-83) is inconsistent with the intrinsic record and *Finjan*. Indeed, while the Board in its Institution Decision "agree[d] with Petitioner" that these components "teach the claimed dielectric structure" (DI, 29-30), in its subsequent decision for IPR2024-

00791 (Ex. 2006), the Board "disagree[d] that merely because the three insulating liners are each constructed, that three constructed liners together constitute a single dielectric structure." Ex. 2006, 17. As the Board found, "[e]very component of Toyama's memory device is something that is constructed. Petitioner does not sufficiently explain how multiple constructed items can be considered to constitute a single structure just because each one of the multiple items is itself constructed." Ex. 2006, 17. This is equally true for Mushiga's memory device, where Petitioner's picking and choosing different structures to combine into a single structure because they are "constructed" is motivated by pure hindsight. Yang, ¶153.

The Board in the Institution Decision also cited the fact that the combined components are continuous, and can be combined into an "inhomogeneous continuous structure" (DI, 9-30), but that same logic would be true of any combination of adjacent components in a memory device, as the Board appears to have recognized IPR2024-00791. In addition, this argument does not address that Petitioner leaves out other dielectric components (270, 282, 280, 290) that would defeat its mapping, with no discernable logic other than hindsight. As discussed above, if Petitioner were permitted to combine continuous dielectric components and actually included all such continuous dielectric components, that would lead to the alleged TACs not extending through the alleged dielectric structure as required by the Challenged Claims. Yang, ¶154.

Therefore, Petitioner has failed to show that Mushiga discloses or renders obvious "a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack" as required by limitation [15.c]. Yang, ¶155.

### 3. Petitioner Fails to Show That Mushiga Discloses or Renders Obvious "TACs extending vertically through the dielectric and the isolation structures" (Limitation [15.h])

Mushiga does not disclose or render obvious "***through array contacts (TACs) extending vertically through the dielectric and the isolation structures***" as required by limitation [15.h] because Mushiga's alleged TACs do not extend through the same structure (the claimed "dielectric structure"). Yang, ¶156.

As an initial matter, for all the reasons explained in §§IX.A.1-2, Mushiga does not disclose or render obvious the claimed isolation structure or the claimed dielectric structure on the isolation structure. Yang, ¶157.

In addition, "insulating spacer 586" fails to meet this limitation in the same way as Toyama's "insulating liner 674"—the plurality of TACs do not extend through the same alleged dielectric structure. *See* §VIII.A.3, *supra*. For example, each of Mushiga's TACs has a separate, unconnected insulating spacer 586, which Petitioner improperly combines for the alleged "dielectric structure." *See* Pet. 98.

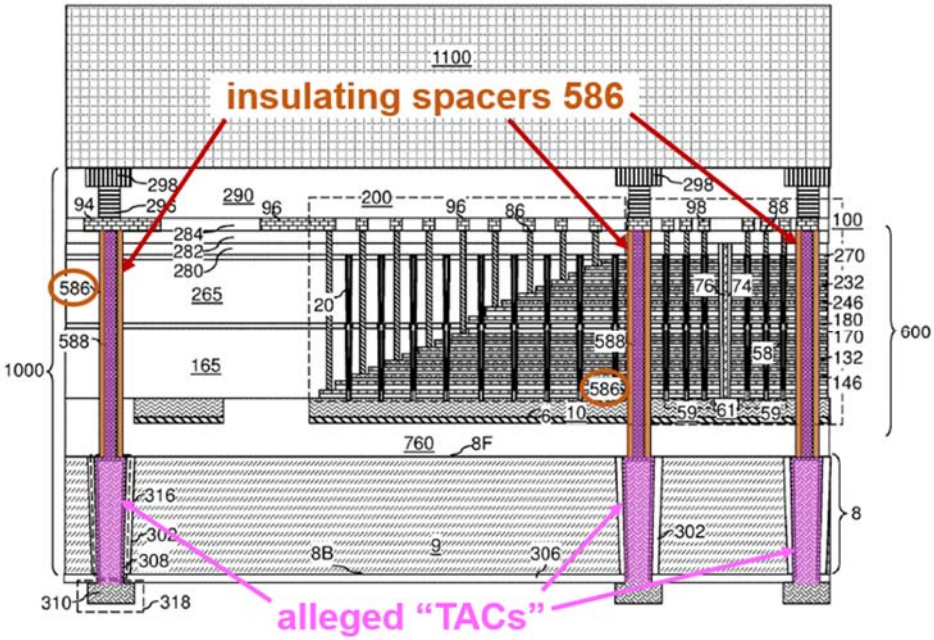



FIG. 11

Ex. 1006, Fig. 11 (annotated). Yang, ¶158.

As discussed in §VIII.A.3, multiple occurrences of a claim element, such as multiple occurrences of insulating spacers 586, cannot be used satisfy a limitation that must be satisfied by a single occurrence of the element. *Finjan*, 84 F.4th at 974-975. Yang, ¶159.

Therefore, Petitioner has failed to show that Mushiga discloses or renders obvious "through array contacts (TACs) extending vertically through the dielectric and the isolation structures" as required by limitation [15.h]. Yang, ¶160.

### B. Claim 17: Petitioner Fails to Show that Mushiga Discloses or Renders Obvious "the dielectric structure comprises a through array contact region of the 3D memory device"

Mushiga does not disclose or render obvious "***the dielectric structure comprises a through array contact region of the 3D memory device***" as further

required by claim 17 because the alleged TAC region of Mushiga is not within or defined by the alleged dielectric structure as required by claim 17. Yang, ¶161.

As discussed in §V.D, the phrase "the dielectric structure comprises a through array contact region of the 3D memory device" means "a region that is within or defined by the dielectric structure and which includes the through array contacts extending through the dielectric structure." Yang, ¶162.

Petitioner's mapping of the TAC region to Mushiga is not within or defined by the alleged dielectric structure. Instead, Petitioner's alleged TAC region is an arbitrarily defined region that extends beyond the dielectric structures and the other structures it contains.

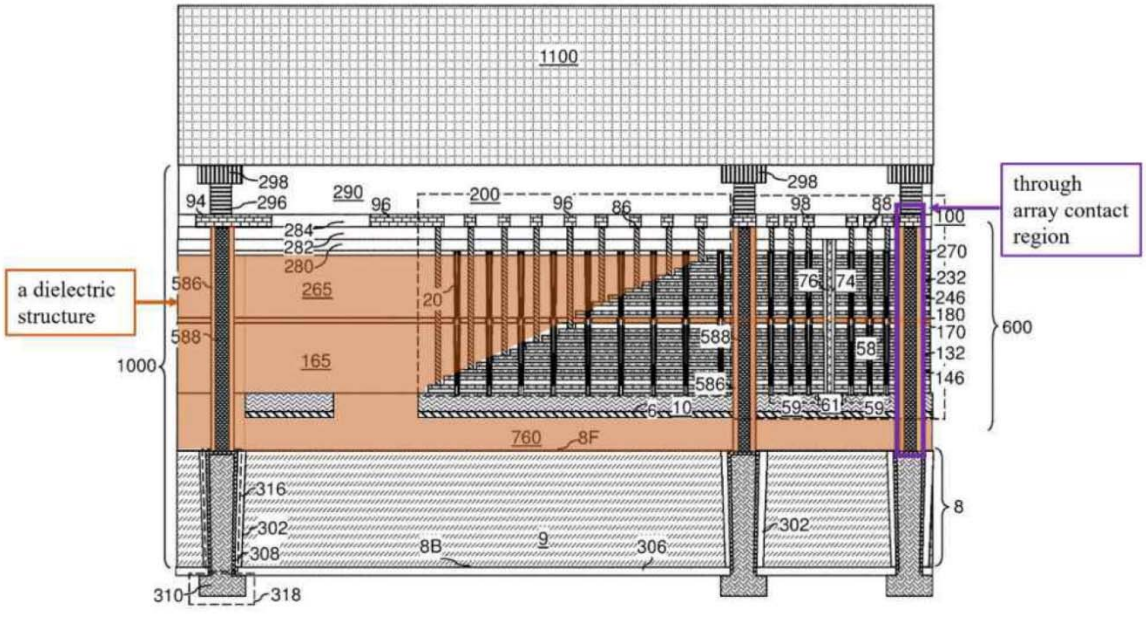



FIG. 11

Ex. 1006, Fig. 11 (annotated by Petitioner at Pet. 100). Yang, ¶163.

As seen in the annotated figure, Petitioner's alleged through array contact region is not within or defined by Petitioner's alleged dielectric structure. For example, the alleged region includes portions of metal structures 94 and bonding pad connection via structures 296. Petitioner's mapping does not address these issues. Pet. 100. Yang, ¶164.

Therefore, Petitioner has failed to show that Toyama's Second Modification discloses or renders obvious "the dielectric structure comprises a through array contact region of the 3D memory device" as required by claim 17. Yang, ¶165.

## X. GROUND 3: MUSHIGA IN VIEW OF MAKALA DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 15-17 AND 19-20

Petitioner fails to show that Mushiga in view of Makala discloses or renders obvious limitations [15.a], [15.c], and [15.h] and the additional limitation of dependent claim 17 for the same reasons discussed above for Ground 2. In Ground 3, Petitioner relies on Mushiga in view of Makala as allegedly rendering obvious claims 15-17 and 19-20 of the '378, but the Petition does not raise any new arguments as to limitations [15.a], [15.c], and [15.h] and claim 17. *See* Pet. 102-105. Rather, Petitioner applies Makala's teaching to Mushiga only for limitation [15.g.ii] ("local contacts disposed on … the slit structures") and "relies solely on Mushiga" for all other limitations. Pet. 102-103. As explained in §IX, Petitioner fails in Ground 2 to show that limitations [15.a], [15.c], and [15.h] and the additional limitation of dependent claim 17 are disclosed or rendered obvious by Mushiga, and

because no additional arguments are introduced in Ground 3 regarding these limitations, the Petition also fails for Ground 3. Yang, ¶166.

Accordingly, Petitioner has failed to meet its burden of showing Mushiga in view of Makala discloses or renders obvious limitations [15.a], [15.c], and [15.h] and the additional limitation of dependent claim 17 in Ground 3. Yang, ¶167.

## XI. CONCLUSION

For the reasons above, Petitioner has failed to demonstrate by a preponderance of the evidence that any of the Challenged Claims of the ’378 is anticipated or obvious. Yang, ¶¶168-170. Accordingly, the Board should find in favor of Patent Owner and uphold the validity of all Challenged Claims.

Dated: February 10, 2025 Respectfully submitted,

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# CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word-processing system's word count, the brief contains 13,989 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

Dated: February 10, 2025

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# CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S RESPONSE UNDER 37 C.F.R. § 42.120 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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