

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

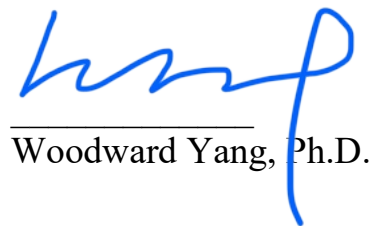
YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00788
Patent 10,658,378

**DECLARATION OF WOODWARD YANG, PH.D. IN SUPPORT OF
PATENT OWNER'S RESPONSE**

Executed this 10th day of February, 2025 in Paris, France.



Woodward Yang, Ph.D.

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	QUALIFICATIONS	2
III.	MY ASSIGNMENT AND BASES OF OPINIONS	8
IV.	SUMMARY OF MY OPINIONS	10
V.	APPLICABLE LEGAL STANDARDS	13
A.	Claim Construction	14
B.	Anticipation	14
C.	Obviousness	15
D.	Claim Dependency	17
VI.	THE '378 PATENT	17
A.	Overview of the '378 Patent	17
B.	Listing of the Challenged Claims	20
C.	File History of the '378 Patent	21
VII.	LEVEL OF ORDINARY SKILL IN THE ART	23
VIII.	CLAIM CONSTRUCTION FOR THE '378 PATENT	25
A.	“a dielectric structure on the isolation structure” (Claim 15)	25
B.	“a substrate with an isolation structure” (Claim 15)	31
C.	“the dielectric and the isolation structures” (Claim 15)	35
D.	“the dielectric structure comprises a through array contact region of the 3D memory device” (Claim 17)	38
IX.	THE ASSERTED PRIOR ART	41
A.	U.S. Patent Publication No. 2017/0179026 (“Toyama”) (Ex. 1005)	41
B.	U.S. Patent No. 10,354,980 (“Mushiga”) (Ex. 1006)	45
C.	U.S. Patent No. 10,262,945 (“Makala”) (Ex. 1007)	47
X.	PETITIONER’S GROUND 1A: Toyama’s First Exemplary Structure Does Not Disclose or Render Obvious Claims 15-17 and 19-20	48

A.	Independent Claim 15: Toyama’s First Exemplary Structure Does Not Disclose Or Render Obvious Limitations [15.a], [15.c.i], and [15.h]	49
(a)	Toyama’s First Exemplary Structure Does Not Disclose or Render Obvious “a Substrate With an Isolation Structure” (Limitation [15.a])	49
(b)	Toyama’s First Exemplary Structure Does Not Disclose or Render Obvious “a Dielectric Structure on the Isolation Structure” (Limitation [15.c.i])	56
(c)	Toyama’s First Exemplary Structure Does Not Disclose or Render Obvious “TACs Extending Vertically Through the Dielectric and the Isolation Structures” (Limitation [15.h])	63
B.	Claim 17: Toyama’s First Exemplary Structure Does Not Disclose or Render Obvious “the Dielectric Structure Comprises a Through Array Contact Region of the 3D Memory Device”	64
XI.	PETITIONER’S GROUND 1B: Toyama’s Second Modification Does Not Disclose or Render Obvious Claims 15-17 and 19-20	64
A.	Independent Claim 15: Toyama’s Second Modification Does Not Disclose Or Render Obvious Limitations [15.a], [15.c.i], and [15.h]	65
(a)	Toyama’s Second Modification Does Not Disclose or Render Obvious “a Substrate With an Isolation Structure” (Limitation [15.a])	65
(b)	Toyama’s Second Modification Does Not Disclose or Render Obvious “a Dielectric Structure on the Isolation Structure” (Limitation [15.c.i])	68
(c)	Toyama’s Second Modification Does Not Disclose or Render Obvious “TACs Extending Vertically Through the Dielectric and the Isolation Structures” (Limitation [15.h])	68
B.	Claim 17: Toyama’s Second Modification Does Not Disclose or Render Obvious “the Dielectric Structure Comprises a Through Array Contact Region of the 3D Memory Device”	71

XII.	PETITIONER’S GROUND 2: Mushiga Does Not Disclose or Render Obvious Claims 15-17 and 19-20	74
A.	Independent Claim 15: Mushiga Does Not Disclose Or Render Obvious Limitations [15.a], [15.c.i], and [15.h]	75
(a)	Mushiga Does Not Disclose or Render Obvious “a Substrate With an Isolation Structure” (Limitation [15.a])	75
(b)	Mushiga Does Not Disclose or Render Obvious “a Dielectric Structure on the Isolation Structure and Extending Vertically through the Alternating Conductor/Dielectric Layer Stack” (Limitation [15.c]).....	79
(c)	Mushiga Does Not Disclose or Render Obvious “TACs Extending Vertically Through the Dielectric and the Isolation Structures” (Limitation [15.h])	89
C.	Claims 17: Mushiga Does Not Disclose or Render Obvious “the Dielectric Structure Comprises a Through Array Contact Region of the 3D Memory Device”	90
XIII.	PETITIONER’S GROUND 3: Mushiga in view of Makala Does Not Disclose or Render Obvious Claims 15-17 and 19-20	92
II.	CONCLUSION.....	93

I, Woodward Yang, Ph.D., hereby declare as follows:

I. INTRODUCTION

1. I have been retained by counsel for Yangtze Memory Technologies Company, LTD (“YMTC”) in the above captioned *inter partes* review of U.S. Patent No. 10,658,378 (Ex. 1001, “’378 patent”). I have been asked to consider the scope and content of the prior art, and respond to certain allegations regarding the prior art, presented by Micron Technology, Inc., (“Petitioner”) in its petition for *inter partes* review of the ’378 patent (“Petition”) and the April 30, 2024 Declaration of Dr. Jack Lee (Ex. 1003). The arguments raised in Dr. Lee’s declaration are similar to those raised in the Petition. Unless otherwise noted, my opinions with respect to the Petition also apply to the corresponding section of Dr. Lee’s declaration, and vice-versa. As explained in Sections X-XIII (discussing the Grounds raised in the Petition), the invalidity arguments raised in the Petition do not show that the prior art anticipates or renders obvious any of the Challenged Claims, and the arguments raised in Dr. Lee’s declaration are insufficient for similar reasons.

2. I am being compensated for my time at my usual consulting rate of \$900 per hour, plus reimbursement for any actual expenses. No part of my compensation depends on the content of the opinions that I herein render or on the outcome of this review proceeding. I have no expectation or promise of additional business with

Patent Owner (“PO”) in exchange for the positions explained herein. I do not have any direct financial interest in any of the parties.

3. Unless otherwise noted, the statements made herein are based on my personal knowledge, and if called to testify about this declaration, I could and would do so competently and truthfully.

II. QUALIFICATIONS

4. My qualifications including cases in which I was an expert are stated more fully in my curriculum vitae which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

5. I am presently the Gordon McKay Professor of Electrical Engineering and Computer Science in the Paulson School of Engineering and Applied Science at Harvard University, where I have taught and pursued research endeavors since 1990. I have taught classes related generally to the design and analysis of microelectronic circuits and Very Large Scale Integration (“VLSI”) systems: the process of creating integrated circuits by combining thousands of transistors into a single chip. The microprocessors and graphics processors found in personal computers and smartphones are examples of VLSI devices. I have also taught graduate and undergraduate level courses in computer architecture, computing hardware, digital logic design, mixed signal circuit design, circuit theory, and engineering design. My research pursuits have been directed to the development of advanced computing and

memory systems for high performance image processing and computer vision applications, data encryption, error correcting codes, and integrated sensor and computing systems.

6. In 2008, I was appointed as the Harvard Business School (“HBS”) University Fellow and have taught courses at HBS as a Visiting Professor. In this capacity, I have conducted research and taught business school courses on the commercialization of new technologies, technological innovation, and industry architecture.

7. I have over 30 years of experience in semiconductor design and manufacturing technology. I graduated with a Bachelor of Science degree in Electrical Engineering and Computer Science from the University of California, Berkeley in 1984. I received a Master’s of Science degree in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology in 1987. I then received a Ph.D. in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology in 1990. My doctoral thesis dealt with the architecture and design of charge-coupled device (“CCD”) processors for computer vision. In the 1990’s and early 2000’s, I developed and successfully commercialized two disruptive technologies, complementary metal oxide semiconductor (“CMOS”) image sensors and pseudo-SRAM (Static Random Access Memory), which were based on advanced DRAM manufacturing technology and are now found in almost

every cell phone and other mobile devices. In addition, I am a named inventor on nine U.S. patents pertaining to semiconductor devices and related technology, which are listed in my curriculum vitae, a true and correct copy of which is attached as Appendix A.

8. My research has focused on the design and implementation of integrated circuits and systems, including dynamic random access memory (“DRAM”), CMOS image sensors, mixed-signal circuitry, and high performance image processing systems. Over the course of my work, I have developed and become familiar with a wide range semiconductor manufacturing technology.

9. In addition, I have received numerous honors and awards for my contributions to the electrical engineering industry, including the National Science Foundation Young Investigator Award, Army Young Investigator Award, Hertz Foundation Fellowship, and National Science Foundation Fellowship. I have given numerous presentations and invited lectures, including at the Consumer Electronics Show as Keynote Speaker, at the U.S. Science and Technology Symposium in Computing and Telecommunication, at the National Research Council Workshop on the Electronics Industry, and before the Institute of Electrical and Electronics Engineers (“IEEE”) Laser and Electro Optical Society. I have also been named an IEEE Distinguished Lecturer. In addition, I have been interviewed three times by The EE Times and once by The Weekly Economist.

10. I have also served as a consultant throughout my career. From 1991 to 1993, I advised on the research and development of advanced Complementary-metal-oxide-semiconductor (“CMOS”)/charge-coupled device (“CCD”) technology and circuitry at the Istituto per la Ricerca Scientifica e Tecnologica (IRST), in Trento, Italy. From 1993 to 1998, I served as a consultant for Hamamatsu Photonics, K.K. in Hamamatsu City, Japan, where I helped develop smart image sensors and CMOS/CCD analog charge-domain circuitry.

11. From 1995 to 2000, I worked as a consultant and Senior Fellow at Hyundai Electronics Industries, in Ichon, Korea. At Hyundai, I developed and commercialized high performance CMOS image sensor technology for embedded image sensing and processing applications and researched advanced Dynamic Random Access Memory (“DRAM”) design and merged memory logic (MML) technology for advanced computer systems. From 1998 to 2001, I served as a member of the Science and Technology Board for Polaroid Corporation, where I evaluated Polaroid’s research and technology developments.

12. In 2000 I founded a company called Silicon7, Inc. Silicon7 was located in Seongnam-si, Kyoungki-do, Korea, and developed application-specific memory products for mobile communications and computing platforms. For example, we developed 4-Mbit and 8-Mbit pseudo SRAMs which featured a 70-nanosecond access time and ultra low power consumption that were targeted for mobile

applications such as handsets and personal digital assistant. These advanced memory components and systems were optimized for the distinct requirements of mobile communication devices.

13. I am also an author (or co-author) of many publications, including:

- “The New Economics of Semiconductor Manufacturing,” IEEE Spectrum, vol. 45, issue 5, pp. 24-29 (May 2008);
- “A Low-Power 256-Mb SDRAM with an On-Chip Thermometer and Biased Reference Line Sensing Scheme,” IEEE Journal of Solid-State Circuits, vol. 38, no. 2, pp. 329-337 (February 2003);
- “An Antifuse EPROM Circuitry Scheme for Field-Programmable Repair in DRAM,” IEEE Journal of Solid-State Circuits, vol. 35, no. 10, pp. 1408-1414, (October 2000);
- “An Improved Digital CMOS Imager,” IEEE Workshop on Charged-Coupled Devices and Advanced Image Sensors, Nagano, Japan (June 1999);
- “A Linear-Response, High-Dynamic Range CMOS Imager Suitable for Spectroscopic Applications,” IEEE Workshop on Charged-Coupled Devices and Advanced Image Sensors, Nagano, Japan (June 1999);

- “An Integrated 800 x 600 CMOS Imaging System,” Digest of Technical Papers of IEEE International Solid-State Circuits Conference, pp. 304-305 (February 1999);
- “A CCD/CMOS Image Sensor Array with Integrated A/D Conversion,” Proceedings of the IEEE International Symposium on Circuits and Systems, vol. 3, pp. 1908-1911 (June 1997);
- “Neuromorphic CMOS Circuitry for Active Bidirectional Delay Lines,” Proceedings of IEEE International Symposium on Circuits and Systems, vol. 3, pp. 473-476 (May 1996);
- “A CCD/CMOS Image Motion Sensor,” Digest of Technical Papers of IEEE International Solid—State Circuits Conference, pp. 194-195 (February 1993);
- “The MIT Vision Chip Project: Analog VLSI Systems for Fast Image Acquisition and Early Vision Processing,” Proceedings of the International Conference on Robotics and Automation, vol. 2, pp. 1330-1335 (April 1991);

- “Optimization of Low Pressure Nitridation/Oxidation of SiO₂ for Scaled MOS Devices,” IEEE Transactions on Electron Devices, vol. ED-35, no. 7, pp. 935-944 (July 1988);
- “MOS Electrical Characteristics of Low Pressure Re—oxidized Nitrided Oxide,” Technical Digest of International Electron Devices Conference, pp. 668-671 (December 1986); and
- “Hot Carriers Induced Degradation in Thin Gate Oxide MOSFETs,” Technical Digest of International Electron Devices Conference, pp. 186-189, (December 1983).

III. MY ASSIGNMENT AND BASES OF OPINIONS

14. I have been asked to provide my opinions as to the scope and content of the '378 patent as well as the prior art presented by Petitioner in the Petition and Dr. Lee. Specifically, I have been asked to opine on what a person of ordinary skill in the art would have understood the '378 patent to disclose, and I have been asked to provide my opinions concerning whether Toyama (Ex. 1005), Mushiga (Ex. 1006), or Mushiga in view of Makala (Ex. 1007) discloses or renders obvious claims 15-17, 19-20 of the '378 patent.

15. In the course of conducting my analysis and forming my opinions, I have reviewed the references and materials cited in the Petition, Preliminary Response, and herein including those listed below:

Exhibit No.	Reference
N/A	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,658,378 (IPR2024-00788, Paper 1)
Ex. 1001	U.S. Patent No. 10,658,378 B2 to Tao et al.
Ex. 1002	File History of U.S. Patent No. 10,658,378 B2 to Tao et al.
Ex. 1003	Declaration of Dr. Jack Lee (“Lee”)
Ex. 1004	<i>Curriculum Vitae</i> of Dr. Jack C. Lee
Ex. 1005	U.S. Patent Publ. No. 2017/0179026 A1 (“Toyama”)
Ex. 1006	U.S. Patent No. 10,354,980 (“Mushiga”)
Ex. 1007	U.S. Patent No. 10,262,945 (“Makala”)
Ex. 1011	CN109075169A Office Action, dated November 14, 2019
Ex. 1012	Certified Translation of CN109075169A Office Action, dated November 14, 2019
Ex. 1013	CN109075169A Reexamination Decision, dated November 25, 2021
Ex. 1014	Certified Translation of CN109075169A Reexamination Decision, dated November 25, 2021
Ex. 1015	Michelsoni, “3D Flash Memories” (2016)
Ex. 1016	Aritome, “NAND Flash Memory Technologies” (2016)
Ex. 1017	U.S. Patent No. 9,620,512 to Nishikawa et al.
Ex. 1018	U.S. Patent Publ. No. 2016/0056188 A1 to Lee et al.
Ex. 1019	U.S. Patent No. 9,293,348 to Lai et al.
Ex. 1020	U.S. Patent No. 10,103,169 to Ge et al.
Ex. 1021	U.S. Patent No. 8,697,519 to Jee et al.
Ex. 1022	Excerpts from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)
N/A	Patent Owner’s Preliminary Response (IPR2024-00788, Paper 12)
Ex. 2001	Micron 4-2 Claim Construction Disclosure
Ex. 2002	YMTC 4-2 Claim Construction Disclosure
N/A	Decision Granting Institution of <i>Inter Partes</i> Review of U.S. Patent No. 10,658,378 (IPR2024-00788, Paper 13)
Ex. 2003	Micron’s Preliminary Claim Constructions
Ex. 2004	YMTC’s Proposed Claim Constructions

Ex. 2006	Decision Granting Institution of <i>Inter Partes Review</i> of U.S. Patent No. 10,937,806 (IPR2024-00791, Paper 11)
Ex. 2007	Deposition Transcript of Dr. Lee

16. My opinions in this declaration are based on my review of these documents, as well as upon my education, training, research, knowledge, and experience.

17. All emphases (such as bolding, underlying, or italics) appearing in quotations and citations cited herein have been added by me, unless otherwise stated.

IV. SUMMARY OF MY OPINIONS

18. It is my opinion that Toyama does not disclose or render obvious claims 15-17, 19-20 of the '378 patent at least because:

- Toyama's First Exemplary Structure does not disclose or render obvious "a substrate with an isolation structure," as required by independent claim 15 (from which claims 16-17, 19-20 depend).
- Toyama's First Exemplary Structure does not disclose or render obvious "a dielectric structure on the isolation structure," as required by independent claim 15 (from which claims 16-17, 19-20 depend).
- Toyama's First Exemplary Structure does not disclose or render obvious "TACs extending vertically through the dielectric and the isolation

structures,” as required by independent claim 15 (from which claims 16-17, 19-20 depend).

- Toyama’s First Exemplary Structure does not disclose or render obvious “the dielectric structure comprises a through array contact region of the 3D memory device,” as required by dependent claim 17.
- Toyama’s Second Modification does not disclose or render obvious “a substrate with an isolation structure,” as required by independent claim 15 (from which claims 16-17, 19-20 depend).
- Toyama’s Second Modification does not disclose or render obvious “a dielectric structure on the isolation structure,” as required by independent claim 15 (from which claims 16-17, 19-20 depend).
- Toyama’s Second Modification does not disclose or render obvious “TACs extending vertically through the dielectric and the isolation structures,” as required by independent claim 15 (from which claims 16-17, 19-20 depend).
- Toyama’s Second Modification does not disclose or render obvious “the dielectric structure comprises a through array contact region of the 3D memory device,” as required by dependent claim 17.

19. It is my opinion that Mushiga does not disclose or render obvious claims 15-17, 19-20 of the '378 patent at least because:

- Mushiga does not disclose or render obvious “a substrate with an isolation structure,” as required by independent claim 15 (from which claims 16-17, 19-20 depend).
- Mushiga does not disclose or render obvious “a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack,” as required by independent claim 15 (from which claims 16-17, 19-20 depend).
- Mushiga does not disclose or render obvious “TACs extending vertically through the dielectric and the isolation structures,” as required by independent claim 15 (from which claims 16-17, 19-20 depend).
- Mushiga does not disclose or render obvious “the dielectric structure comprises a through array contact region of the 3D memory device,” as required by dependent claim 17.

20. It is my opinion that Mushiga in view of Makala does not render obvious claims 15-17, 19-20 of the '378 patent at least because:

- Mushiga in view of Makala does not render obvious “a substrate with an isolation structure,” as required by independent claim 15 (from which claims 16-17, 19-20 depend).
- Mushiga in view of Makala does not render obvious “a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack,” as required by independent claim 15 (from which claims 16-17, 19-20 depend).
- Mushiga in view of Makala does not render obvious “TACs extending vertically through the dielectric and the isolation structures,” as required by independent claim 15 (from which claims 16-17, 19-20 depend).
- Mushiga in view of Makala does not render obvious “the dielectric structure comprises a through array contact region of the 3D memory device,” as required by dependent claim 17.

V. APPLICABLE LEGAL STANDARDS

21. I am not a legal expert and offer no opinions on the law. However, I have been informed by counsel of the various legal standards that apply, and I have applied those standards in arriving at my conclusions.

A. Claim Construction

22. I was informed, unless otherwise noted, I should give claim terms their ordinary and customary meaning as understood by a person of skill in the art at the time of the invention. I was informed and I understand that the words of the patent's claims and the context in which the term is used in the claims can be highly instructive in ascertaining the term's meaning. I further understand that the terms of a claim are to be interpreted in the context of the entire patent, including the patent's other claims, its specification and its figures.

23. I have been further instructed that a patent's "prosecution history" may often provide helpful evidence about how the Patent Office and the applicant understood the patent and its claims. Therefore, I have been instructed that claim terms should also be interpreted in light of the patent's prosecution history. In addition to the claims, the specification, the figures, and the prosecution history, I have been instructed that certain "extrinsic evidence" such as scientific or technical references may also help inform the way in which the person of ordinary skill in the art might understand the claim term. I have been instructed that extrinsic evidence must always be considered in the context of the intrinsic evidence.

B. Anticipation

24. I have been informed by counsel that a patent claim is invalid as anticipated if each element of that claim is present either explicitly or inherently in

a single prior art reference. I have also been informed that, to be an inherent disclosure, the prior art reference must necessarily disclose the limitation, and the fact that the reference might possibly practice or possibly contain a claimed limitation is insufficient to establish that the reference inherently teaches the limitation.

C. Obviousness

25. I understand that a claim is unpatentable if it would have been obvious to a person of ordinary skill in the art at the time the invention was made. I understand that a claim could have been obvious from a single prior art reference or from a combination of two or more prior art references. I understand that an obviousness analysis requires an understanding of the scope and content of the prior art, any differences between the invention and the prior art, and the level of ordinary skill in evaluating the pertinent art.

26. I further understand that a claim would have been obvious if it unites old elements with no change to their respective functions or alters prior art by mere substitution of one element for another known in the field, and that combination yields predictable results. Also, I understand that obviousness does not require physical combination or bodily incorporation, but rather consideration of what the combined teachings would have suggested to persons of ordinary skill in the art at the time of the invention.

27. While it may be helpful to identify a reason for this combination, I understand that there is no rigid requirement of finding an express teaching, suggestion, or motivation to combine within the references. When a product is available, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill in the art can implement a predictable variation, obviousness likely bars its patentability. For the same reason, if a technique has been used to improve one device and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique would have been obvious. I understand that a claim would have been obvious if a person of ordinary skill in the art would have had reason to combine multiple prior art references or add missing features to reproduce the invention recited in the claims.

28. I further understand that certain factors may support or rebut the obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the invention, the failure of others to make the invention, praise of the invention by those having ordinary skill in the art, and copying of the invention by others in the field. I

understand that there must be a nexus, that is, a connection, between any such secondary considerations and the invention.

29. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

D. Claim Dependency

30. I understand that a patent may include two types of claims, independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim or another dependent claim. I understand that a dependent claim includes all the limitations that it recites in addition to all of the limitations recited in the claim from which it depends.

VI. THE '378 PATENT

A. Overview of the '378 Patent

31. The claimed invention of the '378 is directed to a “three-dimensional (3D) memory device” and related methods that address issues arising from the fabrication techniques known in the prior art and as a result, “simplif[ies] the fabrication process and reduce[s] the fabrication cost.” '378, Abstract, 18:36-41.

32. Specifically, the '378 is directed to an improved 3D memory device and methods for forming such a device in which “through array contacts (TACs)”

“extend vertically through” the “dielectric structure” and the “isolation structure.” Ex. ’378, Abstract, 10:57-59, 21:17-25. 3D memory devices in the prior art at the time of filing of the ’378 involved through array vias that form connections between various components of the device in order to reduce the size and increase density. ’378, 1:20-32. These vias were placed within the regions of the alternating dielectric and conductive layer stacks, which required a complex etching process and “increase[d] the fabrication cost.” ’378, 10:59-66.

33. The novel device and methods the ’378 teaches and recites in the claims is characterized by “a **substrate** with an **isolation structure**” and **TACs** that “extend vertically through” the “**dielectric structure**” and the “**isolation structure**.” ’378, Abstract, 10:57-59, 21:17-25, Claim 15. This novel configuration of elements allows for easier and less costly manufacture of 3D memory devices. ’378, 5:55-59, 18:27-33, 20:29-37.

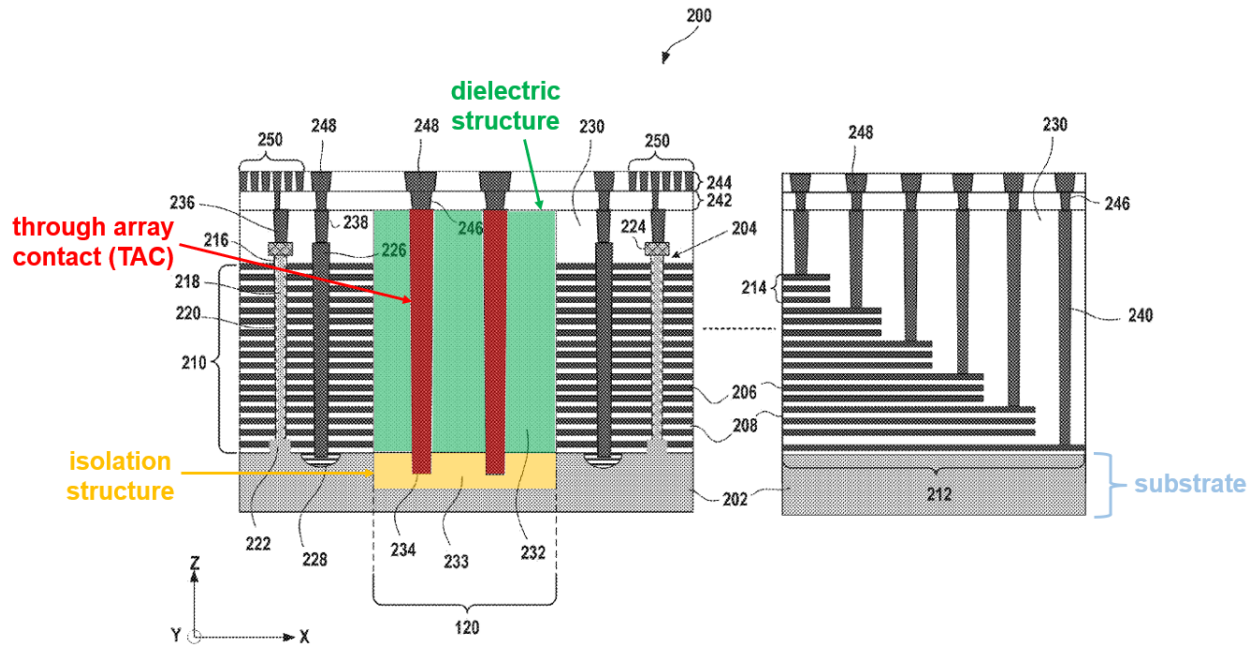


FIG. 2

'378, Fig. 2 (annotated).

34. A representative embodiment of the '378's memory device includes:

- (1) "substrate 202" with "isolation structure 233" ('378, 10:30-35, 22:27-38); (2) "alternating conductor/dielectric layer stack 210" ('378, 8:17-25); (3) "dielectric structure 232" on "isolation structure 233" ('378, 10:18-29); (4) "channel structures 216" and "slit structures 226" extending vertically through "alternating conductor/dielectric layer stack 210" ('378, 9:1-6, 10:1-6); (5) "staircase structure 212" ('378, 8:48-55); (6) "word line contacts 240" (11:24-26); (7) "local contacts" on "channel structures 216" and "slit structures 226" (11:24-26); and (8) "TACs 234" extending vertically through "dielectric structure 232" and "isolation structure 233" ('378, 10:57-59, 20:45-48). A cross-section view of the memory device is below.

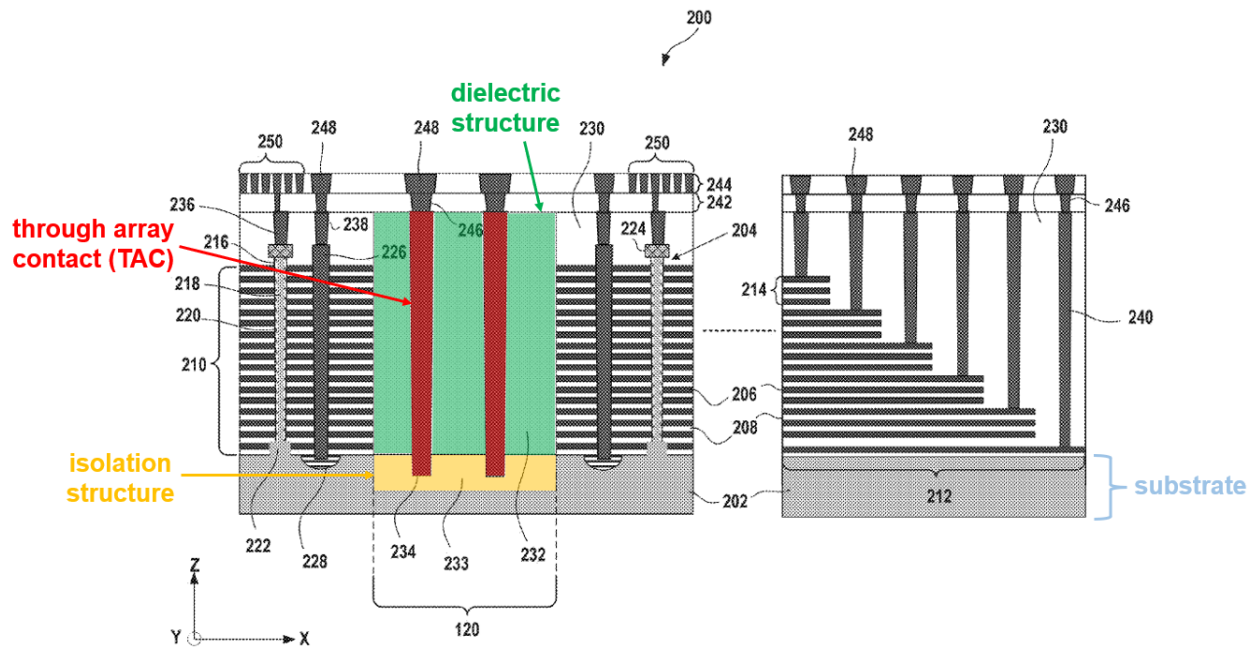


FIG. 2

'378, Fig. 2 (annotated).

B. Listing of the Challenged Claims

35. For reference, claims 15-17, 19-20 ("Challenged Claims") of the '378 Patent are reproduced below:

[15.pre] A three-dimensional (3D) memory device, comprising:

[15.a] a substrate with an isolation structure;

[15.b] an alternating conductor/dielectric layer stack disposed on the substrate;

[15.c] a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

[15.d] channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;

[15.e] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

[15.f] a word line contact disposed on the conductor layer of the each level;

[15.g] local contacts disposed on the channel structures and the slit structures; and

[15.h] through array contacts (TACs) extending vertically through the dielectric and the isolation structures.

[16] The 3D memory device of claim 15, wherein the dielectric structure abuts a sidewall of each TAC of the TACs.

[17] The 3D memory device of claim 15, wherein the dielectric structure comprises a through array contact region of the 3D memory device.

[19] The 3D memory device of claim 15, wherein the dielectric material comprises silicon oxide.

[20] The 3D memory device of claim 15, wherein the TACs comprise a conductive material.

C. File History of the '378 Patent

36. The '378 was filed on July 27, 2018. After a preliminary amendment where Applicant filed to remove multiple claim dependency and correct a typographical error, the application included 3 independent claims (pending claims 1, 10, and 16) and 17 dependent claims (pending claims 2-9 which depend from claim 1, claims 11-15 which depend from claim 10, and claim 17-20 which depend from claim 16). Ex. 1002, 105-111 (12/06/2018 Preliminary Amendment).

37. In a non-final office action, the Examiner rejected pending claims 1, 3-16, and 18-20 under 35 U.S.C. §103 as being allegedly obvious over U.S. Patent 9,620,512 (“Nishikawa”) in view of U.S. Patent Publication No. 2016/0056188 (“Lee”), but found that pending claims 2 and 17 “would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.” Ex. 1002, 529-537 (08/22/2019 Office Action).

38. Applicant followed the Examiner’s suggestion “[w]ithout acquiescing to the propriety of the rejection” and rewrote pending claims 2 and 17 in independent form. Applicant also amended pending claim 10 “[w]ithout acquiescing to the propriety of the rejection” to “recite features that further distinguish it from Nishikawa and Lee.” Ex. 1002, 569 (12/23/2019 Amendment and Reply). Having placed the independent claims in allowable form, Applicant requested that their respective dependent claims also be allowed. Applicant further added two new claims that depend from pending claim 16. Ex. 1002, 563-571 (12/23/2019 Amendment and Reply). The Examiner subsequently allowed all pending claims. Ex. 1002, 579-586 (01/13/2020 Notice of Allowance). The ’378 issued on May 19, 2020 with twenty claims, including the renumbered independent claims 1, 9, and 15. Ex. 1002, 602 (04/29/2020 Issue Notification).

39. After the first office action and before Applicant’s response, Applicant filed an information disclosure statement (IDS) that notified the Examiner of U.S.

Patent Publication No. 2017/0179026 (“Toyama”). Ex. 1002, 555 (12/03/2019 Information Disclosure Statement). The Examiner considered Toyama and explicitly cited it as a “reference[] considered.” Ex. 1002, 593 (01/13/2020 List of References Cited by Applicant and Considered by Examiner). I disagree with Petitioner’s assertion that “Patent Owner only gave Examiner a haystack” because Applicant submitted an IDS solely to cite Toyama, which was then considered by the Examiner. Moreover, the ’378 was issued with only sixteen references (nine U.S. patent documents and six foreign patent documents) one of which is Toyama. ’378, (56). Thus, the Examiner considered Toyama, but found it lacking.

VII. LEVEL OF ORDINARY SKILL IN THE ART

40. My opinions in this declaration are based on the understandings of a person of ordinary skill in the art, which I understand is sometimes referred to as an “ordinary artisan” or by the acronyms “POSITA” (person of ordinary skill in the art) or “POSA,” as of the time of the invention.

41. I have been asked to consider the level of ordinary skill that someone in the field of technology of the ’378 patent would have had at the time the claimed invention disclosed in the ’378 patent was made. In determining the level of ordinary skill in the art, I considered the following: (1) the levels of education and experience of persons working in the field; (2) the types of problems encountered in the field; and (3) the sophistication of the technology.

42. In my opinion, a person of ordinary skill in the art capable of reading and understanding the claims of the '378 patent at the time of the invention would have had at least a bachelor's degree in electrical engineering, materials science, or a similar discipline, along with at least 2 years of professional experience in semiconductor fabrication process integration for memory devices or an equivalent level of knowledge and experience. For example, an advanced degree may replace some of the professional experience, or extensive experience may replace some of the educational requirements.

43. In this case, Dr. Lee has asserted in his declaration that a person of ordinary skill in the art at the time of the invention described in the '378 patent:

would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

Lee, ¶36.

44. In view of my educational background and years of experience, including my many years of experience designing high performance integrated circuits and developing advanced semiconductor manufacturing process technology for advanced DRAM, CMOS image sensors, and NAND flash, I both met and exceeded the qualifications of a person of ordinary skill in the art as of the earliest possible priority date of the '378 Patent in May 2018. That is true under both my

own definition of a person of ordinary skill in the art, as well as under Dr. Lee's definition, and my opinions as set forth herein are the same regardless of which definition of a person of ordinary skill in the art is applied.

VIII. CLAIM CONSTRUCTION FOR THE '378 PATENT

45. I have been asked to opine on the scope and content of the '378 patent and what a person of ordinary skill in the art would have understood the '378 patent to disclose and teach as it relates to the terms "a dielectric structure on the isolation structure," "a substrate with an isolation structure," "the dielectric and the isolation structures," and "the dielectric structure comprises a through array contact region of the 3D memory device."

A. "a dielectric structure on the isolation structure" (Claim 15)

46. The term "on" should be construed consistent with its plain and ordinary meaning to mean "above" in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction. As confirmed by the '378, the term does not permit reorienting the direction of the "on" spatial relationship to encompass any relative position.

47. Both in the claims and specification, the term "on" is used to indicate a specific spatial relationship between the isolation structure and substrate, or the dielectric structure and the isolation structure, in which the former structure is above the latter. The claims consistently use the term "on" to refer to above (e.g., "a

dielectric structure on the isolation structure” as recited in claim 15) and use the different term “abut” to refer to the lateral direction (e.g., “the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure” as recited in claim 15).

48. The specification expressly defines the term consistent with its plain and ordinary meaning:

As used herein, whether one component (e.g., a layer or a device) is “**on**,” “above,” or “below” **another component** (e.g., a layer or a device) **of a semiconductor device** (e.g., 3D memory device 200) **is determined relative to substrate 202 in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction.**

’378, 7:37-43. The specification likewise describes and shows the dielectric structure as above the isolation structure (and the isolation structure as above the substrate). For example, Figure 2 shows the dielectric structure above the isolation structure:



49. Patent Owner's construction is also consistent with the vertically-oriented description of the '378's claimed "three-dimensional (3D) memory device." The "three-dimensional (3D) memory device" of the claim is described as "refer[ring] to a semiconductor device with vertically-oriented strings of memory cell transistors (referred to herein as "memory strings," such as NAND strings) **on** a

laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate.” ’378, 5:24-29. The patent explains that “the term ‘vertical/vertically’ means nominally perpendicular to the lateral surface of a substrate.” *Id.*, 5:29-31; *see also* Ex. 2007 (Depo. Tr. of Dr. Lee (Petitioner’s expert)), 64:5-12 (“‘Vertically’ means 90 degree with respect to the orientation of the substrate.”). Therefore, in the context of the ’378, a component being on another component requires the former to be vertically above the latter, where the vertical direction is the direction perpendicular to the substrate.

50. In contrast, the ’378 uses the terms “abut” and “on the side” to indicate a horizontal spatial relationship. For example, the alternating dielectric/conductor stack “abuts” a sidewall of the dielectric structure. ’378, 20:42-45. While “on the side” includes the word “on” and refers to a horizontal spatial relationship, the term “on” by itself is never used to indicate a lateral or other relationship besides above.

51. I respectfully disagree with the Board’s preliminary conclusion in its Decision to Institute (“DI”) that the device may be reoriented for purposes of determining whether an alleged isolation structure is on the substrate. The Board cites disclosures from the ’378 and preliminarily concludes that “a structure will be considered to be on the substrate even if it is not on the substrate in the displayed orientation so long as it is on the substrate in any possible rotation.” DI, 12-13 (citing ’378, 4:34-40). The cited passage states:

The spatially relative terms are intended to encompass ***different orientations of the device in use or operation*** in addition to the orientation depicted in the figures. ***The apparatus may be otherwise oriented*** (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

'378, 4:34-40.

52. This passage merely ensures that the orientation of ***the entire device*** (***“the apparatus”***) may be rotated ***“in use or operation”*** while remaining within the scope of the claims—it does not change the claimed relative spatial relationships between the components within the device. This is also consistent with how the vertical direction is used within the '378 as the direction perpendicular to the substrate. For example, if the entire vertically-oriented memory device shown in Fig. 2 were rotated 90 degrees, the dielectric structure is still above the isolation structure, and the isolation structure is still above or substrate, because the vertically-oriented direction has been rotated by 90 degrees along with the substrate. As this example illustrates, ***the device itself has not changed, and the same isolation structure is still “on” the substrate***. The word “on” is “interpreted accordingly” to account for the rotation and the vertically-oriented direction of the whole 3D memory cell device.

53. The disclosure does not imply that any two components can have any relative spatial configuration and still be “on” each other, as the Board’s

interpretation would allow—that interpretation would be so broad so as to render the term “on” superfluous. I note that Petitioner’s expert, Dr. Lee, has agreed that this interpretation is so broad that “any layers or any structure in the device perhaps can be considered on other layers or any structures of the devices.” Ex. 2007, 45:10-47:5; *see generally* Ex. 2007, 33:1-47:5. Such an interpretation would also render the patentee’s choice of terms such as “on” or “abut” meaningless.

54. Furthermore, this interpretation would contradict the specification’s consistent use of “on” to describe the spatial position of relevant structures in the vertically-oriented direction of the 3D memory cell device, as discussed above. Spatial terms such as “on” are crucial in properly describing how a memory device is fabricated and how the various components are configured spatially. The specification describes the invention so that all the components are spatially placed and configured correctly to have a functional device.

55. Petitioner’s expert, Dr. Lee, has taken inconsistent positions when it comes to spatial terms. On the one hand, Dr. Lee purports to agree with the Board’s conclusion that spatial terms like “on” can be ignored by random reoriented; on the other hand, he interprets several other spatial terms with definitive orientations. For example, Dr. Lee explains that a “side wall” of a dielectric structure is not just any surface of the dielectric structure, but must be one specific surface that is defined by its spatial geometry. *See* Ex. 2007, 62:13-63:7 (“[T]he side wall is between structure

210 and insulating layer 232 as the side wall, that is the side wall surface of the dielectric structure”). Similarly, Dr. Lee explains that “vertically” in the claims “means 90 degree[s] with respect to the orientation of the substrate.” *Id.* 64:5-12. If Dr. Lee followed his own approach in defining these spatial terms, he would not have interpreted the term “on” to mean any reorientation.

56. Thus, the term “on” should be construed as “above” or “on top off” in a vertical direction relative to the lateral surface of the substrate. The term does not permit reorienting the direction of the “on” spatial relationship to encompass any relative position.

B. “a substrate with an isolation structure” (Claim 15)

57. The term “a substrate with an isolation structure” should be construed as requiring that *the isolation structure is “part of” the substrate.*

58. The ’378 claims support the construction that the isolation structure is “part of” the substrate. Rather than listing the “isolation structure” as its own claim limitation, the “isolation structure” is introduced only in reference to the recited substrate. Specifically, claim 15 recites “a substrate with an isolation structure.”

59. The ’378 specification also supports the construction that the isolation structure is “part of” the substrate. The ’378 consistently depicts the isolation structure as a region in the upper portion of the substrate, for example as shown in Figure 2:

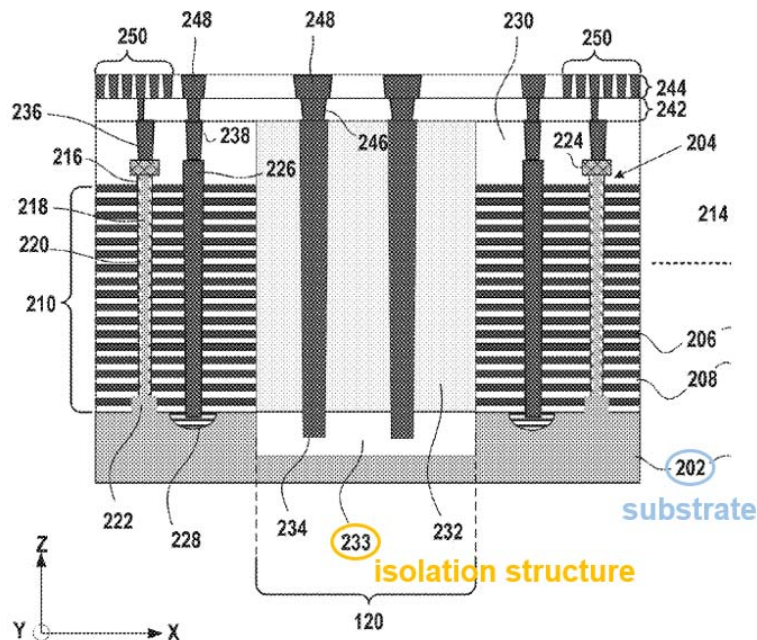


FIG. 2

'378, Fig. 2 (annotated and excerpted); *see also* '378, Figs. 4-13. Specifically, the '378 depicts a shallow region in the upper portion of the substrate (see Fig. 2, above). An example of the isolation structure in the '378 is “shallow trench isolation (STI).” '378, 10:30-43, 12:64-13:3, 14:46-15:32.

60. The '378 consistently describes the isolation structure as part of the substrate. *See* '378, 12:54-66 (“According to some embodiments, **substrate 202 includes isolation regions or structures**, like STI structure 233 shown in FIG. 4.”), 20:38-42 (“In some embodiments, a 3D memory device includes a semiconductor substrate, an alternating layer stack disposed on the semiconductor substrate, and a dielectric structure, extending vertically through the alternating layer stack, on **an isolation region of the substrate**”), 21:7-13 (“In some embodiments a method for

forming 3D memory device includes forming ***an isolation structure on a substrate***, disposing an alternating dielectric layer stack on the substrate, where the alternating dielectric layer stack includes pairs of a first dielectric layer and a second dielectric layer different from the first dielectric layer.”), 21:64 (“an isolation region in the substrate”), 22:27-28 (“In some embodiments, a 3D memory device includes ***a substrate with an isolation structure***”) (emphasis added).

61. The Board agreed in its Institution Decision that the isolation structure is part of the substrate (DI, 12-13), but took the position that an isolation structure could be located in any position relative to the substrate. In my opinion, the Board’s statements are contrary to the ’378 specification, which does not support an interpretation that “any “additional layers or structures added or disposed” on the substrate “could be considered part of, or ‘with’ the substrate,” where “a layer is disposed on the substrate if it is on the substrate in any orientation, including by rotation of the device.” DI, 12-13.

62. ***First***, the Board’s interpretation that “part of” includes structures that are merely “on” the substrate is inconsistent with the claim language, which specifically invokes the term “with” (i.e., part of) rather than “on.” Indeed, the Board’s interpretation would lead to the absurd result that any components or layers positioned “on” the substrate would become “part of” the substrate such that the entire memory device would be subsumed by this unreasonably broad interpretation.

For example, the alternating conductor/dielectric layer stack is disposed “on” the substrate (’378, Abstract, 22:27-29), which under the Board’s interpretation, would somehow become a **part of** the substrate.

63. The Board quotes a passage from the specification states that an “STI structure 233 is formed on a top portion of substrate 202 and filled with a dielectric material” (DI, 12 (citing ’378, 10:30)), but in the context of this discussion, “on a top portion of the substrate” is referring to removing a part of the substrate, which is then “filled with a dielectric material,” so as to form the “STI structure” “on a top portion of the substrate.” ’378, 10:30-44. Thus, this teaching of the specification supports the claim’s recitation of “with” (i.e., part of) instead of “on,” consistent with the other portions of the specification discussed above. Nothing in the specification suggests that the STI structure is merely “on” the substrate.

64. **Second**, even if the “with” relationship encompassed the “on” relationship as preliminarily concluded by the Board (it does not), “on” means “above” in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction, and the ’378 does not permit reorienting the direction of the “on” spatial relationship to encompass any relative position. See my discussion of “on” above in connection with “a dielectric structure on the isolation structure,” where I discuss this issue.

65. Thus, the term “a substrate with an isolation structure” should be construed as requiring that the isolation structure is “part of” the substrate. The term does not encompass structures that are merely positioned “on” the substrate, and even if did, that would not permit reorienting the direction of the “on” spatial relationship to encompass any relative position.

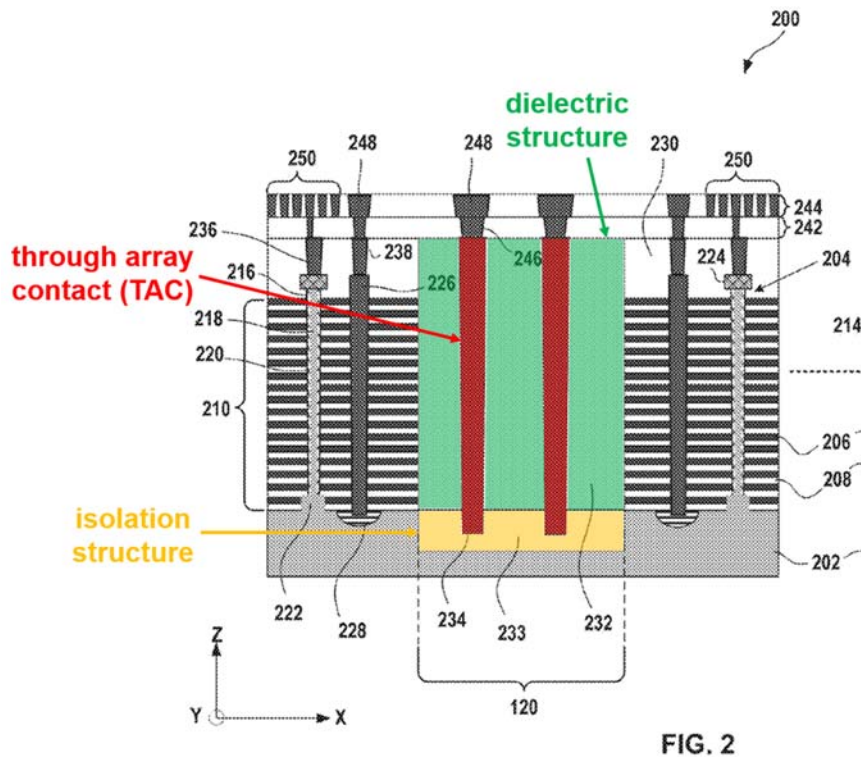
C. “the dielectric and the isolation structures” (Claim 15)

66. The phrase “the dielectric and the isolation structures” in “through array contacts (TACs) extending vertically through the dielectric and the isolation structures” should be construed, consistent with its antecedent terms, as “the dielectric structure and the isolation structure.” In other words, the term refers back to the same “dielectric structure” and the same “isolation structure” recited earlier in the claim.

67. The phrase “the dielectric and the isolation structures” in [15.h] has its antecedent basis in “a dielectric structure” and “an isolation structure” from [15.a] and [15.c], confirming that the phrase is simply shorthand for “the dielectric structure” and “the isolation structure.” There are no other terms in the claim, aside from “a dielectric structure” and “an isolation structure,” that could provide the necessary antecedent basis for “the dielectric and the isolation structures.”

68. The claim language is plural (“structures”) because it refers to both the isolation structure and the dielectric structure (“the dielectric and the isolation

structures”), not because the term may be referring to multiple dielectric structures or multiple isolation structures. An example of the claimed configuration is shown in Fig. 2 of the ’378.



’378, Fig. 2 (annotated and excerpted). As shown in the figure, a plurality of TACs extend through the same dielectric structure and the same isolation structure.

69. While the claims do not preclude multiple dielectric structures or multiple isolation structures, the limitation “through array contacts (TACs) extending vertically through the dielectric and the isolation structures” requires that the plurality of TACs extend through at least one particular dielectric structure and one particular isolation structure—i.e., the previously recited dielectric structure and

isolation structure—regardless of whether additional dielectric structure or isolation structures are also present in the device.

70. In my opinion, the Board’s preliminary analysis in its Institution Decision misinterprets the claim language. The Board concluded:

Limitation [15.H] requires TACs (multiple) extending through “the dielectric and the isolation structures” (multiple). Being plural, the phrase “the dielectric and the isolation structures” is not limited to a single dielectric and a single isolation structure; it may include multiple dielectric structures and/or multiple isolation structures.

DI, 23. As discussed above, the claims and specification support construing this term as referring to the same specific dielectric structure and isolation structure previously recited in the claim, rather than multiple dielectric structures and/or multiple isolation structures. For example, the claims would not encompass each of the TACs extending through different dielectric structures instead of the same dielectric structure.

71. I disagree with the Board’s reliance on what it describes as a disclosure of “a single TAC extending through a single respective dielectric structure” (DI, 23 (citing ’378, 21:17–25)). The cited passage states:

The method also includes filling the opening with a dielectric layer to form a dielectric structure as a TAC region of the 3D memory device, removing portions of the dielectric structure and the isolation structure until the substrate is exposed to form a TAC opening that vertically extends through the dielectric structure and the isolation structure, and filling the TAC opening with a conductor to form a TAC structure in the TAC region, wherein the TAC structure is in contact with the substrate.

'378, 21:17–25. This passage describes the formation of a single TAC, not a plurality of TACs that extend through the dielectric structure and the isolation structure as claimed. The cited passage does not support an interpretation that each TAC in a group of TACs may extend through separate, discontinuous dielectric structures. As discussed above, the specification consistently describes and depicts the ***plurality of TACs*** as extending through the same dielectric structure. Regardless, even if the Board's interpretation of this passage were correct (I disagree with that interpretation), I understand that a claim need not be construed to encompass all disclosed embodiments. As I have explained, claim 15 is directed to a plurality of TACs that extend through a dielectric structure, for example as shown in Fig. 2 of the '378.

72. Under the correct interpretation of “the dielectric and isolation structures” as “the dielectric structure and the isolation structure,” limitation [15.h] requires that multiple TACs extend through a single dielectric structure. Here, the claim requires that a single “dielectric structure” must have multiple “through array contacts (TACs) extending vertically through” it.

D. “the dielectric structure comprises a through array contact region of the 3D memory device” (Claim 17)

73. The term “through array contact region” in the limitation “the dielectric structure comprises a through array contact region of the 3D memory device” should be construed as “a region that is within or defined by the dielectric structure and

which includes the through array contacts extending through the dielectric structure.”

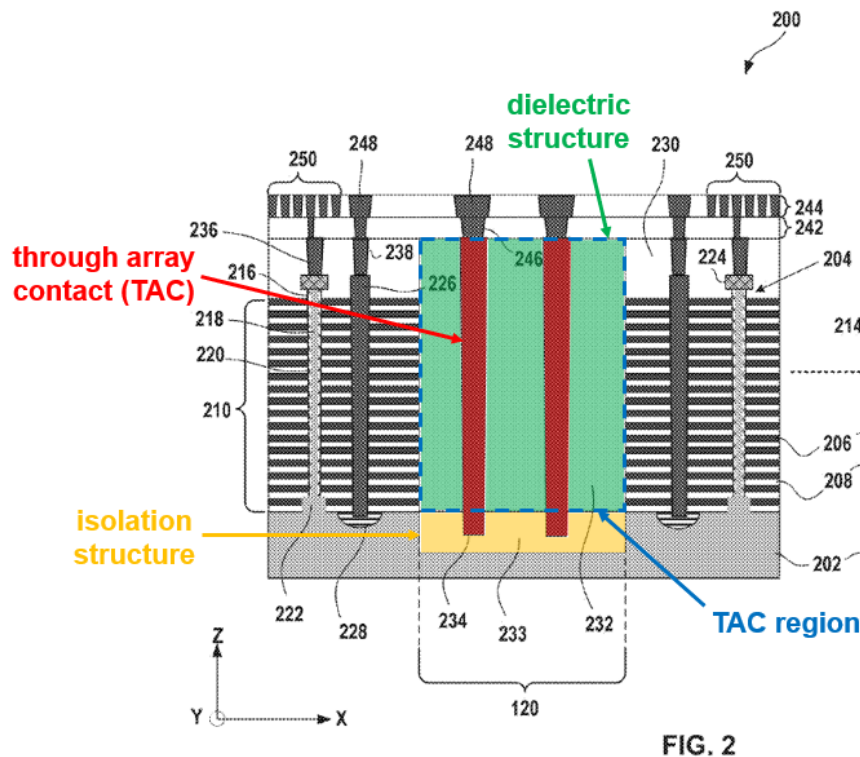
Thus, because the dielectric structure extends through the alternating conductor/dielectric layer stack (independent claim 15), and the through array contact region (“TAC region”) is within or defined by the dielectric structure, the TAC region cannot include the alternating conductor/dielectric layer stack. This interpretation is supported by the claims and specification.

74. Claim 17 recites that “the dielectric structure comprises a through array contact region,” which indicates that the TAC region is nested within the dielectric structure, or at most is coextensive with the dielectric structure. If the TAC region were larger than the dielectric structure, then the TAC region would comprise the dielectric structure instead of the other way around.

75. In addition, Patent Owner’s construction—which provides a limit to the scope of the claimed region—is the only one that gives meaning to the term “through array contact region” in the claims. Independent claim 15 from which claim 17 depends already requires TACs to extend through the dielectric structure, and thus “through array contact region” must have some additional meaning, which Patent Owner’s construction provides.

76. The ’378 discloses a few embodiments of a TAC region, and in all of them the TAC region is within or defined by the dielectric structure and includes the TACs and the dielectric structure through which they extend. ’378, 6:11-16 (“In

some embodiments, TAC region 120 is between two TSG staircase regions 130 in the WL direction of the 3D memory device. ***TAC region 120 can be defined by a single-material dielectric structure 124. Multiple TAC structures 126 can be formed within TAC region 120 in dielectric structure 124.***) (emphasis added), 10:21-24 (“In some embodiments, ***dielectric structure 232 defines the boundaries, the shape, and the size of TAC region 120*** (e.g., shown in FIGS. 1A-1C).”), Figs. 1A-1C, 2; see also ’378, 5:60-7:4.



’378, Fig. 2 (annotated and excerpted). In addition, in every embodiment of ’378, the dielectric structure includes only TACs extending through it and does not include, for example, the alternating conductor/dielectric layer stack.

77. Thus, the term “through array contact region” in “the dielectric structure comprises a through array contact region of the 3D memory device” should be construed as “a region that is within or defined by the dielectric structure and which includes the through array contacts extending through the dielectric structure.” The TAC region does not include the alternating conductor/dielectric layer stack.

IX. THE ASSERTED PRIOR ART

A. U.S. Patent Publication No. 2017/0179026 (“Toyama”) (Ex. 1005)

78. Petitioner does not argue that Toyama anticipates the Challenged Claims, and instead argues only that it renders obvious the Challenged Claims in view of the knowledge of a person of ordinary skill in the art. Pet. 6, 28-77.

79. Toyama teaches a 3D NAND memory device with four exemplary structures and their modifications. Ex. 1005, [0004]. Only two of these exemplary structures are relied on by Petitioner: (1) “the ‘first exemplary structure,’ illustrated in Figures 1A-B to 17A-F,” and (2) “the ‘second modification of the fourth exemplary structure,’ illustrated in Figures 44A-B to 49.” Pet. 25.

80. Toyama’s first exemplary structure includes, among other elements: “**semiconductor substrate 9**” (Ex. 1005, [0163]); “**planar semiconductor material layer 10**” (Ex. 1005, [0170]); “**alternating stack (132, 146, 232, 246)**” (Ex. 1005, [0232]); “**channels**” (Ex. 1005, [0211]); “**laterally-elongated contact via structures 76**” (Ex. 1005, [0236]); “**drain contact via structures 88**” (Ex. 1005,

[0241]); “**source connection via structures 91**” (Ex. 1005, [0250]); “**dielectric fill material portion 430**” (Ex. 1005, [0216]); and “**through-memory-level via structures 488**” (Ex. 1005, [0244]). A cross-section view of Toyama’s first exemplary structure is below.

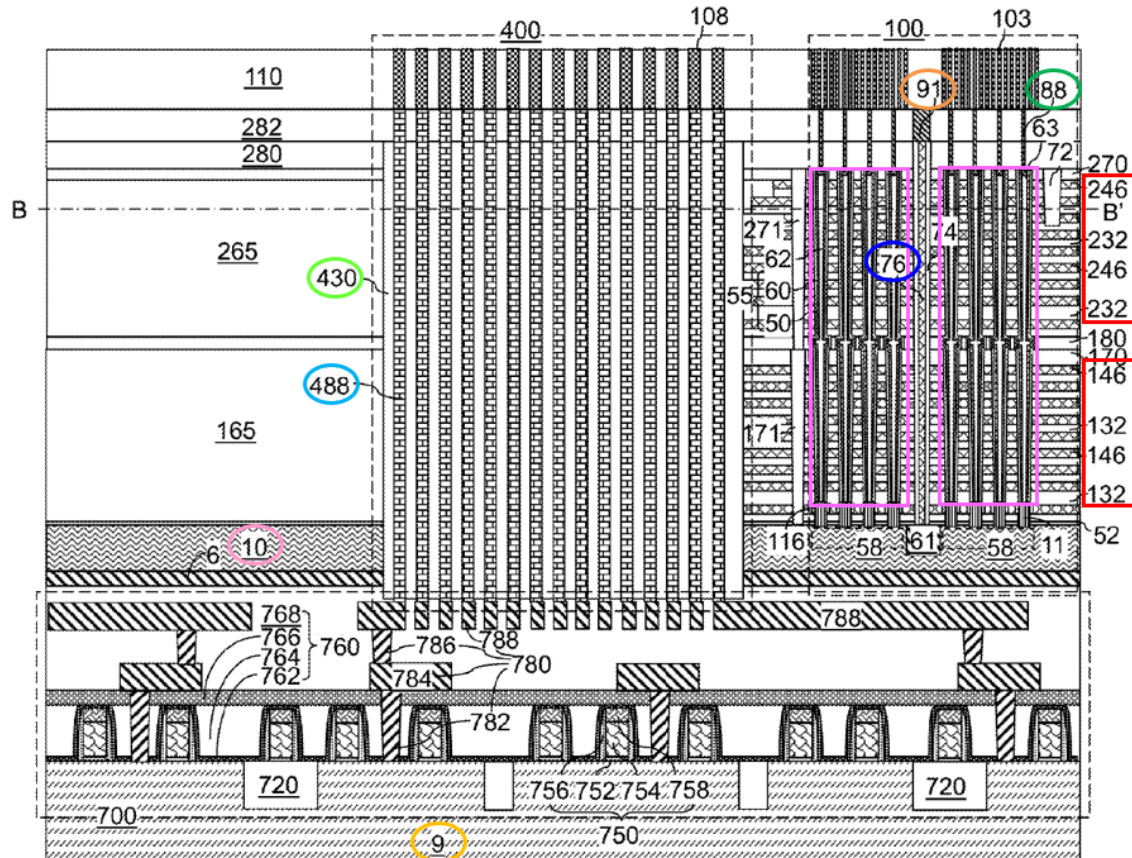


FIG. 17A

Ex. 1005, Fig. 17A (annotated).

81. In Toyama’s first exemplary structure, **dielectric fill material portion 430** forms a hole in **planar semiconductor material layer 10**, which allows **through-memory-level via structures 488** to form vertical interconnects. Toyama’s **planar semiconductor material layer 10** lacks the claimed isolation

structure. While Toyama's **semiconductor substrate 9** seems to comprise "shallow trench isolation structures 720," they do not host **through-memory-level via structures 488** or similar via structures.

82. Toyama's second modification of the fourth exemplary structure includes, among other elements: "**semiconductor substrate 9**" (Ex. 1005, [0163]); "**planar semiconductor material layer 10**" (Ex. 1005, [0170]); "**alternating stack (132, 146, 232, 246)**" (Ex. 1005, [0232]); "**channels**" (Ex. 1005, [0211]); "**laterally-elongated contact via structures 76**" (Ex. 1005, [0236]); "**drain contact via structures 88**" (Ex. 1005, [0241]); "**insulating liners 674**" (Ex. 1005, [0340]); and "**through-memory-level via structure 676**" (Ex. 1005, [0341]). A cross-section view of Toyama's second modification of the fourth exemplary structure is below.

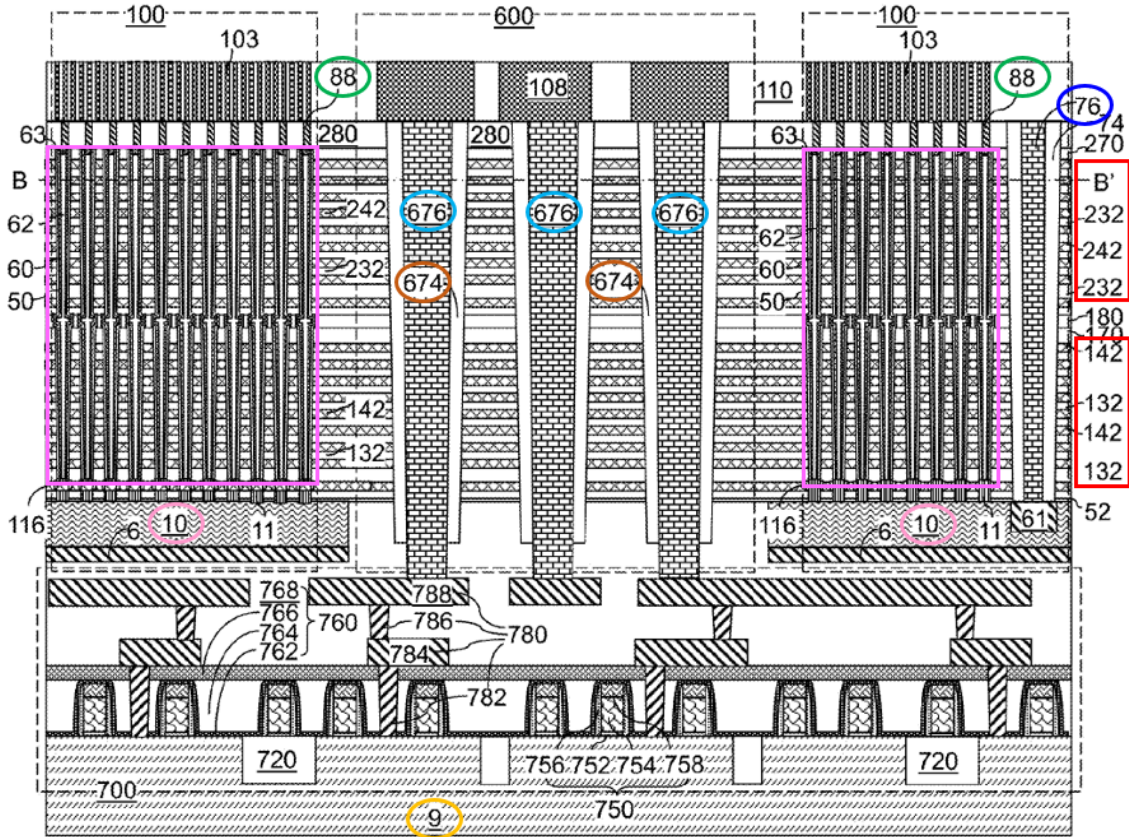


FIG. 49

Ex. 1005, Fig. 49 (annotated). (Note that Petitioner states: “In a clear typographical error, Figure 49 labels its alternating conductor/dielectric layer stack as elements 132, 142, 232, 242. Elements 142, 242 are ‘sacrificial material layers’ which, in a process step prior to Figure 49, were removed and replaced with ‘electrically conductive layers (146, 246).’ Toyama, [0337], [0340].” Pet. 39. I do not challenge this statement for purposes of this declaration.)

83. In Toyama's second modification of the fourth exemplary structure, Toyama's **planar semiconductor material layer 10** again lacks an isolation structure. In addition, **through-memory-level via structures 676** are not formed

through a dielectric structure; instead, they are formed through **alternating stack (132, 146, 232, 246)** and as a result, they require separate **insulating liners 674** around each individual **through-memory-level via structure 676**.

B. U.S. Patent No. 10,354,980 (“Mushiga”) (Ex. 1006)

84. Petitioner does not argue that Mushiga anticipates the Challenged Claims, and instead argues only that it renders obvious the Challenged Claims in view of the knowledge of a person of ordinary skill in the art, alone or in combination with Makala. Pet. 7, 77-105.

85. Mushiga’s 3D NAND memory device includes, among other elements: “**first substrate semiconductor layer 9**” (Ex. 1006, 7:34-44); “**semiconductor material layer 10**” (Ex. 1006, 9:8-14); “**alternating stack (132, 146, 232, 246)**” (Ex. 1006, 10:31-38); “**channels**” (Ex. 1006, 9:50-67); “**backside contact via structures 76**” (Ex. 1006, 10:1-18); “**drain contact via structures 88**” (Ex. 1006, 10:19-30); “**insulating spacers 586**” (Ex. 1006, 10:31-46); and “**through-memory-level via structure 588**” (Ex. 1006, 10:42-57). A cross-section view of Mushiga’s device is below.

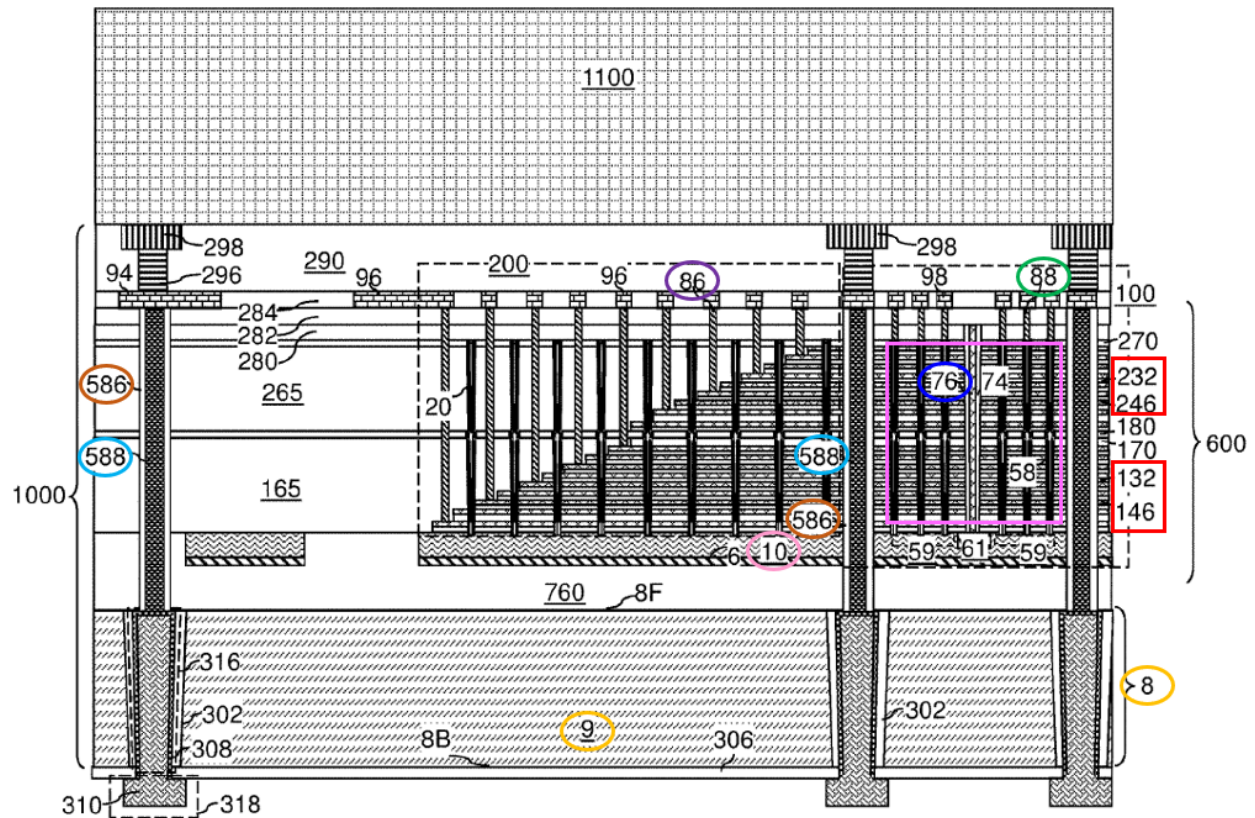


FIG. 11

Ex. 1006, Fig. 11 (annotated).

86. Mushiga's semiconductor material layer 10 and substrate semiconductor layer 9 lack the claimed isolation structure. In addition, in Mushiga, some through-memory-level via structures 588 are placed outside the array, such as the one on the left in Fig. 11 above. For the ones placed inside the array, there is no dielectric structure in a dedicated region for forming through-memory-level via structures 588; instead, they are formed through alternating stack (132, 146, 232, 246) and as a result, they require separate insulating spacers 586 around each individual through-memory-level via structure 588.

C. U.S. Patent No. 10,262,945 (“Makala”) (Ex. 1007)

87. Petitioner does not argue that Makala anticipates the Challenged Claims, and instead argues only that it renders obvious the Challenged Claims in view of the knowledge of a person of ordinary skill in the art in combination with Mushiga. Pet. 7, 102-105.

88. Makala’s 3D NAND memory device includes, among other elements: “**substrate semiconductor layer 9**” (Ex. 1007, 4:53-61); “**planar semiconductor material layer 10**” (Ex. 1007, 17:10-40); “**alternating stack (132, 146, 232, 246)**” (Ex. 1007, 32:8-30); “**channels**” (Ex. 1007, 24:25-43); “**backside contact via structures 76**” (Ex. 1007, 33:4-29); “**drain contact via structures 88**” (Ex. 1007, 33:37-43); “**source connection via structures 91**” (Ex. 1007, 34:27-34); and “**through-memory-level via structure 488**” (Ex. 1007, 34:12-16). A cross-section view of Makala’s device is below.

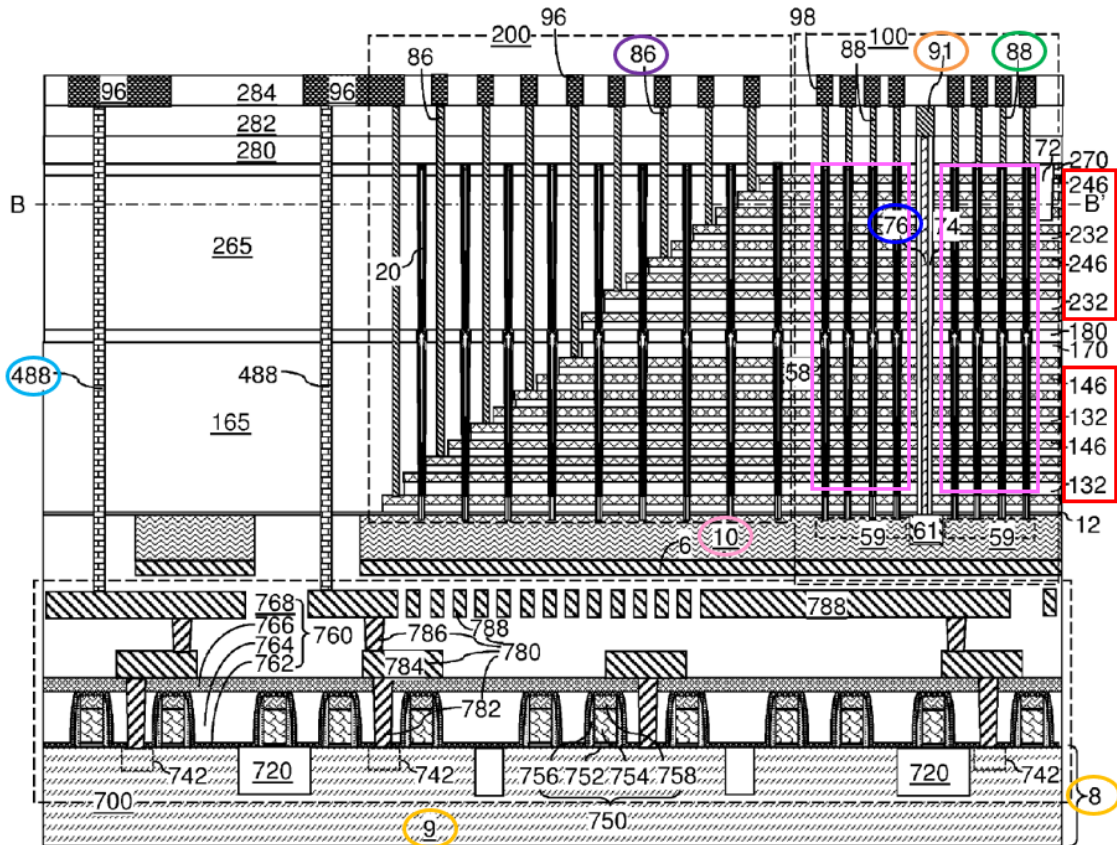


FIG. 16

Ex. 1007, Fig. 16 (annotated).

89. Petitioner relies on Makala only for its disclosure of **source connection via structures 91**. The teachings of Makala are not relevant to any issues raised in this declaration.

X. PETITIONER’S GROUND 1A: TOYAMA’S FIRST EXEMPLARY STRUCTURE DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 15-17 AND 19-20

90. For the reasons explained below, it is my opinion that Toyama's First Exemplary Structure does not disclose or render obvious the Challenged Claims at least because Toyama's First Exemplary Structure does not disclose or render

obvious multiple elements of claim 15—the sole independent claim. For example, Toyama’s First Exemplary Structure does not disclose or render obvious “a substrate with an isolation structure.” Toyama’s First Exemplary Structure also does not disclose or render obvious “a dielectric structure on the isolation structure.” Toyama’s First Exemplary Structure further does not disclose or render obvious “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.” Finally, for claim 17, Toyama’s First Exemplary Structure does not disclose or render obvious “the dielectric structure comprises a through array contact region of the 3D memory device.”

A. Independent Claim 15: Toyama’s First Exemplary Structure Does Not Disclose Or Render Obvious Limitations [15.a], [15.c.i], and [15.h]

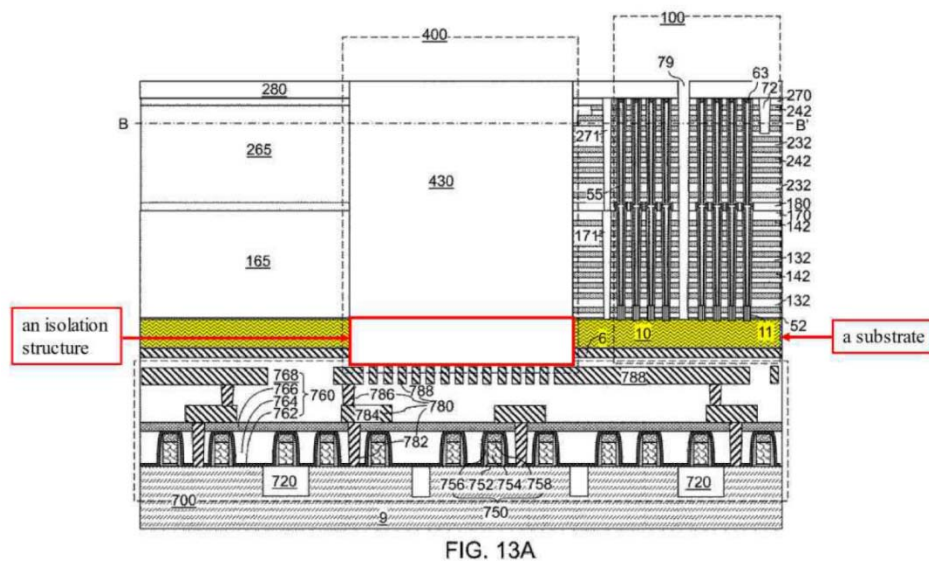
(a) Toyama’s First Exemplary Structure Does Not Disclose or Render Obvious “a substrate with an isolation structure” (Limitation [15.a])

91. Toyama’s First Exemplary Structure does not disclose or render obvious “***a substrate with an isolation structure***” as required by limitation [15.a] because the feature of Toyama that Petitioner maps to the “isolation structure” is, at most, located in the region of a cut through the alleged substrate, and is not “part of” the substrate as required under the proper construction of this term.

92. As I discuss in §VIII.B, ’378 claim 15 requires “a substrate ***with*** an isolation structure,” which means that the isolation structure is ***part of*** the substrate.

This construction of the term does not encompass a structure that is merely next to or abutting the substrate. And I further discuss in §VIII.B, even if the term “with” is construed as encompassing “on,” the term “on” means “above” or “on top off” in a vertical direction relative to the lateral surface of the substrate and the patent does not permit reorienting the direction of the “on” spatial relationship to encompass any relative position between components.

93. Toyama’s First Exemplary Structure includes “dielectric fill material portion 430,” which Petitioner divides into two parts, one of which it then maps to the isolation structure of the ’378. Pet. 33-35.

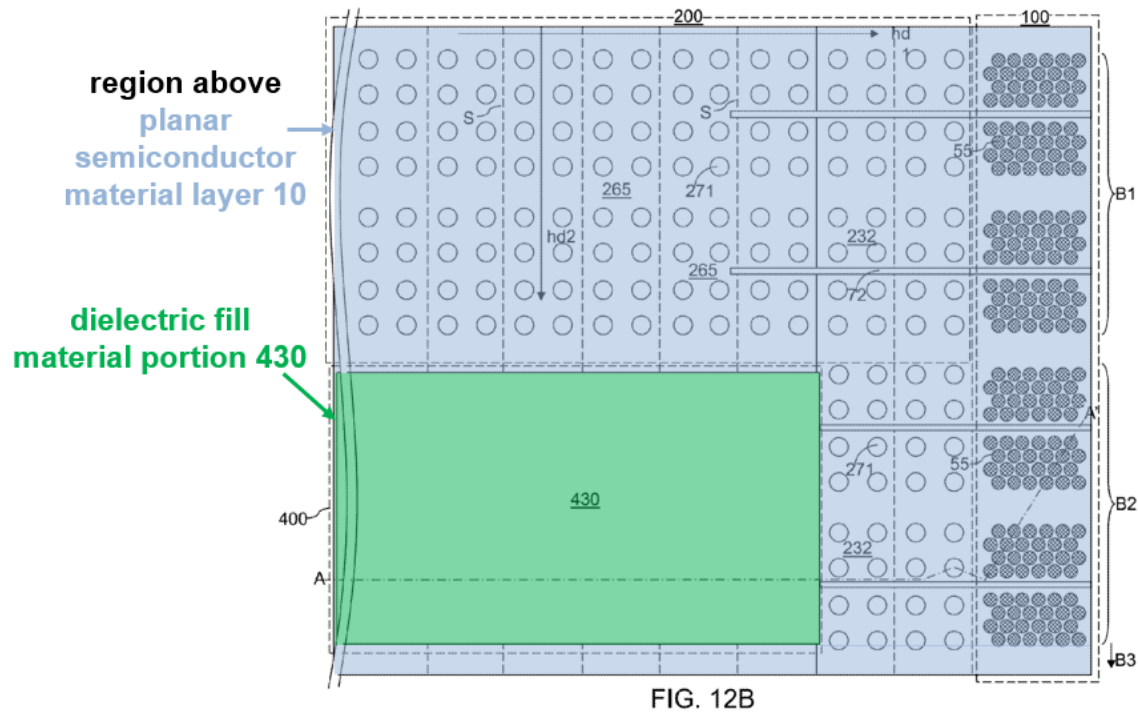


Ex. 1005, Fig. 13A (annotated by Petitioner at Pet. 35).

94. Petitioner’s alleged isolation structure (lower part of “dielectric fill material portion 430”) is not part of the alleged substrate (“planar semiconductor material layer 10”). (For the purposes of this declaration, I do not dispute

Petitioner’s mapping of the claimed “substrate” to Toyama’s “planar semiconductor material layer 10” in Ground 1A.) Petitioner argues that the claimed relationship is satisfied because “Toyama’s isolation structure ... **is formed by removing and is surrounded by** [the] substrate” and “the isolation structure is within the substrate and isolates portions of the substrate from one another” (Pet. 35-36 (emphasis original) (citing Ex. 1003 ¶103)), but Petitioner’s arguments are misplaced for the reasons discussed below.

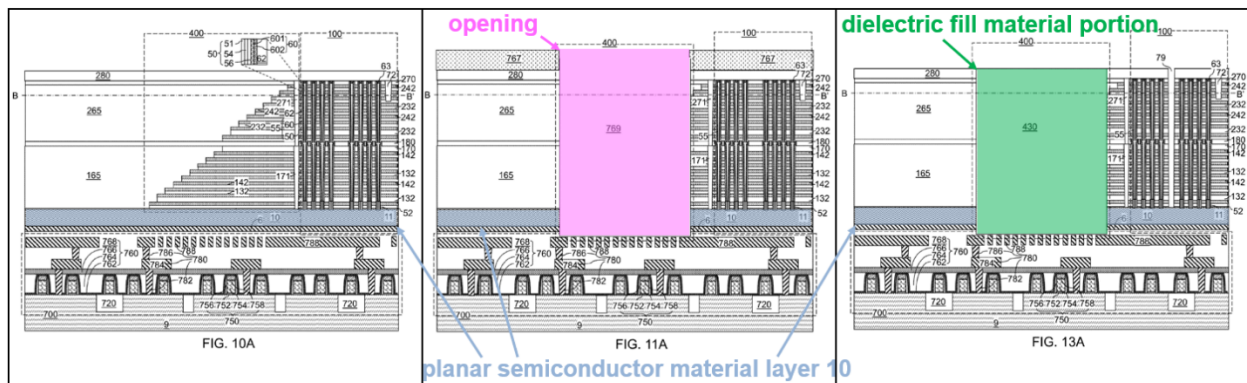
95. As a preliminary matter, Petitioner’s assertion that Toyama’s First Exemplary Structure’s alleged isolation structure “is surrounded by” its alleged substrate is unfounded. Toyama’s relevant figures (Figs. 1A-B to 17A-F) do not depict that dielectric fill material portion “430” is surrounded by other regions. As can be seen below, dielectric fill material portion 430, which I have annotated in green, is shown to extend all the way to the left.



Ex. 1005, Fig. 12B (annotated). Even if the alleged isolation structure were surrounded by the alleged substrate, that would not make it a part of the substrate, just as two structures that are merely horizontally adjacent would not meet this requirement.

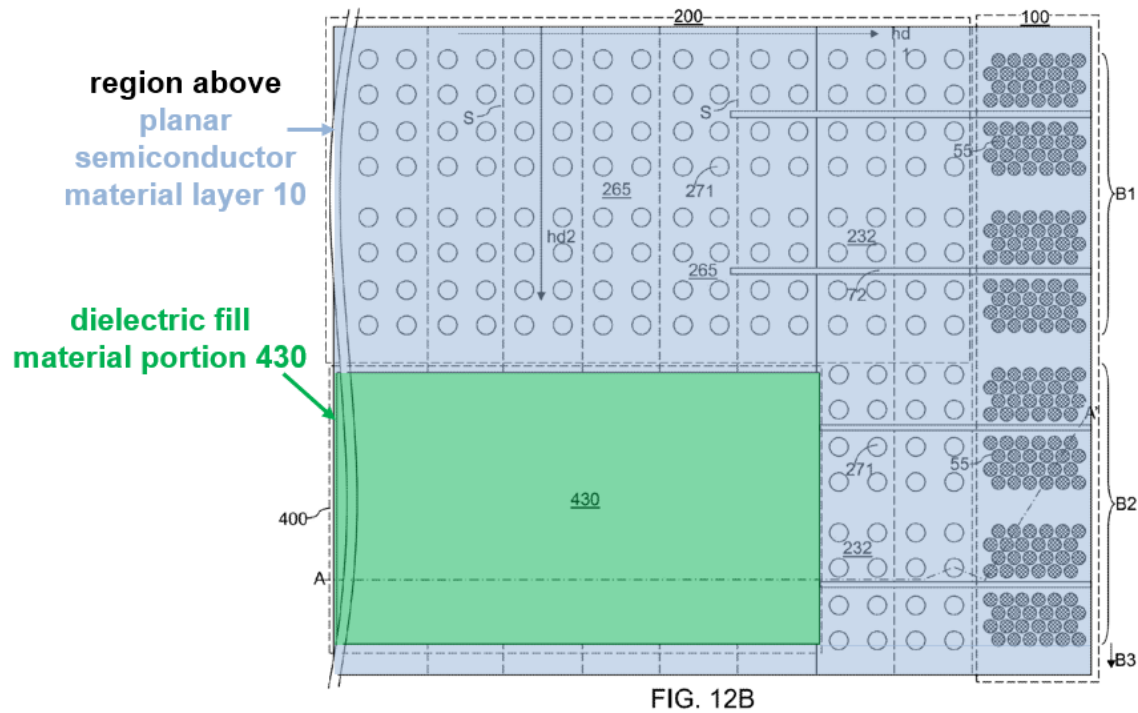
96. The fact that the opening is formed by removing the alleged substrate (Pet. 35-36) does not support Petitioner’s argument because after the substrate is removed there is no longer any portion of the alleged substrate in the relevant region. To further illustrate this, unlike the substrate of ’378, which spans the horizontal area of the memory device and “onto which subsequent material layers are added, or otherwise ‘disposed’” (’378, 4:41-43), Toyama’s “planar semiconductor material layer 10” is completely removed in the relevant region, and is **replaced** by “opening

769.” Ex. 1005, [0213]-[0215], Figs. 12A, 13A. After this step, there is simply no substrate in the region labeled “400.” *Id.*, Fig. 14A. As illustrated below, by forming “opening 769,” Toyama creates a region outside and merely abutting the alleged substrate (“planar semiconductor material layer 10”). It is in this newly opened space, where the alleged substrate has been entirely removed, that “dielectric fill material portion 430” is added. Thus, there is no alleged substrate “with” that dielectric fill material.



Ex. 1005, Figs. 10A, 11A, 13A (annotated). Moreover, I note that these steps that Petitioner cites relate to the manufacturing process, not the final structure, and the Challenged Claims are apparatus claims.

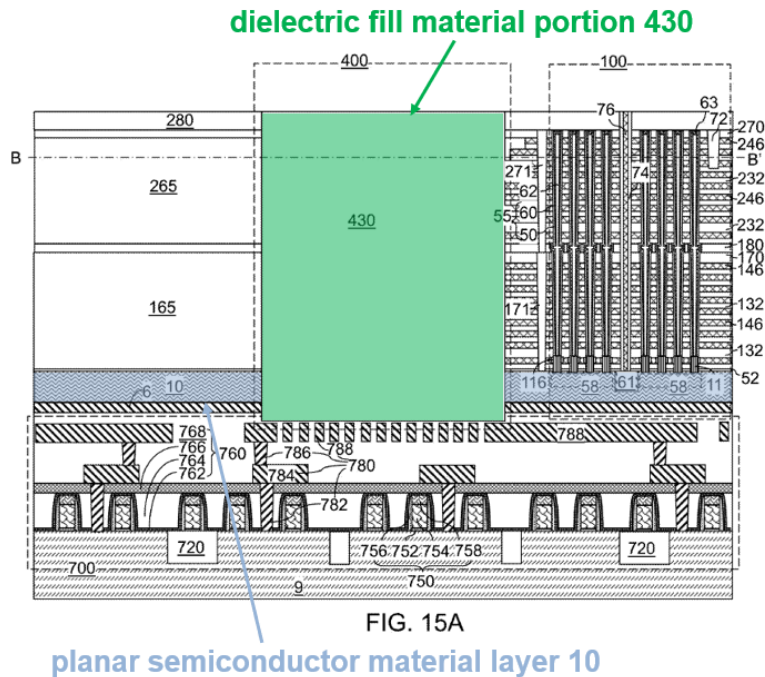
97. Finally, Petitioner’s assertion that “the isolation structure [...] isolates portions of the substrate from one another” is false. As seen in Toyama’s Fig. 12B, the alleged substrate is not divided into isolated portions; *i.e.* it remains connected. Therefore, the alleged isolation structure does not actually isolate portions of the alleged substrate from one another.



Ex. 1005, Fig. 12B (annotated).

98. The Board in its Institution Decision preliminarily concluded that “on the current record for purposes of institution,” the limitation “a substrate with an isolation structure” is taught by Toyama’s First Exemplary Structure,” but the Board’s conclusion was based on its incorrect construction that “an isolation structure may include a substrate having an abutting isolation structure, or an isolation structure ‘formed on’ the substrate, in which ‘on’ may be considered in any orientation of the device.” DI, 15. As I discuss in §VIII.B, this construction is incorrect—as properly construed, the limitation does not encompass an isolation structure that is merely “on” the substrate.

99. Even if “a substrate with an isolation structure” encompassed an isolation structure that is merely “on” the substrate, Toyama’s alleged isolation structure is not “on” the alleged substrate because it is not “above” the substrate in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction (*see* §VIII.A-B). The term “on” does not permit reorienting the direction of the “on” spatial relationship to encompass any relative position for the reasons discussed in §VIII.A-B, and so Toyama’s alleged isolation structure is not “on” the alleged substrate. Specifically, dielectric fill material portion 430 (the alleged isolation structure) is not “on” the alleged substrate because there is simply no alleged substrate below the alleged isolation structure, as shown in Figure 13A. None of the dielectric fill material is above the alleged substrate.



Ex. 1005, Fig. 13A (annotated).

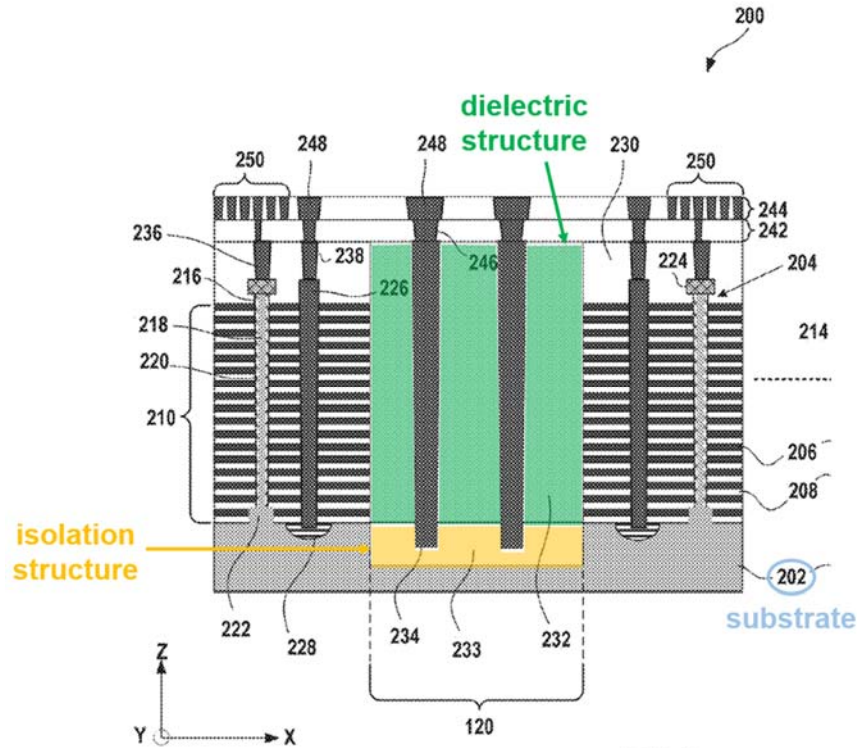
100. For all of these reasons, it is my opinion that Toyama's First Exemplary Structure does not disclose or render obvious ***"a substrate with an isolation structure"*** as required by limitation [15.a].

(b) Toyama's First Exemplary Structure Does Not Disclose or Render Obvious *"a dielectric structure on the isolation structure"* (Limitation [15.c.i])

101. Toyama's First Exemplary Structure does not disclose or render obvious ***"a dielectric structure on the isolation structure"*** as required by limitation [15.c.i] because Petitioner arbitrarily divides Toyama's single dielectric structure into two regions and maps different regions to two separate features of the Challenged Claims: the "dielectric structure" and the "isolation structure."

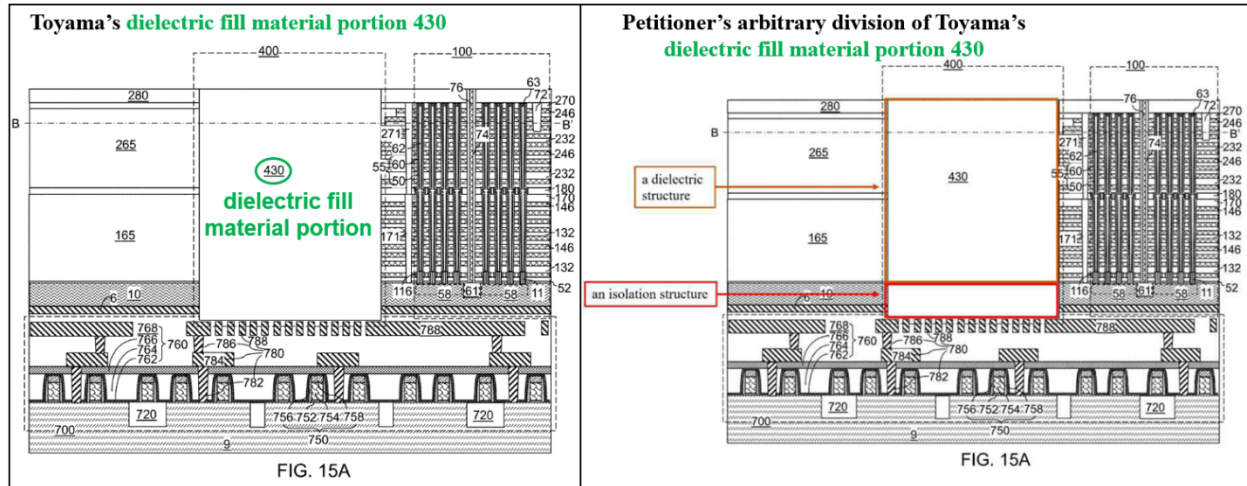
102. As an initial matter, for all the reasons I explain in §X.A.(a), Toyama's First Exemplary Structure does not disclose or render obvious the isolation structure, and as a result, it does not disclose or render obvious a dielectric structure on the isolation structure.

103. Further, Petitioner's only argument for this limitation is to rely on the same substructure for two separate terms in the claim—the claimed dielectric structure and the claimed isolation structure. This arbitrary division of a single structure is different than what is claimed and described in the '378. In the '378, the dielectric structure is a separate structure on the isolation structure. This is expressly recited in the claims, and is shown, for example, in Figure 2 of the '378 which illustrates the two separately claimed structures:



'378, Fig. 2.

104. In contrast, Toyama's First Exemplary Structure includes only a single "dielectric fill material portion 430," which, as illustrated below, Petitioner arbitrarily divides into two parts which it then maps to the separate dielectric structure and isolation structure of the '378. Pet. 33-35, 45.



'378, Fig. 15A (left image annotated by Patent Owner; right image annotated by Petitioner at Pet. 45, with top heading added by Patent Owner). In Toyama, the “fill material portion 430” is a single integral structure. There are not two structures in Toyama and thus there is no dielectric structure that is “on” an isolation structure as required by the Challenged Claims.

105. Petitioner asserts that the specification would not preclude the two structures from being formed during the same process step (Pet. 46), but the issue is not how the device is made, it is whether it has both a dielectric structure **and** an isolation structure with the claimed relationship—Toyama’s First Exemplary Structure does not. The '378 consistently claims, describes, and depicts the isolation structure and the dielectric structure to be separate structures with a specific spatial relationship. '378, 10:30-43, Figs. 2-13. For example, the dielectric structure is “formed so that it is aligned to or covers at least a portion of” the isolation structure ('378, 10:30-33); the dielectric structure is “in contact with” the isolation structure

(’378, 10:35-36); and the dielectric structure “can cover only portion of” the isolation structure (’378, 10:42-43). Thus, I respectfully disagree with the Board’s preliminary conclusion in its Institution Decision that “[n]either the claim nor the specification of the ’378 patent requires different [...] separate depositions for the isolation structure and the dielectric structure thereon.” DI, 20. As the above quotes exemplify, the ’378 teaches forming the isolation structure in the substrate and then depositing the dielectric structure on the isolation structure, resulting in two distinct, identifiable structures.

106. Petitioner argues that the function of the isolation structure is limited to electrically insulating the TACs (Pet. 46-47), but this argument ignores the claims, which are not directed to two functions of a single structure. Rather, the claims recite two structures with a claimed spatial relationship.

107. The Board in its Institution Decision cites the ’378 disclosures that SiO₂ can be used for both the isolation structure and dielectric structure (DI, 20), but even when the same material is used, the isolation structure and dielectric structure are described as two separate structures such that one structure is “in contact with” another. ’378, 10:35-36. Even if the same material (e.g., SiO₂) were used for both the dielectric structure and the isolation structure, there are still two separately identifiable structures, in contrast to Toyama’s single unitary structure.

108. The fact that the '378 allows for “other isolation structures” than “STI structure” ('378, 10:34-35; Pet. 46) is irrelevant and does not mean that it is appropriate to arbitrarily divide any single “dielectric fill material portion” in an attempt to create both the claimed “dielectric structure” and the claimed “isolation structure,” or the claimed spatial relationship that is absent from Toyama.

109. Petitioner argues that “different parts of the same structure can meet distinct claim elements” (Pet. 47). I have been informed that the case cited by Petitioner for this argument involved a structure that had “distinct” portions and that the specification in that case stated that one of the features could be part of the other. In contrast, there are no “distinct” portions of the dielectric fill material portion of Toyama, and the manner in which Petitioner proposes dividing the structure does not correspond to any distinct portions. In addition, the '378 specification does not describe the claimed isolation structure as being part of the claimed dielectric structure, or vice versa.

110. Because the isolation and dielectric structures must be two separate structures as recited in the claims, Toyama’s First Exemplary Structure does not disclose or render obvious “a dielectric structure on the isolation structure”—Petitioner’s arbitrary division of a single structure into two parts does not teach two structures.

111. Finally, Petitioner asserts that Toyama's First Exemplary Structure renders the claims obvious because a different embodiment teaches forming an isolation structure in "opening 151" before forming a dielectric structure (Pet. 47-48 (citing Ex. 1003, ¶ 121)), but the structure formed in Toyama's "opening 151" is not the claimed isolation structure, which must be part of the substrate for the same reasons explained in §X.A.(a) (First Exemplary Structure), and §XI.A.(a) (Second Modification). In addition, Petitioner and Dr. Lee have not identified a motivation for making the proposed changes to the First Exemplary Structure, which are motivated purely by hindsight. Moreover, the proposed modification changes First Exemplary Structure's processing steps, which Petitioner has not addressed. Pet. 47-48. Although Dr. Lee asserts that the process would involve forming the alleged isolation structure before the alleged dielectric structure, instead of forming the isolation and dielectric structures at the same time (Ex. 1003, ¶ 121), he does not address this change within the context of the overall device and the impact that these changes would have on the manufacturing process. For example, he does not address at what stage in the manufacturing process the alleged dielectric structure would be deposited. In addition, he does not address how the process of etching an opening for the dielectric structure would be controlled to stop at the location of the alleged isolation structure, which is an added complication that would have dissuaded a person of ordinary skill in the art from making the proposed modification. Toyama's

Second Modification does not share that same concern because the alleged dielectric structure in that embodiment is a liner with a different geometry that extends into the alleged isolation structure past the top surface of the alleged substrate. Thus, the teachings of Toyama's Second Modification are not directly transferrable to the modification that Dr. Lee proposes making to Toyama's First Exemplary Structure.

112. Thus, Toyama's First Exemplary Structure does not disclose or render obvious "a dielectric structure on the isolation structure" as required by limitation [15.c.i].

(c) Toyama's First Exemplary Structure Does Not Disclose or Render Obvious "TACs extending vertically through the dielectric and the isolation structures" (Limitation [15.h])

113. Toyama's First Exemplary Structure does not disclose or render obvious "*through array contacts (TACs) extending vertically through the dielectric and the isolation structures*" as required by limitation [15.h] because, for all the reasons explained in §§X.A.(a)-(b), Toyama's First Exemplary Structure does not disclose or render obvious the claimed isolation structure or the claimed dielectric structure on the isolation structure.

B. Claim 17: Toyama’s First Exemplary Structure Does Not Disclose or Render Obvious “the dielectric structure comprises a through array contact region of the 3d memory device”

114. Toyama’s First Exemplary Structure does not disclose or render obvious “*the dielectric structure comprises a through array contact region of the 3D memory device*” as required by claim 17.

115. As discussed in §VIII.D, the limitation “the dielectric structure comprises a through array contact region of the 3D memory device” means “a region that is within or defined by the dielectric structure and which includes the through array contacts extending through the dielectric structure.” For all the reasons explained in §X.A.(b), Toyama’s First Exemplary Structure does not disclose or render obvious the claimed dielectric structure, and as a result, does not disclose or render obvious a through array contact region that is within or defined by the dielectric structure.

XI. PETITIONER’S GROUND 1B: TOYAMA’S SECOND MODIFICATION DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 15-17 AND 19-20

116. For the reasons explained below, it is my opinion that Toyama’s Second Modification does not disclose or render obvious the Challenged Claims at least because Toyama’s Second Modification does not disclose or render obvious multiple elements of claim 15—the sole independent claim. For example, Toyama’s Second Modification does not disclose or render obvious “a substrate with an isolation

structure.” Toyama’s Second Modification also does not disclose or render obvious “a dielectric structure on the isolation structure.” Toyama’s Second Modification further does not disclose or render obvious “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.” Finally, for claim 17, Toyama’s Second Modification does not disclose or render obvious “the dielectric structure comprises a through array contact region of the 3D memory device.”

A. Independent Claim 15: Toyama’s Second Modification Does Not Disclose or Render Obvious Limitations [15.a], [15.c.i], and [15.h]

(a) Toyama’s Second Modification Does Not Disclose or Render Obvious “a substrate with an isolation structure” (Limitation [15.a])

117. Toyama’s Second Modification does not disclose or render obvious “**a substrate with an isolation structure**” as required by limitation [15.a] because—just like with Toyama’s First Exemplary Structure—the feature of Toyama that Petitioner maps to the “isolation structure” is, at most, located in the region of a cut through the alleged substrate, and is not “part of” the substrate as required by the Challenged Claims under the proper construction of this term (see §VIII.B).

118. As I discuss in §VIII.B, ’378 claim 15 requires “a substrate **with** an isolation structure,” which means that the isolation structure is **part of** the substrate. This construction of the term does not encompass a structure that is merely next to or abutting the substrate. And I further discuss in §VIII.B, even if the term “with”

is construed as encompassing “on,” the term “on” means “above” in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction, and the patent does not permit reorienting the direction of the “on” spatial relationship to encompass any relative position between components.

119. Toyama’s Second Modification includes “opening 151” that “may be filled with another insulating material layer [...] 760,” which Petitioner erroneously maps to the isolation structure of the ’378. Pet. 30-31. For the same reasons discussed in §VI.A.1, Petitioner’s alleged isolation structure (“opening 151” filled with “insulating material layer 760”) in Toyama’s Second Modification’s is not part of the alleged substrate (“planar semiconductor material layer 10”). (For the purposes of this declaration, I do not dispute Petitioner’s mapping of the claimed “substrate” to Toyama’s “planar semiconductor material layer 10” in Ground 1B.) Specifically, contrary to Petitioner’s arguments about how the device is made, as illustrated below, the alleged substrate is completely removed in the relevant region, thereby creating a region outside and merely abutting the alleged substrate, and the “insulating material layer 760” is added in that through-opening.

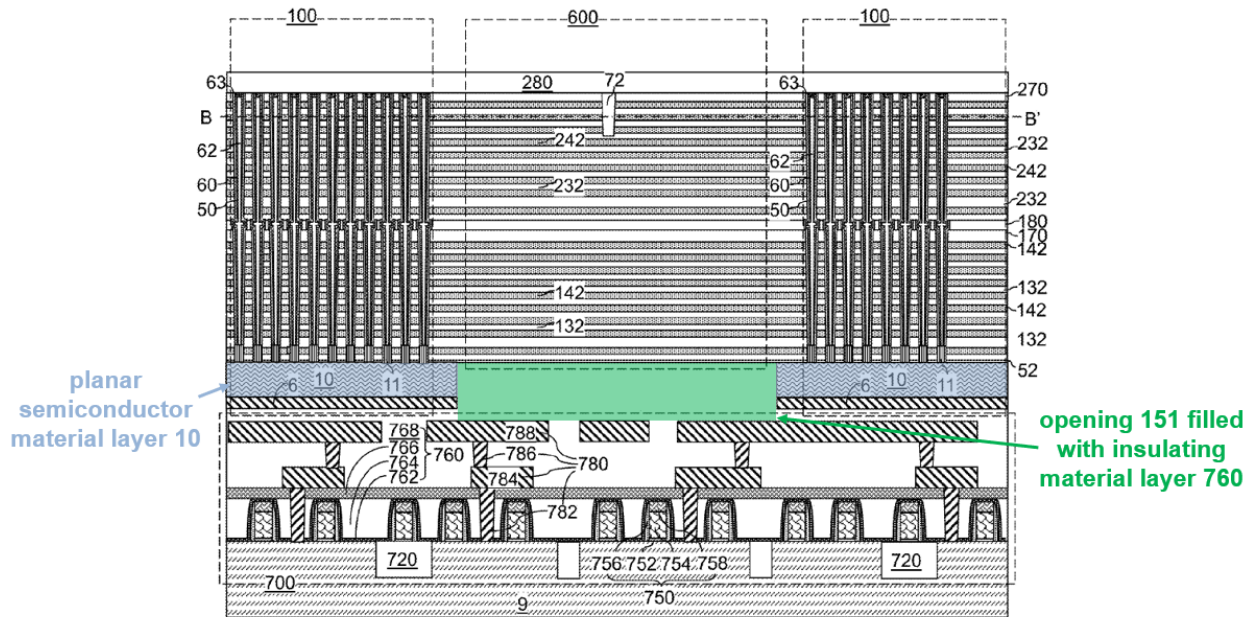


FIG. 44A

Ex. 1005, Fig. 44A (annotated). Thus, the alleged substrate and insulating material layer 760 do not meet the claim “substrate with isolation structure” In the context of Toyama’s Second Modification, Petitioner never addresses the relationship between two claim limitations, *i.e.*, that “a substrate” must be “**with**” “an isolation structure” and simply asserts that it is shown. Pet. 31. While Dr. Lee provides some additional explanation, he merely raises the same process related argument discussed above. Ex. 1003, ¶ 100.

120. I disagree with Petitioner’s additional arguments relevant to this limitation made in the context of Toyama’s First Exemplary Structure (Pet. 35-36) for the same reasons that I discuss in §X.A.(a) above.

121. Therefore, Petitioner has not shown that Toyama's Second Modification discloses or renders obvious "***a substrate with an isolation structure***" as required by limitation [15.a].

(b) Toyama's Second Modification Does Not Disclose or Render Obvious "a dielectric structure on the isolation structure" (Limitation [15.c.i])

122. Toyama's Second Modification does not disclose or render obvious "***a dielectric structure on the isolation structure***" as required by limitation [15.c.i]. For all the reasons explained in § XI.A.(a), Toyama's Second Modification does not disclose or render obvious an isolation structure. As a result, Toyama's Second Modification does not disclose or render obvious a dielectric structure on the isolation structure.

(c) Toyama's Second Modification Does Not Disclose or Render Obvious "TACs extending vertically through the dielectric and the isolation structures" (Limitation [15.h])

123. Toyama's Second Modification does not disclose or render obvious "***through array contacts (TACs) extending vertically through the dielectric and the isolation structures***" as required by limitation [15.h] because Toyama's alleged TACs do not extend through the same structure (the claimed "dielectric structure").

124. As an initial matter, for all the reasons I explain in §§XI.A.(a)-(b), Toyama's Second Modification does not disclose or render obvious an isolation structure or a dielectric structure on the isolation structure. As a result, Toyama's

Second Modification does not disclose or render obvious “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.”

125. In addition, Toyama’s TACs do not extend through the same “dielectric structure.” As I discuss in §IV.C, the phrase “through array contacts (TACs) extending vertically through the dielectric and the isolation structures” means “through array contacts (TACs) extending vertically through the dielectric structure and the isolation structure”—i.e., through the same “a dielectric structure” recited earlier in the claim. As discussed below, the alleged TACs of Toyama’s Second Modification do not meet this requirement.

126. Petitioner maps “insulating liners 674” of “through-memory-level via structures 676” to the “dielectric structure” of the ’378 (Pet. 39-42), but this mapping relies on a separate insulating liner (i.e., a separate alleged dielectric structure) for each TAC. In other words, in Toyama’s Second Modification, only a single “through-memory-level via structure 676” extends through a given “insulating liner 674.” Realizing this problem, Petitioner attempts to map multiple insulating liners 674 to a single “dielectric structure.” Pet. 41 (alleging that “the ‘insulating liners 674’ are collectively a *structure*”).

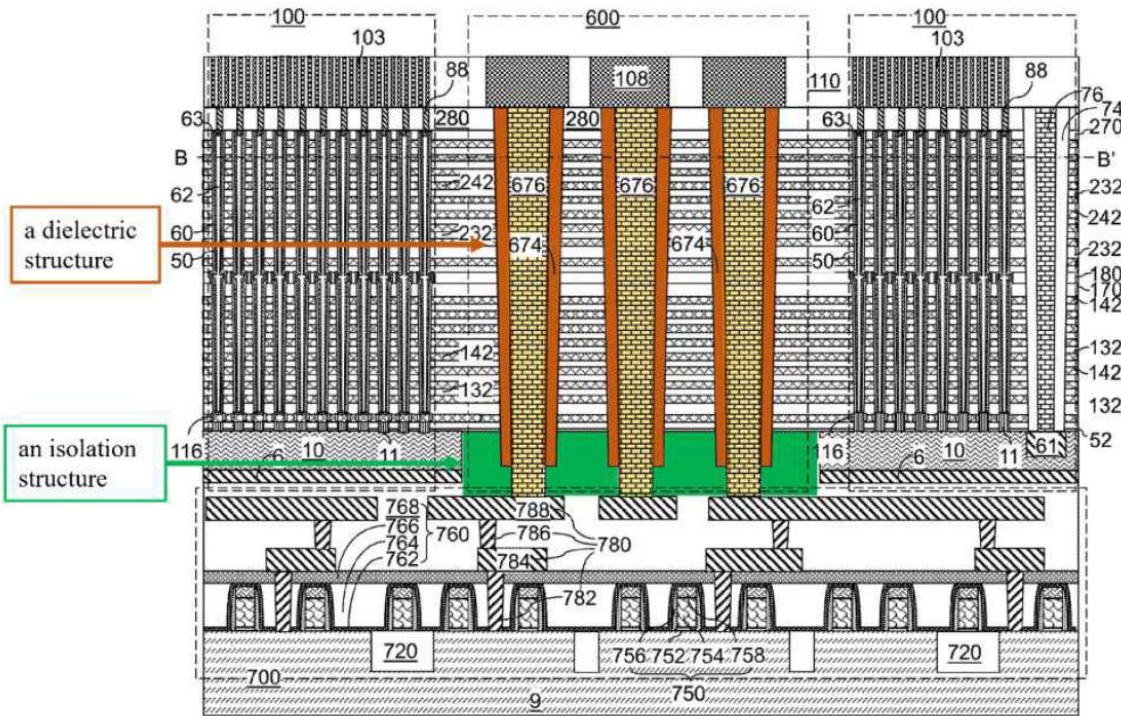


FIG. 49

Ex. 1005, Fig. 49 (annotated by Petitioner at Pet. 40).

127. I disagree with Petitioner’s attempt to rely on separate dielectric structures as a single claimed “dielectric structure.” I understand that in its subsequent decision for IPR2024-00791 (an IPR of the ’806 patent, which is a continuation of the ’378 patent) (Ex. 2006), the Board “disagree[d] [with Petitioner’s assertion] that merely because the three insulating liners are each constructed, that three constructed liners together constitute a single dielectric structure.” Ex. 2006, 17. As a result, the Board found that Toyama’s Second Modification does not show “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” because “Petitioner has not sufficiently shown that Toyama’s three insulating liners are a single dielectric structure.” Ex. 2006, 17. I agree with

this preliminary conclusion from the Board in IPR2024-00791. The '378 limitation at issue here, just like the '806 limitation, requires that multiple TACs extend through a single dielectric structure, and so the Board's reasoning in IPR2024-00791 is equally applicable here.

128. The claim, when correctly interpreted (*see* §VIII.C), requires that a single “dielectric structure” must have multiple “through array contacts (TACs) extend[] vertically through” it, which Toyama’s “insulating liner 674” do not show.

129. Finally, in its attempt to map multiple separate liners to a single structure, Petitioner cites a dictionary to assert that because “these components together are something ‘that is constructed,’ they are a structure” (Pet. 31-32), but this argument does not comport with the claims and specification of the '378.

130. Therefore, Petitioner has not shown that Toyama’s Second Modification discloses or renders obvious “through array contacts (TACs) extending vertically through the dielectric and the isolation structures” as required by limitation [15.h].

B. Claim 17: Toyama’s Second Modification Does Not Disclose or Render Obvious “the dielectric structure comprises a through array contact region of the 3d memory device”

131. Toyama’s Second Modification does not disclose or render obvious “*the dielectric structure comprises a through array contact region of the 3D memory device*” as required by claim 17 because the alleged TAC region of

Toyama's Second Modification is not within or defined by the alleged dielectric structure as required by claim 17.

132. As I discuss in §VIII.E, the limitation “the dielectric structure comprises a through array contact region of the 3D memory device” means “a region that is within or defined by the dielectric structure and which includes the through array contacts extending through the dielectric structure.” As I further discuss in §VIII.E, the TAC region does not include the alternating conductor/dielectric layer stack.

133. Petitioner's alleged TAC region in Toyama's Second Modification is not within or defined by the alleged dielectric structure as required by claim 17. Instead, Petitioner's **alleged TAC region** is an arbitrarily defined region that includes **multiple alleged dielectric structures, TACs**, and large portions of **alternating conductor/dielectric layers**. Petitioner's mapping of the TAC region (cf. Pet. 73) is reproduced below with further annotations:

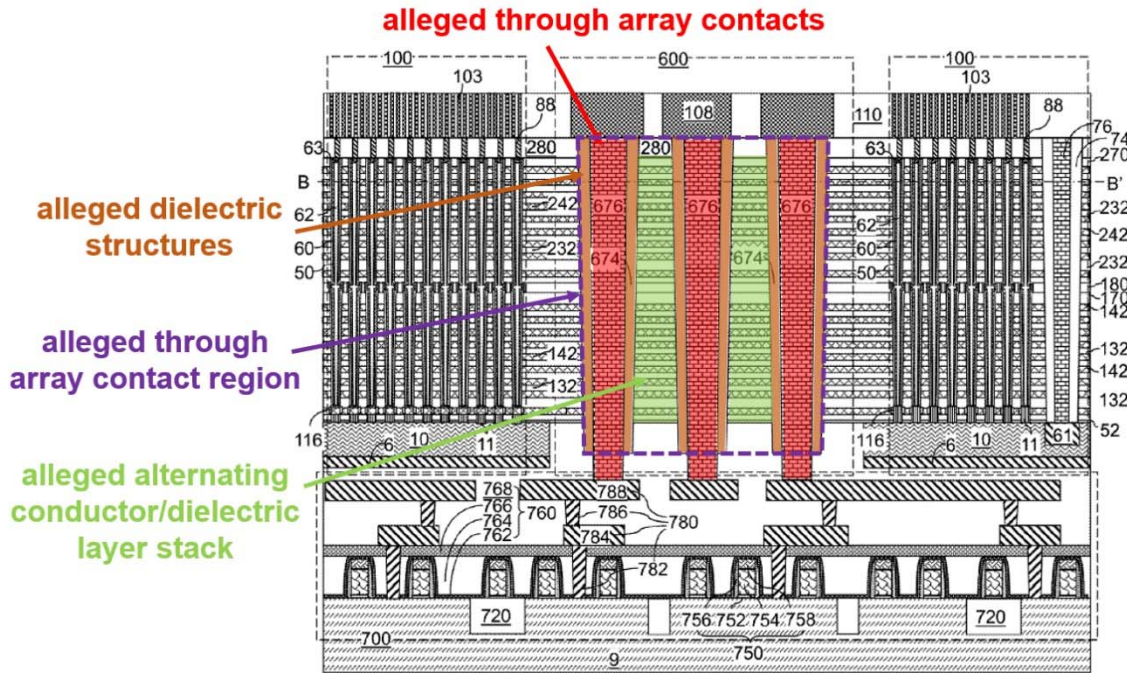


FIG. 49

Ex. 1005, Fig. 49 (annotated).

134. First, Petitioner’s mapping does not meet the claim because, as shown, the alleged TAC region extends beyond the alleged structure, and thus is not within or defined by the alleged dielectric structure (*see* §VIII.E). In other words, because the alleged TAC region extends beyond the alleged structure, the alleged dielectric structure does not “comprise” the TAC region as required by the claim—rather, Petitioner points to an alleged TAC region that comprises a dielectric structure. Second, Petitioner’s alleged TAC region includes the alternating conductor/dielectric layers, which the claim does not permit. As discussed in §VIII.E, because the dielectric structure extends through the alternating conductor/dielectric layer stack (independent claim 15) and the through array contact

region (“TAC region”) is within or defined by the dielectric structure, the TAC region does not include the alternating conductor/dielectric layer stack. Petitioner’s mapping does not address these issues. Pet. 72-74.

135. Therefore, Petitioner has not shown that Toyama’s Second Modification discloses or renders obvious “the dielectric structure comprises a through array contact region of the 3D memory device” as required by claim 17.

XII. PETITIONER’S GROUND 2: MUSHIGA DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 15-17 AND 19-20

136. For the reasons explained below, it is my opinion that Mushiga does not disclose or render obvious the Challenged Claims at least because Mushiga does not disclose or render obvious multiple elements of claim 15—the sole independent claim. For example, Mushiga does not disclose or render obvious “a substrate with an isolation structure.” Mushiga also does not disclose or render obvious “a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material.” Mushiga further does not disclose or render obvious “through array contacts (TACs) extending vertically through the dielectric and the isolation structures.” Finally, for claim 17, Mushiga does not disclose or render obvious “the dielectric structure comprises a through array contact region of the 3D memory device.”

A. Independent Claim 15: Mushiga Does Not Disclose Or Render Obvious Limitations [15.a], [15.c.i], and [15.h]

(a) Mushiga Does Not Disclose or Render Obvious “a substrate with an isolation structure” (Limitation [15.a])

137. Mushiga does not disclose or render obvious “*a substrate with an isolation structure*” as required by limitation [15.a] because—just as with Toyama’s structures—the feature of Mushiga that Petitioner maps to the “isolation structure” is, at most, located in the region of a cut through the alleged substrate, and is not “part of” the substrate as required by the Challenged Claims under the proper construction.

138. As I discuss in §VIII.B, ’378 claim 15 requires “a substrate” to be “*with* an isolation structure,” which means that the isolation structure is *part of* the substrate. This construction of the claim term does not necessarily encompass any insulating structure that is merely next to or abutting the substrate. And as I further discuss in §VIII.B, even if the term “with” is construed as encompassing “on,” the term “on” means “above” or “on top of” in a vertical direction relative to the lateral surface of the substrate and the patent does not permit reorienting the direction of the “on” spatial relationship to encompass any relative position between components.

139. Mushiga includes “**backside insulating layer 306**,” which Petitioner combines with “**insulating material liners 302**” and erroneously maps to the isolation structure of the ’378. Pet. 79-80.

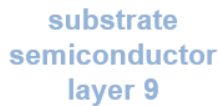


FIG. 11

Ex. 1006, Fig. 11 (annotated). Petitioner identifies “**substrate semiconductor layer 9**” as the alleged substrate. (For the purposes of this declaration, I do not dispute Petitioner’s mapping of the claimed “substrate” to Mushiga’s “substrate semiconductor layer 9” in Ground 2.) Setting aside whether the backside insulating layer 306 and the insulating material liners 302 can be combined to be the purported isolation structure and whether the insulating material liners 302 are part of the purported substrate, the combination still does not meet the claims.

140. No portion of Petitioner’s alleged isolation structure is “part of” the alleged substrate as required by the claims. First, the “**insulating material liners** **302**” portion of Petitioner’s alleged isolation structure in Mushiga is not part of the alleged substrate (“substrate semiconductor layer 9”) for the same reasons I

discussed in §§X.A.(a) and XI.A.(a). Specifically, the alleged substrate is completely removed in cuts that extend through the alleged substrate, thereby creating regions that are outside and merely abutting the alleged substrate, and the “insulating material liners 302” is added in that through-opening.

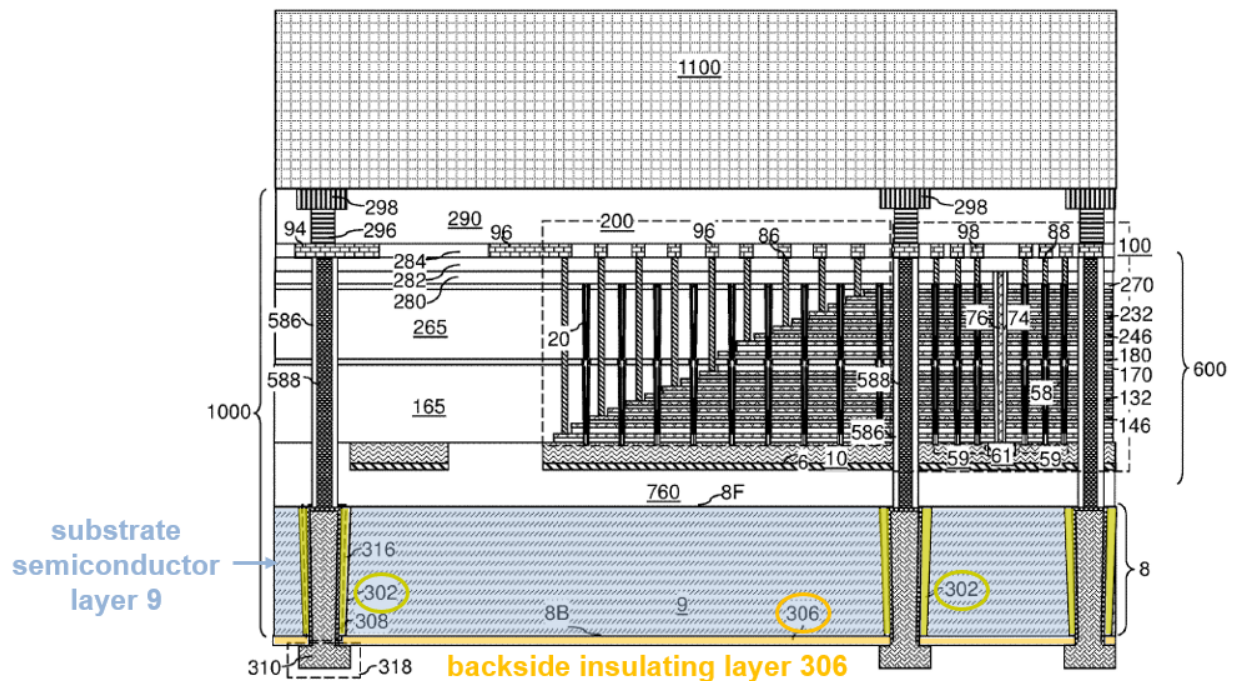
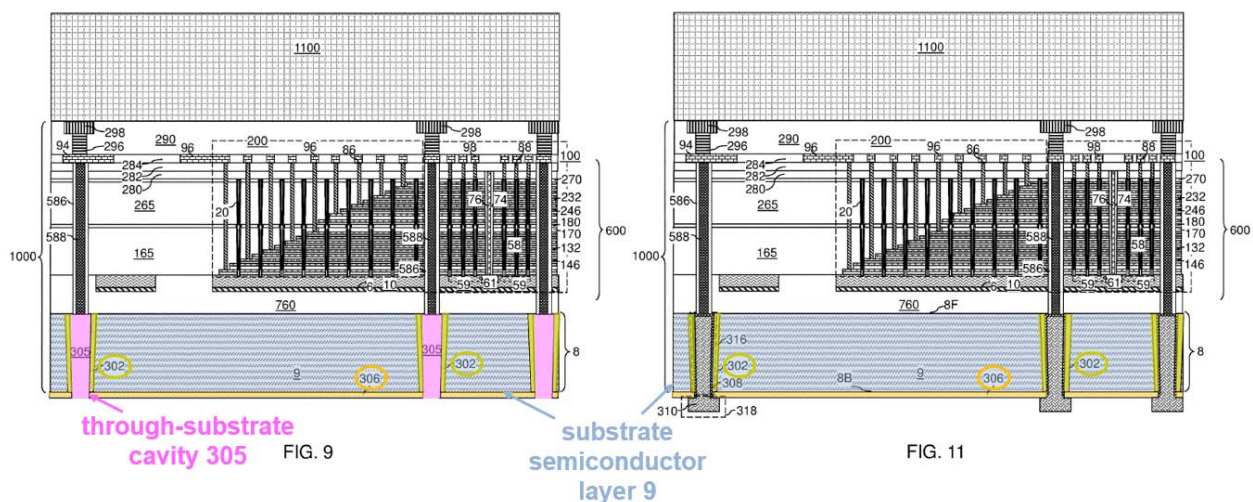


FIG. 11

Ex. 1006, Figure 11 (annotated). Thus, Mushiga teaches a similar spatial relationship to those at issue in Grounds 1A and 1B (Toyama), and I disagree with Petitioner’s arguments for the same reasons. Second, the “backside insulating layer 306” portion of Petitioner’s alleged isolation structure in Mushiga is merely below the substrate, rather than “part of” the substrate. Such a mapping fares no better than Toyama’s alleged structure that is merely “on” the substrate, and as discussed in §VIII.B, the construction “part of” does not encompass structures that

are merely “on” (or in this case, “below”) the substrate. And even if “part of” encompassed structures that are merely “on” the substrate (it does not), “on” means “above” or “on top off” in a vertical direction relative to the lateral surface of the substrate (*see* §VIII.A-B), not below.

141. In an attempt to address the required relationship between two claim terms, *i.e.*, that “a substrate” must be “**with**” “an isolation structure,” Petitioner and Dr. Lee argue that “Mushiga’s isolation structure [...] **is formed by removing portions of the** substrate [...]” (Pet. 79-80 (citing Ex. 1003, ¶ 173-174)), but I disagree with this argument for the same reasons discussed in §VI.A.1. Specifically, as illustrated below, and again contrary to Petitioner’s arguments regarding how the devices are made, the alleged substrate is completely removed in the relevant region, thereby creating regions (“**through-substrate cavities 305**”) outside and merely abutting the alleged substrate, and the “**insulating material liners 302**” is in those through-openings.



Ex. 1006, Figs. 9, 11 (annotated). After the substrate is removed, there is no longer any portion of the alleged substrate in the relevant region. Moreover, and again similar to my discussion in §VI.A.1, Petitioner’s cited processing steps relate to the manufacturing process, not the final structure, and the Challenged Claims are apparatus claims.

142. Therefore, Petitioner has not shown that Mushiga discloses or renders obvious “*a substrate with an isolation structure*” as required by limitation [15.a].

(b) Mushiga Does Not Disclose or Render Obvious “a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack” (Limitation [15.c])

143. Mushiga does not disclose or render obvious “*a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack*” as required by limitation [15.c] because the only alleged “dielectric structure” that extends though the stack is not also “on the isolation structure.”

144. As an initial matter, for all the reasons I explain in §XII.A.(a), Mushiga does not disclose or render obvious an isolation structure. As a result, Mushiga also does not disclose or render obvious the claimed dielectric structure on the isolation structure.

145. I further disagree with Petitioner’s mapping for this element because the alleged “dielectric structure” is not both “extending vertically through the

alternating conductor/dielectric layer stack” (mapped to Mushiga’s “alternating stack (132, 146, 232, 246)”) and “on the isolation structure.” Petitioner maps “insulating material layer 760,” “first retro-stepped dielectric material portion 165,” “inter-tier dielectric layer 180,” “second retro-stepped dielectric material portion 265,” and “insulating spacer 586” collectively to the “dielectric structure” of the ’378. Pet. 81-83.

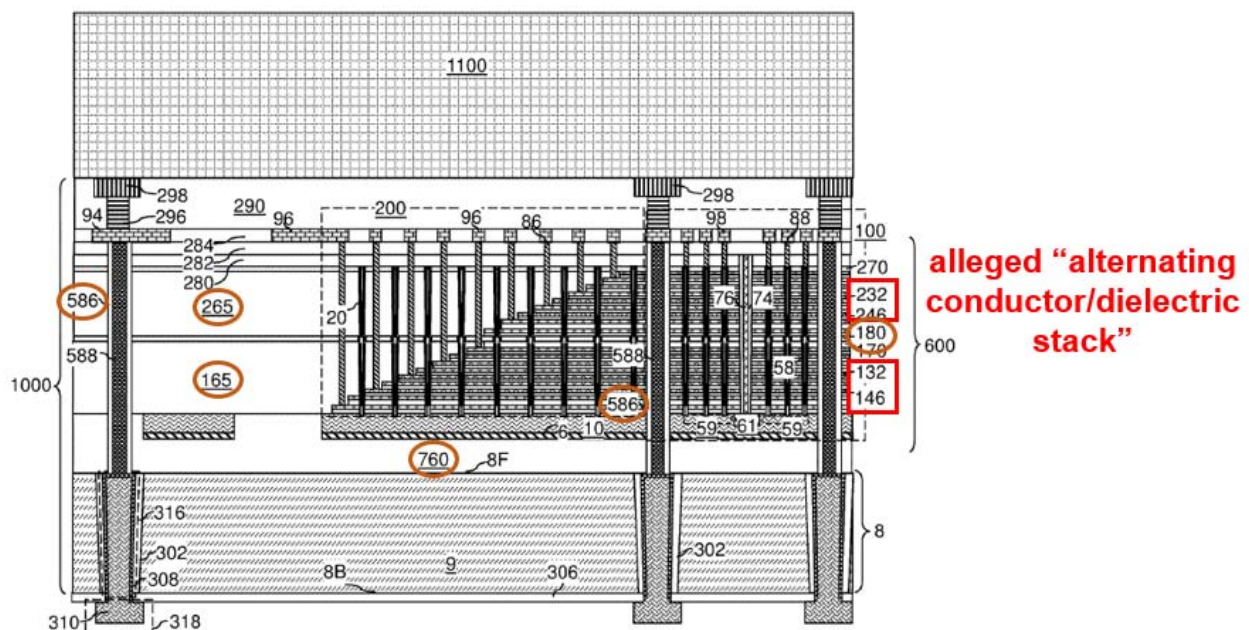


FIG. 11

Ex. 1006, Fig. 11 (annotated).

146. Among these elements, only the “insulating spacers 586” is even arguably “*extending vertically through the alternating conductor/dielectric layer stack*” as required by Limitation [15.c]. As can be seen in the above figure, the other features are either outside the alternating stack altogether or, in the case of “inter-

tier dielectric layer 180,” it makes a horizontal cut across the alternating stack instead of extending vertically through the stack.

147. While “insulating spacers 586” arguably extend through the alleged alternating conductor/dielectric layer stack, they do not meet multiple other claim requirements. First, “insulating spacers 586” are not *“a dielectric structure on the isolation structure”* as required by the Challenged Claims (even assuming, *arguendo*, that Petitioner has identified an isolation structure).

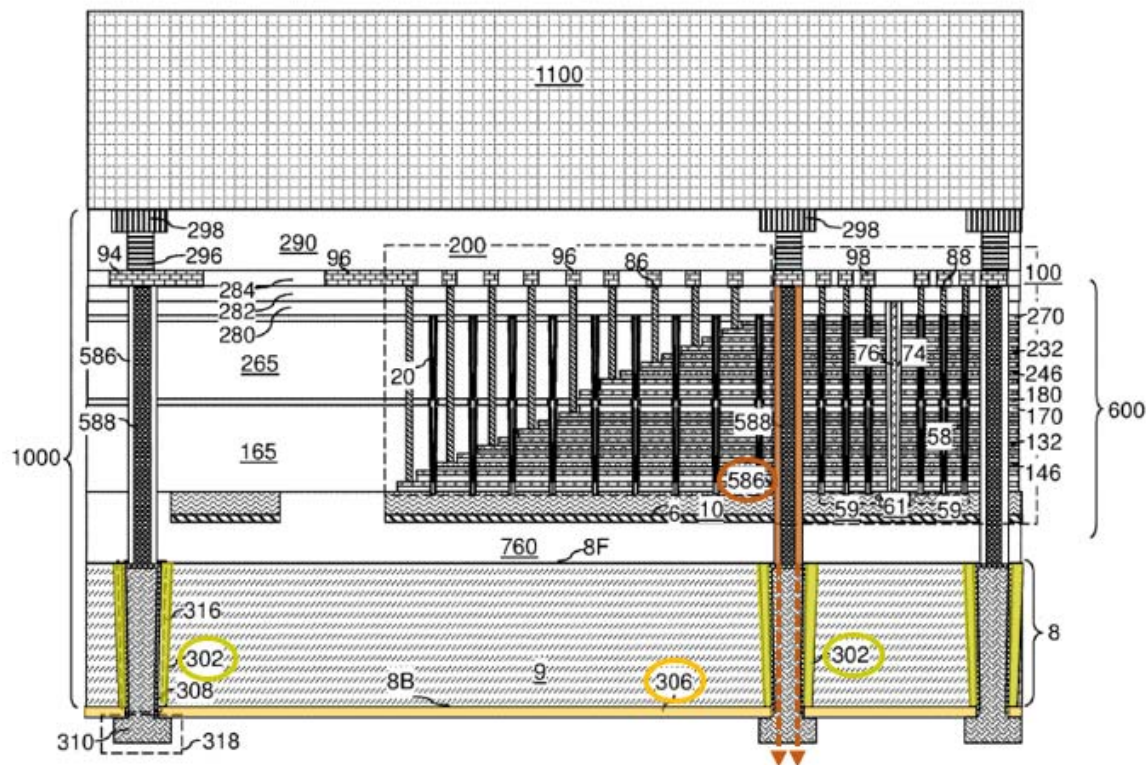


FIG. 11

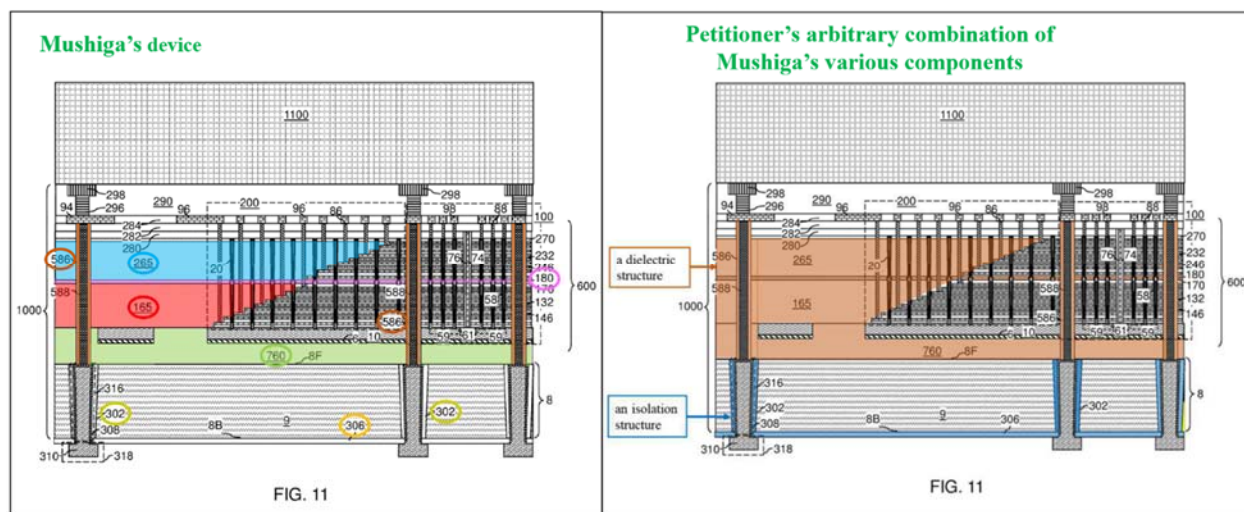
Ex. 1006, Fig. 11 (annotated). As shown in the figure, **insulating spacers 586** are not “on” Petitioner’s alleged isolation structure—**backside insulating layer 306** and **insulating material liners 302**—because **insulating spacers 586** are not above

those structures. The annotated dashed lines show that the edge of the **insulating spacers 586**, if extended downward, do not pass through **backside insulating layer 306** or **insulating material liners 302** and thus are not above them. In the Institution Decision, the Board preliminarily found that “on” does not require direct contact and is not limited to any particular orientation (DI, 29), but as I discuss in §VIII.A, the device may not be reoriented for purposes of determining whether an alleged dielectric structure is on the isolation structure (when the device is reoriented, the vertical direction is reoriented and remains perpendicular to the substrate). In the ’378 specification, it is emphasized that the isolation structure is aligned with the dielectric structure. ’378, 10:30-33 (“In some embodiments, dielectric structure 232 is formed so that it is aligned to or covers at least a portion of an underlying isolation structure or region 233.”), 14:52-54. This allows for the formation of multiple TACs in a single processing step. ’378, Figs. 3, 11-12, 18:27-41 (“TACs 234 can be formed by etching through the entire thickness of dielectric structure 702. ... Forming TACs 234 in dielectric structure 232 can simplify the fabrication process and reduce the fabrication cost.”). Mushiga’s unaligned structures simply do not provide this benefit.

148. Second, “insulating spacer 586” does not meet the claim limitation ***“through array contacts (TACs) [plural] extending vertically through the dielectric and the isolation structures”*** [15.h] in the same way as Toyama’s

“insulating liner 674.” See §XI.A.(c). Specifically, Petitioner has not shown a plurality of TACs that extend through the same insulating spacer 586 because, as shown above, each TAC extends through a separate insulating spacer.

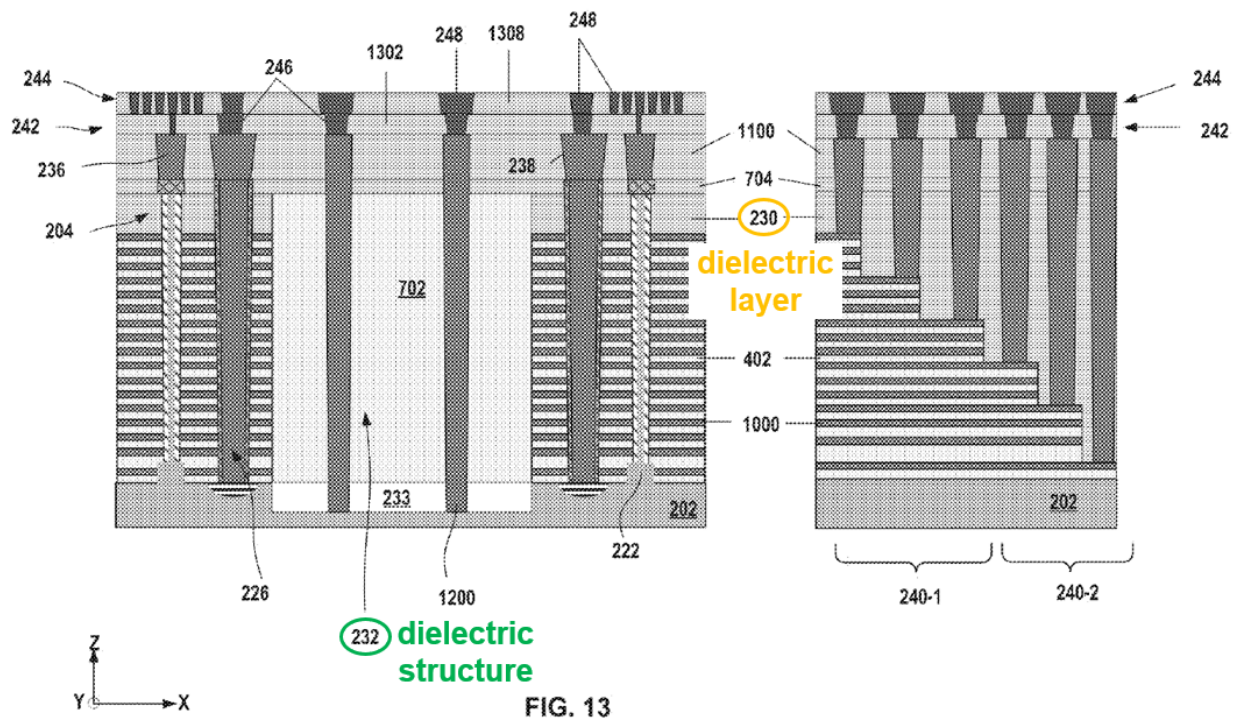
149. Because “insulating spacer 586” does not satisfy all the requirements of the claimed “dielectric structure,” Petitioner attempts to combine the spacer with multiple other dielectric regions (Pet. 81-84), but its grouping has no discernable logic and does not teach the claimed “a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack.”



Ex. 1006, Fig. 11 (left image annotated by Patent Owner; right image annotated by Petitioner at Pet. 82, with top heading added by Patent Owner). As discussed further below, the elements Petitioner arbitrarily combines are separate structures with distinct locations and roles. While the '378's dielectric structure serves as a region for the TACs to be easily formed nearby the memory strings ('378, 11:3-9, 18:27-41), Mushiga's layers 760, 165, 180, and 265 are located partly or entirely away

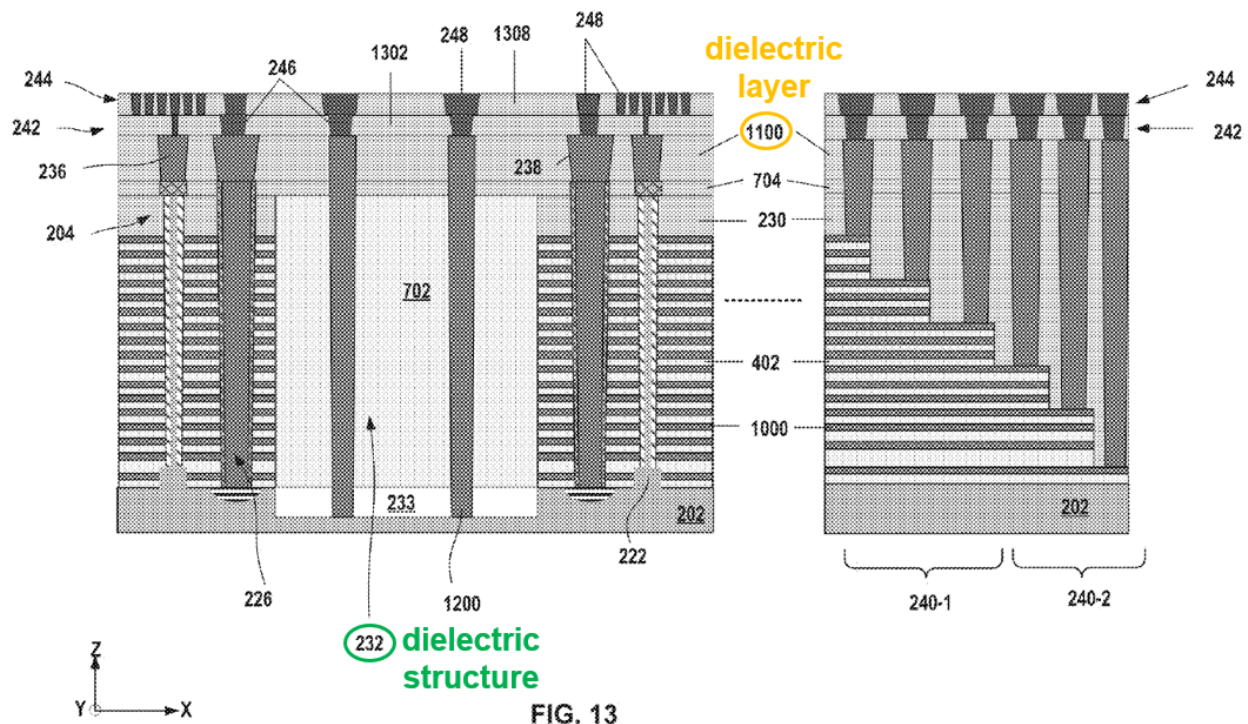
from the memory strings and serve no purpose in forming the alleged TACs. Indeed, Petitioner purports to include structures that are analogous to ones described in the '378 as being separate from the claimed dielectric structure, and thus are not a single "dielectric structure" as claimed.

150. For example, Mushiga's "first retro-stepped dielectric material portion 165" and "second retro-stepped dielectric material portion 265" in combination are nothing more than the dielectric material that covers the stair steps (Ex. 1006, 9:22-26, 9:38-39), which the '378 identifies as "dielectric layer 230" (separate from the '378's "dielectric layer 702" that is on the isolation structure and extending vertically through the stack).



'378, Fig. 13 (annotated).

151. Similarly, Mushiga’s “insulating material layer 760” is a dielectric material layer that separates Mushiga’s alleged substrate (“semiconductor layer 9”) from “semiconductor material layer 10.” Ex. 1006, 9:8-12. Thus, Mushiga’s “insulating material layer 760” is akin to the ’378’s “dielectric layer 1100” shown below, which is above and spans the full area of the alternating stack (and is separate from the ’378’s “dielectric layer 702” that is on the isolation structure and extending vertically through the stack).



’378, Fig. 13 (annotated).

152. In its purported combination of adjacent dielectric elements, Petitioner also inconsistently omitted other adjacent dielectric elements that, if included, would

have hurt its claim mapping. For example, as shown below in Mushiga's Fig. 11, the red annotated dielectric features were not included.

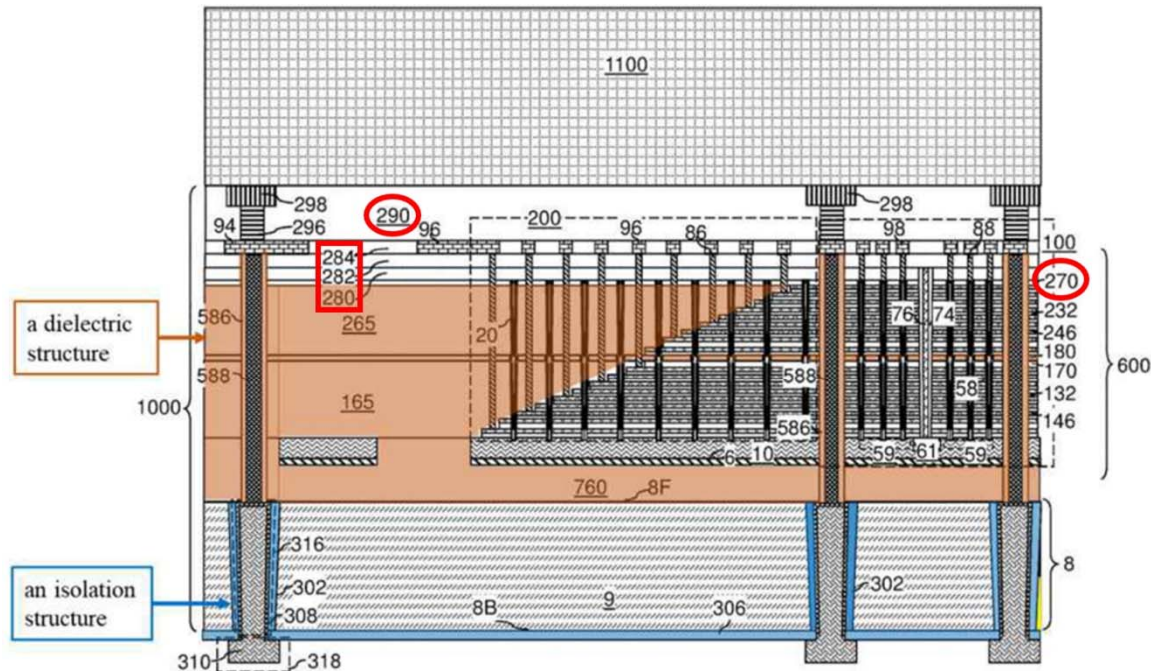


FIG. 11

Ex. 1006, Fig. 11 (annotated by Petitioner at Pet. 82, with red annotations added by Patent Owner). By Petitioner's logic of coloring in as one structure different dielectric features that are merely adjacent, Petitioner also should have included layers 270 ("second insulating cap layer 270"), 280 ("first contact level dielectric layer 280"), 282 ("second contact level dielectric layer 282"), 284 ("line level dielectric layer 284"), and 290 ("additional interconnect level dielectric layers 290"). This would have led to a situation in which Mushiga's through-memory level vias 588 (the alleged TACs) do not extend through the alleged dielectric structure as required by the Challenged Claims, as they would terminate within the dielectric

structure (between layers 282 and 284). Petitioner's choices of which dielectric features to include and which to exclude in its mapping of Mushiga to the claimed dielectric structure is inconsistent and appear to be based on hindsight, rather than a teaching in the cited art or the knowledge of a person of ordinary skill in the art. For example, Dr. Lee acknowledged that there are other dielectric structures in Mushiga that he omitted, and that his process of selecting which structures to combine was guided by the claim language. Ex. 2007, 53:21-57:17.

153. In the Institution Decision, the Board preliminarily found that the '378 does not preclude the claimed dielectric structure from being taught by multiple elements having different purposes (DI, 29), but this conclusion is inconsistent with the claims, which apply multiple requirements to the same "dielectric structure," regardless of whether other dielectric structures are also present in the device. *See, e.g.*, §VIII.C (discussing the requirement that TACs extend through the same dielectric structure). Petitioner does not sufficiently explain how these separate components can be considered a single structure (the claimed "dielectric structure"). Petitioner's argument that these separate components are a "structure" because "these components together are something 'that is constructed'" (Pet. 82-83) is inconsistent with the intrinsic record. While the Board in its Institution Decision "agree[d] with Petitioner" that these components "teach the claimed dielectric structure" (DI, 29-30), in its subsequent decision for IPR2024-00791 (Ex. 2006), the

Board “disagree[d] that merely because the three insulating liners are each constructed, that three constructed liners together constitute a single dielectric structure.” Ex. 2006, 17. As the Board found, “[e]very component of Toyama’s memory device is something that is constructed. Petitioner does not sufficiently explain how multiple constructed items can be considered to constitute a single structure just because each one of the multiple items is itself constructed.” Ex. 2006, 17. This is equally true for Mushiga’s memory device, where Petitioner’s picking and choosing different structures to combine into a single structure because they are “constructed” appears to be motivated by hindsight.

154. The Board in the Institution Decision also cited the fact that the combined components are continuous, and can be combined into an “inhomogeneous continuous structure” (DI, 9-30), but that same logic would be true of any combination of adjacent components in a memory device, as the Board appears to have recognized IPR2024-00791. In addition, this argument does not address that Petitioner leaves out other dielectric components (270, 282, 280, 290) that would defeat its mapping, with no discernable logic other than hindsight. As discussed above, if Petitioner were permitted to combine continuous dielectric components and actually included all such continuous dielectric components, that would lead to the alleged TACs not extending through the alleged dielectric structure as required by the Challenged Claims.

155. Therefore, Petitioner has not shown that Mushiga discloses or renders obvious “a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack” as required by limitation [15.c].

(c) Mushiga Does Not Disclose or Render Obvious “TACs extending vertically through the dielectric and the isolation structures” (Limitation [15.h])

156. Mushiga does not disclose or render obvious “*through array contacts (TACs) extending vertically through the dielectric and the isolation structures*” as required by limitation [15.h] because Mushiga’s alleged TACs do not extend through the same structure (the claimed “dielectric structure”).

157. As an initial matter, for all the reasons I explain in §§XII.A.(a)-(b), Mushiga does not disclose or render obvious the claimed isolation structure or the claimed dielectric structure on the isolation structure.

158. In addition, “insulating spacer 586” do not meet this limitation in the same way as Toyama’s “insulating liner 674”—the plurality of TACs do not extend through the same alleged dielectric structure. See §XI.A.(c). For example, each of Mushiga’s TACs has a separate, unconnected insulating spacer 586, which Petitioner improperly combines for the alleged “dielectric structure.” See Pet. 98.

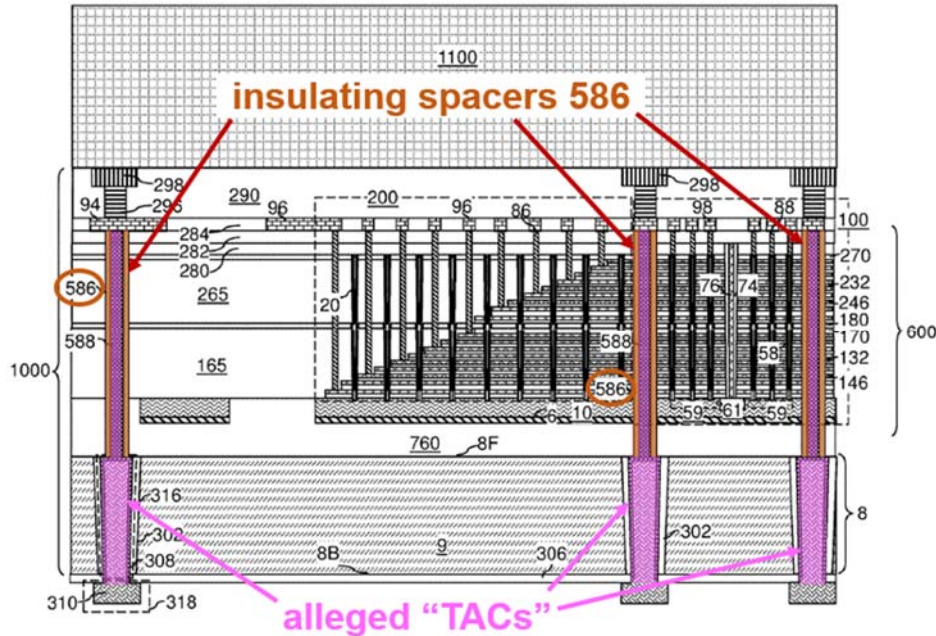


FIG. 11

Ex. 1006, Fig. 11 (annotated).

159. As I discuss in §XI.A.(c), multiple occurrences of a claim element, such as multiple occurrences of insulating spacers 586, cannot be used satisfy a limitation that must be satisfied by a single occurrence of the element.

160. Therefore, Petitioner has not shown that Mushiga discloses or renders obvious “through array contacts (TACs) extending vertically through the dielectric and the isolation structures” as required by limitation [15.h].

C. Claims 17: Mushiga Does Not Disclose or Render Obvious “the dielectric structure comprises a through array contact region of the 3d memory device”

161. Mushiga does not disclose or render obvious “*the dielectric structure comprises a through array contact region of the 3D memory device*” as required

by claim 17 because the alleged TAC region of Mushiga is not within or defined by the alleged dielectric structure as required by claim 17.

162. As I discuss in §VIII.D, the phrase “the dielectric structure comprises a through array contact region of the 3D memory device” means “a region that is within or defined by the dielectric structure and which includes the through array contacts extending through the dielectric structure.”

163. Petitioner’s mapping of the TAC region to Mushiga is not within or defined by the alleged dielectric structure. Instead, Petitioner’s alleged TAC region is an arbitrarily defined region that extends beyond the dielectric structures and the other structures it contains.

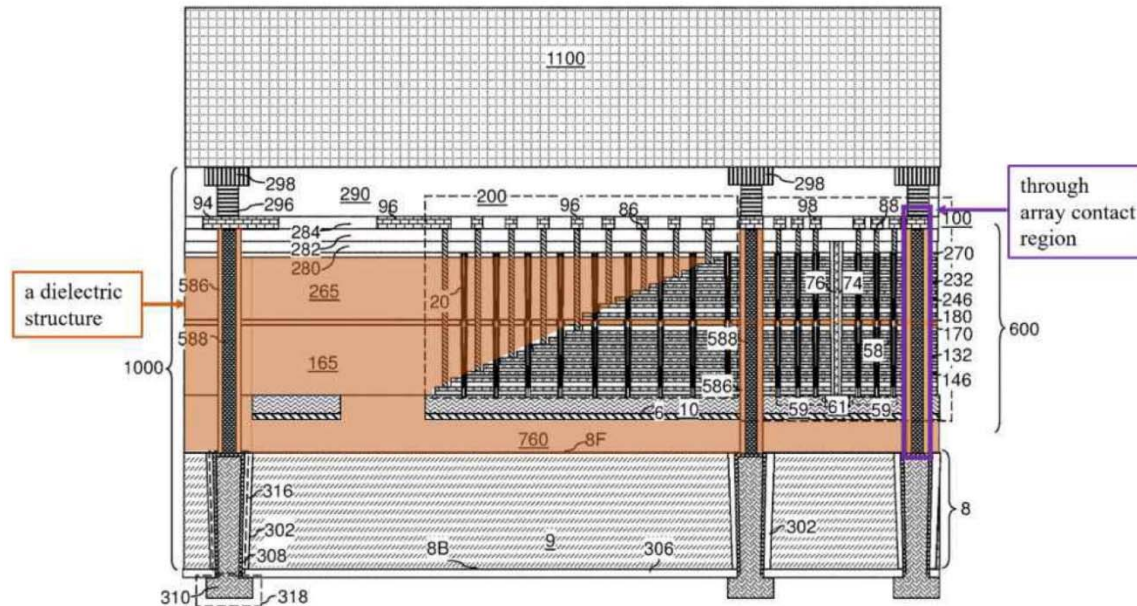


FIG. 11

Ex. 1006, Fig. 11 (annotated by Petitioner at Pet. 100).

164. As seen in the annotated figure, Petitioner's alleged through array contact region is not within or defined by Petitioner's alleged dielectric structure. For example, the alleged region includes portions of metal structures 94 and bonding pad connection via structures 296. Petitioner's mapping does not address these issues. Pet. 100.

165. Therefore, Petitioner has not shown that Toyama's Second Modification discloses or renders obvious "the dielectric structure comprises a through array contact region of the 3D memory device" as required by claim 17.

XIII. PETITIONER'S GROUND 3: MUSHIGA IN VIEW OF MAKALA DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIMS 15-17 AND 19-20

166. Petitioner has not shown that Mushiga in view of Makala discloses or renders obvious limitations [15.a], [15.c], and [15.h] and the additional limitation of dependent claim 17 for the same reasons discussed above for Ground 2. In Ground 3, Petitioner relies on Mushiga in view of Makala as allegedly rendering obvious claims 15-17 and 19-20 of the '378, but the Petition does not raise any new arguments as to limitations [15.a], [15.c], and [15.h] and claim 17. *See* Pet. 102-105. Rather, Petitioner applies Makala's teaching to Mushiga only for limitation [15.g.ii] ("local contacts disposed on ... the slit structures") and "relies solely on Mushiga" for all other limitations. Pet. 102-103. As I explain in §XII, Petitioner in Ground 2 does not show that limitations [15.a], [15.c], and [15.h] and the additional limitation

of dependent claim 17 are disclosed or rendered obvious by Mushiga, and because no additional arguments are introduced in Ground 3 regarding these limitations, the Petition also has not shown that these same limitations are met for Ground 3.

167. Accordingly, Petitioner has not shown that Mushiga in view of Makala discloses or renders obvious limitations [15.a], [15.c], and [15.h] and the additional limitation of dependent claim 17 in Ground 3.

II. CONCLUSION

168. For at least the reasons discussed above, it is my opinion that Petitioner has not demonstrated that any of the Challenged Claims of the '378 patent are anticipated or obvious.

169. This declaration represents my opinions that I have formed to date on the specific issues for which I have been asked to opine and based on the material currently available to me. I reserve the right to supplement this declaration to address any new information offered by Petitioner or provided by the Board. Also, I reserve the right to supplement this declaration insofar as Petitioner is permitted to supplement the record with any additional opinions or arguments.

170. I hereby declare that all statements made herein of my own knowledge are true and all statements made herein on information and belief were and are believed by me to be true, and that all statements herein were and are made with the knowledge that willful false statements and the like so made are punishable by fine

or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that any such willful false statements may jeopardize the validity of the application or any patents issued thereon.

APPENDIX A

Woodward Yang

Home Address

14 Fox Run Lane
Lexington, MA 02420
(781) 863-1407
(617) 512-0296 cell

Work Address

Science Engineering Complex 5.440
School of Engineering and Applied Sciences
Harvard University
Cambridge, MA 02138
Tel: (617) 495-3987

Education:

Massachusetts Institute of Technology August 1990
Ph.D. in Electrical Engineering and Computer Science
Thesis: "The Architecture and Design of CCD Processors for Computer Vision"

Massachusetts Institute of Technology January 1987
S.M. in Electrical Engineering and Computer Science
Thesis: "Low Pressure Nitrided Oxide in MOS Capacitors"

University of California, Berkeley May 1984
B.S. in Electrical Engineering and Computer Science

Research and Professional Experience:

Professor of Electrical Engineering and Computer Science
School of Engineering and Applied Sciences, Harvard University
Gordon McKay Professor September 1997 - present
Associate Professor September 1994 - 1997
Assistant Professor September 1990 - 1994

Analysis, design and implementation of microelectronic circuits and VLSI systems.
Teaching and curriculum planning in electrical engineering and computer science.

Founder and Program Director September 2015 - May 2020
Master in Design Engineering at Harvard University
Collaborative 2-year degree program at Harvard Graduate School of Design and School of Engineering and Applied Sciences

HBS University Fellow and Visiting Professor September 2008 – May 2012
Harvard Business School
Research and teaching in disruptive innovation, technology transfer, and industry evolution.

Founder and CEO March 2000 – March 2008
Silicon7, Incorporated
Seongnam-si, Kyoungki-do, KOREA
Application Specific Memory products for mobile communications and computing platforms.

Science and Technology Board Member June 1998 – June 2001
Polaroid Corporation, Cambridge, Massachusetts
Evaluation of research and technology developments.

Consultant and Senior Fellow Hyundai Electronics Industries, Ichon, Korea Development of high performance CMOS image sensor technology for embedded image sensing and processing applications. Research on advanced DRAM design and merged memory logic (MML) technology for advanced computer systems.	August 1995 – March 2000
Consultant Hamamatsu Photonics K.K., Hamamatsu City, Japan Development of smart image sensors and CCD/CMOS analog charge-domain circuitry.	December 1993 - June 1998
Consultant Istituto per la Ricerca Scientifica e Tecnologica (IRST), Trento, Italy Research and development of advanced CMOS/CCD technology and circuitry.	June 1991 - December 1993
Consultant M.I.T. Lincoln Laboratory, Dr. Alice M. Chiang, Advisor Design and implementation of CCD image sensors and analog signal processors.	June 1988 - August 1990
Research Assistant M.I.T. Artificial Intelligence Laboratory, Professor Tomaso Poggio, Advisor Implementation of analog VLSI hardware for computer vision.	September 1987 - August 1990
Research Assistant M.I.T. Microsystems Technology Laboratory, Professor Charles G. Sodini, Advisor Development and characterization of low pressure ammonia and oxygen annealing process for improved reliability of scaled MOS transistors.	September 1984 - August 1987
Research Assistant U.C. Berkeley Electronic Research Laboratory, Professor Chenming Hu, Advisor Measurement and analysis of hot electron degradation in MOS transistors.	January 1983 - May 1984

Honors and Awards:

National Science Foundation Young Investigator Award	1992
Army Research Office Young Investigator Award	1992
Hertz Foundation Fellowship	1984 – 1990
National Science Foundation Fellowship	1984
University of California Alumni Scholarship	1980 - 1984
Phi Beta Kappa, Eta Kappa Nu, Tau Beta Pi	1984

Patents:

Method and Charge--Coupled Apparatus for Algorithmic Computations, Woodward Yang, May 12, 1992, U.S. Patent No. 5,113,365.

Image Sensor Array With Threshold Voltage Detectors and Charged Storage Capacitors, Woodward Yang, May 25, 1993, U.S. Patent No. 5,214,274.

Error Correcting Sigma-Delta Modulation Decoding, Philip Steiner and Woodward Yang, November 17, 1998, U.S. Patent No. 5,838,272.

CMOS image sensor with equivalent potential diode, Woodward Yang, Ju Il Lee and Nan Yi Lee, February 26, 1999, US Patent No. 6,180,969.

CMOS image sensor with equivalent potential diode and method for fabricating the same, Woodward Yang, Ju Il Lee and Nan Yi Lee, February 26, 1999, US Patent No. 6,184,055.

CMOS image sensor with testing circuit for verifying operation thereof, Oh Bong Kwon, Woodward Yang, Suk Joong Lee, and Gyu Tae Hwang, February 26, 1999, US Patent No. 6,633,335.

Antifuse circuitry for post-package DRAM repair, Woodward Yang, et al., January 10, 2000, US Patent No. 6,240,033.

Image sensor with analog-to-digital converter that generates a variable slope ramp signal, Kang Jin Lee, Chan Ki Kim, Jae Won Eom and Woodward Yang, February 8, 2001, US Patent No. 6,545,624.

Error-correcting circuit for high density memory, Elaine Ou and Woodward Yang, June 9, 2009, US Patent No. 7,546,517.

Selected Presentations, Interviews and Invited Lectures:

"Chip Industry must learn not to overshoot," EE Times cover page, interview and commentary, June 6, 2006.

"Disruptive Innovation," Keynote Speaker at Consumer Electronics Show, January 2006.

"Using DRAM Technology to Make SRAM," The Weekly Economist interview, September 24, 2002.

"Silicon7 8-Mbit SRAM sports single-transistor cell," EE Times interview, September 2001.

"Hyundai modifies DRAM process to produce CMOS image sensors," EE Times interview, March 1999.

"Merged Memory Logic," W. Yang, IEEE Solid-State Circuits Society Distinguished Lecturer, Hanyang University, Korea, March 1999.

"The Dawn of Billion Transistor Chips," W. Yang, 1998 Korea - U.S. Science and Technology Symposium: Computing and Telecommunication, Chicago, April 1998.

"Innovation in Microelectronic Manufacturing," W. Yang, National Research Council Workshop on the Electronics Industry, November 1997.

"Trends in Electronic Image Sensing and Processing," IEEE Laser and Electro Optical Society, Lincoln, MA, March 1996.

Selected Depositions and Trial Testimonies:

In the matter of CERTAIN ELECTRONIC DEVICES, INCLUDING MOBILE PHONES, PORTABLE MUSIC PLAYERS, AND COMPUTERS (ITC, Investigation No. 337-TA-701, deposition and trial) – retained by Nokia

In the matter of APPLE, INC. vs. SAMSUNG ELECTRONICS COMPANY, LTD. (United States District Court, Northern District of California, Civil Action No. 11-CV-01846-LHK, deposition and trial) – retained by Samsung

In the matter of CERTAIN CONSUMER ELECTRONICS WITH DISPLAY AND PROCESSING CAPABILITIES, (ITC, Investigation No. 337-TA-885, deposition and trial) – retained by Toshiba

In the matter of CERTAIN GRAPHICS PROCESSING CHIPS, SYSTEMS ON A CHIP, AND THE PRODUCTS CONTAINING THE SAME, (ITC, Investigation No. 337-TA-941, deposition and trial) – retained by Nvidia

In the matter of US Patent 6,418,310 (US Patent and Trademark Office, Patent Trial and Appeal Board, IPR2015-05183, deposition) – retained by Ericsson Inc.

In the matter of United States of America, Plaintiff, v. Fujian Jinhua Integrated Circuit Co., LTD, Defendant (United States District Court - Northern District of California, Criminal Action No. 18-cr-00465-MMC, trial) – retained by Fujian Jinhua

Publications:

"Cambridge NanoTech," Woodward Yang and David Kiron, Harvard Business School Case Study 9-610-083, Boston, MA, Harvard Business School, May 2010.

"Science and Technology Entrepreneurship for Greater Societal Benefit: Ideas for Curricular Innovation," Fleming, Lee, Woodward Yang, and John Golden in **Spanning Boundaries and Disciplines: University Technology Commercialization in the Information Age**, edited by Gary D. Libecap, Marie Thursby and Sherry Hoskinson, Emerald Group Publishing Limited, 2010.

"The New Economics of Semiconductor Manufacturing," Clayton Christensen, Steve King, Matt Verlinden and Woodward Yang, **IEEE Spectrum**, vol. 45, issue 5, pp. 24-29 May 2008.

"Energy Consumption Model for Power Management in Wireless Sensor Networks," Qin Wang and Woodward Yang, *IEEE Communications Society Conference on Sensor, Mesh and Ad Hoc Communications and Networks SECON 2007*, June 2007.

"A Realistic Power Consumption Model for Wireless Sensor Network Devices," Qin Wang, Mark Hempstead and Woodward Yang, *IEEE Communications Society Conference on Sensor, Mesh and Ad Hoc Communications and Networks SECON 2006*, September 2006.

"Fast Error-Correcting Circuits for Fault-Tolerant Memory," E. Ou and W. Yang, *IEEE International Workshop on Memory Technology, Design and Testing*, pp. 8-12, August 2004.

"A Low-Power 256-Mb SDRAM with an On-Chip Thermometer and Biased Reference Line Sensing Scheme," J.P. Kim, W. Yang, and H.-Y. Tan, **IEEE Journal of Solid-State Circuits**, vol. 38, no. 2, pp. 329-337, February 2003.

"An Antifuse EPROM Circuitry Scheme for Field-Programmable Repair in DRAM," J.K. Wee, W. Yang, E.K. Ryou, J.S. Choi, S.H. Ahn, J.Y. Chung and S.C. Kim, **IEEE Journal of Solid-State Circuits**, vol. 35, no. 10, pp. 1408-1414, October 2000.

"An Embeddable Low Power SIMD Processor Bank," S.-H. Hong and W. Yang, *Digest of Technical Papers of IEEE International Solid-State Circuits Conference*, pp. 192-193, February 2000.

"Antifuse EPROM Circuit for Field Programmable DRAM," J.-S. Choi, J.-K. Wee, P.-J. Kim, J.-K. Oh, C.-H. Lee, H.-Y. Cho, J.-Y. Chung, S.-C. Kim and W. Yang, *Digest of Technical Papers of IEEE International Solid-State Circuits Conference*, pp. 406-407, February 2000.

"A Novel Double Slope Analog-to-Digital Converter for a High-Quality 640 x 480 CMOS Imaging System," O.-B. Kwon, K.-N. Park, D.-Y. Lee, K.-J. Lee, S.-C. Jun, C.-K. Kim, and W. Yang, *6th International Conference on VLSI and CAD 1999*, pp. 335-338, Seoul, Korea, October 1999.

"An Improved Digital CMOS Imager," O.-B. Kwon, K.-N. Park, D.-Y. Lee, K.-J. Lee, S.-C. Jun, C.-K. Kim, Y.-B. Lee and W. Yang, *IEEE Workshop on Charged-Coupled Devices and Advanced Image Sensors*, Nagano, Japan, June 1999.

- "A Linear-Response, High-Dynamic Range CMOS Imager Suitable for Spectroscopic Applications," D. Qian and W. Yang, *IEEE Workshop on Charged-Coupled Devices and Advanced Image Sensors*, Nagano, Japan, June 1999.
- "New Self Refresh Scheme Using Cell Leakage Monitoring Circuit," Y.-H. Seol, H.-Y. Cho, J.-K. Wee, D.-H. Ryu, J.-G. Oh, J.-S. Choi, J.-J. Lee, J.-H. Lee, and W. Yang, (in Korean) *Proceedings of the 6th Korean Conference on Semiconductors*, pp. 377-378, Seoul, Korea, February 1999.
- "High Voltage Circuitry for Post Package DRAM Repair," P.-J. Kim, J.-G. Oh, J.-K. Wee, D.-H. Ryu, Y.-H. Seol, H.-Y. Cho, J.-S. Choi, J.-H. Han, J.-H. Lee, and W. Yang, (in Korean) *Proceedings of the 6th Korean Conference on Semiconductors*, pp. 385-386, Seoul, Korea, February 1999.
- "An Integrated 800 x 600 CMOS Imaging System," W. Yang, O.-B. Kwon, J.-I. Lee, G.-T. Hwang and S.-J. Lee, *Digest of Technical Papers of IEEE International Solid-State Circuits Conference*, pp. 304-305, February 1999.
- "VLSI Hardware for Example-Based Learning," A. Lipman and W. Yang, **IEEE Transactions on VLSI Systems**, vol. 5, no. 3, pp. 320-328, September 1997.
- "A Reconfigurable VLSI Coprocessing System for the Block Matching Algorithm," A. Bugeja and W. Yang, **IEEE Transactions on VLSI Systems**, vol. 5, no. 3, pp. 329-337, September 1997.
- "A CCD/CMOS Image Sensor Array with Integrated A/D Conversion," M. Gottardi and W. Yang, *Proceedings of the IEEE International Symposium on Circuits and Systems*, Vol. III, pp. 1908-1911, June 1997.
- "Circuit integration pushes image sensor performance," W. Yang, **Laser Focus World**, Penwell Publishing, pp. 129-139, February 1997.
- "A Framework for Analysis of High Order Sigma-Delta Modulators," P. Steiner and W. Yang, **IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing**, vol. 44, no. 1, pp. 1-12, January 1997.
- "Competitive learning algorithms for channel optimized vector quantizers," D. Martinez and W. Yang, *The 1996 IEEE International Conference on Neural Networks*, pp. 1462-1467, June 1996.
- "Stability of High Order Sigma-Delta Modulators," P. Steiner and W. Yang, *Proceedings of IEEE International Symposium on Circuits and Systems*, Vol. III, pp. 52-57, May 1996.
- "Simple Pulse Asynchronous State Machines," J. Miller and W. Yang, *Proceedings of IEEE International Symposium on Circuits and Systems*, Vol. III, pp. 405-409, May 1996.
- "Neuromorphic CMOS Circuitry for Active Bidirectional Delay Lines," W. Yang, *Proceedings of IEEE International Symposium on Circuits and Systems*, Vol. III, pp. 473-476, May 1996.
- "A Robust Backward Adaptive Quantizer," D. Martinez and W. Yang, *Proceedings of IEEE Workshop on Neural Networks for Signal Processing V*, pp. 531-540, August 1995.
- "A Real-Time Face Recognition System Using Machine Vision Techniques," W. Yang, invited paper, *CardTech/SecurTech Conference Proceedings*, pp. 179-193, April 1995.
- "Stability Analysis of the Second Order Sigma-Delta Modulator," P. Steiner and W. Yang, *Proceedings of IEEE International Symposium on Circuits and Systems*, Vol. V, pp. 365-368, June 1994.
- "An Interline CCD Imaging Array with On-Chip A/D Conversion," D. J. Friedman and W. Yang, *Proceedings of SPIE, Charge-Coupled Devices and Solid State Optical Sensors IV*, vol. 2172, pp. 54-63, February 1994.

"A Wide Dynamic Range, Low Power Photosensor Array," W. Yang, *Digest of Technical Papers of IEEE International Solid--State Circuits Conference*, pp. 230-231, February 1994.

"A Real--Time Face Recognition System Using Custom VLSI Hardware," J.M. Gilbert and W. Yang, *Proceedings of IEEE Workshop on Computer Architectures for Machine Perception*, pp. 58-66, December 1993.

"A CCD/CMOS Image Motion Sensor," M. Gottardi and W. Yang, *Digest of Technical Papers of IEEE International Solid--State Circuits Conference*, pp. 194-195, February 1993.

"Analog CCD Processors for Image Filtering," W. Yang, *Proceedings of SPIE, Visual Information Processing: From Neurons to Chips*, vol. 1473, pp. 114-127, April 1991.

"The MIT Vision Chip Project: Analog VLSI Systems for Fast Image Acquisition and Early Vision Processing," J.L. Wyatt, D.L. Standley, and W. Yang, *Proceedings of the International Conference on Robotics and Automation*, vol. 2, pp. 1330-1335, April 1991.

"A Full Fill--Factor CCD Imager with Integrated Signal Processors," W. Yang and A.M. Chiang, *Digest of Technical Papers of International Solid--State Circuits Conference*, pp. 218-219, February 1990.

"A Charge--Coupled Device Architecture for On Focal Plane Image Signal Processing," W. Yang, *Proceedings of International Symposium on VLSI Technology, Systems, and Applications*, pp. 266-270, May 1989.

"Optical Flow: Computational Properties and Networks, Biological and Analog," Tomaso Poggio, Woodward Yang, and Vincent Torre, **The Computing Neuron**, R. Durbin, C. Maill, and G. Mitchison (editors), pp. 255-370, Addison--Wesley, New York, 1989.

"Optimization of Low Pressure Nitridation/Oxidation of SiO₂ for Scaled MOS Devices," W. Yang, R. Jayaraman, and C.G. Sodini, **IEEE Transactions on Electron Devices**, vol. ED-35, no. 7, pp. 935-944, July 1988.

"Radiation Effects in Low Pressure Reoxidized Nitrided Oxide Gate Dielectrics," G. Dunn, R. Jayaraman, W. Yang, and C.G. Sodini, **Applied Physics Letters**, vol. 52, no. 20, pp 1713-1715, May 1988.

"The MIT Vision Machine," T. Poggio, J. Little, E. Gamble, W. Gillet, D. Geiger, D. Weinshall, M. Villalba, N. Larson, T. Cass, H. Bulthoff, M. Drumheller, P. Oppenheimer, W. Yang, and A. Hurlbert, *DARPA Image Understanding Workshop*, pp. 177-198, April 1988.

"MOS Electrical Characteristics of Low Pressure Re--oxidized Nitrided Oxide," R. Jayaraman, W. Yang, and C.G. Sodini, *Technical Digest of International Electron Devices Conference*, pp. 668-671, December 1986.

"Hot Carriers Induced Degradation in Thin Gate Oxide MOSFET's," M--S. Liang, C. Chang, W. Yang, C. Hu, and R.W. Brodersen, *Technical Digest of International Electron Devices Conference*, pp. 186-189, December 1983.