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Paper 11
Date: November 27, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00791
Patent 10,937,806 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and MICHAEL T. CYGAN, *Administrative Patent Judges.*

McGRAW, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Micron Technology, Inc. ("Petitioner") filed a Petition to institute an *inter partes* review of claims 8, 9, 11, and 12 of U.S. Patent No. 10,937,806 B2 ("the '806 patent," Ex. 1001). Paper 1 ("Pet."). Yangtze Memory Technologies Company, Ltd. ("Patent Owner") filed a Preliminary Response. Paper 10 ("Prelim. Resp.").

Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314 (2018); *see also* 37 C.F.R. § 42.4 (2023). For the reasons discussed below, we determine that at least one of Petitioner's arguments regarding Toyama (alternative argument 2[1]) establishes a reasonable likelihood of prevailing with respect to the unpatentability of at least one claim of the '806 patent. Accordingly, we institute an *inter partes* review of claims 8, 9, 11, and 12 of the '806 patent on all of Petitioner's asserted arguments regarding Toyama.

A. Real Parties in Interest

Petitioner identifies itself and its subsidiaries, including Micron Consumer Products Group LLC, as the real parties in interest. Pet. 5. Patent Owner identifies itself as the real party in interest. Paper 3 (Mandatory Notice), 2.

B. Related Matters

The parties indicate that the '806 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL

[1] *See* Pet. 27–56 (alternative argument 1), 56–95 (alternative argument 2), 96–122 (alternative argument 3).

(N.D. Cal.). Pet. 5; Paper 3, 2. Petitioner states it filed IPRs challenging other patents asserted in the district court cases, namely U.S. Patent Nos. 10,950,623 (IPR2024-00794), 10,658,378 (IPR2024-00788), 10,861,872 (IPR2024-00789), 10,868,031 (IPR2024-00790), 11,501,822 (IPR2024-00795), 11,468,957 (IPR2024–00792), and 11,600,342 (IPR2024-00793). Pet. 5–6.

C. The '806 Patent

The '806 patent, titled "Through Array Contact (TAC) for Three-Dimensional Memory Devices" relates to "a channel hole plug structure of three-dimensional (3D) memory devices and a method for forming the same." Ex. 1001, code (54), 1:18–20. An embodiment of the 3D memory device is illustrated in Figure 2 of the '806 patent and is reproduced below.

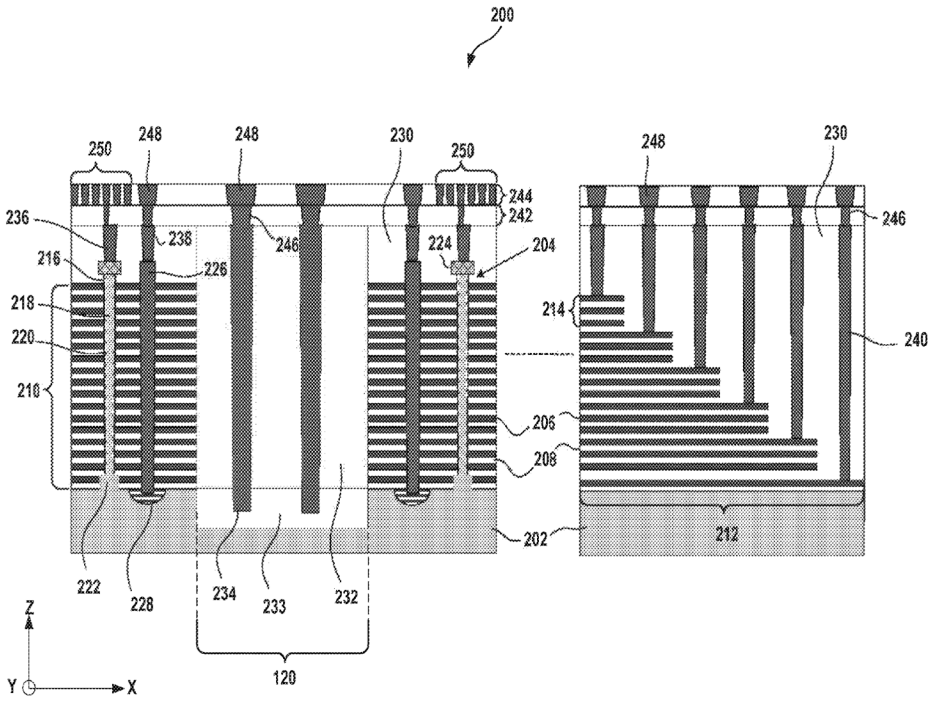

FIG. 2

Figure 2 "is a cross-sectional view of an exemplary 3D memory device 200" disclosed in the '806 patent. Ex. 1001, 3:41–42.

Memory device 200 can be a "NAND Flash memory device[2] in which memory cells are provided in the form of an array of NAND strings 204 extending vertically above substrate 202." *Id.* at 8:17–20. "The array device can include a plurality of NAND strings 204 that extend through a plurality of conductor layer 206 and dielectric layer 208 pairs" that alternate in the vertical direction, also referred to as " 'alternating conductor/dielectric stack' 210." *Id.* at 8:20–31. Alternating conductor/dielectric stack 210 can include staircase structure 212, where each "level" or "step" 214 can include one or more conductor/dielectric layer pairs stacked. *Id.* at 8:54–59. "The top layer in each level 214 of staircase structure 212 is a conductor layer 206 available for interconnection in the vertical direction (e.g., along the z-axis)." *Id.* at 8:61–63. Figure 2 also shows "channel structure 216 that extends through alternating conductor/dielectric stack 210" that is filled with semiconductor materials and dielectric materials. *Id.* at 9:7–12. The embodiment illustrated in Figure 2 also includes slit structures 226 that also extend through alternating conductor/dielectric stack 210 and may extend along the y-axis to separate alternating conductor/dielectric stack into multiple blocks. *Id.* at 9:54–58.

Figure 2 also illustrates through array contacts ("TACs") 234, extending vertically through dielectric structure 232, which are within a TAC region 120 that can have, but are not limited to, a rectangle or square shape. *Id.* at 10:55–64. "TACs 234 can carry electrical signals from and/or

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[2] Though not explicitly defined in the specification, Petitioner's declarant states that "[t]he acronym 'NAND' refers to a 'not-AND' logic gate, and NAND flash memory is a particular type of flash memory where the memory cells form a structure similar to that of a NAND gate." Ex. 1003 ¶ 42.

to 3D memory device 200" and "can provide electrical connections between the 3D memory device 200 and the peripheral device." *Id.* at 11:8–14.

D. Illustrative Claim

Petitioner challenges claims 8, 9, 11, and 12 of the '806 patent. Claim 8, the only independent claim challenged, is illustrative of the claimed subject matter and is reproduced below.

> 8. [1.PRE] A three-dimensional (3D) memory device, comprising:
>
> [8.A] an alternating conductor/dielectric layer stack;
>
> [8.B.i] a dielectric structure [8.B.ii] extending vertically through the alternating conductor/dielectric layer stack;
>
> [8.C] first and second channel regions comprising first and second pluralities of channel structures, respectively;
>
> [8.D] slit structures extending vertically through the alternating conductor/dielectric layer stack;
>
> [8.E] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;
>
> [8.F] local contacts disposed on the first and second channel structures and the slit structures;
>
> [8.G] a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and
>
> [8.H] a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.

Ex. 1001, 23:54–24:8 (bracketed material added).

E. Asserted Ground

Petitioner asserts that claims 8, 9, 11, and 12 would have been unpatentable on the following ground:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
8, 9, 11, 12	103[3]	Toyama[4]

Pet. 6–7. Petitioner presents three alternative arguments that claims 8, 9, 11, and 12 would have been obvious over Toyama, relying on different structures and modifications to support each arguments. Pet. 27–56 (alternative argument 1), 56–95 (alternative argument 2), 96–122 (alternative argument 3). Petitioner relies on the Declaration of Jack C. Lee, Ph. D. ("Lee Dec.," Ex. 1003) in support of its contentions.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art ("POSITA") would have had "a bachelor of science degree in electrical engineering or a similar discipline" with "2–3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience)." Pet. 27 (citing Ex. 1003 ¶¶ 34–38). Petitioner further contends that a "POSITA would also have been aware of and generally

[3] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112–29, 125 Stat. 284 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the '806 patent has an effective filing date after March 16, 2013 (Ex. 1001, codes (22), (63)), we refer to the AIA version of Sections 102 and 103.
[4] Toyama, US Pub. No. 2017/0179026 A1, published June 22, 2017 (Ex. 1005).

knowledgeable about semiconductor manufacturing and 3D NAND's structure, its component parts, how it operates, and how it is controlled." *Id*.

At this stage of the proceeding, Patent Owner neither responds to Petitioner's proposed definition, nor provides a definition of its own. *See generally*, Prelim. Resp. Petitioner's undisputed proposed definition appears to be consistent with the cited prior art and the disclosure of the '806 patent, and we adopt it for purposes of this Decision.

B. Claim Construction

We construe claims challenged in an *inter partes* review proceeding, "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b)," including construing the claims "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data LLC v. Iancu*, 912 F.3d 1348, 1375 (Fed. Cir. 2019).

Petitioner states that the claims should be construed according to their plain and ordinary meaning but does not propose any express construction. Pet. 27 (citing Ex. 1003 ¶ 75). Patent Owner also does not propose any express construction of the claims at this stage of the proceeding, but does reserve the right to raise claim construction issues during trial. *See* Prelim. Resp. 10–11. Patent Owner further states that the joint claim construction

statement filed in the parallel district court proceeding does not impact any issue raised in its Preliminary Response. *Id.* at 11 (citing Ex. 2001).

Claim 8 recites "a dielectric structure extending vertically through the alternating conductor/dielectric layer stack" and "a plurality of through array contacts (TACs) extending vertically through the dielectric structure." Ex. 1001, 23:54–24:8. The parties dispute whether Toyama discloses or suggests the claimed dielectric layer. To the extent the parties' arguments raise issues of claim construction, we address these issues in the context of the patentability discussion below. No other terms require express construction to resolve any issue in dispute at this stage of the proceeding. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *see also Nidec Motor Corp. v. Zhongshan Board Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

C. Obviousness over Toyama

As noted above, Petitioner presents three alternative arguments that claims 8, 9, 11, and 12 would have been obvious over Toyama. Pet. 27–56 (alternative argument 1), 56–95 (alternative argument 2), 96–122 (alternative argument 3). We address Toyama and each of these arguments below.

1. Toyama

Toyama is titled "Through-Memory-Level Via Structures For a Three-Dimensional Memory Device." Ex. 1005, code (54). Toyama relates to three-dimensional NAND memory devices, such as vertical NAND strings, and describes four exemplary structures and modifications thereof. *Id.* ¶¶ 4, 14–155; Prelim. Resp. 13. Toyama's "first exemplary structure" is illustrated in Figures 1 through 17. *Id.* ¶¶ 14–48, 163–260, Figs. 1–17.

Figure 11A, reproduced below, depicts the first exemplary structure after formation of a through-memory-level opening. *Id.* ¶ 30.

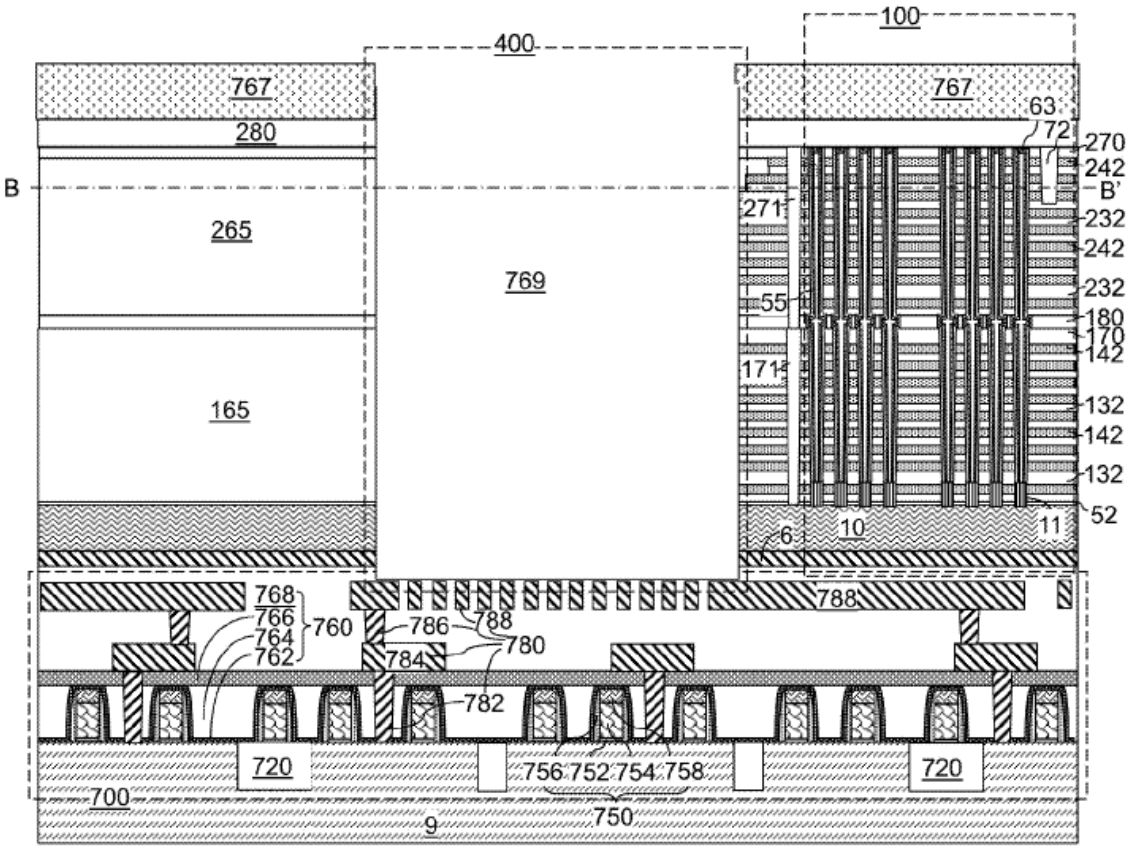


FIG. 11A

Figure 11A is a vertical cross-sectional view of the first exemplary structure according to the first embodiment of the disclosure. *Id.* ¶ 30.

At least one dielectric layer 760 is formed over the semiconductor devices, and lower level metal interconnect structures 780 formed thereon to function as landing pads for through-memory-level via structures. *Id.* ¶ 164. Upon these structures in underlying peripheral region 700 (those having numbers in the 700s), a planar semiconductive layer 10 is formed. On semiconductor layer 10 is an alternating stack of conductive layers 146, 246 (replacing sacrificial material layers 142, 242) and insulating layers 132, 232. *Id.* ¶¶ 172, 196, 228. In portions of the alternating stack, supporting

pillar structures 171 are formed, and other portions of the dielectric stack appear as a stepped region. *Id.* ¶ 182, Fig. 4B. In the stepped region, a through-memory-level opening 769 can extend from the top of the device down to the lower level metal interconnect structures 780 in peripheral region 700. *Id.* ¶ 213. A dielectric fill material portion is formed within each through-memory-level opening 769. *Id.* ¶ 216.

Toyama also describes a "second modification of [a] fourth exemplary structure" ("Second Modification") illustrated in Figures 44A through 49. Ex. 1005 ¶¶ 93–103. Figure 49 is shown below:

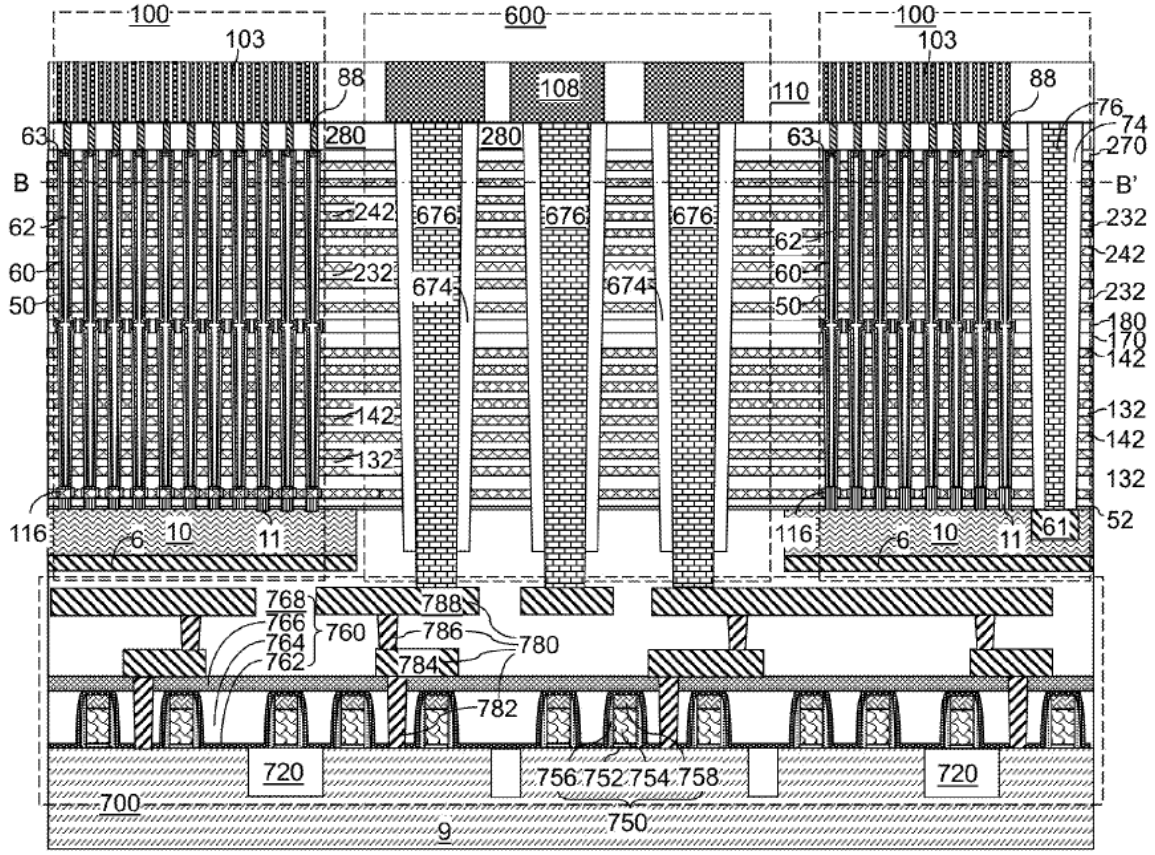


FIG. 49

Figure 49 is a vertical cross-sectional view of Toyama's second modification of its fourth exemplary structure after formation of upper level metal interconnect structures. Ex. 1005 ¶ 103. Shown in Figure 49 is

semiconductor substrate 9 having peripheral region 700, upon which planar semiconductive layer 10 is formed having an alternating stack of conductive layers 146, 246 (replacing sacrificial material layers 142, 242) and insulating layers 132, 232. *Id.* ¶¶ 310–311, 332. Multiple through-memory-level openings 676, surrounded by insulating liners 674, are created within the alternating stack. *Id.* ¶¶ 339–341.

2. Asserted Obviousness over Toyama's Second Modification to its Fourth Exemplary Structure (Alternative Argument 1)

Petitioner argues that claims 8, 9, 11, and 12 would have been obvious over Toyama's second modification to its fourth exemplary structure ("Second Modification"). Pet. 27–56. Patent Owner opposes. For the reasons stated below, Petitioner has not shown a reasonable likelihood that claims 8, 9, 11, or 12 would have been obvious over Toyama's Second Modification.

(a) Claim 8

(1) Petitioner's Contentions

Petitioner contends that Toyama's Second Modification discloses or suggests all elements of independent claim 8. Pet. 27–54. In particular, Petitioner asserts that Toyama's Second Modification is a "three-dimensional non-volatile memory device[]" having an "alternating stack (132, 146, 232, 246)" of "electrically conductive layers" and "insulating layers" as recited in the preamble and claim element [8.A]. *Id.* at 28–29 (citing Ex. 1005 ¶¶ 156, 337, 340, Figs. 45A, 46A, 49; Ex. 1003 ¶¶ 86–89).

Petitioner asserts that Toyama's "insulating liners 674," highlighted orange in Toyama's Figure 49 below, are "a dielectric structure extending vertically" through the alternating conductor/dielectric stack (highlighted green and yellow), as recited in claim element [8.B.i–8.B.ii]. Pet. 29–33

(citing, *inter alia*, Ex. 1005, Fig. 49, ¶¶ 233, 338–340, 381; Lee ¶¶ 91–94, 97).

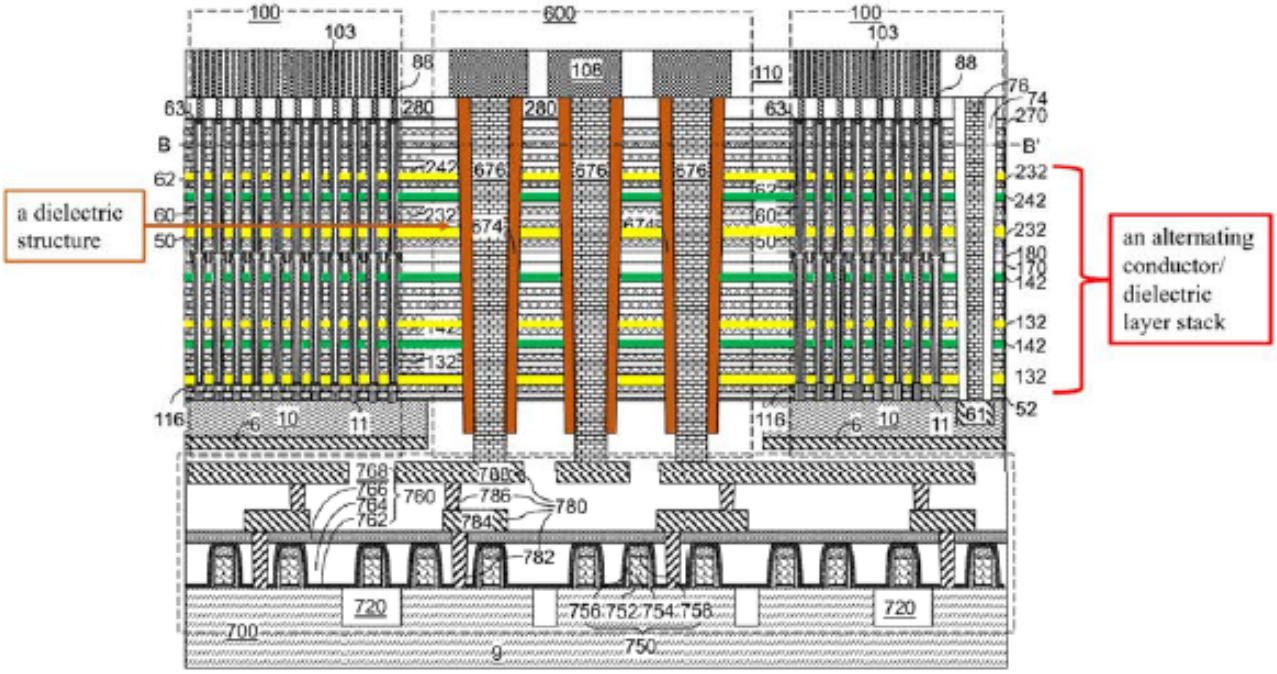


FIG. 49

Toyama's Figure 49, with Petitioner's annotations added, depicts alternating stack 132, 142/146, 232, 242/236[5] (green and yellow) and insulating liners 674 (orange). Pet. 33; Ex. 1005, Fig. 49; Ex. 1003 ¶ 97.

Petitioner states that the three insulating liners (elements 674) in Toyama together are a single dielectric structure as recited in claim element [8.B] at least because the liners "have the same function" and the "components together are something 'that is constructed.'"[6] Pet. 31–32

[5] Petitioner asserts that a POSITA would have understood that elements 142 and 242 in Figure 49, as well as Figures 47A and 48A, were mislabeled and were intended to be labeled 146 and 246 respectively. Pet. 28 n.2 (citing Ex. 1003 ¶ 88).

[6] Petitioner cites to Merriam-Webster's definition of a structure as "something ([such] as a building) that is constructed." Pet. 31–32 (modifications in Pet.).

(citing Ex. 1021, 4; Ex. 1003 ¶ 94). Petitioner also states that although the three insulating liners 674 are collectively a single structure, not multiple structures, the claim is opened ended and, therefore, encompasses a device with multiple dielectric structures. *Id.* at 32 n.4 (citing *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1356 (Fed. Cir. 2000) as stating that use of an indefinite article "a" or "an" means "one or more" in open-ended claims containing the transitional phrase comprising).

Regarding claim element [8.C], Petitioner maps Toyama's "memory array region 100" and "memory stack structures 55," shown in Figures 48B and 49, to the "first and second channel regions comprising first and second pluralities of channel structures, respectively." *Id.* at 33–36 (citing Ex. 1005 ¶¶ 210, 323, 333, 388, Figs. 48B, 49; Ex. 1003 ¶¶ 98–100). Petitioner asserts that the "slit structures extending vertically through the alternating conductor/dielectric layer stack" as recited in claim element [8.D] maps to the "laterally-elongated contact via structures 76" in Toyama and that the slit structures extend vertically through the "alternating stack (132, 146, 232, 246)." *Id.* at 36–39 (citing, *inter alia*, Ex. 1005 ¶¶ 237, 241, 318–320, Figs. 48B, 49; Ex. 1003 ¶¶ 102–104).

Petitioner also contends that Toyama's staircase regions, which contain "conductor layer[s]," shown in Figure 17C, discloses or suggests the "staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon" recited in claim element [8.E]. *Id.* at 39–41 (citing Ex. 1005 ¶ 232, Fig. 17C; Ex. 1003 ¶¶ 105–107); *see also id.* at 41 (stating a POSITA would have understood that Toyama's Second Modification also teaches the above citations to Toyama's first exemplary structure, depicted in Figure 17C).

Claim element [8.F] recites "local contacts disposed on the first and second channel structures and the slit structures." Petitioner asserts that Toyama's "drain contact via structures 88" contacting or extending above the "memory stack structures 55" discloses the recited "local contacts disposed on the first and second channel structures." Pet. 41–42 (mapping Toyama's drain contact structures 88 to "local contacts" and Toyama's memory stack structures to "channel structures" and citing Ex. 1005 ¶ 251, Fig. 49; Ex. 1003 ¶ 109).

Petitioner admits that Toyama's description of its Second Modification does not expressly disclose local contacts (source connection via structures 91) disposed on the slit structures ("laterally-elongated contact via structures 76) as recited in claim element [8.F]. Pet. 43. Petitioner, however, asserts that a POSITA would have understood that the Second Modification includes, or would have rendered obvious, local contacts disposed on the slit structures (source connection via structures 91) to provide a higher-level source connection in order for via structures to serve as source lines for source region 61. Pet. 43–44 (citing Ex. 1005 ¶¶ 250, 342, 382; Ex. 1003 ¶¶ 110–112).

Claim element [8.G.i–iii] requires: [i] "a through array contact (TAC) region" [ii] "formed between the first and second channel regions" [iii] "wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure." Ex. 1001, 24:1–5. Petitioner asserts Toyama's Second Modification, shown in Figure 49 below, depicts a through array contact (TAC) region (part of

"through-memory-level via region 600")[7] that is formed between first and second channel regions ("first and second parts of 'memory array region 100'"). *Id.* at 44–48 (citing Ex. 1005, ¶¶ 334, 378, Figs. 48B, 49; Ex. 1003 ¶¶ 113–114, 116–117).

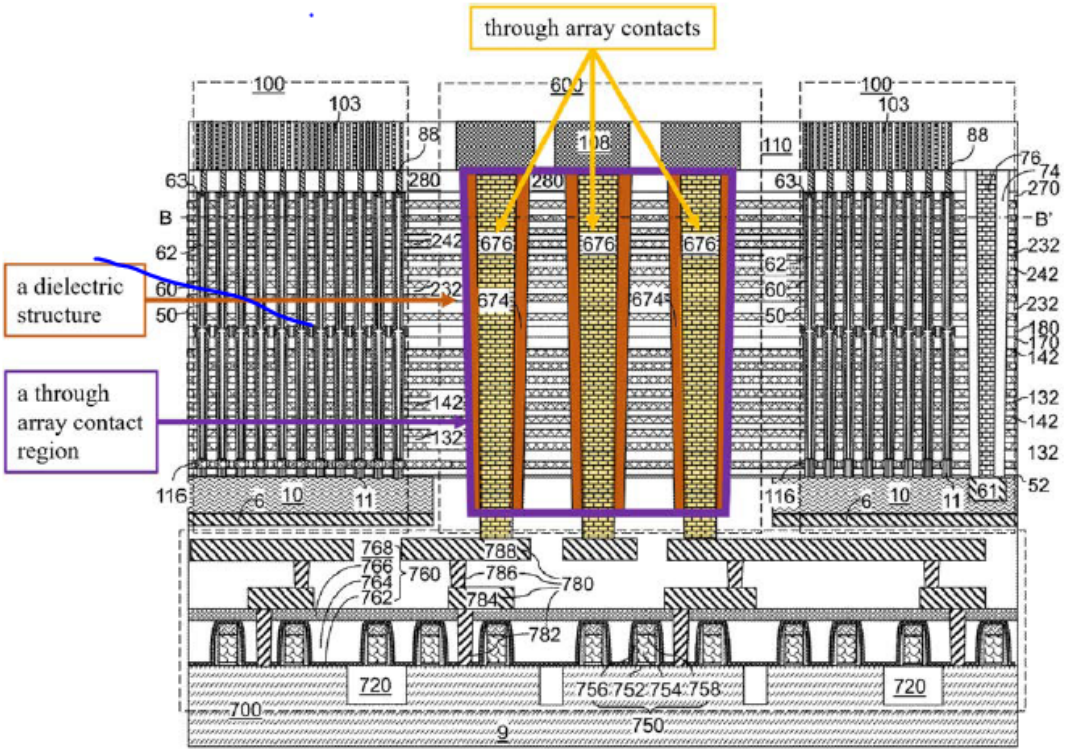


FIG. 49

Toyama's Figure 49 above, with Petitioner's annotations added, depicts though-memory-level via structures 676 (yellow), insulating liners 674 (orange), and through-memory-level via region 600. *See* Pet. 50; Ex. 1005 ¶¶ 341–342, Fig. 49). Petitioner asserts that Toyama's through array contacts (though-memory-level via structures 676 (yellow)) extend vertically through the dielectric structure (insulating liners 674 (orange)). Pet. 49–50 (citing Ex. 1005 ¶¶ 341–342, Fig. 49; Ex. 1003 ¶¶ 114–115).

[7] The "through-memory-level via region 600" in Toyama contains the "through-memory-level via structures 676," which Petitioner maps to the TAC region and TACs, respectively. *See* Pet. 44–46.

Lastly, Petitioner argues that Toyama's "dummy memory stack structures 55D" surrounding the "through-memory-level via region 600" between the "first and second parts of 'memory array region 100'" disclose a "plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions" as recited in claim element [8.H]. *Id.* at 51–54 (citing Ex. 1005 Fig. 48; Ex. 1003 ¶ 118). Petitioner also states that claim 8 does not require non-electrically functional channel structures on four sides of the TAC region, but that a POSITA would have understood (1) that Toyama's dummy memory stack structures 55D encircle Toyama's TAC region or (2) that it would have been obvious to do so. Pet. 52–54 (citing Ex. 1005 ¶¶ 182, 333, Fig. 48B; Ex. 1003 ¶¶ 120–121).

(2) Patent Owner's Response

At this stage of the proceeding, Patent Owner does not challenge many of Petitioner's contentions. Patent Owner, however, does contend that Toyama does not disclose or suggest a *plurality* of TACs extending vertically through *the dielectric structure* as required by claim element [8.G] because Petitioner improperly maps multiple insulating liners 674 to a single dielectric structure. Prelim. Resp. 28–32. Specifically, Patent Owner argues that claim 8 requires that a *plurality of through array contacts* (TACs) extend vertically through a *single dielectric structure*. *Id.* at 31.

(b) Analysis

Based on the preliminary record, it appears Patent Owner' arguments have merit. As noted above, claim element [8.G] recites "a through array contact (TAC) region formed between first and second channel regions, wherein the TAC region comprises a *plurality of through array contacts (TACs)* extending vertically through *the dielectric structure*." Ex. 1001,

24:1–5 (emphasis added). A plain reading of claim element 8.G requires *more than one* (i.e., "a plurality") TAC in the TAC region to extend vertically through a *single dielectric structure* (i.e., "*the* dielectric structure"). *Id.*

Based on the present record, it appears Petitioner has not sufficiently shown that Toyama's three insulating liners are a single dielectric structure. *See, e.g.*, Pet. 31–32. Petitioner asserts that because "these components together are something 'that is constructed,' they are a structure." Pet. 31–32 (citing Ex. 1021, 4; Ex. 1003 ¶ 94); *see also id*. at 32 (stating that all insulating liners 674 have the same function as they pass through the alternating stack). We disagree that merely because the three insulating liners are each constructed, that three constructed liners together constitute a single dielectric structure. Every component of Toyama's memory device is something that is constructed. Petitioner does not sufficiently explain how multiple constructed items can be considered to constitute a single structure just because each one of the multiple items is itself constructed.

We are also not persuaded, at this stage of the proceeding, by Petitioner's argument that, even if dielectric lines 674 are not considered to be a "structure," that the claim encompasses embodiments in which each through array contact extends vertically through a different dielectric structure. Petitioner asserts that because claim 8 uses an open-ended transitional phrase ("comprising") and an indefinite article ("a") preceding "dielectric structure," the claim encompasses a device with multiple dielectric structures. Pet. 32 n.4 (citing *KCJ Corp.*, 223 F.3d at 1356. *KCJ Corp.*, however, does not stand for the proposition that open-ended language with an indefinite article is "patent parlance" for allowing multiple separate structures to be read "collectively [as] a single structure." While the open-

ended language may permit the claimed memory device to have more than one dielectric structure, this does not change the claim language that requires multiple TACs to extend vertically through a single dielectric structure. In other words, even if the claim language's use of indefinite article "a" or "an" or the open-ended transitional phrase "comprising" permits more than one dielectric structure in the memory device, the claim still requires that a plurality of TACs must extend through a single dielectric structure.

Thus, based on the present record, we do not understand Toyama's Second Modification to disclose or suggest a plurality of TACs that extend vertically through a single dielectric structure as required by claim element [8.G].

We invite the parties to develop these arguments further at trial, to the extent permitted by our rules.

(c) Claims 9, 11, and 12

Claims 9, 11, and 12 depend, directly or indirectly, from claim 8. Ex. 1001, 24:9–11, 24:21–24. Petitioner asserts that Toyama's Second Modification teaches or suggests the limitations of these dependent claims. Pet. 54–56. None of Petitioner's arguments remedy the deficiency set forth above regarding independent claim 1.

3. Asserted Obviousness over Toyama's First Exemplary Structure (Alternative Argument 2)

Petitioner contends that claims 8, 9, 11, and 12 would have been obvious over Toyama's first exemplary structure ("First Exemplary Structure"). Pet. 56–95. Patent Owner opposes. For the reasons stated below, Petitioner has shown a reasonable likelihood that claims 8, 9, 11, or 12 would have been obvious over Toyama's First Exemplary Structure.

(a) Claim 8

(1) Petitioner's Contentions

Petitioner contends that Toyama's First Exemplary Structure[8] teaches or renders obvious all elements of independent claim 8. Pet. 56–94. For example, Petitioner asserts that Toyama discloses a three dimensional non-volatile memory device having an alternating conductor/dielectric layer stack ("alternating stack (132, 146, 232, 246)") as recited in the preamble and claim element [8.A]. *Id.* at 56–57 (citing Ex. 1005 ¶¶ 156, 172, Fig. 17A; Ex. 1003 ¶ 128).

Petitioner asserts that, as shown in Toyama's Figure 15A reproduced below, the upper part of "dielectric fill material portion 430" is a dielectric structure that extends vertically through alternating conductor/dielectric stack, (elements 132, 146, 232, 246 highlighted in green and yellow) as required by claim element [8.B]. Pet. 59–64 (citing, *inter alia*, Ex. 1005, 126, 173, 190, 213, 216, Figs. 10A, 15A, 16B; Ex. 1003 ¶¶ 130–135); *see also id.* at 63–64 (stating that Toyama's First Exemplary Structure removes layers 132, 142, 232, 242 to form opening 769, which is then filled with dielectric fill material portion 430).

[8] Toyama's First Exemplary Structure is depicted in Figures 1–17 of Toyama. *See* Ex. 1005 ¶¶ 14–49.

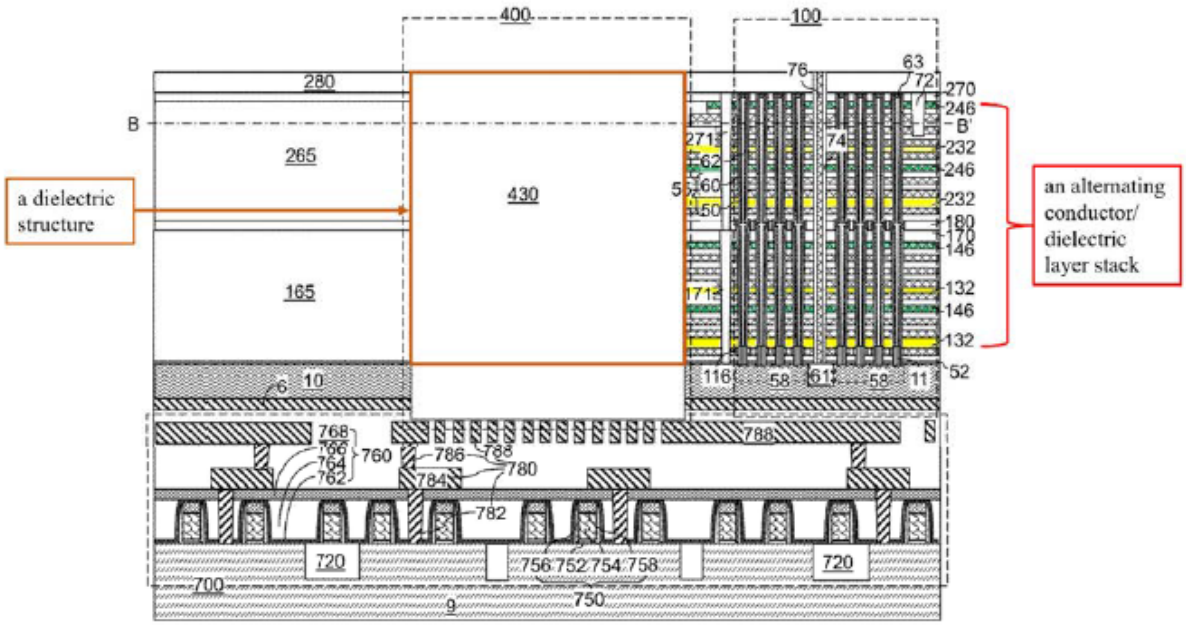


FIG. 15A

Toyama's Figure 15A above, with Petitioner's annotations added, "is a vertical cross-sectional view of the first exemplary structure after formation of electrically conductive layers, insulating spacers, and backside contact via structures." Pet. 60; Ex. 1005 ¶ 39, Fig. 15A.

Petitioner asserts that Toyama renders obvious the "first and second channel regions comprising first and second pluralities of channel structures, respectively" recited in claim element [8.C]. Pet. 64–78. Pointing to, *inter alia,* Toyama Figure 16B reproduced below, Petitioner asserts that each of Toyama's memory stack structures 55 (green) is a channel structure and that part of Toyama's memory array region 100 (red) form a channel region. *Id.* at 66.

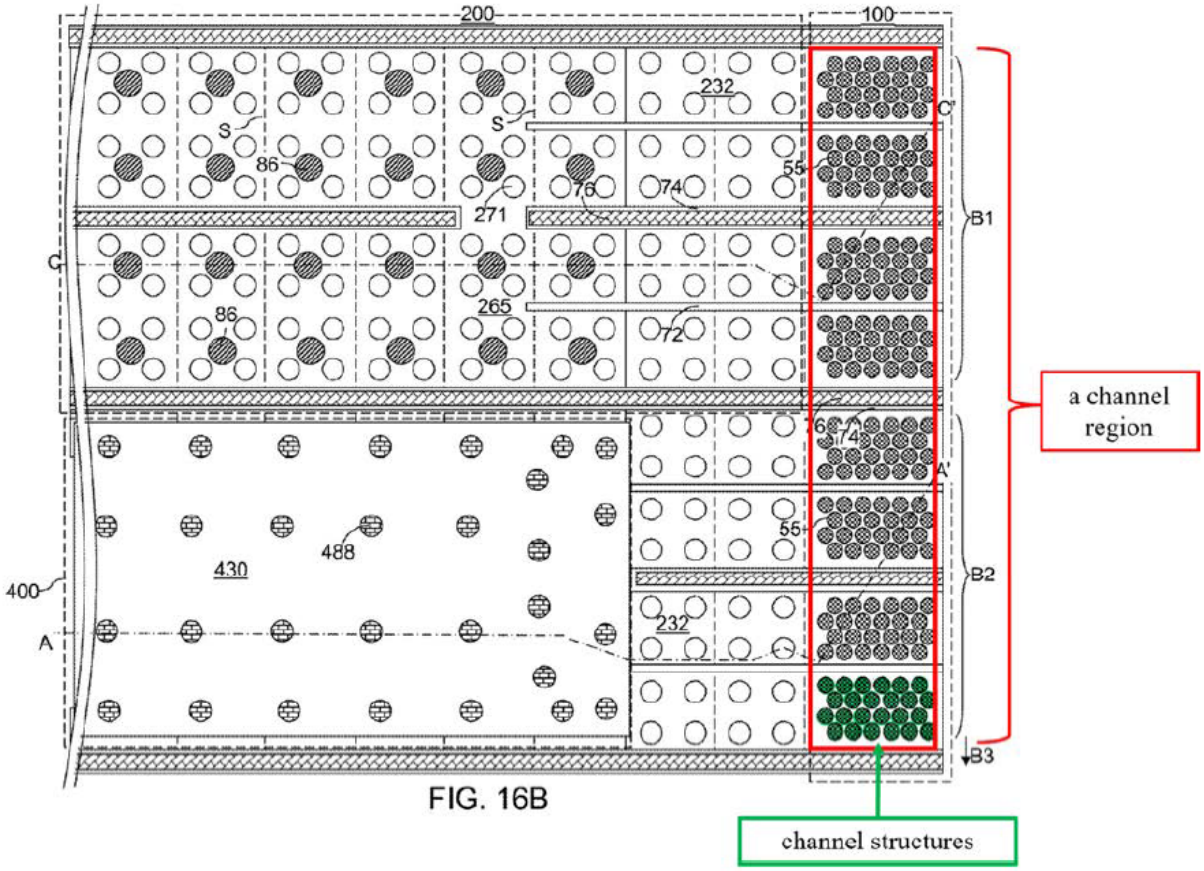
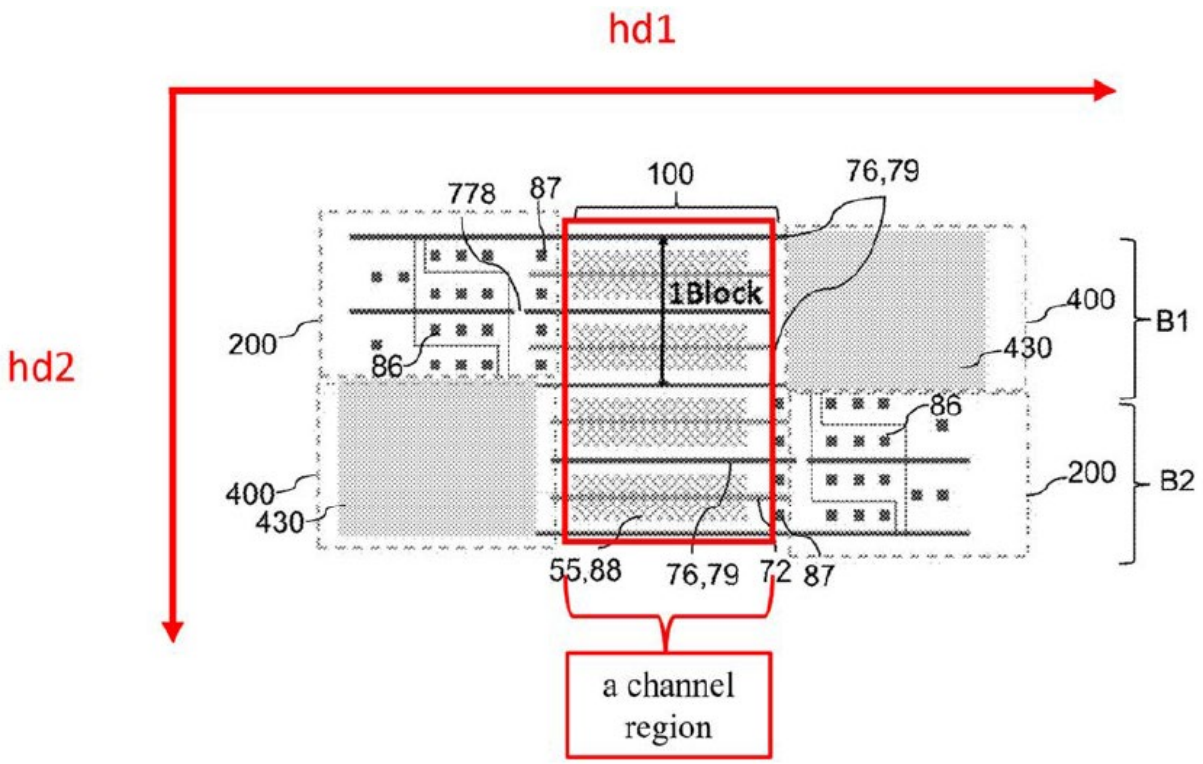


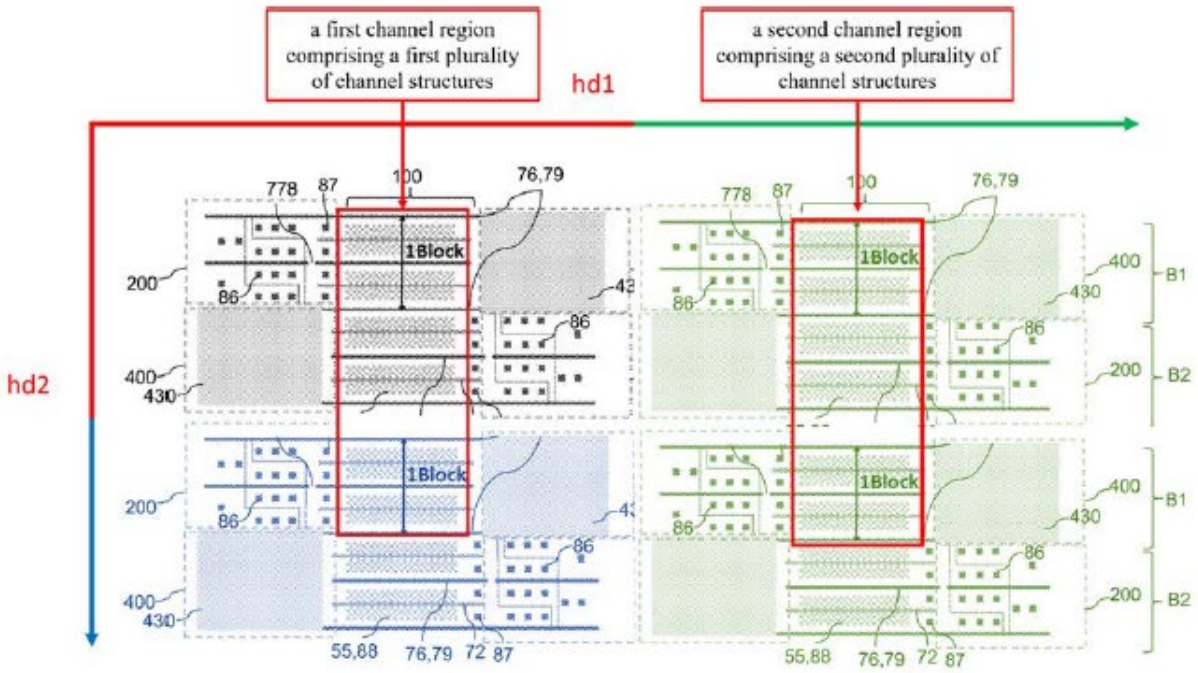
Figure 16B is a horizontal cross-sectional view of the first exemplary structure along the horizontal plane B-B' in Figure 16A. Ex. 1005 ¶ 43, Fig. 16B; Pet. 66.

Petitioner further asserts that memory array region 100 (red) in Toyama's Figure 17E is also a channel region.



Toyama's Figure 17E, with Petitioner's annotations added, is a top-down view of an alternative exemplary structure according to the first embodiment of the present invention, that Petitioner asserts may be used with Toyama's first exemplary structure. Ex. 1005 ¶ 49; Pet. 66–67.

Petitioner asserts that Toyama expressly shows that the layout in Figure 17E repeats in the hd2 (up-down) direction and that a POSITA would have found it obvious to also repeat the layout in the hd1 (left-right direction), as shown in the modified Figure 17E below. Pet. 67–68 (citing Ex. 1005 ¶ 220; Ex. 1003 ¶ 138), 78 (citing Ex. 1003 ¶ 154).



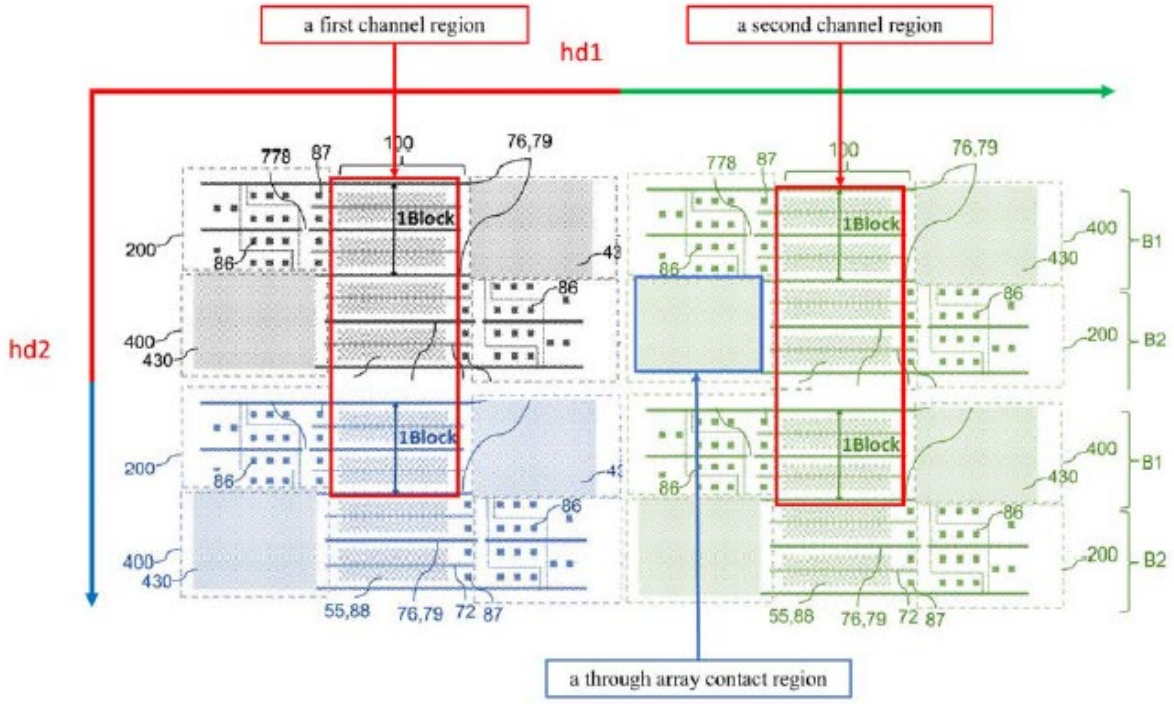
Petitioner's Modified Figure 17E depicts the layout of Figure 17E repeated in both the hd1 (left-right) and hd2 (top-down) direction. *See* Pet. 68–69.

Petitioner asserts that modified Figure 17E depicts first and second channel regions (first and second parts of memory array regions 100 (red)) comprising first and second pluralities of channel structures (first and second pluralities of memory stack structures 55) as required by claim element [8.C]. Pet. 78 (citing Ex. 1003 ¶ 155). Petitioner contends that a POSITA would have known to implement, and the numerous benefits of, such a multi-plane flash memory device. *See id.* at 69–74 (citing, *inter alia*, Ex. 1003 ¶¶ 144–146). Petitioner asserts that a multi-plane memory device renders it possible to issue a read command on multiple planes simultaneously, improves the throughput of program operations, i.e., writing data to the flash memory), and improves the performance of NAND based systems. *Id.* at 74–75 (citing Ex. 1025, 42, 44–45, 171; Ex. 1003 ¶¶ 141–147). Petitioner also asserts that a POSITA would have had a reasonable

expectation of success in implementing multiple planes of Toyama's first exemplary structure in the hd1 direction because NAND flash memory devices with multiple planes existed for many years before the priority date of the '806 patent and repeating the layout in Figure 17E for each plane would have been straightforward and predictable. *Id.* at 76–77 (citing Ex. 1003 ¶ 151); *see also id.* at 71–75 (providing examples of multi-plane flash memory devices). Dr. Lee testifies that this modification is nothing more than applying a known technique (implementing multiple planes of a NAND flash memory array) to a known device (Toyama's first exemplary structure) to yield predictable results (a NAND flash device with improved performance). *See, e.g.*, Ex. 1003 ¶ 151.

With respect to claim element [8.D], Petitioner asserts that Toyama's laterally-elongated contact via structures 76 are the "slit structures" that extend vertically through the alternating conductor/dielectric layer stack ("alternating stack 132, 146, 232, 246"). Pet. 79–80 (citing Ex. 1005, Fig. 17A, 17B; Ex. 1003 ¶¶ 154–156). Petitioner also asserts that Toyama discloses staircase regions (a "staircase structure") that is disposed in alternating stack 132, 146, 232, 246 (an "alternating conductor/dielectric stack layer") as required by claim element [8.E]. *Id.* at 80–81 (citing Ex. 1003 ¶ 157; Ex. 1005, Fig. 17C). Petitioner also contends that Toyama discloses local contacts ("drain contact via structures 88") disposed on (in contact with and extending above) the channel structures ("memory stack structures 55"), and local contacts ("source connection via structures 91") disposed on (above) the slit structures ("laterally-elongated contact via structures 76") as recited in claim element [8.F]. *Id.* at 81–82 (citing Ex. 1005 ¶ 251, Fig. 17A; Ex. 1003 ¶¶ 158–159).

Claim element [8.G] recites "a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure." Petitioner admits that Toyama does not expressly disclose a TAC region formed between the first and second channel regions, but asserts that the limitation would have been obvious to implement in the multiple planes of Toyama's first exemplary structure in the hd1 direction. Pet. 85. Petitioner asserts that, as shown in Toyama's modified Figure 17E below, the TAC region is formed between the first and second channel regions. *Id.*



Toyama's modified Figure 17E, with Petitioner's modifications and annotations added, depicts a top-down view of an alternative exemplary structure according to the first embodiment of the invention, having first and second channel regions (red) and a through array contact (TAC) region (blue). Ex. 1005 ¶ 50; Pet. 86 (citing Ex. 1003 ¶¶ 165–166).

Petitioner asserts that Toyama's through-memory level via structures 488 are through array contacts that extend vertically through part of dielectric fill material portion 430 (dielectric structure) as recited in claim element [8.G]. Pet. 86–87 (citing Ex. 1005 ¶ 239, Fig. 17A; Ex. 1003 ¶¶ 162–163).

Claim element [8.H] recites a "plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions." Petitioner asserts that Toyama's "first-tier support pillar structures 171" and "second-tier support pillar structures 271" are, or render obvious, a plurality of non-electrically functional channel structures. Pet. 86–93 (citing Ex. 1005 ¶¶ 182, 197, 203, 311, Figs. 16B, 17A, 17E; Ex. 1003 ¶ 168–173, 178; Ex. 1016 ¶ 162; Ex. 1017, 9:50–67; Ex. 1015 ¶¶ 73–81). In particular, Petitioner contends that a POSITA would have understood Toyama's first-tier support pillar structures, which "comprise dummy stack structures [that] are not electrically connected to bit lines" are non-electrically functional channel structures. Pet. 89–90 (citing Ex. 1005 ¶ 203). Petitioner also asserts that a POSITA would have understood that (1) Toyama's second-tier support pillar structures 271 are also dummy memory stack structures (Pet. 90 (citing Ex. 1003 ¶¶ 169–171)) or (2) it would have been obvious to form Toyama's support pillar structures 171, 271 as dummy stack structures because they provide structural support and can be formed in the same process steps as the functional channel structures (Pet. 90–91 (citing Ex. 1005 ¶ 311; Ex. 1016 ¶ 162; Ex. 1017, 9:50–67; Ex. 1015 ¶¶ 73–81; Ex. 1003 ¶ 172).

(2) Patent Owner's Response

At this stage of the proceeding, Patent Owner does not challenge many of Petitioner's contentions. Patent Owner, however, does argue that Toyama's First Exemplary Structure does not disclose or suggest "a through

array contact (TAC) region formed between the first and second channel regions" as required by claim element [8.G] because the TAC region only has a channel region on one side. Prelim. Resp. 32–38. Patent Owner asserts that a POSITA would not modify Toyama to repeat portions of the device in the hd1 direction and add a second channel region, as asserted by Petitioner, because doing so would omit necessary neighboring structures, such as the driver circuit that connects to the memory structure on the second side. *Id.* at 32–33; *see also id.* at 36–38 (stating Toyama's layout cannot be repeated in the hd1 direction because Toyama includes peripheral circuitry, such as "driver circuitry," beyond the alleged TAC region and citing Ex. 1005 ¶ 163); Ex. 1005 ¶ 163 (stating the "semiconductor devices can include any semiconductor circuitry to support operation of a memory structure to be subsequently formed, which is typically referred to as a driver circuitry, which is also known as peripheral circuitry).

Patent Owner asserts that Petitioner's proposed modification "ignores the peripheral circuitry, including the driver circuit, and therefore would not work." Prelim. Resp. 37; *see also id.* at 38 (stating "none of the circuitry needed to operate each memory array is included in Petitioner's analysis" and that Petitioner's modification "lacks the necessary support circuitry for a functioning memory device").

(3) Analysis

Based on the preliminary record, we determine Petitioner shows a reasonable likelihood of prevailing on its second alternative argument that claim 8 would have been obvious over Toyama's First Exemplary Embodiment.

With respect to claim element [8.G]'s requirement that the memory device comprise a TAC region formed between the first and second channel

regions, Petitioner provides sufficient argument with supporting evidence that a POSITA would have reason to modify Toyama First Exemplary Structure, which has a channel region (memory array region 100) on only one side of the TAC region (part of "through-memory-level via region 400"), to extend the device in the hd1 region and that such a modified device, having multiple planes, would have a TAC region formed between the first and second channel regions as required by claim element [8.G]. Pet. 66–78, 83–87.

Patent Owner's contention that Petitioner's arguments are based on hindsight and that a POSITA would not modify Toyama to repeat in the hd2 direction—because doing so "does not account for the necessary driver circuitry" and that Petitioner's proposed modification would not work—raises factual issues that are best resolved on a full record. Prelim. Resp. 32–38.

Petitioner provides sufficient argument and evidence at this stage of the proceeding that a POSITA would have modified Toyama to provide a multi-plane flash memory device that could issue a read command on multiple planes simultaneously, thereby improving the throughput of program operations and the performance of NAND based systems. *Id.* at 68–75 (citing, *inter alia,* Ex. 1023, 144; Ex. 1014, 308, 313–314). Petitioner also provides sufficient arguments and evidence that this solution was quite common because power issues related to this kind of solution are still manageable inside the chip and optimized versus two separate NAND devices active at the same time. *Id.* at 75 (citing Ex. 1025, 44–45, 171; Ex. 1003 ¶¶ 141–147); *see also* Ex. 1003 ¶¶ 141–147 (citing, *inter alia*, Ex. 1023, 144, 247, Fig. 6.1; Ex. 1024, 13:37–44; Ex. 1014, 308, 313–314; Ex. 1025, 42, 44–45, 171).

Petitioner also provides sufficient argument and evidence that a POSITA would have had a reasonable expectation of success in implementing multiple planes of Toyama's First Exemplary Structure in the hd1 direction because NAND devices having multiple planes existed for many years before the priority date of the '806 patent and that implementation of such a structure would have been straightforward as it merely applies a known technique (implementing multiple planes of NAND flash memory array) to a known device (Toyama's first exemplary structure) to yield predictable results (a NAND flash device with improved performance). Pet. 69–77 (citing, *inter alia*, Ex. 1003 ¶¶ 148–151); *see also* Ex. 1003 ¶¶ 148–151 (stating a POSITA would have known how to implement multiple planes in Toyama's memory device using the same approach discussed earlier in the declaration); *see also* Ex. 1003 ¶¶ 141–147 (citing, *inter alia*, Ex. 1023, 144, 247, Fig. 6.1; Ex. 1024, 13:37–44; Ex. 1014, 308, 313–314; Ex. 1025, 42, 44–45, 171).

Accordingly, at this stage of the proceeding, Petitioner sufficiently shows that a POSITA would have had reason to modify Toyama's First Exemplary Structure to repeat portions of the device in the hd1 direction in order, *inter alia*, to improve performance of the device and would have done so with a reasonable expectation of success, and that such a modification results in a TAC region formed between first and second channel regions as required by claim element [8.G], notwithstanding Patent Owner's arguments to the contrary, which raise issues best resolved on a full record.

At this stage of the proceeding, Patent Owner does not address Petitioner's specific contentions with respect to the other limitations of claim 8. We reviewed Petitioner's contentions for the remaining limitations

and determine Petitioner sufficiently shows that Toyama teaches or suggests these remaining limitations. Pet. 56–82, 87–95.

Accordingly, based on the record before us, we are persuaded that Petitioner sufficiently shows a reasonable likelihood that claim 8 would have been obvious over Toyama's First Exemplary Structure.

(b) Claims 9, 11, and 12

Petitioner also contends that Toyama's disclosures regarding the First Exemplary Structure teach or suggest all of the limitations of claims 9, 11, and 12, which depend, directly or indirectly, from claim 8. Pet. 94–95; Ex. 1001, 24:9–11, 24:21–24. At this stage of the proceeding, Patent Owner does not dispute Petitioner's contentions. We reviewed Petitioner's contentions with regard to these dependent claims and are persuaded that Petitioner sufficiently shows a reasonable likelihood that claims 9, 11, and 12 would have been obvious over Toyama's First Exemplary Structure.

4. Asserted Obviousness over Toyama's First Exemplary Structure in View of Toyama's Second Modification of its Fourth Exemplary Structure (Alternative Argument 3)

Petitioner argues that claims 8, 9, 11, and 12 would have been obvious over Toyama's First Exemplary Structure in view of Toyama's Second Modification. Pet. 96–122. Having already determined that Petitioner demonstrates a reasonable likelihood that at least one claim would have been obvious, we need not address this ground in full. We offer the following comments in response to the parties' arguments and evidence to provide guidance to the parties.

(a) Claim 8

(1) Parties' Arguments

Petitioner argues that a POSITA would have found it obvious to modify "Toyama's Second Modification that forms the 'through-memory-level structures' within a unitary dielectric fill material (as in Toyama's first exemplary structure) instead of using the Second Modification's 'insulating liners 674." Pet. 96. Petitioner relies on Toyama's statement that "'through-memory-level via structures' can be electrically isolated from the 'alternating stack' by a unitary 'dielectric fill material portion 430.'" *Id.* at 96–97 (pointing to annotated Figure 17A). Petitioner further argues that a POSITA would have been motivated to substitute the insulating liners 674 with a unitary dielectric fill material portion 430 because it would "isolate[] the 'through-memory-level via structures,'" which would be "desirable because otherwise the 'through-memory-level via structures' may electrically interfere with each other and/or with other of the Second Modification's conductive elements." *Id.* at 101. Petitioner also argues that such modification would "reduce capacitive coupling"[9] because it would increase the separation of the conductive elements. *Id.* at 101–102. Lastly, Petitioner argues that the proposed modification would have an additional benefit over Toyama's first exemplary structure, namely that "placing the 'through-memory-level via structures' [would be] closer to the elements that use the signals carried by the [via structures]," leading to benefits that

[9] Petitioner describes capacitive coupling as "an undesirable phenomenon that causes a signal in one conductive element to affect a signal in a different conductive element where the two conductive elements are separated by an insulator." Pet. 101–102 (citing Ex. 1003 ¶ 186).

include "reducing signal propagation delays and electrical losses." *Id.* at 102–104 (citing Ex. 1003 ¶ 189).

Petitioner also argues that a POSITA would have had a reasonable expectation of success of combining the teachings because "Toyama notes that the 'second modification of the fourth exemplary structure can be formed concurrently with the formation of any of the first, second, and third exemplary structures or modifications thereof, or can be formed as a stand-alone structure." *Id.* at 104–105 (quoting Ex. 1005 ¶ 332). Petitioner states that "Toyama further notes that 'where an embodiment employing a particular structure and/or configuration as illustrated in the present disclosure, it is understood that the present disclosure may be practiced with any other compatible structures and/or configurations that are functionally equivalent provided that substitutions are not explicitly forbidden or otherwise known to be impossible to a [POSITA].'" *Id.* at 105 (quoting Ex. 1005 ¶ 390). In other words, Petitioner argues that even if Toyama does not explicitly disclose Petitioner's proposed combination it, nonetheless, would have been obvious because Toyama contemplates employing functionally equivalent substitutions of its disclosed structures. Petitioner argues that a POSITA "would have [also] understood how to manufacture a device implementing the obviousness combination" and that the elements of the proposed combination "are compatible with each other" in part because these are "largely the same [structures]" with "a similar purpose." *Id.* at 105–106 (citing Ex. 1003 ¶¶ 193–95).

Patent Owner responds that Petitioner's modifications to Toyama's First Exemplary Structure in view of Toyama's Second Modification are mere "hindsight . . . because it replaces conductive material . . . with a large dielectric (an insulator), and Petitioner does not even attempt to address the

impact that these changes would have had on Toyama's memory structure." Prelim. Resp. 39–45. According to Patent Owner, "[a] POSITA would not have added a unitary dielectric fill material to Toyama's [Second Modification] because this modification removes large portions of the conductive layers in the active region that form the word lines and replaces them with an insulator." *Id.* at 41. The impact of such modification, argues Patent Owner, is that replacing the "[conductive] word lines" with "a large insulator would eliminate [the current that controls the memory]." *Id.* Such dielectric fill modification would "cause the device to fail," which is why, Patent Owner argues, Toyama "does not teach forming a unitary dielectric block in the memory array region between two channel regions." *Id.* at 43.

Patent Owner also disagrees with Petitioner's argument that reducing "capacitive coupling" is a motivation to combine the structures because "Toyama's Second Modification already 'minimizes' capacitive coupling [with the dielectric liners [674]]." *Id.* at 43–44 (citing Ex. 1005 ¶ 377). Furthermore, Patent Owner attacks Petitioner declarant's testimony because "he fails to address that capacitive coupling is also a function of the length (or area) of overlap" between conductive elements and not just a function of the "distance between conductive elements." *Id.* (citing Ex. 1003 ¶ 186).

Patent Owner further disagrees with Petitioner's alleged benefits of "placing the through-memory-level via structures (the alleged TACs) in the memory array region 100," stating that "Toyama's Second Modification . . . already has through-memory level via structures (the alleged TACs) in the memory array region." Prelim. Resp. 44. Because "Petitioner is not proposing moving the alleged TACs . . . any benefits of having the alleged TACs in [the memory array region] are irrelevant to whether a POSITA would [add a unitary dielectric fill material]." *Id.* at 44–45. Lastly, Patent

Owner argues that the proposed modification is not shown to be "compatible" by Petitioner and a showing that "a POSITA could ***manufacture*** the device" has no bearing on a "motivation to make the proposed combination." *Id.* at 45 (emphasis in Prelim. Resp.).

(2) Analysis

On this record, we find that Patent Owner's arguments may have merit. As Patent Owner points out, based on the present record, Petitioner does not appear to address the impact of replacing the region containing conductive word lines with dielectric fill material. Based on the preliminary record, it appears that replacing the conductive word lines with insulating material would eliminate the current that controls the memory, resulting in a non-functioning device. *See, e.g.*, Prelim. Resp. 41–43.

However, because Petitioner demonstrates that at least one claim of the '806 patent would have been obvious, we institute an *inter partes* review for all claims as challenged in the Petition, including these challenges.

We invite the parties to develop these arguments further at trial, to the extent permitted by our rules.

D. Discretion under 35 U.S.C. § 325(d)

Patent Owner argues that the Board should exercise its discretion to deny institution under 35 U.S.C. § 325(d) because the asserted reference, Toyama, was previously presented to the Office and the Examiner did not err in a manner material to patentability in allowing the claims over Toyama. *Id.* at 16–26.

1. Legal Framework

Under Section 325(d), the Director has the discretion to deny a petition that presents the same or substantially the same prior art or arguments as previously presented to the Office. The Board uses the

following two-part framework for evaluating arguments under Section 325(d):

> (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and
>
> (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.

Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH, IPR2019-01469, Paper 6, 8 (PTAB Feb. 13, 2020) (precedential) ("*Advanced Bionics*"). In applying this two-part framework, we consider the following non-exclusive factors:

> (a) the similarities and material differences between the asserted art and the prior art involved during examination;
>
> (b) the cumulative nature of the asserted art and the prior art evaluated during examination;
>
> (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;
>
> (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;
>
> (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and
>
> (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of prior art or arguments.

Becton, Dickinson & Co. v. B. Braun Melsungen AG, IPR2017-01586, Paper 8 at 17–18 (PTAB Dec. 15, 2017) (precedential). Factors (a), (b), and (d), relate to whether the same or substantially the same art or arguments were previously presented to the Office, and factors (c), (e), and (f) relate to whether the petitioner demonstrates that the Office erred in a manner

material to the patentability of the claims. *Advanced Bionics*, Paper 6 at 9–11. Only if the same or substantially the same art or arguments were previously presented to the Office do we then consider whether the petitioner has demonstrated a material error by the Office. *Id.*

2. Part One of the Advanced Bionics *Framework*

Patent Owner argues, and Petitioner does not dispute, that part one of the *Advanced Bionics* framework is met because Toyama was cited on an Examiner initialed Information Disclosure Statement ("IDS") and therefore was previously presented to the Office. *See* Pet. 10; Prelim. Resp. 18–19. Accordingly, we move on to part two of the framework.

3. Part Two of the Advanced Bionics *Framework*

Patent Owner contends Petitioner fails to show that the Office erred in a manner material to the patentability of the challenged claims, as required by part two of the *Advanced Bionics* framework. Prelim. Resp. 19–27. For example, Patent Owner asserts Toyama does not disclose forming TACs in a dedicated TAC region hosted by a dielectric structure between two channel regions. *Id.* at 20. Patent Owner asserts that Toyama's First Exemplary Structure lacks first and second channel regions such that a TAC region is between the first and second channel regions. *Id.* at 23. Patent Owner further asserts that Toyama intentionally does not teach repeating blocks in the hd1 direction to provide a TAC region between two channel regions, as asserted by Petitioner, because the inactive staircase regions are on the sides of Toyama's device and multiplying the inactive space is "non-sensical," repeating blocks in the hd1 direction would eliminate necessary circuitry on the side of the array, and there is no motivation to make such a change. *Id.* at 23–25.

As described above in Section II.C.3 above, Petitioner provides arguments and evidence, including declaration testimony, not before the Office to show that a POSITA would have had reason to modify Toyama to repeat blocks in the hd1 direction with a reasonable expectation of success and that such a modification would suggest the subject matter of independent claim element 8. We also note that, although Toyama was cited on an IDS, the reference was not expressly addressed by the Examiner nor used as the basis for a rejection. For at least these reasons, we find that Petitioner demonstrates that the Examiner erred in a manner material to the patentability of the challenged claims by misapprehending or overlooking whether a POSITA would have had reason to modify Toyama to repeat blocks in the hd1 direction to arrive at the subject matter of independent claim 8. Accordingly, we determine that the Petition establishes that the Office erred in a manner material to the patentability under the second part of the *Advanced Bionics* framework. As such, we decline to exercise our discretion to deny institution under § 325(d).

III. CONCLUSION

Based on the arguments and evidence presented, we determine that Petitioner establishes a reasonable likelihood that it will prevail on its challenge to at least one claim of the '806 patent. Accordingly, we institute an *inter partes* review of all the challenged claims on all arguments presented.

The factual findings set forth in this Decision, including any claim construction matters, are preliminary and provided for the sole purpose of deciding whether to institute a review. Any final findings will be based on the full trial record, including any information presented in a timely filed response to the Petition. *See Trivascular, Inc. v. Samuels*, 812 F.3d 1056,

1068 (Fed. Cir. 2016) (noting that "there is a significant difference between a petitioner's burden to establish a 'reasonable likelihood of success' at institution, and actually proving invalidity by a preponderance of the evidence at trial") (quoting 35 U.S.C. § 314(a); comparing *id.*, with § 316(e)).

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that that that an *inter partes* review is instituted with respect to all of the grounds asserted in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which shall commence on the entry date of this Decision.

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