Patent Owner's Demonstrative Slides

Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.

***Inter Partes* Review of**

U.S. Patent No. 10,658,378

September 4, 2025

IPR2024-00788 and IPR2024-00909
Patent Trial and Appeal Board
United States Patent and Trademark Office

I. Introduction

Table of Abbreviations

Abbreviation	Description
’378	U.S. Pat. No. 10,658,378
’378FH	File History of U.S. Pat. No. 10,658,378
Challenged Claims	’378, Claims 1-7, 15-20
Patent Owner or PO	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
Board	USPTO Patent Trial and Appeal Board
IPR788	IPR2024-00788 (*Inter Partes* Review of U.S. Patent No. 10,658,378), challenging Claims 15-17, 19-20
IPR909	IPR2024-00909 (*Inter Partes* Review of U.S. Patent No. 10,658,378), challenging Claims 1-7, 18
PET-788	Petition for IPR788 (IPR2024-00788, Paper 1)
PET-909	Petition for IPR909 (IPR2024-00909, Paper 1)
DI-788	Decision Granting Institution for IPR788 (IPR2024-00788, Paper 13)
DI-909	Decision Granting Institution for IPR909 (IPR2024-00909, Paper 12)
POR-788	Patent Owner’s Response for IPR788 (IPR2024-00788, Paper 17)
POR-909	Patent Owner’s Response for IPR909 (IPR2024-00909, Paper 15)
Reply-788	Petitioner’s Reply for IPR788 (IPR2024-00788, Paper 20)
Reply-909	Petitioner’s Reply for IPR909 (IPR2024-00909, Paper 17)
Sur-Reply-788	Patent Owner’s Sur-Reply for IPR788 (IPR2024-00788, Paper 23)
Sur-Reply-909	Patent Owner’s Sur-Reply for IPR909 (IPR2024-00909, Paper 23)

All citations within quotations omitted herein, and emphasis added unless otherwise indicated

Table of Abbreviations (cont'd)

Abbreviation	Description
Leel-788	Original Declaration of Dr. Jack C. Lee for IPR788 (IPR2024-00788, Ex. 1003)
Leell-788	Reply Declaration of Dr. Jack C. Lee for IPR788 (IPR2024-00788, Ex. 1037)
Leel-909	Original Declaration of Dr. Jack C. Lee for IPR909 (IPR2024-00909, Ex. 1003)
Leell-909	Reply Declaration of Dr. Jack C. Lee for IPR909 (IPR2024-00909, Ex. 1037)
Yang-788	Declaration of Dr. Woodward Yang for IPR788 (IPR2024-00788, Ex. 2005)
Yang-909	Declaration of Dr. Woodward Yang for IPR909 (IPR2024-00909, Ex. 2005)
Toyama	U.S. Patent Publication No. 2017/0179026
Mushiga	U.S. Patent No. 10,354,980
Makala	U.S. Patent No. 10,262,945
Lee-378 Tr.	Transcript of January 28, 2025 Deposition of Dr. Lee for IPR788 and IPR909 (IPR2024-00788, Ex. 2007 and IPR2024-00909, Ex. 2007)
Parallel district court litigation	*Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.*, NDCA-3-23-cv-05792 (N.D. Cal.)
POSITA	Person of ordinary skill in art

All citations within quotations omitted herein, and emphasis added unless otherwise indicated

’378, Claim 1

- Claim 1 of the ’378 recites:

[1.Pre] A three-dimensional (3D) memory device, comprising:

[1.a] a semiconductor substrate;

[1.b] an alternating layer stack disposed on the semiconductor substrate;

[1.c] a dielectric structure on an isolation region of the substrate and extending vertically through the alternating layer stack, wherein the alternating layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

[1.d] one or more through array contacts (TACs) extending vertically through the dielectric structure and the isolation region;

[1.e] one or more channel structures extending vertically through the alternating layer stack;

[1.f.] an epitaxial layer between the one or more channel structures and the semiconductor substrate;

[1.g] an etch stop plug on each of the one or more channel structures;

[1.h] a staircase structure in the alternating layer;

[1.i] slit structures extending vertically in the alternating layer stack; and

[1.j] one or more contact layers on the one or more TACs, the one or more channel structures, and the slit structures.

’378, Claim 15

- Claim 15 of the ’378 recites:

[15.Pre] A three-dimensional (3D) memory device, comprising:

[15.a] a substrate with an isolation structure;

[15.b] an alternating conductor/dielectric layer stack disposed on the substrate;

[15.c] a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

[15.d] channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;

[15.e] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

[15.f.] a word line contact disposed on the conductor layer of the each level;

[15.g] local contacts disposed on the channel structures and the slit structures; and

[15.h] through array contacts (TACs) extending vertically through the dielectric and the isolation structures.

’378, Claims 7, 17-18

- Claim 7 of the ’378 recites:

> The 3D memory device of claim 1, wherein the dielectric structure defines a through array contact region within the 3D memory device.

- Claim 17 of the ’378 recites:

> The 3D memory device of claim 15, wherein the dielectric structure comprises a through array contact region of the 3D memory device.

- Claim 18 of the ’378 recites:

> [18.pre] The 3D memory device of claim 15, further comprising:
>
> [18.a] an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures; and
>
> [18.b] an epitaxial layer disposed between the channel structures and the substrate.

Grounds

Claims	Grounds	IPR
’378, claims 1-7, 15-20	(1) Toyama Obviousness (1A) Toyama’s First Exemplary Structure (1B) Toyama’s Second Modification	IPR788 (claims 15-17, 19-20); IPR909 (claims 1-7, 18)
’378, claims 15-17, 19-20	(2) Mushiga Obviousness	IPR788 only
’378, claims 15-17, 19-20	(3) Mushiga in view of Makala Obviousness	IPR788 only

Disputed Issues

Issue	Slides
Claim Construction ▪ "a Substrate With an Isolation Structure" (limitation [15.a]) / "an Isolation Region of the Substrate" (limitation [1.c]) ▪ "a Dielectric Structure on [the/an] Isolation [Structure/Region]" (limitations [15.c]/[1.c]) ▪ Through Array Contacts Limitation (limitation [15.h]) ▪ TAC Region Limitation (Claim 17) ▪ TAC Region Limitation (Claim 7) ▪ "Each Local Contact of the Local Contacts" (Claim 18)	Slides 11-34
Toyama's First Exemplary Structure (Ground 1A) ▪ **All Claims:** Toyama's First Exemplary Structure Fails to Disclose or Render Obvious "a Substrate With an Isolation Structure" (limitation [15.a]) / "an Isolation Region of the Substrate" (limitation [1.c]) ▪ **All Claims:** Toyama's First Exemplary Structure Fails to Disclose or Render Obvious "a Dielectric Structure on [the/an] Isolation [Structure/Region]" (limitations [15.c]/[1.c]) ▪ **Claim 18:** Toyama's First Exemplary Structure Fails to Disclose or Render Obvious "an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the Channel Structures"	Slides 35-43

Disputed Issues

Issue	Slides
Toyama's Second Modification (Ground 1B) ▪ **All Claims:** Toyama's Second Modification Fails to Disclose or Render Obvious "a Substrate With an Isolation Structure" (limitation [15.a]) / "an Isolation Region of the Substrate" (limitation [1.c]) ▪ **Claims 15-20:** Toyama's Second Modification Fails to Disclose or Render Obvious "Through Array Contacts (TACs) Extending Vertically Through the Dielectric and the Isolation Structures" (limitation [15.h]) ▪ **Claim 17 and 7:** Toyama's Second Modification Fails to Disclose or Render Obvious "the Dielectric Structure [Comprises/Defines] a Through Array Contact Region [of/Within] the 3D Memory Device" ▪ **Claim 18:** Toyama's Second Modification Fails to Disclose or Render Obvious "an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the Channel Structures"	Slides 44-53
Mushiga (Ground 2) / Mushiga in View of Makala (Ground 3) ***Grounds 2-3 Are Asserted Against Claims 15-17 and 19-20 Only** ▪ **All Claims:** Mushiga Fails to Disclose or Render Obvious "a Substrate With an Isolation Structure" (limitation [15.a]) ▪ **All Claims:** Mushiga Fails to Disclose or Render Obvious "Through Array Contacts (TACs) Extending Vertically Through the Dielectric and the Isolation Structures" (limitation [15.h]) ▪ **All Claims:** Mushiga Fails to Disclose or Render Obvious "a Dielectric Structure on the Isolation Structure and Extending Vertically through the Alternating Conductor/Dielectric Stack" (limitation [1.c]) ▪ **Claim 17:** Mushiga Fails to Disclose or Render Obvious "the Dielectric Structure Comprises a Through Array Contact Region of the 3D Memory Device"	Slides 54-63

II. Claim Construction

Claims 1 and 15 Require the Isolation Region/Structure to Be Part of the Substrate

- The claimed "isolation [region/structure]" is introduced only in reference to the recited substrate:

Claim 1 of the '378 recites:

> [1.c] a dielectric structure on **an isolation region of the substrate** and extending vertically through the alternating layer stack, wherein the alternating layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

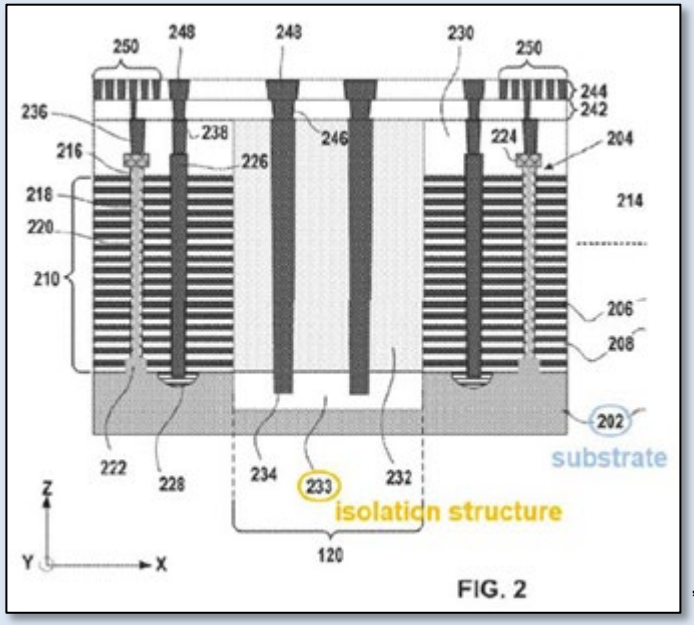
Claim 15 of the '378 recites:

> [15.a] **a substrate with an isolation structure**;

POR-788, 19; Yang-788, ¶58; Sur-Reply-788, 2-3;
POR-909, 14; Yang-909, ¶46; Sur-Reply-909, 2-3.

Claims 1 and 15 Require the Isolation Region/Structure to Be Part of the Substrate

- ***Every disclosed embodiment*** ***describes and depicts the isolation region/structure as part of the substrate***, such that the isolation region/structure ***does not extend beyond the upper or lower portion of the substrate***:



'378, Fig. 2.

- The substrate is a platform for subsequent layers:

> **'378 Patent**: "As used herein, ***the term "substrate" refers to a material onto which subsequent material layers are added, or otherwise "disposed."***

'378, 4:41-43.

'378, 12:54-66, 20:38-42, 21:7-13, 21:64, 22:27-28, Figs. 2, 4-13; POR-788, 19-21, 41-42; Yang-788, ¶¶59-60, 96; Sur-Reply-788, 3; POR-909, 14-16, 42-43; Yang-909, ¶¶48-49, 90; Sur-Reply-909, 2-3.

Claims 1 and 15 Require the Isolation Region/Structure to Be Part of the Substrate

Petitioner argues: "***[T]he specification does not meet the 'exacting' standard required to 'depart from the pain meaning' of 'with' and 'of.'***"

Reply-909, 4; *see also* Reply-788, 4.

- But Petitioner's own evidence shows that Patent Owner's construction does not depart from the plain meaning:

With: "***inclusive of***"

With: "in possession of; ***HAVING***"

Of*:* "used as a function word ***to indicate the whole that includes the part***"

IPR788, Ex. 1038, 7; IPR909, Ex. 1038, 6, 8.

- Petitioner's Reply never defines "of" or "with" or explains its interpretation of the purported plain meaning

Sur-Reply-788, 4; Sur-Reply-909, 4.

Claims 1 and 15 Require the Isolation Region/Structure to Be Part of the Substrate

Petitioner argues: "***The patent repeatedly describes the substrate as distinct from—not part of—the isolation structure.***"

Reply-788, 3-5; Reply-909, 3-5.

- But every embodiment depicts the isolation structure as within and not extending beyond the upper portion of the substrate (slide 13)
- The specification describes that the substrate "includes" an isolation structure:

'378 Patent: "According to some embodiments, ***substrate 202 includes isolation regions or structures***, like STI structure 233 shown in FIG. 4."

'378, 12:54-66.

- The specification never describes or shows the isolation region/structure as merely next to or abutting the substrate
- The specification never describes or shows the isolation region/structure as extending beyond the top or bottom surface of the substrate

Sur-Reply-788, 4-6; POR-788, 19-21; Yang-788, 59-60;
Sur-Reply-909, 4-6; POR-909, 14-16; Yang-909, 48-49.

Claims 1 and 15 Require the Isolation Region/Structure to Be Part of the Substrate

Petitioner argues: "Indeed, it makes a little sense to argue the isolation structure must be part of the substrate, because ***the isolation structure is typically a dielectric material and thus not "part of" the substrate***, which might be made of a semiconductor material."

Reply-788, 4; *see also* Reply-909, 4.

- But Patent Owner's construction does not require the structures to be the same material, and instead limits the spatial relationship between the two structures

Sur-Reply-788, 6; Sur-Reply-909, 6.

Petitioner argues: "As Dr. Lee explained and PO does not dispute, ***the purpose of the isolation structure is to "electrically isolate[] conductors from each other and from electrical interference from the substrate***." Lee ¶ 102. ***Nothing about that purpose requires the isolation structure to be "part of" the substrate***."

Reply-788, 5; *see also* Reply-909, 4.

- But Patent Owner's construction is limited by the claim language "with" and "of" and not merely the structure's isolation function
- It would be improper to reduce the component to only its isolation function

Sur-Reply-788, 6-7; Sur-Reply-909, 7.

Claims 1 and 15 Require a Dielectric Structure That Is on the Isolation Region/Structure

Claim 1 of the ’378 recites:

> [1.c] **a dielectric structure on an isolation region** of the substrate and extending vertically through the alternating layer stack, wherein the alternating layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

Claim 15 of the ’378 recites:

> [15.c] **a dielectric structure on the isolation structure** and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

POR-788, 13-19, 46-51; Yang-788, ¶¶46-56, 103-110; Sur-Reply-788, 7-10; POR-909, 47-53; Yang-909, ¶¶97-106; Sur-Reply-909, 15-18.

Claims 1 and 15 Require a Dielectric Structure That Is on the Isolation Region/Structure

- The parties ***agree*** that "on" means "above" in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction:

Petitioner: "Petitioner does not dispute this construction of 'on'"

Reply-788, 5-6.

'378 Patent: "As used herein, whether one component (e.g., a layer or a device) is ***"on,"*** "above," or "below" ***another component*** (e.g., a layer or a device) ***of a semiconductor device*** (e.g., 3D memory device 200) ***is determined relative to substrate 202 in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction***."

'378, 7:37-43.

POR-788, 13-19; Sur-Reply-788, 7.

The Claimed Dielectric Structure and Isolation Structure/Region Are Separate Structures

Petitioner argues: "***[T]he "dielectric structure" and the "isolation structure" may be formed simultaneously from a unitary material***, or each structure may be composed of multiple components."

Reply-788, 6.

- But the "dielectric structure" and "isolation [region/structure]" are separate and distinct in the '378 claims:

Claim 1: **a dielectric structure** on **an isolation region**

Claim 15: **a dielectric structure** on **an isolation structure**

Federal Circuit: "***The claim lists the "electrical operating unit" separately from the "pair of spaced-apart electrically exposed conductive probe networks,***" and does not suggest that the "pair of ... probe networks" consists in part of a portion of the "electrical operating unit." Rather, ***the clear implication of the claim language is that the pair of probe networks is a distinct component, separate from the electrical operating unit*** of the claimed invention."

Gaus v. Conair Corp., 363 F.3d 1284, 1288 (Fed. Cir. 2004).

- There is no support in the '378 patent for Petitioner's interpretation

POR-788, 46-51; Yang-788, ¶¶103-110; Sur-Reply-788, 7-8;
POR-909, 47-53; Yang-909, ¶¶97-106; Sur-Reply-909, 15-16.

The Claimed Dielectric Structure and Isolation Structure/Region Are Separate Structures

Petitioner argues: "***[T]he "dielectric structure" and the "isolation structure" may be formed simultaneously from a unitary material***, or each structure may be composed of multiple components."

Reply-788, 6.

- But the "dielectric structure" and "isolation structure" are separate and distinct structures in the '378 specification and figures:

'378 Patent: "In some embodiments, ***dielectric structure 232 is formed so that it is aligned to or covers at least a portion of an underlying isolation structure or region 233*** (thereafter "shallow trench isolation (STI) structure 233). Please note that, STI structure 233 is exemplary and is not limiting. As such, other isolation structures can be used. Further, ***dielectric structure 232 is in contact with STI structure 233***."

'378, 10:30-43.

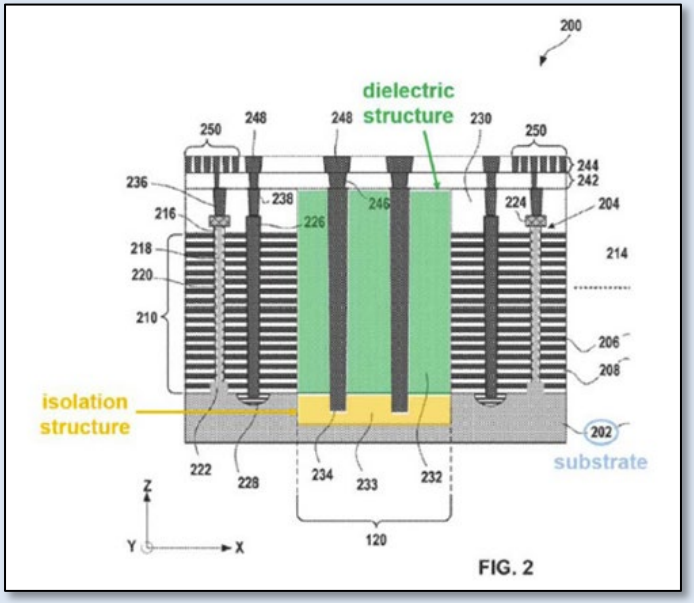


FIG. 2

'378, Fig. 2.

POR-788, 46-49; Yang-788, ¶¶103-105; Sur-Reply-788, 7-8; POR-909, 47-50; Yang-909, ¶¶97-99; Sur-Reply-909, 15-16.

Claim 15 Requires Through Array Contacts (TACs) Extending Through the Dielectric Structure and the Isolation Structure

- Claim 15 of the ’378 recites:

> [15.h] **through array contacts (TACs) extending vertically through the dielectric and the isolation structures**

- The antecedent terms are “a dielectric structure” and “an isolation structure”:

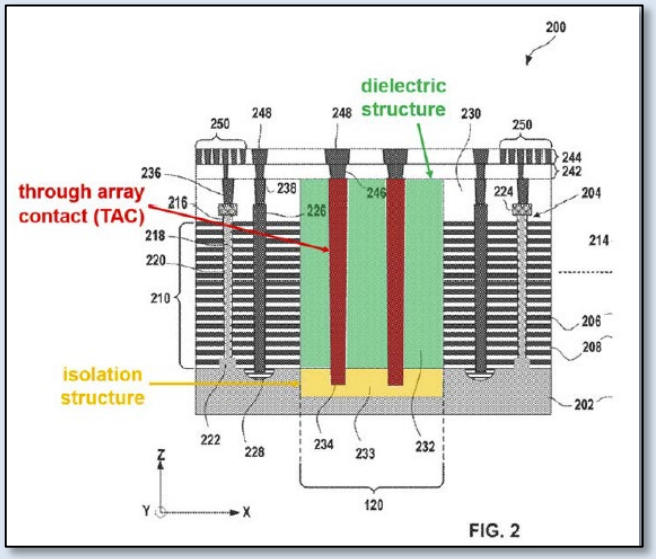
> [15.a] a substrate with **an isolation structure**;

> [15.c] **a dielectric structure** on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

POR-788, 23-27; Yang-788, ¶¶66-72; Sur-Reply-788, 10-13;
POR-909, 23-27; Yang-909, ¶¶61-67; Sur-Reply-909, 7-10.

Claim 15 Requires Through Array Contacts (TACs) Extending Through the Dielectric Structure and the Isolation Structure

- The disclosed embodiments with multiple TACs depict ***the TACs extending through the same dielectric structure***:
- The embodiment with a single TAC is irrelevant, because it does not include the claimed plurality of TACs



’378, Fig. 2.

- The ’378 patent explains the dielectric structure avoids the complex etching process of etching vias through the alternating stack:

> **’378 patent:** “***[E]tching through dielectric structure 232 can be advantageous (e.g., involve fewer etch operations) compared to etching through a stack of alternating layers having the same overall thickness***. For example, ***the formation of TACs 234 in an alternating layer stack*** with a thickness of about 6 μm or more (e.g., for a 64 tier 3D memory device) ***requires multiple etch and fill operations—therefore, increases the fabrication cost***.”

’378, 10:59-66; Yang-788, ¶32; Yang-909, ¶30.

POR-788, 6-7, 23-27; Yang-788, ¶¶32, 66-72; Sur-Reply-788, 11; POR-909, 5-6, 23-27; Yang-909, ¶¶30, 61-67; Sur-Reply-909, 7-8.

Claim 15 Requires Through Array Contacts (TACs) Extending Through the Dielectric Structure and the Isolation Structure

- Federal Circuit precedent requires at least one instance of the element (here, the claimed "a dielectric structure") that meets ***all*** of the requirements applicable to that element:

> **Federal Circuit:** "Even if an infringing system can use "one or more computers," ***the plain language of the claims requires at least one of those computers to perform all the functions listed in the claims of the ARB Patent***."

Finjan LLC v. SonicWall, Inc., 84 F.4th 963, 974-975 (Fed. Cir. 2023)

> **Federal Circuit:** "Here, it does not suffice to have multiple microprocessors, each able to perform just one of the recited functions; ***the claim language requires at least one microprocessor capable of performing each of the recited functions***."

Salazar v. AT&T Mobility LLC, 64 F.4th 1311, 1317 (Fed. Cir. 2023)

POR-788, 26-27; Yang-788, ¶72; Sur-Reply-788, 11-13;
POR-909, 26-27; Yang-909, ¶67; Sur-Reply-909, 8-10.

Claim 17 Requires That the TAC Region Is Within Or Defined by the Dielectric Structure

- Claim 17 of the ’378 recites:

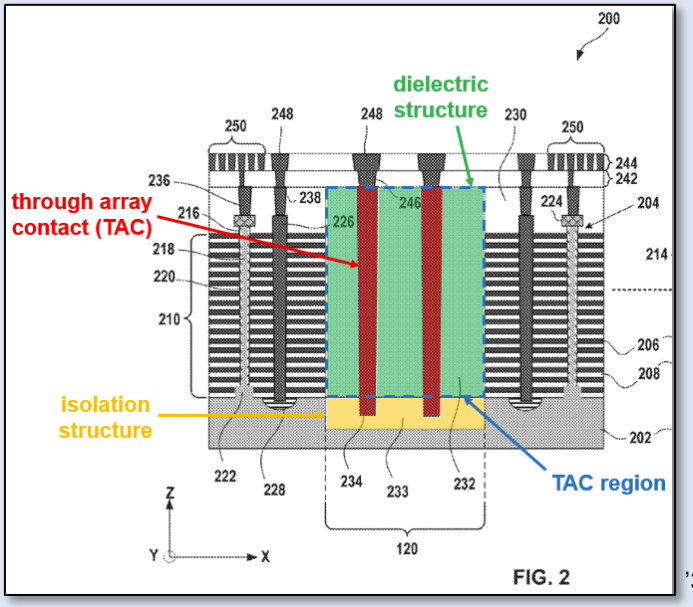
> The 3D memory device of claim 15, wherein ***the dielectric structure comprises a through array contact region of the 3D memory device***.

- This claim language (“***comprising***”) indicates that the TAC region is nested within or defined by the dielectric structure
- Patent Owner’s construction gives meaning to the term “TAC region”

POR-788, 27-29; Yang-788, ¶¶73-77; Sur-Reply-788, 13-17.

Claim 17 Requires That the TAC Region Is Within Or Defined by the Dielectric Structure

- All disclosed embodiments with a TAC region have a TAC region that is within or defined by the dielectric structure:



'378, Figure 2; *see also* Figs. 1A-1C.

'378 Patent: "In some embodiments, TAC region 120 is between two TSG staircase regions 130 in the WL direction of the 3D memory device. ***TAC region 120 can be defined by a single-material dielectric structure 124. Multiple TAC structures 126 can be formed within TAC region 120 in dielectric structure 124***."

'378, 6:11-16.

'378 Patent: "In some embodiments, ***dielectric structure 232 defines the boundaries, the shape, and the size of TAC region 120 (e.g., shown in FIGS. 1A-1C)***."

'378, 10:21-24; *see also* '378, 5:60-7:4.

POR-788, 28-29; Yang-788, ¶76; Sur-Reply-788, 14.

Claim 17 Requires That the TAC Region Is Within Or Defined by the Dielectric Structure

- In addition, because
  - 1) the dielectric structure extends through the alternating conductor/dielectric layer stack (independent claim 15), and
  - 2) the TAC region is within or defined by the dielectric structure (claim 17)

the TAC region cannot include the alternating conductor/dielectric layer stack

Limitation [15.c]: ***a dielectric structure*** on the isolation structure and ***extending vertically through the alternating conductor/dielectric layer stack***, wherein the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

Claim 17: The 3D memory device of claim 15, wherein ***the dielectric structure comprises a through array contact region of the 3D memory device***.

POR-788, 27-29; Yang-788, ¶¶73-77; Sur-Reply-788, 13-14.

Petitioner's Interpretation Puts No Limits on the Boundaries of the TAC Region

Term	Patent Owner's Construction	Petitioner's Construction
"the dielectric structure comprises a through array contact region of the 3D memory device" '378, Cl. 17	"a region that is within or defined by the dielectric structure and which includes the through array contacts extending through the dielectric structure" POR-788, 27; Sur-Reply-788, 13-14.	"a region that includes at least one [TAC]" Reply-788, 12.

Petitioner argues: "***Petitioner submits that through array contact region should be given its plain and ordinary meaning, that is, a region that includes at least one through array contact***."

Reply-788, 12.

- But Petitioner's construction puts no limits on the boundaries of the TAC region, and could include the entire device
- Petitioner's construction also renders claim 17 superfluous, because independent claim 15 already separately recites TACs extending through a dielectric structure

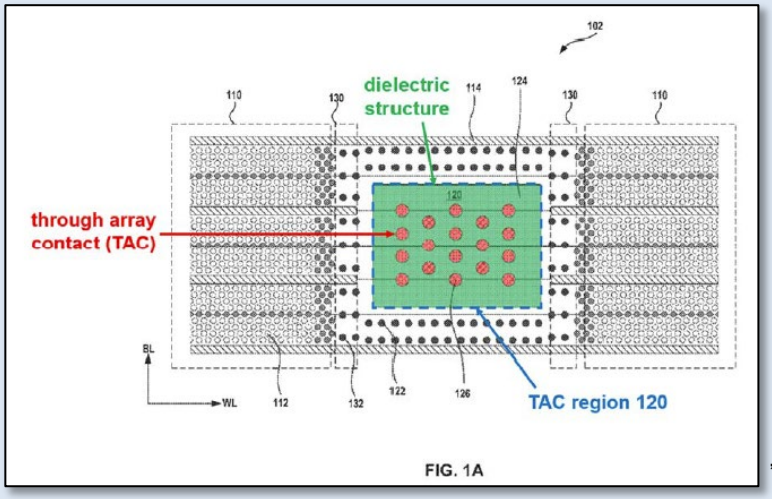
Limitation [15.h]: ***through array contacts (TACs) extending vertically through the dielectric and the isolation structures.***

POR-788, 28; Yang-788, ¶75; Sur-Reply-788, 14-15.

Petitioner's Reliance on Figure 1A is Misplaced

Petitioner argues: "The specification explains that "TAC region 102 includes NAND string regions 110, a TAC region 120, and top selective gate (TSG) staircase regions 130," each of which includes multiple elements. '378, 5:63-67. … Thus, ***a "TAC region" includes elements other than a "dielectric structure" (124) and TACs (126). Indeed, a TAC region (102) can include another TAC region (120).***" Reply-788, 12-13.

- But the claims are not directed to TAC region 102; they are directed to "TAC region 120":



'378, Fig. 1A.

Dr. Yang: "I think what they mean -- and a person of skill in the art would understand what they mean – is they're trying to show an exemplary sort of region that incorporates a TAC. And in reading and understanding the whole specification of '378, ***a person of skill in the art would understand that a TAC region, which is specifically a claim ele- -- a claimed element within the claims, is actually 120, and that should be inside of 120, which is the dielectric structure***, which they actually also call the TAC region." Ex. 1040, 71:4-72:1.

- The larger region 102 illustrates the placement of the claimed TAC region 120 in the context of other components—e.g., "WL TAC region 102" indicates that the location is the word line region (compare "BL TAC region 104" and "staircase TAC region 106")

'378, 6:23-25, 6:41-43, 6:62.

Sur-Reply-788, 16-17.

Claim 7 Requires That the TAC Region Is Defined by the Dielectric Structure

- Claim 7 of the ’378 recites:

> The 3D memory device of claim 1, wherein ***the dielectric structure defines a through array contact region*** within the 3D memory device.

- In addition, because
  - 1) the dielectric structure extends through the alternating layer stack (independent claim 1), and
  - 2) the TAC region is defined by the dielectric structure (claim 7)

  the TAC region cannot include the alternating layer stack

> **Limitation [1.c]**: ***a dielectric structure*** on an isolation region of the substrate and ***extending vertically through the alternating layer stack***, wherein the alternating layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material;

POR-909, 69-71; Yang-909, ¶¶135-137; Sur-Reply-909, 23-25.

Petitioner's Interpretation Is Contrary to the Express Claim Language and All Disclosed Embodiments

Petitioner argues: "***PO's assertion that the TAC region "cannot include the alternating conductor/dielectric layer stack" is … meritless.***"

Reply-909, 28-30.

- Petitioner's interpretation is contrary to the express claim language
- Petitioner's interpretation is incorrect for similar reasons as discussed for claim 17 (slides 27-28)

POR-909, 69-71; Yang-909, ¶¶135-137; Sur-Reply-909, 23-25.

Claim 18 Refers to the Local Contacts Disposed on the Channel Structures and the Slit Structures

- Claim 18 of the ’378 recites:

> an etch stop plug interposed between ***each local contact of the local contacts*** and each channel structure of the channel structures; and.

- The antecedent terms is “local contacts disposed on the channel structures and the slit structures”:

> **Limitation [15.g]:** “***local contacts disposed on the channel structures and the slit structures***”

POR-909, 27-34; Yang-909, ¶¶68-77; Sur-Reply-909, 10-12.

Petitioner Reads the Word “Each” Out of the Claim

Term	Patent Owner’s Construction	Petitioner’s Construction
“each local contact of the local contacts” ’378, Cl. 18	Plain and ordinary meaning: refers to the same antecedent “local contacts disposed on the channel structures and the slit structures” recited in independent claim 15 POR-909, 27; Sur-Reply-909, 10.	Refers to local contacts on the channel structures Reply-909, 10.

Petitioner argues: “The parties’ dispute with respect to this limitation is whether ***the term “each local contact” refers to local contacts on the channel structures*** (Petitioner’s position, Lee-Reply 27-36) or refers to local contacts on the channel structures and on the slit structures (PO’s position). ***PO’s construction, which reads out every embodiment of the specification, cannot be correct***.”

Reply-909, 10.

- But Petitioner’s construction contradicts the plain meaning based on the antecedent basis
- Petitioner’s construction ignores Federal Circuit precent:

Federal Circuit: “In the phrase immediately following the functional language, the claim recites, "said ID being generated as a function of the number, location, and length of ***each*** field in said first image." '961 patent, col. 8, ll. 23-25 (emphasis added). ***This language shows that the claimed algorithm evaluates attributes of each (and every) field in the information to be displayed, i.e., the first image.***”

ResONet.com, Inc. v. Lansa, Inc., 346 F.3d 1374, 1379 (Fed. Cir. 2003)

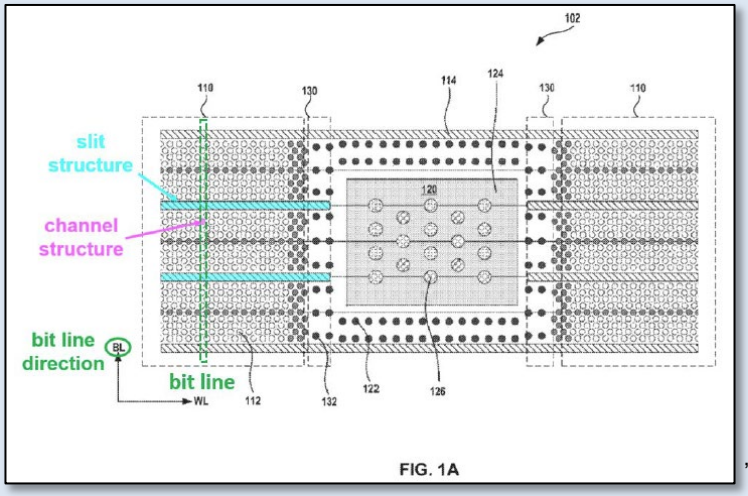
POR-909, 27-28; Yang-909, ¶69; Sur-Reply-909, 10-11.

Petitioner Mischaracterizes the Specification and Its Embodiments

Petitioner argues: "***PO's construction, which reads out every embodiment of the specification, cannot be correct***."

Reply-909, 10-11.

- But the specification discloses bit lines that are local contacts disposed on both the channel structures and the slit structures:



'378, Fig. 1A.

'378 Patent: "In some embodiments, interconnect contacts 248 in interconnect layer 244 can include ***bit lines 250, which are electrically connected to NAND strings 204***, respectively, by corresponding contacts 246 and NAND string contacts 236."

'378, 12:4-9.

'378 Patent: "According to some embodiments, FIGS. 1A-1C are plan-views of various exemplary regions of a 3D memory device along ***a bit line (BL) and a word line (WL) direction as denoted by respective axes labeled BL and WL***. For example, FIG. 1A is a plan-view of an exemplary TAC region 102 of the 3D memory device."

'378, 10:21-2; *see also* '378, 5:60-7:4.

POR-909, 29-33; Yang-909, ¶¶72-76; Sur-Reply-909, 11-12.

Petitioner Mischaracterizes the Specification and Its Embodiments

Petitioner argues: "*As an initial matter, "bit lines 250" are not "local" contacts. … [A]s Figure 2 shows, "bit lines 250" are not in physical contact with "slit structures 226":*"

Reply-909, 11-13.

- But the specification explains that local contacts include contacts "in direct contact with the memory array structures" and that bit lines are connected to memory array structures—contacts 246:

'378 Patent: "The contacts are referred to herein as "***local contacts***" because they ***are in direct contact with the memory array structures***…."

'378, 11:20-30.

'378 Patent: "In some embodiments, interconnect contacts 248 in interconnect layer 244 can include ***bit lines 250, which are electrically connected to NAND strings 204, respectively, by corresponding contacts 246*** and NAND string contacts 236."

'378, 12:4-9.

Petitioner argues: "*The patent describes "local contacts" as distinct from "interconnect contacts.'*"

Reply-909, 12-13.

- But the specification defines "contact" broadly to include any suitable types of interconnects:

'378 Patent: "As used herein, ***the term "contact" can broadly include any suitable types of interconnects*** *including vertical interconnect access (via) lines and lateral lines (interconnect lines)*."

'378, 11:20-30.

POR-909, 30-33; Yang-909, ¶¶73-75; Sur-Reply-909, 11-12.

III. Toyama's First Exemplary Structure

Toyama's First Exemplary Structure Fails to Disclose or Render Obvious "an Isolation Region of the Substrate" / "a Substrate With an Isolation Structure"

- These limitations require the isolation region/structure to be part of the substrate (*see* Slides 12-16)
- ***There is no dispute that the alleged isolation region/structure in the Petition's mapping is not "part of" the substrate—it extends all the way through and beyond the surface of the substrate***

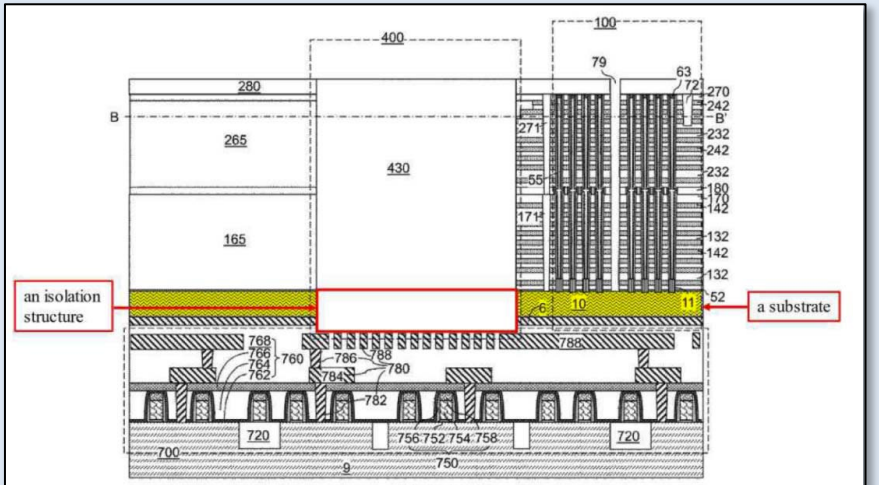


FIG. 13A

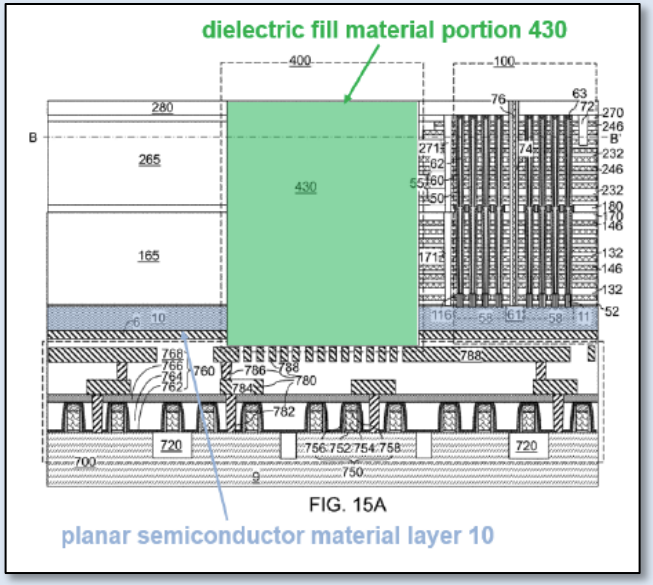


FIG. 15A

Toyama, Figs. 13A, 15A.

POR-788, 38-45; Yang-788, ¶¶91-100; Sur-Reply-788, 18-20; POR-909, 39-46; Yang-909, ¶¶85-94; Sur-Reply-909, 13-15.

Toyama's First Exemplary Structure Fails to Disclose or Render Obvious "an Isolation Region of the Substrate" / "a Substrate With an Isolation Structure"

Petitioner argues: "***[I]n Toyama's first exemplary structure, "planar semiconductor material layer 10" and the lower part of "dielectric fill material portion 430" are collectively a substrate.***"

Reply-909, 14-17; Reply-788, 15-18.

- But this is an improper new claim mapping
- Petitioner's *Apple v. Omni* case does not apply because it only permits new arguments when a claim construction is first raised in the POR, and here the construction was raised earlier in the POPR

Federal Circuit: "In *Axonics*, this Court held that "***where a patent owner in an IPR first proposes a claim construction in a patent owner response, a petitioner must be given the opportunity in its reply to argue and present evidence of anticipation or obviousness under the new construction***, at least where it relies on the same embodiments for each invalidity ground as were relied on in the petition.""

Apple Inc. v. Omni MedSci, Inc., No. 2023-1034, 2024 WL 3084509, at *5 (Fed. Cir. June 21, 2024) (quoting *Axonics, Inc. v. Medtronic, Inc.*, 75 F.4th 1374, 1384 (Fed. Cir. 2023));
POPR-788, 39 ("the 'isolation structure' is … not part of the substrate as required by the Challenged Claims.");
POPR-909, 4 ("the claims require that the 'isolation region' or 'isolation structure' is part of the substrate"), 26, 29.

- The Federal Circuit was concerned with sandbagging by withholding a construction from a preliminary response and raising it for the first time after institution, which is not the situation here

Federal Circuit: "Barring argument and evidence in a reply directed to a new claim construction proposed by the patent owner would create opportunities for sandbagging by the patent owner in order to create an estoppel. … ***[I]f instead of raising the issue in a preliminary response, a patent owner sits on its strongest claim construction arguments before institution and then raises them in response after institution, a patent owner could obtain a favorable final IPR decision and an estoppel without the Board's reaching the merits of any invalidity arguments under the newly adopted claim construction***."

Axonics, Inc. v. Medtronic, Inc., 75 F.4th 1374, 1384 (Fed. Cir. 2023)

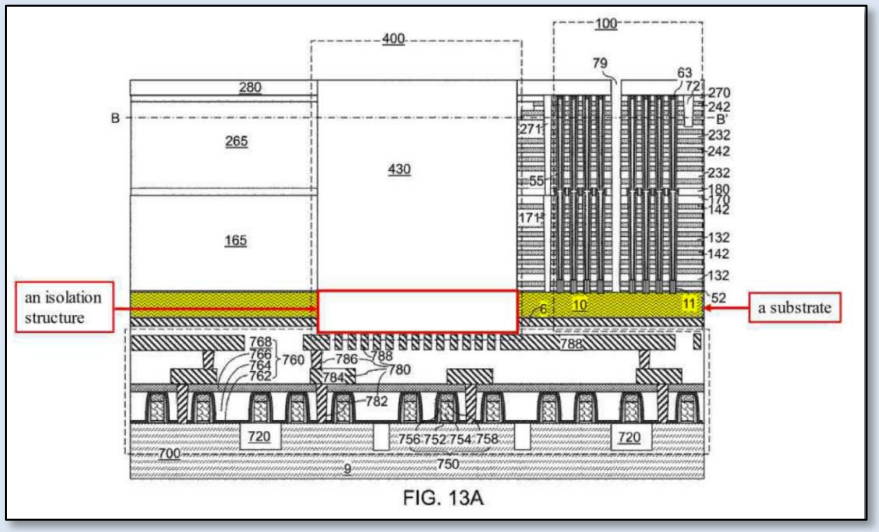
Sur-Reply-788, 18-19; Sur-Reply-909, 13-14.

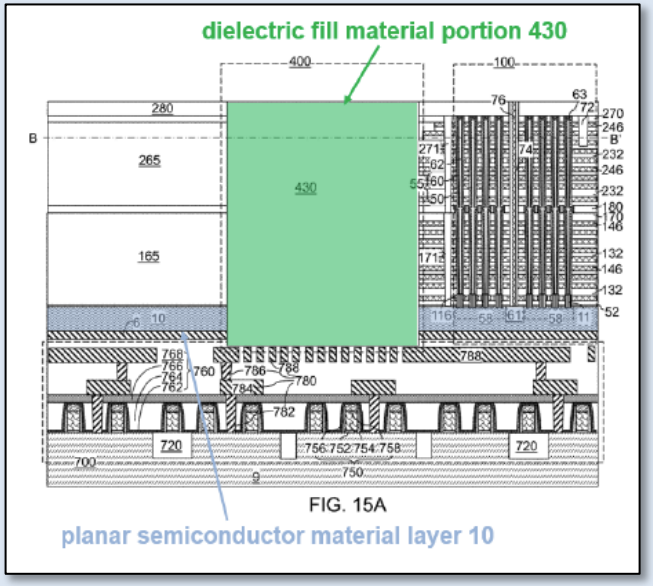
Toyama's First Exemplary Structure Fails to Disclose or Render Obvious "an Isolation Region of the Substrate" / "a Substrate With an Isolation Structure"

Petitioner argues: "*[I]n Toyama's first exemplary structure, "planar semiconductor material layer 10" and the lower part of "dielectric fill material portion 430" are collectively a substrate.*"

Reply-909, 14-17; Reply-788, 15-18.

- Regardless of whether this is an improper new mapping, Petitioner's argument fails because it does not alter the fundamental deficiency with Toyama—***the alleged isolation structure extends all the way through and beyond the surface of the substrate***



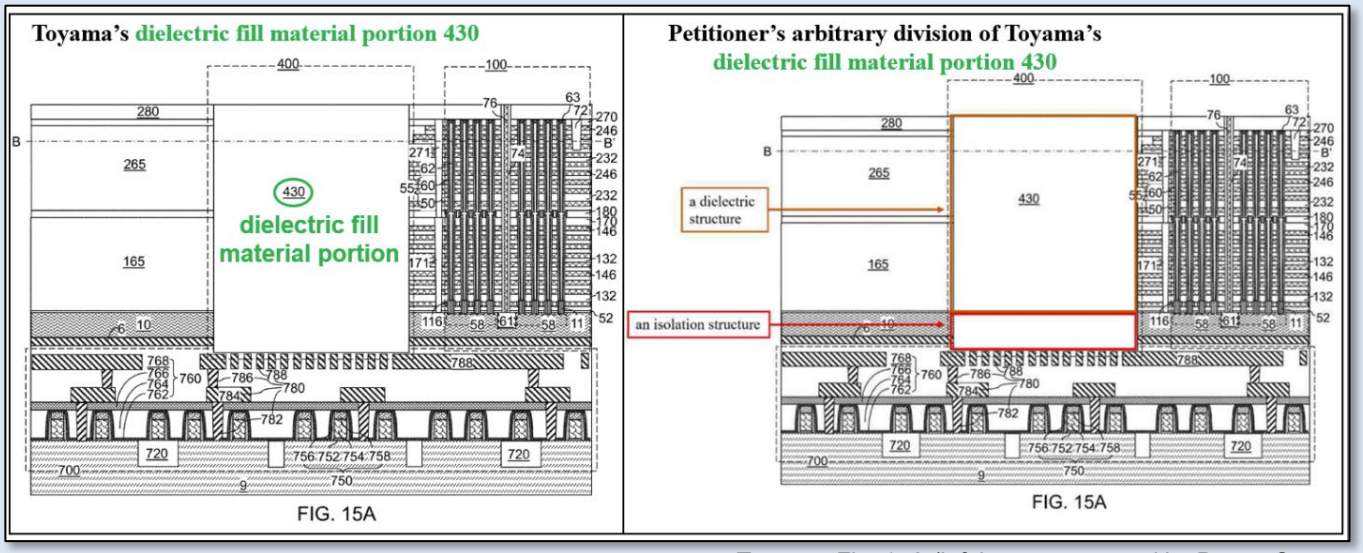


Toyama, Figs. 13A, 15A.

Sur-Reply-788, 19-20; Sur-Reply-909, 14-15.

Toyama's First Exemplary Structure Fails to Disclose or Render Obvious "a Dielectric Structure on [an/the] Isolation [Region/Structure]"

- The claims require ***both*** a "dielectric structure" and an "isolation [region/structure]"
- The claims recite two separate structures and do not encompass a single unitary structure (*see* Slides 17-20)
- ***There is no dispute that Petitioner's mapping fails under Patent Owner's Construction—Petitioner arbitrarily and improperly divides Toyama's single dielectric structure into two regions:***



Toyama, Fig. 15A (left image annotated by Patent Owner; right image annotated by Petitioner at Pet. 45, with top heading added by Patent Owner).

POR-788, 45-51; Yang-788, ¶¶101-112; Sur-Reply-788, 20-21; POR-909, 46-54; Yang-909, ¶¶95-108; Sur-Reply-909, 15-19.

Toyama's First Exemplary Structure Fails to Disclose or Render Obvious "a Dielectric Structure on [an/the] Isolation [Region/Structure]"

Petitioner argues: "***Even under PO's (incorrect) construction requiring the dielectric structure to be formed separately from the isolation structure, Toyama nevertheless renders the limitation obvious.***"

Reply-788, 19-20; Reply-909, 19-20.

- But Petitioner fails to show a motivation to modify Toyama:
  - ***Electrical isolation*** would not have motivated the modification because isolation ***is provided regardless of whether "dielectric fill material portion 430" is formed in two steps***
  - Whether two structures was "well-known" does not address the motivation issue
  - Petitioner does not address manufacturing complications

Dr. Yang: "[H]e does not address this change within the context of the overall device and the impact that these changes would have on the manufacturing process. For example, he does not address at what stage in the manufacturing process the alleged dielectric structure would be deposited. In addition, ***he does not address how the process of etching an opening for the dielectric structure would be controlled to stop at the location of the alleged isolation structure, which is an added complication that would have dissuaded a person or ordinary skill in the art from making the proposed modification***."

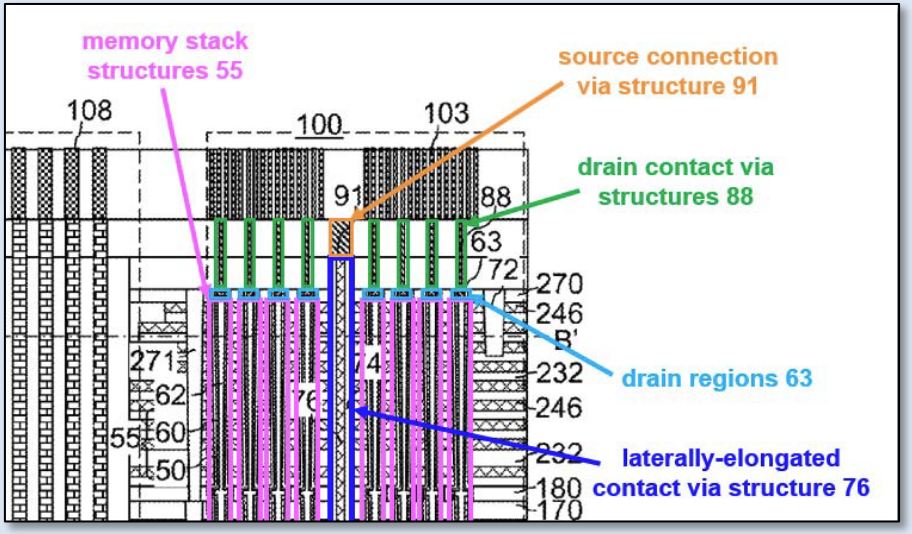
Yang-788, ¶111; Yang-909, ¶107.

- Petitioner's "mere substitution argument" fails to address these same issues

POR-788, 51; Yang-788, ¶111; Sur-Reply-788, 20-21;
POR-909, 53-54; Yang-909, ¶107; Sur-Reply-909, 18-19.

Toyama's First Exemplary Structure Fails to Disclose or Render Obvious "an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the Channel Structures" (Claim 18)

- "each local contact of the local contacts" refers to the "local contacts disposed on the channel structures and the slit structures" (*see* Slides 31-34)
- ***There is no disagreement that the Petition's mapping does not satisfy claim 18 under Patent Owner's construction***
  - The drain regions 63 (alleged etch stop plug) is not interposed between source connection via structures 91 (one of the alleged local contacts) and memory stack structures 55 (the alleged channel structures)



Toyama, Fig. 17.

POR-909, 55-60; Yang-909, ¶¶112-119; Sur-Reply-909, 27.

Toyama's First Exemplary Structure Fails to Disclose or Render Obvious "an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the Channel Structures" (Claim 18)

Petitioner argues: "***[E]ach of Toyama's embodiments discloses local contacts ("bit lines 103") disposed on*** the channel structures ("memory stack structures 55") and ***the slit structures ("laterally elongated contact via structures 76")….***"

Reply-909, 31-34.

- Petitioner's new mapping on reply is deficient
- Toyama's cross-section shows that there is **no bit line** above the **slit structure**
- To the extent Petitioner is relying on obviousness, it provides no motivation to run bit lines over slit structures

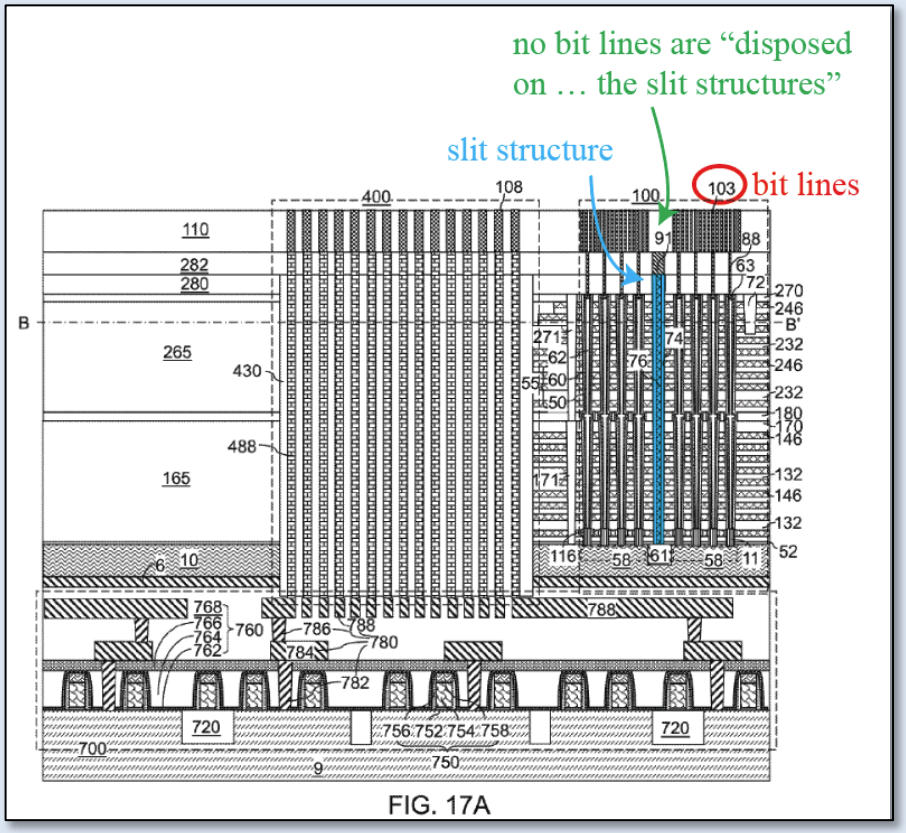


FIG. 17A

Toyama, Fig. 17A.

Sur-Reply-909, 27-30.

Toyama's First Exemplary Structure Fails to Disclose or Render Obvious "an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the Channel Structures" (Claim 18)

- The '378 patent's cross-section, on the other hand, discloses the **bit line** above the **slit structure**

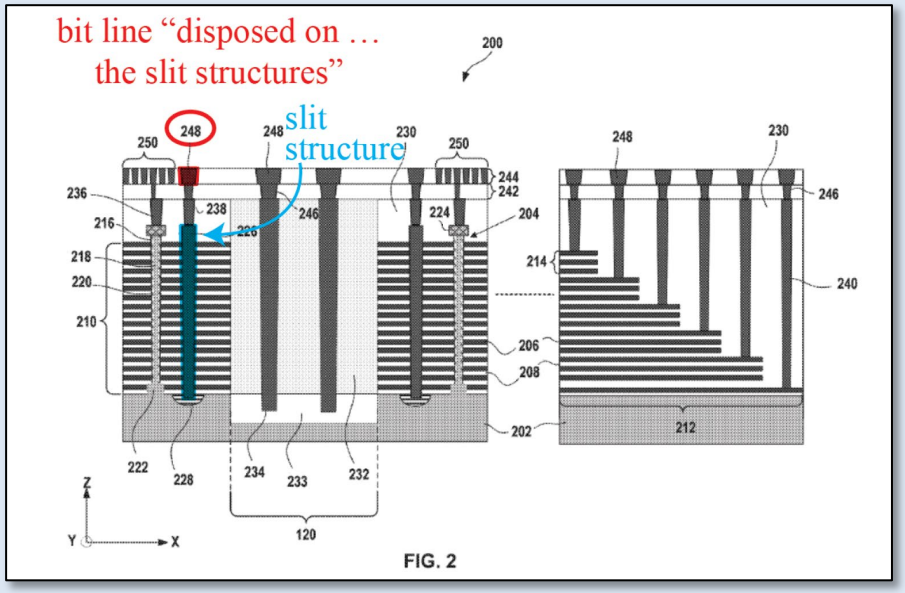


FIG. 2

'378, Fig. 2.

'378 patent: "In some embodiments, ***interconnect contacts 248*** in interconnect layer 244 ***can include bit lines 250***…."

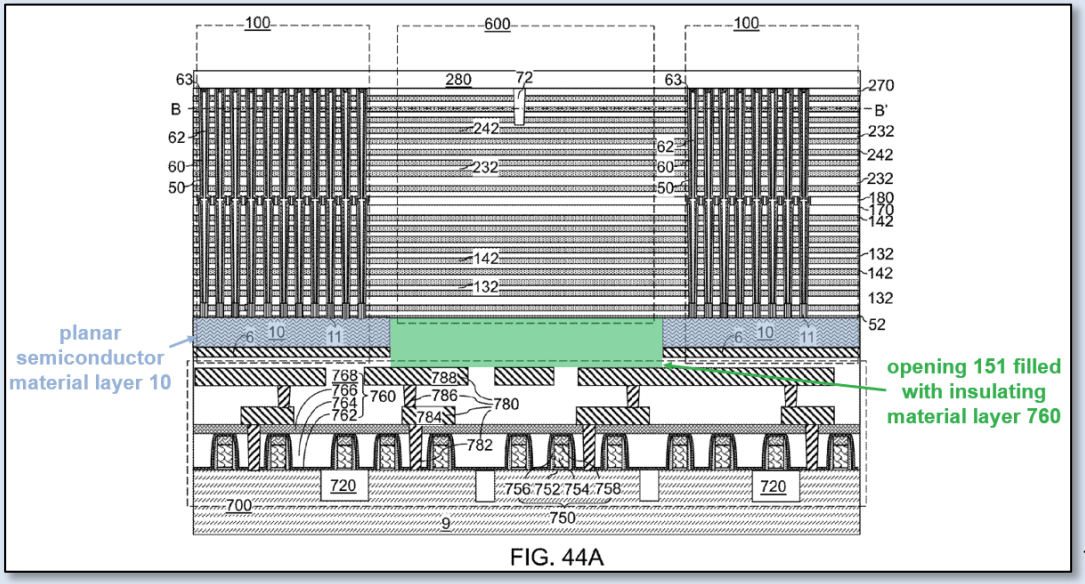
'378, 12:4-5, Fig. 2.

POR-909, 30-34; Yang-909, ¶¶73-77; Sur-Reply-909, 30.

IV. Toyama's Second Modification

Toyama's Second Modification Fails to Disclose or Render Obvious "an Isolation Region of the Substrate" / "a Substrate With an Isolation Structure"

- These limitations require the isolation region/structure to be part of the substrate (*see* Slides 12-16)
- ***There is no dispute that the alleged isolation region/structure in the Petition's mapping is not "part of" the substrate—it extends all the way through and beyond the surface of the substrate***



Toyama, Fig. 44A.

POR-788, 53-56; Yang-788, ¶¶117-121; Sur-Reply-788, 18-20;
POR-909, 62-64; Yang-909, ¶¶121-125; Sur-Reply-909, 13-15.

Toyama's Second Modification Fails to Disclose or Render Obvious "an Isolation Region of the Substrate" / "a Substrate With an Isolation Structure"

Petitioner argues: "***[I]n Toyama's Second Modification, the "planar semiconductor material layer 10" and the insulating material layer that fills "opening 151" (on the top) are collectively a substrate.***"

Reply-909, 14-17; Reply-788, 15-18.

- But this is an improper new claim mapping
- Petitioner's *Apple v. Omni* case does not apply because it only permits new arguments when a claim construction is first raised in the POR, and here the construction was raised earlier in the POPR

Federal Circuit: "In *Axonics*, this Court held that "***where a patent owner in an IPR first proposes a claim construction in a patent owner response, a petitioner must be given the opportunity in its reply to argue and present evidence of anticipation or obviousness under the new construction***, at least where it relies on the same embodiments for each invalidity ground as were relied on in the petition.""

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POPR-788, 39 ("the 'isolation structure' is … not part of the substrate as required by the Challenged Claims.");
POPR-909, 4 ("the claims require that the 'isolation region' or 'isolation structure' is part of the substrate"), 26, 29.

- The Federal Circuit was concerned with sandbagging by withholding a construction from a preliminary response and raising it for the first time after institution, which is not the situation here

Federal Circuit: "Barring argument and evidence in a reply directed to a new claim construction proposed by the patent owner would create opportunities for sandbagging by the patent owner in order to create an estoppel. … ***[I]f instead of raising the issue in a preliminary response, a patent owner sits on its strongest claim construction arguments before institution and then raises them in response after institution, a patent owner could obtain a favorable final IPR decision and an estoppel without the Board's reaching the merits of any invalidity arguments under the newly adopted claim construction***."

Axonics, Inc. v. Medtronic, Inc., 75 F.4th 1374, 1384 (Fed. Cir. 2023)

Sur-Reply-788, 18-19; Sur-Reply-909, 13-14.

Toyama's Second Modification Fails to Disclose or Render Obvious "an Isolation Region of the Substrate" / "a Substrate With an Isolation Structure"

Petitioner argues: "*[I]n Toyama's Second Modification, the "planar semiconductor material layer 10" and the insulating material layer that fills "opening 151" (on the top) are collectively a substrate.*"

Reply-909, 14-17; Reply-788, 15-18.

- Regardless of whether this an improper new mapping, Petitioner's argument fails because it does not alter the fundamental deficiency with Toyama—***the alleged isolation structure extends all the way through and beyond the surface of the substrate***

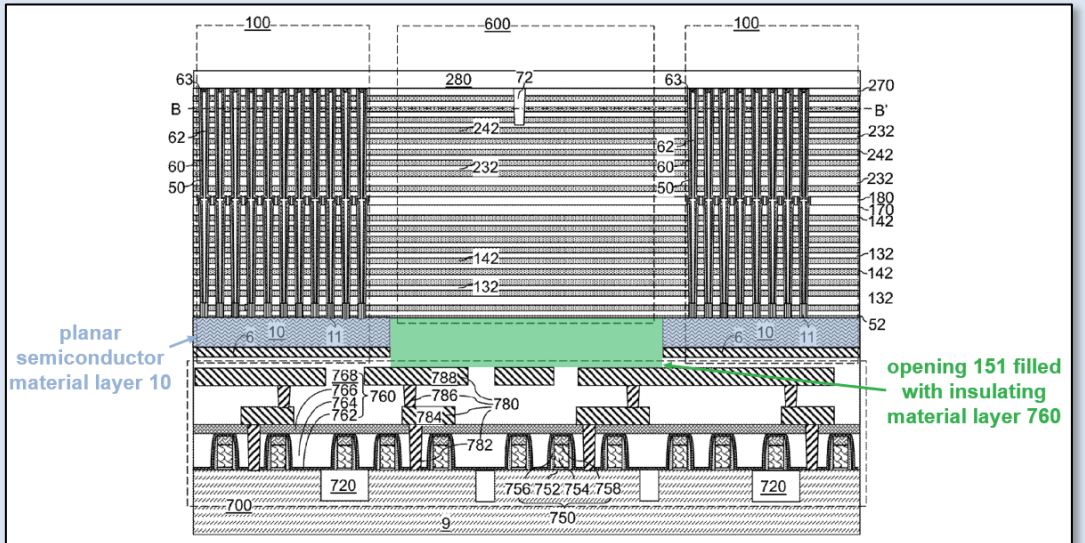


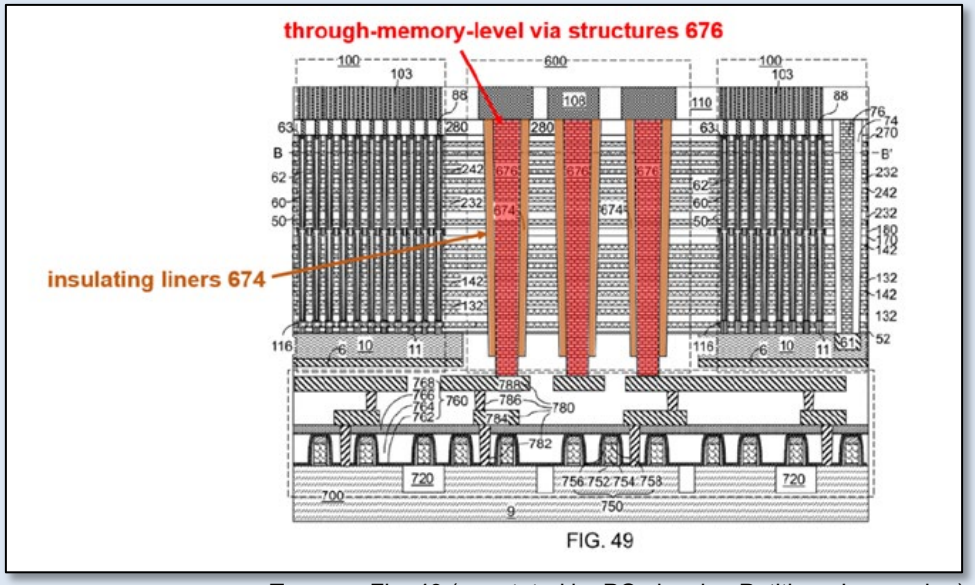
FIG. 44A

Toyama, Fig. 44A.

Sur-Reply-788, 19-20; Sur-Reply-909, 14-15.

Toyama's Second Modification Does Not Disclose or Render Obvious "through array contacts (TACs) extending vertically through the dielectric and the isolation structures" (Limitation [15.h])

- Toyama does not teach TACs extending through the ***same*** dielectric structure as required (slides 21-23)
- Only a single **through-memory-level via structure** extends through any one **insulating liner**



Toyama, Fig. 49 (annotated by PO showing Petitioner's mapping)

POR-788, 57-60; Yang-788, ¶¶123-130; Sur-Reply-788, 21-22;
POR-909, 65-69; Yang-909, ¶¶127-133; Sur-Reply-909, 19-22.

Toyama's Second Modification Does Not Disclose or Render Obvious "through array contacts (TACs) extending vertically through the dielectric and the isolation structures" (Limitation [15.h])

Petitioner argues: "***[T]he combination*** of Toyama's ***'insulating liners 674" are collectively a single dielectric structure.***'"

Reply-788, 22-25; Reply-909, 22-25.

- **But this argument still relies on multiple discrete elements, and therefore is flawed under *Finjan***
- Insulating liners are complete, functional, and separate structures—they do not work together to form a dielectric structure
- The claimed dielectric structure simplifies etching process by avoiding etching multiple vias through the alternating metal/insulator stack (see Slide 22)
- Lacking intrinsic evidence, Petitioner relies on irrelevant extrinsic examples of posts and steps, which are not individually complete and functional structures:

Ex. 1045 Ex. 1046

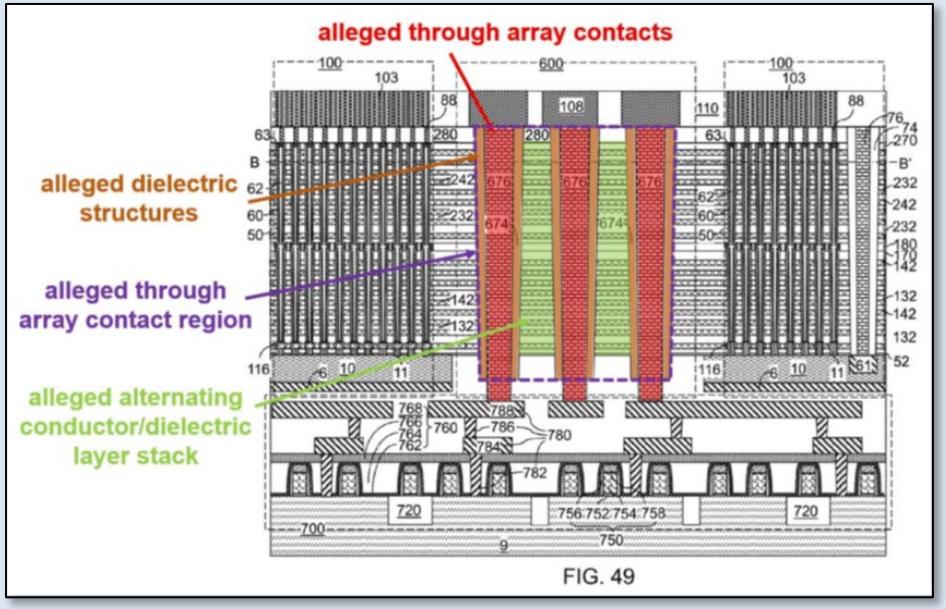
Reply-788, 22-24;
Reply-909, 23-24.

POR-788, 6-7, 57-60; Yang-788, ¶¶32, 123-130; Sur-Reply-788, 21-22;
POR-909, 5-6, 65-69; Yang-909, ¶¶30, 127-133; Sur-Reply-909, 19-22.

Toyama's Second Modification Fails to Disclose or Render Obvious "the Dielectric Structure [Comprises/Defines] a Through Array Contact Region [of/Within] the 3D Memory Device" (Claims 17, 7)

- Claim 17 requires that ***the TAC region is within or defined by the dielectric structure***, and the TAC region ***does not include the alternating conductor/dielectric layer stack*** (see Slides 24-28)
- Similarly, claim 7 requires that ***the TAC region is defined by the dielectric structure***, and the TAC region ***does not include the alternating layer stack*** (see Slides 29-30)

- Petitioner's mapping fails for two independent reasons:
  - First, ***the alleged TAC region is not defined by or within the alleged dielectric structure***; it extends beyond to encompass three separate insulating liners
  - Second, ***the alleged TAC region includes portions of the alternating conductor/dielectric layer stack***



Toyama, Fig. 49.

POR-788, 61-63; Yang-788, ¶¶131-135; Sur-Reply-788, 23-24; POR-909, 69-71; Yang-909, ¶¶134-138; Sur-Reply-909, 22-26.

Toyama's Second Modification Fails to Disclose or Render Obvious "an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the Channel Structures" (Claim 18)

- "each local contact of the local contacts" refers to the "local contacts disposed on the channel structures and the slit structures" (see Slides 31-34)
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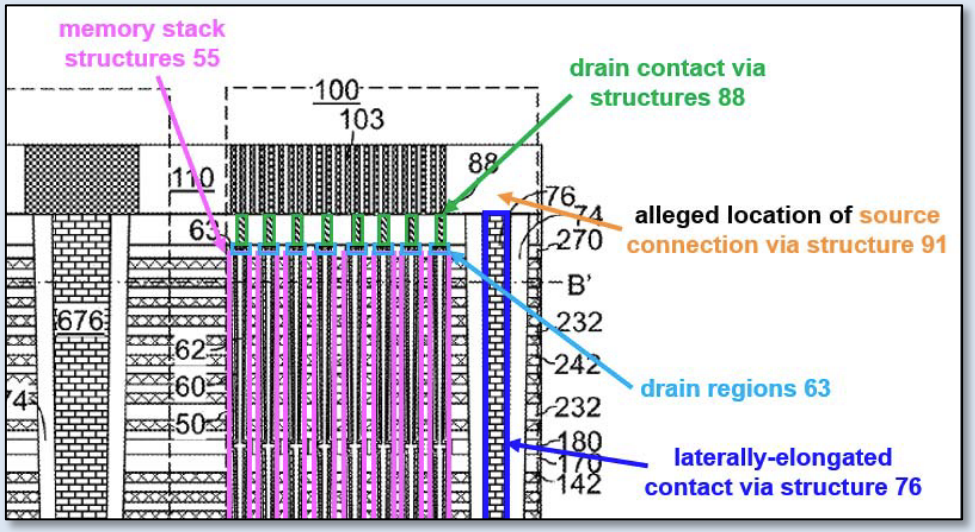

Toyama, Fig. 49.

POR-909, 71-76; Yang-909, ¶¶139-145; Sur-Reply-909, 27.

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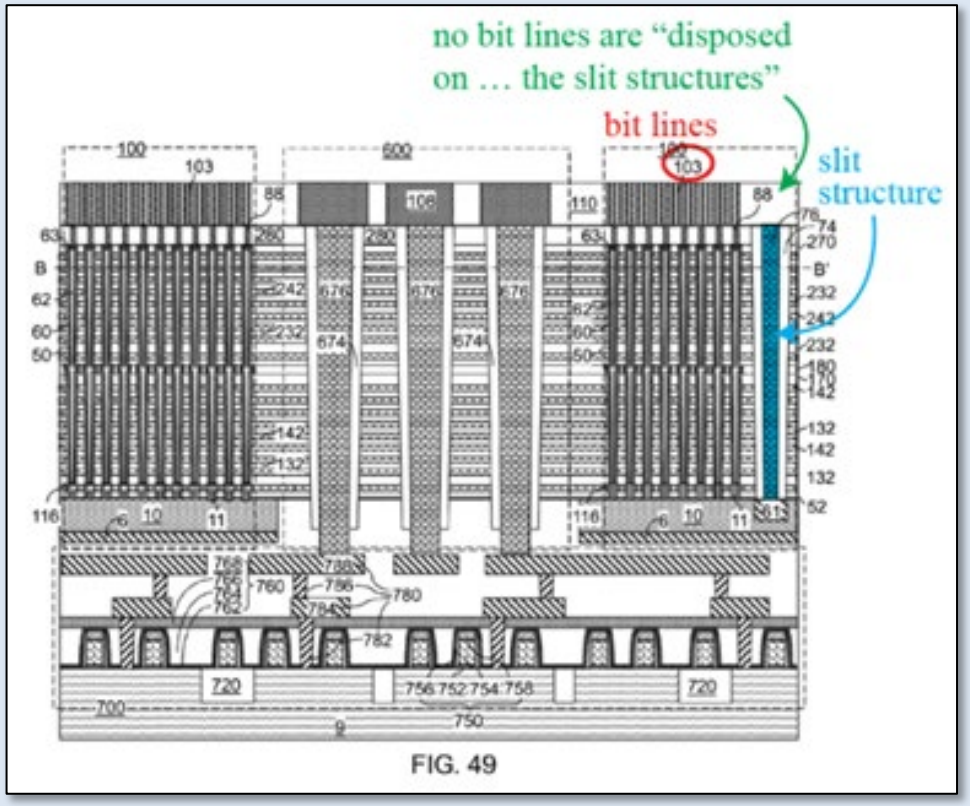
Reply-909, 31-34.

- Petitioner's new mapping on reply is deficient
- Toyama's cross-section shows that there is **no bit line** above the **slit structure**
- To the extent Petitioner is relying on obviousness, it provides no motivation to run bit lines over slit structures



Toyama, Fig. 49.

Sur-Reply-909, 27-30.

Toyama's Second Modification Fails to Disclose or Render Obvious "an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the Channel Structures" (Claim 18)

- The '378 patent's cross-section, on the other hand, discloses the **bit line** above the **slit structure**

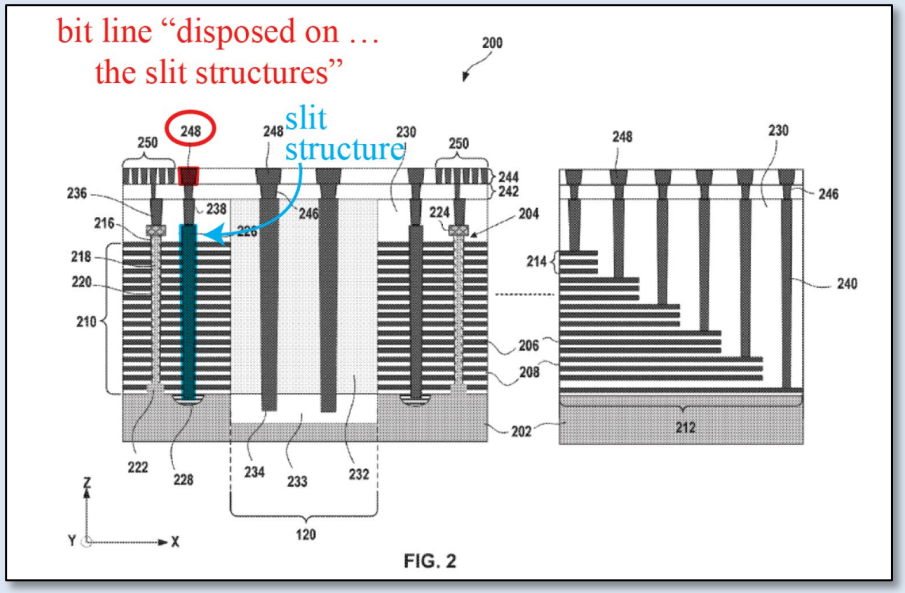


FIG. 2

'378, Fig. 2.

'378 patent: "In some embodiments, ***interconnect contacts 248*** in interconnect layer 244 ***can include bit lines 250***…."

'378, 12:4-5, Fig. 2.

POR-909, 30-34; Yang-909, ¶¶73-77; Sur-Reply-909, 30.

V. Mushiga / Mushiga in View of Makala

Mushiga Fails to Disclose or Render Obvious "a Substrate With an Isolation Structure"

- This limitation requires the isolation structure to be part of the substrate (Slides 12-16)
- ***There is no dispute that the alleged isolation structure in the Petition's mapping is not "part of" the substrate—it extends all the way through and beyond the surface of the substrate***

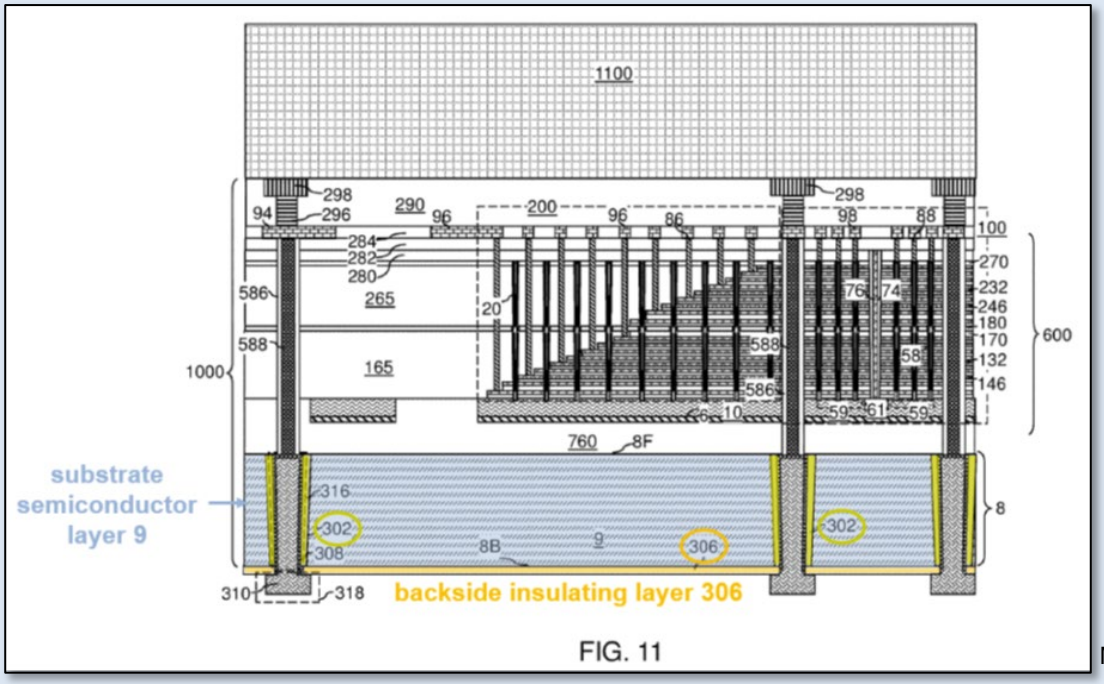


FIG. 11

Mushiga, Fig. 11.

POR-788, 64-68; Yang-788, ¶¶137-142; Sur-Reply-788, 24-25.

Mushiga Fails to Disclose or Render Obvious "a Substrate With an Isolation Structure"

Petitioner argues: "***The combination of elements described meets the specification's definition of a substrate for the same reasons as explained in Ground 1.***"

Reply-788, 30-31.

- But this is an improper new claim mapping
- Petitioner's *Apple v. Omni* case does not apply because it only permits new arguments when a claim construction is first raised in the POR, and here the construction was raised earlier in the POPR

> **Federal Circuit:** "In *Axonics*, this Court held that "***where a patent owner in an IPR first proposes a claim construction in a patent owner response, a petitioner must be given the opportunity in its reply to argue and present evidence of anticipation or obviousness under the new construction***, at least where it relies on the same embodiments for each invalidity ground as were relied on in the petition.""

Apple Inc. v. Omni MedSci, Inc., No. 2023-1034, 2024 WL 3084509, at *5 (Fed. Cir. June 21, 2024) (quoting *Axonics, Inc. v. Medtronic, Inc.*, 75 F.4th 1374, 1384 (Fed. Cir. 2023));
POPR-788, 39 ("the 'isolation structure' is … not part of the substrate as required by the Challenged Claims.");
POPR-909, 4 ("the claims require that the 'isolation region' or 'isolation structure' is part of the substrate"), 26, 29.

- The Federal Circuit was concerned with sandbagging by withholding a construction from a preliminary response and raising it for the first time after institution, which is not the situation here

> **Federal Circuit**: "Barring argument and evidence in a reply directed to a new claim construction proposed by the patent owner would create opportunities for sandbagging by the patent owner in order to create an estoppel. … ***[I]f instead of raising the issue in a preliminary response, a patent owner sits on its strongest claim construction arguments before institution and then raises them in response after institution, a patent owner could obtain a favorable final IPR decision and an estoppel without the Board's reaching the merits of any invalidity arguments under the newly adopted claim construction***."

Axonics, Inc. v. Medtronic, Inc., 75 F.4th 1374, 1384 (Fed. Cir. 2023)

Sur-Reply-788, 18-19, 24.

Mushiga Fails to Disclose or Render Obvious "a Substrate With an Isolation Structure"

Petitioner argues: "***The combination of elements described meets the specification's definition of a substrate for the same reasons as explained in Ground 1.***"

Reply-788, 30-31.

- Regardless of whether this is an improper new mapping, Petitioner's argument fails because it does not alter the fundamental deficiency with Mushiga—***the alleged isolation structure extends all the way through and beyond the surface of the substrate***

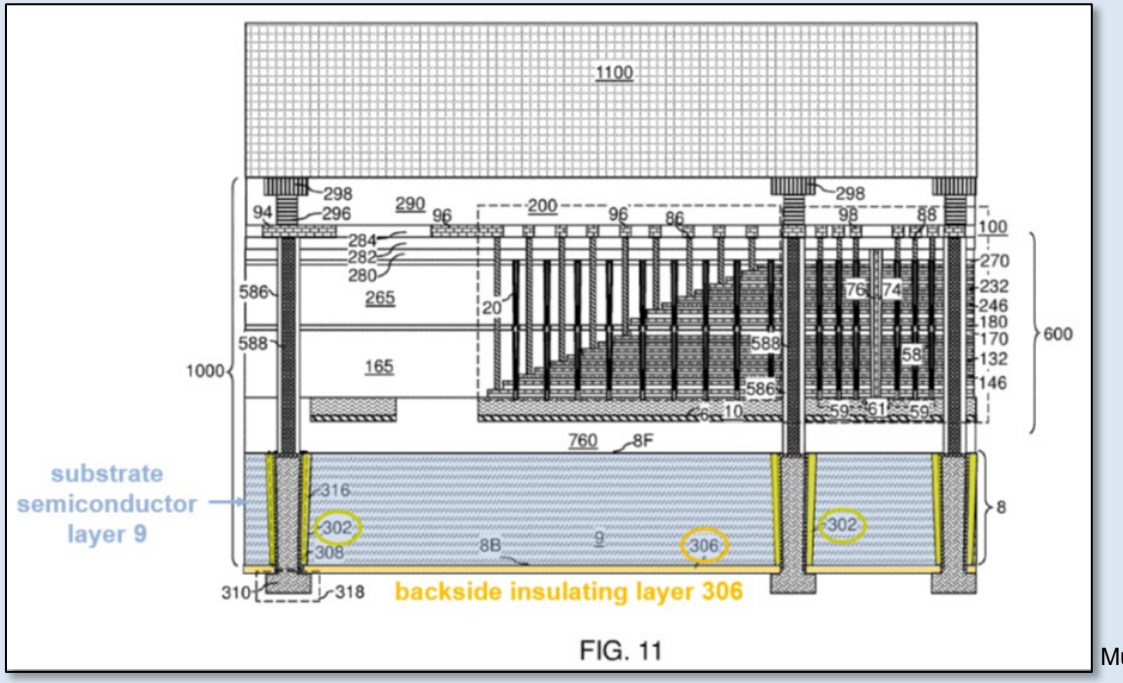


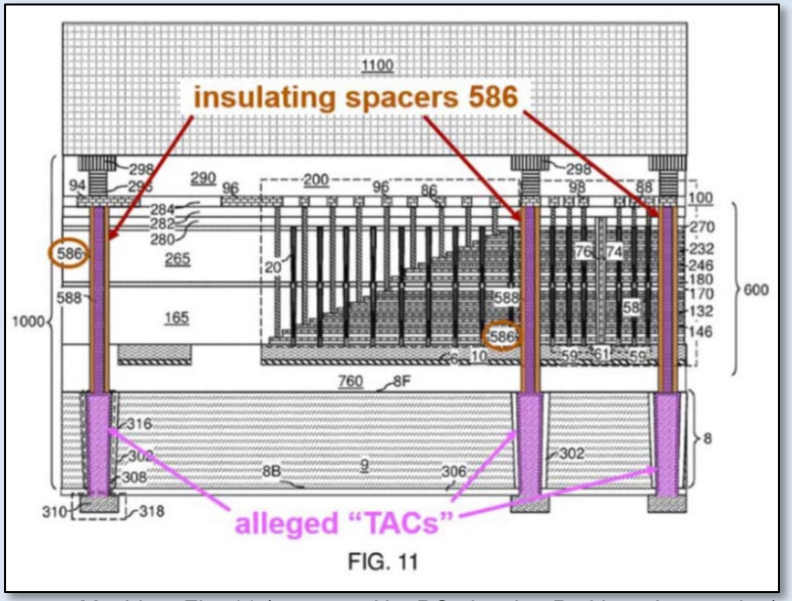
FIG. 11

Mushiga, Fig. 11.

Sur-Reply-788, 24-25.

Mushiga Does Not Disclose or Render Obvious "through array contacts (TACs) extending vertically through the dielectric and the isolation structures" (Limitation [15.h])

- Mushiga does not teach TACs extending through the ***same*** dielectric structure as required (slides 21-23)
- Only a single **alleged TAC** extends through any one **insulating spacer 586**



Mushiga, Fig. 11 (annotated by PO showing Petitioner's mapping).

- Petitioner's arguments regarding combining structures fail for the same reasons discussed for Ground 1B (slide 49)

POR-788, 79-80; Yang-788, ¶¶156-160; Sur-Reply-788, 28-29.

Mushiga Does Not Disclose or Render Obvious "a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack" (Limitation [15.c])

- The parties agree that "on" means "above" in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction (slide 18)

- The only alleged "dielectric structure" that arguably extends through the stack is ***insulating spacer 586***
- ***But insulating spacer 586 is not "on" the isolation structure because the insulating spacer is not above the alleged isolation structure in the z-direction (vertical direction)***

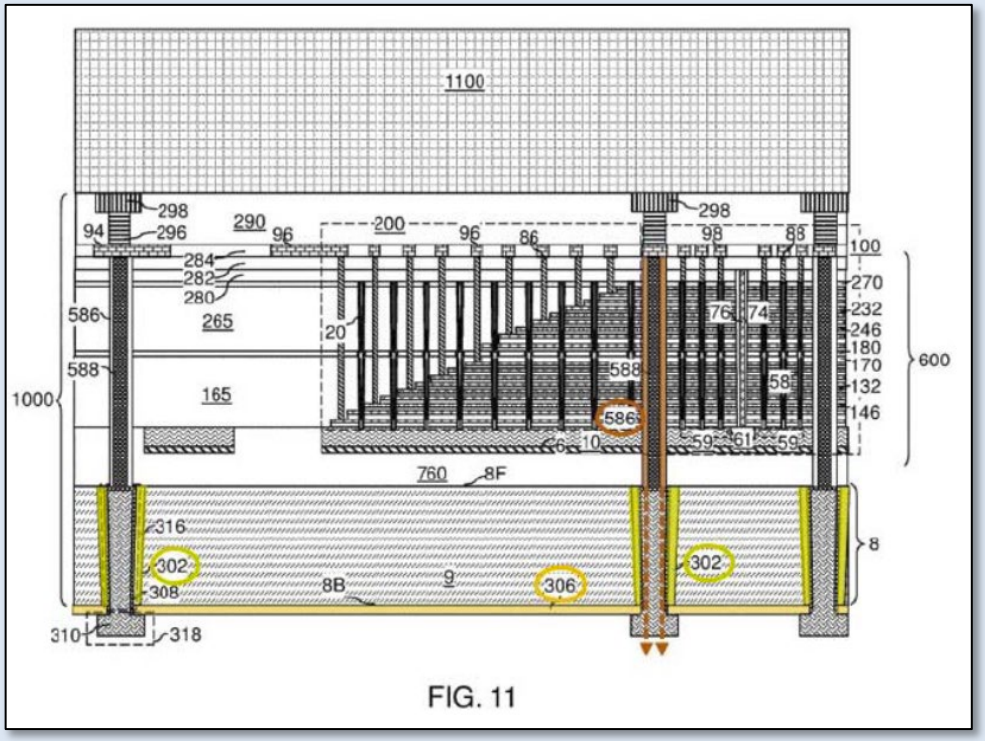


FIG. 11

Mushiga, Fig. 11.

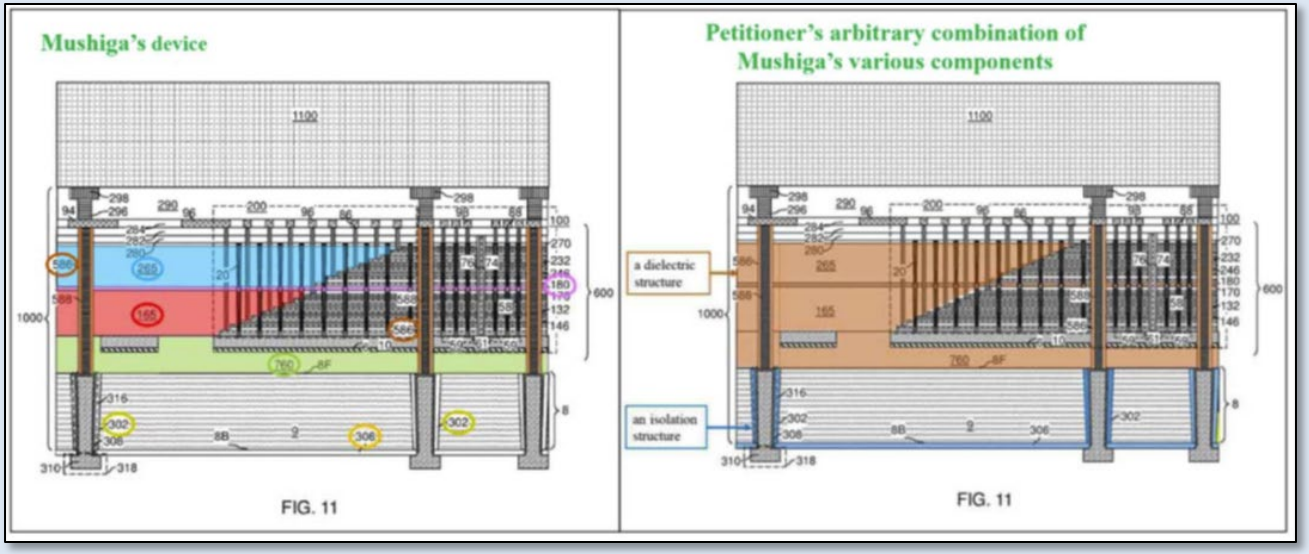
POR-788, 69-72; Yang-788, ¶¶143-147; Sur-Reply-788, 25-26.

Mushiga Does Not Disclose or Render Obvious "a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack" (Limitation [15.c])

Petitioner argues: "PO's argument is based on an unspoken premise: that a single dielectric structure may not include multiple components. That premise is false. Although further supported in this Reply's claim construction section, it scarcely needs to be said that ***a single structure can comprise multiple components.***"

Reply-788, 31-33.

- Petitioner arguments regarding combining structures fail for the same reasons discussed for Ground 1B (slide 49)
- In addition, ***none of the other alleged dielectrics extends vertically through the stack as required***
- Petitioner arbitrarily combines distinct structures that have distinct locations and roles in the '378



Mushiga, Fig. 11 (left annotated by PO; right annotated by Petitioner with top heading added by PO).

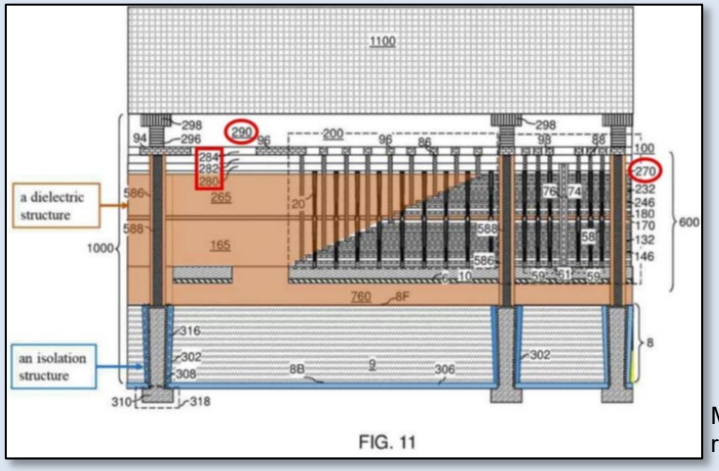
POR-788, 72-75; Yang-788, ¶¶148-151; Sur-Reply-788, 26-28.

Mushiga Does Not Disclose or Render Obvious "a dielectric structure on the isolation structure and extending vertically through the alternating conductor/dielectric layer stack" (Limitation [15.c])

Petitioner argues: "PO's argument is based on an unspoken premise: that a single dielectric structure may not include multiple components. That premise is false. Although further supported in this Reply's claim construction section, it scarcely needs to be said that ***a single structure can comprise multiple components.***"

Reply-788, 31-33.

- Petitioner selectively omits other **neighboring dielectrics** that, if included, would result in the TACs not extending all the way through the dielectric as required by the claims



Mushiga, Fig. 11 (annotated by Petitioner; red annotations added by PO).

- Petitioner cannot have it both ways—***either all of these purported dielectrics are the same structure or they are not***
- Dr. Lee admits hindsight:

Dr. Lee Deposition:
Q. Just to make sure I understand, you chose the particular dielectric structures in the Mushiga reference that you could combine to read on limitation 15.H of the '378 patent?
A. That is correct.

Ex. 2007, 57:13-17.

POR-788, 75-78; Yang-788, ¶¶152-154; Sur-Reply-788, 26-28.

Mushiga Fails to Disclose or Render Obvious "the Dielectric Structure Comprises a Through Array Contact Region of the 3D Memory Device" (Claim 17)

- Claim 17 requires that ***the TAC region is within or defined by the dielectric structure*** (*see* Slides 24-28)
- Petitioner's mapping fails because ***the alleged region extends beyond the dielectric structures and the other structures they contain, e.g. to include portions of metal structures 94 and bonding pad connection via structures 296***

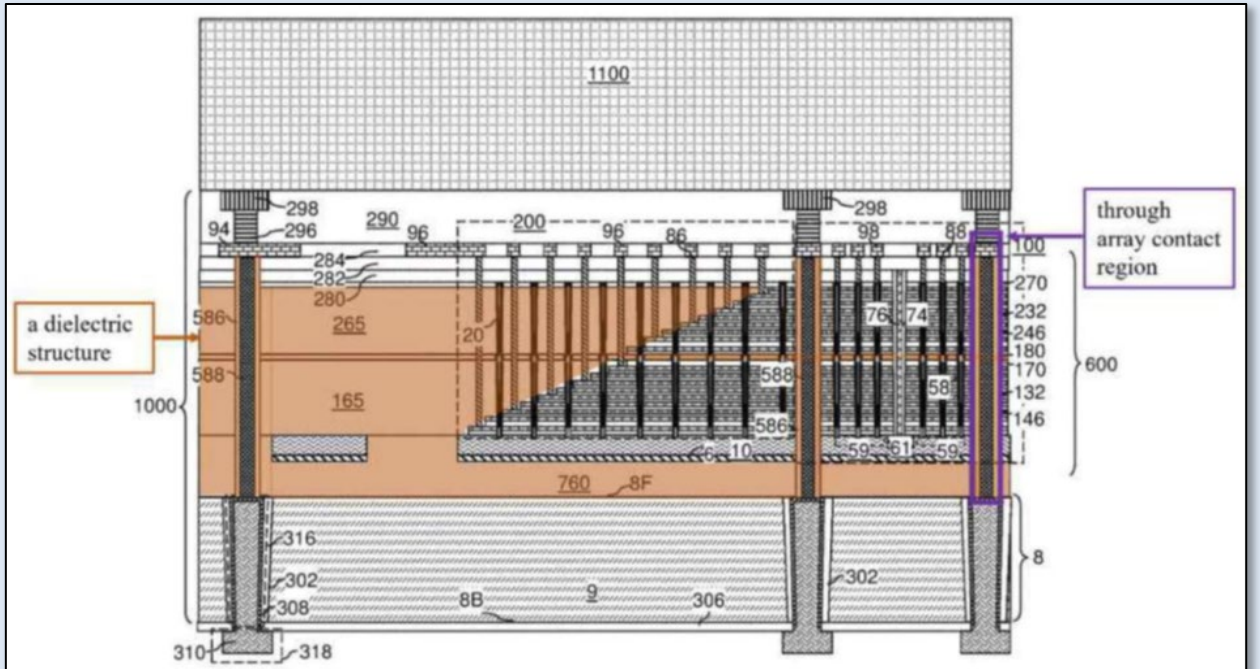


FIG. 11

Mushiga, Fig. 11.

POR-788, 80-82; Yang-788, ¶¶161-165; Sur-Reply-788, 29-30.

Mushiga Fails to Disclose or Render Obvious "the Dielectric Structure Comprises a Through Array Contact Region of the 3D Memory Device" (Claim 17)

Petitioner argues: "Instead of addressing Petitioner's theory head-on, PO attacks an ***annotated figure that inadvertently included parts of elements 94 and 296 in the TAC region***. POR 80-82. PO should have understood that these elements were not intended to be included from the text of the Petition, which does not even mention these elements."

Reply-788, 33-34.

- Petitioner's mapping that excludes elements 94 and 296 from the TAC region should be rejected as an improper new mapping
- Petitioner has not provided an illustration of the purported new region, making it impossible to identify or judge its boundaries

Sur-Reply-788, 29-30.