UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00789
U.S. Patent No. 10,861,872
Issue Date: December 8, 2020

Title: THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,861,872 PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42

TABLE OF CONTENTS **Page**

I. INTRODUCTION 1
II. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW 5
A. Grounds for Standing (37 C.F.R. §42.104(a)) 5
B. Notice of Lead and Backup Counsel and Service Information (37 C.F.R. §§42.8(b)(3-4), 41.10(a)) 6
C. Notice of Real-Parties-in-Interest (37 C.F.R. §42.8(b)(1)) 7
D. Notice of Related Matters (37 C.F.R. §42.8(b)(2)) 7
E. Fee for *Inter Partes* Review 8
F. Proof of Service 8
III. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§42.104(B)) 8
IV. INSTITUTION SHOULD BE GRANTED 9
A. There Are No Grounds For A §314 Discretionary Denial In This Case 9
1. Possibility of a Stay 9
2. Proximity of the Court's Trial Date 10
3. Investment in the Parallel Proceeding 10
4. Issue Overlap 11
5. Party Overlap 11
6. Other Circumstances 11
B. Denial Under §325(d) Would Be Inappropriate 12
V. TECHNOLOGY BACKGROUND 12
VI. THE '872 PATENT AND ITS PROSECUTION HISTORY 16
A. The '872 Patent 16
B. Prosecution History 21
VII. CLAIM CONSTRUCTION 23
A. "dummy source structure" (Claims 1-6, 11-13) 24
B. "surrounding" (Claims 1-6, 11-13) 27

VIII. LEVEL OF ORDINARY SKILL IN THE ART 33
IX. DESCRIPTION OF THE PRIOR ART 33
A. Park 33
B. Tessariol 37
X. GROUND 1: CLAIMS 1-6, 11, AND 13 ARE OBVIOUS OVER PARK 40
A. Claim 1: 40
1. [1.PRE] "A three-dimensional (3D) memory device, comprising:" 40
2. [1.A] "a substrate;" 41
3. [1.B] "a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;" 42
4. [1.C] "a staircase structure on one side of the memory stack;" 44
5. [1.D] "a staircase contact in the staircase structure; and" 48
6. [1.E] "a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact," 50
7. [1.F] "wherein each of the dummy source structures comprises a conductive contact." 62
B. CLAIM 2 64
1. [2] "The 3D memory device of claim 1, wherein the plurality of dummy source structures are located adjacent to the staircase contact." 64
C. Claim 3: 65
1. [3] "The 3D memory device of claim 1, wherein at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact." 65
D. Claim 4: 67

1. [4] "The 3D memory device of claim 1, wherein the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact." 67

E. Claim 5: 68

1. [5] "The 3D memory device of claim 1, wherein in a plan view, at least two of the plurality of dummy source structures are arranged in a first row that extends along a first lateral direction." 68

F. Claim 6: 70

1. [6] "The 3D memory device of claim 5, wherein in the plan view, at least two other dummy source structures are arranged in a second row that extends along a second lateral direction perpendicular to the first lateral direction." 70

G. Claim 11: 71

1. [11] "The 3D memory device of claim 1, comprising first and second staircase contacts, wherein at least one dummy source structure is located between the first and second staircase contacts." 71

H. Claim 13: 72

1. [13] "The 3D memory device of claim 1, wherein the conductive contact comprises a conductor layer, and wherein the at least one dummy source structure further comprises a spacer surrounding the conductor layer along a sidewall of the conductor layer, the spacer comprising a dielectric material." 72

XI. GROUND 2: CLAIMS 1-6 AND 11-13 ARE OBVIOUS OVER TESSARIOL 74

A. Claim 1: 74

1. [1.PRE] "A three-dimensional (3D) memory device, comprising:" 74

2. [1.A] "a substrate;" 75

3. [1.B] "a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;" 76

4. [1.C] "a staircase structure on one side of the memory stack;" 80

5. [1.D] "a staircase contact in the staircase structure; and" 82

6. [1.E] "a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact," 84

7. [1.F] "wherein each of the dummy source structures comprises a conductive contact." 89

B. Claim 2: 92

1. [2] "The 3D memory device of claim 1, wherein the plurality of dummy source structures are located adjacent to the staircase contact." 92

C. Claim 3: 93

1. [3] "The 3D memory device of claim 1, wherein at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact." 93

D. Claim 4: 94

1. [4] "The 3D memory device of claim 1, wherein the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact." 94

E. Claim 5: 94

1. [5] "The 3D memory device of claim 1, wherein in a plan view, at least two of the plurality of dummy source structures are arranged in a first row that extends along a first lateral direction." 94

F. Claim 6: 95

1. [6] "The 3D memory device of claim 5, wherein in the plan view, at least two other dummy source structures are arranged in a second row that extends along a second lateral direction perpendicular to the first lateral direction." 95

G. Claim 11: 97

1. [11] "The 3D memory device of claim 1, comprising first and second staircase contacts, wherein at least one dummy source structure is located between the first and second staircase contacts." 97

H. Claim 12: 98

1. [12] "The 3D memory device of claim 1, wherein at least two dummy source structures are located between the first and second staircase contacts." 98

I. Claim 13: 100

1. [13] "The 3D memory device of claim 1, wherein the conductive contact comprises a conductor layer, and wherein the at least one dummy source structure further comprises a spacer surrounding the conductor layer along a sidewall of the conductor layer, the spacer comprising a dielectric material." 100

XII. SECONDARY CONSIDERATIONS 101

XIII. CONCLUSION 102

TABLE OF AUTHORITIES

Page(s)

Cases

Apple Inc. v. Fintiv, Inc.,
Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020).....9, 10

Phillips v. AWH Corp.,
415 F.3d 1303 (Fed. Cir. 2005) 23

Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC,
IPR2019-01393, Paper 24 (PTAB June 16, 2020) 10, 11

Yangtze Memory Technologies Co., Ltd. v. Micron Technology, Inc. & Micron Consumer Products Group, LLC,
Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023).....7, 24

Statutes

35 U.S.C. §102.....21

35 U.S.C §112.....23

35 U.S.C. §§311-319.....1, 23

35 U.S.C. §314.....8, 9

35 U.S.C. §325.....8, 12

Other Authorities

37 C.F.R. §42.....1, 5, 6, 7, 8

LISTING OF EXHIBITS

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 10,861,872 B2 to Liu et al.
1002	File History of U.S. Patent No. 10,861,872 to Liu et al.
1003	Declaration of Dr. Sanjay Banerjee ("Banerjee")
1004	*Curriculum Vitae* of Dr. Sanjay Banerjee
1005	U.S. Patent No. 9,859,297 B2 to Park et al. ("Park")
1006	U.S. Patent Publ. No. 2019/0081061 A1 to Tessariol et al. ("Tessariol")
1007	Aritome, "NAND Flash Memory Technologies" (2016)
1008	Silvagni, "3D NAND Flash Based on Planar Cells," Computers 2017
1009	Micheloni et al., "Inside Solid State Drives (SSDs)" (2nd Ed. 2018)
1010	U.S. Patent No. 10,381,369 B2 to Kim et al.
1011	U.S. Patent No. 10,475,737 B2 to Tang et al.
1012	Certified English Translation of Chinese Patent Application Publ. No. CN108766971 to Liu ("Liu")
1013	Chinese Patent Application Publ. No. CN108766971 to Liu
1014	U.S. Patent No. 8,945,996 B2 to Tang et al.
1015	YMTC's Exemplary Infringement Claim Chart for U.S. Patent No. 10,861,872 – (Ex. 49) 128L [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]

EXHIBIT NO.	DESCRIPTION
1016	YMTC's Exemplary Infringement Claim Chart for U.S. Patent No. 10,861,872 – (Ex. 50) 176L [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1017	YMTC's Exemplary Infringement Claim Chart for U.S. Patent No. 10,861,872 – (Ex. 51) 232L [PROTECTIVE ORDER MATERIAL – FILED UNDER SEAL]
1018	Print out from Geographic Wiki, https://www.studycountry.com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-side (last visited Mar. 28, 2024)
1019	U.S. Patent No. 9,530,492 to Lee
1020	Minute Order, Dkt. No. 42, dated February 22, 2024 in *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL
1021	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1022	Docket from *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL
1023	Micheloni, "3D Flash Memories" (2016)

I. INTRODUCTION

Pursuant to 35 U.S.C. §§311-319 and 37 C.F.R. §42, Petitioner Micron Technology, Inc. ("Micron" or "Petitioner") respectfully requests *Inter Partes* Review ("IPR") of claims 1-6 and 11-13 ("the Challenged Claims") of U.S. Patent Number 10,861,872, titled "Three-Dimensional Memory Device and Method for Forming the Same" (Ex. 1001, "the '872 Patent"), and cancel those claims as unpatentable.

The '872 Patent relates to 3D NAND. The '872 Patent's earliest priority date is February 26, 2019, which follows more than a decade of 3D NAND development. The claims of the '872 Patent recite conventional 3D NAND components (i.e., substrate, memory stack, staircase structure, and a staircase contact) and "dummy source structures" that surround a staircase contact. Ex. 1001, Abstract. The dummy source structures allegedly improve the process known as the gate-line replacement process. *Id.*, 5:17-34. In that process, a stack is first built with alternating sacrificial layers (which are typically dielectric) and insulating layers. *Id.*, 4:30-33. Then, voids in the stack are formed, and the sacrificial layers are removed and replaced with conductive gate layers using the voids (i.e., the voids are the openings through which the etch and deposition materials are delivered into the stack). *Id.*, 4:46-55. Finally, the voids are filled, e.g., with a dielectric material. *Id.*, 4:44-46. The '872 Patent alleges that the prior art voids (i.e., gate line slits) create problems when

replacing the sacrificial layers with the conductive gate layers. *Id.*, 4:46-55. To solve these alleged problems, the '872 Patent proposes "replacing the [gate line slits] with dummy source structures." *Id.*, 5:30-34.

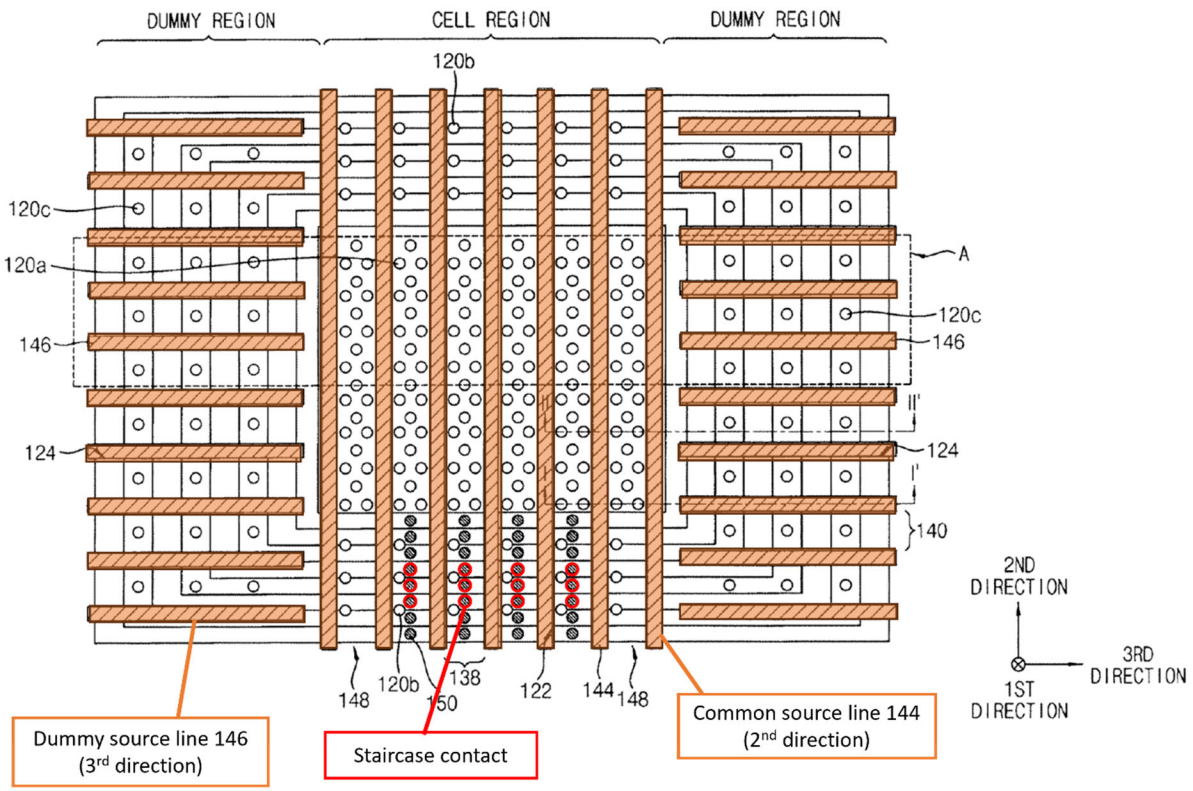
The '872 Patent describes the structure of the "dummy source structures" in broad terms. For example, the structures (1) may or may not be formed using the same etch process as the process for forming channel structures, (2) may or may not be circular, but may extend laterally to separate the memory stack into smaller units, and (3) may not even be inoperable (which is what "dummy" suggests) but, instead, may be operative structures such as interconnects. *Id.*, 2:14-17, 13:3-5, 11:44-49. What is clear is that the structures must occupy the openings that are used in the gate replacement process.

During the brief prosecution of the '872 Patent, the Examiner rejected the pending claims over the prior art, specifically identifying an alleged "dummy source structures." *See* Ex. 1002, 467-78. To distinguish this prior art, Applicant had to amend the claims to require that the "dummy source structures" comprise "a ***conductive contact***." *Id.,* 510-517.

Notwithstanding this amendment, nothing in the Challenged Claims is new or nonobvious. The first primary reference on which this Petition relies is Park. Park's dummy and common source lines are "dummy source structures." To start, Park's dummy and common source lines include the limitation added during prosecution:

that the dummy source structures include a conductive contact. Park, 3:23-24 ("The dummy source lines and the common source lines may include a same conductive material."). And just like the '872 Patent, Park's dummy and common source lines (1) occupy the voids that are used in the gate line replacement process, and (2) surround the staircase contacts. What's more, Park's dummy and common source lines divide the memory stack, which the '872 Patent discloses as an example of dummy source structures. Below is a plan view of Park's memory device, with its dummy and common source lines annotated in orange and the staircase contacts annotated in red.

FIG. 1



Id., Fig. 1.

The second primary reference on which this Petition relies is Tessariol. In the parallel district court case against Petitioner, Patent Owner ("PO") contends that "dummy source structures" need not occupy the voids that are used for the gate line replacement. Thus, Micron expects PO to dispute Micron's proposed construction that "dummy source structures" must occupy the voids that were used in the gate-line replacement process. Should PO do so, and should the Board agree with PO that occupying such voids is not required, in addition to being obvious over Park, the Challenged Claims are obvious over Tessariol. Tessariol employs dummy structures and conductive vias that are just like the '872 Patent's dummy source structures, except that the supporting pillars do not occupy voids that are used for the gate-line replacement process. But like Park, Tessariol's supporting pillars include the amendment added during prosecution: that the dummy source structures include a conductive contact. Tessariol, [0038] ("a conductive core 64 (e.g., metal material)"). Tessariol's dummy structures and conductive vias surround the staircase contacts, as shown below in a plan view.

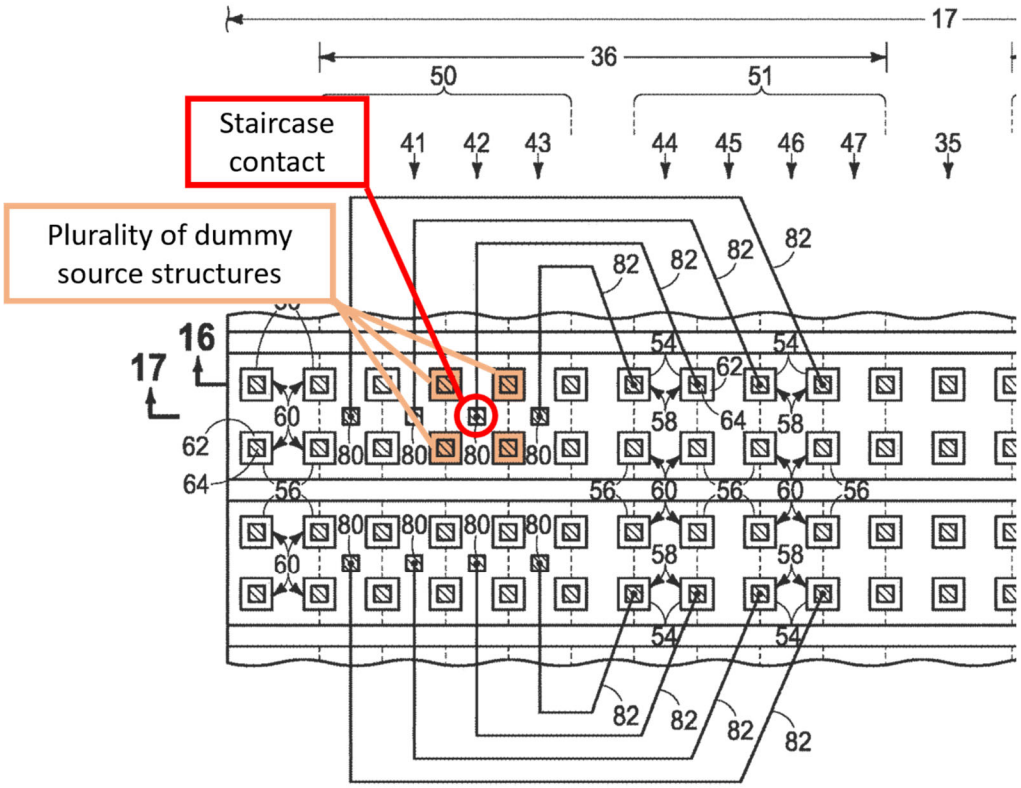


FIG. 15

Id., Fig. 15 (annotated).

Petitioner requests that the Board institute trial and find the Challenged Claims unpatentable as obvious under §103.

II. REQUIREMENTS FOR PETITION FOR INTER PARTES REVIEW

A. Grounds for Standing (37 C.F.R. §42.104(a))

Petitioner certifies that the '872 Patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR of the Challenged Claims of the '872 Patent on the grounds identified herein.

B. Notice of Lead and Backup Counsel and Service Information (37 C.F.R. §§42.8(b)(3-4), 41.10(a))

Pursuant to 37 C.F.R. §§42.8(b)(3-4) and 42.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

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Petitioner consents to service by electronic mail at the following addresses: PTABDocketJJL2@orrick.com, P52PTABDocket@orrick.com, PTABDocketJ3B3@orrick.com, and micron-ymtc_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner's Power of Attorney is attached.

C. Notice of Real-Parties-in-Interest (37 C.F.R. §42.8(b)(1))

Petitioner Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real-parties in interest.

D. Notice of Related Matters (37 C.F.R. §42.8(b)(2))

According to USPTO assignment records, the '872 Patent is currently assigned to Yangtze Memory Technologies, Co., Ltd. ("YMTC" or "Patent Owner"). YMTC has asserted the '872 Patent and U.S. Patent Nos., 10,658,378, 10,868,031, 10,937,806, 10,950,623, 11,468,957, 11,501,822 and 11,600,342 in a co-pending litigation, *Yangtze Memory Technologies Co., Ltd. v. Micron Technology, Inc. & Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) ("Co-Pending Litigation").

In addition to this Petition, Petitioner is filing petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation: Petition for *Inter Partes* Review of U.S. Patent No. 10,658,378, IPR2024-00788, Petition for *Inter Partes* Review of U.S. Patent No. 10,868,031, IPR2024-00790, Petition for *Inter Partes* Review of U.S. Patent No. 10,937,806, IPR2024-00791, Petition for *Inter Partes* Review of U.S. Patent No. 10,950,623, IPR2024-00794, Petition for *Inter Partes* Review of U.S. Patent No. 11,468,957, IPR2024-00792, Petition for *Inter Partes* Review of U.S. Patent No. 11,501,822, IPR2024-00795 and Petition for *Inter Partes* Review of U.S. Patent No. 11,600,342, IPR2024-00793.

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 325(d), and/or 37 C.F.R. §42.108(a).

E. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. §42.15(a), and any other required fees, to Deposit Account No. 15-0665.

F. Proof of Service

Proof of service of this Petition on the Patent Owner at the correspondence addresses of record for the '872 Patent is attached.

III. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§42.104(B))

Petitioner requests IPR of claims 1-6 and 11-13. This Petition discusses claim construction, explains why the claims are unpatentable, provides details regarding where the various claim limitations are found in the prior art, and is supported by the accompanying Declaration of Dr. Sanjay Banerjee ("Banerjee," Ex. 1003), a leading expert in the 3D NAND field. Ex. 1004.

Ground #1: Claims 1-6, 11, and 13 are obvious over U.S. Patent No. 9,859,297 (Ex. 1005, "Park").

Ground #2: Claims 1-6 and 11-13 are obvious over U.S. Patent Application Publication No. US 2019/0081061 (Ex. 1006, "Tessariol").

These references are prior art. *See* §IX.

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There Are No Grounds For A §314 Discretionary Denial In This Case

There is a pending district court action involving the '872 Patent. The PTAB has explained that it "will not … discretionarily deny institution in view of a parallel district court litigation where a petition presents compelling evidence of unpatentability." 6/21/22 Interim Procedure, 2, 4-5. Petitioner submits that it presents a compelling case here: the claims of the '872 Patent are unambiguously unpatentable.

Petitioner also notes that the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential) ("Fintiv"). In particular: the district court may stay the case, any potential trial will occur after the deadline for a final written decision, little district court work has occurred, petitioner diligently prepared this petition, and the petition is substantively strong.

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. Until this issue is adjudicated, any attempt to predict the outcome would require speculation. This

factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) ("Sand Revolution"); Fintiv at 12 (similar).

2. Proximity of the Court's Trial Date

On February 22, 2024, the district court entered a scheduling order which set a trial date of December 1, 2025. *See* Ex. 1020. As a result, if IPR proceedings are instituted, they should be completed well before the scheduled trial date. *See also* Ex. 1021 (statistics indicating that it takes on average 48.9 months to reach trial in district). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

To date, the parties and Court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings, no substantive progress has been made. The parties are months away from the exchange of infringement and invalidity contentions and have not taken any depositions. Fact discovery is in its infancy. No claim construction positions have been exchanged, no claim construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution* at 11.

The Board also has explained that institution is appropriate where "the petitioner filed the petition expeditiously…." *Fintiv* at 11. Here, Patent Owner

asserted eight different patents against Petitioner. *See* Ex. 1022. Yet, Petitioner proceeded with diligence filing approximately 5 months after being served with the original complaint and approximately 2 months after the filing of an amended complaint. *See id.* This also weighs strongly in favor of institution.

4. Issue Overlap

Given the early stage of the parallel proceeding, it is not yet possible to determine the amount of overlap. Patent Owner has not yet served infringement contentions or identified the asserted claims. Moreover, should the Board institute, Micron stipulates that it will not advance in District Court any invalidity defense that formed the basis of any of the grounds in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution* at 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

6. Other Circumstances

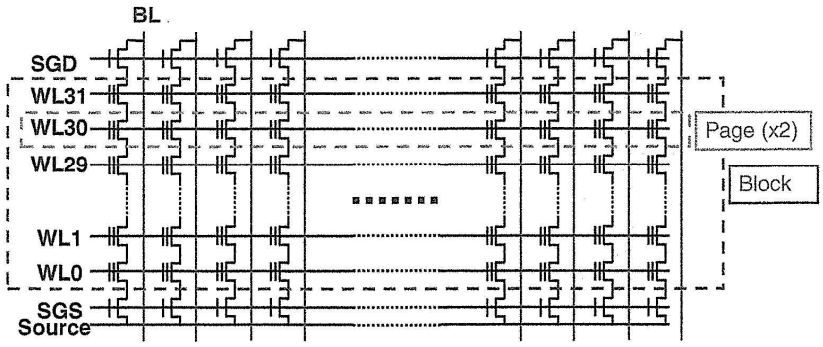
Here, Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that the Patent Office did not previously consider. Thus, this factor also weighs in favor of institution.

B. Denial Under §325(d) Would Be Inappropriate

Neither PO nor the Examiner cited or discussed Park or Tessariol during prosecution of the '872 Patent. *See generally* Ex. 1002. Moreover, as Section VI.B explains, the Examiner allowed the claims because the Applicant amended them to require that the "dummy source structures" include conductive elements. Park's "dummy source structures" have conductive contacts (a conductive core). *See* Section X.A.7. Tessariol also employs "dummy source structures" with conductive contacts (conductive cores). *See* Section XI.A.7.

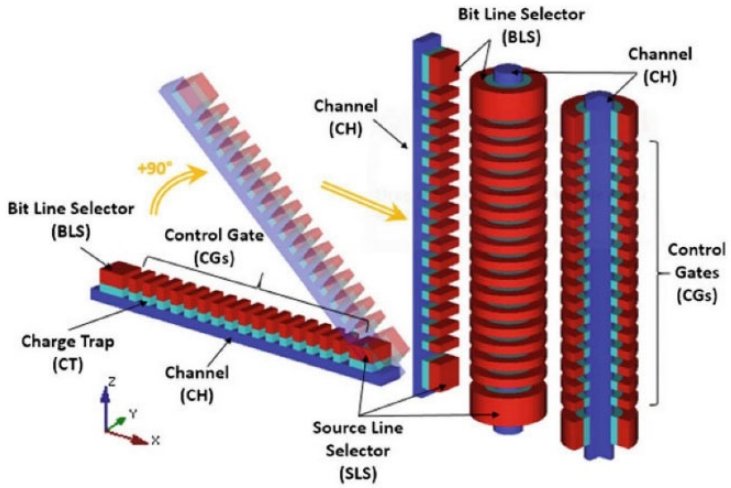
V. TECHNOLOGY BACKGROUND

The '872 Patent and the prior art discussed in this Petition relate to three-dimensional (3D) memory devices, *e.g.*, 3D NAND memory devices. In NAND memory devices, NAND cells are arranged in "strings" with multiple cells "connected in series." Ex. 1007, 38. Early NAND devices were formed as two-dimensional arrays of cells on a substrate surface. *Id.*, 58.

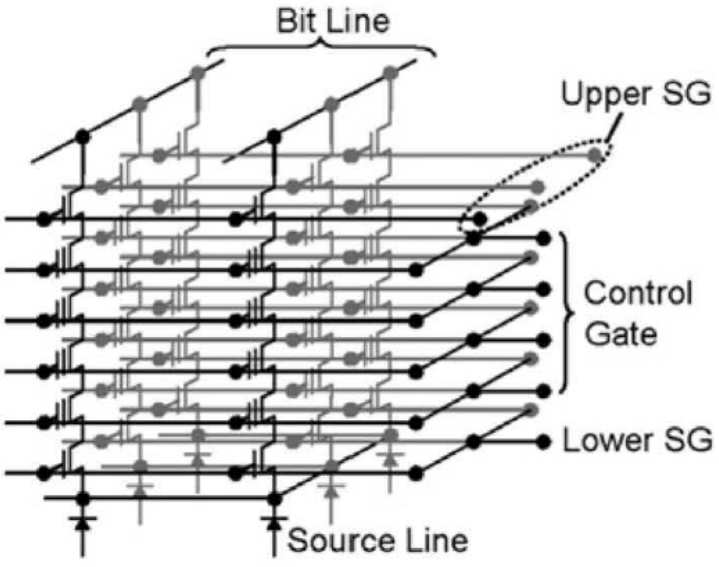


Id., 40. As shown, the cells are grouped into "page[s]" extending along the word lines and "block[s]." *Id.* "[T]o further scale down the memory cell size," "three-

dimensional (3D) NAND flash cells" were developed. *Id.*, 292. "Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block" and "turning the 2D NAND string upside," "resulting" in a "3D structure" with a "vertical channel." Ex. 1008, 3.

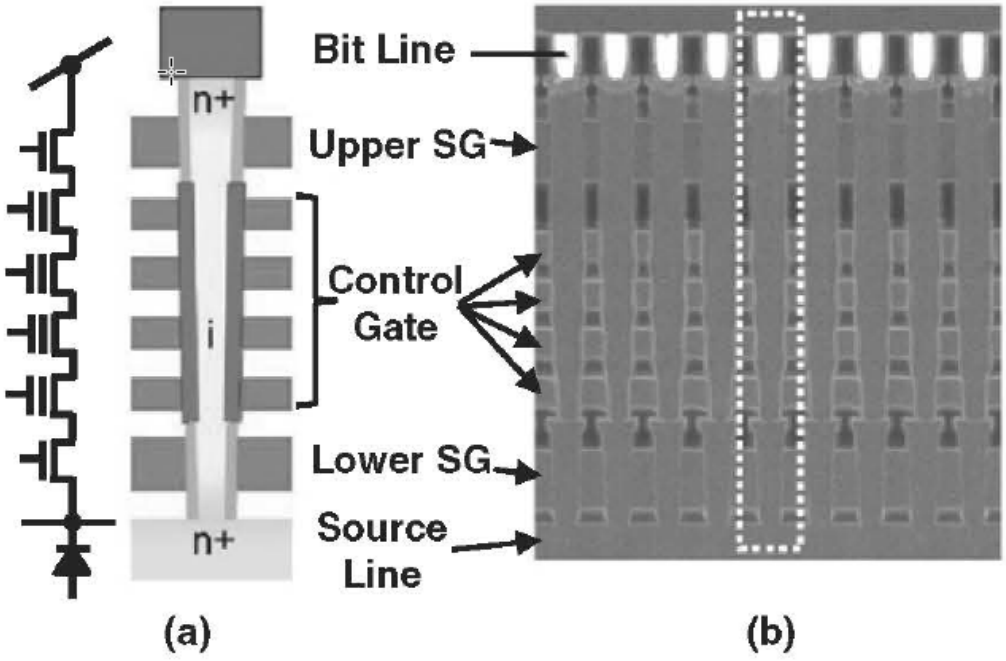


Ex. 1009, 122. Multiple such vertical channels are then repeated in a three-dimensional array:



Ex. 1007, 296; *see also* Banerjee ¶¶ 46-53.

3D NAND includes "multi-stacked layers of gate (plate)" material alternated with "dielectric" in a "[s]tack." Ex. 1007, 294. A "through-hole[]" channel (also known as a channel structure) "filled by memory film … and channel poly-Si" passes through the layers to form the string of vertically arranged memory cells. *Id.*, 295. "Each" layer of "electrode plate acts as a control gate." *Id.* A particular vertical memory cell "string is selected by a bit line and an upper select gate (upper SG)." *Id.*, 295-296. A memory cell "is located in the intersection of a control gate plate" and the memory film/poly-Si channel. *Id.* The lowest layer is a "select gate (lower SG)" allowing the strings to connect to a lower "common source." *Id.*, 295, 297. An example 3D NAND vertical memory cell string is shown below:



Id., 296; Banerjee ¶ 54.

The stacked structure in 3D NAND devices typically include a core region, which includes the memory cells, and a peripheral region, which includes a connection region known as the staircase region. Ex. 1010 (U.S. Pat. No. 10,381,369), 5:43-6:11, 12:20-27. Staircase structures were well known and structurally provide landing areas on the control gates for contacts (below, the contacts 60 connect to different control gates):

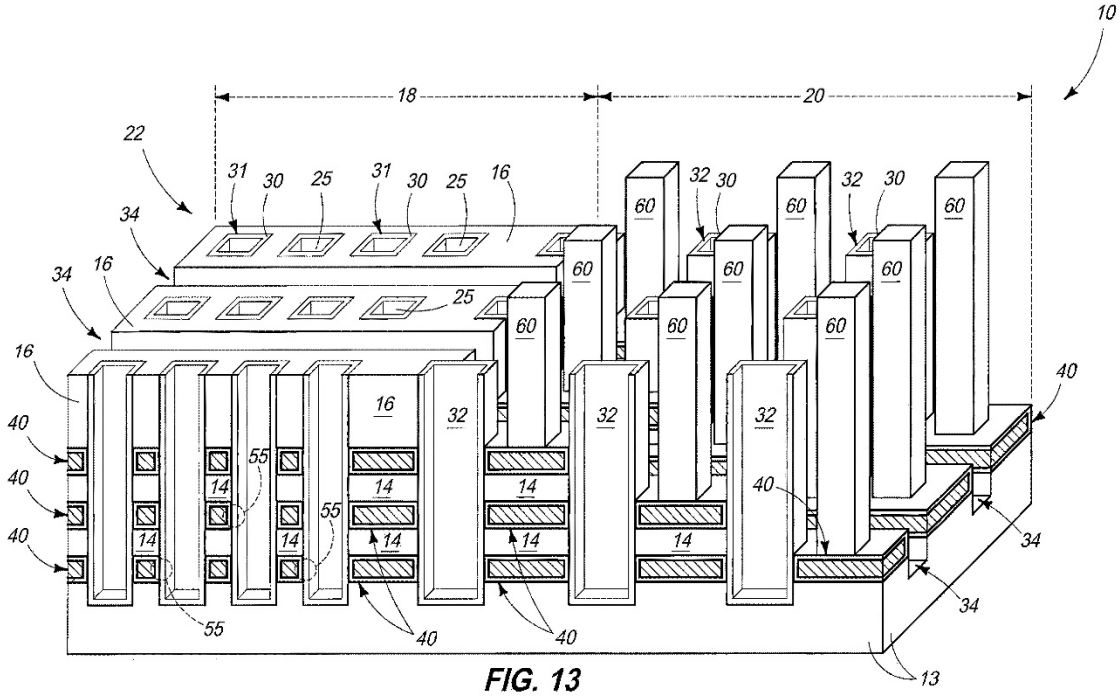


FIG. 13

Ex. 1011 (U.S. Pat. No. 10,475,737), Fig. 13, 4:56-64, 8:45-56.

One method of forming 3D NAND memory devices is to form the alternating stack of sacrificial gate layers and dielectric layers, and then replace the sacrificial gate layers with metal layers. Ex. 1012, [0062]. This is known as a gate replacement process. It was known that to perform this gate replacement process, "support

pillars" were necessary to be included in the staircase structure (the support pillars extend through the stacked structure) to "prevent the stacked structure from collapsing." *Id.* [0002], [0062]; *see also* Ex. 1014, 5:64-6:2 ("dummy" structures have been used for a "load carrying ability of an operative structure"). Support pillars may be made with different materials, e.g., materials of a conductive via or materials of a channel structure, and may be a dummy structure (serve no other role than a supporting member) or an active structure (e.g., also serve as an interconnect to connect two circuit elements). *Id*., 6:5-38, 7:19-23; Ex. 1012, [0044]; Tessariol, [0037], [0038], [0041]; Banerjee ¶¶ 55-58.

VI. THE '872 PATENT AND ITS PROSECUTION HISTORY

A. The '872 Patent

The application that matured into the '872 Patent was filed on May 2, 2019 and is a continuation of application No. PCT/CN2019/076186, filed on February 26, 2019. Ex. 1001. This Petition therefore assumes that February 26, 2019, is the priority date for the '872 Patent (the "Priority Date").

The '872 Patent is directed to "[t]hree-dimensional (3D) memory devices and methods for forming the 3D memory devices." Ex. 1001, Abstract. Three-dimensional (3D) memory devices include basic elements such as a substrate, a memory stack comprised of interleaved conductive layers and dielectric layers

formed on the substrate, a staircase structure, staircase electrical contacts, and dummy structures. *Id.*, 1:34-43; Banerjee, ¶ 59.

The '872 Patent addresses the traditional gate replacement process. Ex. 1001, 1:56-58, 4:30-33; 4:46-55; 5:17-28. As Section V discusses, during this process, the sacrificial layers are etched away and replaced with conductive layers to form gate layers (also known as word lines). *Id.*, 1:56-58, 4:30-33; 4:46-55. The '872 Patent alleges that as three-dimensional (3D) memory devices continued to scale down, the gate replacement process would be more challenging. *Id.*, 4:37-38. The '872 Patent discusses the use of gate line slits ("GLS") in the gate replacement process. GLS divide the interleaved sacrificial/dielectric stack (also known as a memory stack) into smaller memory stacks. *Id.*, 4:37-46. A GLS has "large dimensions and is filled with an insulation structure formed in a trench." *Id.* To form the GLS structure, trenches (voids) are etched through the stack. *Id.*, 4:44-49. These trenches are used in the gate-line replacement process, namely, they are used to etch the sacrificial gate layers and are used to deposit the gate lines (in other words, the etch and deposition material is sourced through the trench). *Id.*, 4:46-48. Annotated Figure 5 below shows a top view of a memory stack that is split into smaller memory stacks by GLSs.

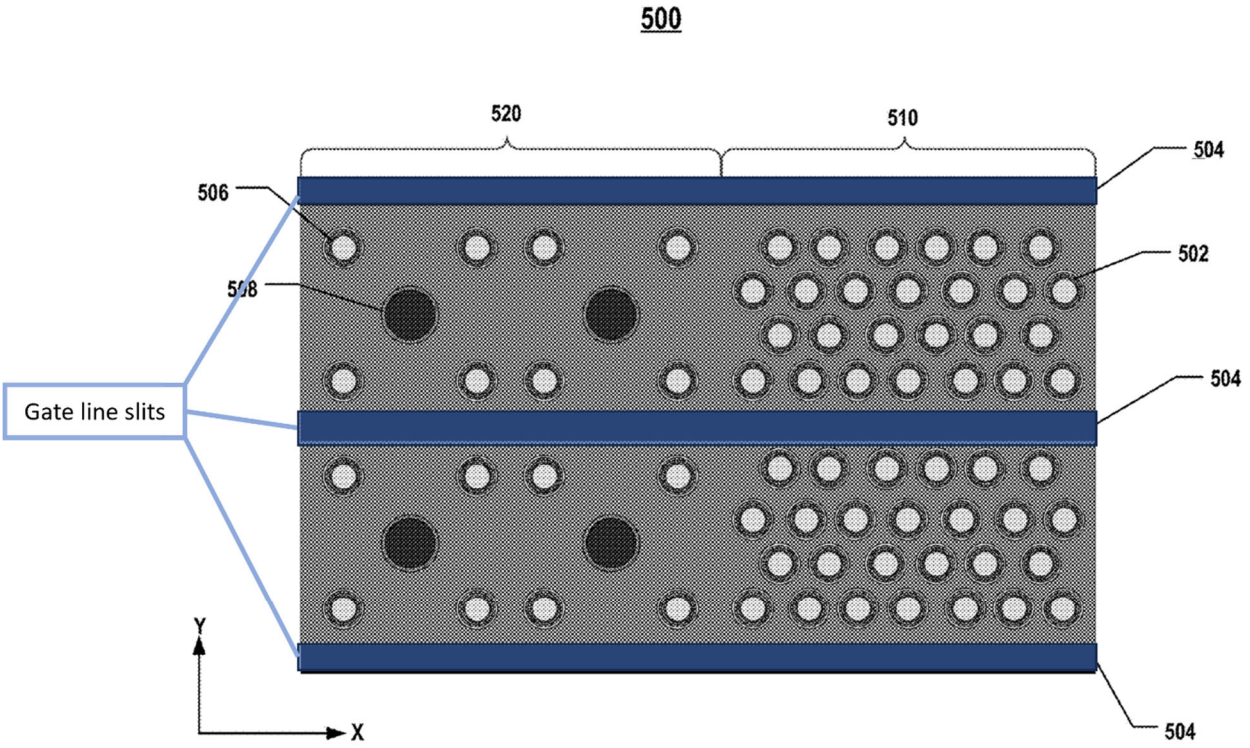


FIG. 5

The '872 Patent alleges that "[u]sing GLSs to perform the gate-replacement process has drawbacks. For example, in the staircase region, the large lateral distance between adjacent GLSs can cause conductive material to be unevenly filled in the lateral recesses formed after the removal of the sacrificial layers, resulting in voids in the formed gate electrodes." Ex. 1001, 4:49-55. Allegedly, this is because "conductive materials for forming the gate electrodes need to travel a relatively long distance between adjacent GLSs 504 to fill in the lateral recesses formed after the removal of sacrificial layers." *Id.*, 5:17-20; Banerjee ¶¶ 60-62.

The ’872 Patent purports to solve this problem by replacing the GLSs in the gate replacement process with “dummy source structures.” Ex. 1001, 5:31-34. Annotated Figure 2A below shows the etched dummy source hole in the staircase structure.

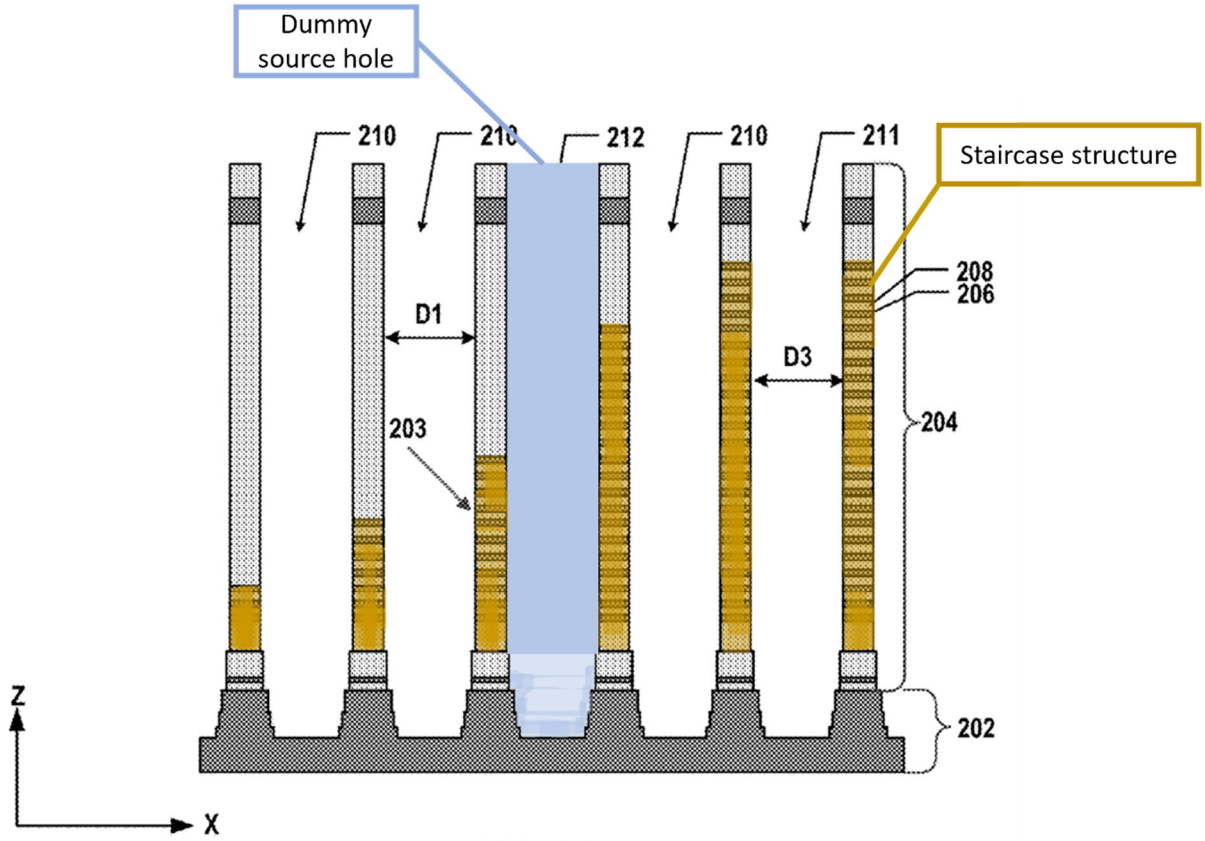


FIG. 2A

Id., Fig. 2A. The ’872 Patent discloses using this void for the gate replacement process. *Id.*, 15:16-25.

After the gate replacement process is complete, the ’872 Patent discloses that dummy source structures “may include an insulating spacer layer in a dummy source hole and a conductive contact within the spacer layer.” Ex. 1001, 5:37-43. An

insulating spacer (177) first lines the dummy source hole and then conductive material is deposited to form a dummy source structure (179), shown below in Figure 1D:

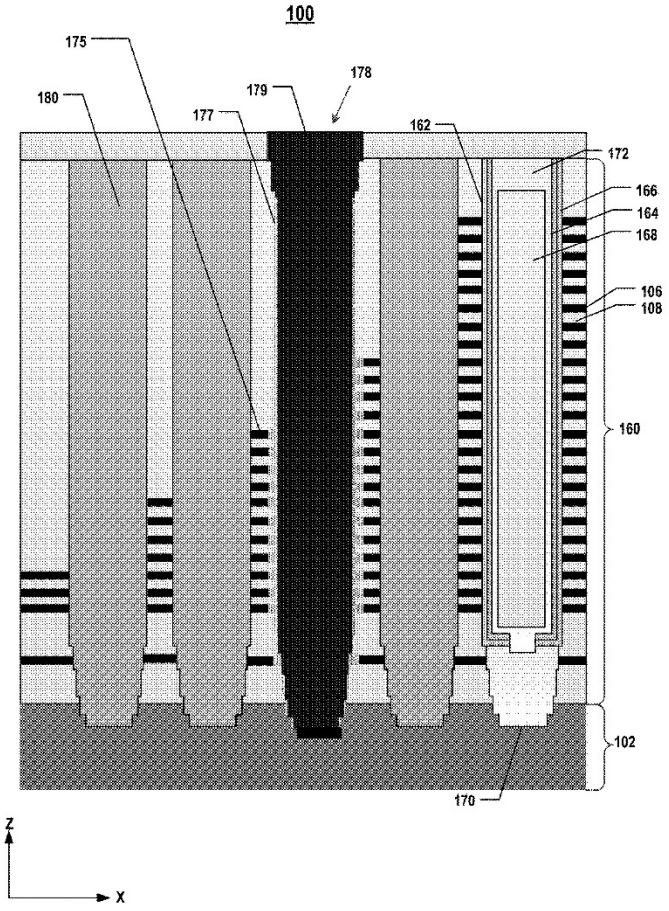


FIG. 1D

Id., Fig. 1D, 5:37-40; Banerjee ¶¶ 63-66.

The ’872 Patent claims that using dummy source structures instead of GLSs may allow gate electrodes “to be formed with improved uniformity and quality, reducing the resistivity of the gate electrodes/word lines.” Ex. 1001, 5:49-52. Because conductive material “travels shorter distances to fill up the lateral recesses

for forming the gate electrodes, the gate electrodes are less susceptible to voids or density nonuniformity." *Id.*, 5:55-58; Banerjee ¶ 67.

B. Prosecution History

There was only one substantive Office Action during prosecution.

On June 11, 2020, the Examiner rejected claims 1-13 under 35 U.S.C. §102(a)(l) as anticipated by U.S. Pub. No. 2016/0293622A1 ("Jeong"). The Examiner found that Jeong disclosed a three-dimensional (3D) memory device with a substrate, a memory stack comprising interleaved conductive/dielectric layers on the substrate, a staircase structure on one side of the memory stack, a staircase contact in the staircase structure, and a plurality of dummy source structures extending vertically through the staircase structure and surrounding the staircase contact. Ex. 1002, 470. The Examiner found that Jeong discloses "dummy pillars DP1 and DP2" that "function as a mechanical support for conductive layers" which were akin to "dummy source structures." *Id.* The Examiner additionally found that Jeong's dummy pillars DP1 and DP2 could also be dummy channel structures.[1] *Id.*, 472.

[1] Claims 7-10 and 14-20 concern "dummy channel structures" and are not being challenged in this Petition.

On August 14, 2020, the Examiner and the Applicant discussed during a telephone interview the distinction between "dummy source" and "dummy channel" as contrasted with Jeong's "dummy pillar" structure and possible amendments. Ex. 1002, 505. Based on the interview, the Applicant amended claims 1 and 8 on August 18, 2020 to add the limitation "wherein each of the dummy source structures comprises a conductive contact." *Id.*, 510-511, 513. The Applicant argued that this feature is "not found in Jeong" because Jeong's "dummy pillars do not include conductive contacts" whereas, citing the specification, "[a] dummy source structure 178 includes a dummy source hole filled with conductive materials …." *Id.*, 513-514. The Applicant further emphasized the specification passage that states: "dummy source structures 178 can [also] laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks," and an exemplary dummy source structure is shown in Figure 1D. *Id.*, 514. In the same amendment and request for reconsideration, the Applicant cancelled claims 15-20 and added claims 21-26.[2] *Id.*, 513.

The Examiner did not consider any other prior art references in connection with or following the August 14, 2020 claim amendments, and allowed claims 1-14

[2] Application claims 21-23 correspond to '872 Patent claims 8-10 and application claims 24-25 correspond to '872 Patent claims 11-12.

and 21-26 on October 26, 2020. Ex. 1002, 524. The reasons for allowance were that Jeong did not disclose a dummy structure that comprised a conductive contact and that Jeong's dummy pillars DP1 and DP2 could be "considered as the dummy channel structures." *Id.*, 525-26.

VII. CLAIM CONSTRUCTION[3]

The Board in IPR proceedings applies the same *Phillips* claim construction standard that is used in federal district court cases. *See Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005). For purposes of institution, Petitioner submits that only "dummy source structure" requires construction and that the rest of the terms of the '872 Patent's claims should be afforded their plain and ordinary meaning. The discussion below, however, also addresses the term "surrounding" to clarify that "surrounding" does require fully encircling.

[3] Petitioner expressly reserves the right to challenge in district court litigation one or more claims (and claim terms) of the '872 Patent for failure to satisfy the requirements of 35 U.S.C §112, which cannot be raised in these proceedings. *See* 35 U.S.C. § 311(b). Nothing in this Petition shall be construed as a waiver of such challenge or agreement that the requirements of 35 U.S.C. §112 are met for any claim of the '872 Patent.

A. "dummy source structure" (Claims 1-6, 11-13)

The term "dummy source structure" is a limitation of all Challenged Claims.

Petitioner contends that the term "dummy source structure" would have been understood to mean a "structure that occupies the void that was used for the gate replacement process." In the Co-Pending Litigation, PO appears to be interpreting this limitation to mean that the dummy source structure need not be formed in the voids that are used for the gate line replacement process. This is apparent from PO's infringement contentions that map the dummy source structures to structures that occupy voids that have nothing to do with gate-line replacement. Ex. 1015 [128L chart], 3; Ex. 1016 [176L chart], 3-4; Ex. 1017 [232L chart], 3-6.

Petitioner's construction is supported by the specification and file history of the '872 Patent. The '872 Patent seeks to address 3D memory structural issues that arise during the gate replacement process "by replacing the [gate line slits] with dummy source structures." Ex. 1001, 5:30-34. The '872 Patent explains that gate replacement processes can become more challenging as three-dimensional memory devices scale down because gate line slits "ha[ve] large dimensions" that, when used to perform the gate replacement process, create problems such as unevenness and gaps in gate electrodes. *Id.*, 4:44-50. In the staircase region, "the large lateral distance between adjacent [gate line slits] can cause conductive material to be unevenly filled in the lateral recesses formed after the removal of the sacrificial

layers, resulting in voids in the formed gate electrodes." *Id.*, 4:50-55. The large area of gate line slits also "limit[s] the usable space on the wafer surface to place other components, such as staircase contacts." *Id.*, 4:65-67; Banerjee ¶ 74.

Replacing gate line slits with "dummy source structures" allegedly solves the aforementioned issues. For example, the gate replacement process performed with dummy source holes results in gate electrodes "less susceptible to voids or density nonuniformity." Ex. 1001, 5:49-58. Since the "gate-replacement process can be performed to deposit a conductive material through the dummy source holes that subsequently form the dummy source structures," the "conductive material travels shorter distances to fill up the lateral recesses for forming the gate electrodes." *Id*; Banerjee ¶ 75.

Note that the '872 Patent describes solving the alleged problems by using the voids that are later occupied by the "dummy source structures," namely, "dummy source holes." For example, the '872 Patent discloses that because the "gate-replacement process can be performed to deposit a conductive material **through the dummy source holes that subsequently form the dummy source structures**," the "conductive material travels shorter distances to fill up the lateral recesses for forming the gate electrodes." Ex. 1001, 5:49-58. Nonetheless, the specification defines the "dummy source structures" as what occupies the "dummy source holes": "dummy source holes that subsequently form the dummy source structures." *Id.*

Thus, when the '872 Patent states that it is "replacing the [gate line slits] with dummy source structures" (*Id.*, 5:30-34), what it means is that it is "replacing the [gate lines slits] with [dummy source holes in which the dummy source structures are subsequently formed]." *Id.*, 4:65-67; Banerjee ¶¶ 76-77.

While the specification makes clear that a "dummy source structure" occupies the void used for the gate replacement process, the specification does not impose any meaningful limitation on the actual structure of the dummy source structure (the claims only require that the structures include a conductive contact). In fact, the specification states that "[d]ifferent layouts, patterns, and designs" for the dummy source structure may be adopted "based on the size of the staircase region." Ex. 1001, 8:51-53. And the specification states that the dummy source holes, which the dummy source structures occupy, may or may not be made using the same process that makes the dummy channel holes. *Id.*, 13:3-5. The dummy source structures and dummy channel structures also may be the same size. *Id.*, 8:11-19. Notably, the dummy source structure may assume the same shape as a gate line slit, because the specification states that "dummy source structures 178 can ***laterally separate*** 3D memory device 100 into multiple memory regions, such as memory blocks." *Id.*, 11:44-46 (emphasis added). This is precisely what the '872 Patent admits that gate line slits do: "[f]or example, in some 3D memory devices such as charge trap 3D NAND memory devices, gate line slits (GLSs) are formed to divide an array of

memory strings (e.g., in the inner region of a 3D memory device) and/or dummy channel structures (e.g., in the staircase region of the 3D memory device) into different memory regions." *Id.*, 4:38-44. Further, while the claim term includes the word "dummy," the specification explains that the structure might not even be an inoperable structure. Rather, the specification states that "dummy source structures" can "contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices." *Id.*, 5:41-43, 16:63-66; Banerjee ¶¶ 78-80.

During prosecution, the Applicant further emphasized the portion of the specification which states: "dummy source structures 178 can [also] laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks." Ex. 1002, 514. This again illustrates that a dummy source structure may assume many forms, including those that are, or resemble, gate line slits. Banerjee ¶ 81.

As demonstrated below, Ground 1 renders the Challenged Claims obvious under Petitioner's construction and PO's construction, while Ground 2 renders the Challenged Claims obvious under PO's construction.

B. "surrounding" (Claims 1-6, 11-13)

The term "surrounding" is a limitation of all Challenged Claims.

Independent claim 1 recites "the plurality of dummy source structures surrounding the staircase contact." Petitioner contends that "surrounding," in the

context of the '872 Patent, does not require that the dummy source structures form a border that fully encloses the staircase contact. This is evident from the specification, claims, and extrinsic evidence.

To start, the specification and claims make clear that "surround" does not even require that four dummy source structures surround the staircase contact (e.g., radially around the staircase contact at angles 0, 90, 180, and 270 degrees). The specification discloses that "the number of dummy source structures surrounding one or more dummy channel structure 124 may be more or less than eight, six, or four." Ex. 1001, 8:8-11. In other words, there may be less than four dummy source structures that "surround" a word line contact. The claims use "surround" in the same way. Dependent claim 15, which depends on claim 14, recites: "wherein at least one dummy channel structure is surrounded by at least four dummy source structures." *Id.*, Claim 15. Under the doctrine of claim differentiation, this implies that "surrounded" in independent claim 14 covers implementations in which fewer than four dummy source structures surround a single dummy channel structure. As shown below, a preferred embodiment employs four dummy source structures (126) around staircase contact (122). If one of these dummy source structures were removed, there would be only three dummy source structures left, leaving even more openings around the staircase contact.

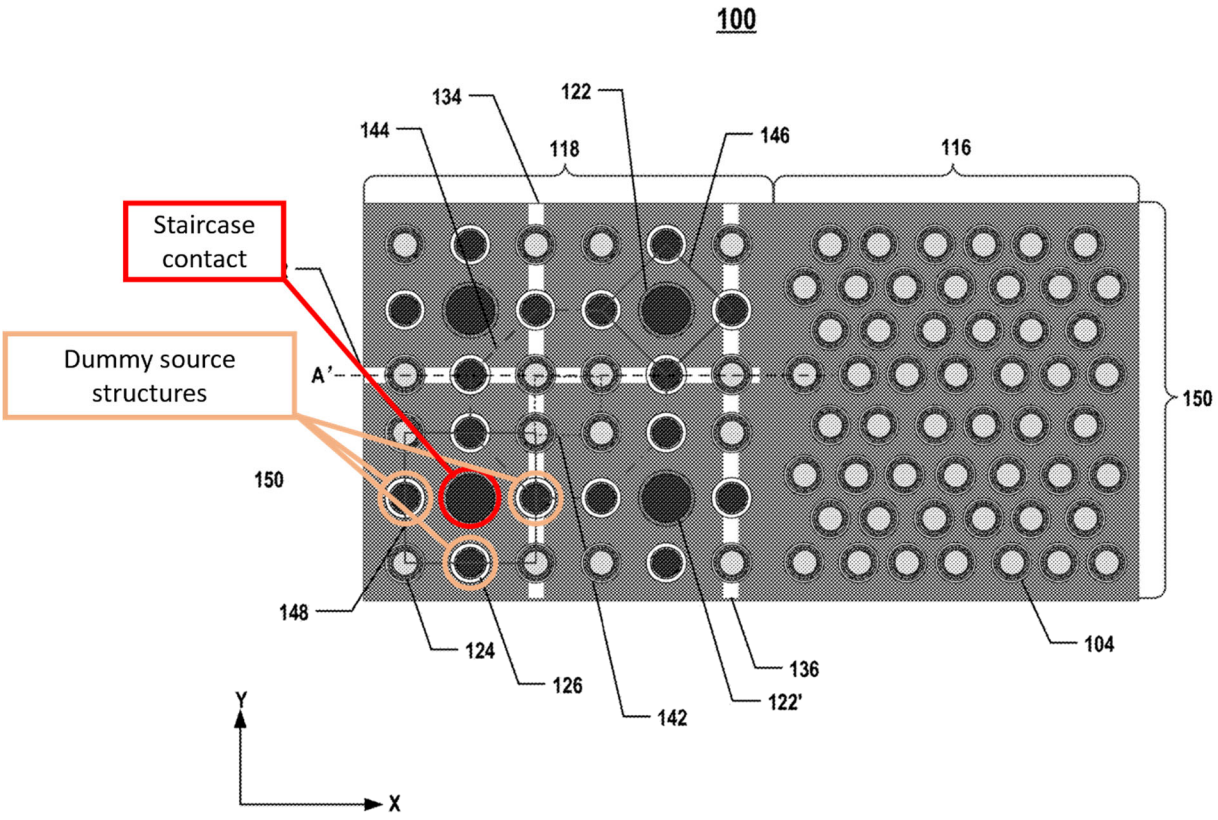
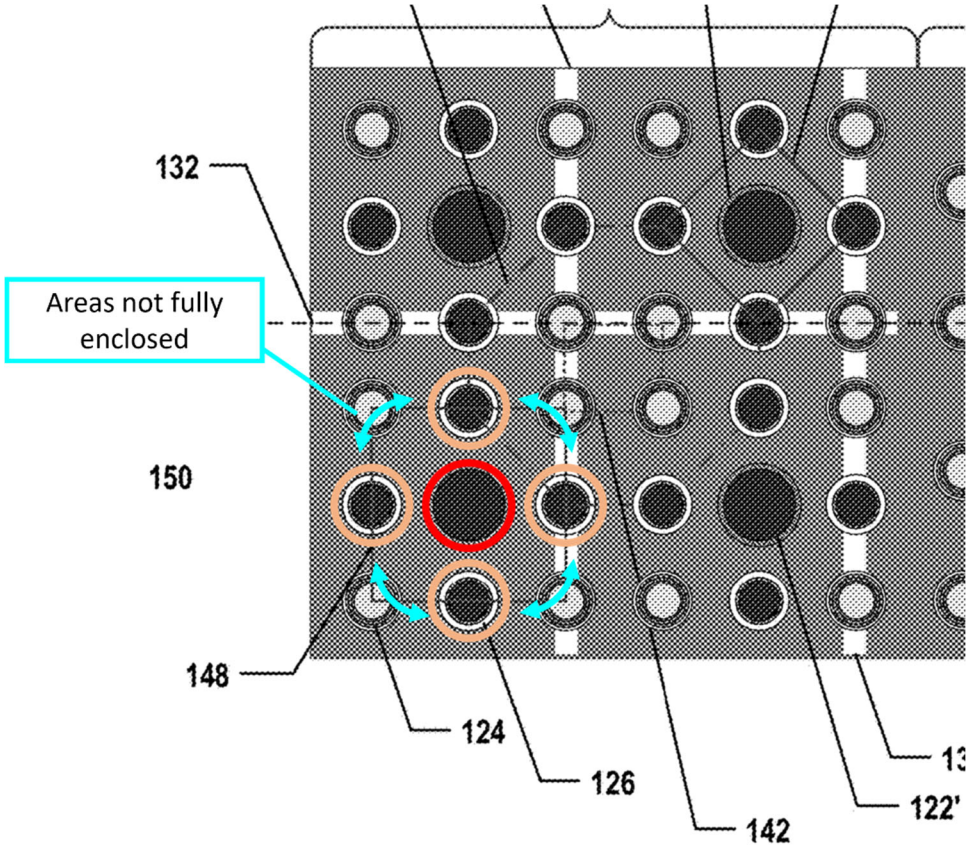


FIG. 1A

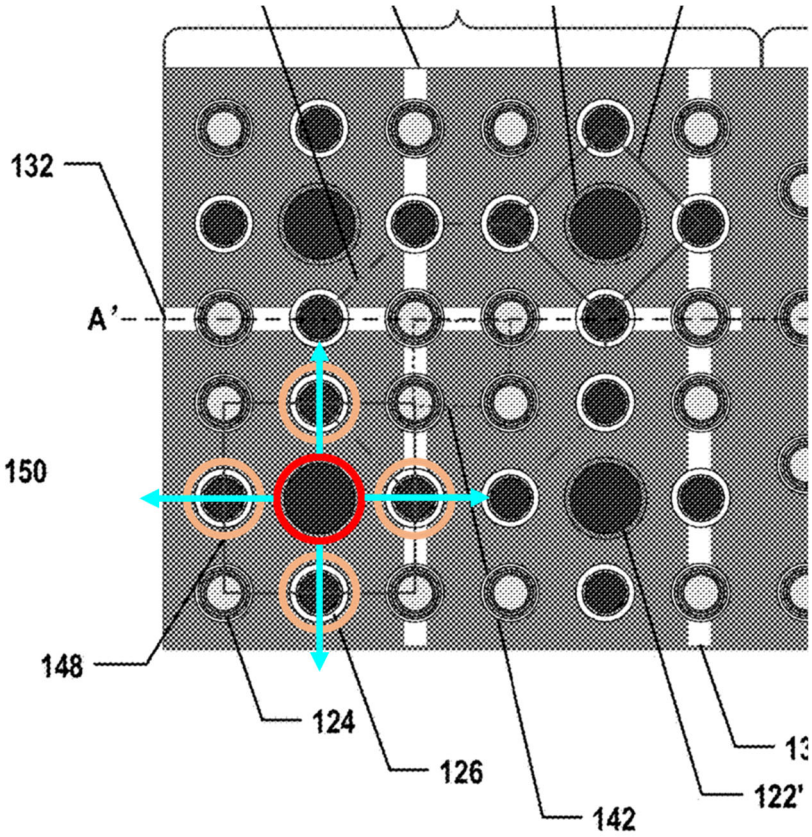
Id., Fig. 1A; Banerjee ¶¶ 84-89.

Indeed, even taking the case of four dummy source structures, these four structures do not come close to fully encircling the staircase contact. As shown below, there are large gaps between the dummy source structures (126), but those structures nonetheless "surround" the staircase contact (122).



Ex. 1001, Fig. 1A (partial) (annotated).

In this preferred embodiment, as shown below, "surrounded" includes being able to draw four lines outward from the staircase contact with each line being separated from the others by 90 degrees and intersecting a dummy source structure.



Id., Fig. 1A (annotated); Banerjee ¶¶ 90-91.

What's more, the specification makes clear that the number of a particular structure, e.g., dummy source structures, is not relevant to whether that structure "surrounds" another object. For example, the specification states that "[a]ny suitable number of dummy channel structures may be surrounded by any suitable number of dummy source structures." Ex. 1001, 7:40-43. In other words, there could be fewer, larger dummy source structures that surround the staircase contact, e.g., only two dummy source structures such that when drawing four lines outward from the staircase contact, those lines intersect the dummy source structure

Using "surrounding" to not require fully encircling is simply a common usage of the term. "An isthmus is a thin strip of land surrounded by water on two sides, which connects two larger landmasses." Ex. 1018 (https://www.studycountry.com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-sides.). The same is true in the context of 3D NAND. For example, two lateral elements on each side of a structure "surround" that structure. Ex. 1019 (U.S. Pat. No. 9,530,492), 2:14-16 ("In other words, the conventional SBPI operations are strongly affected by the stored Vts of two surrounding NAND cells dispersed in the adjacent left and right BLs."); Banerjee ¶ 92.

An express construction of this term is not necessary, because as demonstrated below, the Park prior art reference discloses (1) dummy source structures such that drawing four lines outward from the staircase contact with each line separated by 90 degrees (e.g., at 45, 135, 225, and 315 degrees) will result in each line intersecting a dummy source structure, and (2) dummy source structures that create a border with fewer gaps than shown above in Figure 1A of the '872 Patent. Banerjee ¶ 93. And in any event, as discussed above, "surround" is not even so limited, because the specification and claims make clear that other embodiments include fewer than four dummy source structures shown in the above figures.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

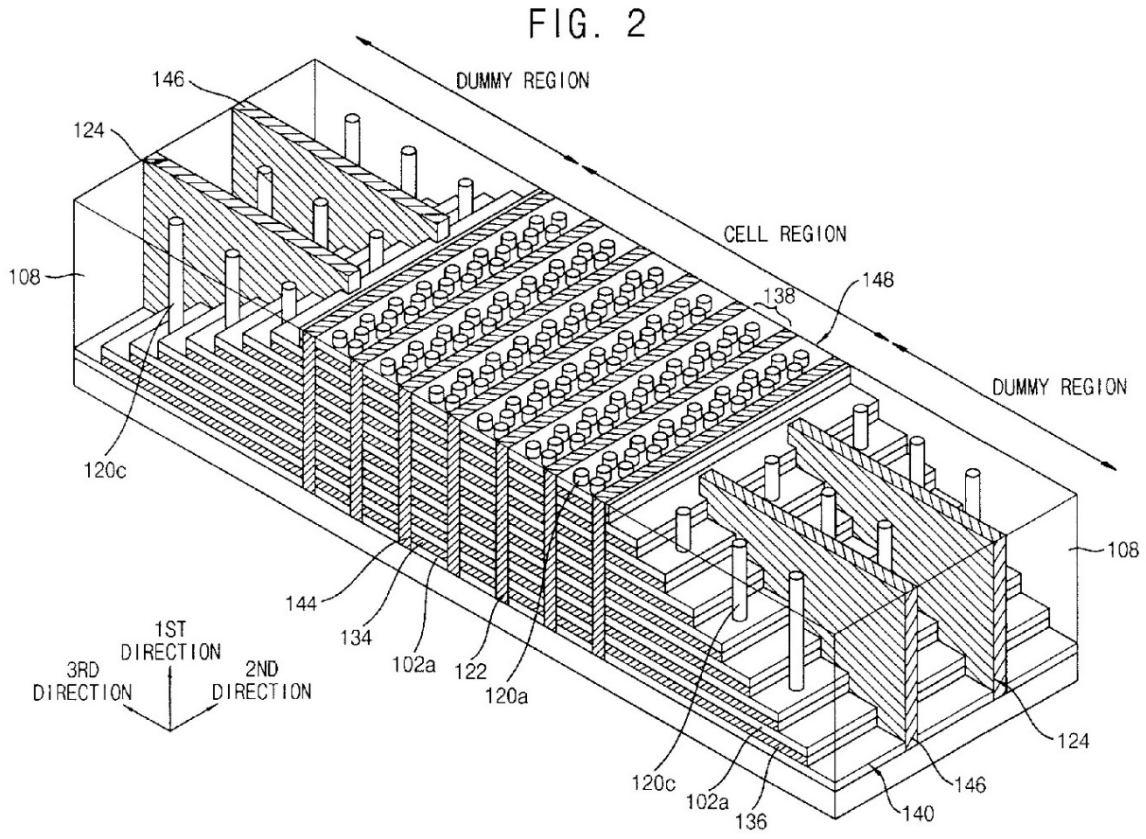
A POSITA in the field of the '872 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, how it is manufactured, and its component parts. *See* Banerjee, ¶¶ 40-43.

IX. DESCRIPTION OF THE PRIOR ART

A. Park

Park was filed on February 19, 2016, and is prior art under AIA §102(a)(2). Park, Cover. Park, like the '872 Patent, is directed to, and teaches the basic structural components of, a three-dimensional memory device and methods for making them. Those basic components include a substrate, interleaved conductive gate lines and insulating layers, and dummy components. *Id.*, 1:39-59. Park also teaches the use of common source lines 144 and dummy source lines 146 (i.e., dummy source structures) to "improve[] structural and electrical reliability" issues. *Id.*, 1:37-38.

Figure 2 below shows a portion[4] of Park's exemplary three-dimensional memory device.



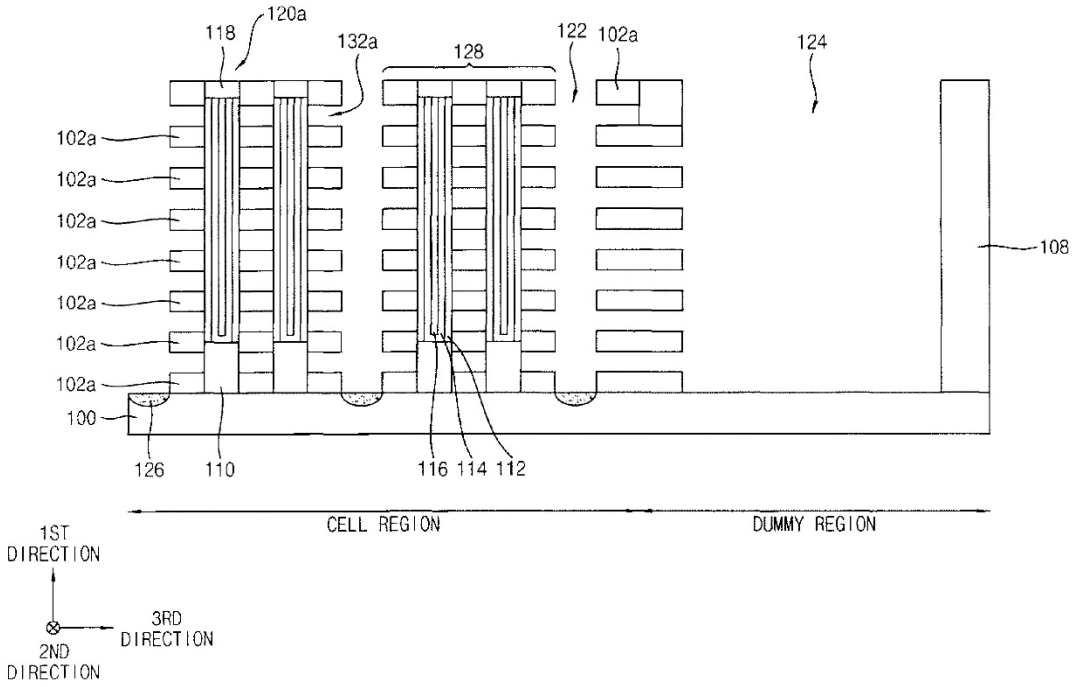
Id., Fig. 2.

Park teaches a method of forming a three-dimensional memory device, similar to the '872 Patent's method, in which an interleaved insulating and sacrificial layer stack is first formed on the substrate, the stack including a cell region and a stepped dummy region. Park, 9:36-46 (discussing Fig. 5). First and second openings (122, 124) are etched in the insulating/sacrificial layer stack during the gate replacement

[4] "FIG. 2 is an enlarged perspective view of a portion 'A' in FIG. 1." Park, 5:48-51.

process. *Id.*, 11:66-12:4. The first opening 122 is formed in the cell region and the second opening 124 is formed in the dummy region.

FIG. 9



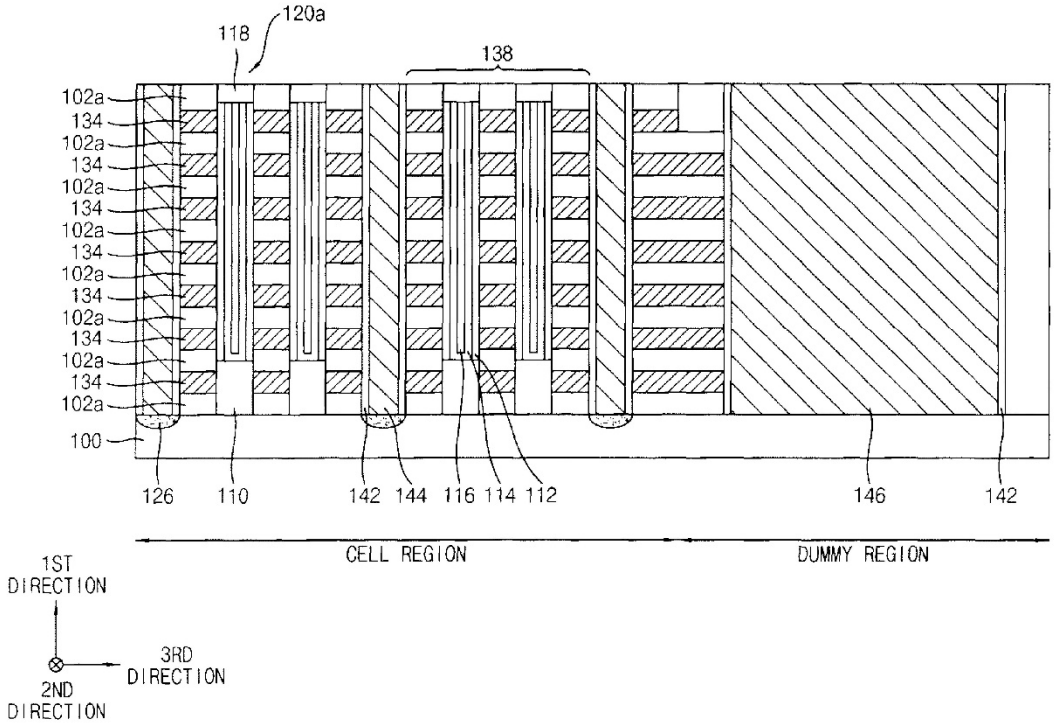
Id., Fig. 9.

The first and second openings (122, 124) are just like the '872 Patent's dummy source holes. Banerjee, ¶¶ 101-02. Specifically, these openings allow for the etching and deposition steps that replace the sacrificial gates. Park, 12:44-13:13.

After the gate replacement process, an insulation layer is formed on the sidewalls of the first and second openings (122, 124), and a conductive layer fills the rest of the opening to form a common source line and dummy source line (144 and 146, respectively). Park, 7:63-64 ("The CSL 144 may be in the first opening

122…"); 13:42-59; 14:67-15:2 ("The dummy source line 146a may be disposed in the second opening 124a…").

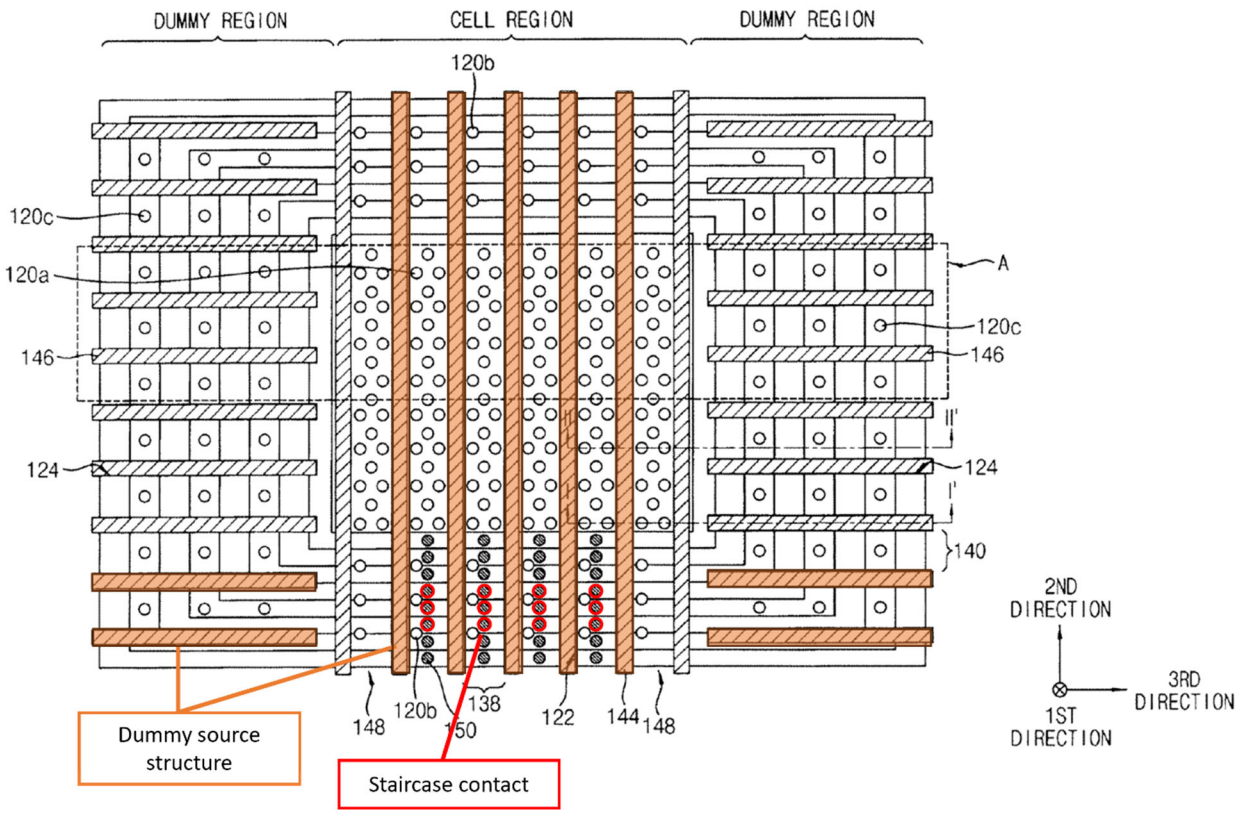
FIG. 13



Id., Fig. 13.

As shown below, the common source lines 144 (shown in orange in the first figure) and dummy source lines 146 (shown in orange in the second figure) surround the staircase contacts:

FIG. 1

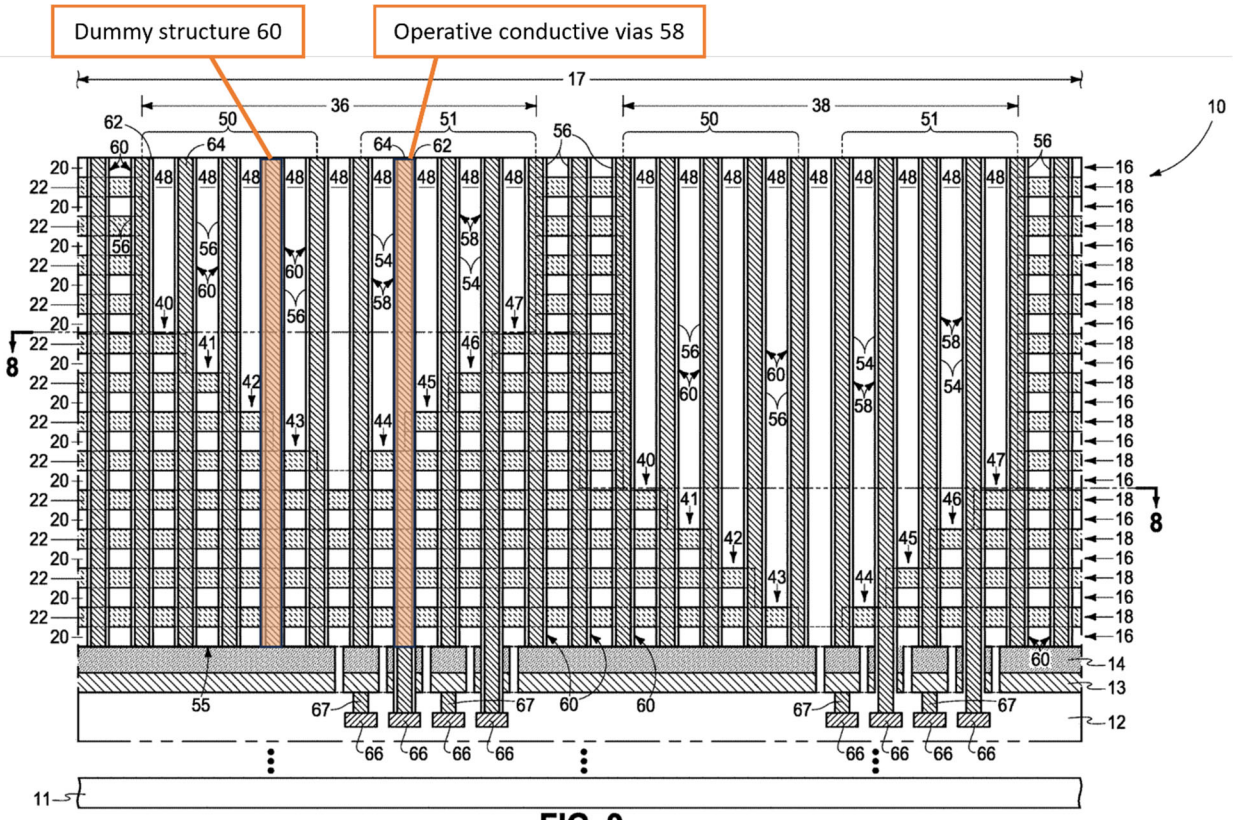


Id., Fig. 1 (annotated); Banerjee ¶¶ 97-104.

B. Tessariol

Tessariol is a U.S. Patent Application Publication that was published on March 14, 2019, and filed on September 14, 2017. Tessariol, Cover. Tessariol is prior art under AIA §102(a)(2). Tessariol, like the '872 Patent, is directed to, and teaches the basic structural components of, a three-dimensional memory device and methods for making them. Those basic components include a substrate, interleaved conductive gate lines and insulating layers, and dummy components. *Id.*, [0027]-[0031], [0041].

Tessariol discloses dummy structures 60 and operative conductive vias 58 that function as support structures for the memory stack during the gate replacement process. Tessariol, [0027]-[0031], [0041]. Tessariol explains that the dummy structures 60 and operative conductive vias 58 include "an insulative lining 62 (e.g., silicon dioxide and/or silicon nitride) and a conductive core 64 (e.g., metal material)." *Id.*, [0038]. The dummy structures 60 and operative conductive vias 58 are formed in dummy structure openings 56 and via openings 54 respectively, which extend through a memory stack comprised of insulating and conductive materials. *Id.*, [0037]-[0038].



Id., Fig. 9.

The dummy structure openings 56 and via openings 54 may be formed simultaneously, and the respective dummy structures 60 and operative conductive vias 58 may also be formed simultaneously. Tessariol, [0037]-[0038]. Further, the dummy structures 60 and operative conductive vias 58 surround the staircase contacts. The dummy structures 60 directly surround the staircase contacts as shown below.

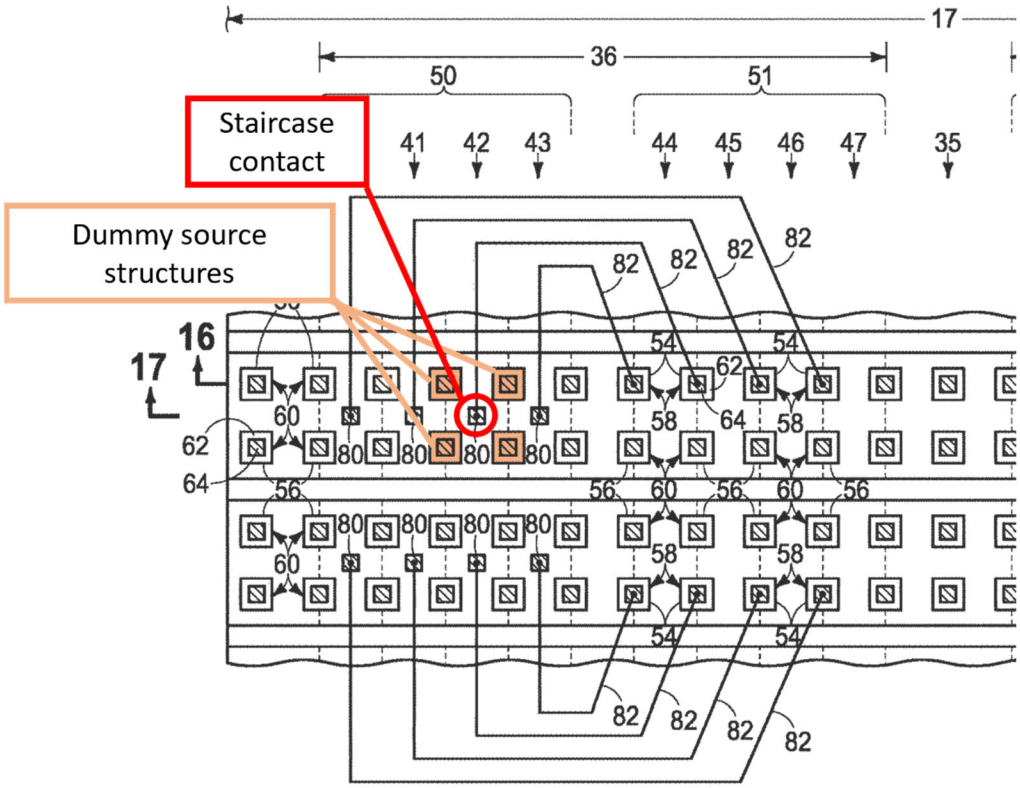


FIG. 15

Tessariol, Fig. 15 (partial) (annotated); Banerjee ¶¶ 105-09.

X. GROUND 1: CLAIMS 1-6, 11, AND 13 ARE OBVIOUS OVER PARK

Park (Ex. 1005), when considered in view of the knowledge of a POSITA, renders claims 1-6, 11, and 13 obvious. Banerjee ¶ 110.

A. Claim 1:

The figures from Park that are discussed below illustrate different views of a three-dimensional semiconductor device, and the manufacturing stages of the device. Figures 1-4 show different views (top plan view, perspective view, and cross-sectional views) of a three-dimensional semiconductor device, in which memory cells are formed on the top surface of a substrate. Park, 5:46-51. Figures 5-13 show the various manufacturing stages involved in forming the semiconductor device depicted by Figures 1-4. *Id.*, 9:29-37; Banerjee ¶ 111.

1. [1.PRE] "A three-dimensional (3D) memory device, comprising:"

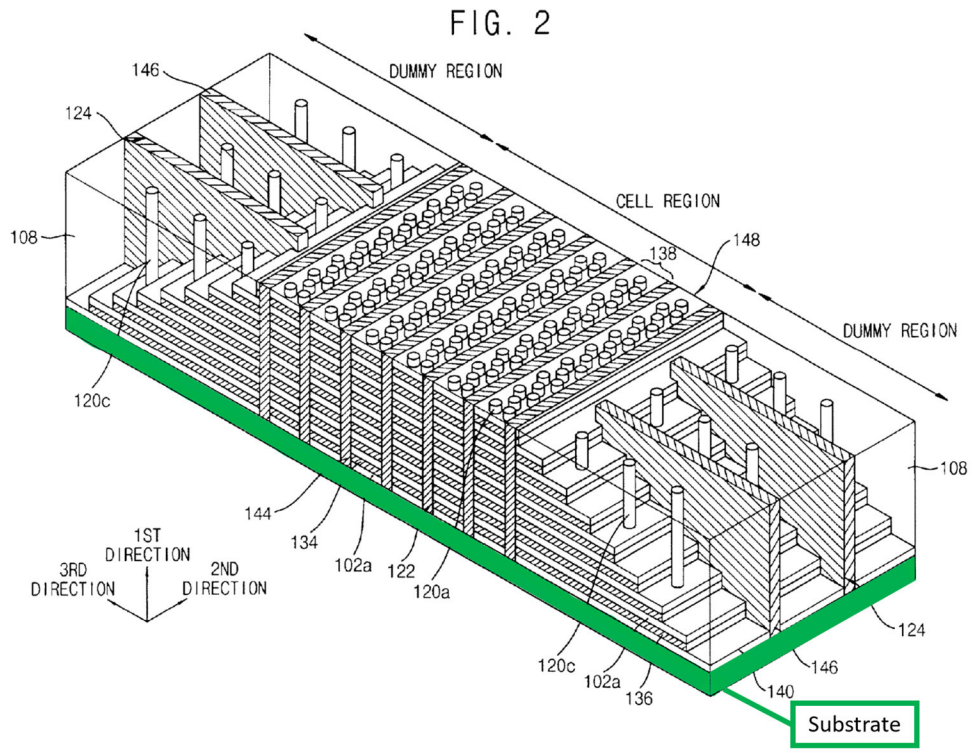
To the extent the preamble is limiting, Park discloses it. Specifically, Park discloses "[a] semiconductor device includes a substrate including cell and dummy regions …" Park, Abstract. Park further discloses "[i]n example embodiments, a nonvolatile memory may be embodied to include a three dimensional (3D) memory array." *Id.*, 23:13-22.

Thus, Park discloses *a three-dimensional (3D) memory device*[5] (e.g., 3D semiconductor device with cell region). Banerjee ¶¶ 112-14.

2. [1.A] "a substrate;"

Park discloses this limitation. Specifically, Park discloses that "a semiconductor device may include a memory cell structure disposed on a cell region of a substrate 100." Park, 6:1-4; *see also id.*, 23:15-22 ("[t]he 3D memory array may be monolithically formed on a substrate (e.g., semiconductor substrate such as silicon, or semiconductor-on-insulator substrate)."). This substrate is annotated in green below.

[5] This Petition uses red and italics for claim language in the claim mapping portion for convenience of the Board.



Id., Fig. 2 (annotated), *see also* Fig. 3 (showing a cross-section view of Fig. 2 and depicting a "substrate 100"); Banerjee ¶¶ 115-17.

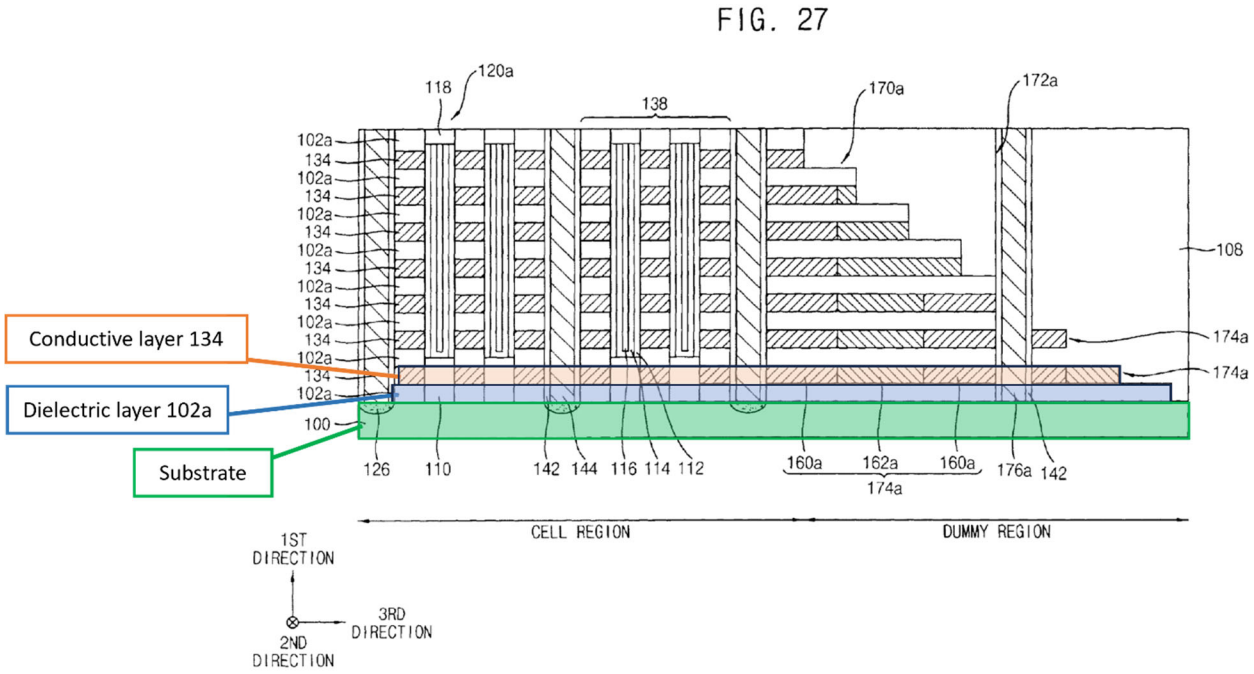
Thus, Park discloses a *substrate* (e.g., substrate 100).

3. [1.B] "a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;"

Park discloses this limitation.

First, Park discloses conductive gate lines 134 that may include a metal, such as "tungsten (W), tungsten nitride, titanium (Ti), titanium nitride, tantalum (Ta), tantalum nitride, platinum (Pt), or the like." Park, 7:6-10. Second, Park discloses that insulating interlayer patterns 102a are formed on the substrate 100, and act as an insulating layer between the gate lines 134, where the insulating layer 102a may

be "a silicon oxide-based material." *Id.*, 7:19-22. Silicon oxide is a known dielectric. Banerjee ¶ 120. Third, Park discloses that these gate lines 134 (i.e., conductive layers) and insulating interlayer pattern 102a (i.e., dielectric layers) are alternately stacked or interleaved on the substrate. Park, 7:23-31 ("The insulating interlayer patterns 102a and the gate lines 134 may be alternately stacked…"). This memory stack is in the "cell region":



Id., Fig. 3; Banerjee ¶¶ 118-22.

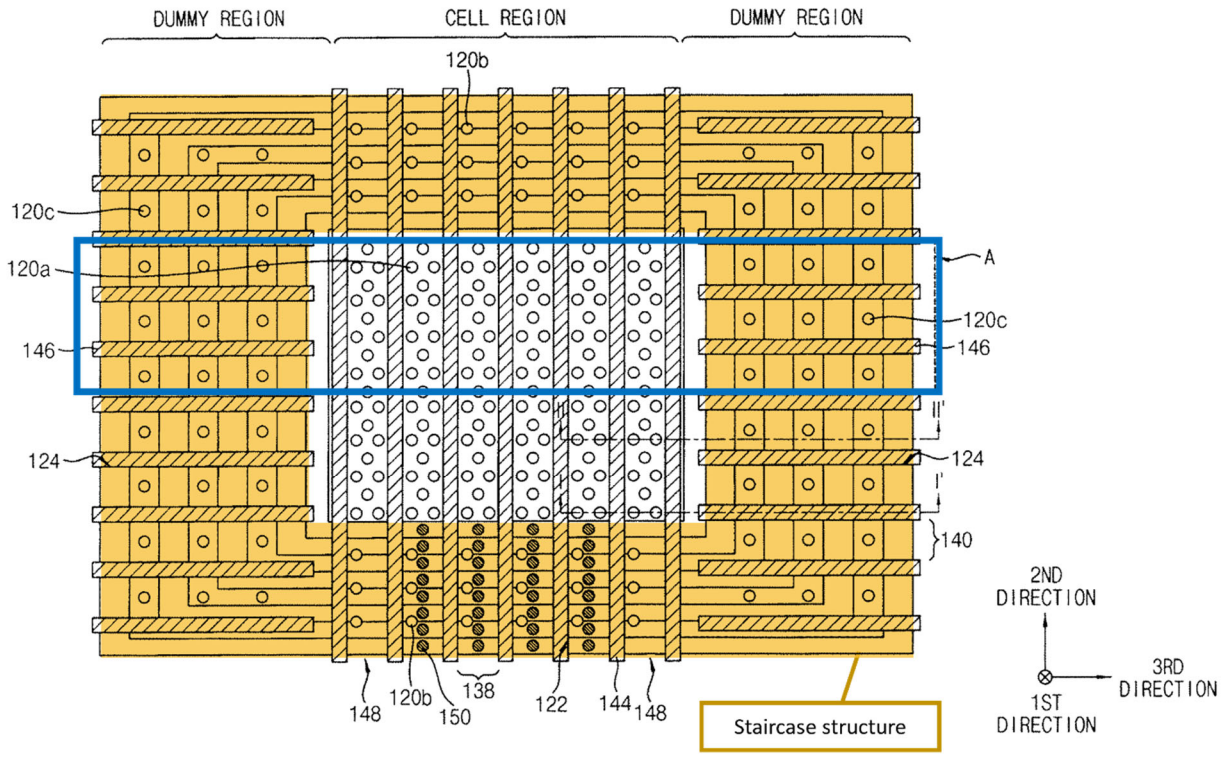
Thus, Park discloses *a memory stack comprising interleaved conductive layers and dielectric layers on the substrate* (e.g., in the cell region, layers 102a and 134, which is a stack on substrate 100).

4. [1.C] "a staircase structure on one side of the memory stack;"

Park discloses this limitation.

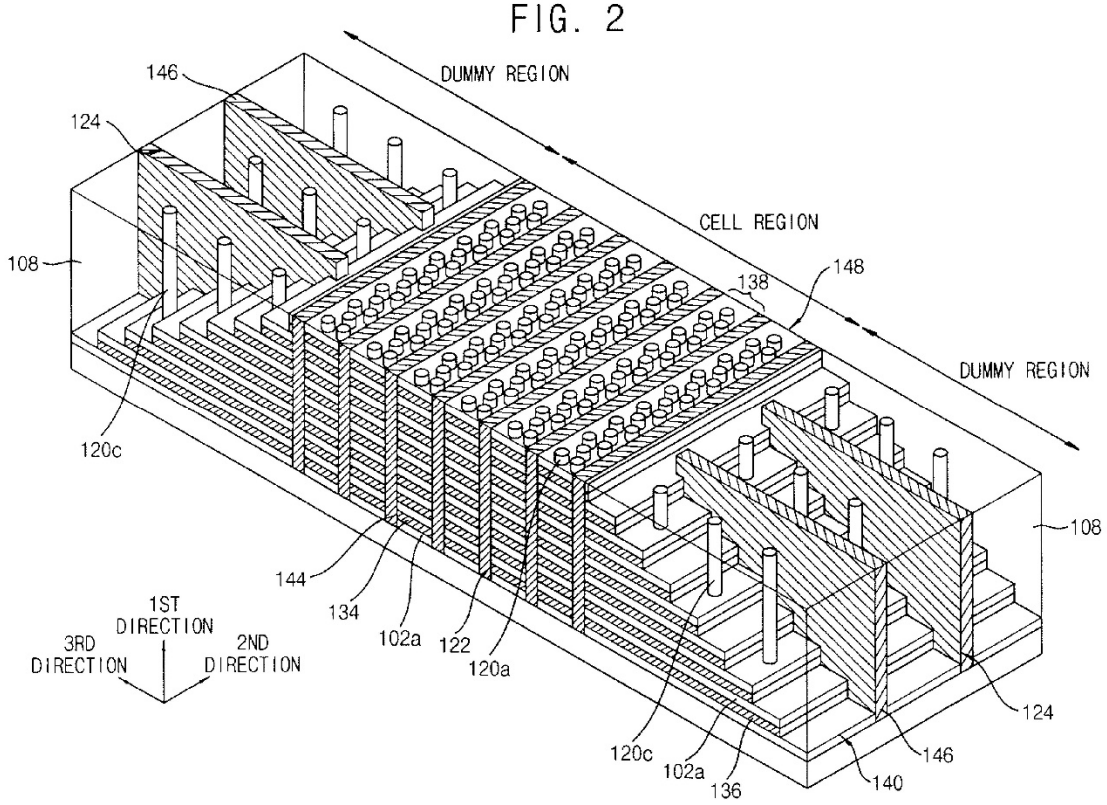
As shown in limitation [1.B], Park discloses an interleaved stack of conductor/dielectric layer pairs in the cell region. For context, the complete view of Park's device is shown in Figure 1 below:

FIG. 1



Park, Fig. 1 (annotated). Park also discloses a cross section of area A of Figure 1 (shown above in the blue box) in Figure 2:

FIG. 2



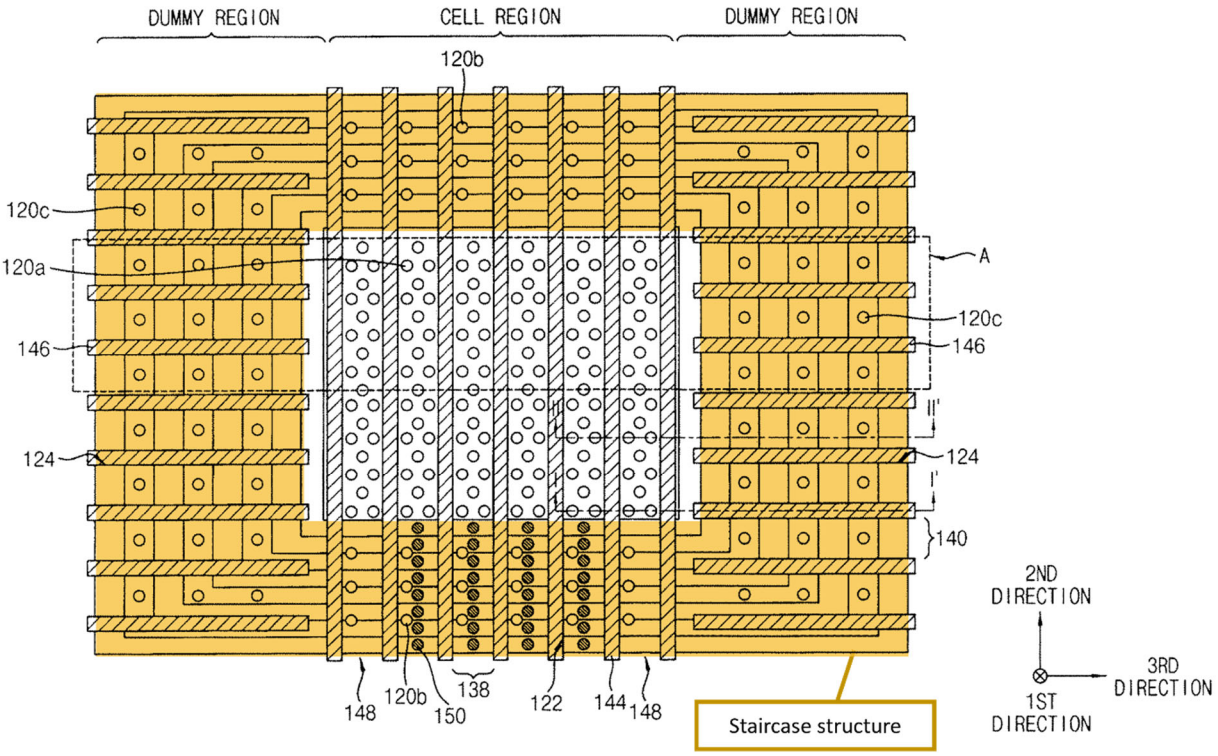
Id., Fig. 2, *id.*, 5:48-50 (stating Figure 2 shows area A of Figure 1).

As can be seen in the above figures, Figure 2 does not depict the regions with respect to the second direction, above and below the uncolored cell region in Figure 1. Park makes clear, however, that the stairstep region is the entire orange-colored region in Figure 1 above and the "main cell region" is in the uncolored portion of Figure 1 above, which includes the active channel structures. Park, Fig. 2, 7:25-27, 9:43-46. First, in discussing the manufacturing of the stack, Park refers to the stack as "first structure 138." *Id.*, 7:23-31. Park explains: "[t]he first structure 138 may extend in the second direction. Both lateral portions of the first structure 138 in the second direction may serve as a wiring region and have a stepped shape." *Id.*, 7:25-

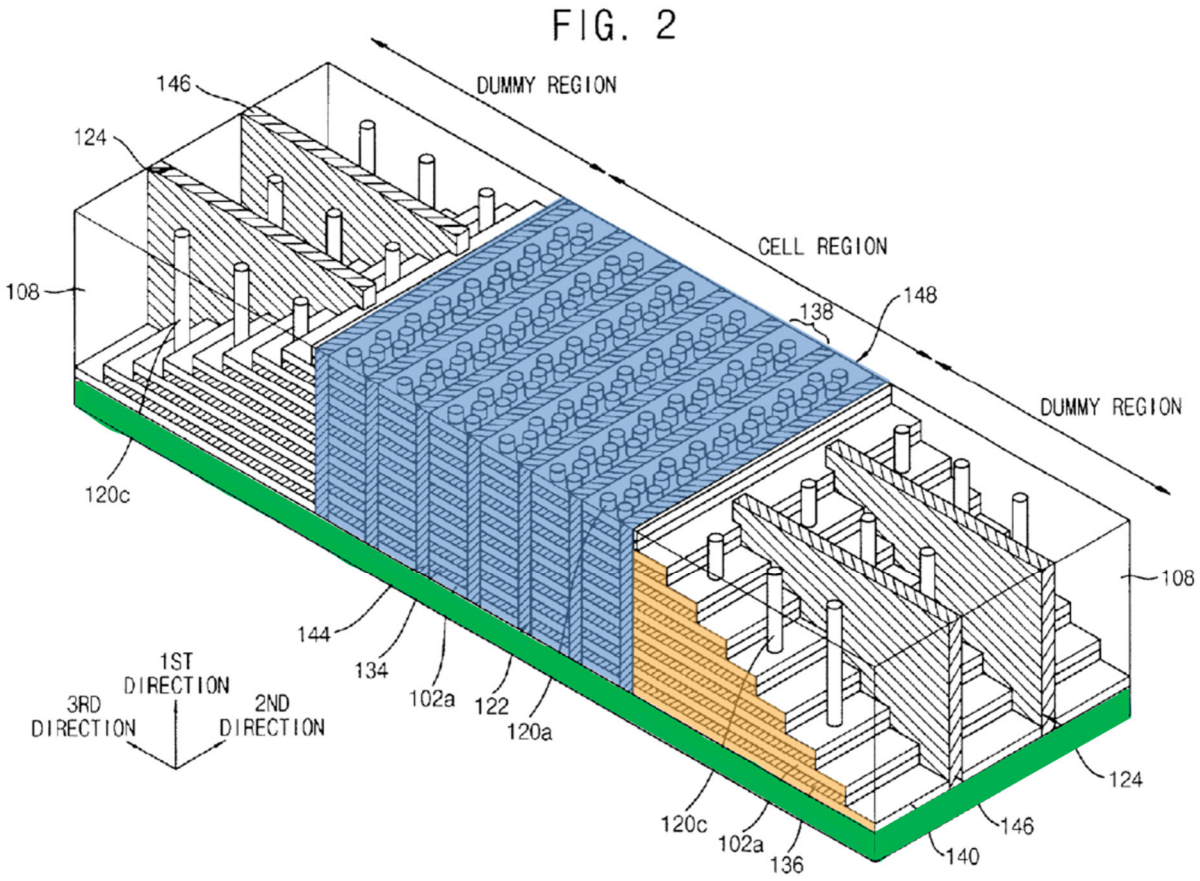
27. Further, "[a] central portion of the first structure 138 which may not have the stepped shape may serve as a main cell region, and the lateral portion having the stepped shape may serve as the wiring region." *Id.*, 7:32-35. Second, in discussing the manufacturing of the stack, Park refers to the resulting structure after the gate replacement process as the "mold structure 106." *Id.*, 9:38-46. Park explains that "[e]nd portion of the mold structure 106 in the second and third directions may have stepped structures." *Id.*, 9:43-46. And Park explains again "[a] portion of the mold structure 106 on the cell region may include stepped structures at both end portions in the second direction." *Id.*, 10:7-10. Third, as the analysis under limitation [1.D] demonstrates, the word line contacts, which extend down to steps of a staircase structure, are in the second direction of the main cell area. *Id.*, 7:32-37. Word line contacts extend to steps in a staircase region.

Accordingly, annotated Figure 1 below marks in orange all portions of the memory stack with a stepped shape – the lateral portions in the second direction and the dummy region in the third direction. Banerjee ¶¶ 124-30.

FIG. 1



Annotated Figure 2 below shows a perspective view of an exemplary "stepped structure" in the third direction, but as discussed above, such stepped structure exists in the second direction of the main cell (a portion of which is shown in blue below) region as well. Park, 5:48-49; Banerjee ¶¶ 131-32.



Id., Fig. 2 (annotated).

Thus, Park discloses *a staircase structure on one side of the memory stack* (e.g., the stepped regions on each side of the main cell region).

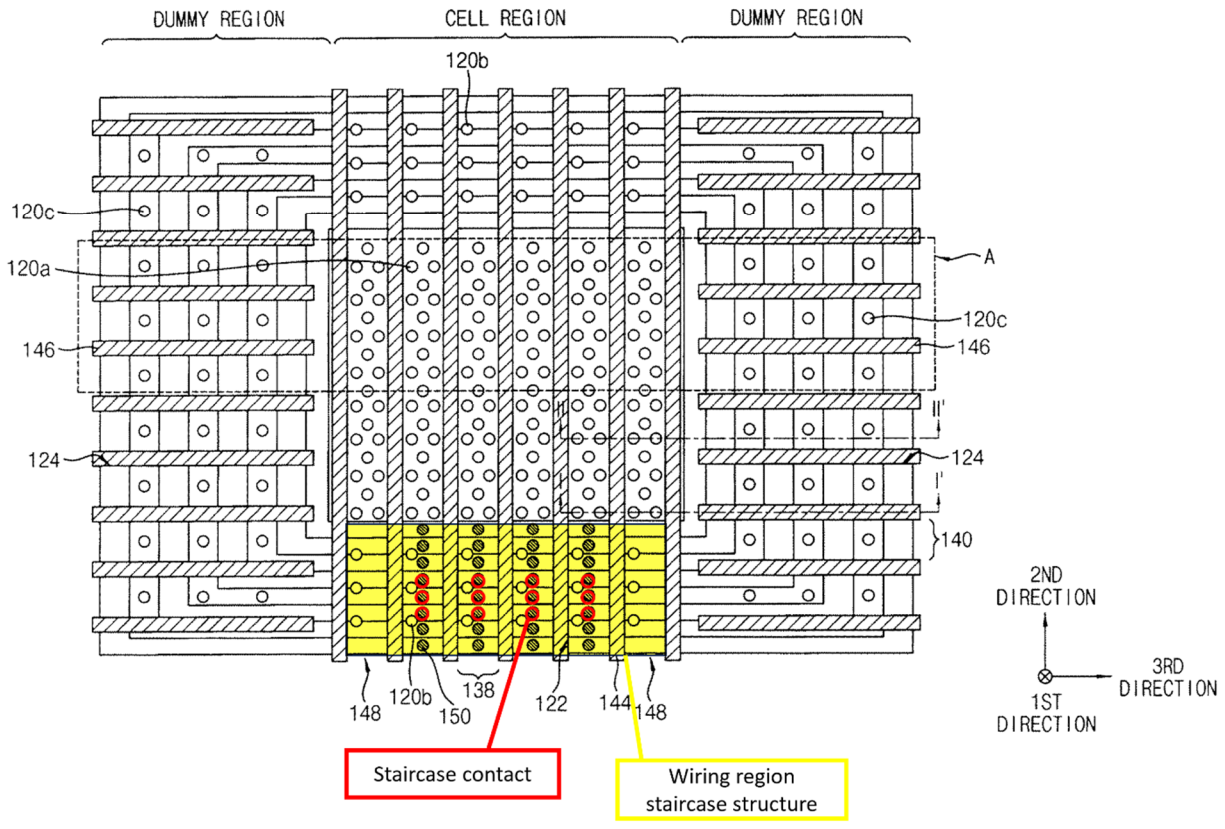
5. [1.D] "a staircase contact in the staircase structure; and"

Park discloses this limitation or at least renders it obvious.

As discussed in limitation [1.C], Park discloses a "staircase structure" in the second direction to the main cell region (as shown in yellow below, in the second direction with respect to figure 2), i.e., the wiring region. Park, 7:33-35. Park also discloses that, within the wiring region, there are interconnects to individual gate

lines: "[T]he lateral portion having the stepped shape may serve as the wiring region. The **wirings may include contact plugs 150 that may be in contact with gate lines 134**, and conductive lines electrically connected to the contact plugs 150." *Id.*, 7:32-37 (emphasis added). In other words, in the staircase structure, there are *staircase contacts* (contact plugs 150) that extend and contact the individual steps of the staircase structure, thereby providing a connection to each gate line. Banerjee ¶¶ 134-35. Annotated Figure 1 below illustrates the contact plug 150 (in red) and the wiring region (in yellow).

FIG. 1



Park, Fig. 1, Banerjee ¶¶ 133-35.

To the extent that PO argues that Park does not disclose a staircase region in the main wiring area, it would have at least been obvious to have one. First, Section X.A.4 illustrates that Park describes the wiring area under the main cell region as having a staircase region. Second, Park describes contacts to the gate lines in this region. A POSITA knew that the region that includes contacts to the gate lines is a staircase region. *See* Section V. The staircase region beneficially provides landing pads for the gate line contacts. *Id.* And implementing such staircase regions, as Park shows in Figure 2, was routine. *Id.*; Banerjee ¶¶ 136-37.

Thus, Park discloses, or renders obvious, *a staircase contact* (e.g., contact plug 150) *in the staircase structure* (e.g., step structure in wiring area).

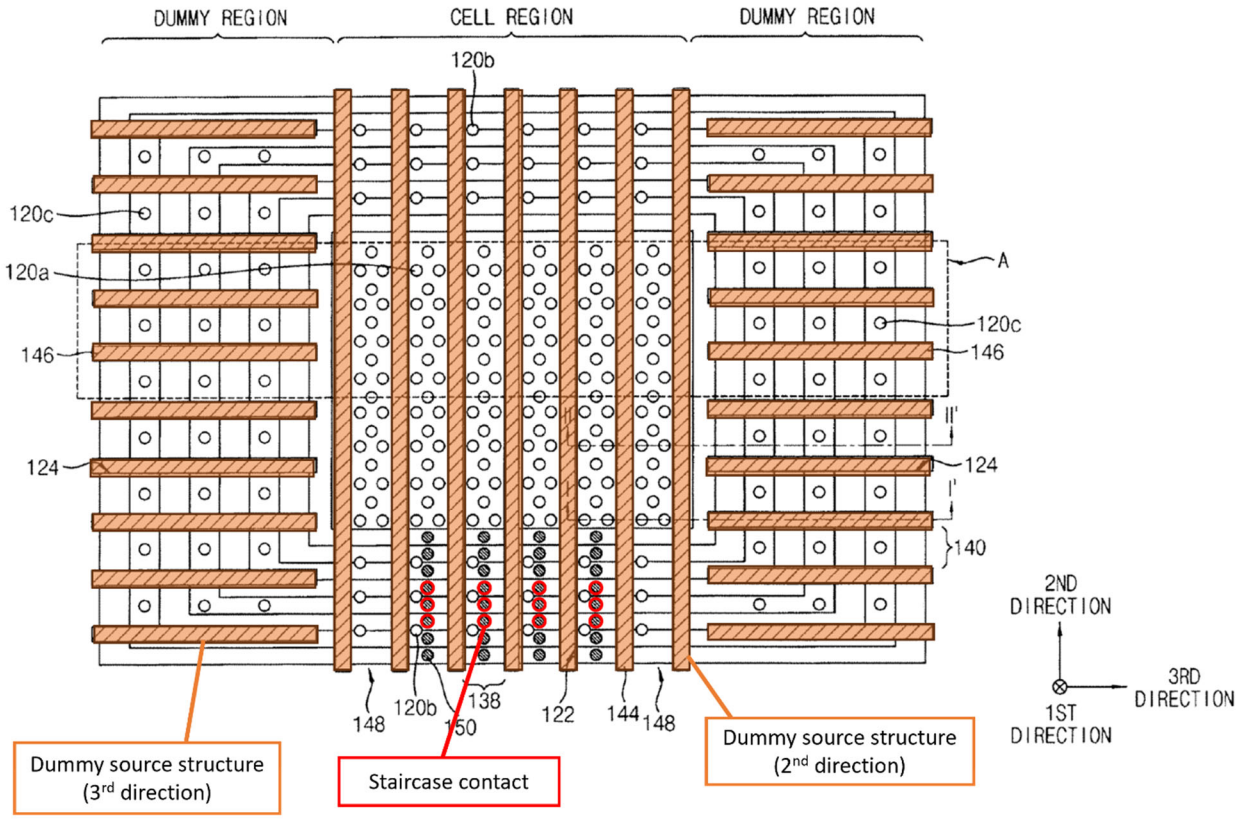
6. [1.E] "a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact,"

Park discloses this limitation under both parties' constructions. Recall that Petitioner's construction is "structure that occupies the void that was used for the gate replacement process" and PO's apparent interpretation does not require that the structure occupy the void that is used for the gate replacement process. *See* Section VII.A.

First, as to *a plurality of dummy source structures*, Park discloses common source lines 144 and dummy source lines 146, which are "structures that occupy the void that was used for the gate replacement process." *See* VII.A. Annotated Figure

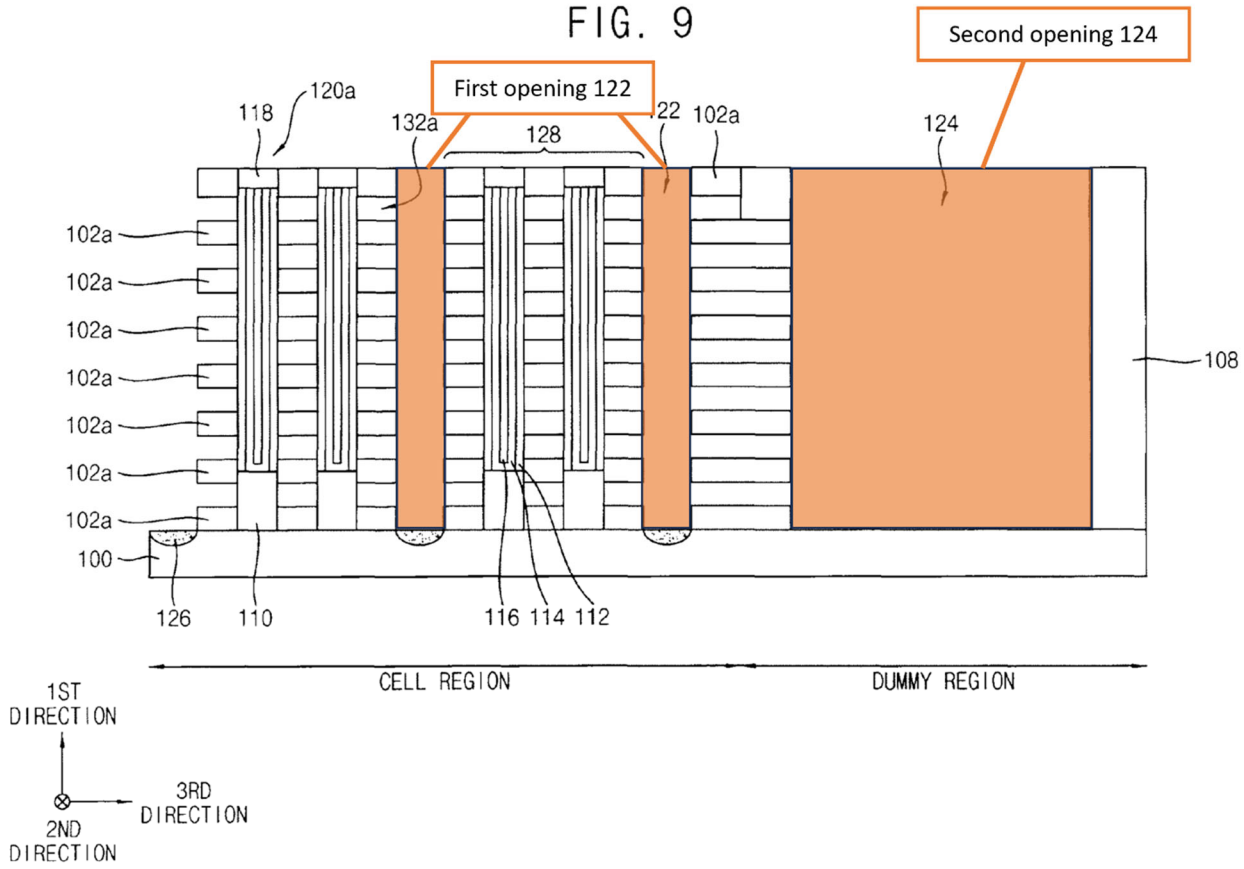
1 below shows, in orange, the position of the common source lines 144 and dummy source lines 146.

FIG. 1



Park, Fig. 1 (annotated).

During the gate replacement process, first openings 122 and second openings 124 are etched in the insulating/sacrificial layer stack. Park, 11:66-12:4, Fig. 9. Annotated Figure 9 below shows the first openings 122 and second openings 124 after etching.

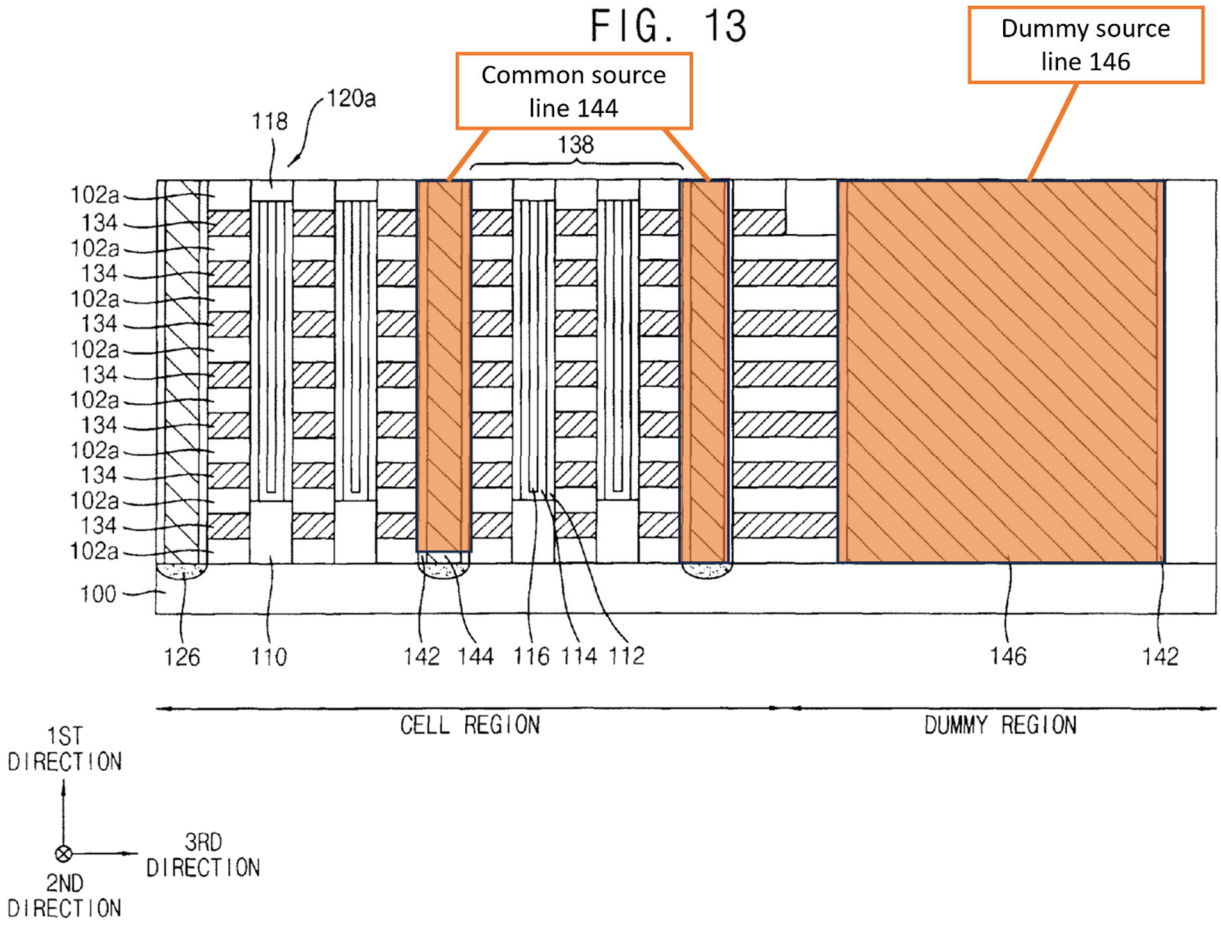


Id., Fig. 9 (annotated).

The first openings 122 and second openings 124 are the voids that are used for the gate replacement process. Specifically, the etch occurs through these voids: "[r]eferring to FIGS. 9 and 10, the sacrificial patterns 104a exposed through the first and second openings 122 and 124 may be removed to form first gaps 132a and second gaps 132b. In example embodiments, the sacrificial patterns 104a may be removed by a wet etching process using, e.g., phosphoric acid and/or sulfuric acid as an etchant solution. … Referring to FIGS. 11 and 12, gate lines 134 may be

formed in the first gaps 132a, and dummy patterns 136 may be formed in the second gaps 132b." Park, 12:44-13:5.

After the gate replacement process, the first opening 122 and the second opening 124 are each lined with an insulating layer and then filled with conductive material to form a common source line 144 and a dummy source line 146, respectively. Park, 13:39-41 ("The CSL 144 and the dummy source line 146 filling the first opening 122 and the second opening 124, respectively, may be formed"); *see also* 7:63-64 ("The CSL 144 may be in the first opening 122…"), 13:50-59 (same), 14:67-15:1 ("The dummy source line 146a may be disposed in the second opening 124a…"). Annotated Figure 13 below shows the filling of the first opening 122 and the second opening 124, in orange, with conductive material to form the common source line 144 and the dummy source line 146 (in orange).

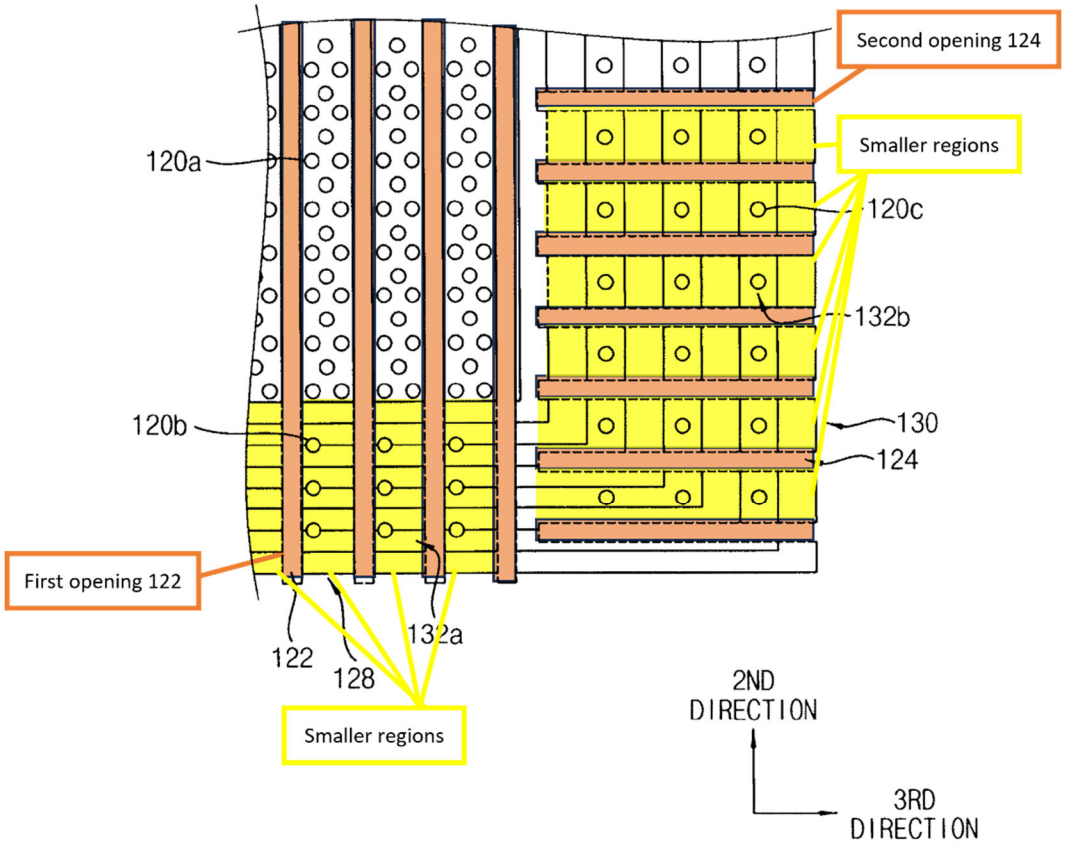


Id., Fig. 13 (annotated); Banerjee ¶¶ 138-44.

The '872 Patent describes almost identical *dummy source structures* to those of Park, i.e., Park's common source lines 144 and dummy source lines 146. Recall that the '872 Patent states that "dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks." Ex. 1001, 11:44-46. Park's common source lines 144 and dummy source lines 146 do the same. Specifically, these structures may "cut" the stack. Park, 12:5-18; *see also* 6:15-18 ("The CSL 144 may extend through the gate lines 134, and may extend in

the second direction. The CSL 144 may serve as a cutting line intersecting the gate lines 134"); Banerjee ¶ 145. Annotated Figure 10 below shows that the first openings 122 and second openings 124 divide the staircase structure into smaller regions.

FIG. 10

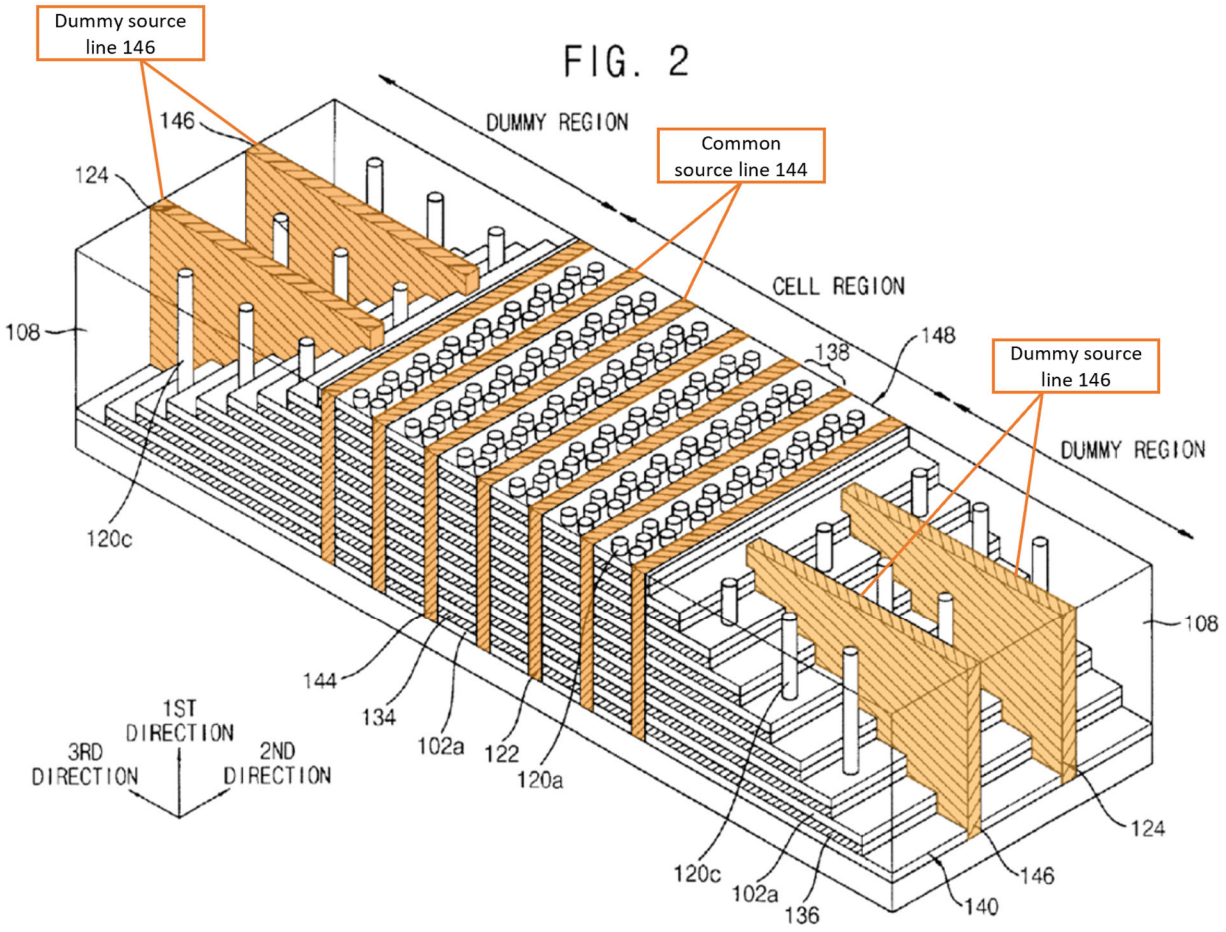


Park, Fig. 10 (annotated).

Further, recall that the '872 Patent explains that "dummy source structures" can "contact with the substrate and may provide interconnect between the 3D

memory device and peripheral devices." Ex. 1001, 5:41-43, 16:63-66. Similarly, the common source lines 144 in Park are an interconnect for a source connection. Park, 7:63-64 ("The CSL 144 may be in the first opening 122…"); Banerjee ¶ 146. And unlike the gate line slits that the '872 patent describes, which have an insulator material in them (Ex. 1001, 4:38-44), Park's common source lines 144 and dummy source lines 146 have a conductive core. *See* Section X.A.7.

Second, as to *each extending vertically through the staircase structure*, Park discloses that both the common source line 144 and dummy source line 146 extend vertically through the stepped region (i.e., "staircase structure"):



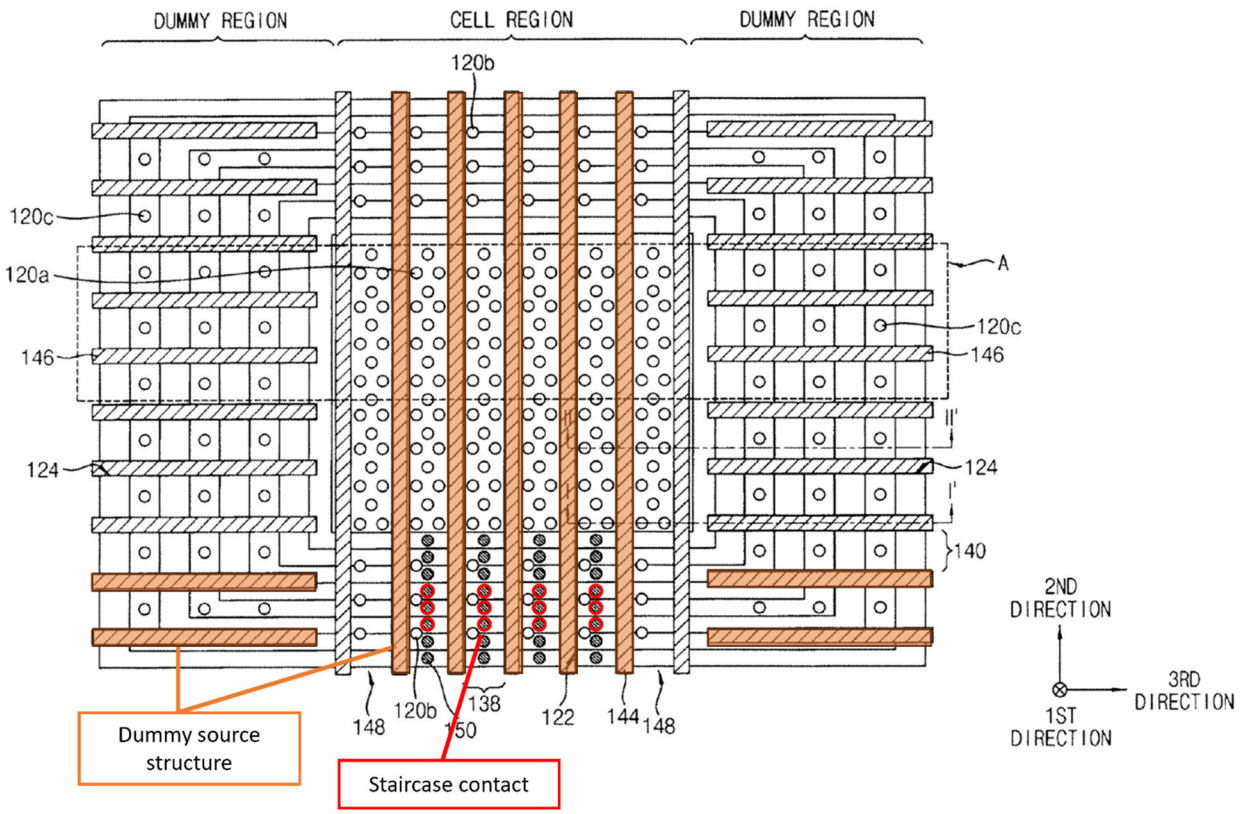
Park, Fig. 2 (annotated). All the embodiments in Park show common source lines 144 and dummy source lines 146 that extend vertically through the staircase structure. *See, e.g., id.*, Fig. 19, Fig. 21, and Fig. 26 (showing different embodiments of common source line 144 and dummy source line 146 configurations that all extend vertically through the staircase structure.). Specifically, these structures may "cut" the stack. Park, 12:5-18, *see also* 6:15-18; Banerjee ¶ 147.

Third, as to *the plurality of dummy source structures surrounding the staircase contact*, recall that the '872 Patent does not use "surround" to mean fully

and continuously encircling, because in all embodiments, the dummy source structures do not do so. *E.g.*, Ex. 1001, Fig. 1A (dummy source structures 124 do not fully surround word line contacts 122); *see also* Section VII.B. Instead, in every embodiment, there are large gaps between the dummy source structures.

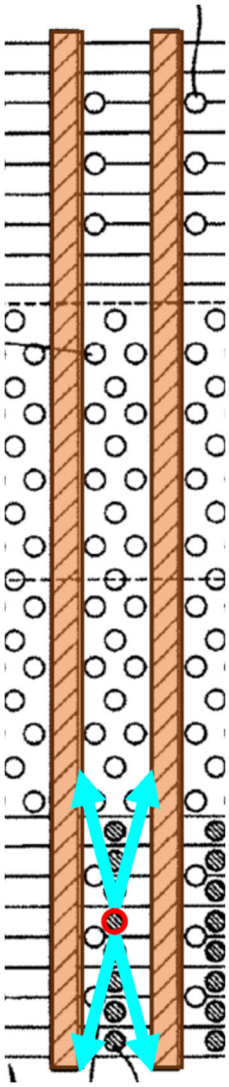
As discussed under limitation [1.D], Park discloses a *staircase contact* (contact plugs 150). *See* [1.D]. As shown in the two annotated versions of Figure 1 below, the common source line 144 and the dummy source line 146 (*dummy source structures*) both surround the contact plugs 150 (i.e., *staircase contacts*). These *dummy source structures surround* the staircase contacts. Indeed, the common source lines 144 *surround* the *staircase contacts* alone. Banerjee ¶ 149.

FIG. 1

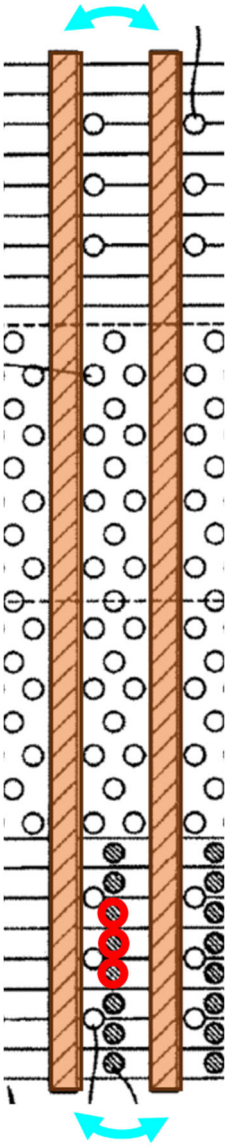


Park, Fig. 1.

Common source lines 144 alone surround the *staircase contacts*, and that is all that is necessary to satisfy claim 1. By way of example, two of the *dummy source structures surround* a *staircase contact* like the '872 Patent, namely, when drawing four lines (each equally radially spread out), each line will intersect one of the *dummy source structures*. *See* Section VII.A. As shown below, when drawing such lines from the *staircase contact* at 45, 135, 225, and 315 degrees (or from a different orientation, at 0, 90, 180, and 270 degrees), each line intersects a *dummy source structure*:



By way of another example, as shown below, two of the *dummy source structures* create a larger angular border around the *staircase contact* than the '872 Patent creates with four *dummy source structures*. *See* Section VII.A; Banerjee ¶¶ 149-52.



Were PO to argue that Park only discloses dummy source structures on two sides (which would be inaccurate, because in the above figure a line from the contact intersects a dummy source structure at four different angles separated by 90 degrees (e.g., 45, 135, and 225, and 315 degrees), the argument fails because an object may be surrounded by structures on two sides, just like an isthmus is surrounded on two

sides by water or like a nitride layer is surrounded on two sides by oxide layers in an ONO dielectric structure. Banerjee ¶¶ 153-54.

Thus, Park discloses *a plurality of dummy source structures* (e.g., common source lines 144 and dummy source lines 146) *each extending vertically through the staircase structure* (e.g., through the stairstep regions), *the plurality of dummy source structures surrounding the staircase contact* (e.g., contact plugs 150).

7. [1.F] "wherein each of the dummy source structures comprises a conductive contact."

Park discloses this limitation.

As an initial matter, the '872 Patent provides as an example of a *contact* a uniform vertical conductive member that extends down towards the substrate, *i.e.*, *contact* need not be a separate element on top of a conductive member. The '872 Patent recites that "[a]s illustrated in FIG. 2L, ***a contact 244*** is formed within spacer 242 in dummy source hole 212 (shown in FIG. 2K). ***Contact 244*** can be formed by depositing conductive materials including, not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof, over spacer 242 in the dummy source hole using one or more thin film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof. ***A dummy source structure 246 including spacer 242 and contact 244*** is thereby formed in the dummy source hole, surrounded by a plurality of dummy channel structures 209." Ex. 1001, 16:21-

32 (emphasis added). As shown below, the "contact" is simply a fill of conductive metal (246) into a hole (212) with an insulating liner (242):

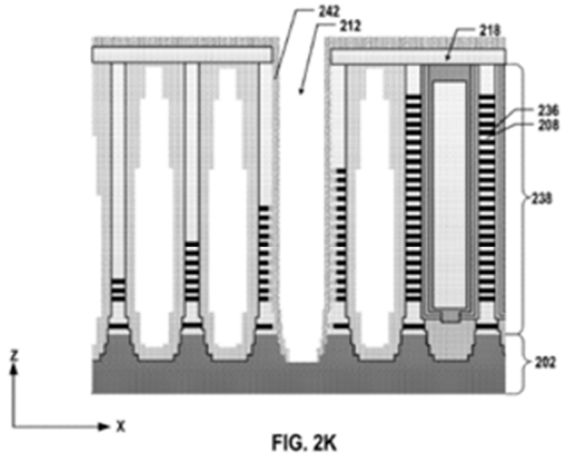


FIG. 2K

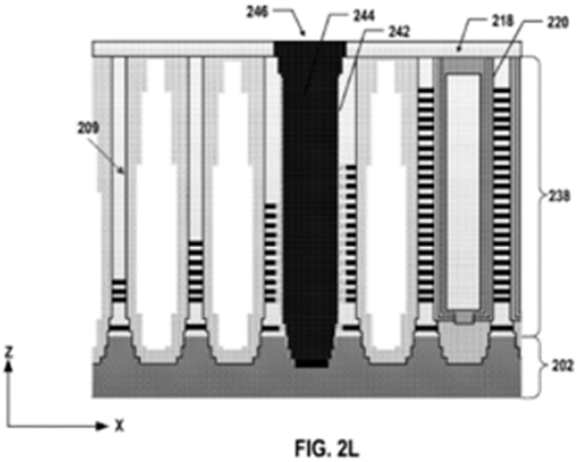


FIG. 2L

Id., Figs. 2K, 2L; Banerjee ¶ 156.

In Park, each of common source line 144 and dummy source line 146, i.e., "dummy source structures") comprises *a conductive contact*, namely, each includes conductive core that extend through the stack. *See* Park, 1:63-65 ("In example embodiments, the dummy lines may include a conductive material the same as that included in the cutting lines."); 7:65-67 ("The CSL 144 may include a metal having a low resistance, e.g., W, Ti, Ta, Pt, etc…"); 3:23-24 ("The dummy source lines and the common source lines may include a same conductive material."). *See also* Limitation [1.E] (describing the common source line 144 and dummy source line 146 "cut" through the stack); Banerjee ¶¶ 157-58.

Thus, Park discloses *wherein each of the dummy source structures comprises a conductive contact* (e.g., a metal or other conductive material).

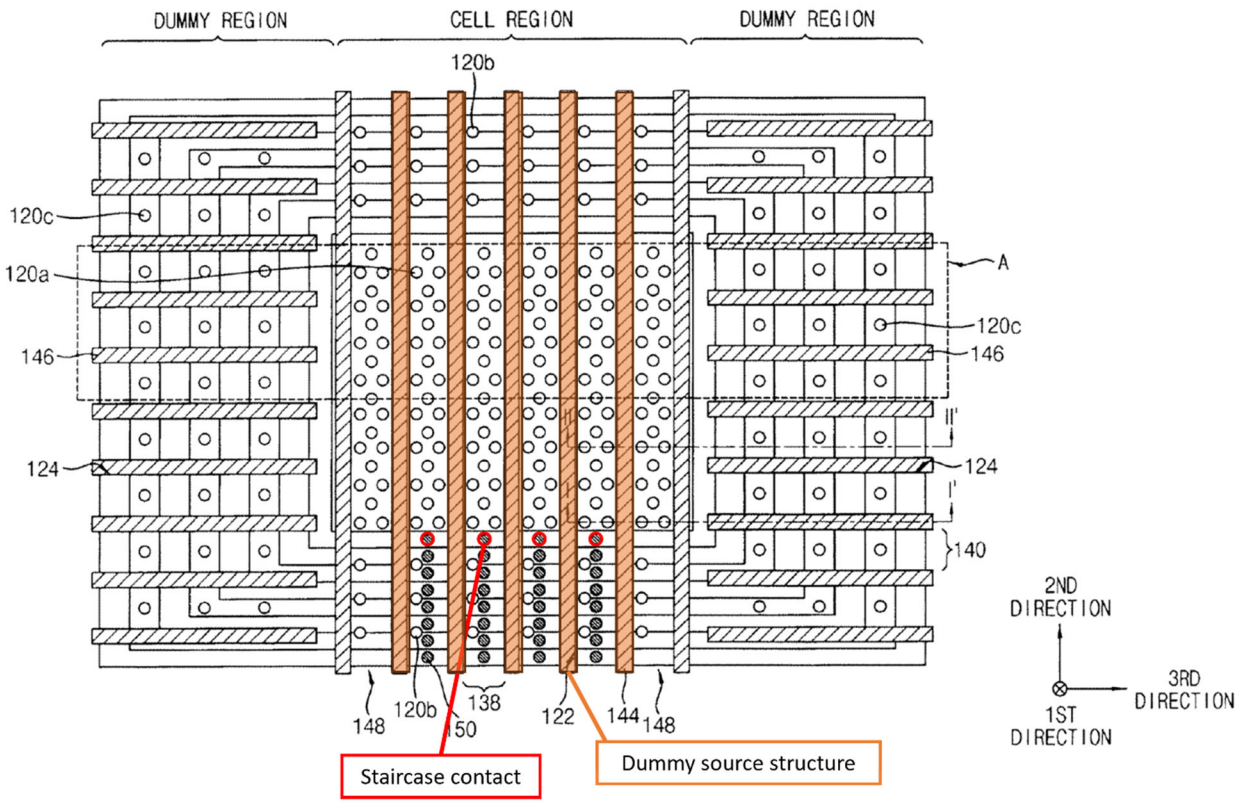
B. CLAIM 2

1. [2] "The 3D memory device of claim 1, wherein the plurality of dummy source structures are located adjacent to the staircase contact."

Park discloses this limitation.

As discussed in [1.E], Park discloses both dummy source lines 146 and common source lines 144 as *dummy source structures*. For this claim mapping, the *dummy source structures* are the plurality of common source lines 144 and the *staircase contacts* is the top row (in the second direction), and the *dummy source structures* surround the *staircase contacts* (*see* limitation [1.E]). Annotated Figure 1 below shows the plurality of common source line 146 (in orange) that are located adjacent to the contact plugs 150 (i.e., *staircase contacts*) (shown in red).

FIG. 1



Park (annotated), Fig. 1; Banerjee ¶¶ 159-60.

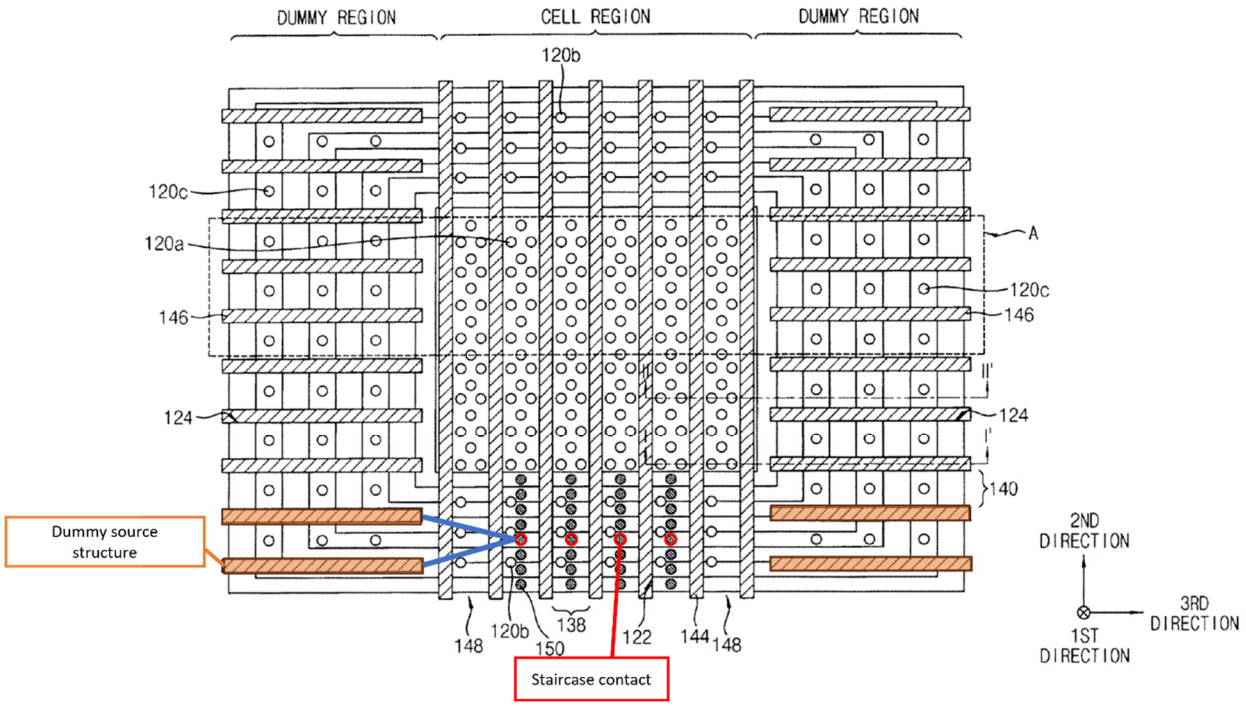
C. Claim 3:

1. [3] "The 3D memory device of claim 1, wherein at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact."

Park discloses "at least two of the plurality of dummy source lines are of nominally equal lateral distances to the staircase contact." Annotated Figure 1 below shows the dummy source lines 146 are positioned nominally equal lateral distances to the contact plugs 150 (i.e., staircase contact). The blue lines indicate that the

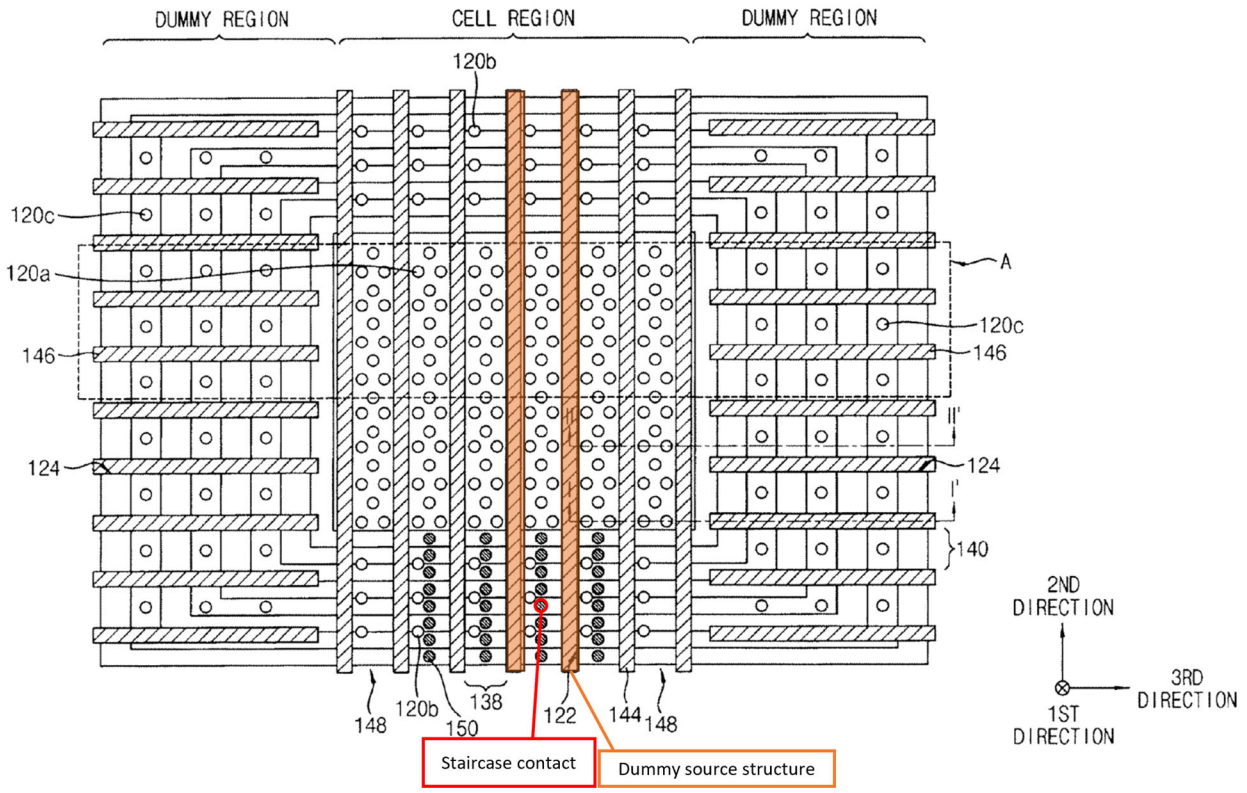
dummy source lines are "evenly or uniformly distributed" (i.e., nominally equal lateral distances) from the middle contact plugs 150 (in red). Ex. 1001, 6:48-50.

FIG. 1



Park (annotated), Fig. 1. Similarly, two of the common source lines (which may be the *plurality of dummy source structures*) are *of nominally equal lateral distances to the staircase contact*, e.g., two that surround one contact (here, *the staircase contact*). Banerjee ¶¶ 161-62.

FIG. 1



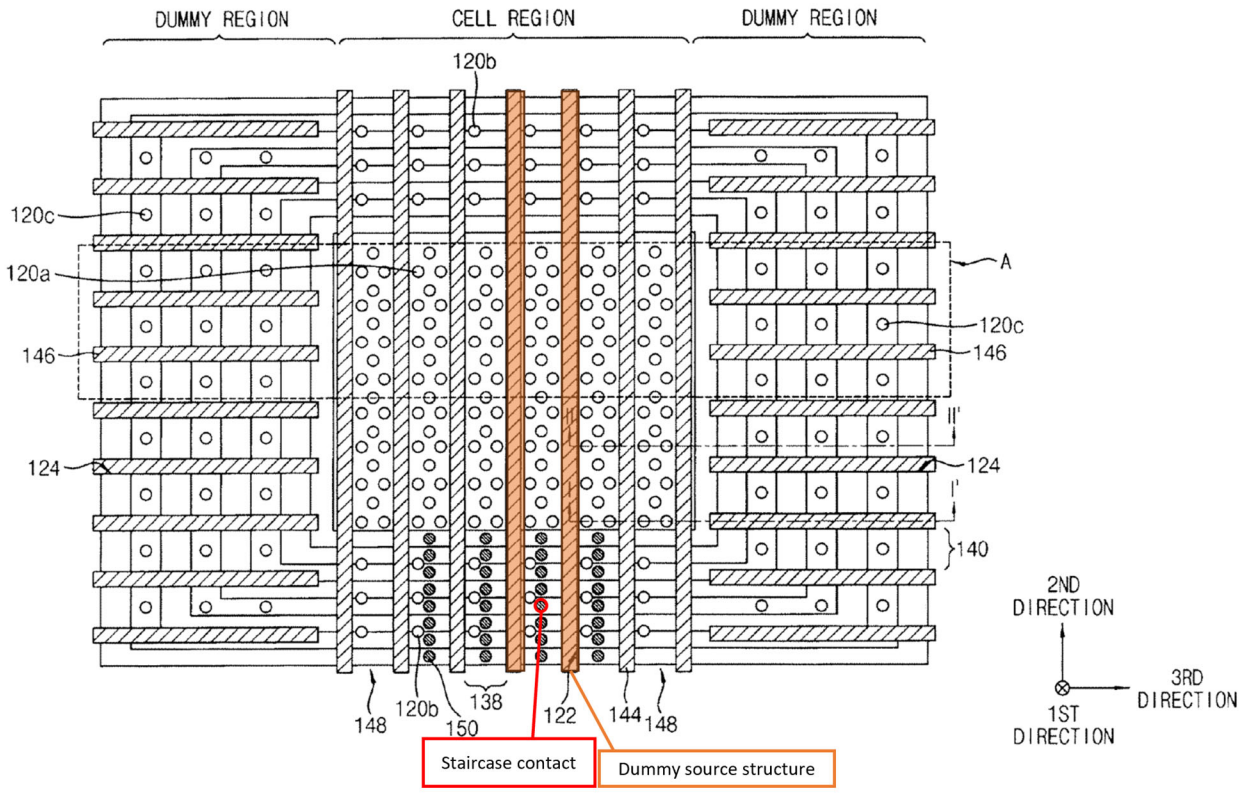
Park, Fig. 1 (annotated).

D. Claim 4:

1. [4] "The 3D memory device of claim 1, wherein the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact."

As discussed in claim [3], Park discloses "the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact." As shown below, when *the plurality of dummy source structures* are two common source lines and when the *staircase contact* is one contact, the common source lines both surround and are of nominally equal lateral distances to that staircase contact.

FIG. 1



Park (annotated), Fig. 1; Banerjee ¶ 163.

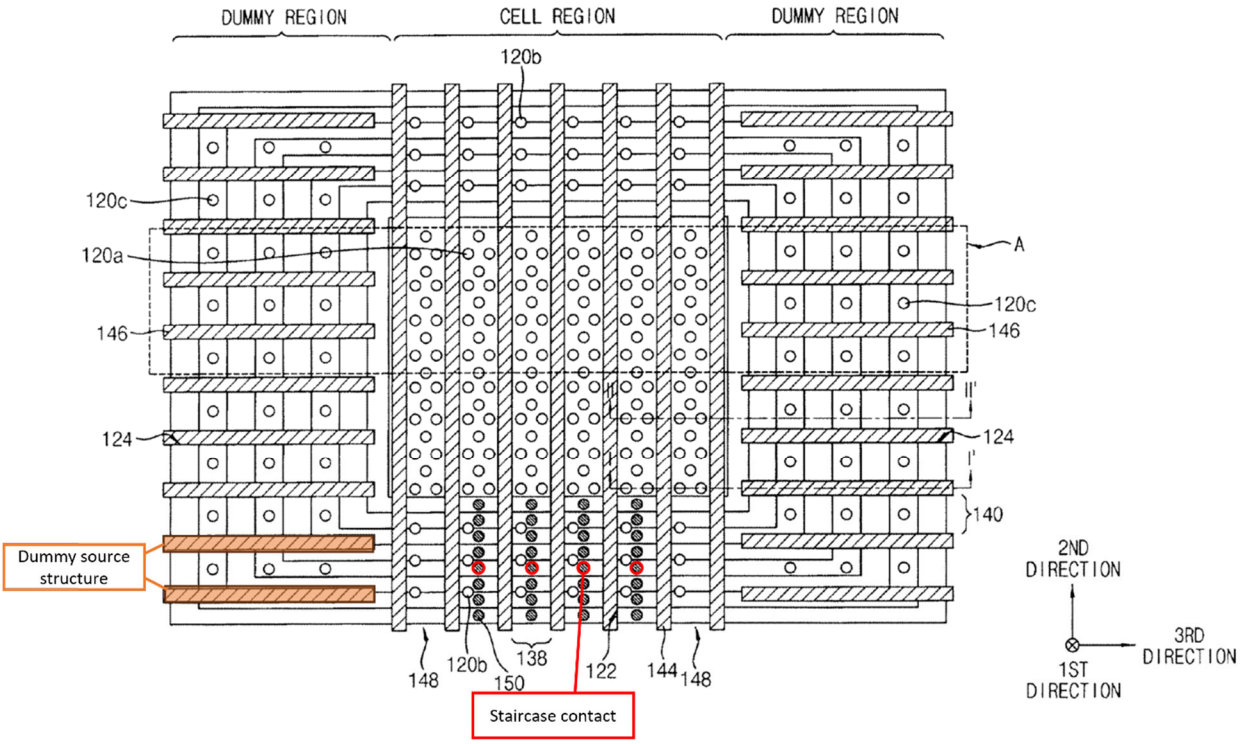
E. Claim 5:

1. [5] "The 3D memory device of claim 1, wherein in a plan view, at least two of the plurality of dummy source structures are arranged in a first row that extends along a first lateral direction."

Park discloses this limitation.

As shown in annotated Figure 1 below, there are *at least two of the plurality of dummy source structures* (in orange) arranged in *a first row that extends along a first lateral direction*. *See* Park, 26:26-29.

FIG. 1



Id., Fig. 1 (annotated).

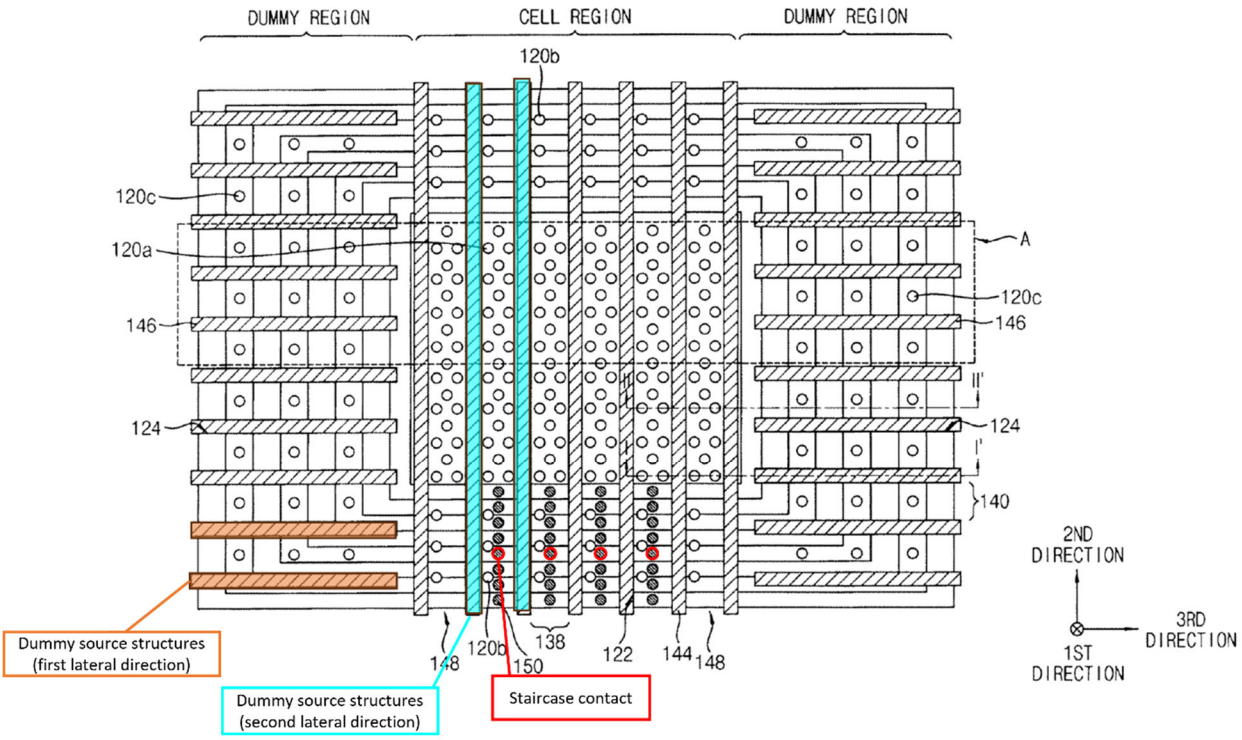
Note that a row is "a number of objects arranged in a usually straight line." (https://www.merriam-webster.com/dictionary/row). The above row is like a row of match sticks going from north to south. Note that the *plurality of dummy source structures* includes all of the *dummy source structures* of Park such that they *surround the staircase contacts*. Banerjee ¶¶ 164-69.

F. Claim 6:

1. [6] "The 3D memory device of claim 5, wherein in the plan view, at least two other dummy source structures are arranged in a second row that extends along a second lateral direction perpendicular to the first lateral direction."

Park discloses this limitation. The '872 Patent states that the first lateral direction may be a X direction, and the second lateral direction may be a Y direction. Ex. 1001, 6:53-58. Annotated Figure 1 below shows two dummy source lines in orange arranged in a first row that extends along a first lateral direction (which also satisfies the limitation of claim 5) and two common source lines in teal arranged in a second row that extends along a second lateral direction (like a row of match sticks laid out in a row from east to west) perpendicular to the first lateral direction.

FIG. 1



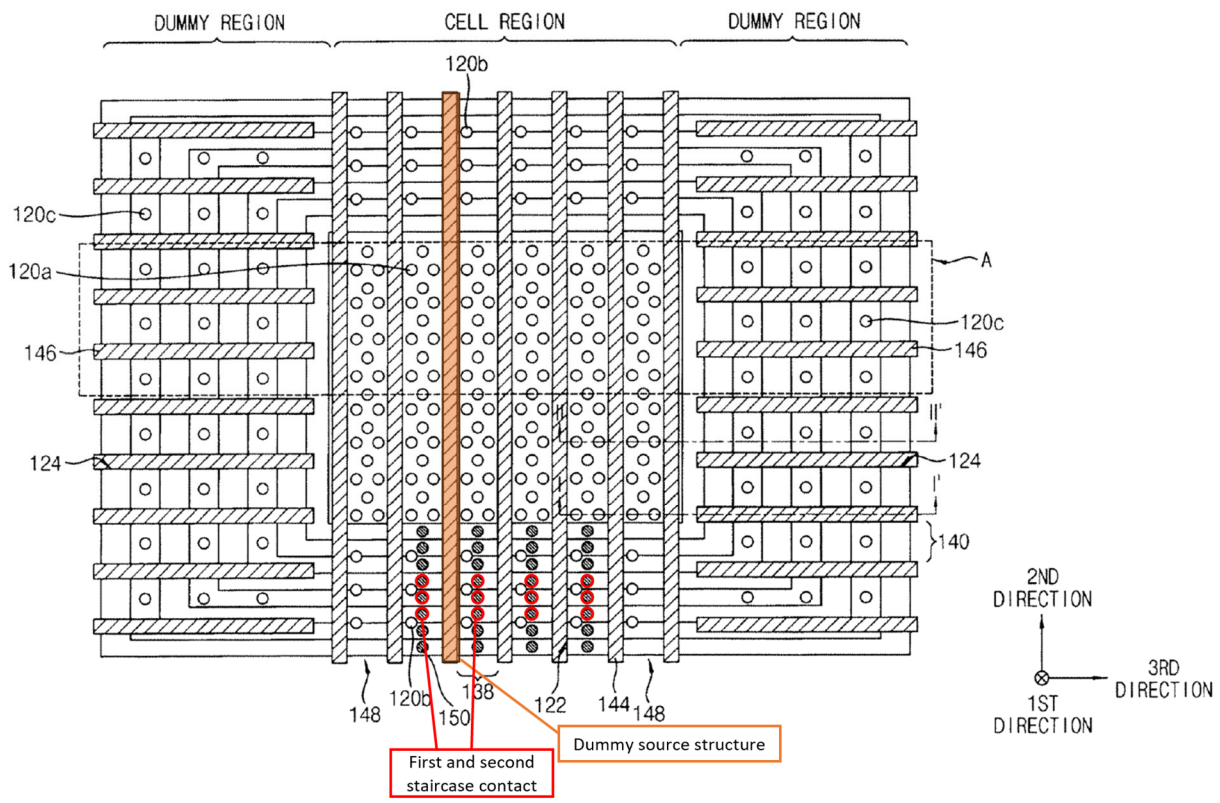
Park (annotated), Fig. 1. Note that the *plurality of dummy source structures* includes all of the *dummy source structures* of Park such that they *surround the staircase contacts*. Banerjee ¶¶ 170-71.

G. Claim 11:

1. [11] "The 3D memory device of claim 1, comprising first and second staircase contacts, wherein at least one dummy source structure is located between the first and second staircase contacts."

Park discloses this limitation. Annotated Figure 1 below shows the first and second contact plugs 150 ("staircase contact") in red, and at least one common source line 144 (i.e., "dummy source structure") in orange, that is located between the first and second staircase contacts.

FIG. 1



Park (annotated), Fig. 1; Banerjee ¶¶ 172-73.

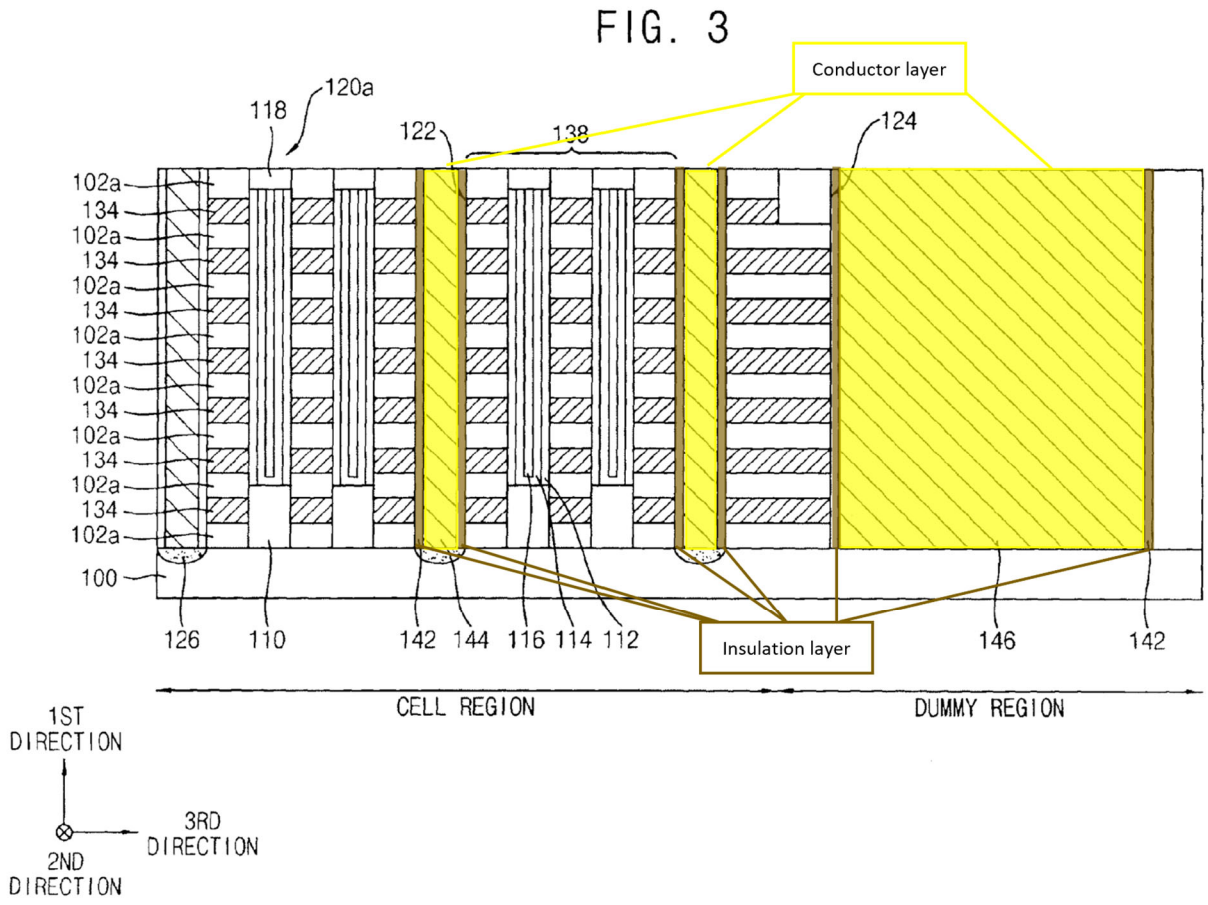
H. Claim 13:

1. [13] "The 3D memory device of claim 1, wherein the conductive contact comprises a conductor layer, and wherein the at least one dummy source structure further comprises a spacer surrounding the conductor layer along a sidewall of the conductor layer, the spacer comprising a dielectric material."

Park discloses, or at least renders obvious, this limitation.

As discussed in [1.E], Park discloses both dummy source line 146 and common source line 144 as *dummy source structures* which are formed in the second opening 124 and first opening 122, respectively. Park states that after the first

opening 122 and second opening 124 are formed, "an insulation layer may be formed conformally on sidewalls and bottoms of the first and second openings 122 and 124." Park, 13:42-46. This insulation layer formed on the sidewalls acts as a spacer and so comprises a *spacer surrounding the conductor layer along a sidewall of the conductor layer, the spacer comprising a dielectric material*. The insulator layer would have been understood to be a dielectric material for two reasons. First, Park consistently describes its insulators as being made with dielectric materials. *Id.*, 6:50-53, 7:19-22, 9:47-51, 10:16-20. Second, in the semiconductor context, the term insulator layer, particularly an insulating liner layer, is understood as a dielectric material, such as silicon oxide, because oxides in the semiconductor context are the preferable, practical material for such liners. Banerjee ¶¶ 174-76. In any event, it would have at least been obvious, because dielectric materials were the practical way to implement such insulation liner layers and were the industry-standard, because such materials, e.g., silicon dioxide were the ideal material for such applications. *Id.*, ¶¶ 176-78 (citing Ex. 1006, [0038] as knowledge of a POSITA). As discussed in [1.F], "conductive layer" then fills the rest of the first opening 122 and second openings 124 to form a common source line 144 and dummy source line 146, respectively. Park, 13:53-54. Annotated Figure 3 shows this below.



XI. GROUND 2: CLAIMS 1-6 AND 11-13 ARE OBVIOUS OVER TESSARIOL

Tessariol (Ex. 1006), when considered in view of the knowledge of a POSITA, renders claims 1-6 and 11-13 obvious under PO's apparent construction of *dummy source structures*. Banerjee ¶ 179.

A. Claim 1:

1. [1.PRE] "A three-dimensional (3D) memory device, comprising:"

To the extent the preamble is limiting, Tessariol discloses it. Tessariol discloses that "[e]mbodiments disclosed herein pertain to devices, to methods used

in forming a circuit structure, and to methods used in forming an array of elevationally-extending transistors and a circuit structure adjacent thereto." Tessariol, [0001]. Tessariol describes its embodiments in the context of "a construction 10." *Id.*, [0027]. Construction 10 would have been understood to be a memory device. For example, Tessariol discloses that construction 10 may include "memory cells." *Id.*, [0042]. An embodiment of construction 10 is a 3D NAND. *Id.*, [0006] ("NAND architecture may be configured in a three-dimensional arrangement comprising vertically-stacked memory cells individually comprising a reversibly programmable vertical transistor."), [0030] ("Elevationally-extending channel openings 26 have been formed into vertically-alternating tiers 16 and 18 in first stack 24.").

Thus, Tessariol discloses *a three-dimensional (3D) memory device* (e.g., construction 10). Banerjee ¶¶ 180-82.

2. [1.A] "a substrate;"

Tessariol discloses this limitation. Specifically, as shown below in light blue, Tessariol discloses that "construction 10 comprises a base substrate 11." Tessariol, [0027].

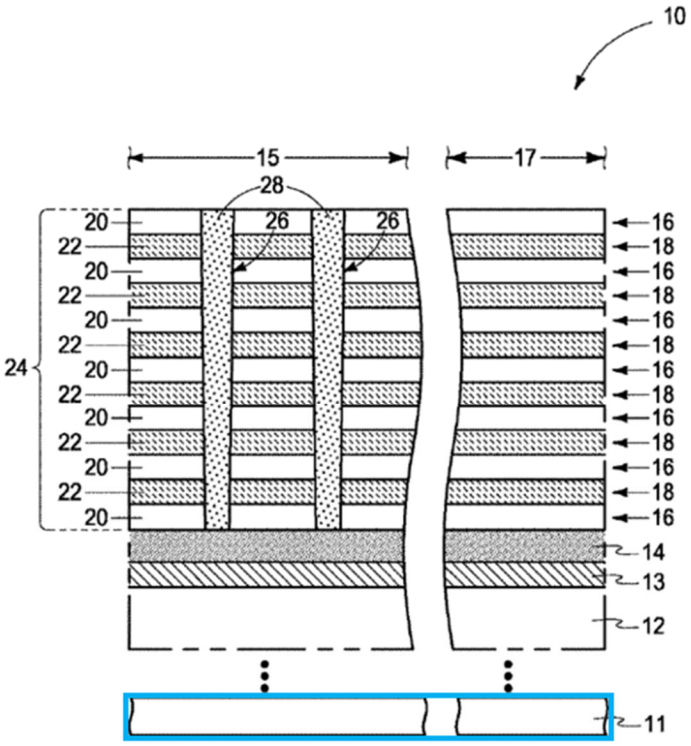


FIG. 1

Id., Fig. 1 (annotated).

Thus, Tessariol discloses *a substrate* (*e.g.*, base substrate 11). Banerjee ¶¶ 183-85.

3. [1.B] "a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;"

Tessariol discloses this limitation.

As an initial matter, the '872 Patent defines "on" as follows: "the meaning of 'on,' 'above,' and 'over' in the present disclosure should be interpreted in the broadest manner such that 'on' not only means 'directly on' something but also includes the meaning of 'on' something with an intermediate feature or a layer therebetween." Ex. 1001, 3:27-33.

Tessariol begins its discussion by stating that "[t]he discussion largely proceeds with a fabrication method forming two stacks." Tessariol, [0028]. Specifically, Tessariol discloses a multiple-stack structure that includes "vertically-alternating tiers [16 and 18] of different composition first [20] and second materials [22], with the vertically-alternating tiers comprising an array portion [15] and a portion adjacent to the array portion [17]." *Id.* As shown below, Tessariol discloses first forming "a ***first stack 24*** of vertically-alternating tiers 16 and 18." *Id.*, [0029] (emphasis added).

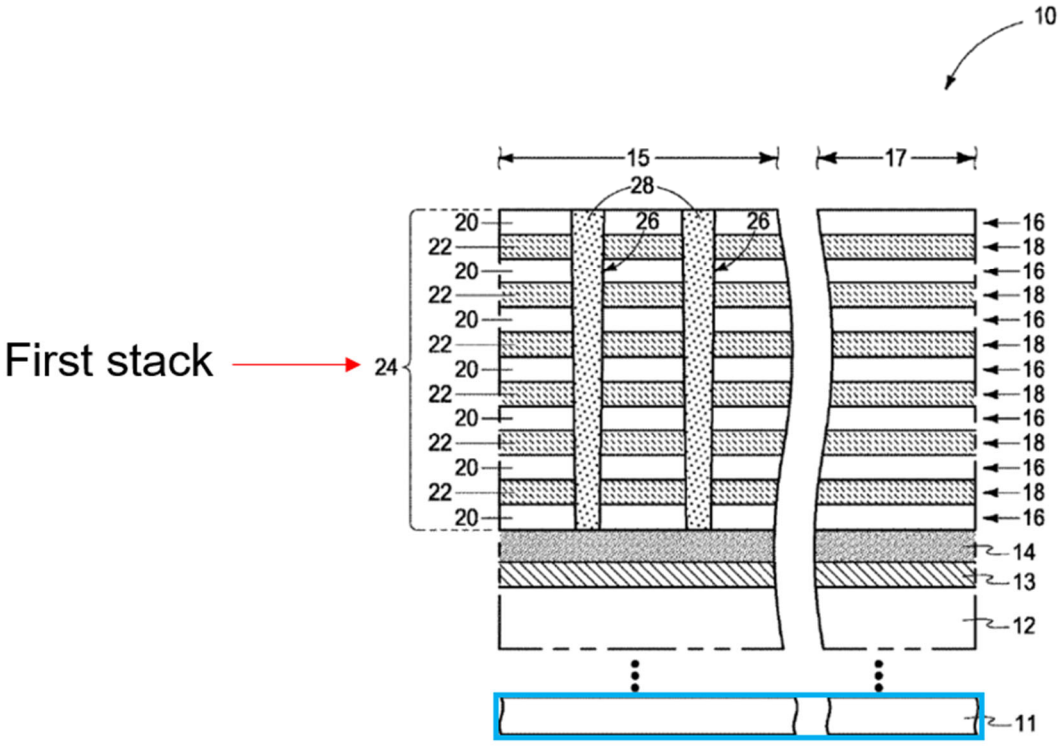


FIG. 1

Id., Fig. 1 (annotated).

Then, as shown below, Tessariol discloses forming "a ***second stack 30*** of vertically alternating tiers 18, 16, of different composition materials 22, 20 . . . over first stack 24." Tessariol, [0031] (emphasis added).

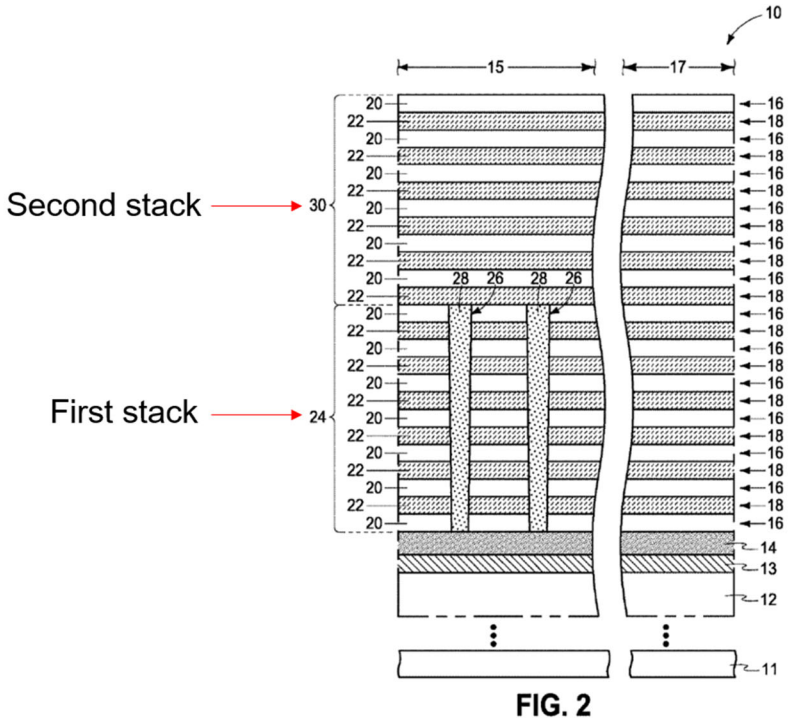


FIG. 2

Id., Fig. 2 (annotated).

First and second stacks 24 and 30 include "[v]ertically-alternating tiers 16 and 18 of different composition first and second materials 20 and 22." Tessariol, [0029]. Tessariol discloses that "[i]deally, materials 20 and 22 are of the same relative compositions with respect to one another in first stack 24 and second stack 30." *Id.*, [0031]. Tessariol further discloses that "[f]irst material 20 comprises insulative material" and "[s]econd material 22 . . . may comprise any one or more of

conductive, semiconductive, and insulative materials. *Id.*, [0029]. The first material layers surround the second material layers (which are gate lines):

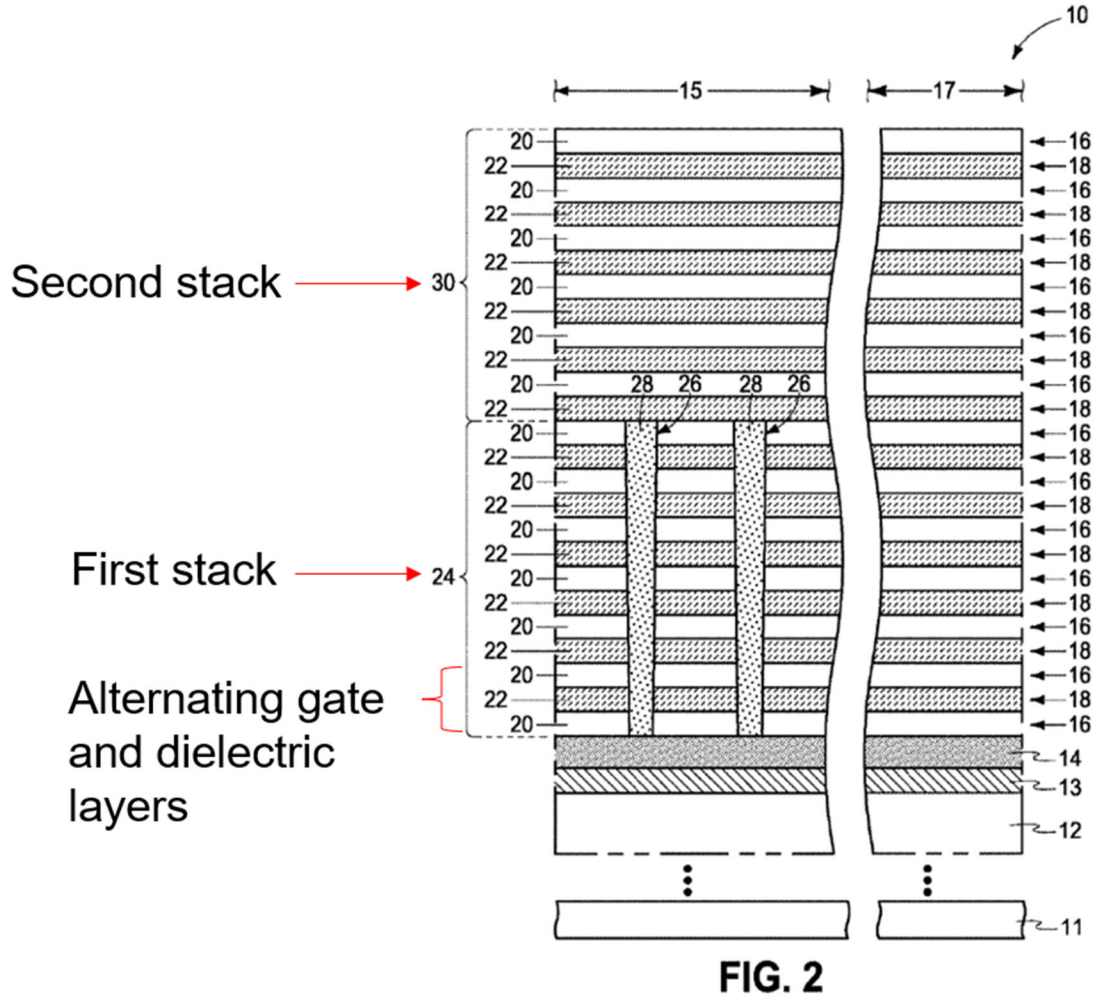


FIG. 2

Id., Fig. 2 (annotated).

Note that the sacrificial gate layers 22 are etched away and replaced with conductive gate layers 72. Tessariol, [0041] ("FIGS. 11-13 show the void space (not shown) resulting from etching away material 22 (not shown) as having been filled with conductive material 72 (e.g., metal material). Steps 40-47 now comprise

conductive steps due to presence of conductive material 72 and that are at least partially elevationally separated from one another by insulative material 20.").

Thus, Tessariol discloses *a memory stack comprising interleaved conductive layers and dielectric layers* (e.g., stacks 24 and 30, which comprise alternating layers 20 and 72) *on the substrate* (e.g., substrate 11). Banerjee ¶¶ 186-93.

4. [1.C] "a staircase structure on one side of the memory stack;"

Tessariol discloses this limitation.

Recall that Tessariol's memory device includes "an array portion [15] and a portion adjacent to the array portion [17]." Tessariol, [0028]. The adjacent region 17 is *on one side of the memory stack*:

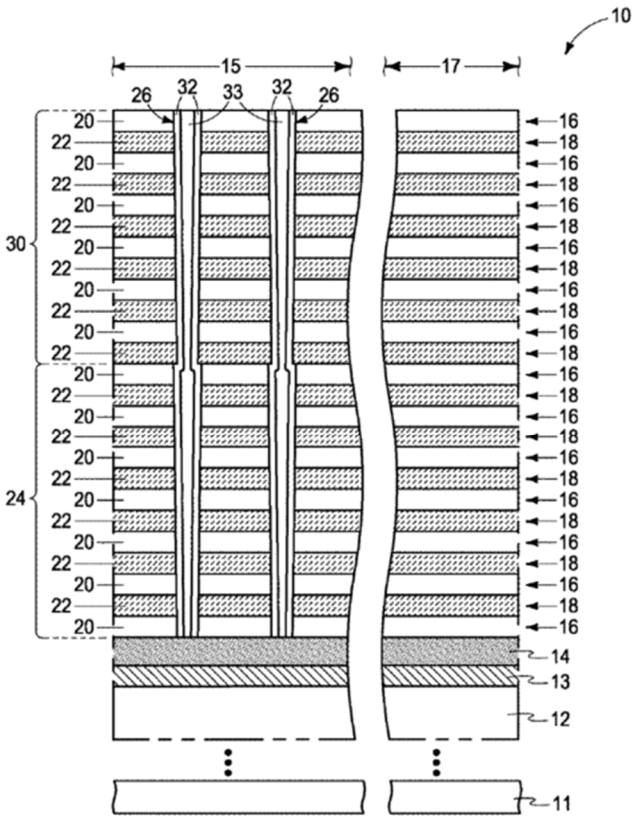


FIG. 5

Id., Fig. 5.

The adjacent region 17 is the *staircase structure* portion of Tessariol's multi-stack structure, and Tessariol discloses exemplary staircases in Figures 6-7: "FIGS. 6 and 7 show an expanded, yet reduced-scale, version of adjacent portion 17 as comprising three stair step structures 34, 36, and 38." Tessariol, [0034].

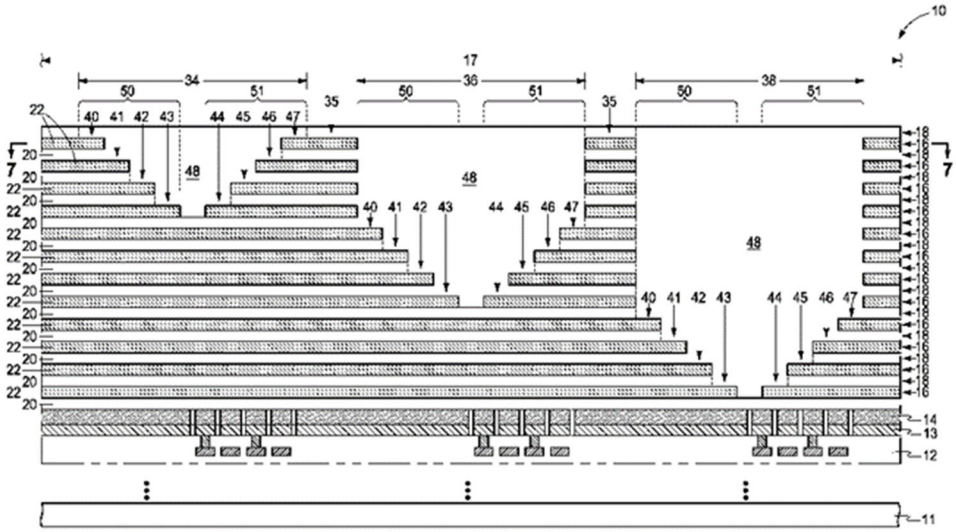


FIG. 6

Id., Fig. 6. Further, Tessariol discloses that "[a]dditionally, only one stair step structure, two stair step structures, or more than three stair step structures may be formed. Such may be formed by any suitable existing or yet-to-be-developed technique, with photolithographic patterning and etch being one example." *Id.,* [0034].

Thus, Tessariol discloses *a staircase structure on one side of the memory stack* (e.g., staircase in adjacent region 17 next to array region 15). Banerjee ¶¶ 194-98.

5. [1.D] "a staircase contact in the staircase structure; and"

Tessariol discloses this limitation.

Tessariol discloses "[r]eferring to FIGS. 15-18, and in one embodiment, operating conducting vias 80 have been formed which individually extend elevationally to and directly electrically couple with conductive material 72 of one of conductive steps 40-47." Tessariol, [0046]; *see also id.*, [0052] ("In one

embodiment, operating conducting vias (e.g., 80) individually extend elevationally to and directly electrically couple with conductive material (e.g., 72) of one of the conductive steps.").

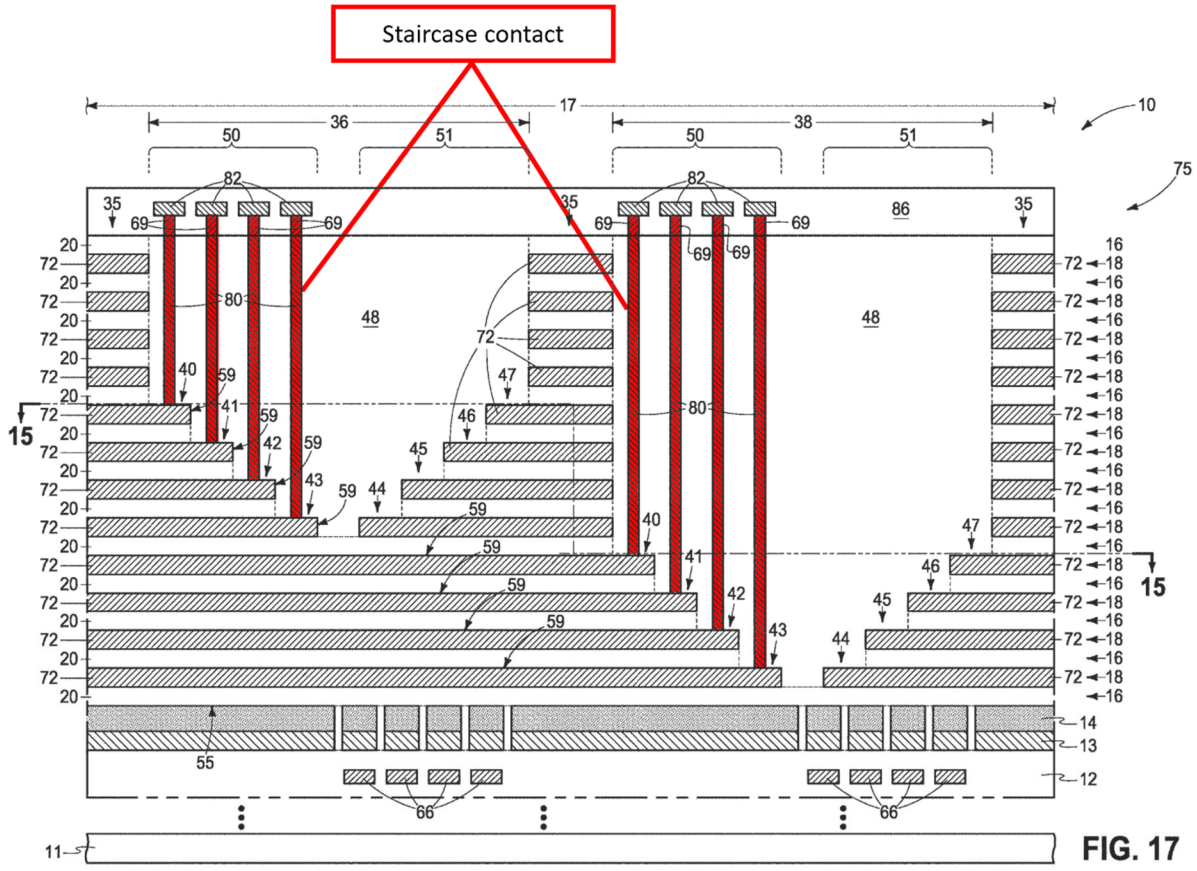


FIG. 17

Id., Fig. 17.

Thus, Tessariol discloses *a staircase contact* (e.g., a staircase-region contact 80) *in the staircase structure* (e.g., staircase in adjacent region 17). Banerjee ¶¶ 199-201.

6. [1.E] "a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact,"

Tessariol discloses this limitation under PO's apparent construction of *dummy source structures*.

First, Tessariol discloses the use of supporting pillars, referred to as dummy structures 60 and operative conductive vias 58, that comprise "an insulative lining 62 (e.g., silicon dioxide and/or silicon nitride) and a conductive core 64 (e.g., metal material)." Tessariol, [0038]; *see also id.*, [0041] (support function). The dummy structures 60 and operative conductive vias 58 are formed in dummy structure openings 56 and elevationally extending via openings 54 that are formed through a memory stack comprised of insulating and conductive materials. *Id.*, [0037]-[0038]. The dummy structure openings 56 and via openings 54 may be formed simultaneously, and the respective dummy structures 60 and operative conductive vias 58 may also be formed simultaneously. *Id.*, [0037]-[0038]. The '872 Patent provides an example of a dummy source structure with a conductive core and insulating liner, and states that it may be an active interconnect. Ex. 1001, 5:37-43. Thus, under PO's interpretation, dummy structures 60 and conductive vias 58 are *dummy source structures*, even though they are not formed in voids that are used in the gate line replacement process.

Second, as shown below, these structures *extend[] vertically through the staircase structure*.

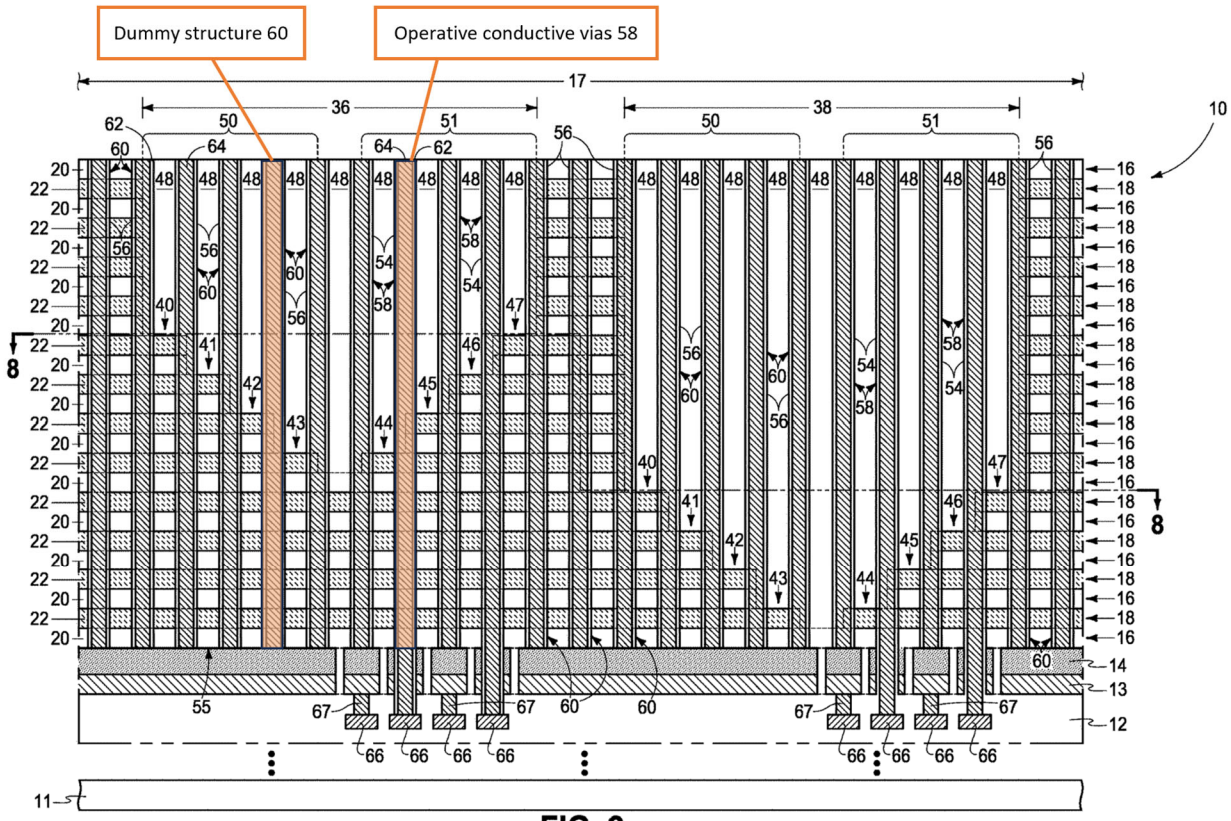


FIG. 9

Tessariol, Fig. 12, [0041] ("Such may thereby temporarily effectively leave void space (not shown) elevationally between first material tiers 20, with such tiers being elevationally supported and prevented from collapsing within array portion 15 by transistor material 32 and by both dummy-support structures 60 and operative conductive vias 58 within the stair step structures in adjacent portion 17.").

Third, Tessariol discloses that *the plurality of dummy source structures surround[] the staircase contact*. Before creating the staircase contacts, Tessariol

forms the dummy support structures 60 and conductive vias 58, both which are shown below in a top-down view (note dummy support structures 60 are in regions 50 and the conductive vias 58 are in regions 51):

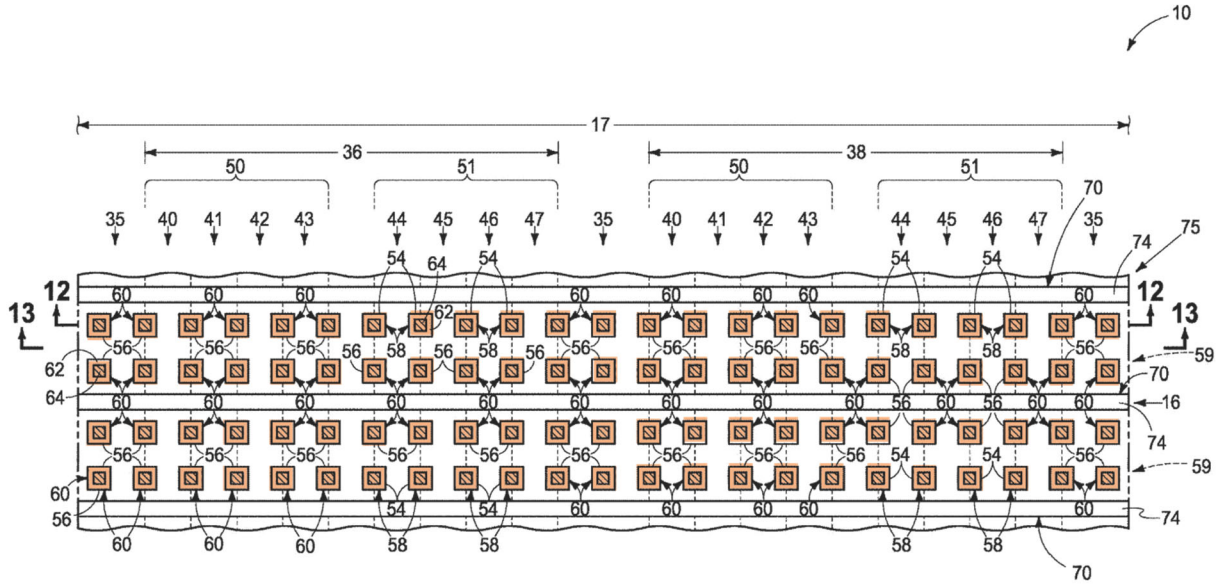


FIG. 11

Tessariol, Fig. 11.

Next, Tessariol forms the *staircase contacts* 80 (in red circles below):

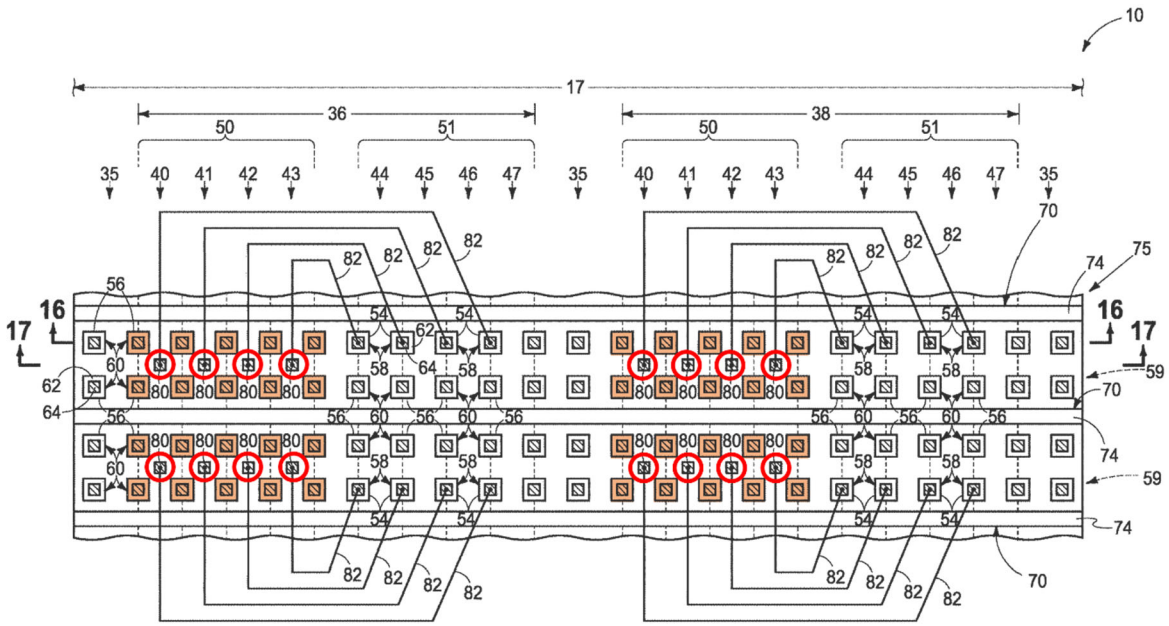


FIG. 15

Tessariol, Fig. 15 (annotated), [0046] ("Referring to FIGS. 15-18, and in one embodiment, operating conducting vias 80 have been formed which individually extend elevationally to and directly electrically couple with conductive material 72 of one of conductive steps 40-47.").

As can be seen above, taking the case of a *staircase contact*, *a plurality of dummy source structures surround* a given *staircase contact*, just like the exemplary embodiments of the '872 Patent in which four *dummy source structures surround the staircase contact*. *See* Section VII. This is shown below:

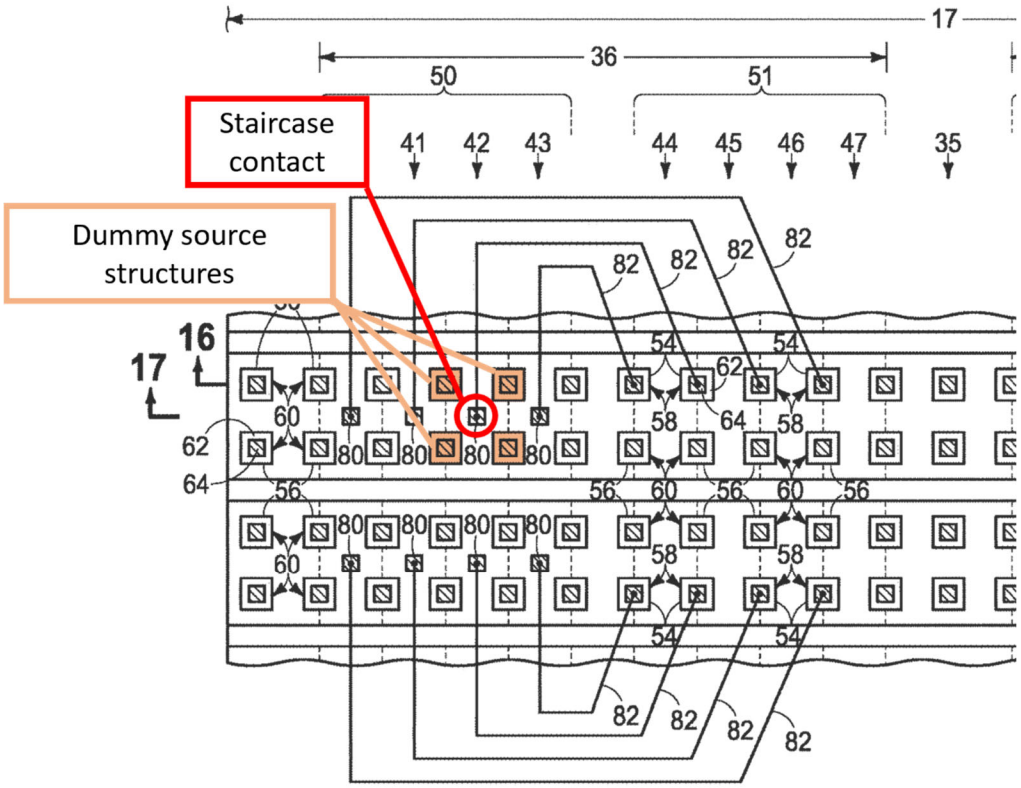


FIG. 15

Tessariol, Fig. 15 (partial) (annotated). As shown above, four *dummy source structures surround* each *staircase contact*.

Thus, Tessariol discloses *a plurality of dummy source structures* (e.g., dummy structures 60) *each extending vertically through the staircase structure* (e.g., through adjacent region 17), *the plurality of dummy source structures surrounding the staircase contact* (e.g., a via 80). Banerjee ¶¶ 202-10.

7. [1.F] "wherein each of the dummy source structures comprises a conductive contact."

Tessariol discloses this limitation or at least renders it obvious.

Tessariol discloses dummy structures 60 and operative conductive vias 58 that comprise "an insulative lining 62 (e.g., silicon dioxide and/or silicon nitride) and a conductive core 64 (e.g., metal material)." Tessariol, [0038]. This is like an embodiment of the '872 Patent in which the dummy structures have a conductive core and insulating liner.[6] Ex. 1001, 11:34-49.

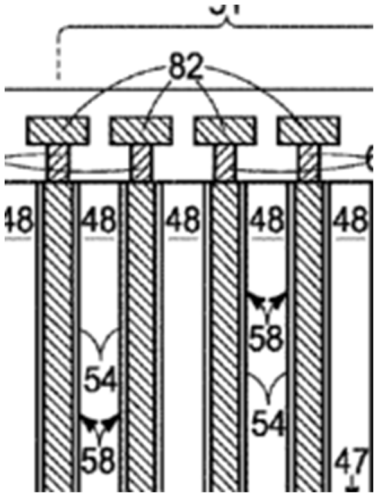
The conductive vias connect to interconnect lines: "Interconnect lines 82 have been formed above stair step structures 36 and 38 and individually directly electrically couple together different individual operating conducting vias 80 to different individual operative conductive vias 58 through conductive extensions 69." Tessariol, [0046], Fig. 16. While the claim term includes the word "dummy," the specification explains that the structure need not be inoperative. Rather, the specification states that "dummy source structures" can "contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices." Ex. 1001, 5:40-43, 16:63-66; Banerjee ¶¶ 211-14.

[6] Unlike the '872 Patent, Tessariol's dummy structures 60 and operative conductive vias 58 do not fill the voids used for the sacrificial gate replacement process.

To the extent that PO argues that Tessariol does not disclose that the dummy structures 60 include a *contact* on the theory that they do not connect to an upper-level interconnect (and thus cannot connect to an upper-level interconnect), PO would be advancing an incorrect construction, but regardless, it would have been obvious for that the dummy source structures 60 can contact an upper-level interconnect.

First, PO's theory would rely on a faulty premise and fail for that reason alone. The claimed *contact* need not be a separate element from a conductive core. *See* Section X.A.7. Nor does the *dummy source structure* need to contact an upper-level interconnect, because the '872 Patent explains that a *dummy* structure does not have to make such contact. *See* Section VII.A. The *dummy source structures* of Tessariol include a conductive core, like the '872 Patent embodiments. *See* Section XI.A.6; Tessariol, [0046]. The claim requires nothing more. Banerjee ¶ 214.

Second, at the very minimum, it would have been obvious that Tessariol's dummy structures would include the same structure as the conductive vias that do *contact* the upper-level interconnect, and thus include a *contact* even under PO's erroneous argument (i.e., they can contact an upper-level interconnect). Again, Tessariol's dummy structures and conductive vias are made at exactly the same. *See* Section XI.A.6. The conductive vias 58 do contact upper-level interconnects 82:



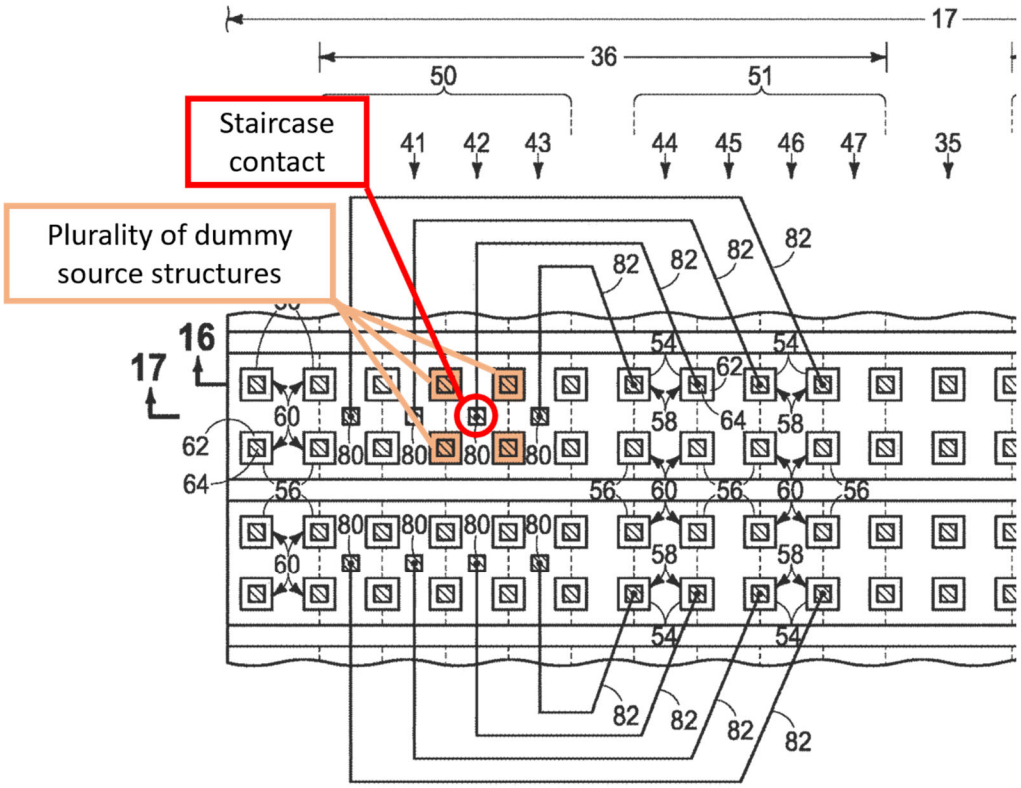
Tessariol, Fig. 16 (partial), [0046]. Accordingly, it would have been obvious to a POSITA for dummy source structures 60 to include a *contact* that could connect to an upper-level interconnect. Indeed, a POSITA would have been motivated to build the dummy source structures and conductive vias with the same process (as Tessariol does), because it reduces processing time and cost. Further, the expectation of success would have been high, because it was common to build structures at the same time using the same process steps. Banerjee ¶¶ 215-16.

Thus, Tessariol discloses, or at least renders obvious, a *conductive contact* (e.g., the metal core of the dummy structures 60 and conductive vias 58). Banerjee ¶ 217.

B. Claim 2:

1. [2] "The 3D memory device of claim 1, wherein the plurality of dummy source structures are located adjacent to the staircase contact."

Tessariol discloses this limitation. *See* Section XI.A.6. Annotated Figure 15 discloses that the plurality of dummy structures 60 (i.e., *dummy source structures*) are located adjacent to and surround the operating conducting via 80 (i.e., *staircase contact*).



Tessariol, Fig. 15 (partial) (annotated); Banerjee ¶ 218.

C. Claim 3:

1. [3] "The 3D memory device of claim 1, wherein at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact."

Tessariol discloses this limitation. *See* Section XI.A.6. Annotated Figure 15 discloses that at least two of the dummy structures 60 (i.e., *dummy source structures*) *are of nominally equal lateral distances* to the operating conducting via 80 (i.e., *staircase contact*).

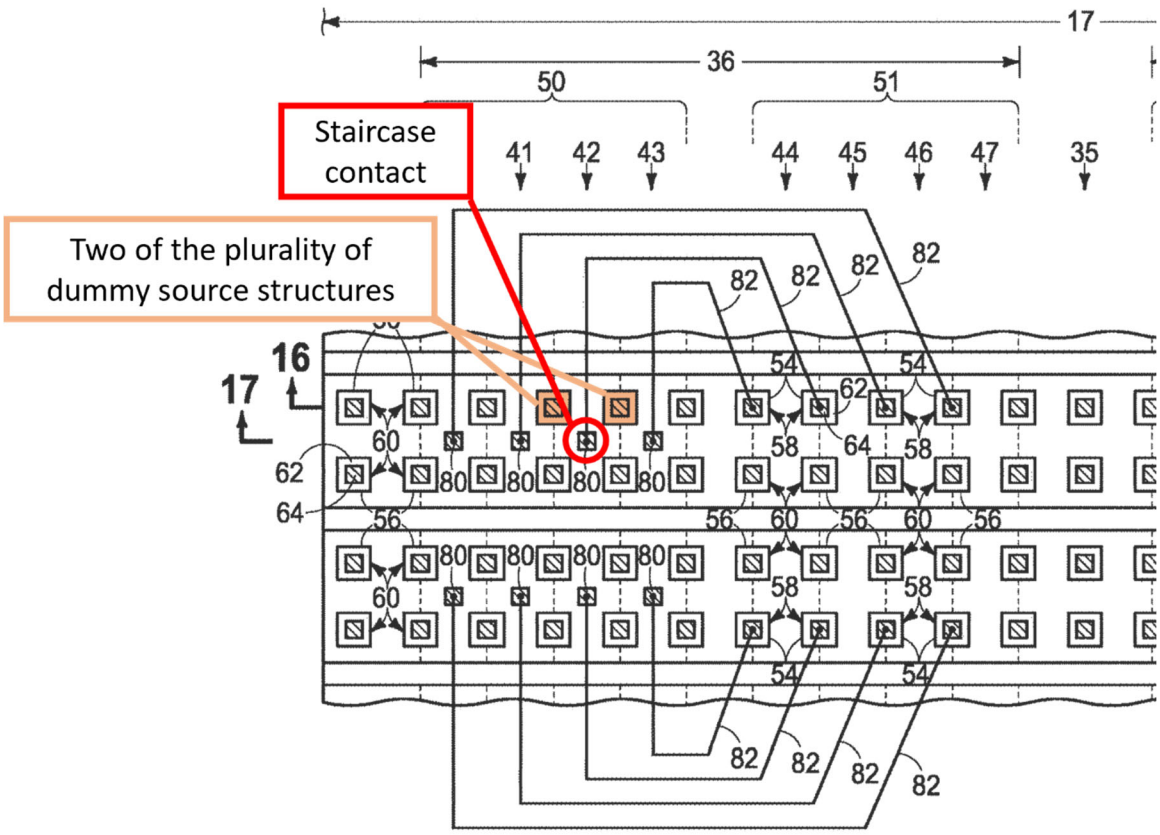


FIG. 15

Tessariol, Fig. 15 (partial) (annotated); Banerjee ¶ 219.

D. Claim 4:

1. [4] "The 3D memory device of claim 1, wherein the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact."

Tessariol discloses this limitation. *See* Sections XI.A.6., XI.C; Banerjee ¶ 220.

E. Claim 5:

1. [5] "The 3D memory device of claim 1, wherein in a plan view, at least two of the plurality of dummy source structures are arranged in a first row that extends along a first lateral direction."

Tessariol discloses this limitation. Annotated Figure 15 below shows dummy structures 60 (i.e., *dummy source structures*) in orange arranged in a first row that extends along a first lateral direction.

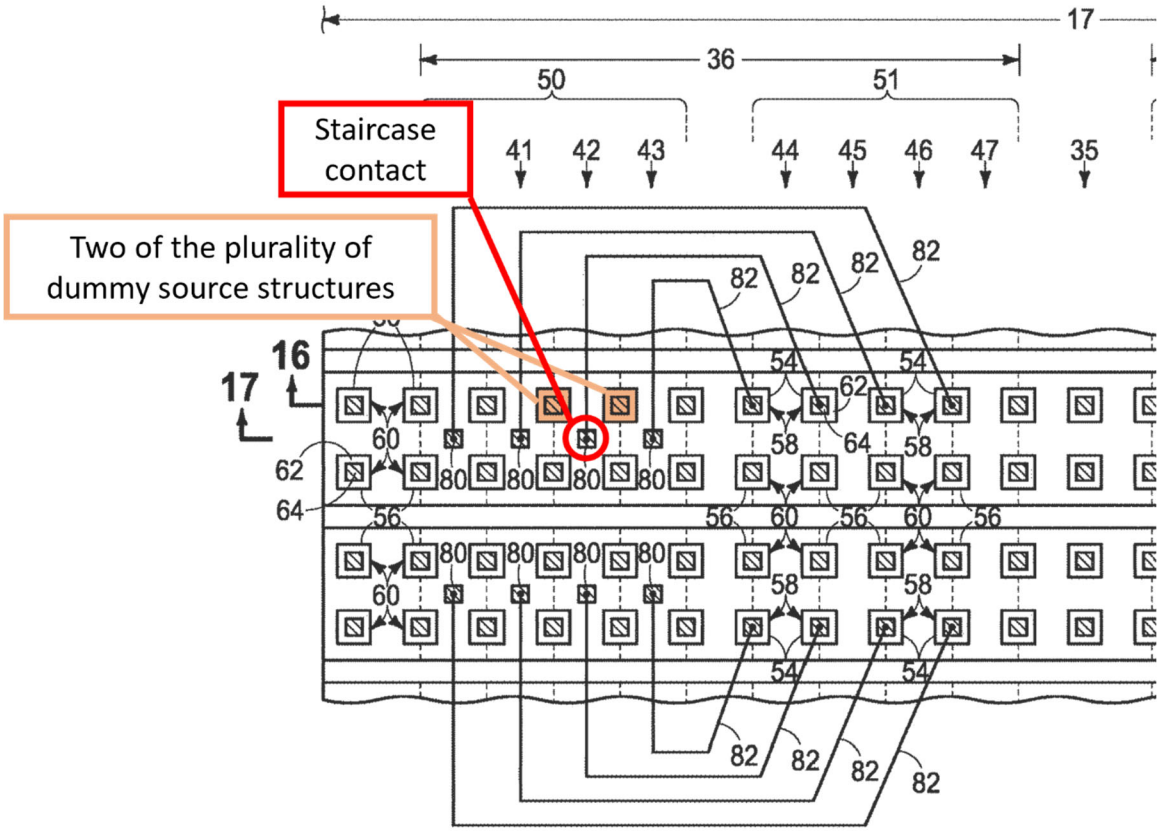


FIG. 15

Tessariol, Fig. 15 (annotated); Banerjee ¶¶ 221-22.

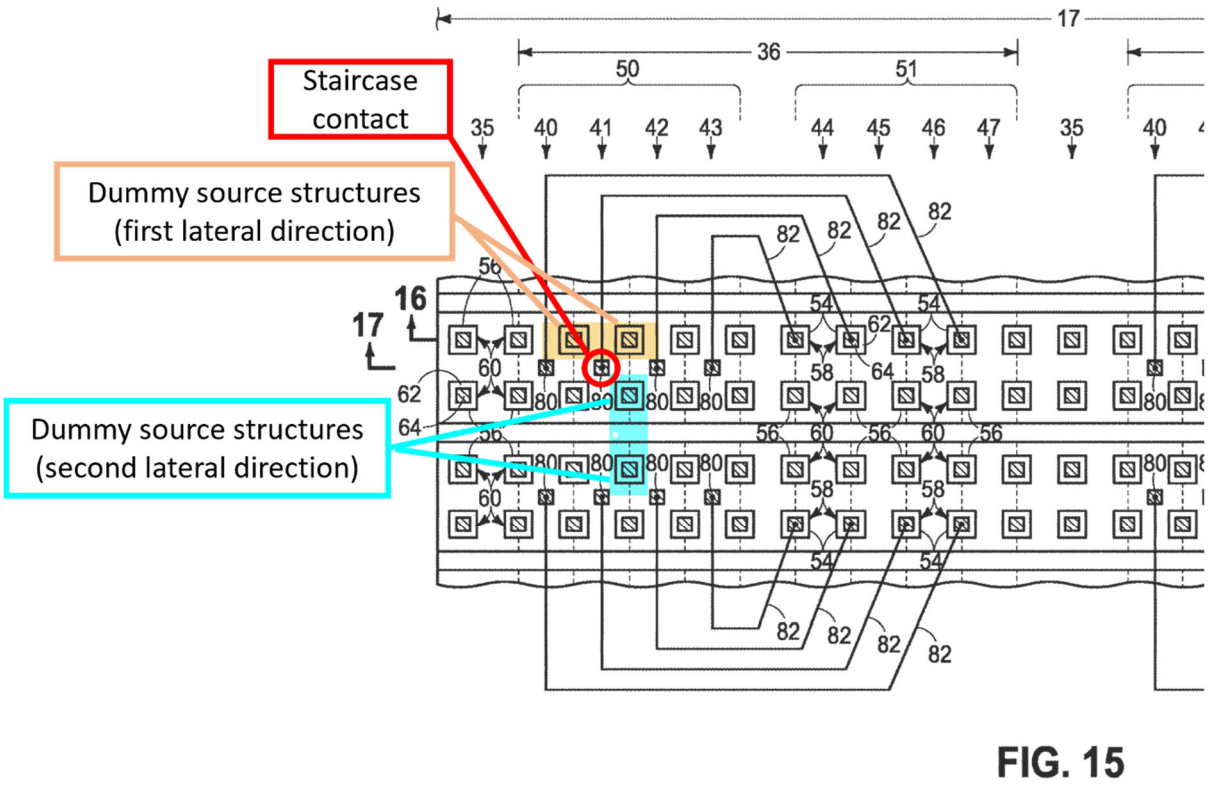
F. Claim 6:

1. [6] "The 3D memory device of claim 5, wherein in the plan view, at least two other dummy source structures are arranged in a second row that extends along a second lateral direction perpendicular to the first lateral direction."

Tessariol discloses this limitation. The '872 Patent states that the first lateral direction may be a X direction, and the second lateral direction may be a Y direction. Ex. 1001, 6:54-59. Figure 1A is an embodiment of claim 6, which shows two dummy source structures along the first row in the X axis and two dummy source

structures along the second row in the Y axis. *Id.*, Figure 1A. The two dummy source structures in the first row do not surround the same staircase contact, and the two dummy source structures in the second row similarly do not surround the same staircase contact.

Annotated Figure 15 below shows two dummy structures 60 (i.e., *dummy source structures*) in orange arranged in a first row that extends along a first lateral direction (highlighted in orange) and two dummy structures 60 in teal arranged in a second row that extends along a second lateral direction (highlighted in teal) perpendicular to the first lateral direction. Note that in cases, the *dummy source structures* of Tessariol surround the *staircase contacts*, because four *dummy source structures* surround each contact.

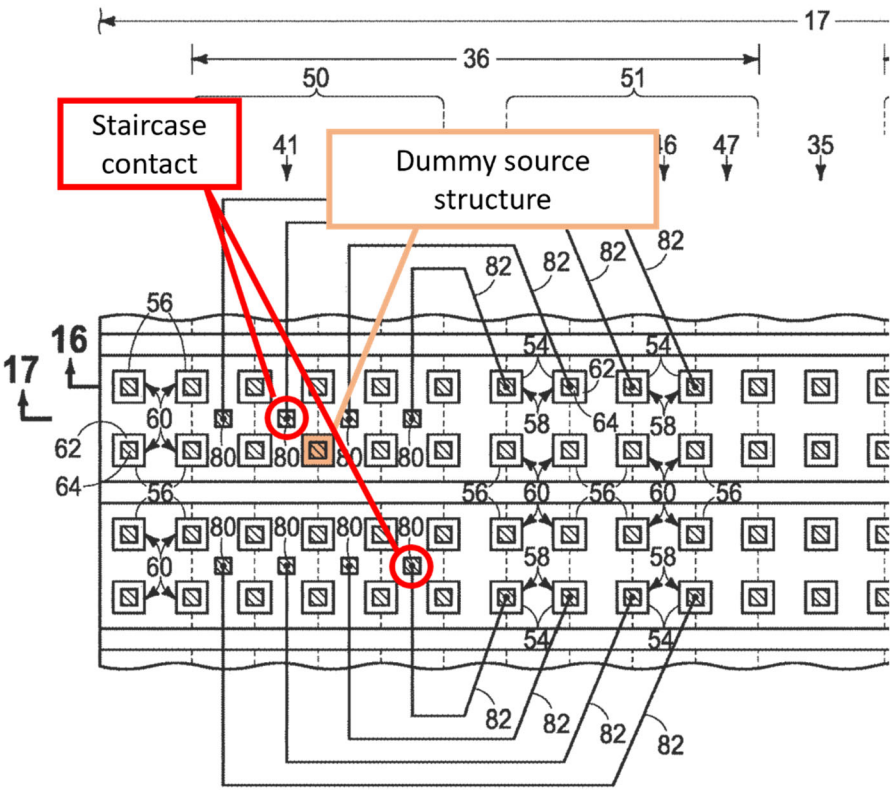


Tessariol, Fig. 15 (partial) (annotated); Banerjee ¶¶ 223-25.

G. Claim 11:

1. [11] "The 3D memory device of claim 1, comprising first and second staircase contacts, wherein at least one dummy source structure is located between the first and second staircase contacts."

Tessariol discloses this limitation. Annotated version of Figure 15 below shows the first and second operating conducting vias 80 (i.e., *staircase contacts*) in red, and at least one dummy structure 60 (i.e., *dummy source structure*) in orange, that is located between the first and second staircase contacts.



Tessariol, Fig. 15 (annotated); Banerjee ¶¶ 226-27. In all cases, the dummy source structures (*plurality of dummy source structures*) above surround the staircase contacts, because 4 dummy source structures surround each staircase contact. *Id.*

H. Claim 12:

1. [12] "The 3D memory device of claim 1, wherein at least two dummy source structures are located between the first and second staircase contacts."

Tessariol discloses this limitation. Annotated Figure 15 below shows the first and second operative vias 80 (*staircase contacts*) in red, and at least two dummy

structures 60 (*dummy source structure*) in orange, that are located between the first and second staircase contacts.

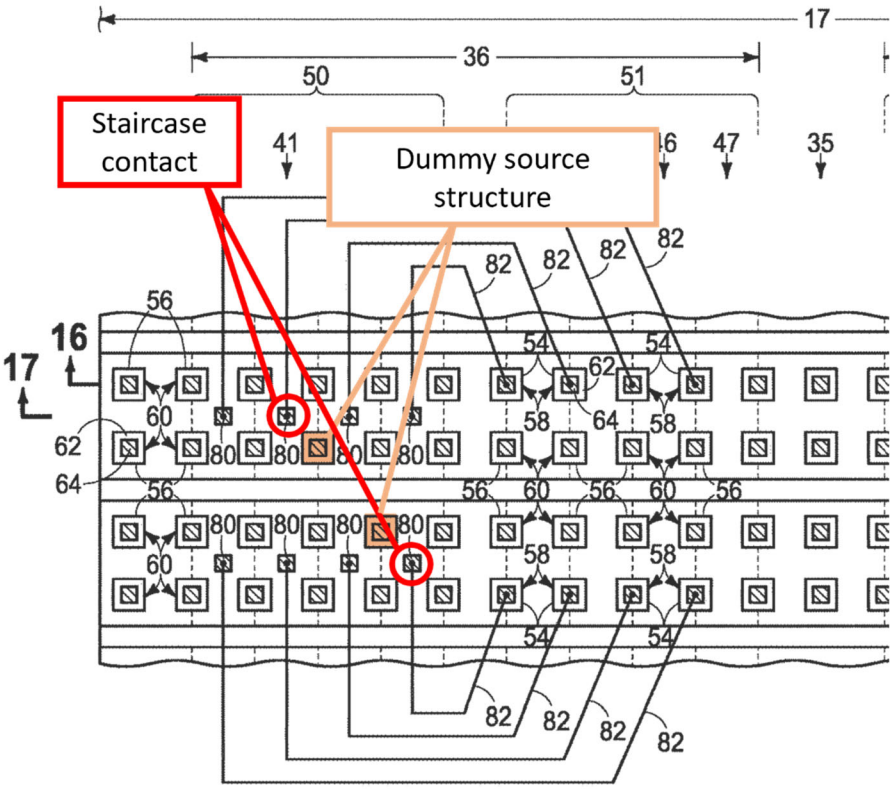


FIG. 15

Tessariol, Fig. 15. In all cases, the dummy source structures above surround the staircase contacts, because 4 dummy source structures surround each staircase contact. *Id.*; Banerjee ¶¶ 228-29.

I. Claim 13:

1. [13] "The 3D memory device of claim 1, wherein the conductive contact comprises a conductor layer, and wherein the at least one dummy source structure further comprises a spacer surrounding the conductor layer along a sidewall of the conductor layer, the spacer comprising a dielectric material."

Tessariol discloses this limitation.

As discussed in limitations [1.E] and [1.F] above, Tessariol discloses both dummy structures 60 and operative conductive vias 58 as *dummy source structures* with *conductive contacts*. Tessariol's dummy structures 60 and operative conductive vias 58 are formed "to comprise an insulative lining 62 (e.g., silicon dioxide and/or silicon nitride) and a conductive core 64 (e.g., metal material)." Tessariol, [0038]. Both silicon oxide and silicon nitride are *dielectrics*. Ex. 1001, 10:9-12. The insulative lining 62 acts as a *spacer* that surrounds the conductor layer along a *sidewall of the conductor layer*.

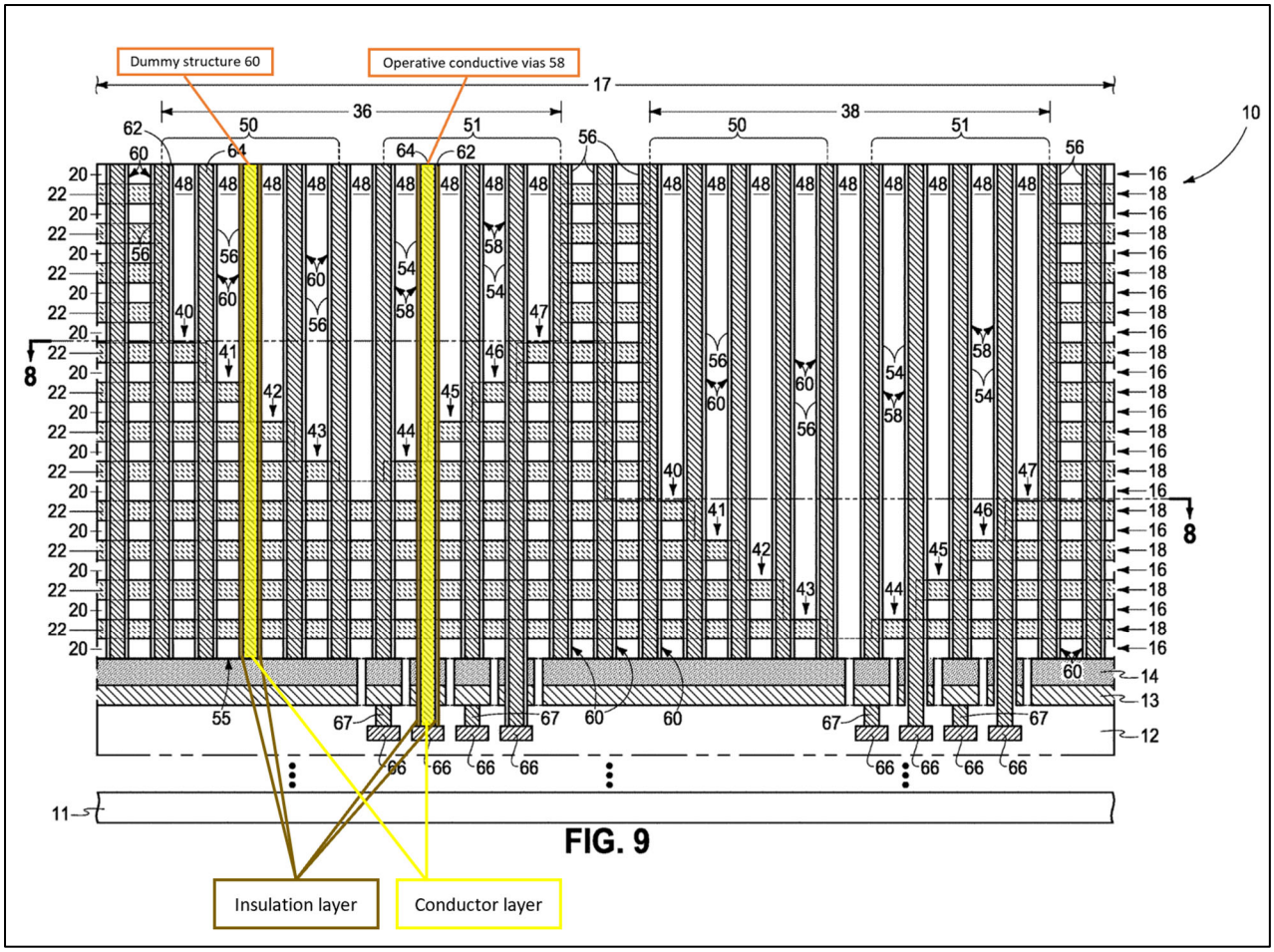


FIG. 9

Tessariol, Fig. 9 (annotated); Banerjee ¶¶ 230-32.

XII. SECONDARY CONSIDERATIONS

Petitioner is unaware of any applicable secondary considerations of nonobviousness. None were identified during prosecution. *See generally* Ex. 1002. Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness.

XIII. CONCLUSION

Petitioner respectfully requests that the Board enter a final written decision finding the Challenged Claims unpatentable.

Respectfully submitted,

ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: April 18, 2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 12,592 words.

Dated: April 18, 2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on April 18, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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Copies of this Petition and accompanying exhibits were also served via electronic mail on Patent Owner's counsel of record in a related district court litigation:

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