505458683 05/02/2019

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT5505486

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
WENYU HUA	03/28/2019
FANDONG LIU	03/28/2019
ZHILIANG XIA	03/28/2019

RECEIVING PARTY DATA

Name:	YANGTZE MEMORY TECHNOLOGIES CO., LTD.
Street Address:	18 GAOXIN 4TH ROAD
Internal Address:	EAST LAKE HIGH-TECH DEVELOPMENT ZONE
City:	WUHAN, HUBEI
State/Country:	CHINA

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	16402202

CORRESPONDENCE DATA

Fax Number: (703)827-8128

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 703-995-9887
Email: uspto@bayes.law
Correspondent Name: BAYES PLLC
Address Line 1: 1765 GREENSBORO STATION PLACE
Address Line 2: SUITE 900
Address Line 4: MCLEAN, VIRGINIA 22102

ATTORNEY DOCKET NUMBER:	10018-01-0045-US
NAME OF SUBMITTER:	JINRONG YUAN
SIGNATURE:	/Jinrong Yuan/
DATE SIGNED:	05/02/2019
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 3
source=10018-01-0045-US_Dec-Assign-SIGNED#page1.tif
source=10018-01-0045-US_Dec-Assign-SIGNED#page2.tif

source=10018-01-0045-US_Dec-Assign-SIGNED#page3.tif

COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

☒ The attached application, or

☐ United States application or PCT international application number _____

filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

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(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 153988** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

1934285-0050393-10.18.40.190
32786-28/03/2019 14:31

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Micron v. YMTC
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IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: **Wenyu Hua** Date: 2019.3.28

Signature of Inventor: Wenyu Hua

Inventor: **Fandong Liu** Date: 2019/3/28

Signature of Inventor: Fandong LIU

Inventor: **Zhiliang Xia** Date: 2019.03.28

Signature of Inventor: Zhiliang XIA

1934285-00507[B]-10.18.40.190
32766-28/03/2019 15:13

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Micron v. YMTC
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DocCode – SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 16402202 Document Date: 05/02/2019

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

- Drawing

At the time of document entry (noted above):

- USPTO employees may access SCORE content via DAV or via the SCORE web page.
- External customers may access SCORE content via PAIR using the Supplemental Content tab.

Form Revision Date: March 1, 2019

PTO/AIA/15 (10-17)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	10018-01-0045-US
First Named Inventor	Wenyu HUA
Title	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME
Priority Mail Express® Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [✔] **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. [ ] **Applicant asserts small entity status.** See 37 CFR 1.27
3. [ ] **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. [✔] **Specification** [*Total Pages* 32] Both the claims and abstract must start on a new page. *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. [✔] **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 13]
6. **Inventor's Oath or Declaration** [*Total Pages* 3] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. [ ] Newly executed (original or copy)
   b. [✔] A copy from a prior application (37 CFR 1.63(d))
7. [✔] **Application Data Sheet** ** See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   [ ] Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   a. [ ] Computer Readable Form (CRF)
   b. [ ] Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] Paper
   c. [ ] Statements verifying identity of above copies

ADDRESS TO:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ACCOMPANYING APPLICATION PAPERS

10. [✔] **Assignment Papers** (cover sheet & document(s))
    Name of Assignee: Yangtze Memory Technologies Co., Ltd.
11. [ ] **37 CFR 3.73(c) Statement** (*when there is an assignee*) [✔] **Power of Attorney**
12. [ ] **English Translation Document** (*if applicable*)
13. [ ] **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    [ ] Copies of citations attached
14. [ ] **Preliminary Amendment**
15. [ ] **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. [ ] **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. [ ] **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. [ ] **Other:**

***Note**: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

[✔] The address associated with Customer Number: 153988 **OR** [ ] Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone	7039959887	Email	

Signature	/Jinrong Yuan/	Date	May 2, 2019
Name (Print/Type)	Jinrong Yuan	Registration No. (Attorney/Agent)	76,066

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/17 (01-18)
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FEE TRANSMITTAL

Complete if known	
Application Number	
Filing Date	Herewith
First Named Inventor	Wenyu HUA
Examiner Name	To Be Determined
Art Unit	To Be Determined
Practitioner Docket No.	10018-01-0045-US

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

TOTAL AMOUNT OF PAYMENT ($) 1720.00

METHOD OF PAYMENT (check all that apply)

☐ Check ■ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

■ Deposit Account Deposit Account Number: 602227 Deposit Account Name: Bayes Deposit Account

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

■ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☐ Credit any overpayment of fee(s)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)

	FILING FEES			SEARCH FEES			EXAMINATION FEES			
Application Type	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**Fees Paid ($)**
Utility	300	150*	75	660	330	165	760	380	190	1720
Design	200	100	50	160	80	40	600	300	150	
Plant	200	100	50	420	210	105	620	310	155	
Reissue	300	150	75	660	330	165	2,200	1,100	550	
Provisional	280	140	70	0	0	0	0	0	0	

* The $150 small entity status filing fee for a utility application is further reduced to $75 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	**Undiscounted Fee ($)**	**Small Entity Fee ($)**	**Micro Entity Fee ($)**
Each claim over 20 (including Reissues)	100	50	25
Each independent claim over 3 (including Reissues)	460	230	115
Multiple dependent claims	820	410	205

Total Claims		**Extra Claims**	**Fee ($)**		**Fee Paid ($)**
20	-20 or HP =	0	x _____	=	0.00

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		**Extra Claims**	**Fee ($)**		**Fee Paid ($)**
3	-3 or HP =	0	x _____	=	0.00

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	**Fee ($)**	**Fee Paid ($)**

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $400 ($200 for small entity) ($100 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		**Extra Sheets**		**Number of each additional 50 or fraction thereof**		**Fee ($)**		**Fee Paid ($)**
13	- 100 =	_____	/ 50 =	_____ (round **up** to a whole number)	x	_____	=	_____

4. OTHER FEE(S) **Fees Paid ($)**

Non-English specification, $130 fee (no small or micro entity discount) _____

Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, $400 fee ($200 small or micro entity) _____

Other (e.g., late filing surcharge): _____ _____

SUBMITTED BY

Signature	/Jinrong Yuan/	Registration No. (Attorney/Agent) 76,066	Telephone 7039959887
Name (Print/Type)	Jinrong Yuan		Date May 2, 2019

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0045-US
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Wenyu		Hua	

Residence Information (Select One) US Residency ● Non US Residency Active US Military Service

City	Wuhan	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	18 Gaoxin 4th Road
Address 2	East Lake High-Tech Development Zone

City	Wuhan	State/Province	
Postal Code		Country [i]	CN

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Fandong		Liu	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Wuhan	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	18 Gaoxin 4th Road
Address 2	East Lake High-Tech Development Zone

City	Wuhan	State/Province	
Postal Code		Country [i]	CN

Inventor 3 Remove

Legal Name

Micron Ex. 1002, p. 9
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IPR2024-00789

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0045-US
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Zhiliang		Xia	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Wuhan	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	18 Gaoxin 4th Road
Address 2	East Lake High-Tech Development Zone

City	Wuhan	State/Province	
Postal Code		**Country** [i]	CN

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	153988		
Email Address	uspto@bayes.law	Add Email	Remove Email

Application Information:

Title of the Invention	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME		
Attorney Docket Number	10018-01-0045-US	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	13	**Suggested Figure for Publication (if any)**	1A

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country [i]

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0045-US
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	153988		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	PCT/CN2019/076186	2019-02-26

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0045-US
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME	

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (11-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0045-US
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0045-US
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0045-US
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First Name	Jinrong	Last Name	Yuan	Registration Number	76,066

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	10018-01-0045-US
	Application Number	
Title of Invention	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME	

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ABSTRACT

Three-dimensional (3D) memory devices and methods for forming the 3D memory devices are provided. In one example, a 3D memory device includes a substrate, a memory stack including interleaved conductive layers and dielectric layers on the substrate, and a staircase structure on one side of the memory stack. The 3D memory device also includes a staircase contact in the staircase structure and a plurality of dummy source structures each extending vertically through the staircase structure. The plurality of dummy source structures surround the staircase contact.

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WHAT IS CLAIMED IS:

1. A three-dimensional (3D) memory device, comprising:

a substrate;

a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;

a staircase structure on one side of the memory stack;

a staircase contact in the staircase structure; and

a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact.

2. The 3D memory device of claim 1, wherein the plurality of dummy source structures are located adjacent to the staircase contact.

3. The 3D memory device of claim 1, wherein at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact.

4. The 3D memory device of claim 1, wherein the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact.

5. The 3D memory device of claim 1, wherein in a plan view, at least two of the plurality of dummy source structures are arranged in a first row that extends along a first lateral direction.

6. The 3D memory device of claim 5, wherein in the plan view, at least two other dummy source structures are arranged in a second row that extends along a second lateral direction perpendicular to the first lateral direction.

7. The 3D memory device of claim 5, further comprising a plurality of dummy channel structures surrounding the staircase contact, each dummy channel structure extending vertically through the staircase structure.

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8. A three-dimensional (3D) memory device, comprising:

a substrate;

a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;

a staircase structure on one side of the memory stack;

an array of dummy channel structures each extending vertically through the staircase structure; and

a plurality of dummy source structures each extending vertically through the staircase stack, wherein a subset of the dummy channel structures is surrounded by the plurality of dummy source structures.

9. The 3D memory device of claim 8, wherein at least one dummy channel structure is surrounded by at least four dummy source structures.

10. The 3D memory device of claim 8, wherein at least two dummy channel structure are surrounded by at least six dummy source structures.

11. The 3D memory device of claim 8, wherein at least four dummy channel structures are surrounded by at least eight dummy source structures.

12. The 3D memory device of claim 8, wherein in a plan view, two dummy source structures and two dummy channel structures are aligned along a first row extending in a first lateral direction.

13. The 3D memory device of claim 12, wherein the two dummy source structures are separated by the two dummy channel structure.

14. The 3D memory device of claim 12, wherein the two dummy source structures are separated by one of the two dummy channel structure.

15. A method for forming a three-dimensional (3D) memory device, comprising:

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forming a dielectric stack comprising interleaved sacrificial layers and dielectric layers on a substrate;

forming a staircase structure on at least one side of the dielectric stack;

forming a plurality of dummy channel holes and a plurality of dummy source holes extending vertically through the staircase structure, wherein a subset of the dummy channel holes is surrounded by the plurality of dummy source holes;

forming a dummy channel structure in each of the plurality of dummy channel holes;

forming interleaved conductive layers and dielectric layers in the staircase structure by replacing, through the dummy source holes, the sacrificial layers in the staircase structure with the conductive layers;

forming a spacer along a sidewall of each of the plurality of dummy source holes to cover the conductive layers in the staircase structure; and

forming a contact within the spacer in each of the plurality of dummy source holes.

16. The method of claim 15, wherein forming the plurality of dummy channel holes and the plurality of dummy source holes comprises performing a patterning process to simultaneously form the plurality of dummy channel holes and the plurality of dummy source holes through the staircase structure.

17. The method of claim 15, further comprising:

forming a plurality of channel holes through the dielectric stack simultaneously with forming the plurality of dummy channel holes and the plurality of dummy source holes through the staircase structure.

18. The method of claim 15, further comprising:

forming a sealing layer in each of the dummy source holes;

after forming the sealing layer in each of the dummy source holes, forming a plurality of channel structures; and

after forming the plurality of channel structures, removing the sealing layer from each of the dummy source holes.

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19. The method of claim 18, wherein replacing, through the dummy source holes, the sacrificial layers in the staircase structure with the conductive layers comprises:

removing the sacrificial layers in the staircase structure through each of the dummy source holes after forming the plurality of channel structures to form a plurality of lateral recesses; and

depositing a conductive material to fill up the plurality of lateral recesses.

20. The method of claim 15, further comprising forming a plurality of recesses abutting a sidewall of each of the dummy source holes prior to forming the spacer.

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THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is continuation of International Application No. PCT/CN2019/076186, filed on February 26, 2019, entitled "THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME," which is hereby incorporated by reference in its entirety.

BACKGROUND

[0002] Embodiments of the present disclosure relate to three-dimensional (3D) memory devices and fabrication methods thereof.

[0003] Planar memory cells are scaled to smaller sizes by improving process technology, circuit design, programming algorithm, and fabrication process. However, as feature sizes of the memory cells approach a lower limit, planar process and fabrication techniques become challenging and costly. As a result, memory density for planar memory cells approaches an upper limit.

[0004] A 3D memory architecture can address the density limitation in planar memory cells. The 3D memory architecture includes a memory array and peripheral devices for controlling signals to and from the memory array.

SUMMARY

[0005] Embodiments of 3D memory devices and methods for forming the same are disclosed herein.

[0006] In one example, a 3D memory device is provided. The 3D memory device includes a substrate, a memory stack including interleaved conductive layers and dielectric layers on the substrate, and a staircase structure on one side of the memory stack. The 3D memory device also includes a staircase contact in the staircase structure. The 3D memory device further includes a plurality of dummy source structures each extending vertically through the staircase structure. The plurality of dummy source structures surround the staircase contact.

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[0007] In another example, a 3D memory device is provided. The 3D memory device includes a substrate, a memory stack including interleaved conductive layers and dielectric layers on the substrate, and a staircase structure on one side of the memory stack. The 3D memory device also includes an array of dummy channel structures each extending vertically through the staircase structure. The 3D memory device further includes a plurality of dummy source structures each extending vertically through the staircase stack. A subset of the dummy channel structures is surrounded by the plurality of dummy source structures.

[0008] In a further example, a method for forming a 3D memory device is provided. The method includes forming a dielectric stack including interleaved sacrificial layers and dielectric layers on a substrate. The method also includes forming a staircase structure on at least one side of the dielectric stack. The method further includes forming a plurality of dummy channel holes and a plurality of dummy source holes extending vertically through the staircase structure. A subset of the dummy channel holes is surrounded by the plurality of dummy source holes. The method also includes forming a dummy channel structure in each of the plurality of dummy channel holes and forming interleaved conductive layers and dielectric layers in the staircase structure by replacing, through the dummy source holes, the sacrificial layers in the staircase structure with the conductive layers. In addition, the method includes forming a spacer along a sidewall of each of the plurality of dummy source holes to cover the conductive layers in the staircase structure and forming a contact within the spacer in each of the plurality of dummy source holes.

[0009] In yet another example, a method for forming a 3D memory device is provided. The method includes alternatingly depositing interleaved sacrificial layers and dielectric layers on a substrate. The method also includes forming a staircase structure on at least one side of the interleaved sacrificial layers and dielectric layers. The method also includes simultaneously etching through the staircase structure to form a plurality of dummy channel holes and a plurality of dummy source holes. The plurality of dummy source holes are aligned with a portion of the plurality of dummy channel holes in a row along a lateral direction in a plan view. The method also includes depositing a sealing layer in each of the plurality of dummy source holes and each of the plurality of dummy channel holes. The method also includes etching away the sealing layer in each of the dummy source holes. In addition, the method includes replacing, through the dummy source holes, the sacrificial layers in the staircase

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structure with a plurality of conductive layers and depositing a spacer along a sidewall of each of the dummy source holes.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.

[0011] FIGS. 1A-1C illustrate plan views of exemplary 3D memory devices, according to some embodiments of the present disclosure.

[0012] FIG. 1D illustrates a cross-sectional view of the 3D memory device shown in FIG. 1A along an A-A' direction, according to some embodiments of the present disclosure.

[0013] FIGS. 2A–2L illustrate an exemplary fabrication process for forming a 3D memory device, according to some embodiments of the present disclosure.

[0014] FIG. 3 illustrates a flowchart of an exemplary method for forming a 3D memory device, according to some embodiments of the present disclosure.

[0015] FIG. 4 illustrates a flowchart of another exemplary method for forming a 3D memory device, according to some embodiments of the present disclosure.

[0016] FIG. 5 illustrates a plan view of an exemplary 3D memory device having gate line slits.

[0017] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

[0018] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.

[0019] It is noted that references in the specification to "one embodiment," "an embodiment," "an example embodiment," "some embodiments," etc., indicate that the

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embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to affect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0020] In general, terminology may be understood at least in part from usage in context. For example, the term "one or more" as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as "a," "an," or "the," again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term "based on" may be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0021] It should be readily understood that the meaning of "on," "above," and "over" in the present disclosure should be interpreted in the broadest manner such that "on" not only means "directly on" something but also includes the meaning of "on" something with an intermediate feature or a layer therebetween, and that "above" or "over" not only means the meaning of "above" or "over" something but can also include the meaning it is "above" or "over" something with no intermediate feature or layer therebetween (i.e., directly on something).

[0022] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0023] As used herein, the term "substrate" refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the

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substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0024] As used herein, the term "layer" refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which interconnect lines and/or via contacts are formed) and one or more dielectric layers.

[0025] As used herein, the term "nominal/nominally" refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term "about" indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term "about" can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., ±10%, ±20%, or ±30% of the value).

[0026] As used herein, the term "3D memory device" refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as "memory strings," such as NAND memory strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term "vertical/vertically" means nominally perpendicular to the lateral surface of a substrate.

[0027] In 3D memory fabrication processes, a gate-replacement process is often used to form interleaved word line/dielectric stacks, in which sacrificial layers are replaced with conductive layers to form gate electrodes/word lines. Dummy channel structures (e.g., formed

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by filling dummy channel holes with dielectric materials) can be used in staircase structures of a 3D memory device to prevent oxide layer bending. As 3D memory devices continue to scale down, the gate-replacement process can become more challenging. For example, in some 3D memory devices such as charge trap 3D NAND memory devices, gate line slits (GLSs) are formed to divide an array of memory strings (e.g., in the inner region of a 3D memory device) and/or dummy channel structures (e.g., in the staircase region of the 3D memory device) into different memory regions. Often, a GLS has large dimensions and is filled with an insulation structure formed in a trench that extends laterally in the array. The gate-replacement process in such a 3D memory device often includes etching away the sacrificial layers and depositing a conductive material through the trench. Using GLSs to perform the gate-replacement process has drawbacks. For example, in the staircase region, the large lateral distance between adjacent GLSs can cause conductive material to be unevenly filled in the lateral recesses formed after the removal of the sacrificial layers, resulting in voids in the formed gate electrodes. The gate electrode may have an undesirably high resistance. Also, because dummy channel holes are formed between adjacent GLSs, the boundary conditions for the etching of dummy channel holes at different locations can be different due to the existence of large-area GLSs, causing dummy channel holes to have nonuniform lateral dimensions. For example, the lateral dimensions of a dummy channel hole may gradually vary as the dummy channel hole moves farther away from the GLSs, causing potential performance variation of the memory cells. In addition, the large areas occupied by the GLSs limit the usable space on the wafer surface to place other components, such as staircase contacts.

[0028] For example, FIG. 5 illustrates a plan view of an exemplary 3D memory device 500 having GLSs 504. 3D memory device 500 includes an array of NAND memory strings 502 in an inner region 510, an array of dummy channel structures 506 in a staircase region 520, and multiple parallel GLSs 504, which divide arrays of NAND memory strings 502 and dummy channel structures 506 into different memory regions (e.g., memory fingers or blocks). As shown in FIG. 5, each GLS 504 extends laterally along the word line direction in a straight-line pattern in the plan view (parallel to the wafer plane). It is noted that x and y axes are included in FIG. 5 to illustrate two orthogonal directions in the wafer plane. The x-direction is the word line direction, and the y-direction is the bit line direction. 3D memory device 500 also includes staircase contacts 508 for forming word line contacts in the staircase structure.

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[0029] During the gate replacement processes, conductive materials for forming the gate electrodes need to travel a relatively long distance between adjacent GLSs 504 to fill in the lateral recesses formed after the removal of sacrificial layers. This deposition process can be susceptible to formation of voids and/or nonuniformly deposited gate electrodes. Further, the shape of GLS 504 (e.g., having a slit shape with a dimension along the extending direction (or the *x*-direction) much greater than the dimension along the expanding dimension (or the *y*-direction)) can contribute to unbalanced variations of wafer flatness (e.g., wafer warpage bias) in different directions. The warpage bias can have an adverse impact on the photolithography process to form device patterns, leading to potential die yield loss.

[0030] Various embodiments in accordance with the present disclosure provide an improved 3D memory structure scheme suitable for solving the aforementioned issues by replacing the GLSs with dummy source structures. The 3D memory structure includes a plurality of dummy source structures distributed in the array of dummy channel structures and/or staircase contacts in the staircase region. Each dummy source structure may include an insulating spacer layer in a dummy source hole and a conductive contact within the spacer layer. In some embodiments, one or more dummy source structures are in contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices. The dummy source structures may be arranged in a pattern, e.g., an array, so the dummy source structures can be uniformly distributed in the staircase structure. The arrangement of the dummy source structures may improve the uniformity and stability for etching dummy channel holes in the staircase region.

[0031] Also, the arrangement of the dummy source structures may allow the gate electrodes/word lines to be formed with improved uniformity and quality, reducing the resistivity of the gate electrodes/word lines. For example, the gate-replacement process can be performed to deposit a conductive material through the dummy source holes that subsequently form the dummy source structures. Because the conductive material travels shorter distances to fill up the lateral recesses for forming the gate electrodes, the gate electrodes are less susceptible to voids or density nonuniformity.

[0032] In the present disclosure, the dummy source holes, which can have the same diameter as the dummy channel holes, can be formed by the same process that forms the dummy channel holes, so the formation of the dummy source holes has minimal impact on the lateral uniformity of dummy channel holes. Further, both the dummy channel holes and the

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dummy source holes in the staircase region can be formed by the same process that forms the channel holes in the inner region. The etching process to form the channel holes may further result in channel holes with more uniform diameters. Meanwhile, the number of dummy channel holes formed in the staircase region can be flexibly determined, e.g., based on design and/or fabrication requirements.

[0033] FIGS. 1A-1C illustrate plan views of exemplary 3D memory devices, according to some embodiments. FIG. 1D illustrates a cross-sectional view of the 3D memory device shown in FIG. 1A. FIGS. 2A-2L illustrate cross-sectional views of the exemplary 3D memory device at various stages of an exemplary fabrication process, according to some embodiments. FIGS. 3 and 4 each illustrates an exemplary method to form a 3D memory device, according to some embodiments.

[0034] FIG. 1A illustrates a plan view of an exemplary 3D memory device 100. 3D memory device 100 may include a memory region 150. Memory region 150 may include an inner region 116 (also known as a "core array region") and an outer region 118 (also known as a "staircase region"). In some embodiments, inner region 116 is the center region of memory region 150 where an array of memory strings 104 (e.g., NAND memory strings) are formed, and outer region 118 is the remaining region of memory region 150 surrounding inner region 116 (including the sides and edges) without memory strings 104.

[0035] Memory strings 104 may be arranged in an array in inner region 116. Memory strings 104 may be arranged in any suitable pattern. Depending on the fabrication and/or design requirements, any suitable number of memory strings 104 may be formed in inner region 116.

[0036] Staircase region 118 may include a plurality of staircase contacts 122, a plurality of dummy channel structures 124, and a plurality of dummy source structures 126 distributed among dummy channel structures 124 and staircase contacts 122. Staircase contacts 122, dummy channel structures 124, and/or dummy source structures 126 may be arranged in any suitable pattern, such as an array, in staircase region 118. As shown in FIG. 1A, multiple dummy source structures, such as the four dummy source structures indicated by a diamond shape 146, may surround a staircase contact, such as staircase contact 122. The four dummy source structures indicated by 146 may be located adjacent to staircase contact 122 (e.g., there is no other components such as dummy channel structures, dummy source structures, and staircase contacts between staircase contact 122 and each of the four dummy source structures. The four dummy source structures indicated by 146 may be spaced with nominally equal lateral

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distances to staircase contact 122. In other words, the four dummy source structures indicated by 146 may be evenly or uniformly distributed around staircase contact 122.

[0037] As shown in FIG. 1A, at least two dummy source structures may be arranged in a first row 132 that extends along a first lateral direction (e.g., *x* direction). For example, row 132 includes two dummy source structures. Another two dummy source structures may be arranged in a second row 134 that extends along a second lateral direction (e.g., *y* direction) that is perpendicular to the first lateral direction (e.g., *x* direction). For example, row 134 includes two dummy source structures.

[0038] A plurality of dummy channel structures, such as the four dummy channel structures indicated by square shape 148, may surround a staircase contact. The four dummy channel structures may be spaced with nominally equal lateral distances to the staircase contact, as shown in FIG. 1A. In other words, the dummy channel structures surrounding a staircase contact may be evenly distributed around the staircase contact.

[0039] In some embodiments, at least two of the plurality of dummy channel structures may be arranged in a third row 136 that extends along a third lateral direction in parallel with the first or the second lateral direction. For example, row 136 includes four dummy channel structures (two in the center and two others at both ends). Row 136 is in parallel to the *y* direction, in parallel to row 134, as shown in FIG. 1A.

[0040] The plurality of dummy source structures may interleave with the plurality of dummy channel structures. For example, the dummy source structures may be arranged among the array of dummy channel structures, where one or more dummy channel structures may be located between two dummy source structures, and vice versa.

[0041] In some embodiments, at least one dummy source structure may be located between two staircase contacts. For example, FIG. 1A shows that two dummy source structures are located between staircase contacts 122 and 122'. FIG. 1B shows another embodiment in which two dummy source structures are located between staircase contacts 123 and 123', while one dummy source structure is located between staircase contacts 123' and 123". FIG. 1C shows yet another embodiment in which one dummy source structure is located between staircase contacts 125 and 125', and one dummy source structure is located between stair case contacts 125' and 125". Other numbers of dummy source structures may also be disposed between two staircase contacts.

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[0042] In some embodiments, a subset of the dummy channel structures may be surrounded by a plurality of dummy source structures. Referring to FIG. 1A, four dummy channel structures indicated by dashed-line square shape 142 are surrounded by eight dummy source structures indicated by an octagon 144. In the embodiment shown in FIG. 1B, two dummy channel structures indicated by dashed-line rectangular shape 143 are surrounded by six dummy source structures indicated by a hexagon 145. In the embodiment shown in FIG. 1C, one dummy channel structure indicated by dashed-line square shape 147 is surrounded by four dummy source structures indicated by a diamond 149. Any suitable number of dummy channel structures may be surrounded by any suitable number of dummy source structures.

[0043] In some embodiments, two dummy source structures and two dummy channel structures may be aligned along a first row extending in a first lateral direction. For example, as shown in FIG. 1A, row 132 includes two dummy channels structures and two dummy source structures aligned along the *x* direction. The two dummy source structures are separated by the two dummy channel structure. In another example, as shown in FIG. 1B, two dummy source structures are separated by one dummy channel structure in row 133, while row 133 includes two dummy channel structures and two dummy source structures aligned along the *x* direction. Returning back to FIG. 1A, two other dummy source structures and two other dummy channel structures are aligned along a second row 134 extending in the *y* direction perpendicular to the *x* direction. Row 132 and row 134 cross each other at a dummy channel structure, as shown in FIG. 1A.

[0044] While FIGS. 1A-1C illustrate certain exemplary arrangements of dummy source structures and dummy channel structures, it is noted that dummy source structures 126 and/or dummy channel structures 124 may be distributed or arranged in any suitable arrangement in staircase region 118. For example, dummy source structures 126 may be arranged in a pattern (e.g., arrangement with a same shape repeated at a regular interval) in the plan view. In some embodiments, dummy source structures 126 are arranged in an array.

[0045] In some embodiments, the number of dummy source structures 126 in each row and the number/arrangement of dummy channel structures 124 aligned with dummy source structure 126 may vary. For example, in a row, each two adjacent dummy source structures 126 may be separated by more or less than two dummy channel structures. In some embodiments, the number of dummy source structures surrounding one or more dummy channel structure 124 may be more or less than eight, six, or four. The lateral dimensions (e.g.,

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diameter) of a dummy source structure 126 may be nominally the same as the lateral dimensions (e.g., diameter) of dummy channel structure 124 and/or memory string 104. The specific arrangement of dummy source structures 126 and dummy channel structure 124 may be determined based on different fabrication and/or design requirements, and should not be limited by the embodiments of the present disclosure.

[0046] The arrangement of dummy source structures 126 may improve the fabrication and device performance of 3D memory device 100 in many aspects. For example, by removing GLSs from the staircase region 118, more space is available for other structures such as staircase contacts 122. The dummy source structures 126 are distributed amongst dummy channel structures 124 and also surround staircase contacts 122 of nominally same lateral distances to the respective staircase contacts 122. In the gate-replacement process, conductive material for forming the gate electrodes may travel nominally same distances to surrounding lateral recesses formed after the removal of sacrificial layers. This may facilitate the gate electrodes to be formed with improved uniformity and quality, reducing the resistivity of the gate electrodes. The arrangement of dummy source structures 126 also allows more staircase contacts to be located closer and more uniformly. Also, the arrangement and dimensions of the dummy source structures 126 can result in a reduced change of boundary conditions of dummy channel holes at different locations in staircase region 118 during the etching process. The lateral dimensions of the formed dummy channel holes may thus have improved uniformity. Further, the number of dummy channel structures may be flexibly determined in staircase region 118. This may further increase the stability of staircase region 118 during etching processes. The lateral dimensions and distribution of dummy source structures 126 may also reduce warpage bias of 3D memory device 100, thus reducing the variations to the surface flatness of 3D memory device 100. The symmetrical architecture of dummy channel structures and dummy source structures can improve the performance and efficiency of etching processes. Different layouts, patterns, and designs may be adopted based on the size of the staircase region.

[0047] FIG. 1D illustrates a cross-sectional view of an exemplary 3D memory device 100 along the A-A' direction shown in FIG. 1A, according to some embodiments of the present disclosure. 3D memory device 100 can include a substrate 102, which can include silicon (e.g., single crystalline silicon), silicon germanium (SiGe), gallium arsenide (GaAs), germanium (Ge), silicon on insulator (SOI), germanium on insulator (GOI), or any other suitable materials.

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In some embodiments, substrate 102 is a thinned substrate (e.g., a semiconductor layer), which was thinned by grinding, etching, chemical mechanical polishing (CMP), or any combination thereof.

[0048] 3D memory device 100 can include memory array devices above substrate 102. It is noted that *x* and *z* axes/directions are included in FIG. 1D to further illustrate the spatial relationship of the components in 3D memory device 100. Substrate 102 includes two lateral surfaces extending laterally in the *x*-*y* plane: a top surface on the front side of the wafer on which 3D memory device 100 can be formed, and a bottom surface on the backside opposite to the front side of the wafer. The *z* axis is perpendicular to both the *x* and *y* axes. As used herein, whether one component (e.g., a layer or a device) is "on," "above," or "below" another component (e.g., a layer or a device) of a semiconductor device (e.g., 3D memory device 100) is determined relative to the substrate of the semiconductor device (e.g., substrate 102) in the *z*-direction (the vertical direction perpendicular to the *x*-*y* plane) when the substrate is positioned in the lowest plane of the semiconductor device in the *z*-direction. The same notion for describing spatial relationship is applied throughout the present disclosure.

[0049] 3D memory device 100 can be part of a monolithic 3D memory device. The term "monolithic" means that the components (e.g., the peripheral device and memory array device) of the 3D memory device are formed on a single substrate. For monolithic 3D memory devices, the fabrication encounters additional restrictions due to the convolution of the peripheral device processing and the memory array device processing. For example, the fabrication of the memory array device (e.g., NAND memory strings) is constrained by the thermal budget associated with the peripheral devices that have been formed or to be formed on the same substrate.

[0050] Alternatively, 3D memory device 100 can be part of a non-monolithic 3D memory device, in which components (e.g., the peripheral device and memory array device) can be formed separately on different substrates and then bonded, for example, in a face-to-face manner. In some embodiments, the memory array device substrate (e.g., substrate 102) remains as the substrate of the bonded non-monolithic 3D memory device, and the peripheral device (e.g., including any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of 3D memory device 100, such as page buffers, decoders, and latches, not shown) is flipped and faces down toward the memory array device (e.g., NAND memory strings) for hybrid bonding. It is understood that in some embodiments, the memory array

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device substrate (e.g., substrate 102) is flipped and faces down toward the peripheral device (not shown) for hybrid bonding, so that in the bonded non-monolithic 3D memory device, the memory array device is above the peripheral device. The memory array device substrate (e.g., substrate 102) can be a thinned substrate (which is not the substrate of the bonded non-monolithic 3D memory device), and the back-end-of-line (BEOL) interconnects of the non-monolithic 3D memory device can be formed on the backside of the thinned memory array device substrate.

[0051] In some embodiments, 3D memory device 100 is a NAND Flash memory device in which memory cells are provided in the form of an array of NAND memory strings 104 each extending vertically above substrate 102. The NAND memory strings 104 can extend through a plurality of pairs each including a conductive layer 106 and a dielectric layer 108 (referred to herein as "conductor/dielectric layer pairs"). The stacked conductor/dielectric layer pairs are also referred to herein as a "memory stack" 160. In some embodiments, an insulation layer (not shown) is formed between substrate 102 and memory stack 160. The number of the conductor/dielectric layer pairs in memory stack 160 (e.g., 32, 64, 96, or 128) determines the number of memory cells in 3D memory device 100. Memory stack 160 can include interleaved conductive layers 106 and dielectric layers 108. At least on one side in the lateral direction, memory stack 160 can include a staircase structure 175. Conductive layers 106 and dielectric layers 108 in memory stack 160 can alternate in the vertical direction. Conductive layers 106 can include conductive materials including, but not limited to, tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), polysilicon, doped silicon, silicides, or any combination thereof. Dielectric layers 108 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.

[0052] As shown in FIG. 1D, memory string 104 can include a channel structure 162 extending vertically through memory stack 160. Channel structure 162 can include a channel hole filled with semiconductor materials (e.g., as a semiconductor channel 164) and dielectric materials (e.g., as a memory film 166). In some embodiments, semiconductor channel 164 includes silicon, such as amorphous silicon, polysilicon, or single crystalline silicon. In some embodiments, memory film 166 is a composite layer including a tunneling layer, a storage layer (also known as a "charge trap layer"), and a blocking layer. The remaining space of the channel hole of channel structure 162 can be partially or fully filled with a capping layer 168 including dielectric materials, such as silicon oxide. Channel structure 162 can have a cylinder

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shape (e.g., a pillar shape). Capping layer 168, semiconductor channel 164, the tunneling layer, the storage layer, and the blocking layer are arranged radially from the center toward the outer surface of the pillar in this order, according to some embodiments. The tunneling layer can include silicon oxide, silicon oxynitride, or any combination thereof. The storage layer can include silicon nitride, silicon oxynitride, silicon, or any combination thereof. The blocking layer can include silicon oxide, silicon oxynitride, high dielectric constant (high-k) dielectrics, or any combination thereof. In one example, memory film 166 can include a composite layer of silicon oxide/silicon oxynitride (or silicon nitride)/silicon oxide (ONO).

[0053] In some embodiments, conductive layer 106 in memory stack 160 functions as a gate electrode/gate conductor/gate line of memory cells in memory string 104. Conductive layer 106 can include multiple control gates of multiple NAND memory cells and can extend laterally as a word line ending at the edge of memory stack 160 (e.g., in staircase structure 175 of memory stack 160). In some embodiments, the word lines extend in the *x*-direction perpendicular to both the *y*-direction and *z*-direction. The bit lines extend in the *y*-direction perpendicular to both the *x*-direction and *z*-direction. In some embodiments, memory cell transistors in memory string 104 include gate conductors (e.g., parts of conductive layers 106 that abut channel structure 162) made from tungsten, adhesion layers (not shown) including titanium/titanium nitride (Ti/TiN) or tantalum/tantalum nitride (Ta/TaN), gate dielectric layers (not shown) made from high-k dielectric materials, and channel structure 162.

[0054] In some embodiments, memory string 104 further includes a semiconductor plug 170 in the lower portion (e.g., at the lower end) of memory string 104. As used herein, the "upper end" of a component (e.g., memory string 104) is the end farther away from substrate 102 in the *z*-direction, and the "lower end" of the component (e.g., memory string 104) is the end closer to substrate 102 in the *z*-direction when substrate 102 is positioned in the lowest plane of 3D memory device 100. Semiconductor plug 170 can include a semiconductor material, such as silicon, which is epitaxially grown from substrate 102 in any suitable directions. It is understood that in some embodiments, semiconductor plug 170 includes single crystalline silicon, the same material of substrate 102. In other words, semiconductor plug 170 can include an epitaxially-grown semiconductor layer that is the same as the material of substrate 102. In some embodiments, part of semiconductor plug 170 is over the top surface of substrate 102 and in contact with semiconductor channel 164. Semiconductor plug 170 can function as a channel controlled by a source select gate of memory string 104.

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[0055] In some embodiments, memory string 104 further includes a channel plug 172 in the upper portion (e.g., at the upper end) of memory string 104. Channel plug 172 can be in contact with the upper end of semiconductor channel 164. Channel plug 172 can include semiconductor materials (e.g., polysilicon) or conductive materials (e.g., metals). In some embodiments, channel plug 172 includes an opening filled with Ti/TiN or Ta/TaN as an adhesion layer and tungsten as a conductor layer. By covering the upper end of channel structure 162 during the fabrication of 3D memory device 100, channel plug 172 can function as an etch stop layer to prevent etching of dielectrics filled in channel structure 162, such as silicon oxide and silicon nitride. In some embodiments, channel plug 172 also functions as the drain of memory string 104.

[0056] In some embodiments, 3D memory device 100 further includes dummy channel structures 180. Each dummy channel structure 180 extends vertically through staircase structure 175. Dummy channel structure 180 may include dielectric materials such as silicon-oxide. In some embodiments, dummy channel structure 180 may reach substrate 102 and in contact with substrate 102. Dummy channel structure 180 may have nominally the same diameter as the diameter of channel structure 162.

[0057] In some embodiments, 3D memory device 100 further includes dummy source structures 178. Each dummy source structure 178 can extend vertically through staircase structure 175. In some embodiments, dummy source structure 178 includes a dummy source hole filled with conductive materials as a contact 179. Dummy source structure 178 can further include a spacer 177 made of any suitable dielectric materials (e.g., silicon oxide) between contact 179 and memory stack 160 to electrically separate surrounding conductive layers 106 in memory stack 160 from contact 179. As a result, dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks. In some embodiments, dummy source structures 178 may function as interconnects to connect 3D memory device 100 with other peripheral devices.

[0058] As described below in detail, due to the limitations of etching process (e.g., deep reactive ion etch (DRIE)) for forming the dummy source hole, in particular when the levels of memory stack 160 continue to increase, the sidewall profile of the dummy source hole is not straight up as shown in FIG. 1D, but rather being tilted. In some embodiments, the lateral dimension of the dummy source hole (and dummy source structure 178) decreases from top to

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bottom. That is, the lateral dimension of dummy source structures 178 in its upper portion can be greater than the lateral dimension in its lower portion.

[0059] FIGS. 2A–2L illustrate an exemplary fabrication process for forming a 3D memory device, according to some embodiments of the present disclosure. FIG. 3 illustrates a flowchart of an exemplary method 300 for forming a 3D memory device, according to some embodiments of the present disclosure. FIG. 4 illustrates a flowchart of another exemplary method 400 for forming a 3D memory device, according to some embodiments of the present disclosure. Examples of the 3D memory device depicted in FIGS. 2A–2L and 3-4 include 3D memory device 100 depicted in FIGS. 1A-1D. FIGS. 2A–2L and 3-4 will be described together. It is understood that the operations shown in methods 300 and 400 are not exhaustive and that other operations can be performed as well before, after, or between any of the illustrated operations. Further, some of the operations may be performed simultaneously, or in a different order than shown in FIGS. 3-4.

[0060] Referring to FIG. 3, method 300 starts at operation 302, in which a dielectric stack is formed on a substrate and a staircase structure is formed on at least one side of the dielectric stack. The substrate can be a silicon substrate. The dielectric stack can include interleaved sacrificial layers and dielectric layers. In the example of method 400 in FIG. 4, at operation 402, interleaved sacrificial layers and dielectric layers are alternatingly deposited on a substrate and a staircase structure on at least one side of the interleaved sacrificial layers and dielectric layers.

[0061] Referring to FIG. 2A, a dielectric stack 204 including a plurality pairs of a first dielectric layer (also known as a "sacrificial layer" 206) and a second dielectric layer 208 (together referred to herein as "dielectric layer pairs") are formed on a silicon substrate 202. That is, dielectric stack 204 includes interleaved sacrificial layers 206 and dielectric layers 208, according to some embodiments. Dielectric layers 208 and sacrificial layers 206 can be alternatingly deposited on silicon substrate 202 to form dielectric stack 204. In some embodiments, each dielectric layer 208 includes a layer of silicon oxide, and each sacrificial layer 206 includes a layer of silicon nitride. Dielectric stack 204 can be formed by one or more thin film deposition processes including, but not limited to, chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), or any combination thereof. In some embodiments, an insulation layer (not shown) is formed between silicon substrate 202

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and dielectric stack 204 by depositing dielectric materials, such as silicon oxide, on silicon substrate 202.

[0062] As illustrated in FIG. 2A, staircase structures 203 are formed on the sides of dielectric stack 204. Staircase structure 203 can be formed by the so-called "trim-etch" processes, which, in each cycle, trim (e.g., etching incrementally and inwardly, often from all directions) a patterned photoresist layer, followed by etching the exposed portions of the dielectric/sacrificial layer pair using the trimmed photoresist layer as an etch mask to form one step of staircase structure 203.

[0063] Method 300 proceeds to operation 304, as illustrated in FIG. 3, in which a plurality of dummy channel holes and a plurality of dummy source holes are formed through the staircase structure. In the example of method 400 in FIG. 4, at operation 404, a plurality of dummy channel holes and a plurality of dummy source holes are formed through the interleaved sacrificial layers and dielectric layers in the staircase structure. The plurality of dummy channel holes and a plurality of dummy source holes can be simultaneously formed through the staircase structure by, e.g., performing an anisotropic etching process to remove portions of staircase structure using an etch mask. In addition, the plurality of dummy channel holes and the plurality of dummy source holes can be simultaneously formed with the channel holes in the dielectric stack by the same etching process. The plurality of dummy source holes may be aligned with a portion of the plurality of dummy channel holes in a row along a lateral direction (e.g., *x* direction). A subset of the dummy channel holes may be surrounded by a plurality of dummy source holes.

[0064] As illustrated in FIG. 2A, a plurality of dummy channel holes 210 and dummy source holes 212 are simultaneously formed through staircase structure 203. A plurality of channel holes 211 may also be simultaneously formed through an inner region of dielectric stack 204. In some embodiments, an etching mask (not shown) is patterned on dielectric stack 204 by photolithography, development, and etching. The etching mask can be a photoresist mask or a hard mask patterned based on a photolithography mask. The photolithography mask and/or etching mask can have patterns of dummy channel holes 210, dummy source holes 212, and/or channel holes 211 thereon. In some embodiments, the etching mask includes an array of first openings for forming dummy channel holes 210 and second openings for forming dummy source holes 212. The first openings and the second openings may have nominally same lateral dimensions (e.g., diameters). In some embodiments, dummy channel holes 210

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and dummy source holes 212 have nominally same lateral dimensions (e.g., diameters). In some embodiments, dummy channel holes 210, dummy source holes 212, and channel holes 211 have nominally same lateral dimensions (e.g., diameters).

[0065] As illustrated in FIG. 2A, parts of dielectric stack 204 are etched through by one or more wet etching and/or dry etching processes, such as DRIE, using the patterned etching mask to simultaneously form dummy channel holes 210 and dummy source holes 212 in a pattern defined by the photolithography mask and/or etching mask. In some embodiments, dummy channel holes 210 and dummy source holes 212 extend vertically further into the upper portion of silicon substrate 202. The etching process through dielectric stack 204 may not stop at the top surface of silicon substrate 202 and may continue to etch part of silicon substrate 202. In some embodiments, a separate etching process is used to etch part of silicon substrate 202 after etching through dielectric stack 204. In some embodiments, the lateral dimensions (e.g., diameter D1) of dummy channel hole 210 are nominally the same as the lateral dimensions (e.g., diameter D2) of dummy source hole 212, and may also be nominally the same as the lateral dimensions (e.g., diameter D3) of channel hole 211.

[0066] Method 300 proceeds to operation 306, as illustrated in FIG. 3, in which a dummy channel structure is formed in each of the dummy channel holes. In the example of method 400 in FIG. 4, at operation 406, a sealing layer is formed in each of the dummy source holes. In some embodiments, a channel structure is formed in each of the channel hole. A semiconductor plug is formed in the lower portion of each of the channel holes, and a channel plug is formed in the upper portion of each of the channel holes.

[0067] As illustrated in FIG. 2B, a sealing layer 214 is formed to fill in and cover dummy channel holes 210, dummy source holes 212, and channel hole 211. Sealing layer 214 can be formed by depositing a sacrificial layer, such as polysilicon, which is to be later removed, to partially fill in and cover channel holes 211 and dummy source holes 212 using one or more thin film deposition processes including ALD, CVD, PVD, any other suitable processes, or any combination thereof. In some embodiments, sealing layer 214 is formed by a rapid-sealing deposition process. Dummy channel structures 209 are formed with dummy channel holes 210 filled with sealing layer 214.

[0068] After sealing layer 214 is formed, channel hole 211 is re-opened. As illustrated in FIG. 2C, a photoresist layer 216 (as a channel hole re-open mask) is patterned to cover part of sealing layer 214 right above dummy channel holes 210 and dummy source hole 212 using

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photolithography and development processes. As illustrated in FIG. 2D, parts of sealing layer 214 right above channel hole 211 are removed using wet etching and/or dry etching processes since they are not covered by photoresist layer 216, leaving sealing layer 214 to fill in and cover only dummy source hole 212 and dummy channel holes 210. Channel hole 211 are thereby re-opened for later processes.

[0069] As illustrated in FIG. 2E, a semiconductor plug 222 is formed by filling the lower portion of channel hole 211 (shown in FIG. 2D) with a semiconductor material (e.g., single crystalline silicon epitaxially grown from silicon substrate 202 or polysilicon deposited over silicon substrate 202) in any suitable directions (e.g., from bottom surface and/or side surface). The fabrication processes for epitaxially growing semiconductor plug 222 can include, but not limited to, vapor-phase epitaxy (VPE), liquid-phase epitaxy (LPE), molecular-beam epitaxy (MBE), or any combinations thereof.

[0070] As illustrated in FIG. 2E, a channel structure 220 is formed above semiconductor plug 222 in channel hole 211. Channel structure 220 can include a memory film 226 (e.g., including a blocking layer, a storage layer, and a tunneling layer) and a semiconductor channel 228 formed above semiconductor plug 222. In some embodiments, memory film 226 is first deposited along the sidewall and bottom surface of channel hole 211, and semiconductor channel 228 is then deposited over memory film 226 and above semiconductor plug 222. The blocking layer, storage layer, and tunneling layer can be sequentially deposited in this order using one or more thin film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof, to form memory film 226. Semiconductor channel 228 can then be deposited on the tunneling layer using one or more thin film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof. In some embodiments, a capping layer 229 is filled in the remaining space of channel hole 211 by depositing dielectric materials after the deposition of semiconductor channel 228, such as silicon oxide.

[0071] As illustrated in FIG. 2E, a channel plug 224 is formed in the upper portion of channel hole 211. In some embodiments, parts of memory film 226, semiconductor channel 228, and capping layer 229 on the top surface of dielectric stack 204 and in the upper portion of channel hole 211 can be removed by CMP, grinding, wet etching, and/or dry etching to form a recess in the upper portion of channel hole 211. Channel plug 224 then can be formed by depositing conductive materials, such as metals, into the recess by one or more thin film

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deposition processes, such as CVD, PVD, ALD, electroplating, electroless plating, or any combination thereof. A memory string 218 (e.g., a NAND memory strings) is thereby formed. In some embodiments, an insulation layer 230 including dielectric materials, such as silicon oxide, is formed on dielectric stack 204 after the formation of channel structures 220 of memory strings 218.

[0072] Method 400 proceeds to operation 408, as illustrated in FIG. 4, in which the sealing layer is removed from each of the dummy source holes after the formation of channel structures in channel holes. As illustrated in FIG. 2F, a photoresist layer 232 (as a dummy source hole re-open mask) is patterned to cover parts of insulation layer 230 right above memory strings 218 and dummy channel structures 209 using photolithography and development processes. As illustrated in FIG. 2G, part of insulation layer 230 right above dummy source hole 212 and sealing layer 214 that fills in and covers dummy source hole 212 (shown in FIG. 2F) are removed using wet etching and/or dry etching processes since they are not covered by photoresist layer 232 (shown in FIG. 2F). Dummy source holes 212 are thereby re-opened for later processes.

[0073] Method 300 proceeds to operation 308, as illustrated in FIG. 3, in which interleaved conductive layers and dielectric layers is formed in the staircase structure. In the example of method 400 in FIG. 4, at operation 410, a plurality of conductive layers is formed through the dummy source holes. In some embodiments, forming the interleaved conductive layers and dielectric layers includes etching the sacrificial layers in the dielectric stack, and depositing the conductive layers of the memory stack through the dummy source holes.

[0074] As illustrated in FIG. 2H, sacrificial layers 206 (shown in FIG. 2G) in dielectric stack 204 are removed by wet etching and/or dry etching selective to dielectric layers 208. Lateral recesses 234 connected to dummy source hole 212 can be formed after sacrificial layers 206 are completely etched away. In some embodiments, the etching process is facilitated by exposing dummy source hole 212 to hot phosphoric acid by which silicon nitride in sacrificial layers 206 is etched preferentially over silicon oxide in dielectric layers 208.

[0075] As illustrated in FIG. 2I, conductive layers 236 are formed along the sidewall of dummy source hole 212 and filling in lateral recesses 234 (shown in FIG. 2H). In some embodiments, conductive layer 236 is a composite layer including an adhesion layer and a conductor layer (e.g., a gate conductor/gate line). In some embodiments, a gate dielectric layer (not shown) is deposited prior to the deposition of conductive layer 236. The gate dielectric

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layer and conductive layer 236 can be formed by one or more thin film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof. The gate dielectric layer can include dielectric materials including silicon nitride, high-k dielectrics, or any combination thereof. Conductive layer 236 can include conductive materials including, but not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof. In some embodiments, the gate dielectric layer, adhesion layer, and conductor layer are each formed by CVD processes in which the reaction gases pass through dummy source hole 212 to lateral recesses 234 and are reacted and deposited along the sidewalls of dummy source hole 212 and lateral recesses 234. Conductive layers 236 thereby replace sacrificial layers 206 to transfer dielectric stack 204 into a memory stack 238.

[0076] As illustrated in FIG. 2J, recesses 240 abutting the sidewall of dummy source hole 212 are formed by etching parts of conductive layers 236 of memory stack 238 that abut the sidewall of dummy source hole 212. In some embodiments, recesses 240 are formed by applying etchants to conductive layers 236 through dummy source hole 212 to completely remove the part of conductive layer 236 along the sidewall of dummy source hole 212 and further etch parts of conductive layers 236 in lateral recesses 234 (shown in FIG. 2H). The dimension of recess 240 can be controlled by the etching rate (e.g., based on the etchant temperature and concentration) and/or etching time.

[0077] Method 300 proceeds to operation 310, as illustrated in FIG. 3, in which a spacer is formed along a sidewall of the dummy source hole to cover the conductive layers and electrically separate the conductive layers of the memory stack from a contact later formed in the dummy source hole. In the example of FIG. 4, at operation 412, a spacer is deposited along the sidewall of each of the dummy source holes. As illustrated in FIG. 2K, a spacer 242 is formed along the sidewall of dummy source hole 212 and in recesses 240 (shown in FIG. 2J) using one or more thin film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof. Spacer 242 can include a single or composite layer of dielectric materials, such as silicon oxide and silicon nitride. By covering the sidewall of the dummy source hole as well as filling in recesses 240 with spacer 242, conductive layers 236 (e.g., gate lines) of memory stack 238 can be electrically separated from a contact later formed in dummy source hole 212 by spacer 242.

[0078] Method 300 proceeds to operation 312, as illustrated in FIG. 3, in which a contact is formed within the spacer in the dummy source hole. In the example of method 400 in FIG.

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4, at operation 414, a contact is formed within the spacer in the dummy source hole. The contact may be electrically connected to other peripheral devices. The contact can be deposited over the spacer in each of the dummy source holes. As illustrated in FIG. 2L, a contact 244 is formed within spacer 242 in dummy source hole 212 (shown in FIG. 2K). Contact 244 can be formed by depositing conductive materials including, not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof, over spacer 242 in the dummy source hole using one or more thin film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof. A dummy source structure 246 including spacer 242 and contact 244 is thereby formed in the dummy source hole, surrounded by a plurality of dummy channel structures 209. In the inner region (e.g., inner region 116 shown in FIG. 1A), source structures may also be formed. Source structures formed in the inner region may be connected with surround channel structures (e.g., channel structure 220 of memory string 218 shown in FIG. 2E) via a common source, such as a doped region (not shown) in substrate 202. In some embodiments, dummy source structure 246 may not connect to channel structures in the inner region. Instead, dummy source structure 246 may be formed simultaneously with source structures in the inner region, while functioning as a mechanical supporting structure after gate-replacement process, without connecting to channel structures in the inner region. In some embodiments, dummy source structure 246 may not reach substrate 202. For example, dummy source structure 246 may be above substrate 202 while still reach the lower part of the dielectric stack to carry out the gate-replacement process.

[0079] In some embodiments, contact 244 may be formed simultaneously with word line contacts by filling conductive materials simultaneously to dummy source hole 212 and staircase contact 122 (shown in FIG. 1A). In this way, dummy source structures can be formed in the same processes of forming the word line contacts.

[0080] In some embodiments, after the gate-replacement process, dummy source hole 212 may be filled with dielectric materials without conductive materials. For example, when dummy source hole 212 is filled in a separate step from forming word line contact, any suitable materials can be used to form dummy source structure 246, including dielectric materials, conductive materials, or any combination thereof. When conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices. When

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dielectric materials are used to fill dummy source hole 212, dummy source structure 246 may function as a mechanical support structure to improve the stability of the staircase region.

[0081] In some embodiments, a 3D memory device includes a substrate, a memory stack comprising interleaved conductive layers and dielectric layers on the substrate, a staircase structure on one side of the memory stack, a staircase contact in the staircase structure, and a plurality of dummy source structures each extending vertically through the staircase structure. The plurality of dummy source structures surrounds the staircase contact.

[0082] In some embodiments, the plurality of dummy source structures are located adjacent to the staircase contact.

[0083] In some embodiments, at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact.

[0084] In some embodiments, the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact.

[0085] In some embodiments, in a plan view, at least two of the plurality of dummy source structures are arranged in a first row that extends along a first lateral direction.

[0086] In some embodiments, in the plan view, at least two other dummy source structures are arranged in a second row that extends along a second lateral direction perpendicular to the first lateral direction.

[0087] In some embodiments, the 3D memory device further includes a plurality of dummy channel structures surrounding the staircase contact, each dummy channel structure extending vertically through the staircase structure.

[0088] In some embodiments, the plurality of dummy channel structures are of nominally equal lateral distances to the staircase contact.

[0089] In some embodiments, in the plan view, the plurality of dummy source structures interleave with the plurality of dummy channel structures.

[0090] In some embodiments, in the plan view, at least two of the plurality of dummy channel structures are arranged in a third row that extends along a third lateral direction in parallel with the first or the second lateral direction.

[0091] In some embodiments, the 3D memory device further includes first and second staircase contacts, wherein at least one dummy source structure is located between the first and second staircase contacts.

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[0092] In some embodiments, at least two dummy source structures are located between the first and second staircase contacts.

[0093] In some embodiments, the plurality of dummy source structures are in contact with the substrate.

[0094] In some embodiments, the plurality of dummy source structures are not in contact with the substrate.

[0095] In some embodiments, a 3D memory device includes a substrate, a memory stack with interleaved conductive layers and dielectric layers on the substrate, a staircase structure on one side of the memory stack, an array of dummy channel structures each extending vertically through the staircase structure, and a plurality of dummy source structures each extending vertically through the staircase stack. A subset of the dummy channel structures is surrounded by the plurality of dummy source structures.

[0096] In some embodiments, at least one dummy channel structure is surrounded by at least four dummy source structures.

[0097] In some embodiments, at least two dummy channel structure are surrounded by at least six dummy source structures.

[0098] In some embodiments, at least four dummy channel structures are surrounded by at least eight dummy source structures.

[0099] In some embodiments, in a plan view, two dummy source structures and two dummy channel structures are aligned along a first row extending in a first lateral direction.

[0100] In some embodiments, the two dummy source structures are separated by the two dummy channel structure.

[0101] In some embodiments, the two dummy source structures are separated by one of the two dummy channel structure.

[0102] In some embodiments, in the plan view, two other dummy source structures and two other dummy channel structures are aligned along a second row extending in a second lateral direction perpendicular to the first lateral direction.

[0103] In some embodiments, the first and second row cross each other at a dummy channel structure.

[0104] In some embodiments, at least one dummy source structure includes a conductor layer in contact with the substrate.

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[0105] In some embodiments, at least one dummy source structure includes a spacer surrounding the conductor layer along a sidewall of the conductor layer, the spacer including a dielectric material.

[0106] In some embodiments, the plurality of dummy source structures are in contact with the substrate.

[0107] In some embodiments, the plurality of dummy source structures are not in contact with the substrate.

[0108] In some embodiments, a method for forming a 3D memory device includes the following operations. First, a dielectric stack including interleaved sacrificial layers and dielectric layers is formed on a substrate. A staircase structure on at least one side of the dielectric stack is formed. A plurality of dummy channel holes and a plurality of dummy source holes extending vertically through the staircase structure are formed. A subset of the dummy channel holes is surrounded by the plurality of dummy source holes. A dummy channel structure in each of the plurality of dummy channel holes is formed. Interleaved conductive layers and dielectric layers in the staircase structure are formed by replacing, through the dummy source holes, the sacrificial layers in the staircase structure with the conductive layers. A spacer along a sidewall of each of the plurality of dummy source holes is formed to cover the conductive layers in the staircase structure. A contact within the spacer in each of the plurality of dummy source holes is formed.

[0109] In some embodiments, forming the plurality of dummy channel holes and the plurality of dummy source holes includes performing a patterning process to simultaneously form the plurality of dummy channel holes and the plurality of dummy source holes through the staircase structure.

[0110] In some embodiments, the method also includes forming a plurality of channel holes through the dielectric stack simultaneously with forming the plurality of dummy channel holes and the plurality of dummy source holes through the staircase structure.

[0111] In some embodiments, the method further includes forming a sealing layer in each of the dummy source holes. After forming the sealing layer in each of the dummy source holes, a plurality of channel structures are formed. After forming the plurality of channel structures, the sealing layer from each of the dummy source holes is removed.

[0112] In some embodiments, replacing, through the dummy source holes, the sacrificial layers in the staircase structure with the conductive layers includes removing the sacrificial

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layers in the staircase structure through each of the dummy source holes after forming the plurality of channel structures to form a plurality of lateral recesses and depositing a conductive material to fill up the plurality of lateral recesses.

[0113] In some embodiments, the method further includes forming a plurality of recesses abutting a sidewall of each of the dummy source holes prior to forming the spacer.

[0114] In some embodiments, forming the plurality of recesses includes etching parts of the conductive layers in the staircase structure that abut the sidewall of the dummy source hole.

[0115] In some embodiments, a method for forming a 3D memory device includes the following operations. First, interleaved sacrificial layers and dielectric layers are alternatively deposited on a substrate. A staircase structure is formed on at least one side of the interleaved sacrificial layers and dielectric layer. A plurality of dummy channel holes and a plurality of dummy source holes are formed by simultaneously etching through the staircase structure. The plurality of dummy source holes are aligned with a portion of the plurality of dummy channel holes in a row along a lateral direction in a plan view. A sealing layer is deposited in each of the plurality of dummy source holes and each of the plurality of dummy channel holes. The sealing layer is etched away in each of the dummy source holes. The sacrificial layers in the staircase structure is replaced, through the dummy source holes, with a plurality of conductive layers. A spacer is deposited along a sidewall of each of the dummy source holes.

[0116] In some embodiments, the method further includes depositing a contact within the spacer in each of the plurality of dummy source holes.

[0117] In some embodiments, the method further includes patterning an etching mask on the staircase structure. The etching mask includes a plurality of first openings corresponding to the plurality of dummy channel holes and a plurality of second openings corresponding to the plurality of dummy source holes.

[0118] In some embodiments, depositing a sealing layer in each of the plurality of dummy source holes includes performing a rapid-sealing deposition process to deposit a sealing material in the plurality of dummy source holes and the plurality of dummy channel holes.

[0119] The foregoing description of the specific embodiments will so reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications of such specific embodiments, without undue experimentation, and without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the

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meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.

[0120] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0121] The Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0122] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

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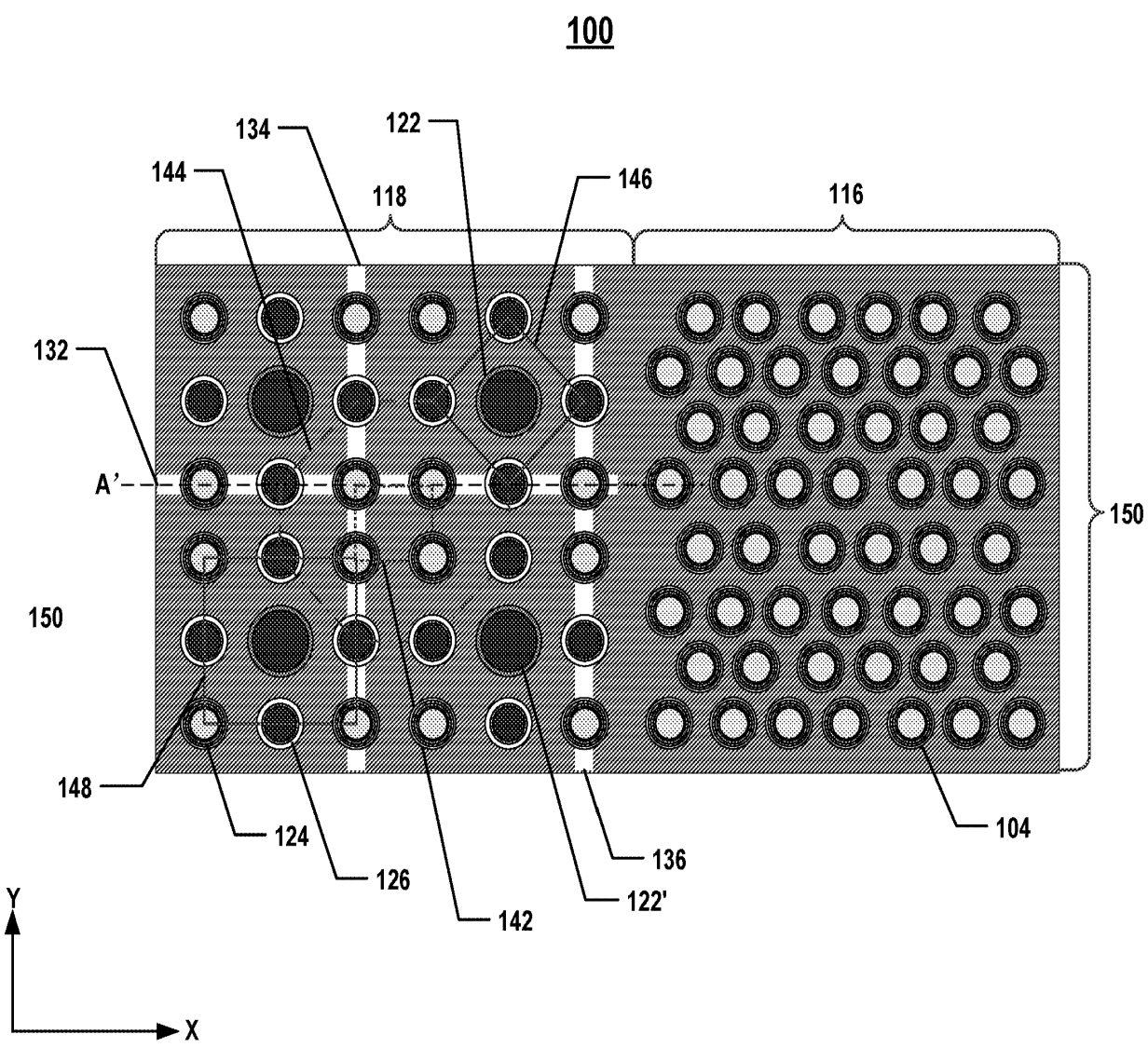


FIG. 1A

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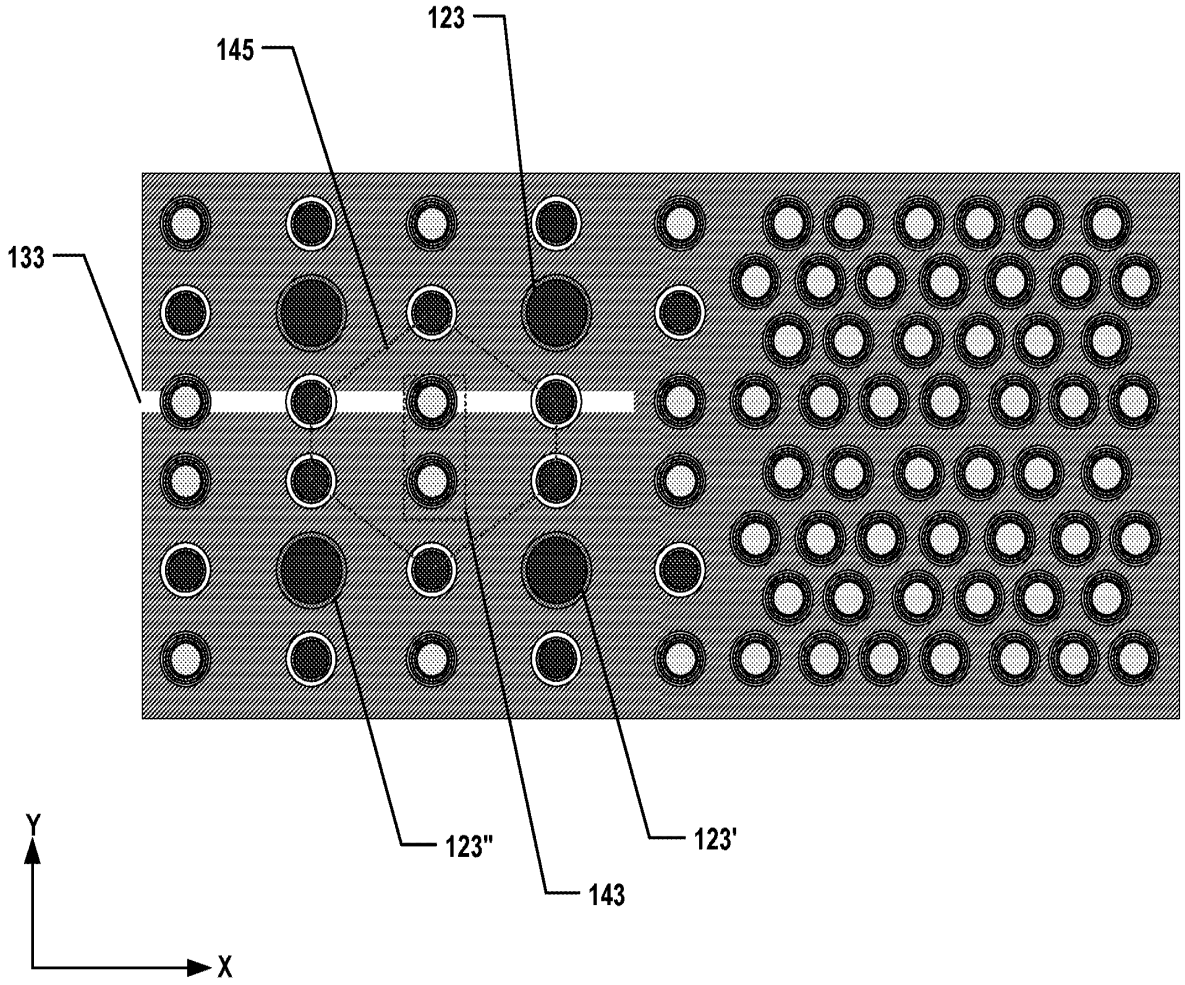


FIG. 1B

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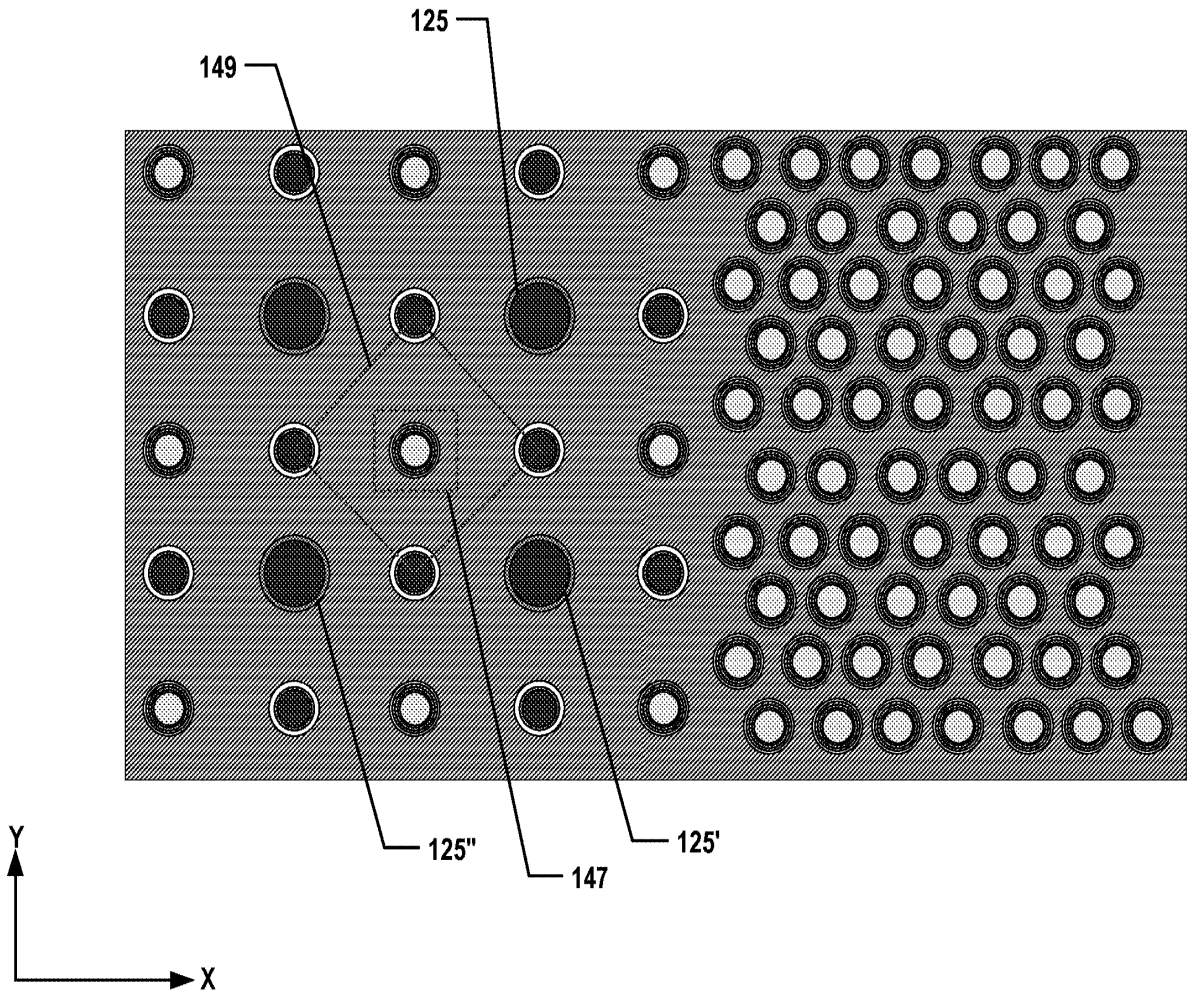


FIG. 1C

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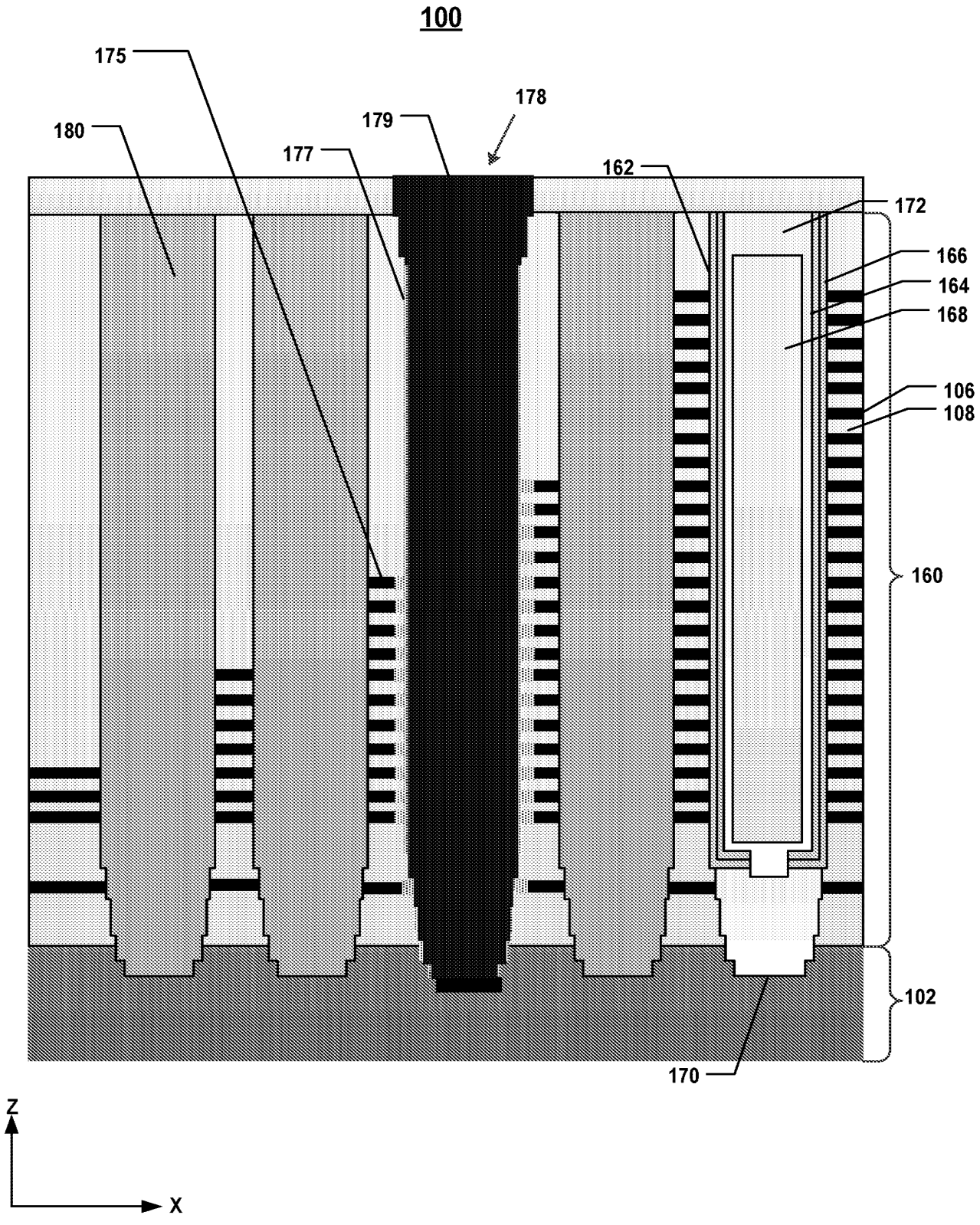

100
175
178
179
180
177
162
172
166
164
168
106
108
160
102
170
Z
X

FIG. 1D

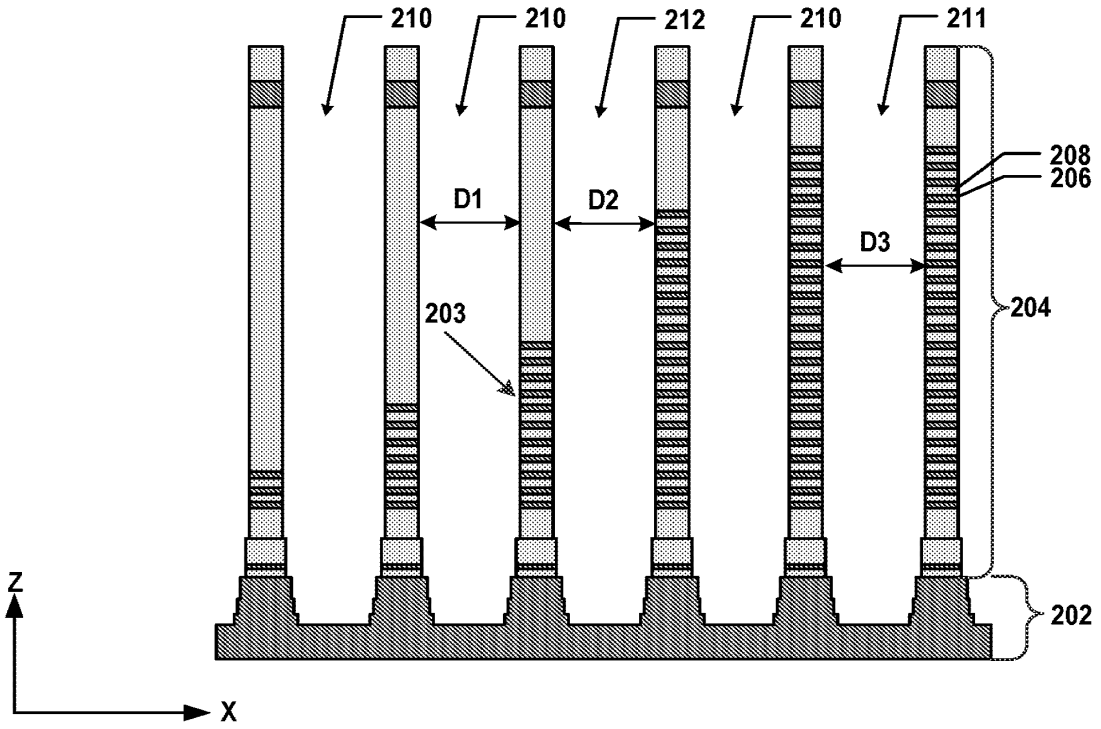

210
210
212
210
211
208
206
D1
D2
D3
204
203
202
Z
X

FIG. 2A

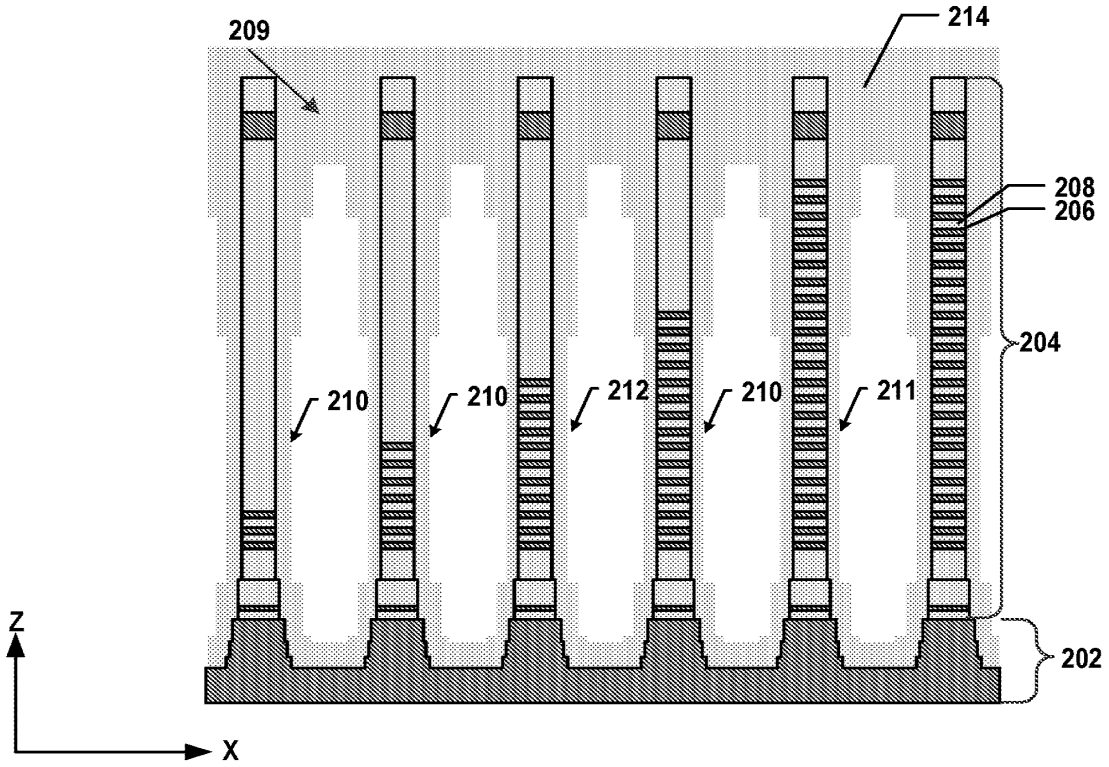

209
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206
204
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212
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211
202
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X

FIG. 2B

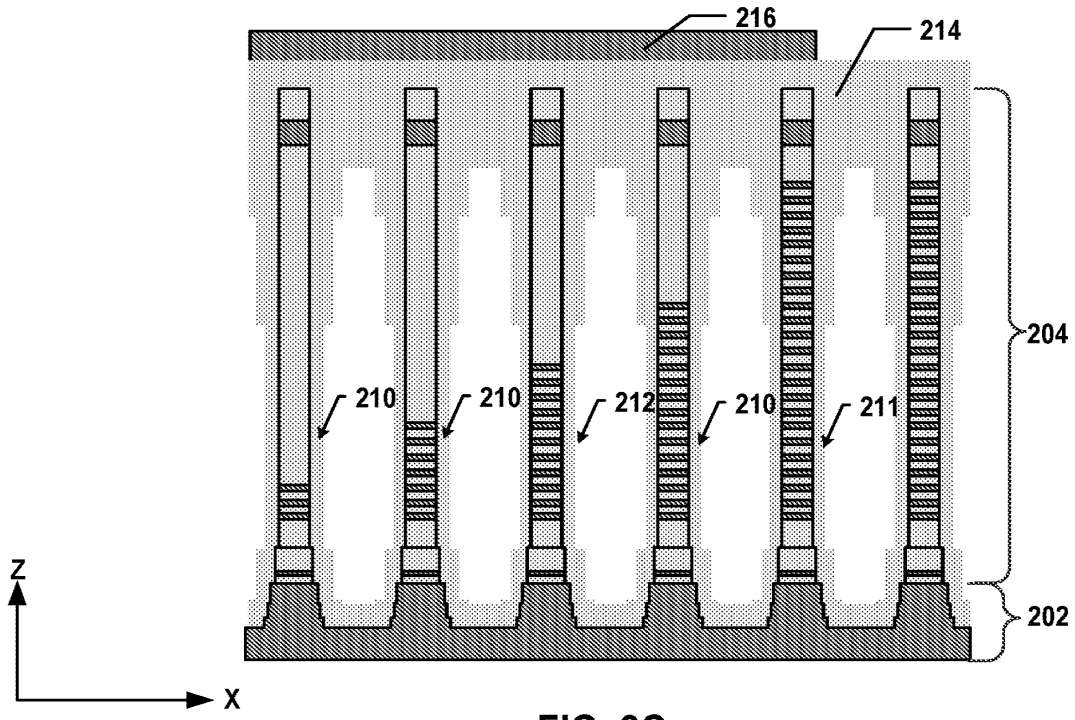

216
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204
210
210
212
210
211
202
Z
X

FIG. 2C

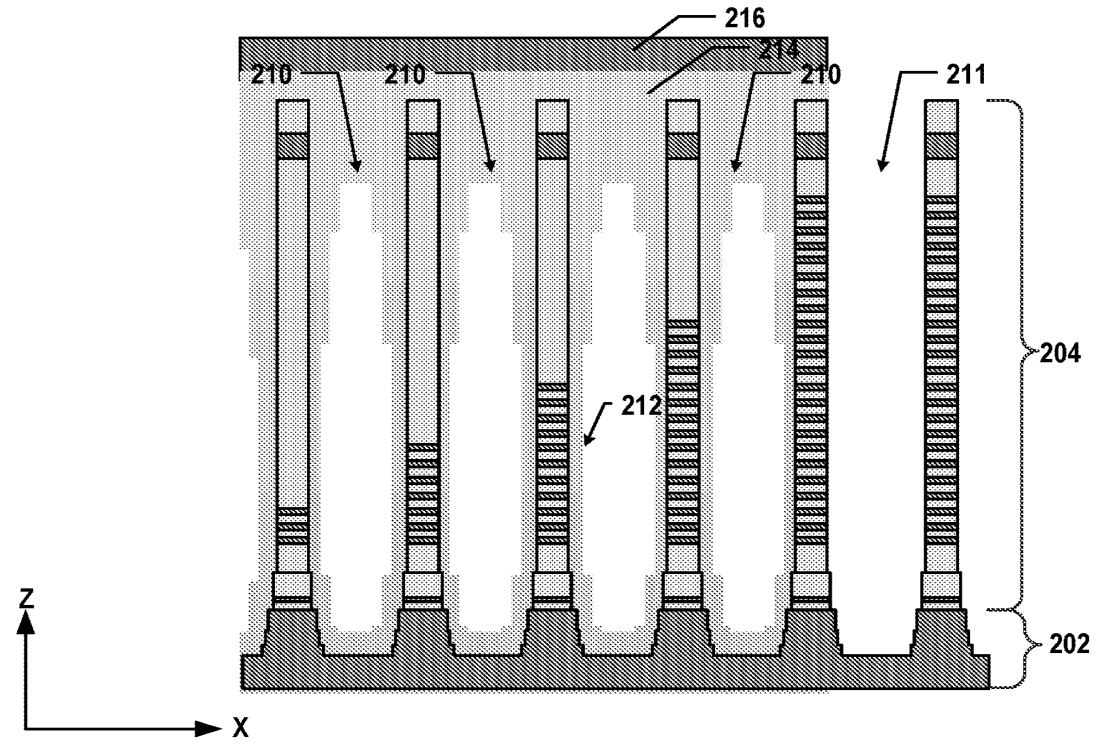

216
214
210
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210
211
204
212
202
Z
X

FIG. 2D

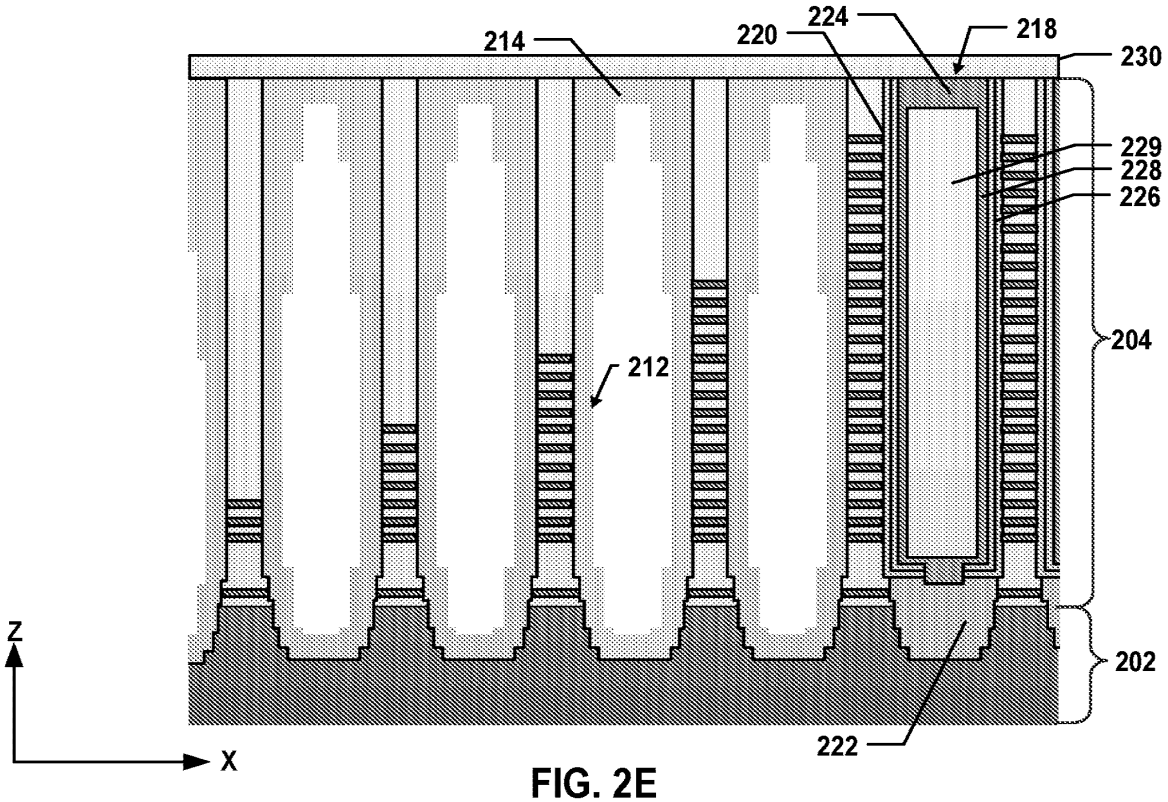

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220
224
218
230
229
228
226
204
212
202
222
Z
X

FIG. 2E

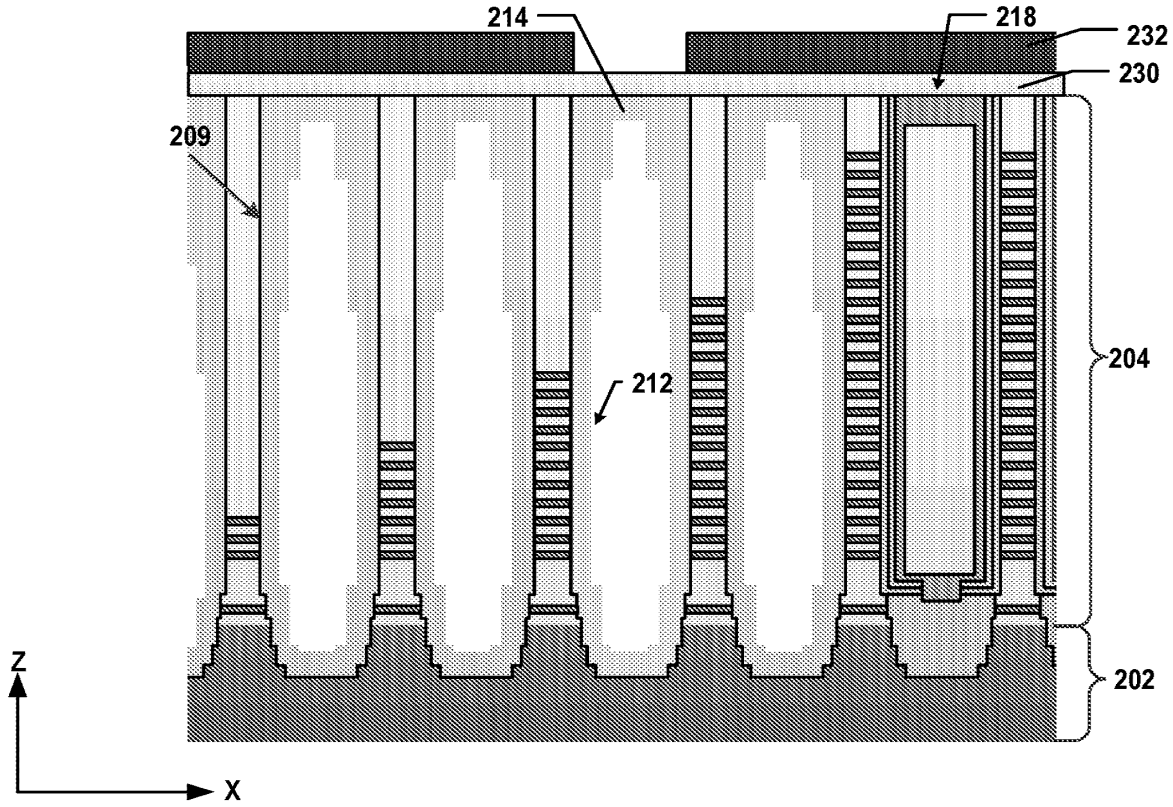

214
218
232
230
209
204
212
202
Z
X

FIG. 2F

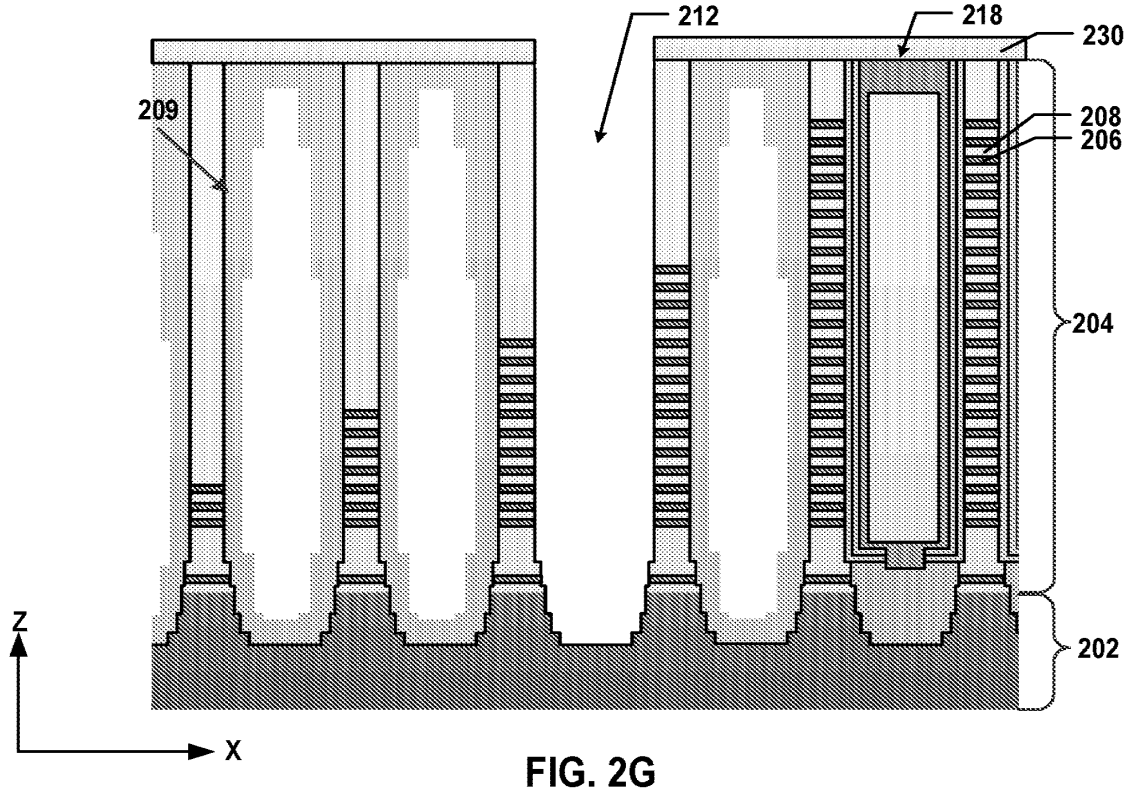


FIG. 2G

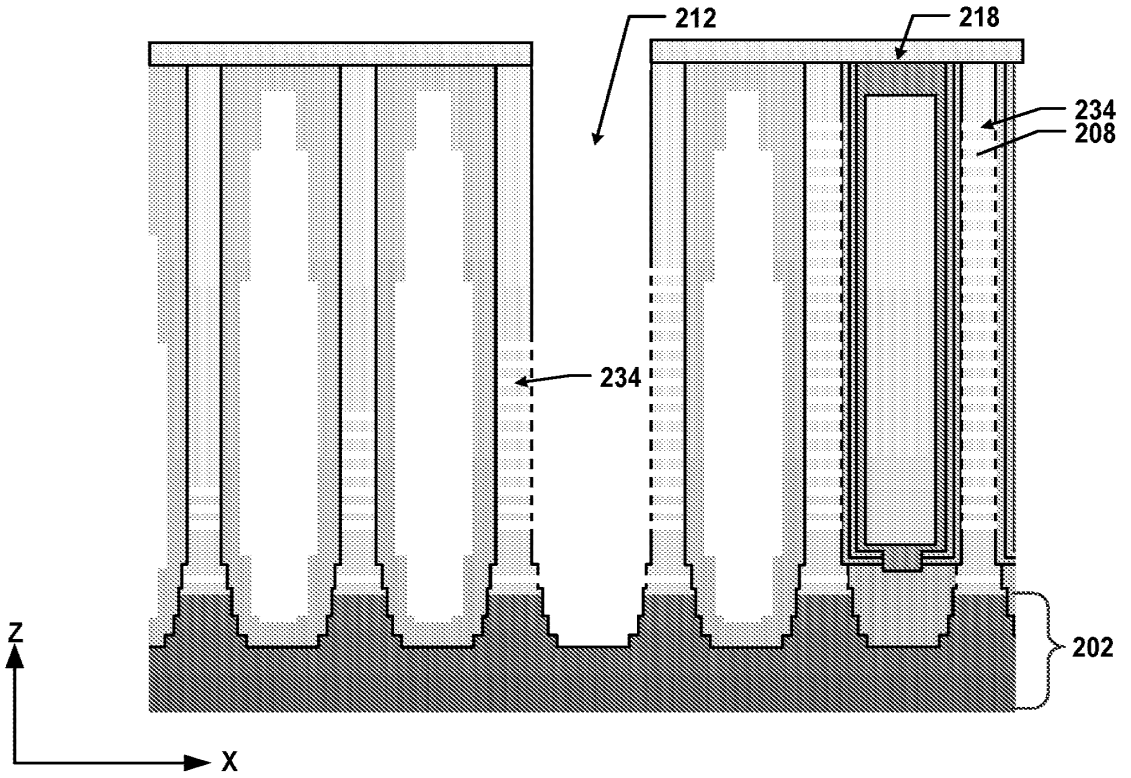


FIG. 2H

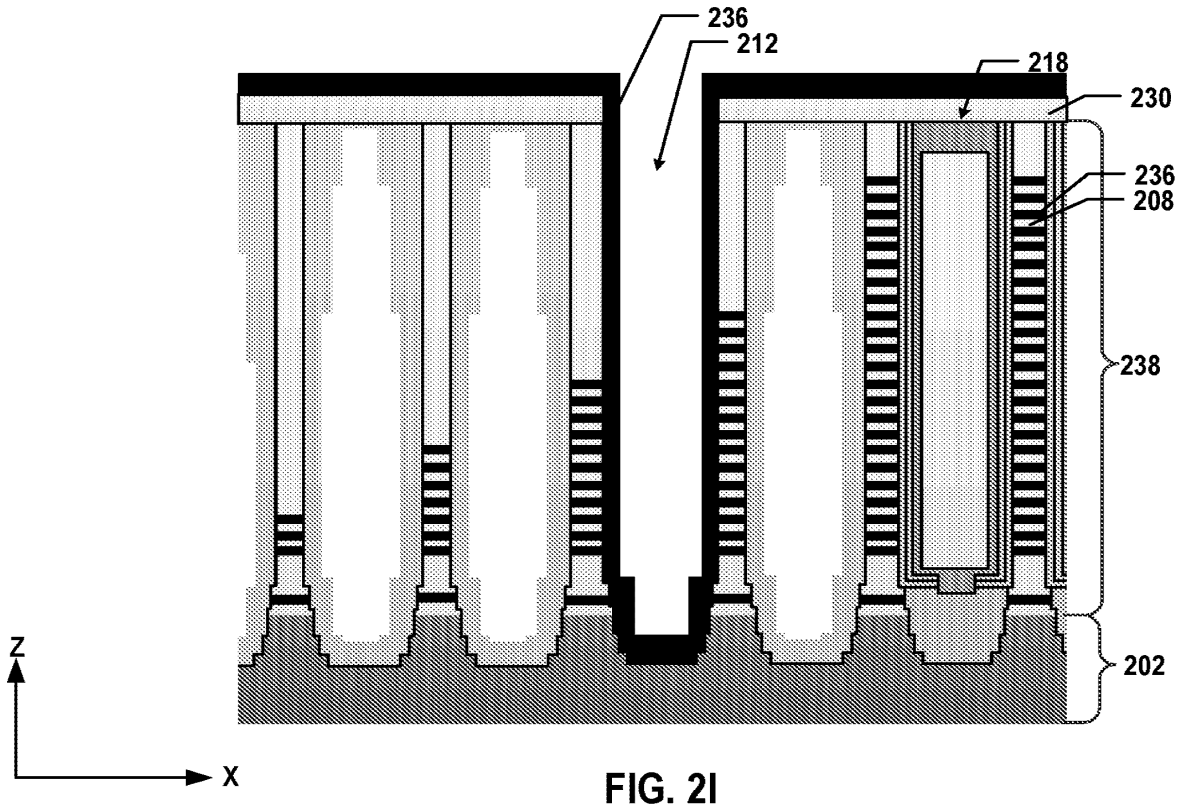

236
212
218
230
236
208
238
202
Z
X

FIG. 2I

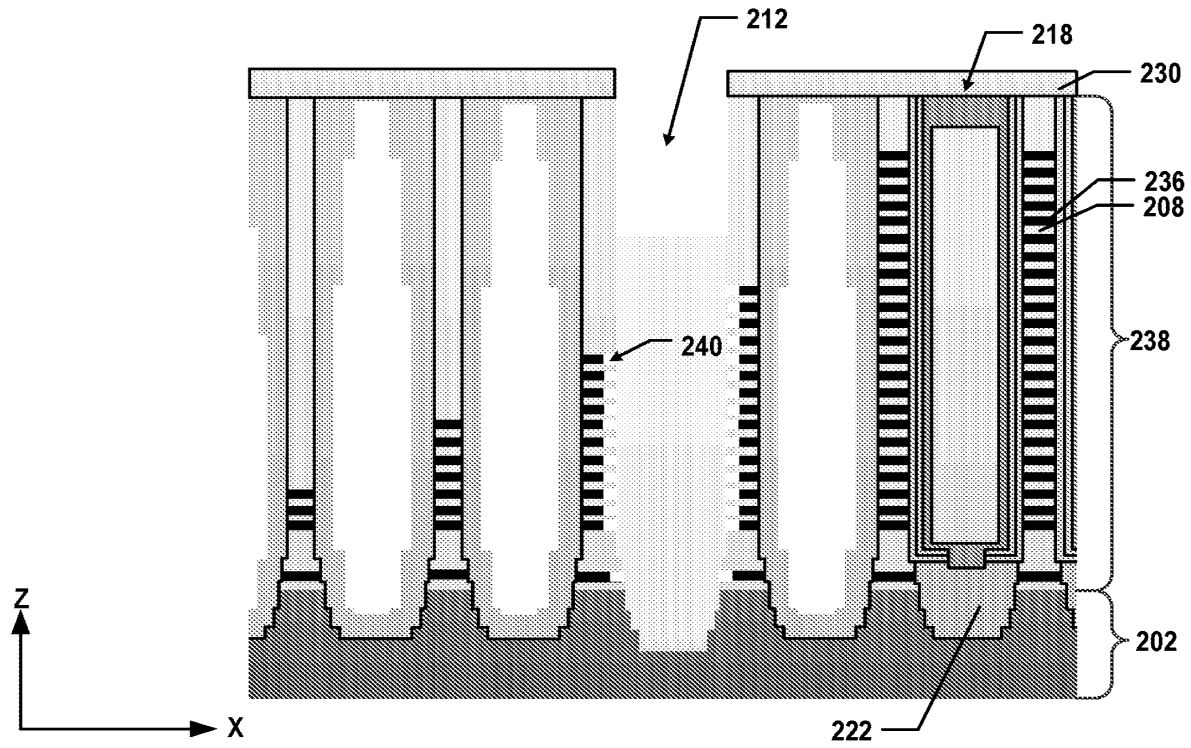

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236
208
240
238
202
222
Z
X

FIG. 2J

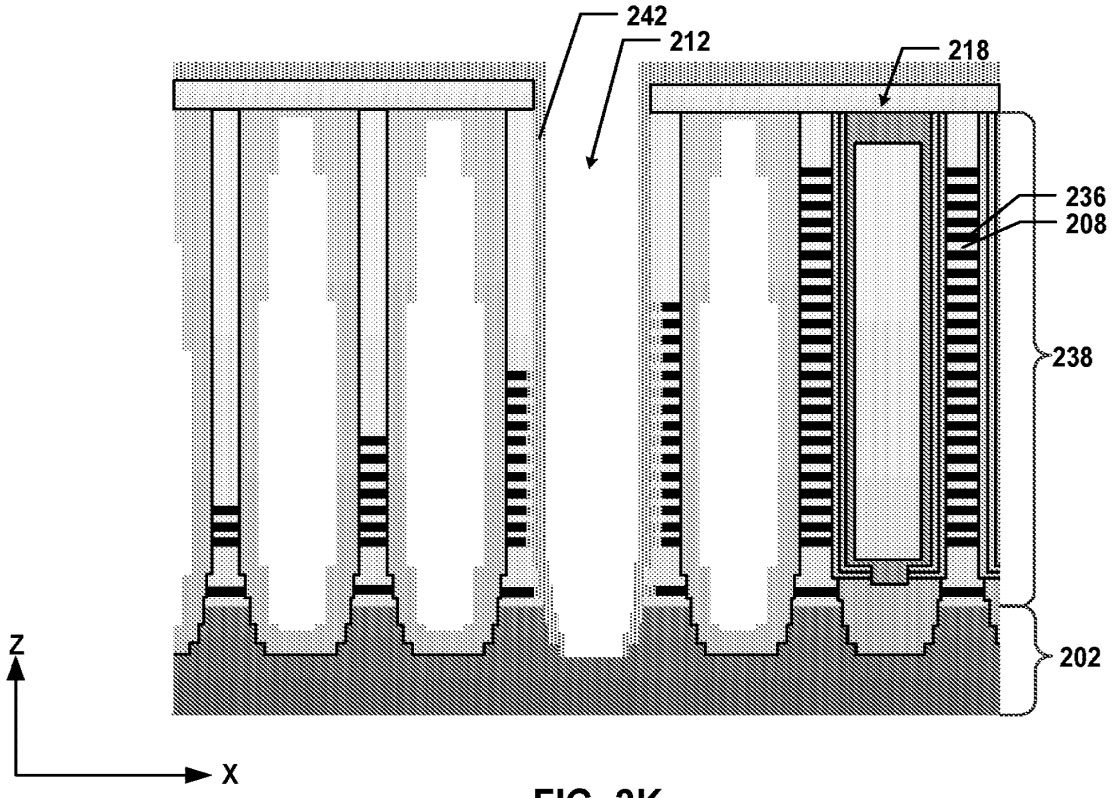


FIG. 2K

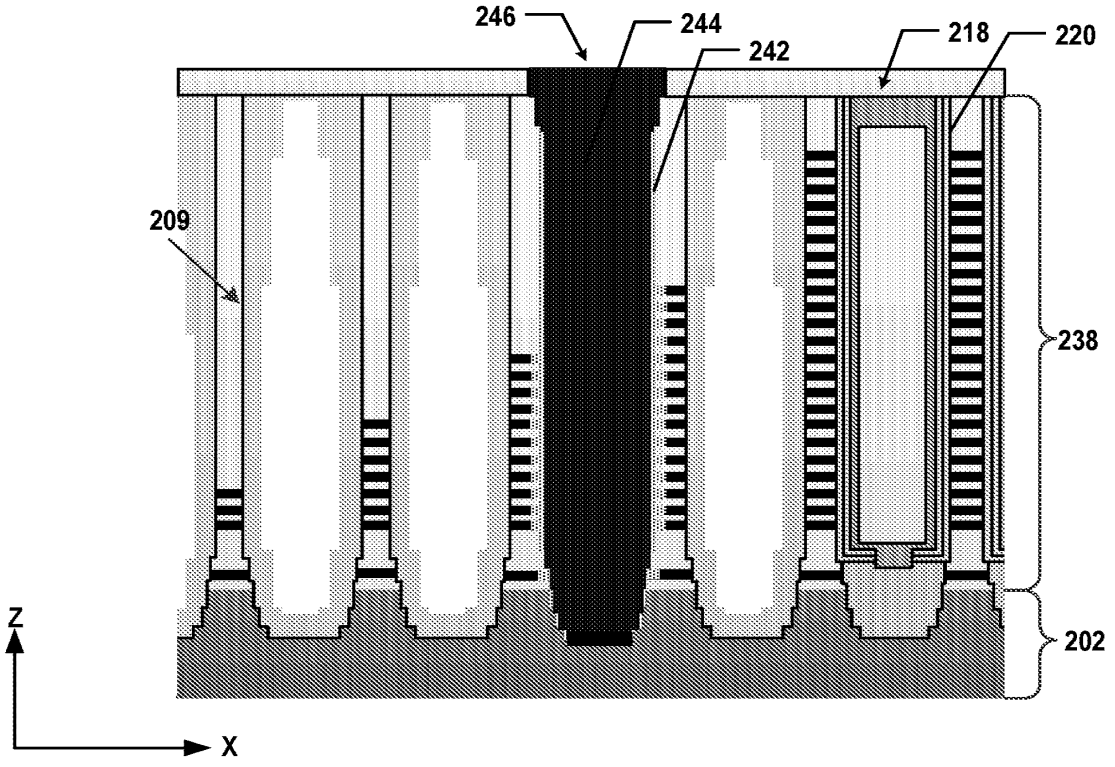


FIG. 2L

300

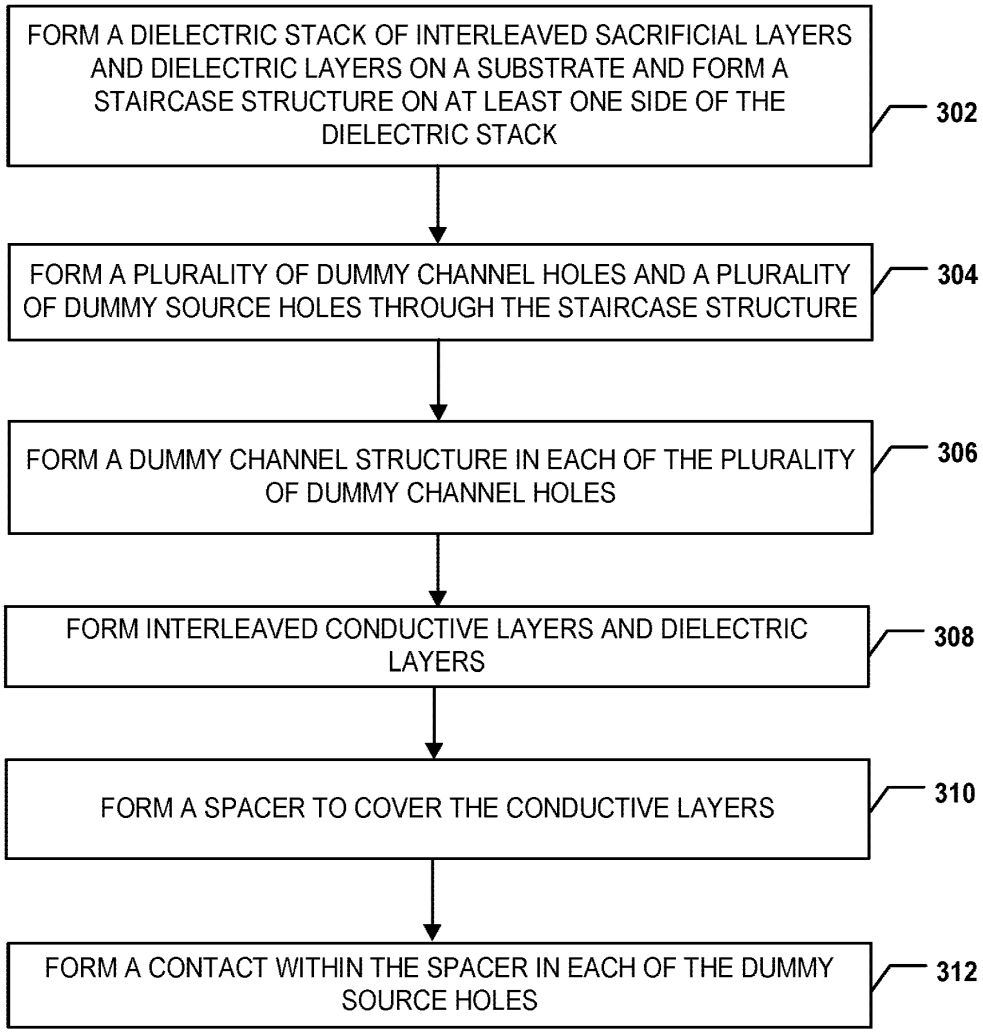

FORM A DIELECTRIC STACK OF INTERLEAVED SACRIFICIAL LAYERS AND DIELECTRIC LAYERS ON A SUBSTRATE AND FORM A STAIRCASE STRUCTURE ON AT LEAST ONE SIDE OF THE DIELECTRIC STACK
302
FORM A PLURALITY OF DUMMY CHANNEL HOLES AND A PLURALITY OF DUMMY SOURCE HOLES THROUGH THE STAIRCASE STRUCTURE
304
FORM A DUMMY CHANNEL STRUCTURE IN EACH OF THE PLURALITY OF DUMMY CHANNEL HOLES
306
FORM INTERLEAVED CONDUCTIVE LAYERS AND DIELECTRIC LAYERS
308
FORM A SPACER TO COVER THE CONDUCTIVE LAYERS
310
FORM A CONTACT WITHIN THE SPACER IN EACH OF THE DUMMY SOURCE HOLES
312

FIG. 3

400

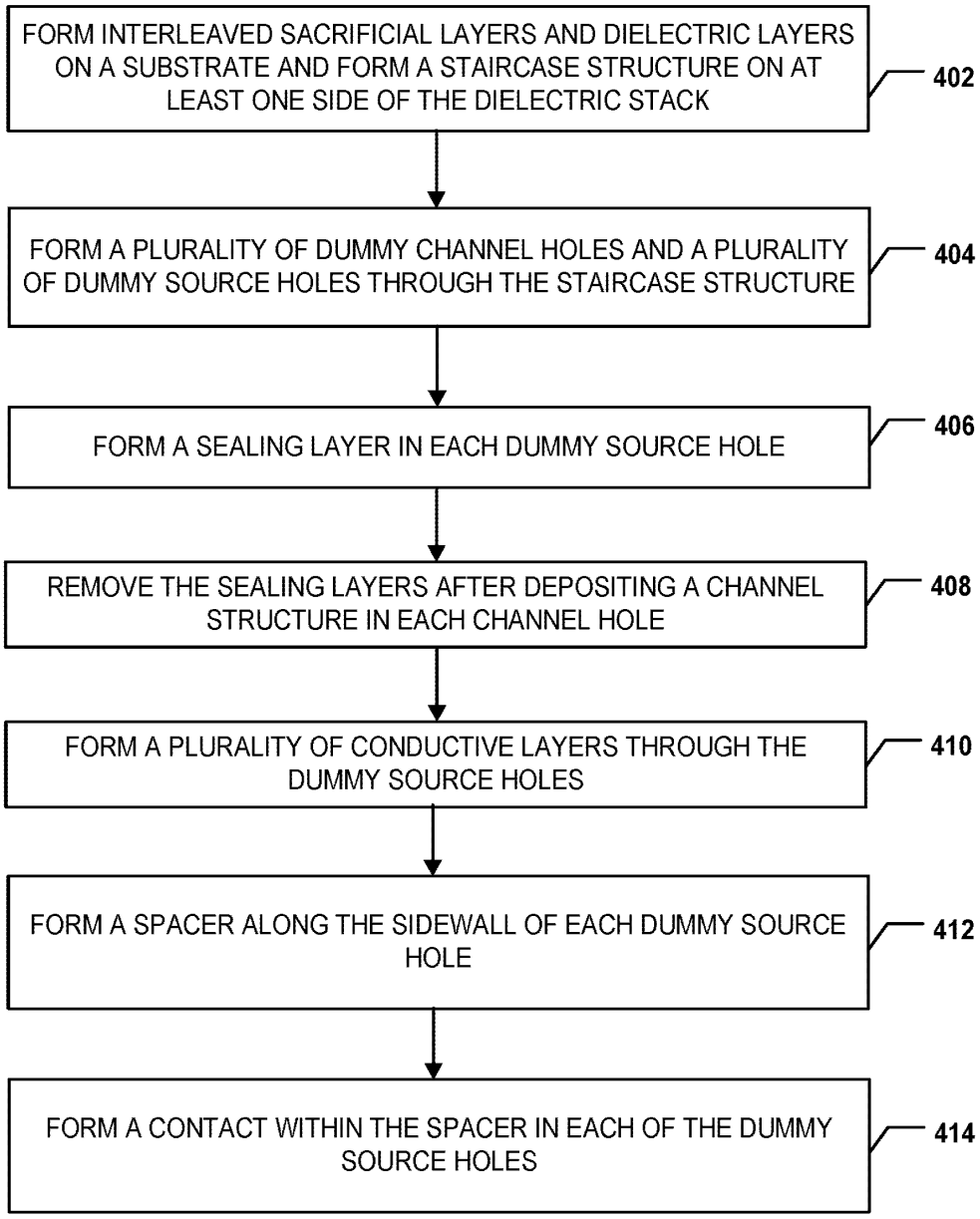

FORM INTERLEAVED SACRIFICIAL LAYERS AND DIELECTRIC LAYERS ON A SUBSTRATE AND FORM A STAIRCASE STRUCTURE ON AT LEAST ONE SIDE OF THE DIELECTRIC STACK
402
FORM A PLURALITY OF DUMMY CHANNEL HOLES AND A PLURALITY OF DUMMY SOURCE HOLES THROUGH THE STAIRCASE STRUCTURE
404
FORM A SEALING LAYER IN EACH DUMMY SOURCE HOLE
406
REMOVE THE SEALING LAYERS AFTER DEPOSITING A CHANNEL STRUCTURE IN EACH CHANNEL HOLE
408
FORM A PLURALITY OF CONDUCTIVE LAYERS THROUGH THE DUMMY SOURCE HOLES
410
FORM A SPACER ALONG THE SIDEWALL OF EACH DUMMY SOURCE HOLE
412
FORM A CONTACT WITHIN THE SPACER IN EACH OF THE DUMMY SOURCE HOLES
414

FIG. 4

500

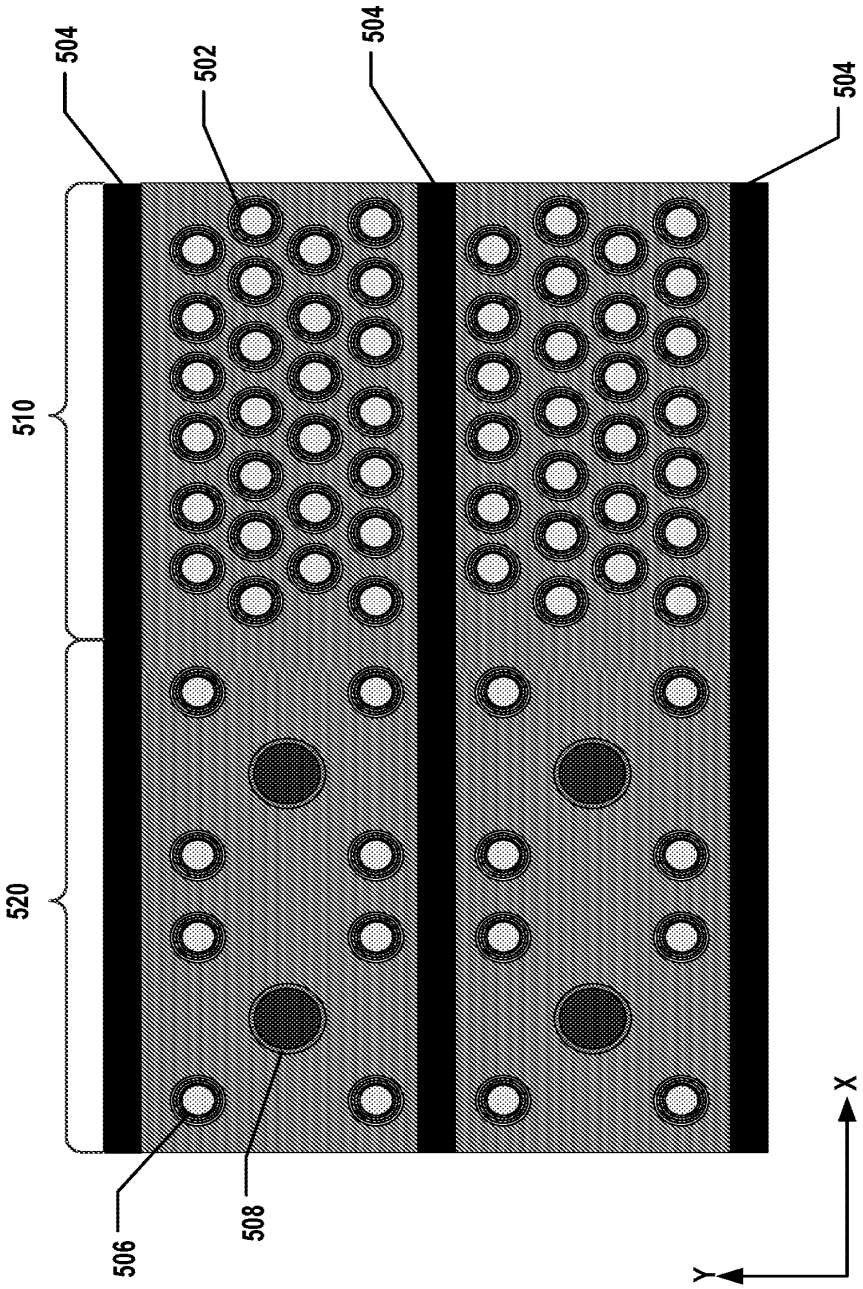


FIG. 5

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COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

☒ The attached application, or

☐ United States application or PCT international application number _____

filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar ($1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

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(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 153988** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

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IPR2024-00789

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

LEGAL NAME OF INVENTOR

Inventor: **Wenyu Hua** Date: 2019.3.28

Signature of Inventor: Wenyu Hua

Inventor: **Fandong Liu** Date: 2019/3/28

Signature of Inventor: Fandong LIU

Inventor: **Zhiliang Xia** Date: 2019.03.28

Signature of Inventor: Zhiliang XIA

1934285-005071BP-10.18.40.190
32766-28/03/2019 15:13

Micron Ex. 1002, p. 65
Micron v. YMTC
IPR2024-00789

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 01/31/2018. OMB 0651-0035
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	
Filing Date	Herewith
First Named Inventor	Wenyu HUA
Title	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME
Art Unit	To Be Determined
Examiner Name	To Be Determined
Attorney Docket Number	10018-01-0045-US

SIGNATURE of Applicant or Patent Practitioner

Signature	/Jinrong Yuan/	Date (Optional)	May 2, 2019
Name	Jinrong Yuan	Registration Number	76,066
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)	Yangtze Memory Technologies Co., Ltd.		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Doc Code: PA.
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

153988

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	
Name	SIMON SHI-NING YANG		
Title	CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of One forms are submitted

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Wenyu Hua
Filer:	Jinrong Yuan/Anna O'Connor
Attorney Docket Number:	10018-01-0045-US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1720**

Electronic Acknowledgement Receipt

EFS ID:	35906110
Application Number:	16402202
International Application Number:	
Confirmation Number:	7288
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Wenyu Hua
Customer Number:	153988
Filer:	Jinrong Yuan/Anna O'Connor
Filer Authorized By:	Jinrong Yuan
Attorney Docket Number:	10018-01-0045-US
Receipt Date:	02-MAY-2019
Filing Date:	
Time Stamp:	22:42:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1720
RAM confirmation Number	050319INTEFSW22434300
Deposit Account	602227
Authorized User	Anna O'Connor
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	10018-01-0045-US_UtilityPatentApp-FEETransmittal.pdf	469827 10256793f8079157675b7129725295a849a92ebe	no	2
Warnings:					
Information:					
2	Application Data Sheet	10018-01-0045-US_ADS.pdf	1829238 dc3abae4ac62b4371367ef19461044d75995b39e	no	9
Warnings:					
Information:					
3		10018-01-0045-US_FINALApplication.pdf	187789 fcc312792f358018ee7aebea27c1373e469fd69c	yes	32

Multipart Description/PDF files in .zip description

Document Description	Start	End
Abstract	32	32
Claims	28	31
Specification	1	27

Warnings:					
Information:					
4	Drawings-only black and white line drawings	10018-01-0045-US_FINALFigures.pdf	204731 3c75ccf0cc8f6f73ba3711ddb97f588436864c8e	no	13
Warnings:					
Information:					
5	Oath or Declaration filed	10018-01-0045-US_Dec-Assign-SIGNED.pdf	117739 e03ba4c89de4bb88cd8242f3bb5d6ab7044ac7fd	no	3

Warnings:					
Information:					
6	Power of Attorney	10018-01-0045-US_GeneralPOA.pdf	734644 1be55e107fcb4dd91dd01160a321af87d822f637	no	2
Warnings:					
Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	34806 52d00b670ce8a5af98e8f4cd6a1d1f27826cdf3a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3578774		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/402,202

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/402,202	05/02/2019		1720	10018-01-0045-US	20	3

CONFIRMATION NO. 7288

153988
Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

FILING RECEIPT

OC000000108231007

Date Mailed: 05/17/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Wenyu Hua, Wuhan, CHINA;
Fandong Liu, Wuhan, CHINA;
Zhiliang Xia, Wuhan, CHINA;

Applicant(s)

YANGTZE MEMORY TECHNOLOGIES CO., LTD., Wuhan, CHINA;

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd.

Power of Attorney: The patent practitioners associated with Customer Number 153988

Domestic Priority data as claimed by applicant

This application is a CON of PCT/CN2019/076186 02/26/2019

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

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Micron v. YMTC
IPR2024-00789

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/16/2019
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/402,202**
Projected Publication Date: 08/27/2020
Non-Publication Request: No
Early Publication Request: No
Title

THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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IPR2024-00789

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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Micron Ex. 1002, p. 76
Micron v. YMTC
IPR2024-00789

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	16402202
Filing Date	2019-05-02
First Named Inventor	Wenyu HUA
Art Unit	2811
Examiner Name	GURLEY, LYNNE ANN
Attorney Docket Number	10018-01-0045-US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8822285	B2	2014-09-02	Hwang et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	108962910	CN	A	2018-12-07	SAMSUNG ELECTRONICS CO LTD		
	2	106057813	CN	A	2016-10-26	SAMSUNG ELECTRONICS CO LTD		

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Micron Ex. 1002, p. 77
Micron v. YMTC
IPR2024-00789

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16402202
	Filing Date	2019-05-02
	First Named Inventor	Wenyu HUA
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	10018-01-0045-US

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	International Search Report issued in corresponding International Application No. PCT/CN2019/076186, mailed October 23, 2019, 4 pages	
	2	Written Opinion of the International Searching Authority issued in corresponding International Application No. PCT/CN2019/076186, mailed October 23, 2019, 5 pages	

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

Micron Ex. 1002, p. 78
Micron v. YMTC
IPR2024-00789

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16402202
	Filing Date	2019-05-02
	First Named Inventor	Wenyu HUA
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	10018-01-0045-US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2019-11-08
Name/Print	Zhiwei Zou	Registration Number	66,041

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Espacenet

Bibliographic data: CN108962910 (A) — 2018-12-07

Vertical memory device

Inventor(s): TAE-HEE LEE; KYOUNG-HOON KIM; HONG-SOO KIM ± (金敬勋, ; 金泓秀, ; 李太熙)

Applicant(s): SAMSUNG ELECTRONICS CO LTD ± (三星电子株式会社)

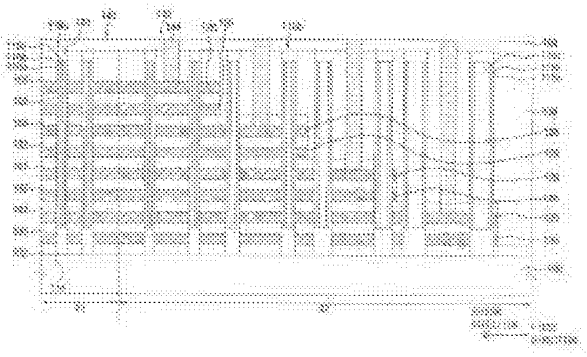
Classification: **- international:** ***H01L27/1157***
- cooperative: H01L23/5226 (US); H01L27/11556 (US); H01L27/11565 (EP, US); H01L27/1157 (CN); H01L27/11575 (EP, US); H01L27/11582 (EP, US)

Application number: CN201810466878 20180516 Global Dossier

Priority number(s): KR20170060927 20170517

Also published as: KR20180126210 (A) US2018337192 (A1)

Abstract of CN108962910 (A)



Provided is a vertical memory device. The vertical memory device includes a conductive pattern structure on a first region of a substrate, the conductive pattern structure including a stack of interleaved conductive patterns and insulation layers. A pad structure is disposed on a second region of the substrate adjacent the first region of the substrate wherein edges of the conductive patterns aredisposed at spaced apart points along a first direction to provide conductive pads arranged as respective steps in a staircase arrangement. A plurality of channel structures extends through the conductive pattern structure and a plurality of dummy channel structures extends through the pad structure. Respective contact plugs are disposed on the conductive pads. Numbers of the dummy channel structures per unit area passing through the conductive pads vary. Widths of the dummy channel structures passing through the conductive pads may also vary.

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(19)中华人民共和国国家知识产权局

(12)发明专利申请

(10)申请公布号 CN 108962910 A
(43)申请公布日 2018.12.07

(21)申请号 201810466878.2

(22)申请日 2018.05.16

(30)优先权数据
10-2017-0060927 2017.05.17 KR

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(51)Int.Cl.
H01L 27/1157(2017.01)

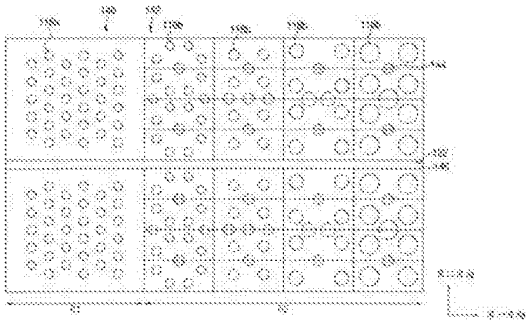
权利要求书3页 说明书9页 附图21页

(54)发明名称

竖直存储器件

(57)摘要

本公开提供了竖直存储器件。一种竖直存储器件包括在基板的第一区域上的导电图案结构，该导电图案结构包括交错的导电图案和绝缘层的堆叠。焊盘结构设置在基板的第二区域上，基板的第二区域与基板的第一区域相邻，其中导电图案的边缘设置在沿着第一方向间隔开的点处以提供布置为阶梯布置中的各台阶的导电焊盘。多个沟道结构延伸穿过导电图案结构，并且多个虚设沟道结构延伸穿过焊盘结构。各接触插塞设置在导电焊盘上。穿过导电焊盘的虚设沟道结构的每单位面积的数量是变化的。穿过导电焊盘的虚设沟道结构的宽度也可以变化。



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1.一种竖直存储器件,包括:

导电图案结构,在基板上并包括交错的导电图案和绝缘层的堆叠,其中所述导电图案的边缘设置在沿着第一方向间隔开的点处以提供布置为阶梯布置中的各台阶的导电焊盘;

多个沟道结构,在垂直于所述第一方向的第二方向上延伸穿过所述导电图案结构;

多个虚设沟道结构,在所述第二方向上延伸穿过所述导电焊盘;以及

各接触插塞,在所述导电焊盘上,

其中所述导电焊盘中的第一个具有从其穿过的第一数量的所述虚设沟道结构,并且其中所述导电焊盘中的第二个具有从其穿过的第二数量的所述虚设沟道结构,所述第二数量不同于所述虚设沟道结构的所述第一数量。

2.如权利要求1所述的竖直存储器件,其中穿过所述导电焊盘中的所述第一个的所述虚设沟道结构具有第一宽度,并且其中穿过所述导电焊盘中的所述第二个的所述虚设沟道结构具有第二宽度,所述第二宽度不同于所述第一宽度。

3.如权利要求2所述的竖直存储器件,其中所述第一数量的虚设沟道结构少于所述第二数量的所述虚设沟道结构,并且其中所述第一宽度大于所述第二宽度。

4.如权利要求1所述的竖直存储器件,其中所述导电焊盘中的所述第一个是所述台阶中的比所述导电焊盘中的所述第二个低的一个。

5.如权利要求4所述的竖直存储器件,其中穿过所述导电焊盘的所述虚设沟道结构的数量从所述导电焊盘中的上部的一个朝向所述导电焊盘中的下部的一个减少。

6.如权利要求1所述的竖直存储器件,其中穿过所述导电焊盘的所述虚设沟道结构的宽度从所述台阶中的最上面的一个朝向所述台阶中的次最下的一个增大,并且其中穿过所述导电焊盘中的最下面的一个的所述虚设沟道结构的宽度小于穿过所述导电焊盘中的次最下的一个的所述虚设沟道结构的宽度。

7.如权利要求6所述的竖直存储器件,其中穿过所述导电焊盘的所述虚设沟道结构的数量从所述导电焊盘中的最上面的一个朝向所述导电焊盘中的次最下的一个减少,并且其中穿过所述导电焊盘中的最下面的一个的所述虚设沟道结构的数量大于穿过所述导电焊盘中的次最下的一个的所述虚设沟道结构的数量。

8.如权利要求1所述的竖直存储器件,其中所述接触插塞在所述第一方向上线性地排列,并且其中所述接触插塞中的一个接触所述导电焊盘中的最下面的一个的中央部分。

9.如权利要求1所述的竖直存储器件,其中各导电焊盘上的所述接触插塞没有在所述第一方向上线性地排列。

10.如权利要求9所述的竖直存储器件,其中所述导电焊盘上的所述接触插塞在相对于所述第一方向具有角度的倾斜方向上排列,并且其中所述接触插塞中的一个接触所述导电焊盘中的最下面的一个的中央部分。

11.如权利要求1所述的竖直存储器件,

其中所述导电图案的第一边缘设置在沿着所述第一方向间隔开的第一点处以提供布置为第一阶梯布置中的各台阶的第一导电焊盘;并且

其中所述导电图案的第二边缘设置在沿着所述第一方向间隔开的第二点处以提供布置为第二阶梯布置中的各台阶的第二导电焊盘。

12.如权利要求1所述的竖直存储器件,其中所述沟道结构具有第一宽度,并且其中所

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述虚设沟道结构具有第二宽度，所述第二宽度与所述第一宽度相同或大于所述第一宽度。

13.一种竖直存储器件，包括：

导电图案结构，在基板的第一区域上，所述导电图案结构包括交错的导电图案和绝缘层的堆叠；

焊盘结构，在所述基板的第二区域上，所述基板的所述第二区域与所述基板的所述第一区域相邻，其中所述导电图案的边缘设置在沿着第一方向间隔开的点处以提供布置为阶梯布置中的各台阶的导电焊盘；

多个沟道结构，延伸穿过所述导电图案结构；

多个虚设沟道结构，延伸穿过所述焊盘结构；以及

各接触插塞，在所述导电焊盘上，

其中穿过所述导电焊盘的所述虚设沟道结构的每单位面积的数量是变化的。

14.如权利要求13所述的竖直存储器件，其中穿过所述导电焊盘的所述虚设沟道结构的宽度是变化的。

15.如权利要求13所述的竖直存储器件，其中穿过所述导电焊盘的所述虚设沟道结构的宽度与穿过所述导电焊盘的所述虚设沟道结构的数量成反比地变化。

16.如权利要求13所述的竖直存储器件，

其中所述导电图案的第一边缘设置在沿着所述第一方向间隔开的第一点处以提供布置为第一阶梯布置中的各台阶的第一导电焊盘；并且

其中所述导电图案的第二边缘设置在沿着所述第一方向间隔开的第二点处以提供布置为第二阶梯布置中的各台阶的第二导电焊盘。

17.如权利要求13所述的竖直存储器件，其中各导电图案上的所述接触插塞在所述第一方向上线性地排列，并且其中所述接触插塞中的一个形成在所述导电图案中的一个的上表面的中央部分上。

18.如权利要求13所述的竖直存储器件，其中相邻的所述接触插塞之间在与所述第一方向垂直的第二方向上的距离从所述导电焊盘中的最上面的一个到所述导电焊盘中的最下面的一个减小，并且其中所述接触插塞中的一个形成在所述导电焊盘中的最下面的一个的中央部分上。

19.一种竖直存储器件，包括：

导电图案结构，在基板上并包括交错的导电图案和绝缘层的堆叠，其中所述导电图案的边缘设置在沿着第一方向间隔开的点处以提供布置为阶梯布置中的各台阶的导电焊盘；

多个沟道结构，在垂直于所述第一方向的第二方向上延伸穿过所述导电图案结构；

多个虚设沟道结构，在所述第二方向上延伸穿过所述导电焊盘；以及

各接触插塞，在所述导电焊盘上，

其中所述导电焊盘中的第一个具有从其穿过的具有第一宽度的第一类虚设沟道结构，并且其中所述导电焊盘中的第二个具有从其穿过的具有第二宽度的第二类虚设沟道结构，所述第二宽度与所述第一宽度不同。

20.如权利要求19所述的竖直存储器件，其中所述虚设沟道结构的宽度从所述导电焊盘中的最上面的一个朝向所述导电焊盘中的最下面的一个增大，并且其中穿过相应的导电焊盘的所述虚设沟道结构数量从所述导电焊盘中的最上面的一个朝向所述导电焊盘中的

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最下面的一个减少。

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竖直存储器件

技术领域

[0001] 示例实施方式涉及竖直存储器件。更具体地，示例实施方式涉及具有由变化尺寸的虚设沟道支撑的导电焊盘的竖直存储器件以及竖直NAND闪存器件。

背景技术

[0002] 已经发展了包括多个存储单元的竖直存储器件，该多个存储单元分别竖直地堆叠在基板上的多个层级上。随着层级的数目增加，竖直存储器件可能具有不稳定的结构。

发明内容

[0003] 示例实施方式能够提供具有提高的稳定性的结构的竖直存储器件。

[0004] 根据示例实施方式，一种竖直存储器件包括导电图案结构，该导电图案结构在基板上并包括交错的导电图案和绝缘层的堆叠，其中导电图案的边缘设置在沿着第一方向间隔开的点处以提供布置为阶梯布置中的各台阶的导电焊盘。多个沟道结构在垂直于第一方向的第二方向上延伸穿过导电图案结构，并且多个虚设沟道结构在第二方向上延伸穿过导电焊盘。各接触插塞设置在导电焊盘上。导电焊盘中的第一个具有从其穿过的第一数量的虚设沟道结构，并且导电焊盘中的第二个具有从其穿过的第二数量的虚设沟道结构，虚设沟道结构的第二数量不同于虚设沟道结构的第一数量。

[0005] 在某些实施方式中，穿过导电焊盘中的第一个的虚设沟道结构可以具有第一宽度，并且穿过导电焊盘中的第二个的虚设沟道结构可以具有不同于第一宽度的第二宽度。虚设沟道结构的第一数量可以少于虚设沟道结构的第二数量，并且第一宽度可以大于第二宽度。

[0006] 在另一些示例实施方式中，一种竖直存储器件包括在基板的第一区域上的导电图案结构，该导电图案结构包括交错的导电图案和绝缘层的堆叠。焊盘结构设置在基板的第二区域上，基板的第二区域与基板的第一区域相邻，其中导电图案的边缘设置在沿着第一方向间隔开的点处以提供布置为阶梯布置中的相应台阶的导电焊盘。多个沟道结构延伸穿过导电图案结构，并且多个虚设沟道结构延伸穿过焊盘结构。各接触插塞设置在导电焊盘上。穿过导电焊盘的虚设沟道结构的每单位面积的数量变化。穿过导电焊盘的虚设沟道结构的宽度也可以变化。例如，穿过导电焊盘的虚设沟道结构的宽度可以与穿过导电焊盘的虚设沟道结构的数量成反比地变化。

[0007] 在另一些实施方式中，一种竖直存储器件包括导电图案结构，该导电图案结构在基板上并包括交错的导电图案和绝缘层的堆叠，其中导电图案的边缘设置在沿着第一方向间隔开的点处以提供布置为阶梯布置中的各台阶的导电焊盘。多个沟道结构在垂直于第一方向的第二方向上延伸穿过导电图案结构，并且多个虚设沟道结构在第二方向上延伸穿过导电焊盘。各接触插塞设置在导电焊盘上。导电焊盘中的第一个具有从其穿过的具有第一宽度的第一类虚设沟道结构。导电焊盘中的第二个具有从其穿过的第二类虚设沟道结构，第二类虚设沟道结构具有与第一宽度不同的第二宽度。虚设沟道结构的宽度可以从导电焊

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盘中的最上面的一个朝向导电焊盘中的最下面的一个增大，并且穿过相应的导电焊盘的虚设沟道结构的数量可以从导电焊盘中的最上面的一个朝向导电焊盘中的最下面的一个减少。

[0008] 在示例实施方式中，通过虚设沟道结构的布置，竖直存储器件可以具有稳定的结构。

附图说明

[0009] 从以下结合附图进行的详细描述，示例实施方式将被更清楚地理解。图1至图20表现了如这里描述的非限制性的示例实施方式。

[0010] 图1A和图2分别是示出根据示例实施方式的竖直存储器件的平面图和截面图；

[0011] 图1B是示出根据示例实施方式的竖直存储器件的平面图；

[0012] 图3至图15是示出根据示例实施方式的制造竖直存储器件的方法的多个阶段的截面图、平面图和透视图；

[0013] 图16和图17分别是示出根据示例实施方式的竖直存储器件的平面图和截面图；

[0014] 图18是示出根据示例实施方式的竖直存储器件的平面图；

[0015] 图19是示出根据示例实施方式的竖直存储器件中的存储单元的布置的平面图；以及

[0016] 图20是示出根据示例实施方式的竖直存储器件的平面图。

具体实施方式

[0017] 图1A和图2分别是示出根据示例实施方式的竖直存储器件的平面图和截面图。图1B是示出根据示例实施方式的竖直存储器件的平面图。

[0018] 参照图1A和图2，基板100可以包括第一区域R1和第二区域R2，存储单元可以三维地形成在第一区域R1上，与存储单元连接的布线可以形成在第二区域R2上。在示例实施方式中，第二区域R2可以在第一方向上与第一区域R1的边缘部分相邻。

[0019] 导电图案结构140和沟道结构118a可以形成在第一区域R1上。焊盘结构142、虚设沟道结构118b和接触插塞144可以形成在第二区域R2上。

[0020] 导电图案结构140和沟道结构118a是多个存储单元的组成部分。焊盘结构142可以用作用于将电信号传输到导电图案结构140以及从导电图案结构140传输电信号的布线。

[0021] 基板100可以包括半导体材料。基板100可以例如包括硅基板、锗基板或硅锗基板。

[0022] 在下文，将描述形成在第一区域R1中的导电图案结构140。

[0023] 导电图案结构140可以包括以交错的方式交替堆叠的导电图案126和绝缘层102。导电图案126可以沿着第三方向间隔开，该第三方向基本上垂直于基板100的上表面。

[0024] 导电图案结构140可以在第一方向上延伸。在示例实施方式中，多个导电图案结构140可以沿着第二方向间隔开，第二方向基本上垂直于第一方向。

[0025] 导电图案结构140中的导电图案126可以包括接地选择线(GSL)、串选择线(SSL)以及在GSL和SSL之间的多条字线。

[0026] 导电图案126可以包括金属。在示例实施方式中，导电图案126可以包括金属图案和阻挡图案。金属图案可以包括例如钨、铜、钴、铝等，阻挡图案可以包括例如钛、钛氮化物、

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钽、钽氮化物等。

[0027] 在下文，将描述形成在第二区域R2上的焊盘结构142。

[0028] 焊盘结构142可以接触导电图案结构140的边缘部分。具体地，导电图案结构140和焊盘结构142可以合并成沿着第一方向延伸的一体。

[0029] 焊盘结构142可以包括交错的导电图案126和绝缘层102。焊盘结构142中的导电图案126和导电图案结构140中的导电图案126可以合并成包括基本上相同的材料的一体。此外，焊盘结构142中的绝缘层102和导电图案结构140中的绝缘层102可以合并成包括基本上相同的材料的一体。

[0030] 在示例实施方式中，焊盘结构142的边缘部分可以具有阶梯布置。具体地，导电图案126的边缘可以布置成阶梯配置形状，其中导电图案126在第三方向上具有不同的层级。具有不同层级的导电图案126的边缘可以用作焊盘，焊盘上可以分别形成接触插塞。在示例实施方式中，焊盘结构142中的焊盘的数量可以与导电图案结构140中的堆叠的导电图案126的数量基本上相同。

[0031] 在示例实施方式中，焊盘结构142可以包括在第一方向和第二方向的每个上的台阶部分。例如，如图11所示，焊盘结构142可以包括分别在第一方向上设置在4个层级处的4个台阶和分别在第二方向上设置在每个层级中的2个子层级处的2个台阶。因此，焊盘结构142可以具有分别在8个不同的子层级处的8个台阶。此外，八个导电图案126可以堆叠在第一区域R1中。

[0032] 第一上绝缘层间层108可以覆盖焊盘结构142。第二上绝缘层间层109可以形成在第一上绝缘层间层108和导电图案结构140上。

[0033] 第一上绝缘层间层108和第二上绝缘层间层109中的每个的上表面可以是基本上平坦的。因此，第一上绝缘层间层108和第二上绝缘层间层109在焊盘结构142上的厚度可以大于第二上绝缘层间层109在导电图案结构140上的厚度。

[0034] 沟道结构118a可以延伸穿过导电图案结构140，并可以具有柱形。虚设沟道结构118b可以延伸穿过第一上绝缘层间层108和焊盘结构142，并可以具有柱形。

[0035] 在示例实施方式中，各个半导体图案114可以形成在基板100和沟道结构118a中的相应沟道结构之间。各个半导体图案114也可以形成在基板100和虚设沟道结构118b中的相应虚设沟道结构之间。在此情况下，沟道结构118a和虚设沟道结构118b中的每个可以形成在相应的半导体图案114上。在某些示例实施方式中，沟道结构118a和虚设沟道结构118b中的每个可以直接接触基板100，即半导体图案114可以被去除。

[0036] 沟道结构118a和虚设沟道结构118b可以具有基本上相同的分层结构。在示例实施方式中，沟道结构118a和虚设沟道结构118b中的每个可以包括电介质结构116a、沟道116b和填充绝缘图案116c。在示例实施方式中，沟道116b可以具有中空圆柱形状或杯状形状。沟道116b可以包括多晶硅或单晶硅。沟道116b的一部分可以掺杂有p型杂质，例如硼。填充绝缘图案116c可以形成在沟道116b上以填充沟道116b的内部空间。填充绝缘图案116c可以包括绝缘材料，例如硅氧化物。

[0037] 在某些示例实施方式中，沟道116b可以具有实心圆柱形状或柱形。在这样的实施方式中，可以没有填充绝缘图案116c。电介质结构116a可以围绕沟道116b的外侧壁。电介质结构116a可以包括层叠在沟道116b的外侧壁上的隧道绝缘层、电荷存储层和阻挡电介质

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层。阻挡电介质层可以包括氧化物，例如硅氧化物或金属氧化物(例如铪氧化物或铝氧化物)。电荷存储层可以包括氮化物(例如硅氮化物)或者金属氧化物。隧道绝缘层可以包括氧化物，例如硅氧化物。半导体图案114可以例如包括多晶硅或单晶硅。

[0038] 在示例实施方式中，沟道结构118a和虚设沟道结构118b还可以包括在电介质结构116a、沟道116b和填充绝缘图案116c上的上导电图案120。上导电图案120可以例如包括多晶硅。

[0039] 沟道结构118a可以具有第一宽度。在示例实施方式中，沟道结构118a可以具有均匀的宽度。然而，虚设沟道结构118b可以具有根据其位置而变化的宽度。每个虚设沟道结构118b可以具有与第一宽度基本上相同或大于第一宽度的宽度。

[0040] 根据虚设沟道结构118b的位置，每单位面积的虚设沟道结构118b的数量(或虚设沟道结构118b的密度)可以变化。例如，在特定台阶处的虚设沟道结构118b的宽度相对大的情况下，形成在该特定台阶处的虚设沟道结构118b的数量可以减少。

[0041] 虚设沟道结构118b的宽度可以从焊盘结构142的与第一区域R1相邻的部分到焊盘结构142的边缘部分逐渐增大。具体地，在焊盘结构142中，虚设沟道结构118b的宽度可以在第一方向上从上部的台阶到下部的台阶逐渐增大。在焊盘结构142中，虚设沟道结构118b的数量可以在第一方向上从上部的台阶到下部的台阶逐渐减少。在示例实施方式中，形成在各台阶处的虚设沟道结构118b的数量可以不同。

[0042] 在某些示例实施方式中，如图1B所示，形成在相邻的台阶处的虚设沟道结构118b的数量可以彼此相等。具体地，第一方向上的相邻台阶可以限定一个台阶组，在图1B中示出第一台阶组G1、第二台阶组G2、第三台阶组G3和第四台阶组G4。在第一至第四台阶组G1、G2、G3和G4的每个中的相邻台阶处形成的虚设沟道结构118b的数量可以彼此相等。例如，当焊盘结构142包括在第一方向上的40个台阶时，第一方向上的10个台阶可以被包括在一个台阶组中(在图1B中，为了便于图示和说明，没有示出每个台阶组的10个台阶，而仅用一个台阶来代表)。形成在第一台阶组G1中的相应的第一至第十台阶处的虚设沟道结构118b的数量可以彼此相等。以同样的方式，形成在第二至第四台阶组G2、G3和G4的每个中的相应台阶处的虚设沟道结构118b的数量可以相等。在焊盘结构142中，虚设沟道结构118b的数量可以从第一台阶组G1至第四台阶组G4逐渐增加。

[0043] 接触插塞144可以穿过第一上绝缘层间层108和第二上绝缘层间层109，并接触焊盘结构142中的导电图案126的上表面。接触插塞144可以形成在相应的台阶上。在示例实施方式中，接触插塞144可以每个包括阻挡图案和金属图案。

[0044] 在示例实施方式中，接触插塞144可以形成在台阶的中央部分上。因此，接触插塞144可以基本上沿着在第一方向和第二方向上的线布置。

[0045] 如上所述，在焊盘结构142中，随着形成在各个台阶处的虚设沟道结构118b的宽度的增大，形成在各个台阶处的虚设沟道结构118b的数量可以减少。因此，在焊盘结构142的第一方向上的各台阶中，没有被接触插塞144和虚设沟道结构118b占据的剩余面积可以基本上相同。换言之，焊盘结构142中的导电图案126的暴露的上表面可以具有基本上相同的面积。布线(未示出)可以进一步形成在接触插塞144上。

[0046] 图3至图15是示出根据示例实施方式的制造竖直存储器件的方法的步骤的截面图、平面图和透视图。更具体地，图3、图4、图7、图9、图12、图13和图14是截面图，图5、图8、图

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10和图15是平面图，图6和图11是透视图。

[0047] 参照图3，初始模结构106可以形成在基板100的第一区域R1和第二区域R2上。绝缘层102和牺牲层104可以交替地形成在基板100上以形成初始模结构106。在示例实施方式中，最下面的绝缘层102可以用作焊盘绝缘层。最上面的绝缘层102可以具有比初始模结构106中的其它绝缘层102大的厚度。

[0048] 在示例实施方式中，绝缘层102可以由基于氧化物的材料例如硅氧化物、SiOC、SiOF等形成。在示例实施方式中，牺牲层104可以由基于氮化物的材料(例如硅氮化物和/或硅硼氮化物)形成。

[0049] 参照图4、图5和图6，第二区域R2上的初始模结构106的边缘部分可以被顺序地蚀刻以形成初始台阶模结构106a。在示例实施方式中，第二区域R2上的初始台阶模结构106a可以具有在第一方向和第二方向的每个上的阶梯布置。

[0050] 第一区域R1上的初始台阶模结构106a的牺牲层104可以通过后续工艺转换成存储单元的导电图案。

[0051] 在第二区域R2上的初始台阶模结构106a中，每个台阶将用作焊盘，该焊盘电连接到通过后续工艺形成的存储单元的导电图案。在初始台阶模结构106a中，台阶的数量可以等于堆叠的牺牲层104(其被示出为包括104a、104b、104c、104d、104e、104f、104g和104h)的台阶的数量。随着台阶在第二方向上的数量增加，台阶在第一方向上的数量可以减少。台阶在第一方向和第二方向上的数量可以变化。如图5和图6所示，当在第二方向上形成2个台阶时，台阶在第一方向上的数量可以是堆叠的牺牲层104的数量的一半。

[0052] 参照图7和图8，第一上绝缘层间层108可以形成在初始台阶模结构106a上。第一上绝缘层间层108的上表面可以是基本上平坦的。

[0053] 在示例实施方式中，第一上绝缘层间层108可以通过沉积包括例如硅氧化物、SiOC或SiOF的氧化物层以及平坦化该氧化物层的上表面而形成。平坦化工艺可以包括化学机械抛光(CMP)工艺和/或回蚀刻工艺。

[0054] 初始台阶模结构106a和第一上绝缘层间层108可以被各向异性蚀刻以形成暴露基板100的上表面的多个孔。孔可以穿过初始台阶模结构106a和第一上绝缘层间层108形成。孔可以包括沟道孔110和虚设沟道孔112。沟道孔110可以形成为穿过第一区域R1上的初始台阶模结构106a，虚设沟道孔112可以形成为穿过第二区域R2上的初始台阶模结构106a。沟道结构可以形成在沟道孔110中，并且虚设沟道结构可以形成在虚设沟道孔112中。

[0055] 沟道孔110可以均匀地具有第一宽度W1。然而，虚设沟道孔112可以根据其位置而具有不同的宽度。每个虚设沟道孔112可以具有与第一宽度W1基本上相同的宽度或大于第一宽度W1的宽度。

[0056] 根据虚设沟道孔112的位置，每单位面积的虚设沟道孔112的数量(或虚设沟道结构的密度)可以变化。在形成在特定台阶处的虚设沟道孔112的宽度相对大的情况下，形成在该特定台阶处的虚设沟道孔112的密度可以相对小。在下文，描述用于形成沟道孔110和虚设沟道孔112的操作。

[0057] 沟道孔110可以形成为穿过第一区域R1中的初始台阶模结构106a，在第二区域R2的阶梯台阶部分之外。绝缘层102和牺牲层104可以被蚀刻以形成沟道孔110。其中形成沟道孔110的被蚀刻的层可以基本上彼此相同，而与其位置无关。因此，沟道孔110可以具有均匀

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的第一宽度W1。

[0058] 虚设沟道孔112可以形成为穿过阶梯区域中的初始台阶模结构106a和第一上绝缘层间层108。由于第二区域R2上的初始台阶模结构106a可以具有阶梯布置，所以第一上绝缘层间层108可以根据其位置具有不同的厚度。因此，其中形成虚设沟道孔112的被蚀刻的层可以根据其位置而变化。例如，初始台阶模结构106a的上部台阶上的第一上绝缘层间层108可以相对薄，而初始台阶模结构106a的下部台阶上的第一上绝缘层间层108可以相对厚。初始台阶模结构106a上的第一上绝缘层间层108的厚度可以朝向初始台阶模结构106a的边缘增大。

[0059] 初始台阶模结构106a的边缘部分处的虚设沟道孔112可以通过蚀刻第一上绝缘层间层108的厚部分和初始台阶模结构106a的薄部分而形成。在初始台阶模结构106a的与第一区域R1相邻的部分处的虚设沟道孔可以通过蚀刻第一上绝缘层间层108的薄部分和初始台阶模结构106a的厚部分而形成。

[0060] 初始台阶模结构106a可以包括交错的硅氧化物层和硅氮化物层的堆叠，并且第一上绝缘层间层108可以包括硅氧化物。因此，当初始台阶模结构106a和第一上绝缘层间层108被一起蚀刻时，第一上绝缘层间层108可以以较大的速率蚀刻。在用于形成沟道孔110和虚设沟道孔112的各向异性蚀刻工艺中，第二区域R2上的初始台阶模结构106a和第一上层间绝缘层108的蚀刻可以在第一区域R1上的初始台阶模结构106a的蚀刻暴露基板100之前暴露基板100。换言之，基板100可以在初始台阶模结构106a的边缘部分处被首先暴露。

[0061] 因此，各向异性蚀刻工艺可以在基板100在边缘部分中被暴露之后继续。因此，每个孔的上侧壁可以被进一步蚀刻，使得虚设沟道孔112的宽度可以增大。因此，虚设沟道孔112的宽度可以大于沟道孔110的宽度。

[0062] 虚设沟道孔112的宽度可以从初始台阶模结构106a的与第一区域R1相邻的部分到初始台阶模结构106a的边缘部分增大。具体地，虚设沟道孔112的宽度可以从上部台阶到下部台阶以阶梯式的方式增大。

[0063] 随着虚设沟道孔112的宽度增大，所希望的是虚设沟道孔112的密度减小。例如，在初始台阶模结构106a中，虚设沟道孔112的数量可以从上部的台阶到下部的台阶减少。虚设沟道孔112的密度可以从上部的台阶到下部的台阶减小。

[0064] 参照图9，沟道结构118a可以形成在每个沟道孔110中。虚设沟道结构118b可以形成在每个虚设沟道孔112中。

[0065] 在示例实施方式中，各个半导体图案114可以形成在基板100上且在沟道结构118a和虚设沟道结构118b中的相应一个之下。第二上绝缘层间层109可以形成在第一上绝缘层间层108和初始台阶模结构106a上。第二上绝缘层间层109的上表面可以是平坦的。

[0066] 半导体图案114可以通过采用由沟道孔110和虚设沟道孔112暴露的基板100的顶表面作为籽晶的选择性外延生长(SEG)工艺形成。沟道结构118a可以形成在半导体图案114上以填充沟道孔110，虚设沟道结构118b可以形成在半导体图案114上以填充虚设沟道孔112。沟道结构118a和虚设沟道结构118b可以具有基本上相同的分层结构。在示例实施方式中，沟道结构118a和虚设沟道结构118b可以每个包括电介质结构116a、沟道116b和填充绝缘图案116c。电介质结构116a可以包括隧道绝缘层、电荷存储层和阻挡电介质层。在示例实施方式中，上导电图案120可以进一步形成在电介质结构116a、沟道116b和填充绝缘图案

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116c上。上导电图案120可以例如由多晶硅形成。

[0067] 虚设沟道结构118b可以形成为填充虚设沟道孔112，使得虚设沟道结构118b的宽度和布置可以分别与虚设沟道孔112的宽度和布置基本上相同。因此，虚设沟道结构118b的宽度可以从初始台阶模结构106a的与第一区域R1相邻的部分到初始台阶模结构106a的边缘部分增大。每单位面积的虚设沟道结构118b的数量可以从初始台阶模结构106a的与第一区域R1相邻的部分到初始台阶模结构106a的边缘部分减少。在初始台阶模结构106a中，虚设沟道结构118b的数量可以从上部的台阶到下部的台阶减少。

[0068] 参照图10和图11，初始台阶模结构106a以及第一上绝缘层间层108和第二上绝缘层间层109可以被各向异性蚀刻以形成沿着第一方向延伸的开口122。因此，初始台阶模结构106a可以被分开以在开口122之间形成台阶模结构130。基板100的上表面可以被开口122暴露。

[0069] 在图11中，沟道结构118a和虚设沟道结构118b没有被示出，而仅示出台阶模结构130。第一区域R1上的台阶模结构130可以通过后续工艺转变成导电图案结构。第二区域R2上的台阶模结构130可以包括在第一方向和第二方向的每个上的台阶。

[0070] 在下面说明的实施方式中，每个台阶模结构130在第一方向上具有4个台阶并在第二方向上具有2个台阶。因此，台阶模结构130具有在不同平面中的8个台阶。

[0071] 参照图12，由开口122暴露的牺牲层104可以被去除以在绝缘层102之间形成间隙124。在示例实施方式中，牺牲层104可以通过各向同性蚀刻工艺去除。在去除牺牲层104之后，绝缘层102保持被沟道结构118a和虚设沟道结构118b支撑。

[0072] 在其中形成具有相对小的宽度的虚设沟道结构118b的区域中，台阶模结构130可以由大量的虚设沟道结构118b支撑。因此，台阶模结构130中的绝缘层102之间的间隙124可以被保持。

[0073] 在其中形成具有相对大的宽度的虚设沟道结构118b的区域中，虚设沟道结构118b的数量可以较少。由于虚设沟道结构118b具有相对大的宽度，所以台阶模结构130可以由少量的虚设沟道结构118b稳定地支撑。此外，可以确保虚设沟道结构118b之间的接触插塞区域。因此，可以降低虚设沟道结构118b和接触插塞144之间短路的可能性。

[0074] 参照图13，导电层可以形成为填充间隙124，使得导电图案126可以形成在第一区域R1和第二区域R2上。

[0075] 因此，包括堆叠的导电图案126和绝缘层102的导电图案结构140可以形成在第一区域R1上。包括堆叠的导电图案126和绝缘层102并具有阶梯布置的焊盘结构142可以形成在第二区域R2上。

[0076] 焊盘结构142中的在第一方向上堆叠的各层中除了虚设沟道结构118b之外的面积可以基本上相同。因此，各层中的用导电层填充的间隙124的体积可以是均一的，并且用于形成导电图案的填充间隙124的导电材料的量可以是均一的。

[0077] 绝缘图案146(参照图15)可以形成为填充开口122(参照图10和图11)。参照图14和图15，各接触插塞144可以穿过第一上绝缘层间层108和第二上绝缘层间层109形成在焊盘结构142中的导电图案126上。接触插塞144可以与虚设沟道结构118b间隔开。

[0078] 第一上绝缘层间层108和第二上绝缘层间层109以及绝缘层102可以被蚀刻以在焊盘结构142中形成暴露导电图案126的接触孔。阻挡层可以形成在接触孔的内壁上，并且金

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属层可以形成在阻挡层上以填充接触孔。金属层和阻挡层可以被平坦化直到第二上绝缘层间层109被暴露。电连接到接触插塞144的布线(未示出)可以形成在第二上绝缘层间层109上。布线可以在第二方向上延伸。

[0079] 图16和图17分别是示出根据示例实施方式的竖直存储器件的平面图和截面图。图16和图17的竖直存储器件可以具有与图1A和图2中示出的那些元件和/或结构基本上相同或相似的元件和/或结构,除了它包括焊盘结构中的不同台阶布置。

[0080] 参照图16和图17,导电图案结构140和沟道结构118a可以形成在第一区域R1上。焊盘结构142、虚设沟道结构118b和接触插塞144可以形成在第二区域R2上。

[0081] 焊盘结构142的边缘部分可以具有阶梯布置。焊盘结构142中的导电图案126可以具有包括不同平面处的台阶的阶梯布置。焊盘结构142中的焊盘的数量可以与导电图案结构140中的堆叠的导电图案126的数量基本上相同。

[0082] 在示例实施方式中,焊盘结构142可以包括在第一方向上下降的台阶。例如,如图16所示,焊盘结构142可以包括在第一方向上的4个台阶。因此,四个导电图案126可以堆叠在第一区域R1中。

[0083] 虚设沟道结构118b的宽度和布置可以与参照图1A和图2说明的虚设沟道结构118b的宽度和布置基本上相同。在焊盘结构142中,虚设沟道结构118b的宽度可以从上部的台阶到下部的台阶增大。虚设沟道结构118b的数量可以在第一方向上从上部的台阶到下部的台阶减少。

[0084] 竖直半导体器件可以通过与参照图3至图14说明的工艺基本上相同的工艺制造。然而,在参照图4至图6描述的用于形成初始台阶模结构的工艺中,初始模结构可以被图案化以在第一方向上形成台阶。在参照图10说明的用于形成开口122的工艺中,开口122的位置可以改变。也就是,初始台阶模结构可以被分成分开的部分以在开口122之间形成在第一方向上具有台阶的台阶模结构。

[0085] 图18是示出根据示例实施方式的竖直存储器件的平面图。图18的竖直存储器件可以具有与图1A和图2中示出的那些元件和/或结构基本上相同或相似的元件和/或结构,除了接触插塞的布置之外。

[0086] 参照图18,导电图案结构140和沟道结构118a可以形成在第一区域R1上。焊盘结构142、虚设沟道结构118b和接触插塞144可以形成在第二区域R2上。

[0087] 焊盘结构142的边缘部分可以具有与图1A和图2中示出的阶梯布置基本上相同的阶梯布置。接触插塞144可以穿过第一上绝缘层间层108和第二上绝缘层间层109形成在焊盘结构142中的导电图案126的上表面上。

[0088] 接触插塞144可以形成在导电图案126的各台阶上,并且接触插塞144在台阶上的位置可以不被限制。在示例实施方式中,接触插塞144可以不被线性地排列。

[0089] 例如,如图18所示,焊盘结构142中的最下面的台阶上的接触插塞144可以形成在最下面的台阶的中央部分上。然而,接触插塞144可以从下部的台阶到上部的台阶沿着相对于第一方向具有角度的倾斜方向设置。

[0090] 在此情况下,在焊盘结构142中,相邻的接触插塞144之间在第二方向上的距离可以朝向上部的台阶增大。也就是,开口122和上部的台阶上的接触插塞144之间的距离可以相对小。由于相邻的接触插塞144之间在第二方向上的距离可以增大,所以接触插塞144上

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的布线区域可以增加。

[0091] 如上所述，接触插塞144的位置可以不被限制，因此布线可以容易地设置在接触插塞144上。

[0092] 图19是示出根据示例实施方式的竖直存储器件中的存储单元的布置的平面图。图20是示出根据示例实施方式的竖直存储器件的平面图。

[0093] 在下文，参照图20，可以示出图19所示的形成在半导体芯片的边缘部分上的存储单元。

[0094] 参照图20，导电图案结构140和沟道结构118a可以形成在第一区域R1上。焊盘结构142、虚设沟道结构118b和接触插塞144可以形成在第二区域R2上。

[0095] 焊盘结构142的边缘部分可以具有与图1A和图2所示的阶梯布置基本上相同的阶梯布置。接触插塞144可以穿过第一上绝缘层间层108和第二上绝缘层间层109形成在焊盘结构142中的导电图案126的上表面上。

[0096] 根据虚设沟道结构118b的位置，每单位面积的虚设沟道结构118b的数量可以改变。随着虚设沟道结构118b的宽度在连续的台阶中增大，台阶处形成的虚设沟道结构118b的数量可以减少。

[0097] 在焊盘结构142中，虚设沟道结构118b的宽度可以从上部的台阶到下部的台阶增大。然而，当存储单元形成在半导体芯片的边缘部分上时，最下面的台阶处的虚设沟道结构118b的宽度可以小于次最下的台阶处的虚设沟道结构118b的宽度。因此，次最下的台阶处形成的虚设沟道结构118b可以具有较大的宽度。

[0098] 在焊盘结构142中，虚设沟道结构118b的数量可以从上部的台阶到下部的台阶减少。然而，当存储单元形成在半导体芯片的边缘部分上时，最下面的台阶处的虚设沟道结构118b的数量可以大于次最下的台阶处的虚设沟道结构118b的数量。因此，次最下的台阶处形成的虚设沟道结构118b可以在数量上较少。

[0099] 如上所述，穿过焊盘结构中的各层级的导电图案的虚设沟道结构118b的宽度可以彼此不同。随着台阶处的虚设沟道结构118b的宽度增大，形成在该台阶处的虚设沟道结构118b的数量可以减少。通过控制虚设沟道结构118b的宽度和数量，竖直半导体器件可以形成为对于后续处理操作具有高稳定性，如上所述。

[0100] 以上是对示例实施方式的说明而不应被解释为对其进行限制。尽管已经描述了几个示例实施方式，但是本领域技术人员将容易地理解，在示例实施方式中可以有许多修改，而在本质上没有脱离本发明构思的新颖教导和优点。因此，所有这样的修改旨在被包括在本发明构思的范围内，本发明构思的范围在权利要求书中限定。在权利要求中，装置加功能条款旨在覆盖这里描述的执行所述功能的结构，覆盖不仅结构等同物而且等同的结构。因此，将理解，以上是对各种示例实施方式的说明，而不应被解释为限制到所公开的特定示例实施方式，对所公开的示例实施方式的修改以及其它示例实施方式旨在被包括在权利要求书的范围内。

[0101] 本申请要求于2017年5月17日在韩国知识产权局(KIPO)提交的韩国专利申请第10-2017-0060927号的优先权，其内容通过引用整体地结合于此。

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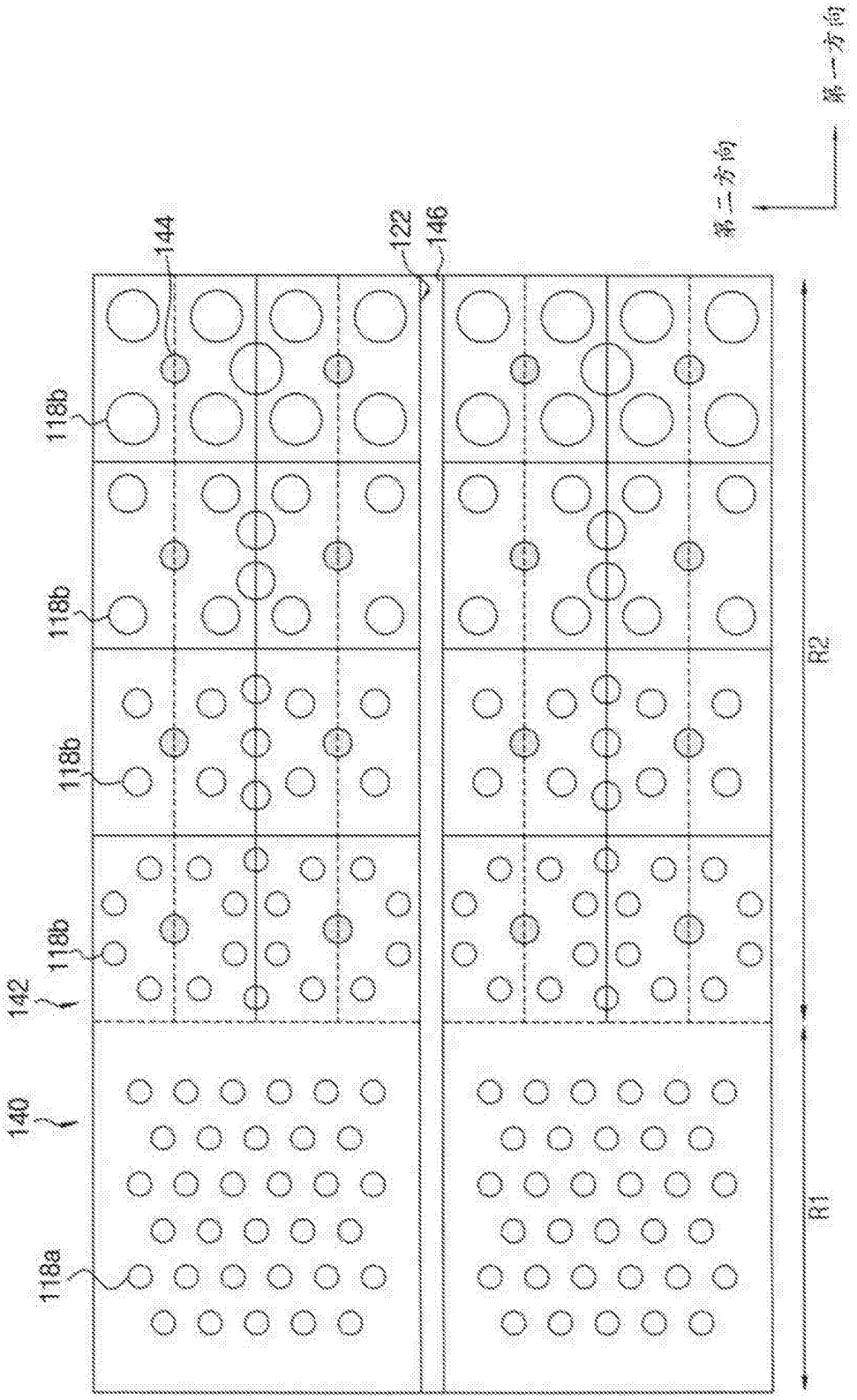


图1A

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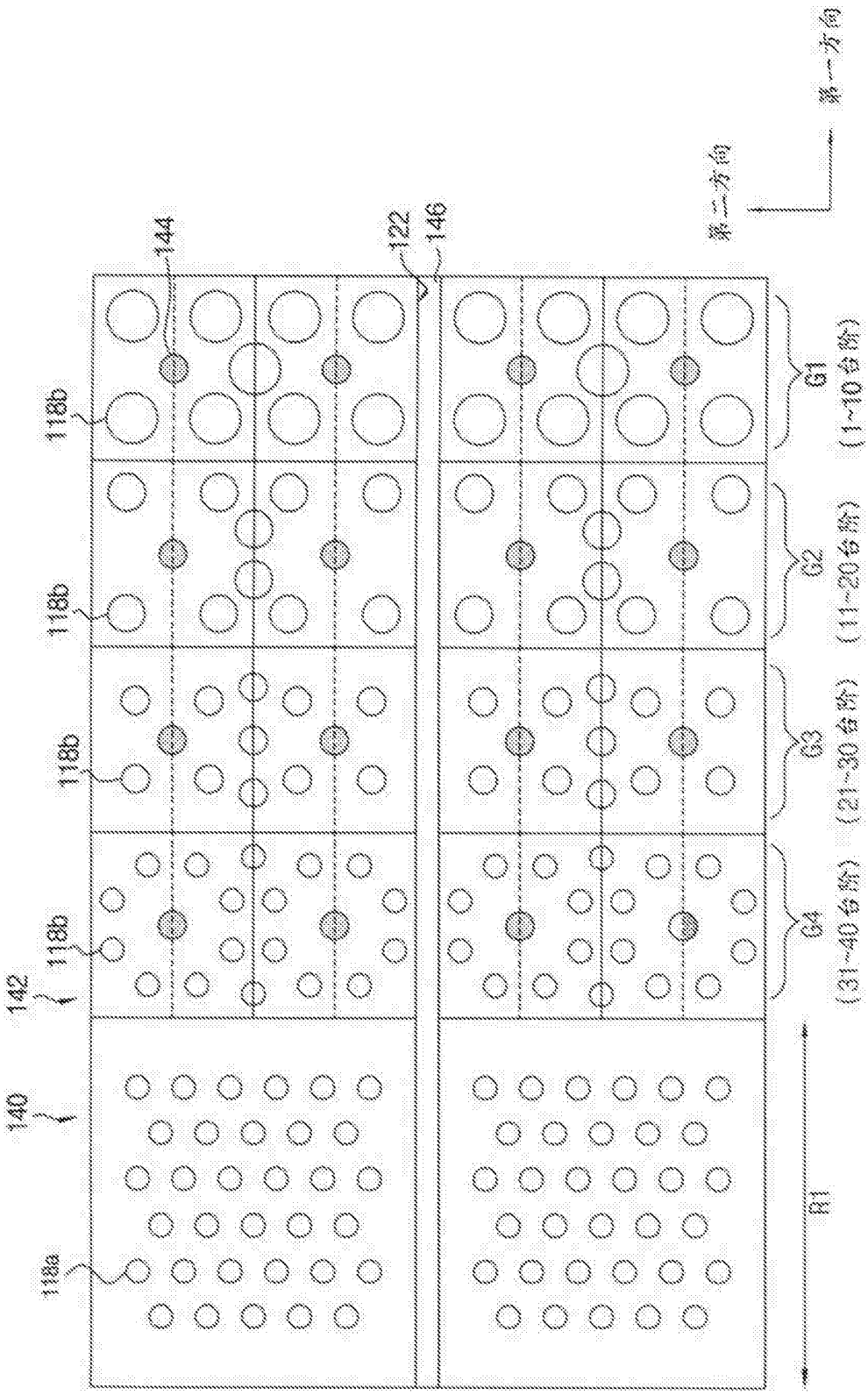


图1B

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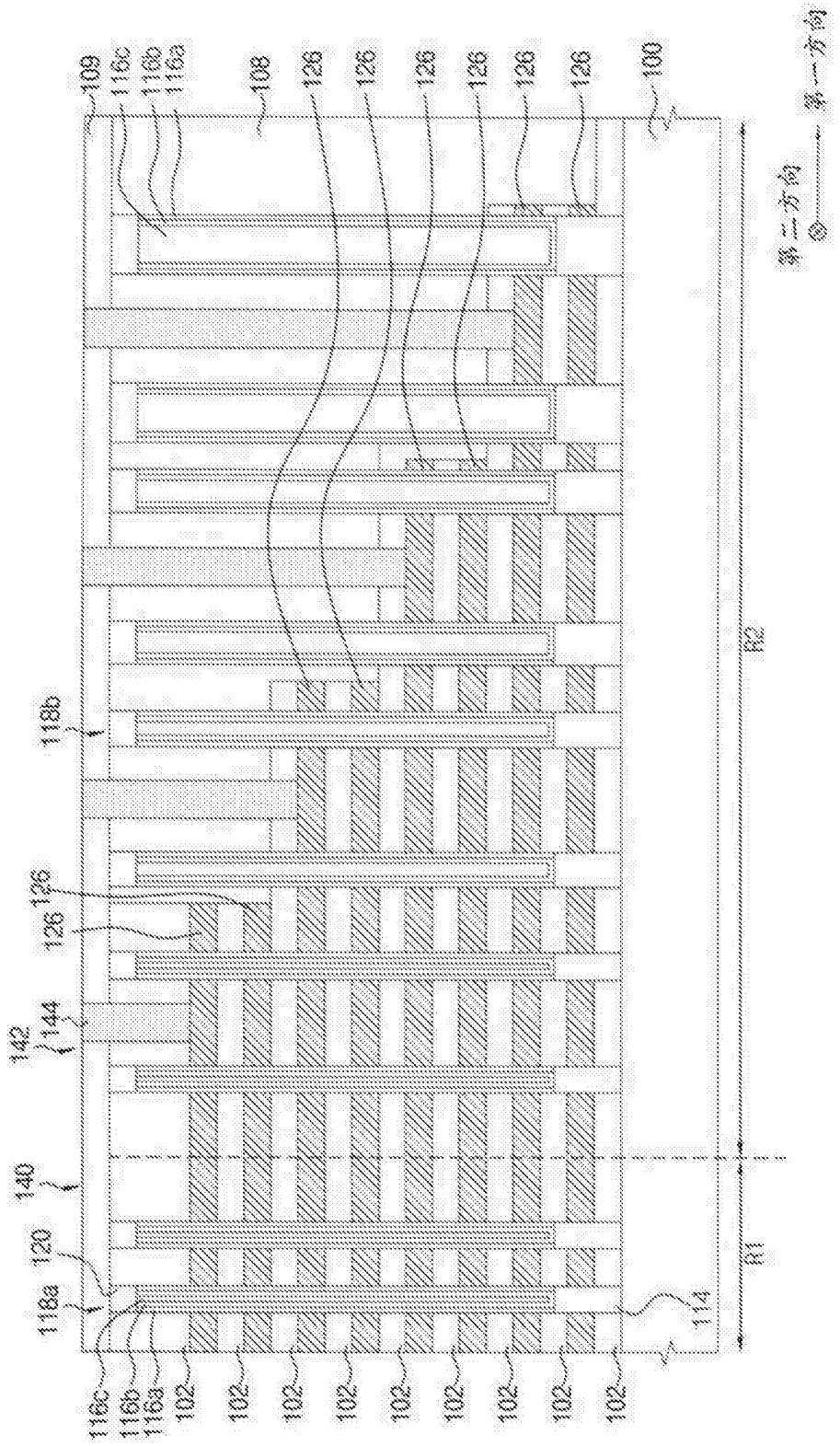


图2

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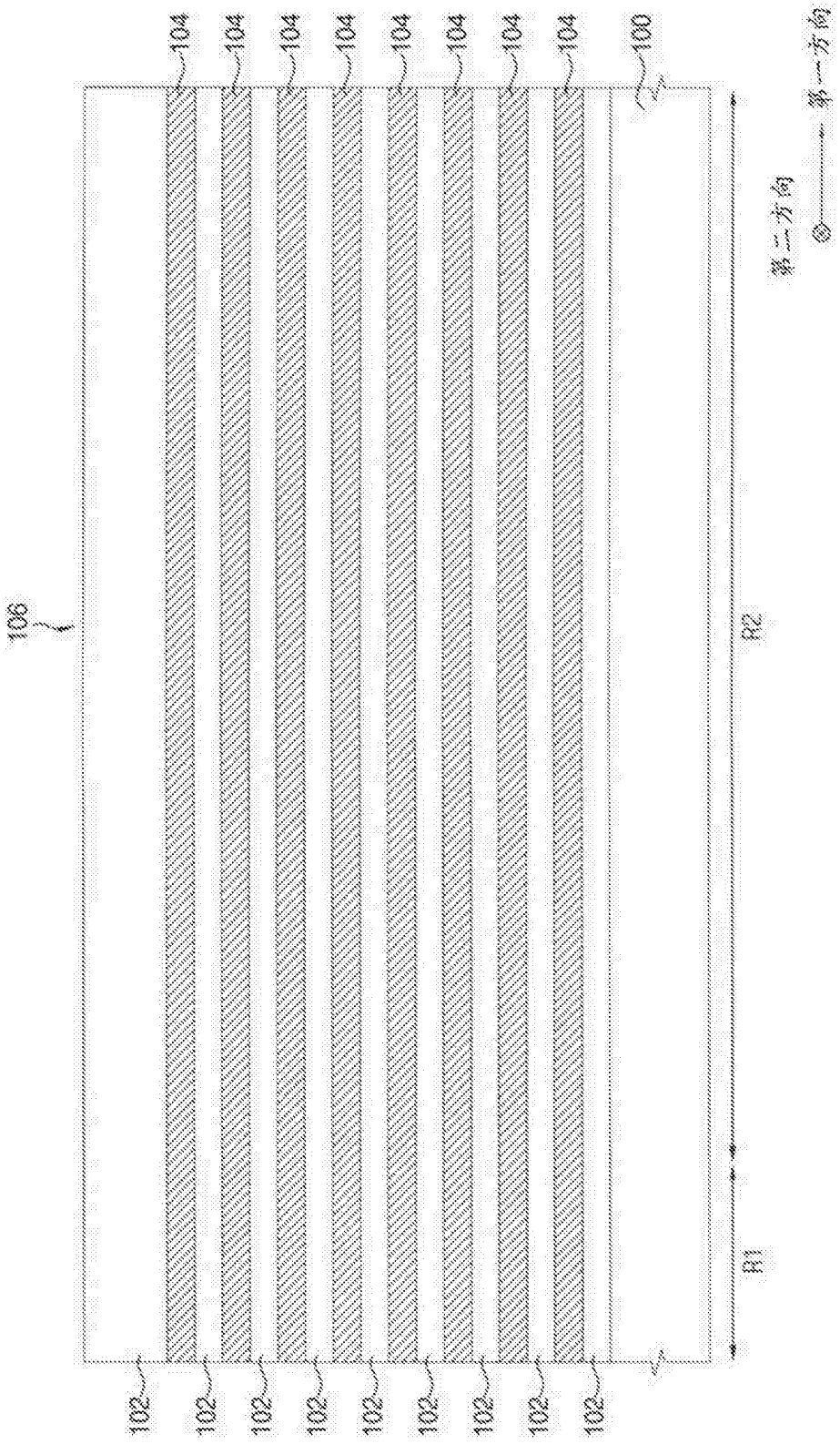


图3

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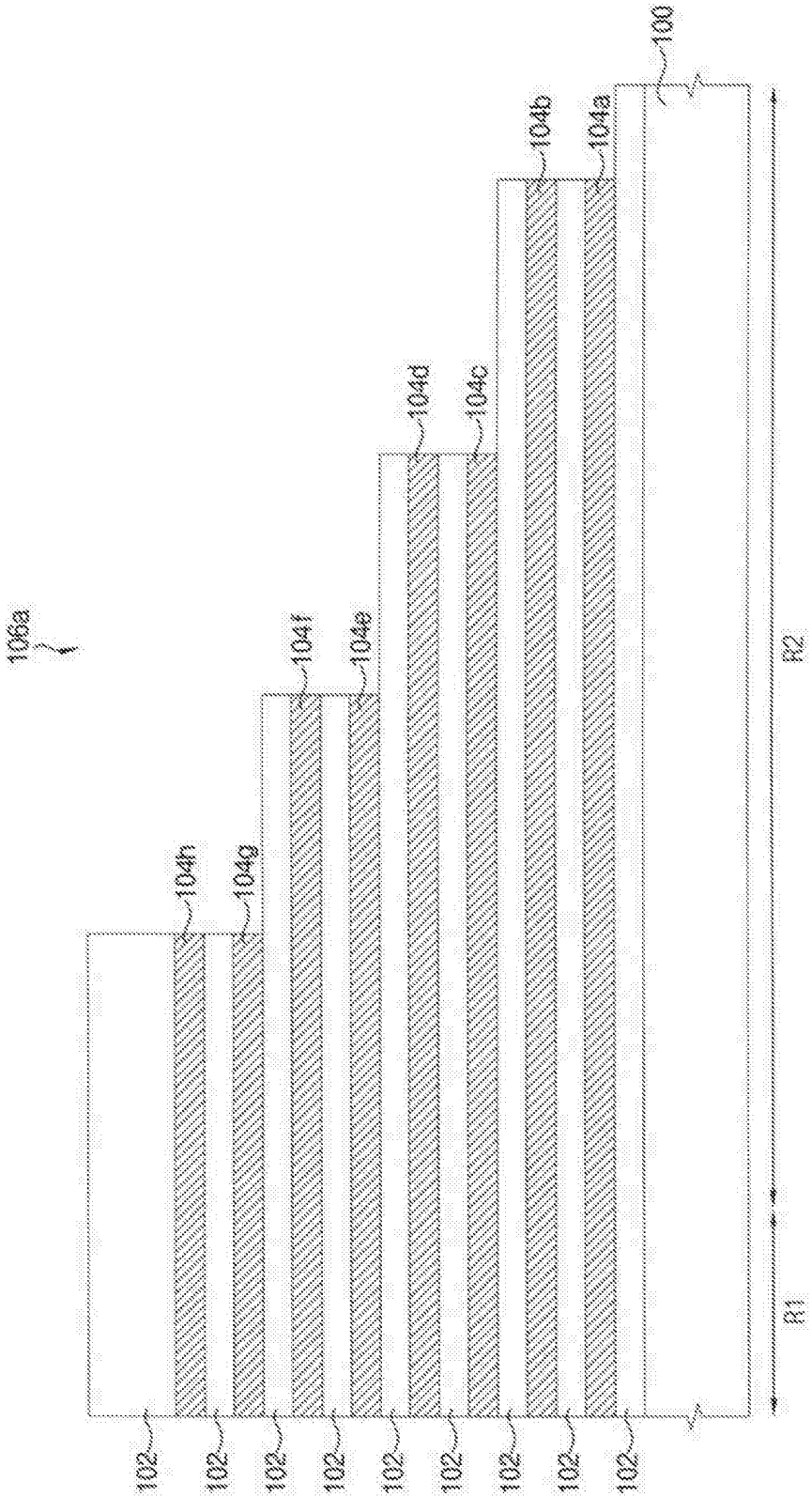


图4

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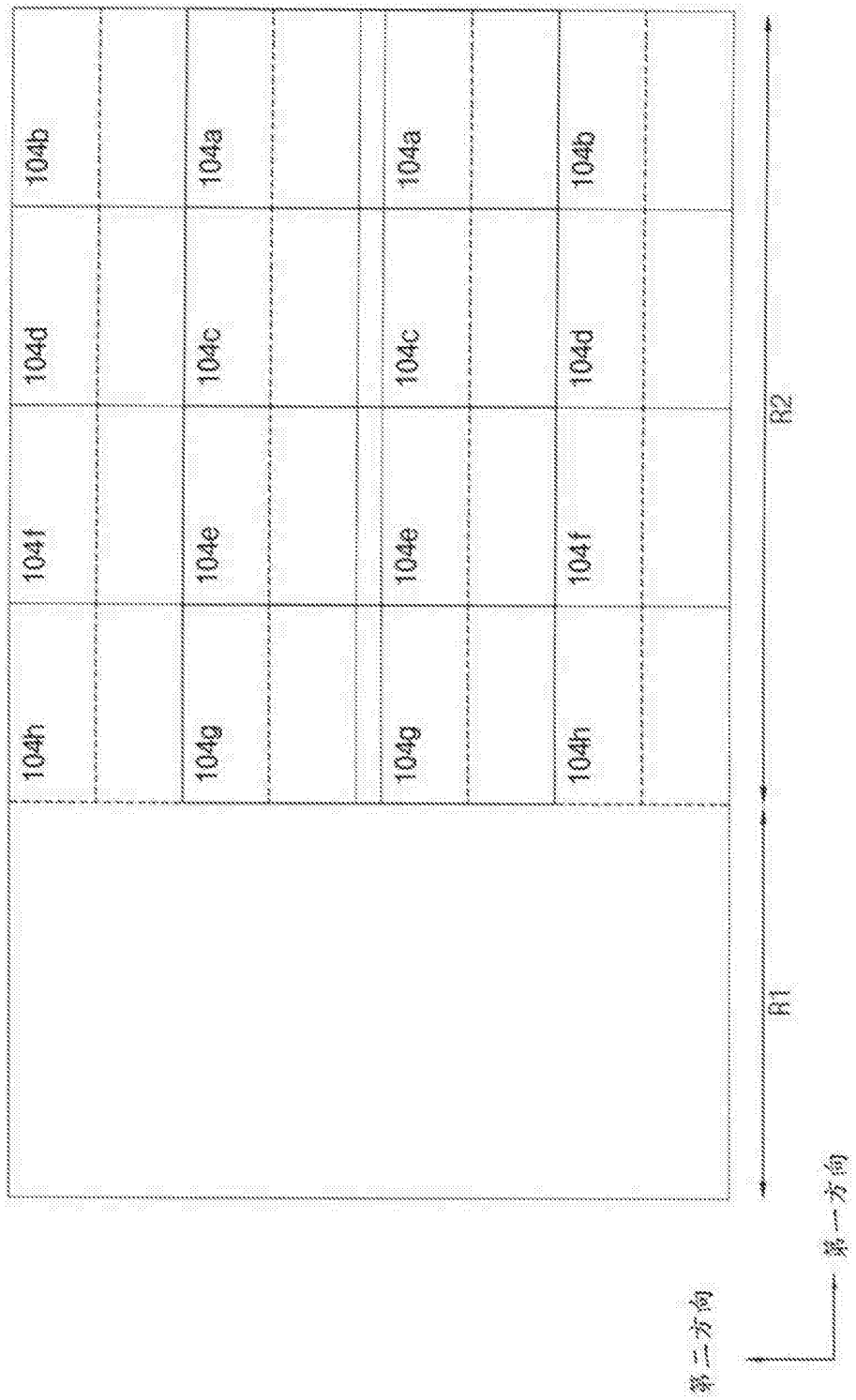


图5

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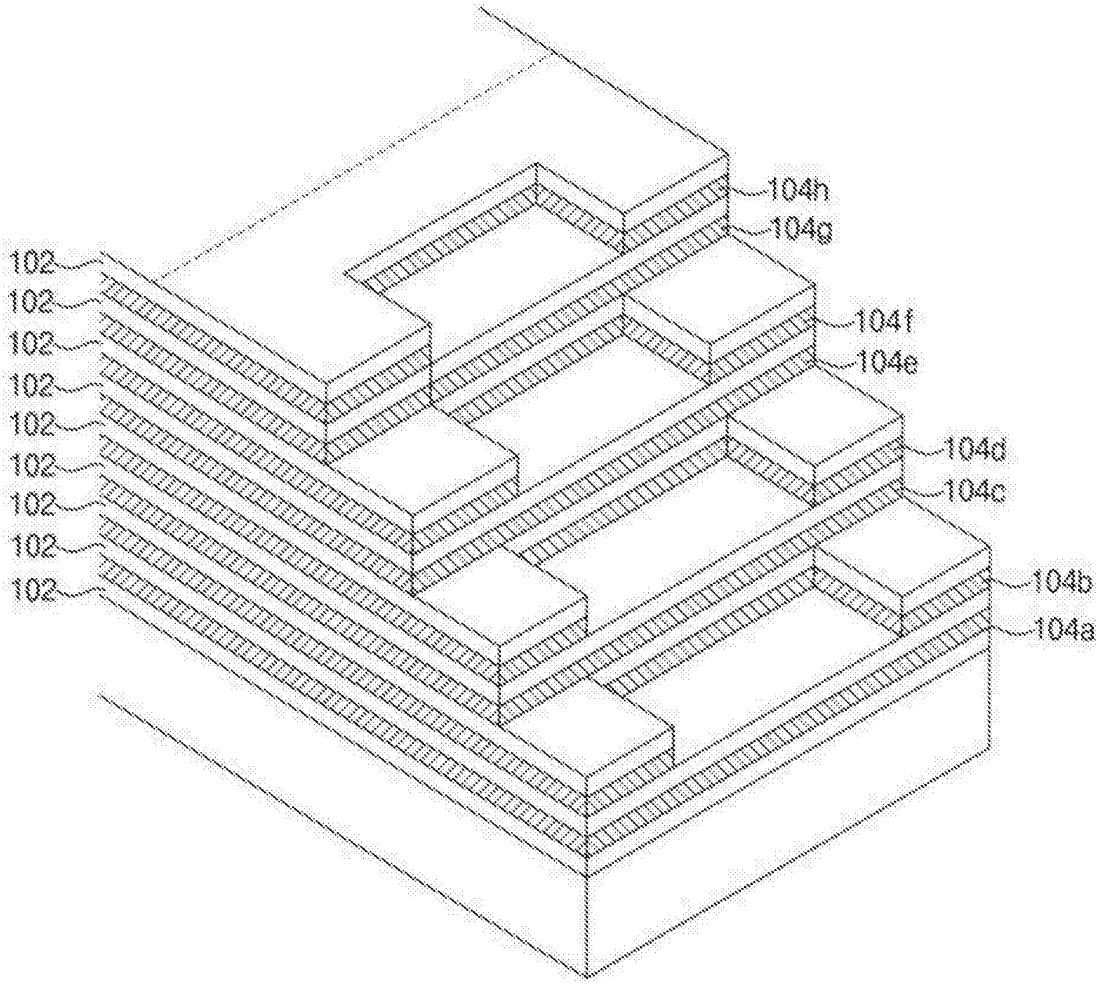


图6

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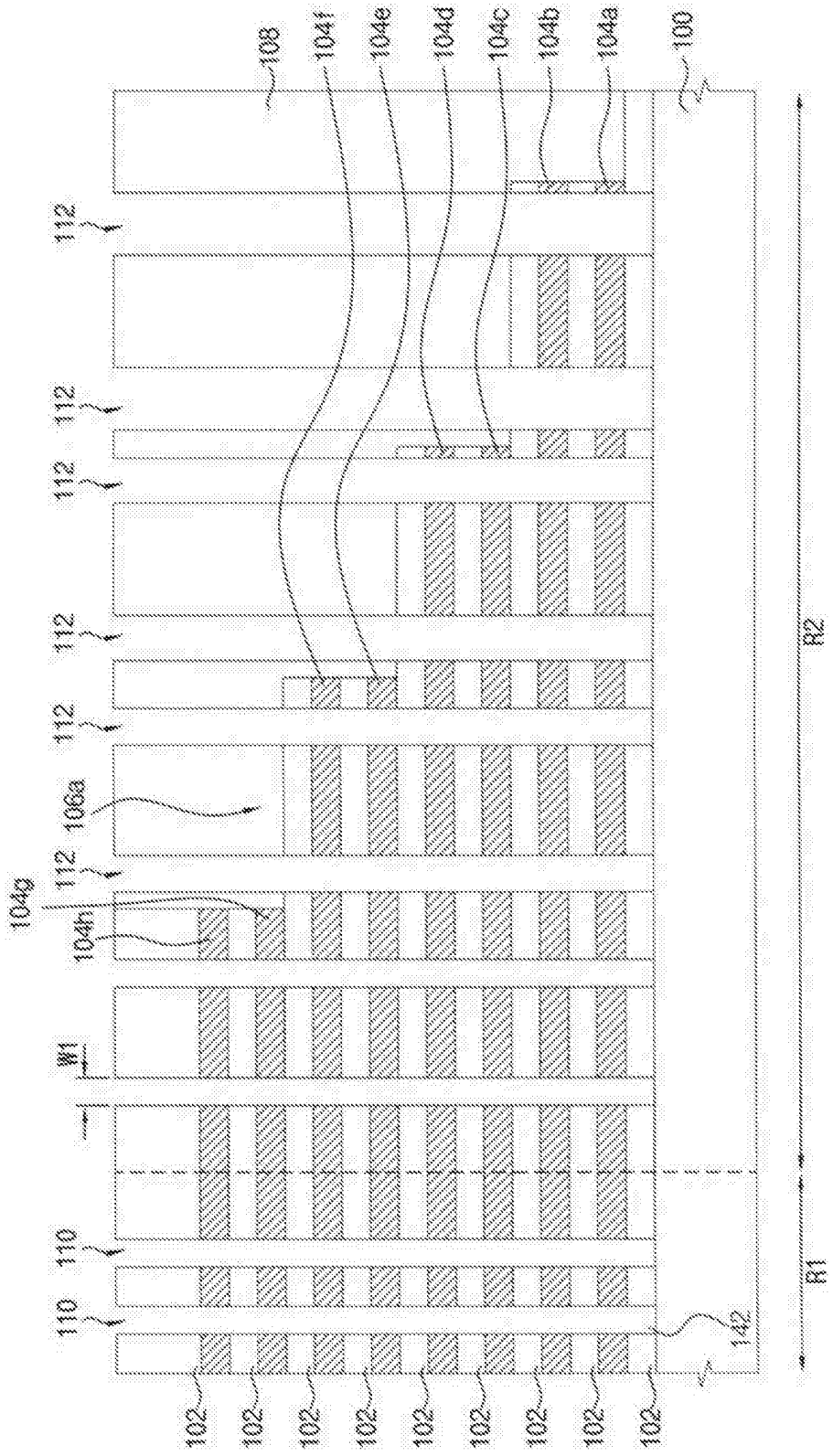


图7

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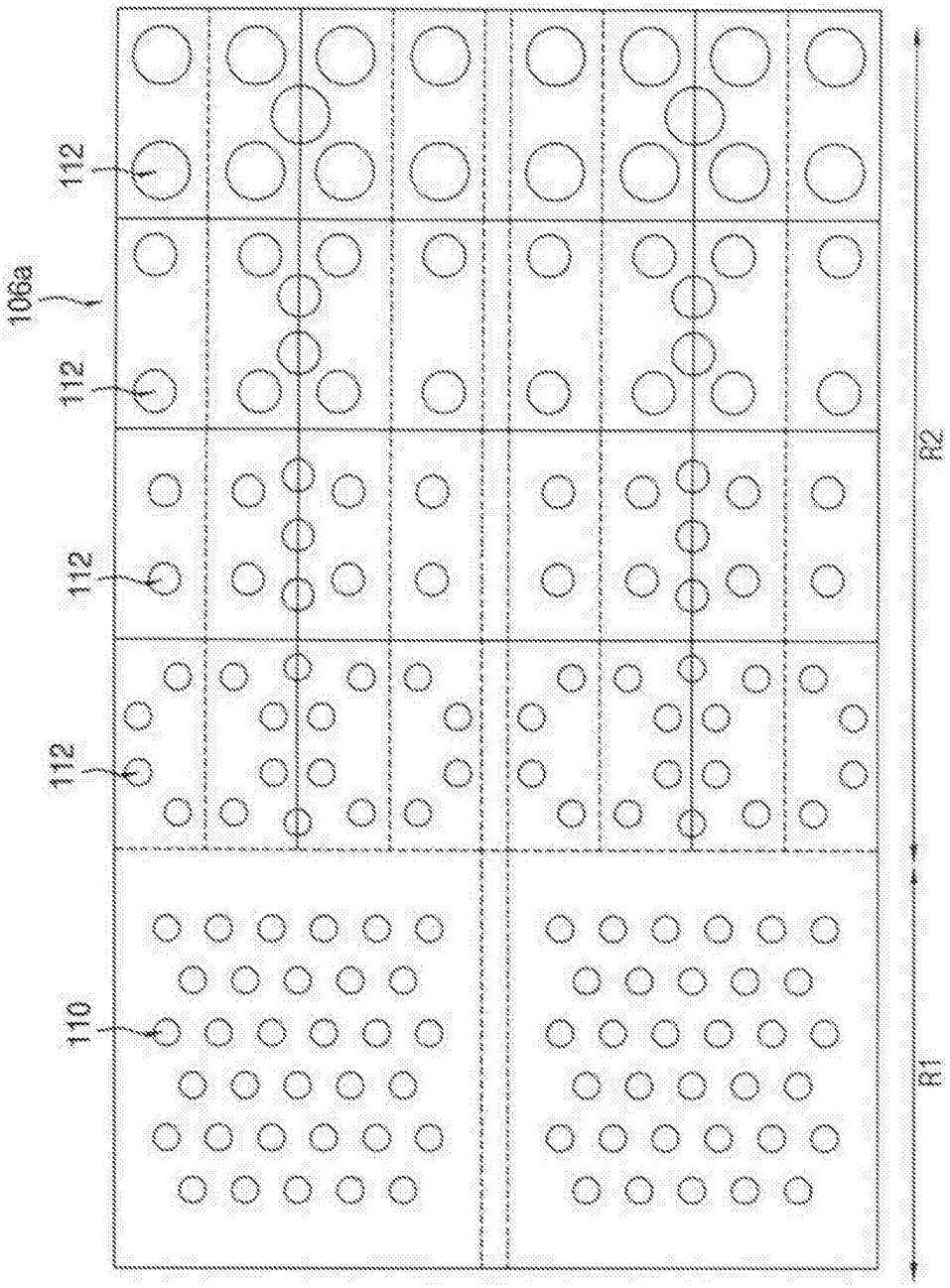


图8

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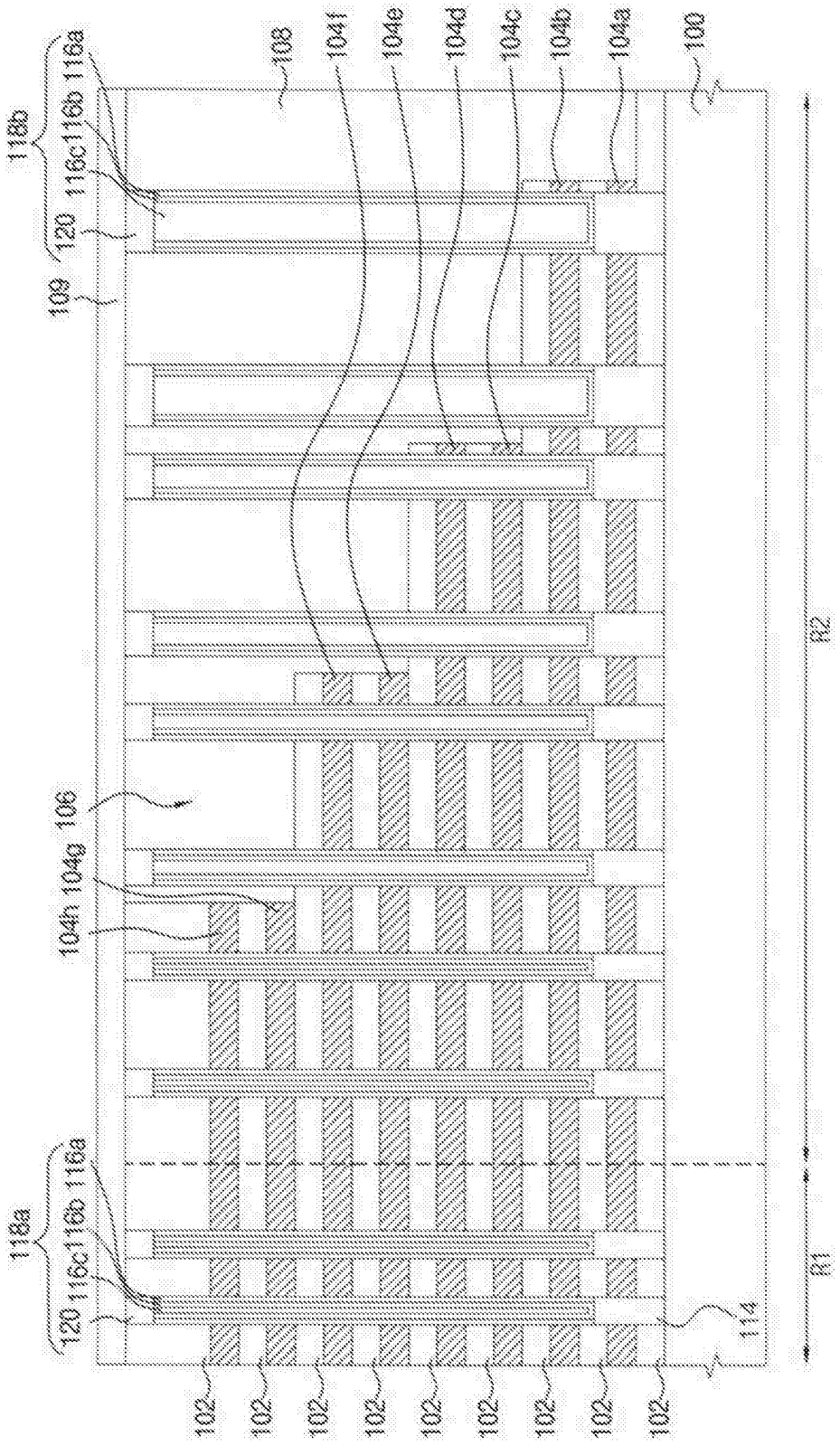


图9

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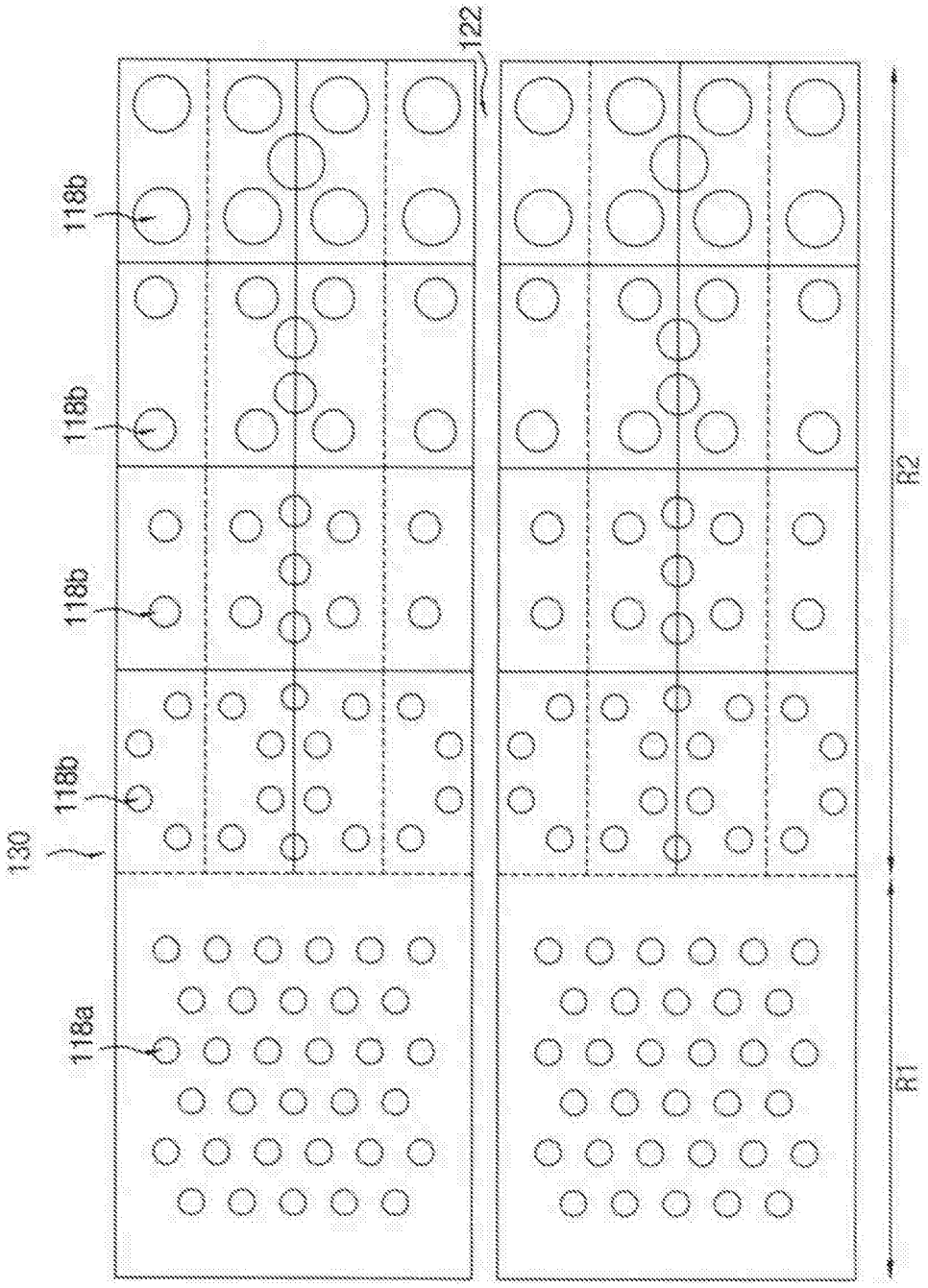


图10

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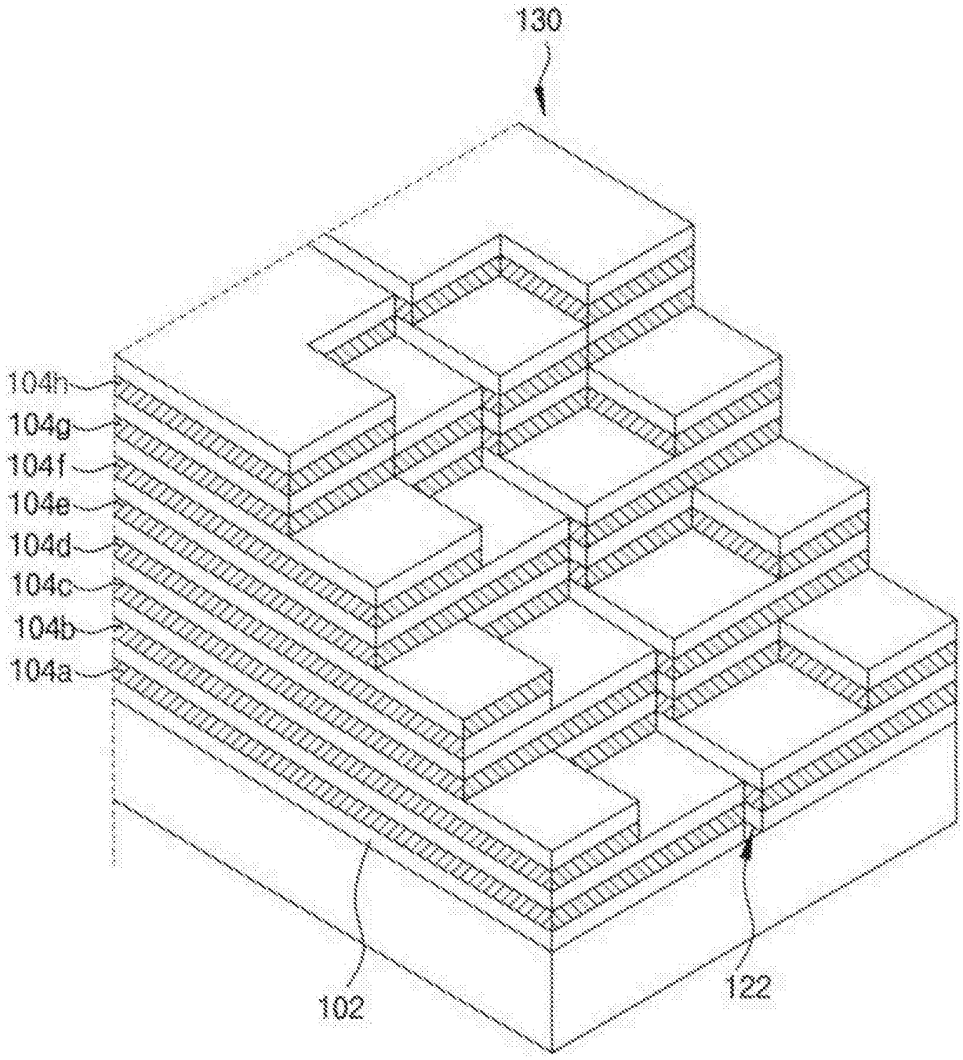


图11

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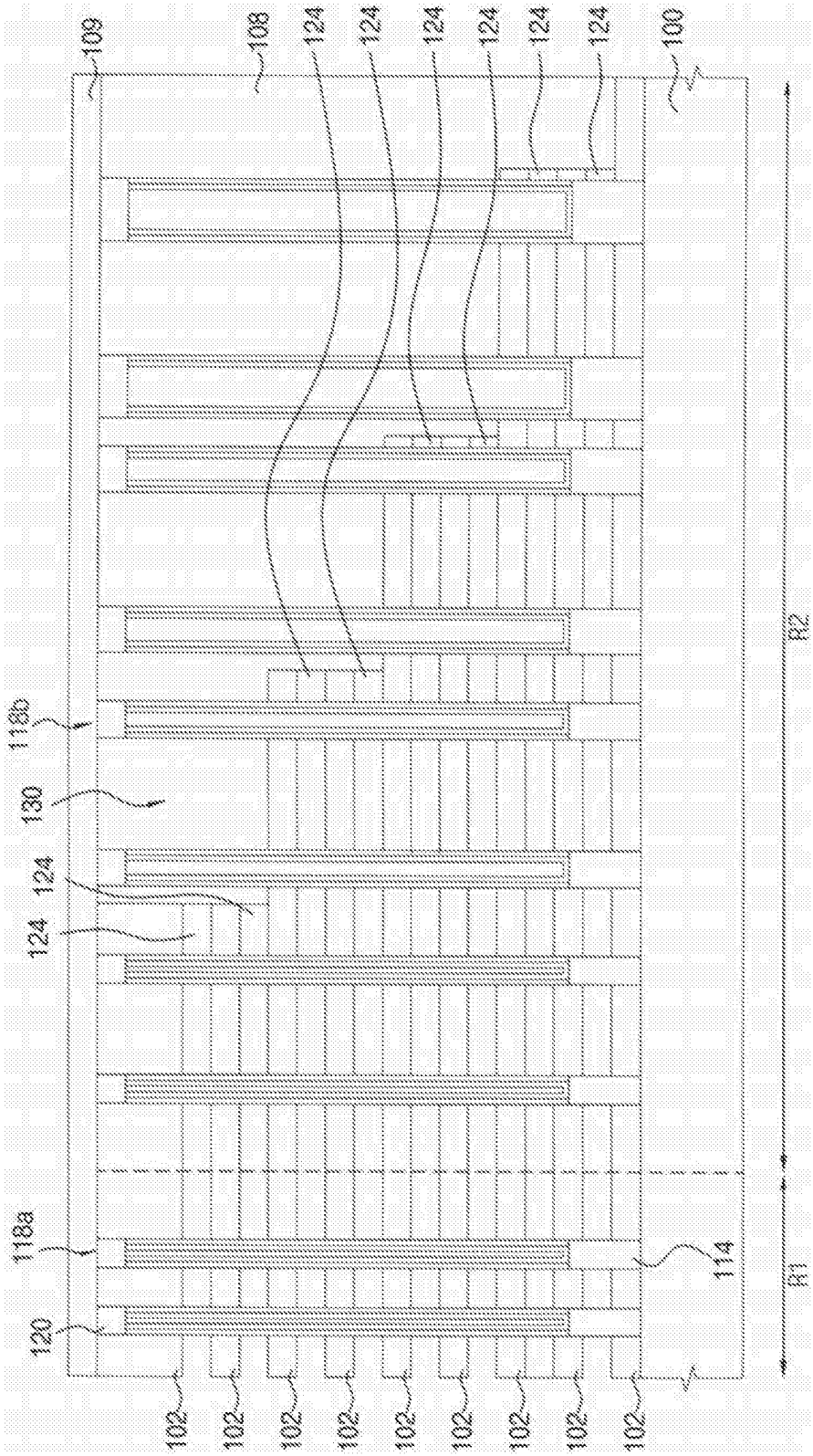


图12

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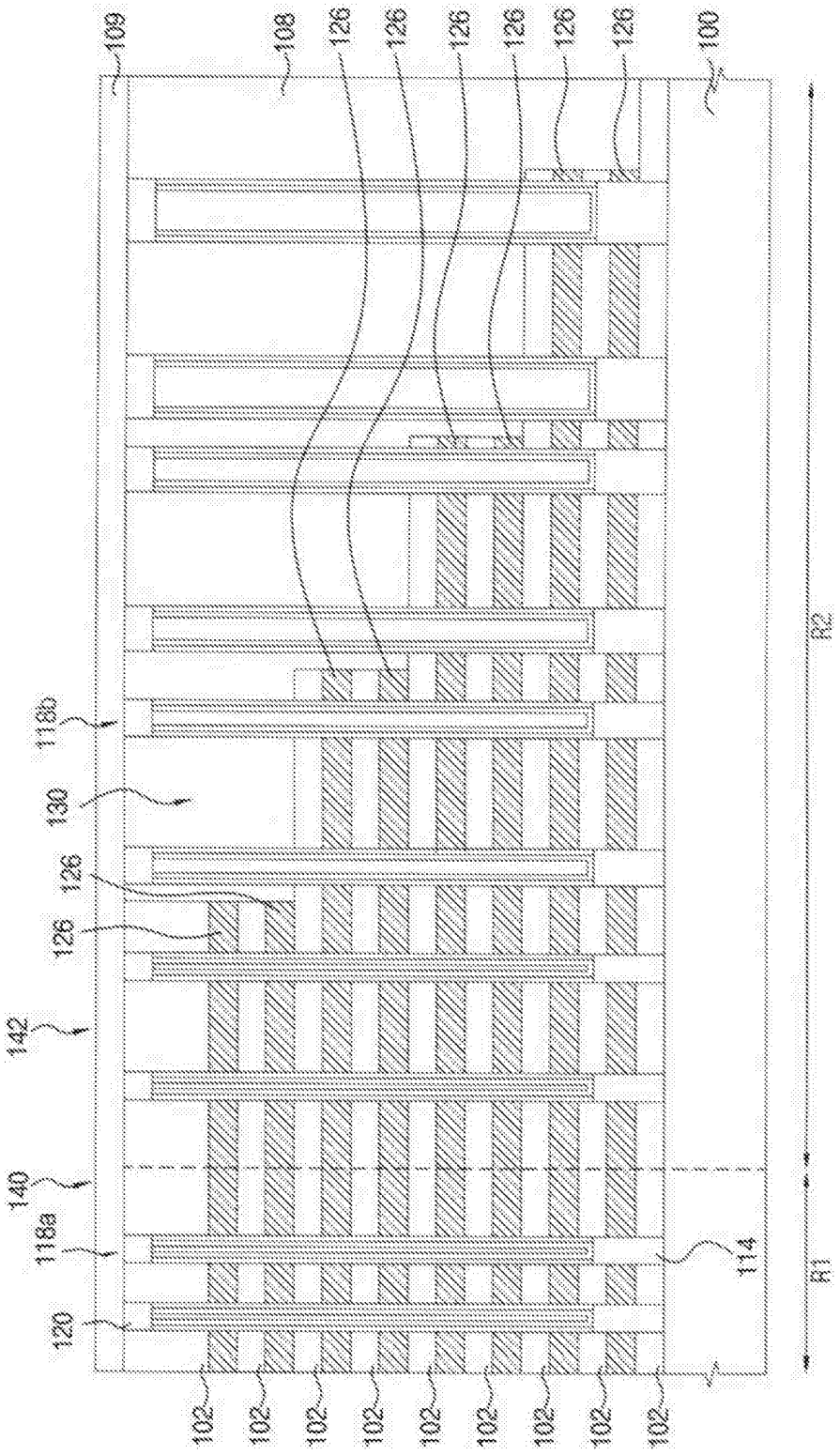


图13

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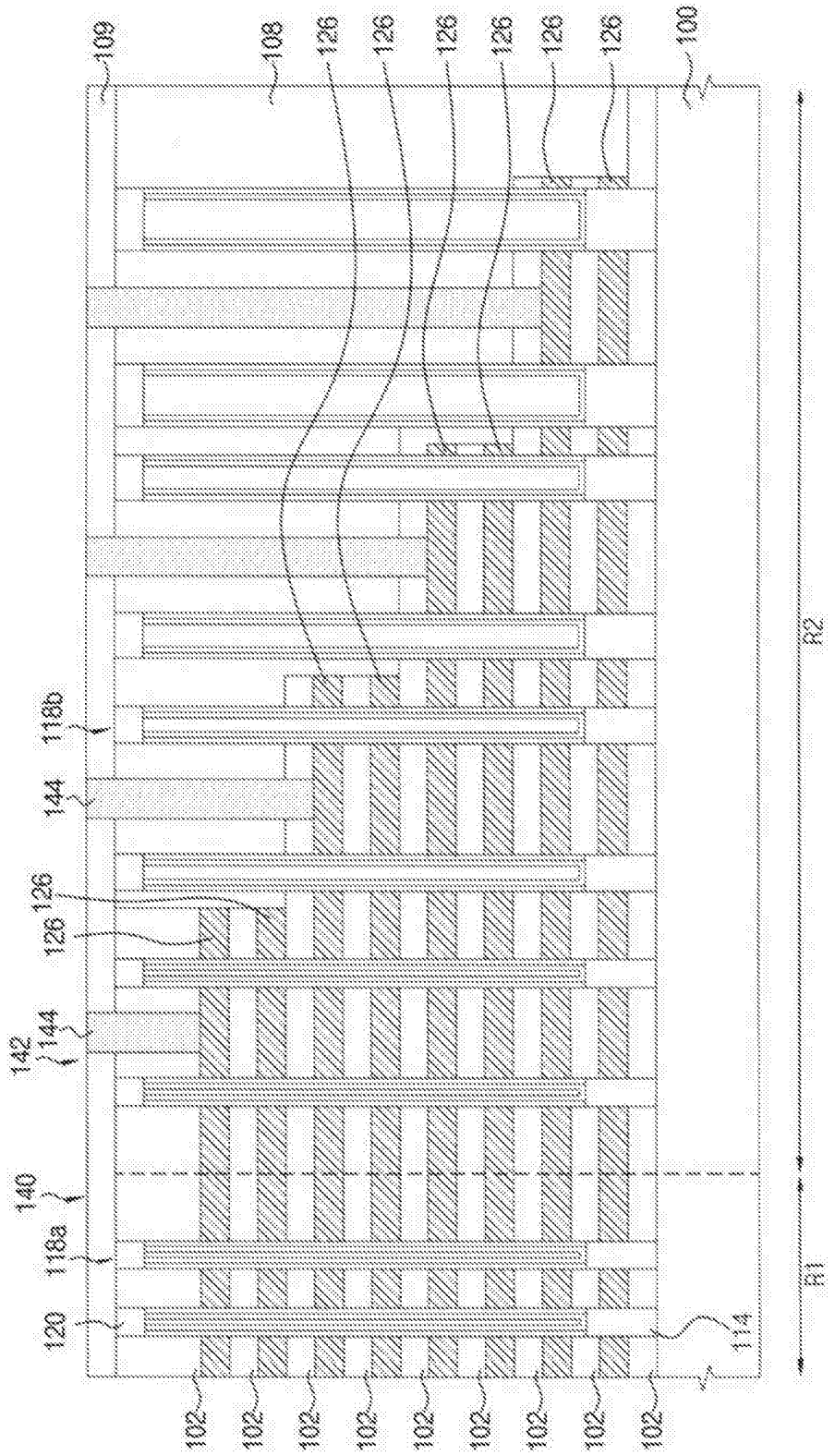


图14

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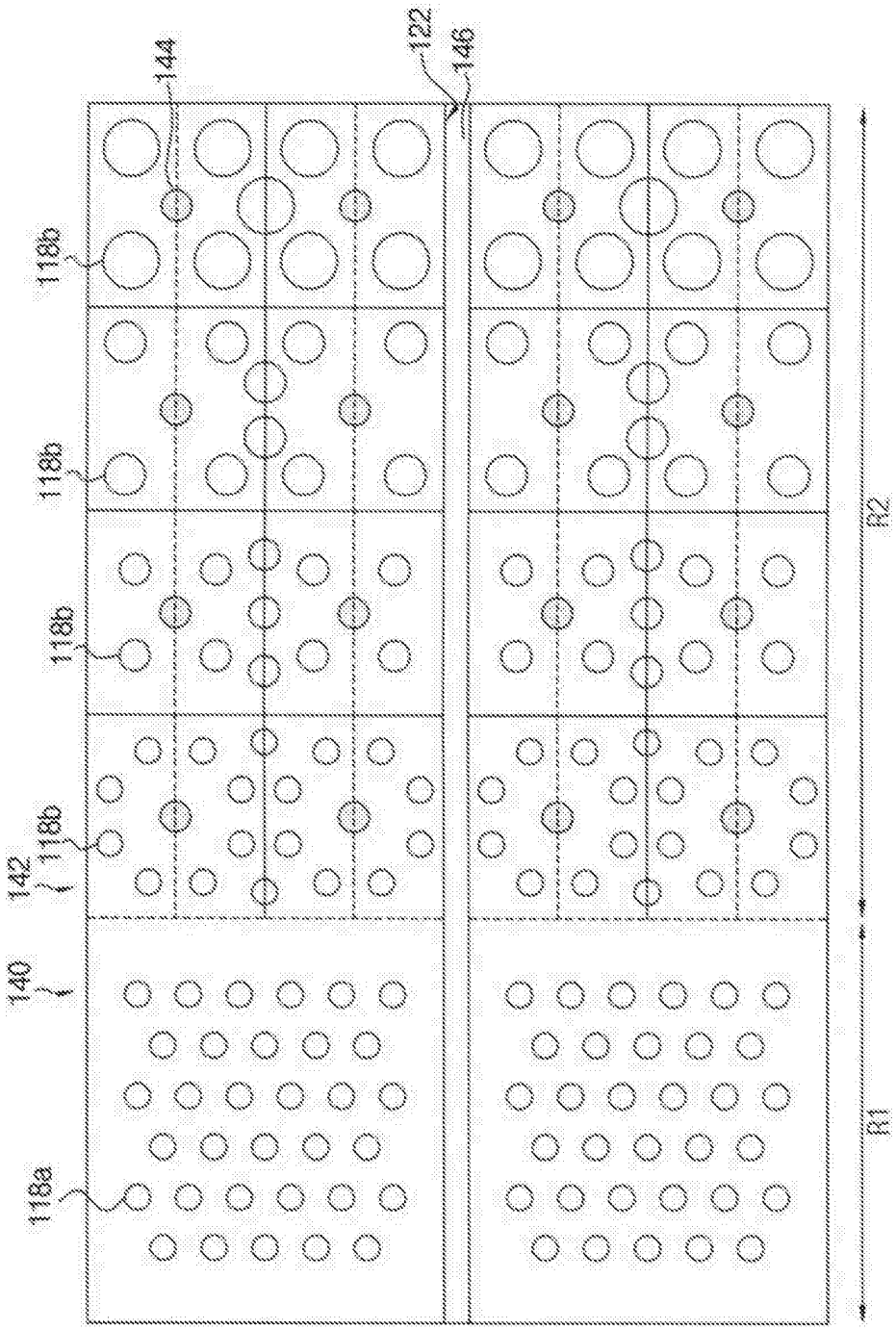


图15

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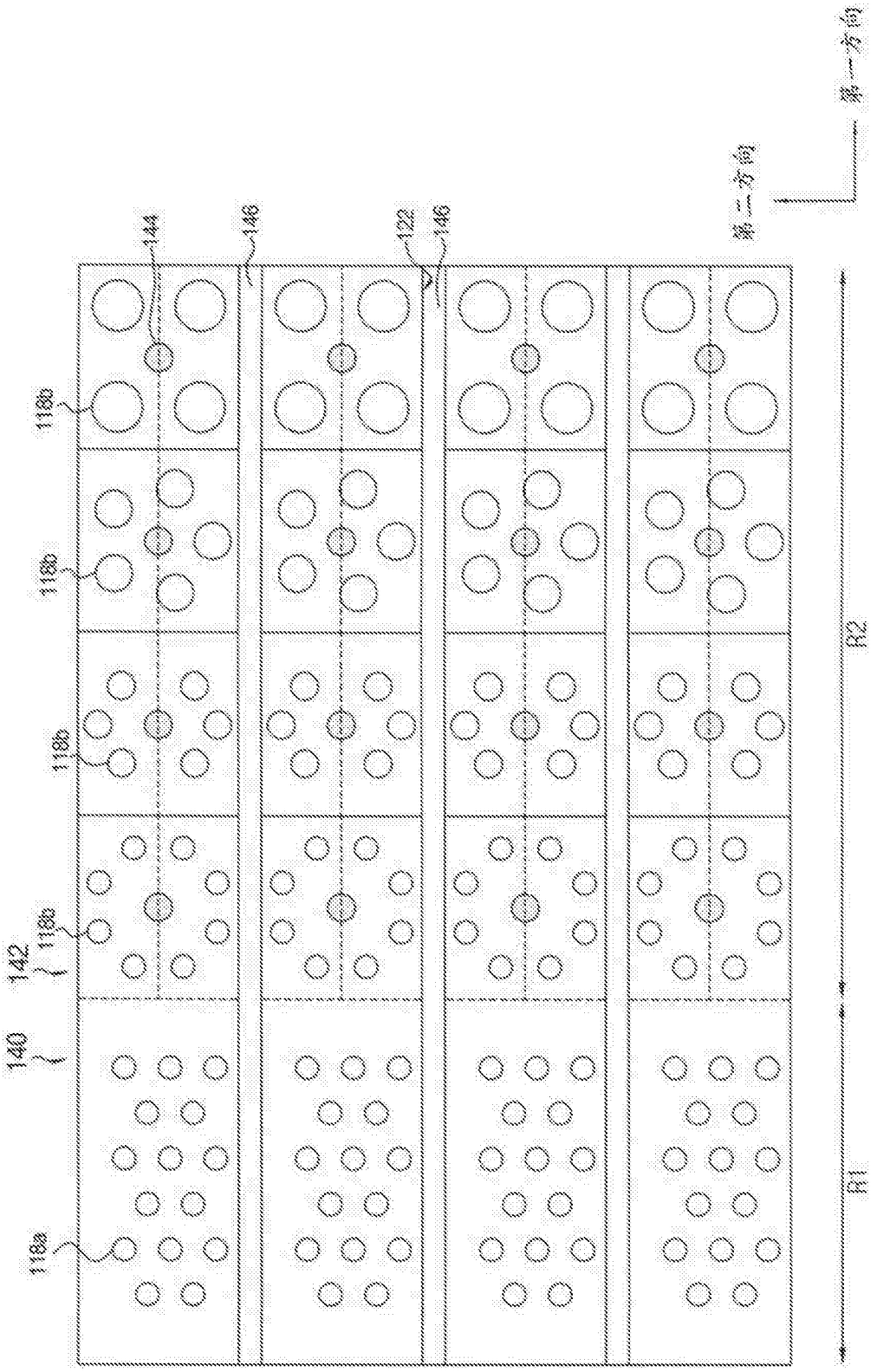


图16

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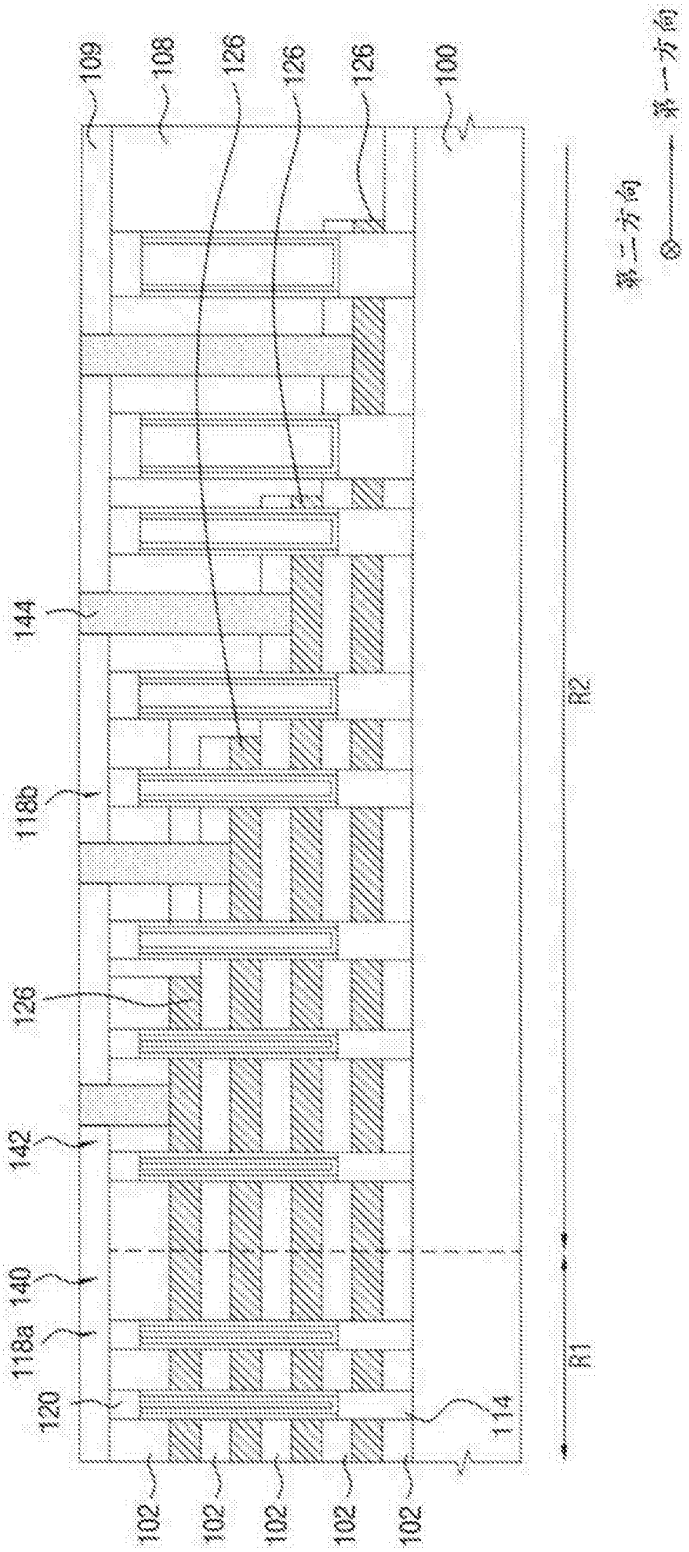


图17

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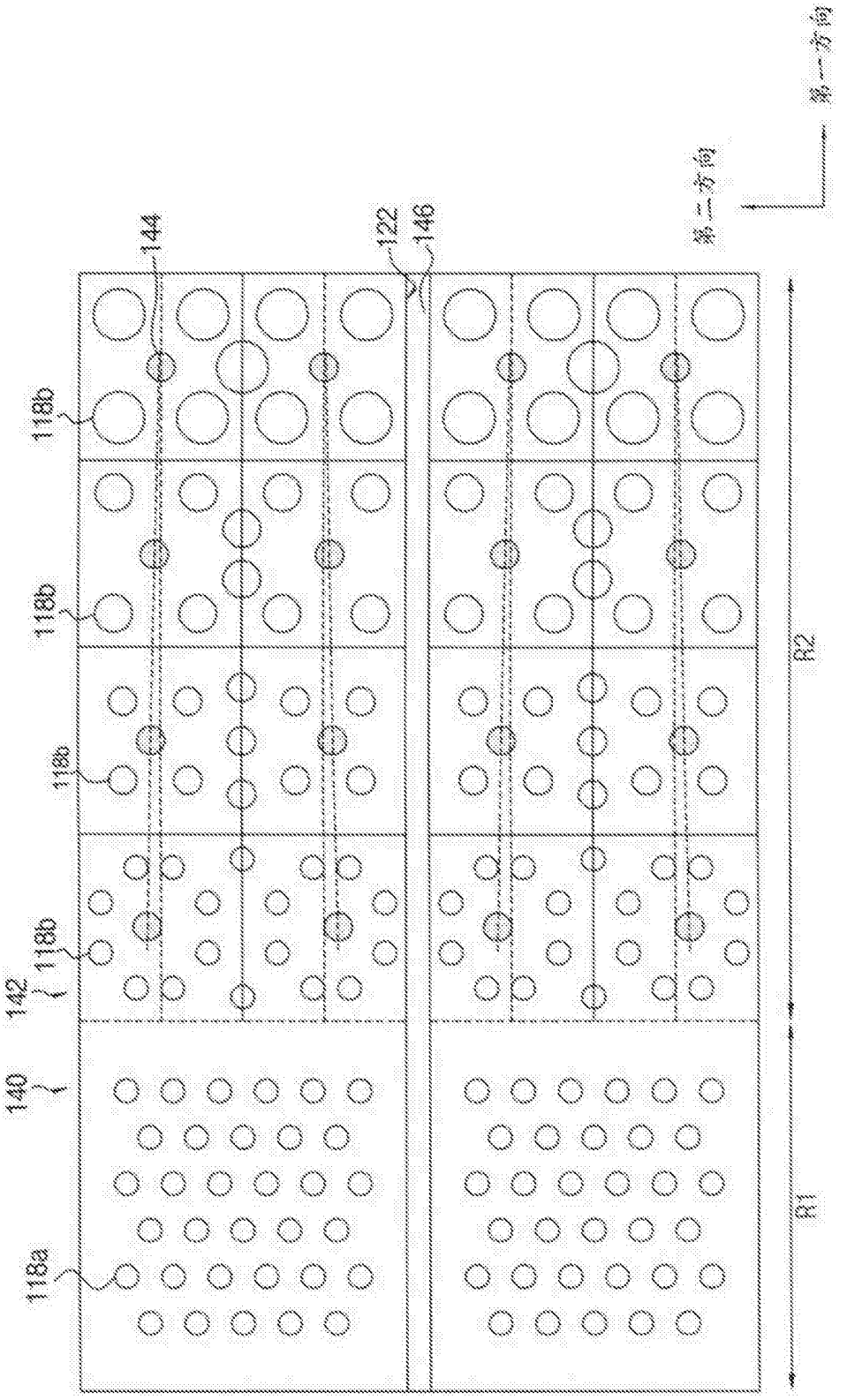


图18

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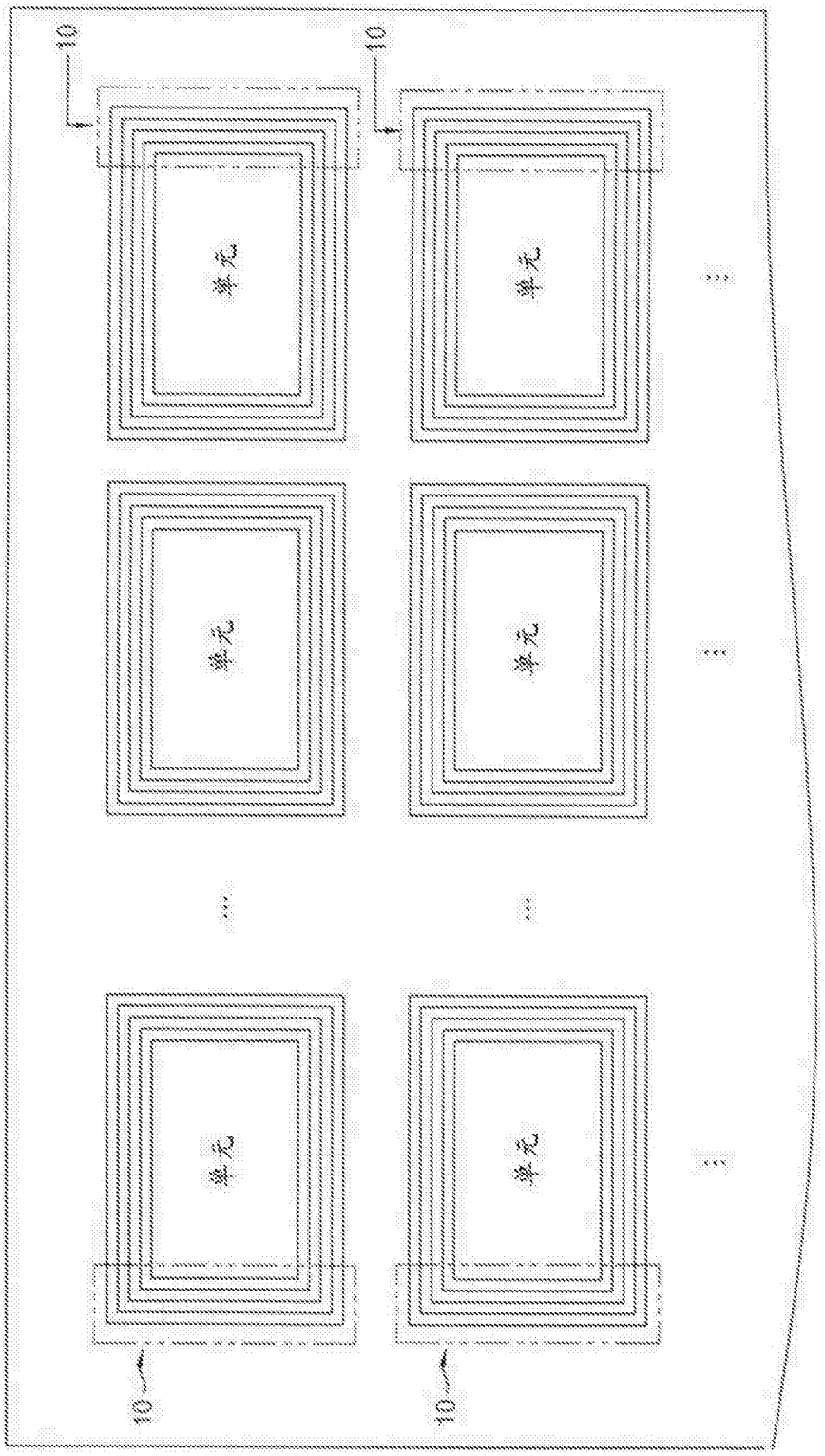


图19

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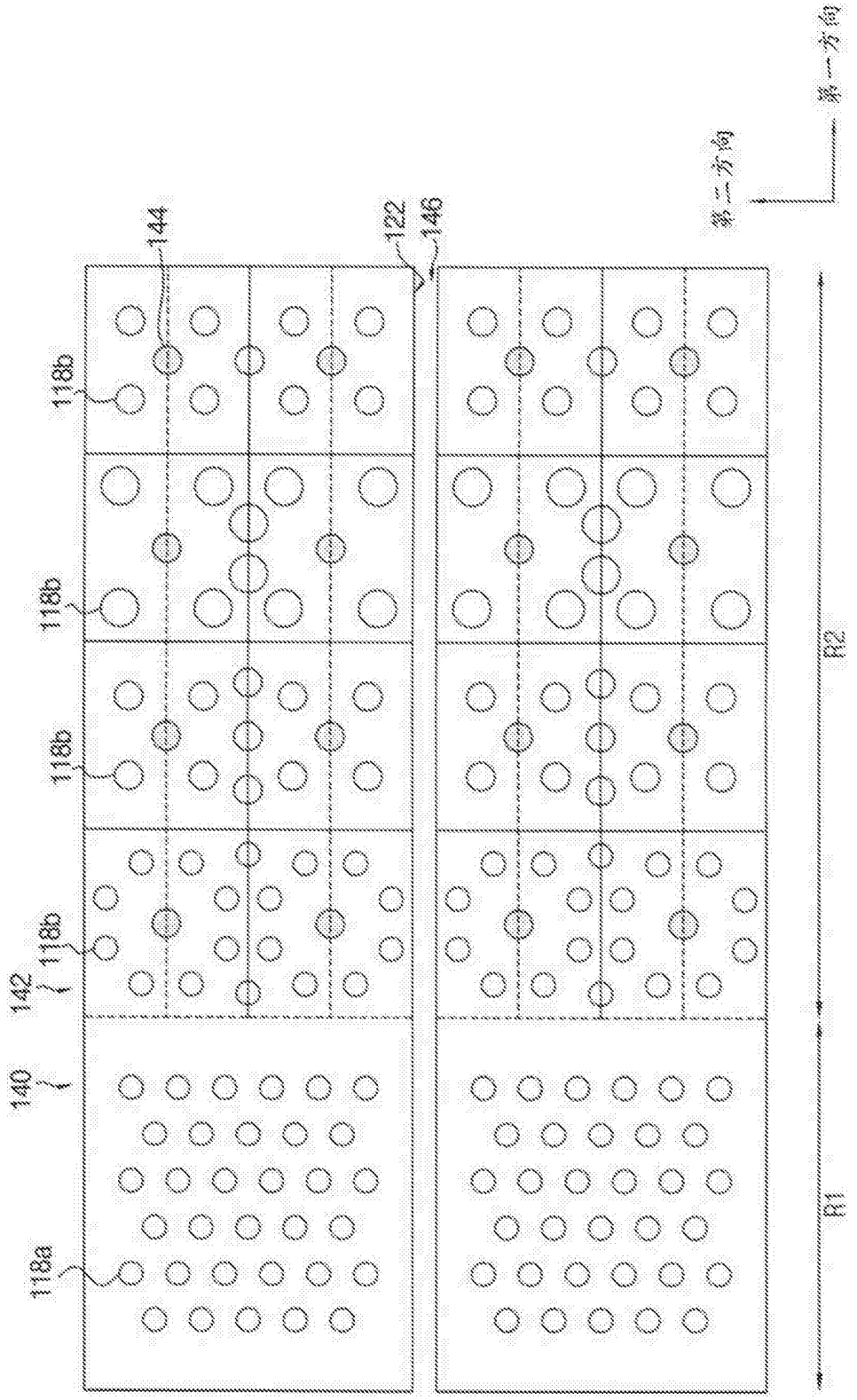


图20

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Espacenet

Bibliographic data: CN106057813 (A) — 2016-10-26

Three-dimensional semiconductor devices

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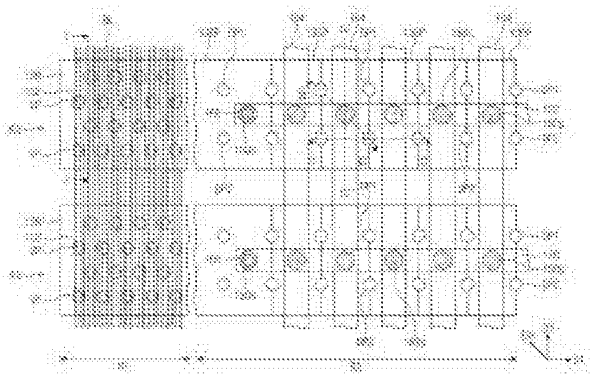
Classification: **- international:** ***H01L27/115***
- cooperative: H01L27/11551 (CN); H01L27/11565 (EP, US); H01L27/1157 (EP, US); H01L27/11575 (EP, US); H01L27/11578 (CN); H01L27/11582 (EP, US)

Application number: CN201610203765 20160401 Global Dossier

Priority number(s): KR20150046040 20150401

Also published as: KR20160118421 (A) US10083977 (B2) US2016293622 (A1) US2017352674 (A1) US2019019804 (A1) more

Abstract of CN106057813 (A)



The invention discloses a three-dimensional semiconductor device, which includes an electrode structure on a substrate that includes a first region and a second region, the electrode structure including a ground selection electrode, cell electrodes, and a string selection electrode which are sequentially stacked on the substrate wherein the ground selection electrode, the cell electrodes, and the string selection electrode respectively include a ground selection pad, cell pads, and a string selection pad which define a stepped structure in the second region of the substrate, a plurality of dummy pillars penetrating each of the cell pads and a portion of the electrode structure under each of the cell pads, and a cell contact plug electrically connected to each of the cell pads, wherein each of the dummy pillars penetrates a boundary between adjacent cell pads, and wherein the adjacent cell pads share the dummy pillars.

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(19)中华人民共和国国家知识产权局

(12)发明专利申请

(10)申请公布号 CN 106057813 A
(43)申请公布日 2016.10.26

(21)申请号 201610203765.4

(22)申请日 2016.04.01

(30)优先权数据
10-2015-0046040 2015.04.01 KR

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(51)Int.Cl.
H01L 27/115(2006.01)

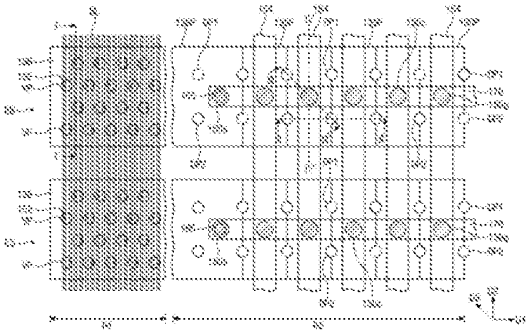
权利要求书3页 说明书15页 附图19页

(54)发明名称

三维半导体器件

(57)摘要

本发明公开了一种三维半导体器件，该三维半导体器件包括：在基板上的电极结构，该基板包括第一区和第二区，该电极结构包括顺序地层叠在基板上的接地选择电极、单元电极和串选择电极，其中接地选择电极、单元电极和串选择电极分别包括接地选择焊盘、单元焊盘和串选择焊盘，该接地选择焊盘、该单元焊盘和该串选择焊盘在基板的第二区中限定阶梯结构；穿透每个单元焊盘和在每个单元焊盘下面的电极结构的一部分的多个虚设柱；和电连接到每个单元焊盘的单元接触插塞，其中每个虚设柱穿透在相邻的单元焊盘之间的边界，以及其中相邻的单元焊盘共用虚设柱。



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1.一种三维半导体器件,包括:

在基板上的电极结构,该基板包括第一区和第二区,该电极结构包括:

接地选择电极,

单元电极,和

串选择电极,

其中所述接地选择电极、所述单元电极和所述串选择电极分别包括接地选择焊盘、单元焊盘和串选择焊盘,该接地选择焊盘、该单元焊盘和该串选择焊盘在所述基板的所述第二区中限定阶梯结构;

穿透每个单元焊盘和在每个单元焊盘下面的所述电极结构的一部分的多个虚设柱;和

电连接到每个单元焊盘的单元接触插塞,

其中每个虚设柱穿透在相邻的单元焊盘之间的边界,以及

其中所述相邻的单元焊盘共用所述虚设柱。

2.如权利要求1所述的三维半导体器件,其中:

所述电极结构在平行于所述基板的顶表面的第一方向上延伸,以及

所述虚设柱包括:

布置在所述第一方向上的一对第一虚设柱,以及

布置在所述第一方向上并且在交叉所述第一方向的第二方向上与所述一对第一虚设柱间隔开的一对第二虚设柱。

3.如权利要求2所述的三维半导体器件,其中:

所述一对第一虚设柱中的一个穿透在每个单元焊盘和与每个单元焊盘相邻的上部焊盘之间的第一边界,所述一对第一虚设柱中的另一个穿透在每个单元焊盘和与每个单元焊盘相邻的下部焊盘之间的第二边界。

所述一对第二虚设柱中的一个穿透所述第一边界,所述一对第二虚设柱中的另一个穿透所述第二边界。

4.如权利要求2所述的三维半导体器件,其中当从平面图看时,所述虚设柱围绕所述单元接触插塞。

5.如权利要求4所述的三维半导体器件,其中:

所述第一虚设柱中的一个在第三方向上与所述第二虚设柱中的一个对准,该第三方向交叉所述第一方向和所述第二方向,以及

所述第一虚设柱中的所述一个、所述单元接触插塞和所述第二虚设柱中的所述一个在所述第三方向上彼此对准。

6.如权利要求4所述的三维半导体器件,其中:

当从平面图看时,所述虚设柱分别在假想多边形的顶点处,以及

当从平面图看时,所述单元接触插塞在所述假想多边形的中心点处。

7.如权利要求6所述的三维半导体器件,其中所述假想多边形是四边形。

8.如权利要求2所述的三维半导体器件,其中所述单元接触插塞在所述第一虚设柱之间以在所述第一方向上与所述第一虚设柱对准。

9.如权利要求8所述的三维半导体器件,其中所述单元接触插塞在所述第一方向上与另一个单元接触插塞对准,该另一个单元接触插塞电连接到与每个单元焊盘直接相邻的另

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一个单元焊盘。

10.如权利要求8所述的三维半导体器件，其中连接到所述单元焊盘的所述单元接触插塞沿着所述第一方向布置成Z字形。

11.如权利要求1所述的三维半导体器件，其中：

穿透每个单元焊盘的虚设柱的数目是四个，以及

每个单元焊盘和与每个单元焊盘的两侧相邻的焊盘共用该四个虚设柱。

12.如权利要求1所述的三维半导体器件，还包括穿透所述第一区中的所述电极结构的多个竖直图案，所述虚设柱包括与所述竖直图案相同的材料。

13.如权利要求12所述的三维半导体器件，其中所述虚设柱的顶表面处于与所述竖直图案的顶表面相同的水平，所述虚设柱的底表面处于与所述竖直图案的底表面相同的水平。

14.如权利要求2所述的三维半导体器件，其中每个竖直图案包括：

在垂直于所述基板的顶表面的方向上延伸的竖直半导体图案；和

设置在所述竖直半导体图案和每个单元电极之间的隧道绝缘层、电荷存储层和阻挡绝缘层。

15.一种三维半导体器件，包括：

在基板上的电极结构，该基板包括第一区和第二区，该电极结构包括：

接地选择电极，

单元电极，和

串选择电极，并且所述接地选择电极、所述单元电极和所述串选择电极分别包括接地选择焊盘、单元焊盘和串选择焊盘，该接地选择焊盘、该单元焊盘和该串选择焊盘在所述第二区中构成阶梯结构；

穿透在所述第一区中的所述电极结构的多个竖直图案；

穿透每个单元焊盘和在每个单元焊盘下面的所述电极结构的一部分的多个虚设柱；和

电连接到每个单元焊盘的单元接触插塞，

其中所述竖直图案包括第一竖直图案和围绕所述第一竖直图案的第二竖直图案，

其中在平面图中，所述第一竖直图案在第一假想多边形的中心点处，并且在平面图中，所述第二竖直图案分别在所述第一假想多边形的顶点处，

其中在平面图中，所述虚设柱分别设置在第二假想多边形的顶点处，以及

其中所述第一假想多边形的所述顶点的数目不同于所述第二假想多边形的所述顶点的数目。

16.一种三维半导体器件，包括：

在基板上的电极结构，该基板包括第一区和第二区，该电极结构包括多个单元电极；

在所述基板的所述第二区中的多个单元焊盘，所述单元焊盘与对应的单元电极一起限定阶梯结构；

穿透所述单元焊盘和在所述单元焊盘下面的所述电极结构的多个虚设柱，该虚设柱仅在相邻的单元焊盘之间的边界处；和

电连接到每个单元焊盘的单元接触插塞。

17.如权利要求16所述的三维半导体器件，其中所述虚设柱在围绕所述单元接触插塞

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的假想多边形的顶点处。

18.如权利要求17所述的三维半导体器件，其中所述单元接触插塞在所述假想多边形的中心处，所述多边形是四边形。

19.如权利要求17所述的三维半导体器件，还包括在所述电极结构、所述虚设柱和所述单元接触插塞外部的公共源极区，当从平面图看时，所述单元接触插塞设置在所述电极结构的中心部分。

20.如权利要求16所述的三维半导体器件，其中所述基板的所述第一区是包括穿透所述电极结构的多个竖直图案的存储区，所述虚设柱具有与所述竖直图案相同的高度并包括与所述竖直图案相同的材料。

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三维半导体器件

技术领域

[0001] 实施方式涉及半导体器件,更具体地,涉及三维(3D)半导体器件。

背景技术

[0002] 半导体器件已经被高集成以提供用户所要求的高性能和低成本。半导体器件的集成度会直接影响半导体器件的成本,所以需要高集成的半导体器件。常规二维(2D)或平面存储器件的集成度可以主要由单位存储单元占据的面积确定,因此,常规2D存储器件的集成度会大大地受形成精细图案的技术影响。然而,因为需要极昂贵的装置来形成精细图案,所以2D存储器件的集成度持续增加,但是仍然受到限制。

[0003] 包括三维布置的存储单元的半导体器件(例如,三维(3D)存储器件)已经被发展从而克服上述限制。然而,3D存储器件的可靠性会由于其结构特性而劣化。

发明内容

[0004] 实施方式可以提供具有优良的可靠性的三维(3D)半导体器件。

[0005] 实施方式还可以提供能够最小化或防止电极结构的劣化的3D半导体器件。

[0006] 在一个方面,三维(3D)半导体器件可以包括设置在包括第一区和第二区的基板上的电极结构。电极结构可包括顺序地层叠在基板上的接地选择电极、单元电极和串选择电极。接地选择电极、单元电极和串选择电极可以分别包括接地选择焊盘、单元焊盘和串选择焊盘,该接地选择焊盘、单元焊盘和串选择焊盘在第二区中构成阶梯结构。3D半导体器件可以还包括穿透每个单元焊盘和设置在每个单元焊盘下面的电极结构的多个虚设柱以及电连接到每个单元焊盘的单元接触插塞。每个虚设柱可以穿透在每个单元焊盘和与每个单元焊盘相邻的焊盘之间的边界。每个单元焊盘和与每个单元焊盘的两侧相邻的焊盘可以共用虚设柱。

[0007] 在实施方式中,电极结构可以在平行于基板的顶表面的第一方向上延伸。虚设柱可以包括在第一方向上布置的一对第一虚设柱以及在第一方向上布置并且在交叉第一方向的第二方向上与该对第一虚设柱间隔开的一对第二虚设柱。

[0008] 在实施方式中,该对第一虚设柱中的一个可以穿透在每个单元焊盘和与每个单元焊盘相邻的上部焊盘之间的第一边界,该对第一虚设柱中的另一个可以穿透在每个单元焊盘和与每个单元焊盘相邻的下部焊盘之间的第二边界。该对第二虚设柱中的一个可以穿透第一边界,该对第二虚设柱中的另一个可以穿透第二边界。

[0009] 在实施方式中,虚设柱可以设置为当从平面图看时围绕单元接触插塞。

[0010] 在实施方式中,第一虚设柱中的一个可以在交叉第一和第二方向的第三方向上与第二虚设柱中的一个对准。第一虚设柱中的所述一个、单元接触插塞和第二虚设柱中的所述一个可以在第三方向上彼此对准。

[0011] 在实施方式中,当从平面图看时,虚设柱可以分别设置在假想多边形的顶点处。当从平面图看时,单元接触插塞可以设置在假想多边形的中心点处。

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[0012] 在实施方式中，假想多边形可以是四边形。

[0013] 在实施方式中，单元接触插塞可以设置在第一虚设柱之间从而在第一方向上与第一虚设柱对准。

[0014] 在实施方式中，单元接触插塞可以在第一方向上与另一个单元接触插塞对准，该另一个单元接触插塞电连接到与每个单元焊盘直接相邻的另一个单元焊盘。

[0015] 在实施方式中，连接到单元焊盘的单元接触插塞可以沿着第一方向布置成Z字形。

[0016] 在实施方式中，穿透每个单元焊盘的虚设柱的数目可以是四个。每个单元焊盘和与每个单元焊盘的两侧相邻的焊盘可以共用该四个虚设柱。

[0017] 在实施方式中，3D半导体器件可以还包括穿透第一区中的电极结构的多个竖直图案。虚设柱可以包括与竖直图案相同的材料。

[0018] 在实施方式中，虚设柱的顶表面可以设置在与竖直图案的顶表面基本相同的水平，虚设柱的底表面可以设置在与竖直图案的底表面基本相同的水平。

[0019] 在实施方式中，每个竖直图案可以包括在垂直于基板的顶表面的方向上延伸的竖直半导体图案、以及设置在竖直半导体图案与每个单元电极之间的隧道绝缘层、电荷存储层及阻挡绝缘层。

[0020] 在另一方面，三维(3D)半导体器件可以包括设置在包括第一区和第二区的基板上的电极结构。电极结构可包括顺序地层叠在基板上的接地选择电极、单元电极和串选择电极。接地选择电极、单元电极和串选择电极可以分别包括接地选择焊盘、单元焊盘和串选择焊盘，该接地选择焊盘、单元焊盘和串选择焊盘在第二区中构成阶梯结构。3D半导体器件可以还包括穿透第一区中的电极结构的多个竖直图案、穿透每个单元焊盘和设置在每个单元焊盘下面的电极结构的多个虚设柱、以及电连接到每个单元焊盘的单元接触插塞。竖直图案可以包括第一竖直图案和围绕第一竖直图案的第二竖直图案，第一竖直图案可以在平面图中设置在第一假想多边形的中心点处，第二竖直图案可以在平面图中分别设置在第一假想多边形的顶点处。虚设柱可以在平面图中分别设置在第二假想多边形的顶点处。第一假想多边形的顶点的数目可以不同于第二假想多边形的顶点的数量。

[0021] 在实施方式中，单元接触插塞可以设置在第二假想多边形的中心点处。

[0022] 在实施方式中，第一假想多边形可以是六边形，第二假想多边形可以是四边形。

[0023] 在实施方式中，每个虚设柱可以穿透在每个单元焊盘和与每个单元焊盘相邻的焊盘之间的边界。

[0024] 在实施方式中，穿透每个单元焊盘的虚设柱的数目可以是四个。每个单元焊盘和与每个单元焊盘的两侧相邻的焊盘可以共用该四个虚设柱。

[0025] 在实施方式中，虚设柱可以包括与竖直图案相同的材料。虚设柱的顶表面可以设置在与竖直图案的顶表面基本相同的水平，虚设柱的底表面可以设置在与竖直图案的底表面基本相同的水平。

[0026] 在另一方面，三维(3D)半导体器件包括：在包括第一区和第二区的基板上的电极结构，该电极结构包括多个单元电极；在基板的第二区中的多个单元焊盘，该单元焊盘与对应的单元电极一起限定阶梯结构；穿过单元焊盘和在单元焊盘下面的电极结构的多个虚设柱，该虚设柱仅在相邻单元焊盘之间的边界处；以及电连接到每个单元焊盘的单元接触插塞。

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[0027] 在实施方式中，虚设柱可以在围绕单元接触插塞的假想多边形的顶点处。

[0028] 在实施方式中，单元接触插塞可以在假想多边形的中心处，该多边形是四边形。

[0029] 在实施方式中，半导体器件可以还包括在电极结构、虚设柱和单元接触插塞外部的公共源极区，当在平面图中看时，单元接触插塞设置在电极结构的中心部分。

[0030] 在实施方式中，基板的第一区可以是穿过电极结构的多个竖直图案的存储区，虚设柱具有与竖直图案相同的高度并包括与竖直图案相同的材料。

附图说明

[0031] 通过参考附图详细描述示范实施方式，对本领域技术人员而言，特征将变得明显，在图中：

[0032] 图1示出根据实施方式的三维(3D)半导体器件的平面图。

[0033] 图2示出图1的一个电极结构的平面图，用于说明根据实施方式的虚设柱。

[0034] 图3示出沿图1的线I-I'、II-II'、III-III'和IV-IV'截取的截面图。

[0035] 图4A示出图3的部分'A'和'B'的放大图，用于说明根据实施方式的竖直图案和虚设柱。

[0036] 图4B示出图3的部分'A'和'B'的放大图，用于说明根据实施方式的竖直图案和虚设柱。

[0037] 图4C示出图3的部分'A'和'B'的放大图，用于说明根据实施方式的竖直图案和虚设柱。

[0038] 图4D示出图3的部分'A'和'B'的放大图，用于说明根据实施方式的竖直图案和虚设柱。

[0039] 图5示出图1的一个电极结构的平面图，用于说明根据实施方式的虚设柱。

[0040] 图6示出图1的一个电极结构的平面图，用于说明根据实施方式的虚设柱。

[0041] 图7至13示出沿图1的线I-I'、II-II'、III-III'和IV-IV'截取的截面图，用于示出根据实施方式的制造3D半导体器件的方法的多个阶段。

[0042] 图14示出平面图，其示出根据实施方式的3D半导体器件。

[0043] 图15示出沿图14的线I-I'、II-II'、III-III'和IV-IV'截取的截面图。

[0044] 图16至19示出沿图14的线I-I'、II-II'、III-III'和IV-IV'截取的截面图，示出根据实施方式的制造3D半导体器件的方法。

具体实施方式

[0045] 现将在下文参考附图更充分地描述示例实施方式；然而，它们可以以不同的形式实现且不应被理解为限于在此阐述的实施方式。而是，提供这些实施方式使得本公开将彻底和完整，并将向本领域技术人员充分传达示范性实施例。

[0046] 在这里使用时，术语"和/或"包括相关列举项目中的一个或多个的任意和所有组合。另外，在附图中，为了图示清楚，可以夸大层和区域的尺寸。将理解，当例如层、区域或基板的元件被称为"在"另一元件"上"时，它可以直接在另一元件上或者也可以存在居间元件。相反，术语"直接地"意指没有居间元件，例如，相同的解释可以应用于术语"在……之间"。通篇说明书中，相同的参考数字或相同的参考指示符指代相同的元件。

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[0047] 此外，在此参考是理想化示范性图示的截面图和/或平面图描述示范实施方式。因此，可以预期由于例如制造技术和/或公差引起的图示的形状的变化。因此，示范实施方式不应被解释为限于这里所示的区域的形状，而是将包括由于例如制造引起的形状的偏离。例如，被示为矩形的蚀刻区域典型地将具有修圆或弯曲的特征。因此，附图中示出的区域本质上是示意的，并且它们的形状不旨在限制。还将理解，虽然术语第一、第二、第三等可以在此用来描述不同的元件，但是这些元件不应该受到这些术语限制。这些术语仅用于区别一个元件与另一元件。因此，在一些实施方式中的第一元件可以在其他实施方式中被称为第二元件。在此解释和示出的示范实施方式包括它们的相似物。

[0048] 在此使用的术语仅用于描述具体实施方式而不旨在限制。在这里使用时，单数形式“一”和“该”也旨在包括复数形式，除非上下文清楚地指示另外的意思。将进一步理解，当在此使用时，术语“包含”、“包含……的”、“包括”和/或“包括……的”说明所述特征、整体、步骤、操作、元件和/或组分的存在，但是不排除一个或更多其他特征、整体、步骤、操作、元件、组分和/或其组的存在或添加。

[0049] 在下文，将参考附图描述实施方式。

[0050] 图1是示出根据实施方式的三维(3D)半导体器件的平面图。图2是示出图1的一个电极结构的平面图，用于说明根据实施方式的虚设柱。在图2中，图1的互连被省略以清楚地示出虚设柱的布置。图3是沿图1的线I-I’、II-II’、III-III’和IV-IV’截取的截面图。

[0051] 参考图1、2和3，基板100可以包括第一区R1和第二区R2。基板100可以是半导体基板(例如，硅基板、锗基板或硅锗基板)。第一区R1可以是在其中存储单元三维地布置的单元区，第二区R2可以是在其中提供焊盘(pad)的连接区。用于施加电压到存储单元的接触插塞可以设置在焊盘的顶表面上。

[0052] 电极结构ES可以设置在基板100上。电极结构ES可以从第一区R1延伸到第二区R2中。电极结构ES可以在第一方向D1上延伸，并可以在交叉第一方向D1的第二方向D2上彼此间隔开。

[0053] 每个电极结构ES可以包括顺序地层叠在第一区R1的基板100上的电极130、135和138，以及设置在电极130、135和138之间的绝缘层110。电极130、135和138和绝缘层110可以交替地层叠在基板100上。电极130、135和138可以通过绝缘层110彼此电绝缘。电极130、135和138可以分别包括焊盘130P、135P和138P，其在第二区R2中构成阶梯结构。焊盘130P、135P和138P可以分别从第一区R1的电极130、135和138在第一方向D1上延伸，从而在第二区R2中构成阶梯结构(参考图3的II-II’、III-III’)。绝缘层110也可以从第一区R1延伸到第二区R2中从而分别覆盖焊盘130P、135P和138P。

[0054] 每个电极结构ES的电极130、135和138可以包括接地选择电极130、串选择电极138和设置在接地选择电极130与串选择电极138之间的单元电极135。单元电极135可以在接地选择电极130与串选择电极138之间在垂直于基板100的顶表面的方向上层叠。焊盘130P、135P和138P可以分别包括从接地选择电极130延伸的接地选择焊盘130P、从串选择电极138延伸的串选择焊盘138P、和从单元电极135延伸的单元焊盘135P。

[0055] 每个电极结构ES可以还包括至少覆盖在第二区R2中的单元焊盘135P和接地选择焊盘130P的盖绝缘层115。盖绝缘层115可以包括绝缘材料(例如，硅氧化物)。另外，每个电极结构ES可以还包括被提供在接地选择电极130和接地选择焊盘130P下面的缓冲绝缘层

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105。缓冲绝缘层105可以包括绝缘材料(例如,硅氧化物)。

[0056] 多个竖直图案VP可以设置在第一区R1的基板100上并且可以穿透每个电极结构ES。竖直图案VP可以穿透每个电极结构ES从而与基板100接触。每个竖直图案VP可以包括半导体层。竖直图案VP将在后面参考图4A至4D更详细地描述。

[0057] 如图1和2所示,当从平面图看时,竖直图案VP可以二维地布置在基板100上。在实施方式中,竖直图案VP可以构成平行于第一方向D1的多个行。构成所述多个行中的相邻两行的竖直图案VP可以沿着第一方向D1布置成Z字形,例如,每行竖直图案VP可以沿着第一方向D1相对于相邻行偏移以使得竖直图案VP沿着第二方向D2布置成Z字形图案。

[0058] 多个虚设柱DP1和DP2可以设置在第二区R2的基板100上,并且可以穿透每个电极结构ES。虚设柱DP1和DP2可以穿透每个电极结构ES从而与基板100接触。如图3所示,虚设柱DP1和DP2的顶表面可以设置在与竖直图案VP的顶表面基本相同的水平(或高度),虚设柱DP1和DP2的底表面可以设置在与竖直图案VP的底表面基本相同的水平(或高度)。每个虚设柱DP1和DP2可以包括与竖直图案VP相同的材料。虚设柱DP1和DP2将在后面参考图4A至4D更详细地描述。

[0059] 虚设柱DP1和DP2可以穿透每个焊盘130P、135P和138P以及在每个焊盘130P、135P和138P下面的电极结构ES。另外,虚设柱DP1和DP2也可以穿透覆盖至少单元焊盘135P和接地选择焊盘130P的盖层115。虚设柱DP1和DP2可以包括在第一方向D1上布置的第一虚设柱DP1以及在第一方向D1上布置并且在第二方向D2上与第一虚设柱DP1间隔开的第二虚设柱DP2。在实施方式中,第二虚设柱DP2可以在第二方向D2上分别与第一虚设柱DP1对准。

[0060] 穿透每个单元焊盘135P的虚设柱DP1和DP2可以包括沿着第一方向D1彼此直接相邻的一对第一虚设柱DP1和沿着第一方向D1彼此直接相邻的一对第二虚设柱DP2。该对第一虚设柱DP1中的第一个可以穿透在每个单元焊盘135P和沿着第一方向D1的相邻焊盘(上部焊盘135P或138P)之间的第一边界,例如,在图1中的每个单元焊盘135P的左侧的边界,该对第一虚设柱DP1中的第二个可以穿透每个单元焊盘135P和沿着第一方向D1的相邻焊盘(下部焊盘135P或130P)之间的第二边界,例如,在图1中的每个单元焊盘135P的右侧的边界。该对第二虚设柱DP2中的第一个可以穿透第一边界,例如,左边界,该对第二虚设柱DP2中的第二个可以穿透第二边界,例如,右边界。该对第二虚设柱DP2中的第一个可以沿着第二方向D2在第一边界上与该对第一虚设柱DP1中的第一个对准,该对第二虚设柱DP2中的第二个可以沿着第二方向D2在第二边界上与该对第一虚设柱DP1中的第二个对准。在实施方式中,穿透每个单元焊盘135P的虚设柱DP1和DP2的数目可以是四个,每个单元焊盘135P和设置在其两侧的焊盘可以共用所述四个虚设柱DP1和DP2。

[0061] 在实施方式中,穿透串选择焊盘138P的虚设柱DP1和DP2可以也包括例如沿着第一方向D1彼此直接相邻的一对第一虚设柱DP1和例如沿着第一方向D1彼此直接相邻的一对第二虚设柱DP2。穿透串选择焊盘138P的该对第一虚设柱DP1中的第一个可以穿透在串选择焊盘138P和沿着第一方向D1与其相邻的单元焊盘135P之间的边界,该对第一虚设柱DP1中的第二个可以与该边界间隔开。穿透串选择焊盘138P的该对第二虚设柱DP2中的第一个可以穿透该边界,该对第二虚设柱DP2中的第二个可以与该边界间隔开。串选择焊盘138P可以设置在电极结构ES的最上层处,所以串选择焊盘138P可具有一个边界。穿透串选择焊盘138P的该对第二虚设柱DP2中的第一个可以例如沿着第二方向D2在该边界上与穿透串选择焊盘

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138P的该对第一虚设柱DP1中的第一个对准，该对第二虚设柱DP2中的第二个可以在第二方向D2上与该对第一虚设柱DP1中的第二个对准。在实施方式中，穿透串选择焊盘138P的虚设柱DP1和DP2的数目可以是四个，串选择焊盘138P和与其相邻的单元焊盘135P可以共用该四个虚设柱DP1和DP2中沿着它们的边界的两个虚设柱。

[0062] 穿透接地选择焊盘130P的虚设柱DP1和DP2也可以包括彼此直接相邻的一对第一虚设柱DP1和彼此直接相邻的一对第二虚设柱DP2。穿透接地选择焊盘130P的该对第一虚设柱DP1中的第一个可以穿透在接地选择焊盘130P和与其相邻的单元焊盘135P之间的边界，该对第一虚设柱DP1中的第二个可以与该边界间隔开。穿透接地选择焊盘130P的该对第二虚设柱DP2中的第一个可以穿透该边界，该对第二虚设柱DP2中的第二个可以与该边界间隔开。穿透接地选择焊盘130P的该对第二虚设柱DP2中的第一个可以在该边界上与穿透接地选择焊盘130P的该对第一虚设柱DP1中的第一个对准，该对第二虚设柱DP2中的第二个可以在第二方向D2上与该对第一虚设柱DP1中的第二个对准。在实施方式中，穿透接地选择焊盘130P的虚设柱DP1和DP2的数目可以是四个，接地选择焊盘130P和与其相邻的单元焊盘135P可以共用这四个虚设柱DP1和DP2中的两个。

[0063] 公共源极区CS可以例如在沿着在图3中的线IV-IV'的横截面中设置在基板100中在每个电极结构ES的两侧。基板100可以掺杂有第一导电类型的掺杂剂，公共源极区CS可以掺杂有不同于第一导电类型的第二导电类型的掺杂剂。公共源极线CSL可以设置在每个电极结构ES的两侧从而连接到公共源极区CS。公共源极线CSL可以包括导电材料(例如，金属材料，诸如钨)。绝缘间隔物140可以分别设置在每个电极结构ES与公共源极线CSL之间。绝缘间隔物140可以包括例如硅氧化物。第一绝缘层145可以设置在电极结构ES的顶表面上。第一绝缘层145可以覆盖电极结构ES的顶表面，并且可以延伸到绝缘间隔物140的顶表面和公共源极线CSL的顶表面上。第一绝缘层145可以包括例如硅氧化物层、硅氮化物层或硅氮氧化物层中的至少之一。

[0064] 单元接触插塞150c可以设置在第二区R2的基板100上从而分别连接到每个电极结构ES的单元焊盘135P。单元接触插塞150c可以穿透在第二区R2中的第一绝缘层145、盖绝缘层115和绝缘层110。串选择接触插塞150s可以设置在第二区R2中的基板100上从而连接到每个电极结构ES的串选择焊盘138P。接地选择接触插塞150g可以设置在第二区R2的基板100上从而连接到每个电极结构ES的接地选择焊盘130P。串选择接触插塞150s可以穿透设置在串选择焊盘138P上的第一绝缘层145和绝缘层110，接地选择接触插塞150g可以穿透设置在接地选择焊盘130P上的第一绝缘层145、盖绝缘层115和绝缘层110。根据实施方式，串选择接触插塞150s、单元接触插塞150c和接地选择接触插塞150g可以沿着第一方向D1布置，例如，对准。

[0065] 根据实施方式，穿透每个单元焊盘135P的虚设柱DP1和DP2可以布置为当从平面图看时，围绕连接到每个单元焊盘135P的单元接触插塞150c，如图2所示。即，当从平面图看时，穿透每个单元焊盘135P的虚设柱DP1和DP2可以分别设置在第一假想多边形10的顶点处。穿透每个单元焊盘135P的虚设柱DP1和DP2的中心点可以分别与第一假想多边形10的顶点交叠。第一假想多边形10可以是四边形。换句话说，四个虚设柱DP1和DP2可以围绕单元接触插塞150c，例如，四个虚设柱DP1和DP2可以定义围绕单元接触插塞150c的多边形的四个顶点。当从平面图看时，单元接触插塞150c可以设置在第一假想多边形10的中心点处。在此

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情况下，穿透每个单元焊盘135P的该对第一虚设柱DP1中的第一个可以在交叉第一方向D1和第二方向D2的第三方向D3上与穿透每个单元焊盘135P的该对第二虚设柱DP2中的第二个对准。在此情况下，该对第一虚设柱DP1中的第一个、单元接触插塞150c、和该对第二虚设柱DP2中的第二个可以在第三方向D3上彼此对准。

[0066] 穿透串选择焊盘138P的虚设柱DP1和DP2可以布置为当从平面图看时围绕连接到串选择焊盘138P的串选择接触插塞150s。穿透串选择焊盘138P的虚设柱DP1和DP2可以分别设置在当从平面图看时限定在串选择焊盘138P上的第一假想多边形10的顶点处，串选择接触插塞150s可以设置在第一假想多边形10的中心点处。同样地，穿透接地选择焊盘130P的虚设柱DP1和DP2可以布置为当从平面图看时围绕连接到接地选择焊盘130P的接地选择接触插塞150g。穿透接地选择焊盘130P的虚设柱DP1和DP2可以分别设置在当从平面图看时限定在接地选择焊盘138P上的第一假想多边形10的顶点处，接地选择接触插塞150g可以设置在第一假想多边形10的中心点处。

[0067] 竖直图案VP可以包括构成所述多个行中的最外面的行的外部竖直图案VP，以及构成所述多个行中的内部行的内部竖直图案VP。如图2所示，在平面图中，围绕每个内部竖直图案VP的相邻竖直图案VP可以分别设置在第二假想多边形20的顶点处，并且在平面图中，每个内部竖直图案VP可以设置在第二假想多边形20的中心点处。第二假想多边形20的顶点的数目可以不同于第一假想多边形10的顶点的数目。在实施方式中，第二假想多边形20可以是六边形。

[0068] 位线BL可以设置在第一区R1的第一绝缘层145上。位线BL可以在第二方向D2上延伸并且可以在第一方向D1上彼此间隔开。穿透每个电极结构ES的竖直图案VP可以分别电连接到位线BL。每个竖直图案VP可以经由穿透第一绝缘层145的位线接触插塞152而电连接到位线BL中的对应的一条位线。单元电极135可以对应于字线，接地选择电极130可以对应于接地选择线，串选择电极138可以对应于串选择线。

[0069] 第一互连154可以设置在第二区R2的第一绝缘层145上。第一互连154可以在第二方向D2上延伸，并且可以在第一方向D1上彼此间隔开。第一互连154可以分别电连接到电极结构ES的单元接触插塞150c和接地选择接触插塞150g。在实施方式中，第一互连154可以设置在与位线BL基本相同的水平(或高度)。然而，实施方式不限于此。

[0070] 第二绝缘层160可以设置在第一绝缘层145、位线BL和第一互连154上。第二绝缘层160可以包括例如硅氧化物层、硅氮化物层和硅氮氧化物层中的至少之一。

[0071] 第二互连170可以设置在第二绝缘层160上。在实施方式中，第二互连170可以在第一方向D1上延伸并且可以在第二方向D2上彼此间隔开。然而，实施方式不限于此。每个第二互连170可以电连接到每个电极结构ES的串选择接触插塞150s。串选择接触插塞150s可以经由穿透第二绝缘层160的互连插塞165而电连接到第二互连170中的对应一个。

[0072] 根据本实施方式，虚设柱DP1和DP2可以穿透在第二区R2中构成阶梯结构的焊盘130P、135P和138P从而与基板100接触。穿透每个单元焊盘135P的虚设柱DP1和DP2可以例如仅穿透在每个单元焊盘135P和与每个单元焊盘135P的两侧相邻的焊盘之间的第一边界和第二边界。换句话说，每个单元焊盘135P与与其两侧相邻的焊盘共用穿透每个单元焊盘135P的虚设柱DP1和DP2，由此最小化第二区R2中的虚设柱的数目。因为电极结构ES使用最少的虚设柱DP1和DP2来支撑，所以电极结构ES的形状变化可以最小化。另外，该最少的虚设

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柱DP1和DP2可以支撑在形成电极结构ES的置换工艺期间使用的模制层叠结构，因而，焊盘130P、135P和138P的形状变化可以利用该最少的虚设柱DP1和DP2而最小化。结果，可以最小化或防止电极结构ES的劣化。

[0073] 此外，穿透每个单元焊盘135P的虚设柱DP1和DP2可以设置为当从平面图看时围绕连接到每个单元焊盘135P的单元接触插塞150c。因此，单元接触插塞150c和与其相邻的公共源极线CSL之间的距离可以增加，从而使单元接触插塞150c容易地与公共源极线CSL绝缘。

[0074] 结果，可以提供具有优良的可靠性的3D半导体器件。

[0075] 图4A示出图3的部分'A'和'B'的放大图，用于说明根据实施方式的竖直图案和虚设柱。

[0076] 参考图4A，竖直图案VP可包括从基板100向上延伸的竖直半导体图案SP。竖直图案VP可还包括设置在单元电极135和竖直半导体图案SP之间的阻挡绝缘层BIL、电荷存储层CL和隧道绝缘层TL。阻挡绝缘层BIL可以邻近于单元电极135，隧道绝缘层TL可以邻近于竖直半导体图案SP。电荷存储层CL可以设置在阻挡绝缘层BIL和隧道绝缘层TL之间。例如，隧道绝缘层TL可包括硅氧化物层和硅氮氧化物层中的至少之一。电荷存储层CL可包括包含陷阱位置(trap sites)的硅氮化物层和包含传导纳米点的绝缘层中的至少之一。阻挡绝缘层BIL可包括其介电常数高于隧道绝缘层TL的介电常数的高k介电层。另外，阻挡绝缘层BIL可还包括其能带隙大于该高k介电层的能带隙的阻挡绝缘层(例如，硅氧化物层)。

[0077] 在本实施方式中，阻挡绝缘层BIL、电荷存储层CL和隧道绝缘层TL可在基本上垂直于基板100的顶表面的方向上延伸从而设置在竖直半导体图案SP和绝缘层110之间。竖直半导体图案SP可具有通心粉(macaroni)或管形状，竖直图案VP可还包括填充竖直半导体图案SP的内部空间的竖直绝缘图案VI。例如，竖直绝缘图案VI可包括硅氧化物。

[0078] 第二虚设柱DP2可以包括与竖直图案VP相同的材料。根据本实施方式，类似于竖直图案VP，虚设柱DP2可包括阻挡绝缘层BIL、电荷存储层CL、隧道绝缘层TL、竖直半导体图案SP和竖直绝缘图案VI。第一虚设柱DP1可具有与第二虚设柱DP2相同的结构。

[0079] 图4B示出图3的部分'A'和'B'的放大图，用于说明根据实施方式的竖直图案和虚设柱。

[0080] 参考图4B，竖直图案VP可包括从基板100向上延伸的竖直半导体图案SP。竖直图案VP可还包括设置在单元电极135和竖直半导体图案SP之间的电荷存储层CL和隧道绝缘层TL。根据本实施方式，阻挡绝缘层BIL可以设置在单元电极135和竖直图案VP之间，并且可在平行于基板100的顶表面的方向上延伸从而设置在单元电极135和绝缘层110之间。电荷存储层CL可以设置在阻挡绝缘层BIL和隧道绝缘层TL之间。竖直半导体图案SP可具有通心粉或管形状，竖直图案VP可还包括填充竖直半导体图案SP的内部空间的竖直绝缘图案VI。

[0081] 第二虚设柱DP2可以包括与竖直图案VP相同的材料。根据本实施方式，类似于竖直图案VP，虚设柱DP2可包括电荷存储层CL、隧道绝缘层TL、竖直半导体图案SP和竖直绝缘图案VI。第一虚设柱DP1可具有与第二虚设柱DP2相同的结构。

[0082] 图4C示出图3的部分'A'和'B'的放大图，用于说明根据实施方式的竖直图案和虚设柱。

[0083] 参考图4C，竖直图案VP可包括从基板100向上延伸的竖直半导体图案SP。竖直图案

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VP可还包括设置在单元电极135和竖直半导体图案SP之间的隧道绝缘层TL。根据本实施方式，阻挡绝缘层BIL和电荷存储层CL可以设置在单元电极135和竖直图案VP之间，并且可在平行于基板100的顶表面的方向上延伸从而设置在单元电极135和绝缘层110之间。电荷存储层CL可以设置在阻挡绝缘层BIL和隧道绝缘层TL之间。竖直半导体图案SP可具有通心粉或管形状，竖直图案VP可还包括填充竖直半导体图案SP的内部空间的竖直绝缘图案VI。

[0084] 第二虚设柱DP2可以包括与竖直图案VP相同的材料。根据本实施方式，类似于竖直图案VP，虚设柱DP2可包括隧道绝缘层TL、竖直半导体图案SP和竖直绝缘图案VI。第一虚设柱DP1可具有与第二虚设柱DP2相同的结构。

[0085] 图4D示出图3的部分'A'和'B'的放大图，用于说明根据实施方式的竖直图案和虚设柱。

[0086] 参考图4D，竖直图案VP可包括从基板100向上延伸的竖直半导体图案SP。根据本实施方式，阻挡绝缘层BIL、电荷存储层CL和隧道绝缘层TL可以设置在单元电极135和竖直图案VP之间，并且可在平行于基板100的顶表面的方向上延伸从而设置在单元电极135和绝缘层110之间。电荷存储层CL可以设置在阻挡绝缘层BIL和隧道绝缘层TL之间。竖直半导体图案SP可具有通心粉或管形状，竖直图案VP可还包括填充竖直半导体图案SP的内部空间的竖直绝缘图案VI。

[0087] 第二虚设柱DP2可以包括与竖直图案VP相同的材料。根据本实施方式，类似于竖直图案VP，虚设柱DP2可包括竖直半导体图案SP和竖直绝缘图案VI。第一虚设柱DP1可具有与第二虚设柱DP2相同的结构。

[0088] 图5是示出图1的一个电极结构的平面图，用于说明根据实施方式的虚设柱。在下文，为了说明上的容易和方便，将主要描述图1、2和3的实施方式与本实施方式之间的差别。

[0089] 参考图5，根据本实施方式，串选择接触插塞150s、单元接触插塞150c和接地选择接触插塞150g可以沿着第一方向D1布置成Z字形。

[0090] 详细地，当从平面图看时，穿透每个单元焊盘135P的虚设柱DP1和DP2可以分别设置在第一假想多边形10的顶点处。穿透每个单元焊盘135P的虚设柱DP1和DP2的中心点可以分别与第一假想多边形10的顶点交叠。第一假想多边形10可以是四边形。当从平面图看时，连接到每个单元焊盘135P的单元接触插塞150c可以设置在第一假想多边形10的一条边上。例如，如图5所示，连接到单元焊盘135P中的每个奇数编号的单元焊盘135P的单元接触插塞150c可以设置在穿透每个奇数编号的单元焊盘135P的一对第二虚设柱DP2之间(图5中的单元焊盘135P的底部)，并且可以在第一方向D1上与在相邻的奇数编号的单元焊盘135P中的一对第二虚设柱DP2对准。类似地，连接到单元焊盘135P中的每个偶数编号的单元焊盘135P的单元接触插塞150c可以设置在穿透每个偶数编号的单元焊盘135P的一对第一虚设柱DP1之间(图5中的单元焊盘135P的顶部)，并且可以在第一方向D1上与在相邻的偶数编号的单元焊盘135P中的一对第一虚设柱DP1对准。

[0091] 当从平面图看时，穿透串选择焊盘138P的虚设柱DP1和DP2可以分别设置在第一假想多边形10的顶点处，并且当从平面图看时，串选择接触插塞150s可以设置在第一假想多边形10的一条边上。串选择接触插塞150s可以设置在穿透串选择焊盘138P的该对第一虚设柱DP1之间并且例如与穿透串选择焊盘138P的该对第一虚设柱DP1对准，或者设置在穿透串选择焊盘138P的该对第二虚设柱DP2之间。串选择接触插塞150s可以在第一方向D1上与该

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对第一虚设柱DP1或者该对第二虚设柱DP2对准。同样地，当从平面图看时，穿透接地选择焊盘130P的虚设柱DP1和DP2可以分别设置在第一假想多边形10的顶点处，并且当从平面图看时，接地选择接触插塞150g可以设置在第一假想多边形10的一条边上。接地选择接触插塞150g可以设置在穿透接地选择焊盘130P的该对第一虚设柱DP1之间或者在穿透接地选择焊盘130P的该对第二虚设柱DP2之间。接地选择接触插塞150g可以在第一方向D1上与该对第一虚设柱DP1或者该对第二虚设柱DP2对准。

[0092] 图6是示出图1的一个电极结构的平面图，用于说明根据实施方式的虚设柱。在下文，为了说明上的容易和方便，将主要描述图1、2和3的实施方式与本实施方式之间的差别。

[0093] 参考图6，串选择接触插塞150s、单元接触插塞150c和接地选择接触插塞150g可以在第一方向D1上布置成一行。根据本实施方式，第一虚设柱DP1可以分别设置在串选择接触插塞150s和与串选择接触插塞150s相邻的单元接触插塞150c之间、在彼此相邻的单元接触插塞150c之间，以及在接地选择接触插塞150g和与接地选择接触插塞150g相邻的单元接触插塞150c之间。

[0094] 详细地，当从平面图看时，穿透每个单元焊盘135P的虚设柱DP1和DP2可以分别设置在第一假想多边形10的顶点处。穿透每个单元焊盘135P的虚设柱DP1和DP2的中心点可以分别与第一假想多边形10的顶点交叠。第一假想多边形10可以是四边形。当从平面图看时，连接到每个单元焊盘135P的单元接触插塞150c可以设置在第一假想多边形10的一条边上。单元接触插塞150c可以设置在穿透每个单元焊盘135P的该对第一虚设柱DP1之间，并且可以在第一方向D1上与该对第一虚设柱DP1对准。

[0095] 穿透串选择焊盘138P的虚设柱DP1和DP2在平面图中可以分别设置在第一假想多边形10的顶点处，串选择接触插塞150s在平面图中可以设置在第一假想多边形10的一条边上。串选择接触插塞150s可以设置在穿透串选择焊盘138P的该对第一虚设柱DP1之间，并且可以在第一方向D1上与该对第一虚设柱DP1对准。同样地，穿透接地选择焊盘130P的虚设柱DP1和DP2在平面图中可以分别设置在第一假想多边形10的顶点处，接地选择接触插塞150g在平面图中可以设置在第一假想多边形10的一条边上。接地选择接触插塞150g可以设置在穿透接地选择焊盘130P的该对第一虚设柱DP1之间，并且可以在第一方向D1上与该对第一虚设柱DP1对准。

[0096] 根据本实施方式，虚设柱DP1和DP2可以穿透构成第二区R2中的阶梯结构的焊盘130P、135P和138P从而与基板100接触。穿透每个单元焊盘135P的虚设柱DP1和DP2可以穿透在每个单元焊盘135P和与每个单元焊盘135P的两侧相邻的焊盘之间的边界。换句话说，每个单元焊盘135P和与其两侧相邻的焊盘可共用穿透每个单元焊盘135P的虚设柱DP1和DP2。因为电极结构ES使用最少数量的虚设柱DP1和DP2支撑，所以电极结构ES的形状变化可以最小化。另外，该最少数量的虚设柱DP1和DP2可以支撑在形成电极结构ES的置换工艺期间使用的模制层叠结构，由此焊盘130P、135P和138P的形状变化可以利用最少数量的虚设柱DP1和DP2而最小化。结果，可以实现具有优良可靠性的3D半导体器件。

[0097] 图7至13是沿图1的线I-I'、II-II'、III-III'和IV-IV'截取的截面图，用于示出在根据实施方式的制造3D半导体器件的方法中的多个阶段。

[0098] 参考图7，缓冲绝缘层105可以形成在包括第一区R1和第二区R2的基板100的整个顶表面上。牺牲层120和绝缘层110可以交替地形成在具有缓冲绝缘层105的基板100上。牺

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牲层120可以由相对于缓冲绝缘层105和绝缘层110具有蚀刻选择性的材料形成。例如，缓冲绝缘层105和绝缘层110可以由硅氧化物层形成，牺牲层120可以由硅氮化物层形成。

[0099] 参考图8，第二区R2中的绝缘层110和牺牲层120可以被图案化以形成阶梯结构。在实施方式中，掩模图案(未示出)可以形成在最高的绝缘层110上，最高的绝缘层110和最高的牺牲层120可以使用掩模图案作为蚀刻掩模被蚀刻以暴露第二区R2中的次高的绝缘层110。随后，掩模图案可以被蚀刻以减小掩模图案的宽度。次高的绝缘层110和次高的牺牲层120可以利用蚀刻掩模图案作为蚀刻掩模被蚀刻。绝缘层110和牺牲层120的蚀刻工艺以及掩模图案的蚀刻工艺可以被重复执行以在第二区R2中形成阶梯结构。

[0100] 此后，盖绝缘层115可以形成在基板100上并且然后可以被平坦化。根据实施方式，盖绝缘层115可以被平坦化直到第一区R1的最高的绝缘层110被暴露。根据实施方式，平坦化的盖绝缘层115可以保留在第一区R1的最高的绝缘层110上。

[0101] 参考图9，第一区R1的绝缘层110、牺牲层120和缓冲绝缘层105可以被连续地图案化以形成暴露基板100的竖直孔H1。另外，第二区R2的盖绝缘层115、绝缘层110、牺牲层120和缓冲绝缘层105可以被连续地图案化以形成暴露基板100的虚设孔H2。竖直孔H1和虚设孔H2可以同时形成。

[0102] 竖直孔H1可以如参考图2描述的竖直图案VP那样地布置。同样地，虚设孔H2可以如参考图2描述的虚设柱DP1和DP2那样地布置。换句话说，虚设孔H2可以分别设置在图2的第一假想多边形10的顶点处，竖直孔H1可以分别设置在图2的第二假想多边形20的顶点和中心处。

[0103] 竖直图案VP可以分别形成在竖直孔H1中，虚设柱DP1和DP2可以分别形成在虚设孔H2中。竖直图案VP和虚设柱DP1及DP2可以同时形成。竖直图案VP和虚设柱DP1及DP2可以如在图4A至4D的实施方式之一中所描述那样地形成。

[0104] 参考图10，盖绝缘层115、绝缘层110、牺牲层120和缓冲绝缘层105可以被连续地图案化以形成暴露基板100的沟槽T。沟槽T可从第一区R1延伸到第二区R2中，所以从第一区R1延伸到第二区R2中的模制层叠结构可以被限定在沟槽T之间。模制层叠结构可包括绝缘层110、牺牲层120、缓冲绝缘层105和盖绝缘层115。绝缘层110、牺牲层120、缓冲绝缘层105和盖绝缘层115可具有通过沟槽T暴露的侧壁。牺牲层120可具有构成第二区R2中的阶梯结构的牺牲焊盘。绝缘层110可分别覆盖牺牲层120的牺牲焊盘。盖绝缘层115可覆盖构成第二区R2中的阶梯结构的牺牲焊盘。竖直图案VP和虚设柱DP1及DP2可穿透模制层叠结构从而与基板100接触。

[0105] 可以对模制层叠结构执行置换工艺，从而形成图3的电极结构ES。在下文，将参考图11和12详细描述置换工艺。

[0106] 参考图11，通过沟槽T暴露的牺牲层120可以被去除以在绝缘层110之间形成空区域122。空区域122可在平行于基板100的顶表面的方向上从沟槽T延伸到绝缘层110之间。牺牲层120可以通过各向同性蚀刻工艺(例如，湿蚀刻工艺)被去除。

[0107] 当牺牲层120被去除时，虚设柱DP1和DP2支撑在第二区R2中的绝缘层110和盖层115，竖直图案VP可支撑在第一区R1中的绝缘层110。因此，可以最小化或防止可能由牺牲层120的去除所引起的问题。

[0108] 例如，如果不存在虚设柱DP1和DP2，在第二区R2中彼此竖直地相邻的绝缘层110会

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彼此靠近或彼此接触。因此，即将在后续工艺中形成在空区域122中的焊盘的形状会变化，例如，焊盘的至少一部分不能被形成。然而，根据实施方式，在第二区R2中穿过绝缘层110形成的虚设柱DP1和DP2在牺牲层120的去除期间支撑绝缘层110，由此最小化或防止上述问题，例如，绝缘层110的未对准和/或破裂。

[0109] 参考图1和12，第一导电层可以形成在基板100上以填充沟槽T和空区域122。第一导电层可包括共形地覆盖沟槽T和空区域122的内表面的阻挡层以及填充沟槽T和空区域122的剩余区域的电极层。此后，设置在沟槽T中的第一导电层可以被去除以在空区域122中形成电极130、135和138以及焊盘130P、135P和138P。因此，可以形成参考图1至3描述的电极结构ES。

[0110] 当竖直图案VP和虚设柱DP1及DP2如图4B所示地被形成时，阻挡绝缘层BIL可以在第一导电层的形成之前共形地形成在空区域122中。当竖直图案VP和虚设柱DP1及DP2如图4C所示地被形成时，电荷存储层CL和阻挡绝缘层BIL可以在第一导电层的形成之前顺序地形成在空区域122中。当竖直图案VP和虚设柱DP1及DP2如图4D所示地被形成时，隧道绝缘层TL、电荷存储层CL和阻挡绝缘层BIL可以在第一导电层的形成之前顺序地形成在空区域122中。

[0111] 掺杂剂离子可以注入到设置在沟槽T下面的基板100中以形成公共源极区CS。公共源极区CS可以在电极130、135和138的形成之后被形成。替换地，公共源极区可以在沟槽T的形成之后并且在牺牲层120的去除之前被形成。

[0112] 公共源极线CSL和绝缘间隔物140可以形成在沟槽T中。公共源极线CSL可以电连接公共源极区CS，绝缘间隔物140可以使公共源极线CSL与电极130、135和138电绝缘。形成绝缘间隔物140可包括形成共形地覆盖公共源极区CS的顶表面和沟槽T的内侧壁的绝缘间隔物层(未示出)，并且各向异性地蚀刻该绝缘间隔物层。公共源极区CS可以通过绝缘间隔物层的各向异性蚀刻工艺被暴露。随后，第二导电层可以被形成以填充沟槽T的剩余区域。第二导电层可以被平坦化以分别在沟槽T中限制地形成公共源极线CSL。

[0113] 参考图1和13，第一绝缘层145可以形成在基板100的整个顶表面上。第一绝缘层145可覆盖电极结构，并且可在平行于基板100的顶表面的方向上延伸以覆盖绝缘间隔物140的顶表面和公共源极线CSL的顶表面。

[0114] 接触插塞150s、150c和150g可以在第二区R2中形成为分别连接到焊盘130P、135P和138P。接触插塞150s、150c和150g可以穿透第一绝缘层145、盖绝缘层115和绝缘层110。位线接触插塞152可以形成为穿透在第一区R1中的第一绝缘层145。位线接触插塞152可以分别连接到竖直图案VP。接触插塞150s、150c和150g以及位线接触插塞152可以由导电材料形成并且可以同时形成。

[0115] 位线BL可以形成在第一区R1中的第一绝缘层145上，第一互连154可以形成在第二区R2中的第一绝缘层145上。位线BL可以连接到位线接触插塞152，第一互连154可以分别连接到接地选择接触插塞150g和单元接触插塞150c。位线BL和第一互连154可以由导电材料形成并且可以同时形成。

[0116] 再次参考图1和3，第二绝缘层160可以形成在第一绝缘层145、位线BL和第一互连154上。第二互连170可以形成在第二绝缘层160上。第二互连170可以分别电连接到串选择接触插塞150s。串选择接触插塞150s可以经由穿透第二绝缘层160的互连插塞165而电连接

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到第二互连170中的对应一个。

[0117] 图14是平面图，示出根据实施方式的3D半导体器件。图15是沿图14的线I-I'、II-II'、III-III'和IV-IV'截取的截面图。在下文，与在图1至3的实施方式中描述的相同元件将通过相同的附图标记或相同的参考指示符来表示，并且为了说明上的容易和方便，将主要描述本实施方式与图1至3的实施方式之间的差别。

[0118] 参考图14和15，在本实施方式中，电极结构ES可包括多个串选择电极138a和138b。切割绝缘图案200可以设置在串选择电极138a和138b之间。换句话说，第一串选择电极138a和第二串选择电极138b可以通过切割绝缘图案200彼此分开。切割绝缘图案200的底表面可以高于最高的单元电极135的顶表面。换句话说，所述多个串选择电极138a和138b可以设置在一个最高的单元电极135上。切割绝缘图案200可包括例如硅氧化物。

[0119] 切割绝缘图案200可从第一区R1延伸到第二区R2中，所以第一串选择电极138a的第一串选择焊盘138Pa可以通过切割绝缘图案200与第二串选择电极138b的第二串选择焊盘138Pb分开。

[0120] 竖直图案VP和DVP可穿透第一区R1的电极结构ES。竖直图案VP和DVP可以构成平行于第一方向D1的多个行。构成所述多个行中的相邻两行的竖直图案VP和DVP可以沿着第一方向D1布置成Z字形。竖直图案VP和DVP可包括与切割绝缘图案200交叠的虚设竖直图案DVP以及与切割绝缘图案200间隔开的单元竖直图案VP。虚设竖直图案DVP可以布置在第一方向D1上以构成所述多个行中的一行。单元竖直图案VP可构成所述多个行中的其余行。

[0121] 构成所述多个行中最外面的行的竖直图案VP可以被定义为外部竖直图案，构成所述多个行中的内部行的竖直图案VP和DVP可以被定义为内部竖直图案。每个内部竖直图案VP和DVP可以设置在参考图2描述的第二假想多边形20的中心点处，围绕每个内部竖直图案VP和DVP的相邻的竖直图案VP和DVP可以分别设置在第二假想多边形20的顶点处。第二假想多边形20可以是六边形。

[0122] 第一串选择接触插塞150sa和第二串选择接触插塞150sb可以分别连接到第一串选择焊盘138Pa和第二串选择焊盘138Pb。根据本实施方式，当从平面图看时，第一和第二串选择接触插塞150sa和150sb可以分别设置在参考图2描述的第一假想多边形10的多个顶点中的两个顶点处。当从平面图看时，穿透第一和第二串选择焊盘138Pa和138Pb的虚设柱DP1和DP2可以分别设置在第一假想多边形10的所述多个顶点中的其余顶点处。第一串选择接触插塞150sa可以在第一方向D1上与穿透第一串选择焊盘138Pa的第一虚设柱DP1对准。第二串选择接触插塞150sb可以在第一方向D1上与穿透第二串选择焊盘138Pb的第二虚设柱DP2对准。附加的虚设柱DP3可以进一步提供在第一假想多边形10的中心点处。然而，实施方式不限于此。在实施方式中，可以省略附加的虚设柱DP3。

[0123] 第一上互连170a和第二上互连170b可以分别电连接到第一串选择焊盘138Pa和第二串选择焊盘138Pb。第一串选择焊盘138Pa可以经由第一串选择接触插塞150sa和穿透第二区R2的第二绝缘层160的第一互连插塞165a电连接到第一上互连170a。第二串选择焊盘138Pb可以经由第二串选择接触插塞150sb和穿透第二区R2的第二绝缘层160的第二互连插塞165b电连接到第二上互连170b。

[0124] 在第一区R1中，每条位线BL可以电连接到在第二方向D2上布置的单元竖直图案VP。在此情况下，在第二方向D2上布置的单元竖直图案VP可分别穿透所述多个串选择电极

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138a和138b。

[0125] 图16至19是沿图14的线I-I'、II-II'、III-III'和IV-IV'截取的截面图，用于示出根据实施方式的制造3D半导体器件的方法。在下文，与在图7至13的实施方式中描述的相同元件将通过相同的附图标记或相同的参考指示符来表示，并且为了说明上的容易和方便，将主要描述本实施方式与图7至713的实施方式之间的差别。

[0126] 参考图14和16，缓冲绝缘层105可以形成在包括第一区R1和第二区R2的基板100的整个顶表面上。牺牲层120和绝缘层110可以交替地形成在具有缓冲绝缘层105的基板100上。第二区R2中的绝缘层110和牺牲层120可以被图案化以形成阶梯结构。盖绝缘层115可以形成为覆盖该阶梯结构。

[0127] 最高的绝缘层110和最高的牺牲层120可以被图案化以形成切割区域200H。切割区域200H可以从第一区R1延伸到第二区R2中。切割绝缘图案200可以形成为填充切割区域200H。在实施方式中，切割区域200H和切割绝缘图案200可以在牺牲层120和盖绝缘层115的阶梯结构形成之后形成。替换地，牺牲层120和盖绝缘层115的阶梯结构可以在切割区域200H和切割绝缘图案200的形成之后形成。

[0128] 参考图14和17，第一区R1的绝缘层110、牺牲层120和缓冲绝缘层105可以被连续地图案化以形成暴露基板100的竖直孔H1。另外，第二区R2的盖绝缘层115、绝缘层110、牺牲层120和缓冲绝缘层105可以被连续地图案化以形成暴露基板100的虚设孔H2。竖直孔H1和虚设孔H2可以同时形成。竖直孔H1可以如图14的竖直图案VP和DVP那样布置，虚设孔H2可以如图14的虚设柱DP1、DP2和DP3那样布置。

[0129] 竖直图案VP和DVP可以分别形成在竖直孔H1中，虚设柱DP1、DP2和DP3可以分别形成在虚设孔H2中。竖直图案VP和DVP以及虚设柱DP1、DP2和DP3可以同时形成。竖直图案VP和DVP以及虚设柱DP1、DP2和DP3可以如图4A至4D的实施方式之一所描述地那样被形成。

[0130] 盖绝缘层115、绝缘层110、牺牲层120和缓冲绝缘层105可以被连续地图案化以形成暴露基板100的沟槽T。沟槽T可从第一区R1延伸到第二区R2中，所以从第一区R1延伸到第二区R2中的模制层叠结构可以被限定在沟槽T之间。模制层叠结构可包括绝缘层110、牺牲层120、缓冲绝缘层105和盖绝缘层115。此时，模制层叠结构的最高的牺牲层120可包括通过切割绝缘图案200而彼此横向地分开的最高的牺牲图案。绝缘层110、牺牲层120、缓冲绝缘层105和盖绝缘层115可具有通过沟槽T暴露的侧壁。

[0131] 参考图18，通过沟槽T暴露的牺牲层120可以被去除以在绝缘层110之间形成空区域122。当牺牲层120被去除时，竖直图案VP和DVP以及虚设柱DP1、DP2和DP3可支撑绝缘层110。因为牺牲层120被去除，所以分别与牺牲图案对应的空区域122可以形成在模制层叠结构中。

[0132] 参考图14和19，第一导电层可以形成在基板100上以填充沟槽T和空区域122。此后，设置在沟槽T中的第一导电层可以被去除以在空区域122中形成电极130、135、138a和138b以及焊盘130P、135P、138Pa和138Pb。因此，可以形成参考图14和15描述的电极结构ES。

[0133] 第一串选择电极138a和第二串选择电极138b可以分别形成在最高的空区域122中。第一串选择电极138a和第二串选择电极138b可以通过切割绝缘图案200而彼此横向地间隔开。另外，第一串选择电极138a的第一串选择焊盘138Pa也可通过切割绝缘图案200与第二串选择电极138b的第二串选择焊盘138Pb横向地间隔开。

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[0134] 掺杂剂离子可以被注入到设置在沟槽T下面的基板100中以形成公共源极区CS。公共源极线CSL和绝缘间隔物140可以形成在沟槽T中。公共源极线CSL可以电连接到公共源极区CS，绝缘间隔物140可以使公共源极线CSL与电极130、135、138a和138b电绝缘。

[0135] 第一绝缘层145可以形成在基板100的整个顶表面上。第一绝缘层145可覆盖电极结构，并且可在平行于基板100的顶表面的方向上延伸以覆盖绝缘间隔物140的顶表面和公共源极线CSL的顶表面。

[0136] 位线接触插塞152可以形成为穿透第一区R1的第一绝缘层145。位线接触插塞152可以分别连接到竖直图案VP和DVP中的单元竖直图案VP。换句话说，位线接触插塞152可以不形成在虚设竖直图案DVP上。

[0137] 接触插塞150sa、150sb、150c和150g可以形成为穿透第二区R2中的第一绝缘层145、盖绝缘层115和绝缘层110。接触插塞150sa、150sb、150c和150g可以分别连接到焊盘138Pa、138Pb、135P和130P。

[0138] 位线BL可以形成在第一区R1中的第一绝缘层145上，第一互连154可以形成在第二区R2中的第一绝缘层145上。位线BL可以连接到位线接触插塞152，第一互连154可以分别连接到接地选择接触插塞150g和单元接触插塞150c。

[0139] 参考图14和15，第二绝缘层160可以形成在第一绝缘层145、位线BL和第一互连154上。第一上互连170a和第二上互连170b可以形成在第二绝缘层160上。第一上互连170a可以经由第一互连插塞165a和第一串选择接触插塞150sa而电连接到第一串选择焊盘138Pa。第二上互连170b可以经由第二互连插塞165b和第二串选择接触插塞150sb而电连接到第二串选择焊盘138Pb。第一和第二互连插塞165a和165b可穿透第二区R2的第二绝缘层160。

[0140] 根据实施方式，提供了具有优良的可靠性的3D半导体器件。即，虚设柱可穿透在基板的第二区中构成阶梯结构的焊盘，从而与基板接触。穿透每个单元焊盘的虚设柱可穿透相邻单元焊盘之间的边界，所以每个单元焊盘和与其两侧相邻的焊盘可共用穿透每个单元焊盘的虚设柱。因为在电极结构中相邻的单元焊盘共用虚设柱，所以支撑电极结构的虚设柱的数量被最小化。此外，支撑电极结构的最小数量的虚设柱使电极结构的形状变化最小化。另外，因为在形成电极结构的置换工艺期间使用了支撑模制层叠结构的最小数量的虚设柱，所以单元焊盘的形状变化可以最小化，由此最小化或防止电极结构的劣化。

[0141] 此外，穿透每个单元焊盘的虚设柱可以设置为当从平面图看时围绕连接到每个单元焊盘的单元接触插塞。因此，单元接触插塞和与其相邻的公共源极线之间的距离可以增大以使单元接触插塞与公共源极线容易地绝缘。

[0142] 在此已经公开了实例实施方式，虽然采用了特定术语，但是它们仅以一般描述性含义被使用和解释，而不是为了限制。在一些情况下，如对于提交本申请时本领域普通技术人员将明显的是，结合具体实施方式描述的特征、特性和/或元件可以单独使用或与结合其他实施方式描述的特征、特性和/或元件组合，除非另外特别地声明。因此，本领域普通技术人员将理解，可以进行形式和细节上的各种改变而没有脱离在权利要求中阐述的本发明的精神和范围。

[0143] 2015年4月1日向韩国知识产权局提交并且发明名称为“Three-Dimensional Semiconductor(三维半导体器件)”的韩国专利申请No.10-2015-0046040通过引用被整体结合于此。

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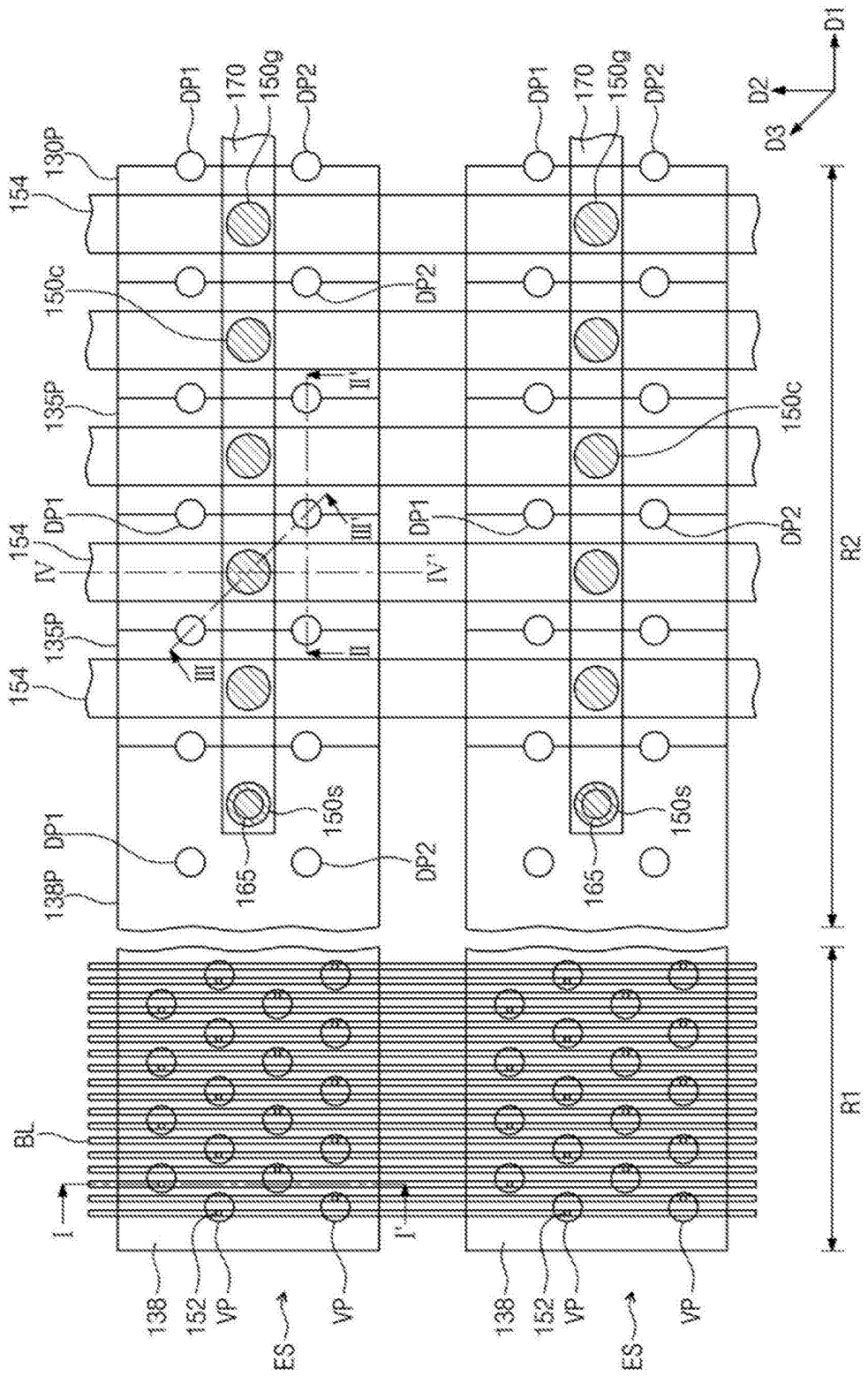


图1

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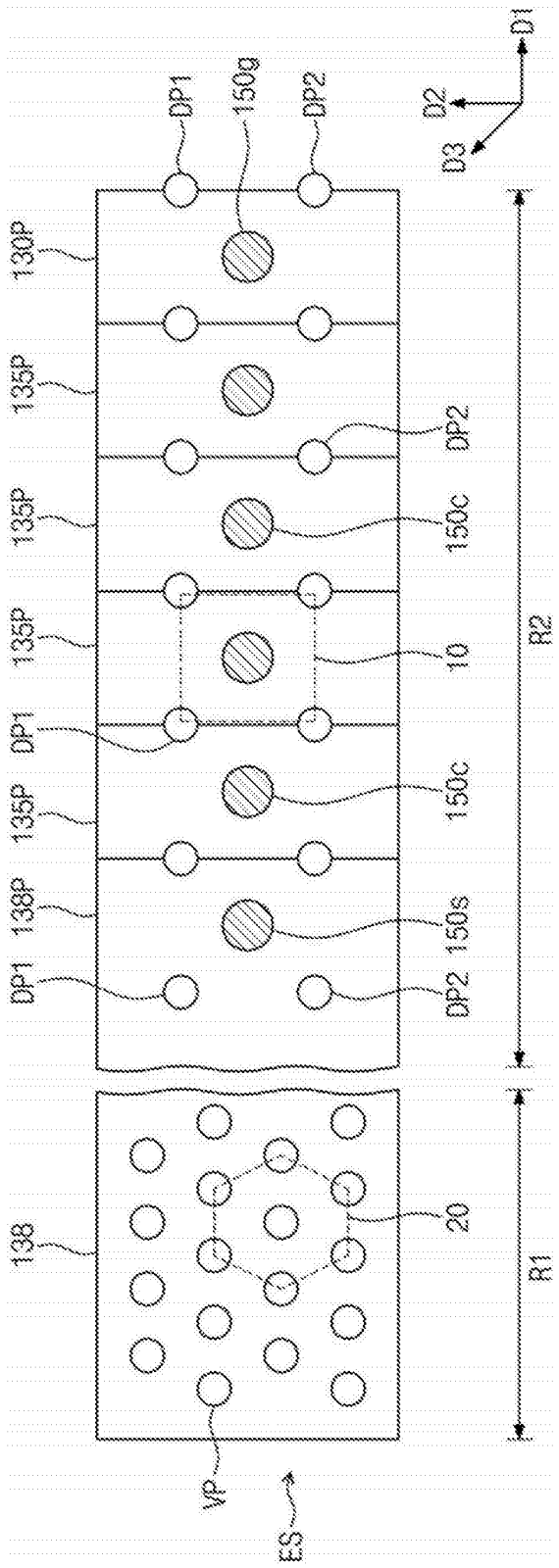


图2

Micron Ex. 1002, p. 139
Micron v. YMTC
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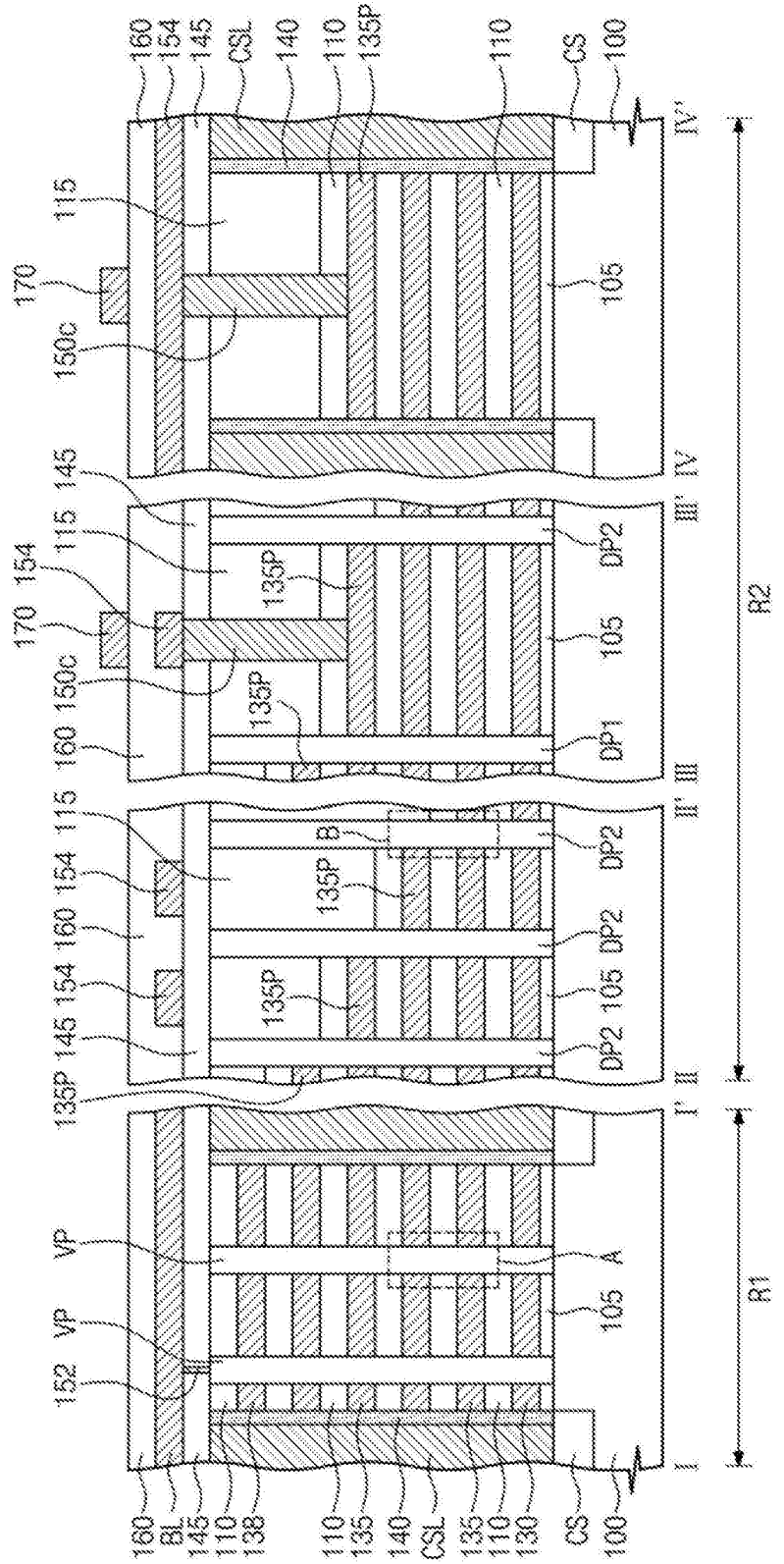


图3

Micron Ex. 1002, p. 140
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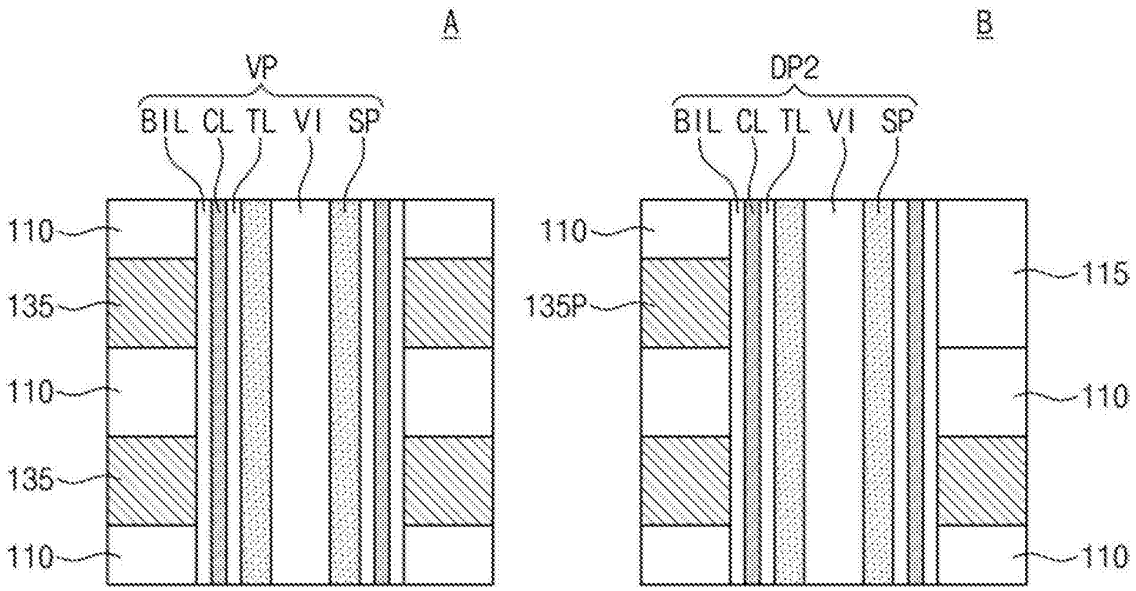


图4A

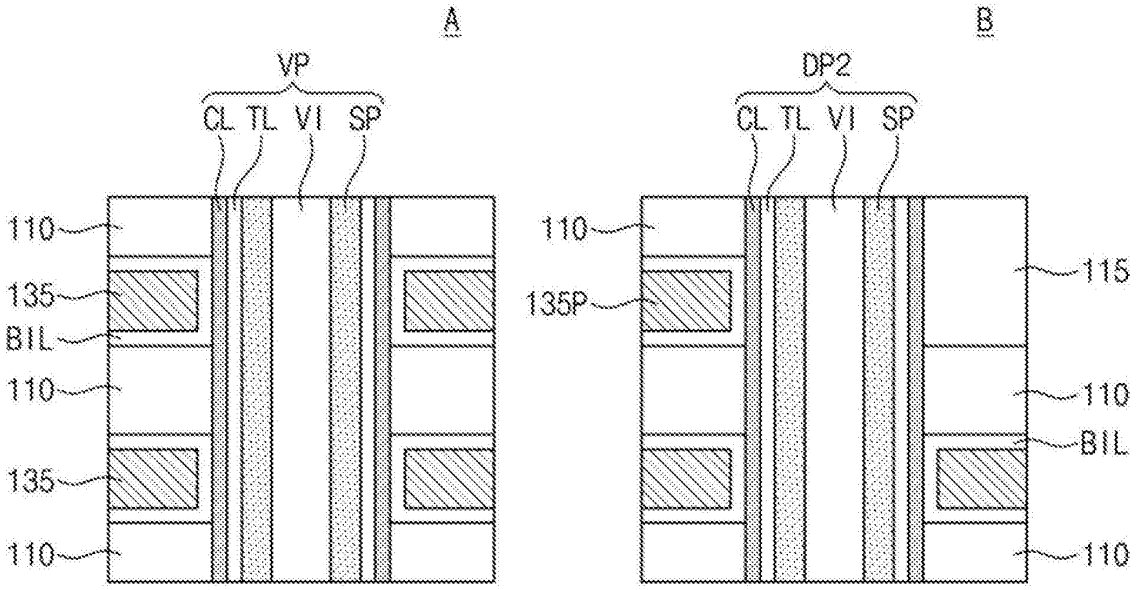


图4B

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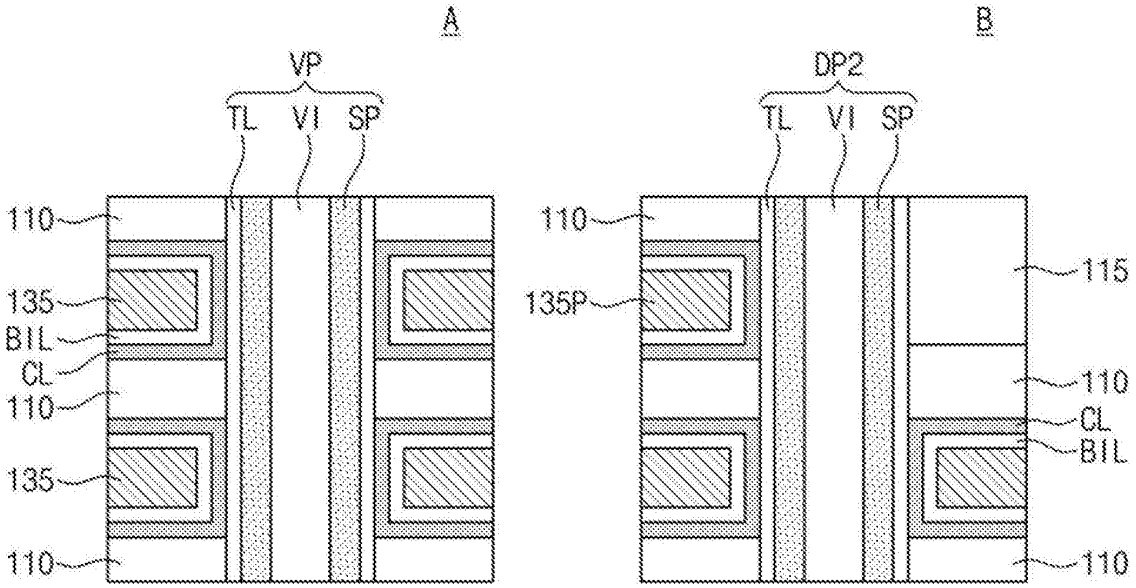


图4C

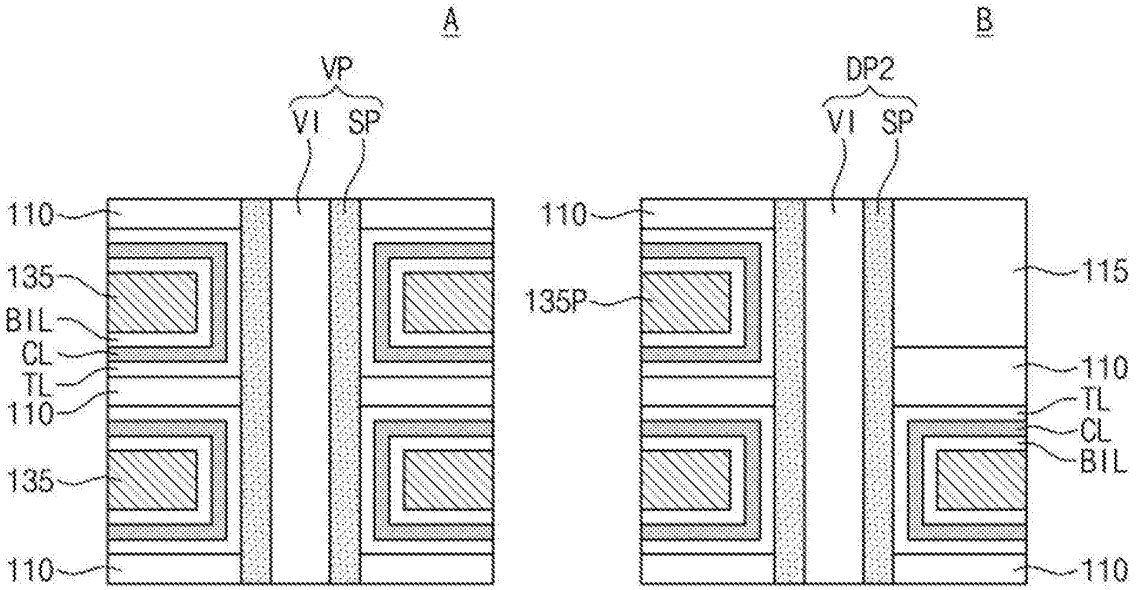


图4D

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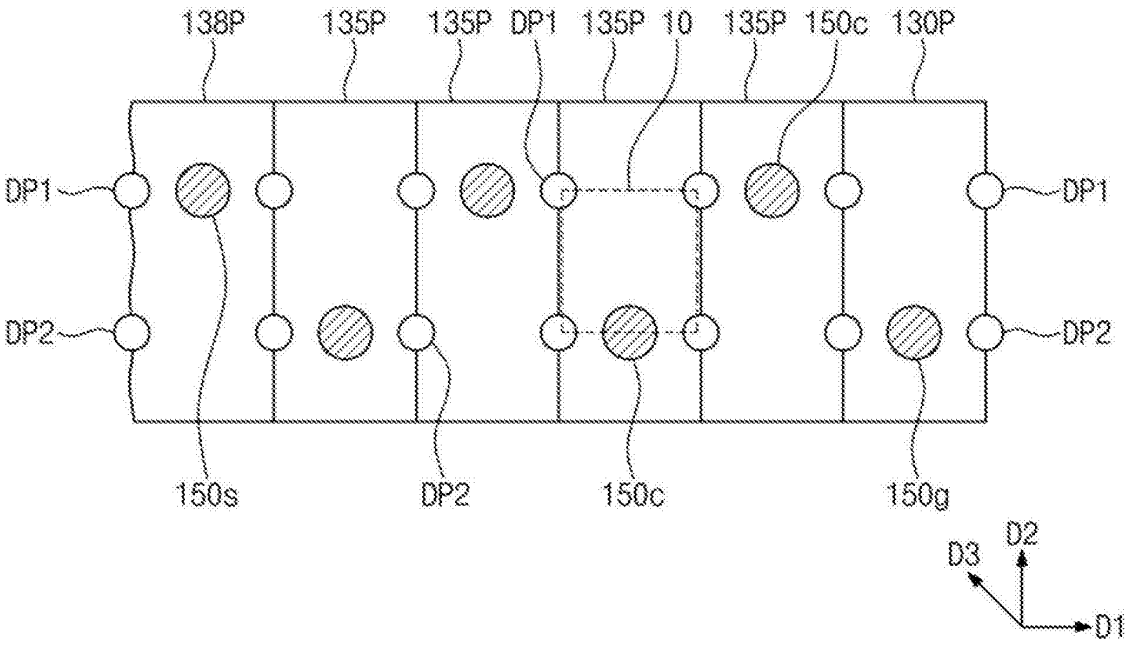


图5

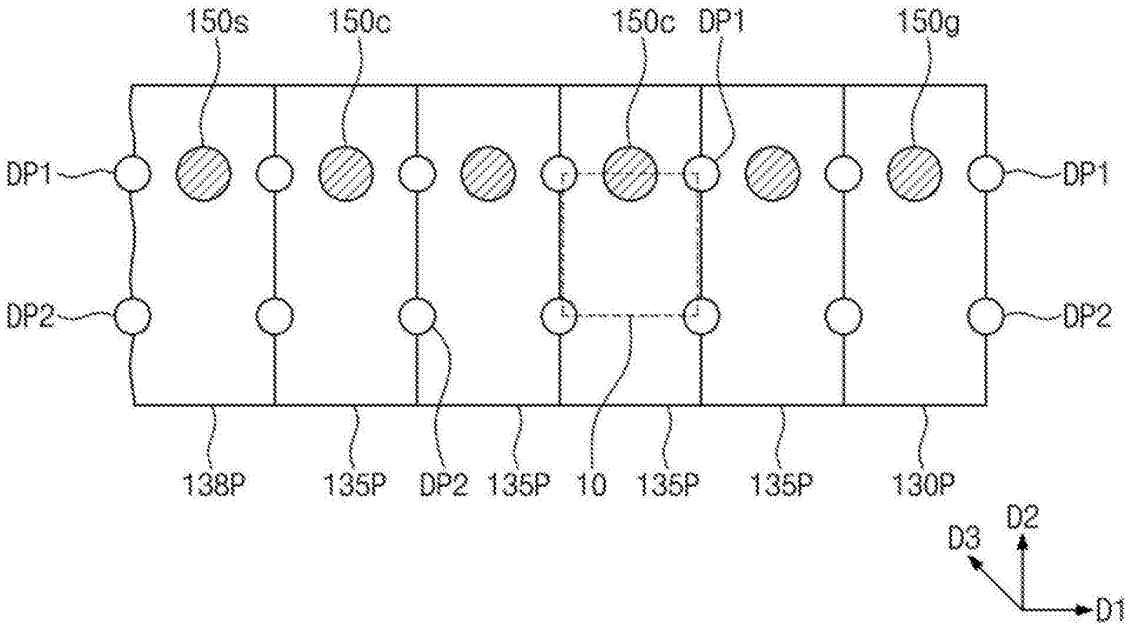


图6

Micron Ex. 1002, p. 143
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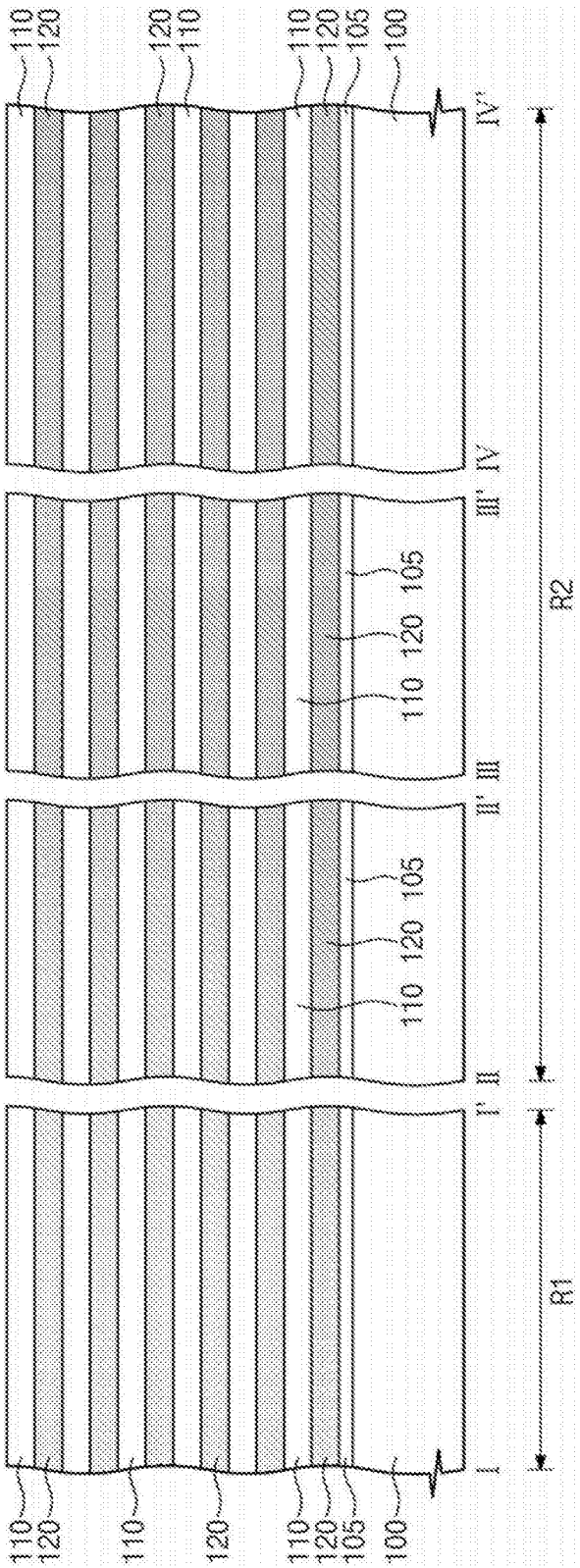


图7

Micron Ex. 1002, p. 144
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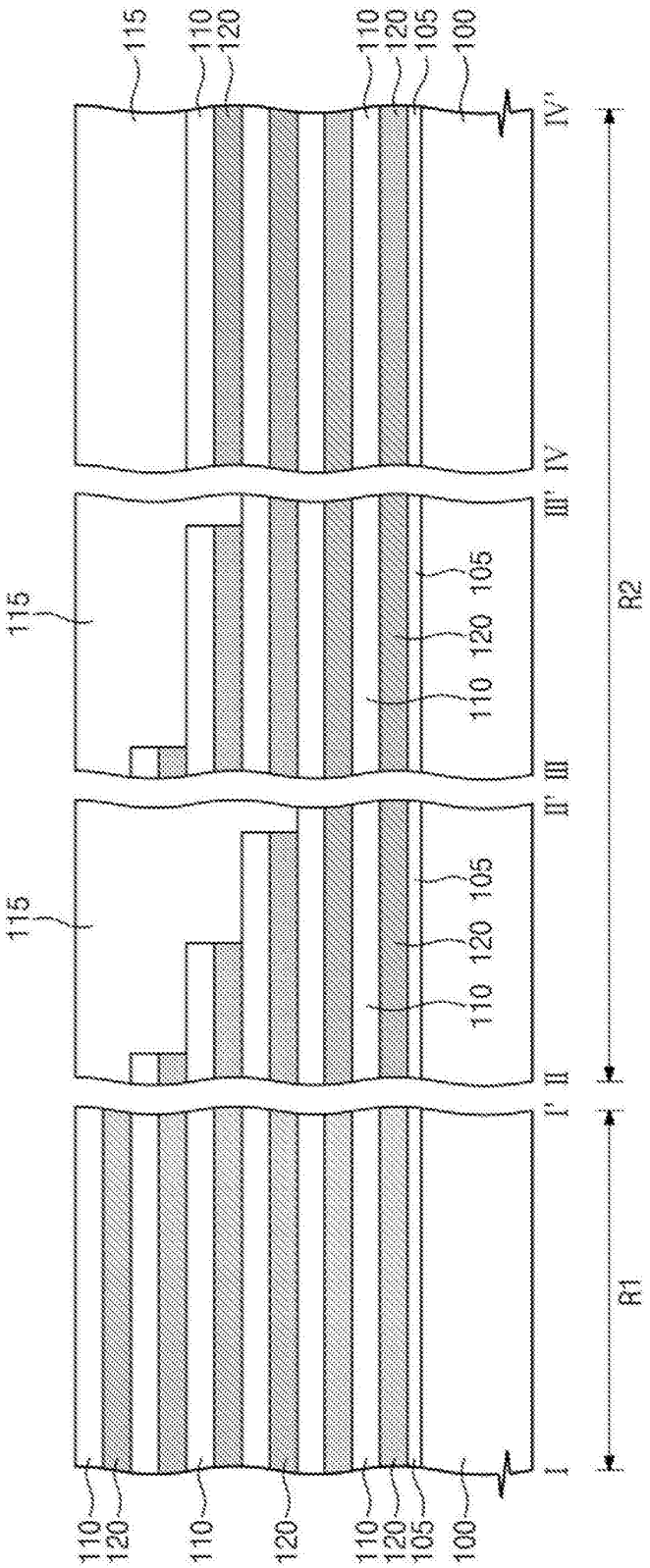


图8

Micron Ex. 1002, p. 145
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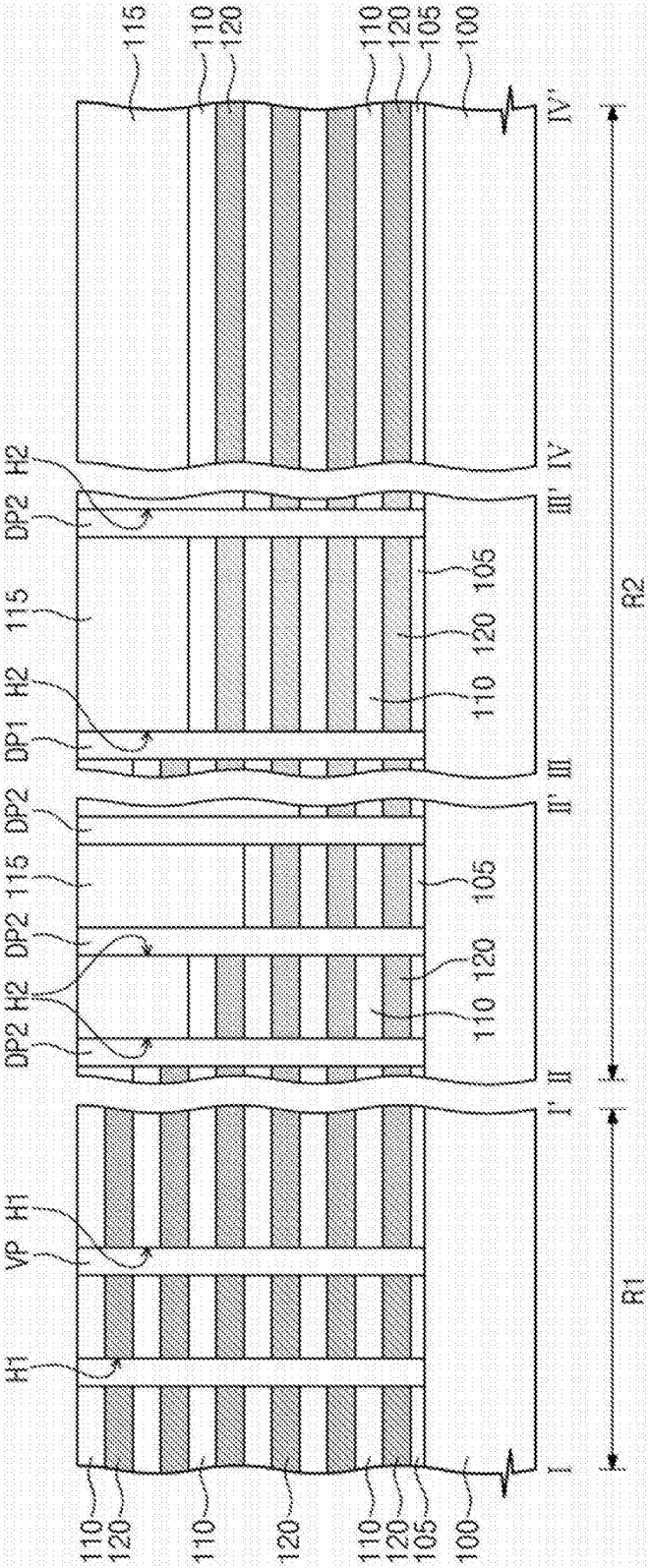


图9

Micron Ex. 1002, p. 146
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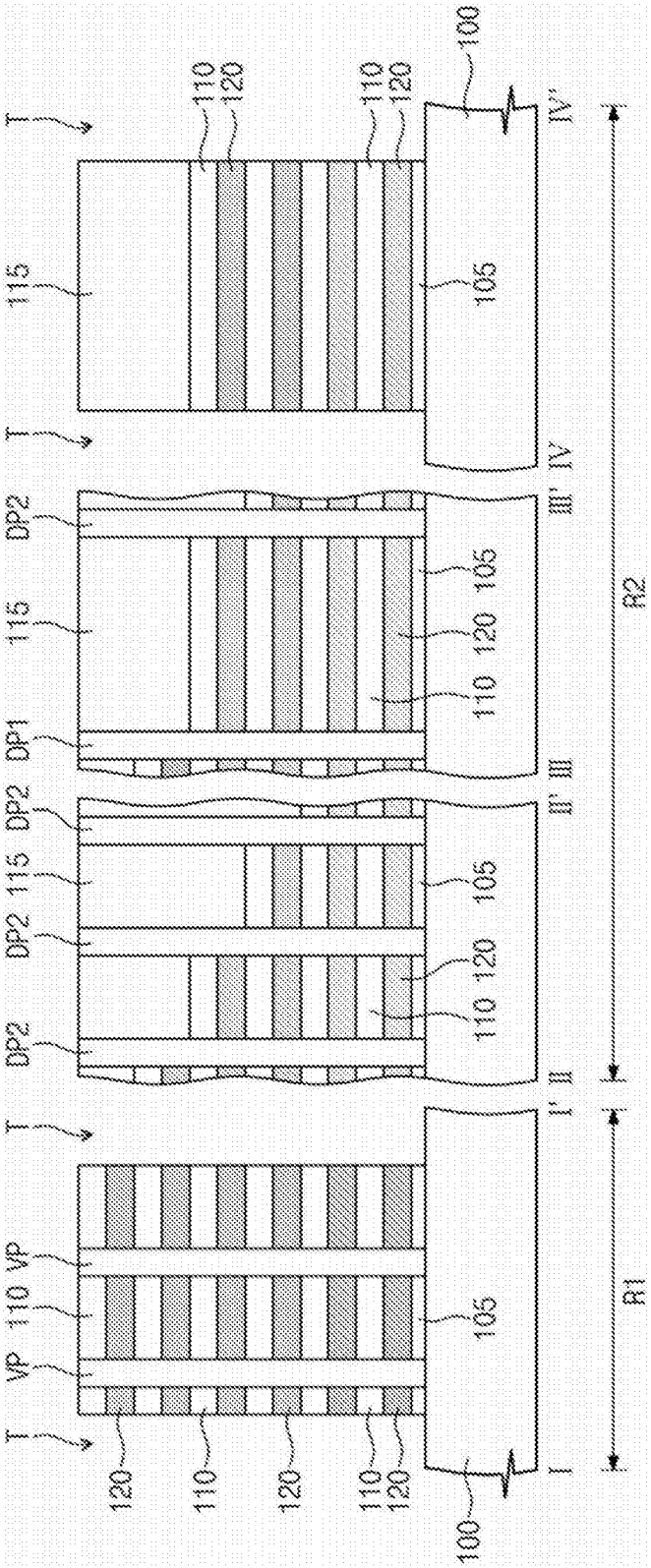


图10

Micron Ex. 1002, p. 147
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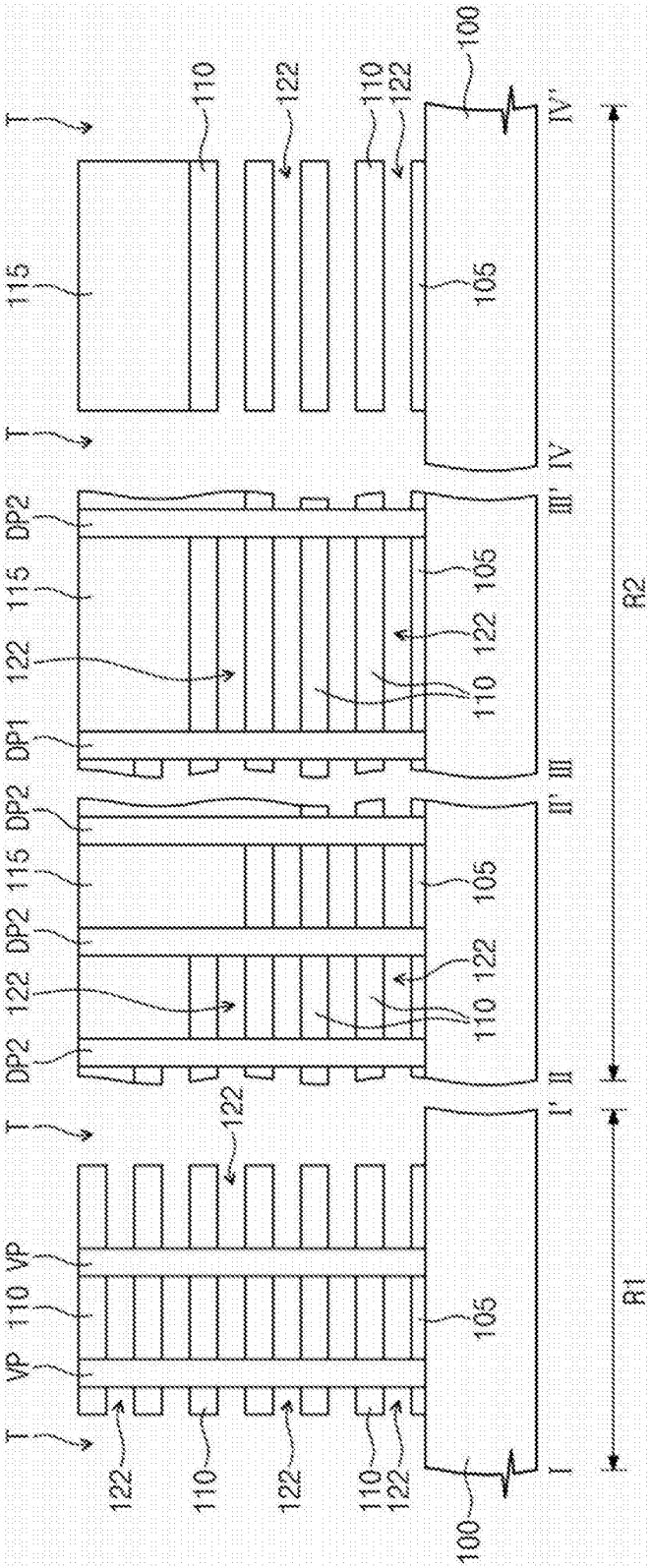


图11

Micron Ex. 1002, p. 148
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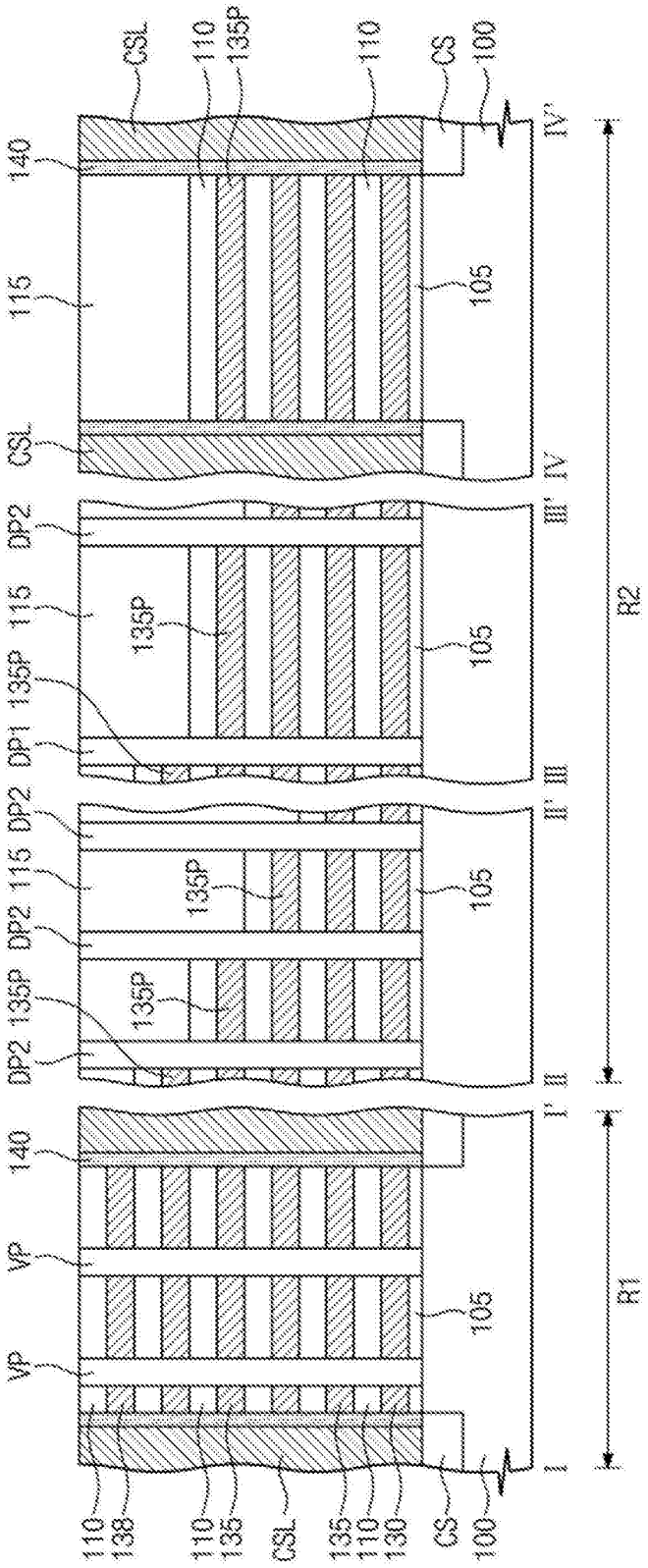


图12

Micron Ex. 1002, p. 149
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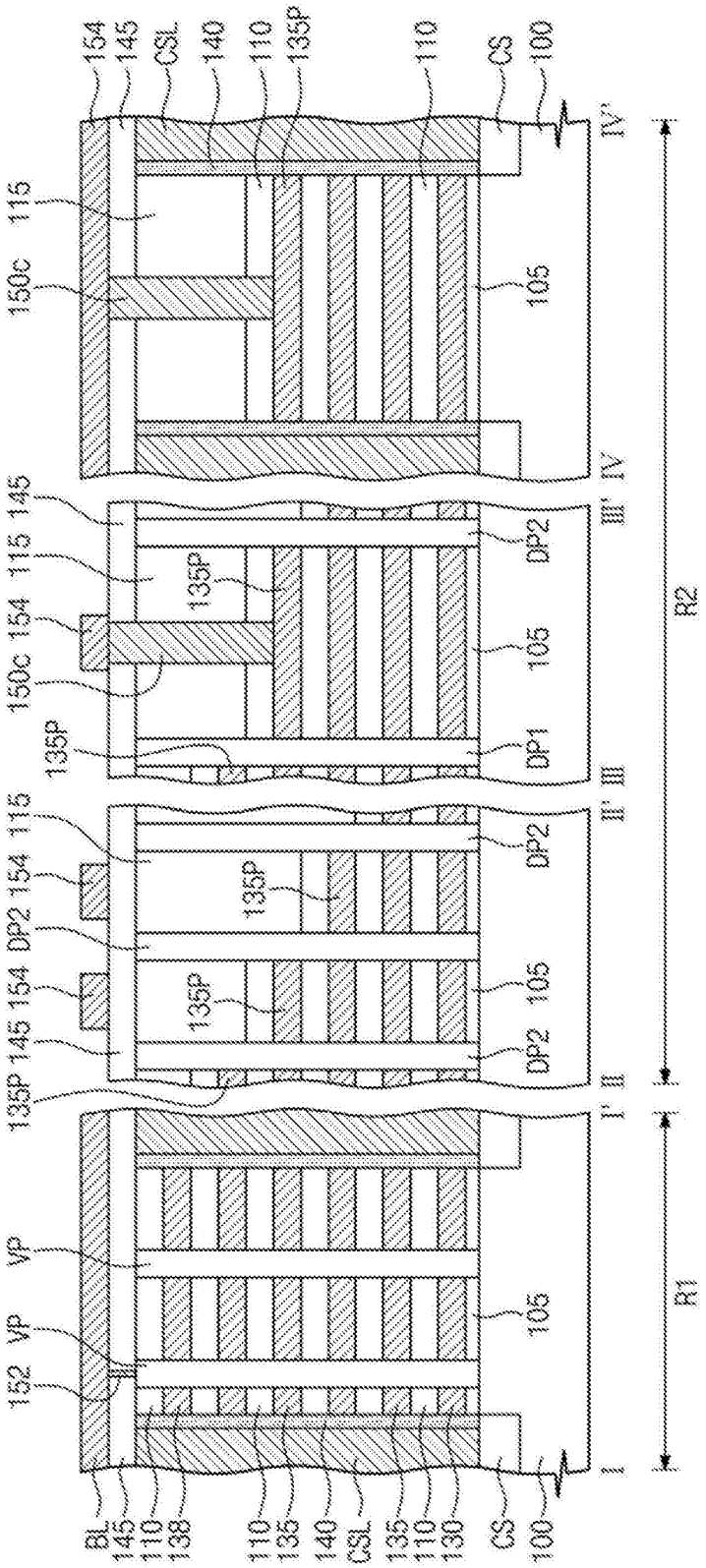


图13

Micron Ex. 1002, p. 150
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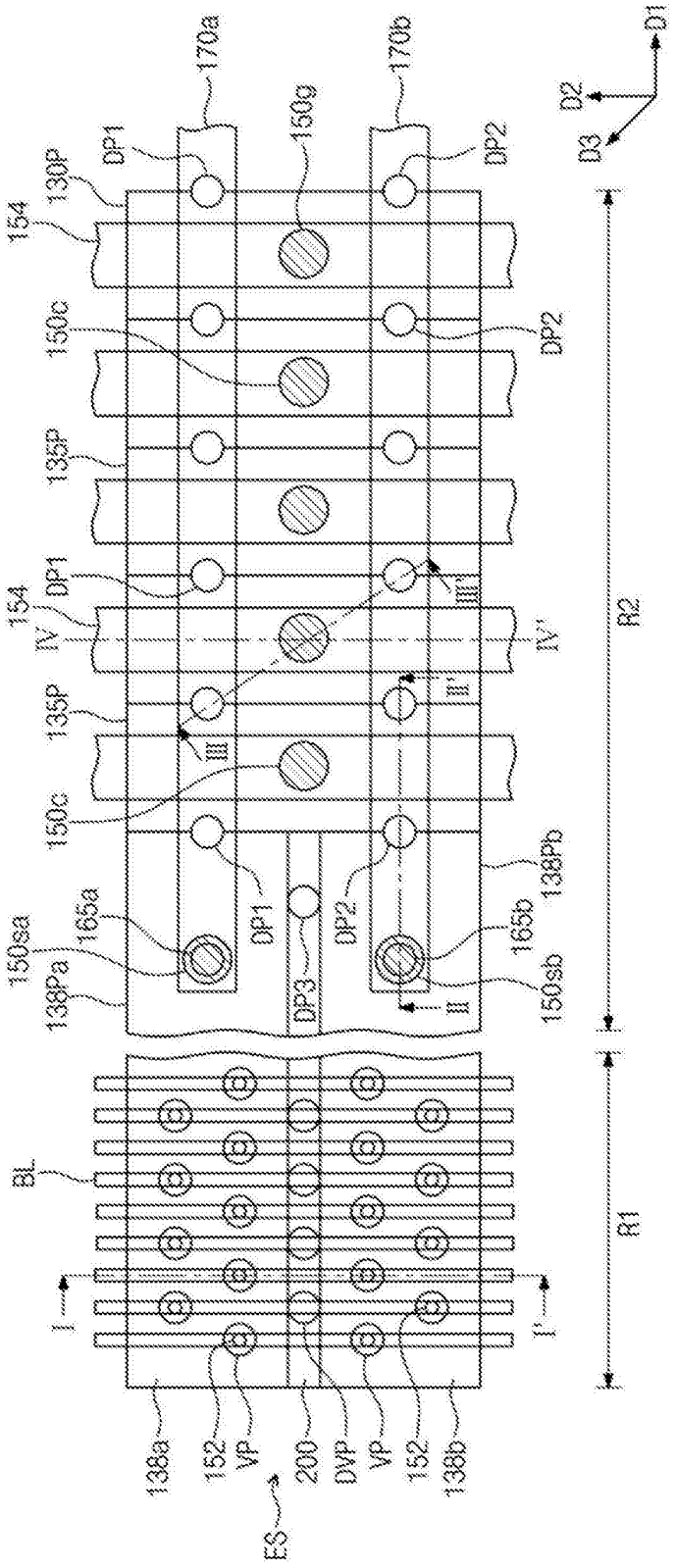


图14

Micron Ex. 1002, p. 151
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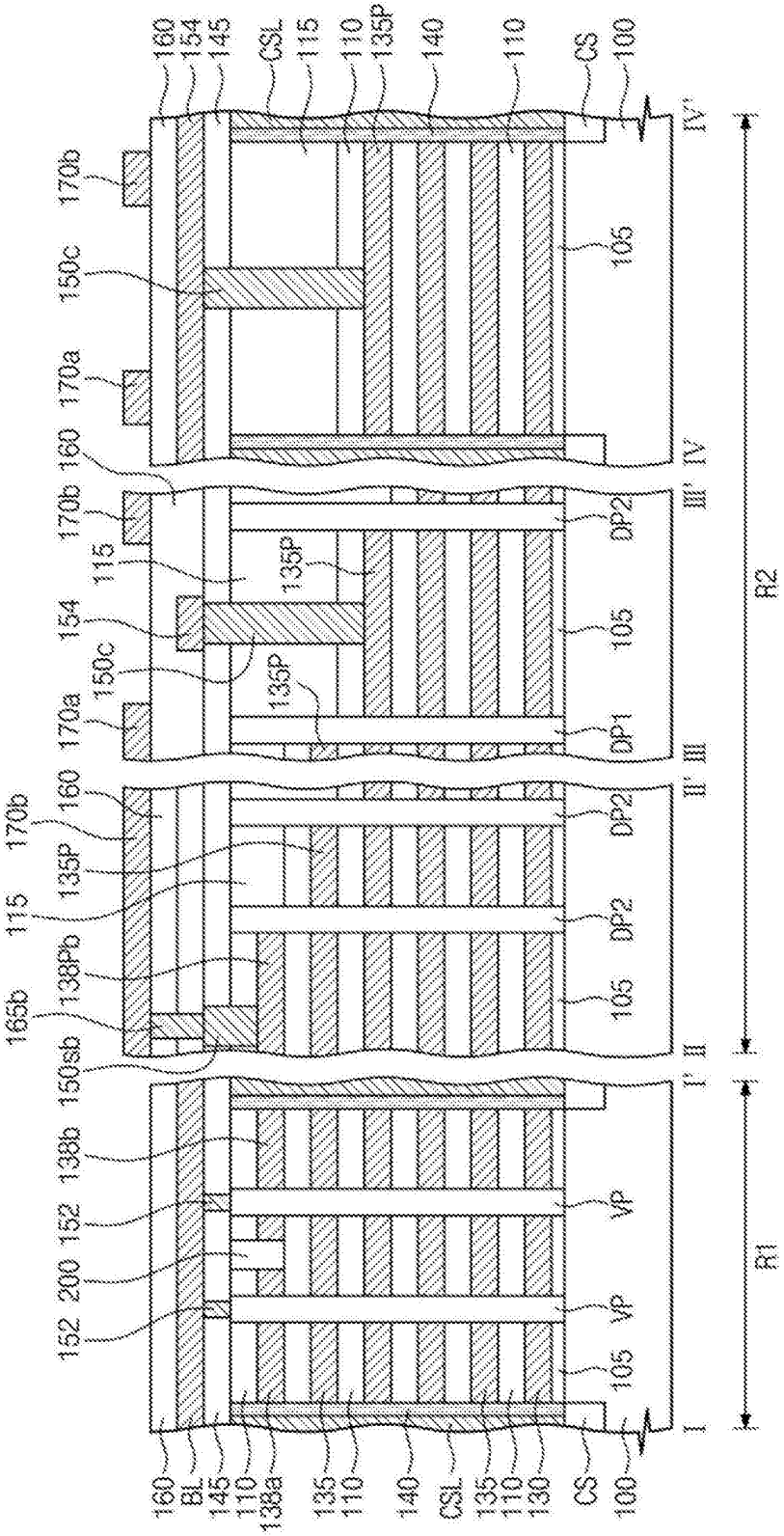


图15

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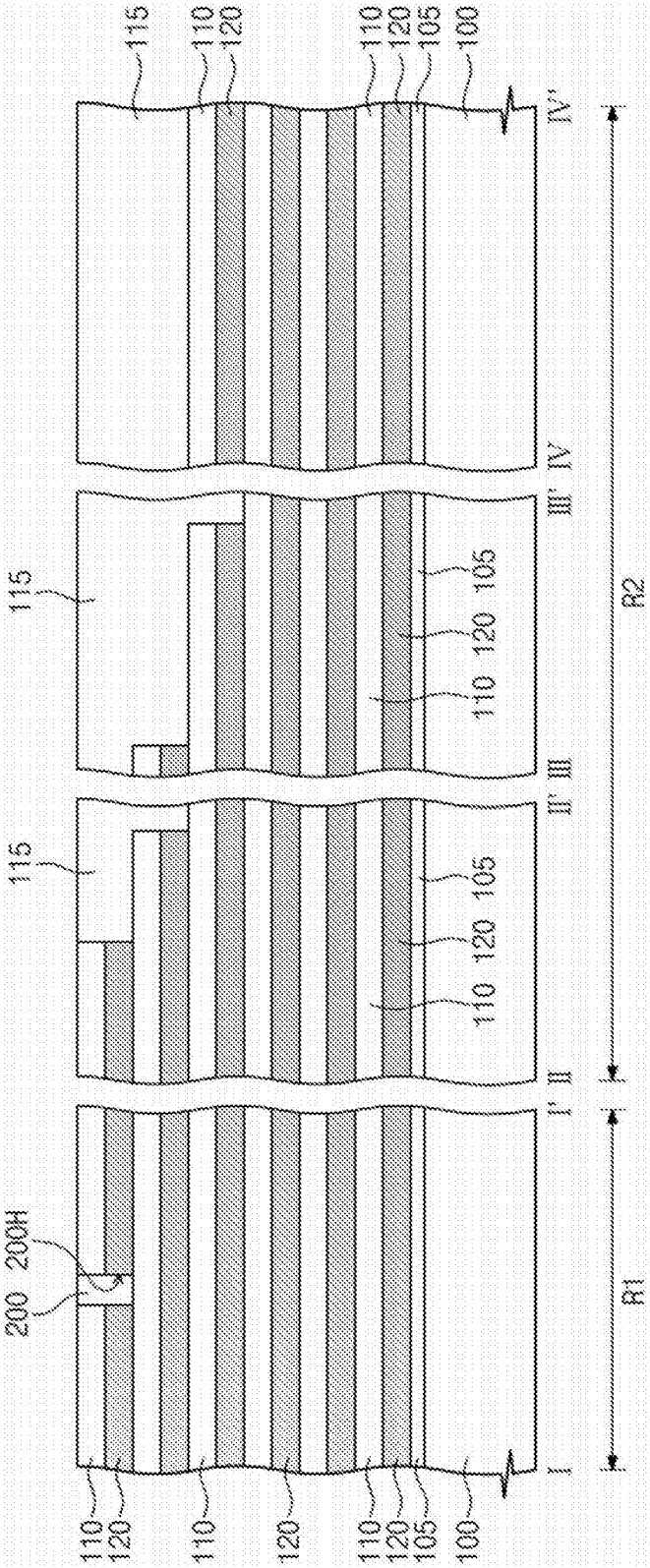


图16

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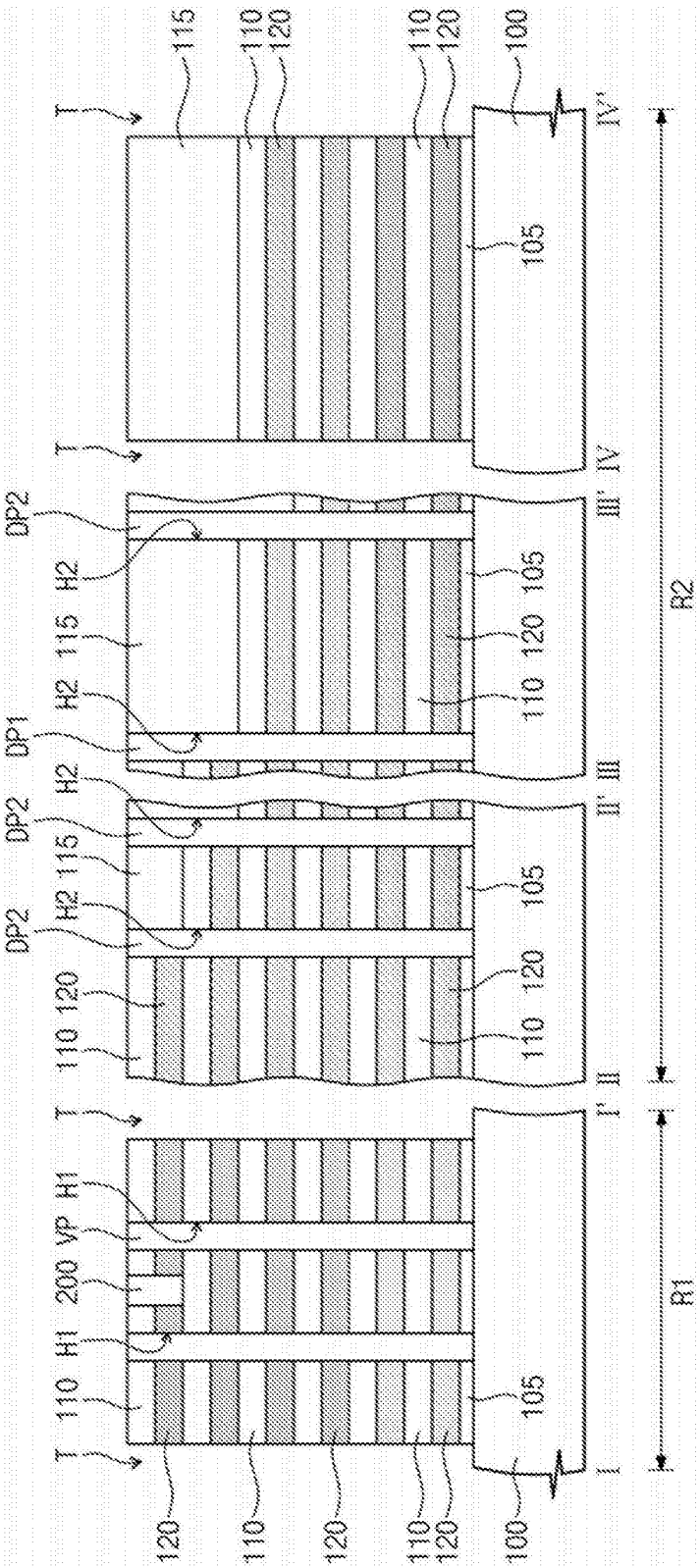


图17

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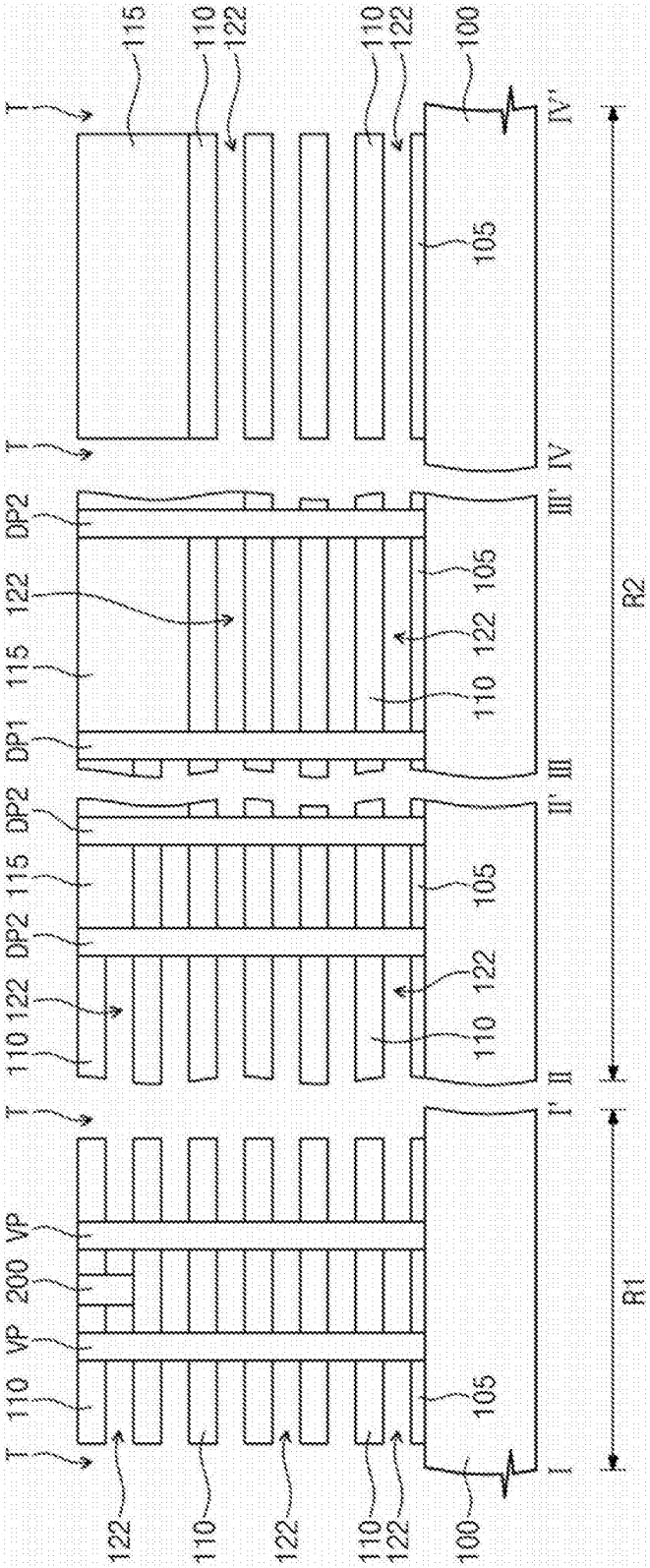


图18

Micron Ex. 1002, p. 155
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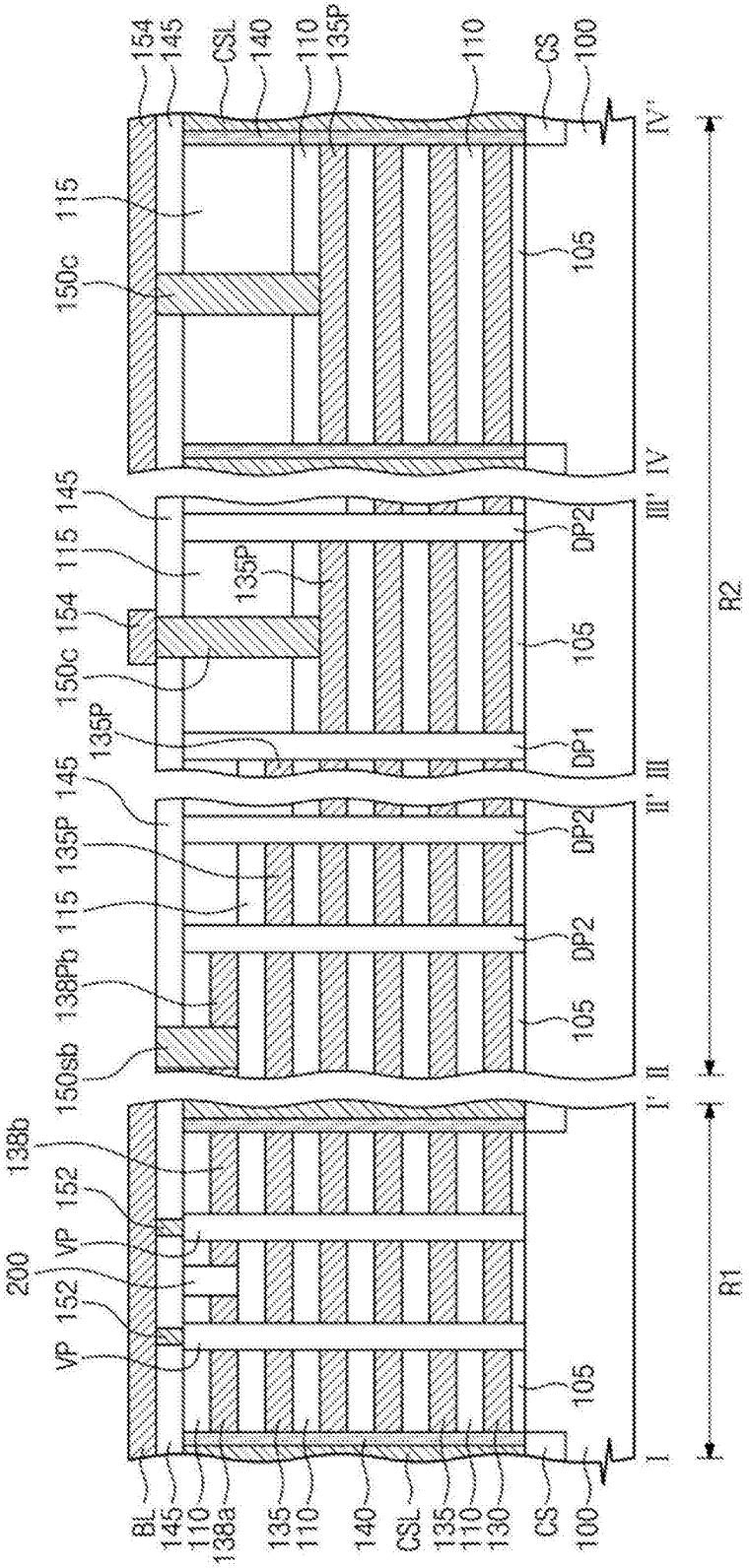


图19

Micron Ex. 1002, p. 156
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PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
P2019TC728		
International application No.	International filing date *(day/month/year)*	(Earliest)Priority date *(day/month/year)*
PCT/CN2019/076186	26 Feb. 2019 (26. 02. 2019)	

Applicant

YANGTZE MEMORY TECHNOLOGIES CO., LTD.

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 4 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed

☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6bis(a)).

c. ☐ With regard to any **nucleotide and /or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II)

3. ☐ **Unity of invention is lacking** (see Box No. III)

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. The figure of the **drawings** to be published with the abstract is Figure No. 1A

☒ as suggested by the applicant

☐ as selected by this Authority, because the applicant failed to suggest a figure

☐ as selected by this Authority, because this figure better characterizes the invention

b. ☐ none of the figures is to be published with the abstract

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2019/076186

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/11578(2017.01)i; H01L 27/11563(2017.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
CNABS, SIPOABS, CNTXT, DWPI, CNKI: memory, substrate, stack, conductive, dielectric, stair+, step+, contact, dummy, source, channel, sacrificial, hole?, spacer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 108962910A (SAMSUNG ELECTRONICS CO LTD) 07 Dec.2018(07.12.2018) description, paragraphs [0017]-[0078], claim 1, figures 1-15	30-40
Y	CN 108962910A (SAMSUNG ELECTRONICS CO LTD) 07 Dec.2018(07.12.2018) description, paragraphs [0017]-[0078], claim 1, figures 1-15	1-29
Y	CN 106057813A (SAMSUNG ELECTRONICS CO LTD) 26 Oct.2016(26.10.2016) description, paragraphs [0050]-[0091], figures 1-4	1-29
A	US 8822285B2 (SK HYNIX INC) 02 Sep.2014(02.09.2014) the whole document	1-40

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&"document member of the same patent family
Date of the actual completion of the international search 14 Oct. 2019(14. 10. 2019)	Date of mailing of the international search report 23 Oct. 2019(23. 10. 2019)
Name and mailing address of the ISA/CN National Intellectual Property Administration, PRC 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China Facsimile No.(86-10)62019451	Authorized officer SUN, Weiwei Telephone No.: 62412076

Form PCT/ISA /210 (3 sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2019/076186

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
CN108962910A	07.12.2018	KR20180126210A	27.11.2018
		US2018337192A1	22.11.2018
CN106057813A	26.10.2016	US9748258B2	29.08.2017
		US2016293622A1	06.10.2016
		KR20160118421A	12.10.2016
US8822285B2	02.09.2014	US2013161821A1	27.06.2013
		KR20130072522A	02.07.2013

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PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:

100013

10th Floor, Tower C, Beijing Global Trade Center, 36 North Third Ring Road East, Dongcheng District, Beijing, China

NTD UNIVATION INTELLECTUAL PROPERTY AGENCY LTD.

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43 *bis*.1)

	Date of mailing(*day/month/year*) 23. Oct. 2019 (23. 10. 2019)
Applicant's or agent's file reference P2019TC728	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date(*day/month/year*)	Priority date (*day/month/year*)
PCT/CN2019/076186	26. Feb. 2019 (26. 02. 2019)	

International Patent Classification (IPC) or both national classification and IPC

H01L 27/11578 (2017. 01) i; H01L 27/11563 (2017. 01) i

Applicant

YANGTZE MEMORY TECHNOLOGIES CO., LTD.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No.II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No.VI Certain documents cited
- ☒ Box No. VII Certain defects in the international application
- ☐ Box No.VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of **3** months from the date of mailing of Form PCT/ISA/220 or before the expiration of **22** months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/CN	Date of completion of this opinion	Authorized officer
National Intellectual Property Administration, PRC 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China Facsimile No. (86—10) 62019451	15. Oct. 2019 (15. 10. 2019)	**SUN,Weiwei** Telephone No.:**62412076**

Form PCT/ISA/237 (cover sheet) (January 2015)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CN2019/076186

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of:
☒ the international application in the language in which it was filed.
☐ a translation of the international application into_____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91(Rule 43bis.1(b))

3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:

a. ☐ forming part of the international application as filed:
☐ in the form of an Annex C/ST.25 text file.
☐ on paper or in the form of an image file.

b. ☐ furnished together with the international application under PCT Rule 13ter.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.

c. ☐ furnished subsequent to the international filing date for the purposes of international search only:
☐ in the form of an Annex C/ST.25 text file (Rule 13ter.1(a)).
☐ on paper or in the form of an image file (Rule 13ter.1(b) and Administrative Instructions, Section 713).

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

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WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CN2019/076186

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement:

Novelty (N)	Claims 1-40	YES
	Claims None	NO
Inventive step (IS)	Claims None	YES
	Claims 1-40	NO
Industrial applicability (IA)	Claims 1-40	YES
	Claims None	NO

2. Citations and explanations

(1) Reference is made to the following documents:

D1: CN108962910 A 07 December 2018 (07.12.2018)

D2: CN106057813 A 26.December 2016 (26.10.2016)

(2) D1 is regarded as being the closest prior art to the subject-matter of claims 1, 17 , 30 and 37.

D1 discloses a vertical memory device and a method of manufacturing a vertical memory device (description, paragraphs [0017]-[0078], claim 1, figures 1-15): a substrate 100 which includes a first region R1 and a second region R2. A conductive pattern structure 140 is formed on R1. A pad structure 142, a dummy channel structure 118b and a contact plug 144 is formed on R2. The conductive pattern structure 140 may include conductive patterns 126 and insulation layers 102 alternately stacked in an interleaved manner. The edges of the conductive patterns 126 may be arranged in a staircase configuration shape. The contact plugs 144 contact upper surfaces of the conductive patterns 126 in the pad structure 142 and may be formed on respective ones of the steps. The conductive pattern structure 140 may extend in the first direction. A plurality of dummy channel structures may extend through the conductive pads in the second direction which is perpendicular to the first direction. Figures 3 to 15 illustrate stages of a method of manufacturing a vertical memory device. Referring to FIG. 3, insulation layers 102 and sacrificial layers 104 may be alternately formed on the substrate 100. Referring to FIGS. 4, 5 and 6, edge portions of the preliminary mold structure 106 on R2 may be sequentially etched to form a preliminary step mold structure 106a. The dummy channel holes 112 may be formed through the preliminary step mold structure 106a on R2. Dummy channel structures may be formed in the dummy channel hole 112. The sacrificial layers 104 of the preliminary step mold structure 106a on R1 may be transformed into conductive patterns of memory cells. Referring to FIG. 12, the sacrificial layers 104 may be removed by an isotropic etching process. Referring to FIG. 13, a conductive layer may be formed to fill the gaps 124 so that conductive

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patterns 126 may be formed on R1 and R2. Referring to FIGS. 14 and 15, respective contact plugs 144 may be formed on the conductive patterns 126 in the pad structure 142, through the first and second upper insulating interlayers 108 and 109.

Claim 1 or 17 therefore differs from D1 in that: (1) a plurality of dummy source structures each extending vertically through the staircase structure; (2) the plurality of dummy source structures surrounding the staircase contact or a subset of the dummy channel structures is surrounded by the plurality of dummy source structures.

Claim 30 therefore differs from D1 in that: (3) a plurality of dummy source holes; a subset of the dummy channel holes is surrounded by the plurality of dummy source holes; the step of forming a spacer; the step of forming a contact within the spacer.

Claim 37 therefore differs from D1 in that: (4) a plurality of dummy source holes; the plurality of dummy source holes are aligned with a portion of the plurality of dummy channel holes in a row along a lateral direction in a plan view; the step of depositing a sealing layer; the step of etching away the sealing layer; the step of depositing a spacer.

Claims 1, 17, 30 and 37 and the dependent claims 2-16, 18-29, 31-36 and 38-40 are therefore novel under PCT Article 33 (2). The problem solved by claims 1, 17, 30 and 37 is how to limit the density of 3D memory device.

D2 discloses (description, paragraphs [0050]-[0091], figures 1-4): the dummy pillars DP1 and DP2 vertically penetrating each of the cell pads 130P, 135P or 138P may be arranged to surround the cell contact plug 150g or 150c or 150s connected to each of the cell pads 130P, 135P ors 138P in FIG. 2. The electrodes 130, 135, and 138 may respectively include pads 130P, 135P, and 138P that constitute a stepped structure in the second region R2. The features (1) and (2) are disclosed by D2. The features (3) and (4) are common general knowledge on the basis of D1 and D2. Claims 1, 17, 30 and 37 do not involve an inventive step in the sense of PCT Article 33(3).

The appended feature in claims 2-6, 11-12 are disclosed in D2. The appended feature in claims 7-8 and 10 are disclosed in D1. The appended feature in claims 9, 13-16, 18-29, 31-36 and 38-40 are common general knowledge. Claims 2-16, 18-29, 31-36 and 38-40 do not involve an inventive step in the sense of PCT Article 33(3).

(3) Claims 1-40 are industrially applicable under PCT Article 33(4), because the technical schemes claimed can be made or used in the industry.

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WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/CN2019/076186

Box No. VII Certain defects in the international application

The following defects in the form or contents of the international application have been noted:

Claims 4, 5, 7, 9-13, 15, 16, 20, 21, 24, 26, 28, 29, 33, 35, 40 are dependent claims referring back to several previous claims, but one or more of previous claims 3-5, 7, 9-13, 19, 20, 21, 24, 26, 32, 33, 39 they referring back are also dependent claims and refers back to another several previous claims, thereby claims 4, 5, 7, 9-13, 15, 16, 20, 21, 24, 26, 28, 29, 33, 35, 40 do not meet the requirements of Rule 6.4(a)PCT.

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Electronic Acknowledgement Receipt

EFS ID:	37696323
Application Number:	16402202
International Application Number:	
Confirmation Number:	7288
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Wenyu Hua
Customer Number:	153988
Filer:	Zhiwei Zou/Anna O'Connor
Filer Authorized By:	Zhiwei Zou
Attorney Docket Number:	10018-01-0045-US
Receipt Date:	08-NOV-2019
Filing Date:	02-MAY-2019
Time Stamp:	12:03:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	10018-01-0045-US_IDS_SB08.pdf	612200 1316b489124bcd1afe2b7e870ef5fe3dac8354e2	no	4

Warnings:

Information:					
2	Foreign Reference	CN108962910_Bibl.pdf	4129598 de2f14995b3434d66c437bf3d27bdff889aca113	no	36
Warnings:					
Information:					
3	Foreign Reference	CN106057813_Bibl.pdf	4803571 9d3be8601aab5828d8bf4c8771ce290a5f2bda19	no	40
Warnings:					
Information:					
4	Other Reference-Patent/App/Search documents	2018-00434-YMTC-PCT-P2019TC728-210.pdf	188181 40b1d13b2f56000dc6b34a20955bcb4ca2155834	no	4
Warnings:					
Information:					
5	Other Reference-Patent/App/Search documents	2018-00434-YMTC-PCT-P2019TC728-237.pdf	329839 92790fb750092968e80d255803370eaafe84401e	no	5
Warnings:					
Information:					
		Total Files Size (in bytes):	10063389		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	16402202
Filing Date	2019-05-02
First Named Inventor	Wenyu HUA
Art Unit	2811
Examiner Name	GURLEY, LYNNE ANN
Attorney Docket Number	10018-01-0045-US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	109103199	CN	A	2018-12-28	YANGTZE MEMORY TECH CO LTD		

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16402202
	Filing Date	2019-05-02
	First Named Inventor	Wenyu HUA
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	10018-01-0045-US

	1		

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Micron v. YMTC
IPR2024-00789

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16402202
	Filing Date	2019-05-02
	First Named Inventor	Wenyu HUA
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	10018-01-0045-US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2019-11-15
Name/Print	Zhiwei Zou	Registration Number	66,041

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Espacenet

Bibliographic data: CN109103199 (A) — 2018-12-28

3D memory device and manufacturing method thereof

Inventor(s): XIAO LIHONG; HU BIN ± (肖莉红, ; 胡斌)

Applicant(s): YANGTZE MEMORY TECH CO LTD ± (长江存储科技有限责任公司)

Classification: **- international:** ***H01L27/1157; H01L27/1158***
- cooperative: **H01L27/1157 (CN); H01L27/1158 (CN)**

Application number: CN201810892025 20180807 Global Dossier

Priority number(s): CN201810892025 20180807

Abstract of CN109103199 (A)

A 3D memory device and a manufacture method thereof are disclosed. The 3D memory device includes a first array structure including a semiconductor substrate, a first gate stack structure located abovethe semiconductor substrate, and a plurality of first channel pillars penetrating the first gate stack structure; a second array structure stacked over the first array structure, including a second gate stack structure over the first gate stack structure, a semiconductor layer over the second gate stack structure, and a plurality of second channel posts penetrating the second gate stack structure; and an interconnect structure between the first array structure and the second array structure, wherein the interconnect structure includes a plurality of bit lines, and the plurality of first channel posts are respectively connected to a respective one of the plurality of bit lines in common with a respective one of the plurality of second channel posts. The bit lines in the 3D memory device also serve as interconnects between array structures of different layers, thereby reducing the size of the 3D memory device and improving product yield.

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(19)中华人民共和国国家知识产权局

(12)发明专利申请

(10)申请公布号 CN 109103199 A
(43)申请公布日 2018.12.28

(21)申请号 201810892025.5

(22)申请日 2018.08.07

(71)申请人 长江存储科技有限责任公司
地址 430074 湖北省武汉市洪山区东湖开发区关东科技工业园华光大道18号7018室

(72)发明人 肖莉红 胡斌

(74)专利代理机构 北京成创同维知识产权代理有限公司 11449
代理人 蔡纯 刘静

(51)Int.Cl.
H01L 27/1157(2017.01)
H01L 27/1158(2017.01)

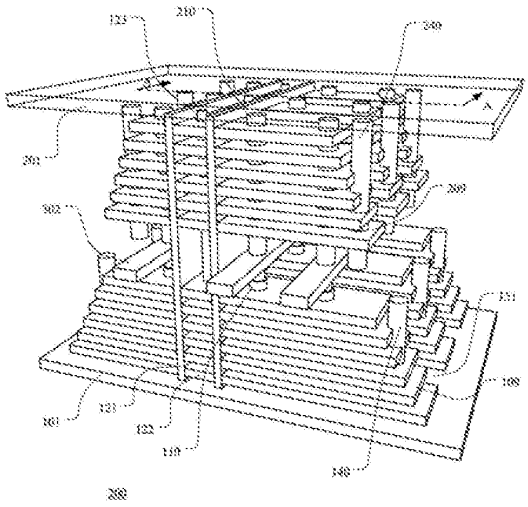
权利要求书3页 说明书11页 附图13页

(54)发明名称

3D存储器件及其制造方法

(57)摘要

本申请公开了一种3D存储器件及其制造方法。该3D存储器件包括:第一阵列结构,包括半导体衬底、位于半导体衬底上方的第一栅叠层结构、以及贯穿第一栅叠层结构的多个第一沟道柱;第二阵列结构,堆叠在第一阵列结构上方,包括位于第一栅叠层结构上方的第二栅叠层结构、位于第二栅叠层结构上方的半导体层、以及贯穿第二栅叠层结构的多个第二沟道柱;以及互连结构,位于第一阵列结构和第二阵列结构之间,其中,互连结构包括多条位线,多个第一沟道柱分别与多个第二沟道柱中的相应一个共同连接至多条位线中的相应一条位线。该3D存储器件中的位线兼作为不同层面的阵列结构之间的互连,从而可以减小3D存储器件的尺寸以及提高产品良率。



CN 109103199 A

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1.一种3D存储器件,包括:

第一阵列结构,所述第一阵列结构包括半导体衬底、位于所述半导体衬底上方的第一栅叠层结构、以及贯穿所述第一栅叠层结构的多个第一沟道柱;

第二阵列结构,堆叠在所述第一阵列结构上方,所述第二阵列结构包括位于所述第一栅叠层结构上方的第二栅叠层结构、位于所述第二栅叠层结构上方的半导体层、以及贯穿所述第二栅叠层结构的多个第二沟道柱;以及

互连结构,位于所述第一阵列结构和所述第二阵列结构之间,

其中,所述互连结构包括多条位线,所述多个第一沟道柱分别与所述多个第二沟道柱中的相应一个共同连接至所述多条位线中的相应一条位线。

2.根据权利要求1所述的3D存储器件,其中,所述第一栅叠层结构和所述第二栅叠层结构分别包括交替堆叠的多个栅极导体和多个层间绝缘层,并且所述多个栅极导体图案化为台阶状,从而形成台阶区域,在所述台阶区域提供字线的电连接区。

3.根据权利要求1所述的3D存储器件,其中,在所述第一阵列结构中,所述多个第一沟道柱位于所述第一栅叠层结构的中间区域,在所述第二阵列结构中,所述多个第二沟道位于所述第二栅叠层结构的中间区域。

4.根据权利要求1所述的3D存储器件,其中,所述第一阵列结构还包括位于所述台阶区域的多个第一伪沟道柱,所述多个第一伪沟道柱贯穿所述第一栅叠层结构中的一部分栅极导体且未连接至所述多条位线,所述第二阵列结构还包括位于所述台阶区域的多个第二伪沟道柱,所述多个第二伪沟道柱贯穿所述第二栅叠层结构中的一部分栅极导体且未连接至所述多条位线。

5.根据权利要求1所述的3D存储器件,还包括:位于所述半导体衬底中的CMOS电路。

6.根据权利要求5所述的3D存储器件,还包括:

第一绝缘层,用于围绕绝缘区域,所述第一栅叠层结构和所述第二栅叠层结构位于所述绝缘区域的外部;

第一绝缘叠层结构和第二绝缘叠层结构,位于所述绝缘区域的内部,并且分别与所述第一栅叠层结构和所述第二栅叠层结构相对应;以及

第一导电通道,位于所述绝缘区域的内部,从所述半导体衬底向上延伸,依次贯穿所述第一绝缘叠层结构、所述第二绝缘叠层结构,到达所述第二阵列结构的顶部,

其中,所述第一导电通道提供所述CMOS电路与外部电路之间的电连接。

7.根据权利要求6所述的3D存储器件,其中,所述第一导电通道包括多个导电柱组成的阵列。

8.根据权利要求1所述的3D存储器件,还包括:

第一公共源区,形成在所述半导体衬底中;

第一高压阱区,与所述第一公共源区邻接并且掺杂类型相反;

第二公共源区,形成在所述半导体层中;以及

第二高压阱区,与所述第二公共源区邻接并且掺杂类型相反,

其中,所述多个第一沟道柱的第一端分别接触所述多条位线中的相应一条位线,所述多个第二沟道柱的第一端分别接触所述多条位线中的相应一条位线,

所述多个第一沟道柱的第二端连接至所述第一公共源区,

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所述多个第二沟道柱的第二端连接于所述第二公共源区。

9.根据权利要求8所述的3D存储器件，还包括：

第二导电通道，从所述第二阵列结构的表面到达所述第一公共源区；以及

第三导电通道，从所述第二阵列结构的表面到达所述第二公共源区。

10.根据权利要求1所述的3D存储器件，还包括：栅线缝隙，用于将所述第一栅叠层结构和所述第二栅叠层结构中的栅极导电层分割成多条栅线。

11.根据权利要求10所述的3D存储器件，还包括：位于所述栅线缝隙中的导电通道。

12.根据权利要求1所述的3D存储器件，其中，所述第一栅叠层结构中的多个栅极导体与所述多个第一沟道柱形成多个第一晶体管，所述第二栅叠层结构中的多个栅极导体与所述多个第二沟道柱形成多个第二晶体管，所述多个第一晶体管和所述多个第二晶体管的堆叠顺序相反。

13.根据权利要求1所述的3D存储器件，其中，所述互连结构还包括：

第三绝缘层，所述多条位线形成在所述第三绝缘层中；以及

第三导电通道，所述第三导电通道穿过所述第三绝缘层，使得所述多条位线经由所述第三导电通道连接至所述多个第一沟道柱和所述多个第二沟道柱中的至少一个沟道柱。

14.根据权利要求1所述的3D存储器件，其中，所述多个第一沟道柱分别与所述多个第二沟道柱中的相应一个对准。

15.一种制造3D存储器件的方法，包括：

形成第一阵列结构，所述第一阵列结构包括半导体衬底、位于所述半导体衬底上方的第一栅叠层结构、以及贯穿所述第一栅叠层结构的多个第一沟道柱；

形成互连结构；

形成第二阵列结构，所述第二阵列结构和所述第一阵列结构将所述互连结构夹在二者之间，所述第二阵列结构包括位于所述第一栅叠层结构上方的第二栅叠层结构、位于所述第二栅叠层结构上方的半导体层、以及贯穿所述第二栅叠层结构的多个第二沟道柱，

其中，所述互连结构包括多条位线，所述多个第一沟道柱分别与所述多个第二沟道柱中的相应一个共同连接至所述多条位线中的相应一条位线。

16.根据权利要求15所述的方法，其中，形成第一阵列结构的步骤包括：

在所述半导体衬底上形成第一绝缘叠层结构，所述第一绝缘叠层结构包括交替堆叠的多个牺牲层和多个层间绝缘层；

将所述多个牺牲层图案化为台阶状；

将所述多个牺牲层置换成多个栅极导体，从而形成所述第一栅叠层结构。

17.根据权利要求16所述的方法，其中，形成第二阵列结构的步骤包括：

在所述互连结构上形成第二绝缘叠层结构，所述第二绝缘叠层结构包括交替堆叠的多个牺牲层和多个层间绝缘层；

将所述多个牺牲层图案化为台阶状；

将所述多个牺牲层置换成多个栅极导体，从而形成所述第二栅叠层结构；以及

在所述第二栅叠层结构上形成所述半导体层。

18.根据权利要求17所述的方法，还包括：

在所述半导体衬底中形成CMOS电路；

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形成第一绝缘层，所述第一绝缘层围绕所述第一绝缘叠层结构和所述第二绝缘叠层结构的一部分，从而形成绝缘区域；以及

在所述绝缘区域的内部形成第一导电通道，所述第一导电通道从所述半导体衬底向上延伸，依次贯穿所述第一绝缘叠层结构、所述第二绝缘叠层结构，到达所述第二阵列结构的顶部，

其中，所述第一导电通道提供所述CMOS电路与外部电路之间的电连接。

19.根据权利要求18所述的方法，其中，所述第一导电通道包括多个导电柱组成的阵列。

20.根据权利要求18所述的方法，还包括：

在所述半导体衬底中形成第一公共源区；

在所述半导体衬底中形成与所述第一公共源区邻接的第一高压阱区，所述第一公共源区与所述第一高压阱区的掺杂类型相反；

在所述半导体层中形成第二公共源区；以及

在所述半导体层中形成与所述第二公共源区邻接的第二高压阱区，所述第二公共源区与所述第二高压阱区的掺杂类型相反；

其中，所述多个第一沟道柱的第一端分别接触所述多条位线中的相应一条位线，所述多个第二沟道柱的第一端分别接触所述多条位线中的相应一条位线，

所述多个第一沟道柱的第二端连接至所述第一公共源区，

所述多个第二沟道柱的第二端连接于所述第二公共源区。

21.根据权利要求20所述的方法，还包括：

形成第二导电通道，从所述第二阵列结构的表面到达所述第一公共源区；以及

形成第三导电通道，从所述第二阵列结构的表面到达所述第二公共源区。

22.根据权利要求15所述的方法，还包括：

形成栅线缝隙，用于将所述第一栅叠层结构和所述第二栅叠层结构中的栅极导电层分割成多条栅线。

23.根据权利要求22所述的方法，还包括：在所述栅线缝隙中形成导电通道。

24.根据权利要求15所述的方法，其中，形成互连结构的步骤包括：

在所述第一阵列结构上形成第三绝缘层；

在所述第三绝缘层中形成第三导电通道；以及

在所述第三绝缘层中形成所述多条位线，

其中，所述多条位线经由所述第三导电通道连接至所述多个第一沟道柱和所述多个第二沟道柱中的至少一个沟道柱。

25.根据权利要求15所述的方法，在形成所述第一阵列结构和所述第二阵列结构的步骤中，将所述多个第一沟道柱分别与所述多个第二沟道柱中的相应一个对准。

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3D存储器件及其制造方法

技术领域

[0001] 本发明涉及存储器技术，更具体地，涉及3D存储器件及其制造方法。

背景技术

[0002] 存储器件的存储密度的提高与半导体制造工艺的进步密切相关。随着半导体制造工艺的特征尺寸越来越小，存储器件的存储密度越来越高。为了进一步提高存储密度，已经开发出三维结构的存储器件(即，3D存储器件)。3D存储器件包括沿着垂直方向堆叠的多个存储单元，在单位面积的晶片上可以成倍地提高集成度，并且可以降低成本。

[0003] 现有的3D存储器件主要用作非易失性的闪存。两种主要的非易失性闪存技术分别采用NAND和NOR结构。与NOR存储器件相比，NAND存储器件中的读取速度稍慢，但写入速度快，擦除操作简单，并且可以实现更小的存储单元，从而达到更高的存储密度。因此，采用NAND结构的3D存储器件获得了广泛的应用。

[0004] 在NAND结构的3D存储器件中，可以堆叠多个层面的阵列结构以提高存储密度。例如，对于128个层面的存储单元，可以采用两个阵列结构堆叠而成，每个阵列结构包括多个(例如32或64个)层面的存储单元串，两个阵列结构的存储单元串彼此互连。每个阵列结构包括叠层结构和贯穿叠层结构的沟道柱，采用叠层结构提供选择晶体管和存储晶体管的栅极导体，采用沟道柱提供选择晶体管和存储晶体管的沟道层和栅介质叠层，以及采用贯穿叠层结构的导电通道实现存储单元串的互连。叠层结构中的栅极导体与导电通道彼此距离接近，二者之间由绝缘层隔开。

[0005] 期望进一步改进3D存储器件的结构及其制造方法，不仅提高3D存储器件的存储密度，而且进一步简化制造工艺，降低制造成本，提高良率和可靠性。

发明内容

[0006] 本发明的目的是提供一种改进的3D存储器件及其制造方法，其中，在互连结构中形成位线，使得位线兼作为不同层面的阵列结构之间的互连，从而可以简化制造工艺和减小3D存储器件的尺寸。

[0007] 根据本发明的第一方面，提供一种3D存储器件，包括:第一阵列结构，所述第一阵列结构包括半导体衬底、位于所述半导体衬底上方的第一栅叠层结构、以及贯穿所述第一栅叠层结构的多个第一沟道柱;第二阵列结构，堆叠在所述第一阵列结构上方，所述第二阵列结构包括位于所述第一栅叠层结构上方的第二栅叠层结构、位于所述第二栅叠层结构上方的半导体层、以及贯穿所述第二栅叠层结构的多个第二沟道柱;以及互连结构，位于所述第一阵列结构和所述第二阵列结构之间，其中，所述互连结构包括多条位线，所述多个第一沟道柱分别与所述多个第二沟道柱中的相应一个共同连接至所述多条位线中的相应一条位线。

[0008] 优选地，所述第一栅叠层结构和所述第二栅叠层结构分别包括交替堆叠的多个栅极导体和多个层间绝缘层，并且所述多个栅极导体图案化为台阶状，从而形成台阶区域，在

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所述台阶区域提供字线的电连接区。

[0009] 优选地，在所述第一阵列结构中，所述多个第一沟道柱位于所述第一栅叠层结构的中间区域，在所述第二阵列结构中，所述多个第二沟道位于所述第二栅叠层结构的中间区域。

[0010] 优选地，所述第一阵列结构还包括位于所述台阶区域的多个第一伪沟道柱，所述多个第一伪沟道柱贯穿所述第一栅叠层结构中的一部分栅极导体且未连接至所述多条位线，所述第二阵列结构还包括位于所述台阶区域的多个第二伪沟道柱，所述多个第二伪沟道柱贯穿所述第二栅叠层结构中的一部分栅极导体且未连接至所述多条位线。

[0011] 优选地，还包括：位于所述半导体衬底中的CMOS电路。

[0012] 优选地，还包括：第一绝缘层，用于围绕绝缘区域，所述第一栅叠层结构和所述第二栅叠层结构位于所述绝缘区域的外部；第一绝缘叠层结构和第二绝缘叠层结构，位于所述绝缘区域的内部，并且分别与所述第一栅叠层结构和所述第二栅叠层结构相对应；以及第一导电通道，位于所述绝缘区域的内部，从所述半导体衬底向上延伸，依次贯穿所述第一绝缘叠层结构、所述第二绝缘叠层结构，到达所述第二阵列结构的顶部，其中，所述第一导电通道提供所述CMOS电路与外部电路之间的电连接。

[0013] 优选地，所述第一导电通道包括多个导电柱组成的阵列。

[0014] 优选地，还包括：第一公共源区，形成在所述半导体衬底中；第一高压阱区，与所述第一公共源区邻接并且掺杂类型相反；第二公共源区，形成在所述半导体层中；以及第二高压阱区，与所述第二公共源区邻接并且掺杂类型相反，其中，所述多个第一沟道柱的第一端分别接触所述多条位线中的相应一条位线，所述多个第二沟道柱的第一端分别接触所述多条位线中的相应一条位线，所述多个第一沟道柱的第二端连接至所述第一公共源区，所述多个第二沟道柱的第二端连接于所述第二公共源区。

[0015] 优选地，还包括：第二导电通道，从所述第二阵列结构的表面到达所述第一公共源区；以及第三导电通道，从所述第二阵列结构的表面到达所述第二公共源区。

[0016] 优选地，还包括：栅线缝隙，用于将所述第一栅叠层结构和所述第二栅叠层结构中的栅极导电层分割成多条栅线。

[0017] 优选地，还包括：位于所述栅线缝隙中的导电通道。

[0018] 优选地，所述第一栅叠层结构中的多个栅极导体与所述多个第一沟道柱形成多个第一晶体管，所述第二栅叠层结构中的多个栅极导体与所述多个第二沟道柱形成多个第二晶体管，所述多个第一晶体管和所述多个第二晶体管的堆叠顺序相反。

[0019] 优选地，所述互连结构还包括：第三绝缘层，所述多条位线形成在所述第三绝缘层中；以及第三导电通道，所述第三导电通道穿过所述第三绝缘层，使得所述多条位线经由所述第三导电通道连接至所述多个第一沟道柱和所述多个第二沟道柱中的至少一个沟道柱。

[0020] 优选地，所述多个第一沟道柱分别与所述多个第二沟道柱中的相应一个对准。

[0021] 根据本发明的第二方面，提供一种制造3D存储器件的方法，包括：形成第一阵列结构，所述第一阵列结构包括半导体衬底、位于所述半导体衬底上方的第一栅叠层结构、以及贯穿所述第一栅叠层结构的多个第一沟道柱；形成互连结构；形成第二阵列结构，所述第二阵列结构和所述第一阵列结构将所述互连结构夹在二者之间，所述第二阵列结构包括位于所述第一栅叠层结构上方的第二栅叠层结构、位于所述第二栅叠层结构上方的半导体层、

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以及贯穿所述第二栅叠层结构的多个第二沟道柱，其中，所述互连结构包括多条位线，所述多个第一沟道柱分别与所述多个第二沟道柱中的相应一个共同连接至所述多条位线中的相应一条位线。

[0022] 优选地，形成第一阵列结构的步骤包括：在所述半导体衬底上形成第一绝缘叠层结构，所述第一绝缘叠层结构包括交替堆叠的多个牺牲层和多个层间绝缘层；将所述多个牺牲层图案化为台阶状；将所述多个牺牲层置换成多个栅极导体，从而形成所述第一栅叠层结构。

[0023] 优选地，形成第二阵列结构的步骤包括：在所述互连结构上形成第二绝缘叠层结构，所述第二绝缘叠层结构包括交替堆叠的多个牺牲层和多个层间绝缘层；将所述多个牺牲层图案化为台阶状；将所述多个牺牲层置换成多个栅极导体，从而形成所述第二栅叠层结构；以及在所述第二栅叠层结构上形成所述半导体层。

[0024] 优选地，还包括：在所述半导体衬底中形成CMOS电路；形成第一绝缘层，所述第一绝缘层围绕所述第一绝缘叠层结构和所述第二绝缘叠层结构的一部分，从而形成绝缘区域；以及在所述绝缘区域的内部形成第一导电通道，所述第一导电通道从所述半导体衬底向上延伸，依次贯穿所述第一绝缘叠层结构、所述第二绝缘叠层结构，到达所述第二阵列结构的顶部，其中，所述第一导电通道提供所述CMOS电路与外部电路之间的电连接。

[0025] 优选地，所述第一导电通道包括多个导电柱组成的阵列。

[0026] 优选地，还包括：在所述半导体衬底中形成第一公共源区；在所述半导体衬底中形成与所述第一公共源区邻接的第一高压阱区，所述第一公共源区与所述第一高压阱区的掺杂类型相反；在所述半导体层中形成第二公共源区；以及在所述半导体层中形成与所述第二公共源区邻接的第二高压阱区，所述第二公共源区与所述第二高压阱区的掺杂类型相反；其中，所述多个第一沟道柱的第一端分别接触所述多条位线中的相应一条位线，所述多个第二沟道柱的第一端分别接触所述多条位线中的相应一条位线，所述多个第一沟道柱的第二端连接至所述第一公共源区，所述多个第二沟道柱的第二端连接于所述第二公共源区。

[0027] 优选地，还包括：形成第二导电通道，从所述第二阵列结构的表面到达所述第一公共源区；以及形成第三导电通道，从所述第二阵列结构的表面到达所述第二公共源区。

[0028] 优选地，还包括：形成栅线缝隙，用于将所述第一栅叠层结构和所述第二栅叠层结构中的栅极导电层分割成多条栅线。

[0029] 优选地，还包括：在所述栅线缝隙中形成导电通道。

[0030] 优选地，形成互连结构的步骤包括：在所述第一阵列结构上形成第三绝缘层；在所述第三绝缘层中形成第三导电通道；以及在所述第三绝缘层中形成所述多条位线，其中，所述多条位线经由所述第三导电通道连接至所述多个第一沟道柱和所述多个第二沟道柱中的至少一个沟道柱。

[0031] 优选地，在形成所述第一阵列结构和所述第二阵列结构的步骤中，将所述多个第一沟道柱分别与所述多个第二沟道柱中的相应一个对准。

[0032] 根据本发明实施例的3D存储器件及其制造方法，互连结构位于所述第一阵列结构和所述第二阵列结构之间，并且互连结构包括多条位线。所述多条位线兼作为不同层面的阵列结构之间的互连，该位线可以提供第一阵列结构和第二阵列结构之间的对准标记，并

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且该位线有较大的表面积，从而允许第一阵列结构和第二阵列结构中的沟道柱的对准容差。

[0033] 与现有技术不同，本发明实施例的3D存储器采用位线兼作互连结构中的导电通道，以实现第一阵列结构和第二阵列结构中的沟道柱之间的互连，不仅可以减小3D存储器件的尺寸，而且可以简化制造工艺，降低3D存储器件的制造成本。

[0034] 进一步地，采用位线作为互连结构，可以获得更大的导电路径截面积，以及减少互连结构中的缺陷数量，从而减小互连电阻，提高3D存储器件的性能。

附图说明

[0035] 通过以下参照附图对本发明实施例的描述，本发明的上述以及其他目的、特征和优点将更为清楚。

[0036] 图1a和1b分别示出3D存储器件的存储单元串的等效电路图和结构示意图。

[0037] 图2示出根据本发明实施例的3D存储器件的透视图。

[0038] 图3示出根据本发明实施例的3D存储器件的等效电路图。

[0039] 图4a至4i示出根据本发明实施例的3D存储器件制造方法的各个阶段的截面图。

具体实施方式

[0040] 以下将参照附图更详细地描述本发明。在各个附图中，相同的元件采用类似的附图标记来表示。为了清楚起见，附图中的各个部分没有按比例绘制。此外，可能未示出某些公知的部分。为了简明起见，可以在一幅图中描述经过数个步骤后获得的半导体结构。

[0041] 应当理解，在描述器件的结构时，当将一层、一个区域称为位于另一层、另一个区域“上面”或“上方”时，可以指直接位于另一层、另一个区域上面，或者在其与另一层、另一个区域之间还包含其它的层或区域。并且，如果将器件翻转，该一层、一个区域将位于另一层、另一个区域“下面”或“下方”。

[0042] 如果为了描述直接位于另一层、另一个区域上面的情形，本文将采用“直接在……上面”或“在……上面并与之邻接”的表述方式。

[0043] 在本申请中，术语“半导体结构”指在制造存储器件的各个步骤中形成的整个半导体结构的统称，包括已经形成的所有层或区域。在下文中描述了本发明的许多特定的细节，例如器件的结构、材料、尺寸、处理工艺和技术，以便更清楚地理解本发明。但正如本领域的技术人员能够理解的那样，可以不按照这些特定的细节来实现本发明。

[0044] 在理想的工艺中，采用单蚀刻步骤形成贯穿叠层结构的沟道柱和导电通道。对于小尺寸的沟道柱而言，进一步的特征尺寸(CD)缩小和形状优化是提高存储密度的关键。然而，由于干法蚀刻的工艺限制，实际上难以采用单蚀刻步骤形成贯穿叠层结构的沟道孔。为了克服该工艺限制，已经提出分别制造多个阵列结构，以及将多个阵列结构堆叠成3D存储器件的方法。在该3D存储器件中，多个阵列结构之间设置有互连结构。

[0045] 本申请的发明人发现，多个阵列结构之间的互连容易俘获缺陷，从而形成高阻互连，此外，多个阵列结构与互连之间的对准困难，从而影响产品良率。因此，期待进一步改进阵列结构的互连结构以减小3D存储器件的尺寸和提高产品良率。

[0046] 本发明可以各种形式呈现，以下将描述其中一些示例。

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[0047] 图1a和1b分别示出3D存储器件的存储单元串的电路图和结构示意图。在该实施例中示出的存储单元串包括4个存储单元的情形。可以理解，本发明不限于此，存储单元串中的存储单元数量可以为任意多个，例如，32个或64个。

[0048] 如图1a所示，存储单元串100的第一端连接至位线BL，第二端连接至源极线SL。存储单元串100包括在第一端和第二端之间串联连接的多个晶体管，包括：第一选择晶体管Q1、存储晶体管M1至M4、以及第二选择晶体管Q2。第一选择晶体管Q1的栅极连接至第一选择线SSL，第二选择晶体管Q2的栅极连接至第二选择线GSL。存储晶体管M1至M4的栅极分别连接至字线WL1至WL4中的相应字线。

[0049] 如图1b所示，存储单元串100的第一选择晶体管Q1和第二选择晶体管Q2分别包括栅极导体109b和109c，存储晶体管M1至M4分别包括栅极导体109a。栅极导体109a、109b和109c与存储单元串100中的晶体管的堆叠顺序一致，相邻的栅极导体之间彼此采用层间绝缘层隔开，从而形成栅叠层结构。进一步地，存储单元串100包括沟道柱110。沟道柱110与栅叠层结构相邻或者贯穿栅叠层结构。在沟道柱110的中间部分，栅极导体109a与沟道层111之间夹有隧穿介质层112、电荷存储层113和阻挡介质层114，从而形成存储晶体管M1至M4。在沟道柱110的两端，栅极导体109b和109c与沟道层111之间夹有阻挡介质层114，从而形成第一选择晶体管Q1和第二选择晶体管Q2。

[0050] 在该实施例中，沟道层111例如由掺杂多晶硅组成，隧穿介质层112和阻挡介质层114分别由氧化物组成，例如氧化硅，电荷存储层113由包含量子点或者纳米晶体的绝缘层组成，例如包含金属或者半导体的微粒的氮化硅及氮氧化硅，栅极导体109a、109b和109c由金属组成，例如钨。沟道层111用于提供选择晶体管和存储晶体管的沟道区，沟道层111的掺杂类型与选择晶体管和存储晶体管的类型相同。例如，对于N型的选择晶体管和存储晶体管，沟道层111可以是N型掺杂的多晶硅。

[0051] 在该实施例中，沟道柱110的芯部为沟道层111，隧穿介质层112、电荷存储层113和阻挡介质层114形成围绕芯部侧壁的叠层结构。在替代的实施例中，沟道柱110的芯部为附加的绝缘层，沟道层111、隧穿介质层112、电荷存储层113和阻挡介质层114形成围绕芯部的叠层结构。

[0052] 在该实施例中，第一选择晶体管Q1和第二选择晶体管Q2、存储晶体管M1至M4使用公共的沟道层111和阻挡介质层114。在沟道柱110中，沟道层111提供多个晶体管的源漏区和沟道层。在替代的实施例中，可以采用彼此独立的步骤，分别形成第一选择晶体管Q1和第二选择晶体管Q2的半导体层和阻挡介质层以及存储晶体管M1至M4的半导体层和阻挡介质层。在沟道柱110中，第一选择晶体管Q1和第二选择晶体管Q2的半导体层与存储晶体管M1至M4的半导体层彼此电连接。

[0053] 在写入操作中，存储单元串100利用FN隧穿效率将数据写入存储晶体管M1至M4中的选定存储晶体管。以存储晶体管M2为例，在源极线SL接地的同时，第二控制栅选择线(Gate Selective Line)GSL偏置到大约零伏电压，使得对应于第二控制栅选择线GSL的选择晶体管Q2断开，第一源级选择线(Source Selective Line)SSL偏置到高电压VDD，使得对应于第一选择线SSL的选择晶体管Q1导通。进一步地，位线BIT2接地，字线WL2偏置于编程电压VPG，例如20V左右，其余字线偏置于低电压VPS1。由于只有选定存储晶体管M2的字线电压高于隧穿电压，因此，该存储晶体管M2的沟道区的电子，经由隧穿介质层112到达电荷存储

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层113，从而将数据转变成电荷存储于存储晶体管M2的电荷存储层113中。

[0054] 在读取操作中，存储单元串100根据存储晶体管M1至M4中的选定存储晶体管的导通状态判断电荷存储层中的电荷量，从而获得该电荷量表征的数据。以存储晶体管M2为例，字线WL2偏置于读取电压VRD，其余字线偏置于高电压VPS2。存储晶体管M2的导通状态与其阈值电压相关，即与电荷存储层中的电荷量相关，从而根据存储晶体管M2的导通状态可以判断数据值。存储晶体管M1、M3和M4始终处于导通状态，因此，存储单元串100的导通状态取决于存储晶体管M2的导通状态。控制电路根据位线BL和源极线SL上检测的电信号判断存储晶体管M2的导通状态，从而获得存储晶体管M2中存储的数据。

[0055] 图2示出根据本发明实施例的3D存储器件的透视图。为了清楚起见，在图2中未示出3D存储器件中的各个绝缘层。

[0056] 在该实施例中示出的3D存储器件200包括堆叠的第一阵列结构和第二阵列结构。每个阵列结构包括3*3共计9个存储单元串100，每个存储单元串100包括4个存储单元，从而分别形成3*3*4共计36个存储单元的存储器阵列。3D存储器件200中的第一阵列结构和第二阵列结构共计形成72个存储单元。可以理解，本发明不限于此，3D存储器件可以包括任意多个存储单元串，例如，1024个，每个存储单元串中的存储单元数量可以为任意多个，例如，32个或64个。

[0057] 以3D存储器件200中的第一阵列结构为例，在半导体衬底101上形成第一栅叠层结构和贯穿所述第一栅叠层结构的多个沟道柱110。优选地，在第一栅叠层结构中，相邻的栅极导体109之间彼此采用层间绝缘层隔开。在图中未示出层间绝缘层。沟道柱110的内部结构如图1b所示，在此不再进行详细说明。

[0058] 第一阵列结构中的存储单元串分别包括各自的沟道柱110，以及公共的栅极导体109。栅极导体109与存储单元串100中的晶体管的堆叠顺序一致。在沟道柱110的中间部分，栅极导体109与沟道柱110内部的沟道层111、隧穿介质层112、电荷存储层113和阻挡介质层114一起，形成存储晶体管M1至M4。在沟道柱110的两端，栅极导体109与沟道柱110内部的沟道层111和阻挡介质层114一起，形成第一选择晶体管Q1和第二选择晶体管Q2。

[0059] 第二阵列结构包括半导体层201以及在半导体层201下方形成的第二栅叠层结构。第二阵列结构与第一阵列结构基本相同，但是在垂直方向上晶体管的堆叠顺序与第一阵列结构相反。在第一阵列结构中，第一栅叠层结构位于半导体衬底101的上方。在第二阵列结构中，第二栅叠层结构位于半导体层201的下方。在半导体层201上形成第二栅叠层结构和贯穿所述栅叠层结构的多个沟道柱210。优选地，在第二栅叠层结构中，相邻的栅极导体209之间彼此采用层间绝缘层隔开。

[0060] 互连结构位于第一阵列结构和第二阵列结构之间。互连结构包括多条位线302。第一阵列结构和第二阵列结构共用多条位线302。如图所示，第一阵列结构中的沟道柱110从半导体衬底101向上延伸至相应的位线302，第二阵列结构中的沟道柱210从半导体层201向下延伸至相应的位线302。

[0061] 在该实施例中，第一阵列结构中的沟道柱110和第二阵列结构中的沟道柱210分别排列成阵列，不仅贯穿各自的栅叠层结构，而且第一阵列结构中的沟道柱110的第一端和第二阵列结构中的相应沟道柱210的第一端连接至互连层中的公共位线302。进一步地，第一阵列结构中的沟道柱110的第二端共同连接至半导体衬底101，形成共源极连接，第二阵列

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结构中的沟道柱210的第二端共同连接至半导体层201，形成共源极连接。

[0062] 第一阵列结构还可以包括伪沟道柱140，第二阵列结构还可以包括伪沟道柱240。伪沟道柱140和240与沟道柱110和210的内部结构可以相同，并且至少穿过栅叠层结构中的至少一部分栅极导体。然而，伪沟道柱140和240并未与位线302相连接，从而仅仅提供机械支撑作用，而没有用于形成选择晶体管和存储晶体管。因此，伪沟道柱140和240也没有形成有效的存储单元。

[0063] 第一阵列结构和第二阵列结构中的第一选择晶体管的栅极导体由栅线缝隙151(gate line slit)分割成不同的栅线。同一行的多个第一选择晶体管的栅极导体共同连接至同一条第一选择线。

[0064] 第一阵列结构和第二阵列结构中的存储晶体管的栅极导体分别连接至各自的字线。如果存储晶体管的栅极导体由栅线缝隙151分割成不同的栅线，则同一层面的的存储晶体管的栅极导体经由相应的导电通道到达互连层，从而彼此互连，然后经由导电通道连接至同一条字线(即字线WL1至WL4之一)。

[0065] 第一阵列结构和第二阵列结构中的第二选择晶体管的栅极导体连接至各自的第二选择线。如果第二选择晶体管的栅极导体由栅线缝隙151分割成不同的栅线，则多个第二选择晶体管的栅极导体经由相应的导电通道到达互连层，从而彼此互连，然后经由导电通道连接至同一条第二选择线。

[0066] 优选地，在第一阵列结构的衬底半导体衬底101中例如包括CMOS电路。采用导电通道提供CMOS电路与外部电路之间的电连接。

[0067] 第一阵列结构和第二阵列结构包括由隔离层121围绕的绝缘区域，在该区域中，与栅叠层结构不同，该部分仍然保留着绝缘叠层结构，其中，多个牺牲层和多个层间绝缘层交替堆叠。在绝缘区域中，导电通道123例如是多个导电柱组成的阵列，分别从第一阵列结构的半导体衬底101向上延伸，依次贯穿第一阵列结构的绝缘叠层结构、第二阵列结构的绝缘叠层结构、第二阵列结构的半导体层201，到达第二阵列结构的顶部。

[0068] 在该实施例中，该3D存储器件中的位线302位于第一阵列结构和第二阵列结构之间，位线兼作为不同层面的阵列结构之间的互连，从而可以简化制造工艺和减小3D存储器件的尺寸。此外，第二阵列结构中的沟道柱210可以直接形成在位线302的表面上。第二阵列结构中的沟道柱210与多个位线302对准，由于多个位线302的表面尺寸较大并且排列成图案，因此，采用位线作为互连可以便于对准和提高良率。

[0069] 图3示出根据本发明实施例的3D存储器件的等效电路图。该等效电路图示出3D存储器件的一个存储单元串300。

[0070] 参见图2，可以理解，该存储单元串300包括第一阵列结构中的一个沟道柱110和第二阵列结构中的相应一个沟道柱210，以及相邻的栅叠层结构。

[0071] 如图3所示，存储单元串300包括连接至公共的位线BL的第一子串和第二子串。进一步地，第一子串连接在位线BL和源极线SL1之间，第二子串连接在位线BL和源极线SL2之间。第一子串包括在第一阵列结构中形成的多个晶体管，包括在位线BL和源极线SL1之间依次串联连接的第一选择晶体管Q11、存储晶体管M11至M14、第二选择晶体管Q12。第二子串包括在第二阵列结构中形成的多个晶体管，包括在位线BL和源极线SL2之间依次串联连接的第一选择晶体管Q21、存储晶体管M21至M24、第二选择晶体管Q22。由于第一子串和第二子串

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均连接至公共的位线BL，因此，第一子串和第二子串中的多个晶体管的堆叠顺序相反。

[0072] 在第一子串中，第一选择晶体管Q11的栅极连接至第一选择线SSL1，第二选择晶体管Q12的栅极连接至第二选择线GSL1。存储晶体管M11至M14的栅极分别连接至字线WL11至WL14中的相应字线。在第二子串中，第一选择晶体管Q21的栅极连接至第一选择线SSL2，第二选择晶体管Q22的栅极连接至第二选择线GSL2。存储晶体管M21至M24的栅极分别连接至字线WL21至WL24中的相应字线。

[0073] 图4a至4i示出根据本发明实施例的3D存储器件制造方法的各个阶段的截面图。所述截面图沿着图2中的AA线截取。

[0074] 该方法开始于已经在半导体衬底101上形成绝缘叠层结构的第一阵列结构L01，如图4a所示。

[0075] 第一阵列结构L01包括半导体衬底101及其上的绝缘叠层结构。该绝缘叠层结构包括交替堆叠的多个层间绝缘层108和多个牺牲层122。在该实施例中，半导体衬底101例如是单晶硅衬底，层间绝缘层108例如由氧化硅组成，牺牲层122例如由氮化硅组成。

[0076] 如下文所述，牺牲层122将替换成栅极导体，栅极导体进一步连接至字线。为了形成从栅极导体到达字线的导电通道，多个牺牲层122例如图案化为台阶状，即，每个牺牲层122的边缘部分相对于上方的牺牲层暴露以提供电连接区。在多个牺牲层122的图案化步骤之后，可以采用绝缘层覆盖绝缘叠层结构。在图4a中将多个牺牲层122之间的层间绝缘层108和覆盖绝缘叠层结构的层间绝缘层整体示出。然而，本发明不限于此，可以采用多个独立的沉积步骤形成多个牺牲层122之间及其上方的层间绝缘层。

[0077] 为了便于对3D存储器件中的存储单元进行编程操作，在半导体衬底101中形成多个阱区以及用于驱动选择晶体管和存储晶体管的CMOS电路(未示出)。所述多个阱区例如包括深N阱102、位于深N阱102中的高压P阱103、与高压P阱103相邻接的高压N阱105、位于高压P阱103中的P+掺杂区104、位于高压N阱105中的N+掺杂区106。在该实施例中，高压P阱103作为沟道柱的公共源区，高压N阱105用于对公共源区的预充电，P+掺杂区104和N+掺杂区106分别作为接触区以减小接触电阻。该高压P阱103作为多个沟道柱的公共源区，因此位于绝缘叠层结构的下方。

[0078] 进一步地，在第一阵列结构L01与绝缘叠层结构的中间区域(core region)对应的第一区域A01中，形成贯穿绝缘叠层结构的沟道柱110，在绝缘叠层结构的台阶区域(stair-step region)对应的第二区域A02中，形成贯穿绝缘叠层结构的伪沟道柱140，如图4b所示。

[0079] 沟道柱110的下部包括半导体层116。进一步地，沟道柱110包括从其上部延伸至半导体层116的沟道层111。如图所示，在沟道柱110的中间部分，沟道柱110包括依次堆叠在沟道层111上的隧穿介质层112、电荷存储层113和阻挡介质层114，在沟道柱110的两端，沟道柱110包括堆叠在沟道层111或半导体层116上的阻挡介质层114。沟道柱110的下端与半导体衬底101中的高压P阱103相接触。在最终的3D存储器件中，沟道柱110的上端与位线相连接，从而形成有效的存储单元。

[0080] 伪沟道柱140与沟道柱110的内部结构可以相同或不同，并且至少穿过栅叠层结构中的至少一部分栅极导体。在最终的3D存储器件中，伪沟道柱140并未与位线相连接，从而仅仅提供机械支撑作用，而没有用于形成选择晶体管和存储晶体管。因此，伪沟道柱140没有形成有效的存储单元。

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[0081] 在该实施例中，沟道柱110还包括作为芯部的绝缘层115，沟道层111、隧穿介质层112、电荷存储层113和阻挡介质层114形成围绕芯部的叠层结构。在替代的实施例中，沟道柱110中可以省去绝缘层115。

[0082] 进一步地，在第一阵列结构L01上形成互连结构L03，如图4c所示。

[0083] 该互连结构L03包括层间绝缘层301、位于层间绝缘层301中的多条位线302，以及连接位线302与相应的沟道柱110中的沟道层111的导电通道303。所述多条位线302沿着第一方向(即垂直于纸面的方向)延伸，从而分别将多个沟道柱110的上端连接在一起。在该实施例中，层间绝缘层301例如由氧化硅组成，位线302和导电通道303例如由Ti/TiN或W组成。

[0084] 进一步地，在互连结构L03上形成第二阵列结构L02，如图4d所示。

[0085] 第二阵列结构L02包括绝缘叠层结构。该绝缘叠层结构包括交替堆叠的多个层间绝缘层208和多个牺牲层222。在该实施例中，层间绝缘层208例如由氧化硅组成，牺牲层222例如由氮化硅组成。

[0086] 如下文所述，牺牲层222将替换成栅极导体，栅极导体进一步连接至字线。为了形成从栅极导体到达字线的导电通道，多个牺牲层222例如图案化为台阶状，即，每个牺牲层222的边缘部分相对于上方的牺牲层暴露以提供电连接区。在多个牺牲层222的图案化步骤之后，可以采用绝缘层覆盖绝缘叠层结构。在图4d中将多个牺牲层222之间的层间绝缘层208和覆盖绝缘叠层结构的层间绝缘层整体示出。然而，本发明不限于此，可以采用多个独立的沉积步骤形成多个牺牲层222之间及其上方的层间绝缘层。

[0087] 进一步地，在第二阵列结构L02与绝缘叠层结构的中间区域(core region)对应的第一区域A01中，形成贯穿绝缘叠层结构的沟道柱210，在绝缘叠层结构的台阶区域(stair-step region)对应的第二区域A02中，形成贯穿绝缘叠层结构的伪沟道柱240，如图4e所示。

[0088] 第二阵列结构L02中的沟道柱210与第一阵列结构L01中的沟道柱110大致对准，二者的内部结构相同，但在垂直方向上沿着相反的方向延伸，从而在后续步骤中与栅极导体一起形成在垂直方向上沿着相反的方向堆叠的多个晶体管。第一阵列结构L01中的沟道柱110的第一端和第二阵列结构L02中的相应沟道柱210的第一端连接至互连层中的公共位线302。为了简明起见，在此不再详述沟道柱110和210的内部结构。

[0089] 伪沟道柱240与沟道柱210的内部结构可以相同或不同，并且至少穿过栅叠层结构中的至少一部分栅极导体。伪沟道柱240并未与位线相连接，从而仅仅提供机械支撑作用，而没有用于形成选择晶体管和存储晶体管。因此，伪沟道柱240没有形成有效的存储单元。

[0090] 进一步地，在第一阵列结构L01和第二阵列结构L02中形成隔离层121，如图4f所示。

[0091] 隔离层121从第一阵列结构L01的半导体衬底101向上延伸，依次贯穿第一阵列结构L01的绝缘叠层结构、第二阵列结构L02的绝缘叠层结构，到达第二阵列结构的顶部。在垂直于堆叠方向的平面上观察，隔离层121围绕绝缘叠层结构的一部分区域，形成绝缘区域A03。在该实施例中，隔离层121例如由氧化硅组成。

[0092] 进一步地，在第一阵列结构L01和第二阵列结构L02的绝缘叠层结构中形成栅线缝隙151(参见图2)，经由栅线缝隙151去除绝缘区域A03外部的绝缘叠层中的牺牲层122和222以形成空腔，以及采用金属层填充空腔以形成栅极导体109和209，如图4g所示。

[0093] 在形成栅线缝隙151时，可以采用各向异性蚀刻，例如采用干法蚀刻，如离子铣蚀

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刻、等离子蚀刻、反应离子蚀刻、激光烧蚀。例如，通过控制蚀刻时间，使得蚀刻在半导体衬底101的表面附近停止。

[0094] 在该实施例中，栅线缝隙151将栅极导体分割成多条栅线。为此，栅线缝隙151贯穿第一阵列结构L01和第二阵列结构L02的绝缘叠层结构。

[0095] 在形成空腔时，利用栅线缝隙151作为蚀刻剂通道，采用各向同性蚀刻去除绝缘叠层结构中的牺牲层122和222从而形成空腔。各向同性蚀刻可以采用选择性的湿法蚀刻或气相蚀刻。在湿法蚀刻中使用蚀刻溶液作为蚀刻剂，其中，将半导体结构浸没在蚀刻溶液中。在气相蚀刻中使用蚀刻气体作为蚀刻剂，其中，将半导体结构暴露于蚀刻气体中。

[0096] 在绝缘叠层结构中的层间绝缘层和牺牲层分别由氧化硅和氮化硅组成的情形下，在湿法蚀刻中可以采用磷酸溶液作为蚀刻剂，在气相蚀刻中可以采用C4F8、C4F6、CH2F2和O2中的一种或多种。在蚀刻步骤中，蚀刻剂充满栅线缝隙151。绝缘叠层结构中的牺牲层的端部暴露于栅线缝隙151的开口中，因此，牺牲层接触到蚀刻剂。蚀刻剂由栅线缝隙151的开口逐渐向绝缘叠层结构的内部蚀刻牺牲层。由于蚀刻剂的选择性，该蚀刻相对于绝缘叠层结构中的层间绝缘层去除牺牲层。

[0097] 在形成栅极导体时，利用栅线缝隙151作为沉积物通道，采用原子层沉积(ALD)，在栅线缝隙151和空腔中填充金属层。

[0098] 在该实施例中，金属层例如由钨组成。在原子层沉积中采用的前驱源例如是六氟化钨WF6，采用的还原气体例如是硅烷SiH4或乙硼烷B2H6。在原子层沉积的步骤中，利用六氟化钨WF6与硅烷SiH4的反应产物的化学吸附获得钨材料实现沉积过程。

[0099] 在形成栅极导体之后，在绝缘区域A03内部，仍然保留着绝缘叠层结构，其中，多个牺牲层和多个层间绝缘层交替堆叠。在绝缘区域A03外部，将绝缘叠层结构替换为栅叠层结构中，其中，多个栅极导体和多个层间绝缘层交替堆叠。

[0100] 在第一阵列结构L01和第二阵列结构L02中，均形成了选择晶体管和存储晶体管。以第一阵列结构L01为例，在沟道柱110的中间部分，栅极导体109与沟道柱110内部的沟道层111、隧穿介质层112、电荷存储层113和阻挡介质层114一起，形成存储晶体管。在沟道柱110的两端，栅极导体109与沟道柱110内部的沟道层111(或半导体层116)和阻挡介质层114一起，形成选择晶体管。

[0101] 进一步地，在绝缘区域A03中形成多个导电通道123，提供半导体衬底中的CMOS电路与外部电路之间的电连接，如图4h所示。

[0102] 在绝缘区域A03内部，导电通道123例如是多个导电柱组成的阵列，分别从第一阵列结构的半导体衬底101向上延伸，依次贯穿第一阵列结构的绝缘叠层结构、第二阵列结构的绝缘叠层结构，到达第二阵列结构的顶部。

[0103] 在该实施例中，导电通道123位于绝缘区域A03中。在替代的实施例中，可以在栅线缝隙151中形成导电通道，或者在栅叠层结构中形成导电通道。例如，导电通道与沟道柱相邻，并且在与沟道孔类似的通道孔中形成导电柱和绝缘层。该导电通道贯穿第一阵列结构和第二阵列结构的栅叠层结构，并且导电通道与邻近的栅极导体之间由绝缘层隔开。

[0104] 在该实施例中，导电通道123提供CMOS电路与外部电路之间的电连接。在替代的实施例，导电通道还可以提供第一阵列结构L01的公共源区103与外部电路之间的电连接。在该替代的实施例中，导电通道从第一阵列结构的半导体衬底101中的公共源区103向上延

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伸，依次贯穿第一阵列结构的栅叠层结构、第二阵列结构的栅叠层结构，到达第二阵列结构的顶部。

[0105] 在该实施例中，导电通道中的导电柱例如由Ti/TiN或W组成，绝缘层例如由氧化硅组成。

[0106] 进一步地，在第二阵列结构L02的栅叠层结构上形成半导体层201，在半导体层201中形成多个掺杂区，以及形成多个导电通道，如图4i所示。

[0107] 与图4a所示的半导体衬底101中形成的掺杂区类似，在半导体层201中形成多个阱区。如图4i所示，所述多个阱区例如包括深N阱202、位于深N阱202中的高压P阱203、与高压P阱203相邻接的高压N阱205、位于高压P阱203中的P+掺杂区204、位于高压N阱205中的N+掺杂区206。在该实施例中，公共源区203作为沟道柱的公共源区，高压N阱205用于对公共源区的预充电，P+掺杂区204和N+掺杂区206分别作为接触区以减小接触电阻。该高压P阱203作为多个沟道柱的公共源区，因此位于绝缘叠层结构的下方。

[0108] 与图4a所示的半导体衬底101中形成的掺杂区不同之处在于，由于第二阵列结构L02中的多个晶体管在垂直方向上的堆叠顺序与第一阵列结构L01中的多个晶体管的堆叠顺序相反，因此，半导体层201中的高压P阱203从半导体衬底201的内部延伸至与栅叠层结构相接触的下表面，从而与沟道柱210的第二端接触，形成公共源区。

[0109] 该3D存储器件中的多个导电通道分别包括作为芯部的导电柱131和作为隔离层的绝缘层132，所述绝缘层132用于将导电柱131与周围的导电材料彼此隔开。所述多个导电通道例如包括导电通道TAC、SL1、HV1、SL2、HV2。导电通道TAC贯穿半导体层201，将从第一阵列结构L01的衬底101向上延伸至第二阵列结构L02的导电通道123与外部电路之间的电连接。导电通道SL1和HV1分别与第一阵列结构L01中的P+掺杂区104和N+掺杂区106相接触，从而提供第一阵列结构L01的公共源区和高压N阱与外部电路之间的电连接。导电通道SL2和HV2分别与第二阵列结构L02中的P+掺杂区204和N+掺杂区206相接触，从而提供第一阵列结构L01的公共源区和高压N阱与外部电路之间的电连接。

[0110] 在以上的描述中，对于各层的构图、蚀刻等技术细节并没有做出详细的说明。但是本领域技术人员应当理解，可以通过各种技术手段，来形成所需形状的层、区域等。另外，为了形成同一结构，本领域技术人员还可以设计出与以上描述的方法并不完全相同的方法。另外，尽管在以上分别描述了各实施例，但是这并不意味着各个实施例中的措施不能有利地结合使用。

[0111] 以上对本发明的实施例进行了描述。但是，这些实施例仅仅是为了说明的目的，而并非为了限制本发明的范围。本发明的范围由所附权利要求及其等价物限定。不脱离本发明的范围，本领域技术人员可以做出多种替代和修改，这些替代和修改都应落在本发明的范围之内。

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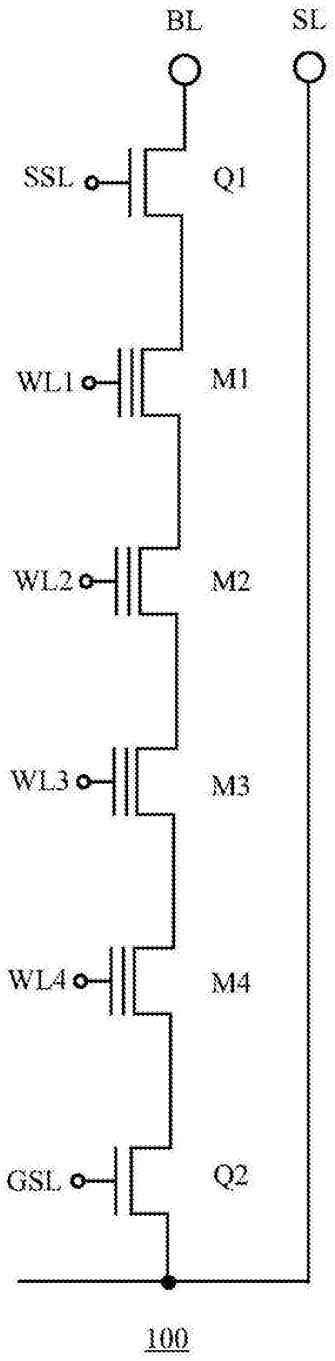


图1a

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Micron v. YMTC
IPR2024-00789

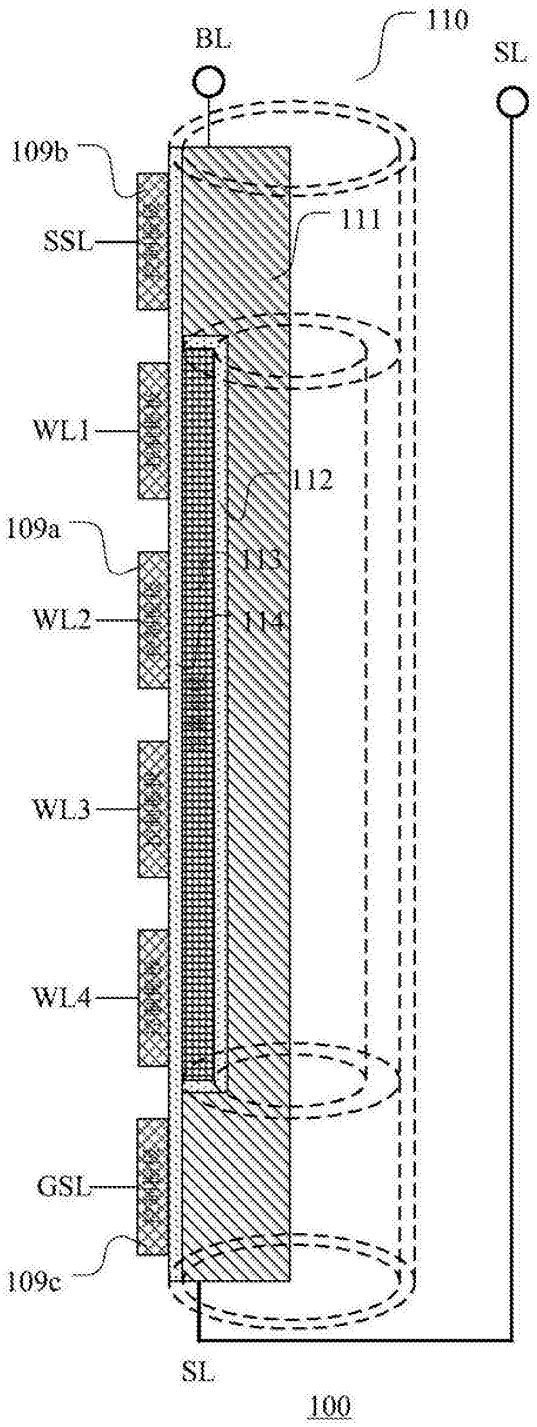


图1b

Micron Ex. 1002, p. 189
Micron v. YMTC
IPR2024-00789

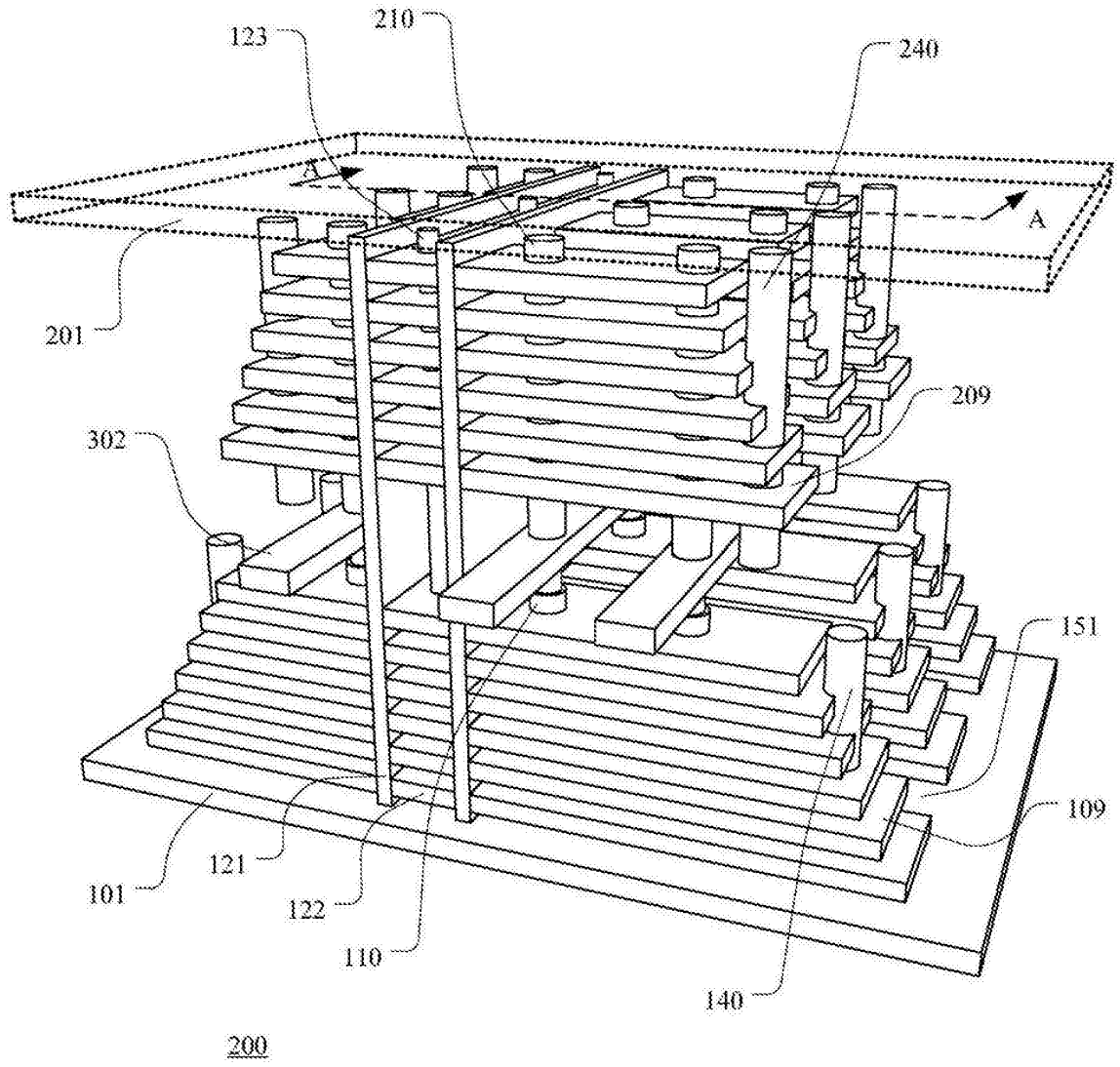


图2

Micron Ex. 1002, p. 190
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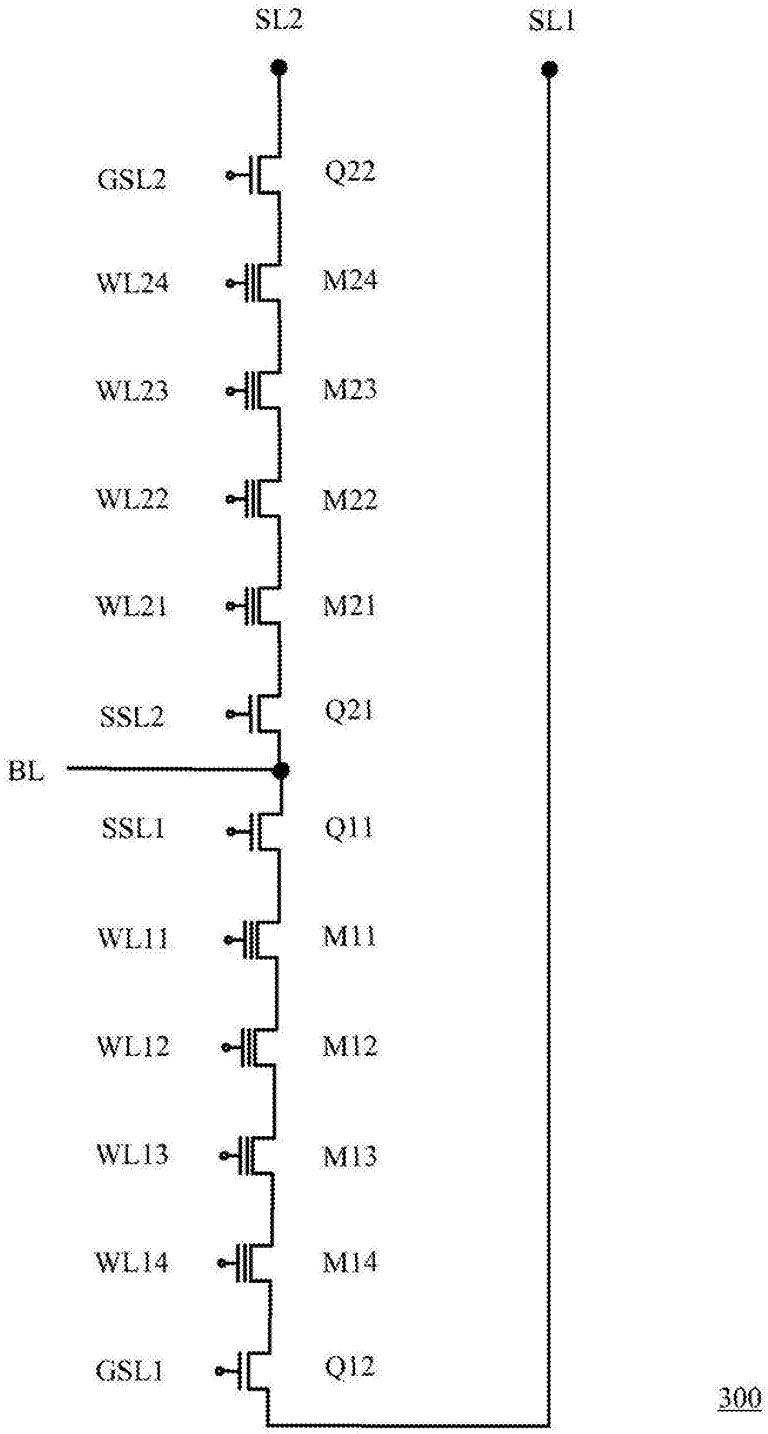


图3

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IPR2024-00789

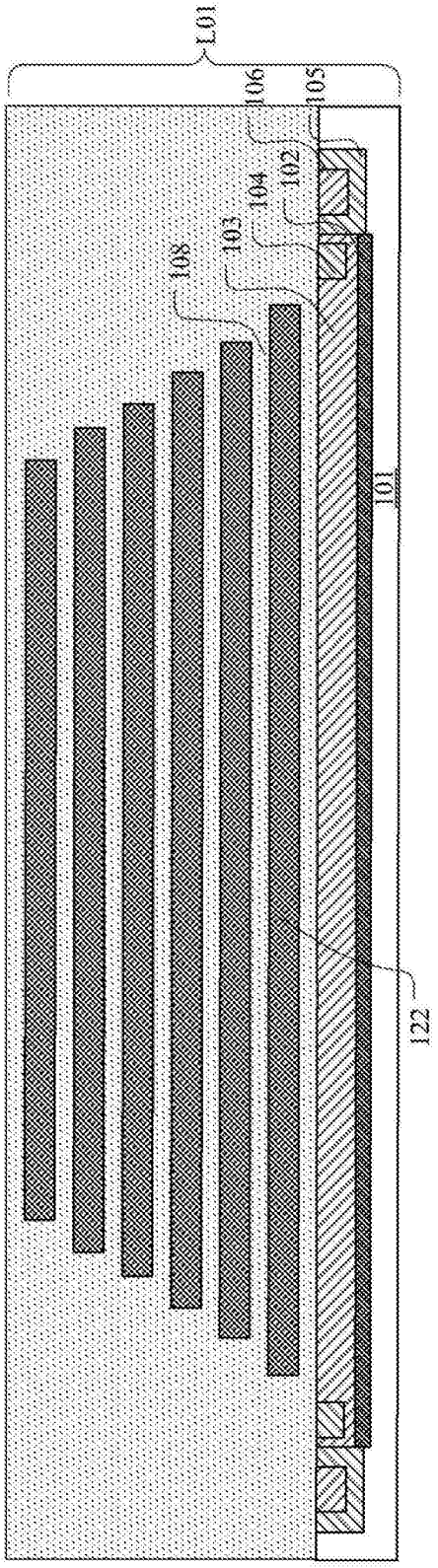


图4a

Micron Ex. 1002, p. 192
Micron v. YMTC
IPR2024-00789

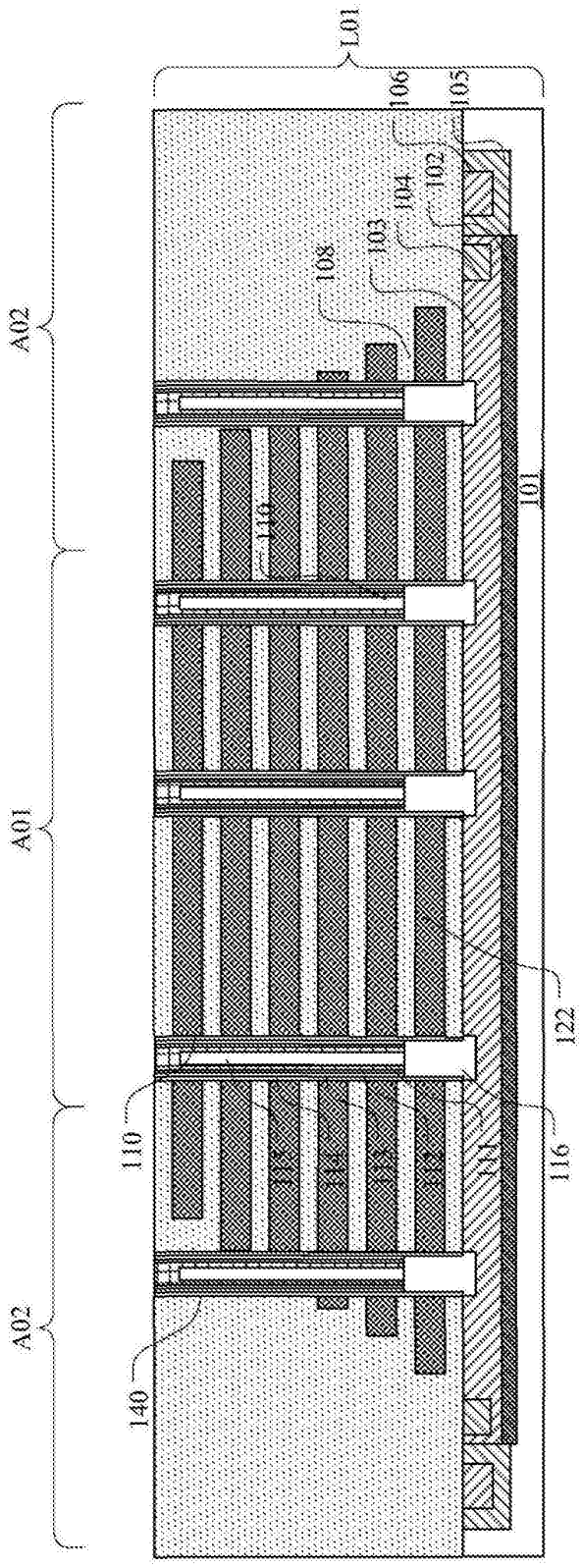


图4b

Micron Ex. 1002, p. 193
Micron v. YMTC
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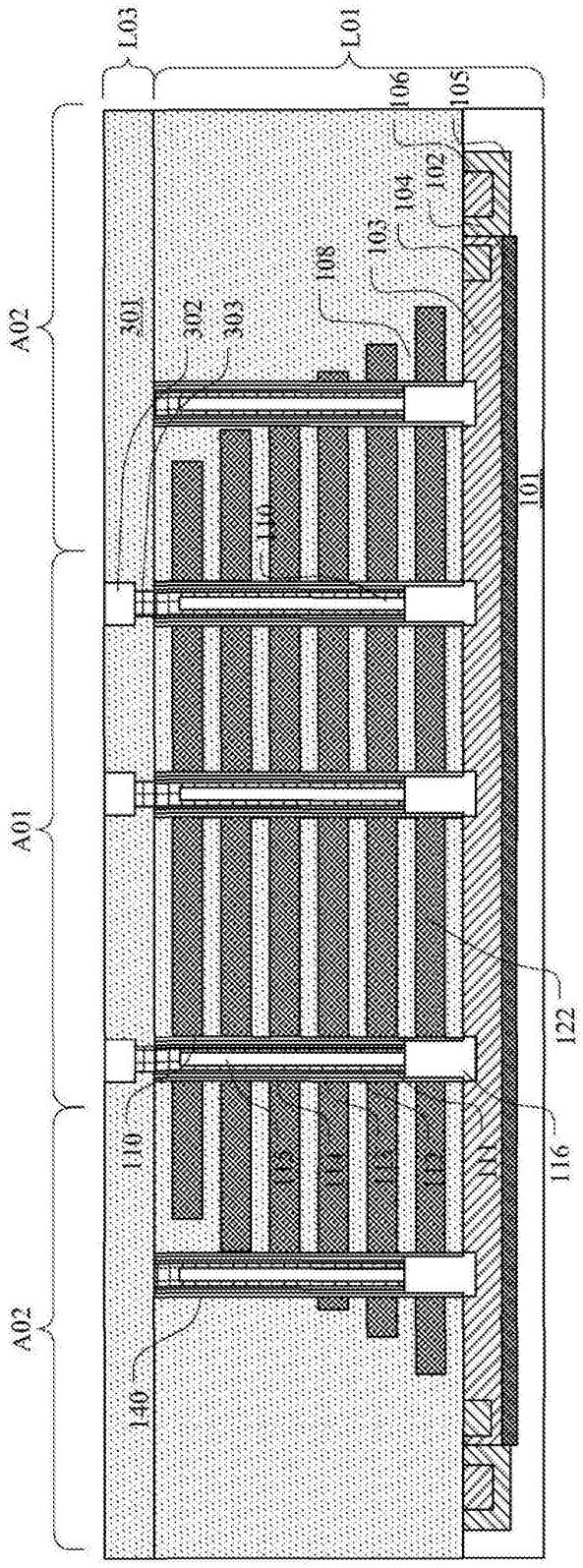


图4c

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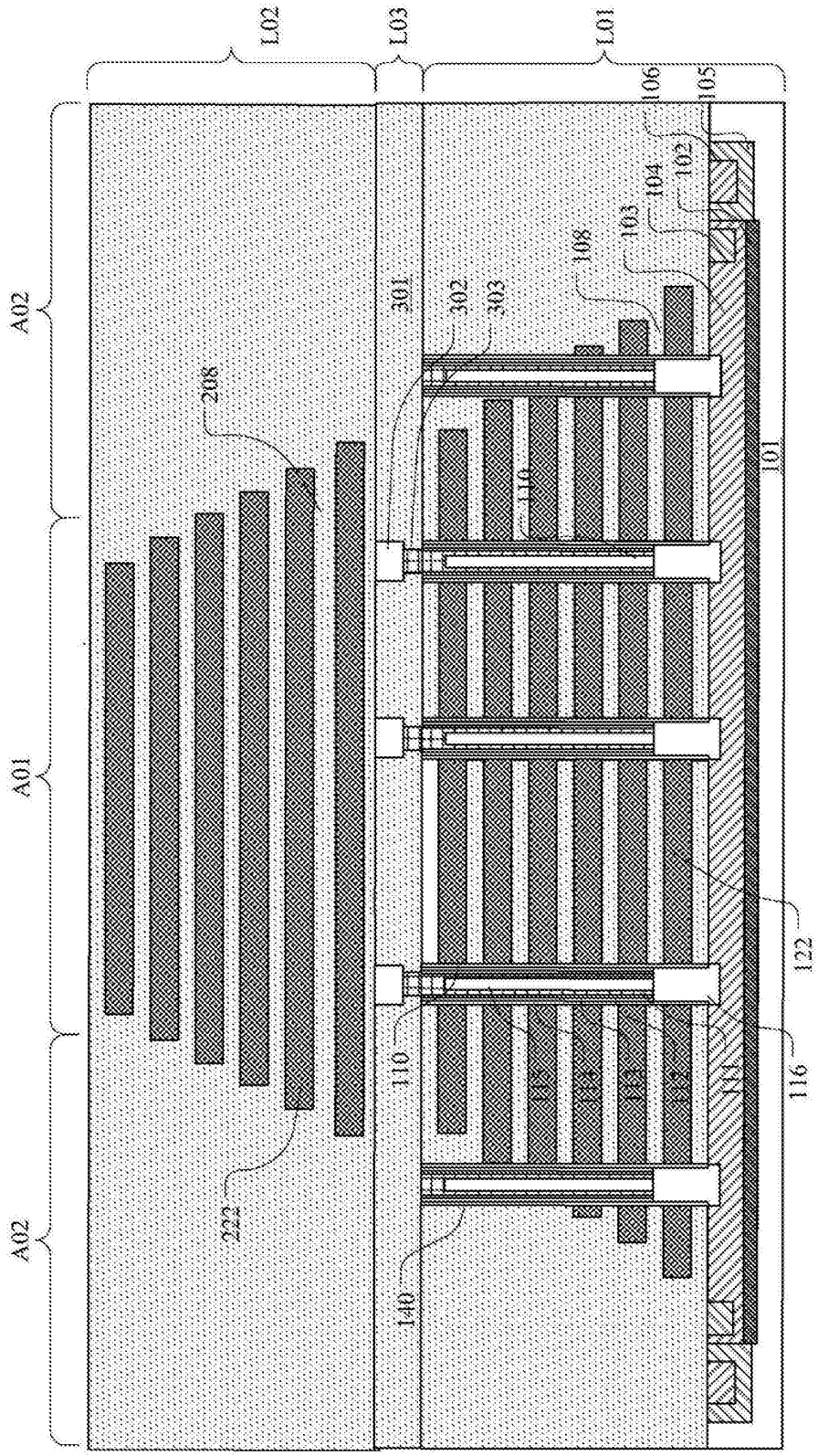


图4d

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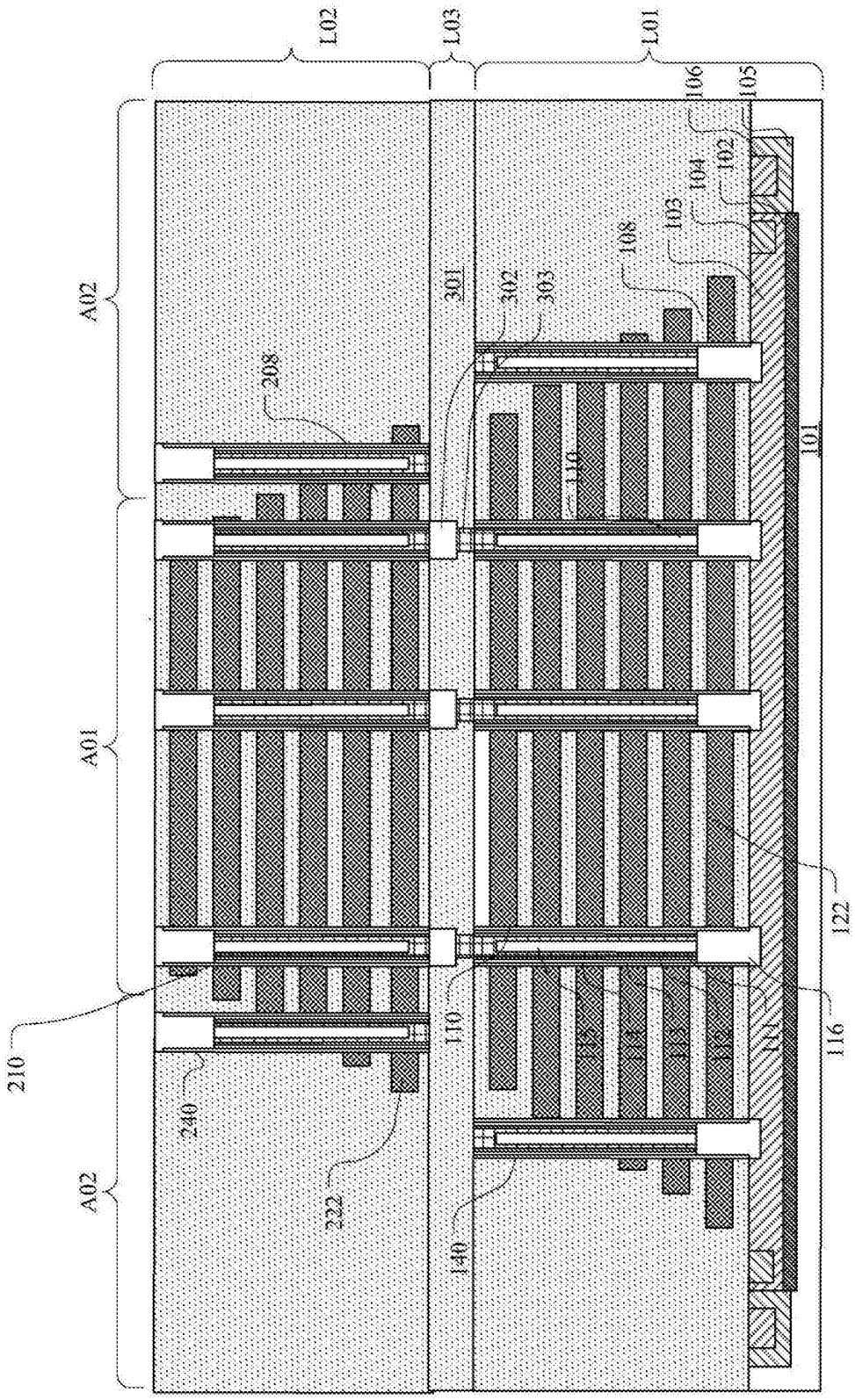


图4e

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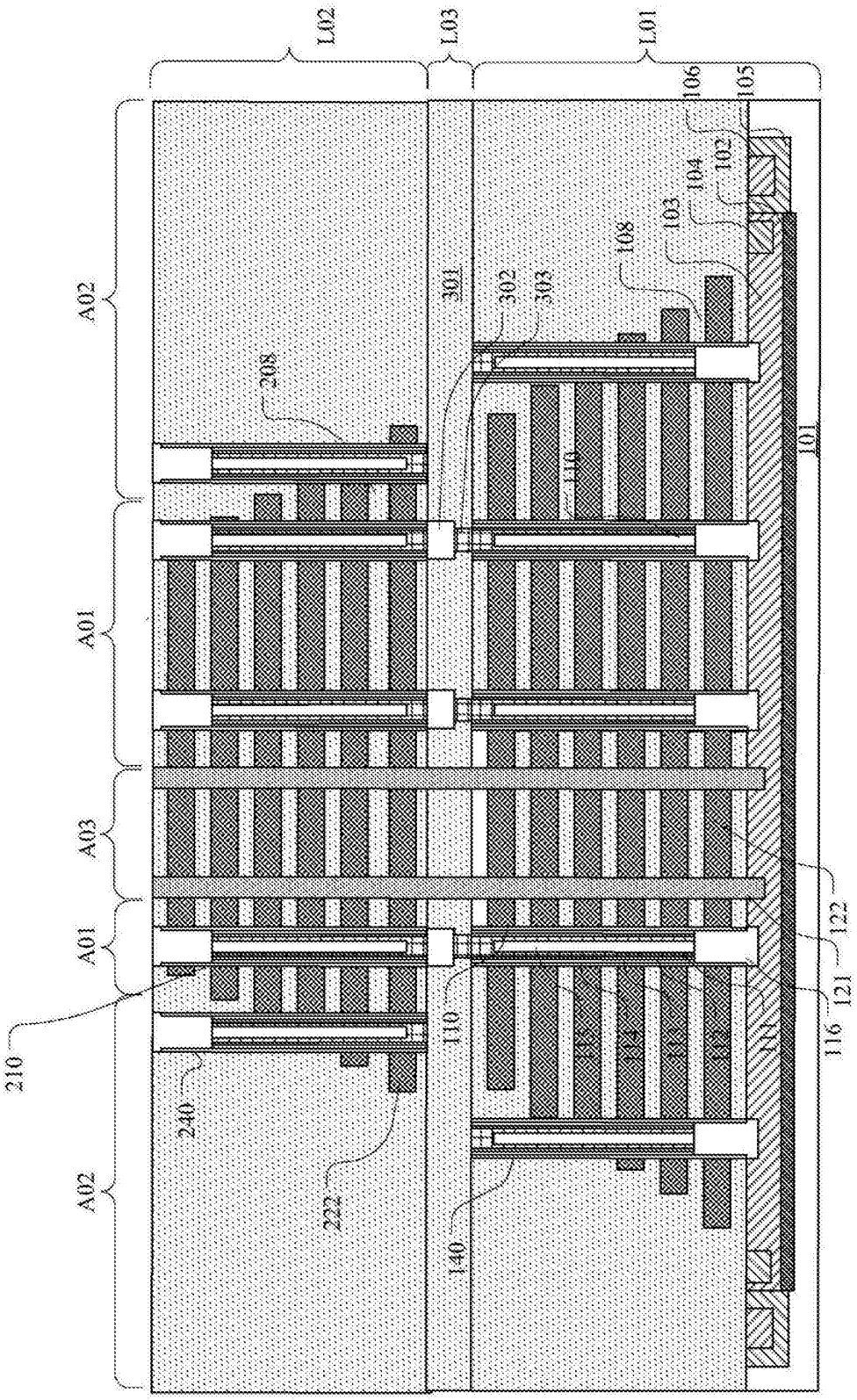


图4f

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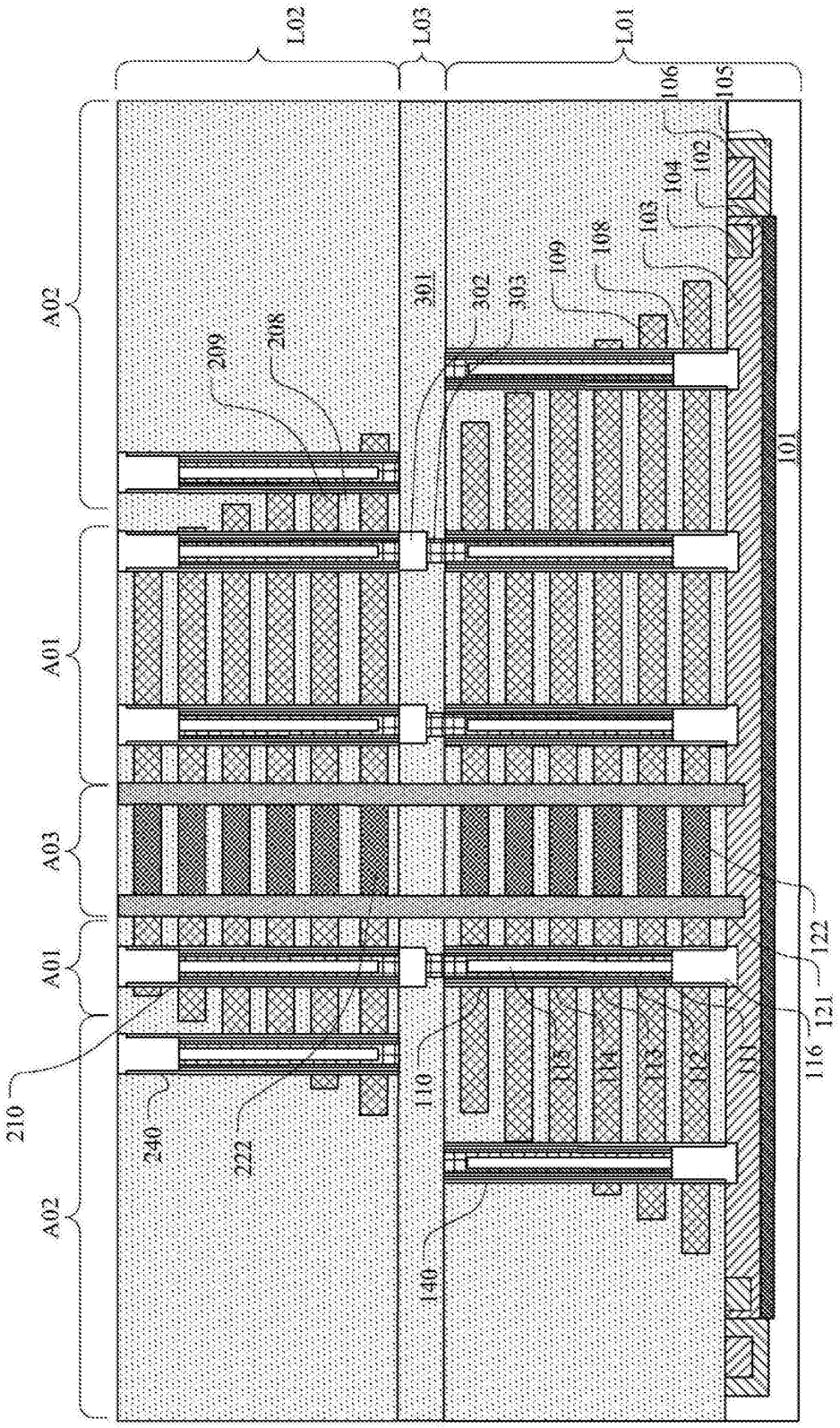


图4g

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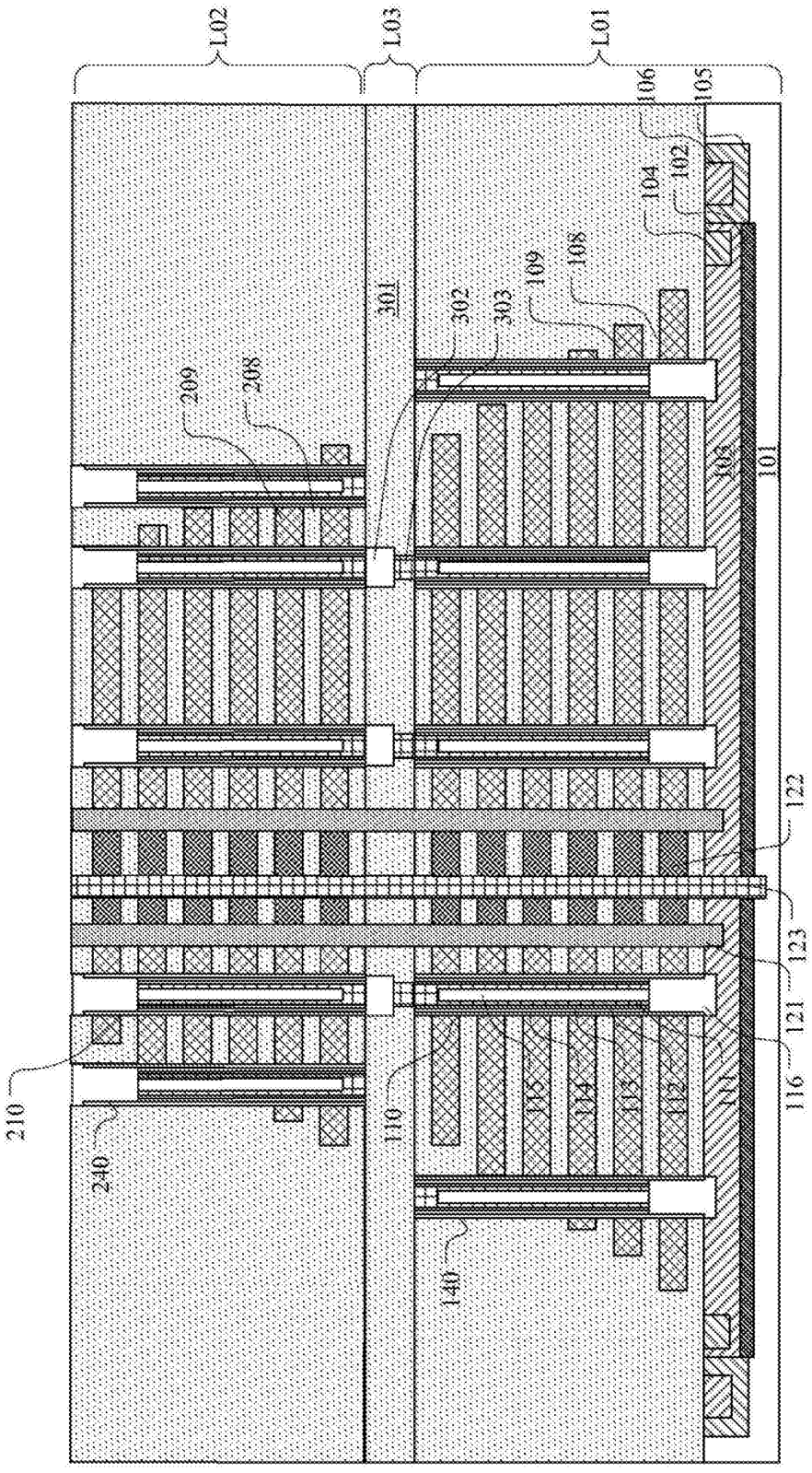


图4h

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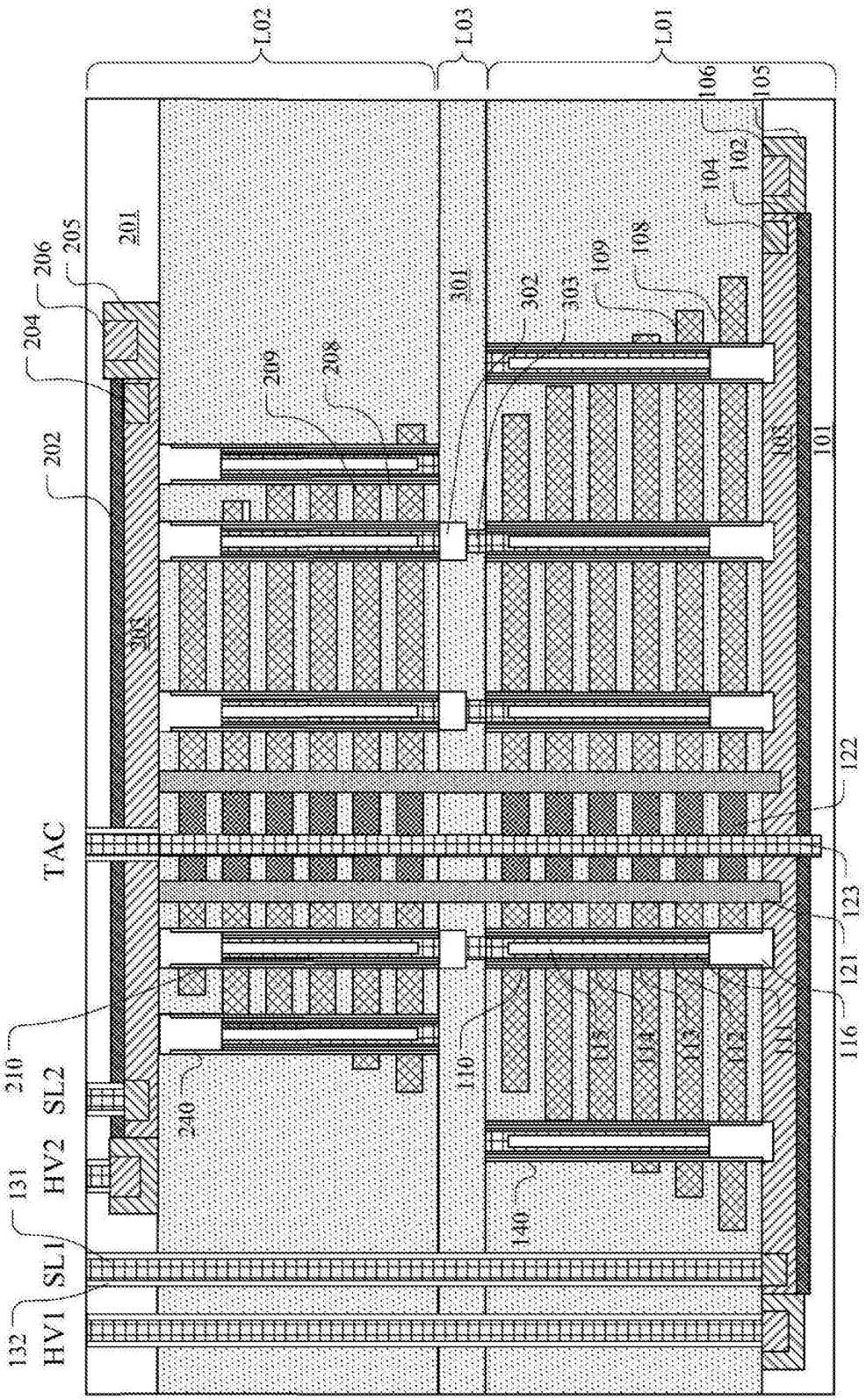


图4i

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Micron v. YMTC
IPR2024-00789

Electronic Acknowledgement Receipt

EFS ID:	37763615
Application Number:	16402202
International Application Number:	
Confirmation Number:	7288
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Wenyu Hua
Customer Number:	153988
Filer:	Zhiwei Zou/Anna O'Connor
Filer Authorized By:	Zhiwei Zou
Attorney Docket Number:	10018-01-0045-US
Receipt Date:	15-NOV-2019
Filing Date:	02-MAY-2019
Time Stamp:	12:48:47
Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	10018-01-0045-US_IDS_SB082.pdf	611949 81699797ba7e0d752c5cec79a72d3ec544aee5f8	no	4

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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Application Number	16402202
Filing Date	2019-05-02
First Named Inventor	Wenyu HUA
Art Unit	2811
Examiner Name	GURLEY, LYNNE ANN
Attorney Docket Number	10018-01-0045-US

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	1	201834207	TW	A	2018-09-16	YANGTZE MEMORY TECHNOLOGIES CO LTD		
	2	201539724	TW	A	2015-10-16	TOSHIBA KK		
	3	201533887	TW	A	2015-09-01	MACRONIX INT CO LTD		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16402202
	Filing Date	2019-05-02
	First Named Inventor	Wenyu HUA
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	10018-01-0045-US

	4	I569405	TW	A	2016-10-16	MACRONIX INT CO LTD		

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	Application Number	16402202
	Filing Date	2019-05-02
	First Named Inventor	Wenyu HUA
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	10018-01-0045-US

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That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2019-11-29
Name/Print	Zhiwei Zou	Registration Number	66,041

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Espacenet

TW201834207A Interconnect structure of three-dimensional memory device

Applicants: YANGTZE MEMORY TECHNOLOGIES CO LTD [CN]
Inventors: LI YONGNA [US], LU ZHENYU [US], PAN FENG [US], SHI WEN-GUANG [CN], SONG LIDONG [US], YANG STEVE WIYI [US]

IPC ***H01L21/8239; H01L27/105;***

CPC **H01L21/76895H01L23/5226H01L24/05H01L27/11519H01L27/11529H01L27/11531H01L27/11548H01L27/11556H01L27/11565H01L27/1157H01L27/11573H01L27/115** **(US); (US); (US); (US); (CN); (CN); (US); (US); (US); (EP,US); (CN); (EP,US);**

Application number: TW107107648A
Priority numbers: CN201710134788A 2017-03-08; CN2018077741W 2018-03-01
Publication date: 2018-09-16
Filing date: 2018-03-07
Priority date: 2017-03-08
Published as: **CN106920796A; CN106920796B; WO2018161839A1; CN109935593A; CN110121775A; KR20190119149A;** TW201834207A;**US2019067314A1**

Abstract: Interconnect structure of three-dimensional memory device

Embodiments of interconnect structures of a three-dimensional (3D) memory device and method for forming the interconnect structures are disclosed. In an example, a 3D NAND memory device includes a substrate, an alternating layer stack including a staircase structure on the substrate, and a barrier structure extending vertically through the alternating layer stack. The alternating layer stack includes an alternating dielectric stack and an alternating conductor/dielectric stack. The alternating dielectric stack includes dielectric layer pairs enclosed by at least the barrier structure. The alternating conductor/dielectric stack includes conductor/dielectric layer pairs. The memory device further includes a channel structure and a slit structure each extending vertically through the alternating conductor/dielectric stack, an etch stop layer on an end of the channel structure, and first contacts.

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201834207

(19)中華民國智慧財產局

(12)發明說明書公開本 (11)公開編號：TW 201834207 A

(43)公開日： 中華民國 107 (2018) 年 09 月 16 日

(21)申請案號：107107648 (22)申請日： 中華民國 107 (2018) 年 03 月 07 日

(51)Int. Cl.： *H01L27/105 (2006.01)* *H01L21/8239(2006.01)*

(30)優先權：2017/03/08 中國大陸 201710134788.9

2018/03/01 世界智慧財產權組織 PCT/CN2018/077741

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申請實體審查：有 申請專利範圍項數：20 項 圖式數：12 共 53 頁

(54)名稱

三維記憶體裝置的互連結構

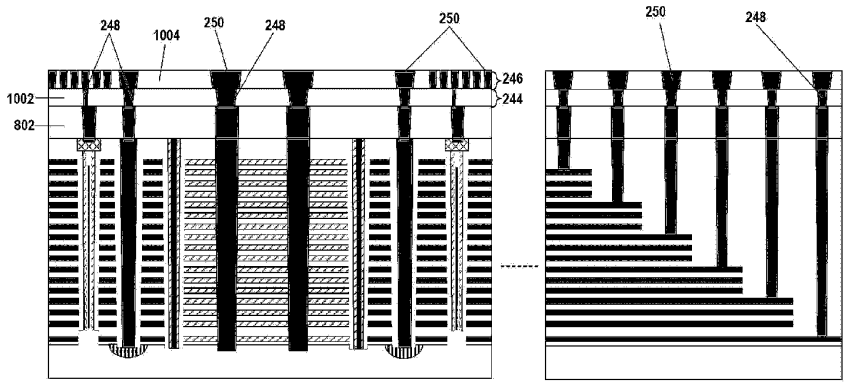
INTERCONNECT STRUCTURE OF THREE-DIMENSIONAL MEMORY DEVICE

(57)摘要

本發明揭露三維(3D)記憶體裝置的互連結構及其製作方法之實施例。在一實例中，3D 反及(NAND)記憶體裝置包括基底、設置於基底上並包括階梯結構的交替堆疊層以及垂直延伸並貫穿交替堆疊層的阻障結構。交替堆疊層包括介電質交替堆疊以及導體/介電質交替堆疊。介電質交替堆疊包括被至少阻障結構環繞的介電層對。導體/介電質交替堆疊包括複數個導體/介電層對。記憶體裝置另包括通道結構、狹縫結構、蝕刻停止層以及複數個第一接觸，通道結構與狹縫結構中的每一個垂直延伸並貫穿導體/介電質交替堆疊，且蝕刻停止層設置於通道結構的一端上。

Embodiments of interconnect structures of a three-dimensional (3D) memory device and method for forming the interconnect structures are disclosed. In an example, a 3D NAND memory device includes a substrate, an alternating layer stack including a staircase structure on the substrate, and a barrier structure extending vertically through the alternating layer stack. The alternating layer stack includes an alternating dielectric stack and an alternating conductor/dielectric stack. The alternating dielectric stack includes dielectric layer pairs enclosed by at least the barrier structure. The alternating conductor/dielectric stack includes conductor/dielectric layer pairs. The memory device further includes a channel structure and a slit structure each extending vertically through the alternating conductor/dielectric stack, an etch stop layer on an end of the channel structure, and first contacts.

指定代表圖：



第10圖

符號簡單說明：

802、1002、

1004・・・介電層

244・・・接觸層

246・・・互連導體層

248、250・・・接觸

【發明說明書】

【中文發明名稱】三維記憶體裝置的互連結構

【英文發明名稱】INTERCONNECT STRUCTURE OF THREE-DIMENSIONAL MEMORY DEVICE

【技術領域】

【0001】　本揭露的實施例係關於三維(three-dimensional, 3D)記憶體裝置及其製作方法。

【先前技術】

【0002】　平面記憶體單元係透過改善製程技術、電路設計、演算法程式設計與製作方法來縮小至較小的尺寸。然而，隨著記憶體單元的特徵尺寸接近下限時，平面製程與製作技術變得艱難且耗費成本，因此平面記憶體單元的記憶體密度接近上限。

【0003】　3D記憶體架構可處理平面記憶體單元的密度受限制的問題。3D記憶體架構包括記憶體陣列與用以控制訊號進出記憶體陣列的周邊元件。

【發明內容】

【0004】　下文揭露3D記憶體互連線與其製作方法。

【0005】　依據本揭露的一些實施例，3D反及(NAND)記憶體裝置包括基底、設置於基底上並包括階梯結構之交替堆疊層以及垂直延伸並貫穿交替堆疊層的阻障結構。交替堆疊層包括介電質交替堆疊以及導體/介電質交替堆疊。介電質交替堆疊包括被至少阻障結構環繞的複數個介電層對。導體/介電質交替堆疊包括

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複數個導體/介電層對。記憶體裝置另包括通道結構、狹縫結構，通道結構與狹縫結構中的每一個垂直延伸並貫穿導體/介電質交替堆疊。蝕刻停止層設置於通道結構的一端上。設置於階梯結構中的導體/介電質交替堆疊的導體層、蝕刻停止層以及狹縫結構中的每一個與複數個第一接觸中的一個相接觸。

【0006】　於一些實施例中，蝕刻停止層包括多晶矽、鈦、氮化鈦以及鎢中之一個或多個。阻障結構包括氧化矽與氮化矽。各介電層對可包括一氧化矽層以及一氮化矽層，且各導體/介電層對包括一金屬層以及一氧化矽層。

【0007】　於一些實施例中，記憶體裝置另包括一虛置通道結構，垂直延伸並貫穿該導體/介電質交替堆疊。

【0008】　於一些實施例中，記憶體裝置另包括互連導體層以及接觸層。接觸層包括複數個第二接觸。設置於階梯結構中的導體/介電質交替堆疊的導體層、通道結構以及狹縫結構中的每一個透過對應的一第一接觸以及第二接觸中的相應一個電性連接至互連導體層。

【0009】　於一些實施例中，記憶體裝置另包括一第三接觸(例如貫穿陣列接觸(through array contact, TAC))，垂直延伸並貫穿被至少阻障結構環繞的介電質交替堆疊。

【0010】　根據本揭露的一些實施例，形成3D NAND記憶體裝置的方法揭露如下。於基底上形成介電質交替堆疊。介電質交替堆疊包括複數個介電層對，各介電層對包括第一介電層與不同於第一介電層的第二介電層。於介電質交替堆疊中形成第一階梯結構。形成通道結構以及阻障結構，通道結構與阻障結構中的每一個垂直延伸並貫穿介電質交替堆疊。阻障結構將介電質交替堆疊區隔出第一部分與第二部分，第一部分被至少阻障結構環繞，且第二部分包括第一階梯結構。於通道結構的一上端形成蝕刻停止層。形成狹縫。透過狹縫將設置於介電質交替堆疊的第二部分中的第一介電層取代為複數個導體層，以形成包括

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複數個導體/介電層對的導體/介電質交替堆疊。透過於狹縫中填入導體以形成狹縫結構。形成複數個第一接觸。設置於第一階梯結構中的導體/介電質交替堆疊的第一導體層、蝕刻停止層以及狹縫結構中的每一個與第一接觸中的一個相接觸。

【0011】　於一些實施例中，形成複數個第二接觸。第二接觸中之一個垂直延伸並貫穿介電質交替堆疊中被至少阻障結構環繞的第一部分，且第二接觸中之另一個與第一階梯結構中的導體/介電質交替堆疊的第二導體層相接觸。

【0012】　於一些實施例中，形成包括複數個第三接觸之接觸層。於接觸層上形成互連導體層。設置於第一階梯結構中的導體/介電質交替堆疊的第一導體層、通道結構以及狹縫結構中的每一個可透過對應的一第一接觸以及第二接觸中的相應一個電性連接至互連導體層。

【0013】　於一些實施例中，各第二接觸透過第三接觸中的相應一個電連接至互連導體層。

【0014】　於一些實施例中，在形成狹縫之前，於基底中形成摻雜區。狹縫結構與摻雜區相接觸。

【0015】　於一些實施例中，於相鄰於阻障結構的介電質交替堆疊中形成第二階梯結構。

【0016】　於一些實施例中，蝕刻停止層包括多晶矽、鈦、氮化鈦與鎢中之一或多者。阻障結構包括氧化矽與氮化矽。各介電層對可包括氧化矽層與氮化矽層。各導體/介電層對可包括金屬層與氧化矽層。

【圖式簡單說明】

【0017】

所附圖式併入本文並構成說明書的一部分，其例示出了本揭露所揭示的實

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施例，並且進一步與詳細說明一起用於解釋本揭露所揭示的原理，以使相關領域的技術人員能夠製作及使用本揭露所揭示的內容。

第1A圖至第1C圖依據本案揭露的一些實施例所繪示的3D記憶體裝置的不同區域的平面示意圖。

第2圖依據本案揭露的一些實施例所繪示的3D記憶體裝置的剖視示意圖。

第3圖依據本案揭露的一些實施例所繪示的形成3D記憶體裝置的方法範例流程圖。

第4圖至第10圖依據本案揭露的一些實施例所繪示的形成3D記憶體裝置的製程範例示意圖。

第11圖依據本案揭露的一些實施例所繪示的形成3D記憶體裝置的方法範例流程圖。

第12圖依據本案揭露的一些實施例所繪示的形成3D記憶體裝置的另一方法範例流程圖。

本揭露所揭露的實施例將參照所附圖式進行說明。

【實施方式】

【0018】 儘管本文討論了具體的結構及配置，但應該理解，這僅僅是為了說明及示例的目的而完成的。相關領域的技術人員應可理解，在不脫離本揭露的精神及範圍的情況下，可以使用其他結構及配置。對於相關領域的技術人員顯而易見的是，本揭露還可以用於各種其他應用中。

【0019】 值得注意的是，在說明書中對提及「一個實施例」、「一實施例」、「示範性實施例」、「一些實施例」等的引用表示所描述的實施例可以包括特定的特徵、結構或特性，但並非每個實施例都一定需要包括此特定的特徵、結構或特性，而且這些用語不一定指相同的實施例。此外，當特定特徵、結構或特性結

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合實施例描述時，無論是否於文中明確教示，結合其他實施例來實現這些特徵、結構或特性皆屬於相關領域的技術人員的知識範圍所及。

【0020】　一般而言，術語可以至少部分地根據上、下文中的用法來理解。例如，如本文所使用的術語「一個或多個」可用於以單數意義描述任何特徵、結構或特性，或可用於描述特徵、結構或特徵的複數組合，至少可部分取決於上、下文。類似地，術語諸如「一」、「一個」或「該」也可以被理解為表達單數用法或傳達複數用法，至少可部分取決於上、下文。

【0021】　應該容易理解的是，本文中的「在...上面(on)」、「在...之上(above)」及「在...上方(over)」的含義應該以最寬泛的方式來解釋，使得「在...上面」不僅意味著「直接在某物上」，而且還包括在某物上且兩者之間具有中間特徵或中間層，並且「在...之上」或「在...上方」不僅意味著在某物之上或在某物上方的含義，而且還可以包括兩者之間沒有中間特徵或中間層（即，直接在某物上）的含義。

【0022】　此外，為了便於描述，可以在說明書使用諸如「在...下面(beneath)」、「在...之下(below)」、「較低(lower)」、「在...之上(above)」、「較高(upper)」等空間相對術語來描述一個元件或特徵與另一個或多個元件或特徵的關係，如圖式中所表示者。除了圖式中描繪的方向之外，這些空間相對術語旨在涵蓋使用或操作中的元件的不同方位或方向。該元件可以其他方式定向（例如以旋轉90度或以其它方向來定向），並且同樣能相應地以說明書中所使用的空間相關描述來解釋。

【0023】　如本文所使用的，術語「基底」是指在其上添加後續材料層的材料。基底本身可以被圖案化。添加在基底頂部的材料可以被圖案化或可以保持未圖案化。此外，基底可以包括多種半導體材料，例如矽、鍺、砷化鎵、磷化銦等。或者，基底可以由非導電材料製成，例如玻璃、塑料或藍寶石晶圓。

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【0024】　如本文所使用的，術語「層」是指一材料部分，其一區域具有一厚度。一層的範圍可以在整個下層或上層結構上延伸，或者其範圍可以小於下層或上層結構的範圍。此外，一層可以為均勻或不均勻連續結構的一區域，其厚度可小於該連續結構的厚度。例如，一層可以設置於該連續結構的上表面及下表面之間或在該連續結構的上表面及下表面之間的任何一對水平平面之間。一層可以水平地、垂直地及/或沿著漸縮表面延伸。一基底可以為一層，其可以包括一層或多層，及/或可以在其上面及/或下面具有一層或多層。一層可以包含多層。例如，互連層可以包括一個或多個導體及接觸層（其中形成有接觸、互連線及/或通孔）以及一個或多個介電層。

【0025】　如本文所使用的，術語「名義上(nominal)/名義上地(nominally)」是指在產品或製程的設計階段期間設定的組件或製程操作的特性或參數的期望值或目標值，以及高於及/或低於期望值的數值範圍。數值範圍可能由於製造工藝或公差而有輕微變化。如本文所使用的術語「約/大約」表示可能會隨著與對象半導體裝置相關聯的特定技術點而改變的給定量數值。基於特定的技術點，術語「約/大約」可以指示出給定量數值，例如在該數值的10-30%內變化（例如，該數值的±10%、±20%或±30%）。

【0026】　如本文所使用的，術語「三維(3D)記憶體裝置」是指一種於橫向定向的基底上具有垂直定向的記憶體單元電晶體串（例如稱為「記憶體串」，諸如NAND串(NAND string)）半導體裝置，使得記憶體串相對於基底在垂直方向上延伸。如本文所使用的，術語「垂直/垂直地」名義上是指垂直於基底的橫向表面。

【0027】　本揭露的各式實施例提供一種具有互連結構以作為記憶體陣列（於本文也被稱為「陣列元件」）的3D記憶體裝置，互連結構可在有限的步驟中（於單一步驟或兩步驟）製造而使其接觸於各種記憶體陣列結構(例如NAND串、閘

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極線狹縫(gate line slit)以及字元線(word line)等)，藉此降低製程複雜度以及製造成本。在一些實施例中，本文所揭露的互連結構包括設置於上互連導體層中的位元線，此互連結構適用於3D記憶體架構，這些記憶體架構的陣列元件與周邊元件係形成在不同的基底上，且基底係以面對面混和接合(hybrid bonding)的方式而彼此連結。

【0028】 本所所揭露的互連結構可包括用以在堆疊陣列元件與周邊元件之間提供垂直互連(例如用於電源匯流排與金屬佈線）的TAC，藉此減少金屬層以及縮減晶粒尺寸。在一些實施例中，本文所揭露在互連結構中的TAC係貫穿形成於介電層的交替堆疊中，與導體和介電層的交替堆疊相比，介電層的交替堆疊可以更容易地被蝕刻而形成穿孔。

【0029】 第1A圖至第1C圖依據本案揭露的一些實施例所繪示的3D記憶體裝置的不同區域的平面示意圖。第1圖繪示出3D記憶體裝置的字元線(word line, WL)TAC區102，其中包含有NAND串區110、TAC區120以及頂選擇閘極(top selective gate, TSG)階梯區130。NAND串區110可包括複數個NAND串112所構成的陣列，各NAND串112包括複數個堆疊的記憶體單元。TSG階梯區130在平面圖上可設置於NAND串區110的兩側並鄰近TAC區120。TSG階梯區130可包括形成在一階梯結構(例如具有兩階層)上的TSG接觸132所構成的陣列，用以與NAND串區110中的NAND串112的TSG達到電性連接。

【0030】 在一些實施例中，TAC區120設置於3D記憶體裝置的字元線方向(在第1A圖至第1C圖中標示為「WL」)上的兩TSG階梯區130。TAC區120可透過阻障結構124定義出，且TAC區120中可形成有多個TAC 126，並透過阻障結構124橫向環繞。在一些實施例中，TAC區120外側可形成有虛置通道結構122，以對記憶體陣列結構提供機構上的支撐。可理解的是，虛置通道結構122可形成於TAC區120外側的任一區域中，例如NAND串區110鄰近TSG階梯區130的邊緣。如第

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1A圖所示，WL TAC區102也可包括複數個狹縫結構114，且各狹縫結構沿著字元線方向延伸。至少一些狹縫結構114可作為用於NAND串區110中的NAND串112陣列的共用源極接觸。狹縫結構114也可將3D記憶體裝置分隔成多個記憶體區塊及/或多個指狀記憶體。

【0031】 第1B圖繪示出3D記憶體裝置的位元線(bit line, BL)TAC區104，其中包含有NAND串區110以及TAC區120。NAND串區110可包括NAND串112所構成的陣列，且各NAND串112包括複數個堆疊的記憶體單元。在一些實施例中，TAC區120在3D記憶體裝置的位元線方向(在第1A圖至第1C圖中標示為「BL」)上設置於兩NAND串區110之間。TAC區120可透過阻障結構124搭配3D記憶體裝置的BL TAC區104的邊緣定義出。TAC區120中可形成有多個TAC 126，並透過阻障結構124以及BL TAC區104的邊緣橫向環繞。如第1B圖所示，BL TAC區104還可包括狹縫結構114，各狹縫結構114沿著字元線方向延伸。至少一些狹縫結構114可作為用於NAND串區110中NAND串112所構成的陣列的共用源極接觸。狹縫結構114也可將3D記憶體裝置分隔成多個記憶體區塊及/或多個指狀記憶體。在一些實施例中，虛置通道結構122可形成於部分的NAND串區110中，例如形成於在位元線方向上鄰近TAC區120的指狀記憶體中。

【0032】 第1C圖繪示出3D記憶體裝置的階梯TAC區106，其中包含有NAND串區110、階梯區140以及TAC區120。NAND串區110可包括複數個NAND串112所構成的陣列，且各NAND串112包括複數個堆疊的記憶體單元。階梯區140可包括階梯結構與形成於階梯結構上的字元線接觸142所構成的陣列。在一些實施例中，TAC區120設置於階梯區140中。階梯區120可透過阻障結構獨自或結合3D記憶體裝置的階梯TAC區106的邊緣定義出。TAC區120中可形成有多個TAC 126，且被至少阻障結構124橫向環繞。如第1C圖所示，階梯TAC區106可另包括狹縫結構114，且各狹縫結構114沿著字元線方向延伸。至少一些狹縫結構114可作為

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用於NAND串區110中NAND串112所構成的陣列的共用源極接觸。狹縫結構114也可將記憶體裝置分隔成多個記憶體區塊及/或多個指狀記憶體。在一些實施例中，虛置通道結構可形成於TAC區120外側的階梯區140中。

【0033】 第2圖依據本案揭露的一些實施例所繪示的3D記憶體裝置200的剖視示意圖。3D記憶體裝置200可包括基底202，其中基底202可包括矽(例如單晶矽)、矽鍺(SiGe)、砷化鎵 (GaAs)、鍺(germanium, Ge)、矽覆絕緣層(silicon on insulator, SOI)、鍺覆絕緣層(germanium on insulator, GOI)或其適合的組合。在一些實施例中，基底202係透過研磨(grinding)、濕/乾蝕刻(wet/dry etching)、化學機械拋光(chemical mechanical polishing, CMP)或其組合薄化，而為薄化基底（例如半導電層）。

【0034】 3D記憶體裝置200可包括設置於基底202之上的陣列元件。值得注意的是，在第2圖中所增加的x軸與y軸係用於進一步例示出3D記憶體裝置200中的元件的空間關係。基底202包括兩橫向表面(例如上表面與下表面)沿著x方向(橫向方向)橫向延伸。本文所使用的，當基底(例如基底202)設置於半導體裝置(例如3D記憶體裝置200)在y方向上的最底層平面中時，無論半導體裝置中的一個元件（例如層或元件）是在另一元件（例如層或元件）「上面」、「上方」或「下方」，皆是以在y方向(垂直方向)上與半導體裝置的基底相對的關係來決定。本揭露以相同的概念來描述空間關係。

【0035】 3D記憶體裝置200可為非單片式(non-monolithic)的3D記憶體裝置的一部分，其中元件(例如周邊元件與陣列元件)可分別形成於不同的基底上，然後以面對面的方式彼此接合。在一些實施例中，陣列元件基底(例如基底202)仍可作為被接合的非單片式3D記憶體裝置的基底，且為了混和接合，周邊元件(例如任何適合用於幫助3D記憶體裝置200運作的數位、類比及/或數位類比混合訊號的周邊電路，3D記憶體裝置200例如頁面緩衝器(page buffer)、解碼器(decoder)

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與鎖存器(latch)；圖未示)係被翻轉至面朝下，以面向3D記憶體裝置200。可理解的是，在一些實施例中，為了混和接合，3D記憶體裝置200係被翻轉至面朝下，以面向周邊元件，使得在接合的非單片式3D記憶體裝置中，陣列元件係設置於周邊元件的上方。陣列元件基底(例如基底202)可為薄化基底(其並非接合的非單片式3D記憶體裝置的基底)，且非單片式3D記憶體裝置的後段製程(back-end-of-line, BEOL)互連線可形成於薄化陣列元件基底202的背側。

【0036】　然而，無論3D記憶體裝置200設置於非單片式3D記憶體裝置中的周邊元件的上方或下方，3D記憶體裝置200可為非單片式3D記憶體裝置的一部分。為方便參考，不管基底202是否為非單片式3D記憶體裝置的基底或為形成有非單片式3D記憶體裝置的BEOL互連線於其上的薄化基底，第2圖所繪示3D記憶體裝置200係為基底202(陣列元件基底)在y方向上設置於陣列元件下方的狀態。

【0037】　在一些實施例中，3D記憶體裝置200為NAND快閃記憶體裝置，其中記憶體單元係以垂直延伸於基底202上方的NAND串204的陣列的形式提供。陣列元件可包括複數個NAND串204，其垂直貫穿複數個導體層206與介電層208對。本文所指的複數個導體/介電層對也可稱為「導體/介電質交替堆疊」210。導體/介電質交替堆疊中導體/介電層對的數量(例如32、64或96個)可決定3D記憶體裝置200中記憶體單元的數量。導體/介電質交替堆疊210中的導體層206與介電層208係在垂直方向上交替配置。換句話說，除了導體/介電質交替堆疊210的最上層或最下層之外，各導體層206可在其兩側緊鄰兩介電層208，且各介電層208可在其兩側緊鄰兩導體層206。導體層206可具有相同的厚度或不同的厚度。同樣地，介電層208可具有相同的厚度或不同的厚度。導體層206可包括導體材料，其包括但不限於鎢(tungsten, W)、鈷(cobalt, Co)、銅(copper, Cu)、鋁(aluminum, Al)、多晶矽(polycrystalline silicon, polysilicon)、摻雜矽(doped silicon)、矽化物(silicide)或上述之任何組合。介電層208可包括介電材料，其包括但不限於氧化

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矽(silicon oxide)、氮化矽(silicon nitride)、氮氧化矽(silicon oxynitride)或上述之任何組合。在一些實施例中，導體層206包括金屬層，例如鎢，介電層包括氧化矽。

【0038】　如第2圖所示，導體/介電質交替堆疊210在橫向方向上的至少一側可包括一階梯結構212。各階梯結構212的各「階層」213可包括一或多個導體/介電層對，其中各導體/介電層對包括導體層206與介電層208。階梯結構212的各階層213中的頂層可為導體層206，用以在垂直方向上互連。在一些實施例中，階梯結構212的每兩相鄰階層213係以在垂直方向上名義相同的距離以及在橫向方向上名義相同的距離彼此錯開。針對階梯結構212的每兩相鄰階層213而言，較接近基底202的第一階層(其中有導體層與介電層)可較第二階層(其中有導體層與介電層)橫向延伸更多，藉此於第一階層上形成「平台區域」，以在垂直方向上達到互連。

【0039】　如第2圖所示，各NAND串204可包括延伸貫穿導體/介電質交替堆疊的一通道結構218。通道結構218可包括填有半導體材料(例如半導體通道220)以及介電材料(例如為記憶體薄膜222)的通道孔。在一些實施例中，半導體通道220包括矽，例如非晶矽(amorphous silicon)、多晶矽或單晶矽。在一些實施例中，記憶體薄膜222為複合層，其包括穿隧層、儲存層(也可理解為「電荷捕捉/儲存層」)以及阻擋層。各NAND串204可具有柱狀(例如圓柱形狀)。依據一些實施例，半導體通道220、穿隧層、儲存層與阻擋層係沿著從圓柱中心朝向圓柱外表面的方向依序排列。穿隧層可包括氧化矽、氮化矽或上述之任何組合。儲存層可包括氮化矽、氮氧化矽、矽或上述之任何組合。阻擋層可包括氧化矽、氮化矽、高介電常數(high-k)介電質或上述之任何組合。

【0040】　在一些實施例中，NAND串204包括對應NAND串204的複數個控制閘極(各控制閘極為字元線的一部分)。在導體/介電質交替堆疊中的導體層206可作為用於NAND串204的記憶體單元的控制閘極。導體層206可包括對應多個NAND

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串204的多個控制閘極，且導體層206可橫向延伸，並作為階梯結構212中的字元線端點。

【0041】　在一些實施例中，NAND串204包括一磊晶插塞224以及一蝕刻停止插塞226，且磊晶插塞224與蝕刻停止插塞226設置於NAND串204在垂直方向上相應的一端。磊晶插塞224與蝕刻停止插塞226中的每一個可與通道結構218相應的一端相接觸。磊晶插塞224可包括半導體材料，例如矽，磊晶插塞224係從基底202磊晶成長而成。磊晶插塞224可作為由NAND串204的源極選擇閘極控制的通道。蝕刻停止插塞226可設置於NAND串204的上端並與通道結構218相接觸(例如設置於通道結構218的上端)。當基底202設置於3D記憶體裝置200的最低平面時，本文所使用的元件(例如NAND串204)的「上端」係指在y方向上較遠離基底202的端點，而元件(例如NAND串204)的「下端」係指在y方向上較接近基底202的端點。

【0042】　蝕刻停止插塞226可包括半導體材料(例如多晶矽)或導體材料(例如金屬)。在一些實施例中，蝕刻停止插塞226包括填有鈦(Ti)/氮化鈦(TiN)(以鈦/氮化鈦作為阻障層)以及鎢(作為導體)的開口。透過在製作3D記憶體裝置200的過程中將蝕刻停止插塞226覆蓋通道結構218的上端，蝕刻停止插塞226可作為蝕刻停止層，以避免對填入通道結構218中的介電質蝕刻，其中介電質例如氧化矽與氮化矽。在一些實施例中，蝕刻停止插塞226作為NAND串204的汲極。

【0043】　在一些實施例中，陣列元件另包括複數個狹縫結構228。各狹縫結構228可垂直延伸貫穿導體/介電質交替堆疊210。狹縫結構228也可橫向延伸，以將導體/介電質交替堆疊210分隔成多個區塊。狹縫結構228可包括填有導體材料的狹縫，導體材料包括但不限於鎢、鈷、銅、鋁、矽化物或上述之任何組合。狹縫結構228可另包括設置於所填入的導體材料與導體/介電質交替堆疊210之間並具有任何適合的介電材料的介電層，以電性絕緣所填入的導體材料與導體/介電

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質交替堆疊210中環繞狹縫結構228的導體層206。因此，狹縫結構228可將3D記憶體裝置200分隔成多個記憶體區塊及/或指狀記憶體(例如如第1A圖至第1C圖所示的平面圖)。

【0044】 在一些實施例中，狹縫結構228作為對應共享相同的陣列共同源極(array common source)的相同記憶體區塊或相同指狀記憶體中的NAND串204的源極接觸。因此，狹縫結構228可稱為多個NAND串204的「共同源極接觸」。在一些實施例中，基底202包括摻雜區230(包括具有預期摻雜濃度的p型或n型摻質)，且狹縫結構228的下端與基底202的摻雜區230相接觸。狹縫結構228因此可透過摻雜區230電性連接至NAND串204。

【0045】 如第2圖所示，導體/介電質交替堆疊210可為交替堆疊層216的一部分，且交替堆疊層216亦可包括設置於基底202上的一介電質交替堆疊214。介電質交替堆疊214可包括複數個介電層對，例如第一介電層232與不同於第一介電層232的第二介電層234的交替堆疊。在一些實施例中，第一介電層232與第二介電層234中的每一個包括氮化矽與氧化矽。介電質交替堆疊214中的第一介電層232可與導體/介電質交替堆疊210中的介電層208相同。在一些實施例中，介電質交替堆疊214中的介電層對的數量與導體/介電質交替堆疊中的導體/介電層對的數量相同。

【0046】 在一些實施例中，3D記憶體裝置200包括一阻障結構235，垂直延伸並貫穿交替堆疊層216。阻障結構235可將交替堆疊層216橫向分隔成導體/介電質交替堆疊210與介電質交替堆疊214。也就是說，阻障結構235可為導體/介電質交替堆疊210與介電質交替堆疊214之間的邊界。介電質交替堆疊214可被至少阻障結構235橫向環繞。在一些實施例中，阻障結構235在平面圖上為一封閉形狀(例如矩形、正方形、圓形等)，以完全環繞介電質交替堆疊214。舉例來說，如第1A圖所示，阻障結構124在平面圖上為矩形，以完全環繞TAC區120中的介電質交替

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堆疊。在一些實施例中，阻障結構214在平面圖上並非封閉形狀，而是可與交替堆疊層216的一或多個邊緣結合以環繞介電質交替堆疊214。舉例來說，如第1B圖與第1C圖，阻障結構124與3D記憶體裝置的邊緣結合以環繞TAC區120中的介電質交替堆疊。

【0047】 如第2圖所示，3D記憶體裝置200另包括TAC 236，其中各TAC垂直延伸並貫穿介電質交替堆疊214。TAC 236可僅形成於被至少阻障結構235橫向環繞的區域中，此區域包括複數層介電層對。也就是說，TAC 236可垂直延伸並貫穿介電層(例如第一介電層232與第二介電層234)，但並未貫穿任何導電層(例如導電層206)。各TAC 236可延伸貫穿介電質交替堆疊214的整個厚度(例如貫穿在垂直方向上的所有介電層對)。在一些實施例中，TAC 236另延伸通過至少部分的基底202。

【0048】 TAC 236可搭配縮短的互連佈線傳輸從3D記憶體裝置200(例如部分電源匯流排)進出的電子訊號。在一些實施例中，TAC 236可在3D記憶體裝置200與周邊元件(例如設置於互補式金屬氧化物半導體(CMOS)晶片；圖未示)之間及/或在BEOL互連線(圖未示)與周邊元件之間提供電性連接。TAC 236亦可對交替堆疊層216提供機構上的支撐。各TAC 236可包括貫穿介電質交替堆疊的垂直開口，其中填有導體材料，導體材料包括但不限於鎢、鈷、銅、鋁、矽化物或上述之任何組合。在一些實施例中，為了絕緣的目的，當在介電質交替堆疊214中形成TAC 236(被介電層所環繞)時，TAC 236與介電質交替堆疊214之間並不需額外的介電層。

【0049】 在一些實施例中，3D記憶體裝置200包括與本文所揭露的各種記憶體陣列結構(例如NAND串204、狹縫結構228以及階梯結構212中的字元線206)相接觸的複數個局部接觸。本文的接觸在與記憶體陣列結構直接接觸時可稱為「局部接觸」。如第2圖所示，局部接觸可包括NAND串接觸238、狹縫結構接觸240

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以及字元線接觸242。在本揭露中，TAC 236亦可被稱為局部接觸。本文所使用的術語「接觸」可廣泛地包括任何形式的互連，其中互連方式包括垂直互連通道(例如通孔)以及橫向線路(例如互連線)。

【0050】 在一些實施例中，各局部接觸的一端(例如上端)係彼此齊平，例如與形成有局部接觸於其中的介電層的上表面齊平。各局部接觸的另一端(例如下端)可與相應的記憶體陣列結構相接觸。舉例來說，NAND串接觸238的下端可與NAND串204的蝕刻停止插塞226相接觸，且狹縫結構接觸240的下端可與狹縫結構228的上端相接觸。各字元線接觸242的下端可與設置於階梯結構212的相應一階層中的上導體層206(字元線)相接觸。各局部接觸可包括填有導體材料的開口(例如通孔或溝槽)，導體材料包括但不限於鎢、鈷、銅、鋁、矽化物或上述之任何組合。一些或所有的局部接觸可在下文詳細描述的單接觸形成製程中同時形成。

【0051】 如第2圖所示，3D記憶體裝置200除了局部接觸之外另包括一接觸層244以及作為其互連結構的一部分的一互連導體層246。接觸層244可包括介電層以及設置於介電層中的複數個接觸248(例如通孔)。互連導體層246可形成於接觸層244上，並包括介電層與設置於介電層中的複數個接觸250(例如互連線)。本文中的局部接觸、接觸層244中的接觸248以及互連導體層246中的接觸可共同稱為3D記憶體裝置200的互連結構。

【0052】 在一些實施例中，接觸層244中的各接觸248的一端(例如上端)彼此齊平，例如與形成有接觸248的介電層的上表面齊平；接觸層244的各接觸248的另一端(例如下端)彼此齊平，例如與形成有接觸248的介電層的下表面齊平。各接觸248的下端可與相應的一局部接觸的上端相接觸。各接觸248可包括填有導體材料的開口(例如通孔)，導體材料包括但不限於鎢、鈷、銅、鋁、矽化物或上述之任何組合。所有的接觸248可在下文詳細描述的單接觸形成製程中同時形成。

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【0053】　在一些實施例中，互連導體層246的各接觸250的一端(例如上端)彼此齊平，例如與形成有接觸250的介電層的上表面齊平；互連導體層246的各接觸的另一端彼此齊平，例如互連導體層246中的介電層的下表面。各接觸250的下端與相應的一接觸248的上端相接觸。各接觸250包括填有導體材料的開口(例如溝槽)，導體材料包括但不限於鎢、鈷、銅、鋁、矽化物或上述之任何組合。所有的接觸250可在下文詳細描述的單接觸形成製程中同時形成。

【0054】　在一些實施例中，互連導體層246中的接觸250包括複數條位元線252，其中位元線252分別透過對應的接觸248與NAND串接觸238電性連接至NAND串204，以單獨定位對應的NAND串204。接觸250可另包括電性連接至狹縫結構228(源極接觸)的源極線、電性連接至TAC 236的互連線以及電性連接至階梯結構212中的字元線206的互連線。可理解的是3D記憶體裝置200中的互連層的數量並不限於第2圖所示的範例。並且可形成具有接觸的額外互連層，以提供3D記憶體裝置200所需的互連結構。

【0055】　第3圖依據本案揭露的一些實施例所繪示的形成3D記憶體裝置的方法300範例流程圖。第4圖至第10圖依據本案揭露的一些實施例所繪示的形成3D記憶體裝置的製程範例示意圖。繪示第3圖至第10圖中的3D記憶體裝置的範例為繪示於第2圖中的3D記憶體裝置。應可理解的是，方法300所示的步驟並非全部，且所繪示的步驟之前、之後或之間亦可進行其他步驟。

【0056】　請參考第3圖，方法300從步驟302開始，其中介電質交替堆疊形成於基底上，基底可為矽基底。如第4圖所示，介電質交替堆疊214形成於基底202上。形成複數個第一介電層232與第二介電層234對於基底202上，以形成介電質交替堆疊214。在一些實施例中，各介電層對包括氮化矽層與氧化矽層。介電質交替堆疊214可透過一或多個薄膜沉積製程所形成，此一或多個薄膜沉積製程包括但不限於化學氣相沉積(CVD)、物理氣相沉積(PVD)、原子層沉積(ALD)或上述之

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任何組合。

【0057】　方法300進行步驟304，如第3圖所示，其中階梯結構形成於介電質交替堆疊中。在一些實施例中，可對介電質交替堆疊214的至少一側(在橫向方向上)進行修剪(trim)-蝕刻製程，以形成具有多個階層的階梯結構。各階層可包括具有第一介電層232與第二介電層234交替堆疊的一或多個介電層對。

【0058】　方法300進行步驟306，如第3圖所示，其中形成通道結構與阻障結構。通道結構與阻障結構的每一個可垂直延伸並貫穿介電質交替堆疊214。在一些實施例中，磊晶插塞224透過從基底202磊晶成長單晶矽而形成。通道結構218可形成於磊晶插塞224上。

【0059】　在一些實施例中，用於形成通道結構218的製程另包括透過例如濕蝕刻及/或乾蝕刻形成通道孔，其中通道孔垂直延伸並貫穿介電質交替堆疊214。在一些實施例中，用於形成通道結構218的製程另包括於介電質交替堆疊214中形成半導體通道220與設置於半導體通道220與介電層對之間的記憶體薄膜222。半導體通道220可包括半導體材料，例如多晶矽。記憶體薄膜222可為複合介電層，例如穿隧層、儲存層與阻擋層的組合。

【0060】　穿隧層可包括介電材料，其可包括但不限於氧化矽、氮化矽、氮氧化矽或上述之任何組合。半導體通道中的電子或電洞可通過穿隧層穿隧至儲存層中。儲存層可包括為了達到記憶功能而能儲存電荷的材料。儲存層的材料可包括但不限於氮化矽、氮氧化矽、氧化矽與氮化矽的組合或上述之任何組合。阻擋層可包括介電材料，其包括但不限於氧化矽或氧化矽/氮化矽/氧化矽(ONO)的組合。阻擋層可另包括high-k介電層(如氧化鋁(aluminum oxide)層)。半導體通道220與記憶體薄膜222可透過一或多個薄膜沉積製程所形成，此一或多個薄膜沉積製程例如為ALD、CVD、PVD、任何其他適合的製程或上述之任何組合。

【0061】　在一些實施例中，用於形成阻障結構235的製程與用於形成通道結構

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218的製程相似且同時進行，藉此可降低製程複雜度與製作成本。在形成貫穿介電質交替堆疊214的通道結構218的開口與阻障結構235的開口之後，可進行一或多個薄膜沉積製程，以同時填入通道結構218的開口與阻障結構235的開口中。因此，阻障結構235可包括一或多個填充通道結構218的材料，例如多晶矽、氧化矽、氮化矽以及high-k介電質。在一些實施例中，阻障結構235係填入氧化矽與氮化矽。可理解的是，在一些實施例中，通道結構218與阻障結構235係於不同的步驟中形成，使阻障結構235可填有與填入通道結構218的材料不同的材料。透過形成阻障結構235，介電質交替堆疊214可被分隔為兩個區域：被至少阻障結構235橫向環繞(在一些實施例中可與介電質交替堆疊的邊緣結合環繞)的一內部區域402以及形成有通道結構218的一外部區域404。

【0062】　在一些實施例中，同時形成虛置通道結構(未繪示於第4圖至第10圖中；例如第1A圖至第1B圖中所示的虛置通道結構122)與通道結構218。虛置通道結構可垂直延伸並貫穿交替堆疊層，且可填入與填至通道結構218中的材料相同的材料。不同於通道結構218，接觸並未形成於虛置通道結構上，使得接觸可提供與3D記憶體裝置的其他元件的電性連接。因此，虛置通道結構並不能用於形成3D記憶體裝置的記憶體單元。

【0063】　方法300進行步驟308，如第3圖所示，其中蝕刻停止層形成於通道結構上。如第5圖所示，於各通道結構218上形成一凹陷502。凹陷502可透過對通道結構218的介電層(例如氧化矽層)與上部分進行濕蝕刻及/或乾蝕刻而形成。如第6圖所示，透過使用一或多個薄膜沉積製程填入凹陷502中，以於通道結構218上形成蝕刻停止層226(在本文中稱為對應各通道結構218的「蝕刻停止插塞」)，其中此一或多個薄膜沉積製程例如為ALD、CVD、PVD、任何其他適合的製程或上述之任何組合。在一些實施例中，可沉積多晶矽，以填入凹陷502中，隨後進行化學機械研磨(CMP)製程，以移除多餘的多晶矽，並平坦化頂介電層的上表

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面。在一些實施例中，可沉積複合金屬層，例如鈦/氮化鈦/鎢，以填入凹陷502中，隨後進行CMP製程，以移除多餘的金屬層，並平坦化頂介電層的上表面。

【0064】　方法300進行步驟310，如第3圖所示，其中形成一狹縫，且透過此狹縫將介電質交替堆疊的一部分中的第一介電層取代為導體層。舉例來說，可先透過介電質(例如氧化矽與氮化矽)的濕蝕刻及/或乾蝕刻形成狹縫結構228的狹縫(如第7圖所示)，其貫穿外部區域404(如第6圖所示)中的介電質交替堆疊214。在一些實施例中，在形成狹縫之後，可透過例如離子佈植及/或熱擴散穿過狹縫於各狹縫下的基底202中形成摻雜區230。可理解的是，摻雜區230可形成於較早的製程階段，例如依據一些實施例，可早於形成狹縫的步驟。

【0065】　在一些實施例中，所形成的狹縫係用於閘極替換製程(也可稱為「字元線替換」製程)，閘極替換製程係將介電質交替堆疊214的外部區域404中的第二介電層234(如第6圖所示；例如氮化矽)取代為導體層206(如第7圖所示；例如鎢)。如第7圖所示，由於阻障結構235已形成，因此閘極替換只發生在介電質交替堆疊214的外部區域404中，而非內部區域402中。並且，因為阻障結構235填有無法被閘極替換製程所蝕刻的材料，故阻障結構235可避免第二介電層234的蝕刻進入介電質交替堆疊214的內部區域402中。因此，於閘極替換製程之後，第1圖至第6圖中所示的介電質交替堆疊214可成為包含有設置於外部區域404中的導體/介電質交替堆疊210與設置於內部區域402中的介電質交替堆疊214的交替堆疊層216。將第二介電層234取代為導體層206的替換步驟可包括選擇性地對第二介電層234(例如氮化矽)進行濕蝕刻，而非對第一介電層232(例如氧化矽)蝕刻，然後將導體層206(例如鎢)填入此結構中。導體層206可透過PVD、CVD、ALD、任何其他適合的製程或上述之任何組合。導體層206可包括導體材料，其包括但不限於鎢、鈷、銅、鋁、多晶矽、矽化物或上述之任何組合。在閘極替換之後，可形成NAND串204，其中各NAND串204可包括通道結構218、磊晶插

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塞224、蝕刻停止插塞226以及多個控制閘極與多個選擇閘極(例如環繞導體層206)。

【0066】 方法300進行步驟312，如第3圖所示，其中形成狹縫結構。如第7圖所示，狹縫結構228可透過將導體材料填入(例如沉積)狹縫所形成，填入導體材料的方法可利用PVD、CVD、ALD、任何其他適合的製程或上述之任何組合。狹縫結構228可包括導體材料，其包括但不限於鎢、鈷、銅、鋁、多晶矽、矽化物或上述之任何組合。在一些實施例中，為了絕緣的目的，可於狹縫結構228的導體材料與導體/介電質交替堆疊210中環繞狹縫結構228的導體層206之間先形成介電層(例如氧化矽層)。狹縫結構228的下端可與摻雜區230相接觸。在一些實施例中，狹縫結構228可作為源極接觸，其透過基底202的摻雜區230電連接至NAND串204。如第7圖所示，依據一些實施例，各狹縫結構228的上端係與各蝕刻停止插塞226的上端齊平(例如與形成有蝕刻停止插塞226與狹縫結構228的介電層的上表面齊平)。

【0067】 方法300進行步驟314，如第3圖所示，其中形成複數個第一接觸(例如局部接觸)。如第8圖所示，介電層802可透過一或多個薄膜沉積製程形成，此一或多個薄膜沉積製程例如為ALD、CVD、PVD、任何其他適合的製程或上述之任何組合。介電層802可包括介電材料，其包括但不限於氧化矽、氮化矽、氮氧化矽或上述之任何組合。局部接觸(包括NAND串接觸238、狹縫結構接觸240與上字元線接觸242-1)係形成至貫穿介電層802，其形成方法可包括形成第一蝕刻垂直開口(例如透過濕蝕刻及/或乾蝕刻)，然後利用ALD、CVD、PVD、任何其他適合的製程或上述之任何組合將導電材料填入開口中。用於填入局部接觸的導體材料包括但不限於鎢、鈷、銅、鋁、多晶矽、矽化物或上述之任何組合。在一些實施例中，也可用其他導體材料填入開口中，以作為阻障層、黏著層、及/或晶種層。蝕刻介電層以形成局部接觸的開口的方法可透過蝕刻停止在不同

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的材料來控制。舉例來說，針對NAND串接觸238而言，填有半導體及/或金屬材料的蝕刻停止層226可避免進一步對通道結構蝕刻。關於狹縫結構接觸240與上字元線接觸242-1，介電層的蝕刻可在達到狹縫結構228的上端與字元線206的上端停止。

【0068】　如第8圖所示，NAND串接觸238、狹縫結構接觸240以及一或多個上字元線接觸242-1係靠近介電層802的上表面(也就是相較於其他字元線接觸242而言具有較小的長度)。NAND串接觸238的下端可與蝕刻停止插塞226的上端相接觸，且狹縫結構接觸240的下端可與狹縫結構228的上端相接觸。第8圖亦繪示出在閘極替換之後在各階層中具有導體層206的階梯結構212。各上字元線接觸242-1的下端可與設置於階梯結構212的一階層中對應的導體層206(字元線)相接觸。

【0069】　局部接觸(包括NAND串接觸238、狹縫結構接觸240以及上字元線接觸242-1)可於相同的接觸形成製程中同時形成。可理解的是，接觸形成製程可包括多個製程，例如微影(photolithography)、蝕刻、薄膜沉積以及CMP。在一些實施例中，在接觸形成製程中的每一個製程可僅需針對所有的NAND串接觸238、狹縫結構接觸240與上字元線接觸242-1進行一次。舉例來說，可進行單一顯影製程，以圖案化用於所有的NAND串接觸238、狹縫結構接觸240與上字元線接觸242-1的遮罩；然後，可進行單一蝕刻製程，以蝕刻所有NAND串接觸238、狹縫結構接觸240與上字元線接觸242-1的開口；接著，可進行單一沉積製程，以將相同的導體材料填入所有NAND串接觸238、狹縫結構接觸240與上字元線接觸242-1的開口。

【0070】　如第9圖所示，在一些實施例中，在形成局部接觸的第一組合(包括如第8圖所示的NAND串接觸238、狹縫結構接觸240以及上字元線接觸242-1)之後，可形成局部接觸的第二組合，其包括TAC 236與接近基底202的下字元線接

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觸242-2(也就是，相較於上字元線接觸242-1，下字元線接觸242-1具有較長的長度)。TAC 236與下字元線接觸242-2可形成至貫穿介電層802，其形成方法可包括形成第一蝕刻垂直開口(例如透過濕蝕刻及/或乾蝕刻)，然後利用ALD、CVD、PVD、任何其他適合的製程或上述之任何組合將導電材料填入開口中。用於填入局部接觸的導體材料包括但不限於鎢、鈷、銅、鋁、多晶矽、矽化物或上述之任何組合。在一些實施例中，也可用其他導體材料填入開口中，以作為阻障層、黏著層、及/或晶種層。

【0071】 TAC 236可透過蝕穿介電質交替堆疊214形成。由於介電質交替堆疊214包括介電質層的交替堆疊，其中介電質例如為氧化矽與氮化矽，因此TAC 236的開口可透過介電材料的深蝕刻所形成(例如透過深反應性離子蝕刻(deep reactive-ion etching(DRIE)製程或其他適合的非等向性蝕刻製程)。在一些實施例中，雖然TAC 236係形成於閘極替換之後，但透過在保留不被閘極替換製程影響的介電質交替堆疊214的區域(不轉換為導體/介電質堆疊210的區域)的情況下，形成貫穿介電層的TAC 236(不貫穿任何導體層)可簡化製程並降低成本。再者，由於在閘極替換之後可相對更容易形成TAC 236，因此TAC 236可與一些或所有其他局部接觸在相同的接觸形成製程中形成，以進一步降低製程複雜度與製作成本。

【0072】 在一些實施例中，TAC 236的下端可與基底202相接觸。如第9圖所示，TAC 236可延伸並進一步通過至少一部分的基底202。各下字元線接觸242-2的下端可與階梯結構212的一階層中的對應的導體層206(字元線)相接觸。所有局部接觸(包括形成在第8圖與第9圖中的局部接觸的第一與第二組合的兩個組合)的上端可彼此齊平，並設置於介電層802的上表面。局部接觸的第二組合(包括TAC 236與下字元線接觸242-2)可在局部接觸的第一組合形成之後於相同的接觸形成製程中同時形成。也就是說，所有的局部接觸(包括局部接觸的第一與第二

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組合的兩個組合)可於第8圖與第9圖所示的兩個接觸形成製程中形成。

【0073】 可理解的是，在一些實施例中，所有的局部接觸(包括局部接觸的第一與第二組合的兩個組合)可於單一接觸形成製程中同時形成。也就是說，如第8圖與第9圖所示的兩接觸形成製程可結合為單一接觸形成製程。在一些實施例中，在接觸形成製程中的每一個製程需對所有的NAND串接觸238、狹縫結構接觸240、TAC 236、上字元線接觸242-1與下字元線接觸242-2進行一次。舉例來說，可進行單一顯影製程，以圖案化用於所有的NAND串接觸238、狹縫結構接觸240、TAC 236以及上字元線接觸242-1與下字元線接觸242-2的遮罩；然後，可進行單一蝕刻製程，以蝕刻所有NAND串接觸238、狹縫結構接觸240、TAC 236以及上字元線接觸242-1與下字元線接觸242-2的開口；接著，可進行單一沉積製程，以將相同的導體材料填入所有NAND串接觸238、狹縫結構接觸240、TAC 236以及上字元線接觸242-1與下字元線接觸242-2的開口。

【0074】 方法300進行步驟316，如第3圖所示，其中形成複數個第二接觸於接觸層中。如第10圖所示，接觸層244(包括介電層1002與接觸248)形成於介電層802之上。各接觸248的上端可彼此齊平，並設置於介電層1002的下表面。介電層1002可透過一或多個薄膜製程形成，其中一或多個薄膜製程例如為ALD、CVD、PVD、任何其他適合的製程或上述之任何組合。介電層1002可包括介電材料，其包括但不限於氧化矽、氮化矽、氮氧化矽或上述之任何組合。接觸248可形成至貫穿介電層1002，其形成的方法可包括形成第一蝕刻垂直開口(例如透過濕蝕刻及/或乾蝕刻)，然後利用ALD、CVD、PVD、任何其他適合的製程或上述之任何組合將導電材料填入開口中。用於填入接觸248的導體材料包括但不限於鎢、鈷、銅、鋁、多晶矽、矽化物或上述之任何組合。在一些實施例中，也可用其他導體材料填入開口中，以作為阻障層、黏著層、及/或晶種層。

【0075】 如第10圖所示，各接觸248的下端可與對應的局部接觸的上端相接

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觸，例如與NAND串接觸238、狹縫結構接觸240、TAC 236或字元線接觸242相接觸。在一些實施例中，所有在接觸層244中的接觸248可在相同的接觸形成製程中同時形成。在一些實施例中，各接觸248為一通孔，且接觸層244可稱為3D記憶體裝置200的互連結構的第「V0」階層。

【0076】 方法300進行步驟318，如第3圖所示，其中形成複數個第三接觸於互連導體層中。如第10圖所示，互連導體層246(包括介電層1004與接觸250)形成於接觸層244之上。各接觸250的上端可彼此齊平，並設置於介電層1004的上表面。介電層1004可透過一或多個薄膜沉積製程所形成，此一或多個薄膜沉積製程例如為ALD、CVD、PVD、任何其他適合的製程或上述之任何組合。介電層1004可包括介電材料，其包括但不限於氧化矽、氮化矽、氮氧化矽或上述之任何組合。接觸250可形成貫穿介電層1004，其形成方法可包括形成第一蝕刻垂直開口(例如透過濕蝕刻及/或乾蝕刻)，然後利用ALD、CVD、PVD、任何其他適合的製程或上述之任何組合將導電材料填入開口中。用於填入接觸248的導體材料包括但不限於鎢、鈷、銅、鋁、多晶矽、矽化物或上述之任何組合。在一些實施例中，也可用其他導體材料填入開口中，以作為阻障層、黏著層、及/或晶種層。

【0077】 如第10圖所示，各接觸250的下端可與接觸層244中對應的接觸248的上端相接觸，使得各接觸250可電性連接至對應的記憶體陣列結構，例如NAND串204、狹縫結構228、基底202以及字元線206。在一些實施例中，所有在互連導體層246中的接觸250可在相同的接觸形成製程中同時形成。在一些實施例中，各接觸250為一互連線，且互連導體層246可稱為3D記憶體裝置200的互連結構的第「M0」階層。可理解的是，在一些實施例中，接觸248與接觸250係於單一接觸形成製程中形成，單一接觸形成製成可例如為用於形成銅接觸的雙鑲嵌(dual damascene)製程。然而，如第8圖與第9圖所示，包含有局部接觸與接觸248以及接觸250的互連結構可在有限數量的製程步驟中形成，以降低製程複雜度與

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製作成本。

【0078】　第11圖依據本案揭露的一些實施例所繪示的形成3D記憶體裝置的方法範例流程圖。第11圖中所描述的3D記憶體裝置的範例為第2圖所繪示的3D記憶體裝置200。可理解的是，方法1100所示的步驟並非全部，且所繪示的步驟之前、之後或之間亦可進行其他步驟。

【0079】　請參考第11圖，方法1100從步驟1102開始，其中形成導體/介電質交替堆疊。導體/介電質交替堆疊可包括階梯結構。方法1100進行步驟1104，其中形成一NAND串與一狹縫結構。NAND串與狹縫結構中的每一個可垂直延伸並貫穿導體/介電質交替堆疊。方法1100進行步驟1106，其中形成複數個第一接觸(例如局部接觸)，且各第一接觸的相應一第一端彼此齊平。階梯結構中的導體/介電質交替堆疊的一第一導體層、NAND串以及狹縫結構中的每一個與第一接觸的相應一第二端相接觸。方法1100進行步驟1108，其中形成包含有複數個第二接觸的接觸層。各第二接觸的第一端可彼此齊平，且各第二接觸的相應第二端可彼此齊平。各第二接觸可與第一接觸中的相應一個相接觸。方法1100進行步驟1110，其中形成包含有複數個互連線(例如位元線)的互連導體層。各第二接觸可與互連線中之相應一個相接觸。

【0080】　第12圖依據本案揭露的一些實施例所繪示的形成3D記憶體裝置的另一方法範例流程圖。第12圖中所描述的3D記憶體裝置的範例為第2圖所繪示的3D記憶體裝置200。可理解的是，方法1200所示的步驟並非全部，且所繪示的步驟之前、之後或之間亦可進行其他步驟。

【0081】　請參考第12圖，方法1200從步驟1202開始，其中形成一交替堆疊層於基底上。方法1200進行步驟1204，其中形成一阻障結構。阻障結構可垂直延伸並貫穿交替堆疊層，使得交替堆疊層被橫向分隔成包括複數個介電層對的介電質交替堆疊以及包括複數個導體/介電層對的導體/介電質交替堆疊。方法1200

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進行步驟1206，其中形成NAND串。NAND串可垂直延伸並貫穿導體/介電質交替堆疊。方法1200進行步驟1208，其中形成一第一接觸。第一接觸可包括兩端，其中一端與NAND串相接觸。方法1200進行步驟1210，其中形成一TAC。TAC可垂直延伸並貫穿介電質交替堆疊。並且，TAC可包括一端與第一接觸的一端齊平。

【0082】　依據本揭露的各種實施例提供一種具有作為記憶體陣列的互連結構的3D記憶體裝置。互連結構可使各種記憶體陣列結構(例如NAND串、閘極線狹縫、字元線等)之間具有接觸，這些接觸是在有限數量的步驟中(例如在一個步驟或兩個步驟中)所形成，藉此可降低製程複雜度與製作成本。在一些實施例中，本文所揭露的互連結構包括設置於上互連導體層中的位元線，此互連結構適用於3D記憶體架構，且此3D記憶體架構中設置於不同基底上的陣列元件與周邊元件係透過面對面混和接合的方式彼此連結。

【0083】　再者，本所所揭露的互連結構可包括用於在堆疊陣列元件與周邊元件之間提供垂直互連(例如用於電源匯流排與金屬佈線)的TAC，藉此可降低金屬階層與縮小晶粒尺寸。在一些實施例中，本所所揭露的設置於互連結構中的TAC係形成至貫穿介電層的交替堆疊，相較於導體與介電層的交替堆疊而言，介電層的交替堆疊可更容易被蝕穿而形成穿孔。

【0084】　在一些實施例中，NAND記憶體裝置包括基底、設置於基底上並包括階梯結構的交替堆疊層，以及垂直貫穿交替堆疊層的阻障結構。交替堆疊層包括介電質交替堆疊以及導體/介電質交替堆疊，介電質交替堆疊包括被至少阻障結構橫向環繞的複數個介電層對，且導體/介電質交替堆疊包括複數個導體/介電層對。記憶體裝置另包括一通道結構、一狹縫結構、一蝕刻停止層以及複數個第一接觸，通道結構以及狹縫結構中之每一個垂直延伸並貫穿導體/介電質交替堆疊，且蝕刻停止層設置於通道結構的一端上。階梯結構上的一導電層、蝕刻停止層以及狹縫結構中的每一個與第一接觸中的相應一個相接觸。

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【0085】　在一些實施例中，3D記憶體裝置包括一基底、一導體/介電質交替堆疊、一NAND串、一狹縫結構以及複數個第一接觸，其中導體/介電質交替堆疊設置於基底上，並包括一階梯結構，NAND串與狹縫結構中的每一個垂直延伸並貫穿導體/介電質交替堆疊，第一接觸的相應第一端彼此齊平。階梯結構中的導體/介電質交替堆疊的一導體層、NAND串以及狹縫結構中的每一個與第一接觸中相應的一第二端相接觸。

【0086】　在一些實施例中，3D記憶體裝置包括一基底、一交替堆疊層以及一阻障結構，其中交替堆疊層設置於基底上，且阻障結構垂直延伸並貫穿交替堆疊層。阻障結構橫向將交替堆疊層分隔成包括複數個介電層對的介電質交替堆疊以及包括複數個導體/介電層對的導體/介電質交替堆疊。記憶體裝置另包括垂直延伸並貫穿導體/介電質交替堆疊的NAND串、垂直延伸並貫穿介電質交替堆疊的TAC以及第一接觸，其中第一接觸包括與TAC第一端齊平的第一端以及與NAND串相接觸的第二端。

【0087】　在一些實施例中，形成NAND記憶體裝置的方法揭露如下。於一基底上形成一介電質交替堆疊。介電質交替堆疊包括複數個介電層對，各介電層對包括一第一介電層與不同於第一介電層的一第二介電層。於介電質交替堆疊中形成一第一階梯結構。形成一通道結構以及一阻障結構，其中通道結構與阻障結構中的每一個垂直延伸並貫穿介電質交替堆疊。阻障結構將介電質交替堆疊分隔出一第一部分與一第二部分，第一部分被至少阻障結構橫向環繞，且第二部分包括第一階梯結構。於通道結構的一上端形成一蝕刻停止層。形成一狹縫。透過狹縫將設置於介電質交替堆疊的第二部分中的第一介電層取代為複數個導體層，以形成一導體/介電質交替堆疊，且該導體/介電質交替堆疊包括複數個導體/介電層對。透過於狹縫中沉積一導體，以形成一狹縫結構。形成複數個第一接觸。設置於階梯結構中的導體/介電質交替堆疊的一第一導體層、蝕刻停

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止層以及狹縫結構中的每一個與第一接觸中的一個相接觸。

【0088】　在一些實施例中，形成3D記憶體裝置的方法揭露如下。形成包括一階梯結構的一導體/介電質交替堆疊。形成一NAND串與一狹縫結構，其中NAND串與狹縫結構中的每一個垂直延伸並貫穿導體/介電質交替堆疊。形成複數個第一接觸，其中第一接觸的相應第一端彼此齊平。階梯結構中的導體/介電質交替堆疊的一第一導體層、NAND串以及狹縫結構中的每一個與第一接觸中相應的一第二端相接觸。

【0089】　在一些實施例中，形成NAND記憶體裝置的方法揭露如下。於一基底上形成一交替堆疊層。形成垂直延伸並貫穿交替堆疊層的一阻障結構，使交替堆疊層被橫向分隔成包括複數個介電層對的介電質交替堆疊以及包括複數個導體/介電層對的導體/介電質交替堆疊。形成包括垂直延伸並貫穿導體/介電質交替堆疊的NAND串。形成包括第一端以及與NAND串相接觸的第二端的一第一接觸。形成垂直延伸並貫穿介電質交替堆疊的TAC。TAC包括與第一接觸的第一端齊平的第一端。

【0090】　以上對具體實施例的描述將充分揭示本揭露內容的一般性質，其他人可以通過應用相關領域技術範圍內的知識，輕易地將特定實施例調整及/或修改於各種應用，而無需過度實驗與背離本揭露內容的一般概念。因此，基於這裡給出的教導及指導，這樣的修改及調整仍應屬於本揭露的實施例的均等意涵及範圍內。應該理解的是，本文中的措辭或術語是為了描述的目的而非限制的目的，使得本說明書的術語或措辭將由相關領域技術人員根據教導及指導來解釋。

【0091】　以上本揭露的實施例已借助於功能構建塊來描述，該功能構建塊示出了特定功能及其關係的實現。為了描述的方便，這些功能構建塊的邊界/範圍在本文中係被任意的定義，在適當地實現所指定的功能及關係時，可以定義出

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替代邊界/範圍。

【0092】　發明內容及摘要部分可以闡述出發明人所設想的本揭露的一個或多個的示範性實施例，但並非全部的示範性實施例，並且因此不旨在以任何方式限制本揭露內容及所附權利要求範圍。

【0093】　本揭露的廣度及範圍不應受上述任何示範性實施例所限制，而應僅根據以下權利要求及其均等物來限定。

【符號說明】

【0094】

102	字元線貫穿陣列接觸(TAC)區
104	位元線TAC區
106	階梯TAC區
110	NAND串區
120	TAC區
130	頂選擇閘極(TSG)階梯區
112	反及(NAND)串
114	狹縫結構
132	TSG接觸
122	虛置通道結構
124	阻障結構
126、236	TAC
140	階梯區
142	字元線接觸
200	3D記憶體裝置

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202	基底
204	NAND串
206	導體層
208、802、1002、1004	介電層
210	導體/介電質交替堆疊
212	階梯結構
213	階層
214	介電質交替堆疊
216	交替堆疊層
218	通道結構
220	半導體通道
222	記憶體薄膜
224	磊晶插塞
226	蝕刻停止插塞
228	狹縫結構
230	摻雜區
232	第一介電層
234	第二介電層
235	阻障結構
238	NAND串接觸
240	狹縫結構接觸
242	字元線接觸
242-1	上字元線接觸
242-2	下字元線接觸

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244	接觸層
246	互連導體層
248、250	接觸
252	位元線
402	內部區域
404	外部區域
502	凹陷
300、1100、1200	方法
302、304、306、308、310、312、314、316、318、1102、1104、1106、1108、1202、1204、1206、1208、1210	步驟

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【發明摘要】

【中文發明名稱】　三維記憶體裝置的互連結構

【英文發明名稱】　INTERCONNECT STRUCTURE OF THREE-DIMENSIONAL MEMORY DEVICE

【中文】

本發明揭露三維(3D)記憶體裝置的互連結構及其製作方法之實施例。在一實例中，3D反及(NAND)記憶體裝置包括基底、設置於基底上並包括階梯結構的交替堆疊層以及垂直延伸並貫穿交替堆疊層的阻障結構。交替堆疊層包括介電質交替堆疊以及導體/介電質交替堆疊。介電質交替堆疊包括被至少阻障結構環繞的介電層對。導體/介電質交替堆疊包括複數個導體/介電層對。記憶體裝置另包括通道結構、狹縫結構、蝕刻停止層以及複數個第一接觸，通道結構與狹縫結構中的每一個垂直延伸並貫穿導體/介電質交替堆疊，且蝕刻停止層設置於通道結構的一端上。

【英文】

Embodiments of interconnect structures of a three-dimensional (3D) memory device and method for forming the interconnect structures are disclosed. In an example, a 3D NAND memory device includes a substrate, an alternating layer stack including a staircase structure on the substrate, and a barrier structure extending vertically through the alternating layer stack. The alternating layer stack includes an alternating dielectric stack and an alternating conductor/dielectric stack. The alternating dielectric stack includes dielectric layer pairs enclosed by at least the barrier structure. The alternating conductor/dielectric stack includes

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conductor/dielectric layer pairs. The memory device further includes a channel structure and a slit structure each extending vertically through the alternating conductor/dielectric stack, an etch stop layer on an end of the channel structure, and first contacts.

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【指定代表圖】第（ 10 ）圖。

【代表圖之符號簡單說明】

802、1002、1004	介電層
244	接觸層
246	互連導體層
248、250	接觸

【特徵化學式】

無

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【發明申請專利範圍】

【第1項】 一種三維(3D)反及(NAND)記憶體裝置，包括：

一基底；

一交替堆疊層(alternating layer stack)，設置於該基底上，該交替堆疊層包括一階梯結構(staircase structure)；

一阻障結構，垂直延伸並貫穿該交替堆疊層，其中該交替堆疊層包括(i)一介電質交替堆疊以及(ii)一導體/介電質交替堆疊，其中該介電質交替堆疊包括被至少該阻障結構橫向環繞的複數個介電層對，且該導體/介電質交替堆疊包括複數個導體/介電層對；

一通道結構以及一狹縫結構，該通道結構與該狹縫結構中的每一個垂直延伸並貫穿該導體/介電質交替堆疊；

一蝕刻停止層，設置於該通道結構的一端上；以及

複數個第一接觸，其中(i)設置於該階梯結構中的該導體/介電質交替堆疊的一導體層、(ii)該蝕刻停止層以及(iii)該狹縫結構中的每一個與該等第一接觸中的一個相接觸。

【第2項】 如請求項1所述的記憶體裝置，其中該蝕刻停止層包括多晶矽、鈦、氮化鈦(titanium nitride)以及鎢中之一個或多個。

【第3項】如請求項1所述的記憶體裝置，其中該阻障結構包括氧化矽與氮化矽。

【第4項】 如請求項1所述的記憶體裝置，另包括一虛置通道結構，垂直延伸並貫穿該導體/介電質交替堆疊。

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【第5項】 如請求項1所述的記憶體裝置，其中各該介電層對包括一氧化矽層以及一氮化矽層，且各該導體/介電層對包括一金屬層以及一氧化矽層。

【第6項】 如請求項1所述的記憶體裝置，另包括一互連導體層以及一接觸層，該接觸層包括複數個第二接觸，其中(i)設置於該階梯結構中的該導體/介電質交替堆疊的該導電層、(ii)該通道結構以及(iii)該狹縫結構中的每一個透過對應的一第一接觸以及該等第二接觸中的相應一個電性連接至該互連導體層。

【第7項】 如請求項1所述的記憶體裝置，另包括一第三接觸，垂直延伸並貫穿被至少該阻障結構橫向環繞的該介電質交替堆疊。

【第8項】 一種形成3D NAND記憶體裝置的方法，包括：

於一基底上形成一介電質交替堆疊，其中該介電質交替堆疊包括複數個介電層對，各該介電層對包括一第一介電層與不同於該第一介電層的一第二介電層；

於該介電質交替堆疊中形成一第一階梯結構；

形成一通道結構以及一阻障結構，該通道結構與該阻障結構中的每一個垂直延伸並貫穿該介電質交替堆疊，其中該阻障結構將該介電質交替堆疊分隔出一第一部分與一第二部分，該第一部分被至少該阻障結構橫向環繞，且該第二部分包括該第一階梯結構；

於該通道結構的一上端上形成一蝕刻停止層；

形成一狹縫，並透過該狹縫將設置於該介電質交替堆疊的該第二部分中的該等第一介電層取代為複數個導體層，以形成一導體/介電質交替堆疊，且該導體/介電質交替堆疊包括複數個導體/介電層對；

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透過於該狹縫中沉積一導體，以形成一狹縫結構；以及

形成複數個第一接觸，其中(i)設置於該第一階梯結構中的該導體/介電質交替堆疊的一第一導體層、(ii)該蝕刻停止層以及(iii)該狹縫結構中的每一個與該等第一接觸中的一個相接觸。

【第9項】 如請求項8所述的方法，另包括形成複數個第二接觸，其中該等第二接觸中之一個垂直延伸並貫穿該介電質交替堆疊由至少該阻障結構橫向環繞的該第一部分，且該等第二接觸中之另一個與該第一階梯結構中的該導體/介電質交替堆疊的一第二導體層相接觸。

【第10項】 如請求項9所述的方法，另包括形成一接觸層以及一互連導體層，該接觸層包括複數個第三接觸，且該互連導體層設置於該接觸層上，其中(i)設置於該第一階梯結構中的該導體/介電質交替堆疊的該第一導電層、(ii)該通道結構以及(iii)該狹縫結構中的每一個透過對應的一第一接觸以及該等第二接觸中的相應一個電性連接至該互連導體層。

【第11項】 如請求項8所述的方法，另包括在形成一狹縫之前，於該基底中形成一摻雜區，其中該狹縫結構與該摻雜區相接觸。

【第12項】 如請求項8所述的方法，另包括於相鄰於該阻障結構的該介電質交替堆疊中形成一第二階梯結構。

【第13項】 一種3D記憶體裝置，包括：

一基底；

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一導體/介電質交替堆疊，設置於該基底上，且該導體/介電質交替堆疊包括一階梯結構；

一NAND串與一狹縫結構，該NAND串與該狹縫結構中的每一個垂直延伸並貫穿該導體/介電質交替堆疊；以及

複數個第一接觸，該等第一接觸的相應第一端彼此齊平，其中(i)該階梯結構中的該導體/介電質交替堆疊的一導體層、(ii)該NAND串以及(iii)該狹縫結構中的每一個與該等第一接觸的相應第二端相接觸。

【第14項】 如請求項13所述的記憶體裝置，另包括一接觸層，該接觸層包括複數個第二接觸，該等第二接觸的相應第一端彼此齊平，該等第二接觸的相應第二端彼此齊平，其中各該第二接觸與該等第一接觸中的相應一個相接觸。

【第15項】 如請求項14所述的記憶體裝置，另包括一互連導體層，該互連導體層包括複數條互連線，其中各該第二接觸與該等互連線中的相應一個相接觸。

【第16項】 如請求項15所述的記憶體裝置，其中該等互連線包括一位元線，且該位元線透過對應的一第一接觸與對應的一第二接觸電連接至該NAND串。

【第17項】 如請求項13所述的記憶體裝置，另包括：

一阻障結構；以及

一介電質交替堆疊，透過該阻障結構與該導體/介電質交替堆疊橫向分隔。

【第18項】 如請求項17所述的記憶體裝置，其中該等第一接觸包括一貫穿陣列

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接觸(through array contact，TAC)，且該貫穿陣列接觸垂直延伸並貫穿該介電質交替堆疊。

【第19項】 如請求項13所述的記憶體裝置，其中該NAND串包括一插塞，且該插塞與對應的一第一接觸相接觸。

【第20項】 如請求項19所述的記憶體裝置，其中該插塞包括多晶矽與金屬中的至少一個。

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Espacenet

TW201539724A Semiconductor memory device and method for manufacturing same

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IPC ***H01L27/115;***

CPC **G11C16/0408G11C16/0483H01L23/528H01L27/11519H01L27/11556H01L27/11582H01L29/0649H01L29/66825H01L29/7926 (US); (US); (US); (US); (EP,CN,US); (US); (US); (EP,CN,US); (EP,CN,US);**

Application number: TW104100803A
Priority numbers: JP2014003793A 2014-01-10; JP2015000044W 2015-01-07
Publication date: 2015-10-16
Filing date: 2015-01-09
Priority date: 2014-01-10
Published as: **CN104779253A; CN104779253B; CN106165098A; JP2017010951A;** TW201539724A;**TWI599022B; TW201803030A; US2015200199A1; US2016322373A1; US10242992B2; US2019181150A1**

Abstract: Semiconductor memory device and method for manufacturing same

According to one embodiment, a semiconductor memory device includes a substrate, a semiconductor pillar provided on the substrate to extend in a vertical direction, a plurality of first electrode films provided sideward of the semiconductor pillar to extend in a first direction. The plurality of first electrode films are disposed to be separated from each other along the vertical direction. The semiconductor memory device further includes a plurality of second electrode films provided between the semiconductor pillar and the first electrode films. The plurality of second electrode films are disposed to be separated from each other along the vertical direction. The semiconductor memory device further includes a first insulating film provided between the semiconductor pillar and the second electrode films, and a second insulating film provided between the second electrode film and the first electrode film.

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201539724

(19)中華民國智慧財產局

(12)發明說明書公開本 (11)公開編號：TW 201539724 A

(43)公開日： 中華民國 104 (2015) 年 10 月 16 日

(21)申請案號：104100803 (22)申請日： 中華民國 104 (2015) 年 01 月 09 日

(51)Int. Cl.： *H01L27/115 (2006.01)*

(30)優先權：2014/01/10 日本 2014-003793

2015/01/07 世界智慧財產權組織 PCT/JP2015/000044

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申請實體審查：有 申請專利範圍項數：22 項 圖式數：69 共 118 頁

(54)名稱

半導體記憶體裝置及其製造方法

SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

(57)摘要

根據一項實施例，一種半導體記憶體裝置包括：一基板；一半導體支柱，其提供於該基板上以在一垂直方向上延伸；複數個第一電極膜，其提供於該半導體支柱側方以在一第一方向上延伸。該複數個第一電極膜經安置為沿著該垂直方向彼此分離。該半導體記憶體裝置進一步包括提供於該半導體支柱與該等第一電極膜之間的複數個第二電極膜。該複數個第二電極膜經安置為沿著該垂直方向彼此分離。該半導體記憶體裝置進一步包括：提供於該半導體支柱與該等第二電極膜之間的一第一絕緣膜；及提供於該第二電極膜與該第一電極膜之間的一第二絕緣膜。

According to one embodiment, a semiconductor memory device includes a substrate, a semiconductor pillar provided on the substrate to extend in a vertical direction, a plurality of first electrode films provided sideward of the semiconductor pillar to extend in a first direction. The plurality of first electrode films are disposed to be separated from each other along the vertical direction. The semiconductor memory device further includes a plurality of second electrode films provided between the semiconductor pillar and the first electrode films. The plurality of second electrode films are disposed to be separated from each other along the vertical direction. The semiconductor memory device further includes a first insulating film provided between the semiconductor pillar and the second electrode films, and a second insulating film provided between the second electrode film and the first electrode film.

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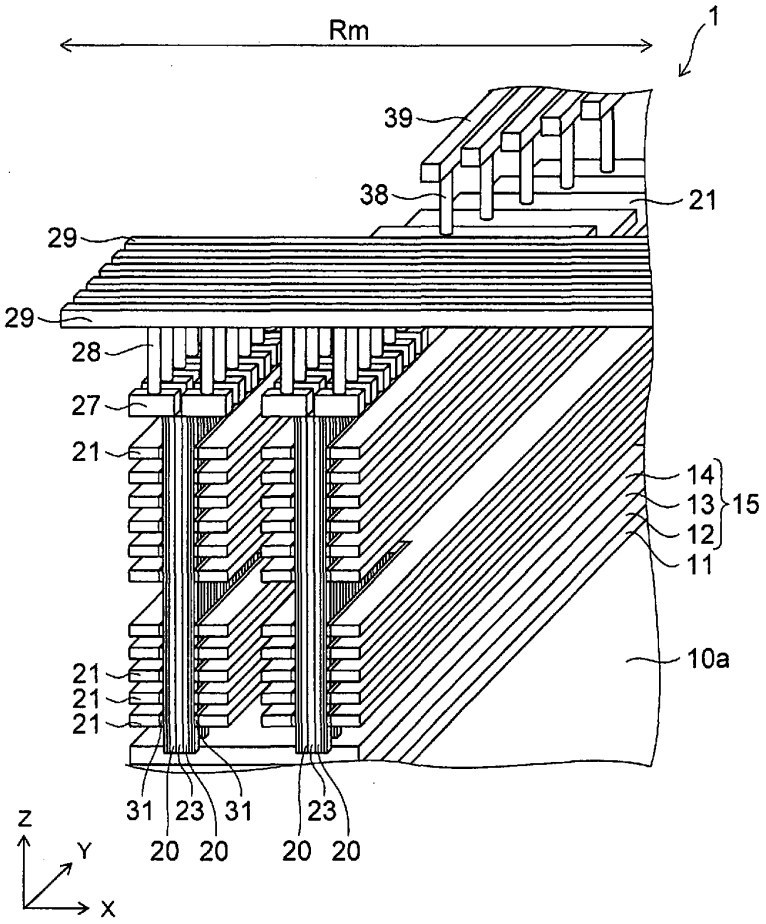


圖1

1・・・半導體記憶體裝置

10a・・・上部表面

11・・・絕緣膜

12・・・導電層

13・・・互連層

14・・・導電層

15・・・胞元源極線

20・・・矽支柱

21・・・控制閘電極膜

23・・・層間絕緣膜

27・・・互連件

28・・・導孔

29・・・位元線

31・・・浮動閘電極膜

38・・・導孔

39・・・字線

Rm・・・記憶體胞元區域

X・・・方向

Y・・・方向

Z・・・方向

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發明專利說明書

（本說明書格式、順序，請勿任意更動）

【發明名稱】

半導體記憶體裝置及其製造方法

SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

相關申請案之交叉參考

本申請案係基於以下專利申請案且主張專利申請案之優先權益：2014年1月10日申請之日本專利申請案第2014-003793號、2014年5月27號申請之臺灣專利申請案第103118501號，及2015年1月7日申請之PCT國際專利申請案第PCT/JP2015/000044號；該等專利申請案之全部內容係以引用方式併入本文中。

【技術領域】

本文所描述之實施例係關於一種半導體記憶體裝置及其製造方法。

【先前技術】

儘管通常已收縮NAND快閃記憶體之平坦結構以增加位元密度且縮減位元成本，但此收縮正在接近極限。因此，近年來，已提出用以在垂直方向上堆疊記憶體胞元(memory cell)之技術。記憶體胞元之資料保留特性(data retention characteristic)在此堆疊式記憶體裝置中係有問題的。

【圖式簡單說明】

圖1為展示根據第一實施例之半導體記憶體裝置的透視圖；

圖2為展示根據第一實施例之半導體記憶體裝置的橫截面圖；

圖3為展示圖2所展示之區域A的橫截面圖；

圖4為沿著圖2所展示之線B-B'的橫截面圖；

圖5A至圖17B為展示用於製造根據第一實施例之半導體記憶體裝置之方法的平面圖及橫截面圖；

圖18為展示根據第一實施例之修改之半導體記憶體裝置的橫截面圖；

圖19為根據第二實施例之半導體記憶體裝置的橫截面圖；

圖20A至圖30C為展示用於製造根據第二實施例之半導體記憶體裝置之方法的平面圖及橫截面圖；

圖31為展示根據第二實施例之第一修改之半導體記憶體裝置的橫截面圖；

圖32為展示根據第二實施例之第二修改之半導體記憶體裝置的橫截面圖；

圖33為展示根據第二實施例之第三修改之半導體記憶體裝置的橫截面圖；

圖34為根據第三實施例之半導體記憶體裝置的橫截面圖；

圖35A至圖37C為展示用於製造根據第三實施例之半導體記憶體裝置之方法的平面圖及橫截面圖；

圖38A至圖38C為展示根據第三實施例之修改之半導體記憶體裝置的橫截面圖；

圖39A至圖39C為展示用於製造根據第三實施例之修改之半導體記憶體裝置之方法的橫截面圖；

圖40為展示根據第四實施例之半導體記憶體裝置的橫截面圖；

圖41為展示圖40所展示之區域E的橫截面圖；

圖42A為展示用於製造根據第四實施例之半導體記憶體裝置之方法的橫截面圖；且圖42B為平面圖；

圖43及圖44為展示根據第五實施例之半導體記憶體裝置的橫截

面圖；

圖45至圖53為展示用於製造根據第五實施例之半導體記憶體裝置之方法的橫截面圖；

圖54為展示根據第五實施例之修改之半導體記憶體裝置的橫截面圖；

圖55至圖57為展示用於製造根據第五實施例之修改之半導體記憶體裝置之方法的橫截面圖；

圖58至圖59為展示根據第六實施例之半導體記憶體裝置的橫截面圖；

圖60為展示根據第六實施例之半導體記憶體裝置的示意性電路圖；

圖61為展示根據第六實施例之半導體記憶體裝置的示意性平面圖；

圖62展示根據第六實施例之半導體記憶體裝置中之胞元源極線(cell source line)的連接關係；

圖63A為展示選擇NAND串及非選擇NAND串之示意性電路圖，圖63B展示施加至選擇NAND串之電位，且圖63C展示施加至非選擇NAND串之電位；

圖64為展示根據第七實施例之半導體記憶體裝置的橫截面圖；

圖65展示根據第七實施例之半導體記憶體裝置中之胞元源極線的連接關係；

圖66為展示根據第八實施例之半導體記憶體裝置的橫截面圖；

圖67展示根據第八實施例之半導體記憶體裝置中之胞元源極線的連接關係；

圖68為展示根據第九實施例之半導體記憶體裝置的透視圖；及

圖69為展示根據第十實施例之半導體記憶體裝置的透視圖。

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【實施方式】

一般而言，根據一項實施例，一種半導體記憶體裝置包括：一基板；一半導體支柱，其提供於該基板上以在一垂直方向上延伸；複數個第一電極膜，其提供於該半導體支柱側方以在一第一方向上延伸。該複數個第一電極膜經安置為沿著該垂直方向彼此分離。該半導體記憶體裝置進一步包括提供於該半導體支柱與該等第一電極膜之間的複數個第二電極膜。該複數個第二電極膜經安置為沿著該垂直方向彼此分離。該半導體記憶體裝置進一步包括提供於該半導體支柱與該等第二電極膜之間的一第一絕緣膜，及提供於該第二電極膜與該第一電極膜之間的一第二絕緣膜。

第一實施例

現在將參看圖式來描述本發明之實施例。

首先，將描述第一實施例。

圖1為展示根據實施例之半導體記憶體裝置的透視圖。

圖2為展示根據實施例之半導體記憶體裝置的橫截面圖。

圖3為展示圖2所展示之區域A的橫截面圖。

圖4為沿著圖2所展示之線B-B'的橫截面圖。

如圖1及圖2所展示，矽基板10提供於根據實施例之半導體記憶體裝置1中。記憶體胞元區域Rm及周邊電路區域Rc設定於矽基板10中。在下文中，出於描述方便起見而在本說明書中使用XYZ正交座標系統。平行於矽基板10之上部表面10a的兩個相互正交方向被視為X方向及Y方向；且垂直於上部表面10a之方向被視為Z方向。

在記憶體胞元區域Rm中，由(例如)氧化矽製成之絕緣膜11 (第三絕緣膜)、由(例如)多晶矽製成之導電層12、由(例如)鎢製成之互連層13及由(例如)多晶矽製成之導電層14以此次序堆疊於矽基板10上。胞元源極線15係由導電層12、互連層13及導電層14形成。由(例如)氧化

矽製成之絕緣膜17提供於胞元源極線15上。在Z方向上延伸之多個矽支柱20提供於胞元源極線15上。矽支柱20係由(例如)多晶矽製成；且矽支柱20之下部末端刺穿絕緣膜17以連接至胞元源極線15。矽支柱20沿著X方向及Y方向依矩陣組態而配置，如自Z方向所觀看，且具有與單一胞元源極線15之共同連接。

多個控制閘電極膜(第一電極膜) 21提供於矽支柱20側方以沿著Z方向彼此分離。控制閘電極膜21中之每一者係由(例如)鎢製成，且在Y方向上延伸。因此，控制閘電極膜21未安置於沿著Y方向而配置之矽支柱20之間。又，在X方向上，矽支柱20中之兩者與控制閘電極膜21中之兩者交替地配置。換言之，當沿著X方向而配置之矽支柱20被組織成每隔兩個相互鄰近矽支柱20多個集合22時，且當控制閘電極膜21中之兩者經配置以定位於集合22之間時，控制閘電極膜21未安置於屬於每一集合22之兩個矽支柱20之間。

層間絕緣膜23提供於矽支柱20之間。由(例如)氧化矽製成之層間絕緣膜24提供於控制閘電極膜21之間、最下部層之控制閘電極膜21下方，及最上部層之控制閘電極膜21上方。硬質遮罩26提供於由多個控制閘電極膜21、層間絕緣膜23及層間絕緣膜24製成之堆疊式本體25上。

矽支柱20被抽出至硬質遮罩26上以成為具有在X方向上延伸之互連件27之單一本體。導孔28提供於互連件27上；且在X方向上延伸之位元線29提供於導孔28上。位元線29係藉由導孔28而連接至互連件27。因此，矽支柱20中之每一者連接於位元線29與胞元源極線15之間。換言之，半導體記憶體裝置1為I狀支柱型堆疊式記憶體裝置。

堆疊式本體25之Y方向末端部分經圖案化成階梯組態；且在階梯組態之末端部分處，在Z方向上具有相同位置之多個控制閘電極膜21捆束在一起。導孔38提供於捆束式控制閘電極膜21之末端部分上。在

Y方向上延伸之字線39提供於導孔38上。在Z方向上，字線39之位置與位元線29之位置相同。字線39係藉由導孔38而連接至控制閘電極膜21。

如圖3及圖4所展示，由(例如)多晶矽製成之浮動閘電極膜31 (第二電極膜)提供於矽支柱20與控制閘電極膜21之間。因為浮動閘電極膜31提供於矽支柱20與控制閘電極膜21之間的每一相交點處，所以浮動閘電極膜31依矩陣組態而配置為沿著Y方向及Z方向彼此分離。如上文所描述，因為矽支柱20及控制閘電極膜21沿著X方向而配置，所以浮動閘電極膜31亦沿著X方向而配置。因此，浮動閘電極膜31依XYZ三維矩陣組態而配置。當自Z方向觀看時，浮動閘電極膜31之組態為在控制閘電極膜21側上較寬之類扇形狀。因此，矽支柱20側上之浮動閘電極膜31之末端部分在Y方向上的長度L1短於控制閘電極膜21側上之浮動閘電極膜31之末端部分在Y方向上的長度L2。

由(例如)氧化矽製成之穿隧絕緣膜33提供於矽支柱20與浮動閘電極膜31之間。穿隧絕緣膜33提供於每一矽支柱20處；且穿隧絕緣膜33之組態為在Z方向上延伸且具有X方向作為厚度方向及具有Y方向作為寬度方向之條帶組態。

另一方面，阻擋絕緣膜34提供於浮動閘電極膜31與控制閘電極膜21之間。阻擋絕緣膜34為(例如)三層膜，其中氮化矽層35、氧化矽層36及氮化矽層37以此次序自浮動閘電極膜31側朝向控制閘電極膜21側堆疊。氮化矽層35形成於浮動閘電極膜31周圍以覆蓋浮動閘電極膜31之上部表面31a及下部表面31b。氧化矽層36及氮化矽層37形成於控制閘電極膜21周圍以覆蓋控制閘電極膜21之上部表面21a及下部表面21b。

儘管穿隧絕緣膜33通常為絕緣的，但穿隧絕緣膜33為當施加半導體記憶體裝置1之驅動電壓之範圍內之電壓時穿隧電流在其中流動

的膜。阻擋絕緣膜34為即使當施加半導體記憶體裝置1之驅動電壓之範圍內之電壓時電流仍實質上不在其中流動的膜。穿隧絕緣膜33之等效氧化物厚度(equivalent oxide thickness, EOT)厚於阻擋絕緣膜34之等效氧化物厚度；且穿隧絕緣膜33之介電常數低於阻擋絕緣膜之介電常數。

在如圖2所展示之周邊電路區域Rc中，源極區域40s及汲極區域40d在矽基板10中形成為彼此分離。源極區域40s與汲極區域40d之間的區域為通道區域40c。由(例如)氧化矽製成之閘極絕緣膜41 (第四絕緣膜)在矽基板10上提供於通道區域40c正上方之區域中；且由(例如)多晶矽製成之導電層42及由(例如)鎢製成之互連層43以此次序堆疊於閘極絕緣膜41上。閘電極45係由導電層42及互連層43形成。電晶體46包括源極區域40s、汲極區域40d、通道區域40c、閘極絕緣膜41及閘電極45。電晶體46包括於周邊電路中。

如下文所描述，處於記憶體胞元區域Rm中之絕緣膜11及處於周邊電路區域Rc中之閘極絕緣膜41係藉由劃分同一氧化矽膜而形成；處於記憶體胞元區域Rm中之導電層12及處於周邊電路區域Rc中之導電層42係藉由劃分同一多晶矽層而形成；且處於記憶體胞元區域Rm中之互連層13及處於周邊電路區域Rc中之互連層43係藉由劃分同一鎢層而形成。

現在將描述用於製造根據實施例之半導體記憶體裝置之方法。

圖5A至圖17B為展示用於製造根據實施例之半導體記憶體裝置之方法的平面圖及橫截面圖。

圖5A至圖17B中僅展示記憶體胞元區域Rm。

首先，如圖1及圖2所展示，在周邊電路區域Rc中在矽基板10之上部層部分中形成通道區域40c、源極區域40s及汲極區域40d。接著，在記憶體胞元區域Rm及周邊電路區域Rc兩者中在矽基板10上形

成氧化矽膜。因此，在周邊電路區域Rc中，在低崩潰電壓電晶體(LV Tr)區域中形成相對薄的氧化矽膜；且在高崩潰電壓電晶體(HV Tr)區域中形成相對厚的氧化矽膜。又，在記憶體胞元區域Rm中形成相對厚的氧化矽膜。

接著，在整個表面上形成多晶矽層。使用適當遮罩(未圖示)而在周邊電路區域Rc中在矽基板10之上部層部分中形成淺渠溝隔離(Shallow Trench Isolation, STI)。接著，形成鎢層。接著，僅在記憶體胞元區域Rm中形成多晶矽層及氧化矽膜。接著，藉由反應性離子蝕刻(Reactive Ion Etching, RIE)來圖案化此等層。

藉此，針對記憶體胞元區域Rm中之每一區塊形成絕緣膜11、導電層12、互連層13、導電層14及絕緣膜17。胞元源極線15係由堆疊式本體形成，該堆疊式本體係由導電層12、互連層13及導電層14製成。藉由形成胞元源極線15以針對每一區塊而劃分，按區塊為單位進行抹除為可能的。另一方面，在周邊電路區域Rc中形成閘極絕緣膜41、導電層42及互連層43。閘電極45係由堆疊式本體形成，該堆疊式本體係由導電層42及互連層43製成。藉此，在周邊電路區域Rc中形成電晶體46。

接著，如圖5A及圖5B所展示，在記憶體胞元區域Rm中之絕緣膜17 (參看圖2)上交替地堆疊氧化矽膜51與氮化矽膜52。藉此，形成堆疊式本體25。此時，因為電極側上之閘極長度(控制閘電極膜21及提供於控制閘電極膜21周圍之阻擋絕緣膜之總厚度)長於通道側上之閘極長度(浮動閘電極膜31及提供於浮動閘電極膜31周圍之阻擋絕緣膜之總厚度)，所以根據自兩個側填充之阻擋膜的膜厚度來調整所堆疊之氧化矽膜51與氮化矽膜52之膜厚度比。圖5A為橫截面圖；且圖5B為俯視圖。此情形對於以下圖式亦類似。

繼而如圖6A及圖6B所展示，在堆疊式本體25上形成由(例如)氮

化矽製成之硬質遮罩26。接著，圖案化硬質遮罩26；且使用經圖案化硬質遮罩26作為遮罩來執行堆疊式本體25之諸如RIE等等之各向異性蝕刻。藉此，在堆疊式本體25中製得多個渠溝53以在Y方向上延伸。渠溝53刺穿堆疊式本體25。

接著，如圖7A及圖7B所展示，藉由經由渠溝53來執行濕式蝕刻而使氮化矽膜52凹入。藉此，氮化矽膜52之曝露表面在渠溝53之內部表面處後退以製得在Y方向上延伸之凹部54。接著，藉由SPA等等來執行氧化處理。藉此，運用薄氧化矽層50來覆蓋渠溝53之內部表面處的氮化矽膜52之曝露表面。

繼而如圖8A及圖8B所展示，在整個表面上形成氮化矽層35。接著，在整個表面上形成多晶矽膜55。亦在渠溝53之內部表面上形成氮化矽層35及多晶矽膜55以進入凹部54。

接著，如圖9A及圖9B所展示，藉由沿著渠溝53執行諸如RIE等等之各向異性蝕刻，選擇性地移除多晶矽膜55及氮化矽層35以餘留於凹部54內部；且使在Z方向上彼此鄰近地餘留於凹部54內部之多晶矽膜55彼此分離。類似地，亦使在Z方向上彼此鄰近地餘留於凹部54內部之氮化矽層35彼此分離。

繼而如圖10A及圖10B所展示，將穿隧絕緣膜33、多晶矽膜56及絕緣膜57以此次序沈積。

接著，如圖11A及圖11B所展示，在堆疊式本體25及堆疊於堆疊式本體25上方之堆疊式本體中製得渠溝58以在Y方向上延伸於渠溝53之間。藉此，沿著X方向交替地配置渠溝53與渠溝58。

繼而如圖12A及圖12B所展示，藉由經由渠溝58來執行使用熱磷酸之濕式蝕刻而使氮化矽膜52凹入。該凹入受到凹部59之背部表面處曝露的氧化矽層50擋止。藉此，移除氮化矽膜52；且在渠溝58之內部表面中製得凹部59以在Y方向上延伸。此時，因為氮化矽層35受到氧

化矽層50保護，所以氮化矽層35未受到損害。

接著，如圖13A及圖13B所展示，移除凹部59之背部表面處曝露的氧化矽層50。藉此，在凹部59之背部表面處曝露氮化矽層35。接著，在渠溝58之內部表面上形成氧化矽層36及氮化矽層37。因此，如圖3所展示，阻擋絕緣膜34係由氮化矽層35、氧化矽層36及氮化矽層37形成。接著，藉由(例如)化學氣相沈積(Chemical Vapor Deposition, CVD)而在整個表面上形成鎢膜61。氧化矽層36、氮化矽層37及鎢膜61亦經由渠溝58而進入凹部59。

繼而如圖14A及圖14B所展示，藉由執行諸如RIE等等之各向異性蝕刻來選擇性地移除鎢膜61。藉此，致使鎢膜61餘留於凹部59內部；且使在Z方向上彼此鄰近地餘留於凹部59內部之鎢膜61彼此分離。因此，在凹部59內部形成由鎢膜61製成之控制閘電極膜21。隨後，將層間絕緣膜24填充至渠溝58中；且平坦化層間絕緣膜24之上部表面。圖14B為沿著圖14A所展示之線B-B'的橫截面圖。

接著，如圖15A至圖15C所展示，形成硬質遮罩62，其中開口62a沿著X方向及Y方向依矩陣組態而配置。開口62a中之每一者之組態為矩形，其中X方向作為縱向方向；且開口62a在多晶矽膜56及多晶矽膜56之間的絕緣膜57正上方之區域中沿著Y方向間歇地配置，但未安置於層間絕緣膜24正上方之區域中。接著，藉由使用硬質遮罩62及硬質遮罩26作為遮罩來執行諸如RIE等等之各向異性蝕刻而沿著Y方向劃分多晶矽膜56及絕緣膜57。藉此，在開口62a正下方之區域中在多晶矽膜56及絕緣膜57中製得通孔63。形成於硬質遮罩26上的多晶矽膜56之部分變為互連件27；且藉由通孔63劃分的多晶矽膜56之部分變為矽支柱20。圖15B為沿著圖15A所展示之線C-C'的平面圖；且圖15C為沿著圖15A所展示之線B-B'的橫截面圖。

繼而如圖16所展示，藉由經由通孔63而執行諸如化學乾式蝕刻

(Chemical Dry Etching, CDE)、濕式蝕刻等等之各向同性蝕刻來選擇性地移除穿隧絕緣膜33及多晶矽膜55。藉此，沿著Y方向劃分穿隧絕緣膜33及多晶矽膜55。亦移除絕緣膜57 (參見圖15A)。因此，浮動閘電極膜31係由多晶矽膜55形成。此時，因為自矽支柱20側蝕刻多晶矽膜55，所以矽支柱20側上之浮動閘電極膜31之末端部分在Y方向上的長度L1短於控制閘電極膜21側上之浮動閘電極膜31之末端部分在Y方向上的長度L2。此時，另一方面，層間絕緣膜24餘留而不被移除。

接著，如圖17A及圖17B所展示，在整個表面上沈積層間絕緣膜23。亦將層間絕緣膜23填充於通孔63內部。氧化矽膜51亦變為層間絕緣膜23之一部分。

繼而如圖1及圖2所展示，形成導孔28、導孔38、位元線29及字線39。因此，製造根據實施例之半導體記憶體裝置1。

現在將描述實施例之效果。

在實施例中，提供由多晶矽製成之浮動閘電極膜31作為電荷儲存單元。因此，記憶體胞元之資料保留特性良好；且因為可藉由移動電子而非電洞來抹除儲存於浮動閘電極膜31中之電荷，所以抹除操作快速。因為浮動閘電極膜31彼此分離，所以資料保留特性甚至更好。

在實施例中，因為阻擋絕緣膜34為由氮化矽層35、氧化矽層36及氮化矽層37製成之三層膜，所以可確保耦合比，同時抑制洩漏電流。又，氮化矽層35在圖8A及圖8B所展示之製程中係由矽支柱20側形成；且氧化矽層36及氮化矽層37在圖13A及圖13B所展示之製程中係由控制閘電極膜21側形成。

因此，藉由將阻擋絕緣膜34之三層膜劃分成兩個且由兩個側形成三層膜，與由僅一個側形成之狀況相比較，阻擋絕緣膜34之厚度可分佈於浮動閘電極膜31之兩個X方向側上；且可縮減整體上在Z方向上之厚度。藉此，可縮減凹部54 (參看圖8A及圖8B)及凹部59 (參看圖

13A及圖13B)在Z方向上之高度；可增加記憶體胞元在Z方向上之位元密度；且可縮減縱橫比。

在實施例中，沿著Z方向針對控制閘電極膜21中之每一者劃分阻擋絕緣膜34。藉此，可防止儲存於浮動閘電極膜31中之電子傳播通過阻擋絕緣膜34及洩漏。因此，記憶體胞元之資料保留特性良好。

在實施例中，如圖4所展示，浮動閘電極膜31之組態為在控制閘電極膜21側上較寬之類扇形狀。藉此，浮動閘電極膜31與控制閘電極膜21之間的IPD電容可大；且耦合比可大。

儘管在實施例中說明阻擋絕緣膜34為三層膜的實例，但此實施例並不限於此實例。阻擋絕緣膜34之層並不限於氧化矽層(SiO_2層)及氮化矽層(Si_3N_4層)，且可為高介電常數層，諸如，Al_2O_3層、MgO層、SrO層、SiN層、BaO層、TiO層、Ta_2O_5層、$BaTiO_3$層、BaZrO層、ZrO_2層、Y_2O_3層、ZrSiO層、HfAlO層、HfSiO層、La_2O_3層、LaAlO層等等。

儘管在實施例中說明浮動閘電極膜31係由多晶矽形成的實例，但浮動閘電極膜31並不限於此實例，且可由(例如)金屬矽化物或金屬形成。

儘管在實施例中說明控制閘電極膜21係由鎢形成的實例，但控制閘電極膜21並不限於此實例，且可藉由填充多晶矽膜且隨後矽化多晶矽膜而由(例如)金屬矽化物形成。

在圖5A及圖5B所展示之製程中，可將最下部層及最上部層之氮化矽膜52形成為厚於其他氮化矽膜52。藉此，形成於控制閘電極膜21下方及上方之選擇閘電極膜的膜厚度可厚於控制閘電極膜21之膜厚度。因此，可形成閘極長度長於記憶體胞元電晶體之閘極長度的選擇電晶體。

堆疊式本體25之上部部分處提供的控制閘電極膜21之若干層可

彼此短路以用作選擇閘電極膜；且堆疊式本體25之下部部分處提供的控制閘電極膜21之若干層可彼此短路以用作選擇閘電極膜。藉此，可形成閘極長度長於記憶體胞元電晶體之閘極長度的選擇電晶體。

第一實施例之修改

現在將描述實施例之修改。

圖18為展示根據該修改之半導體記憶體裝置的橫截面圖。

在如圖18所展示之根據該修改之半導體記憶體裝置1a中，一個寬矽支柱65提供於在X方向上彼此鄰近之兩個浮動閘電極膜31之間。換言之，層間絕緣膜24未提供於屬於集合22中之每一者的兩個矽支柱20之間；且兩個矽支柱20被形成為一個本體。

在根據該修改之半導體記憶體裝置1a中，寬矽支柱65之兩個X方向側部分用作相異通道。在其他方面，該修改之組態、製造方法及效果類似於上述第一實施例之組態、製造方法及效果。

第二實施例

現在將描述第二實施例。

圖19為展示根據實施例之半導體記憶體裝置的橫截面圖。

如圖19所展示，根據實施例之半導體記憶體裝置2不同於根據上述第一實施例之半導體記憶體裝置1 (參看圖1至圖4)之處在於穿隧絕緣膜33及阻擋絕緣膜34之安置為顛倒的。

換言之，在半導體記憶體裝置2中，阻擋絕緣膜34安置於矽支柱20與浮動閘電極膜31之間；且穿隧絕緣膜33安置於浮動閘電極膜31與控制閘電極膜21之間。因此，包括於記憶體胞元中之組件係以矽支柱20-阻擋絕緣膜34-浮動閘電極膜31-穿隧絕緣膜33-控制閘電極膜21之次序而配置。

更具體而言，在半導體記憶體裝置2中，氧化矽膜71經配置為沿著Z方向彼此分離；且浮動閘電極膜31及控制閘電極膜21提供於相互

鄰近氧化矽膜71之間的空間中。又，穿隧絕緣膜33經安置為在浮動閘電極膜31側上覆蓋控制閘電極膜21之上部表面及下部表面以及控制閘電極膜31之側表面。另一方面，阻擋絕緣膜34沿著矽支柱20之側表面線性地安置。

類似於第一實施例，阻擋絕緣膜34可為多層膜，例如，三層膜。然而，阻擋絕緣膜34在矽支柱20側與控制閘電極膜21側之間未被再分；且整個阻擋絕緣膜34安置於矽支柱20側上。

在半導體記憶體裝置2中，屬於集合22之兩個矽支柱20的下部末端部分彼此連接；且未提供胞元源極線15。源極線(未圖示)提供於堆疊式本體上方。換言之，半導體記憶體裝置2為U狀支柱型堆疊式記憶體裝置。在其他方面，實施例之組態類似於上述第一實施例之組態。

半導體記憶體裝置2之基本操作及讀出方法類似於正常NAND快閃記憶體之基本操作及讀出方法；且在程式化操作及抹除操作中施加於矽支柱20與控制閘電極膜21之間的電壓之極性與正常NAND快閃記憶體之極性相反。藉此，致使電荷自控制閘電極膜21移進及移出矽支柱20。

現在將描述用於製造根據實施例之半導體記憶體裝置之方法。

圖20A至圖30C為展示用於製造根據實施例之半導體記憶體裝置之方法的平面圖及橫截面圖。

首先，如圖20A及圖20B所展示，在矽基板10 (參看圖2)上形成由氧化矽製成之絕緣膜17；且隨後，藉由交替地堆疊氧化矽膜71與多晶矽膜72來形成堆疊式本體73。多晶矽膜72可被摻雜有硼(B)、可被摻雜有磷(P)，或可未被摻雜。圖20A為橫截面圖；且圖20B為俯視圖。此情形對於以下圖式亦類似。

接著，如圖21A及圖21B所展示，藉由在堆疊式本體73上形成硬

質遮罩(未圖示)、藉由微影進行圖案化且使用經圖案化硬質遮罩作為遮罩來執行諸如RIE等等之各向異性蝕刻而在堆疊式本體73中製得多個渠溝75以在Y方向上延伸。渠溝75在Z方向上刺穿堆疊式本體73，但並不刺穿絕緣膜17。

繼而如圖22A及圖22B所展示，在渠溝75之內部表面上，形成阻擋絕緣膜34；且隨後，形成多晶矽膜77。在渠溝75之側表面上及在渠溝75之底部表面上形成阻擋絕緣膜34及多晶矽膜77以向後摺疊成U狀，如自Y方向所觀看。因此，設定渠溝75之寬度與阻擋絕緣膜34及多晶矽膜77之膜厚度之間的關係，使得此向後摺疊為可能的。接著，藉由沈積氧化矽而將層間絕緣膜24填充至渠溝75中。

接著，如圖23A及圖23B所展示，藉由在堆疊式本體73上形成硬質遮罩(未圖示)、藉由微影進行圖案化且使用經圖案化硬質遮罩作為遮罩來執行諸如RIE等等之各向異性蝕刻而在渠溝75之間的堆疊式本體73之部分中製得渠溝78以在Y方向上延伸。沿著X方向交替地配置渠溝75與渠溝78。

繼而如圖24A及圖24B所展示，使用(例如)膽鹼水溶劑(choline aqueous solution, TMY)來執行濕式蝕刻。藉此，經由渠溝78各向同性地蝕刻多晶矽膜72；且致使渠溝78之內部表面處之多晶矽膜72的曝露表面後退。藉此，在渠溝78之內部表面處製得凹部79。

接著，如圖25A及圖25B所展示，藉由在渠溝78之內部表面上沈積氧化矽來形成穿隧絕緣膜33。此時，亦在凹部79之內部表面上形成穿隧絕緣膜33以接觸多晶矽膜72。可藉由多晶矽膜72之曝露表面之熱氧化來形成穿隧絕緣膜33。

繼而如圖26A及圖26B所展示，藉由(例如)根據CVD來沈積鎢而在渠溝78內部形成鎢膜81。此時，亦將鎢膜81填充至凹部79中。

接著，如圖27A及圖27B所展示，藉由蝕刻鎢膜81來移除未被填

充至凹部79中的鎢膜81之部分。藉此，使餘留於凹部79內部之鎢膜81在凹部79之間彼此分離以變為控制閘電極膜21。接著，將層間絕緣膜24填充至渠溝78中；且平坦化層間絕緣膜24之上部表面。代替鎢，可在圖26A及圖26B所展示之製程中沈積矽；且可在此製程中矽化該矽。藉此，控制閘電極膜21係由金屬矽化物形成。

繼而如圖28A至圖28C所展示，藉由使用適當遮罩執行各向異性蝕刻來選擇性地移除層間絕緣膜24、多晶矽膜77及阻擋絕緣膜34而在渠溝75中製得通孔82。藉由通孔82沿著Y方向週期性地劃分多晶矽膜77以變為矽支柱20。圖28A為橫截面圖；圖28B為沿著圖28A所展示之線C-C'的橫截面圖；且圖28C為沿著圖28A所展示之線B-B'的橫截面圖。此情形對於圖29A至圖29C及圖30A至圖30C類似。

接著，如圖29A至圖29C所展示，藉由執行諸如CDE、濕式蝕刻等等之各向同性蝕刻而經由導孔82來進一步移除阻擋絕緣膜34、多晶矽膜72及穿隧絕緣膜33以沿著Y方向而劃分。藉此，沿著Y方向而劃分之多晶矽膜72變為浮動閘電極膜31。此時，根據各向同性蝕刻之條件，浮動閘電極膜31之組態變為在控制閘電極膜21側上較寬之類扇形狀。

繼而如圖30A至圖30C所展示，藉由(例如)沈積氧化矽且平坦化氧化矽之上部表面而將層間絕緣膜24填充至通孔82中。接著，藉由正常方法來形成導孔28、導孔38、源極線、位元線29及字線39 (參看圖1及圖2)。因此，製造根據實施例之半導體記憶體裝置2。

現在將描述實施例之效果。

在NAND記憶體裝置之程式化操作及抹除操作中，有必要使電流在穿隧絕緣膜中流動且有必要使電流不容易在阻擋絕緣膜中流動。為此，有必要使阻擋絕緣膜之實體膜厚度厚於穿隧絕緣膜之實體膜厚度。因此，若阻擋絕緣膜34待形成為在周圍延伸至氧化矽膜71之間的

間隙中，則有必要將氧化矽膜71之間的間距設定為在Z方向上長，此情形阻礙記憶體胞元在Z方向上之較高整合。另外，渠溝75及78之縱橫比不良地增加；且圖案化變得困難。

若氧化矽膜71之間距仍然被設定為短，則在控制閘電極膜21之上部表面及下部表面處運用阻擋絕緣膜34所覆蓋的控制閘電極膜21之厚度變得短於氧化矽膜71之間距。因此，控制閘電極膜21之互連電阻增加；記憶體胞元電晶體之閘極長度變短；且記憶體胞元電晶體之特性歸因於短通道效應而不良地降級。

相反地，在實施例中，在圖22A及圖22B所展示之製程中在渠溝75之內部表面上形成阻擋絕緣膜34。因此，藉由在早期形成阻擋絕緣膜34，不再有必要使阻擋絕緣膜34在周圍延伸至氧化矽膜71之間的間隙中；且氧化矽膜71之間距可較短。如圖19所展示，在實施例中，儘管穿隧絕緣膜33在周圍延伸至氧化矽膜71之間的間隙中，但存在很少問題，此係因為穿隧絕緣膜33薄於阻擋絕緣膜34，如上文所描述。因此，根據實施例，可在確保控制閘電極膜21之厚度之後增加記憶體胞元在Z方向上之位元密度；且可縮減縱橫比。在其他方面，實施例之效果類似於上述第一實施例之效果。

第二實施例之第一修改

現在將描述實施例之第一修改。

圖31為展示根據該修改之半導體記憶體裝置的橫截面圖。

在如圖31所展示之根據該修改之半導體記憶體裝置2a中，提供由絕緣電荷儲存材料製成之電荷儲存膜85以代替由導電材料製成之浮動閘電極膜31。電荷儲存膜85係由(例如)氮化矽形成。因此，半導體記憶體裝置2a之記憶體胞元具有MONOS結構。在其他方面，該修改之組態、製造方法、操作及效果類似於上述第二實施例之組態、製造方法、操作及效果。

第二實施例之第二修改

現在將描述實施例之第二修改。

圖32為展示根據該修改之半導體記憶體裝置的橫截面圖。

在如圖32所展示之根據該修改之半導體記憶體裝置2b中，提供胞元源極線15；且矽支柱20之下部末端連接至胞元源極線15。換言之，半導體記憶體裝置2b為I狀支柱型堆疊式記憶體裝置。

為了在製造根據該修改之半導體記憶體裝置2b時將矽支柱20之下部末端連接至胞元源極線15，有必要在圖22A及圖22B所展示之製程中藉由蝕刻來移除形成於渠溝75之底部表面上的阻擋絕緣膜34之部分。然而，蝕刻並不損害穿隧絕緣膜33，此係因為此時仍未形成穿隧絕緣膜33。在其他方面，該修改之組態、製造方法、操作及效果類似於上述第二實施例之組態、製造方法、操作及效果。

第二實施例之第三修改

現在將描述實施例之第三修改。

圖33為展示根據該修改之半導體記憶體裝置的橫截面圖。

如圖33所展示，該修改為組合上述之第一修改與第二修改的實例。即，在根據該修改之半導體記憶體裝置2c中，提供由絕緣電荷儲存材料製成之電荷儲存膜85；且矽支柱20之下部末端連接至胞元源極線15。因此，半導體記憶體裝置2c具有MONOS結構且為I狀支柱型。在其他方面，該修改之組態、製造方法、操作及效果類似於上述第二實施例以及上述第二實施例之第一修改及第二修改之組態、製造方法、操作及效果。

第三實施例

現在將描述第三實施例。

圖34為展示根據實施例之半導體記憶體裝置的橫截面圖。

與根據上述第二實施例之半導體記憶體裝置2 (參看圖19)相比

較，在如圖34所展示之根據實施例之半導體記憶體裝置3中，在矽支柱20、控制閘電極膜21、浮動閘電極膜31、穿隧絕緣膜33與阻擋絕緣膜34之間製得氣隙86。更具體而言，在以下各者之間製得氣隙86：在Z方向上彼此鄰近之控制閘電極膜21之間、在Z方向上彼此鄰近之浮動閘電極膜31之間、在Y方向上彼此鄰近之矽支柱20之間、在阻擋絕緣膜34之間、在浮動閘電極膜31之間、在穿隧絕緣膜33之間，及在X方向上彼此鄰近且屬於同一集合22之兩個矽支柱20之間。

現在將描述用於製造根據實施例之半導體記憶體裝置之方法。

圖35A及圖35B至圖37A至圖37C為展示用於製造根據實施例之半導體記憶體裝置之方法的平面圖及橫截面圖。

圖35A為橫截面圖；且圖35B為平面圖。圖36A為橫截面圖；圖36B為沿著圖36A所展示之線C-C'的橫截面圖；且圖36C為沿著圖36A所展示之線B-B'的橫截面圖。此情形對於圖37A至圖37C類似。

首先，如圖35A及圖35B所展示，藉由在矽基板10 (參看圖2)上形成由氧化矽製成之絕緣膜17且隨後交替地堆疊氮化矽膜87與多晶矽膜72來形成堆疊式本體。

接著，實施圖21A及圖21B至圖29A至圖29C所展示之製程。然而，在圖24A及圖24B以及圖27A及圖27B所展示之製程中，填充氮化矽膜88以代替由氧化矽製成之層間絕緣膜24。

藉此，如圖36A至圖36C所展示，製得類似於圖29A至圖29C所展示之中間結構本體的中間結構本體。然而，在實施例之中間結構本體中，提供氮化矽膜87以代替氧化矽膜71；且提供氮化矽膜88以代替層間絕緣膜24。

接著，如圖37A至圖37C所展示，藉由(例如)濕式蝕刻來移除氮化矽膜87及氮化矽膜88。藉此，在氮化矽膜87及氮化矽膜88被安置的空間中製得氣隙86。因此，製造根據實施例之半導體記憶體裝置3。

根據實施例，因為在矽支柱20、控制閘電極膜21、浮動閘電極膜31、穿隧絕緣膜33與阻擋絕緣膜34之間製得氣隙86，所以可抑制近接效應；且可增加崩潰電壓。

在其他方面，實施例之組態、製造方法、操作及效果類似於上述第二實施例之組態、製造方法、操作及效果。

有可能在圖35A及圖35B所展示之製程中藉由交替地堆疊氧化矽膜71與多晶矽膜72以代替氮化矽膜87與多晶矽膜72而僅在矽支柱20之間製得氣隙。

第三實施例之修改

現在將描述實施例之修改。

圖38A至圖38C為展示根據該修改之半導體記憶體裝置的橫截面圖。

圖38A為橫截面圖；圖38B為沿著圖38A所展示之線C-C'的橫截面圖；且圖38C為沿著圖38A所展示之線B-B'的橫截面圖。圖38A為沿著圖38C所展示之線D-D'的橫截面圖。此情形對於下文所描述之圖39A至圖39C類似。

如圖38A至圖38C所展示，根據該修改之半導體記憶體裝置3a不同於根據上述第三實施例之半導體記憶體裝置3 (參看圖34)之處在於藉由致使氮化矽膜87及88部分地餘留而在多個區域中形成加強構件89。加強構件89在Z方向上延伸，且沿著Y方向間歇地安置於半導體記憶體裝置3a內部。

圖39A至圖39C為展示用於製造根據該修改之半導體記憶體裝置之方法的橫截面圖。

在如圖39A至圖39C所展示之修改中，不在加強構件89將被形成的區域中製得通孔82。藉此，在圖37A至圖37C所展示之製程中，當經由通孔82而執行氮化矽膜87及88之濕式蝕刻時，氮化矽膜87及88局

部地餘留以變為加強構件89。

根據該修改，藉由提供加強構件89，可確保半導體記憶體裝置3a之機械強度；且可防止崩陷。在其他方面，該修改之組態、製造方法、操作及效果類似於上述第三實施例之組態、製造方法、操作及效果。

第四實施例

現在將描述第四實施例。

圖40為展示根據實施例之半導體記憶體裝置的橫截面圖。

圖41為展示圖40所展示之區域E的橫截面圖。

如圖40及圖41所展示，根據實施例之半導體記憶體裝置4不同於根據上述第一實施例之半導體記憶體裝置1 (參看圖1至圖4)之處在於阻擋絕緣膜34未安置於最上部層級之控制閘電極膜21u與最上部層級之浮動閘電極膜31u之間；且最上部層級之控制閘電極膜21u連接至最上部層級之浮動閘電極膜31u。

現在將描述根據實施例之半導體記憶體裝置。

圖42A為展示用於製造根據實施例之半導體記憶體裝置之方法的橫截面圖；且圖42B為平面圖。

首先，實施圖5A及圖5B至圖12A及圖12B所展示之製程。

接著，如圖42A及圖42B所展示，在渠溝58之內部表面上形成氧化矽層36及氮化矽層37。接著，將抗蝕劑材料90填充至渠溝58中；且藉由使抗蝕劑材料90之上部表面凹入來曝露最上部層級之凹部59u。接著，藉由(例如)濕式蝕刻來移除自抗蝕劑材料90曝露的氮化矽層37、氧化矽層36及氮化矽層35之部分。藉此，在最上部層級之凹部59u之背部表面處曝露多晶矽膜55。接著，移除抗蝕劑材料90。

繼而如圖13A及圖13B所展示，在渠溝58之內部表面上形成鎢膜61。此時，鎢膜61接觸最上部層級之凹部59u內部的多晶矽膜55。後

續製程類似於上述第一實施例之製程。

根據實施例，可藉由致使最上部層級之控制閘電極膜21u連接最上部層級之浮動閘電極膜31u來電氣整合控制閘電極膜21u與浮動閘電極膜31u以用作選擇閘電極膜。藉此，可形成臨限值並不波動的選擇閘極電晶體，此係因為未儲存電荷。

在其他方面，實施例之組態、製造方法、操作及效果類似於上述第一實施例之組態、製造方法、操作及效果。

第五實施例

現在將描述第五實施例。

圖43及圖44為展示根據實施例之半導體記憶體裝置的橫截面圖。

在如圖43及圖44所展示之根據實施例之半導體記憶體裝置5中，多個矽支柱20沿著X方向及Y方向依矩陣組態而提供及配置。矽支柱20中之每一者具有在Z方向上延伸之圓形柱狀組態。穿隧絕緣膜33、浮動閘電極膜31及阻擋絕緣膜34係自內部(亦即，矽支柱20側)按次序依圓形環組態而提供於矽支柱20中之每一者周圍。換言之，浮動閘電極膜31提供於矽支柱20周圍，如自Z方向所觀看。

穿隧絕緣膜33及浮動閘電極膜31在Z方向上被劃分。氧化矽膜51提供於堆疊式本體之間，該等堆疊式本體在Z方向上具有由穿隧絕緣膜33及浮動閘電極膜31製成之圓形環組態。在浮動閘電極膜31中，多晶矽層91安置於內側上；且金屬矽化物層92安置於外側上。金屬矽化物層92係由金屬矽化物形成，但可由金屬形成。

在阻擋絕緣膜34中，氧化矽層93安置於內側上；且高介電常數層94安置於外側上。高介電常數層94係由相較於氧化矽具有較高介電常數之材料(例如，鉿(Hf)、氧化鋁(AlO)、氮化鈦(TiN)、氮化鉭(TaN)，或氧化鉭(TaO))製成。氧化矽層93係在Z方向上依管狀組態而

連續地提供。然而，管件之直徑週期性波動，使得對應於浮動閘電極膜31之部分之直徑相對小且對應於氧化矽膜51之部分之直徑相對大。因此，氧化矽層93具有圓形管狀類波紋管組態。高介電常數層94在由氧化矽層93製成之圓形管狀類波紋管組態之外部表面處安置於凹部93a內部，且針對凹部93a中之每一者而劃分。阻擋絕緣膜34之組態並不限於由氧化矽層93及高介電常數層94製成之兩層結構。舉例而言，該組態可為以下各者中之任何層的組合：氧化矽層(SiO_2層)、氮化矽層(Si_3N_4層)、Al_2O_3層、MgO層、SrO層、SiN層、BaO層、TiO層、Ta_2O_5層、$BaTiO_3$層、BaZrO層、ZrO_2層、Y_2O_3層、ZrSiO層、HfAlO層、HfSiO層、La_2O_3層、LaAlO層等等。

在半導體記憶體裝置5中，提供多個控制閘電極膜21以沿著X方向及Z方向依矩陣組態而配置。控制閘電極膜21具有在Y方向上延伸之條帶組態。控制閘電極膜21為導電膜，例如，由氮化鈦層(TiN)及鎢層(W)製成之兩層膜、由氮化鎢層(WN)及鎢層(W)製成之兩層膜，或由氮化鉭層(TaN)及鎢層(W)製成之兩層膜。然而，控制閘電極膜21之組態並不限於此情形；且舉例而言，可使用藉由矽化多晶矽膜而形成之金屬矽化物層。

由矽支柱20、穿隧絕緣膜33、浮動閘電極膜31及阻擋絕緣膜34製成之結構本體刺穿控制閘電極膜21。控制閘電極膜21安置於凹部93a中。換言之，控制閘電極膜21提供於浮動閘電極膜31周圍，如自Z方向所觀看。層間絕緣膜24提供於由矽支柱20、穿隧絕緣膜33、浮動閘電極膜31、阻擋絕緣膜34及控制閘電極膜21製成之結構本體之間。

現在將描述用於製造根據實施例之半導體記憶體裝置之方法。

圖45至圖53為展示用於製造根據實施例之半導體記憶體裝置之方法的橫截面圖。

首先，類似於上述第一實施例，在矽基板10上形成絕緣膜11、胞

元源極線15及絕緣膜17 (參看圖1及圖2)。

接著，如圖45所展示，藉由交替地堆疊氧化矽膜51與氮化矽膜52來形成堆疊式本體60。

繼而，在堆疊式本體60中製得多個記憶體孔(memory hole) 95。記憶體孔95在Z方向上延伸，且刺穿堆疊式本體60及絕緣膜17 (參看圖2)以到達胞元源極線15。

接著，如圖46所展示，藉由執行濕式蝕刻來致使記憶體孔95之內部表面處的氮化矽膜52之曝露表面後退。藉此，在記憶體孔95之內部表面中製得具有環形組態之凹部96。

繼而如圖47所展示，藉由沈積多晶矽且藉由執行各向同性蝕刻來選擇性地移除多晶矽而將多晶矽層91填充至凹部96中。接著，藉由氧化多晶矽層91之曝露表面來形成穿隧絕緣膜33。

接著，如圖48所展示，藉由將多晶矽填充至記憶體孔95中來形成矽支柱20。矽支柱20連接至胞元源極線15 (參看圖2)。

繼而如圖49所展示，在記憶體孔95之間的堆疊式本體60之部分中製得渠溝97。渠溝97在Y方向及Z方向上擴展，且在Z方向上刺穿堆疊式本體60，但並不刺穿絕緣膜17 (參看圖2)。

接著，如圖50所展示，藉由經由渠溝97而執行濕式蝕刻來移除氮化矽膜52。藉此，在渠溝97之內部表面處製得凹部98。在凹部98之背部表面處曝露多晶矽層91。

繼而如圖51所展示，藉由經由渠溝97及凹部98而矽化來矽化凹部98內部之多晶矽層91之曝露表面。藉此，形成金屬矽化物層92。浮動閘電極膜31包括多晶矽層91及金屬矽化物層92。

接著，如圖52所展示，在渠溝97之內部表面上形成氧化矽層93。接著，在氧化矽層93上形成高介電常數層94。氧化矽層93及高介電常數層94具有反映凹部98之圓形管狀類波紋管組態。

繼而如圖53所展示，藉由根據(例如) CVD來沈積導電材料而在高介電常數層94上形成導電膜99。亦將導電膜99填充至凹部98中，但將導電膜99形成為使得不填充渠溝97。

接著，如圖43及圖44所展示，藉由執行各向同性蝕刻而使導電膜99及高介電常數層94凹入，使得導電膜99及高介電常數層94僅餘留於氧化矽層93之凹部93a內部。藉此，餘留於凹部93a內部之導電膜99變為控制閘電極膜21。又，阻擋絕緣膜34係由氧化矽層93及高介電常數層94之剩餘部分形成。因此，製造根據實施例之半導體記憶體裝置5。

現在將描述實施例之效果。

根據實施例，因為控制閘電極膜21提供於浮動閘電極膜31及矽支柱20周圍，所以可實現具有良好可控制性之記憶體胞元。

因為浮動閘電極膜31係由導體形成，所以程式化特性良好。又，因為浮動閘電極膜31彼此分離，所以電荷之移動得以抑制；且資料保留特性高。因為可藉由自浮動閘電極膜31進行FN抹除或輔助抹除來實施抹除操作，所以抹除特性良好。

在實施例中，因為矽支柱20因在圖48所展示之製程中形成矽支柱20之前在圖47所展示之製程中形成穿隧絕緣膜33而連接至胞元源極線15 (參看圖2)，所以沒有必要藉由蝕刻來移除形成於記憶體孔95之底部表面上的穿隧絕緣膜33。因此，形成於記憶體孔95之側表面上的穿隧絕緣膜並不會因蝕刻而受到損害。

在其他方面，實施例之組態、製造方法、操作及效果類似於上述第一實施例之組態、製造方法、操作及效果。儘管在實施例中說明I狀支柱型裝置，但類似於上述第二實施例之第一修改，可使用U狀支柱型裝置。

第五實施例之修改

現在將描述第五實施例之修改。

圖54為展示根據該修改之半導體記憶體裝置的橫截面圖。

如圖54所展示，該修改為組合上述之第四實施例與第五實施例的實例。即，根據該修改之半導體記憶體裝置5a不同於根據上述第五實施例之半導體記憶體裝置5 (參看圖43)之處在於阻擋絕緣膜34未安置於最上部層級之控制閘電極膜21u與最上部層級之浮動閘電極膜31u之間；且最上部層級之控制閘電極膜21u連接至最上部層級之浮動閘電極膜31u。然而，控制閘電極膜21連接至浮動閘電極膜31所處的層級並不限於最上部層級，且可為包括最上部層級之多個層級。

現在將描述用於製造根據該修改之半導體記憶體裝置之方法。

圖55至圖57為展示用於製造根據該修改之半導體記憶體裝置之方法的橫截面圖。

首先，實施圖45至圖52所展示之製程。

接著，如圖55所展示，將抗蝕劑材料90填充至渠溝97中，且藉由曝露而使抗蝕劑材料90自上部表面側凹入。藉此，自抗蝕劑材料90曝露最上部層級之凹部93a。儘管此時可曝露包括最上部層級之多個層級的凹部93a，但在下文中之描述中描述僅曝露最上部層級之凹部93a的實例。

繼而如圖56所展示，藉由執行諸如濕式蝕刻等等之各向同性蝕刻來移除自抗蝕劑材料90曝露的高介電常數層94及氧化矽層93之部分。藉此，在最上部層級之凹部93a之背部表面處曝露金屬矽化物層92。

接著，如圖57所展示，移除抗蝕劑材料90。

繼而，實施圖53所展示之製程。因此，可製造根據該修改之半導體記憶體裝置5a。

根據該修改，類似於上述第四實施例，最上部層級之控制閘電

極膜21u及浮動閘電極膜31u可經電氣整合以用作選擇閘電極膜。因此，可形成臨限值並不波動的選擇閘極電晶體。在其他方面，該修改之組態、製造方法、操作及效果類似於上述第五實施例之組態、製造方法、操作及效果。

第六實施例

現在將描述第六實施例。

圖58及圖59為展示根據實施例之半導體記憶體裝置的橫截面圖。

圖60為展示根據實施例之半導體記憶體裝置的示意性電路圖。

圖61為展示根據實施例之半導體記憶體裝置的示意性平面圖。

圖62展示根據實施例之半導體記憶體裝置中之胞元源極線的連接關係。

在圖59中，出於方便觀看圖式起見，主要展示導電構件且省略絕緣構件。在圖60中，藉由虛線來展示控制閘電極膜21，且藉由雙點鏈線來展示源極線SL及位元線29。僅展示安置於圖式所展示之兩個末端處的連接至源極線SL之NAND串，且省略其他者。此外，僅展示控制閘電極膜21之四個層級。

如圖58及圖59所展示，根據實施例之半導體記憶體裝置6在胞元源極線15被劃分成多個部分的點上不同於根據上述第一實施例之半導體記憶體裝置1 (參見圖1至圖4)。在下文中，經劃分之胞元源極線15之每一部分被稱作「源極線SL」。源極線SL在與控制閘電極膜21之方向相同的Y方向上延伸，且係每隔一行沿著Y方向成一條直線而配置之矽支柱20被提供。源極線SL係每隔多個沿著Z方向成一條直線而配置之控制閘電極膜21被提供。絕緣膜16內埋於源極線SL之間。絕緣膜16係由(例如)氧化矽形成。

如圖60所展示，在半導體記憶體裝置6中，最上部層級之控制閘

電極膜21被視為選擇閘極線SGD，最下部層級之控制閘電極膜21被視為選擇閘極線SGS，且其他控制電極膜21被視為字線WL。如圖1所展示，沿著X方向而配置之多個字線WL在Y方向上之末端處彼此連接。沿著X方向而配置之最下部層級之多個選擇閘極線SGS亦在Y方向上之末端處彼此連接。另一方面，配置於X方向上之最上部層級之選擇閘極線SGD彼此不連接，且可將獨立電位施加至選擇閘極線SGD中之每一者。

包括穿隧絕緣膜33、浮動閘電極膜31及阻擋絕緣膜34之記憶體胞元電晶體MT形成於矽支柱20與字線WL之相交部分處。上部選擇電晶體STD形成於最上部層級之矽支柱20與選擇閘極線SGD之相交部分處。下部選擇電晶體STS形成於最下部層級之矽支柱與選擇閘極線SGS之相交部分處。

沿著一個矽支柱20而形成之上部選擇電晶體STD、多個記憶體胞元電晶體MT及下部選擇電晶體STS串聯地連接於位元線29與源極線SL之間以形成一個NAND串NS。NAND串NS沿著X方向及Y方向依矩陣組態而配置。沿著Y方向成一條直線而配置之NAND串NS連接至同一源極線SL，且分別連接至不同位元線29。沿著X方向成一條直線而配置之NAND串NS分別連接至不同源極線SL，且連接至同一位元線BL。

如圖61所展示，在半導體記憶體裝置6中，記憶體胞元區域Rm之形狀為矩形。沿著Y方向而配置之多個區塊Blk提供於記憶體胞元區域Rm中。列解碼器RD及感測放大器SA提供於周邊電路區域Rc中之記憶體胞元區域Rm附近的區域中。列解碼器RD在自記憶體胞元區域Rm觀看的情況下位於Y方向上，且連接至字線WL。感測放大器SA在自記憶體胞元區域Rm觀看的情況下位於X方向上，且連接至位元線29(BL)。

高電位輸出電路HVG及低電位輸出電路LVG提供於周邊電路區域Rc中。高電位輸出電路HGV及低電位輸出電路LVG係(例如)以4個層級而提供，且分別安置於記憶體胞元區域Rm之4個拐角附近。舉例而言，一對高電位輸出電路HVG及低電位輸出電路LVG在自列解碼器RD觀看的情況下安置於X方向側上，且在自感測放大器SA觀看的情況下安置於Y方向側上。高電位輸出電路HVG及低電位輸出電路LVG為輸出施加至源極線SL的兩個層級之源極線電位Vsl的電路，高電位輸出電路HVG輸出相對高電位，且低電位輸出電路LVG輸出相對低電位，例如，接地電位。

如圖62所展示，在每一區塊中，分別提供於在X方向上之位置彼此不同之字線正下方之區域上的源極線SL彼此不連接。另一方面，安置於彼此不同之區塊中且安置於彼此對應之字線正下方之區域上的源極線SL彼此連接。舉例而言，安置於屬於第一區塊之字線WL1正下方之區域上的源極線SL1與安置於屬於第一區塊之字線WL2正下方之區域上的源極線SL2彼此不連接。另一方面，安置於屬於第一區塊之字線WL1正下方之區域上的源極線SL1與安置於屬於第二區塊之字線WL1正下方之區域上的源極線SL1彼此連接。

現在將描述根據實施例之半導體記憶體裝置之驅動方法。

圖63A為展示選擇NAND串及非選擇NAND串的示意性電路圖，圖63B展示施加至選擇NAND串之電位，且圖63C展示施加至非選擇NAND串之電位。

如63A所展示，將描述自一個記憶體胞元電晶體MT讀出資料的狀況。在下文中，將此記憶體胞元電晶體MT描述為「選擇胞元(selection cell) MT0」，且將除此之外的記憶體胞元電晶體MT描述為「非選擇胞元(non-selection cell) MT1」。將包括選擇胞元MT0之NAND串NS描述為「選擇串(selection string) NS0」，且將除此之外的

NAND串NS描述為「非選擇串(non-selection string) NS1」。圖63B及圖63C展示施加至選擇NAND串NS0及連接至同一位元線之非選擇NAND串NS1的電位。

如圖63A至圖63C所展示，舉例而言，將0.2至0.5 V (伏特)施加至選定位元線29作為位元線電位Vbl。不將位元線電位Vbl施加至除此之外的位元線29。

如圖63B所展示，將自低電位輸出電路LVG輸出之相對低源極電位(例如，0 V (0伏特))施加至連接至選擇串NS0之源極線SL作為源極線電位Vsl。藉此，舉例而言，將大約0.2至0.5 V之低電位差施加於連接至選擇串NS0之位元線29與源極線SL之間。在此狀態下，舉例而言，將2.5至4 V施加至選擇閘極線SGD及SGS作為選擇閘極電位Vsgd及Vsgs。藉此，選擇串NS0之上部選擇電晶體STD及下部選擇電晶體STS分別進入接通狀態。

舉例而言，將4.5至7 V施加至形成非選擇胞元MT1之非選擇字線WL作為讀出電位Vread。讀出電位Vread為使得記憶體胞元電晶體MT在與由記憶體胞元電晶體MT保持之值無關的情況下進入接通狀態的電位。另一方面，將低於讀出電位Vread之電位(例如，0至5 V)施加至形成選擇胞元MT0之選擇字線WL作為字線電位Vwl。字線電位Vwl為使得記憶體胞元電晶體MT之傳導狀態取決於由記憶體胞元電晶體MT保持之值而不同的電位。在此狀態下，偵測到經由選擇串NS0而傳遞通過位元線29與源極線SL之間的電流，且藉此可讀出程式化至選擇胞元MT0中之值。

此時，致使電壓施加至作為位元線29與源極線SL之間的選擇串NS0而連接至同一位元線29之非選擇串NS，以及選擇串NS0。接著，如圖63C所展示，舉例而言，將0 V施加至非選擇串NS1之選擇閘極線SGD作為選擇閘極電位Vsgd。藉此，上部選擇電晶體STD進入關斷狀

態，且可抑制電流傳遞通過非選擇串NS1。

然而，因為將相同選擇閘極電位Vsgs施加至屬於同一區塊之所有選擇閘極線SGS，所以非選擇串NS1之下部選擇電晶體STS進入關斷狀態。出於此原因，將源極電位Vsl施加至非選擇串NS1之矽支柱20。因為將相同電位施加至同一層級中之字線WL，所以亦將讀出電位Vread或字線電位Vwl施加至非選擇串NS1之字線WL。出於此原因，當執行選擇胞元MT0之讀出操作時，致使為(Vread-Vsl)之近似強度之電壓亦施加至屬於矽支柱20與字線WL之間的非選擇串NS1之非選擇胞元MT，且有可能藉由此電壓而將電子注入至浮動閘電極膜31中且致使值被程式化。亦即，可發生讀取干擾。

接著在實施例中，如圖63C所展示，將高於連接至選擇串NS0之源極線SL (在下文中被稱作「選擇源極線」)的電壓施加至連接至非選擇串NS1之源極線SL (在下文中被稱作「非選擇源極線」)作為源極線電位Vsl。更具體而言，將自高電位輸出電路HVG輸出之相對高源極電位施加至非選擇源極線。

若將非選擇源極線之電位設定為高於選擇源極線之電位，則有可能在非選擇胞元MT1中鬆弛施加於矽支柱20與字線WL之間的電壓且抑制讀取干擾。舉例而言，在將接地電位(0 V)施加至選擇源極線且將4.5至7 V施加至字線WL作為讀出電壓Vread之狀況下，將高於0 V之電位(較佳地，1 V或更高之電位)施加至非選擇源極線。

非選擇源極線之電位可等於選擇閘極電位Vsgs。在此狀況下，非選擇串NS1之下部選擇電晶體STS進入關斷狀態。此時，因為上部選擇電晶體STD亦處於關斷狀態，所以使矽支柱20與源極線SL及位元線29分離以進入浮動狀態。與字線WL之耦合將矽支柱20之電位增加至接近讀出電位Vread。此情形亦縮減矽支柱20與字線WL之間的電壓。

在程式化操作及抹除操作中，將相同電位施加至所有源極線

SL。

現在將描述實施例之效果。

如上文所描述，在實施例中，藉由將胞元源極線15劃分成多個源極線SL，可將高於連接至選擇串之選擇源極線的電位施加至連接至非選擇串之非選擇源極線。藉此，有可能在非選擇串中鬆弛矽支柱20與字線WL之間的電壓且抑制讀取干擾。

在其他方面，實施例之組態、製造方法、操作及效果類似於上述第一實施例之組態、製造方法、操作及效果。

第七實施例

現在將描述第七實施例。

圖64為展示根據實施例之半導體記憶體裝置的橫截面圖。

圖65展示根據實施例之半導體記憶體裝置中之胞元源極線的連接關係。

如圖64及圖65所展示，在根據實施例之半導體記憶體裝置7中，一個源極線SL係每隔兩列沿著Y方向而配置NAND串NS被提供。亦即，沿著Y方向而配置之多個矽支柱20連接至同一源極線SL，且在X方向上之兩個鄰近矽支柱20連接至同一源極線SL。舉例而言，包夾層間絕緣膜23之兩個矽支柱20連接至同一源極線SL。

根據實施例，因為每一源極線SL與上述第六實施例相比較可厚，所以可縮減每一源極線SL之互連電阻。此情形允許半導體記憶體裝置7以高速度而操作。

在其他方面，實施例之組態、操作及效果類似於上述第六實施例之組態、操作及效果。

第八實施例

現在將描述第八實施例。

圖66為展示根據實施例之半導體記憶體裝置的橫截面圖。

圖67展示根據實施例之半導體記憶體裝置中之胞元源極線的連接關係。

如圖66及圖67所展示，在根據實施例之半導體記憶體裝置8中，存在屬於每一區塊Blk之兩個源極線SL，且源極線SL在鄰近區塊Blk中被共用。亦即，源極線SL之數目與區塊Blk之數目相同，且源極線及區塊經配置為移位半循環。

在安置於區塊Blk之間的渠溝58 (參見圖11A)中，提供導電構件18。屬於鄰近區塊Blk且彼此連接之源極線SL之群組安置於包夾導電構件18之位置處。導電構件18為板狀且沿著YZ平面而延伸，且其下部末端連接至源極線SL。絕緣膜19提供於導電構件18之兩個側表面上，且將導電構件18與控制閘電極膜21隔離。連接至導電構件18之源極線SL連接至在自導電構件18觀看的情況下安置於X方向上之兩個側上的矽支柱20。

在Y方向上延伸之上部層源極線30提供於導電構件18上，且連接至導電構件18之上部末端。上部層源極線30有可能連接至高電位輸出電路HVG及低電位輸出電路LVG。藉此，將源極電位經由上部層源極線30及導電構件18而自高電位輸出電路HVG或低電位輸出電路LVG供應至源極線SL。

根據實施例，與第六實施例及第七實施例相比較，可進一步縮減源極線SL之電阻。另一方面，根據第六實施例，因為可將相對高源極電位施加至每一區塊Blk中除了連接至選擇串NS0之源極線SL以外的所有源極線，所以可有效地抑制讀取干擾。

在其他方面，實施例之組態、操作及效果類似於上述第六實施例之組態、操作及效果。

第九實施例

現在將描述第九實施例。

圖68為展示根據實施例之半導體記憶體裝置的透視圖。

如圖68所展示，在根據實施例之半導體記憶體裝置9a中，未提供胞元源極線15 (參見圖1及圖2)，且矽支柱20之下部末端連接至矽基板10。雜質被引入至矽基板10之上部部分中，且該上部部分導電。藉此，矽基板10之上部部分充當源極線。導電構件18 (參見圖66)提供於安置於區塊Blk之間的渠溝58 (參見圖11A)中，且可將源極電位施加至矽基板10。

根據實施例，與上述第一實施例相比較，可省略胞元源極線。

在其他方面，實施例之組態、製造方法、操作及效果類似於上述第一實施例之組態、製造方法、操作及效果。

雜質濃度高於周邊之接觸層可形成於矽基板10中之渠溝53 (參見圖9A)正下方的區域中。

第十實施例

現在將描述第十實施例。

圖69為展示根據實施例之半導體記憶體裝置的透視圖。

如圖69所展示，在根據實施例之半導體記憶體裝置9b中，未提供胞元源極線15 (參見圖1及圖2)，且在X方向上之兩個鄰近矽支柱20之下部末端被連接。在Y方向上延伸之源極線49提供於互連件27與位元線29之間。在使下部末端被連接之兩個矽支柱20之中，一個矽支柱20經由導孔28而連接至位元線29，且另一矽支柱20連接至源極線49。藉此，由兩個矽支柱20製成之U狀矽構件連接於位元線29與源極線49之間。

根據實施例，在形成包括矽支柱20及控制閘電極膜21或其類似者之堆疊式本體25之後，可形成源極線49。出於此原因，源極線49之材料略微受到後續製程限定，且材料選擇之自由度高。藉此，舉例而言，源極線49可由具有相對低熔點之金屬材料形成。因此，舉例而

言，容易縮減源極線49之互連電阻。

在其他方面，實施例之組態、製造方法、操作及效果類似於上述第一實施例之組態、製造方法、操作及效果。

根據上述實施例，可實現一種具有良好資料保留特性之半導體記憶體裝置及一種用於製造該半導體記憶體裝置之方法。

雖然已描述某些實施例，但此等實施例係僅作為實例被呈現，且並不意欲限制本發明之範疇。實際上，可以多種其他形式來體現本文所描述之新穎實施例；此外，可在不脫離本發明之精神的情況下進行本文所描述之實施例之形式的各種省略、取代及改變。隨附申請專利範圍及其等效者意欲涵蓋將屬於本發明之範疇及精神的此等形式或修改。另外，上述實施例可被相互組合。

【符號說明】

1	半導體記憶體裝置
1a	半導體記憶體裝置
2	半導體記憶體裝置
2a	半導體記憶體裝置
2b	半導體記憶體裝置
2c	半導體記憶體裝置
3	半導體記憶體裝置
3a	半導體記憶體裝置
4	半導體記憶體裝置
5	半導體記憶體裝置
5a	半導體記憶體裝置
6	半導體記憶體裝置
7	半導體記憶體裝置
8	半導體記憶體裝置

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9	半導體記憶體裝置
9a	半導體記憶體裝置
9b	半導體記憶體裝置
10	矽基板
10a	上部表面
11	絕緣膜
12	導電層
13	互連層
14	導電層
15	胞元源極線
16	絕緣膜
17	絕緣膜
18	導電構件
19	絕緣膜
20	矽支柱
21	控制閘電極膜
21a	上部表面
21b	下部表面
21u	控制閘電極膜
22	集合
23	層間絕緣膜
24	層間絕緣膜
25	堆疊式本體
26	硬質遮罩
27	互連件
28	導孔

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29	位元線
30	上部層源極線
31	浮動閘電極膜
31a	上部表面
31b	下部表面
31u	浮動閘電極膜
33	穿隧絕緣膜
34	阻擋絕緣膜
35	氮化矽層
36	氧化矽層
37	氮化矽層
38	導孔
39	字線
40c	通道區域
40d	汲極區域
40s	源極區域
41	閘極絕緣膜
42	導電層
43	互連層
45	閘電極
46	電晶體
49	源極線
50	氧化矽層
51	氧化矽膜
52	氮化矽膜
53	渠溝

54	凹部
55	多晶矽膜
56	多晶矽膜
57	絕緣膜
58	渠溝
59	凹部
59u	凹部
60	堆疊式本體
61	鎢膜
62	硬質遮罩
62a	開口
63	通孔
65	矽支柱
71	氧化矽膜
72	多晶矽膜
73	堆疊式本體
75	渠溝
77	多晶矽膜
78	渠溝
79	凹部
81	鎢膜
82	通孔
85	電荷儲存膜
86	氣隙
87	氮化矽膜
88	氮化矽膜

89	加強構件
90	抗蝕劑材料
91	多晶矽層
92	金屬矽化物層
93	氧化矽層
93a	凹部
94	高介電常數層
95	記憶體孔
96	凹部
97	渠溝
98	凹部
99	導電膜
Blk	區塊
HVG	高電位輸出電路
L1	長度
L2	長度
LVG	低電位輸出電路
MT	記憶體胞元電晶體
MT0	選擇胞元
MT1	非選擇胞元
NS	NAND串
NS0	選擇NAND串
Rc	周邊電路區域
RD	列解碼器
Rm	記憶體胞元區域
SA	感測放大器

SGD	選擇閘極線
SGS	選擇閘極線
SL	源極線
SL1	源極線
SL2	源極線
STD	上部選擇電晶體
STS	下部選擇電晶體
Vbl	位元線電位
Vread	讀出電位
Vsgd	選擇閘極電位
Vsgs	選擇閘極電位
Vsl	源極線電位
Vwl	字線電位
WL	字線
X	方向
Y	方向
Z	方向

201539724

發明摘要

※ 申請案號：104100803

※ 申請日： 104.1.9 ※IPC 分類：H01L 27/115 (2006.01)

【發明名稱】

半導體記憶體裝置及其製造方法

SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME

【中文】

根據一項實施例，一種半導體記憶體裝置包括：一基板；一半導體支柱，其提供於該基板上以在一垂直方向上延伸；複數個第一電極膜，其提供於該半導體支柱側方以在一第一方向上延伸。該複數個第一電極膜經安置為沿著該垂直方向彼此分離。該半導體記憶體裝置進一步包括提供於該半導體支柱與該等第一電極膜之間的複數個第二電極膜。該複數個第二電極膜經安置為沿著該垂直方向彼此分離。該半導體記憶體裝置進一步包括：提供於該半導體支柱與該等第二電極膜之間的一第一絕緣膜；及提供於該第二電極膜與該第一電極膜之間的一第二絕緣膜。

【英文】

According to one embodiment, a semiconductor memory device includes a substrate, a semiconductor pillar provided on the substrate to extend in a vertical direction, a plurality of first electrode films provided sideward of the semiconductor pillar to extend in a first direction. The plurality of first electrode films are disposed to be separated from each other along the vertical direction. The semiconductor memory device further includes a plurality of second electrode films provided between the semiconductor pillar and the first electrode films. The plurality of second electrode films are disposed to be separated from each other along the vertical direction. The semiconductor memory device further includes a first insulating film provided between the semiconductor pillar and the second electrode films, and a second insulating film provided between the second electrode film and the first electrode film.

【代表圖】

【本案指定代表圖】：第（1）圖。

【本代表圖之符號簡單說明】：

1	半導體記憶體裝置
10a	上部表面
11	絕緣膜
12	導電層
13	互連層
14	導電層
15	胞元源極線
20	矽支柱
21	控制閘電極膜
23	層間絕緣膜
27	互連件
28	導孔
29	位元線
31	浮動閘電極膜
38	導孔
39	字線
Rm	記憶體胞元區域
X	方向
Y	方向
Z	方向

【本案若有化學式時，請揭示最能顯示發明特徵的化學式】：

(無)

申請專利範圍

1. 一種半導體記憶體裝置，其包含：

一基板；

一半導體支柱，其提供於該基板上以在一垂直方向上延伸；

複數個第一電極膜，其提供於該半導體支柱側方以在一第一方向上延伸，該複數個第一電極膜經安置為沿著該垂直方向彼此分離；

複數個第二電極膜，其提供於該半導體支柱與該等第一電極膜之間，該複數個第二電極膜經安置為沿著該垂直方向彼此分離；

一第一絕緣膜，其提供於該半導體支柱與該等第二電極膜之間；及

一第二絕緣膜，其提供於該第二電極膜與該第一電極膜之間。

2. 如請求項1之裝置，其中

該第一絕緣膜之一等效氧化物厚度厚於該第二絕緣膜之一等效氧化物厚度，且

該第一絕緣膜之一介電常數低於該第二絕緣膜之一介電常數。

3. 如請求項2之裝置，其中該第二絕緣膜包括：

一第一層，其提供於該第一電極膜側上以覆蓋該第一電極膜之一上部表面及一下部表面；及

一第二層，其提供於該第二電極膜側上以覆蓋該第二電極膜之一上部表面及一下部表面。

4. 如請求項1之裝置，其中

該第二絕緣膜之一等效氧化物厚度厚於該第一絕緣膜之一等效氧化物厚度，且

該第二絕緣膜之一介電常數低於該第一絕緣膜之一介電常數。

5. 如請求項4之裝置，其中該第一絕緣膜沿著該半導體支柱之一側表面而安置。

6. 如請求項1之裝置，其中

提供複數個該等半導體支柱，

該複數個半導體支柱沿著該第一方向及與該第一方向相交之一第二方向依一矩陣組態而配置，如自上方所觀看，

該第一電極膜未安置於沿著該第一方向而配置之該等半導體支柱之間，且

當沿著該第二方向而配置之該等半導體支柱被組織成每隔兩個相互鄰近半導體支柱若干集合時，且當該等第一電極膜中之兩者定位於該等集合之間時，該等第一電極膜未安置於屬於每一集合之該兩個半導體支柱之間。

7. 如請求項6之裝置，其中屬於該集合之該兩個半導體支柱被形成為一個本體。

8. 如請求項6之裝置，其中該半導體支柱側上之該第二電極膜之一末端部分在該第一方向上的一長度短於該第一電極膜側上之該第二電極膜之一末端部分在該第一方向上的一長度。

9. 如請求項6之裝置，其中在該等半導體支柱之間、在該垂直方向上彼此鄰近之該等第一電極膜之間及/或在該垂直方向上彼此鄰近之該等第二電極膜之間的至少一個部位中製得一氣隙。

10. 如請求項1之裝置，其中該等第二電極膜提供於該半導體支柱周圍，如自上方所觀看，且該等第一電極膜提供於該等第二電極

膜周圍，如自上方所觀看。

11. 如請求項1之裝置，其中針對最上部層級或針對包括該最上部層級之複數個層級，該第二絕緣膜未安置於該第一電極膜與該第二電極膜之間，且針對該最上部層級或針對包括該最上部層級之該複數個層級，該第一電極膜連接至該第二電極膜。

12. 如請求項1之裝置，其中該第二絕緣膜針對該等第一電極膜中之每一者沿著該垂直方向而劃分。

13. 如請求項1之裝置，其進一步包含：

一胞元源極線，其提供於該基板與該半導體支柱之間以連接至該半導體支柱之一下部末端；

一位元線，其提供於該半導體支柱上以連接至該半導體支柱之一上部末端；

一第三絕緣膜，其提供於該基板與該胞元源極線之間；

一源極區域及一汲極區域，該源極區域及該汲極區域被形成為在該半導體支柱正下方之一區域遠端的該基板之一區域中彼此分離；

一第四絕緣膜，其提供於該源極區域與該汲極區域之間的該基板之一區域正上方的一區域中；及

一閘電極，其提供於該第四絕緣膜上。

14. 如請求項1之裝置，其進一步包含：

其他半導體支柱；及

複數個源極線，其提供於該基板與該等半導體支柱之間，

該複數個源極線中之一者連接至該半導體支柱中之一者的一下部末端。

15. 如請求項14之裝置，其進一步包含：

一第一電位產生電路，其輸出一第一電位；及

一第二電位產生電路，其輸出高於該第一電位之一第二電位，

該等源極線包括一第一源極線及一第二源極線，

在該第一電位產生電路將該第一電位施加至該第一源極線之狀況下，該第二電位產生電路將該第二電位施加至該第二源極線。

16. 如請求項14之裝置，其中

該等源極線中之一者連接至沿著該第一方向成一條直線而配置之該等半導體支柱。

17. 如請求項14之裝置，其中

該等源極線中之一者連接至沿著該第一方向成兩條直線而配置之該等半導體支柱。

18. 如請求項14之裝置，其進一步包含：

一導電構件，其提供於該等半導體支柱之間且在該第一方向上延伸，該導電構件之一下部末端連接至該等源極線中之一者，

連接至該導電構件之該等源極線連接至在自該導電構件觀看的情況下在與該第一方向相交之一第二方向上安置於兩個側上的該半導體支柱。

19. 一種用於製造一半導體記憶體裝置之方法，其包含：

藉由交替地堆疊一絕緣膜與一第一膜而在一基板上形成一堆疊式本體；

在該堆疊式本體中製得一第一渠溝以在一第一方向上延伸；

藉由致使該第一渠溝之一內部表面處的該第一膜之一曝露表面後退來製得一第一凹部；

在該第一渠溝之該內部表面上形成一第一絕緣層；

在該第一絕緣層上形成一第一導電膜；

藉由蝕刻及餘留位於該第一凹部內部的該第一導電膜之另一部分及該第一絕緣層之另一部分來移除位於該第一凹部外部的該第一導電膜之一部分及該第一絕緣層之一部分；

在該第一渠溝之該內部表面上形成一第一絕緣膜；

在該第一絕緣膜上形成一半導體膜；

在該等第一渠溝之間的該堆疊式本體中製得一第二渠溝以在該第一方向上延伸；

藉由經由該第二渠溝而移除該第一膜來製得一第二凹部；

在該第二凹部之一內部表面上形成一第二絕緣層；

在該第二凹部內部形成一第二導電膜；及

沿著該第一方向劃分該半導體膜及該第一導電膜，

由該第一絕緣層及該第二絕緣層製成之一第二絕緣膜之一等效氧化物厚度薄於該第一絕緣膜之一等效氧化物厚度，該第二絕緣膜之一介電常數高於該第一絕緣膜之一介電常數。

20. 如請求項19之方法，其進一步包含在該半導體膜之該形成之後及製得在該第二渠溝之前將一層間絕緣膜填充至該第一渠溝中，

製得該第一渠溝包括：

在該堆疊式本體上依在該第一方向上延伸之一線與空間組態而形成一第一遮罩；及

使用該第一遮罩執行各向異性蝕刻，

沿著該第一方向劃分該半導體膜及該第一導電膜包括：

在該第一遮罩上依在與該第一方向相交之一第二方向上延伸之一線與空間組態而形成一第二遮罩；

藉由使用該第二遮罩及該第一遮罩執行各向異性蝕刻來選

擇性地移除該層間絕緣膜及該半導體膜而製得一通孔；及

經由該通孔而執行該第一導電膜之各向同性蝕刻。

21. 如請求項19之方法，其進一步包含：製得在該第一凹部之後及在該第一絕緣層之該形成之前，在該第一凹部之一背部表面上形成一第二膜，該第二膜係由不同於該第一膜之一材料的一材料製成，

製得該第二凹部包括使用該第二膜作為一擋止件來移除該第一膜。

22. 一種用於製造一半導體記憶體裝置之方法，其包含：

藉由交替地堆疊一絕緣膜與一第一導電膜而在一基板上形成一堆疊式本體；

在該堆疊式本體中製得一第一渠溝以在一第一方向上延伸；

在該第一渠溝之一內部表面上形成一第一絕緣膜；

在該第一絕緣膜上形成一半導體膜；

在該等第一渠溝之間的該堆疊式本體中製得一第二渠溝以在該第一方向上延伸；

藉由致使該第二渠溝之一內部表面處的該第一導電膜之一曝露表面後退來製得一凹部；

在該凹部之一內部表面上形成一第二絕緣膜，該第二絕緣膜之一等效氧化物厚度厚於該第一絕緣膜之一等效氧化物厚度，該第二絕緣膜之一介電常數低於該第一絕緣膜之一介電常數；

在該凹部內部形成一第二導電膜；及

沿著該第一方向劃分該半導體膜及該第一導電膜。

圖式

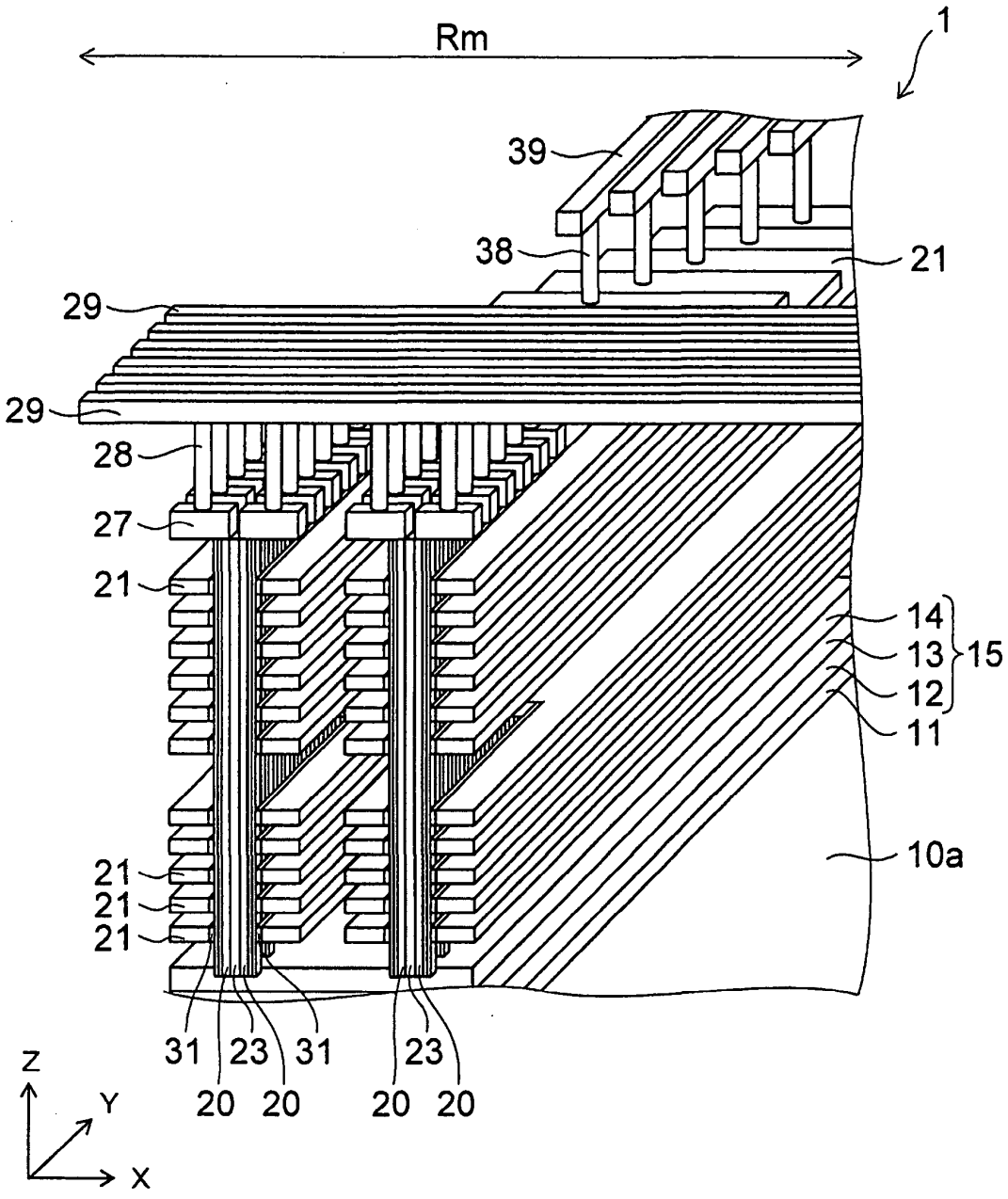


圖1

Micron Ex. 1002, p. 315
Micron v. YMTC
IPR2024-00789

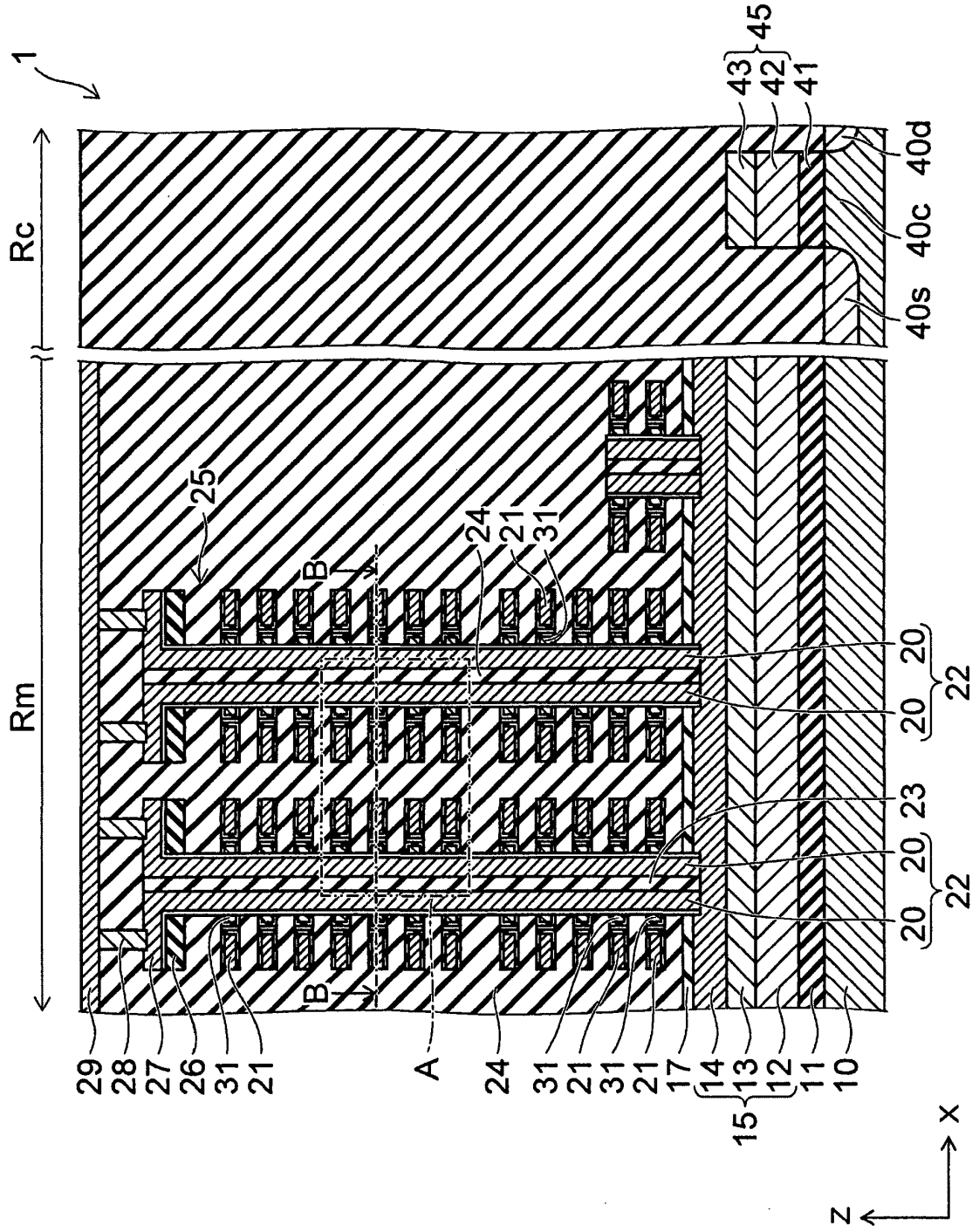

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40d
40c
40s
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Rm
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圖2

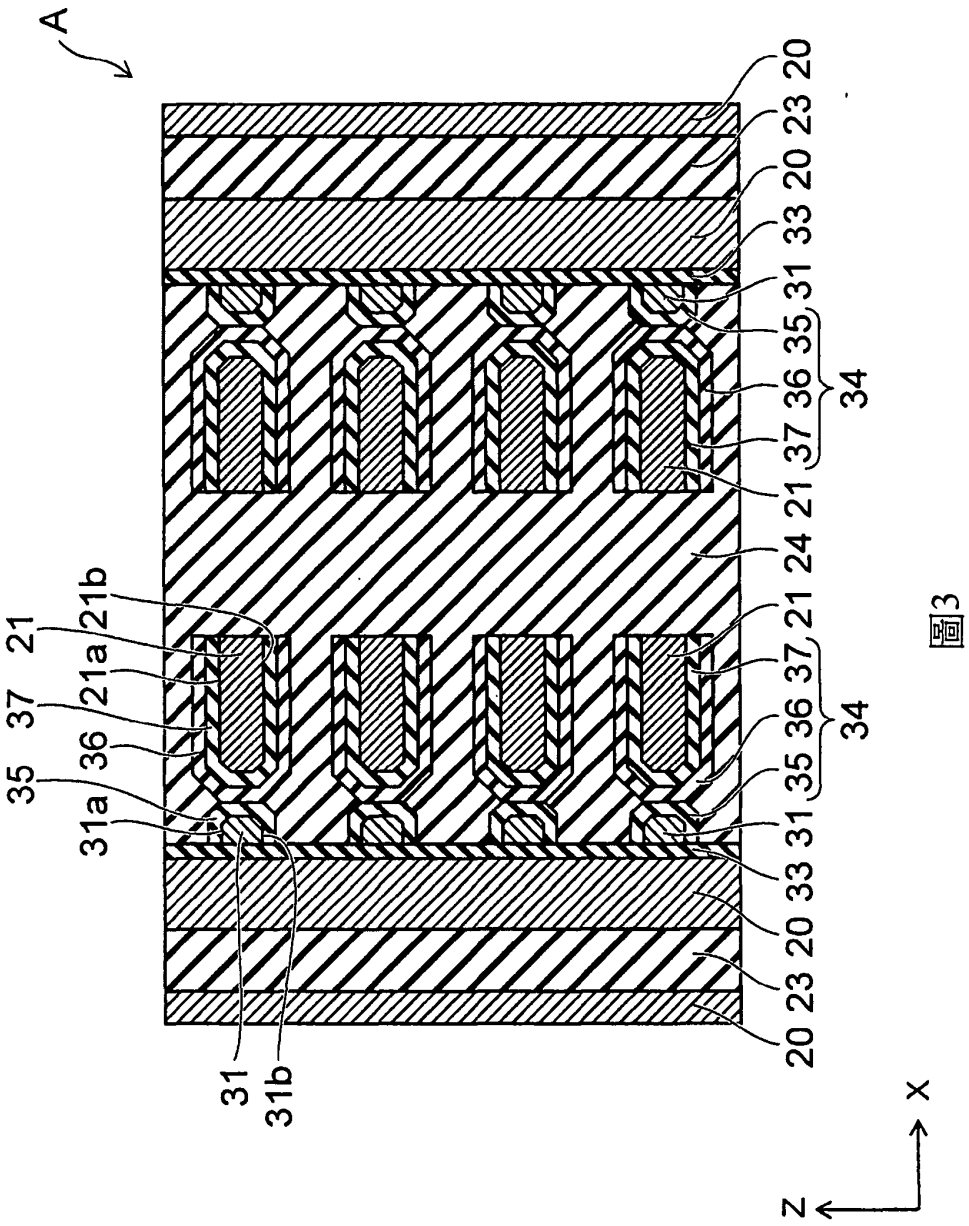


圖3

Micron Ex. 1002, p. 317
Micron v. YMTC
IPR2024-00789

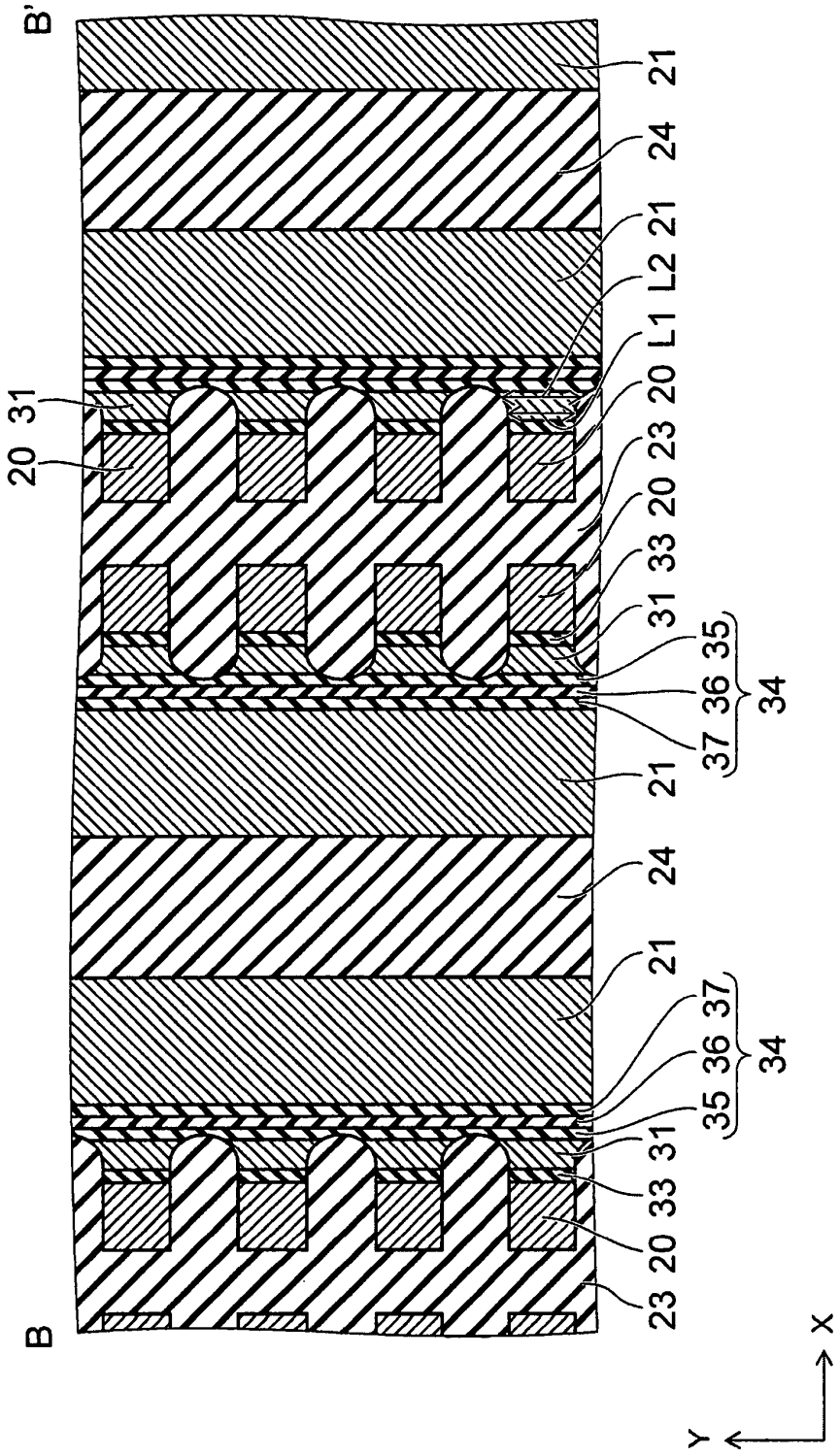

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圖4

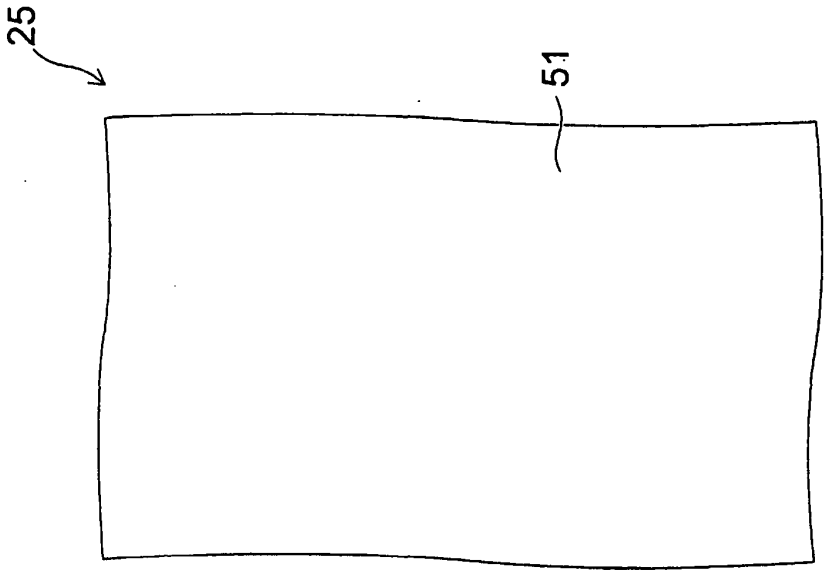


圖5B

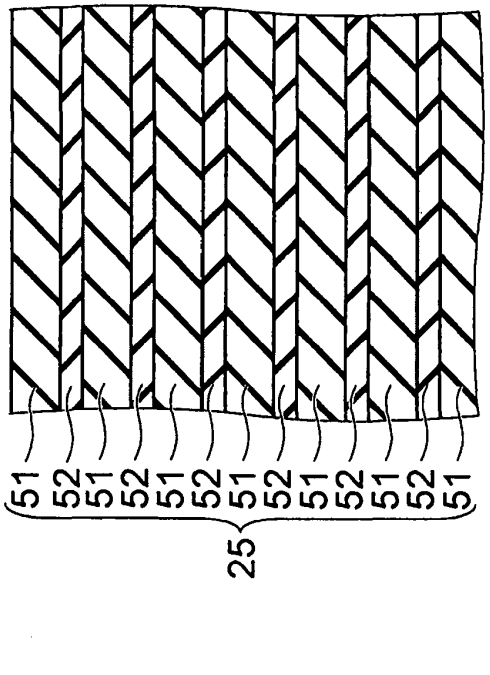


圖5A

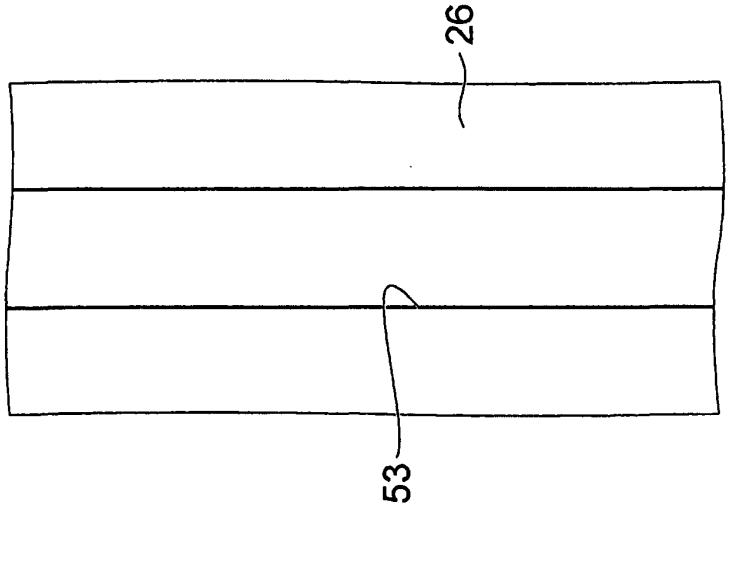


圖6B

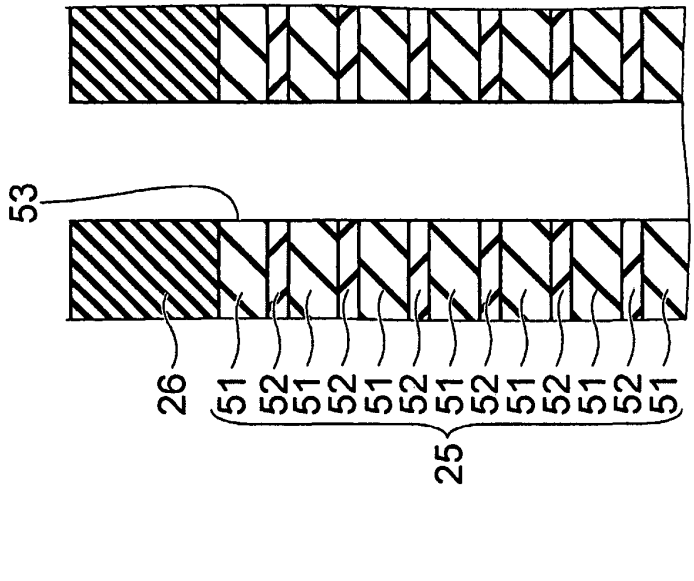


圖6A

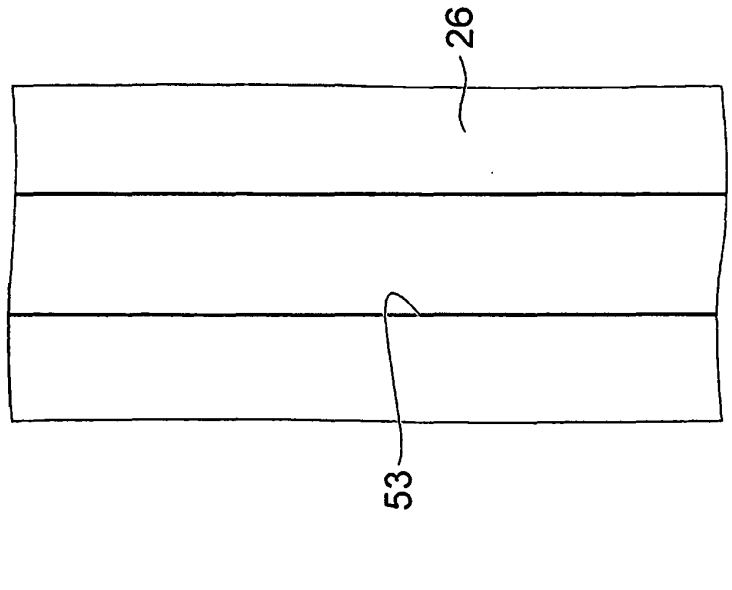


圖7B

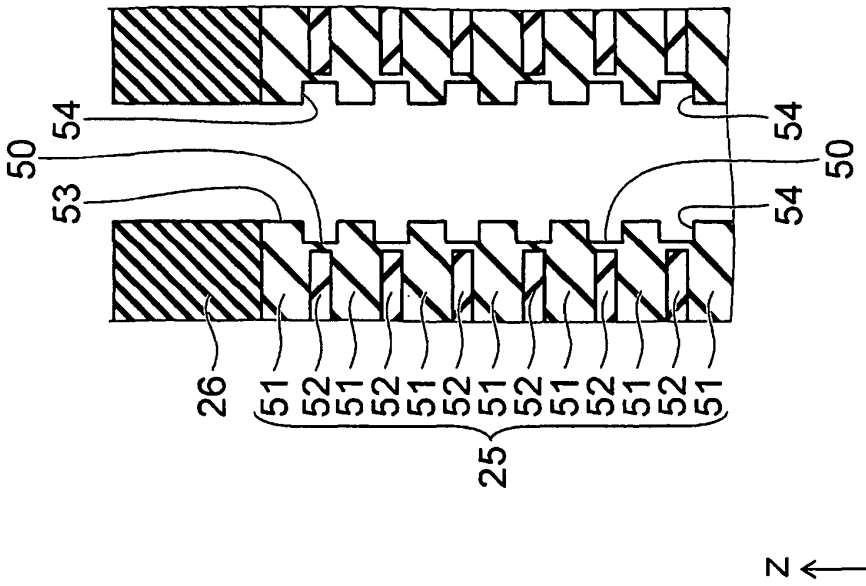


圖7A

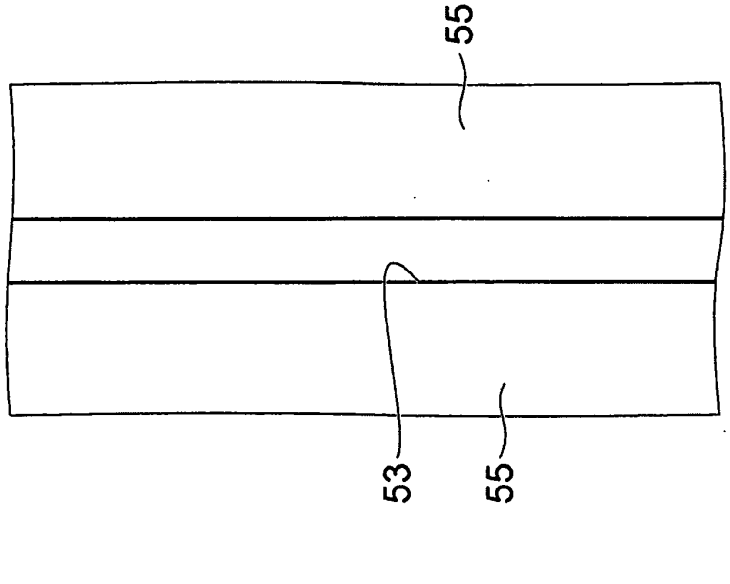


圖8B

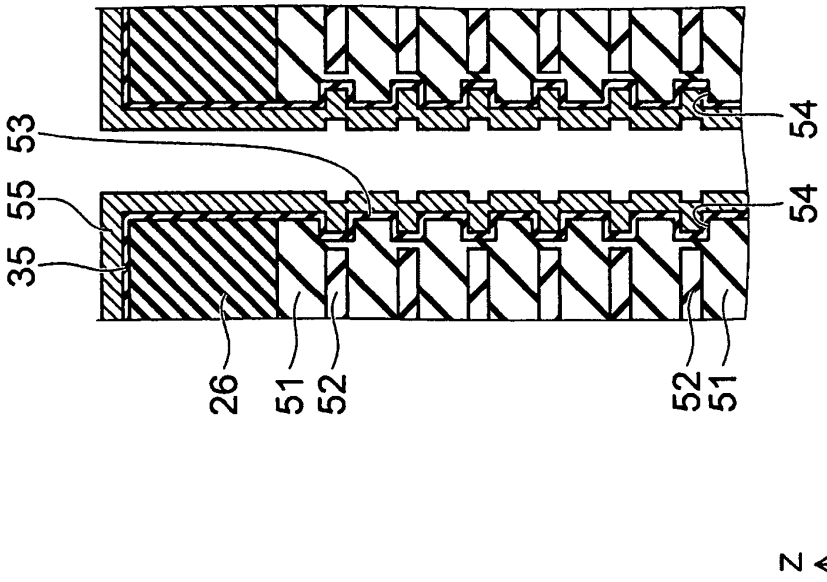


圖8A

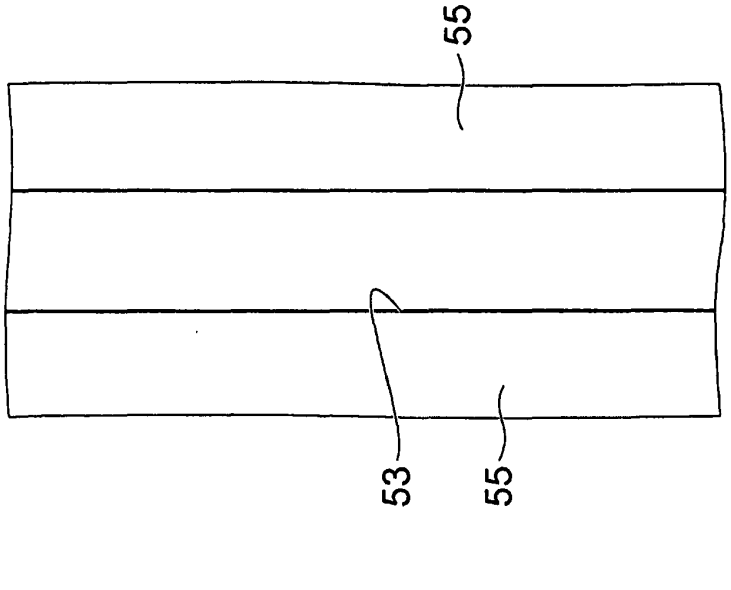


圖9B

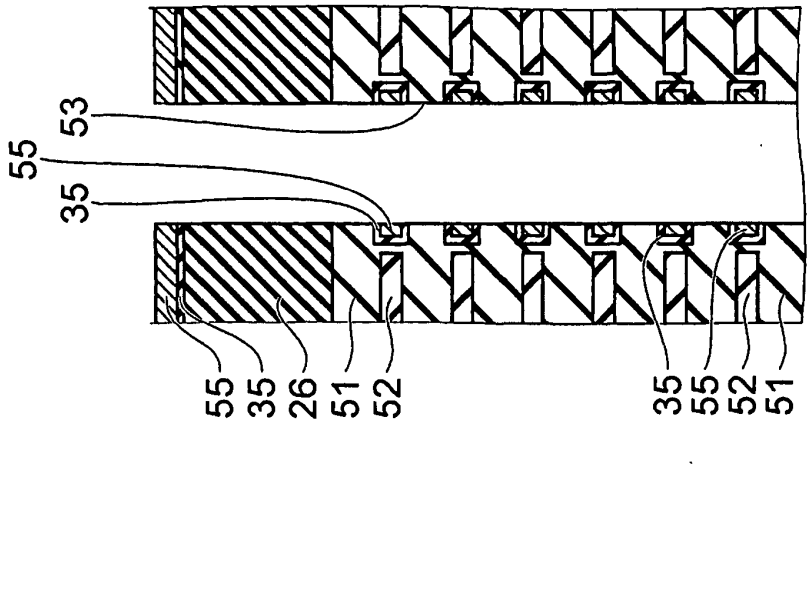


圖9A

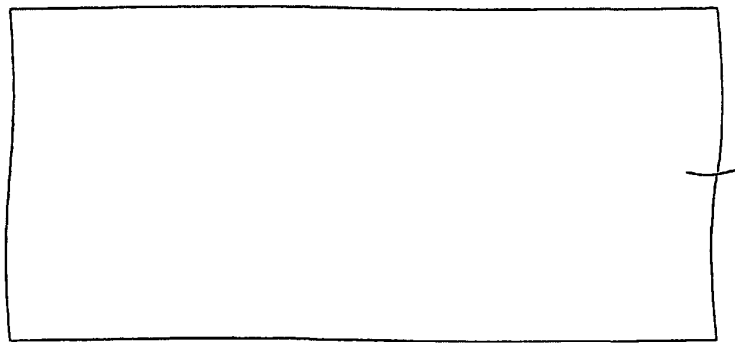


圖10B

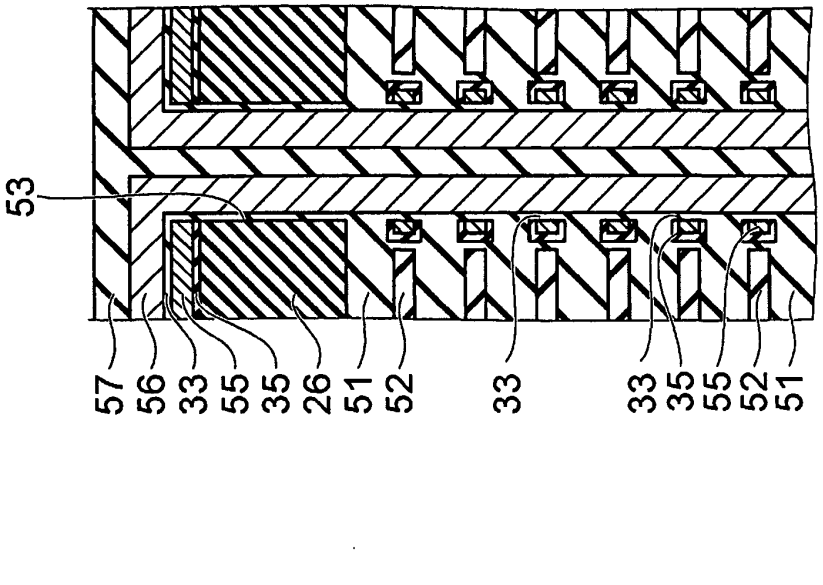


圖10A

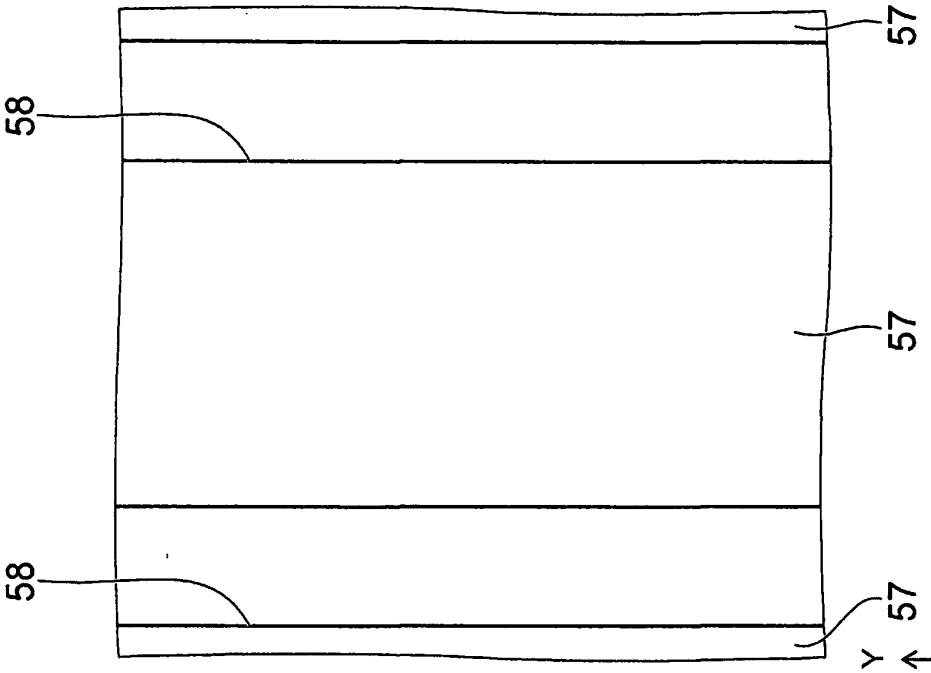


圖11B

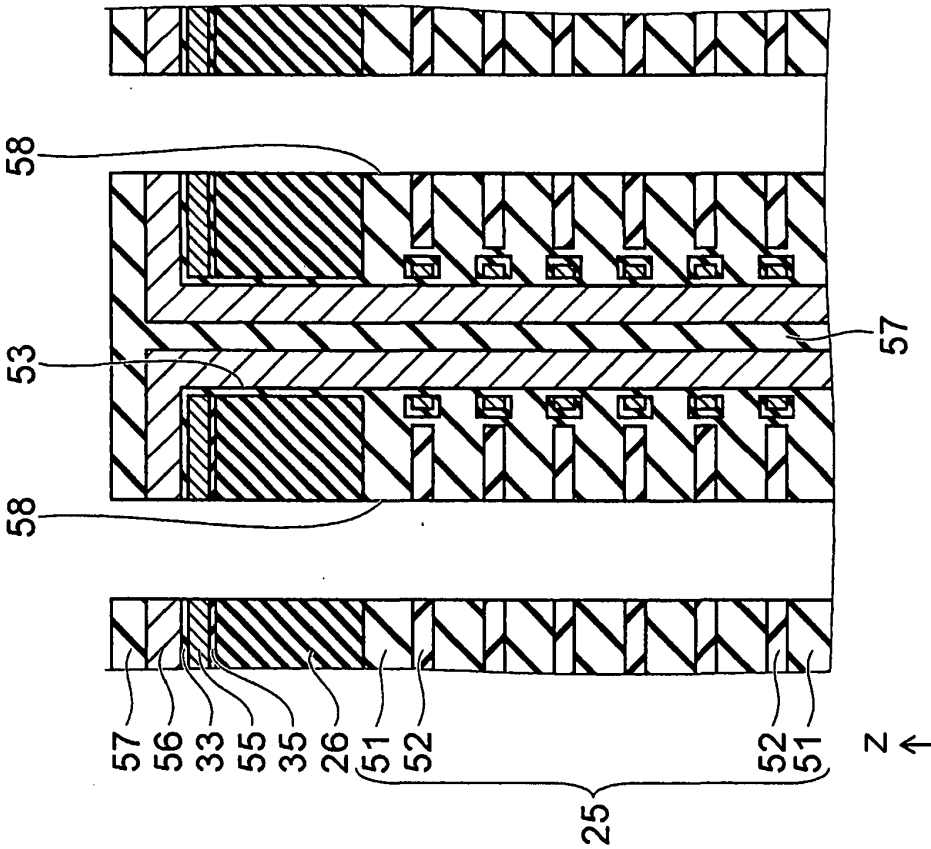


圖11A

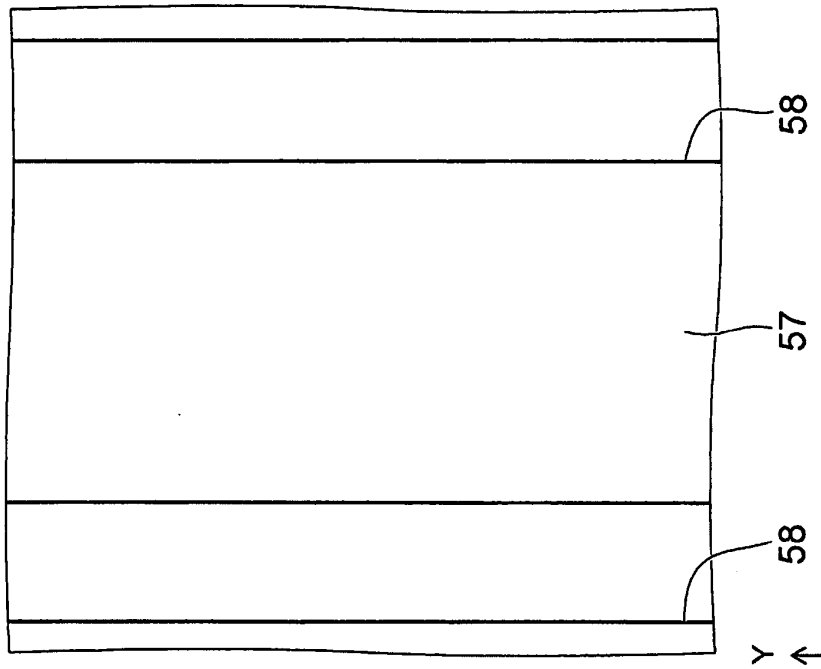


圖12B

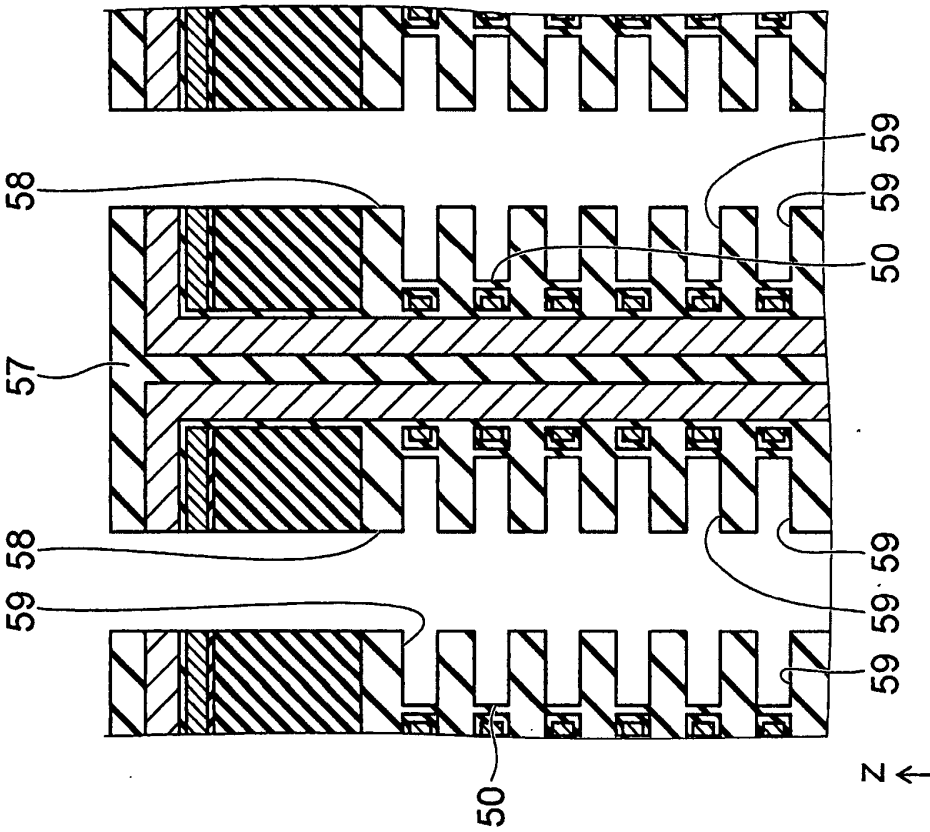


圖12A

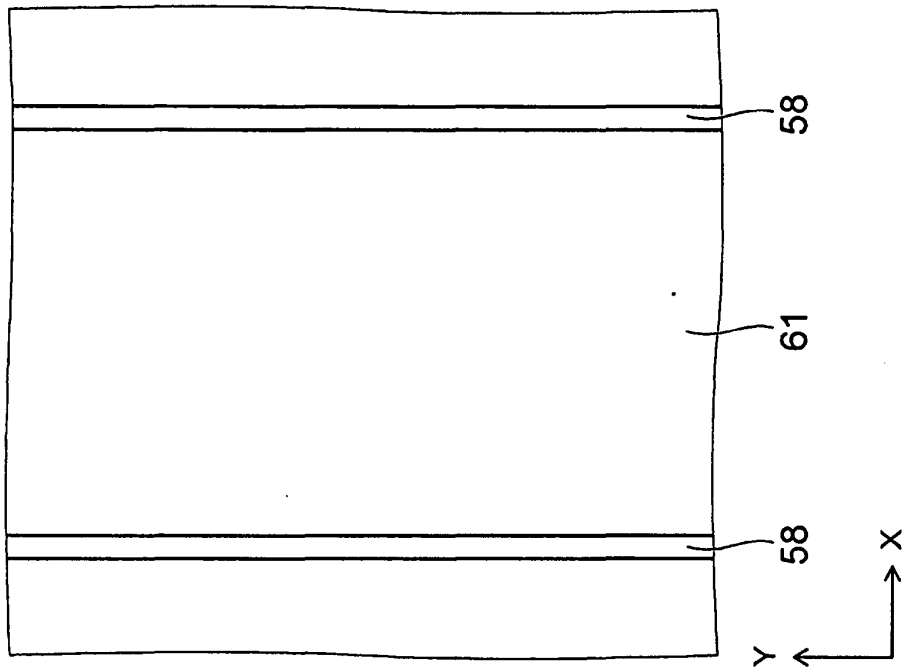


圖13B

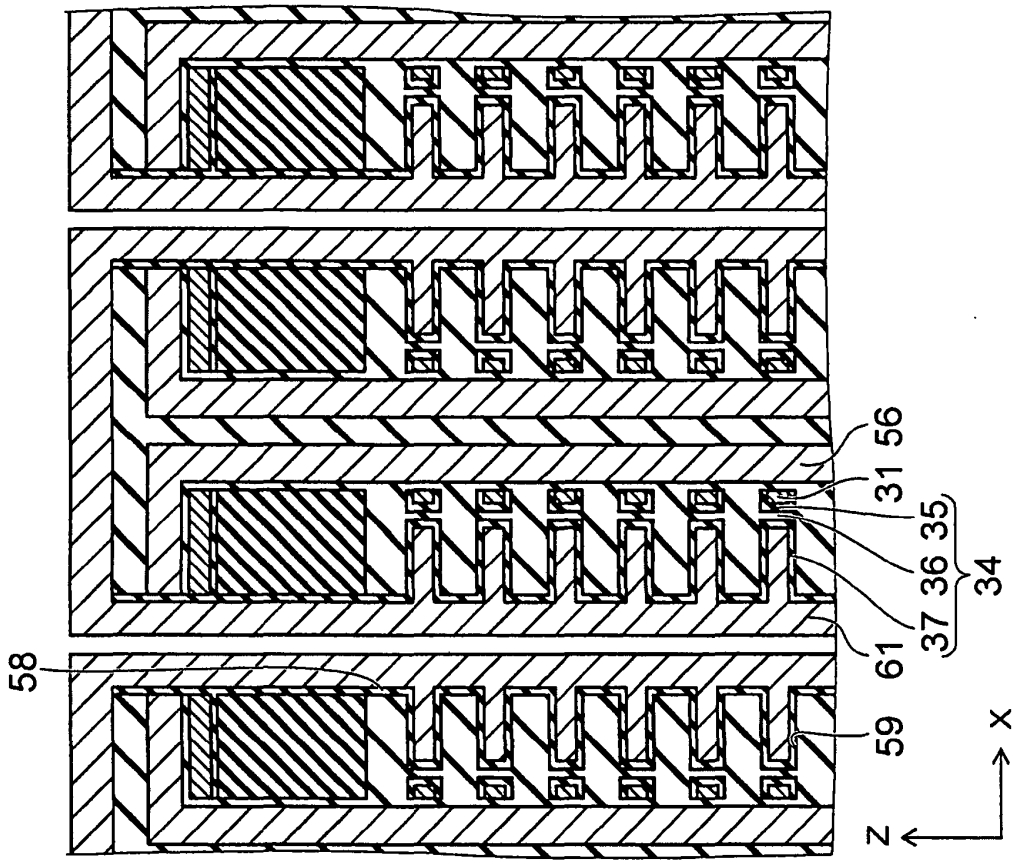


圖13A

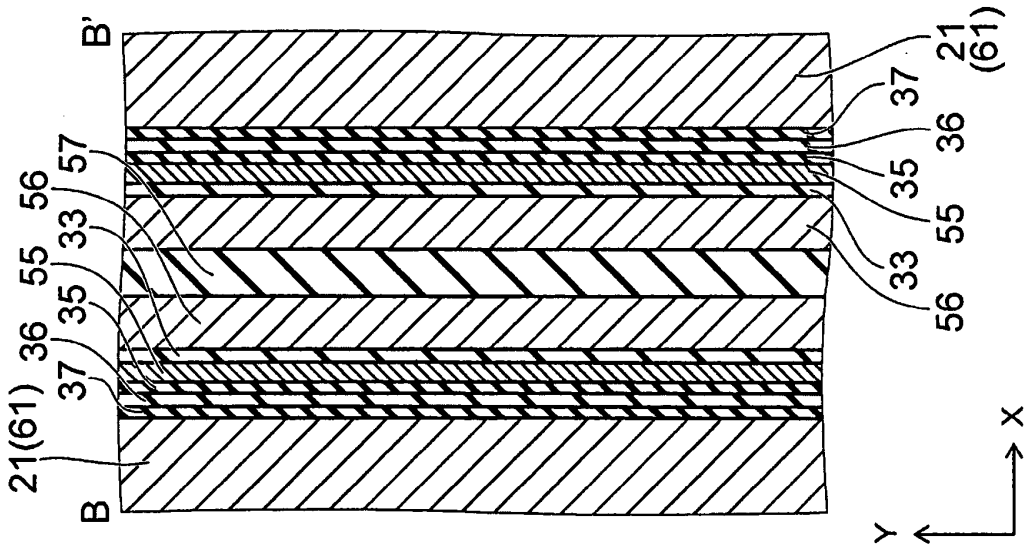

B'
B
21(61)
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21
(61)
37
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56
X
Y

圖14B

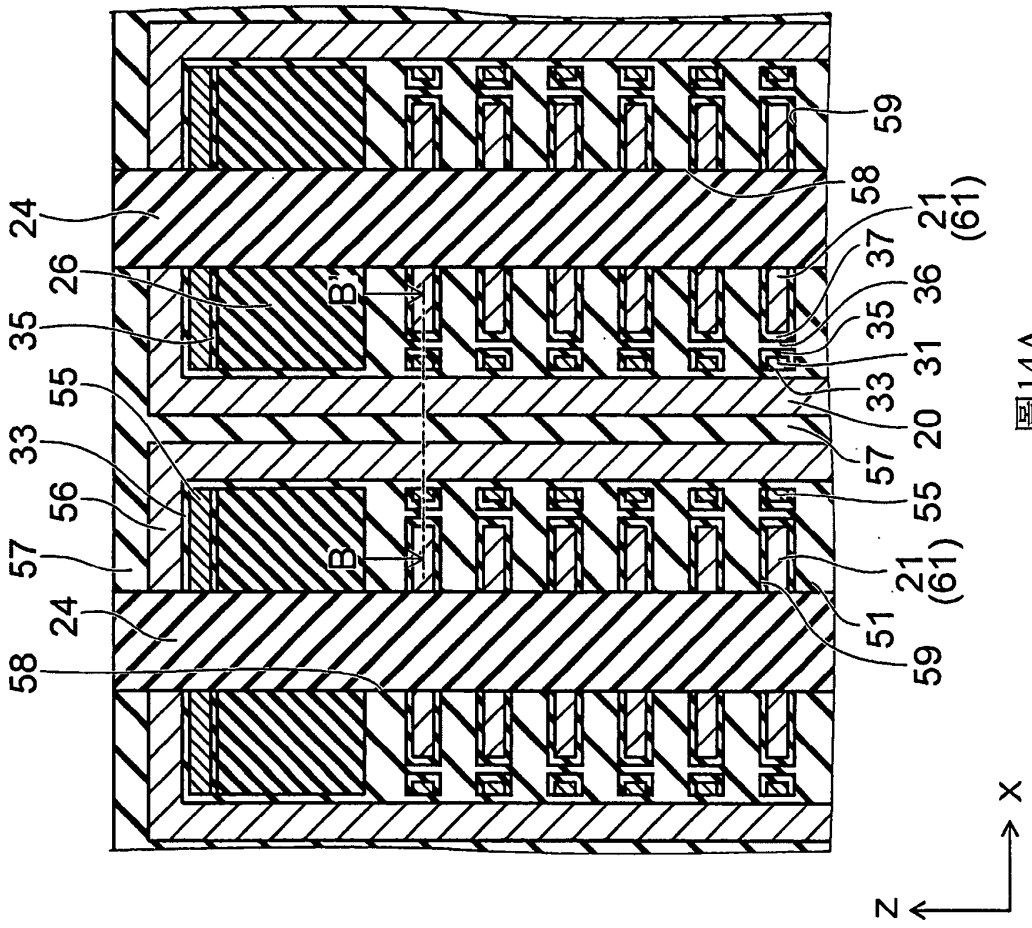

24
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35
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B'
B'
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58
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(61)
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20
57
55
21
(61)
51
59
X
Z

圖14A

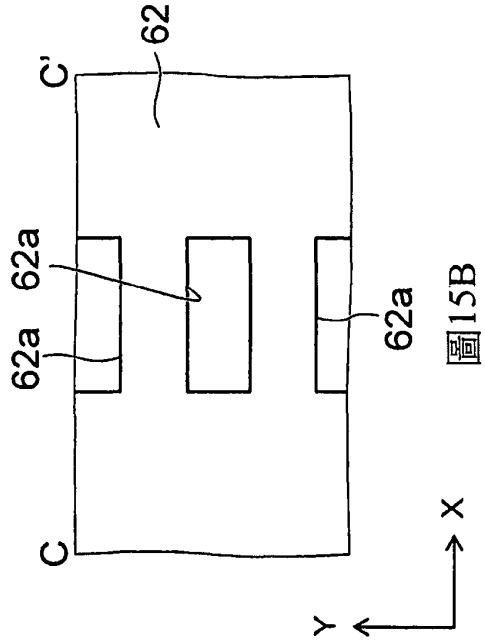


圖15B

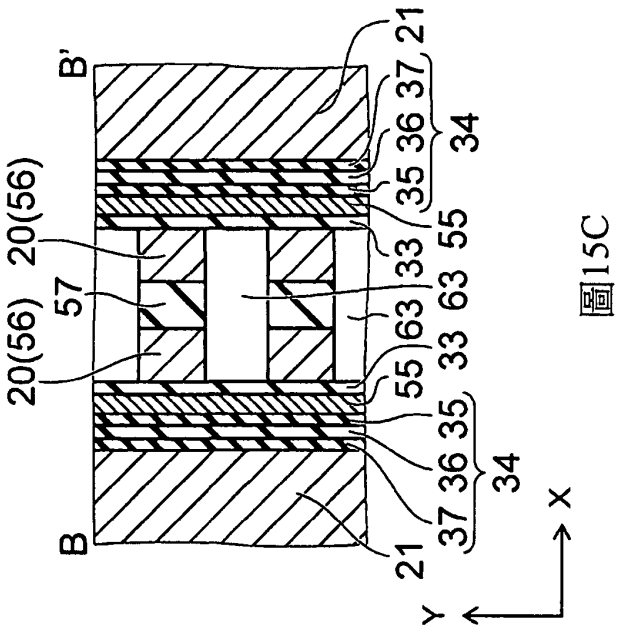


圖15C

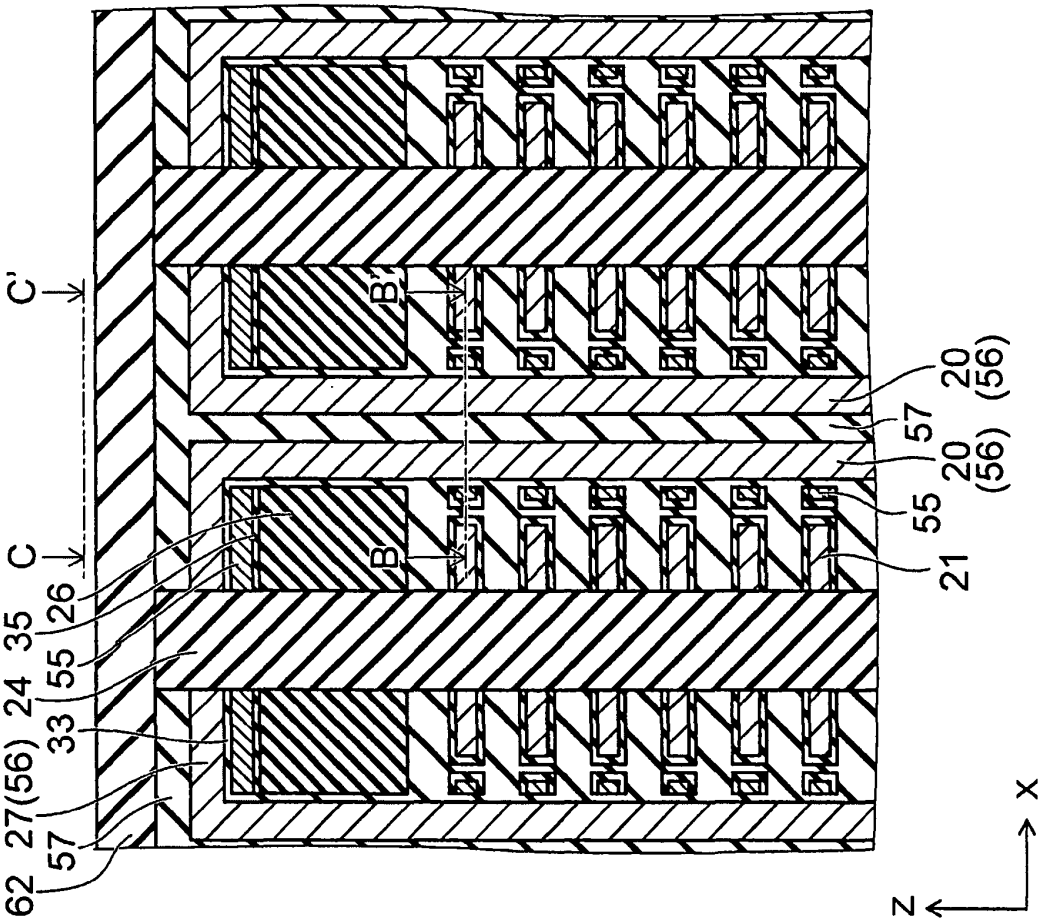


圖15A

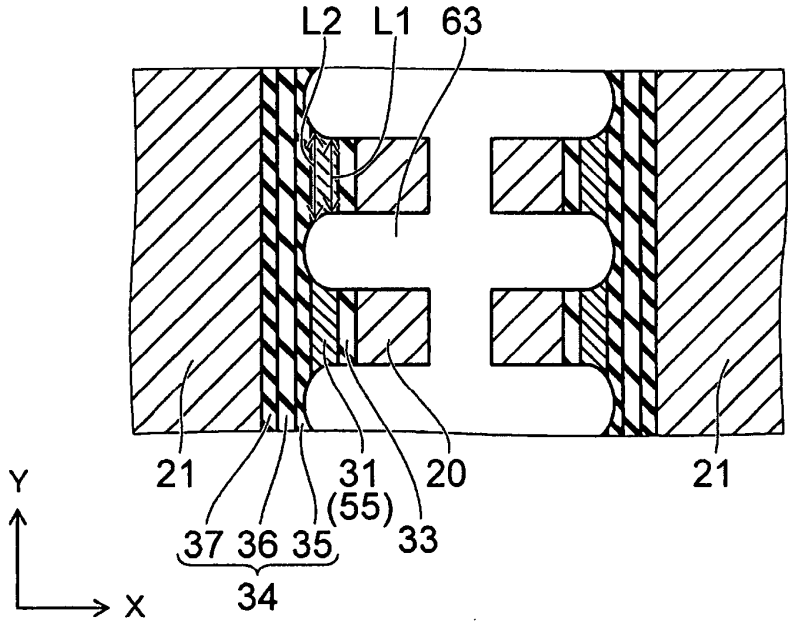


圖16

Micron Ex. 1002, p. 330
Micron v. YMTC
IPR2024-00789

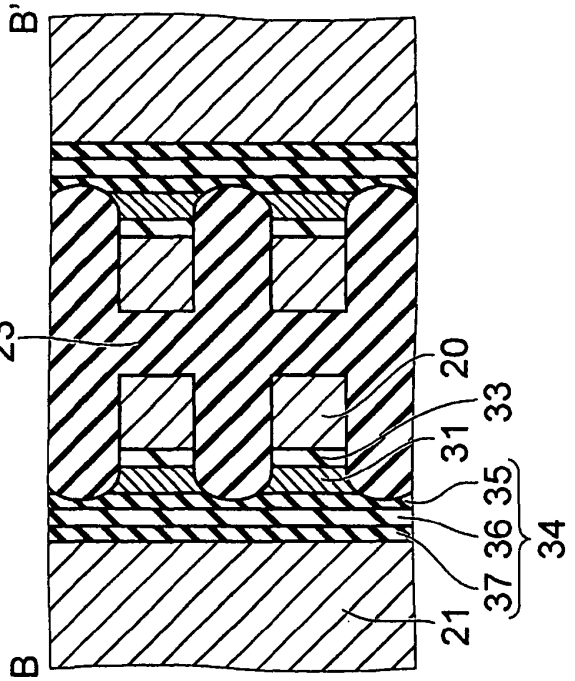


圖17B

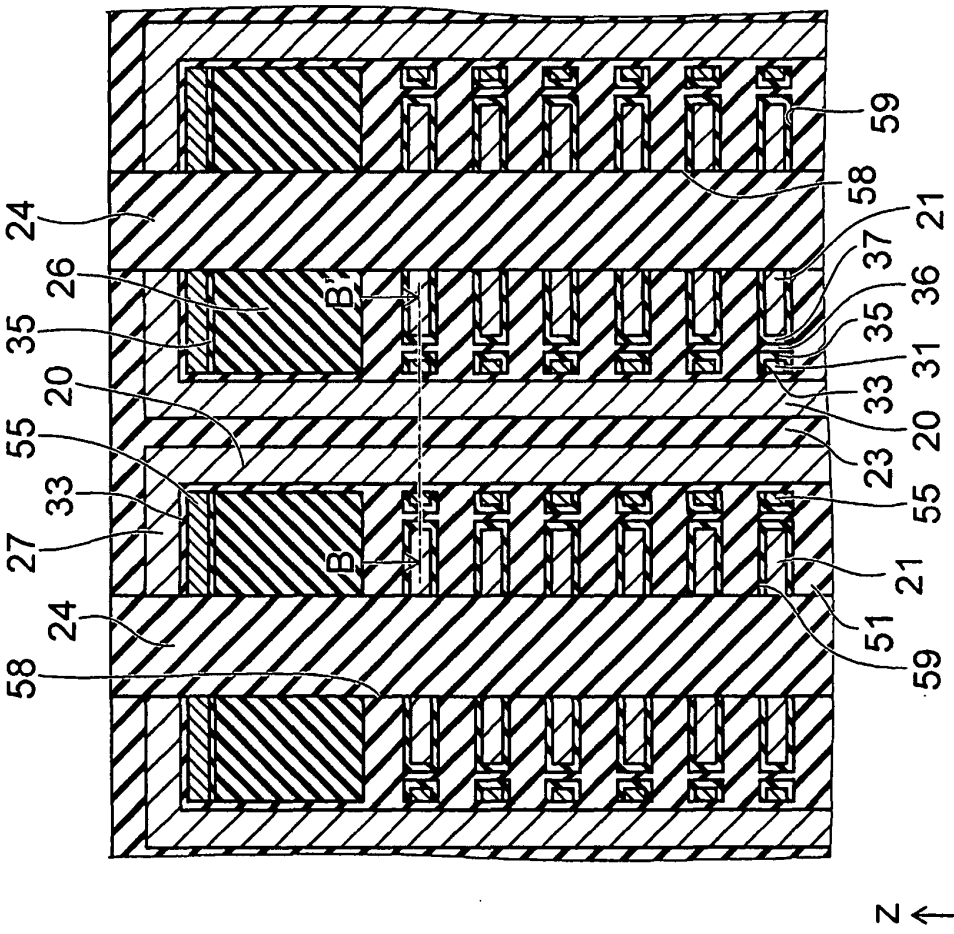


圖17A

Micron Ex. 1002, p. 331
Micron v. YMTC
IPR2024-00789

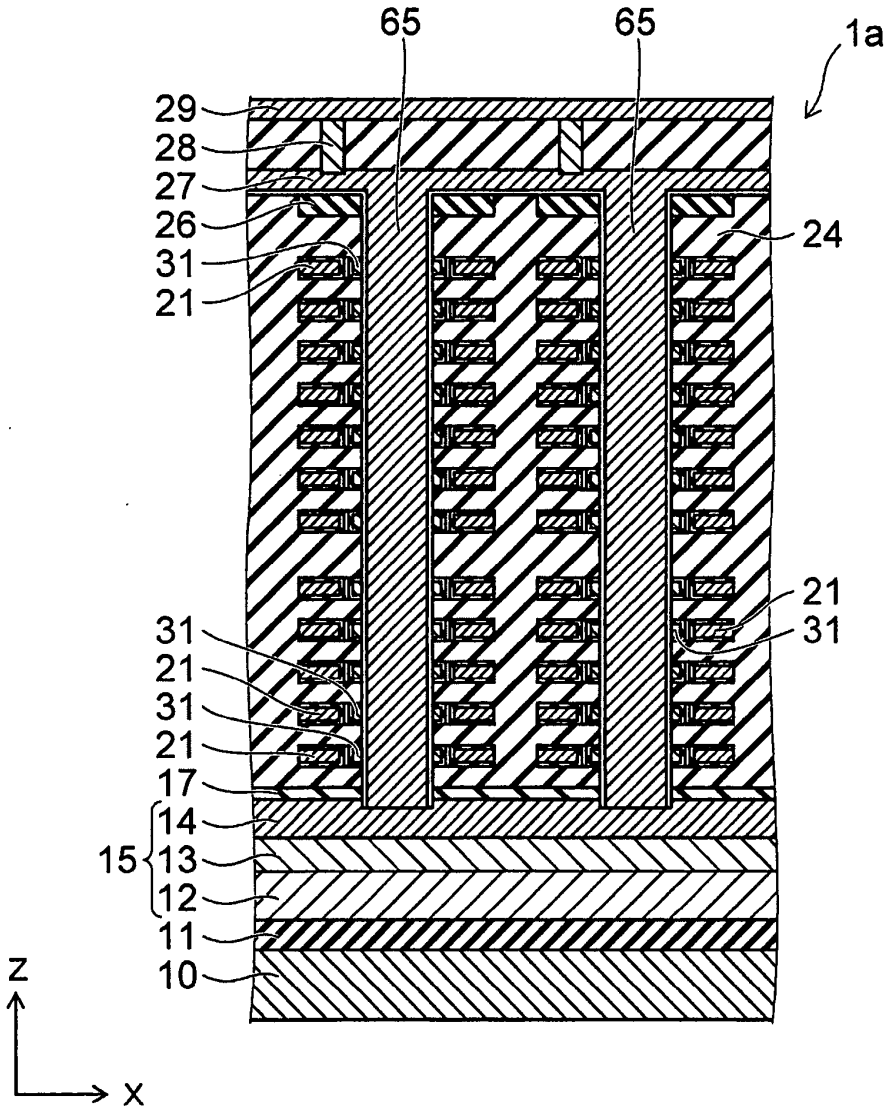


圖18

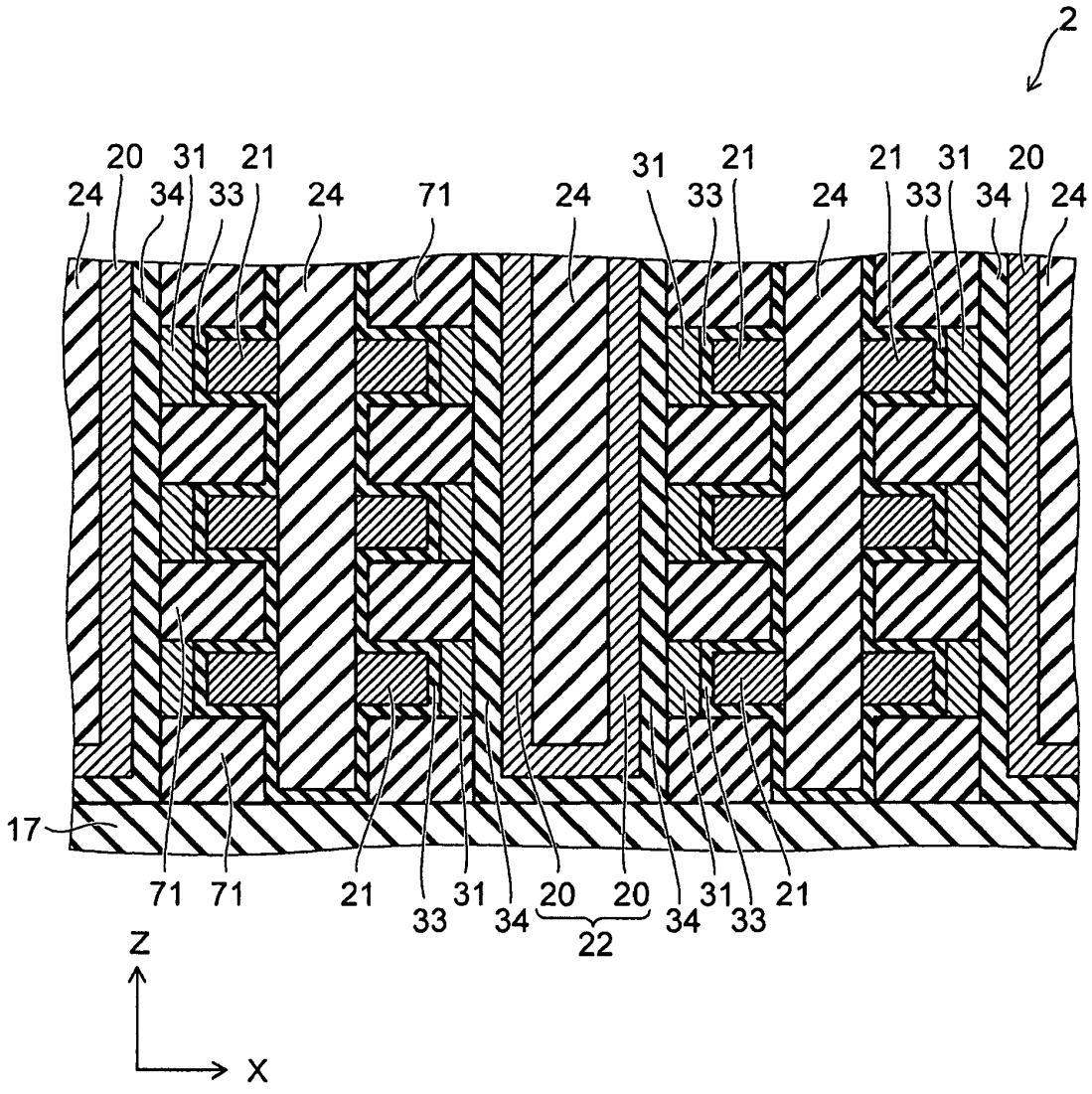

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圖19

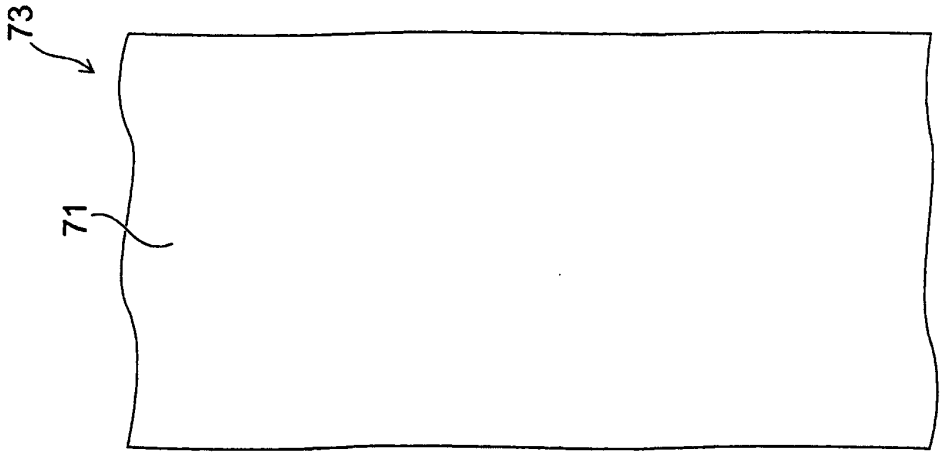


圖20B

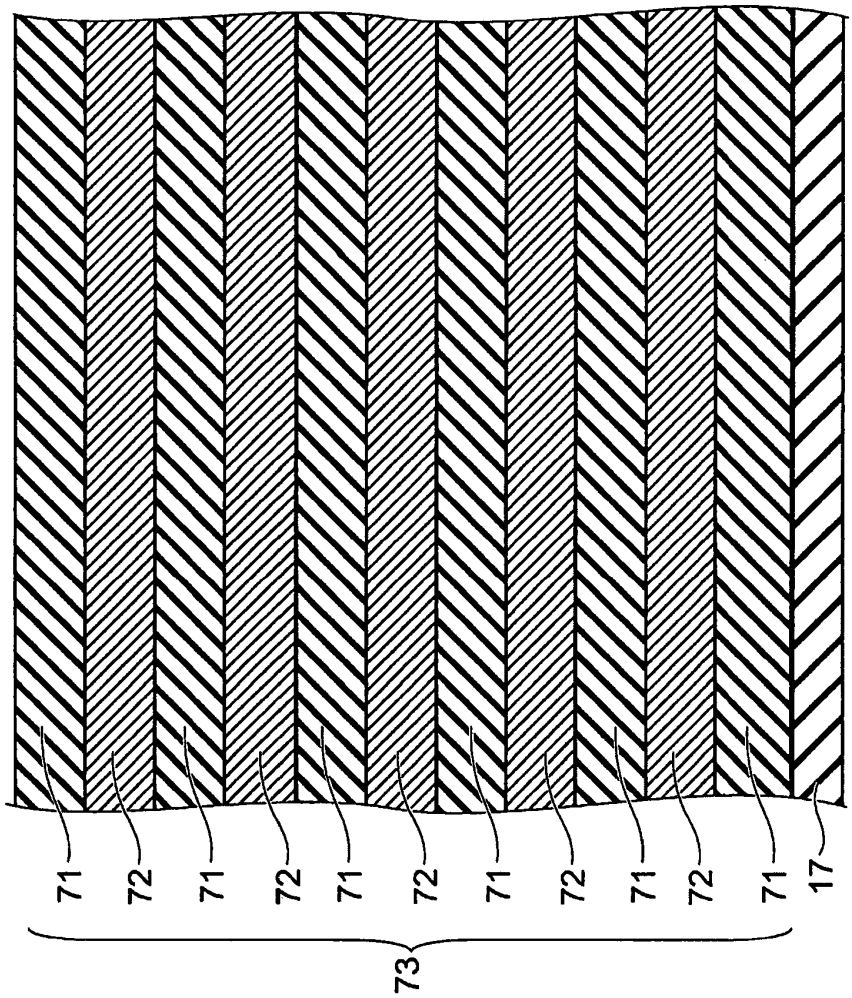


圖20A

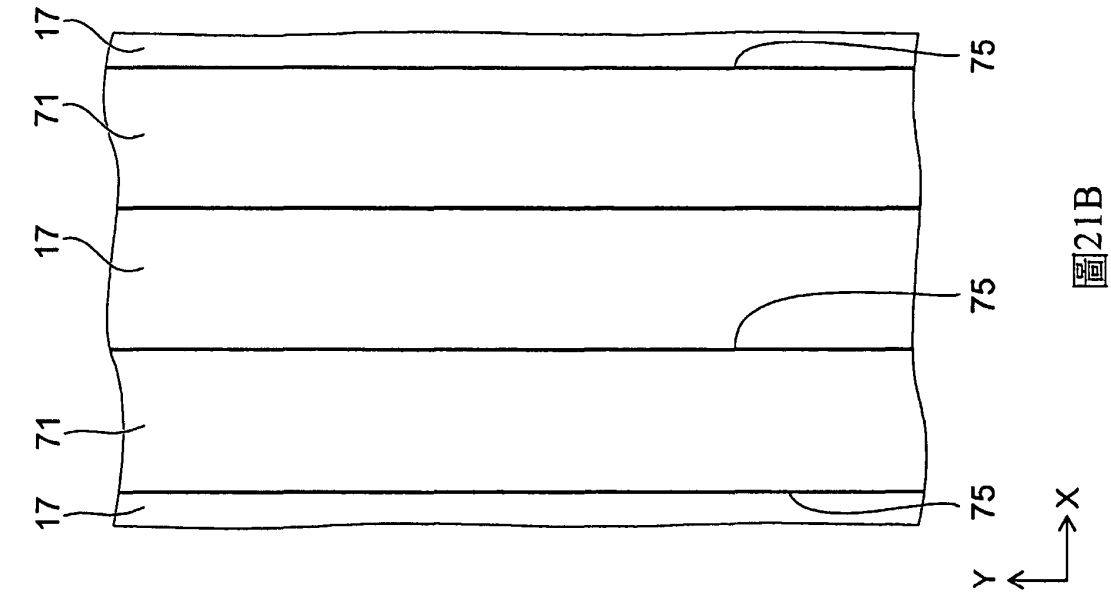


圖21B

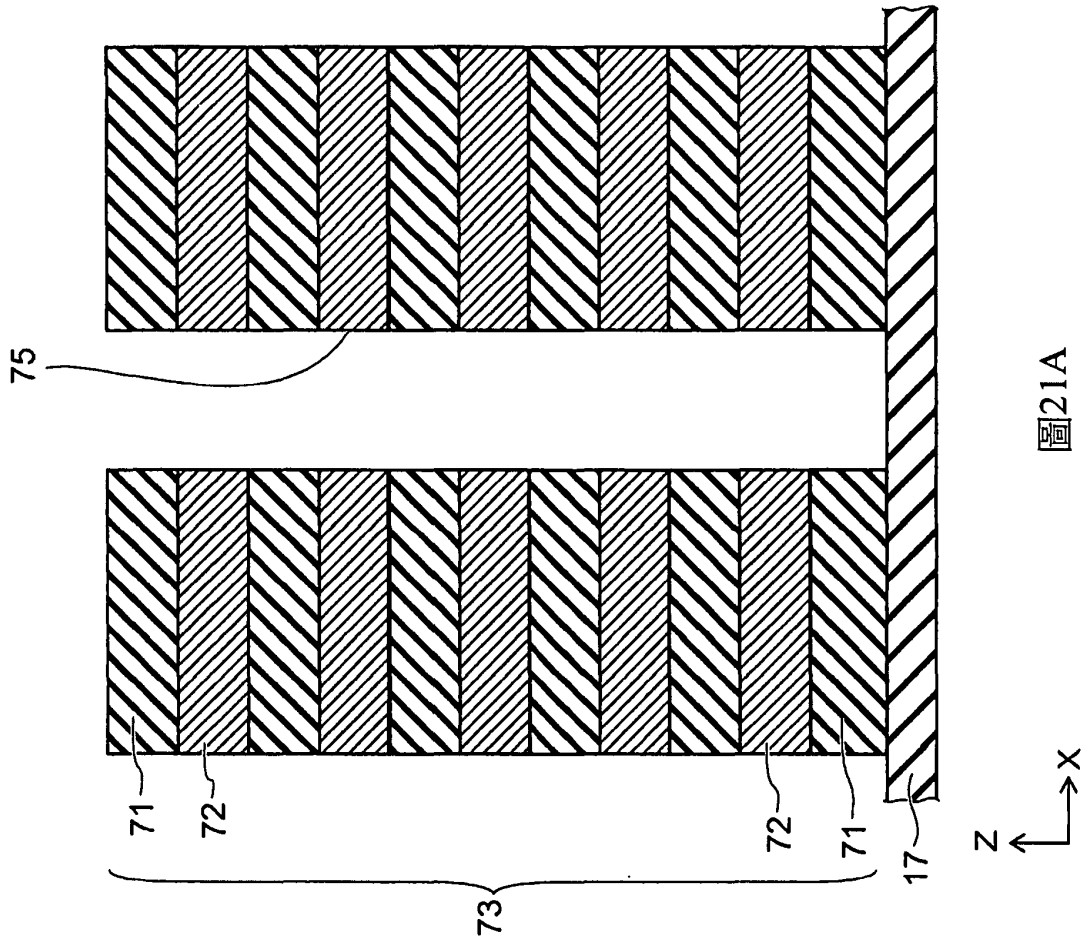


圖21A

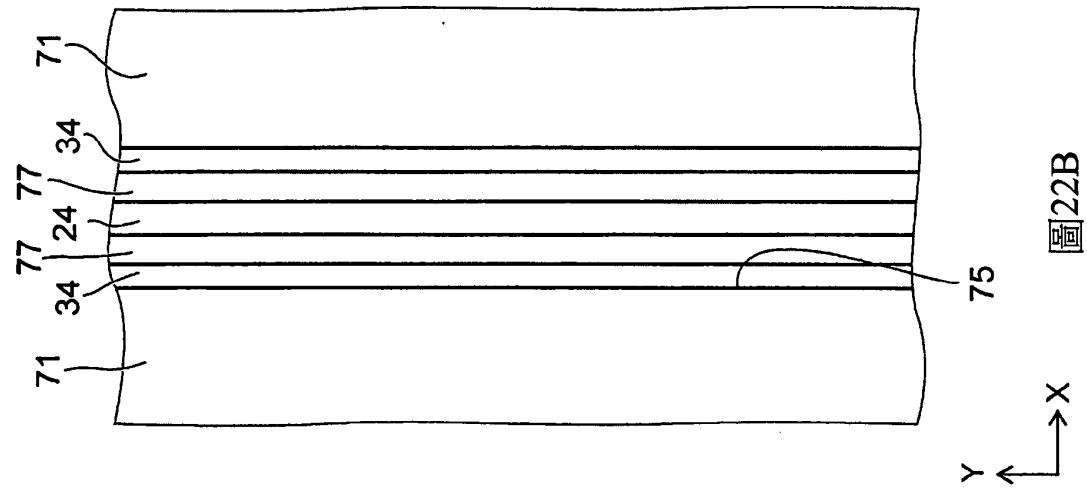


圖22B

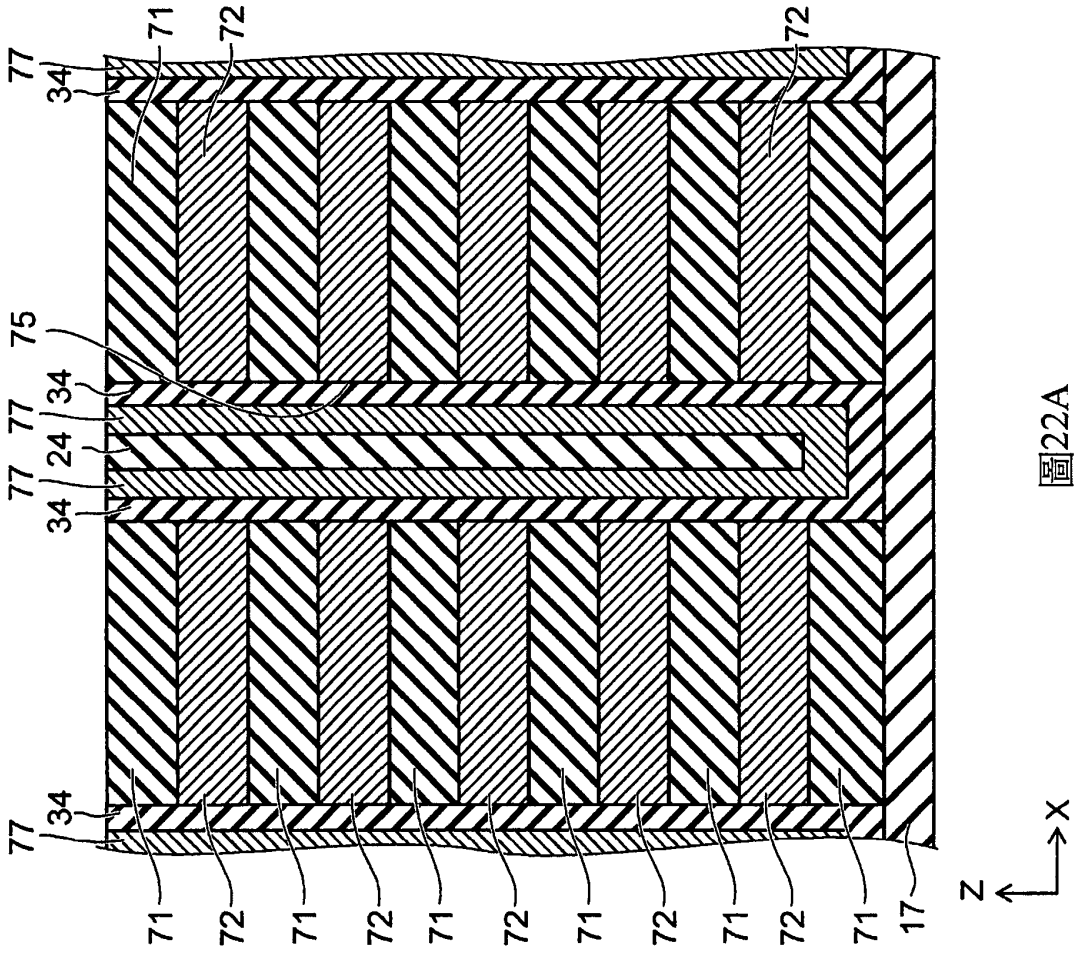


圖22A

Micron Ex. 1002, p. 336
Micron v. YMTC
IPR2024-00789

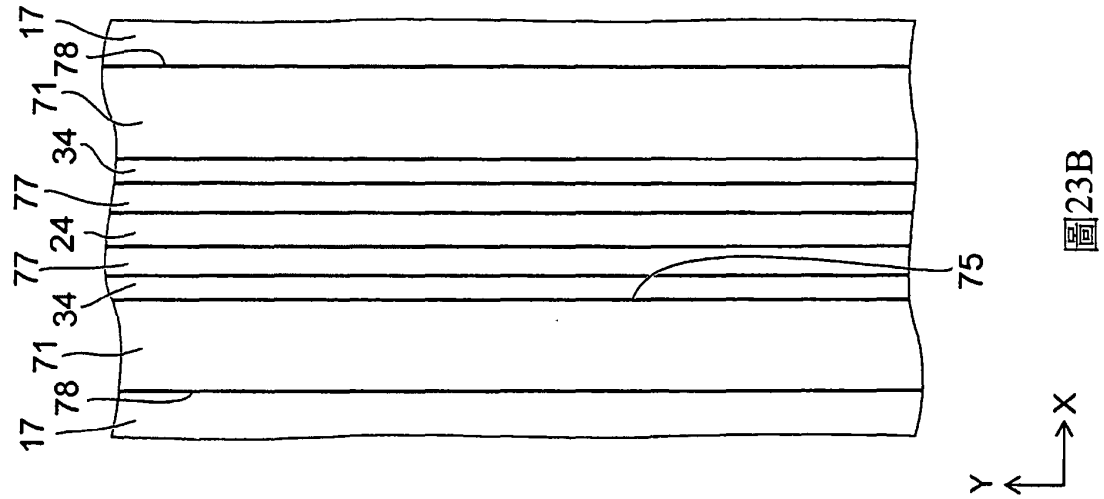

17
78
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77
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75
Y
X

圖23B

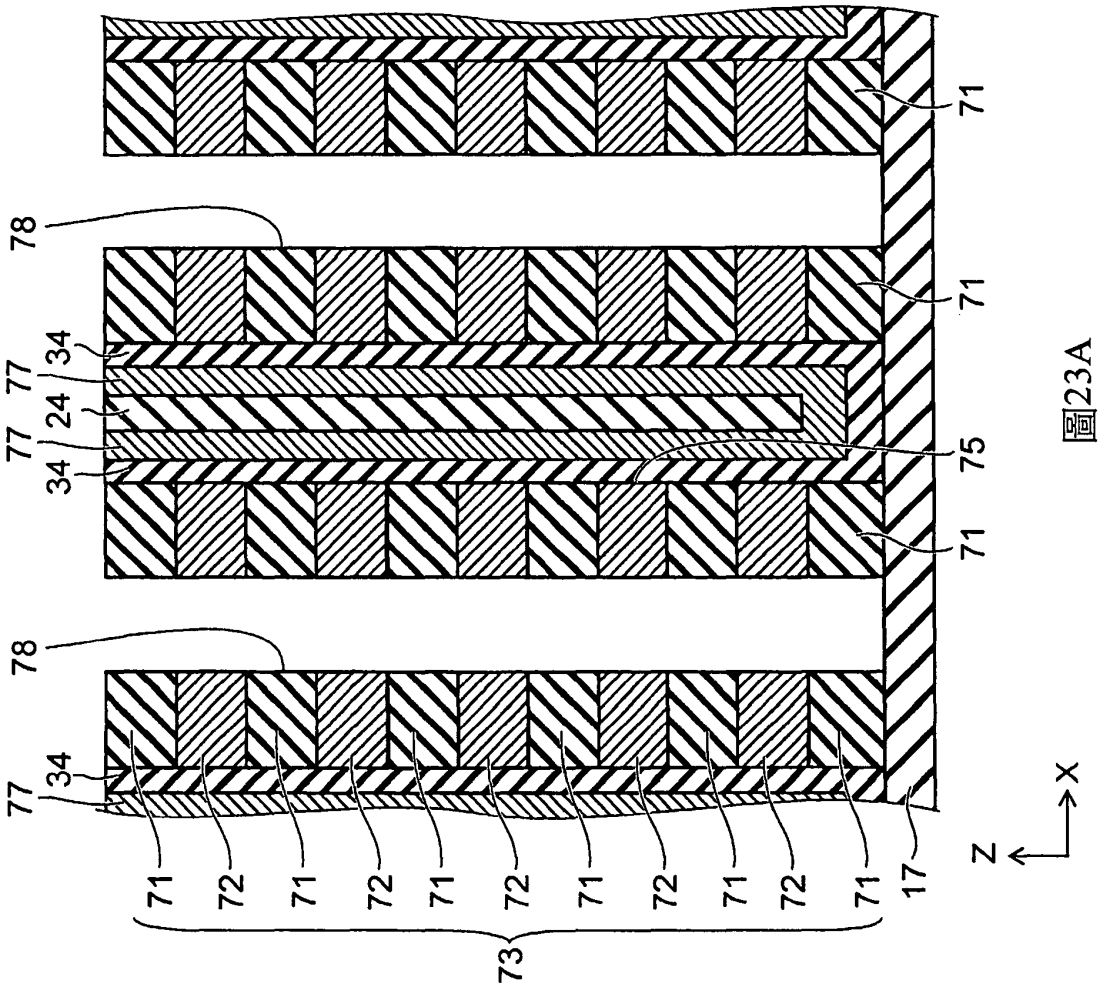

71
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73
Z
X

圖23A

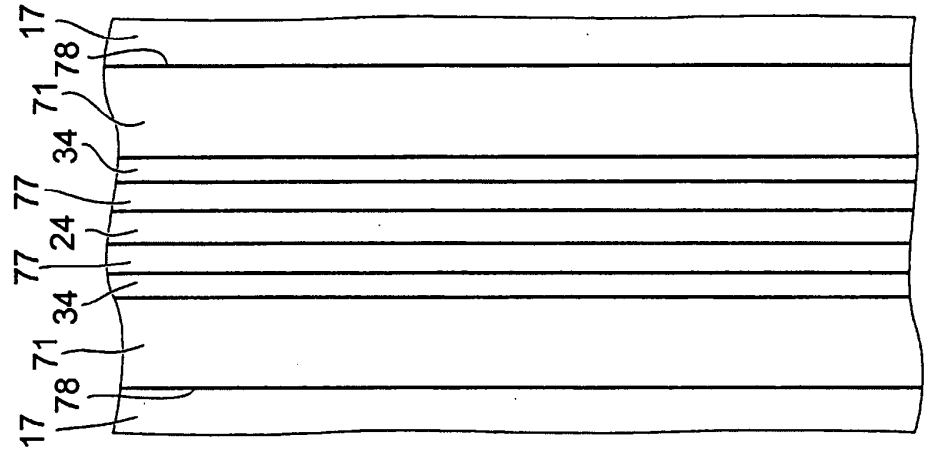


圖24B

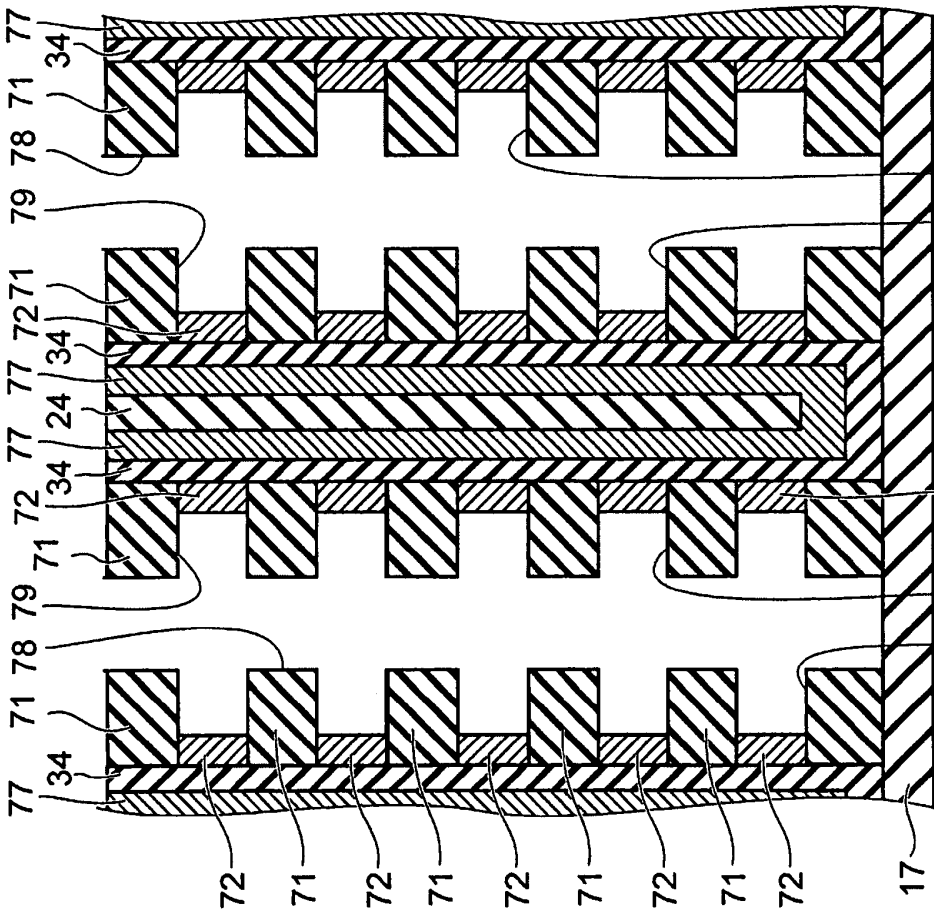


圖24A

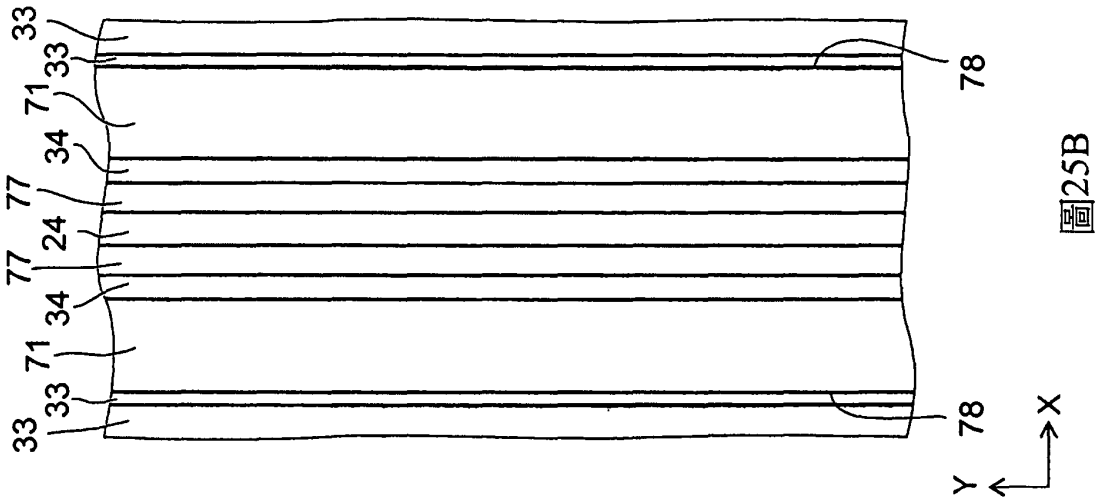

33
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77
24
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78
78
X
Y

圖25B

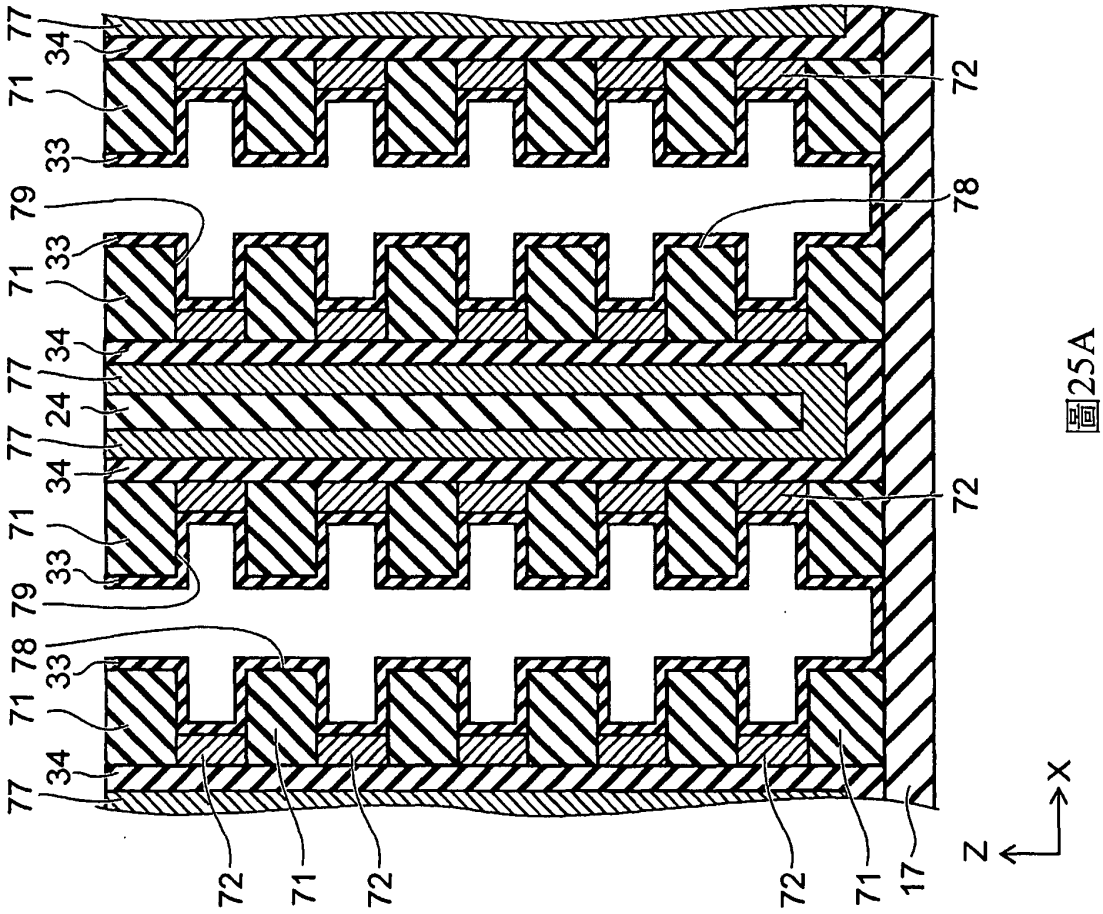

77
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72
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72
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71
17
X
Z

圖25A

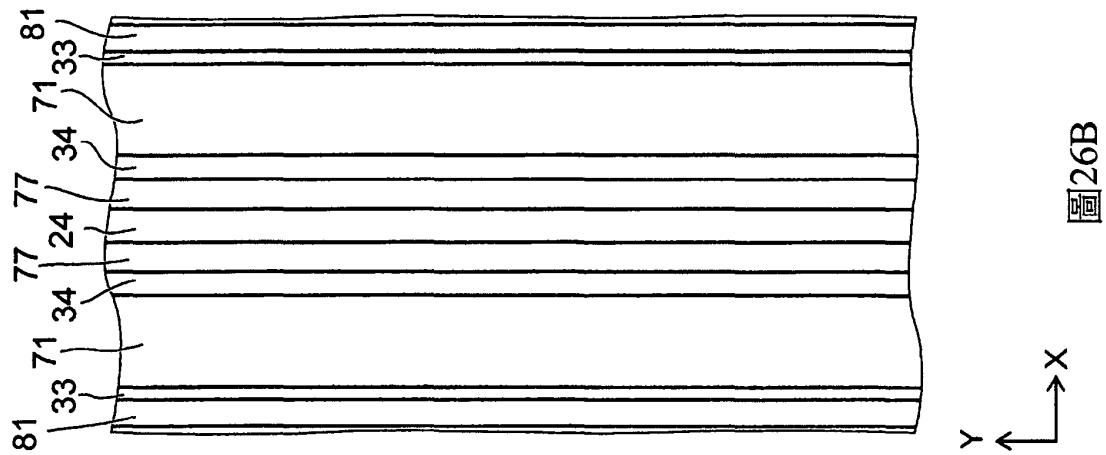

81
33
71
34
77
24
77
34
71
33
81
Y
X

圖26B

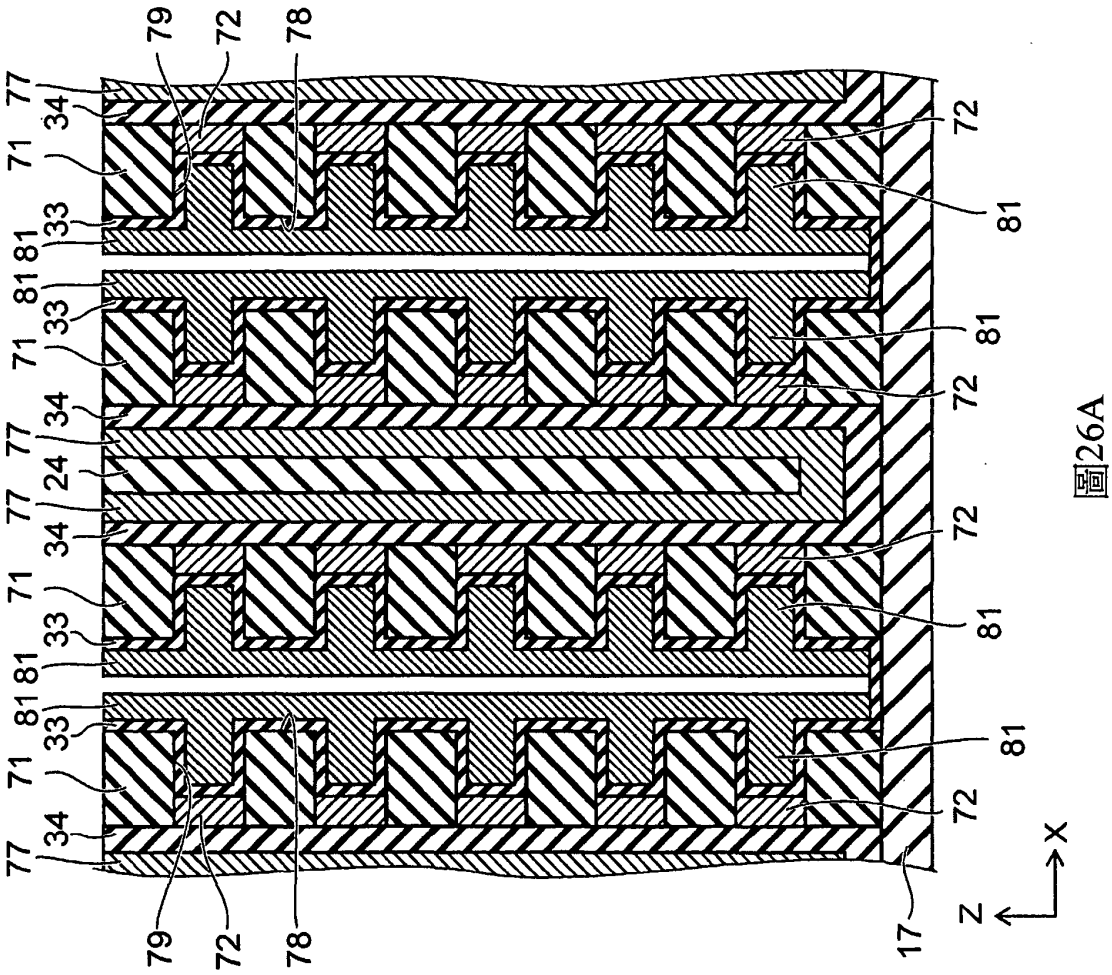

79
72
78
77
34
71
33
81
24
72
81
17
Z
X

圖26A

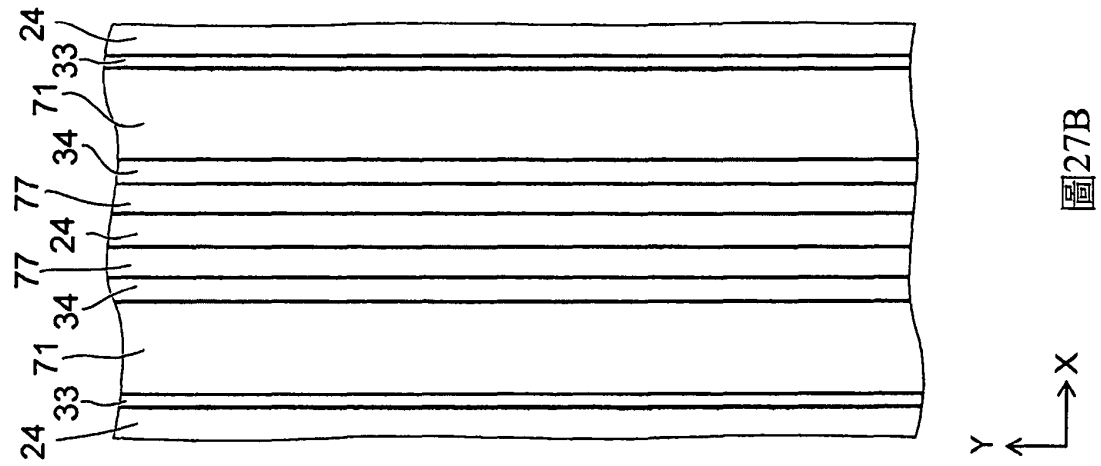

24
33
71
34
77
24
77
34
71
33
24
Y
X

圖27B

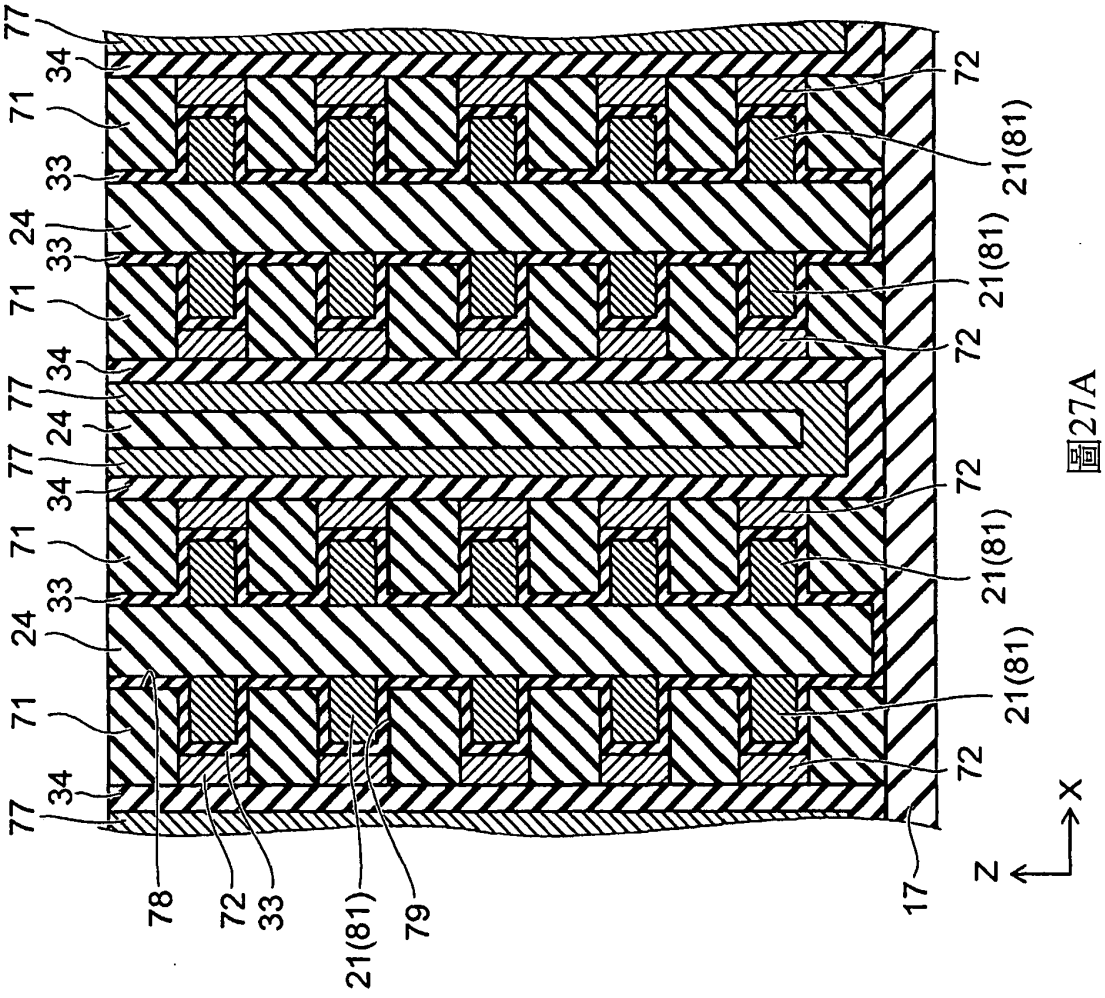

77
34
71
33
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77
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34
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33
24
71
34
77
72
21(81)
72
21(81)
72
21(81)
72
21(81)
78
72
33
21(81)
79
17
Z
X

圖27A

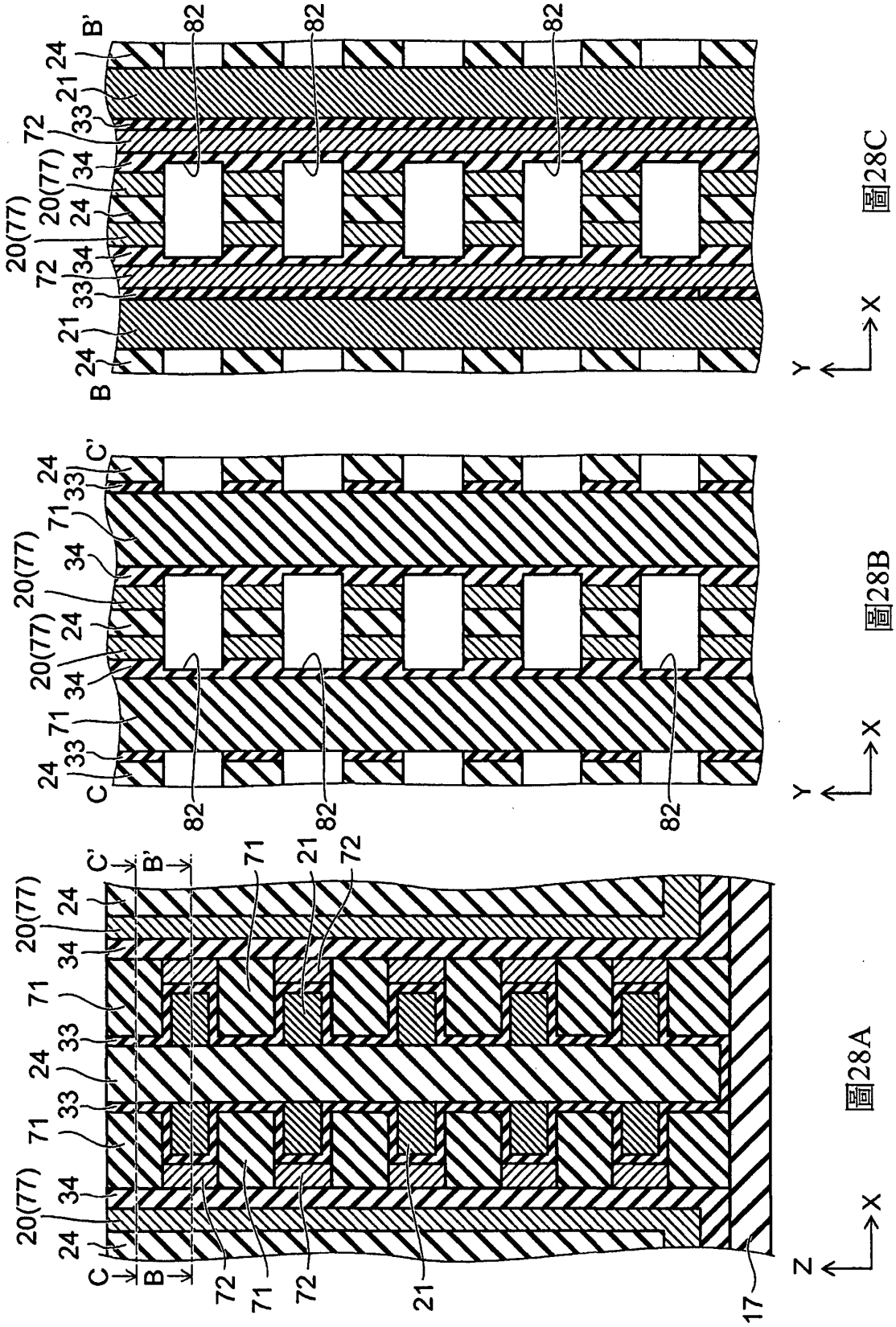


圖28C 圖28B 圖28A

Micron Ex. 1002, p. 342
Micron v. YMTC
IPR2024-00789

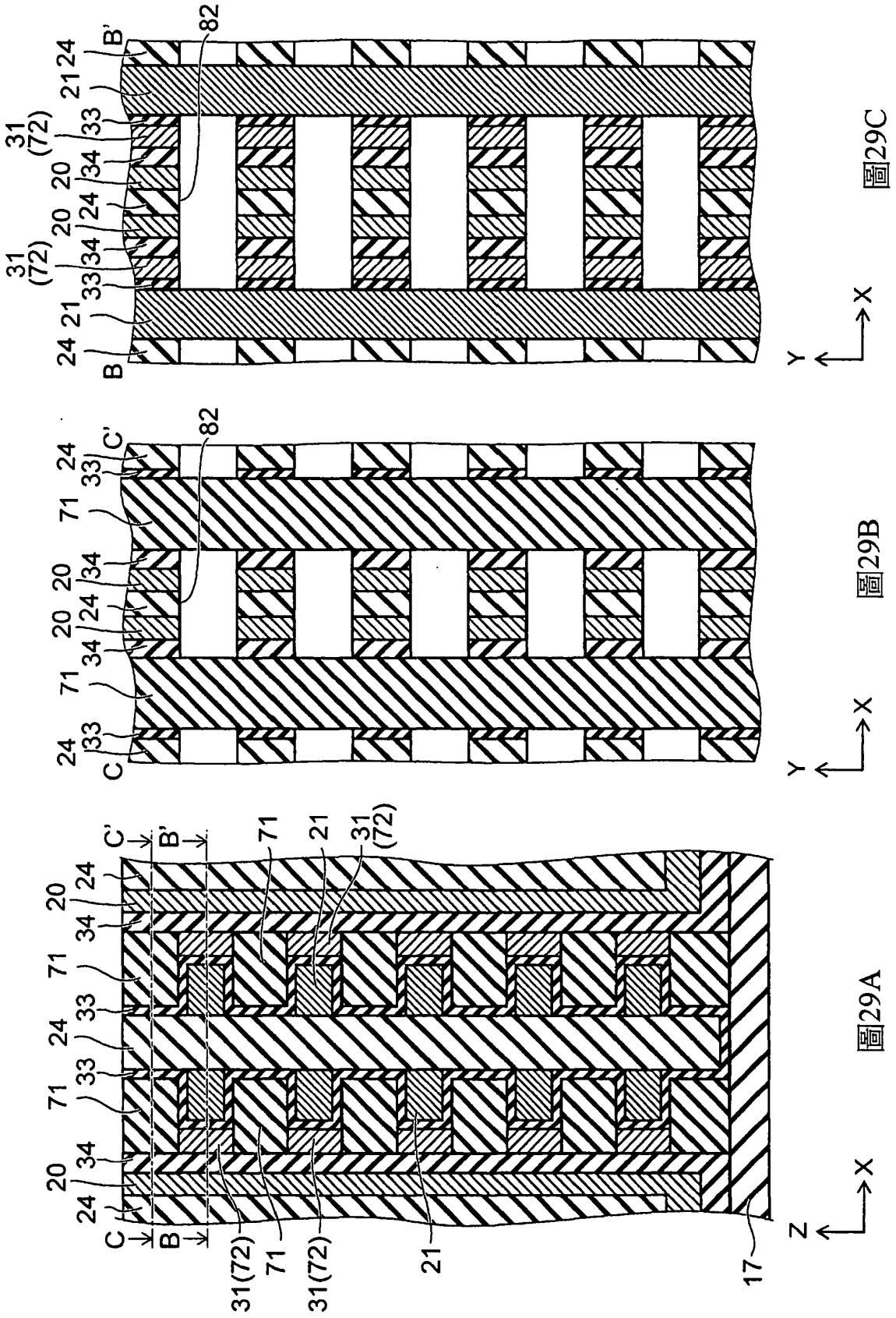


圖29C

圖29B

圖29A

Micron Ex. 1002, p. 343
Micron v. YMTC
IPR2024-00789

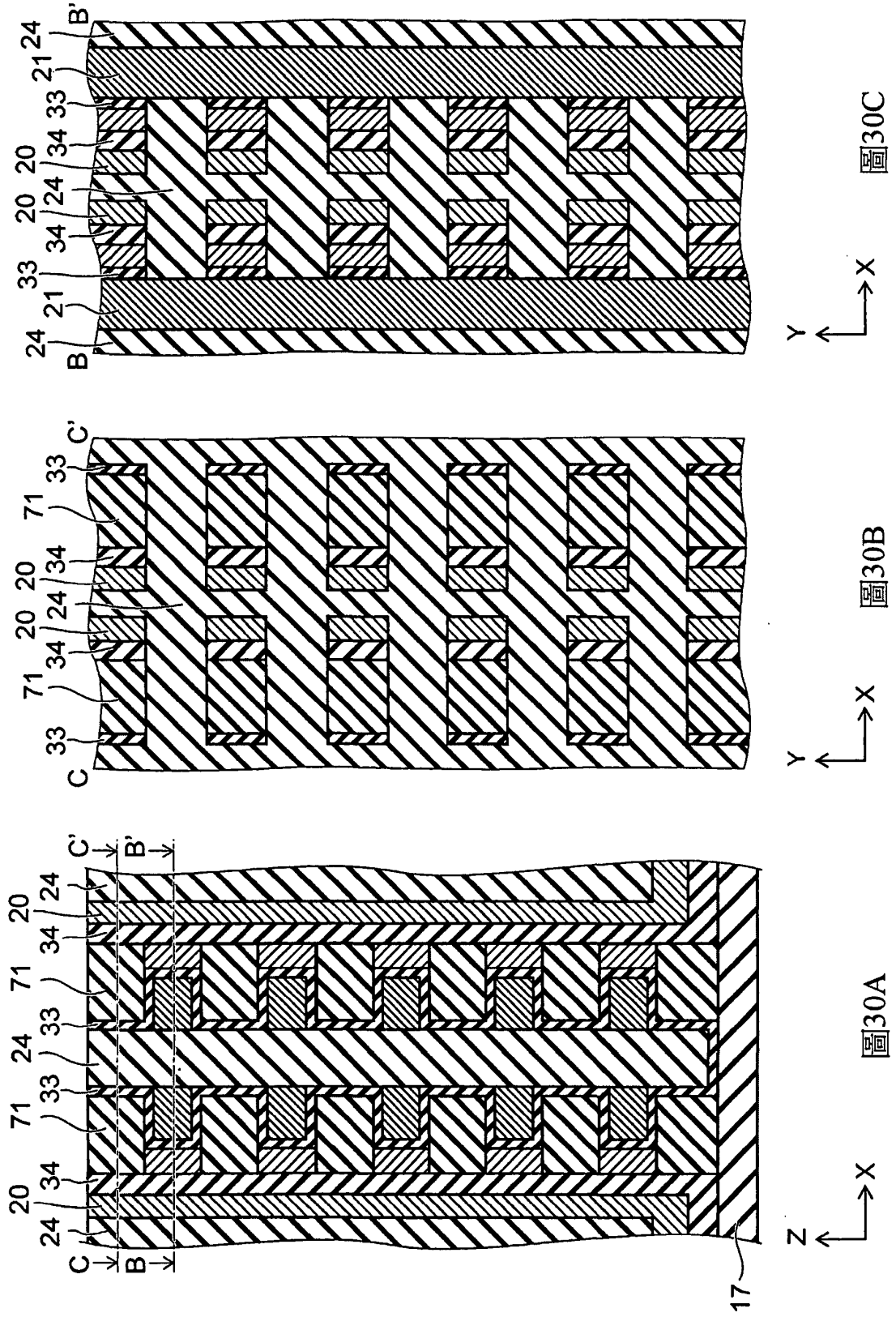


圖30C

圖30B

圖30A

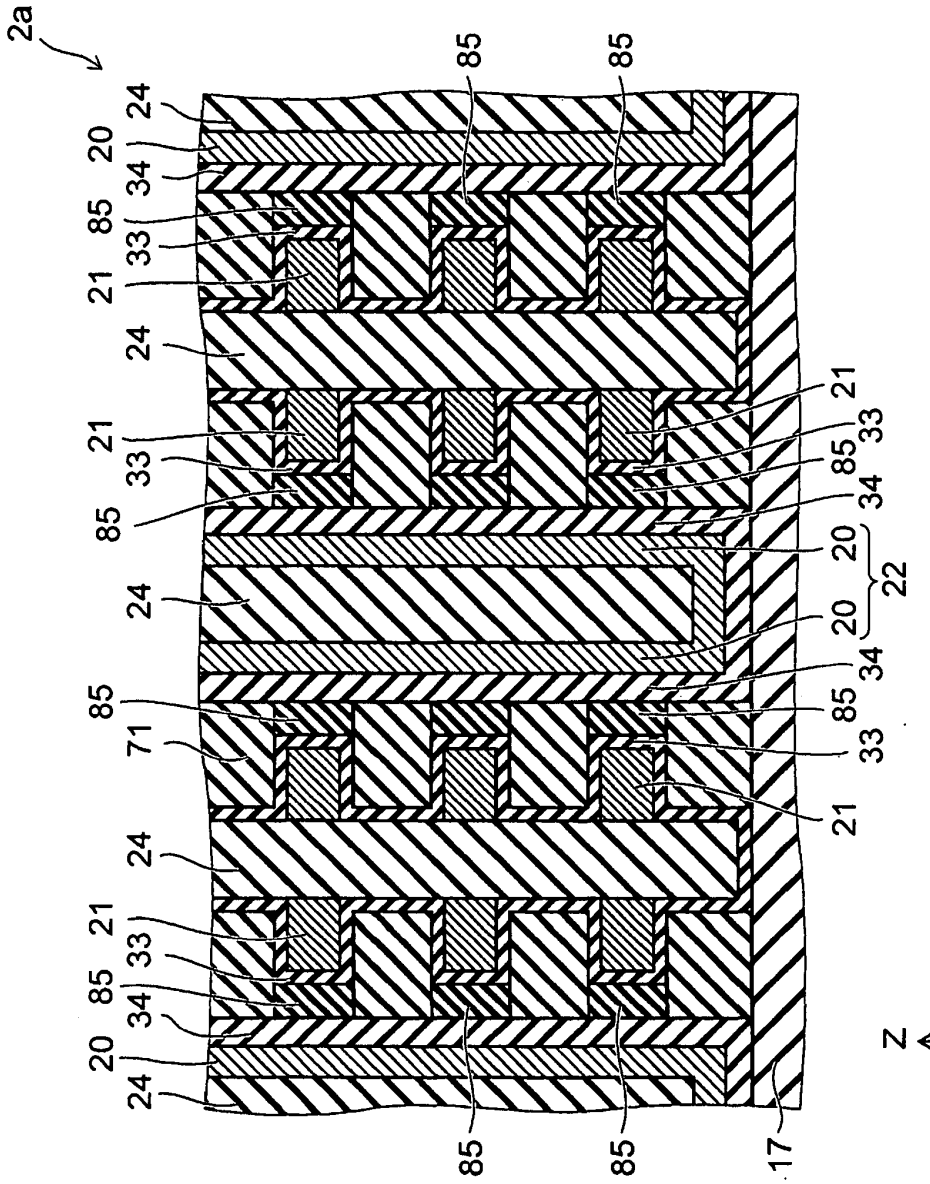

2a
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24
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85
17
X
Z

圖31

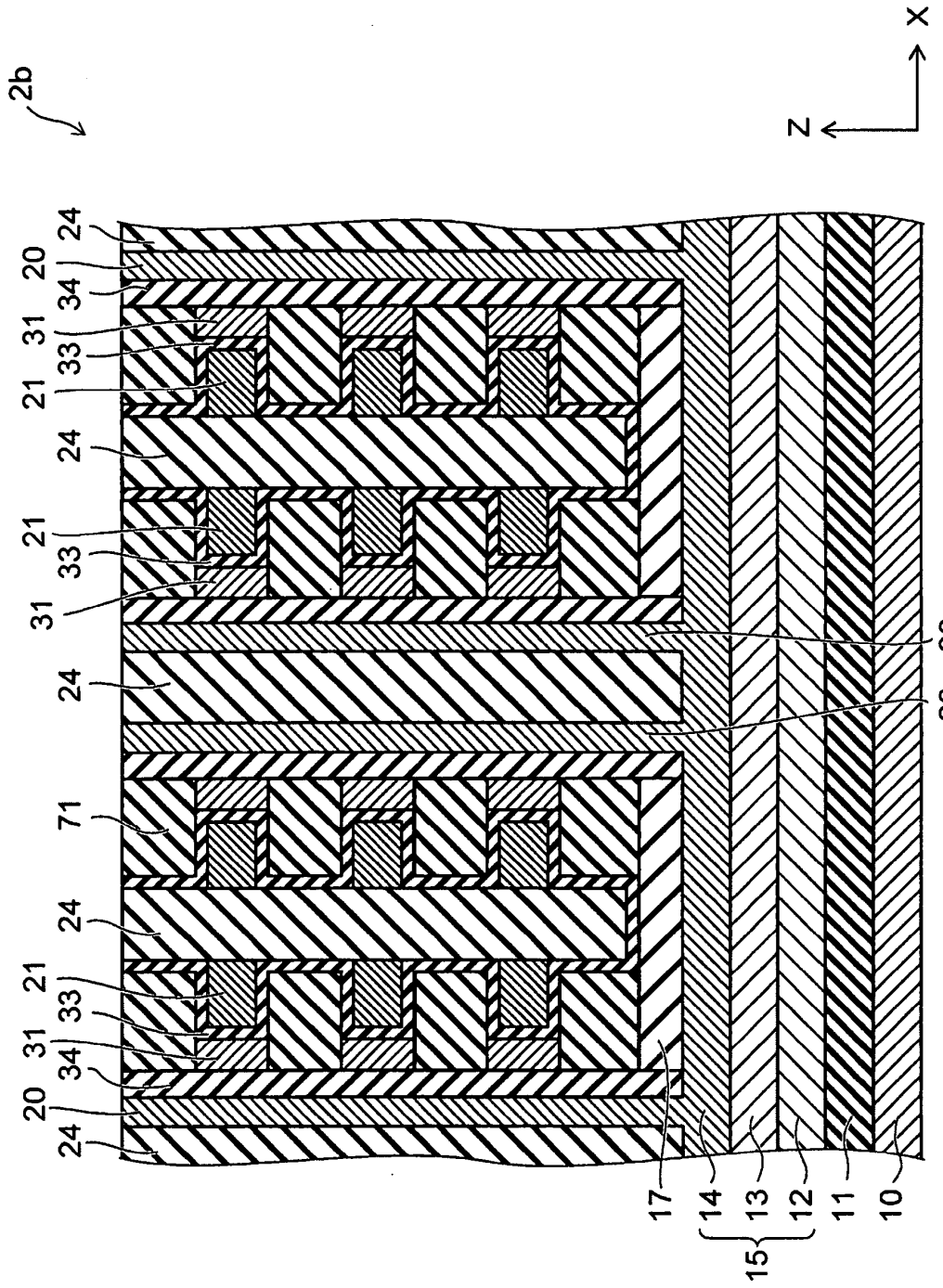

2b
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圖32

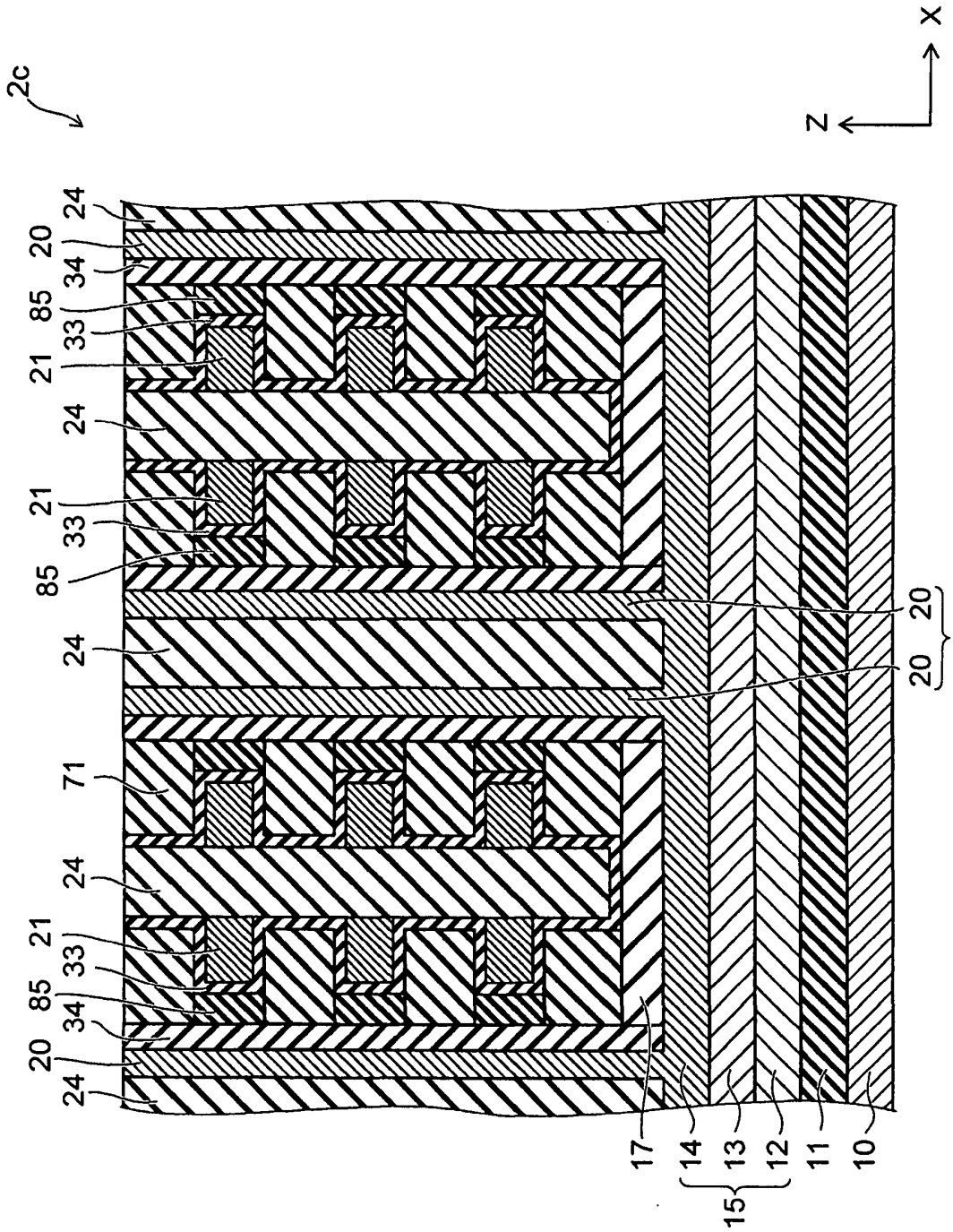

2c
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71
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圖33

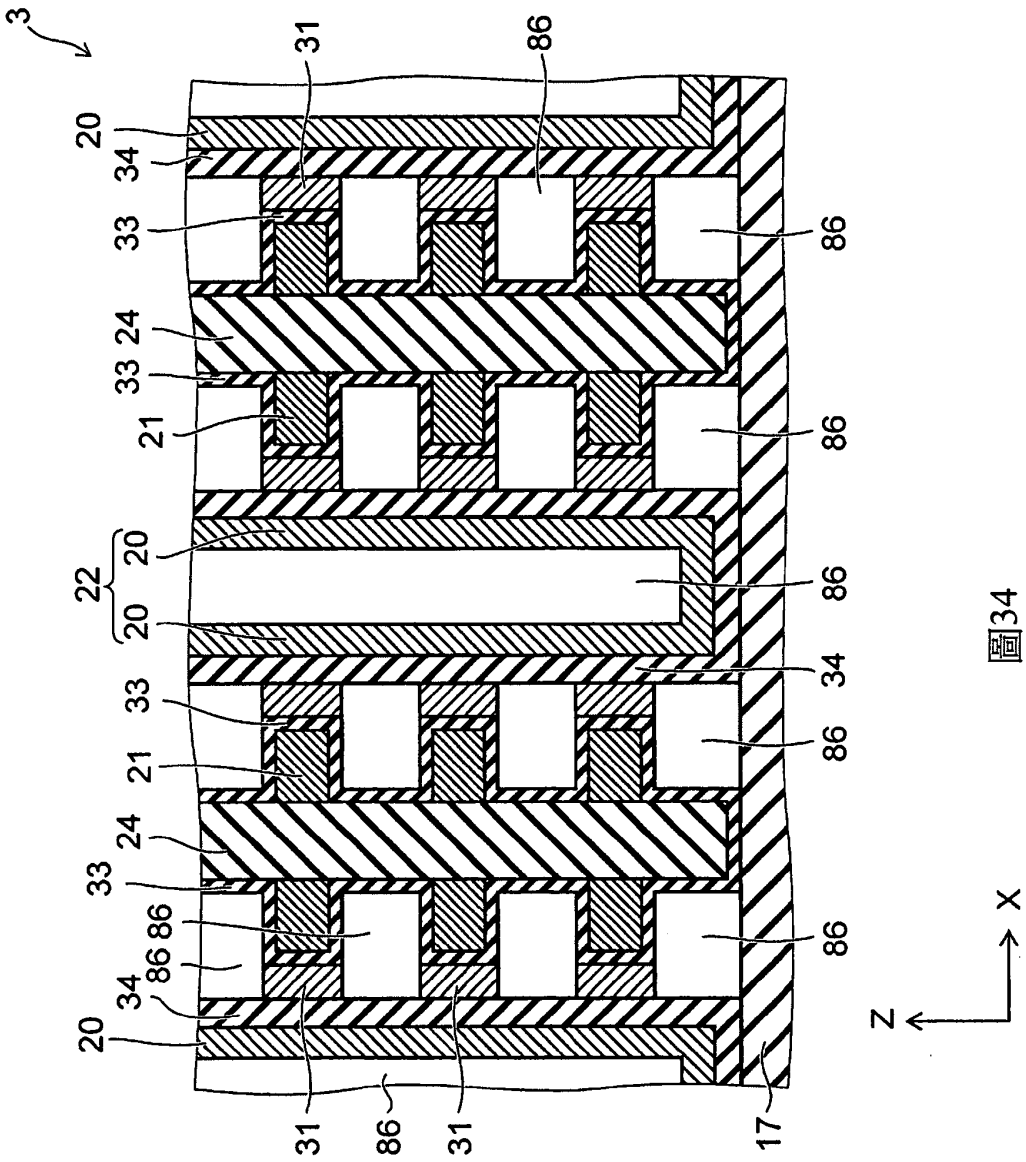

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17
X
Z

圖34

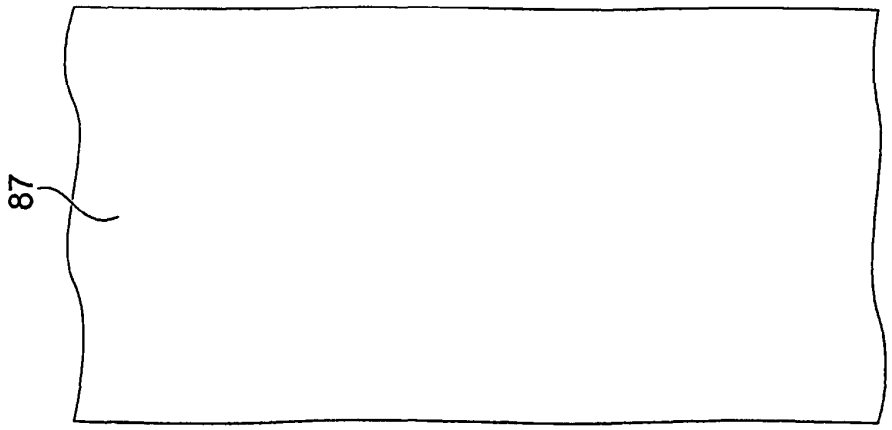


圖35B

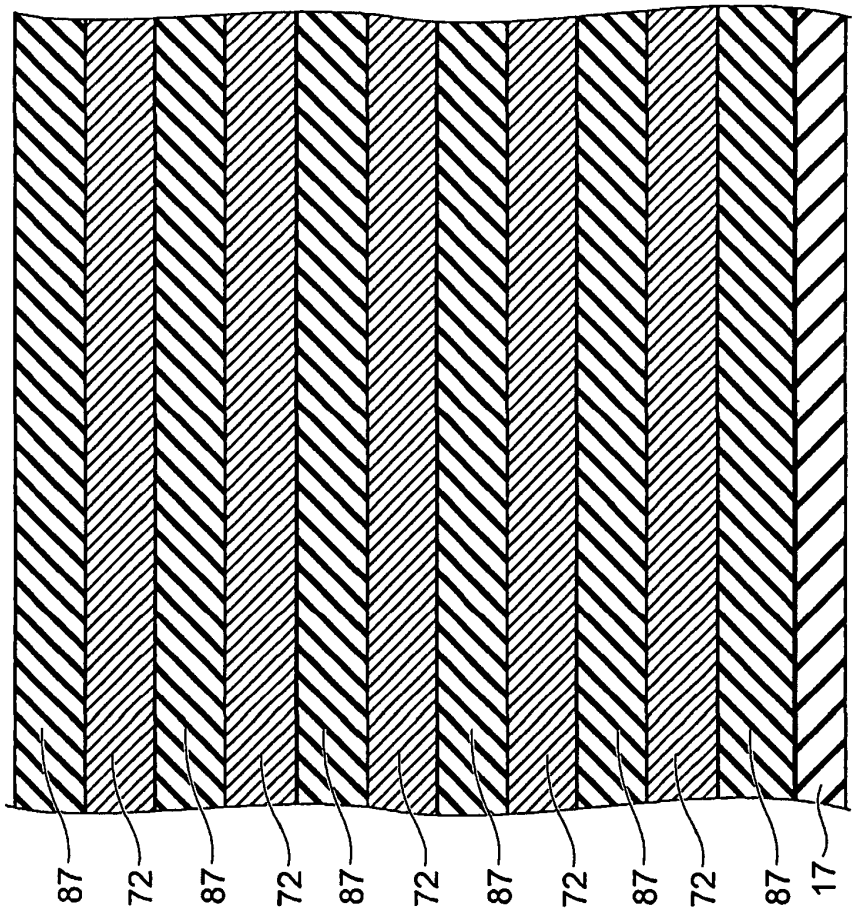


圖35A

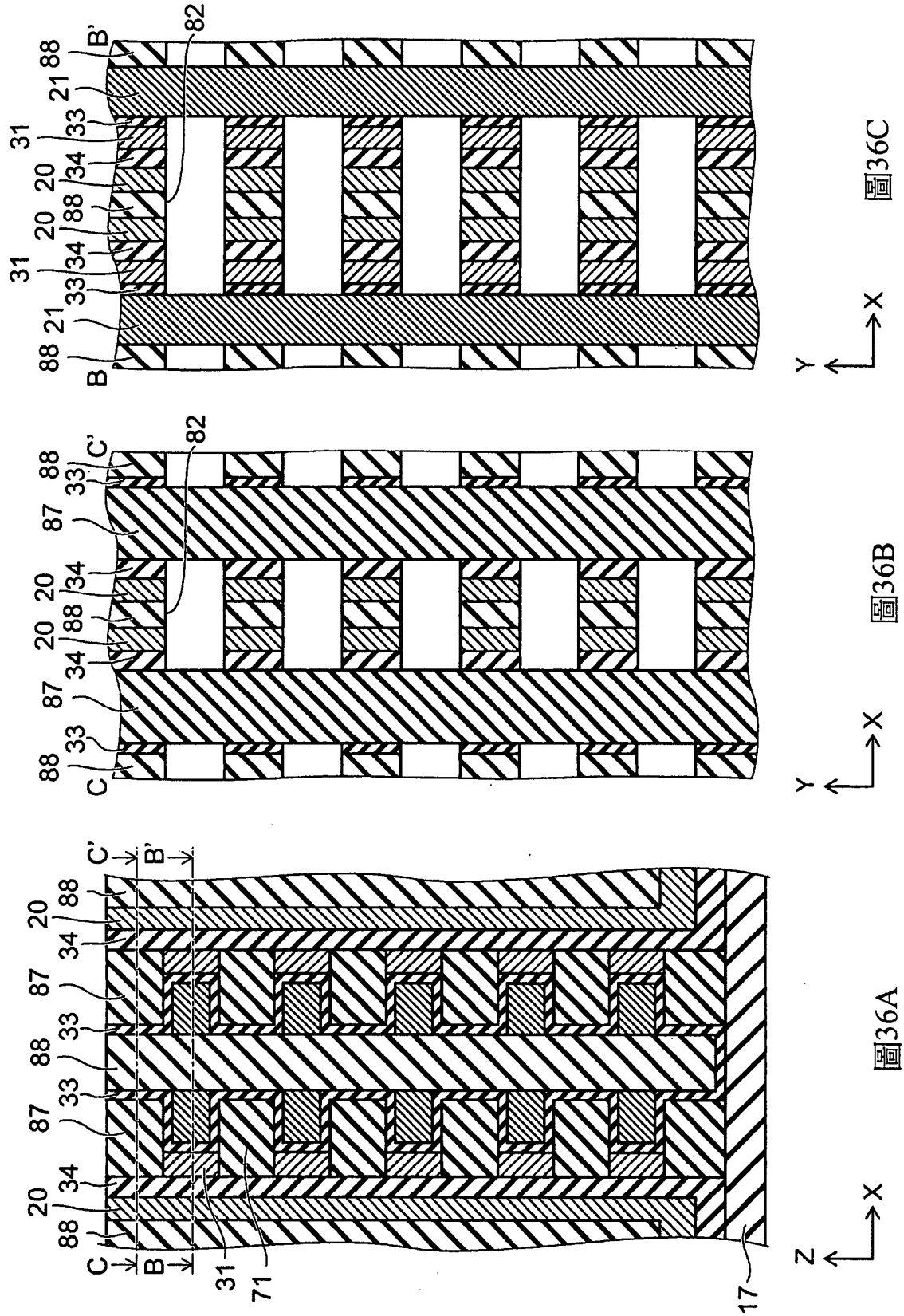


圖36C

圖36B

圖36A

Micron Ex. 1002, p. 350
Micron v. YMTC
IPR2024-00789

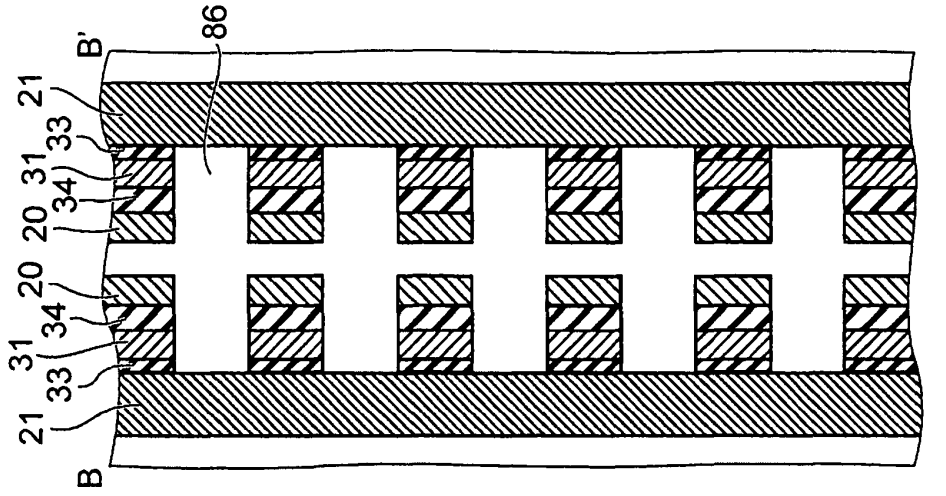


圖37C

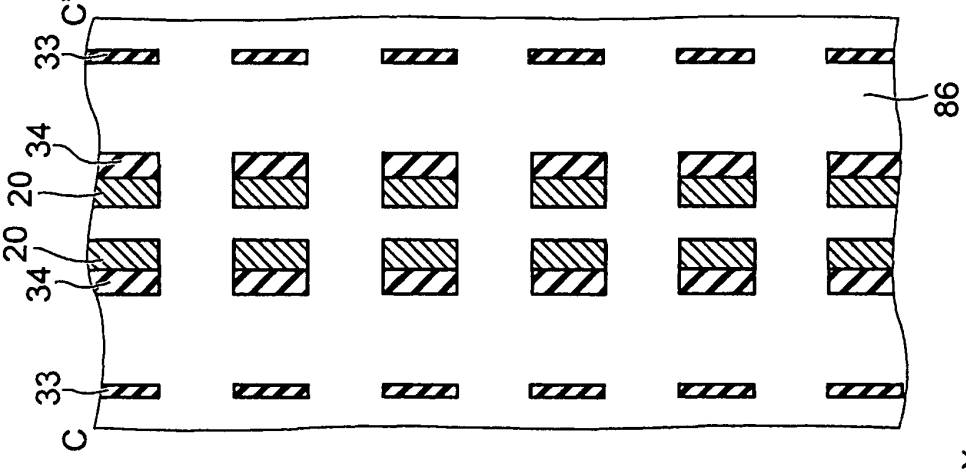


圖37B

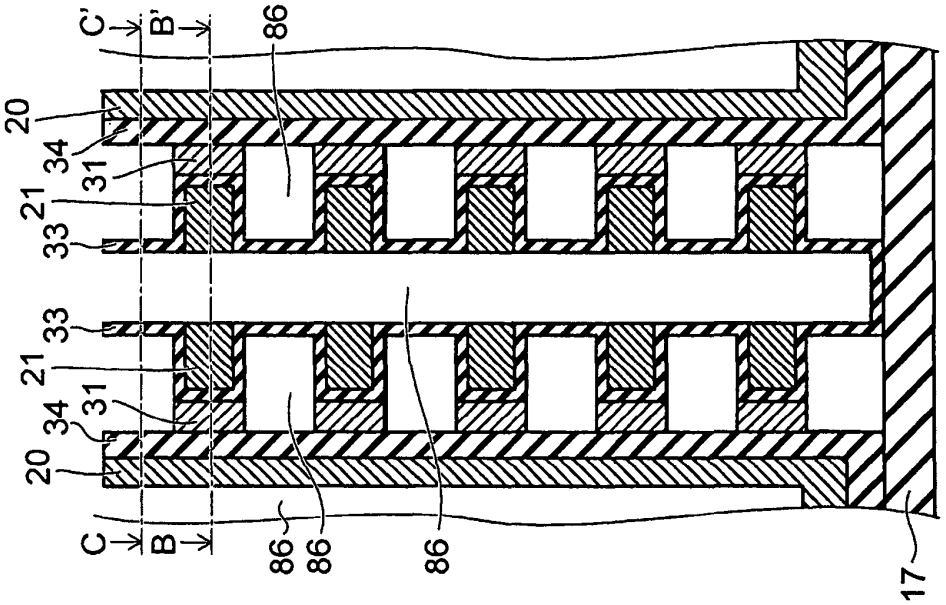


圖37A

Micron Ex. 1002, p. 351
Micron v. YMTC
IPR2024-00789

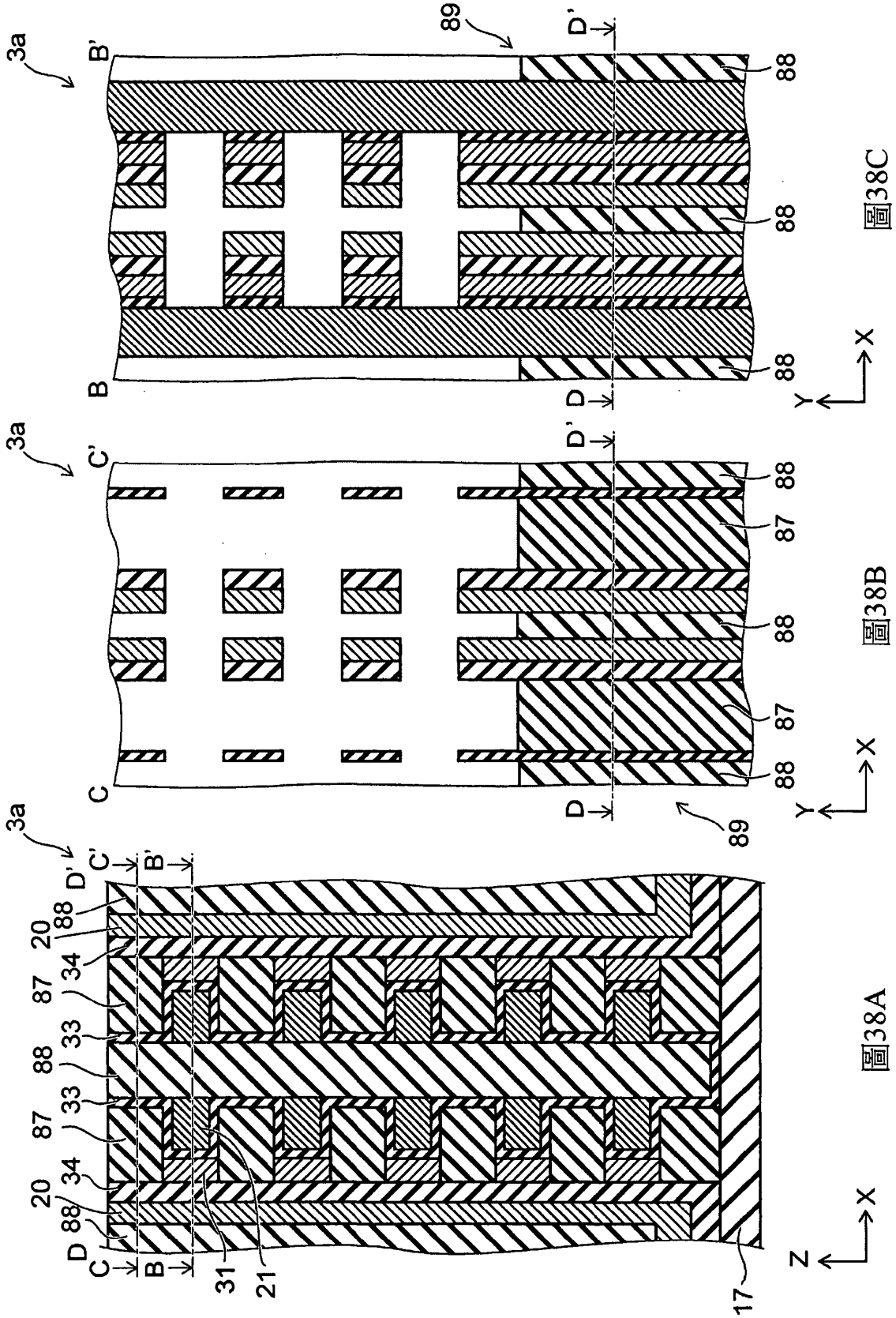


圖38C

圖38B

圖38A

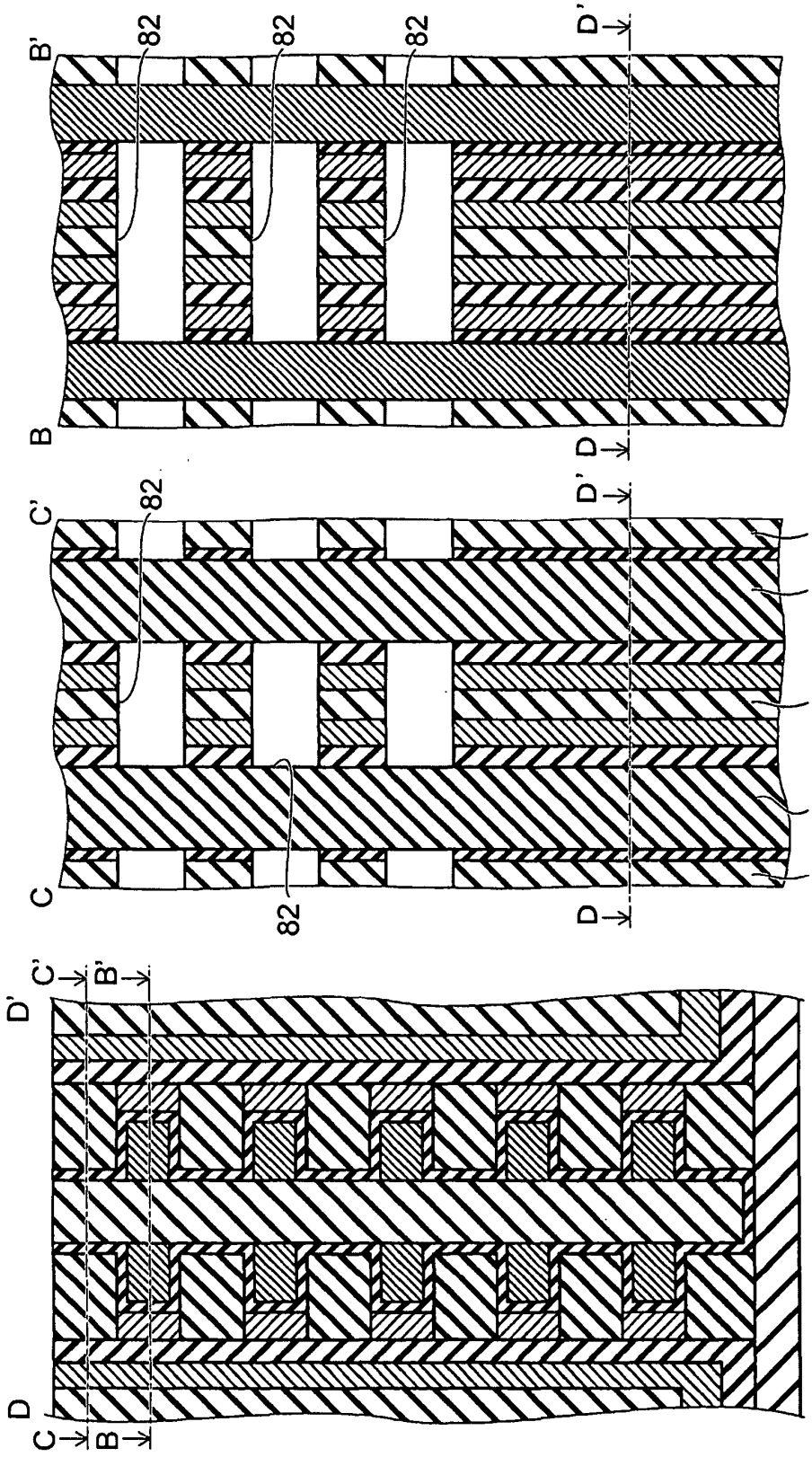


圖39C

圖39B

圖39A

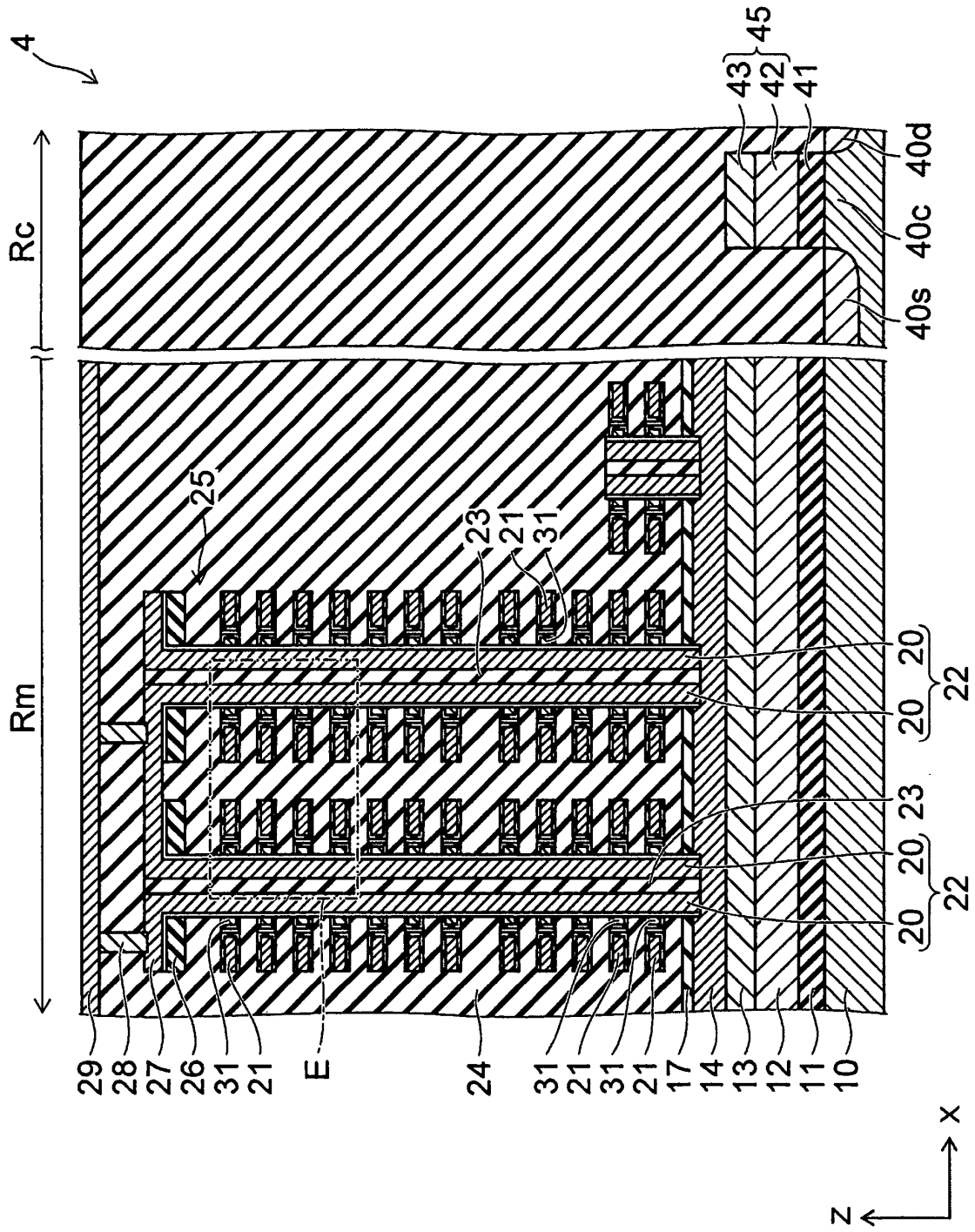

4
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40d
40c
40s
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Rm
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圖40

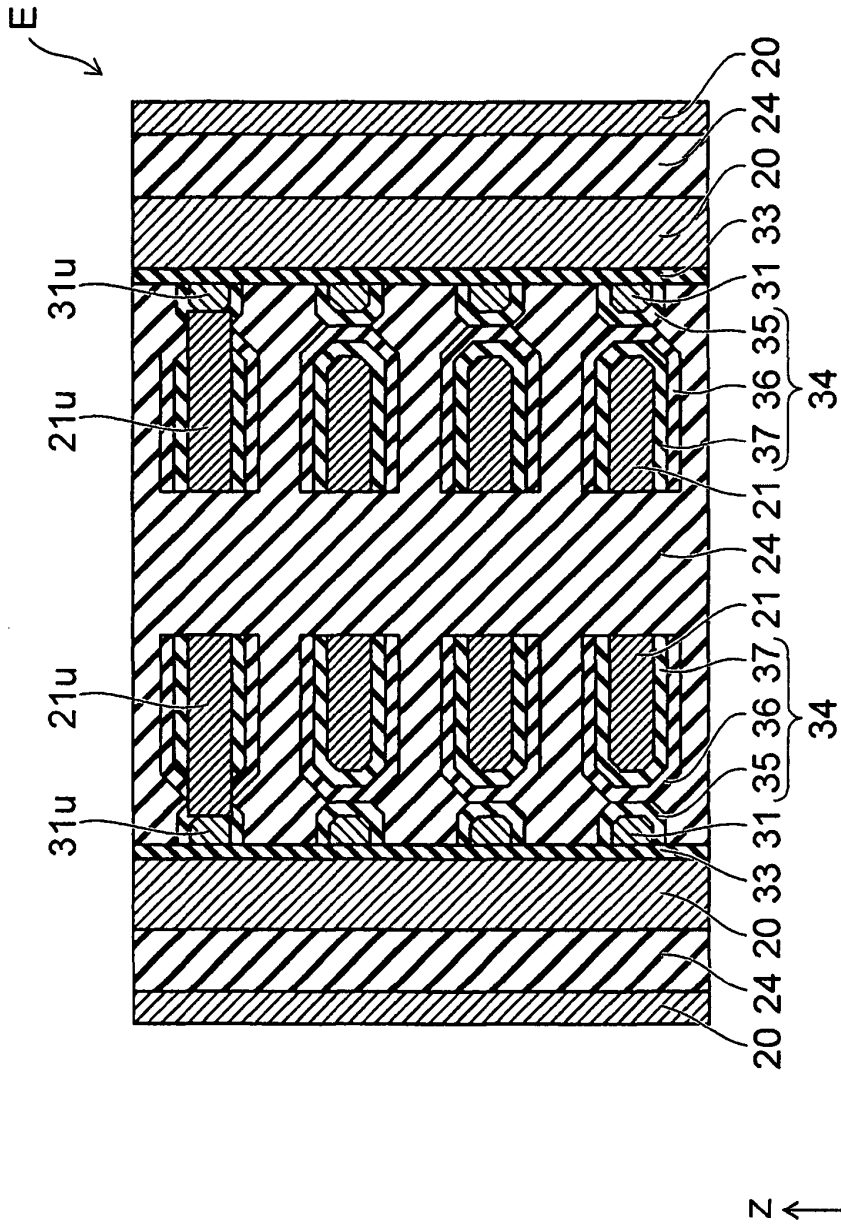

E
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31u
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X
Z

圖41

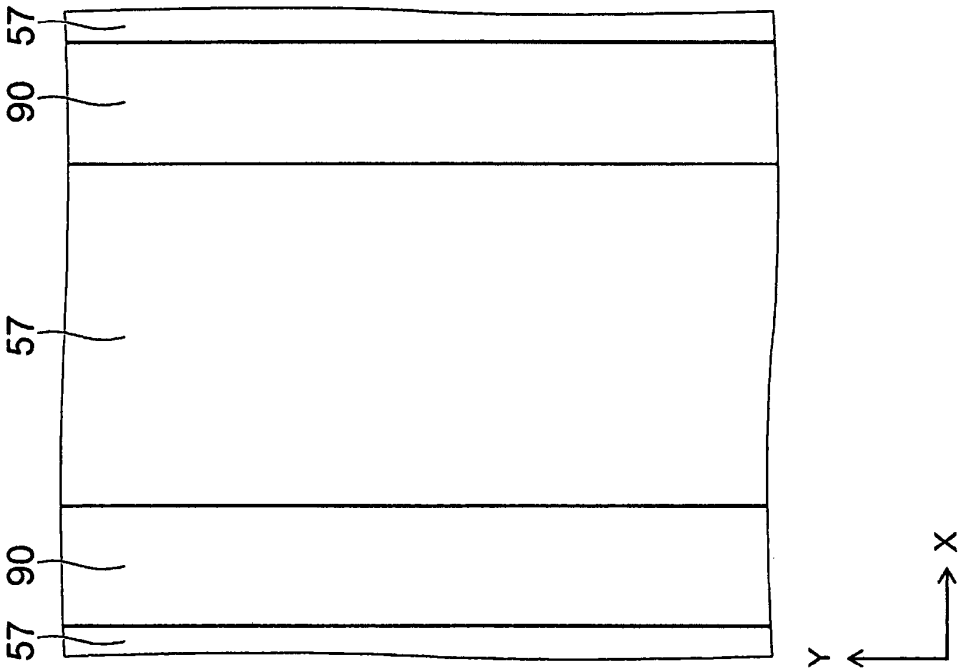


圖42B

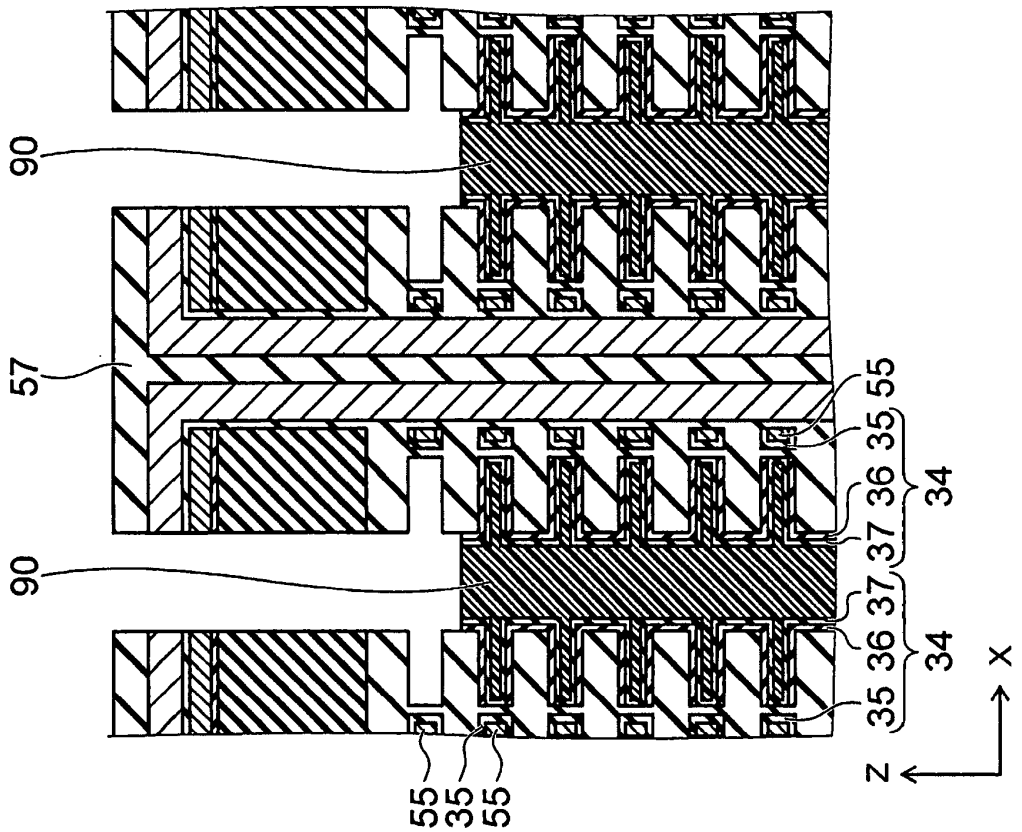


圖42A

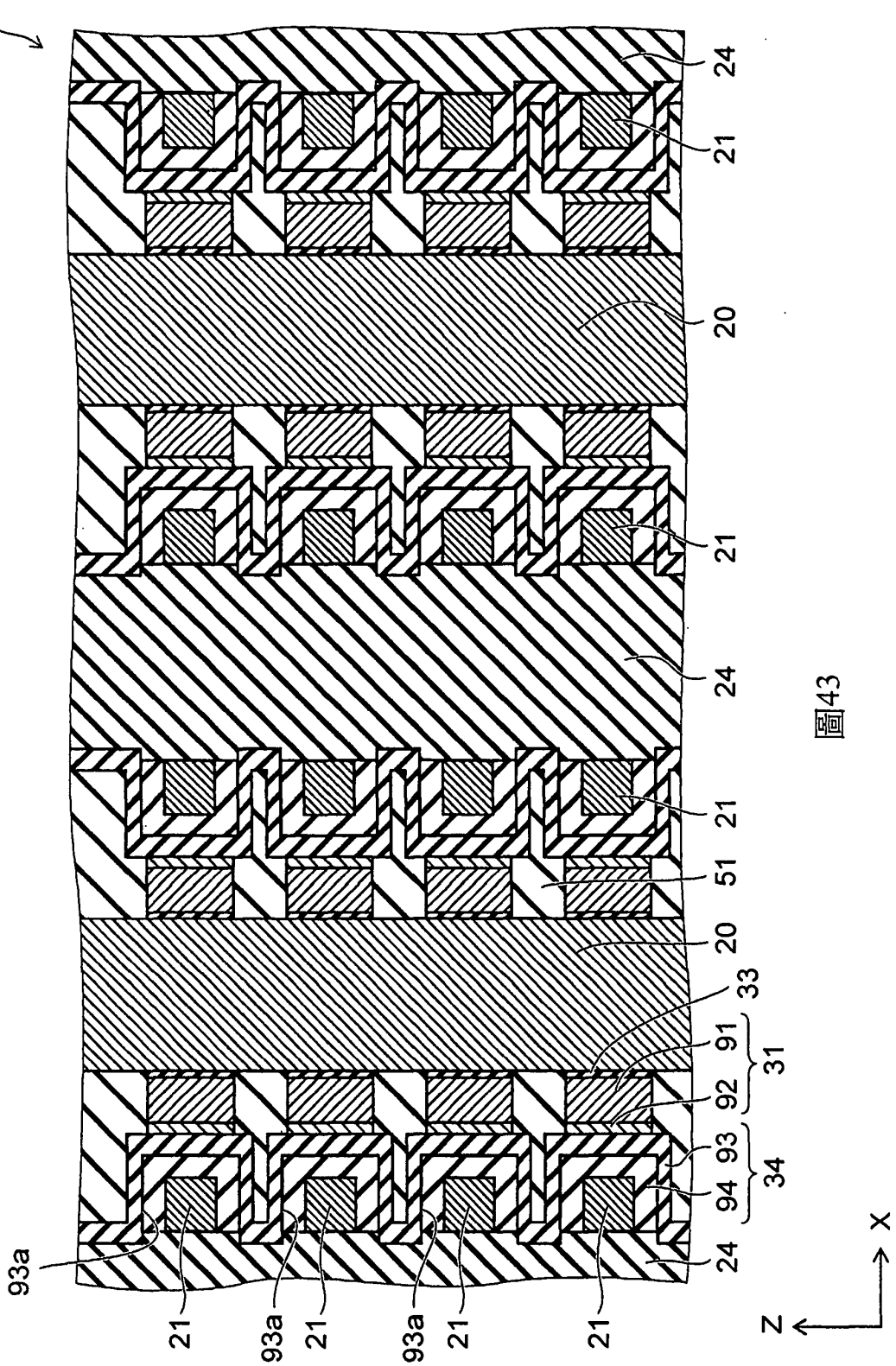


圖43

Micron Ex. 1002, p. 357
Micron v. YMTC
IPR2024-00789

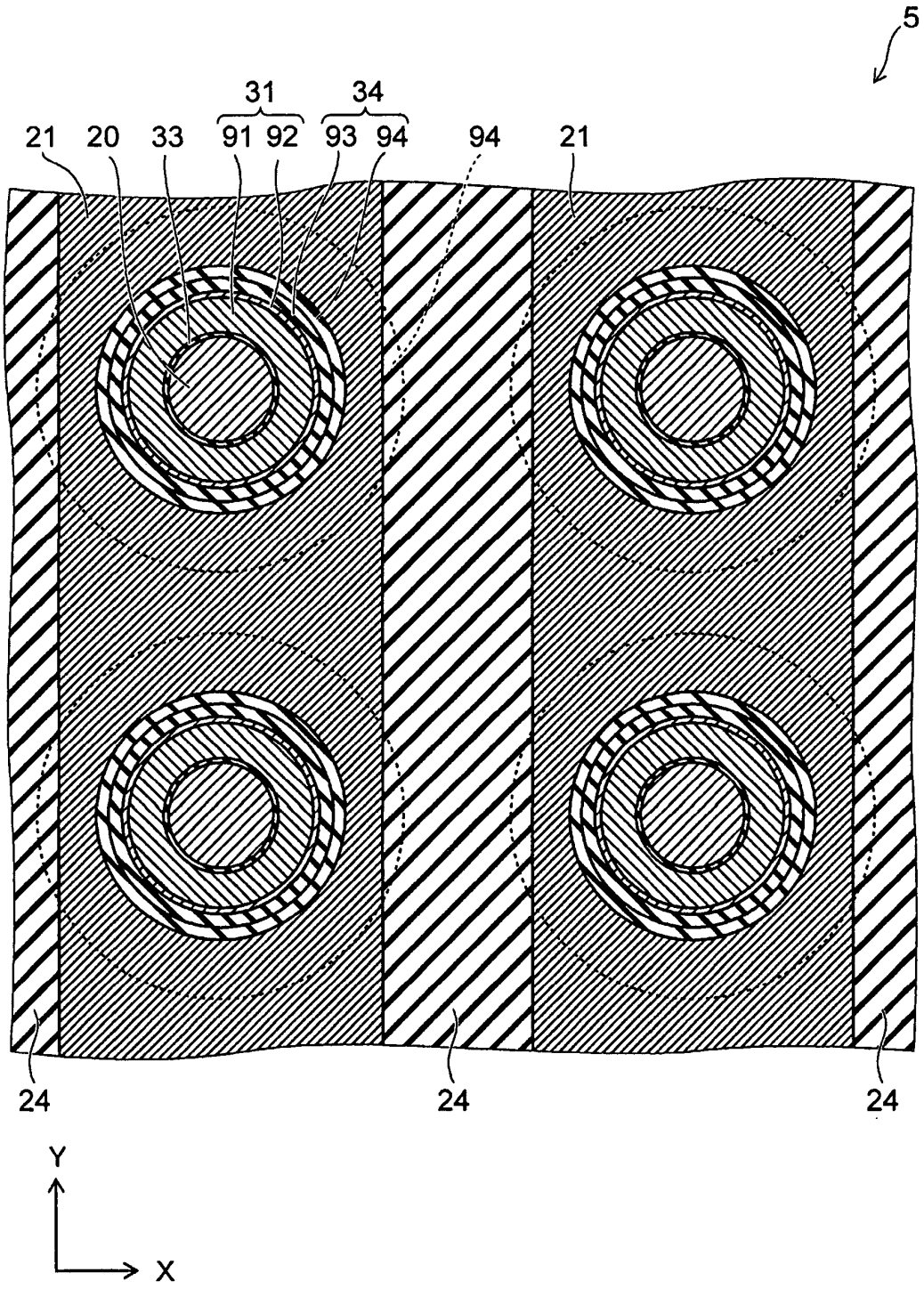


圖44

Micron Ex. 1002, p. 358
Micron v. YMTC
IPR2024-00789

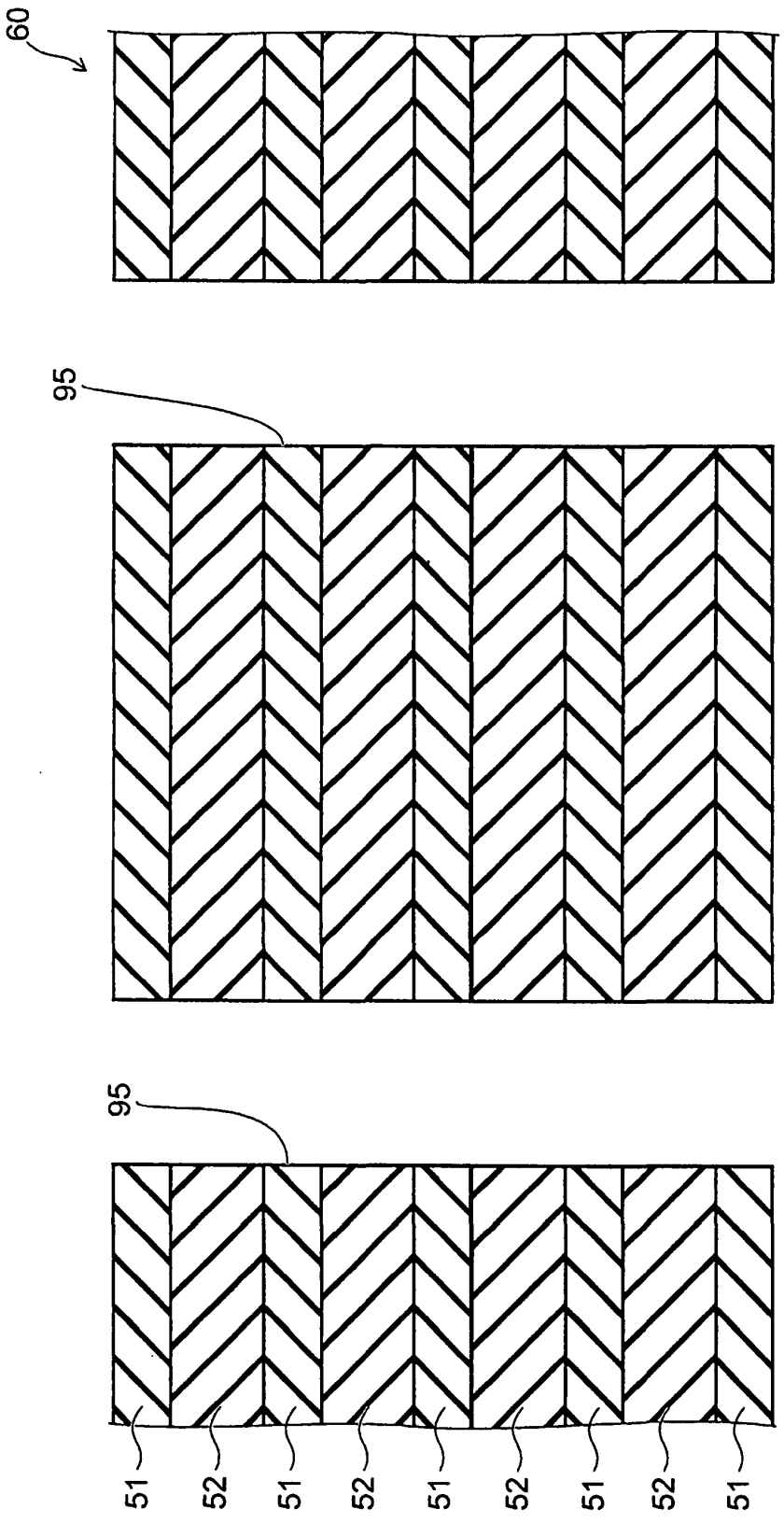


圖45

Micron Ex. 1002, p. 359
Micron v. YMTC
IPR2024-00789

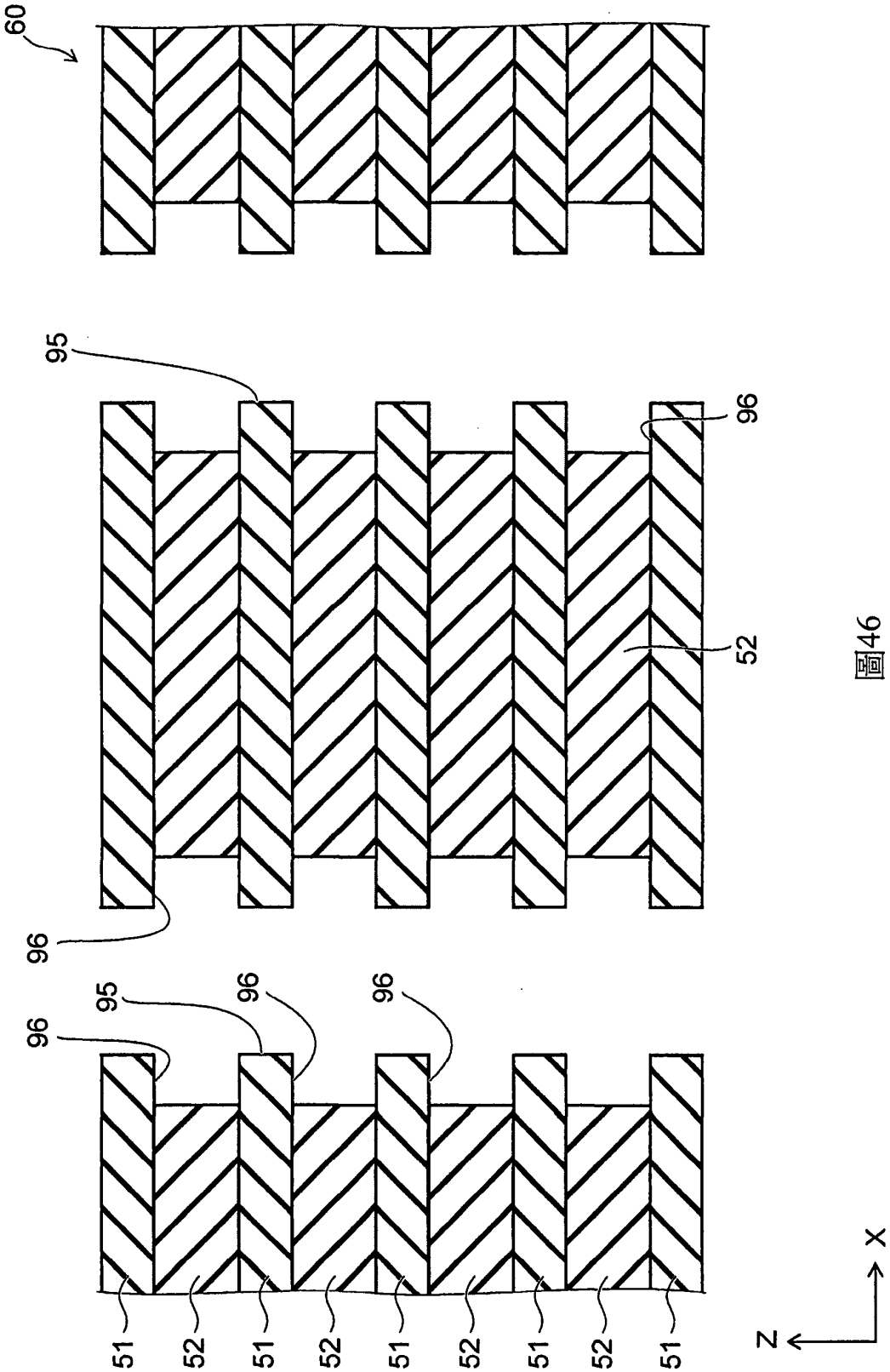


圖46

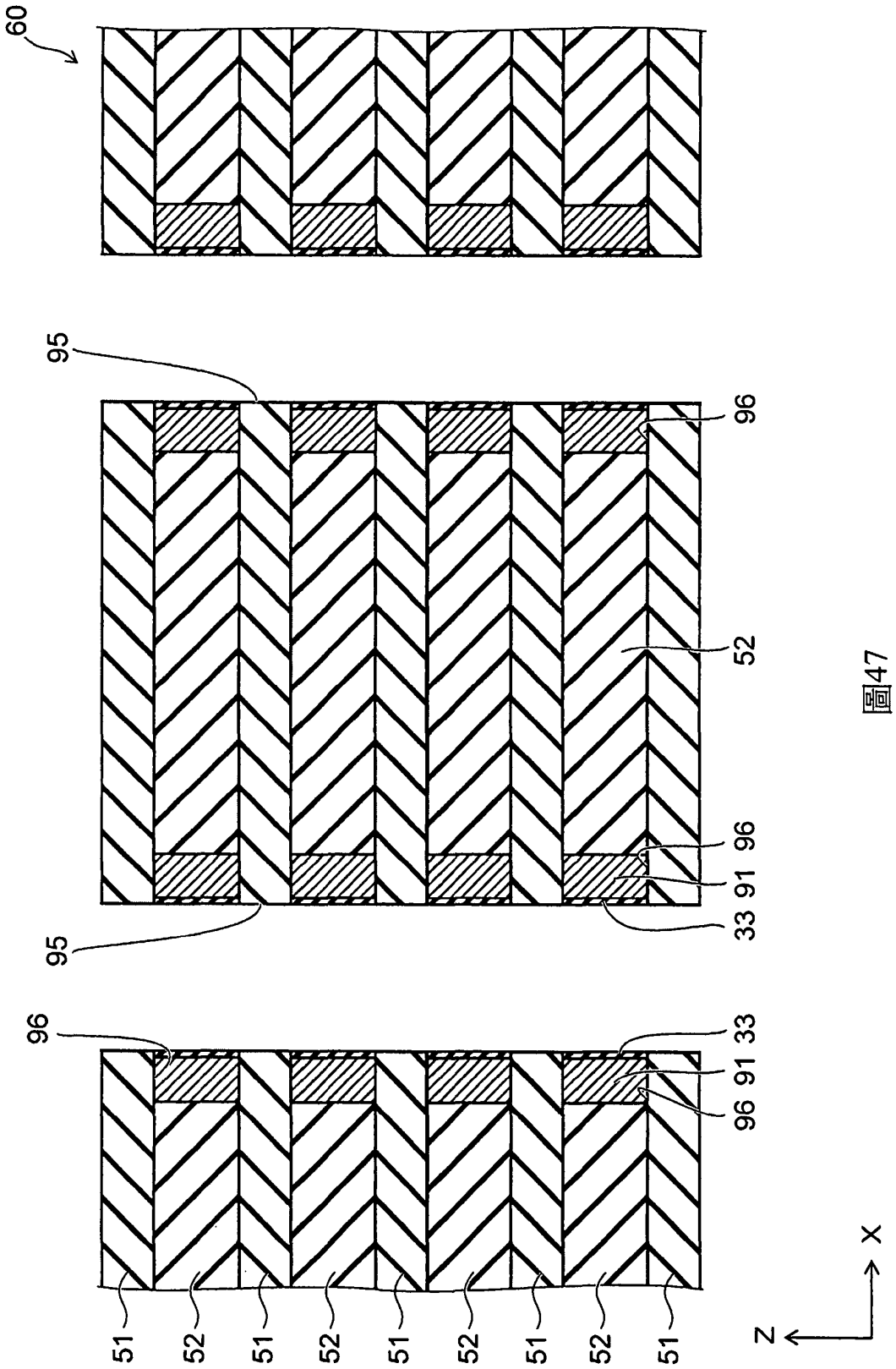


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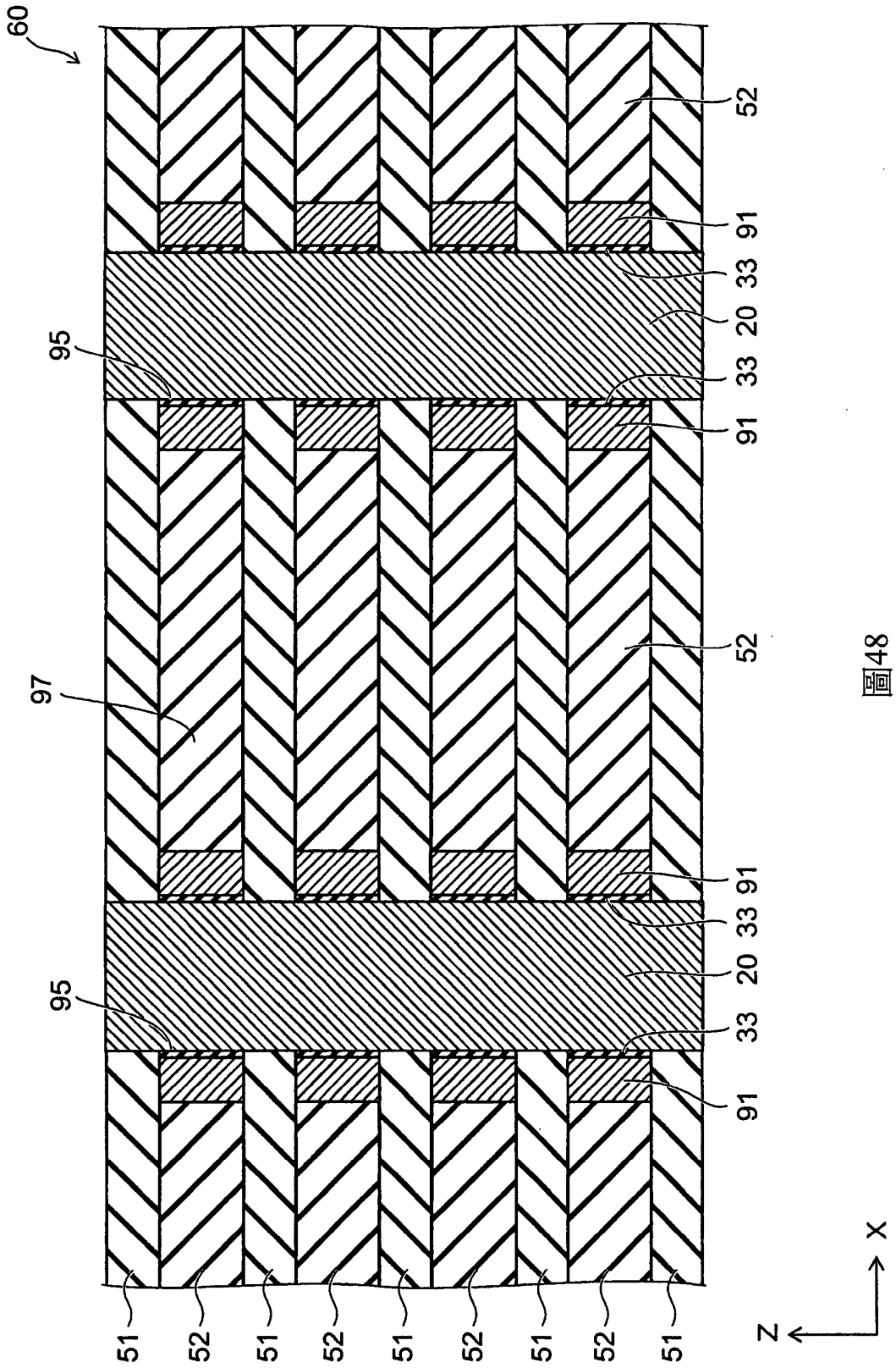

60
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51
52
51
X
Z

圖48

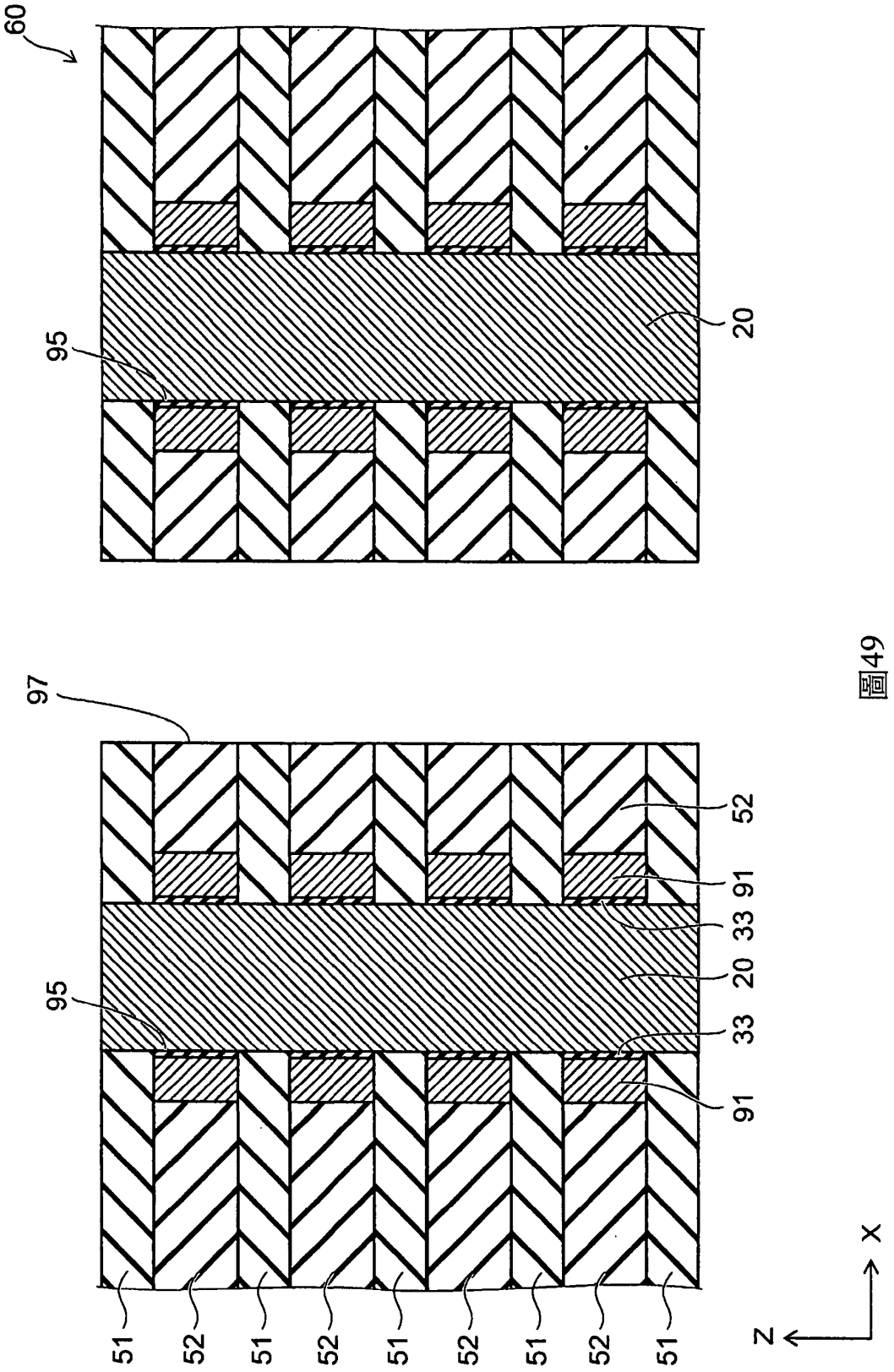


圖49

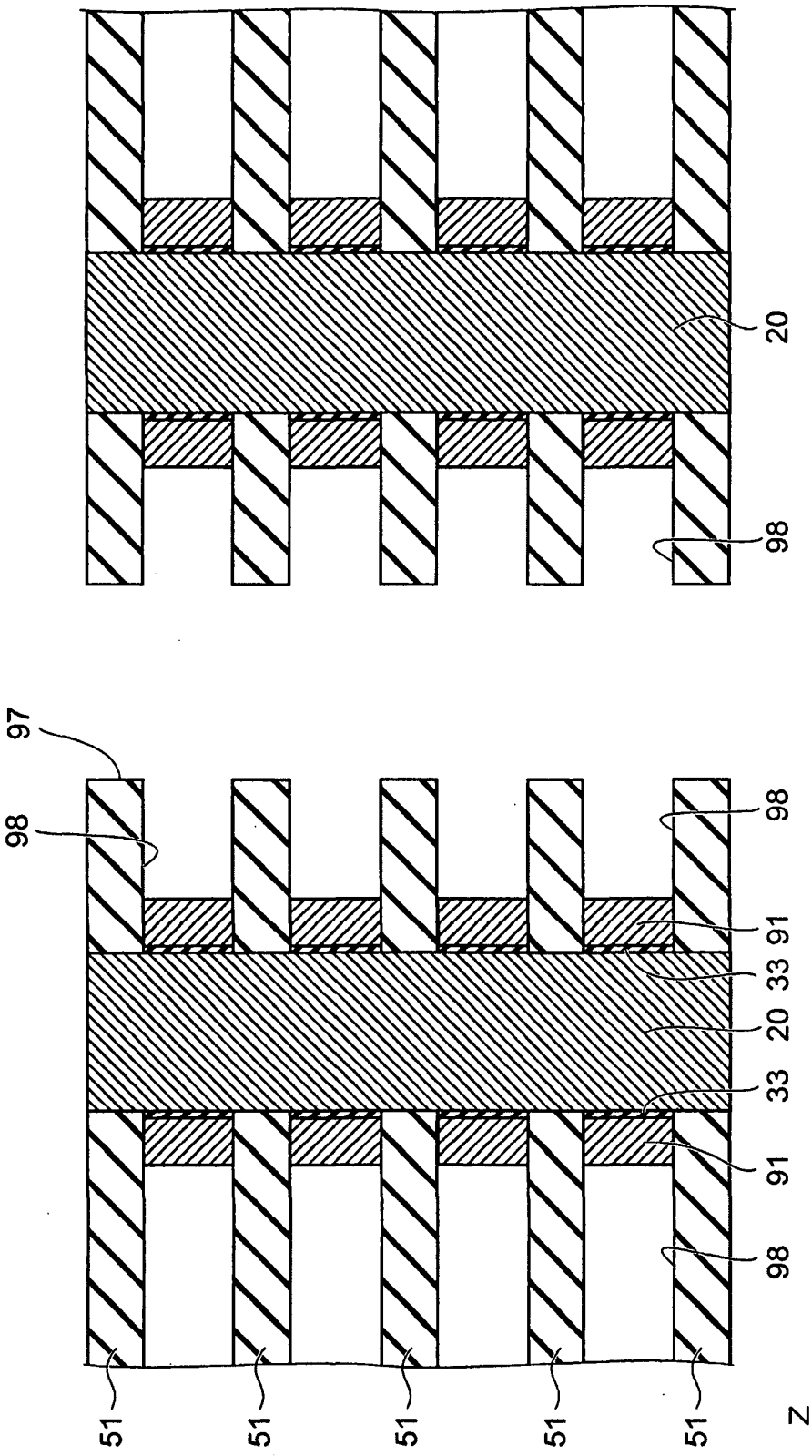


圖50

Micron Ex. 1002, p. 364
Micron v. YMTC
IPR2024-00789

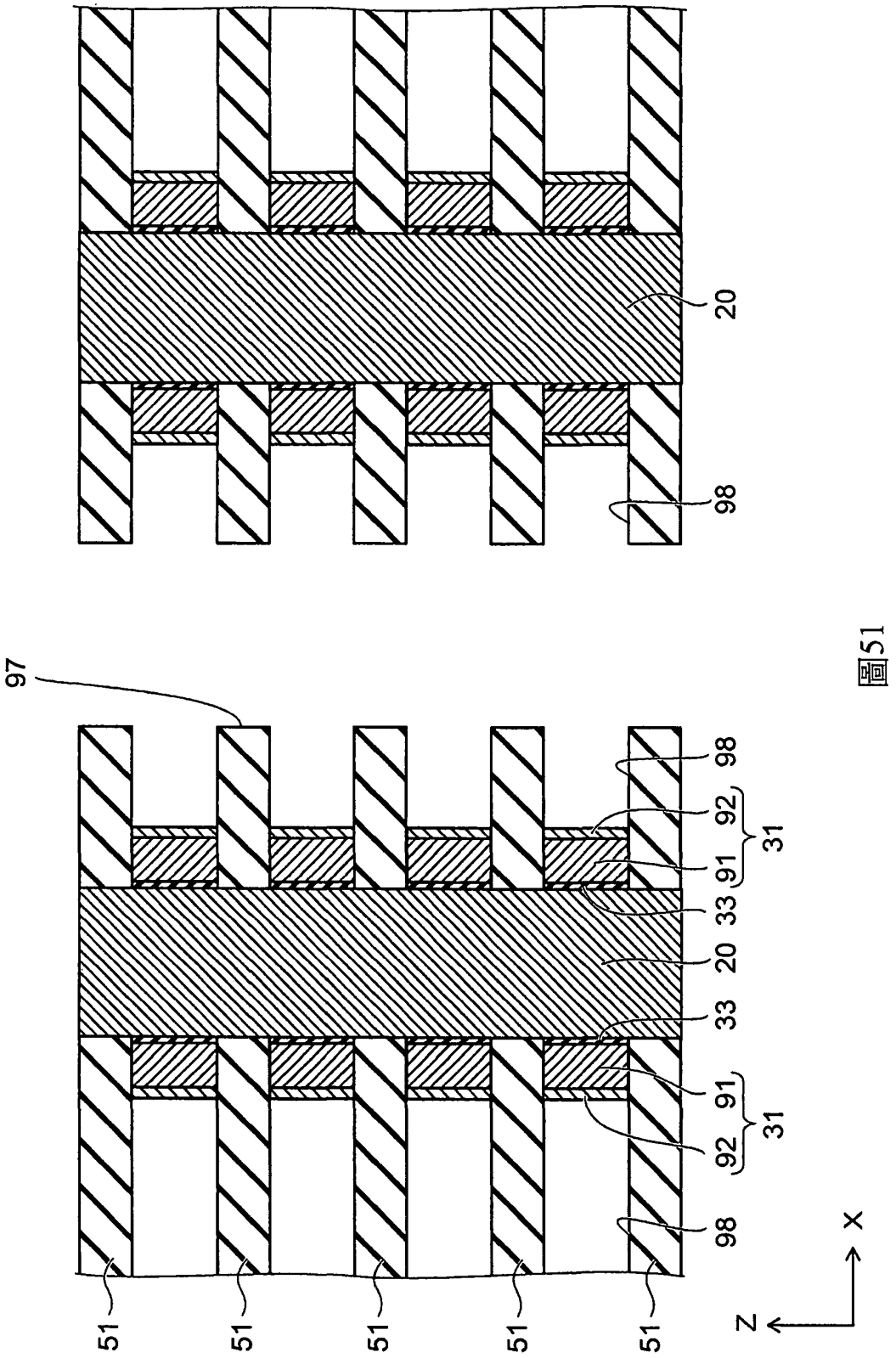


圖51

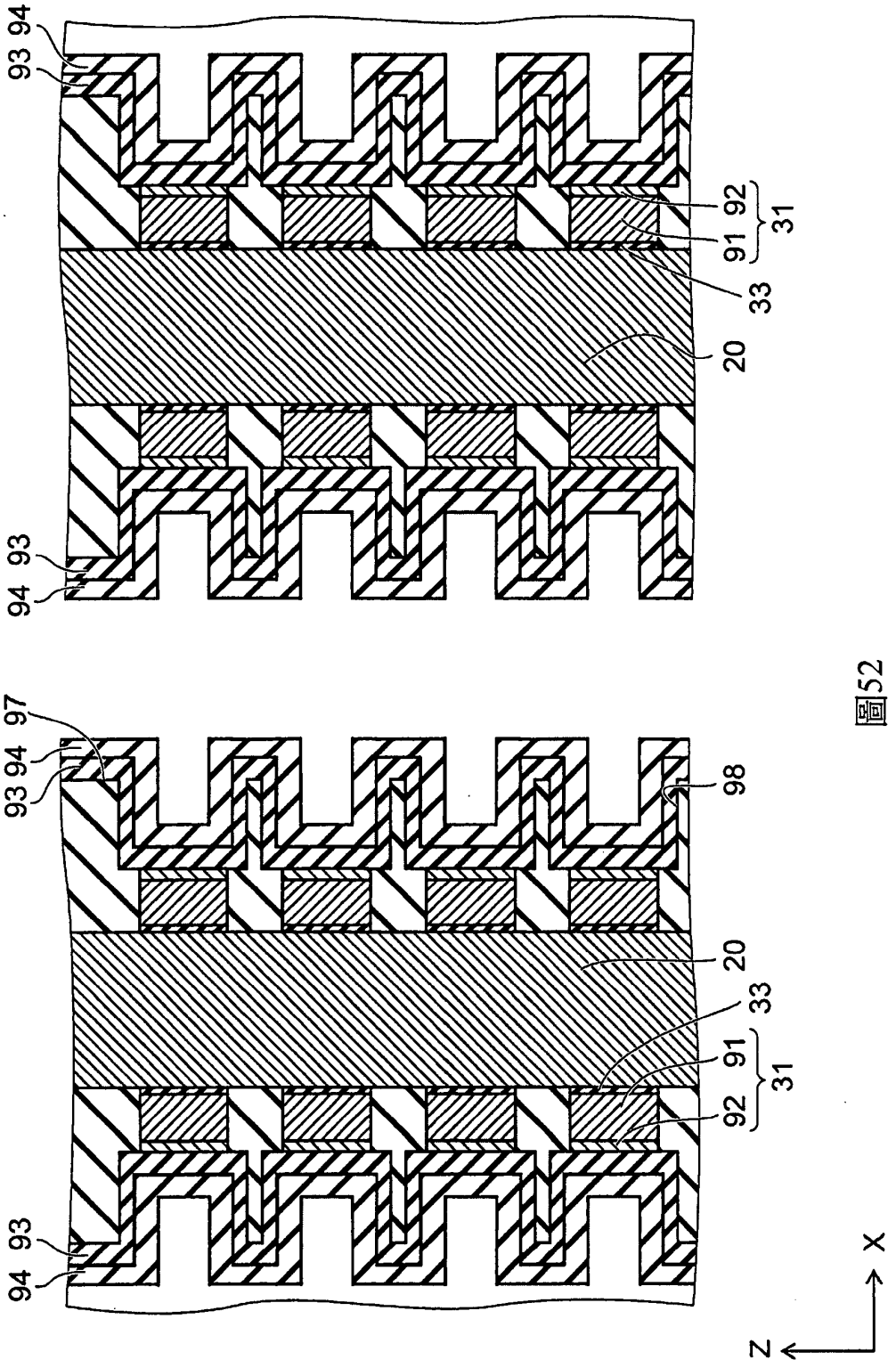


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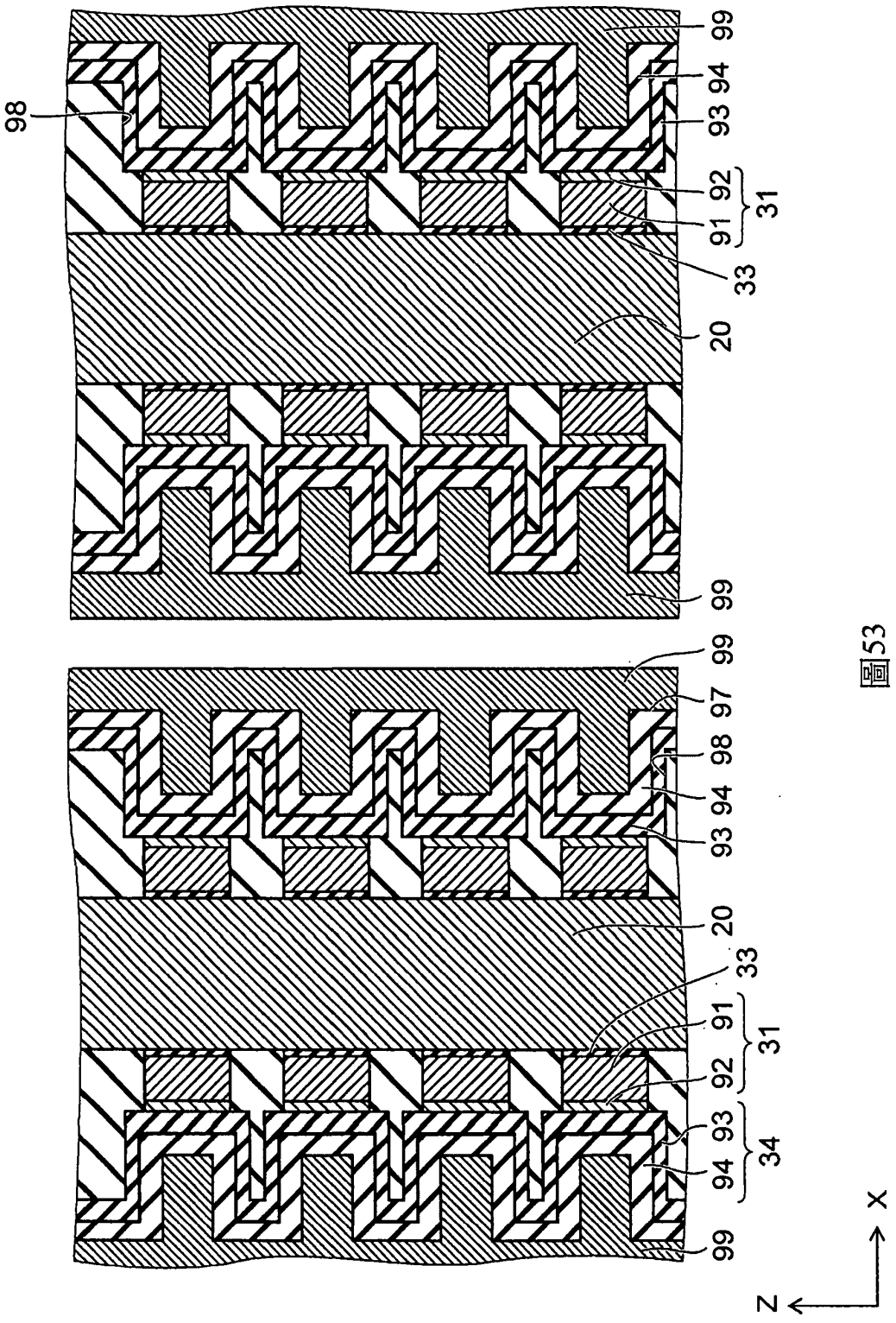


圖53

Micron Ex. 1002, p. 367
Micron v. YMTC
IPR2024-00789

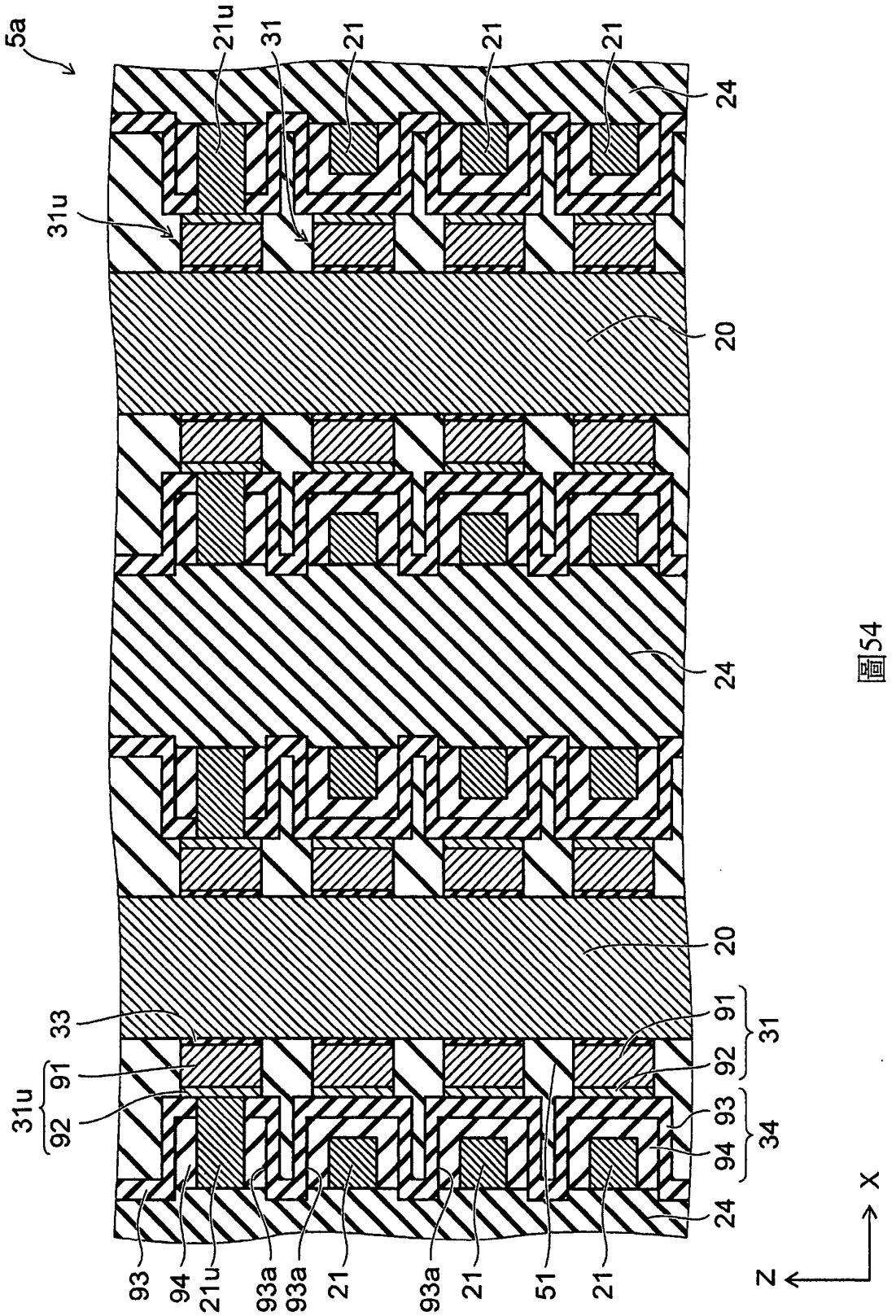

5a
21u
31
21
21
21
24
31u
20
24
20
33
91
31
31u
91
92
92
93
34
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24
93
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21u
93a
93a
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93a
21
51
21
X
Z

圖54

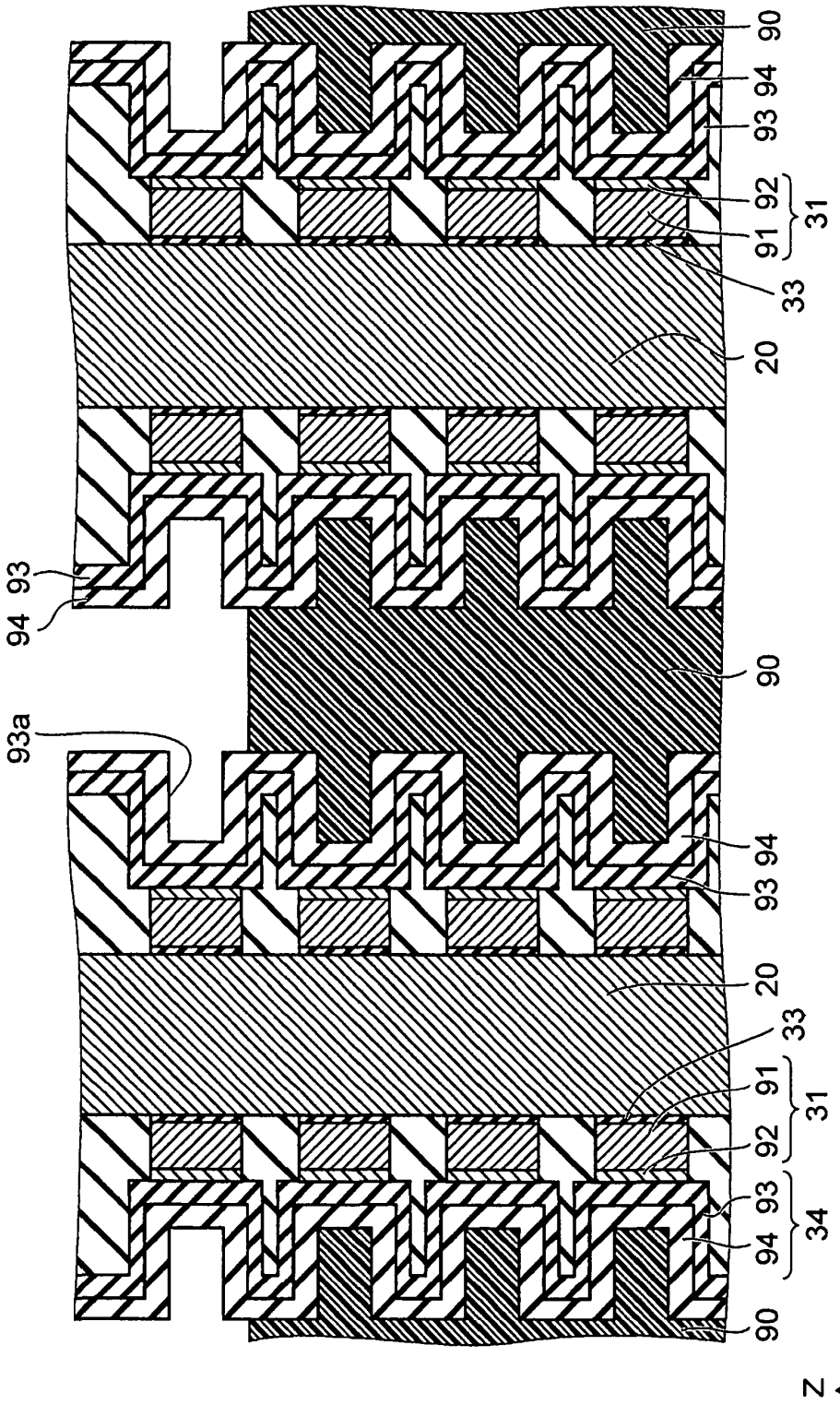


圖55

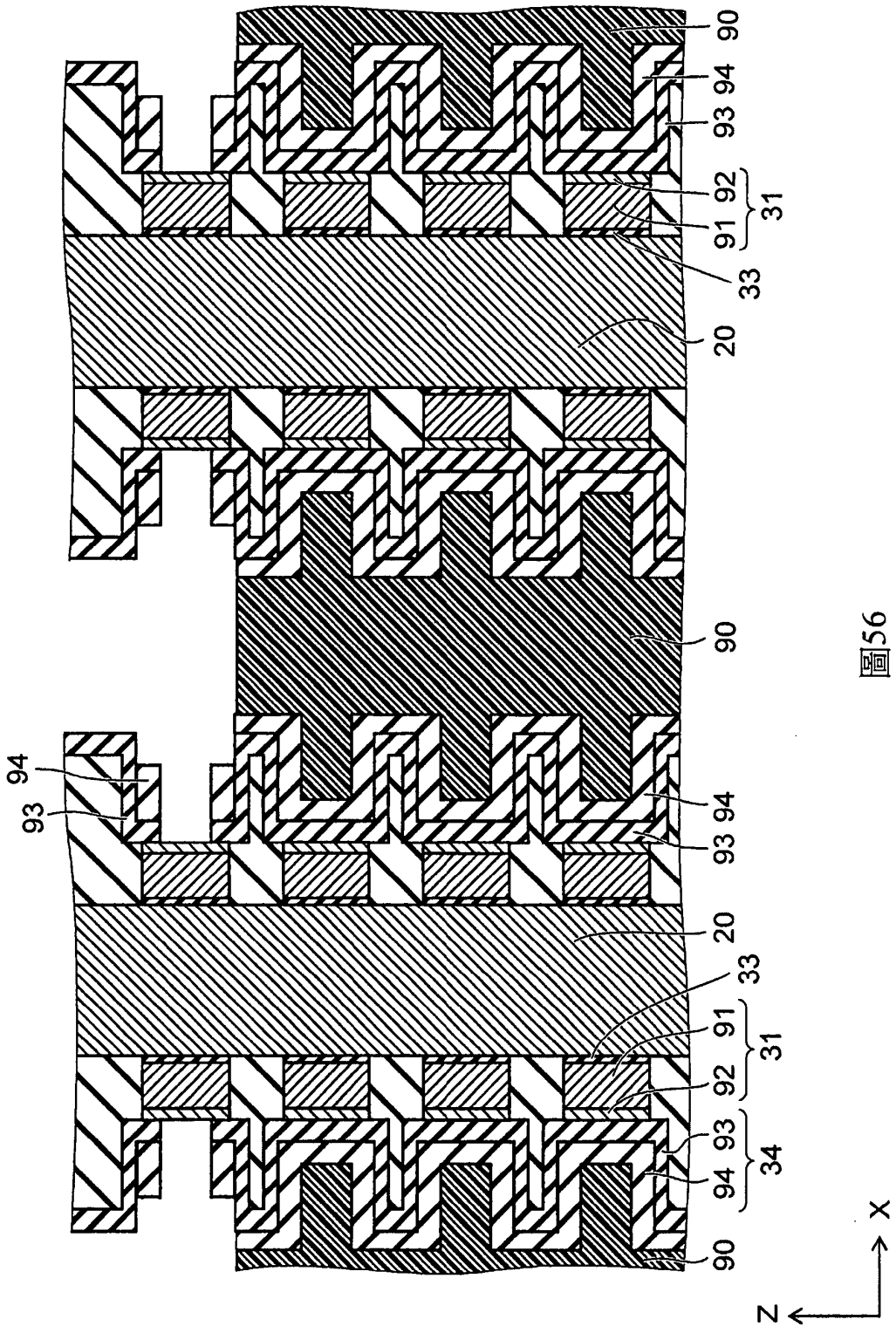


圖56

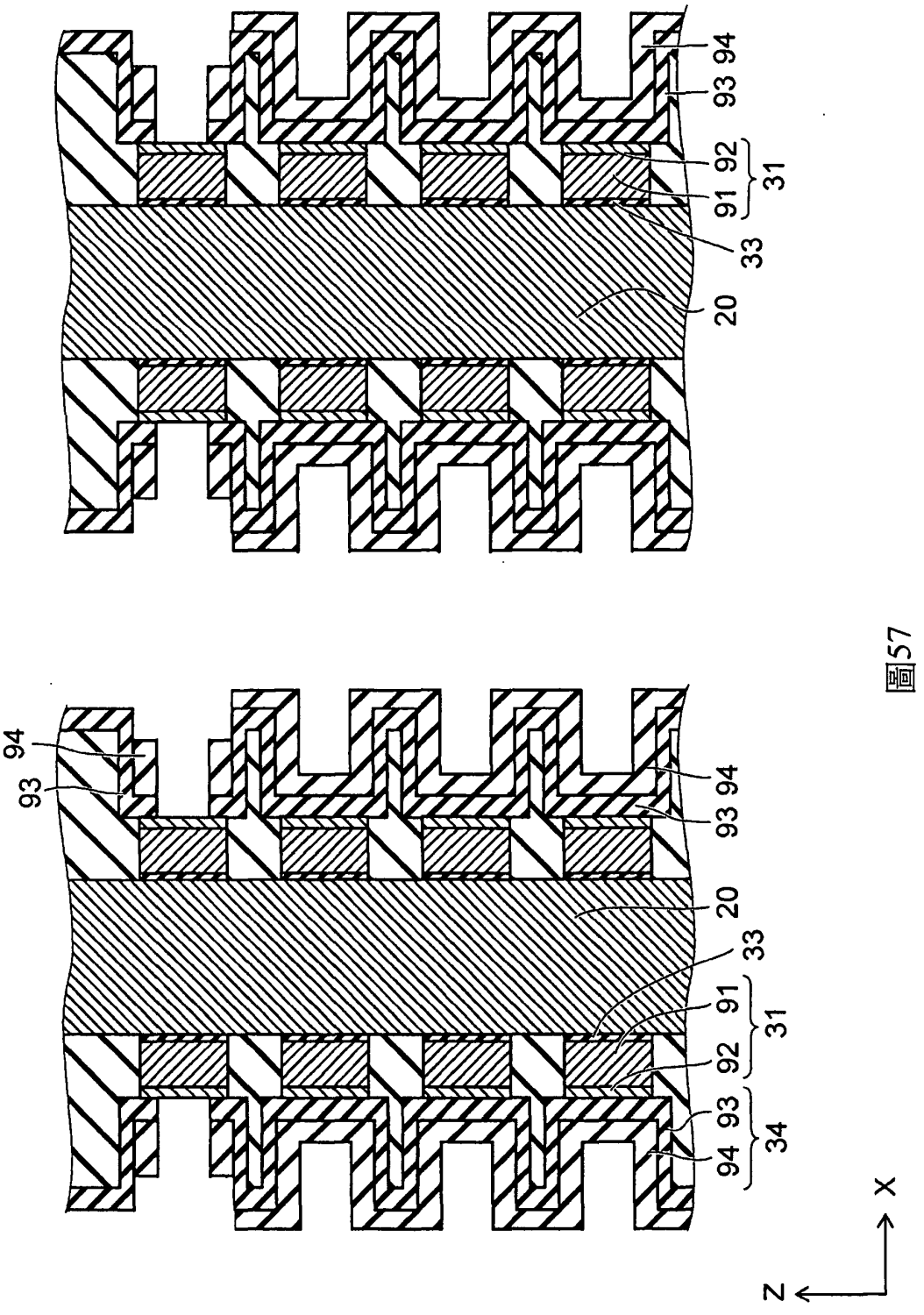


圖57

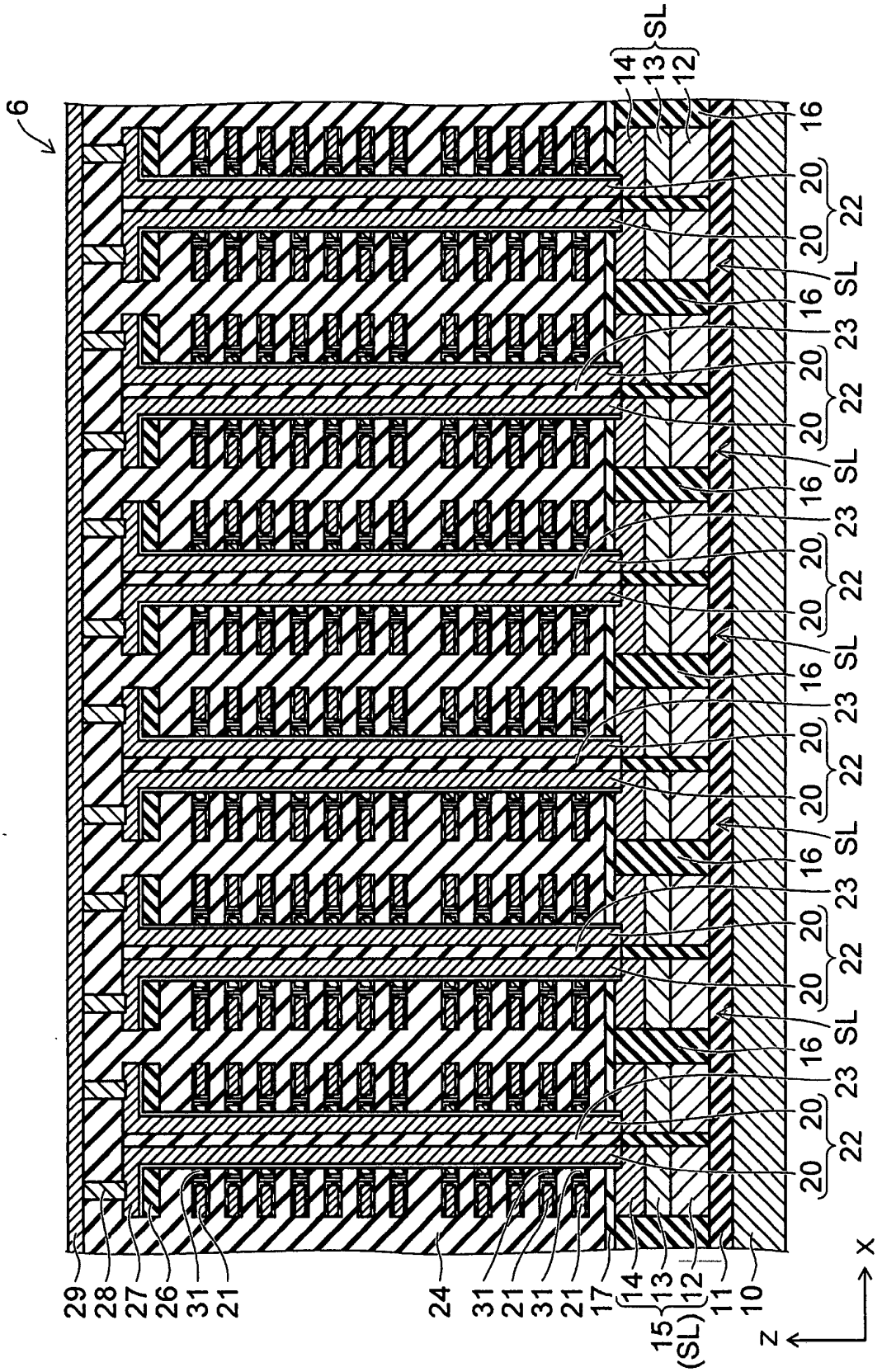


圖58

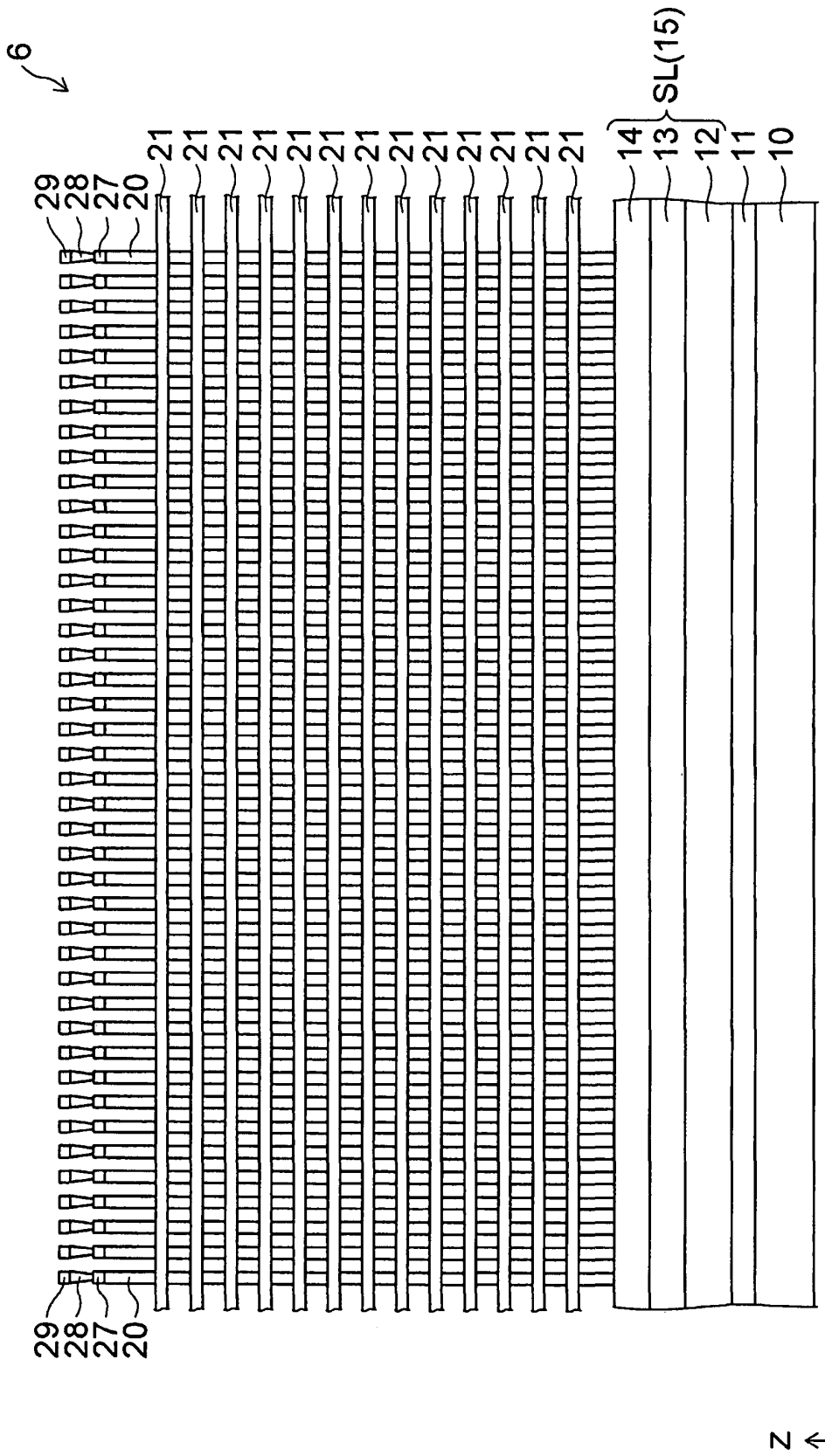


圖59

Micron Ex. 1002, p. 373
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IPR2024-00789

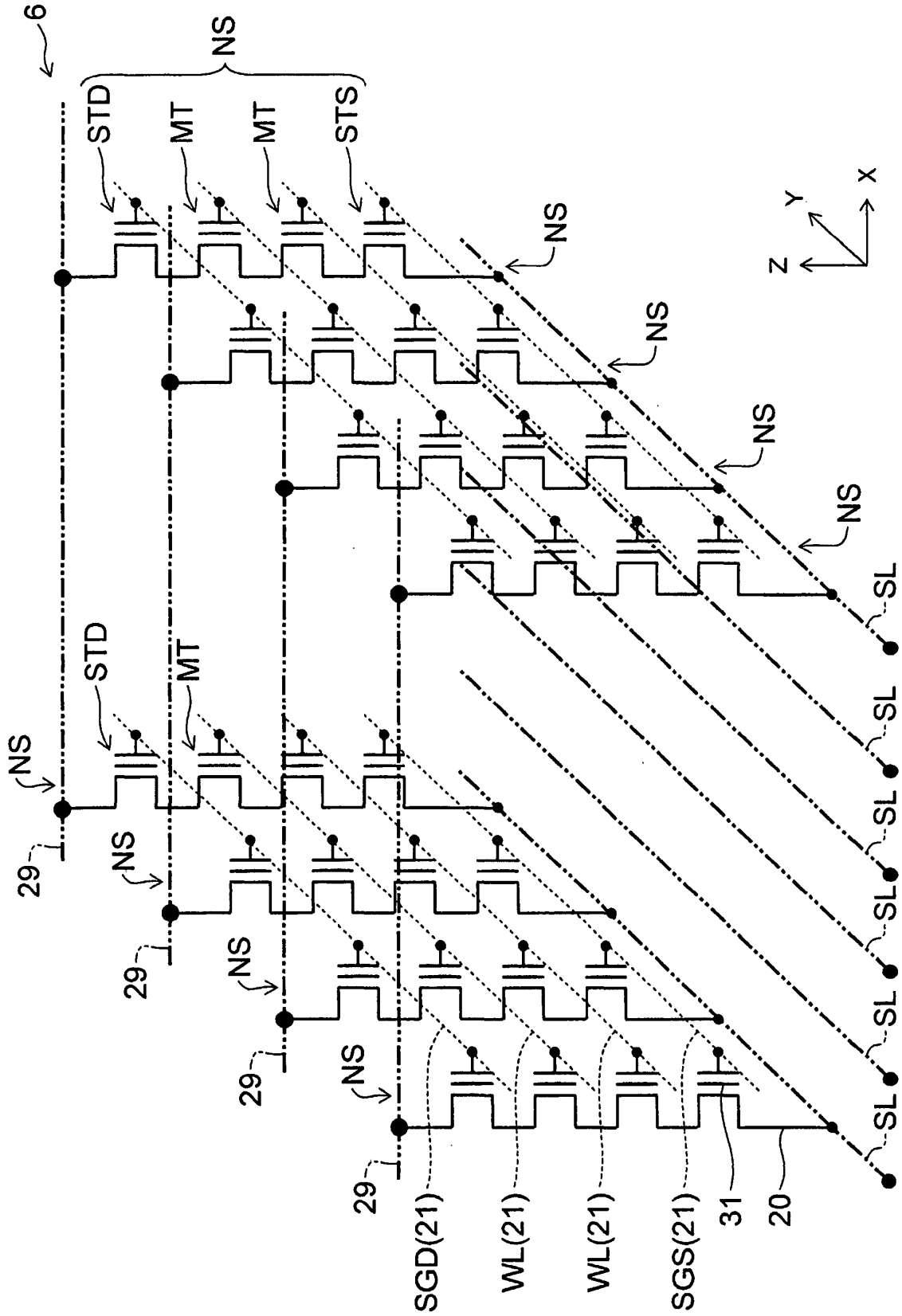

6
NS
STD
MT
MT
STS
NS
NS
NS
NS
SL
SL
SL
SL
SL
SL
STD
MT
NS
29
NS
29
NS
29
NS
29
SGD(21)
WL(21)
WL(21)
SGS(21)
31
20
Z
Y
X

圖60

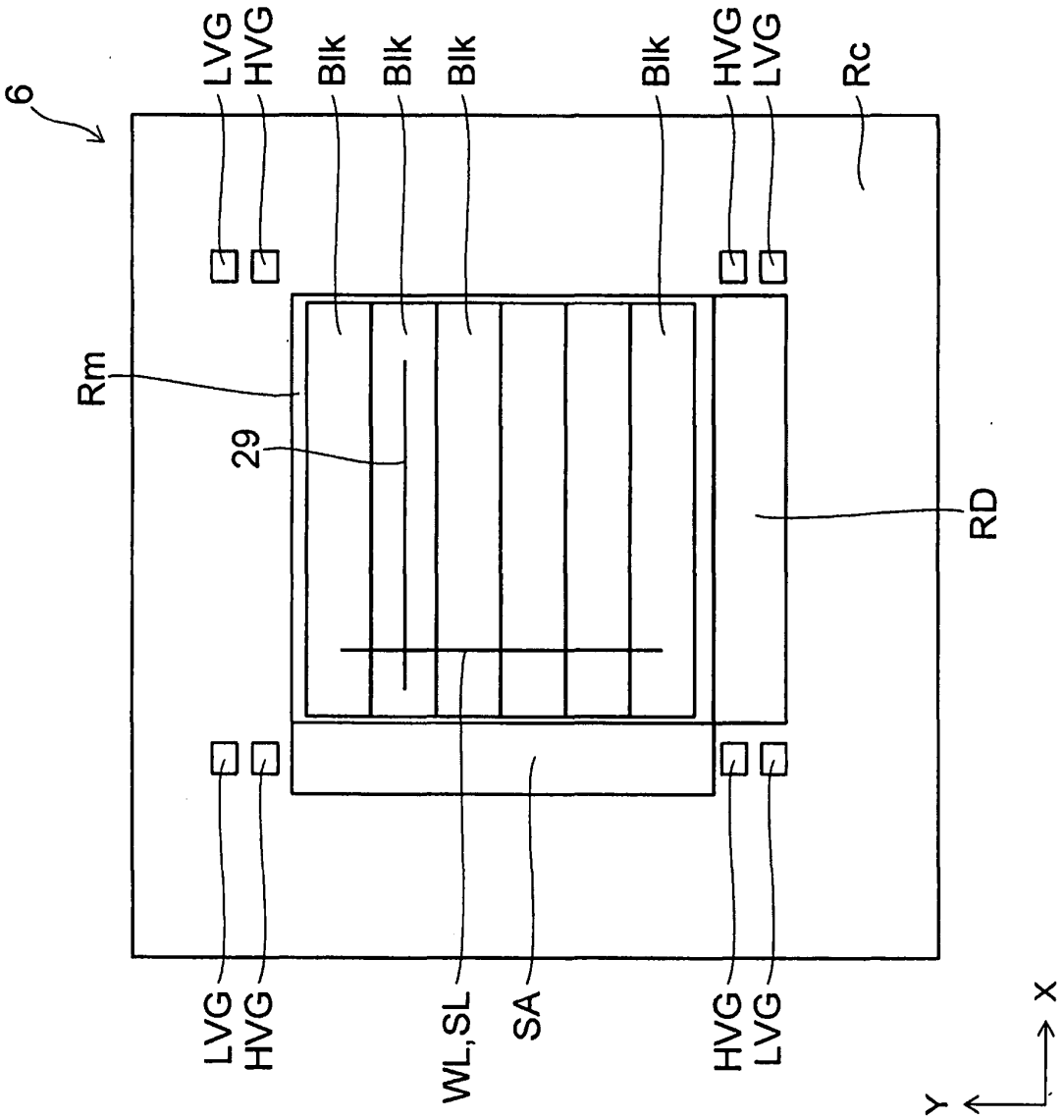

6
LVG
HVG
Blk
Blk
Blk
Blk
HVG
LVG
Rc
Rm
29
RD
LVG
HVG
WL,SL
SA
HVG
LVG
X
Y

圖61

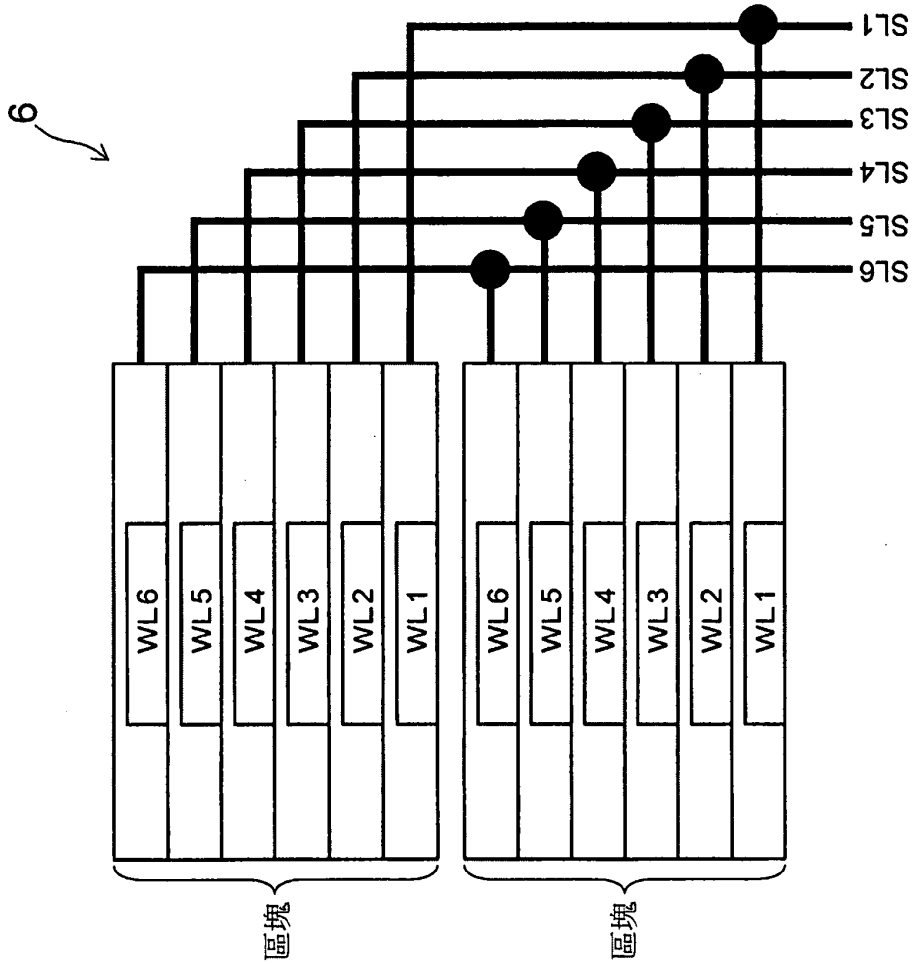


圖62

Micron Ex. 1002, p. 376
Micron v. YMTC
IPR2024-00789

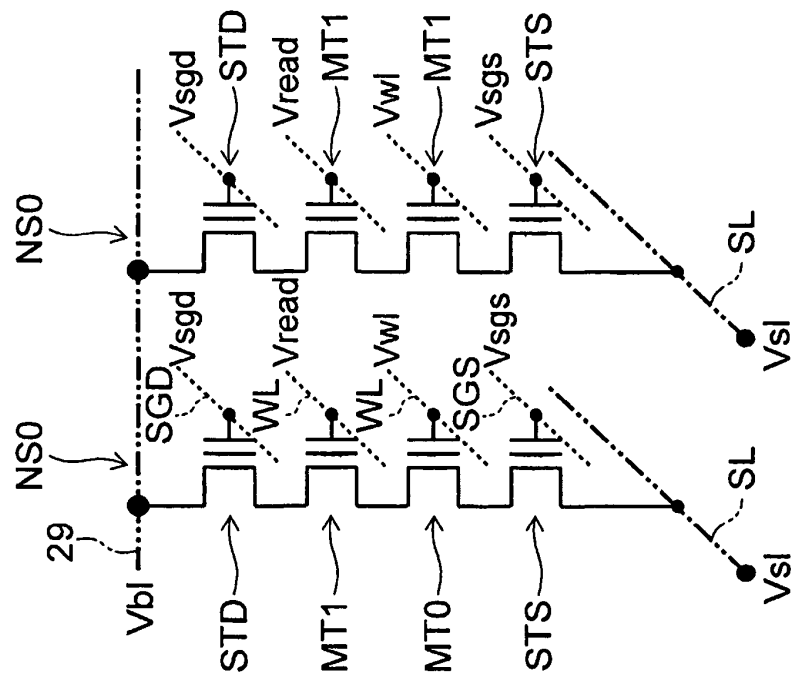


圖63A

節點	電位	電位之數值實例(V)
位元線29	Vbl	0.2~0.5
選擇閘極線SGD	Vsgd	2.5~4
非選擇字線WL	Vread	4.5~7
選擇字線WL	Vwl	0 ~ 5 (低於Vread)
選擇閘極線SGS	Vsgs	2.5~4
源極線SL	Vsl	0

選擇串

圖63B

節點	電位	電位之數值實例(V)
位元線29	Vbl	0.2~0.5
選擇閘極線SGD	Vsgd	0
非選擇字線WL	Vread	4.5~7
選擇字線WL	Vwl	0 ~ 5 (低於Vread)
選擇閘極線SGS	Vsgs	2.5~4
源極線SL	Vsl	高於零且不高於Vsgs

非選擇串

圖63C

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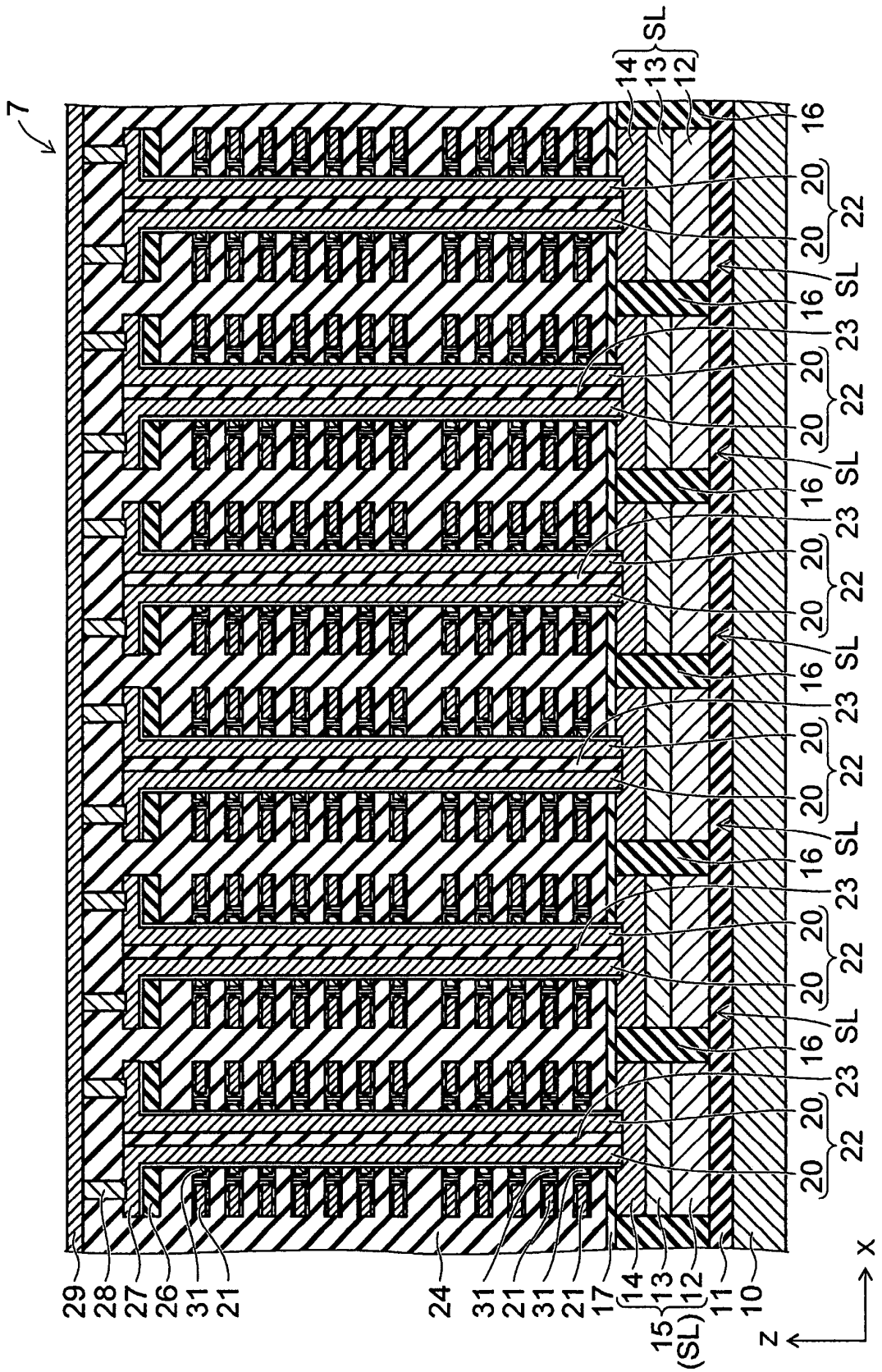


圖64

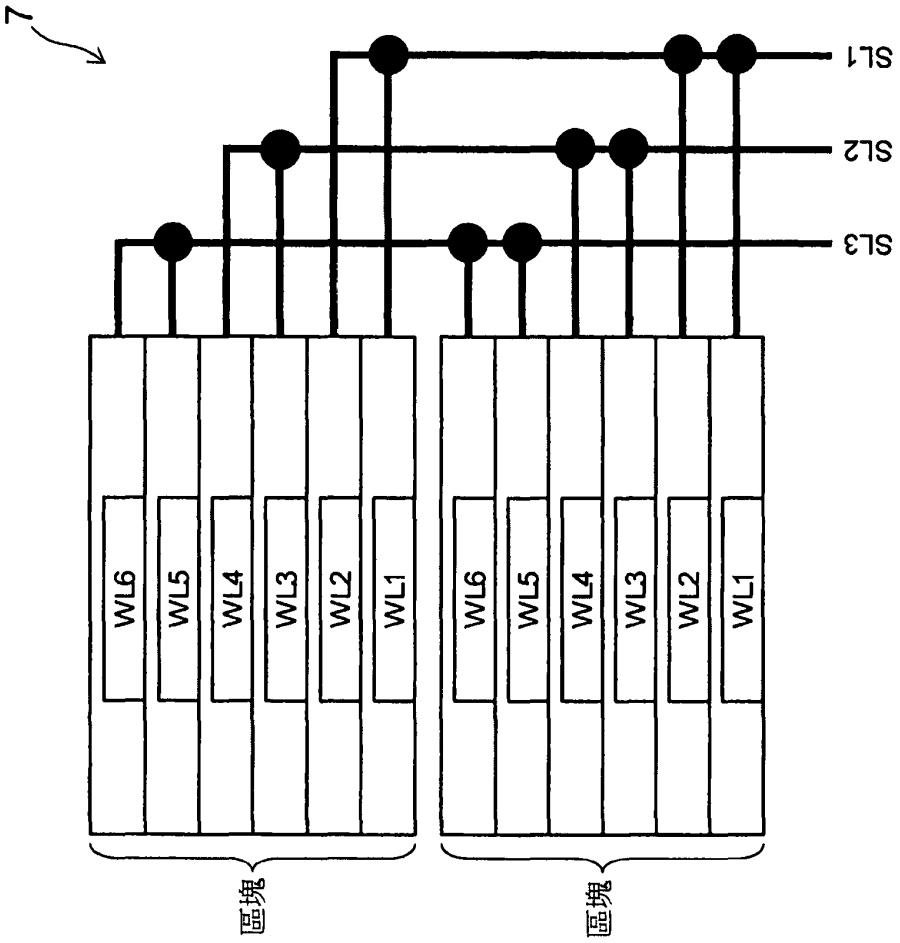

7
SL1
SL2
SL3
WL6
WL5
WL4
WL3
WL2
WL1
WL6
WL5
WL4
WL3
WL2
WL1
區塊
區塊

圖65

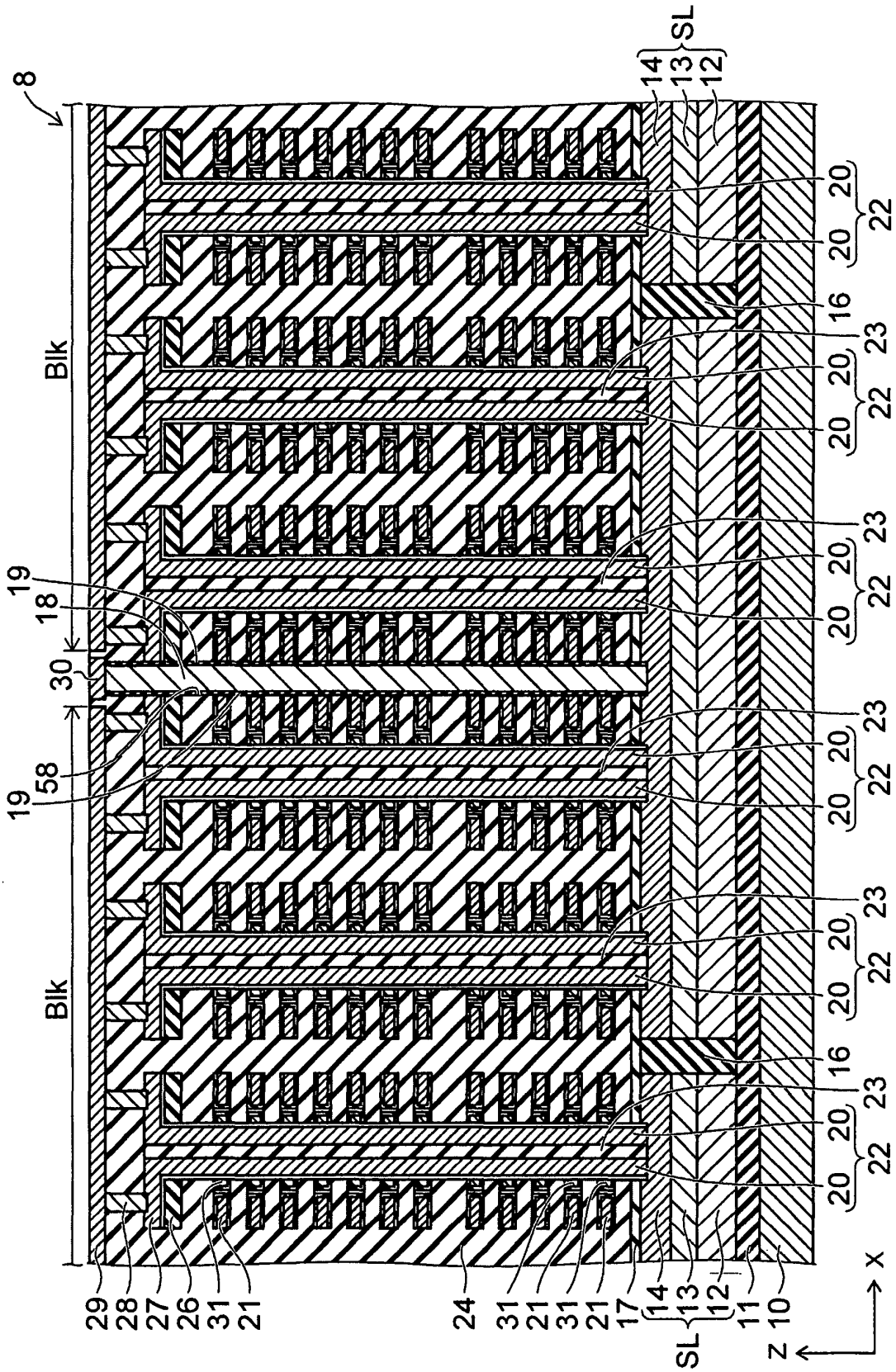

8
SL
14
13
12
Blk
Blk
19
18
30
19
58
20
22
23
16
29
28
27
26
31
21
24
17
11
10
SL
X
Z

圖66

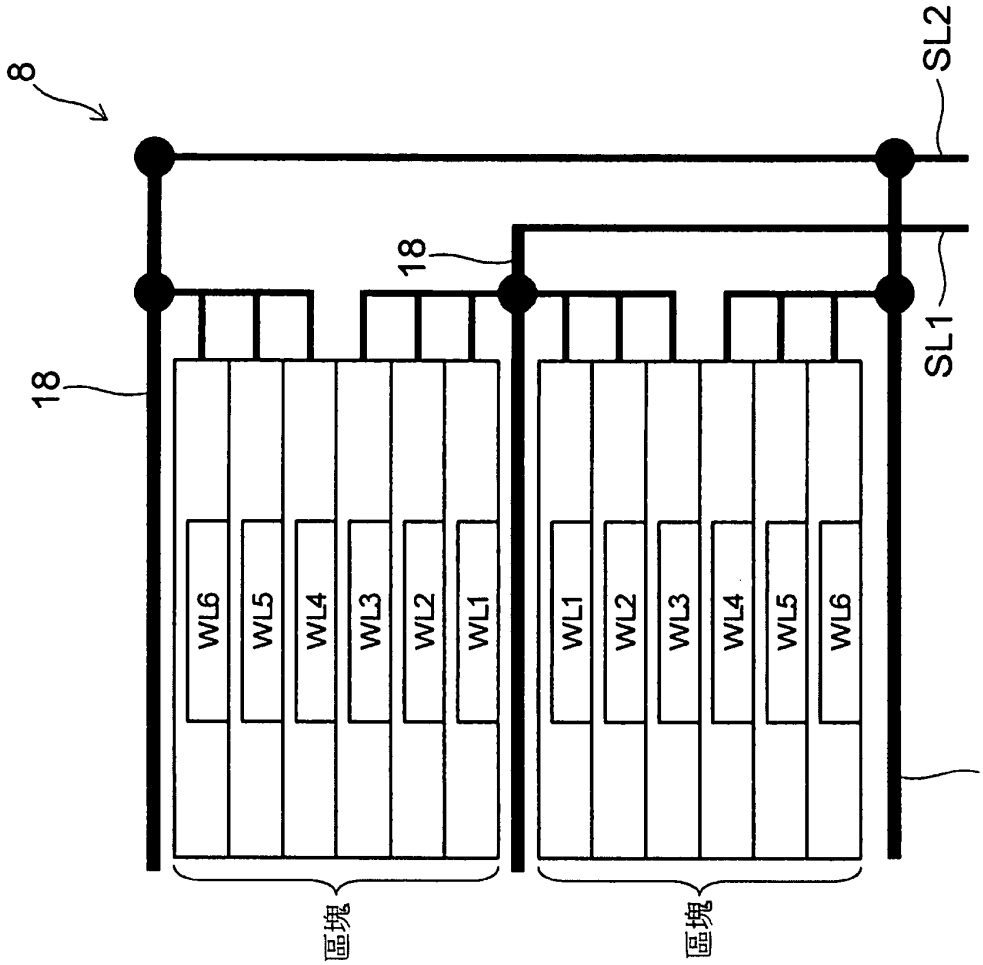


圖67

Micron Ex. 1002, p. 381
Micron v. YMTC
IPR2024-00789

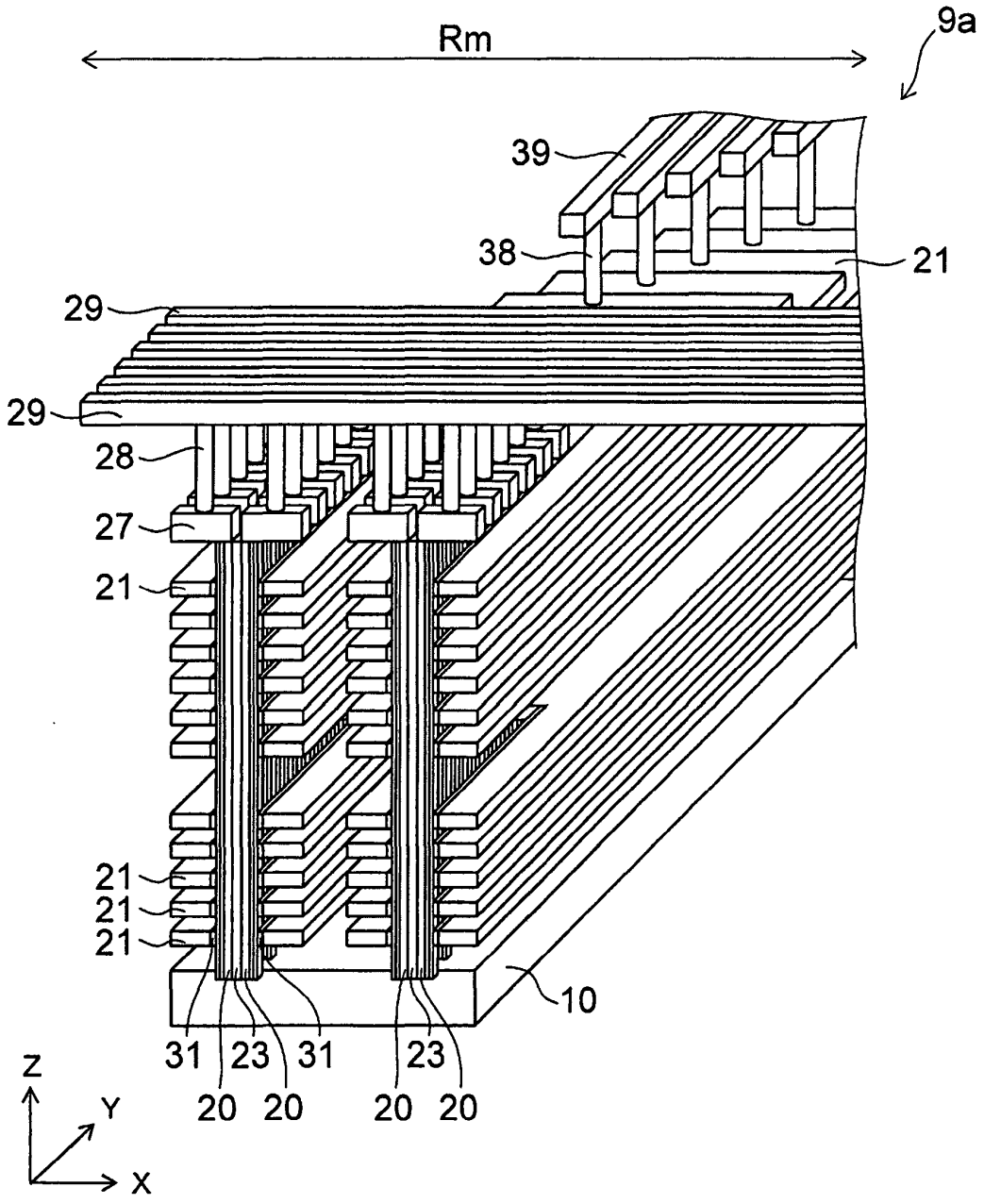


圖68

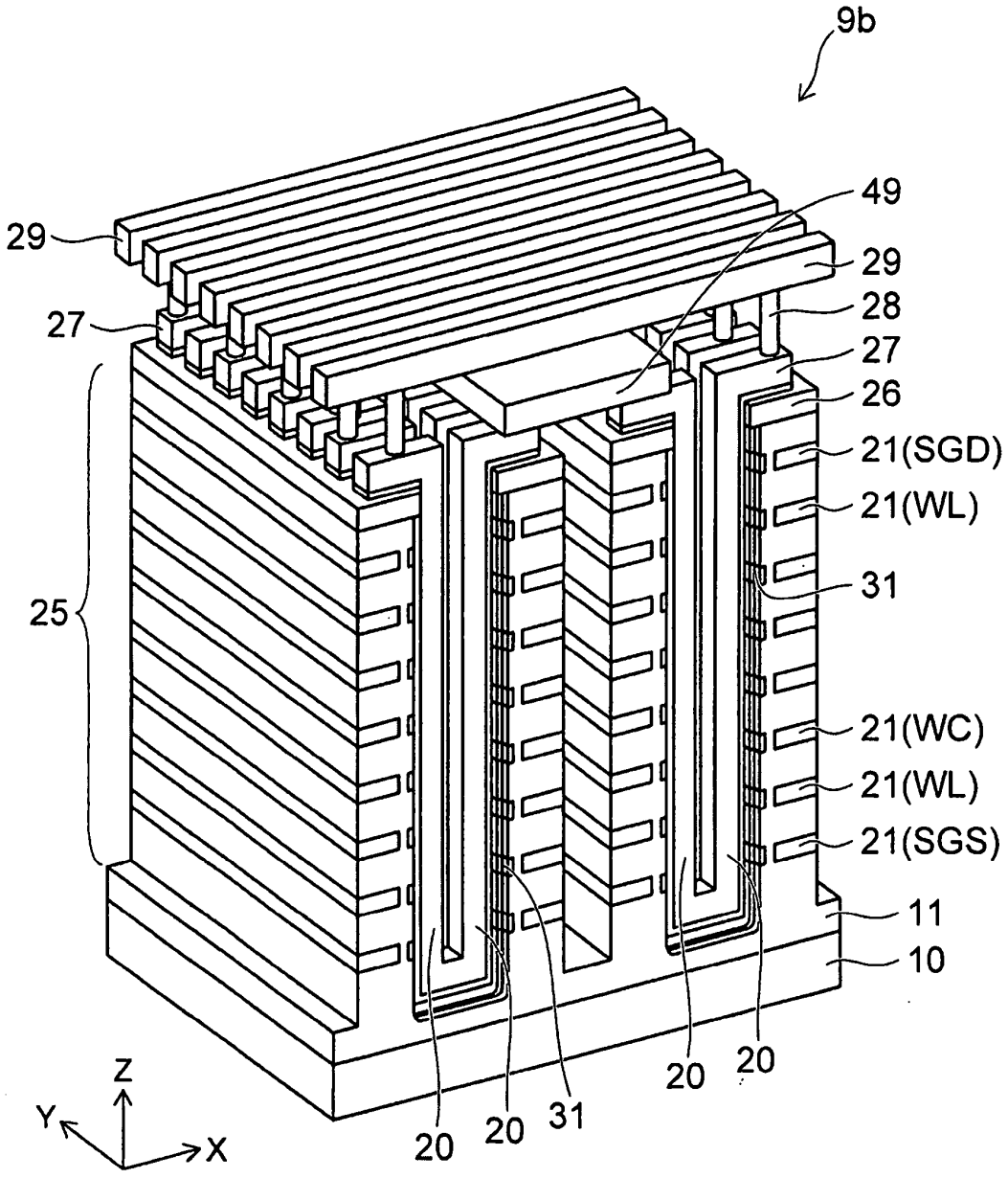

9b
49
29
29
28
27
27
26
21(SGD)
21(WL)
31
25
21(WC)
21(WL)
21(SGS)
11
10
20
20
31
20
20
Z
Y
X

圖69

Espacenet

TW201533887A Semiconductor structure and method for manufacturing the same
Applicants: MACRONIX INT CO LTD [TW]
Inventors: JIANG YU-WEI [TW], LEE GUAN-RU [TW]
IPC ***H01L21/28; H01L27/105;***

Application number: TW103106107A
Priority numbers: TW103106107A 2014-02-24
Publication date: 2015-09-01
Filing date: 2014-02-24
Priority date: 2014-02-24
Published as: TW201533887A;**TWI527196B**

Abstract: Semiconductor structure and method for manufacturing the same
A semiconductor structure and a method for manufacturing the same are disclosed. The semiconductor structure includes a substrate, a first conductive structure, a second conductive structure, a dielectric structure, a dielectric layer, a first conductive plug, and a second conductive plug. The first conductive structure is on the substrate. The second conductive structure is on the substrate and has a material different from an upper conductive portion of the first conductive structure. The dielectric structure includes an upper dielectric portion and a lower dielectric portion. The dielectric layer is between the upper dielectric portion and the lower dielectric portion, and has a material different from materials of the upper dielectric portion and the lower dielectric portion. The first conductive plug passes through only the upper dielectric portion, the dielectric layer and the lower dielectric portion to physically and electrically contact with the first conductive structure. The second conductive plug passes through the upper dielectric portion, the dielectric layer and the lower dielectric portion to physically and electrically contact with the second conductive structure.

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201533887

(19)中華民國智慧財產局

(12)發明說明書公開本 (11)公開編號：TW 201533887 A

(43)公開日： 中華民國 104 (2015) 年 09 月 01 日

(21)申請案號：103106107 (22)申請日： 中華民國 103 (2014) 年 02 月 24 日

(51)Int. Cl.： *H01L27/105 (2006.01)* *H01L21/28 (2006.01)*

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(74)代理人：祁明輝；林素華

申請實體審查：有 申請專利範圍項數：10 項 圖式數：2 共 21 頁

(54)名稱

半導體結構及其製造方法

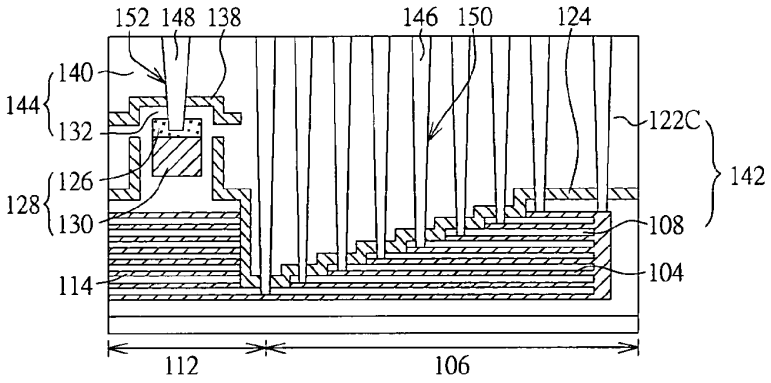
SEMICONDUCTOR STRUCTURE AND METHOD FOR MANUFACTURING THE SAME

(57)摘要

半導體結構及其製造方法。半導體結構包括一基板、一第一導電結構、一第二導電結構、介電結構、介電層、一第一導電插塞、及一第二導電插塞。第一導電結構位於基板上。第二導電結構位於基板上，並具有材料異於第一導電結構的一上導電部分。介電結構包括一上介電部分與一下介電部分。介電層介於上介電部分與下介電部分之間，且材料異於上介電部分與下介電部分。第一導電插塞僅穿過上介電部分、介電層與下介電部分，以物性且電性接觸第一導電結構。第二導電插塞穿過上介電部分、介電層與下介電部分，以物性且電性接觸第二導電結構。

A semiconductor structure and a method for manufacturing the same are disclosed. The semiconductor structure includes a substrate, a first conductive structure, a second conductive structure, a dielectric structure, a dielectric layer, a first conductive plug, and a second conductive plug. The first conductive structure is on the substrate. The second conductive structure is on the substrate and has a material different from an upper conductive portion of the first conductive structure. The dielectric structure includes an upper dielectric portion and a lower dielectric portion. The dielectric layer is between the upper dielectric portion and the lower dielectric portion, and has a material different from materials of the upper dielectric portion and the lower dielectric portion. The first conductive plug passes through only the upper dielectric portion, the dielectric layer and the lower dielectric portion to physically and electrically contact with the first conductive structure. The second conductive plug passes through the upper dielectric portion, the dielectric layer and the lower dielectric portion to physically and electrically contact with the second conductive structure.

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第 1H 圖

104・・・第一導電結構
106・・・第一電路區
108・・・下介電部分
112・・・第二電路區域
114・・・導電條紋
122C・・・上介電部分
124・・・介電層
126・・・上導電部分
128・・・第二導電結構
130・・・下導電部分
132・・・下介電部分
138・・・介電層
140・・・上介電部分
142・・・介電結構
144・・・介電結構
146・・・第一導電插塞
148・・・第二導電插塞
150・・・穿孔
152・・・穿孔

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【發明說明書】

【中文發明名稱】　半導體結構及其製造方法

【英文發明名稱】　semiconductor structure and method for manufacturing the same

【技術領域】

【0001】　本發明是有關於一種半導體結構及其製造方法，且特別是有關於一種具有導電插塞的半導體結構及其製造方法。

【先前技術】

【0002】　半導體結構包括記憶裝置係使用於許多產品之中，例如MP3播放器、數位相機、電腦檔案等等之儲存元件中。隨著應用的增加，對於記憶裝置的需求也趨向較小的尺寸、較大的記憶容量。因應這種需求，係需要製造高元件密度的記憶裝置。

【0003】　由於裝置臨界尺寸已經降低到技術之極限，因此設計者們開發一種提高記憶裝置密度的方法係使用三維堆疊記憶裝置，藉以達成更高的記憶容量，同時降低每一位元之成本。然而，此種記憶裝置複雜的結構也使得製造方法變得複雜。

【發明內容】

【0004】　根據一實施例，揭露一種半導體結構的製造方法。方法包括以下步驟。形成一第一導電結構於一基板上。形成一第二導電結構於基板上。第二導電結構具有材料異於第一導電結構的一上導電部分。形成一介電結構的一下介電部分於第一導電結構與第二導電結構上。形成介電層於下介電部分上。形成介電結構的一上介電

部分於介電層上。介電層的材料異於上介電部分與下介電部分。形成一第一導電插塞，僅穿過上介電部分、介電層與下介電部分，以物性且電性接觸第一導電結構。形成一第二導電插塞，穿過上介電部分、介電層與下介電部分，以物性且電性接觸第二導電結構。

【0005】 根據另一實施例，揭露一種半導體結構，包括一基板、一第一導電結構、一第二導電結構、介電結構、介電層、一第一導電插塞、及一第二導電插塞。第一導電結構位於基板上。第二導電結構位於基板上，並具有材料異於第一導電結構的一上導電部分。介電結構包括一上介電部分與一下介電部分。介電層介於上介電部分與下介電部分之間，且材料異於上介電部分與下介電部分。第一導電插塞僅穿過上介電部分、介電層與下介電部分，以物性且電性接觸第一導電結構。第二導電插塞穿過上介電部分、介電層與下介電部分，以物性且電性接觸第二導電結構。

【0006】 爲了對本發明之上述及其他方面有更佳的瞭解，下文特舉較佳實施例，並配合所附圖式，作詳細說明如下：

【圖式簡單說明】

【0007】 第1A圖至第1H圖繪示根據實施例之半導體結構的製造方法。

第2圖繪示根據一比較例之半導體結構。

【實施方式】

【0008】 第1A圖至第1H圖繪示根據實施例之半導體結構的製造方法。

【0009】 請參照第1A圖，提供基板102。基板102可包括矽基板，例如多晶矽，或其他合適的半導體基板。第一導電結構104形成於第一電

路區域106的基板102上。下介電部分108形成於第一導電結構104上。一實施例中，第一導電結構104包括數個不同階層的導電階梯，藉由下介電部分108彼此分開。一實施例中，第一導電結構104的導電階梯包括(未被金屬化的)多晶矽材料。

【0010】 含矽結構110形成於第二電路區域112的基板102上。一實施例中，含矽結構110包括多晶矽。含矽結構110可形成在三維堆疊記憶體之交錯堆疊的導電條紋114與介電條紋116上方，並藉由絕緣材料118分開自導電條紋114與介電條紋116。一實施例中，第一導電結構104的導電階梯與第二電路區域112的導電條紋114可配置在相同的階層，含矽結構110可配置高過第一導電結構104。

【0011】 形成第一蝕刻停止層120，以覆蓋第一電路區域106中的下介電部分108與第二電路區域112中含矽結構110上的絕緣材料118。形成介電材料在第一蝕刻停止層120上，以在第一電路區域106中形成上介電部分122。一實施例中，可對上述介電材料進行平坦化製程，例如化學機械研磨，其停止在第一蝕刻停止層120。

【0012】 請參照第1B圖，可進行蝕刻步驟，移除部分的上介電部分122(第1A圖)、第一蝕刻停止層120(第1A圖)與絕緣材料118，以露出含矽結構110的上部分，並留下第一電路區域106中的第一蝕刻停止層120以形成位在上介電部分122A下方的介電層124。

【0013】 請參照第1C圖，可對含矽結構110(第1B圖)露出的上部分進行金屬化程序，以形成材料包括金屬矽化物的上導電部分126。形成的第二導電結構128包括上導電部分126與下導電部分130，其中下導電部分130維持包括如同含矽結構110未被金屬化的多晶矽材

料。第二導電結構128並不限於金屬氧化物半導體(MOS)的閘極結構，也可應用至源極及汲極，或其他接觸結構。

【0014】 請參照第1D圖，可形成介電材料在第一電路區域106與第二電路區域112，以形成下介電部分132覆蓋第二導電結構128，並形成上介電部分122B。形成第二蝕刻停止層134覆蓋第一電路區域106中的上介電部分122B與第二電路區域112中的下介電部分132。

【0015】 請參照第1E圖，形成圖案化的遮罩136覆蓋第二電路區域112中的第二蝕刻停止層134(第1D圖)。進行蝕刻製程，以移除第二蝕刻停止層134在第一電路區域106中未被遮蔽的部分，其中留下的第二蝕刻停止層134形成介電層138。移除圖案化的遮罩136，以形成如第1F圖所示的結構。

【0016】 請參照第1G圖，形成介電材料在第一電路區域106的上介電部分122B(第1F圖)與第二電路區域112的介電層138上，以在第一電路區域106形成上介電部分122C，並在第二電路區域112形成上介電部分140。介電層124的材料異於介電結構142的上介電部分122C與下介電部分108。介電層138的材料異於介電結構144的上介電部分140與下介電部分132。一實施例中，舉例來說，上介電部分122C、140與下介電部分108、132包括氧化物，例如氧化矽。介電層124、138包括氮化物，例如氮化矽。

【0017】 請參照第1H圖，形成第一導電插塞146，僅穿過上介電部分122C、介電層124與下介電部分108，以物性且電性接觸第一導電結構104。形成第二導電插塞148，僅穿過上介電部分140、介電層138與下介電部分132，以物性且電性接觸第二導電結構128的上導電

部分126。一實施例中，舉例來說，第一導電插塞146的深寬比或高度是大於第二導電插塞148。第一導電插塞146可具有高深寬比。

【0018】 第一導電插塞146與第二導電插塞148可利用蝕刻製程形成穿孔150、152，並以導電材料填充穿孔150、152所形成。

【0019】 舉例來說，可利用相同的遮罩(未顯示)，進行第一蝕刻步驟，同時從上介電部分122C與上介電部分140的上表面向下蝕刻，以形成停止在介電層124、138的穿孔。其中相較於介電層124、138，第一蝕刻步驟對於上介電部分122C、140具有較高的蝕刻選擇性(亦即第一蝕刻步驟對上介電部分122C、140的蝕刻速率高於介電層124、138，或者實質上不會蝕刻介電層124、138，相同概念此後不再重複贅述)，因此，雖然上介電部分122C是厚於上介電部分140，第一蝕刻步驟及藉此所形成的穿孔可依期望控制停止在介電層124與介電層138，且穿孔可具期望的不同深寬比、高度。

【0020】 然後，一實施例中，可藉由異於第一蝕刻步驟的第二蝕刻步驟，來移除上述穿孔露出的介電層124、138，以使上述穿孔向下延伸而形成露出下介電部分108、132的穿孔。舉例來說，相較於上介電部分122C、140與下介電部分108、132，第二蝕刻步驟對於介電層124、138可具有較高的蝕刻選擇性，因此，第二蝕刻步驟及藉此所形成的穿孔可依期望控制停止在下介電部分108、132。

【0021】 然後，一實施例中，可藉由異於第二蝕刻步驟的第三蝕刻步驟，來移除上述穿孔露出的下介電部分108、132，以使上述穿孔向下延伸而形成分別露出第一導電結構104與第二導電結構128的穿孔

150與穿孔152。相較於介電層124、138、第一導電結構104與第二導電結構128，第三蝕刻步驟對於下介電部分108、132具有較高的蝕刻選擇性，因此，第三蝕刻步驟及藉此所形成的穿孔150、152可依期望控制停止在第一導電結構104與第二導電結構128。

【0022】 舉例來說，當上介電部分122C、140與下介電部分108、132材料相同時，用以移除上介電部分122C、140的第一蝕刻步驟與用以移除下介電部分108、132的第三蝕刻步驟可使用相同的蝕刻環境，例如相同的蝕刻溶液。

【0023】 其他實施例中，由於介電層124與下介電部分108的厚度近似或實質上等於介電層138與下介電部分132的厚度，因此上述用以移除介電層124、138的第二蝕刻步驟可在移除介電層124、138之後持續進行，以連續移除下介電部分108、132，例如控制蝕刻時間或對材料蝕刻選擇的關係，使得第二蝕刻步驟停止在第一導電結構104與第二導電結構128。

【0024】 半導體結構及其製造方法可根據上述之概念任意變化。以下例舉幾種變化的方式。舉例來說，上介電部分122C、140與下介電部分108、132並不限於氧化物，介電層124、138並不限於氮化物，在其他實施例中，上介電部分122C、140、下介電部分108、132與介電層124、138可根據用以形成穿孔150、152的蝕刻製程參數其蝕刻選擇特性任意改變材料。一些實施例中，可省略導電條紋114，或將導電條紋114的堆疊數目改變成少於第一導電結構104的導電階梯，使得第二導電結構128實質上與第一導電結構104位在相近或相同的階層。其他實施例中，第一導電插塞146可等長

或短於第二導電插塞148。實施例之概念亦可應用至其他類型的裝置，其需要形成數個導電插塞，分別電性且物性接觸不同結構特徵及/或不同階層(高度)的導電結構。

【0025】 第2圖繪示根據一比較例之半導體結構，其與實施例之半導體結構的差異在於，第一導電插塞246依序穿過上介電部分222C、介電層238、中介電部分254、介電層224、及下介電部分208，以物性且電性接觸第一導電結構104。其中舉例來說，介電結構242的上介電部分222C、中介電部分254及下介電部分208包括氧化物，如氧化矽，介電層224、238包括氮化物，如氮化矽。相較於比較例之半導體結構的必須使用兩個光罩(其中一個光罩用以移除上介電部分222C與介電層238，另一個光罩用以移除中介電部分254、介電層224與下介電部分208)，如第1A圖至第1H圖所示實施例之半導體結構只需使用單一個光罩蝕刻出用以形成第一導電插塞146與第二導電插塞148的穿孔150、152，且蝕刻製程步驟少、時間短。此外，實施例可使用特徵尺寸(例如非臨界尺寸)大於比較例(例如臨界尺寸)的光罩。因此，實施例之半導體結構的製造成本低，且產出速度高(WPH; wafer per hour)。

【0026】 綜上所述，雖然本發明已以實施例揭露如上，然其並非用以限定本發明。本發明所屬技術領域中具有通常知識者，在不脫離本發明之精神和範圍內，當可作各種之更動與潤飾。因此，本發明之保護範圍當視後附之申請專利範圍所界定者為準。

【符號說明】

【0026】 102：基板

104：第一導電結構

106：第一電路區

108、208：下介電部分

110：含矽結構

112：第二電路區域

114：導電條紋

116：介電條紋

118：絕緣材料

120：第一蝕刻停止層

122、122A、122B、122C、222C：上介電部分

124、224：介電層

126：上導電部分

128：第二導電結構

130：下導電部分

132：下介電部分

134：第二蝕刻停止層

136：圖案化的遮罩

138、238：介電層

140：上介電部分

142、242：介電結構

144：介電結構

146、246：第一導電插塞

148：第二導電插塞

150：穿孔

152：穿孔

254：中介電部分

201533887 專利案號：103106107

申請日：103. 2. 24

201533887

IPC分類：

【發明摘要】

H01L 27/105 2006.01

【中文發明名稱】 半導體結構及其製造方法 H01L 21/28 2006.01

【英文發明名稱】 semiconductor structure and method for manufacturing the same

【中文】

半導體結構及其製造方法。半導體結構包括一基板、一第一導電結構、一第二導電結構、介電結構、介電層、一第一導電插塞、及一第二導電插塞。第一導電結構位於基板上。第二導電結構位於基板上，並具有材料異於第一導電結構的一上導電部分。介電結構包括一上介電部分與一下介電部分。介電層介於上介電部分與下介電部分之間，且材料異於上介電部分與下介電部分。第一導電插塞僅穿過上介電部分、介電層與下介電部分，以物性且電性接觸第一導電結構。第二導電插塞穿過上介電部分、介電層與下介電部分，以物性且電性接觸第二導電結構。

【英文】

A semiconductor structure and a method for manufacturing the same are disclosed. The semiconductor structure includes a substrate, a first conductive structure, a second conductive structure, a dielectric structure, a dielectric layer, a first conductive plug, and a second conductive plug. The first conductive structure is on the substrate. The second conductive structure is on the substrate and has a material different from an upper conductive portion of the first conductive structure. The dielectric structure includes an upper dielectric portion and a lower dielectric portion. The dielectric layer is between the upper dielectric portion and the lower dielectric portion, and has a material different from materials of the upper dielectric portion and the lower dielectric portion. The first conductive plug passes through only the upper dielectric portion, the dielectric layer and the lower dielectric portion to physically and electrically contact with the first conductive structure. The second conductive plug passes through the upper

dielectric portion, the dielectric layer and the lower dielectric portion to physically and electrically contact with the second conductive structure.

【指定代表圖】 第1H圖

【代表圖之符號簡單說明】

104：第一導電結構

106：第一電路區

108：下介電部分

112：第二電路區域

114：導電條紋

122C：上介電部分

124：介電層

126：上導電部分

128：第二導電結構

130：下導電部分

132：下介電部分

138：介電層

140：上介電部分

142：介電結構

144：介電結構

146：第一導電插塞

148：第二導電插塞

150：穿孔

152：穿孔

【特徵化學式】

無

【發明申請專利範圍】

【第1項】 一種半導體結構的製造方法，包括：

形成一第一導電結構於一基板上；

形成一第二導電結構於該基板上，該第二導電結構具有材料異於該第一導電結構的一上導電部分；

形成一介電結構的一下介電部分於該第一導電結構與該第二導電結構上；

形成介電層於該下介電部分上；

形成該介電結構的一上介電部分於該介電層上，該介電層的材料異於該上介電部分與該下介電部分；

形成一第一導電插塞，僅穿過該上介電部分、該介電層與該下介電部分，以物性且電性接觸該第一導電結構；以及

形成一第二導電插塞，穿過該上介電部分、該介電層與該下介電部分，以物性且電性接觸該第二導電結構。

【第2項】 如申請專利範圍第1項所述之半導體結構的製造方法，包括：

形成一含矽結構；

形成一第一蝕刻停止層，覆蓋一第一電路區域中的該下介電部分與一第二電路區域中的該含矽結構上；

移除該第二電路區域中的該第一蝕刻停止層，以露出該含矽結構，並留下該第一電路區域中的該第一蝕刻停止層以形成該介電層；以及

對該含矽結構露出的部分進行金屬化程序，以形成該上導電部分

。

【第3項】 如申請專利範圍第1項所述之半導體結構的製造方法，包括：

形成一第二蝕刻停止層覆蓋該上介電部分；以及

移除一第一電路區域中的該第二蝕刻停止層，並留下一第二電路區域中的該第二蝕刻停止層以形成該介電層。

【第4項】 如申請專利範圍第1項所述之半導體結構的製造方法，其中該第一導電插塞與該第二導電插塞的形成方法包括：

藉由一第一蝕刻步驟來移除部分該上介電部分以形成數個穿孔，該第一蝕刻步驟停止在該介電層；

藉由異於該第一蝕刻步驟的一第二蝕刻步驟，來移除該些穿孔露出的該介電層，以使該些穿孔向下延伸而露出該下介電部分，該第二蝕刻步驟停止於該下介電部分；

藉由異於該第二蝕刻步驟的一第三蝕刻步驟，來移除該些穿孔露出的該下介電部分，以使該些穿孔向下延伸而分別露出該第一導電結構與該第二導電結構；以及

以導電材料填充該些穿孔以形成該第一導電插塞與該第二導電插塞。

【第5項】 如申請專利範圍第4項所述之半導體結構的製造方法，其中，

相較於該介電層，該第一蝕刻步驟對於該上介電部分具有較高的蝕刻選擇性，

相較於該上介電部分與該下介電部分，該第二蝕刻步驟對於該介電層具有較高的蝕刻選擇性，

相較於該介電層，該第三蝕刻步驟對於該下介電部分具有較高的蝕刻選擇性。

【第6項】 如申請專利範圍第4項所述之半導體結構的製造方法，其中用於該

第一導電插塞與該第二導電插塞的該些穿孔是使用相同光罩定義出。

【第7項】 如申請專利範圍第1項所述之半導體結構的製造方法，其中該第一導電插塞與該第二導電插塞的形成方法包括：

藉由一第一蝕刻步驟來移除部分該上介電部分以形成數個穿孔，該第一蝕刻步驟停止在該介電層；

藉由異於該第一蝕刻步驟的一第二蝕刻步驟，來移除該些穿孔露出的該介電層，以使該些穿孔向下延伸而露出該第一導電結構與該第二導電結構，該第二蝕刻步驟停止於該第一導電結構與該第二導電結構；以及

以導電材料填充該些穿孔以形成該第一導電插塞與該第二導電插塞。

【第8項】 一種半導體結構，包括：

一基板；

一第一導電結構，位於該基板上；

一第二導電結構，位於該基板上，並具有材料異於該第一導電結構的一上導電部分；

介電結構，包括一上介電部分與一下介電部分；

介電層，介於該上介電部分與該下介電部分之間，且材料異於該上介電部分與該下介電部分；

一第一導電插塞，僅穿過該上介電部分、該介電層與該下介電部分，以物性且電性接觸該第一導電結構；以及

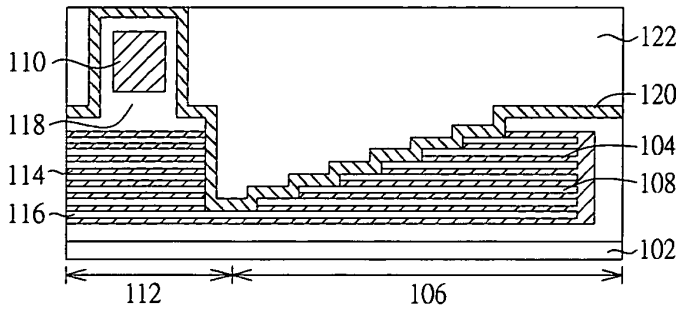
一第二導電插塞，穿過該上介電部分、該介電層與該下介電部分，以物性且電性接觸該第二導電結構。

【第9項】 如申請專利範圍第8項所述之半導體結構，其中該第一導電插塞的

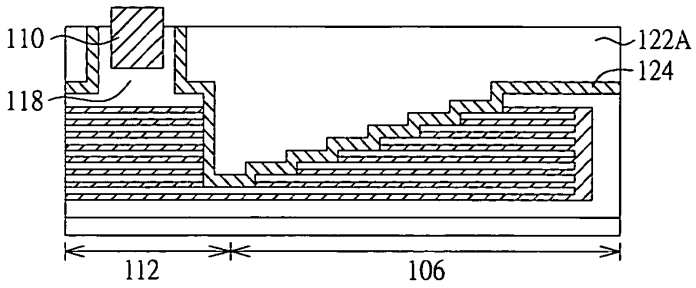
深寬比大於該第二導電插塞的深寬比。

【第10項】 如申請專利範圍第8項所述之半導體結構，其中該第一導電結構包括多晶矽，該第二導電結構的該上導電部分包括金屬矽化物，該介電結構的該上介電部分與該下介電部分包括氧化物，該介電層包括氮化物。

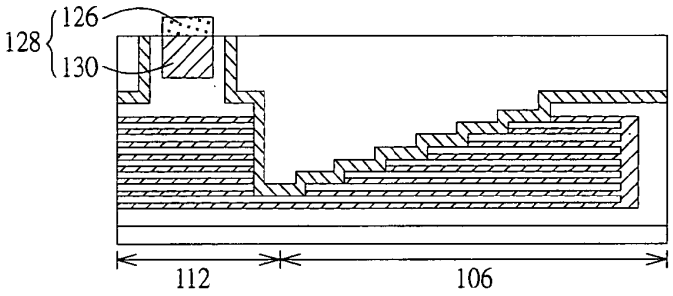
【發明圖式】



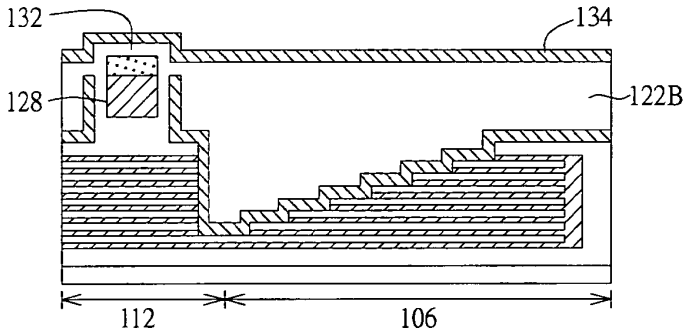
第 1A 圖



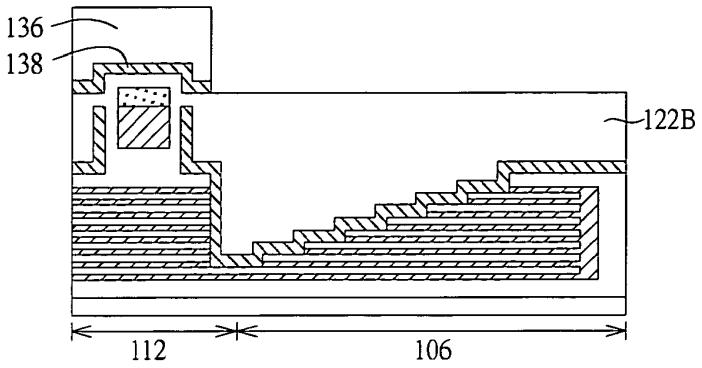
第 1B 圖



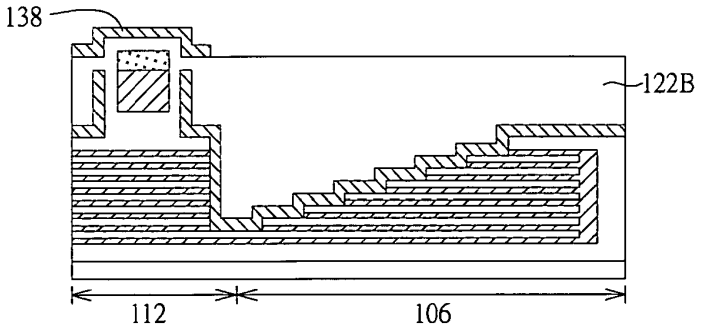
第 1C 圖



第 1D 圖

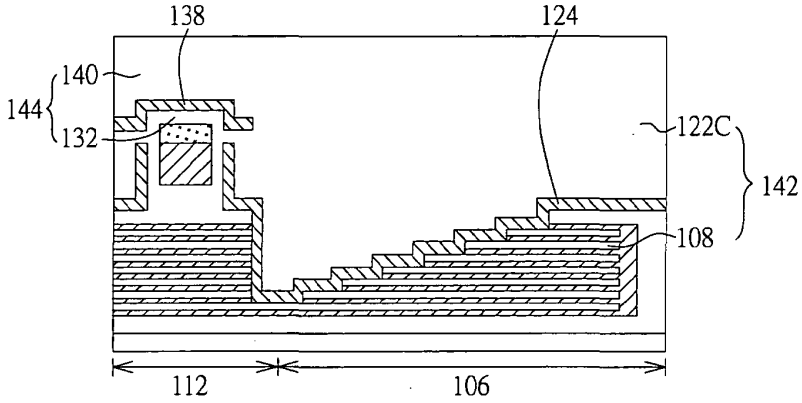


第 1E 圖

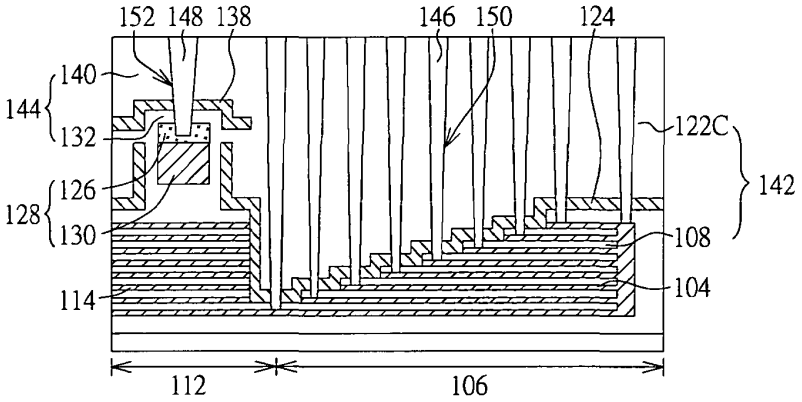


第 1F 圖

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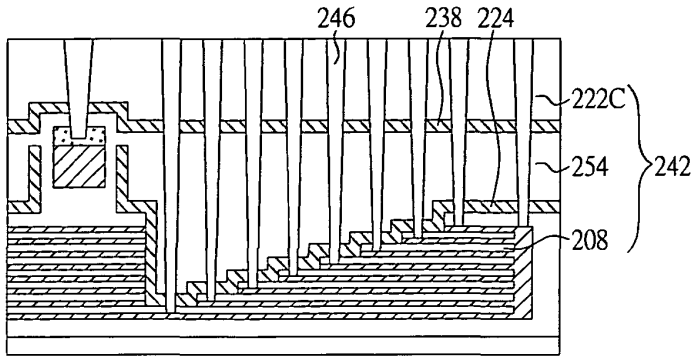


第 1G 圖



第 1H 圖

Micron Ex. 1002, p. 406
Micron v. YMTC
IPR2024-00789



第 2 圖

Micron Ex. 1002, p. 407
Micron v. YMTC
IPR2024-00789

Espacenet

TWI569405B A SEMICONDUCTOR DEVICE AND APPLICATIONS THEREOF

Applicants: MACRONIX INT CO LTD [TW]
Inventors: CHEN SHIH-HUNG [TW]

IPC ***H01L25/04; H01L27/115;***

Application number: TW104111877A
Priority numbers: TW104111877A 2015-04-14
Publication date: 2017-02-01
Filing date: 2015-04-14
Priority date: 2015-04-14
Published as: **TW201637168A;** TWI569405B

Abstract: A SEMICONDUCTOR DEVICE AND APPLICATIONS THEREOF
Roughly described, a memory device has a multilevel stack of conductive layers which are divided laterally into separate word lines, each defining a block of memory cells. Vertically oriented pillars each include series-connected memory cells at cross-points between the pillars and the conductive layers. String select lines run above the conductive layers, each intersection of a pillar and an string select line defining a respective select gate of the pillar. Bit lines run above the SSLs. Ground select lines run below the conductive layers, each intersection of a pillar and a ground select line defining a respective ground select gate of the pillar. The ground select lines are divided laterally such that the number of ground select lines in each block is greater than 1 but less than the number of string select lines in the block.

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Micron v. YMTC
IPR2024-00789

I569405

(19)中華民國智慧財產局

(12)發明說明書公告本 **(11)證書號數：TW I569405 B**

(45)公告日： 中華民國 106 (2017) 年 02 月 01 日

(21)申請案號：104111877 (22)申請日： 中華民國 104 (2015) 年 04 月 14 日

(51)Int. Cl.： ***H01L25/04 (2014.01)*** ***H01L27/115 (2006.01)***

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(56)參考文獻：

US 2008/0130360A1 US 2012/0007167A1

US 2014/0140131A1

審查人員：王人毅

申請專利範圍項數：18 項 圖式數：10 共 52 頁

(54)名稱

記憶體裝置及其應用

A SEMICONDUCTOR DEVICE AND APPLICATIONS THEREOF

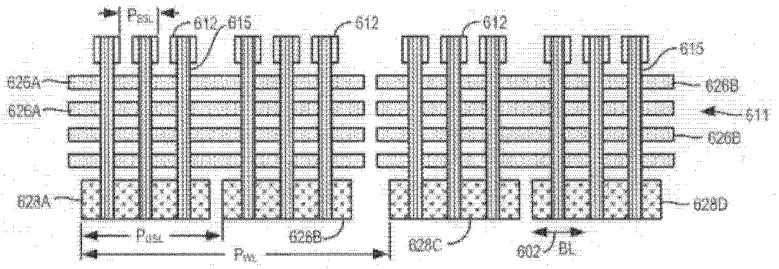
(57)摘要

一種記憶體裝置，具有複數個導電層的多層堆疊結構，其中每一個導電層係分割成彼此分離的字元線，且每一條字元線定義一區塊的記憶胞。垂直走向的複數個柱狀體，每一個柱狀體包括複數個串聯連接的記憶胞，位於柱狀體與導電層的交叉點上。複數條串選擇線位於導電層之上，在這些柱狀體與串選擇線的每一交叉點分別定義出一柱狀體的選擇閘極。複數條位元線位於這些串選擇線之上。複數條接地選擇線位於導電層之下，在柱狀體與接地選擇線的每一交叉點分別定義出一柱狀體接地選擇閘極。接地選擇線係橫向分割以使每一區塊中接地選擇線的數量大於 1，但少於此區塊中串選擇線的數量。

Roughly described, a memory device has a multilevel stack of conductive layers which are divided laterally into separate word lines, each defining a block of memory cells. Vertically oriented pillars each include series-connected memory cells at cross-points between the pillars and the conductive layers. String select lines run above the conductive layers, each intersection of a pillar and an string select line defining a respective select gate of the pillar. Bit lines run above the SSLs. Ground select lines run below the conductive layers, each intersection of a pillar and a ground select line defining a respective ground select gate of the pillar. The ground select lines are divided laterally such that the number of ground select lines in each block is greater than 1 but less than the number of string select lines in the block.

指定代表圖：

Micron Ex. 1002, p. 409
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第6A圖

符號簡單說明：

602・・・位元線方向

611・・・字元線導電層

612・・・串選擇線

615・・・柱狀體

626A、626B・・・字元線

628A、628B、628C、628D・・・接地選擇線

P_{GSL}・・・接地選擇線被隔開的間距

P_{SSL}・・・串選擇線被隔開的間距

P_{WL}・・・字元線被隔開的間距

105年 09月 08日 修正替換頁

發明專利說明書

（本說明書格式、順序，請勿任意更動）

【發明名稱】（中文/英文）

記憶體裝置及其應用/ A SEMICONDUCTOR DEVICE AND APPLICATIONS THEREOF

【相關申請案】

【0001】 本申請案引用(makes reference)下列美國專利申請案，此處通過引用併入(incorporated by reference)的方式，將所有專利全文收載於本說明書之中：

【0002】 2014 年 1 月 17 提出申請，編號 14/157,550，標題為「三維半導體裝置(THREE-DIMENSIONAL SEMICONDUCTOR DEVICE)」的美國申請案。

【0003】 2014 年 12 月 24 提出申請，編號 14/582,848，標題為「高速垂直通道之三維反及閘記憶體的平行四邊形單元胞設計(PARALLELOGRAM CELL DESIGN FOR HIGH SPEED VERTICAL CHANNEL 3D NAND MEMORY)」，發明人為陳士鴻的美國申請案。

【0004】 2014 年 12 月 24 提出申請，編號 14/582,963，標題為「高速垂直通道之三維反及閘記憶體的扭轉陣列設計(TWISTED ARRAY DESIGN FOR HIGH SPEED VERTICAL CHANNEL 3D NAND MEMORY)」，發明人為陳士鴻的美國申請案。

【0005】 2015 年 3 月 3 提出申請，編號 14/637,187，標題為「垂直薄通道閘記憶體(VERTICAL THIN-CHANNEL MEMORY)」，發明人為呂函庭的美國申請案。

【技術領域】

【0006】 本發明是有關於一種高密度記憶體裝置(high density memory devices)。特別是有關於一種內含多層記憶胞平面層(multiple planes of memory cells)並且排列而形成三維(Three-Dimension，3D)陣列的記憶體裝置。

【先前技術】

【0007】 隨著積體電路裝置之臨界尺寸(critical dimensions)縮小至一般記憶胞技術的極限，設計者開始尋求記憶胞的多平面層堆疊技術(techniques for stacking multiple planes of memory cells)，以得到較大儲存容量與較小位元成本(costs per bit)。例如，Lai, *et al.*, "A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory," IEEE Int'l Electron Devices Meeting, 11-13 Dec. 2006；以及 Jung *et al.*, "Three Dimensionally Stacked NAND Flash Memory Technology Using Stacking Single Crystal Si Layers on ILD and TANOS Structure for Beyond 30nm Node," IEEE Int'l Electron Devices Meeting, 11-13 Dec. 2006，內容描述將薄膜電晶體技術(thin film transistor techniques)運用至電荷捕捉式記憶體技術(charge trapping memory technologies)中。而上述期刊內容將通過引用併入的方式，全文收載於本說明書之中。

【0008】 另外，Katsumata, *et al.*, "Pipe-shaped BiCS Flash Memory with 16 Stacked Layers and Multi-Level-Cell Operation for Ultra High Density Storage Devices," 2009 Symposium on VLSI Technology Digest of Technical Papers, 2009，內容描述一種在電荷捕捉式記憶體中提供垂直反及閘記憶胞(vertical NAND cells)的另一結構。該期刊內容亦通過引用併入的方式，全文收載於本說明書之中。Katsumata 所描述的結構包括垂直反及閘閘極(vertical NAND gate)，使用矽-氧-氮-氧-矽(silicon-oxide-nitride-oxide-silicon，SONOS) 電荷捕捉技術，在每一個閘極/垂直通道(vertical channel)相交的位置形成儲存位置(storage site)。此種記憶體結構係建基於排列來作為反及閘閘極之垂直通道的一半導體材料柱(column of semiconductor material)，以及靠近於基板的一下選擇閘極與位於頂部的一上選擇閘極。複數個水平字元線係利用與多個半導體材料柱相交的多個平面字元線層來形成，並在每一層中形成所謂的閘極環繞式記憶胞(gate all-around cell)。

【0009】 第 1 圖係繪示一管狀(pipe-shaped)BiCS 快閃記憶胞(flash cell)柱在字元線層高度(level)的水平剖面圖，例如是 Katsumata 等人的公開內容所述。此一結構包含具有半導體材料中軸心(center core)110 的柱狀體(pillar)15，垂直延伸穿過字元線層的堆疊結構(stack of word line layers)。軸心 110 可以具有通過中央的接縫(seam)111，接縫 111 係由沉積技術產生。介電電荷捕

捉結構，包括例如第一矽氧化物層 112、氮化矽層 113 和第二矽氧化物層 114(可稱為 ONO 結構)，或其他圍繞軸心 110 的多層介電電荷捕捉結構。一環繞式閘極字元線(gate all-around word line)115 係與柱狀體 15 相交。每一層中的柱狀體 15 之平截頭體(frustum)與該層中的閘極環繞式字元線結合，以形成一記憶胞。

【0010】 第 2 圖係繪示一三維半導體裝置的透視圖。其包含複數個字元線導電層 11 的多層堆疊結構，每個字元線導電層 11 係平行基板(未繪示)；複數個柱狀體 15 正交於(oriented orthogonally to)基板，每個柱狀體包括複數個以串聯方式連接的(series-connected)記憶胞，位於柱狀體與導電層的交叉點上；以及複數條串列選擇線(string select lines，SSLs)12，平行於基板並位於導電層 11 之上，每一條串列選擇線與對應的一行(row)柱狀體相交。在每一個柱狀體與串列選擇線的相交處，定義出一個該柱狀體的串列選擇閘極(String Select Gate, SSG)。此一結構也包括接地選擇線(GSL)13(有時亦稱作下方選擇線(lower select lines)，特別是在如第 2 圖中的實施例，其中這些下方選擇線位於柱狀體的下端)，其排列方向平行基板並且於字元線導電層 11 下方形成一個階層。在每一個柱狀體與接地選擇線 13 的相交處，定義出一個接地選擇閘極(Ground Select Gate, GSG)(有時亦稱作該柱狀體的下方選擇閘極(Lower Select Gate, LSG))。一共同源極線(Common Source Line, CSL)10 形成於平行基板且位於接地選擇線下方的一個階層中。此一結構亦包括複數條位於一階層中的平

行位元線 20，此一階層平行基板且位於串列選擇線之上。每一條位元線疊置於一各自行的柱狀體上，且每一個柱狀體位於這些位元線之一者的下方。這些柱狀體 15 可以被建構成如上述第 1 圖所繪示的結構。

【0011】 由於字元線導體層 11 的兩個部分 26A 和 26B 之間係橫向斷開(lateral split)，因此第 2 圖顯示出了兩個橫向的記憶胞區塊。例如，字元線 26A 定義出一個記憶胞區塊，而字元線 26B 定義出第二個記憶胞區塊。相似地，此圖示顯示了兩個相對應的接地選擇線 28A 和 28B。

【0012】 第 3 圖係繪示第 2 圖之部分結構的上視圖。由此二圖可以看出，一條字元線，例如字元線 26A 僅與整體結構中的部分柱狀體相交；每一條字元線 26A 或字元線 26B 定義出一個記憶胞區塊(a block of memory cells)。因此，要從特定記憶胞區塊中讀取資料(data)，控制電路要先活化(activates)一個字元線 26A、26B，以選擇一特定記憶胞區塊以及多層堆疊結構中的一特定階層，並進一步活化一條串列選擇線 12 以選擇一特定行。並同時活化接地選擇閘極。接著一行記憶胞通過位元線 20 被平行(in parallel)讀取至一頁面緩衝器(page buffer) (未繪示)。(此處所使用之「活化」意指施與特定偏壓以啟閉(to give effect to)被連結的記憶胞或開關。這個偏壓可以是高或低，端視記憶體的設計而定)。依照產品的規格和設計，頁面緩衝器可以保存一或兩列資料，在此一情況下，整頁讀取操作(full page read operation)可以包含活

化後續二條或更多條串列選擇線 12。

【0013】 當三維堆疊記憶體結構如預期地大幅增加記憶密度(memory density)同時也衍生了許多製程上的挑戰，因為需要蝕刻非常深的孔以穿過許多階層。這些深孔的寬度必須加寬，且每一深孔中心至中心的橫向距離必須增加，以符合製程裕度(process windows)。隨著製作流程的進步，不僅可以藉由增加堆疊中的字元線平面(word line planes)的數量來增加電容，更可以藉由減少柱狀體間之間距的方式來增加電容。第 4 圖繪示等比例縮小的結構的上視圖，其中區塊中位元線 20 和串列選擇線 12 的數量已經增加。因為，較多數量的位元線 20 代表平行操作(parallel operation)的增加。這不僅降低成本，同時也可以達到增進資料讀/寫速率(read/write data rate)的目的。但另一方面，較多數量的串列選擇線 12 代表更多記憶胞會遭受到由字元線的選擇操作所引起的通過電壓干擾(Vpass disturb)。單元記憶胞電容(unit cell capacitance)也會隨著串列選擇線 12 數量的增加而增加，因而導致電力消耗增加並減緩裝置的操作速度。

【0014】 藉由增加堆疊中字元線導電層 11 的數量以增加位元線密度(bit density)，除了層數量增加所衍生可預期的製程挑戰之外，還有其缺點。於第 2 圖中可以看到一個具有階梯狀接觸結構(stepped contact structure)連接至字元線導電層 11 的典型排列方式。為了形成觸點(contacts)22，藉以將導電層 11 連接至上方的金屬內連線(metal interconnects)24，必須製作穿過此結構的深

溝渠(deep trench)。這些觸點 22 也象徵性地由第 4 圖的上視圖所繪示。在典型設計中，一區塊中柱狀體 15 的的行數至少會和觸點 22 以及記憶層的數量一樣多。例如，請參見 Komori, Y., et. al., "Disturbless flash memory due to high boost efficiency on BiCS structure and optimal memory film stack for ultra high density storage device," Electron Devices Meeting, 2008, IEDM 2008, IEEE International , vol., no., pp.1-4, 15-17 (Dec. 2008) at 2, 上述期刊內容將通過引用併入的方式，全文收載於本說明書之中。由於記憶層的增加也促使串列選擇線 12 的數量增加，因而也會導致電力消耗增加並減緩裝置的操作速度。

【0015】 於第 2 圖的傳統排列中，接地選擇線 13 在位元線方向(bit line direction)具有與字元線導電層 11 近乎相同的寬度。換言之，每個區塊只有一個接地選擇線。因此，當活化下方選擇閘極以活化一行記憶胞，此一相同的動作也會活化區塊中下方選擇閘極的其他記憶胞。因此，共用被活化的下方選擇線的未被選擇的柱狀體會連接至源極，如此更進一步加劇了通過電壓干擾的問題。

【0016】 上述併入的 Komori 的期刊以下述方式解決此問題。藉由改變接地選擇線 13(其在第 2 圖中被繪示得較像是平板)的佈線與空間格局使其與串列選擇線 12 的佈線與空間格局相同，藉以使串列選擇線和接地選擇線可以同步打開和關閉。在 Komori 的概念中，接地選擇線 13 具有與位於其上方數層高度之

串列選擇線 12，大致相同的橫向格局和位置。此結構允許控制電路僅活化位於所欲選擇之記憶胞行(desired rows of memory cells)中柱狀體的的上方與下方選擇線，不需要同時活化在此區塊中任何其他記憶胞的下方選擇閘極。然而，Komori 的結構大幅地降低位元線方向的位元密度，因為不僅設計規則需要針對串列選擇線相對於一行柱狀體之間的潛在錯位排列(potential misalignment)來分配餘裕空間(margin)，其也需要分配額外的餘裕空間給接地選擇線，而此舉將使位元線相對於該行柱狀體於相反方向錯位排列。

【0017】 於上述併入引用的 Komori 中，另外提出一個解決通過電壓干擾問題的結構。於 Komori 中，一管狀的位元可變成本(Pipe-shaped Bit Cost Scalable, P-BiCS)快閃記憶體係被提出，其是由彎折成 U 型的管狀反及閘串列所組成，而非由直線型的管狀反及閘串列所組成。兩個相鄰的柱狀體在底部被水平地連接在一起，藉由所謂的管道連接法(pipe-connection)。因此，反及閘串的兩端位於或接近於此結構的頂部而非位於此結構的底部。特別是，串列選擇線和接地選擇線兩者都位於結構的頂部，消除了彌補接地選擇線在結構底部因為線距(line-space)的潛在錯位排列所需的設計規則餘裕空間的需求。然而，因為需要在反及閘串的兩列柱狀體之間形成較深的狹縫以分別地控制位於同一串列且與相同字元線導電層交叉的兩個記憶胞，此舉又會損失一些密度改善的成效。

【0018】 因此，有需要創造出一種可靠的解決方案，在增加立體記憶體結構之位元線密度同時降低其所引發的負面衝擊，以得到較佳的晶片良率、更緊密、效能更強大的電路、裝置或系統。

【發明內容】

【0019】 本發明技術提供一種記憶體裝置，具有平行於基板之複數個導電層的多層堆疊結構，每一個導電層係分割成複數條字元線。複數個柱狀體正交於基板，每一個柱狀體包括複數個以串聯方式連接的記憶胞，位於此柱狀體與這些導電層的交叉點上。複數條串列選擇線平行於基板並位於這些導電層之上，每一條串列選擇線與柱狀體中一各自不同的柱狀體子集(a respective distinct subset of pillars)相交，並在這些柱狀體與串列選擇線的每一交叉點分別定義出一柱狀體串列選擇閘極。複數條平行的位元線，佈置成一層平行基板並位於串列選擇線之上，每一條位元線疊置於一各自不同的柱狀體子集上，且每一個柱狀體位於這些位元線之一者的下方。每一條字元線導電層下方是複數條接地選擇線，平行於基板且位於這些導電層之下，每一條接地選擇線與一各自不同的柱狀體子集相交，並在這些柱狀體與接地選擇線的每一交叉點上分別定義出一柱狀體接地選擇閘極。接地選擇線位於每一條字元線下方的數量大於 1，但少於串列選擇線位於每一條字元線上的數量。此技術允許設計者藉由在不同實施例中改變每一區塊中彼此分離的接地選擇線的數量，來權衡在位元線方向的密度以利於降低通過電壓干擾。

【0020】 前述的發明內容僅係針對本發明的各種面向(aspect)提供基礎的理解。本發明內容並非用以識別本發明之關鍵或必要的元件，也非用以描繪本發明申請專利範圍的輪廓。其目的僅係以簡化的方式展現本發明的概念，以作為後述之詳細實施方式的序幕。本發明的特定面向(aspects)將以申請專利範圍、說明書以及圖式詳述於下。

【圖式簡單說明】

【0021】 本發明將參照所附圖式對具體實施例進行描述，其中：

第 1 圖繪示一行管狀 BiCS 快閃記憶胞的水平剖面圖。

第 2 圖繪示一三維半導體裝置的透視圖。

第 3 圖係繪示第 2 圖之部分結構的上視圖。

第 4 圖係繪示第 2 圖之部分結構的上視圖，尺寸等比例縮小以容納更多位元線和串列選擇線。

第 5A 圖與第 5B 圖(統稱第 5 圖)係繪示第 2 圖之三維記憶體結構的兩種視圖。

第 6A 圖與第 6B 圖(統稱第 6 圖)係繪示併入本發明的特徵之三維記憶體結構的兩種視圖。

第 7A 圖、第 7B 和 7C 圖(統稱第 7 圖)係繪示併入本發明的特徵之另一三維記憶體結構的兩種視圖。

第 8A 圖、第 8B 和 8C 圖(統稱第 8 圖)係繪示併入本發明的特徵之又一三維記憶體結構的兩種視圖。

第 9 圖係繪示第 7 圖之部分結構的另一視圖。

第 10 圖係繪示具有本發明特徵(aspects)的一記憶體區塊的電路圖(electrical view)。

【實施方式】

【0022】 以下說明內容可提供任何該技術領域中具有通常知識者具以使用、製作本發明。該說明內容僅針對特定運用與需求背景提供。技術領域中具有通常知識者可對被揭露之實施例進行潤飾，且此處所揭露的一般原則將可適用於其他實施例與應用，而不會脫離本發明的精神範圍。因此，實施例的提出，僅係用以例示本發明的技術特徵，並非用以限定本發明的申請專利範圍。

【0023】 第 5A 圖與第 5B 圖(統稱第 5 圖)係繪示第 2 圖之傳統三維記憶體結構的兩種視圖。第 5A 圖係在第 2 圖沿著剖面線 A-A'的剖面圖，且第 5B 圖係繪示第 5A 圖左半邊結構的上視圖。剖面線 A-A'亦顯示於第 5B 圖中。由此二圖可以看出，此結構包括複數個如第 1 圖所繪示的柱狀體 515。此結構也包括複數條串列選擇線 512(16 條顯示於第 5A 圖中，且其中 8 條出現在第 5B 圖中)。此二圖亦繪示四個字元線導電層 511，平行基板(未繪示)而形成，且位於串列選擇線 512 下方。字元線導電層 511 係橫向斷開(split laterally)，因此每一層包含兩個彼此分離的字元線 526A 和 526B(統稱 526)，在位元線方向彼此隔開。字元線 526A 和 526B 係「彼此分離」的意義是指，他們與控制電路的連結允許他們被驅動至不同層級(levels)；他們永遠不會被連接一起。每

一條字元線 526 與每一個柱狀體 515 的相交處定義出一個記憶胞，且由於記憶胞是沿著一個柱狀體 515 加以串聯，該柱狀體定義出一「串(string)」的記憶胞。位元線並未繪示於第 5A 圖與第 5B 圖中，但他們形成在平行於基板且位於串列選擇線 512 上方的一個階層中，且一般係正交於串列選擇線 512。每一條位元線分別疊置於一個柱狀體 515 上，每一個柱狀體 515 位於一條位元線下方。箭頭 502 代表位元線方向。第 5A 圖中亦顯示接地選擇線 528A 和 528B(統稱 528)，分別位於字元線 526A 和 526B 下方。柱狀體 515 亦顯示於第 5A 圖中，在位元線方向上每條串列選擇線 512 對應一個柱狀體。字元線 526A 與接地選擇線 528A 亦顯示於第 5B 圖中，但字元線 526B 與接地選擇線 528B 並未顯示於其中。第 5B 圖亦顯示字元線 526A 與接地選擇線 528A 的階梯狀接觸結構。為了清楚繪示起見，於第 5B 圖中省略柱狀體 515 的繪示。

【0024】 如此處所使用的「橫向」空間維度(“lateral” dimensions)是指平行於基板的空間維度。例如，於第 2 圖中標示為 X 軸和 Y 軸的空間維度即為此處所說的「橫向」空間維度，而標示為 Z 軸的空間維度有時稱作「垂直」空間維度。此外，此處所述的位於其他階層「之上(above)」或「之下(below)」的一特定階層，在不同實施例中，可以藉由一或多層的中間層(intervening layers)而與其他階層分開。如果沒有使用中間層，則此處即使用「正上方(immediately above)」或「正下方(immediately

below)」一詞。相同的解釋方式也適用於描述「疊置(superposing)」於其他階層上、位於其他階層「下方(underlying)」或位於其他階層「之上(over)」的一特定階層。

【0025】 在操作中，可以藉由活化柱狀體 515 的串列選擇閘極與接地選擇閘極來選擇一記憶胞串列，藉此將此記憶胞串列的一末端連接至一位元線(未繪示)，且將此記憶胞串列的另一末端連接該至一共同源極線 CSL(未繪示)。藉由提供一適當的訊號給與柱狀體 515 交叉的串列選擇線 512 來活化串列選擇閘極，且藉由提供一適當的訊號給接地選擇線 528 來活化接地選擇閘極。儘管以「接地(ground)」選擇閘極和「接地」選擇線命名，但理應理解的是，在不同實施例中，共同源極線可以具有除了接地以外的電位。

【0026】 如第 5 圖所繪示，為了滿足製程裕度，在位元線方向上的每一對串列選擇線之間需要有一定的距離(spacing)。在位元線方向上橫向的每一對接地選擇線 528 之間也需要一定的距離，且在串列選擇線 512 的邊緣和字元線 526 的邊緣之間也需要餘裕空間。這兩個方面的考量增加了兩條串列選擇線 512 之間，橫跨在兩字元線 526 間之斷開處的間距。因此，可以看出，在位元線方向上用來隔開串列選擇線 512 的間距(pitch)P_{SSL} 小於(於第 5 圖中二者的比值大於 8 倍)在位元線方向上用來隔開接地選擇線 528 被的間距 P_{GSL}。且在位元線方向上用來隔開字元線 526 的間距 P_{WL} 與在位元線方向上用來隔開接地選擇線 528 的間距 P_{GSL} 相

同。需要注意的是，橫跨於同一條接地選擇線 528 之寬度(在位元線方向)上的間距 P_{SSL} 是不變的，但橫跨於一條以上接地選擇線之寬度(在位元線方向)上的間距 P_{SSL} 是可以改變的。為了討論的目的，位於一給定寬度範圍內的間距 P_{SSL} 被認定為是在此寬度範圍內的最小間距。相同的規則在此也適用於間距 P_{GSL} 與 P_{WL}。

【0027】 此外，於一些實施例中，兩條以上的字元線係橫向地相互交叉(interdigitated)。參見，例如 2015 年 3 月 3 提出申請，編號 14/637,187，標題為「垂直薄通道閘記憶體(VERTICAL THIN-CHANNEL MEMORY)」，發明人為呂函庭的美國申請案，該專利內容係通過引用併入的方式，全文收載於本說明書之中。此申請案描述一種結構安排，其中導電層橫向斷開為彼此分離的偶數與奇數字元線，且在位元線方向上彼此相互交叉。於此結構安排之中，每一條字元線(偶數或奇數)的「寬度範圍」，在此處，被認定是在位元線方向上跨過整條字元線的距離，這包括其他字元線所佔據之部分的距離。於此實施例中每一條字元線(偶數或奇數)的「間距」P_{WL} 在此處被認為是字元線的寬度加上該字元線至下一個出現之相同型態的字元線(偶數或奇數)的近邊(near edge)的距離。相同的規則在此也適用於間距 P_{SSL} 與 P_{GSL}。

【0028】 以另一種方式觀看第 5 圖的結構，可以看出覆蓋在一條接地選擇線 528 上面的串列選擇線的數量 N_{SSL} 大於 1(於第 5 圖中是 8)，且在一條字元線下方的接地選擇線 528 的數量 N_{GSL}(每個區塊中接地選擇線的數量)正好是一。

【0029】 再以另一種方式觀看第 5 圖的結構，並考量到典型的記憶體陣列在位元線方向上會包括多於兩個以上的區塊，可以看出覆蓋此陣列寬度(array width)的接地選擇線 528 的總數量 N_{GSL} 與覆蓋此陣列寬度的字元線的數量 N_{WL} 相同，但與覆蓋此陣列寬度的串列選擇線的數量 N_{SSL} 不同(且於第 5 圖中小於 8 倍)。

【0030】 如上所提及的，第 2 圖和第 5 圖的結構安排會遭受通過電壓干擾，因為 8 個接地選擇閘極(繪示於第 5 圖中)共用一個單一共同的接地選擇線 528。因此當活化接地選擇閘極以活化一行柱狀體 515 時，其他七行共用相同接地選擇線 528 的柱狀體將同時有害地被活化，進而將這些柱狀體連接至源極線。

【0031】 第 6A 圖與第 6B 圖(統稱第 6 圖)係繪示併入本發明的特徵之三維記憶體結構的兩種視圖。第 6A 圖是一概要的剖面圖，且第 6B 圖是此相同結構的上視圖。第 6A 圖是沿著第 6B 圖中的剖面線 A-A’ 進行繪示。可以看出此結構包括複數個柱狀體 615，其可以是如第 1 圖所繪示。另一方面，其也可以具有其他剖面特徵。如另一例子，其可以是如上述引用且被併入本說明書的美國專利號 US 14/637187 所描述的結構。此結構也包括 12 條串列選擇線 612。此二圖亦繪示四條字元線導電層 611，平行於基板(未繪示)且位於串列選擇線 612 下方。如同第 5 圖所繪示的結構，字元線導電層 611 也被橫向地分隔，因此每一個字元線導電層 611 包含兩個在位元線方向上彼此分離的字元線 626A 和 626B(統稱 626)。箭頭 602 代表位元線方向。柱狀體 615 亦顯示

於第 6A 圖中，在位元線的方向上每條串列選擇線 612 對應一個柱狀體。為了清楚繪示起見，於第 6B 圖中省略柱狀體 615 的繪示。

【0032】 第 6A 圖亦繪示四條接地選擇線 628A、628B、628C 以及 628D(統稱 628)：接地選擇線 628A 與 628B 位在字元線 626A 下方，且接地選擇線 628C 與 628D 在字元線 626B 下方。因此相較於第 5 圖，每一條接地選擇線 628 已經一分為二。如此雖然某個程度減少了柱狀體在位元線方向的平均密度，但卻是有利的，當其中一條串列選擇線 628 被活化時，只有很少量的記憶胞會遭受到通過電壓干擾。理應理解的是，於不同實施例中，只要每一條接地選擇線位於整數條串列選擇線 612 下方，每個區塊的接地選擇線可以被分裂為任何數量的片段(segments)。接地選擇線越狹窄，柱狀體在位元線方向上的平均密度越低，但遭受通過電壓干擾的柱狀體數量越少。因此，於不同實施例中，藉由改變每個區塊中彼此分離之接地選擇線 628 的數量，設計者可以在降低通過電壓干擾和降低位元線方向之柱狀體密度兩者之間選擇一個折衷的點。而必須理解的是，在一些實施例中，只要至少一條接地選擇線位於至少兩條串列選擇線 612 的下方，不同的接地選擇線 628 在位元線方向上可以具有不同的寬度。

【0033】 如上述關於第 5 圖所解釋，為了滿足製程裕度，在位元線方向上的每一對串列選擇線 612、每一對接地選擇線 628 以及每一對字元線 626 之間都需要有一定的距離。在接地選擇線

段開的兩側以及在字元線段開的兩側也需要餘裕空間。因此，可以看出，如同的 5 圖的結構，在位元線方向上用來隔開兩條串列選擇線 612 的最小間距 P_{SSL} 小於(於第 6 圖中大於 3 倍)在位元線方向上用來隔開兩條接地選擇線 628 的間距 P_{GSL}。但不像第 5 圖，在位元線方向上用來隔開兩條接地選擇線 628 的間距 P_{GSL} 小於(於第 6 圖中大於 2 倍)在位元線方向上用來隔開兩條字元線 626 的間距 P_{WL}。於不同實施例中，在於位元線方向上彼此鄰接的接地選擇線 628 的任何寬度上，接地選擇線的最小間距 P_{GSL} 大於串列選擇線 612 的最小間距 P_{SSL}，但小於字元線 626 的最小間距 P_{WL}。優選的是 $P_{WL} \geq 2*P_{GSL}$，且更優選的是 $P_{WL} > 2*P_{GSL}$。另外，優選的是 $P_{GSL} \geq 2*P_{SSL}$, 且優選的是 $P_{GSL} > 2*P_{SSL}$。

【0034】 如此處所使用的描述方式中，所謂兩個項目彼此「鄰接」，是指如果他們沒有被另一相同型態的項目隔離。例如，兩條線被認為是彼此「鄰接」，如果沒有中間線存在於他們之間，即使兩條線並沒有彼此碰觸。除非有明確要求，否則「鄰接」一詞並不需要二者要直接毗連。

【0035】 以另一種方式觀看第 6 圖的結構，可以看出覆蓋在一條接地選擇線 628 上面的串列選擇線 612 的數量 N_{SSL} 係大於 1(於第 6 圖中是 3)，且優選的是介於 1 和 9 之間。不像第 5 圖的結構，第 6 圖的結構具有一條以上的接地選擇線 628 位於一條字元線下方。特別是，第 6 圖中每個區塊接地選擇線的數量 N_{GSL} 是為 2。於不同實施例中，對每一第 i 條字元線 626 而言，位於

此第 i 條字元線下方之接地選擇線的數量 N_{GSLi}，係介於 1 與疊置於此第 i 條字元線上方之串列選擇線的數量 N_{SSLi} 之間。對於所有第 i 條字元線而言，優選地，位於每一第 i 條字元線下方之接地選擇線 628 的數量 N_{GSLi} 係，且對於所有第 i 條字元線而言，疊置於每一第 i 條字元線上方之串列選擇線 612 的數量 N_{SSLi} 也相同。然而，在所有實施例中上述條件之任一者皆非必要，對於所有第 i 條字元線而言，有可能需要額外的步驟才得以成功地操作一數量 N_{GSLi} 不相同或數量 N_{SSLi} 不相同或兩者皆不相同的實施例。

【0036】 再以另一種方式觀看第 6 圖的結構，並考慮到典型的記憶體陣列在位元線方向上包括有多於兩個以上的區塊，可以看出覆蓋此陣列寬度之接地選擇線的總數量 N_{GSL} 與覆蓋此陣列寬度的串列選擇線的數量 N_{SSL} 以及與覆蓋此陣列寬度的字元線的數量 N_{WL} 二者皆不相同。優選的是 $N_{SSL}>N_{GSL}$，且優選的是 $N_{GSL}>N_{WL}$。

每條串列選擇線多個柱狀體

【0037】 於第 6 圖的實施例中，每一行柱狀體 615 垂直於位元線方向,且每一條串列選擇線 612 與單一行柱狀體相交。事實上可以藉由柱狀體和串列選擇線的排列方式來增加密度，此方式是藉由使每一條串列選擇線多行柱狀體相交。前述所引用已併入本說明書中，於 2014 年 12 月 24 提出申請，編號 14/582,848，標題為「高速垂直通道之三維反及閘記憶體的平行四邊形單元胞設計 (PARALLELOGRAM CELL DESIGN FOR HIGH SPEED

VERTICAL CHANNEL 3D NAND MEMORY)」，發明人為陳士鴻的美國申請案，描述了一種類型的柱狀體排列方式，其大致上描述柱狀體排列在一具有非矩形平行四邊形(non-rectangular parallelogram)的單位格子(unit cell)的規律網格(regular grid)上。這些柱狀體可被排列而定義出複數條平行柱狀體排線(parallel pillar lines)，這些柱狀體排線與這些位元線相交夾銳角(acute angle) θ (θ >0°)，每一條柱狀體排線具有一個以上的柱狀體，所有的柱狀體排線都只和這些串列選擇線中的一條相交。

【0038】 相似地，前述所引用已併入本說明書中，於 2014 年 12 月 24 提出申請，編號 14/582,963，標題為「高速垂直通道之三維反及閘記憶體的扭轉陣列設計(TWISTED ARRAY DESIGN FOR HIGH SPEED VERTICAL CHANNEL 3D NAND MEMORY)」，發明人為陳士鴻的美國申請案，描述了另一種類型的柱狀體排列方式，其大致上描述柱狀體排列在相對於位元線旋轉的一規則網格上。網格可以具有正方形、矩形或菱形的格子單元，且可以相對於位元線旋轉一個 θ 角度，其中 tan(θ)=±X/Y，且其中 X 和 Y 為互質的整數。串列選擇線可以被製備成具有足夠寬，藉以與位於格子單元之一側的兩個柱狀體相交，或與格子單元的所有柱狀體相交，或具有足夠寬以與位於兩個或更多非相鄰之格子單元中的柱狀體相交。

【0039】 平行四邊形排列的柱狀體和扭轉陣列排列的柱狀體允許高密度的位元線，可藉由所增加的平行操作(parallel)，來達

到較高的資料處理速率。其也減少串列選擇線的數量，藉由降低單元記憶胞電容來降低干擾、以及降低電力消耗，並進一步增進資料處理速率。

【0040】 第 7A 圖、第 7B 和 7C 圖(統稱第 7 圖)係繪示修飾第 6 圖所得的結構，其中增加串列選擇線在位元線方向的寬度，且以每條串列選擇線所對應的一平行四邊形柱狀體陣列取代了第 6 圖中每條串列選擇線所對應的單一個柱狀體。第 7A 圖繪示一概要的結構剖面圖，第 7B 圖則繪示此相同結構的上視圖。第 7A 圖係沿著第 7B 圖所示的剖面線 A-A'所擷取的視圖。為了清楚繪示起見，第 7B 圖中只有一個區塊(區塊 1)顯示於第 7A 圖中。由此二圖可以看出，此結構包括 12 條串列選擇線 712，只有其中 6 條顯示於第 7A 圖中。此二圖亦僅繪示四條字元線導電層 711，平行於基板(未繪示)且位於串列選擇線 712 下方。如同在第 5 圖與第 6 圖中的結構，字元線導電層 711 係橫向斷開，而使每一層包含兩個在位元線方向上彼此分離的字元線 726A 和 726B(統稱 726)。只有相對應於字元線 726A 的區塊顯示於第 7A 圖中。第 7C 圖繪示一條串列選擇線 712 的一區域的上視圖，其顯示一個具有五行相鄰柱狀體之平行四邊形柱狀體 715 結構安排的實施例，每一行柱狀體往正交於位元線的方向平移，且相對於相鄰行(immediately adjacent row)之柱狀體平移了 d/5 的距離，其中 d 是柱狀體的最小間距。其結果可以容納 5 倍的位元線 720，因此大幅地增加了平行操作。字元線的間距降低至 p=d/5，且單一的合

併串列選擇線 712 將網格中串列選擇線的數量減少至原來的 4/5，此舉可藉由降低單元記憶胞電容來降低干擾和降低電力消耗，並更進一步增進資料處理速率。最後，因為合併串列選擇線的使用，使得整個柱狀體網格對於串列選擇線際空間(inter-SSLs spacings)的設計準則要求和閘極厚度設計準則(gate thicknesses)在位元線方向上的嚴重性降低。

【0041】 相似地，第 8A 圖、第 8B 和 8C 圖(統稱第 8 圖)係繪示修飾第 6 圖所得的結構，其中增加了串列選擇線在位元線方向的寬度，且每條串列選擇線對應的一柱狀體扭轉陣列取代了第 6 圖中每條串列選擇線所對應的單一個柱狀體。第 8A 圖與第 8B 圖等同於第 7A 圖與第 7B 圖，在此不重複描述。第 8C 圖係繪示一條串列選擇線 712 的一區域的上視圖，其顯示一柱狀體 815 扭轉陣列結構安排的實施例，其中柱狀體的正方形網格已經被旋轉一角度 $\theta=\arctan(3/4)$，其大約為 36.9°。柱狀體於此網格中正交於位元線之橫向空間維度間的距離可以被幾何計算且係等於 0.2d，其中 d 是柱狀體的最小間距。因此位元線可以由一間距 $P_p=0.2d$ 隔開，導致可以被平行讀取的資料位元(data bits)數量增加五倍。此外，單一個串列選擇線 712 覆蓋多行柱狀體 815。使用單一條串列選擇線 712 是可能的，這是因為，由於旋轉角度的關係，先前已經沿著單一個位元線排列相互對準的多個柱狀體，現在被不同的位元線所對準。其結果是，一條串列選擇線 712 和一條位元線 820 的交叉點仍可單獨識別出單一個柱狀體 815。使用第 8C 圖

的網格，帶寬(bandwidth)增加五倍，且功率消耗和應力降低五倍。此外，每個區塊中所需要之分離串列選擇線的數量大幅減少，也表示需要較少的解碼器(decoders)，因而降低成本。

【0042】 如上述關於第 6 圖所解釋，於第 7 圖與第 8 圖之分斷開的串列選擇線佈局(topology)中，串列選擇線 712 在位元線方向被隔開的最小間距 P_{SSL} 小於接地選擇線 728A-728D(統稱為 728)在位元線方向被隔開的間距 P_{GSL}。但不像第 5 圖，接地選擇線 728 在位元線方向被隔開的間距 P_{GSL} 小於字元線 726 在位元線方向被隔開的間距 P_{WL}。此外，於第 7 圖與第 8 圖中，柱狀體在位元線方向被隔開的間距 P_P 小於串列選擇線 712 在位元線方向被隔開的間距 P_{SSL}。因此在不同的實施例中，在沿著位元線方向彼此鄰接之任何寬度的接地選擇線 728 上方，不僅接地選擇線 728 的最小間距 P_{GSL} 大於串列選擇線 712 的最小間距 P_{SSL}，且也小於字元線 726 的最小間距 P_{WL}，但在位元線方向用來隔開柱狀體的最小間距 P_P 仍小於在位元線方向用來隔開串列選擇線 712 的間距 P_{SSL}。

【0043】 以另一種方式觀看第 7 圖與第 8 圖的結構，再次如上述關於第 6 圖所解釋，於第 7 圖與第 8 圖中斷開之串列選擇線的佈局中，覆蓋在一條接地選擇線 728 上面的串列選擇線 712 的數量 N_{SSL} 大於 1，且接地選擇線 728 位於一條字元線 726 下方的數量 N_{GSLi} 也是大於 1。此外，於第 7 圖與第 8 圖中，在位元線方向之柱狀體位於每一條串列選擇線下方的數量也是大於 1。

【0044】 再以另一種方式觀看第 7 圖與第 8 圖的結構，再次

如上述關於第 6 圖所解釋，於第 7 圖與第 8 圖中斷開之串列選擇線的佈局中，可以看出覆蓋此陣列寬度的接地選擇線的總數量 N_{GSL} 與覆蓋此陣列寬度之串列選擇線的數量 N_{SSL} 以及覆蓋此陣列寬度之字元線的數量 N_{WL} 皆不相同。此外，於第 7 圖與第 8 圖中，在位元線方向之柱狀體的數量 N_p 列也是大於在位元線方向之串列選擇線 712 的數量 N_{SSL}。

【0045】 第 9 圖繪示多個在本發明的實施例中可以展示記憶體陣列內部的周期性圖案。第 9 圖繪示使用第 7C 圖的平行四邊形結構安排來增加位元線密度和降低串列選擇線 912 的密度，但第 8C 圖則是使用扭轉陣列結構安排來被替。第 9 圖的左半部係繪示記憶體陣列的部分結構上視圖。顯示四個區塊的記憶胞：區塊 1 係由字元線 926A 所定義，區塊 2 係由字元線 926B 所定義，區塊 3 係由字元線 926C 所定義以及區塊 4 係由字元線 926D 所定義(統稱 926)。每個區塊包含兩條接地選擇線，位於字元線下方，且在位元線方向彼此隔開。具體來說，區塊 1 包含接地選擇線 928A 和 928B，區塊 2 包含接地選擇線 928C 和 928D，區塊 3 包含接地選擇線 928E 和 928F 以及區塊 4 包含接地選擇線 928G 和 928H(統稱 928)。每一條接地選擇線 928 位於三條串列選擇線 912 下方。第 9 圖的右半部係繪示區域 930 的放大圖，僅顯示區塊 1 和區塊 2 在位元線方向上的一個條帶(strip)。位於平行四邊形的結構安排中的個別柱狀體 915 是可見於此一放大圖中。在位元線方向的間距 P_p 是被標示為柱狀體 915 的最小間距；P_{SSL} 被標示為

串列選擇線 912 的最小間距；P_{GSL} 被標示為接地選擇線 928 的最小間距以及 P_{WL} 被標示為字元線 926 的最小間距。因此整個陣列沿字元線方向柱狀體 915 係以最小週期 P_p 重複出現；串列選擇線 912 係以較大(next smallest)週期 P_{SSL} 重複出現；接地選擇線 928 係以再大一點的週期 P_{GSL} 重複出現；字元線 926 係以最大的週期 P_{WL} 重複出現。優選地字元線 926 不重複出現超過 4096 次。

【0046】 第 10 圖繪示具有本發明之特徵(aspect)的一記憶體區塊的電路圖。如圖所示，記憶體包括 N_p 個以串聯方式連接多個記憶胞 1004 所組成的串列 1015(24 串顯示於第 10 圖中)的。每一記憶胞串列 1015 具有 N_C 個(於第 10 圖中顯示為 4 個)記憶胞 1004。每一個記憶胞 1004 係如第 1 圖所顯示的結構，且電性結構包括一源極一汲極以及一控制閘極。由於在許多電晶體中源極和汲極的電性互換(electrical interchangeability)，這兩個端點在此處有時統稱作「電流通道端點(current path terminals)」。

【0047】 每一記憶胞串列 1015 亦包括一串列選擇閘極 1006 與一接地選擇閘極 1008，以串聯方式連接於此串列的記憶胞 1004 之相對兩末端(opposite ends)，更具體地，每一個串列選擇閘極 1006 與接地選擇閘極 1008 包括一個控制閘極電極和兩個電流通道端點，且電流通端點係以串聯方式連接於串列的記憶胞 1004 的電流通路終端。

【0048】 此一記憶體亦包括 N_C 條(於第 10 圖中顯示為 4 條)彼此分離的字元線 1026A，一條字元線 1026A 相對應一條記憶胞

串列 1015 中的每一個記憶胞 1004。每一條字元線 1026A 連接至區塊中所有記憶胞串列 1005 相對應的記憶胞 1004 之控制閘極電極。

【0049】 記憶體中的串列選擇閘極 1006 被分割成 N_{SSL} 個，且 $N_{SSL}>1$(於第 10 圖中顯示為 6 個)，的包含不同串列選擇閘極 1006 的子集。因此所有子集都是「非空集合(non-null)」，意指每一個子集包括至少一個串列選擇閘極 1006。每一個子集於第 10 圖中包含四個串列選擇閘極 1006。此記憶體也包括 N_{SSL} 條彼此分離的串列選擇線 1012，每一條連接至一相對應串列選擇閘極子集中的所有串列選擇閘極 1006 的控制閘極電極。

【0050】 記憶體中的接地選擇閘極 1008 被分割成不同的數量 N_{GSL}，其中 $N_{GSL}>1$(於第 10 圖中顯示為 2 個)，之接地選擇閘極 1008 的不同非空集合子集。每一個接地選擇閘極 1008 的子集，於第 10 圖中，包含了 12 個記憶胞串列 1015 中的接地選擇閘極。此記憶體也包括 N_{GSL} 個彼此分離的接地選擇線 1028A，每一條連接至一相對應接地選擇閘極子集中之所有接地選擇閘極 1008 的控制閘極電極。

【0051】 於第 10 圖中，在一般情況下，區塊中接地選擇線的數量 N_{GSL} 係大於 1。此外，區塊中串列選擇線的數量 N_{SSL} 不同於(優選的是大於)區塊中接地選擇線的數量 N_{GSL}。優選地，然而，N_{SSL} 不會超過八倍的 N_{GSL}。

【0052】 值得注意的是，第 10 圖代表第 6 圖、第 7 圖以及第

8 圖中所有結構的電路圖。於第 6 圖中，在位元線方向上，每一條串列選擇線 612 僅與一個柱狀體 615 相交，但是在垂直位元線方向(即垂直第 6A 圖的頁面)上與多個柱狀體相交。於第 10 圖中的結構安排是滿足此要求的，因為在一個串列選擇線 1012 子集中的每一個記憶胞串列 1015 被連接至(在圖示的頂部)不同的位元線。相同的位元線連接次序會在所有的串列選擇線 1012 子集中重複。也就是說，如果四條位元線被連接至一個串列選擇線子集中的四條記憶串列 1015 的頂部，且被編號為 BL1、BL2、BL3 與 BL4，則相同的四條位元線 BL1、BL2、BL3 與 BL4 也會連接至每一其他串列選擇線子集中相對應記憶胞串列 1015 的頂部。

【0053】 相反地，於第 7 圖與第 8 圖中，在位元線方向上，每一條串列選擇線 712 與多個柱狀體 715/815 相交。然而，於第 7 圖與第 8 圖中，在垂直位元線方向上柱狀體[與串列選擇線相交的數量]被抵消(offset)，使得在每一條串列選擇線 712 之上，每一條位元線僅與這些圖中可見的一個柱狀體相交。也就是說，一條串列選擇線 712 和一條位元線的相交處仍可獨特識別出一個明確的柱狀體 715/815。因此，在第 7 圖或第 8 圖中，五個與其中一條串列選擇線線 712 相交的柱狀體會將其頂部連接至五條不同的位元線，且這些相同的位元線會重複用於每一條串列選擇線 712。於第 10 圖中，這種結構安排是滿足此要求的，因為，同樣地，每一個記憶體串 1015 於一個串列選擇線 1012 子集中，會將其頂部連接至不同的位元線，且位元線的相同連接次序會在所有

串列選擇線 1012 的子集中重複出現。

【0054】 理應注意的是，第 10 圖的電路圖也代表一個混和結構(hybrid structure)，例如在位元線方向上，每一條串列選擇線 712 僅與 715/815 這兩個柱狀體相交。在此情況下，於每一個串列選擇線 1012 子集中的記憶胞串列 1015 代表示兩柱狀體 715/815，每一條相交兩列柱狀體 715/815，其中柱狀體在垂直位元線方向上彼此抵消。因此同樣地，所有四個柱狀體以其頂部連接至不同的四條位元線。此混合結構也藉由下述特徵適當的表現於第 10 圖中，其中每一個記憶胞串列 1015 於一個串列選擇線 1012 子集中以其頂部連接至不同的位元線，且位元線的相同連接次序在所有串列選擇線 1012 的子集中重複。

【0055】 還要注意的是，一個典型的記憶體裝置具有多個如第 10 圖所繪示的記憶胞區塊，每一個區塊係由連接至單一條字元線 1026A 的記憶胞 1004 控制閘極電極的集合所定義。每一個區塊典型的具有相同的 N_{SSL}/N_{GSL} 比例，但在所有實施例中，此要求並非必要。

【0056】 本文所用的給定值(given value)係「響應(responsive)」一個先前值(predecessor value)，是指如果此先前值影響了給定值。如果有中間製程裝置、步驟或時段，給定值仍會「響應」先前值。如果此中間製程、裝置或步驟與一個以上的值結合，中間製程、裝置或步驟的輸出信號被認為是「響應」每一個輸入值。如果給定值等於先前值，這僅僅是一個退化情況

(degenerate case)，其中該給定值仍然被認為是「響應」該先前值。給定值對另一值的「依賴程度(dependency)」也可作類似的定義。

【0057】 本文所用的某一資訊項目(an item of information)的「識別(identification)」，並不需要該資訊項目的直接說明(direct specification)。資訊可以藉由通過間接的一個或多層(one or more layers of indirection)簡單地參照一實體資訊(actual information)進而在某一個領域中被「識別(identified)」，或者通過識別一或多個不同的資訊項目而被識別，其中這些不同的資訊項目整體加總起來足以確定資訊的實體項目(actual item of information)。此外，本文所用的術語「指出（indicate）」意思等於「辨別（identify）」。

【0058】 本文揭露了個別獨立的技術特徵或二個或多個該些獨立技術特徵的組合。在某個程度上，該技術領域具有通常知識者可以基於本說明書的整體說明，按照一般知識來實施該些個別獨立的技術特徵與技術特徵的組合。無論該些個別獨立的技術特徵與技術特徵的組合是否解決了本文所述的問題，且不會限制本發明的申請專利範圍。本案所揭露的實施例可以包含該些個別獨立的技術特徵與技術特徵的組合。基於前述理由，本發明所屬技術領域中具有通常知識者，在不脫離本發明之精神和範圍內，當可作各種之更動與潤飾。

【0059】 本發明前述的較佳實施例已經被提供用於解釋和描述的目的。其並非意指窮盡的或限定本發明公開至精確的形式。明顯地，對於本領域業者是顯而易見的，當可作許多潤飾與更

動。例如，儘管在本文的實施例中係使用垂直通道的電荷儲存記憶胞來進行描述，柱狀體與其他型態之記憶胞仍可以利用本發明的各方面技術特徵，而不必實現本文所述的所有優點。特別是，但不限於，各種變化類型、建議或本文有關技術背景之段落中任何和所有通過引用併入方式被納入本說明書的內容，都被納入本發明說明書的實施例之中。另外，各種變化類形、建議或本文有關技術背景之段落中任何和所有通過引用併入方式被納入本說明書的內容，也都被認為已被本案的其他實施例所教示。本文所描述的實施例僅係被選擇來對本發明的原理和其實際應用作最好的解釋，進而使本領域中具有通常知識者能夠理解本發明的各種實施例和各種適合於達到預期特定用途的修改與潤飾。因此，本發明之保護範圍當視後附之申請專利範圍所界定者為準。

【符號說明】

【0060】

10：基板

11、511、611、711：導電層

12、512、612、712、912、1012：串列選擇線

13、28(28A、28B)、528(528A、528B)、628(628A、628B、628C、628D)、728(728A-728D)、928(928A、928B、928C、928D、928E、928F、928G、928H)、1028A：接地選擇線

15、515、615、715、815、915：柱狀體

20、720、820、920、BL_1...BL_n：位元線

22：觸點

24：金屬內連線

26(26A、26B)、526(526A、526B)、626(626A、626B)、726(726A、726B)、926(926A、926B、926C、926D)、1026A：字元線

110：核心

111：接縫

112：第一氧化矽層

113、ONO：氮化矽層

114：第二氧化矽層

115：閘極環繞式字元線

502、602：位元線方向

930：區域

1015：記憶體串

P_{GSL}：接地選擇線被隔開的間距

P_{SSL}：串列選擇線被隔開的間距

P_{WL}：字元線被隔開的間距

X、Y：橫向空間維度

Z：垂直空間維度

105年 09月 08日 修正替換頁

發明摘要

公告本

※ 申請案號：104111877

※ 申請日：104.4.14　　※IPC 分類：H01L 25/04 (2014.01)
H01L 27/115 (2006.01)

【發明名稱】(中文/英文)

記憶體裝置及其應用/ A SEMICONDUCTOR DEVICE AND APPLICATIONS THEREOF

【中文】

一種記憶體裝置，具有複數個導電層的多層堆疊結構，其中每一個導電層係分割成彼此分離的字元線，且每一條字元線定義一區塊的記憶胞。垂直走向的複數個柱狀體，每一個柱狀體包括複數個串聯連接的記憶胞，位於柱狀體與導電層的交叉點上。複數條串選擇線位於導電層之上，在這些柱狀體與串選擇線的每一交叉點分別定義出一柱狀體的選擇閘極。複數條位元線位於這些串選擇線之上。複數條接地選擇線位於導電層之下，在柱狀體與接地選擇線的每一交叉點分別定義出一柱狀體接地選擇閘極。接地選擇線係橫向分割以使每一區塊中接地選擇線的數量大於 1，但少於此區塊中串選擇線的數量。

【英文】

Roughly described, a memory device has a multilevel stack of conductive layers which are divided laterally into separate word lines, each defining a block of memory cells. Vertically oriented pillars each include series-connected memory cells at cross-points

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between the pillars and the conductive layers. String select lines run above the conductive layers, each intersection of a pillar and an string select line defining a respective select gate of the pillar. Bit lines run above the SSLs. Ground select lines run below the conductive layers, each intersection of a pillar and a ground select line defining a respective ground select gate of the pillar. The ground select lines are divided laterally such that the number of ground select lines in each block is greater than 1 but less than the number of string select lines in the block.

【代表圖】

【本案指定代表圖】：第 6A 圖。

【本代表圖之符號簡單說明】：

602：位元線方向

611：字元線導電層

612：串選擇線

615：柱狀體

626A、626B：字元線

628A、628B、628C、628D：接地選擇線

P_{GSL}：接地選擇線被隔開的間距

P_{SSL}：串選擇線被隔開的間距

P_{WL}：字元線被隔開的間距

【本案若有化學式時，請揭示最能顯示發明特徵的化學式】：無。

105年 09月 08日 修正替換頁

申請專利範圍

1. 一種記憶體裝置位於一基板上，包括:

一多層堆疊，具有複數個導電層，每一該些導電層分割成相鄰的複數條字元線；

複數個柱狀體，正交於該些導電層，每一該些柱狀體包括以串聯方式連接的複數個記憶胞，該些記憶胞係位於該些柱狀體與該些字元線的複數個交叉點上；

相鄰的複數條串列選擇線，位於該些導電層之上，每一該些串列選擇線與該些柱狀體中各自不同的一第一柱狀體子集(a respective distinct subset of pillars)相交，並在該些柱狀體與該些串列選擇線的每一交叉點上分別定義出該柱狀體的一串列選擇閘極；

平行的複數條位元線，位於該些串列選擇線之上，每一該些位元線疊置於各自不同的一第二柱狀體子集上，且每一該些柱狀體位於該些位元線之一者的下方；以及

相鄰的複數條接地選擇線，位於該些導電層之下，每一該些接地選擇線與該些柱狀體中各自不同的一第三柱狀體子集相交，並在該些柱狀體與該些接地選擇線的每一交叉點上分別定義出該柱狀體的一接地選擇閘極；

其中在垂直該些串列選擇線的一空間維度上，相鄰的該些接地選擇線的一最小間距 P_{GSL} 係大於相鄰的該些

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串列選擇線的一最小間距 P_{SSL}，但小於相鄰的該些字元線的一最小間距 P_{WL}。

2. 如申請專利範圍第 1 項所述之記憶體裝置，其中相鄰的該些字元線的該最小間距 P_{WL} 係至少為相鄰的該些接地選擇線的該最小間距 P_{GSL} 的兩倍。

3. 如申請專利範圍第 1 項所述之記憶體裝置，其中相鄰的該些接地選擇線的該最小間距 P_{GSL} 係至少為相鄰的該些串列選擇線的該最小間距 P_{SSL} 的兩倍。

4. 一種記憶體裝置位於一基板上，包括:

一多層堆疊，具有複數個導電層，每一該些導電層係橫向分割成具有至少一字元線的一字元線組；

複數個柱狀體，正交於該些導電層，每一該些柱狀體包括以串聯方式連接的複數個記憶胞，該些記憶胞係位於該些柱狀體與該些導電層之間的複數個交叉點上；

複數條串列選擇線，位於該些導電層之上，每一該些串列選擇線與該些柱狀體中各自不同的一第一柱狀體子集相交，並在該些柱狀體與該些串列選擇線的每一交叉點分別定義出一柱狀體串列選擇閘極，數量為 N_{SSL} 之該些串列選擇線係疊置於該字元線組中的一第一順位字元線

上；

平行的複數條位元線，位於該些串列選擇線之上，每一該些位元線疊置於各自不同的一第二柱狀體子集上，且每一該些柱狀體位於該些位元線之一者的下方；以及

複數條接地選擇線，位於該些導電層之下，每一該些接地選擇線與該些柱狀體中各自不同的一第三柱狀體子集相交，並在該些柱狀體與該些接地選擇線的每一交叉點分別定義出一柱狀體接地選擇閘極，數量為 N_{GSL} 之該些接地選擇線係位於該第一順位字元線下方；

其中該些接地選擇線位於該第一順位字元線下方的數量 N_{GSL} 係介於 1 與該些串列選擇線疊置於該第一順位字元線上的數量 N_{SSL} 之間。

5. 如申請專利範圍第 4 項所述之記憶體裝置，其中：

該字元線組包括包含該第一順位字元線的複數條字元線，

其中該些字元線中的每一第 i 條字元線係分別被數量為 N_{SSLi} 之該些串列選擇線所疊置，且分別疊置於數量為 N_{GSLi} 之該些接地選擇線上，

且其中對於該些字元線中的每一第 i 條字元線而言，該些接地選擇線位於該第 i 條字元線下方的數量 N_{GSLi} 係介於 1 與該些串列選擇線疊置於該第 i 條字元線上的數

量 N_{SSLi} 之間。

6. 如申請專利範圍第 5 項所述之記憶體裝置，其中該些接地選擇線位於每一該些字元線下方的數量 N_{GSLi} 係與所有該些第 i 條字元線的數量相同，且該些串列選擇線疊置於每一該些字元線上的數量 N_{SSLi} 係與所有該些第 i 條字元線的數量相同。

7. 如申請專利範圍第 4 項所述之記憶體裝置，其中該些串列選擇線疊置於該第一順位字元線上的數量 N_{SSLi} 係不超過該些接地選擇線位於該第一順位字元線下方的數量 N_{GSLi} 的 8 倍。

8. 一種記憶體裝置位於一基板上，包括:

一多層堆疊，具有複數個導電層，每一該些導電層係橫向分割成包含數量 $N_{WL} \geq 1$ 之複數條字元線的一字元線組，該些字元線在一位元線方向係彼此分離，該字元線組在該位元線方向定義出一陣列寬度；

複數個柱狀體，正交於該些導電層，每一該些柱狀體包括複數個以串聯方式連接的記憶胞，該些記憶胞係位於該些柱狀體與該些導電層的複數個交叉點上；

數量 N_{SSL} 之複數條串列選擇線，位於該些導電層之

上，每一該些串列選擇線與該些柱狀體中各自不同的一第一柱狀體子集相交，並在該些柱狀體與該些串列選擇線的每一交叉點分別定義出一柱狀體串列選擇閘極，該些串列選擇線在該位元線方向係彼此分離，且集體覆蓋該陣列寬度；

平行的複數條位元線，位於該些串列選擇線之上且定義該位元線方向，每一該些位元線疊置於各自不同的一第二柱狀體子集上，且每一該些柱狀體位於該些位元線之一者的下方；以及

數量 N_{GSL} 之複數條接地選擇線，位於該些導電層之下，每一該些接地選擇線與該些柱狀體中各自不同的一第三柱狀體子集相交，並在該些柱狀體與該些接地選擇線的每一交叉點分別定義出一柱狀體接地選擇閘極，該些接地選擇線在該位元線方向係彼此分離，且集體覆蓋該陣列寬度；

其中該些接地選擇線覆蓋該陣列寬度的數量 N_{GSL} 係不同於該些串列選擇線覆蓋該陣列寬度的數量 N_{SSL} 與該些字元線覆蓋該陣列寬度的數量 N_{WL}。

9. 如申請專利範圍第 8 項所述之記憶體裝置，其中該些串列選擇線覆蓋該陣列寬度的數量 N_{SSL} 係大於該些接地選擇線覆蓋該陣列寬度的數量 N_{GSL}。

10. 如申請專利範圍第 8 項所述之記憶體裝置，其中該些接地選擇線覆蓋該陣列寬度的數量 N_{GSL} 係大於該些字元線覆蓋該陣列寬度的數量 N_{WL}。

11. 如申請專利範圍第 8 項所述之記憶體裝置，其中該些柱狀體係排列成垂直該位元線方向彼此分離且數量為 N_p 的柱狀體行(row)，並覆蓋該陣列寬度，

且其中該些柱狀體行的數量 N_p 列係不同於該些接地選擇線覆蓋該陣列寬度的數量 N_{GSL}、該些串列選擇線覆蓋該陣列寬度的數量 N_{SSL} 以及該些字元線覆蓋該陣列寬度的數量 N_{WL}。

12. 如申請專利範圍第 11 項所述之記憶體裝置，其中該些柱狀體行覆蓋該陣列寬度的數量 N_p 列係大於該些串列選擇線覆蓋該陣列寬度的數量 N_{SSL}。

13. 如申請專利範圍第 12 項所述之記憶體裝置，其中該些串列選擇線覆蓋該陣列寬度的數量 N_{SSL} 係大於該些接地選擇線覆蓋該陣列寬度的數量 N_{GSL}。

14. 一種記憶體裝置，包括:

由以串聯方式連接之複數個記憶胞所組成，且數量為 N_P 的複數個第一串列，每一該些第一串列具有相同數量 N_C >1 之該些記憶胞，且每一該些第一串列進一步具有一第一串列選擇閘極與一第一接地選擇閘極，以串聯方式連接於每一該些第一串列之相對兩末端，每一該些記憶胞、該第一串列選擇閘極與該第一接地選擇閘極分別具有一控制閘極電極；

彼此分離的複數條第一字元線，該些第一字元線之第 i 條字元線中的每一者係連接至該些第一串列中之一相對應的一第 i 個記憶胞的該控制閘極電極；

數量為 N_{SSL} 且彼此分離的複數條第一串列選擇線，該些第一串列選擇線之第 j 條串列選擇線中的每一者，係連接至在含有不同該些第一串列選擇閘極的一相對應第 j 非空集合子集(non-null subset)中的所有該些第一串列選擇閘極的該些控制閘極電極；以及

數量為 N_{GSL} 且彼此分離的複數條第一接地選擇線，該些第一接地選擇線中第 k 條接地選擇線的每一者係連接至在含有不同該些第一接地選擇閘極的一相對應第 k 非空集合子集中的所有該些第一接地選擇閘極的該些控制閘極電極；

其中該些第一串列選擇線之數量 N_{SSL} 係不同於該些第一接地選擇線之數量 N_{GSL}。

15. 如申請專利範圍第 14 項所述之記憶體裝置，其中該些第一串列選擇線之該數量 N_{SSL} 係大於該些第一接地選擇線之數量 N_{GSL}。

16. 如申請專利範圍第 15 項所述之記憶體裝置，其中該些第一串列選擇線之數量 N_{SSL} 係少於該些第一接地選擇線之數量 N_{GSL} 的 9 倍。

17. 如申請專利範圍第 14 項所述之記憶體裝置，更包括：

由以串聯方式連接之複數個記憶胞所組成，且數量為 N_{P2} 的複數個第二串列，每一該些第二串列具有數量為 N_C 的該些記憶胞，且每一該些第二串列進一步具有一第二串列選擇閘極與一第二接地選擇閘極，以串聯的方式連接於每一該些第二串列之相對兩末端，在該些第二串列中的每一該些記憶胞、每一該第二串列選擇閘極與每一該第二接地選擇閘極分別具有一控制閘極電極；

彼此分離的複數條第二字元線，每一該些第二字元線係連接至在該些第二串列中的該些記憶胞之相對應一者的該控制閘極電極，該些第二字元線係與該些第一字元線分離；

數量為 N_{SSL2} 且彼此分離之複數條第二串列選擇線，

每一該些第二串列選擇線係連接至在含有不同第二串列選擇閘極的一相對應非空集合子集中的所有該些第二串列選擇閘極的該些控制閘極電極；以及

數量 N_{GSL2} 之複數條隔開的第二接地選擇線，每一該些第二接地選擇線係連接至在含有不同第二接地選擇閘極的一相對應非空集合子集中的所有該些第二接地選擇閘極的該些控制閘極電極；

其中該些第二串列選擇線之數量 N_{SSL2} 係不同於該些第二接地選擇線之該第二數量 N_{GSL2}。

18. 如申請專利範圍第 17 項所述之記憶體裝置，其中數量 N_{SSL2} = 數量 N_{SSL} 且數量 N_{GSL2} =數量 N_{GSL}。

between the pillars and the conductive layers. String select lines run above the conductive layers, each intersection of a pillar and an string select line defining a respective select gate of the pillar. Bit lines run above the SSLs. Ground select lines run below the conductive layers, each intersection of a pillar and a ground select line defining a respective ground select gate of the pillar. The ground select lines are divided laterally such that the number of ground select lines in each block is greater than 1 but less than the number of string select lines in the block.

【代表圖】

【本案指定代表圖】：第 6A 圖。

【本代表圖之符號簡單說明】：

602：位元線方向

611：字元線導電層

612：串選擇線

615：柱狀體

626A、626B：字元線

628A、628B、628C、628D：接地選擇線

P_{GSL}：接地選擇線被隔開的間距

P_{SSL}：串選擇線被隔開的間距

P_{WL}：字元線被隔開的間距

【本案若有化學式時，請揭示最能顯示發明特徵的化學式】：無。

Electronic Acknowledgement Receipt

EFS ID:	37888734
Application Number:	16402202
International Application Number:	
Confirmation Number:	7288
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Wenyu Hua
Customer Number:	153988
Filer:	Zhiwei Zou/Anna O'Connor
Filer Authorized By:	Zhiwei Zou
Attorney Docket Number:	10018-01-0045-US
Receipt Date:	29-NOV-2019
Filing Date:	02-MAY-2019
Time Stamp:	12:21:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	10018-01-0045-US_IDS2_SB082.pdf	612167 4a955ec7a6bcf4a176d67918c0435e6b2972df96	no	4

Warnings:

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IPR2024-00789

Information:					
2	Foreign Reference	TW201834207_Bibl.pdf	8140147 dd2e11cb9e04fe2229b9c04943a1594e02ce79c4	no	56
Warnings:					
Information:					
3	Foreign Reference	Part1_TW201539724_Bibl.pdf	12343973 e6d6a4d6347a0645c04256225b308d194f748289	no	61
Warnings:					
Information:					
4	Foreign Reference	Part2_TW201539724.pdf	12371400 4c9c770dc14a1e1d3cc1dac876153448f213531c	no	60
Warnings:					
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5	Foreign Reference	TW201533887_Bibl.pdf	3427542 82ea40f9d5bf75ac8a110a784787aa46db5610e0	no	24
Warnings:					
Information:					
6	Foreign Reference	TWI569405_Bibl.pdf	8260354 501ab5a93846fab62853deb821c25e08b3b88497	no	45
Warnings:					
Information:					
			Total Files Size (in bytes):	45155583	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/402,202	05/02/2019	Wenyu Hua	10018-01-0045-US	7288

153988 7590 05/21/2020

Bayes PLLC
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EXAMINER	
GHEYAS, SYED I	

ART UNIT	PAPER NUMBER
2812	

NOTIFICATION DATE	DELIVERY MODE
05/21/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@dockettrak.com
eofficeaction@appcoll.com
uspto@bayes.law

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IPR2024-00789

Office Action Summary	Application No. 16/402,202	Applicant(s) Hua et al.	
	Examiner SYED I GHEYAS	Art Unit 2812	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 05/02/2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☐ Claim(s) _____ is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☑ Claim(s) 1-20 are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

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Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Election/Restriction

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-14, drawn to a three-dimensional (3D) memory device, classified in class H01L27/11565.

II. Claims 15-20, drawn to a method for forming a three-dimensional (3D) memory device, classified in class H01L21/76802.

1. The inventions are distinct each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process wherein the memory stack comprising interleaved conductive layers and dielectric layers could be formed by replacing the sacrificial layers in the staircase structure with the conductive layers through the dummy channel holes instead of through the dummy source holes.

2. Restriction for examination purposes as indicated is proper because all the inventions listed in this action are independent or distinct for the reasons given above and there would be a

serious search and/or examination burden if restriction were not required because one or more of the following reasons apply:

- the inventions have acquired a separate status in the art in view of their different classification
- the inventions have acquired a separate status in the art due to their recognized divergent subject matter
- the inventions require a different field of search (e.g., searching different classes/subclasses or electronic resources, or employing different search strategies or search queries).

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) **and (ii) identification of the claims encompassing the elected invention**.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103 or pre-AIA 35 U.S.C. 103(a) of the other invention.

3. The examiner has required restriction between product or apparatus claims and process claims. Where applicant elects claims directed to the product/apparatus, and all product/apparatus claims are subsequently found allowable, withdrawn process claims that include all the limitations of the allowable product/apparatus claims should be considered for rejoinder. All claims directed to a nonelected process invention must include all the limitations of an allowable product/apparatus claim for that process invention to be rejoined.

In the event of rejoinder, the requirement for restriction between the product/apparatus claims and the rejoined process claims will be withdrawn, and the rejoined process claims will be fully examined for patentability in accordance with 37 CFR 1.104. Thus, to be allowable, the rejoined claims must meet all criteria for patentability including the requirements of 35 U.S.C. 101, 102, 103 and 112. Until all claims to the elected product/apparatus are found allowable, an otherwise proper restriction requirement between product/apparatus claims and process claims may be maintained. Withdrawn process claims that are not commensurate in scope with an allowable product/apparatus claim will not be rejoined. See MPEP § 821.04. Additionally, in order for rejoinder to occur, applicant is advised that the process claims should be amended during prosecution to require the limitations of the product/apparatus claims. **Failure to do so may result in no rejoinder.** Further, note that the prohibition against double patenting rejections of 35 U.S.C. 121 does not apply where the restriction requirement is withdrawn by the examiner before the patent issues. See MPEP § 804.01.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SYED I GHEYAS whose telephone number is (571)272-0592. The examiner can normally be reached on M-F 8:30 AM - 5:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

05/18/2020
/SYED I GHEYAS/
Primary Examiner, Art Unit 2812

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/402,202	Hua et al.
	Examiner	Art Unit
	SYED I GHEYAS	2812

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant					☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE								
Final	Original	05/12/2020								
	1	÷								
	2	÷								
	3	÷								
	4	÷								
	5	÷								
	6	÷								
	7	÷								
	8	÷								
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	19	÷								
	20	÷								

Micron Ex. 1002, p. 462
Micron v. YMTC
IPR2024-00789

Electronic Acknowledgement Receipt

EFS ID:	39515708
Application Number:	16402202
International Application Number:	
Confirmation Number:	7288
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Wenyu Hua
Customer Number:	153988
Filer:	Zhiwei Zou/Anna O'Connor
Filer Authorized By:	Zhiwei Zou
Attorney Docket Number:	10018-01-0045-US
Receipt Date:	22-MAY-2020
Filing Date:	02-MAY-2019
Time Stamp:	13:32:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Response to Election / Restriction Filed	2018-00434-YMTC-US_ResponseRR_05-21-20.pdf	36191 f96c2b8dce9bf02271eae4599f0f0da100821d73	no	2
Warnings:					

Information:	
Total Files Size (in bytes):	36191

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor:	Wenyu Hua	Art Unit	2812
Serial No.	16/402,202	Examiner	Syed I. Gheyas
Filed	May 2, 2019	Conf. No.	7288
Title	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME		

U.S. Patent and Trademark Office
Customer Window, **Mail Stop Amendment**
Randolph Building
401 Dulany Street
Alexandria, VA 22314

RESPONSE TO RESTRICTION REQUIREMENT OF MAY 21, 2020

Please consider and allow the claims of the present application in view of the election presented in the remarks that follow.

Remarks begin on page 2 of this paper.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 60-2227.

REMARKS

The Office Action presented a restriction between the following inventions:

Group I: claims 1-14 drawn, according to the Office Action, to a three-dimensional (3D) memory device, classified in H01L27/11565; and

Group II: claims 15-20 drawn, according to the Office Action, to a method for forming a 3D memory device, classified in H01L21/76802.

In response to the restriction requirement, Applicant respectfully elects **Group I**, **claims 1-14**, without traverse, and without prejudice to the presentation of the claims of Group II in later applications.

Conclusion

All the stated grounds of restriction have been properly accommodated. Applicant therefore respectfully requests that the Examiner consider and allow the elected claims. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Response is respectfully requested.

Respectfully submitted,
BAYES PLLC

/Zhiwei Zou/_____

Zhiwei Zou
Attorney for Applicant
Registration No. 66,041

Date: May 22, 2020___
1765 Greensboro Station Place, Suite 900
McLean, VA 22102
(703) 995-9887

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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/402,202	05/02/2019	Wenyu Hua	10018-01-0045-US	7288

153988 7590 06/11/2020

Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

EXAMINER
GHEYAS, SYED I

ART UNIT	PAPER NUMBER
2812	

NOTIFICATION DATE	DELIVERY MODE
06/11/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@dockettrak.com
eofficeaction@appcoll.com
uspto@bayes.law

Micron Ex. 1002, p. 467
Micron v. YMTC
IPR2024-00789

Office Action Summary	Application No. 16/402,202	Applicant(s) Hua et al.	
	Examiner SYED I GHEYAS	Art Unit 2812	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 05/22/2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) 15-20 is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-14 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 05/02/2019 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 11/08/2019, 11/15/2019 & 11/29/2019.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

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Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on November 8, 2019, November 15, 2019 & November 29, 2019 were in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Election/Restrictions

Applicant's election without traverse of Invention I (claims 1-14) in the reply filed on 05/22/2020 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

1. Claims 1-13 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by **Jeong et al. (Pub. No.: US 2016/0293622 A1).**

Regarding Claim 1, Jeong et al. discloses

a three-dimensional (3D) memory device, comprising:

a substrate (Par 0055, Fig. 3 - substrate 100);

a memory stack comprising interleaved conductive layers and dielectric layers on the substrate (Par. 0057-0058, Fig. 3 - interleaved conductive layers 130, 135 & 138 and dielectric layers 110);

a staircase structure on one side of the memory stack (Par. 0057-0058, Fig. 3 – staircase structure (stepped structure) shown in region R2);

a staircase contact in the staircase structure (Par. 0068, Figs. 1-3 – staircase contact (cell contact plug) 150c shown in region R2); and

a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact (Par. 0062-0065 & 0082-0085, Figs. 1-3 – dummy pillars DP1 & DP2 shown in region R2 could be considered as the dummy source; dummy pillars of this prior art, like the dummy source of the instant application, function as a mechanical support for conductive layers).

Regarding Claim 2, Jeong et al., as applied to claim 1, discloses

the 3D memory device, wherein the plurality of dummy source structures are located adjacent to the staircase contact (Figs. 1-2 – dummy source structures (dummy pillars) DP1 and DP2; staircase contact 150c).

Regarding Claim 3, Jeong et al., as applied to claim 1, discloses

the 3D memory device, wherein at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact (Figs. 1-2 – dummy source structures

(dummy pillars) DP1 and DP2; staircase contact 150c; 4 dummy source structures are shown to be of nominally equal lateral distances to the staircase contact).

Regarding Claim 4, Jeong et al., as applied to claim 1, discloses

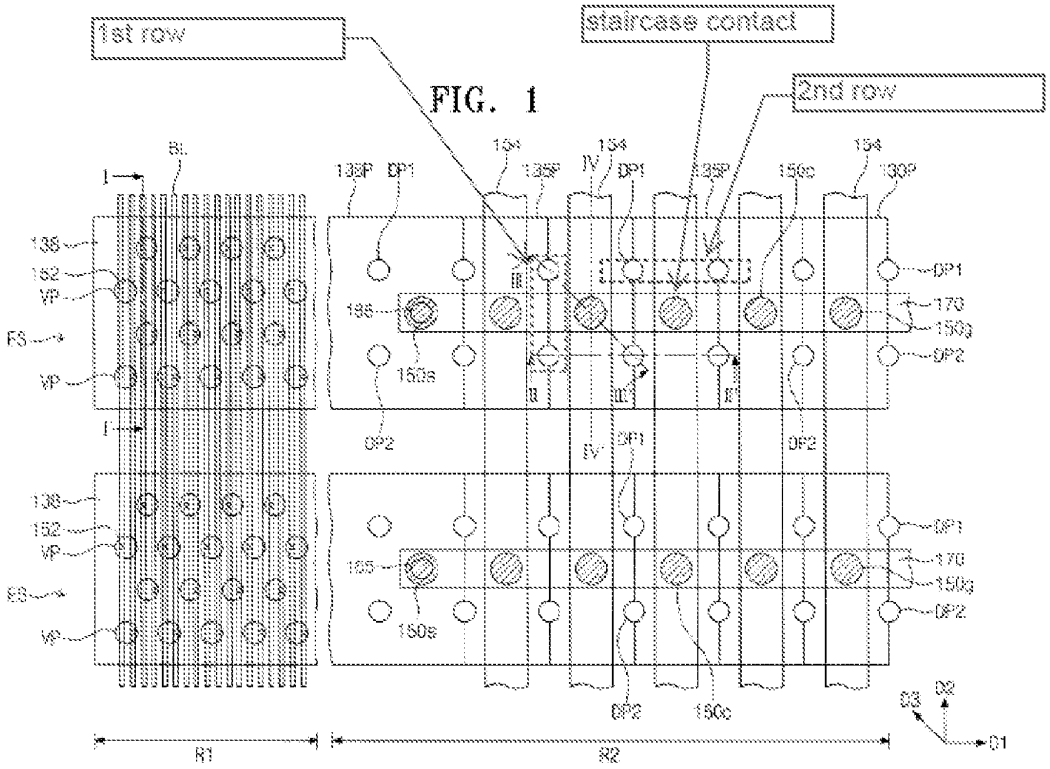
the 3D memory device, wherein the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact (Figs. 1-2 – dummy source structures (dummy pillars) DP1 and DP2; staircase contact 150c; 4 dummy source structures are shown to be of nominally equal lateral distances to the staircase contact).

Regarding Claim 5, Jeong et al., as applied to claim 1, discloses

the 3D memory device, wherein in a plan view, at least two of the plurality of dummy source structures are arranged in a first row that extends along a first lateral direction (Figs. 1-2 – dummy source structures (dummy pillars) DP1 and DP2; staircase contact 150c; 2 of the plurality of dummy source structures one DP1 and one DP2 are shown to be arranged in a first row towards direction D2).

Regarding Claim 6, Jeong et al., as applied to claim 5, discloses

the 3D memory device, wherein in the plan view, at least two other dummy source structures are arranged in a second row that extends along a second lateral direction perpendicular to the first lateral direction (see annotated Fig. 1 below).



Regarding Claim 7, Jeong et al., as applied to claim 5, discloses

the 3D memory device, further comprising a plurality of dummy channel structures surrounding the staircase contact, each dummy channel structure extending vertically through the staircase structure (see annotated Fig. 1 below – two of the dummy pillars on the right and two of the dummy pillars on the left in the D2 direction could be considered as dummy channels at least under the BRI and these dummy pillars at least partially surround the staircase contact).

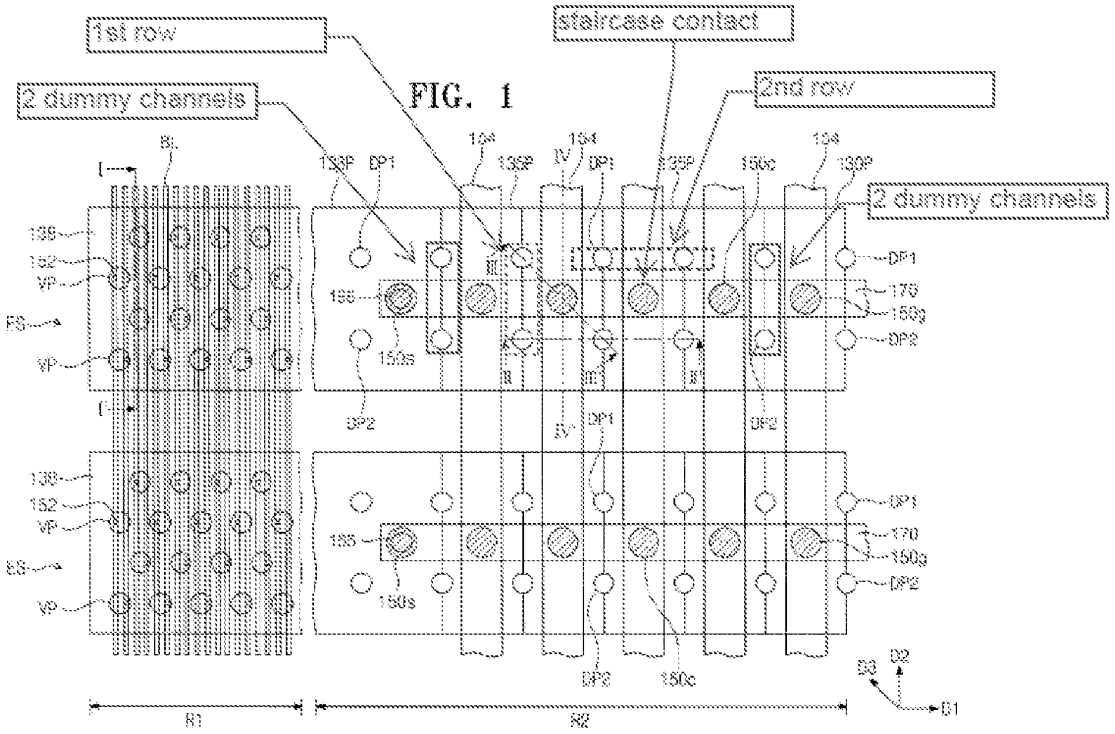


FIG. 1

Regarding Claim 8, Jeong et al. discloses

a three-dimensional (3D) memory device, comprising:

a substrate (Par 0055, Fig. 3 - substrate 100);

a memory stack comprising interleaved conductive layers and dielectric layers on the substrate (Par. 0057-0058, Fig. 3 - interleaved conductive layers 130, 135 & 138 and dielectric layers 110);

a staircase structure on one side of the memory stack (Par. 0057-0058, Fig. 3 – staircase structure (stepped structure) shown in region R2);

an array of dummy channel structures each extending vertically through the staircase structure (Par. 0062-0065 & 0082-0085; see annotated Fig. 1 below – some of the dummy pillars

DP1 and DP2 could be considered as the dummy channel structures); and

a plurality of dummy source structures each extending vertically through the staircase stack, wherein a subset of the dummy channel structures is surrounded by the plurality of dummy source structures (Par. 0062-0065 & 0082-0085, Figs. 1-3 and annotated Fig. – some of the dummy pillars DP1 & DP2 shown in region R2 could be considered as the dummy source; dummy pillars of this prior art, like the dummy source of the instant application, function as a mechanical support; it is important to note that under BRI we are considering some of the dummy pillars DP1 and DP2 as dummy channels and others as the dummy sources; a subset of the dummy channel structures is at least partially surrounded by the plurality of dummy source structures).

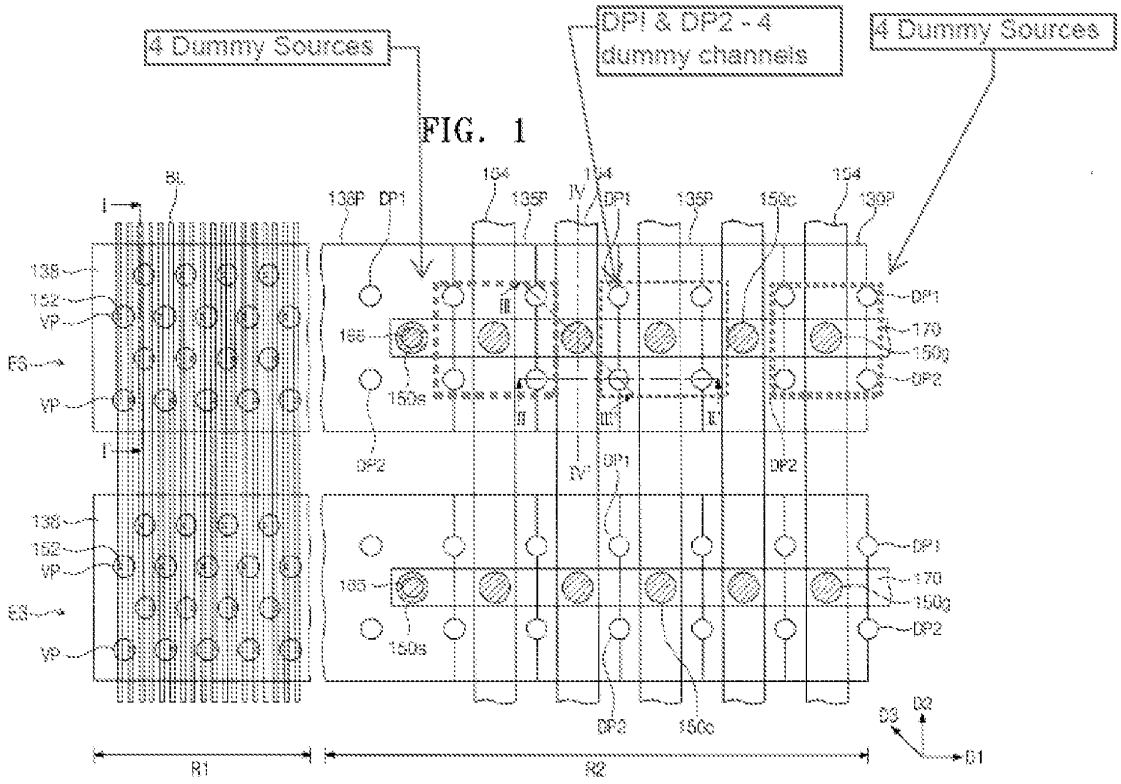


FIG. 1

Regarding Claim 9, Jeong et al., as applied to claim 8, discloses

the 3D memory device, wherein at least one dummy channel structure is surrounded by at least four dummy source structures (see annotated Fig. 1).

Regarding Claim 10, Jeong et al., as applied to claim 8, discloses

the 3D memory device, wherein at least two dummy channel structures are surrounded by at least six dummy source structures (see annotated Fig. 1 – under BRI, at least two dummy channel structure could be considered to be at least partially surrounded by eight dummy source structures).

Regarding Claim 11, Jeong et al., as applied to claim 8, discloses

the 3D memory device, wherein at least four dummy channel structures are surrounded by at least eight dummy source structures (see annotated Fig. 1 – under BRI, at least four dummy channel structure could be considered to be at least partially surrounded by eight dummy source structures).

Regarding Claim 12, Jeong et al., as applied to claim 8, discloses

the 3D memory device, wherein in a plan view, two dummy source structures and two dummy channel structures are aligned along a first row extending in a first lateral direction (see annotated Fig. 1).

Regarding Claim 13, Jeong et al., as applied to claim 12, discloses

the 3D memory device, wherein the two dummy source structures are separated by the two dummy channel structure (see annotated Fig. 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102 of this title, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103 are summarized as follows:

> 1. Determining the scope and contents of the prior art.
> 2. Ascertaining the differences between the prior art and the claims at issue.
> 3. Resolving the level of ordinary skill in the pertinent art.
> 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claim 14 is rejected under 35 U.S.C. 103 as obvious over **Jeong et al. (Pub. No.: US 2016/0293622 A1)**.

<u>Regarding Claim 14,</u> Jeong et al., as applied to claim 12, does not explicitly disclose the 3D memory device, wherein the two dummy source structures are separated by one of the two dummy channel structure.

However, Jeong et al. teaches

the 3D memory device, wherein the two dummy source structures are separated by the two dummy channel structure (see annotated Fig. 1 above; also Jeong et al. teaches that the dummy

pillars are used to give mechanical support to the conductive layers).

Jeong et al. discloses the claimed invention except for the 3D memory device, wherein the two dummy source structures are separated by one of the two dummy channel structure. It would have been obvious to one having ordinary skill in the art at the time the invention was filed to adapt the 3D memory device, wherein the two dummy source structures are separated by one of the two dummy channel structure, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse, 86 USPQ 70 (CCPA 1950).*

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SYED I GHEYAS whose telephone number is (571)272-0592. The examiner can normally be reached on M-F 8:30 AM - 5:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

06/03/2020
/SYED I GHEYAS/
Primary Examiner, Art Unit 2812

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/402,202	Hua et al.
	Examiner	Art Unit
	SYED I GHEYAS	2812

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L27/11582, H01L23/535, H01L29/0847, H01L29/1037	06/03/2020	Syed Gheyas

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
EAST search	06/03/2020	Syed Gheyas
NPL search using Google.com & IP.com	06/03/2020	Syed Gheyas

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**

/SYED I GHEYAS/ Primary Examiner, Art Unit 2812	

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Micron v. YMTC
IPR2024-00789

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	16402202
Filing Date	2019-05-02
First Named Inventor	Wenyu HUA
Art Unit	2811
Examiner Name	GURLEY, LYNNE ANN
Attorney Docket Number	10018-01-0045-US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8822285	B2	2014-09-02	Hwang et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	108962910	CN	A	2018-12-07	SAMSUNG ELECTRONICS CO LTD		
	2	106057813	CN	A	2016-10-26	SAMSUNG ELECTRONICS CO LTD		

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Micron Ex. 1002, p. 480
Micron v. YMTC
IPR2024-00789

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16402202
Filing Date	2019-05-02
First Named Inventor	Wenyu HUA
Art Unit	2811
Examiner Name	GURLEY, LYNNE ANN
Attorney Docket Number	10018-01-0045-US

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	International Search Report issued in corresponding International Application No. PCT/CN2019/076186, mailed October 23, 2019, 4 pages	
	2	Written Opinion of the International Searching Authority issued in corresponding International Application No. PCT/CN2019/076186, mailed October 23, 2019, 5 pages	

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EXAMINER SIGNATURE

Examiner Signature	/SYED I GHEYAS/	Date Considered	05/26/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.I.G/

Micron Ex. 1002, p. 481
Micron v. YMTC
IPR2024-00789

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16402202
	Filing Date	2019-05-02
	First Named Inventor	Wenyu HUA
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	10018-01-0045-US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2019-11-08
Name/Print	Zhiwei Zou	Registration Number	66,041

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Micron Ex. 1002, p. 482
Micron v. YMTC
IPR2024-00789

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

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Micron Ex. 1002, p. 483
Micron v. YMTC
IPR2024-00789

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	16402202
Filing Date	2019-05-02
First Named Inventor	Wenyu HUA
Art Unit	2811
Examiner Name	GURLEY, LYNNE ANN
Attorney Docket Number	10018-01-0045-US

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	109103199	CN	A	2018-12-28	YANGTZE MEMORY TECH CO LTD		

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Micron Ex. 1002, p. 484
Micron v. YMTC
IPR2024-00789

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16402202
	Filing Date	2019-05-02
	First Named Inventor	Wenyu HUA
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	10018-01-0045-US

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If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/SYED I GHEYAS/	Date Considered	05/26/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Micron Ex. 1002, p. 485
Micron v. YMTC
IPR2024-00789

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16402202
	Filing Date	2019-05-02
	First Named Inventor	Wenyu HUA
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	10018-01-0045-US

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2019-11-15
Name/Print	Zhiwei Zou	Registration Number	66,041

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Micron Ex. 1002, p. 486
Micron v. YMTC
IPR2024-00789

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Micron Ex. 1002, p. 487
Micron v. YMTC
IPR2024-00789

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	16402202
Filing Date	2019-05-02
First Named Inventor	Wenyu HUA
Art Unit	2811
Examiner Name	GURLEY, LYNNE ANN
Attorney Docket Number	10018-01-0045-US

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20190043883	A1	2019-02-07	XU et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	201834207	TW	A	2018-09-16	YANGTZE MEMORY TECHNOLOGIES CO LTD		
	2	201539724	TW	A	2015-10-16	TOSHIBA KK		
	3	201533887	TW	A	2015-09-01	MACRONIX INT CO LTD		

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Micron Ex. 1002, p. 488
Micron v. YMTC
IPR2024-00789

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16402202
	Filing Date	2019-05-02
	First Named Inventor	Wenyu HUA
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	10018-01-0045-US

	4	I569405	TW	A	2016-10-16	MACRONIX INT CO LTD		

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
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EXAMINER SIGNATURE

Examiner Signature	/SYED I GHEYAS/	Date Considered	05/26/2020

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.I.G/

Micron Ex. 1002, p. 489
Micron v. YMTC
IPR2024-00789

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	16402202
	Filing Date	2019-05-02
	First Named Inventor	Wenyu HUA
	Art Unit	2811
	Examiner Name	GURLEY, LYNNE ANN
	Attorney Docket Number	10018-01-0045-US

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Signature	/Zhiwei Zou/	Date (YYYY-MM-DD)	2019-11-29
Name/Print	Zhiwei Zou	Registration Number	66,041

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Micron Ex. 1002, p. 490
Micron v. YMTC
IPR2024-00789

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Micron Ex. 1002, p. 491
Micron v. YMTC
IPR2024-00789

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	"16402202"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/26 15:41
S2	9	("8822285" | "20190043883").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/26 15:44
S3	354	(Wenyu near2 Hua).in. (Fandong near2 Liu).in. (Zhiliang near2 Xia).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/26 17:14
S4	1,469	(YANGTZE near2 MEMORY).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/26 17:15
S5	14	S4 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/26 17:16
S6	11,806	(YANGTZE).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/26 17:16
S7	14	S6 and S3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/26 17:17
S8	62,816	((three-dimension$2) or (3D)) near5 (memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/26 17:23
S9	746	S6 and S8	US-PGPUB; USPAT; USOCR;	OR	ON	2020/05/26 17:28

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S10	1,470	(((three-dimension$2) or (3D)) near5 (memory)) and (staircase)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/27 09:48
S11	1,481	(((three-dimension$2) or (3D)) near5 (memory)) and (staircase or stair adj case)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/27 09:49
S12	11,806	(YANGTZE).as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/27 09:50
S13	68	S12 and S11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/27 09:50
S14	104	(((three-dimension$2) or (3D)) near5 (memory)) and (staircase or stair adj case) and @ad<"20100101"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/27 09:51
S15	43	(((three-dimension$2) or (3D)) near5 (memory)) and (staircase or stair adj case) and @ad<"20050101"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/27 09:53
S16	3	(((three-dimension$2) or (3D)) near5 (memory)).ab. and (staircase or stair adj case) and @ad<"20050101"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/27 09:54
S17	10	(((three-dimension$2) or (3D)) near5 (memory)).ab. and (staircase or stair adj case) and @ad<"20100101"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/27 09:55
S18	61	(((three-dimension$2) or (3D)) near5 (memory)).ab. and (staircase or stair adj case) and (interleav$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/27 09:56

S19	332	(((three-dimension$2) or (3D)) near5 (memory)).ab. and (staircase or stair adj case) and (interleav$3 or alternat$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/05/27 09:56
S20	53,524	(H01L27/11582 or H01L23/535 or H01L29/0847 or H01L29/1037).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 08:49
S21	29,263	(H01L29/0847 or H01L29/1037).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 08:50
S22	25,616	(H01L29/0847).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 08:50
S23	12,013	H01L27/11524.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:21
S24	3,922	H01L27/11529.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:22
S26	15,267	(H01L27/11526-11548).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:24
S27	9,886	(H01L27/11526).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:25
S28	2,242	(H01L27/11548).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:25
S29	12,690	(H01L27/11551-11556).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/06/03 14:26

			DERWENT; IBM_TDB			
S30	4,003	(H01L27/11551).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:26
S31	10,148	(H01L27/11556).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:26
S32	14,400	S23 or S24	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:27
S33	4,649	S32 and S29	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:27
S34	1,840	S33 and S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:29
S35	4,724	dummy near2 source	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:29
S36	4,832	(dummy or nonfunctional) near2 source	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:30
S37	5,020	(dummy or nonfunctional or non adj functional) near2 source	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:30
S38	5,060	(dummy or nonfunction$3 or non adj function$3) near2 source	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:31

S39	23	S34 and S38	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:31
S40	2	"20180337192".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 14:54
S41	2	"20160293622".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 15:19
S42	4	"20130161182"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 15:32
S43	4	"20130161821"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 15:33
S44	315	((dummy or nonfunction$3 or non adj function$3) near2 (source)) and ((dummy or nonfunction$3 or non adj function$3) near2 (channel))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 18:13
S45	12,013	H01L27/11524.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 18:21
S46	3,922	H01L27/11529.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 18:21
S47	15,267	(H01L27/11526-11548).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 18:21
S48	12,690	(H01L27/11551-11556).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/06/03 18:21

			DERWENT; IBM_TDB			
S49	14,400	S45 or S46	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 18:21
S50	4,649	S49 and S48	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 18:21
S51	1,840	S50 and S47	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 18:21
S52	10	S51 and S44	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 18:21
S53	14,413	(H01L27/11524 or H01L27/11529).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 12:26
S54	12,702	(H01L27/11551-11556).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 12:36
S55	4,656	S54 and S53	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 12:36
S56	317	((dummy or nonfunction$3 or non adj function$3) near2 (source)) and ((dummy or nonfunction$3 or non adj function$3) near2 (channel))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 12:37
S57	11	S55 and S56	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 12:37

S58	237	S54 and S53 and (stair)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 12:39
S59	507	S54 and S53 and (stair or staircase)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 12:39
S60	507	S54 and S53 and (stair or staircase or stair adj case)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 12:39
S61	507	S54 and S53 and (stair or staircase or stair-case)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 12:40
S62	507	S54 and S53 and (stair or staircase or stair adj case)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 12:40
S63	1,908	S54 and S53 and (stair or staircase or stair adj case or step)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 12:41
S64	10	S63 and S56	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 12:41
S65	85	(NAND) and ((dummy or nonfunction$3 or non adj function$3) near2 (source)) and ((dummy or nonfunction$3 or non adj function$3) near2 (channel))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 14:30
S66	80	S65 NOT S64	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 14:31
S67	4	"20180026047"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2020/06/04 15:10

			DERWENT; IBM_TDB			

EAST Search History (Interference)

<This search history is empty>

6/7/2020 11:38:54 PM
C:\Users\sgheyas\Documents\EAST\Workspaces\16402202-05262020.wsp

Bibliographic Data

Application No: 16/402,202

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☐ No ☐ Met After Allowance

Verified and Acknowledged: /SYED I GHEYAS/ Examiner's Signature | Initials

Title: THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
05/02/2019	257	2812	10018-01-0045-US
RULE			

APPLICANTS

YANGTZE MEMORY TECHNOLOGIES CO., LTD., Wuhan, CHINA

INVENTORS

Wenyu Hua Wuhan, CHINA

Fandong Liu Wuhan, CHINA

Zhiliang Xia Wuhan, CHINA

CONTINUING DATA

This application is a CON of PCT/CN2019/076186 02/26/2019

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

05/16/2019

STATE OR COUNTRY

CHINA

ADDRESS

Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102
UNITED STATES

FILING FEE RECEIVED

$1,720

UNITED STATES PATENT AND TRADEMARK OFFICE

USPTO Automated Interview Request (AIR)

Aug 2 2020

This paper requesting to schedule and/or conduct an interview is appropriate because:

This submission is requested to be accepted as an authorization for this interview to communicate via the internet. Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned concerning scheduling of the interview via video conference, instant messaging, or electronic mail, and to conduct the interview in accordance with office practice including video conferencing.

Name(s):
Peter Flanagan

S-signature:
/Peter Flanagan/

Registration Number:
58178

U.S. Application Number:
16402202

Confirmation Number:
7288

E-mail Address:
peter.flanagan@bayes.law

Phone Number:
+1 7033712110

Proposed Time of Interview:
8-10-2020 2:00 PM ET

Alternative Proposed Time(s) of Interview:
8-11-2020 2:00 PM ET

Alternative Proposed Time(s) of Interview:
8-12-2020 2:00 PM ET

Prefered Interview Type:
Telephonic

I am the applicant or applicant's representative for this application.

Topic for Discussion:
Amendments to the claims to clarify difference from cited references.

Micron Ex. 1002, p. 501
Micron v. YMTC
IPR2024-00789

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/402,202	05/02/2019	Wenyu Hua	10018-01-0045-US	7288

153988 7590 08/14/2020

Bayes PLLC
1765 Greensboro Station Place
Suite 900
McLean, VA 22102

EXAMINER	
GHEYAS, SYED I	

ART UNIT	PAPER NUMBER
2812	

NOTIFICATION DATE	DELIVERY MODE
08/14/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTO@dockettrak.com
eofficeaction@appcoll.com
uspto@bayes.law

Micron Ex. 1002, p. 502
Micron v. YMTC
IPR2024-00789

Applicant-Initiated Interview Summary	**Application No.** 16/402,202	**Applicant(s)** Hua et al.	
	Examiner SYED I GHEYAS	**Art Unit** 2812	**AIA (FITF) Status** Yes

All participants (applicant, applicants representative, PTO personnel):

(1) SYED I. GHEYAS. (3) _____.

(2) PETER FLANAGAN. (4) _____.

Date of Interview: 11 August 2020.

Type: ☑ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☑ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☑Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1.

Identification of prior art discussed: Jeong et al. (Pub. No.: US 2016/0293622 Al).

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

The Applicant's Representative and the Examiner talked about the Non-Final Rejection Office Action mailed on 06/11/2020. The Applicant's Representative also talked about possible amendments. No consensus was reached..

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☑ Attachment

/SYED I GHEYAS/ Primary Examiner, Art Unit 2812	

Micron Ex. 1002, p. 503
Micron v. YMTC
IPR2024-00789

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiners responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicants correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,-
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicants record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiners version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, Interview Record OK on the paper recording the substance of the interview along with the date and the examiners initials.

From: Peter Flanagan
To: Gheyas, Syed
Cc: Peter Flanagan
Subject: Informal Interview Agenda | US Patent Application No. 16/402,202 | 10018-01-0045-US
Date: Friday, August 7, 2020 4:29:36 PM

Hi Examiner Gheyas,

According to my records, I have not yet received your confirmation regarding a telephone interview, possibly as early as 8/10 at 2 pm. If you would like a different time or date, please let me know.

During the interview, I propose to discuss the following:

1. Background discussion of the invention
2. Discussion of "dummy source" and "dummy channel" as contrasted with "dummy pillar" in cited art
3. Discuss possible amendments to clarify distinctions from cited art
4. Any other suggestions the Examiner may have

Best regards,

Peter

Peter Flanagan
Counsel | Patent Attorney
Bayes PLLC | www.bayes.law
1765 Greensboro Station Place, Suite 900 | McLean, VA 22102
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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/402,202	Filing Date 05/02/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	08/18/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/VINCENT S BUTLER/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Wenyu Hua	Confirmation No.: 7288
Applicant: YANGTZE MEMORY TECHNOLOGIES CO. LTD.	Art Unit: 2812
Application No.: 16/402,202	Examiner: GHEYAS, SYED I
Filing Date: May 2, 2019	Atty. Docket: 10018-01-0045-US

Title: **THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME**

Amendment and Reply Under 37 C.F.R. § 1.111

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Office Action dated June 11, 2020, Applicant submits the following Amendments and Remarks.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 5 of this paper.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 60-2227.

Electronic Acknowledgement Receipt

EFS ID:	40315521
Application Number:	16402202
International Application Number:	
Confirmation Number:	7288
Title of Invention:	THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME
First Named Inventor/Applicant Name:	Wenyu Hua
Customer Number:	153988
Filer:	Peter Charles Flanagan/Anna O'Connor
Filer Authorized By:	Peter Charles Flanagan
Attorney Docket Number:	10018-01-0045-US
Receipt Date:	18-AUG-2020
Filing Date:	02-MAY-2019
Time Stamp:	16:34:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2018-00434-YMTC_ResponsetoNFOA6-11-20.pdf	74380 6d352029c1bed6d5f5ebed4cfadeff4d6c5fc821	yes	9

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Arguments/Remarks Made in an Amendment	6	9
	Claims	2	5
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Warnings:			
Information:			
	Total Files Size (in bytes):	74380	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A three-dimensional (3D) memory device, comprising:

a substrate;

a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;

a staircase structure on one side of the memory stack;

a staircase contact in the staircase structure; and

a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact,

wherein each of the dummy source structures comprises a conductive contact.

2. (Original) The 3D memory device of claim 1, wherein the plurality of dummy source structures are located adjacent to the staircase contact.

3. (Original) The 3D memory device of claim 1, wherein at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact.

4. (Original) The 3D memory device of claim 1, wherein the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact.

5. (Original) The 3D memory device of claim 1, wherein in a plan view, at least two of the plurality of dummy source structures are arranged in a first row that extends along a first lateral direction.

6. (Original) The 3D memory device of claim 5, wherein in the plan view, at least two other dummy source structures are arranged in a second row that extends along a second lateral direction perpendicular to the first lateral direction.

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7. (Original) The 3D memory device of claim 5, further comprising a plurality of dummy channel structures surrounding the staircase contact, each dummy channel structure extending vertically through the staircase structure.

8. (Currently Amended) A three-dimensional (3D) memory device, comprising:

a substrate;

a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;

a staircase structure on one side of the memory stack;

an array of dummy channel structures each extending vertically through the staircase structure; and

a plurality of dummy source structures each extending vertically through the staircase stack, wherein a subset of the dummy channel structures is surrounded by the plurality of dummy source structures,

wherein each of the dummy source structures comprises a conductive contact.

9. (Original) The 3D memory device of claim 8, wherein at least one dummy channel structure is surrounded by at least four dummy source structures.

10. (Currently Amended) The 3D memory device of claim 8, wherein at least two dummy channel structures are surrounded by at least six dummy source structures.

11. (Original) The 3D memory device of claim 8, wherein at least four dummy channel structures are surrounded by at least eight dummy source structures.

12. (Original) The 3D memory device of claim 8, wherein in a plan view, two dummy source structures and two dummy channel structures are aligned along a first row extending in a first lateral direction.

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13. (Original) The 3D memory device of claim 12, wherein the two dummy source structures are separated by the two dummy channel structure.

14. (Original) The 3D memory device of claim 12, wherein the two dummy source structures are separated by one of the two dummy channel structure.

15-20. (Cancelled)

21. (New) The 3D memory device of claim 7, wherein the plurality of dummy channel structures are of nominally equal lateral distances to the staircase contact.

22. (New) The 3D memory device of claim 7, wherein in the plan view, the plurality of dummy source structures interleave with the plurality of dummy channel structures.

23. (New) The 3D memory device of claim 7, wherein in the plan view, at least two of the plurality of dummy channel structures are arranged in a third row that extends along a third lateral direction in parallel with the first or the second lateral direction.

24. (New) The 3D memory device of claim 1, comprising first and second staircase contacts, wherein at least one dummy source structure is located between the first and second staircase contacts.

25. (New) The 3D memory device of claim 1, wherein at least two dummy source structures are located between the first and second staircase contacts.

26. (New) The 3D memory device of claim 1, wherein the conductive contact comprises a conductor layer, and wherein the at least one dummy source structure further comprises a spacer surrounding the conductor layer along a sidewall of the conductor layer, the spacer comprising a dielectric material.

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Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendments, claims 1-14 and 21-26 are pending in the application, with claims 1 and 8 being independent claims. Applicant hereby amends claims 1, 8, and 10, adds claims 21-26, and cancels claims 15-20, without prejudice or disclaimer. These changes introduce no new matter, and their entry is respectfully requested. Support for the amendments may be found throughout the application as filed including, for example, FIGs. 1A and 1B, paragraphs [0036], [0038] – [0041], [0057], and [0078]. Applicant reserves the right to file a divisional application directed to the subject matter of claims 15-20.

Throughout the arguments, Applicant reminds the Examiner that the claims are given their broadest reasonable meaning in view of the specification, and any paraphrasing of the claim features is not to be interpreted as reading any features into, or characterizing of, the claims.

Based on the above amendments and the following remarks, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections.

Examiner Interview

An interview was conducted by telephone on August 10, 2020, between the Examiner and Applicant's representative, Peter Flanagan (Reg. No. 58,178). Applicant thanks the Examiner for the courtesies extended to Applicant's representative during the interview. The above amendments to claims 1 and 8 are based on the discussion during the interview, as further explained below.

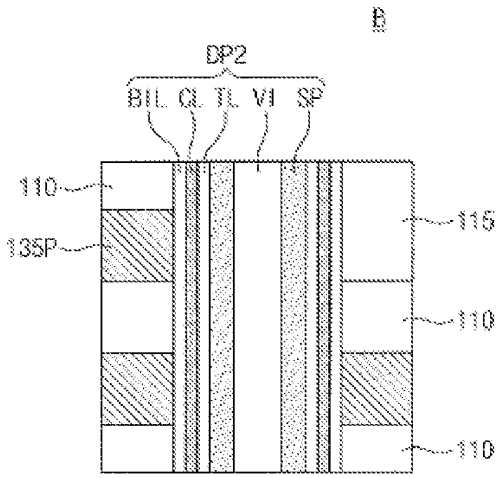
Rejections under 35 U.S.C. § 102

Claims 1-13 were rejected under 35 U.S.C. § 102 as being allegedly anticipated by Jeong (U.S. Patent Application Publication No. 2016/0293622). Applicant respectfully submits that the claims recite subject matter that is neither disclosed nor suggested by the cited references.

For example, amended claim 1 recites, in part, "a plurality of dummy source structures each extending vertically through the staircase structure … wherein each of the dummy source structures comprises a conductive contact." Amended claim 8 recites similar features. These features are not found in Jeong.

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Jeong does not disclose dummy source structures, but simply discloses dummy pillars. The dummy pillars in Jeong are different from the claimed "dummy source structure" in amended independent claims 1 and 8 at least because the dummy pillars do not include conductive contacts. Jeong explains the construction of the dummy pillars in FIGs. 4A, 4B, 4C, and 4D. Taking FIG. 4A as an example (because it is the most elaborate example in Jeong), the dummy pillar (DP2) includes the following:



As shown at left:

BIL = blocking insulating layer

CL = charge storage layer

TL = tunnel insulating layer

VI = vertical insulating pattern

SP = vertical semiconductor pattern

By contrast, FIG. 1D (reproduced below) illustrates an example of a dummy source structure 178, including contact 179 and spacer 177 (see also, FIG. 2L, dummy source structure 178, contact 244, and spacer 244). Nothing in Jeong's pillar is conductive contact, as the pillar consists of insulating layers, a semiconductor pattern, and a charge storage layer. By contrast, as explained at paragraph [0057] of the present application: "In some embodiments, dummy source structure 178 includes a dummy source hole filled with conductive materials as a contact 179. Dummy source structure 178 can further include a spacer 177 made of any suitable dielectric materials (e.g., silicon oxide) between contact 179 and memory stack 160 to electrically separate surrounding conductive layers 106 in memory stack 160 from contact 179. As a result, dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks."

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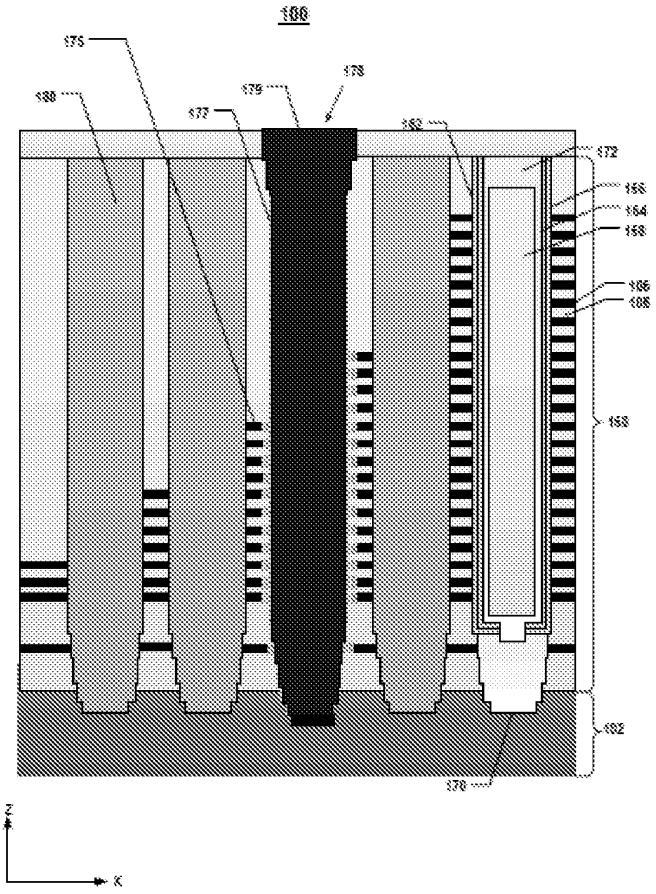


FIG. 1D

It is respectfully submitted that Jeong does not disclose a dummy source structure, and that Jeong's dummy pillar does not include a conductive contact. Accordingly, Jeong does not disclose or suggest at least , "a plurality of dummy source structures each extending vertically through the staircase structure … wherein each of the dummy source structures comprises a conductive contact," as recited in claim 1 or "a plurality of dummy source structures each extending vertically through the staircase stack … wherein each of the dummy source structures comprises a conductive contact," as recited in claim 8. Withdrawal of the rejection of claims 1 and 8 is respectfully requested.

Claims 2-7 and 9-13 depend from and further limit claims 1 and 8. Withdrawal of the rejection of claims 2-7 and 9-13 is respectfully requested in view of their dependency and further limitation.

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Rejections under 35 U.S.C. § 103

Claim 14 was rejected under 35 U.S.C. § 103 as being allegedly unpatentable over Jeong. Claim 14 depends from and further limits claim 12, which depends from and further limits claim 8. The rejection is premised on the rejection of those claims. Withdrawal of the rejection of claim 14 is respectfully requested in view of its dependency and further limitations.

New Claims

New claims 21-26 depend from and further limit claim 1. Claims 21-26 should be allowed over Jeong in view of their dependency and further limitation.

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Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider the presently outstanding rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

BAYES PLLC

/Peter Flanagan/

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Date: August 18, 2020

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