UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00789
U.S. Patent No. 10,861,872
Issue Date: December 8, 2020

Title: THREE-DIMENSIONAL MEMORY DEVICE AND METHOD FOR FORMING THE SAME

DECLARATION OF SANJAY BANERJEE, Ph.D., IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,861,872

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G. Claim 11 123

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I, Sanjay Banerjee, hereby declare as follows:

I. INTRODUCTION

1. My name is Sanjay Banerjee. I have been retained on behalf of Petitioner Micron Technology, Inc. ("Micron") to provide this Declaration concerning technical subject matter relevant to the *inter partes* review petition ("Petition") concerning U.S. Patent No. 10,861,872 (Ex. 1001, the "'872 Patent").

2. In the preparation of this Declaration, I have confined my analysis to the materials and opinions that were available at the time of the preparation of this Declaration. I reserve the right to supplement this Declaration in response to additional evidence that may come to light.

3. If requested, I am prepared to explain (in a deposition or at a trial before the Patent Trial and Appeal Board (the "Board")) the technology disclosed in the Challenged Patents—including the state of the art in the relevant timeframe. Similarly, I am prepared to explain the technology disclosed in the Park (Ex. 1005, U.S. Patent No. 9,859,297) and Tessariol (Ex. 1006, U.S. Patent Application Publ. No. 2019/0081061) references, and in any other prior art references cited herein. This may include, among other things, background information on 3D NAND technology.

4. I am over 18 years of age and competent to testify to the matters addressed in this Declaration.

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II. QUALIFICATIONS

5. I currently serve as the Cockrell Family Regents Chair Professor of Electrical and Computer Engineering and Director of the Microelectronics Research Center at the University of Texas at Austin ("UT"). Prior to this position, I was first an Assistant Professor (September 1987-August 1990) and later an Associate Professor (September 1990-August 1993) at UT, before being named a Professor in September 1993. Prior to starting my academic work at UT, I was a member of the technical staff at Texas Instruments (Corporate R&D) from the time I completed my doctoral studies in 1983 until August 1987. I worked on vertical 3D Dynamic Random Access Memory (DRAM) cells (*see* S. Banerjee and M. Bordelon, "A Model for the Trench Transistor," *IEEE Trans. Elec. Dev.*, 34 (12), 2485-2493, December 1987).

6. In addition to my academic work at UT, I was also the Director of the South West Academy of Nanoelectronics, one of three centers created by the Semiconductor Research Corporation Nanoelectronics Research Initiative in 2006 to research and develop a replacement for conventional metal oxide semiconductor field effect transistors ("MOSFETs") during the entire program.

7. I received my Ph.D. in Electrical Engineering from the University of Illinois in 1983. I also received an M.S. in Electrical Engineering from the

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University of Illinois in 1981. I received a B. Tech. in Electronics from the Indian Institute of Technology at Kharagpur in 1979.

8. As described in my CV (Ex.1004), I have more than 40 years of experience in the field of electrical engineering, including extensive experience in semiconductor development and fabrication including that of 3-Dimensional Dynamic Random Access Memory ("DRAM") cells, MOSFETs, flash memory, and beyond-complementary metal-oxide-semiconductor ("CMOS") transistors. My work in these fields has resulted in thirty-five United States patents related to methods of forming polysilicon and novel transistors, flash memory, and vertical DRAM cells. I have been elected a Fellow of the National Academy of Inventors.

9. Much of my research and experience has related to methods for MOSFET fabrication and design, including deposition of thin films by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), patterning using photolithography and etching using plasma-based Reactive Ion Etching (RIE) which are some of the processing techniques used to make 3D NAND flash. I have worked extensively on polysilicon thin film transistors similar to the ones used in the channel of NAND flash memory cells, high-k and other dielectrics used for charge storage, and for tunneling. A number of the sponsored research grants on which I have been a principal or coinvestigator have related to chemical deposition methods and/or ultra-shallow source/drain junction technology,

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including "Transport in MOSFETs" (Motorola, August 1993-August 1994), "Ultra Shallow Junction Technology" (SEMATECH January 1994-December 1996), and "Vertical Si-Ge-C MOSFETS" (Semiconductor Research Corporation September 2000-August 2003). In addition, I am an author on over forty publications relating to flash memory cells, including vertical 3D memory that can be used in NAND flash (e.g., Sarkar J, Dey S, Shahrjerdi D, Banerjee SK, Vertical Flash memory cell with nanocrystal floating gate for ultradense integration and good retention IEEE ELECTRON DEVICE LETTERS 28 (5): 449-451 MAY 2007.) One of my papers on flash memory was given a Best Paper Award by the SRC.

10. I am a Fellow of the Institute of Electrical and Electronics Engineers ("IEEE"), the American Physical Society ("APS"), and the American Association for the Advancement of Science ("AAAS"). I have served on numerous professional and government committees in the electrical engineering field, including chairing multiple IEEE committees, meetings, and programs, serving on Morgan & Claypool's editorial board, and serving as a member on the International Technology Roadmap for Semiconductors ("ITRS").

11. I have taught courses in Semiconductor Physics, Solid State Electronic Devices, and Microelectronic and VLSI Device Fabrication at UT. In addition, I have delivered many courses to industry on Semiconductor Devices and Memory and Semiconductor Processing. I have taught courses that cover 3D memories, such

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as 3D NAND (Ultra Large Scale Integration Techniques and Solid State Electronic Devices). As a principal investigator, I have been the advisor to over 80 Doctoral and Masters students.

12. I am the co-author of several books and invited book chapters covering the area of electronic and semiconductor devices, including: Dopant Diffusion, Solid State Electronic Devices (three editions), Silicon-germanium Devices, and Novel 3D CMOS. I have authored or co-authored more than 1,000 papers and presentations in the areas of semiconductor devices and electronics development over the course of my career.

13. I have been the recipient of fifty grants to fund my research from a variety of funding agencies including the National Science Foundation ("NSF"), DARPA, the Department of Energy, Semiconductor Research Corporation, the Department of Defense-Multidisciplinary University Research Initiative, and the Office of Naval Research.

14. I have received numerous awards for my work, including the NSF Presidential Young Investigator Award. The NSF Presidential Young Investigator

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Award was [1] a highly competitive honor and grant bestowed annually upon recognized young academic leaders in science and engineering. I have received numerous other awards, including some the highest honors for semiconductor devices such as the Andrew Grove Award from IEEE, and the Semiconductor Industry Association/Semiconductor Research Corporation University Researcher Award, for my work in semiconductor memory and transistors , which are described in more detail in my CV (Ex.1004).

III. COMPENSATION

15. I am being compensated for my work in this matter at an hourly rate of $650.00 for consulting services. My compensation is not based on the outcome of this matter or on the substance of my opinions.

IV. MATERIALS CONSIDERED

16. In preparing this declaration, I reviewed and considered the following materials, along with any other materials referenced in the body of my declaration:

[1] The NSF Presidential Young Investigator Award was an award given out by the NSF until 1991, at which time it was replaced with the NSF Young Investigator Awards and Presidential Faculty Fellows Program.

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EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 10,861,872 B2 to Liu et al.
1002	File History of U.S. Patent No. 10,861,872 to Liu et al.
1005	U.S. Patent No. 9,859,297 B2 to Park et al. ("Park")
1006	U.S. Patent Publ. No. 2019/0081061 A1 to Tessariol et al. ("Tessariol")
1007	Aritome, "NAND Flash Memory Technologies" (2016)
1008	Silvagni, "3D NAND Flash Based on Planar Cells," Computers 2017
1009	Micheloni et al., "Inside Solid State Drives (SSDs)" (2nd Ed. 2018)
1010	U.S. Patent No. 10,381,369 B2 to Kim et al.
1011	U.S. Patent No. 10,475,737 B2 to Tang et al.
1012	Certified English Translation of Chinese Patent Application Publ. No. CN108766971 to Liu ("Liu")
1013	Chinese Patent Application Publ. No. CN108766971 to Liu
1014	U.S. Patent No. 8,945,996 B2 to Tang et al.
1018	Print out from Geographic Wiki, https://www.studycountry.com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-side (last visited Mar. 28, 2024)
1019	U.S. Patent No. 9,530,492 to Lee
1023	Micheloni, "3D Flash Memories" (2016)

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V. UNDERSTANDING OF THE GOVERNING LAW

17. I am not an attorney but have been instructed in and applied the law as described in this section.

A. Claim Construction

18. I understand that the first step in determining whether a patent claim would have been anticipated or obvious is to ascertain how a person of ordinary skill in the art ("POSITA") would have understood the claim terms.

19. I have been instructed by counsel on the law regarding claim construction and patent claims, and I understand that a patent may include two types of claims: independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim, or it can further depend from another dependent claim. I understand that a dependent claim includes all the limitations that it recites, in addition to all the limitations recited in the claim(s) from which it depends.

20. It is my understanding that in proceedings before the USPTO, the claims of a patent are to be construed under what is referred to as the "*Phillips* standard." I understand that this means that claim terms of a patent are given the ordinary and customary meaning they would have to a POSITA in view of the description provided in the patent itself and the patent's file history.

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21. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a person of skill in the art would have understood the disputed claim language to mean. I understand that, in construing a claim term, one looks primarily to the intrinsic patent evidence, including the words of the claims themselves, the remainder of the patent specification, and the patent's prosecution history. I understand that extrinsic evidence, which is evidence external to the patent and the prosecution history, may also be useful in interpreting patent claims when the intrinsic evidence itself is insufficient.

22. I understand that words or terms should be given their ordinary and accepted meaning unless it clearly appears that the inventors were using them to mean something else. In making this determination, the claims, the remainder of the patent, and the prosecution history are of paramount importance. Additionally, the patent and its prosecution history must be consulted to confirm whether the patentee has acted as its own lexicographer (*i.e.*, provided its own special meaning to any disputed terms) or intentionally disclaimed, disavowed, or surrendered any claim scope.

23. I further understand that in proceedings before the PTAB, claim terms need only be construed to the extent necessary to resolve any controversy that may arise.

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24. In comparing the claims of the Challenged Patent to the prior art, I have considered the '872 Patent and its file history in light of the understanding of a POSITA at the time of the alleged invention. I address further how a POSITA would have understood the claims of the alleged invention in §X.

B. Obviousness

25. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious under 35 U.S.C. §103(a) to a person of ordinary skill in the art of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed. I also understand that the Board considers certain objective factors if they are present, generally referred to as "secondary considerations" or "objective indicia" of nonobviousness, as further discussed below in this section.

26. I have been informed that there are two ways to determine whether prior art is analogous and thus can be considered prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the patentee's endeavor, whether the reference still is

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reasonably pertinent to the particular problem with which the patentee is involved. I have also been informed that the field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference is reasonably pertinent if, even though it may be in a different field from that of the patentee's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to a patentee's attention in considering his or her problem.

27. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there generally must have been some reason or motivation for one of ordinary skill in the art to combine the teachings of the prior art references to arrive at the claimed subject matter.

28. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a person of ordinary skill in the art at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

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29. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine, but that other times the motivation linking two or more prior art references is common sense to a POSITA at the time of the invention.

30. I understand that a particular combination may be proven obvious merely by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. I have further been informed and understand that a POSITA combines the teachings of the prior art references and does not necessarily combine the embodiments of those teachings physically.

31. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

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32. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all of the elements of a claim are used in substantially the same manner in devices in the same field of endeavor, the claim is likely obvious.

33. Additionally, I understand that a patent is likely to be invalid for obviousness if a person of ordinary skill can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

34. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

35. I also understand that one of ordinary skill in the art must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

36. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but

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unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

37. I also understand that evidence of objective indicia of nonobviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a "nexus," between any such secondary indicia and the claimed invention. I also have been informed that even when they are present, secondary considerations may be unable to overcome primary evidence of obviousness (*e.g.*, motivation to combine with predictable results) that is sufficiently strong.

38. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

39. I provide my opinions in this declaration based on the guidelines set forth above.

VI. LEVEL OF SKILL IN THE ART

40. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

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41. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a POSITA is also a person of ordinary creativity.

42. A POSITA in the field of the '872 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, its component parts, how it operates, and how it is controlled.

43. In view of my educational background and work experience, I am a person of more than the ordinary level of skill in the art of the '872 Patent and was so by February 26, 2019. In forming my opinions, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed taking into account the perspective of a POSITA.

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VII. THE '872 PATENT'S EFFECTIVE FILING DATE

44. I understand that the application leading to the '872 Patent was filed on May 2, 2019. I further understand that the patent claims priority to a an earlier-filed PCT publication No. PCT/CN2019/076186, filed on February 26, 2019.

45. For purposes of this declaration, I have been instructed to use February 26, 2019, as the priority date of the '872 Patent. My opinions in this declaration were formed from the perspective of a POSITA as of February 26, 2019, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art.

VIII. TECHNOLOGY OVERVIEW

46. The '872 Patent and the prior art discussed in this Petition relate to three-dimensional (3D) memory devices, *e.g.*, 3D NAND memory devices. The basic building block of the non-volatile semiconductor memory is the memory cell, a structure that stores one or more bits of data. These memory cells are based on the Metal Oxide Semiconductor Field Effect Transistor, or MOSFET. This overview is for N-channel MOSFET-based 3D NAND flash devices. When the proper voltage conditions are applied, (1) electrons are attracted to the surface of the semiconductor device in the channel region forming a conductive path between source and drain and (2) electrons flow through the channel from the source to the drain when a drain voltage is applied. The flow of electrons through the channel is electrically

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controlled by the gate. The voltage on the gate needed to cause significant conduction in the channel is known as the threshold voltage.

47. A traditional type of non-volatile semiconductor memory can store information using a MOSFET that includes an extra "floating" gate. Floating gates were historically made out of conductive electrodes that were not electrically connected to the external terminals such as source, drain and control gate of the memory cell. But charges can also be stored in charge traps in the gate dielectric, where these act as the "floating gates." The shapes of the energy band diagrams in the two cases are somewhat different, but the overall charge storage mechanisms have similarities. I will discuss charge-trap memories in more detail shortly. The floating gate stores the charge that is used to represent the data. A floating gate is surrounded by electrical insulators on all sides - it electrically "floats" in the insulation - and therefore has no direct electrical contact to the rest of the device. Instead, the floating gate is capacitively coupled to the various electrodes. Electrically Erasable Programmable Read Only Memory (EEPROM) can both store and *erase* data electrically. In EEPROM devices, the insulator, or dielectric, between the floating gate and the channel is known as the tunnel dielectric, while the dielectric between the floating gate and the control gate is known as the control dielectric. Flash memory is a type of EEPROM where a large number of memory

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cells can be erased very quickly - that is, in a "flash." Flash memory cells are not erased individually like other EEPROMs, but rather in a group called a "block."

48. The two most common memory cell architectures used for flash EEPROMs are NOR and NAND. The conditions that must be applied to a memory cell in a NOR or NAND architecture in order to program, erase or read the cell are discussed below. Conditions for programming, reading, and erasing memory cells in the various cell architectures were known to those of ordinary skill in the field at the time the '031 Patent was filed. The logic value associated with the "erased" and "programmed" states of a memory cell is a matter of convention. In some sources, the logic value "1" denotes the erased state and "0" denotes the programmed state - in others, the reverse is true. Either of these conventions is appropriate. For this background discussion of NAND architecture, I will use the convention where "1" represents the logic value of the erased state and "0" represents the logic value of the programmed state. In the NOR architecture, a single memory cell exists at each intersection of a bit line (drain) and a word line (control gate). In the NAND memory cell architecture, groups of cells are connected together in series between source and drain (*i.e.*, the bit line). This group of cells, is known as a NAND string. The control gates of these cells are the word lines.

49. One generally programs the cells using tunneling of electrons from the substrate into the floating gate by applying a high positive voltage to the control gate.

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One gets Fowler-Nordheim tunneling through triangular barriers for thicker tunnel dielectrics, or direct tunneling through trapezoidal barriers for thinner tunneling layers. This high voltage applied to the control gate increases the electric field across the tunnel dielectric and narrows the triangular potential barrier for Fowler Nordheim tunneling, thereby making it easier for electrons to quantum mechanically tunnel through the dielectric. There is also an increase of tunneling current for direct tunneling. These tunneled electrons are stored (trapped) on the floating gate. This results in the high threshold voltage state, generally known as the "0" state. One also erases the NAND cell by tunneling, by either applying a high positive voltage to the substrate electrode, or applying a negative voltage to the control gate. This increases the electric field across the tunnel dielectric, reduces the barrier width and thus increases the probability of tunneling (*i.e.*, removing charge from the floating gate). This results in the low threshold voltage state, generally known as the "1" state. For metallic or semiconducting floating gates, the electrons are trapped at the same energy at the Fermi level, or bottom of the conduction band, respectively, and the carriers pile up next to the tunnel dielectric interface. This also makes it necessary to pattern the conducting floating gate to isolate them between adjacent cells. On the other hand, if the charges are trapped in a charge trap layer, there is no need to pattern and etch the layer because the traps states are already isolated from each other. In this case, the electrons can be trapped at multiple trap energy levels and slightly

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different distances from the tunnel dielectric and channel depending on the spatial distribution of the traps, making the threshold voltage distribution wider than for conducting floating gates. The trap potentials are also different. Instead of a trapezoidal well, traps have a Coulombic well that is subject to Poole-Frenkel barrier lowering upon application of a field.

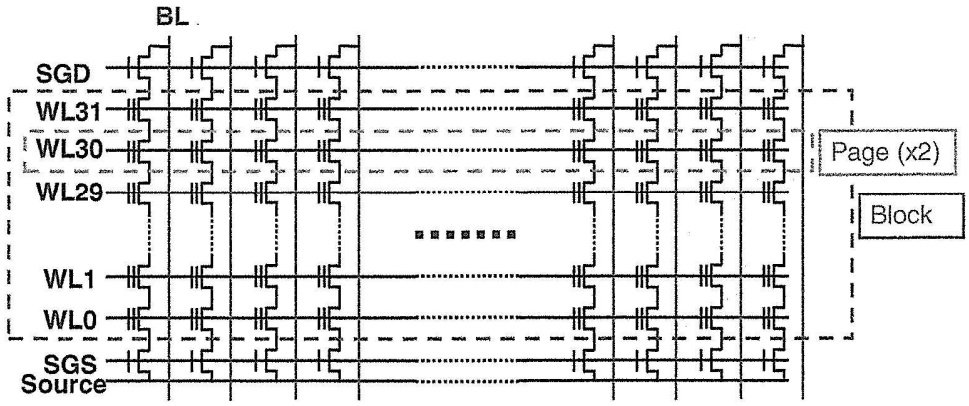
50. NAND cells are read by applying a high voltage (V_PASS) to all the word lines in the NAND string except the cell that is being read. This ensures that all other cells in the string will conduct current. The conduction of the cell being read will depend on whether it is in the "0" or "1" state. This conduction can be determined through the use of a sense amplifier, which may sense either voltage or current on the bit line.

51. NAND memories are more compact than NOR memories because NAND cells are connected in a string. Adjacent NOR cells need to be isolated from each other, which is accomplished using isolation regions which consume "silicon real estate." For NAND architectures, individual cells in a string do not need such isolation -- one only needs to isolate one string from the adjacent strings. This consumes less surface space for isolation and makes the NAND architectures more attractive for mass storage applications. Ex. 1007, 38.

52. In the early days, NAND devices were formed as two-dimensional arrays of cells on a substrate surface (*viz.*, only in the horizontal X- and Y-

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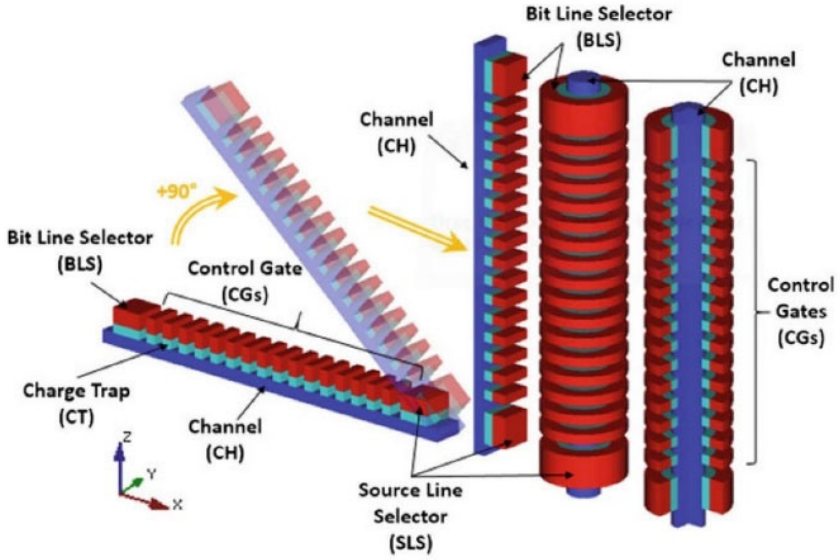
directions). Ex. 1007, 58. The example below from a NAND flash memory textbook is a schematic showing a 2D NAND memory architecture where cells grouped into "page[s]" and "block[s]," which are only fabricated in the X- and Y-directions.



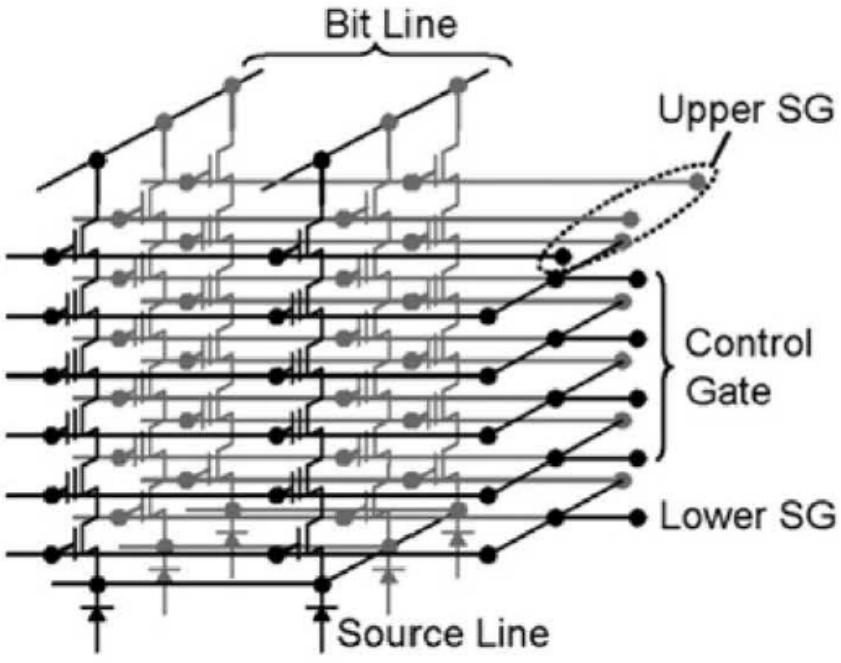
Id., 40.

53. "[T]o further scale down the memory cell size" and achieve higher memory densities, "three-dimensional (3D) NAND flash cells" were developed. Ex. 1007, 292. "Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND string building block" and "turning the 2D NAND string upside," "resulting" in a "3D structure" with a "vertical channel." Ex. 1008, 3. The evolution of NAND architectures from 2D to 3D led to further savings of silicon real estate. The image below illustrates the concept of rotating a NAND memory string on its side (*i.e.*, placing it in the vertical dimension on the z-axis).

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Ex. 1009, 122. The vertical memory cell strings can then be repeated numerous times to form a three-dimensional memory array:

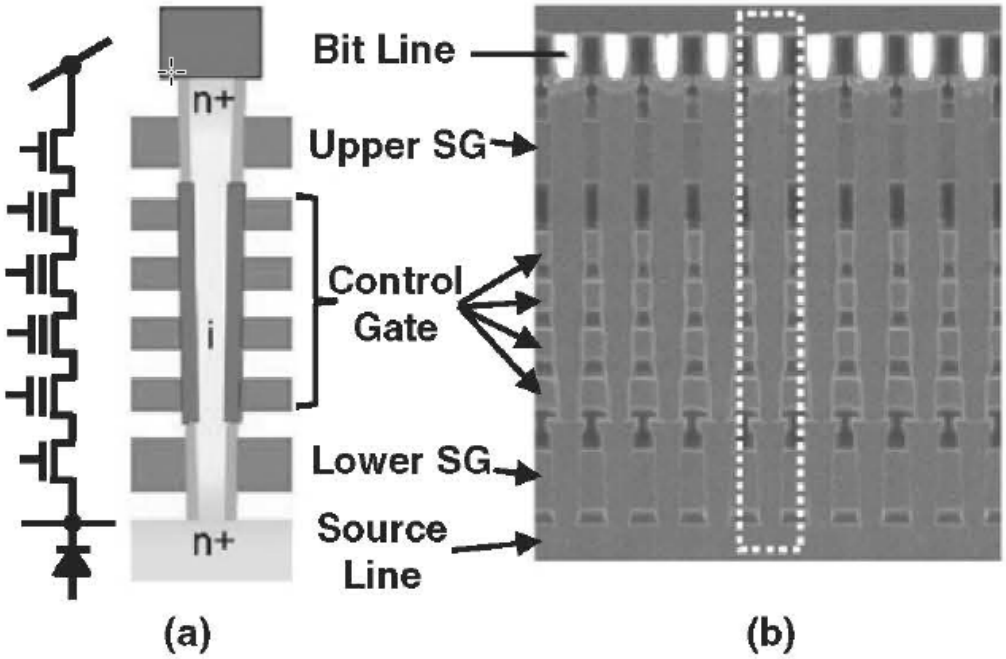


Ex. 1007, 296. This is structurally different than simply stacking various 2D NAND memory arrays on top of one another, because the memory channels/strings in a 3D

NAND run in the vertical (not horizontal) direction which has important implications for semiconductor fabrication of the 3D NAND structures.

54. 3D NAND memory devices typically include alternating horizontal layers of conductors and dielectric in a "[s]tack." Ex. 1007, 294. A vertically aligned "through-hole[]" channel (also known as a channel structure) "filled by memory film … and channel poly-Si" passes through the layers to form the vertical memory cell strings. *Id.*, 295. Control gates for the memory cells are formed where the wordlines (formed by the horizontal conduction layers) intersect the vertical memory strings and act as a control gate. *Id.*, 295-296. A particular vertical memory cell "string is selected by a bit line and an upper select gate (upper SG)." *Id*. The lowest layer is a "select gate (lower SG)" that allows the strings to connect to a lower "common source." *Id.*, 295, 297. An example 3D NAND vertical memory cell string is shown below.

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Id., 296.

55. It was well-known to POSITAs to use so-called "staircase structures" to provide electrical access points for the various wordlines. For example, as illustrated below, each subsequent wordline (40) progressively extends further in the horizontal X-direction to provide landing pads for the contacts 60.

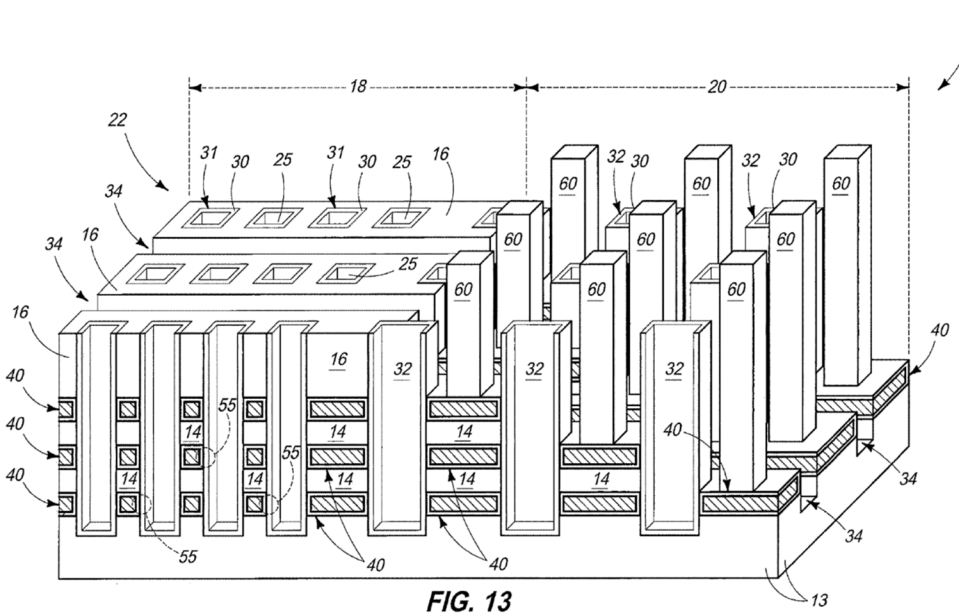


FIG. 13

Ex. 1010 (U.S. Pat. No. 10,475,737), Fig. 13, 4:56-64, 8:45-56.

56. To manufacture such 3D NAND devices, it was known in the art to utilize sacrificial layers. Rather the simply depositing alternating layers of dielectric and conductor, the "sacrificial" approach entailed first creating an alternating stack of dielectric layers and interim "sacrificial layers," which are subsequently removed and replaced with conductive control gate layers. Ex. 1010 (U.S. Pat. No. 10,475,737), 4:25-55. Due to the increased number of layers in 3D NAND relative to 2D NAND, there was a greater need for vertical stability, and it was known to use supporting pillars that extend through the stack to provide mechanical support during the process of replacing the sacrificial gate layers with conductive gate layers. *Id.*, 7:44-8:3.

57. The stacked structure in 3D NAND devices typically include a core region, which includes the memory cells, and a peripheral region, which includes a connection region known as the staircase region. Ex. 1010 (U.S. Pat. No. 10,381,369), 5:43-6:11, 12:20-27. Staircase structures were well known and structurally provide landing areas for contacts to the control gates or wordlines (below, the contacts 60 connect to different control gates):

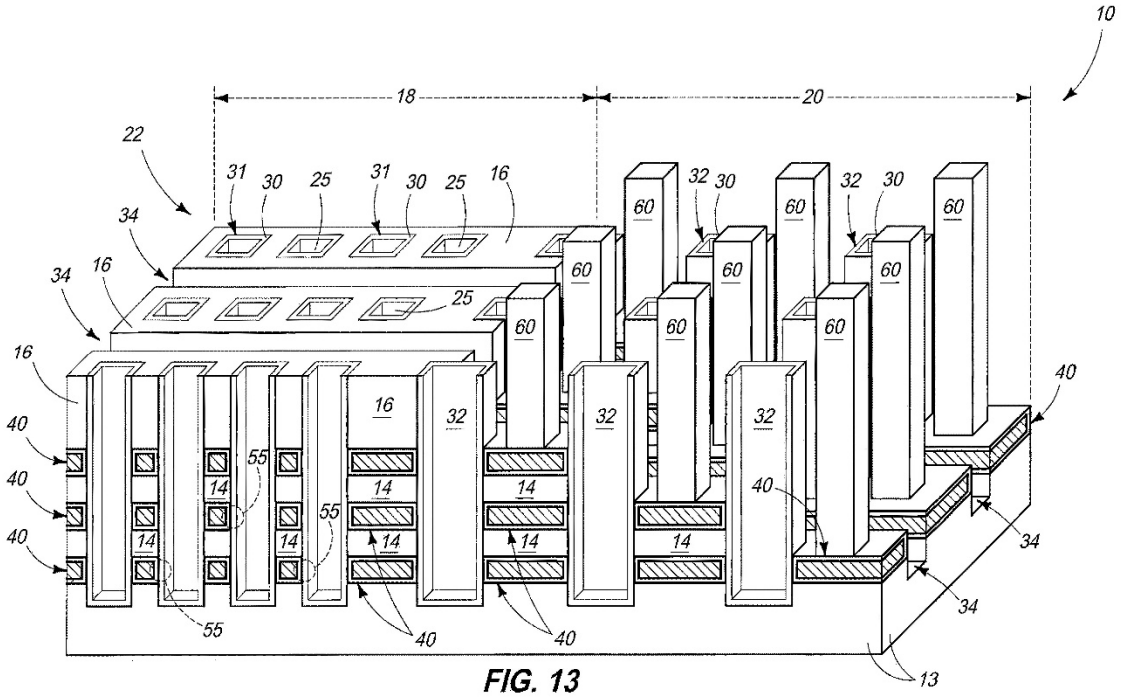


FIG. 13

Ex. 1011 (U.S. Pat. No. 10,475,737), Fig. 13, 4:56-64, 8:45-56.

58. One method of forming 3D NAND memory devices is to form the alternating stack of sacrificial gate layers and dielectric layers, and then replace the sacrificial gate layers with metal layers. Ex. 1012 (CN Patent Appl. Publ. No. CN108766971), [0062]. This is known as a gate replacement or gate last process.

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It was known that to perform this gate replacement process, "support pillars" were necessary to be included in the staircase structure (the support pillars extend through the stacked structure) to "prevent the stacked structure from collapsing." *Id.* [0002], [0062]; *see also* Ex. 1014 (U.S. Pat. No. 8,945,996), 5:64-6:2 ("dummy" structures have been used for a "load carrying ability of an operative structure"). Support pillars may be made with different materials, e.g., materials of a conductive via or materials of a channel structure, and may be a dummy structure (serve no other role than a supporting member) or an active structure (e.g., also serve as an interconnect to connect two circuit elements or conductive via, in the case the filler is a conductive material). *Id*., 6:5-38, 7:19-23; Ex. 1012 (CN Patent Appl. Publ. No. CN108766971), [0044]; Ex. 1006, [0037], [0038], [0041].

IX. THE '872 PATENT

A. Summary of Patent

59. The '872 Patent relates to "[t]hree-dimensional (3D) memory devices and methods for forming the 3D memory devices." Ex. 1001, Abstract. Three-dimensional (3D) memory devices include a core set of structural components. The '872 Patent includes these basic components. These include a substrate upon which subsequent layers are formed. On the substrate, an alternating stack of conductive layers and dielectric layers is formed. From this stack, a staircase structure is formed by trimming the layers to form a structure with stepped surfaces. These stepped

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surfaces provide landing areas for staircase electrical contacts that connect to each conductive layer (each of which serves as a word line). Finally, dummy structures provide a mechanical support function for the stack. *Id.*, 1:34-43, 16:40-44.

60. The '872 Patent discusses the traditional gate replacement process. Ex. 1001, 1:56-58, 4:30-33; 4:46-55; 5:17-28. As I discuss in Section VII, the alternating stack is first constructed using sacrificial gate layers. Then, subsequently, the sacrificial layers are etched away and replaced with conductive layers to form gate layers (also known as word lines). *Id.*, 1:56-58, 4:30-33; 4:46-55. This process facilitates using more conductive gate layer materials.

61. The '872 Patent alleges that the gate replacement process became more challenging because of the memory devices scaling down in size. Ex. 1001, 4:37-38. The '872 Patent addresses gate line slits ("GLS"). GLS was, and is, a term of art. GLS typically divide the alternating stack (also known as a memory stack) into smaller memory stacks. *Id.*, 4:37-46. Dividing a memory array (here, a stack) into smaller units using such structures was well known, and the smaller units are often referred to as blocks or sub-blocks.

62. The '872 Patent recognizes that a GLS has "large dimensions and is filled with an insulation structure formed in a trench." Ex. 1001, 4:37-46. GLS are formed by etching trenches in the memory stack. *Id.*, 4:44-49. Notably, the trenches are used in the gate-line replacement process. The trenches are the source for the

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etch materials that etch the sacrificial gate layers to form voids between the dielectric layers in the stack (support pillars support the stack during this process). That is, the etch occurs through the trench voids. The trenches are also the source for the deposition materials that form the control or word lines. *Id.*, 4:46-48. That is, the deposition occurs through the trench voids. Annotated Figure 5 below shows a top view (meaning the perspective as if one were to cut through the stack at a given point and look straight downward) of a memory stack that is split into smaller memory stacks (e.g., blocks) by GLSs.

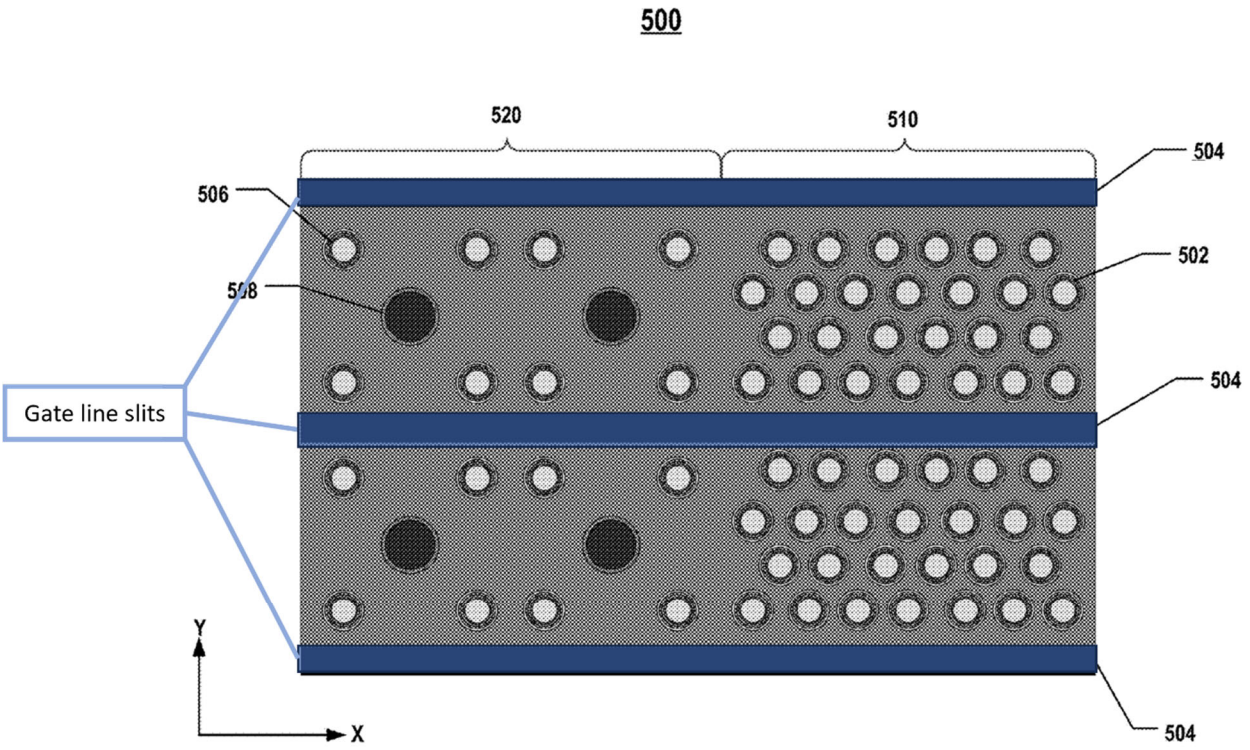


FIG. 5

63. The ’872 Patent alleges that the problem with “[u]sing GLSs to perform the gate-replacement process” was “the large lateral distance between adjacent GLSs” that “cause conductive material to be unevenly filled in the lateral recesses formed after the removal of the sacrificial layers, resulting in voids in the formed gate electrodes.” Ex. 1001, 4:49-55. In other words, because the deposition material must travel a long distance, it was difficult to form uniform gate layers. *Id.*, 5:17-20.

64. The ’872 Patent alleges that the solution to this problem is replacing the GLSs with “dummy source structures.” Ex. 1001, 5:31-34. Annotated Figure 2A below shows the etched dummy source hole in the staircase structure.

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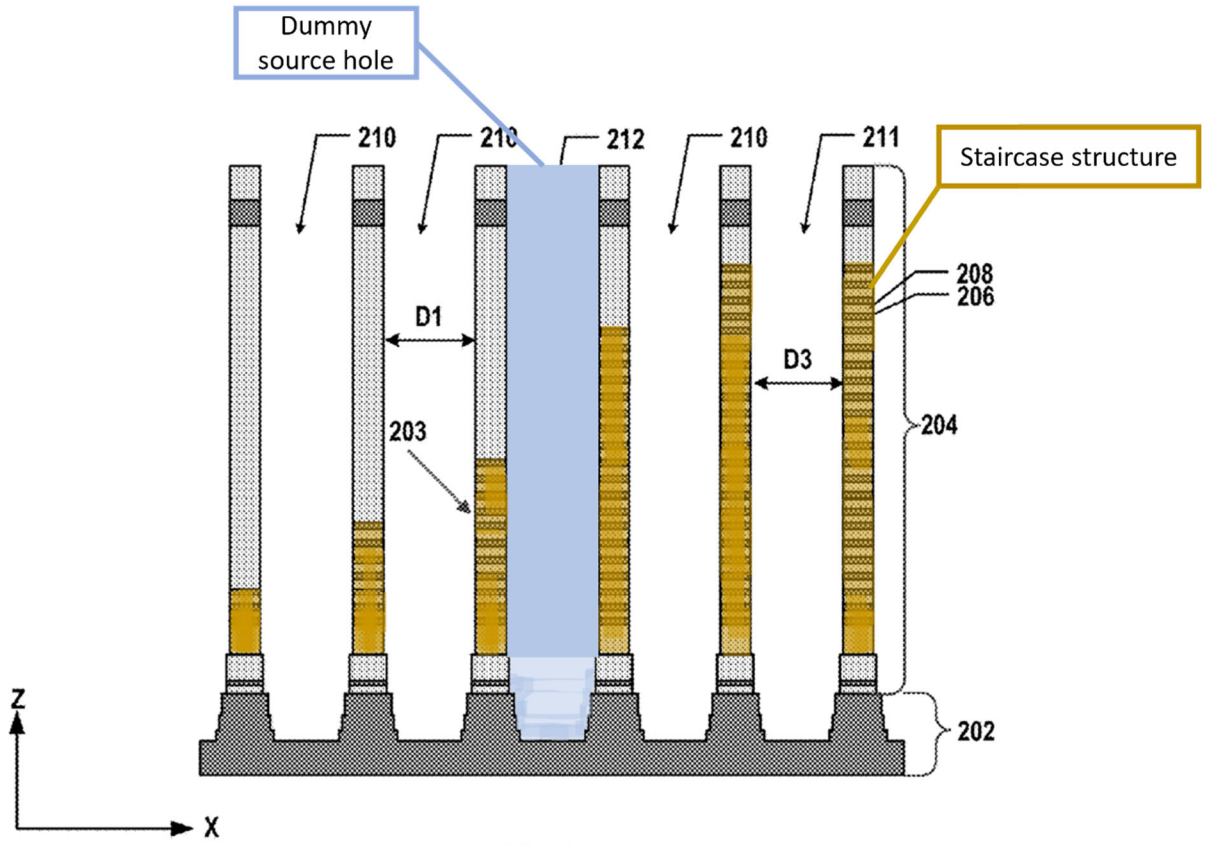


FIG. 2A

65. The '872 Patent discloses using this void for the gate replacement process. *Id.*, 15:16-25.

66. After the gate replacement process is complete, the '872 Patent discloses that dummy source structures "may include an insulating spacer layer in a dummy source hole and a conductive contact within the spacer layer." Ex. 1001, 5:37-43. This specific structure can be thought of a dummy or operative interconnect through the stack (which I discuss further in Section X.A). An insulating spacer (177) first lines the dummy source hole, which insulates the conductive core from the surrounding conductive elements, e.g., the gate layers. Then conductive material

is deposited to form a core conductive element. Dummy source structure (179) is shown below in Figure 1D:

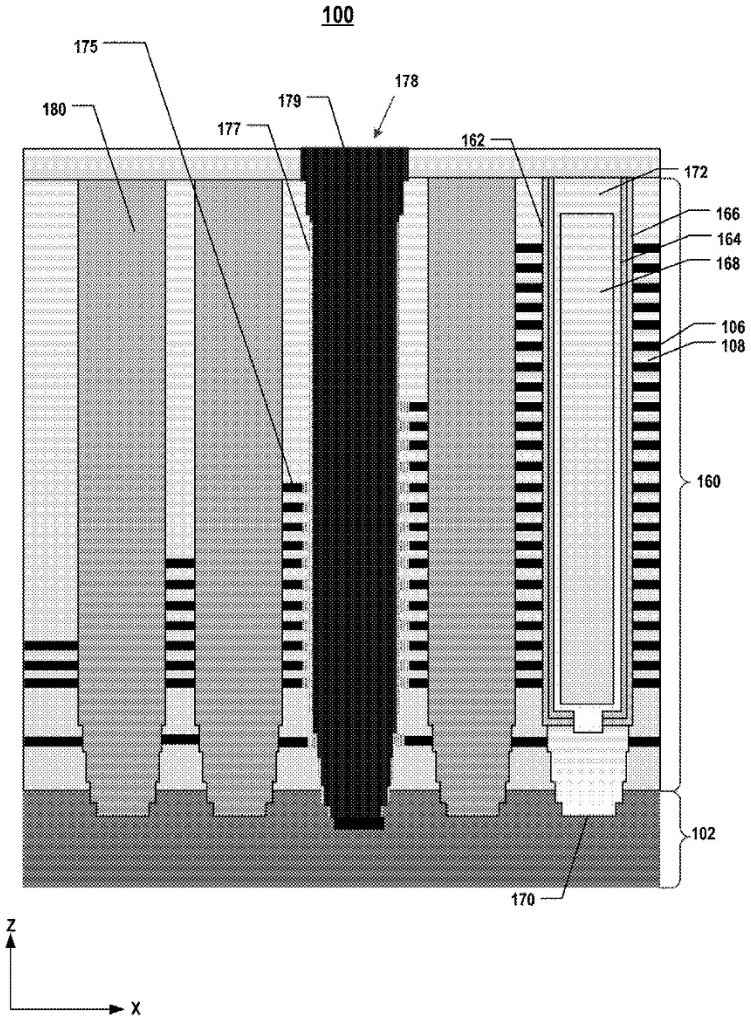


FIG. 1D

Id., Fig. 1D, 5:37-40

67. The '872 Patent claims that replacing GLSs with dummy source structures allows gate electrodes "to be formed with improved uniformity and quality, reducing the resistivity of the gate electrodes/word lines." Ex. 1001, 5:49-52. The '872 Patent alleges that since conductive material "travels shorter distances

to fill up the lateral recesses for forming the gate electrodes, the gate electrodes are less susceptible to voids or density nonuniformity." *Id.*, 5:55-58.

B. Prosecution History of the '872 Patent

68. On June 11, 2020, the Examiner rejected claims 1-13 under 35 U.S.C. §102(a)(l) as anticipated by U.S. Pub. No. 2016/0293622A1 ("Jeong"). Relevant here, the Examiner found that Jeong discloses "dummy pillars DP1 and DP2" that "function as a mechanical support for conductive layers" which were akin to "dummy source structures." Ex. 1002, 470.

69. On August 14, 2020, the Examiner and the Applicant discussed during a telephone interview the distinction between "dummy source" and "dummy channel." Ex. 1002, 505. Based on the interview, the Applicant amended claims 1 and 8 on August 18, 2020 to add the limitation "wherein each of the dummy source structures comprises a conductive contact." *Id.*, 510-511, 513. The Applicant argued that this feature is "not found in Jeong." *Id.*, 513-514. The Applicant further emphasized a portion of the specification: "dummy source structures 178 can [also] laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks." *Id.*, 514.

70. The Examiner then allowed the claims. Ex. 1002, 524. The reasons for allowance were that Jeong did not disclose a dummy structure that comprised a

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conductive contact and that Jeong's dummy pillars DP1 and DP2 could be "considered as the dummy channel structures." *Id.*, 525-26.

X. CLAIM CONSTRUCTION

71. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. As discussed in §V.A above, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review and I have applied them in forming my opinions.

72. I have been asked to provide my opinion on how the term "dummy source structure" would be understood and also my opinion on whether "surrounding" would have been understood to require fully bordering or fully encircling.

A. "dummy source structure" (Claims 1-6, 11-13)

73. The term "dummy source structure" is a limitation of all Challenged Claims.

74. In my opinion, the term "dummy source structure" would have been understood to mean a "structure that occupies the void that was used for the gate replacement process," which is supported by both the specification and the file history. I have been instructed that in the Co-Pending Litigation, PO appears to be interpreting this limitation to mean that the dummy source structure need not be

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formed in the voids that are used for the gate line replacement process. Accordingly, in this Declaration, I offer opinions under the correct construction of "dummy source structure" and what I understand PO's interpretation to be.

75. First, the '872 Patent is clear that it is "replacing the [gate line slits] with dummy source structures." Ex. 1001, 5:30-34. As I have discussed in Section IX.A, the '872 Patent details alleged problems using GLSs for the gate replacement process. *Id.*, 4:44-55, 4:65-67. The '872 Patent then explains that replacing GLSs with "dummy source structures" allegedly solves these problems, e.g., because the gate layers will be "less susceptible to voids or density nonuniformity." Ex. 1001, 5:49-58. Specifically, because the "gate-replacement process can be performed to deposit a conductive material through the dummy source holes that subsequently form the dummy source structures," the "conductive material travels shorter distances to fill up the lateral recesses for forming the gate electrodes." *Id*.

76. As I describe above, the '872 Patent solves the alleged problems by using the voids, which the '872 Patent refers to as "dummy source holes," that are later occupied by the "dummy source structures." In other words, the dummy source holes are used like the GLS trenches (i.e., the voids are used in the gate line replacement process), and a respective structure fills the respective voids. Thus, the '872 Patent discusses the alleged solution in the context of "dummy source holes." For example, the '872 Patent discloses that because the "gate-replacement process

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can be performed to deposit a conductive material **through the dummy source holes that subsequently form the dummy source structures**," the "conductive material travels shorter distances to fill up the lateral recesses for forming the gate electrodes." Ex. 1001, 5:49-58. And the specification defines the "dummy source structures" as what occupies the "dummy source holes": "dummy source holes that subsequently form the dummy source structures." *Id.* Thus, when the '872 Patent states that it is "replacing the [gate line slits] with dummy source structures" (*Id.*, 5:30-34), a POSITA would have understood that the '872 Patent is "replacing the [gate lines slits] with [dummy source holes in which the dummy source structures are subsequently formed]." *Id.*, 4:65-67. In other words, the dummy source holes are used for the gate line replacement process. Thus, the GLSs are replaced with dummy source holes, and the dummy source holes are subsequently filled and become dummy source structures.

77. Thus, in view of the above, a POSITA would have understood that a "dummy source structure" occupies the void used for the gate replacement process.

78. From the specification, however, a POSITA would not have understood there to be any meaningful limitation on the actual structure (or layout pattern) of the dummy source structure because the specification broadly describes that it may assume different structures, sizes, and shapes. For example, the specification states that "[d]ifferent layouts, patterns, and designs" for the dummy source structure may

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be adopted "based on the size of the staircase region." Ex. 1001, 8:51-53. The specification further states that the dummy source holes, which the dummy source structures occupy, may or may not be made using the same process that makes the dummy channel holes. *Id.*, 13:3-5. Dummy channel structures will fill the dummy channel holes. Dummy channel structures are inoperative channel structures (memory strings). Often, dummy channel structures are used as support pillars, e.g., during the gate line replacement process or more generally as a support member for the memory stack. The specification discloses that the dummy source structures and dummy channel structures also may be the same size. *Id.*, 8:11-19. If the dummy source holes and dummy channel holes were made by the same process, they would appear, effectively identical in size. So here, the specification is stating the dummy source structures may be the same size or a different size, shape, etc., as dummy channel structures.

79. Importantly, the dummy source structure may assume the same shape as a GLS, because the specification states that "dummy source structures 178 can ***laterally separate*** 3D memory device 100 into multiple memory regions, such as memory blocks." Ex. 1001, 11:44-46 (emphasis added). Recall my discussion on dividing the memory stack into smaller units. *See* Section IX.A. This is what it means to "laterally separate" the memory device. This separating is exactly what GLSs do. The '872 Patent itself recognizes this: "[f]or example, in some 3D memory

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devices such as charge trap 3D NAND memory devices, gate line slits (GLSs) are formed to divide an array of memory strings (e.g., in the inner region of a 3D memory device) and/or dummy channel structures (e.g., in the staircase region of the 3D memory device) into different memory regions." Ex. 1001, 4:38-44. Thus, from the discussion above regarding dummy channel holes and the "laterally separate" disclosures, a POSITA would have understood the structure can assume many different shapes, whether that be circular or a long wall shape that laterally divides the stack.

80. As to what "dummy" would have been understood to mean, a POSITA generally would have understood "dummy" to refer to an inoperable component. For example, as I discuss with respect to Tessariol in Section XII.A.2, there may be dummy vias (which Tessariol refers to as dummy structures 60) and operable vias (which Tessariol refers to as operative conductive vias 58). These elements are often mostly the same, but for example, the dummy components are not interconnected to electrically functional elements (e.g., connected to a circuit element). But here the specification explains that the dummy source structure might not even be an inoperable structure. The specification states that "dummy source structures" can "contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices." Ex. 1001, 5:41-43, 16:63-66. The "interconnect" is referring to connecting two elements, namely, an element within the memory portion

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with a peripheral circuit element. Thus, the '872 Patent does not use "dummy" to exclude the dummy source structure from being an operable, functioning element such as a conductive via.

81. As to the file history, in the Office Action response, the Applicant emphasized the portion of the specification which states: "dummy source structures 178 can [also] laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks." Ex. 1002, 514. This confirms that the structure not only can be circular, but also the shape as a long wall that divides the memory stack, like a GLS.

82. In Ground 1, I apply both what I understand to be the Petitioner's construction ("structure that occupies the void that was used for the gate replacement process") and what I will refer to as PO's construction (the structure need not fill the void that was used for the gate line replacement process). In Ground 2, I only apply PO's construction.

B. "surrounding" (Claims 1-6, 11-13)

83. The term "surrounding" is a limitation of all Challenged Claims.

84. In context, the term appears in independent claim 1 as follows "the plurality of dummy source structures surrounding the staircase contact." I have been asked to opine on whether "surrounding," in the context of the '872 Patent, would have been understood to require that the dummy source structures form a border that

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fully encloses the staircase contact. It does not. This is clear from the specification, claims, and extrinsic evidence.

85. As a preliminary note, of course, "surround" here is not referring to the top and bottom portions of the staircase contact, because there is not any dummy source contact at all above or below the staircase contact. Thus, this discussion is with respect to the lateral sides of the staircase contact, not the top or bottom of the staircase contact.

86. In the figures of the '872 patent, four dummy source structures are shown to "surround" a staircase contact. *See* Section IX.A. That is, four dummy source structures are at radial positions around the staircase contact, e.g., angles 0, 90, 180, and 270 degrees. Thus, "surround" certainly does not mean fully encircle, fully border, as there are large, open gaps around the staircase contact.

87. In addition, the specification and claims make clear to a POSITA that "surround" does not require that four dummy source structures "surround" the staircase contact. The specification expressly states that "the number of dummy source structures surrounding one or more dummy channel structure 124 may be more or less than eight, six, or four." Ex. 1001, 8:8-11. In other words, there may be ***less*** than four dummy source structures that radially "surround" a staircase contact. What "surround" looks like with three dummy source structures surrounding a staircase contact is shown below in annotated Figure 1A.

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88. The claims also make it clear that only three dummy source structures may "surround" the staircase contact. Dependent claim 15, which depends on claim 14, recites: "wherein at least one dummy channel structure is surrounded by at least four dummy source structures." Ex. 1001, Claim 15. I understand that under the doctrine of claim differentiation, an independent claim is presumably broader than a dependent claim. Here, this would mean claim 14, which is independent and uses the term "surround" as well, includes within its scope that fewer than four dummy source structures may "surround" a dummy channel structure. While here the claim is referring to dummy channel structures surrounding a dummy source structure, to a POSITA, the '872 patent is not using "surround" differently.

89. As shown below, a preferred embodiment employs four dummy source structures (126) around staircase contact (122). According to the specification and claims, three dummy source structures may "surround" the staircase contact. This would leave even more openings around the staircase contact.

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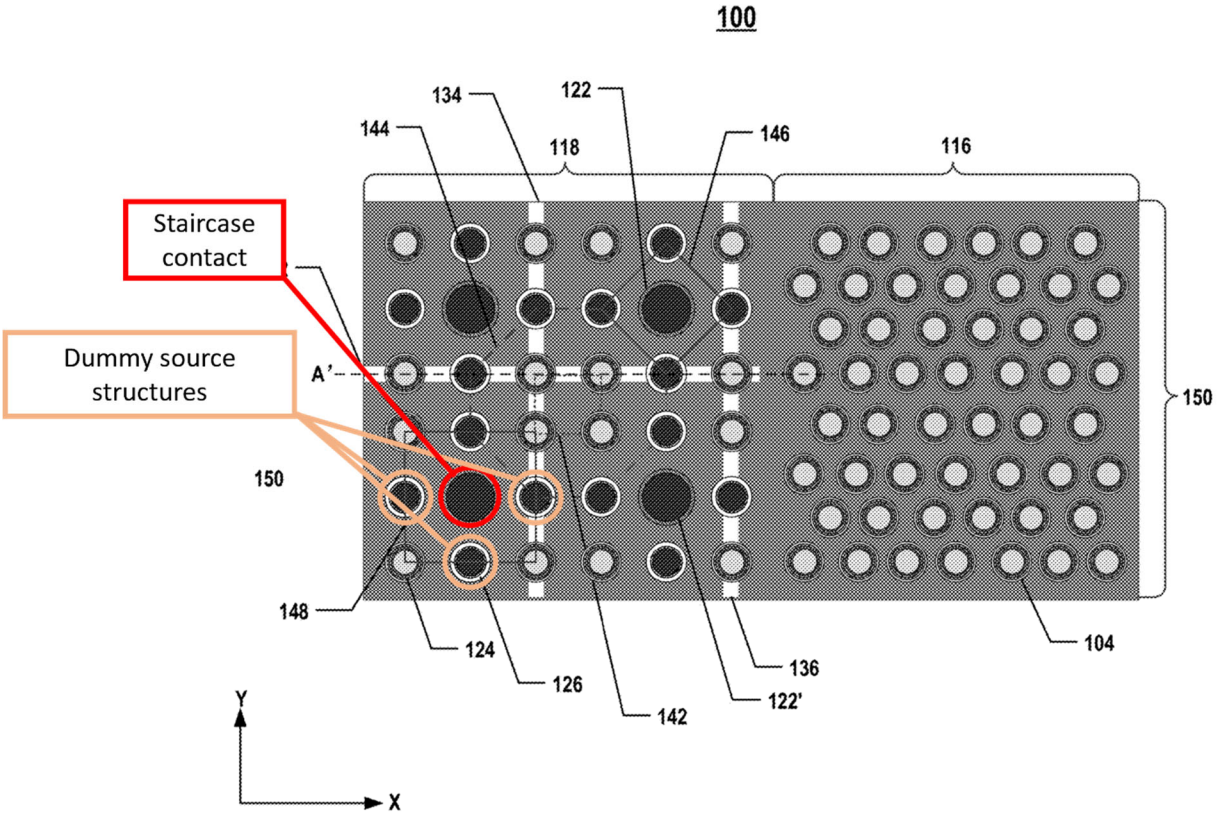
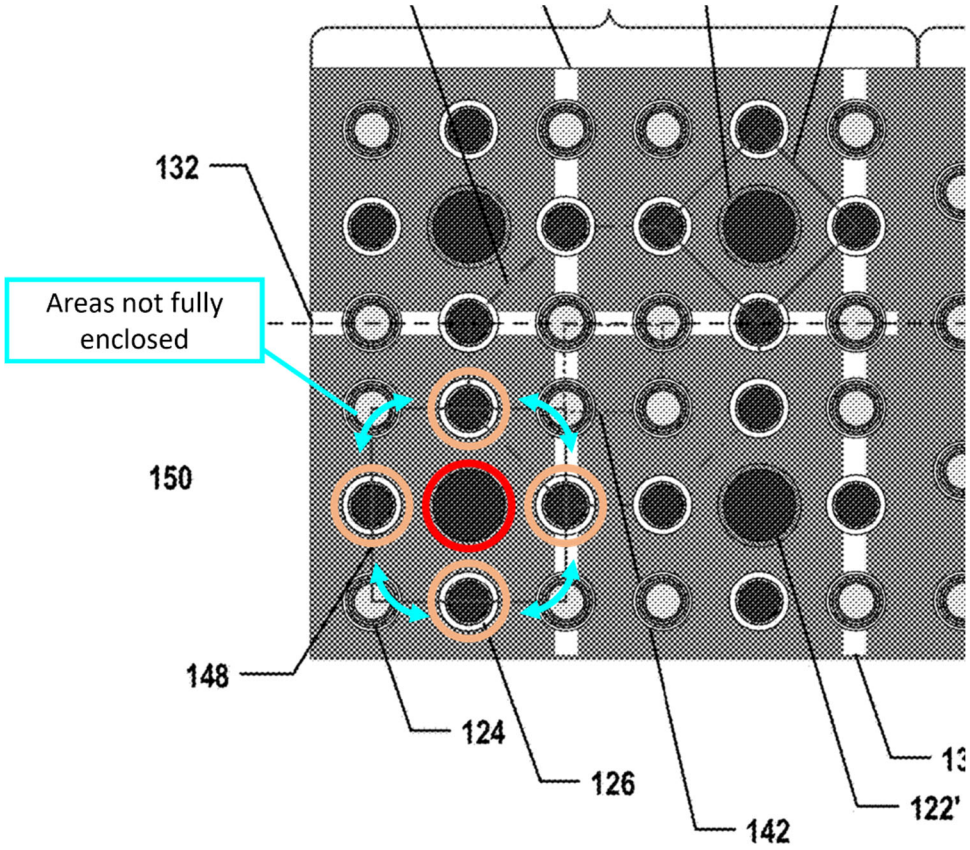


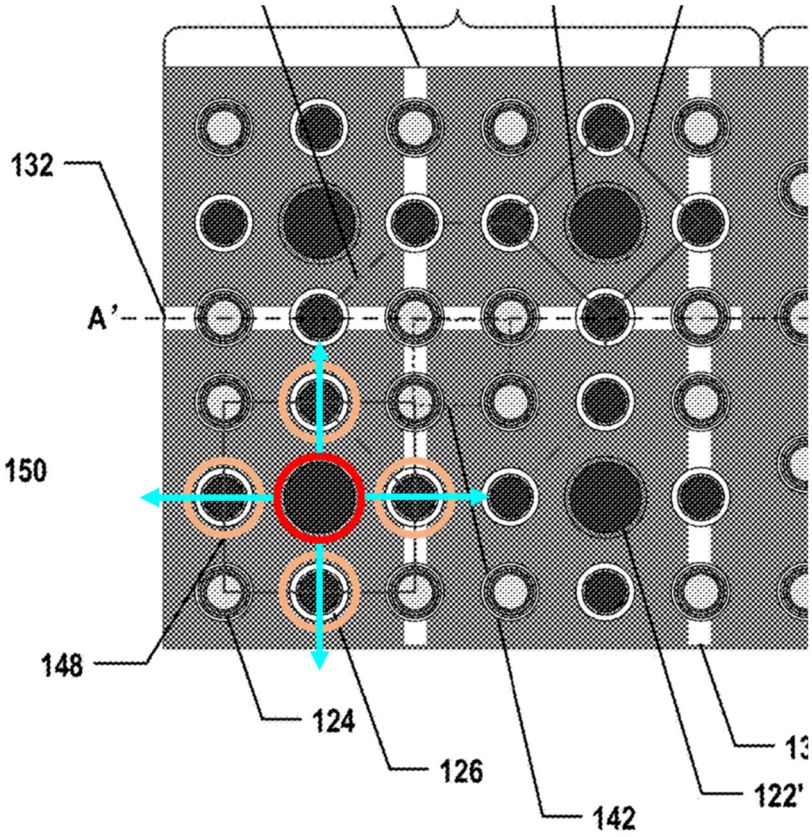
FIG. 1A

Ex. 1001, Fig. 1A.

90. It can also be seen that "surround" does not mean fully enclose when viewing the gaps (areas in which there is not a dummy source structure) in the direction radially outwards from the staircase contact. For example, taking the case of four dummy source structures, there are large gaps. These large gaps between the dummy source structures (126) are shown in blue below. Regardless of these gaps, the '872 Patent still refers to the dummy source structures (126) "surrounding" the staircase contact (122).



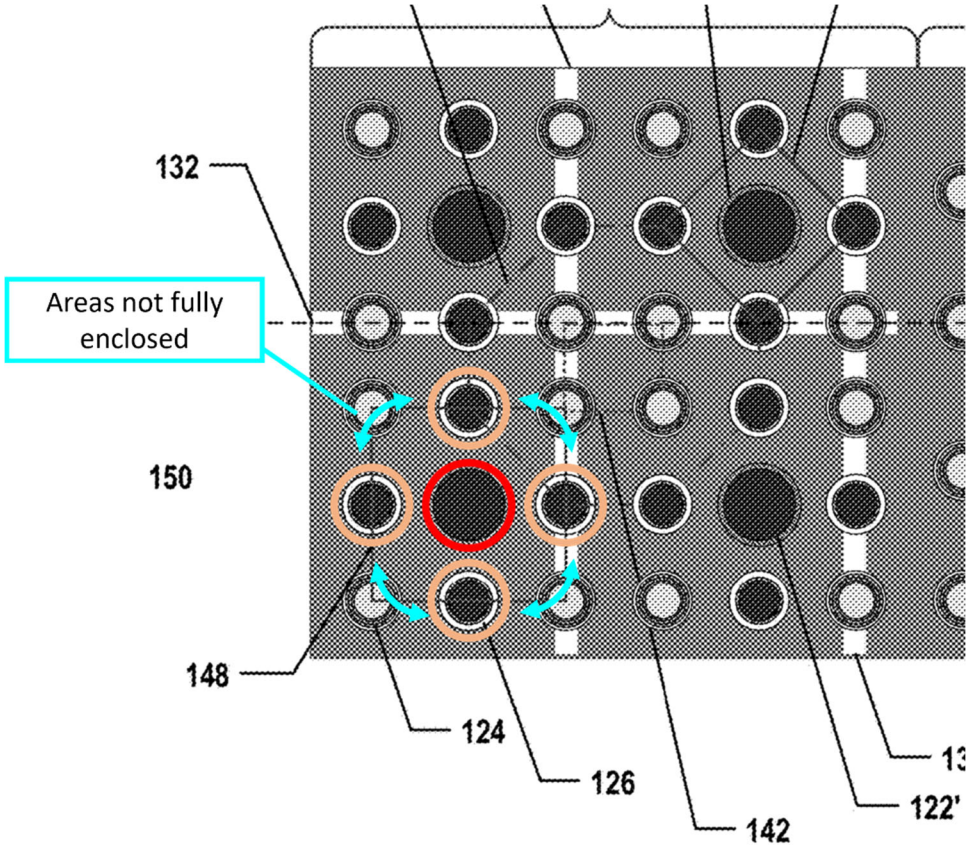
Ex. 1001, Fig. 1A (partial) (annotated). In view of this, a POSITA would have understood one way to be "surrounding" in this context, consistent with the above figure, is to be able to draw four lines outward from the staircase contact with each line being separated from the others by 90 degrees and intersecting a dummy source structure.



Id., Fig. 1A (annotated).

91. A POSITA would have also understood one way to consider "surrounding" is to consider the amount of radial border that the dummy source structures create. In fact, the specification makes clear that the number of a particular structure, e.g., dummy source structures, is not relevant to whether that structure "surrounds" another object. The specification states that "[a]ny suitable number of dummy channel structures may be surrounded by any suitable number of dummy source structures." Ex. 1001, 7:40-43. Thus, there could be fewer, larger dummy source structures that surround the staircase contact. For example, two

dummy source structures could "surround" the staircase contact. Here, one would view the areas not fully enclosed to determine the extent of "surrounding," as shown below:



Id., Fig. 1A (partial) (annotated).

92. The meaning of the term "surround" is context dependent. A POSITA does not necessarily have to assume that "surround" in the semiconductor context means fully encircle. I also note that the term does not always mean fully encircle outside of the semiconductor context as well. For example, "[a]n isthmus is a thin strip of land surrounded by water on two sides, which connects two larger

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landmasses." Ex. 1018 (https://www.studycountry.com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-sides.). In the 3D NAND context, for example, two lateral elements on each side of a structure "surround" that structure. Ex. 1019 (U.S. Pat. No. 9,530,492), 2:14-16 ("In other words, the conventional SBPI operations are strongly affected by the stored Vts of two surrounding NAND cells dispersed in the adjacent left and right BLs."). Thus, consistent with other uses of "surround," the '872 Patent is not using "surround" to mean fully encircle.

93. As I will discuss in greater detail, Park discloses dummy source structures that more fully "surround" a staircase contact than the '872 Patent. Tessariol discloses dummy source structures, under PO's construction, that "surround" the staircase contacts just like the '872 Patent's exemplary embodiments.

XI. SUMMARY OF OPINIONS

94. I have reviewed and analyzed the prior art references and materials listed in §XII below.

95. For the reasons I explain in greater detail below, it is my opinion that before the earliest possible filing date of the '872 Patent on February 26, 2019, a POSITA would have considered claims 1-6 and 11-13 of the '872 Patent to be unpatentable as obvious over the prior art discussed in this declaration. Below is the summary of the grounds detailed in this declaration:

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Ground	Claim(s)	Prior Art Asserted
1	1-6, 11, and 13	Obvious under §103 based on U.S. Patent No. 9,859,297 (Ex. 1005, "Park") [2]
2	1-6 and 11-13	Obvious under §103 based on U.S. App. Pub. No. 2019/0081061 (Ex. 1006, "Tessariol")[3]

XII. THE PRIOR ART

A. Overview of the Prior Art

96. Next, I provide an overview of the main prior art references I discuss throughout this declaration.

1. Park (Ex. 1005)

97. Park is a U.S. Patent filed on February 19, 2016.

98. Park teaches the basic structural components of a three-dimensional memory device and methods for making them. Those basic components include a substrate, interleaved conductive gate lines and insulating layers (that is, the alternating stack of gate and dielectric layers), and dummy components (that is, support members). Ex. 1005, 1:39-59. Park also teaches the use of common source lines 144 and dummy source lines 146 (i.e., dummy source structures) to "improve[]

[2] Park was filed February 19, 2016 and is prior art under at least AIA §102(a)(2).

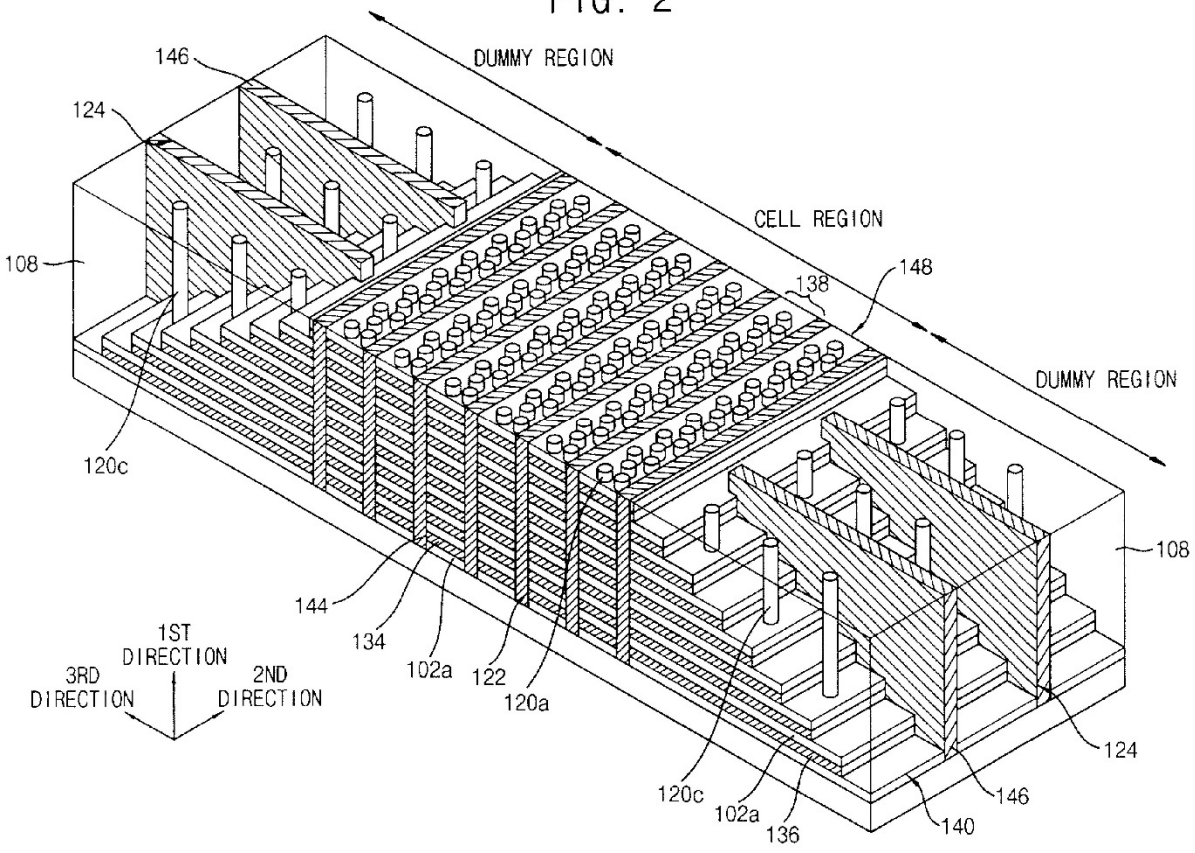
[3] Tessariol was filed September 14, 2017 and is prior art under at least AIA §102(a)(2).

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structural and electrical reliability" issues. *Id.*, 1:37-38. These source lines connect an upper-level circuit element to the source layers in or on the substrate.

99. "FIG. 2 is an enlarged perspective view of a portion 'A' in FIG. 1." Ex. 1005, 5:48-51. Thus, it is just a view of a portion of the memory device that excludes the areas above and below (from the second direction) of the cell region.

FIG. 2



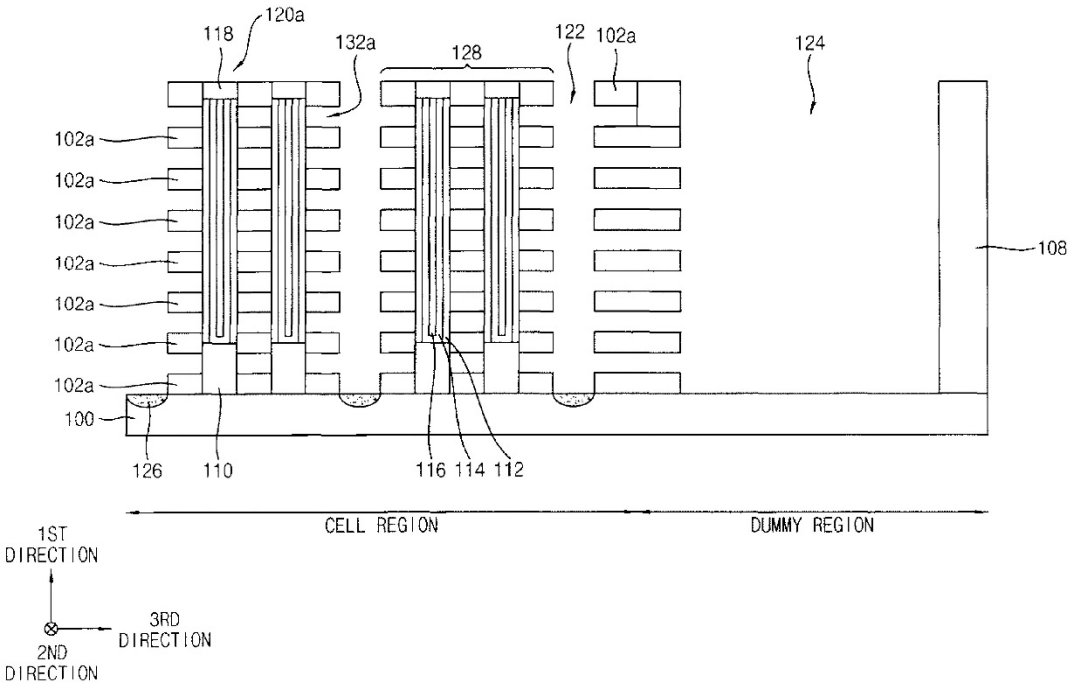
Id., Fig. 2.

100. Park teaches first forming an interleaved insulating and sacrificial layer stack. This stack includes a cell region, i.e., the region in which the active channel

structures (memory strings) are located. Surrounding the cell region are stepped regions (I discuss this in greater detail in Section XIII.A.4). Shown above, the stepped regions are in the dummy region. Ex. 1005, 9:36-46 (discussing Fig. 5). These stepped regions are known as staircase structures. *See* Section VIII.

101. First and second openings (122, 124) are etched in the insulating/sacrificial layer stack during the gate replacement process. Ex. 1005, 11:66-12:4. The first opening 122 is formed in the cell region and the second opening 124 is formed in the dummy region.

FIG. 9



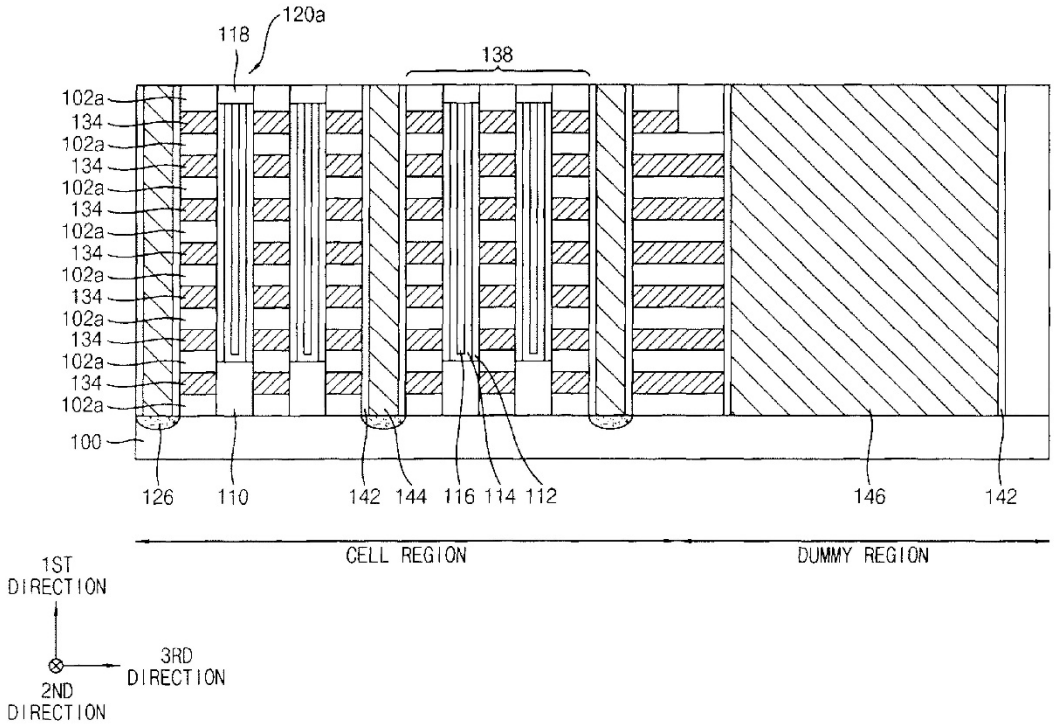
Id., Fig. 9.

102. The first and second openings (122, 124) are the same as the '872 Patent's dummy source holes. Specifically, these openings allow for the etching and deposition steps that replace the sacrificial gates. Ex. 1005, 12:44-13:13. In other words, the etching and deposition materials are directed into these openings to remove the sacrificial layers and form the actual gate layers, respectively.

103. After the gate replacement process, an insulation layer is formed on the sidewalls of the first and second openings (122, 124). This insulation layer, also known as a liner, serves to electrically isolate the core (which is subsequently deposited) from the gate layers. Next, a conductive layer fills the rest of the opening (via a deposition step) to form a common source line and dummy source line (144 and 146, respectively). Ex. 1005, 7:63-64 ("The CSL 144 may be in the first opening 122…"); 13:42-59; 14:67-15:2 ("The dummy source line 146a may be disposed in the second opening 124a…"). Again, with a vertical common source line, ultimately a connection will be made from the top of the common source line to an upper-level interconnect, such that a source connection is formed between the upper-level area and portions of the substrate (or material on the substrate).

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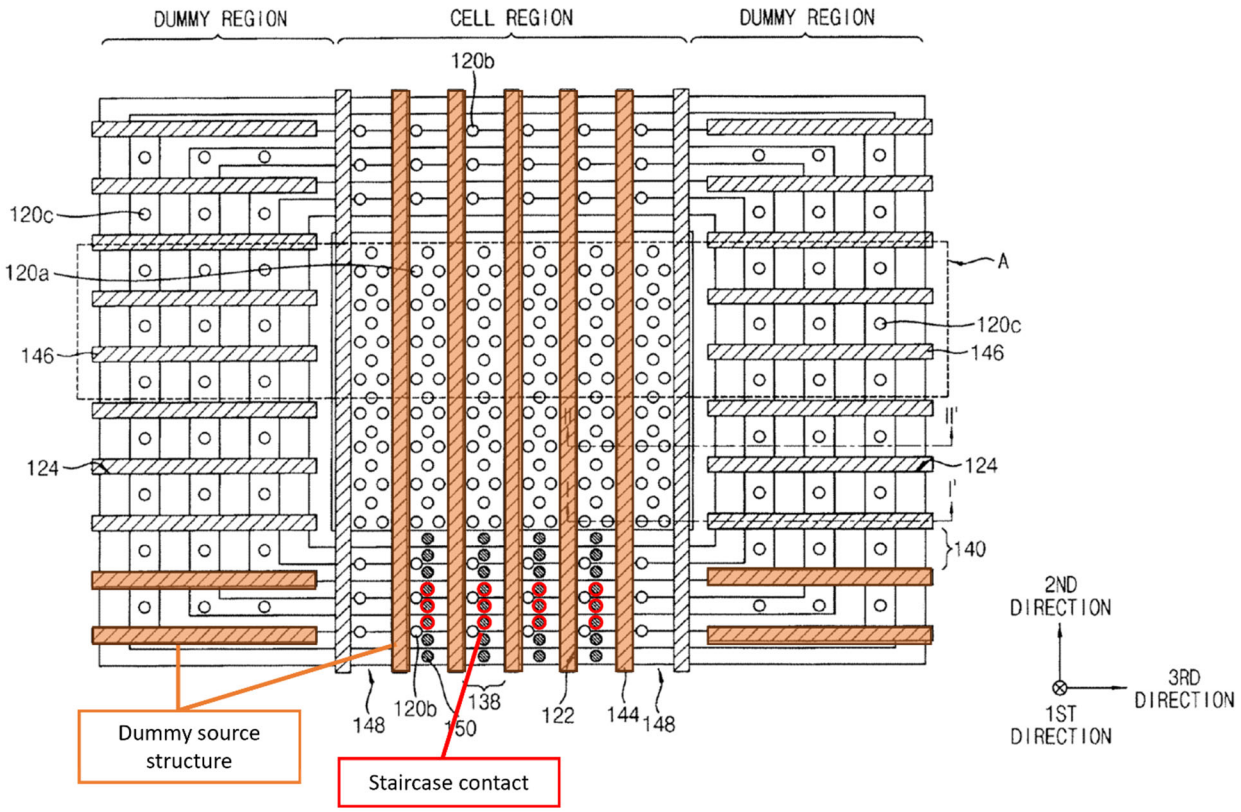
FIG. 13



Id., Fig. 13.

104. While I discuss this in greater detail in Section XIII.A.6, as shown below, the common source lines 144 (shown in orange in the first figure) and dummy source lines 146 (shown in orange in the second figure) surround the staircase contacts:

FIG. 1



Ex. 1005, Fig. 1 (annotated).

2. Tessariol (Ex. 1006)

105. Tessariol is a U.S. Patent Application Publication published on March 14, 2019.

106. Tessariol also relates to 3D NAND. Ex. 1006, [0006], [0027]. Tessariol refers to this device as construction 10 throughout its disclosures. *See generally id.*

107. Tessariol teaches the basic components of a 3D memory device, including a substrate, interleaved conductive gate lines and insulating layers (the

stack), and dummy components (e.g., that function as support members). Ex. 1006, [0027]-[0031], [0041].

108. Tessariol discloses dummy structures 60 and operative conductive vias 58 that function as support structures for the memory stack during the gate replacement process. Ex. 1006, [0027]-[0031], [0041]. These structures may be formed the same. Recall that with dummy structures, the structures may not be interconnected to upper-level interconnects, see Section X.A. Tessariol explains that the dummy structures 60 and operative conductive vias 58 include "an insulative lining 62 (e.g., silicon dioxide and/or silicon nitride) and a conductive core 64 (e.g., metal material)." *Id.*, [0038]. This structure is basically a conductive via and the liner insulates the conductive via from the gate layers. The dummy structures 60 and operative conductive vias 58 are formed in dummy structure openings 56 and via openings 54, respectively, which extend through a memory stack. *Id.*, [0037]-[0038]:

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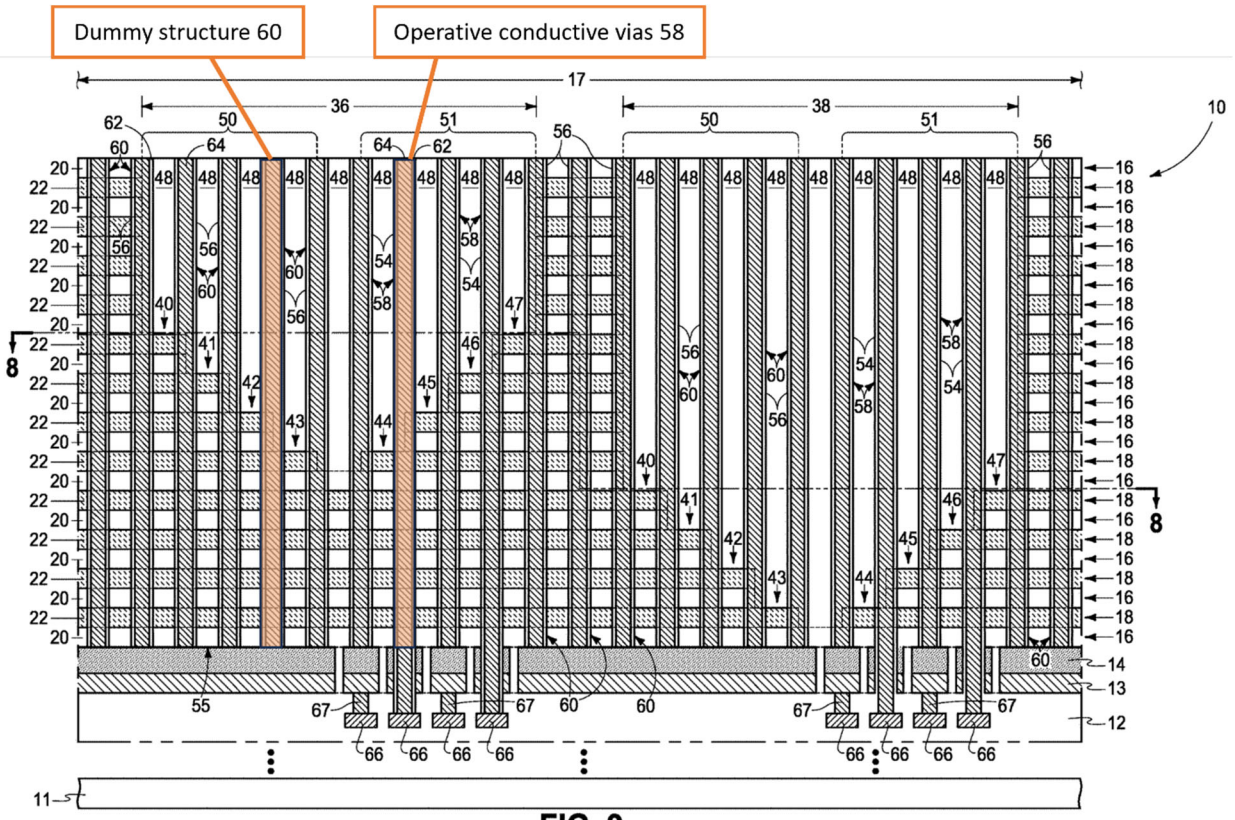


FIG. 9

Id., Fig. 9.

109. The dummy structure openings 56 and via openings 54 may be formed simultaneously. This saves time and process steps, because the holes may be formed with the same masking and etching steps. Ex. 1006, [0037]. Similarly, the respective dummy structures 60 and operative conductive vias 58 may also be formed simultaneously. *Id.*, [0037]-[0038]. Again, this saves time and process steps. Further, the dummy structures 60 and operative conductive vias 58 surround the staircase contacts (just like the '872 Patent embodiments). Shown below are four dummy structures 60 that surround a staircase contact.

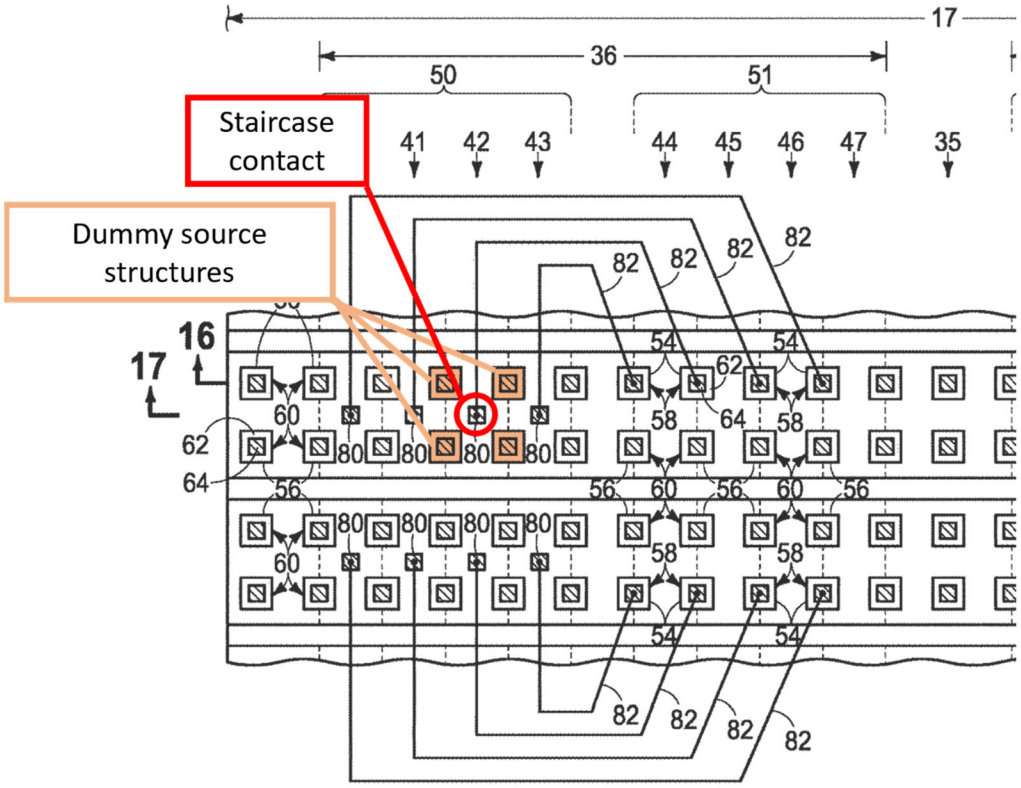


FIG. 15

Id., Fig. 15 (partial) (annotated).

XIII. GROUND 1: CLAIMS 1-6, 11, AND 13 ARE OBVIOUS OVER PARK

110. Ground 1 demonstrates that claims 1-6, 11 and 13 are obvious in view of Park when considered in view of the knowledge of a POSITA.

A. Claim 1

111. The figures from Park that are discussed below illustrate different views of a three-dimensional semiconductor device, and the manufacturing stages of the device. Figures 1-4 show different views (top plan view, perspective view, and cross-sectional views) of a three-dimensional semiconductor device, in which

memory cells are formed on the top surface of a substrate. Ex. 1005, 5:46-51. As I will discuss, some of these Figures do not illustrate the entire memory device. Figures 5-13 show the various manufacturing stages involved in forming the semiconductor device depicted by Figures 1-4. *Id.*, 9:29-37

1. [1.PRE] "A three-dimensional (3D) memory device, comprising:"

112. I offer no opinion on whether the preamble is or is not limiting. To the extent the preamble is limiting, Park discloses it.

113. Park discloses "[a] semiconductor device includes a substrate including cell and dummy regions …" Ex. 1005, Abstract. The cell region includes the memory strings. Park further discloses "[i]n example embodiments, a nonvolatile memory may be embodied to include a three dimensional (3D) memory array." *Id.*, 23:13-22.

114. Thus, Park discloses *a three-dimensional (3D) memory device*[4] (e.g., 3D semiconductor device with cell region).

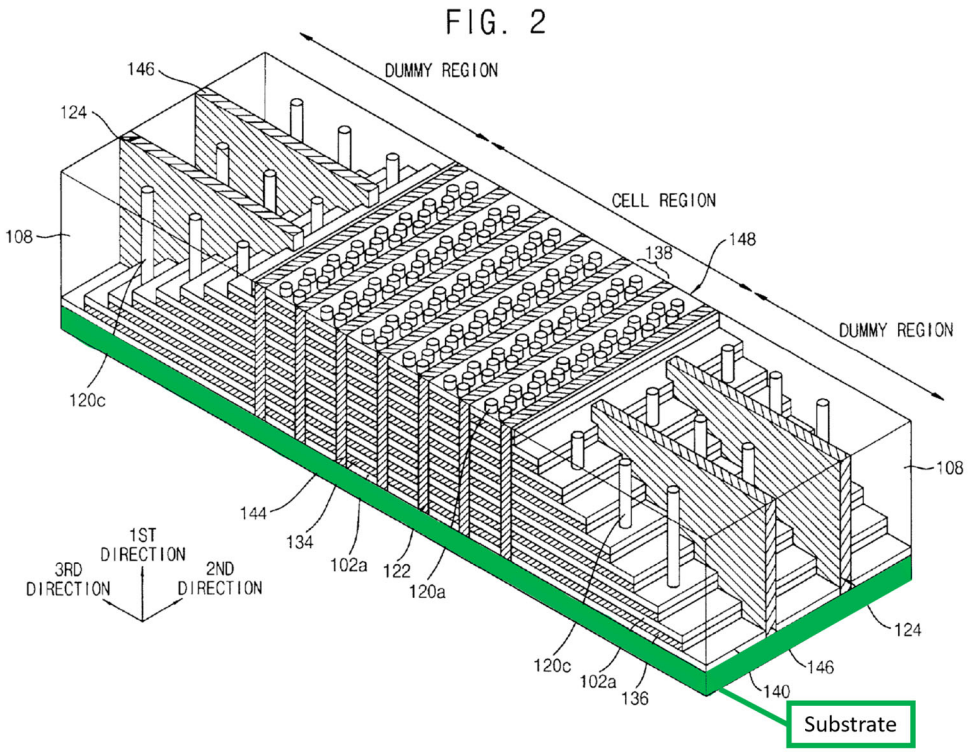
2. [1.A] "a substrate;"

115. Park discloses this limitation.

[4] In this Declaration, and in the claim mapping portion, I denote claim language using red and italics.

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116. Park discloses that "a semiconductor device may include a memory cell structure disposed on a cell region of a substrate 100." Ex. 1005, 6:1-4; *see also id.*, 23:15-22 ("[t]he 3D memory array may be monolithically formed on a substrate (e.g., semiconductor substrate such as silicon, or semiconductor-on-insulator substrate)."). This substrate is annotated in green below.



Id., Fig. 2 (annotated), *see also* Fig. 3 (showing a cross-section view of Fig. 2 and depicting a "substrate 100").

117. Thus, Park discloses a *substrate* (e.g., substrate 100).

3. [1.B] "a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;"

118. Park discloses this limitation.

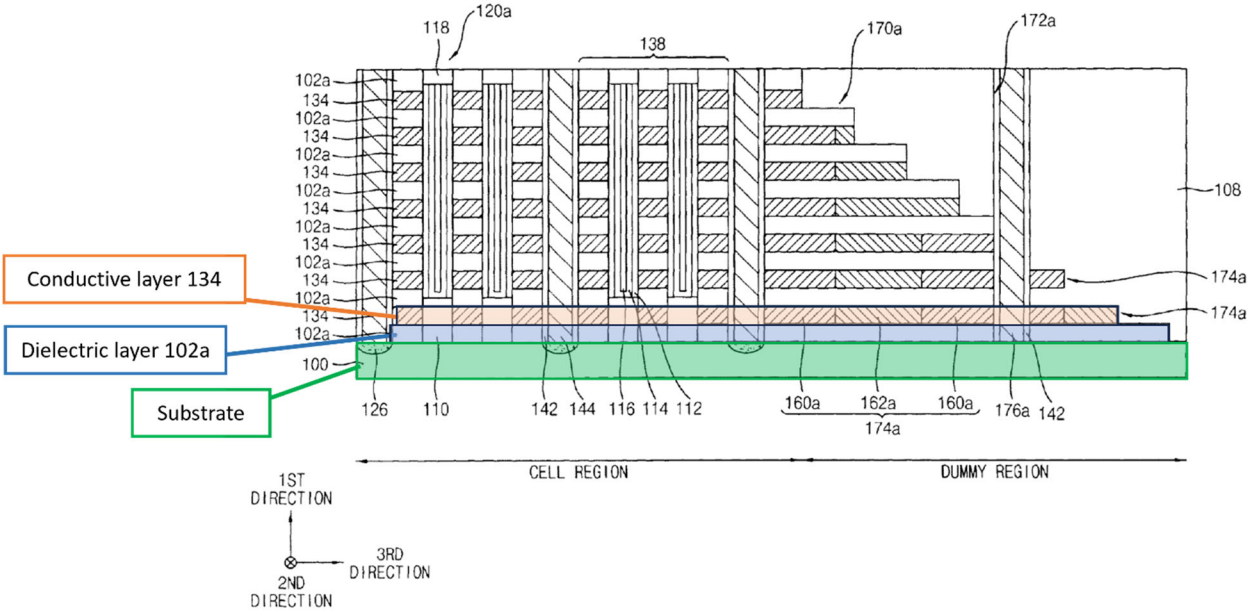
119. As an initial matter, this limitation refers to the conventional memory stack, that is, the stack of alternating gate layers and dielectric layers.

120. First, Park discloses conductive gate lines 134 that may include a metal, such as "tungsten (W), tungsten nitride, titanium (Ti), titanium nitride, tantalum (Ta), tantalum nitride, platinum (Pt), or the like." Ex. 1005, 7:6-10. Second, Park discloses that insulating interlayer patterns 102a are formed on the substrate 100, and act as an insulating layer between the gate lines 134, where the insulating layer 102a may be "a silicon oxide-based material." *Id.*, 7:19-22. Silicon oxide is a known dielectric. Ex. 1023, 85 (referring to such layers as "Inter Wordline Dielectric"). Third, Park discloses that these gate lines 134 (i.e., conductive layers) and insulating interlayer pattern 102a (i.e., dielectric layers) are alternately stacked or interleaved on the substrate. Ex. 1005, 7:23-31 ("The insulating interlayer patterns 102a and the gate lines 134 may be alternately stacked…"). In summary, Park discloses the basic stack of alternating gate and dielectric layers.

121. This memory stack is in the "cell region," which again, is where the active channel structures are located (that is, memory strings).

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FIG. 27



Ex. 1005, Fig. 3.

122. Thus, Park discloses *a memory stack comprising interleaved conductive layers and dielectric layers on the substrate* (e.g., in the cell region, layers 102a and 134, which is a stack on substrate 100).

4. [1.C] "a staircase structure on one side of the memory stack;"

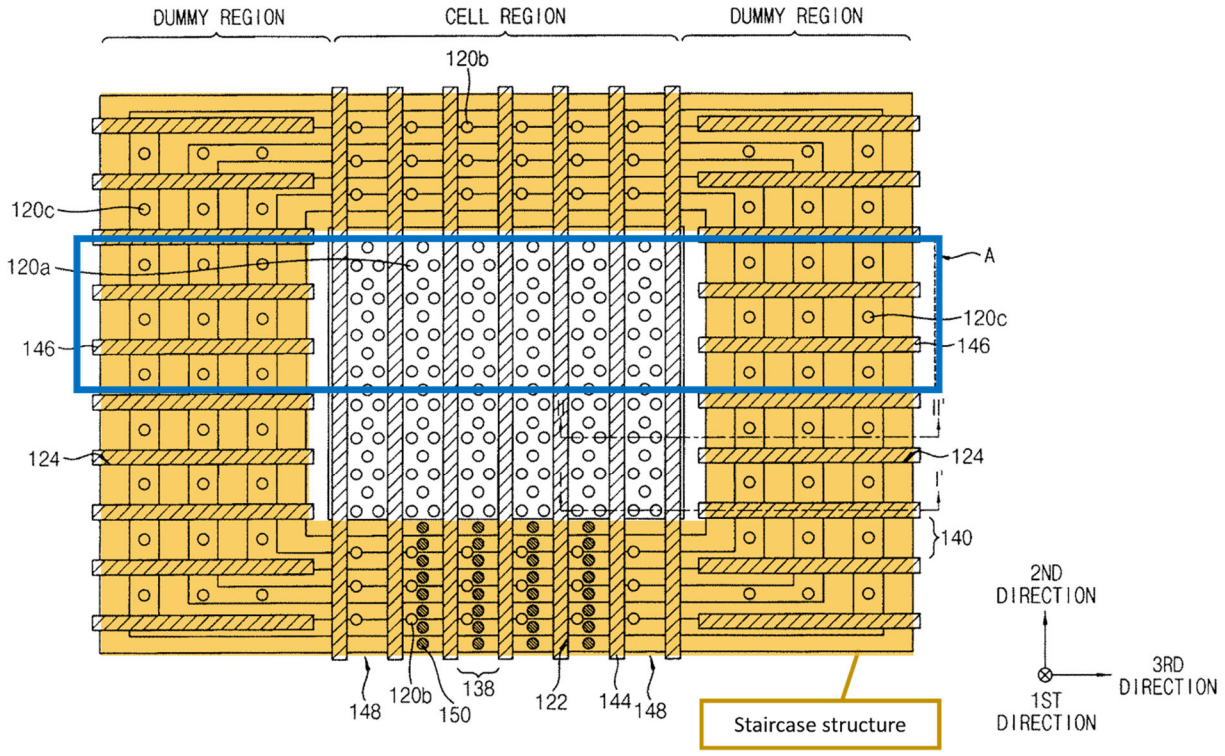
123. Park discloses this limitation.

124. As an initial matter, I discuss what staircase structures are in Section VIII. These are structures with stepped surfaces, which provide landing spots for vias that travel through the stack and connect to respective gate layers.

125. As shown in limitation [1.B], Park discloses a memory stack with staircase regions. Recall that Figure 2, however, was a partial view of the entire

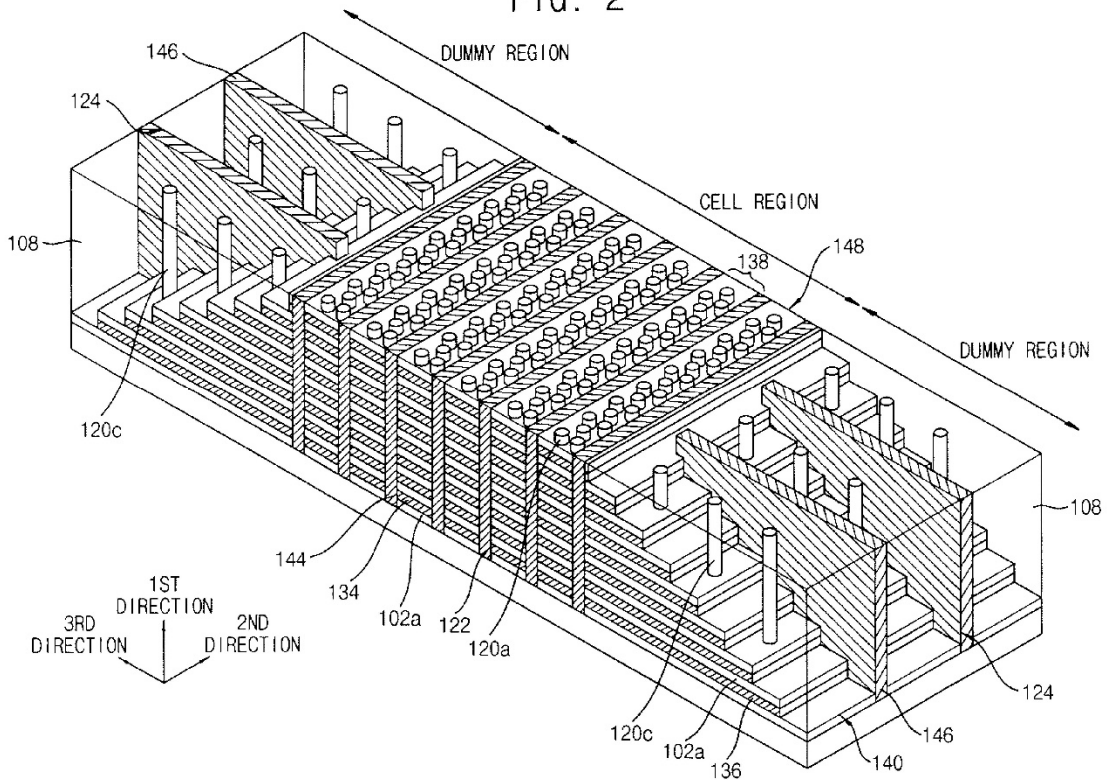
memory device. For context, the complete view of Park's device is shown in Figure 1 below:

FIG. 1



Ex. 1005, Fig. 1 (annotated). Park also discloses a cross section of area A (shown in the blue box above) of Figure 1 in Figure 2 below. As can be seen from above, this area A excludes the region in the second direction above and below the cell region:

FIG. 2



Id., Fig. 2, *id.*, 5:48-50 (stating Figure 2 shows area A of Figure 1).

126. As I describe below, the stairstep region is the entire orange-colored region in Figure 1 above. Ex. 1005, Fig. 2, 7:25-27, 9:43-46.

127. First, in discussing the manufacturing of the stack, Park refers to the memory stack as "first structure 138." Ex. 1005, 7:23-31. Park explains: "[t]he first structure 138 may extend in the second direction. Both lateral portions of the first structure 138 in the second direction may serve as a wiring region and have a stepped shape." *Id.*, 7:25-27. Here, Park is disclosing that the region above and below in the second direction are staircase regions. Indeed, the wiring portion requires the stepped surfaces for the word line contacts. *See* Section VIII. Further, Park discloses

that "[a] central portion of the first structure 138 which may not have the stepped shape may serve as a main cell region, and the lateral portion having the stepped shape may serve as the wiring region." *Id.*, 7:32-35. Thus, the main cell region, which includes the active channel structures, is surrounded by the staircase region.

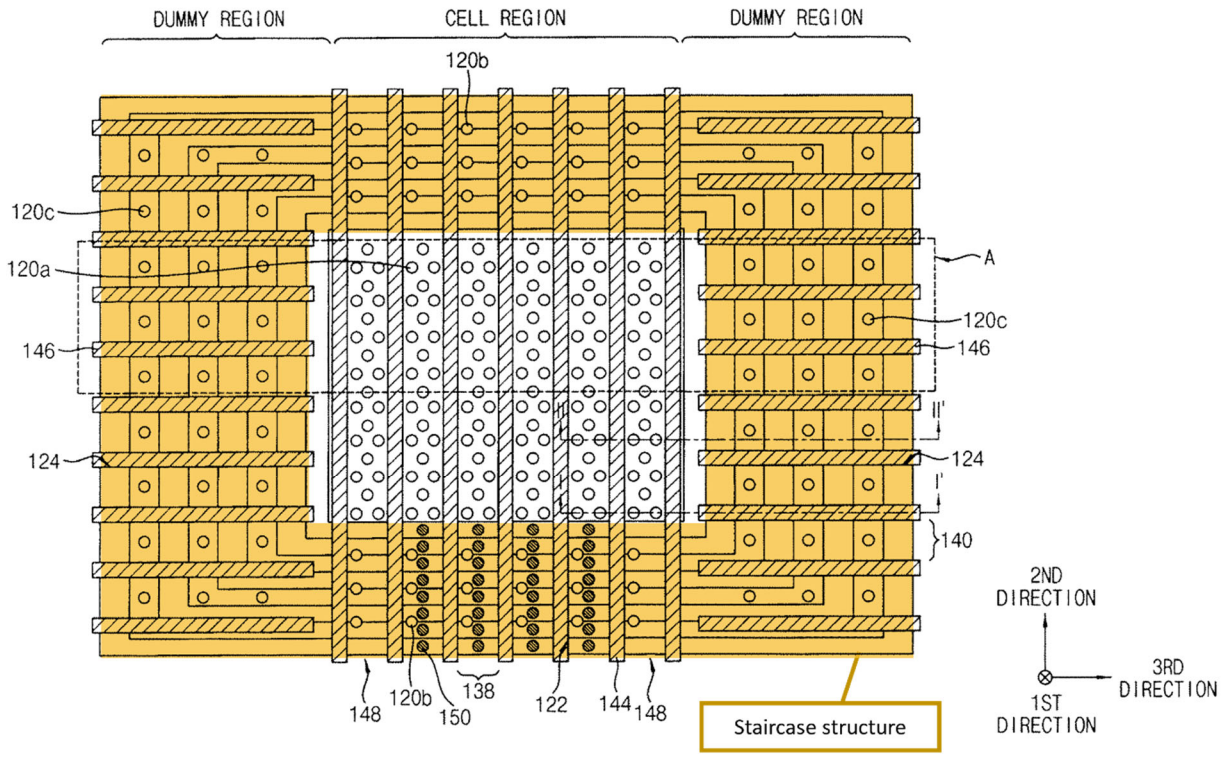
128. Second, in discussing the manufacturing of the stack, Park refers to the resulting structure after the gate replacement process as the "mold structure 106." Ex. 1005, 9:38-46. Park explains that "[e]nd portion of the mold structure 106 in the second and third directions may have stepped structures." *Id.*, 9:43-46. And Park explains again "[a] portion of the mold structure 106 on the cell region may include stepped structures at both end portions in the second direction." *Id.*, 10:7-10. Thus, again, the main cell region, which includes the active channel structures, is surrounded by the staircase region.

129. Third, as I discuss under limitation [1.D], the word line contacts, which extend down to steps of a staircase structure, are in the second direction of the main cell area. Ex. 1005, 7:32-37. I discuss how word line contacts extend to steps in a staircase region in Section VIII.

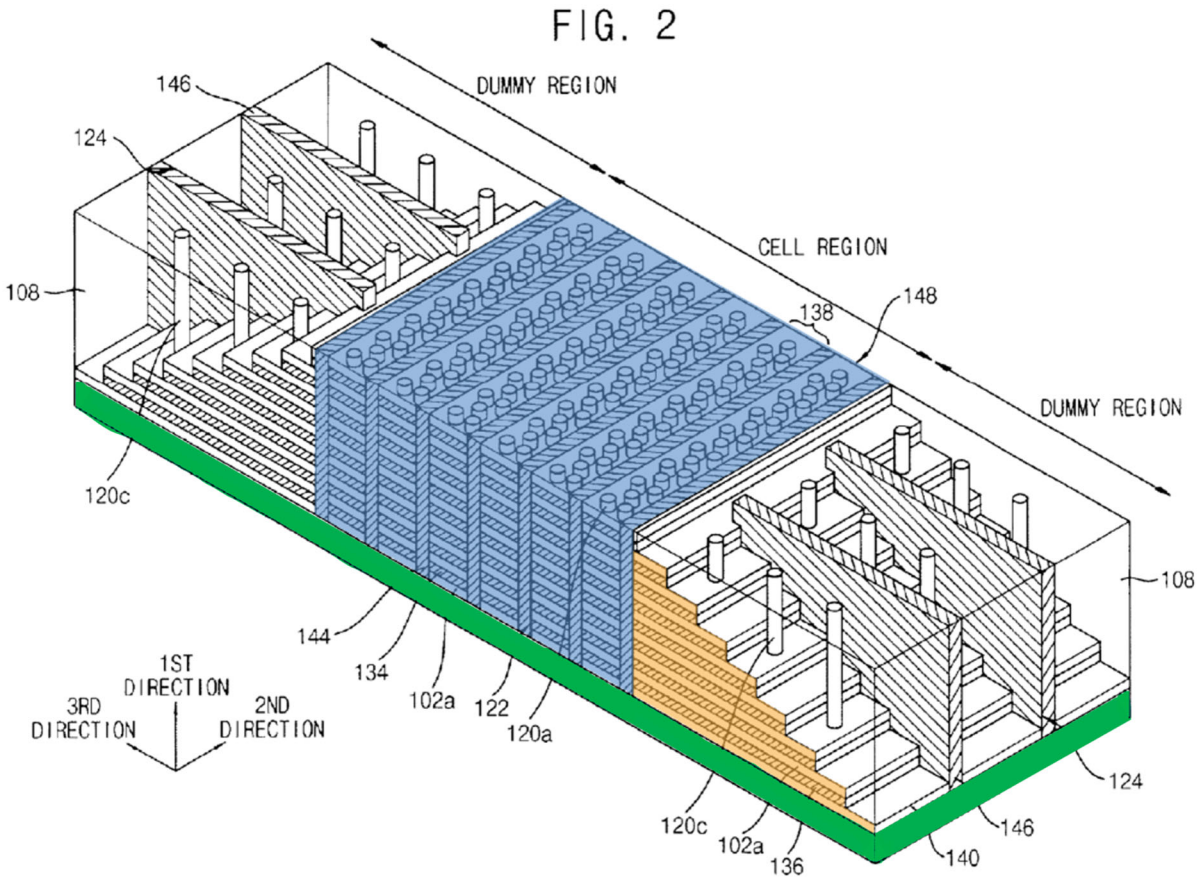
130. Accordingly, annotated Figure 1 below marks in orange all portions of the memory stack with a stepped shape – the lateral portions in the second direction and the dummy region in the third direction.

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FIG. 1



131. Annotated Figure 2 below shows a perspective view of an exemplary "stepped structure" in the third direction. The same, or similar, stepped region exists in the wiring region as discussed above:



Id., Fig. 2 (annotated).

132. Thus, Park discloses *a staircase structure on one side of the memory stack* (e.g., the stepped regions on each side of the main cell region).

5. [1.D] "a staircase contact in the staircase structure; and"

133. Park discloses this limitation or at least renders it obvious.

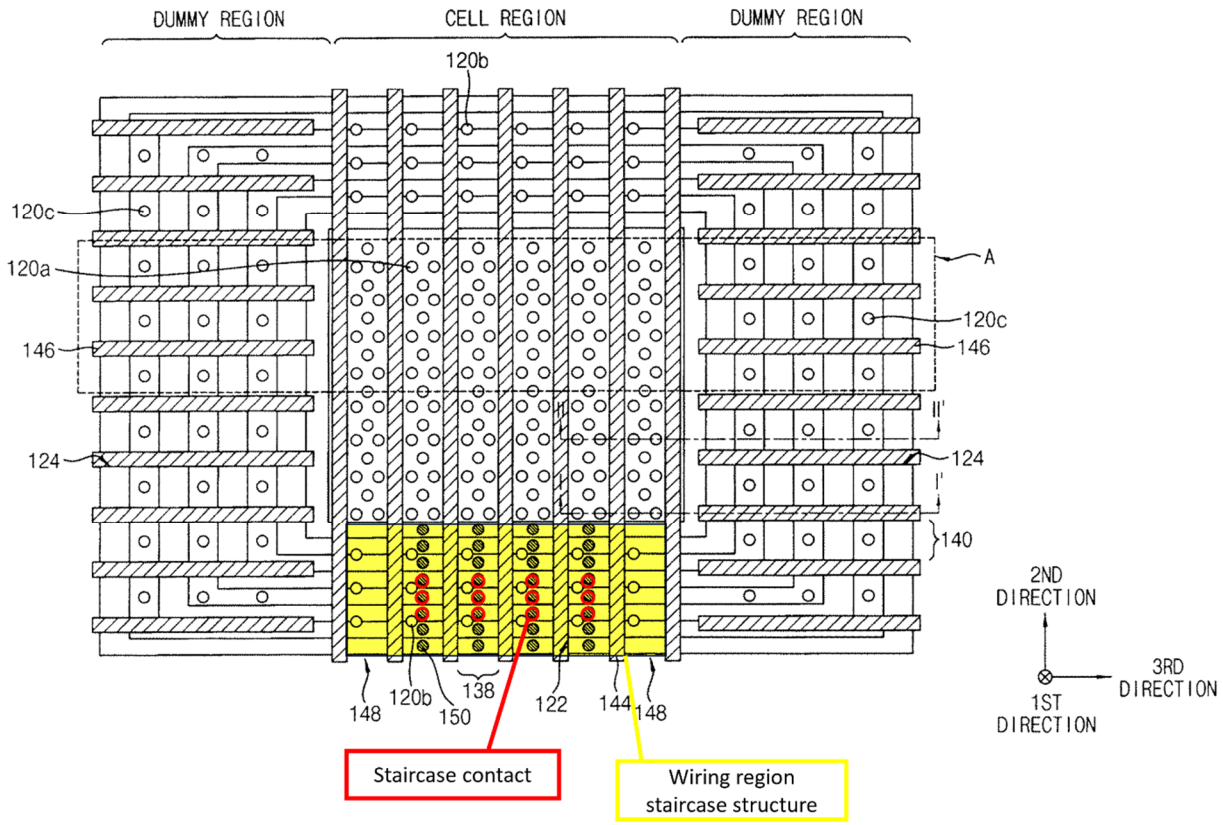
134. As I discussed in limitation [1.C], Park discloses a "staircase structure" in the second direction to the main cell region (as shown in yellow below, in the second direction with respect to figure 2), i.e., the wiring region. Ex. 1005, 7:33-35. In this wiring region, there are interconnects to individual gate lines: "[T]he lateral

portion having the stepped shape may serve as the wiring region. The **wirings may include contact plugs 150 that may be in contact with gate lines 134**, and conductive lines electrically connected to the contact plugs 150." *Id.*, 7:32-37 (emphasis added). In other words, these contact plugs extend down towards the gate layers, and respective plugs contact respective gate layers. The gate layers are also known as word lines. These contacts provide for control of the word lines for, e.g., program and read operations.

135. Thus, in the staircase structure, there are *staircase contacts* (contact plugs 150) that extend and contact the individual steps of the staircase structure. Annotated Figure 1 below illustrates the contact plugs 150 (in red) and the wiring region (in yellow).

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FIG. 1



Ex. 1005, Fig. 1.

136. To the extent that PO argues that Park does not disclose a staircase region in the main wiring area, I disagree. But in any event, it would have at least been obvious to have one for several reasons. First, while Park does not depict the wiring region in Figure 2 as having a staircase profile, I illustrate that Park describes the wiring region as having a staircase region in Section XIII.A.4. Second, Park describes contacts to the gate lines in this wiring region. As I explain in Section XIII.A.4, the region that includes contacts to the gate lines is a staircase region,

because the staircase structure provides landing spots for the gate (word line) contacts. *See* Section VIII. Implementing such staircase regions was routine. *See* Section VIII. In fact, staircase structures were conventional, as it is a fundamental structure for the word line contact. And Park already etches one, as shown in Figure 2, which was a routine that involves trimming the stack layers to create the stepped surfaces.

137. Thus, Park discloses, or renders obvious, *a staircase contact* (e.g., contact plug 150) *in the staircase structure* (e.g., step structure in wiring area).

6. [1.E] "a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact,"

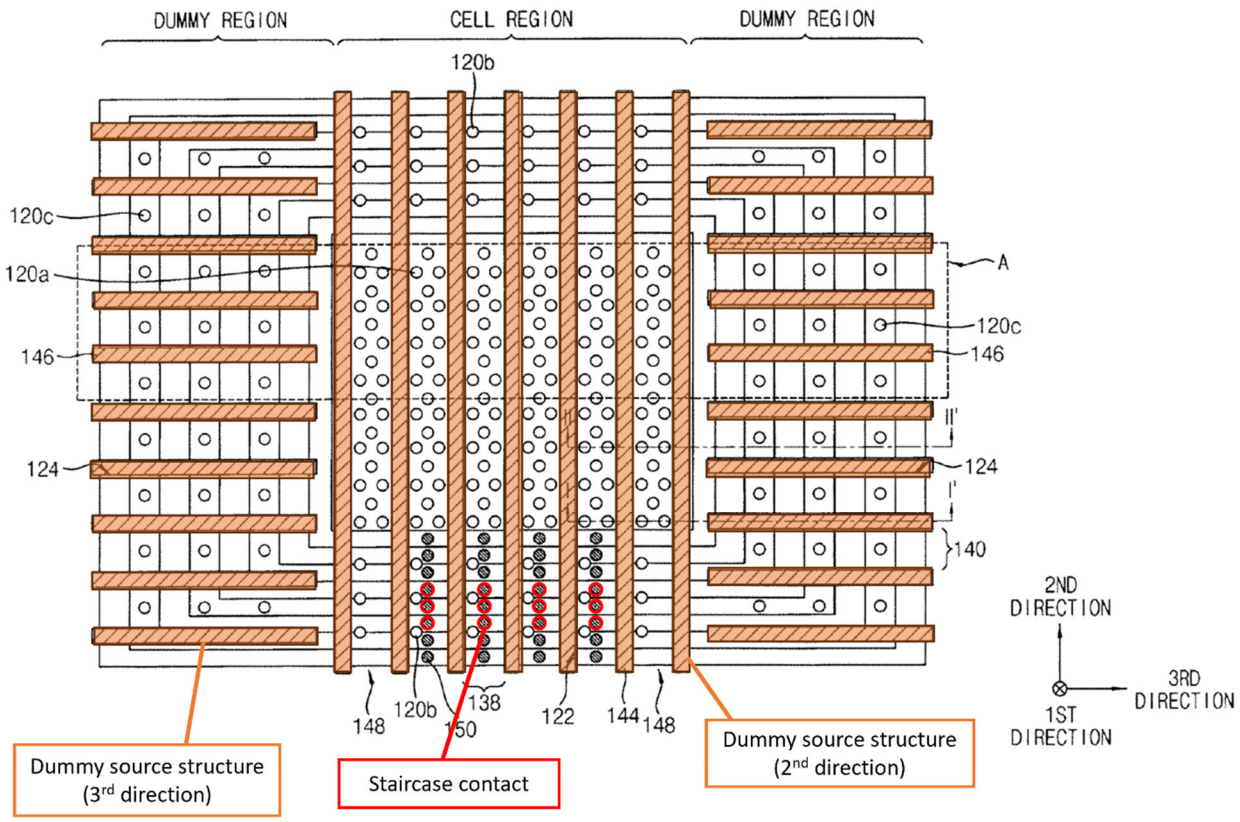
138. Park discloses this limitation under both parties' constructions.

139. Petitioner's construction is "structure that occupies the void that was used for the gate replacement process," and PO's apparent interpretation does not require that the structure occupy the void that is used for the gate replacement process. *See* Section X.A.

140. First, as to *a plurality of dummy source structures*, Park's common source lines 144 and dummy source lines 146 are *a plurality of dummy source structures*, because these are structures "that occup[y] the void that was used for the

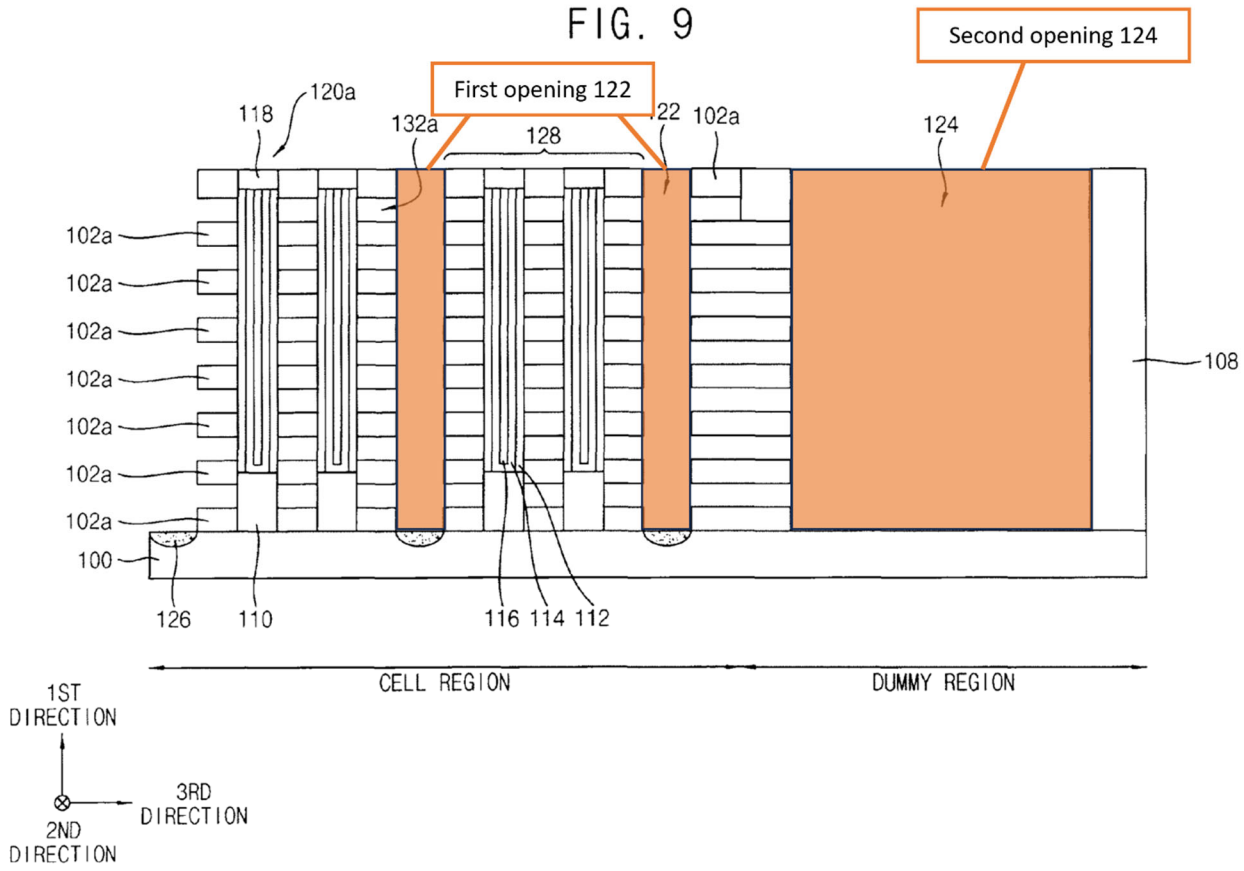
gate replacement process." *See* Section X.A. Annotated Figure 1 below shows, in orange, the position of the common source lines 144 and dummy source lines 146.

FIG. 1



Ex. 1005, Fig. 1 (annotated).

141. During the gate replacement process, first openings 122 and second openings 124 are etched in the memory stack. Ex. 1005, 11:66-12:4, Fig. 9. Note that a mask would be used to only etch to form the first and second openings. These openings are shown below:



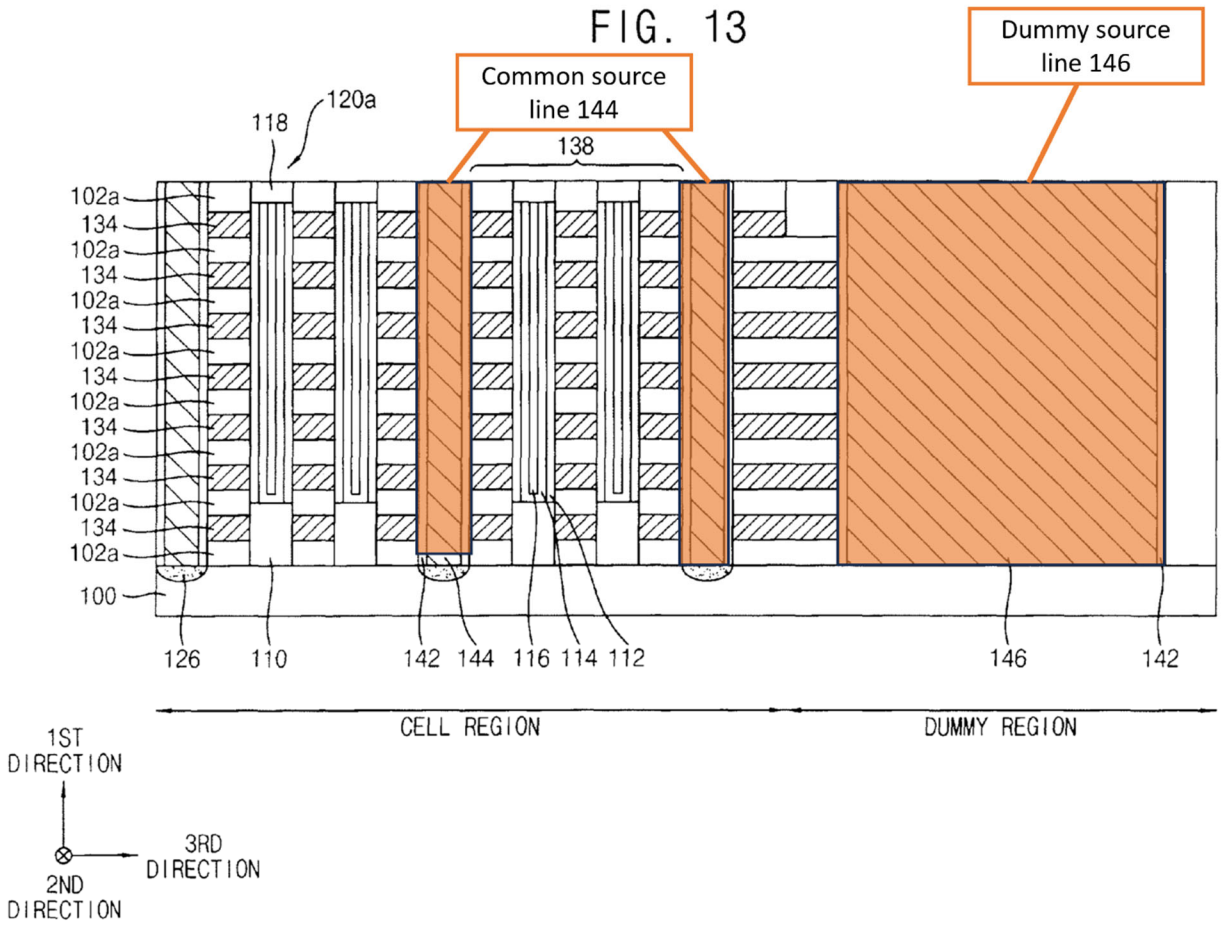
Id., Fig. 9 (annotated).

142. In the gate replacement process, the etch occurs through these voids: "[r]eferring to FIGS. 9 and 10, the sacrificial patterns 104a exposed through the first and second openings 122 and 124 may be removed to form first gaps 132a and second gaps 132b. In example embodiments, the sacrificial patterns 104a may be removed by a wet etching process using, e.g., phosphoric acid and/or sulfuric acid as an etchant solution. … Referring to FIGS. 11 and 12, gate lines 134 may be formed in the first gaps 132a, and dummy patterns 136 may be formed in the second gaps 132b." Ex. 1005, 12:44-13:5.

143. After the gate replacement process, the first opening 122 and the second opening 124 are each lined with an insulating layer. This electrically isolates the subsequently-deposited cores from the gate layers. After the lining is deposited, the holes are filled with conductive material to form a common source line 144 and a dummy source line 146, respectively. Ex. 1005, 13:39-41 ("The CSL 144 and the dummy source line 146 filling the first opening 122 and the second opening 124, respectively, may be formed"); *see also* 7:63-64 ("The CSL 144 may be in the first opening 122…"), 13:50-59 (same), 14:67-15:1 ("The dummy source line 146a may be disposed in the second opening 124a…"). Again, a common source line connects an upper-level source connection to areas of the substrate.

144. Annotated Figure 13 below shows the filling of the first opening 122 and the second opening 124, in orange, with conductive material to form the common source line 144 and the dummy source line 146 (in orange).

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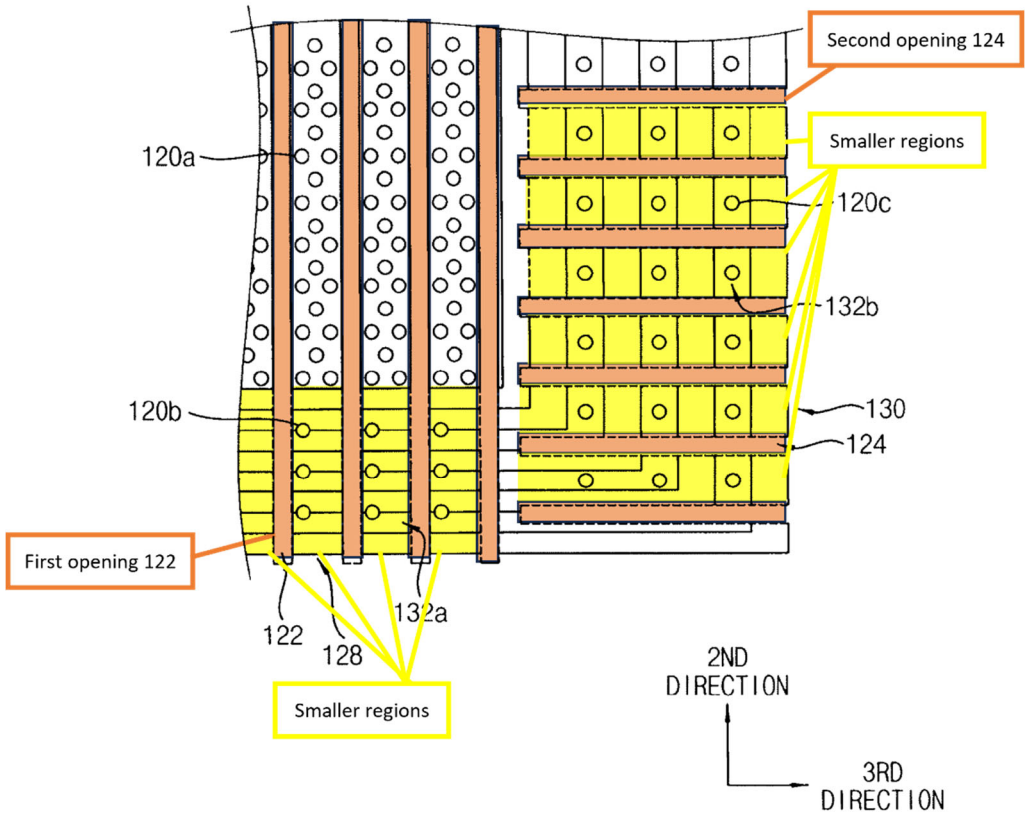


Ex. 1005, Fig. 13 (annotated).

145. I have compared Park's *dummy source structures* to certain exemplary embodiments of the '872 Patent, and they are almost identical *dummy source structures*. The '872 Patent states that "dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks." Ex. 1001, 11:44-46. This refers to a structure that may appear as a wall that extends lengthwise in the 3rd direction and extend in the 1st direction as well, separating the memory array. Park's common source lines 144 and dummy source

lines 146 have this shape and separate the array. Park describes this separation by referring to the structures "cut[ing]" the stack. Ex. 1005, 12:5-18; *see also* 6:15-18 ("The CSL 144 may extend through the gate lines 134, and may extend in the second direction. The CSL 144 may serve as a cutting line intersecting the gate lines 134"). Park uses the word "cut" because the structures cut through the stack and separate the stack into smaller units. This is shown below in annotated Figure 10:

FIG. 10

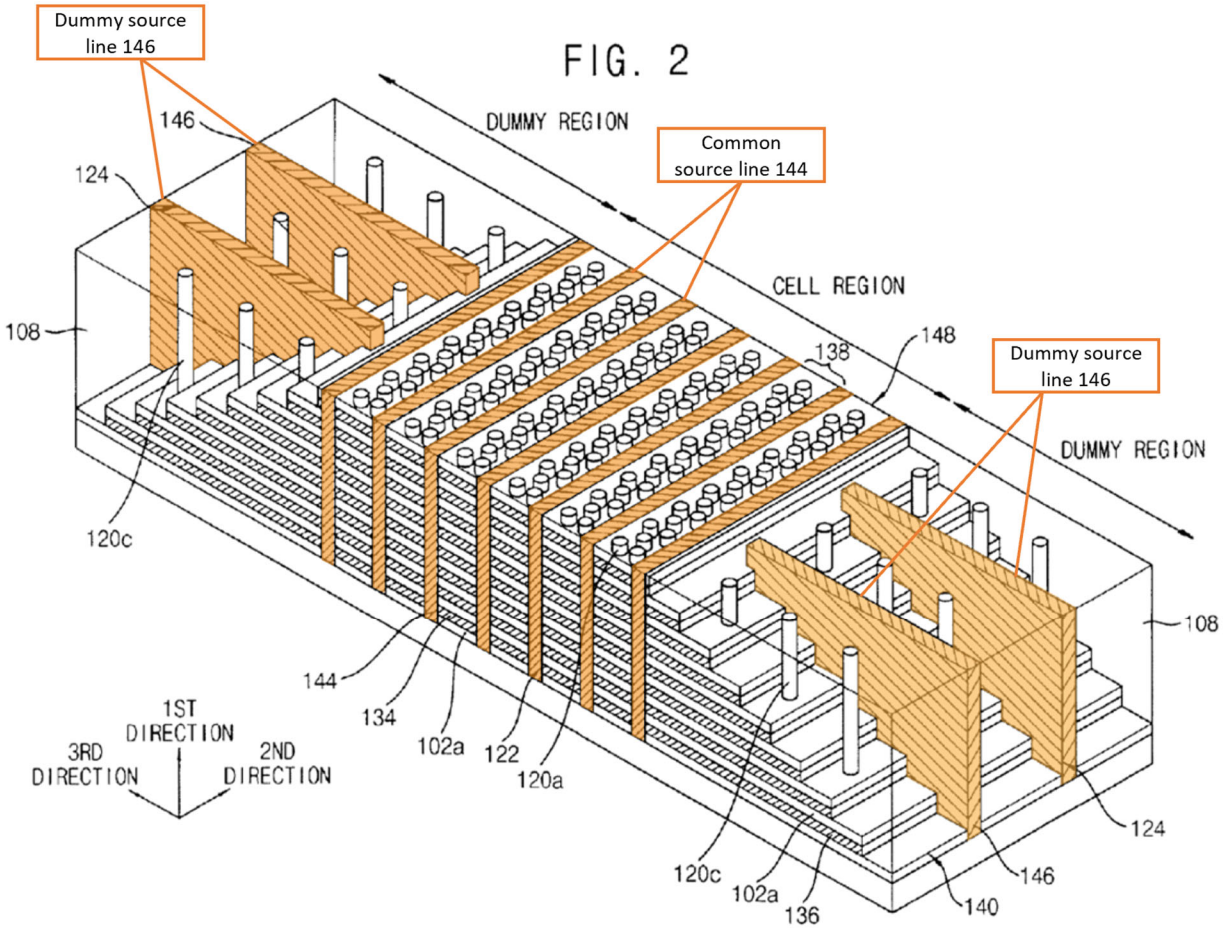


Ex. 1005, Fig. 10 (annotated).

146. As to a further structural point, the '872 Patent explains that "dummy source structures" can "contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices." Ex. 1001, 5:41-43, 16:63-66. In other words, the dummy source structures may serve to interconnect an upper-level element (source connection) and portion of the substrate (creating a common source region). The common source lines 144 in Park are an interconnect for a source connection. Ex. 1005, 7:63-64 ("The CSL 144 may be in the first opening 122…").

147. Next, as to the portion of the limitation that states *each extending vertically through the staircase structure*, Park discloses that both the common source line 144 and dummy source line 146 *extend[] vertically through the stepped region* (i.e., "staircase structure"):

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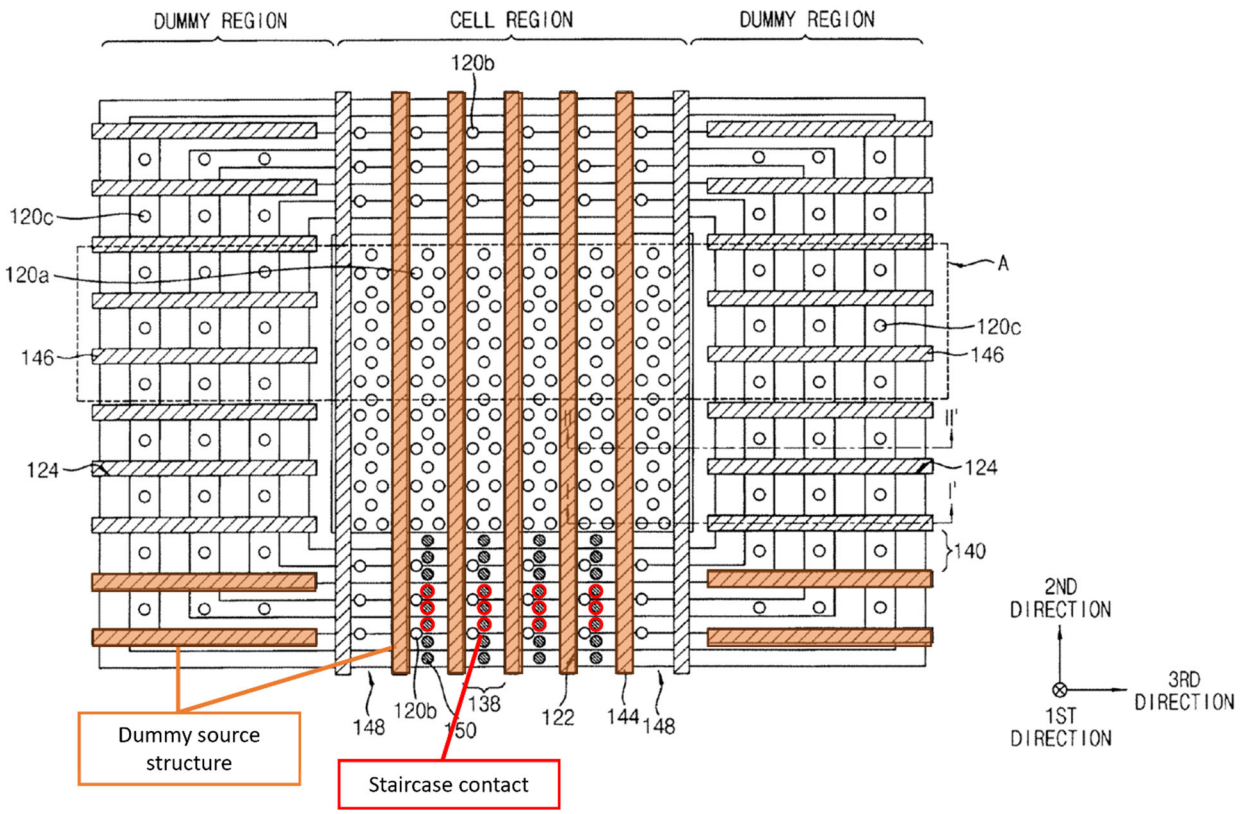
Ex. 1005, Fig. 2 (annotated); *see also id.*, Figure 13. This is consistent with all of Park's embodiments. *See, e.g., id.*, Fig. 19, Fig. 21, and Fig. 26 (showing different embodiments of common source line 144 and dummy source line 146 configurations that all extend vertically through the staircase structure.). Again, these structures may "cut" the stack, i.e., separate the stack. *Id.*, 12:5-18, *see also* 6:15-18. This creates smaller units because the gate lines are local to a particular unit and do not extent into multiple units.

148. Third, as to portion of the limitation that recites *the plurality of dummy source structures surrounding the staircase contact*, the '872 Patent does not use "surround" to mean fully and continuously encircling as I describe in Section X. As I demonstrate there, in all embodiments of the '872 Patent, the dummy source structures to not fully and continuously encircle the staircase contact. *E.g.*, Ex. 1001, Fig. 1A (dummy source structures 124 do not fully surround word line contacts 122); *see also* Section VII.B. Rather, there are large gaps between the dummy source structures.

149. Park discloses a *staircase contact* (contact plugs 150), and the common source line 144 and the dummy source line 146 (*dummy source structures*) both surround the contact plugs 150 (i.e., *staircase contacts*). Note that common source lines 144 alone surround the *staircase contacts*, and that is all that is necessary to satisfy claim 1.

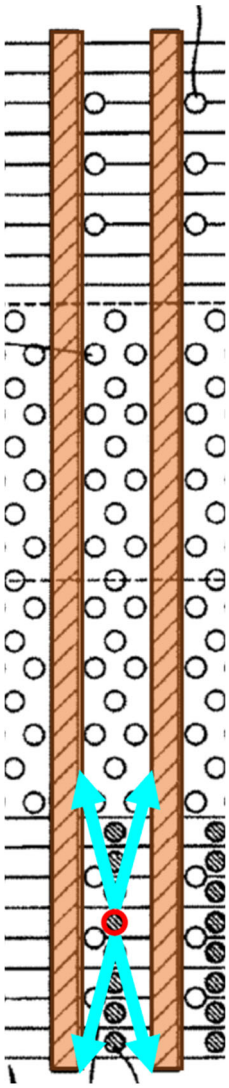
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FIG. 1



Ex. 1005, Fig. 1.

150. One way to "surround" in view of the '872 Patent is when drawing four lines (each equally radially spread out), each line will intersect one of the *dummy source structures*. *See* Section X. In Park, two of the *dummy source structures surround* a *staircase contact* in this way. When drawing such lines from the *staircase contact* at approximately 45, 135, 225, and 315 degrees, each line intersects a *dummy source structure*:

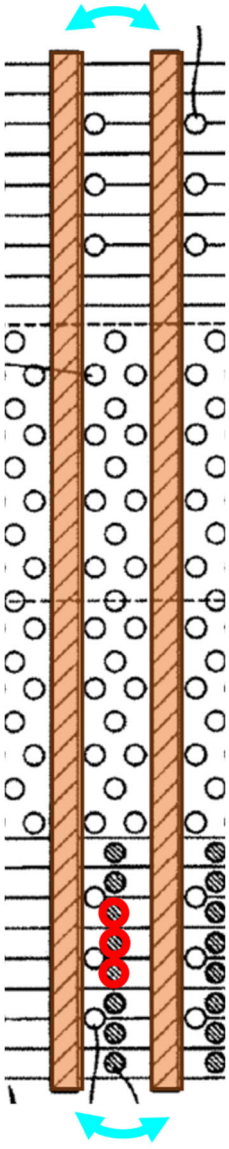


151. Note that the actual angles are merely a matter of perspective. If one were to define the orientation as 0 degrees extending half way between west and north, the points of intersection would be at approximately 0, 90, 180, and 270 degrees.

152. From another perspective, one could consider the gaps in the radial border. *See* Section X. Here, two of the *dummy source structures* create a larger

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angular border around the *staircase contact* than the '872 Patent (which uses four *dummy source structures*).



153. I also note that it would be inaccurate if the Patent Owner were to argue that Park's dummy source structures only surround the staircase contacts on two sides. There are only small gaps in the radial border, and just like the '872 Patent, in the above figure a line from the contact intersects a dummy source structure at

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four different angles separated by 90 degrees (e.g., 45, 135, and 225, and 315 degrees). But I would disagree with Patent Owner for the additional reason that an object may be surrounded by structures on two sides, just like an isthmus is surrounded on two sides by water or like a nitride layer is surrounded on two sides by oxide layers in an ONO dielectric structure.

154. Thus, Park discloses *a plurality of dummy source structures* (e.g., common source lines 144 and dummy source lines 146) *each extending vertically through the staircase structure* (e.g., through the stairstep regions), *the plurality of dummy source structures surrounding the staircase contact* (e.g., contact plugs 150).

7. [1.F] "wherein each of the dummy source structures comprises a conductive contact."

155. Park discloses this limitation.

156. First, the '872 Patent provides an example of a *contact* of uniform vertical conductive member that extends down towards the substrate, *i.e.*, *contact* need not be a separate element on top of a conductive member. For example, sometimes the word "contact" is used to refer to an element that sits on the top of another element and is placed there so another element can connect to it. But the '872 Patent explains that "[a]s illustrated in FIG. 2L, ***a contact 244*** is formed within spacer 242 in dummy source hole 212 (shown in FIG. 2K). ***Contact 244*** can be formed by depositing conductive materials including, not limited to W, Co, Cu, Al,

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polysilicon, silicides, or any combination thereof, over spacer 242 in the dummy source hole using one or more thin film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof. ***A dummy source structure 246 including spacer 242 and contact 244*** is thereby formed in the dummy source hole, surrounded by a plurality of dummy channel structures 209." Ex. 1001, 16:21-32 (emphasis added). As shown below, the "contact" is simply a fill of conductive metal (246) into a hole (212) with an insulating liner (242). This is a conductive via that provides a conductive path through the stack (with an insulating liner):

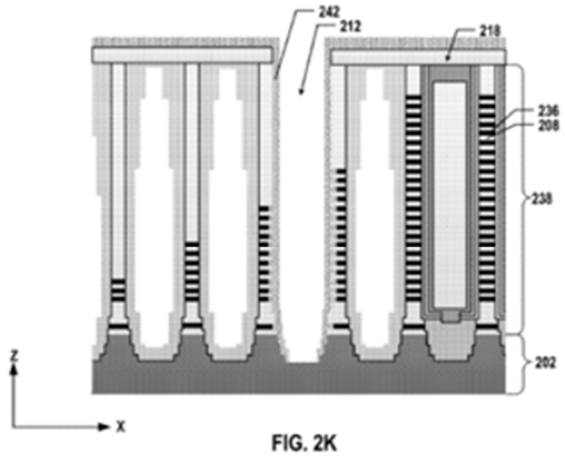


FIG. 2K

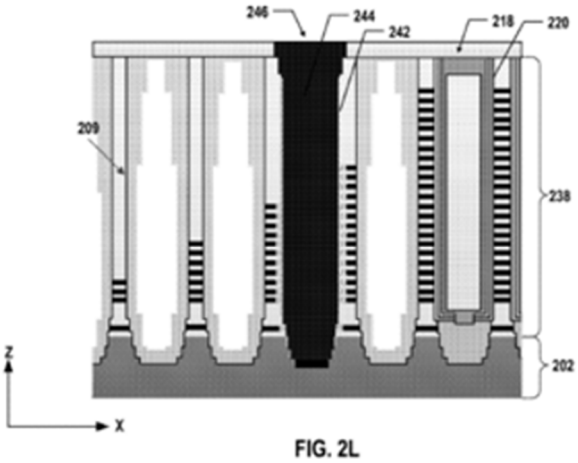


FIG. 2L

Id., Figs. 2K, 2L.

157. Park's common source line 144 and dummy source line 146, i.e., *dummy source structures*, comprises *a conductive contact* just like the '872 Patent,

namely, each includes conductive core that extend through the stack. *See* Ex. 1005, 1:63-65 ("In example embodiments, the dummy lines may include a conductive material the same as that included in the cutting lines."); 7:65-67 ("The CSL 144 may include a metal having a low resistance, e.g., W, Ti, Ta, Pt, etc. …"); 3:23-24 ("The dummy source lines and the common source lines may include a same conductive material."). *See also* Limitation [1.E] (describing the common source line 144 and dummy source line 146 "cut" through the stack).

158. Thus, Park discloses *wherein each of the dummy source structures comprises a conductive contact* (e.g., a metal or other conductive material).

B. Claim 2

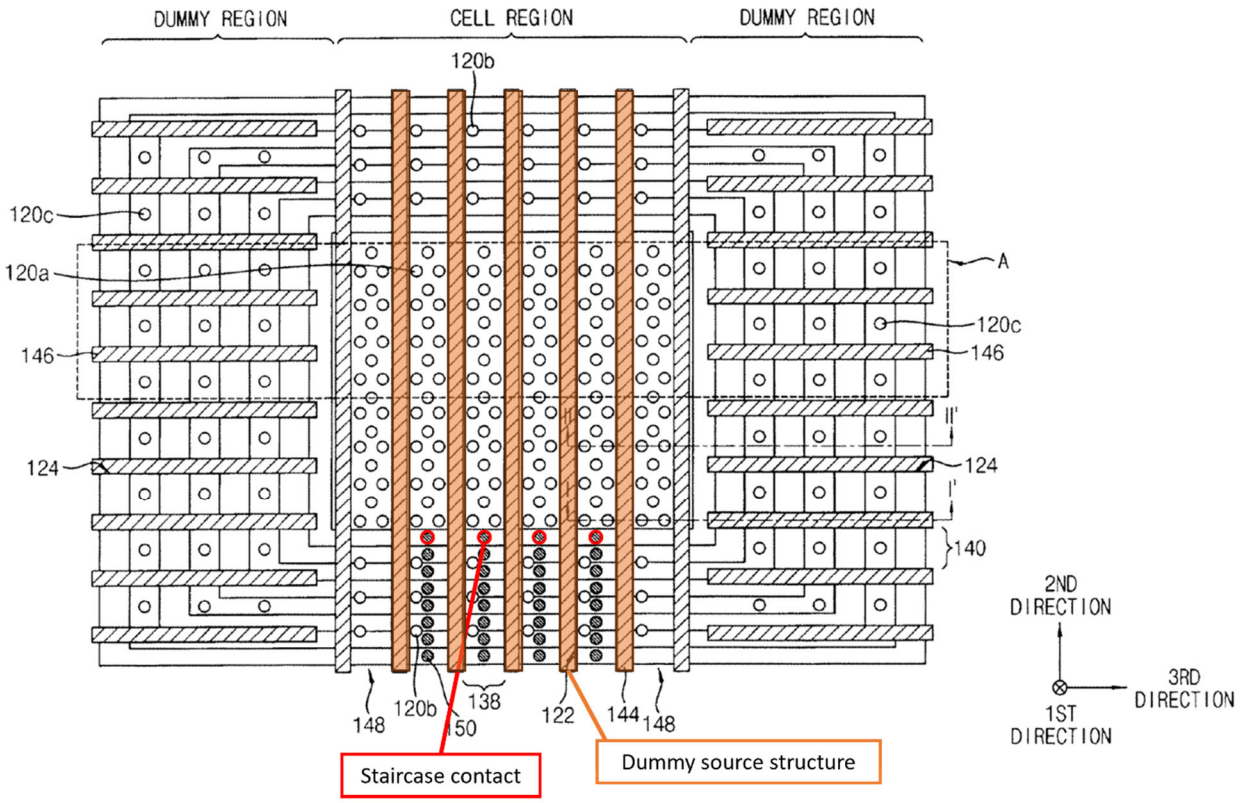
1. [2] "The 3D memory device of claim 1, wherein the plurality of dummy source structures are located adjacent to the staircase contact."

159. Park discloses this limitation.

160. As I discuss in [1.E], Park discloses both dummy source lines 146 and common source lines 144 as *dummy source structures*. For this claim mapping, the *dummy source structures* are the plurality of common source lines 144, which also surround the staircase contacts (*see* limitation [1.E]). The *staircase contacts* are the top row (in the second direction) of *staircase contacts*. As shown below, the plurality of common source line 144 (in orange) are located adjacent to the contact plugs 150 (i.e., *staircase contacts*) (shown in red).

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FIG. 1



Ex. 1005 (annotated), Fig. 1.

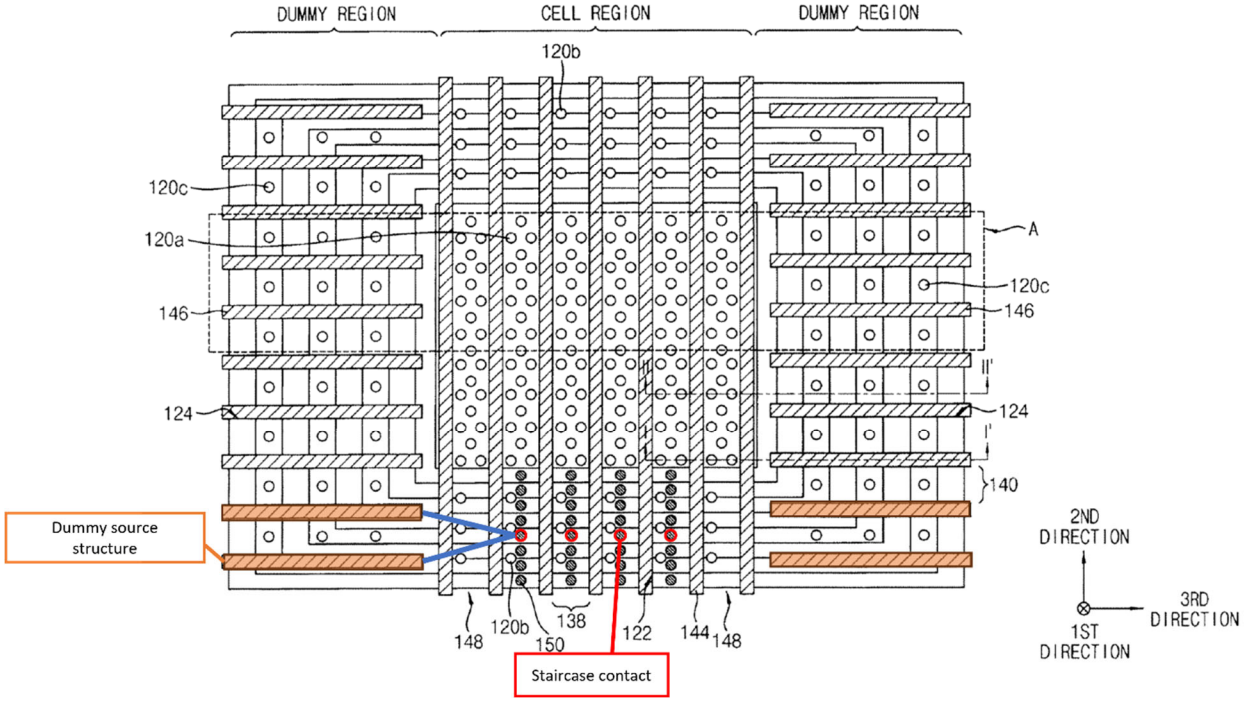
C. Claim 3

1. [3] "The 3D memory device of claim 1, wherein at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact."

161. Park discloses this limitation.

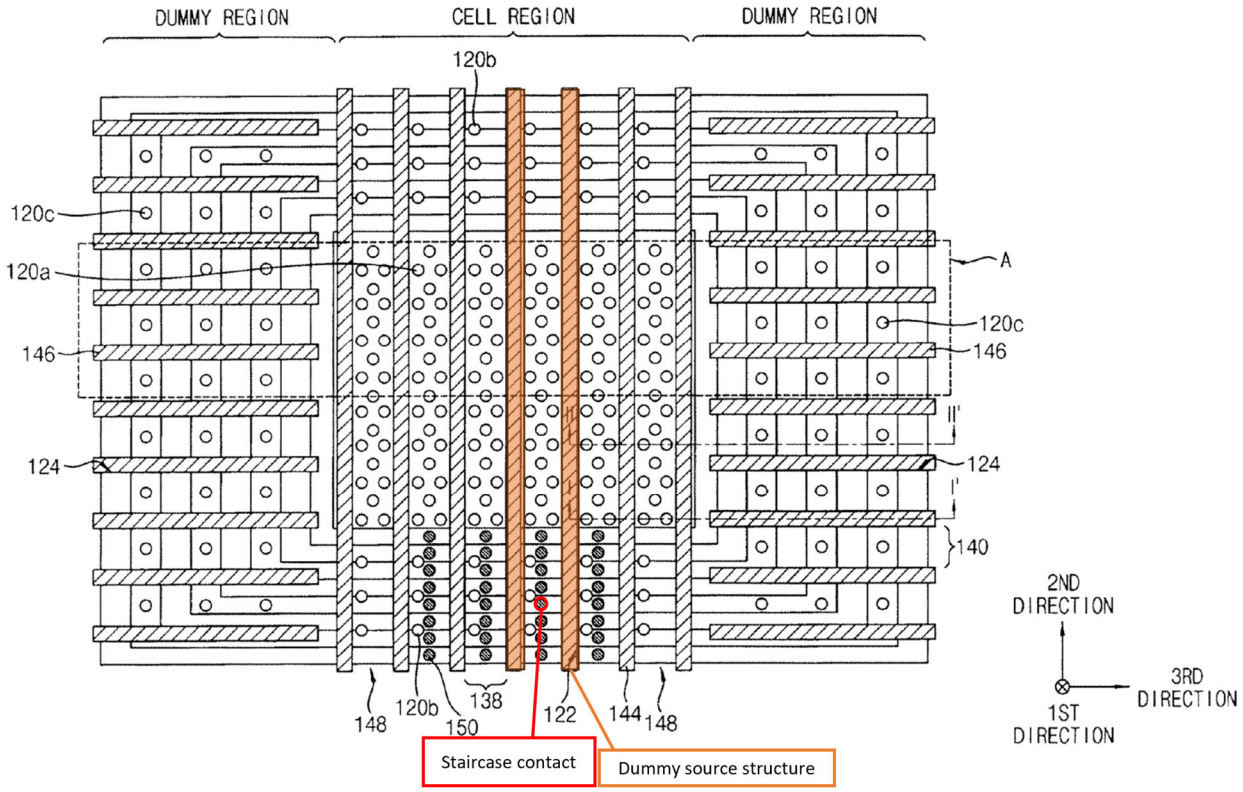
162. Nominally equal lateral distances to, in the context of the '872 Patent, includes being "evenly or uniformly distributed." Ex. 1001, 6:48-50. As shown below, the dummy source lines 146 are positioned nominally equal lateral distances to the contact plugs 150 (i.e., staircase contact).

FIG. 1



Ex. 1005 (annotated), Fig. 1. Similarly, two of the common source lines (which may be the *plurality of dummy source structures*) are *of nominally equal lateral distances to the staircase contact*, e.g., two that surround one contact (here, *the staircase contact*).

FIG. 1



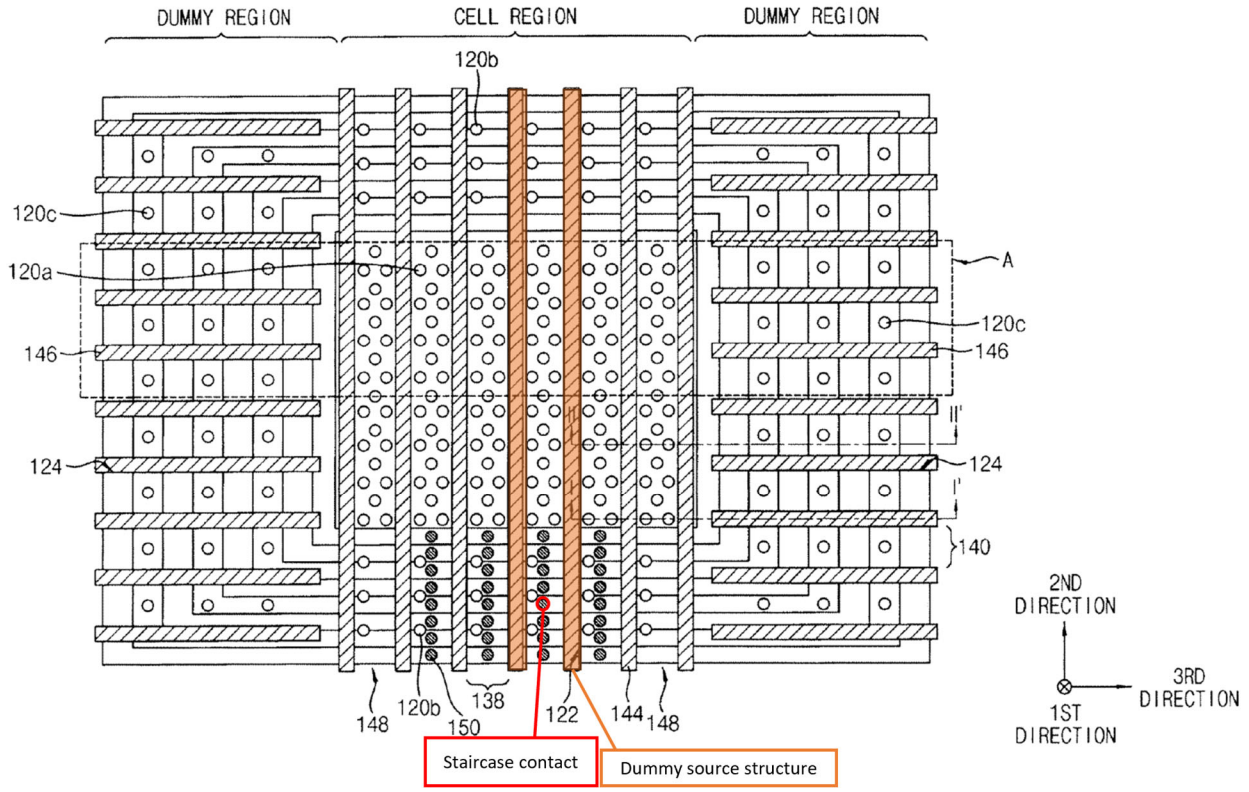
Id., Fig. 1 (annotated).

D. Claim 4

1. [4] "The 3D memory device of claim 1, wherein the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact."

163. As I discuss in claim [3], Park discloses "the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact." As shown below, when *the plurality of dummy source structures* are two common source lines and when the *staircase contact* is one contact, the common source lines both surround and are of nominally equal lateral distances to that staircase contact.

FIG. 1



Ex. 1005 (annotated), Fig. 1.

E. Claim 5

1. [5] "The 3D memory device of claim 1, wherein in a plan view, at least two of the plurality of dummy source structures are arranged in a first row that extends along a first lateral direction."

164. Park discloses this limitation.

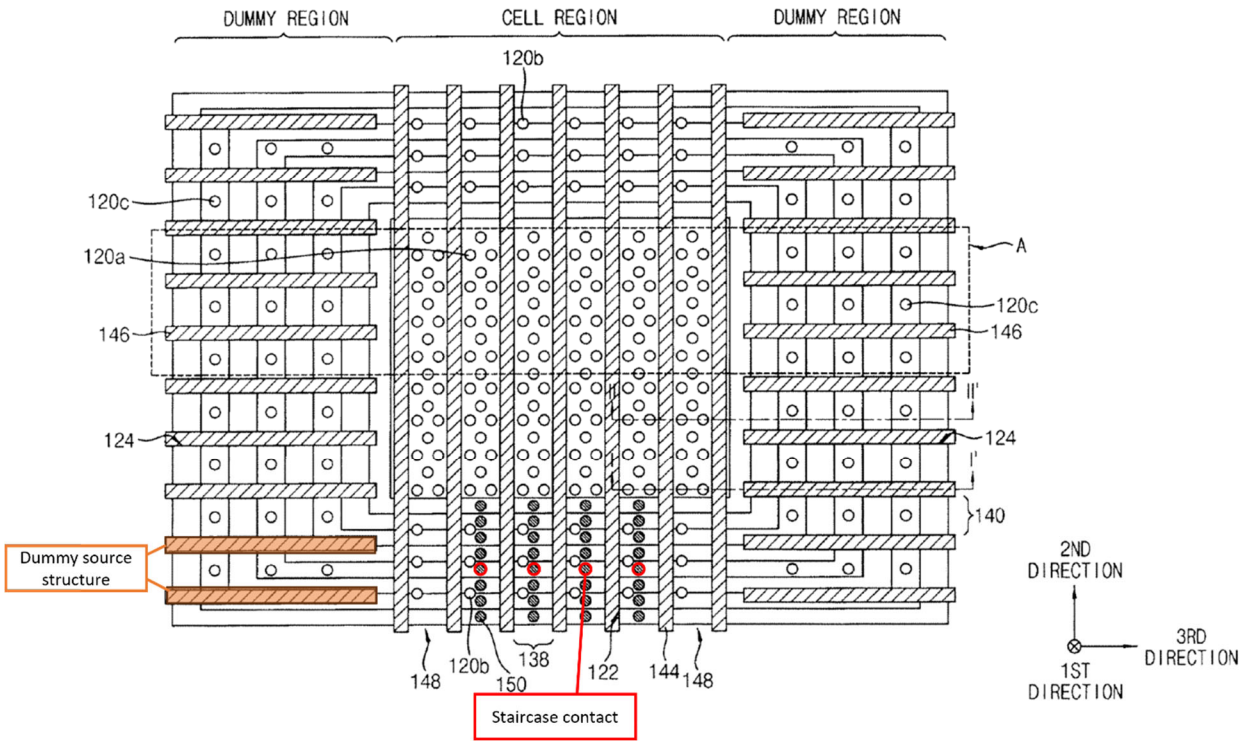
165. Plan view refers to a top-down view. That is, imagine looking from above the device in a downward direction.

166. Also note that a row is "a number of objects arranged in a usually straight line." (https://www.merriam-webster.com/dictionary/row). A row need not

extend west to east (or east to west). A row can be along any "straight line." The '872 Patent confirms this because two rows can be in the X and Y directions. Ex. 1001, 6:53-58.

167. As shown below, there are at least two of the plurality of dummy source structures (in orange) arranged in a first row that extends along a first lateral direction (i.e., "north to south" or "2nd direction" indicated in Fig. 1). *See* Ex. 1005, 26:26-29.

FIG. 1



Id., Fig. 1 (annotated).

168. The above row is like a row of match sticks repeating along a line traveling from north to south.

169. Note that the *plurality of dummy source structures* includes all of the *dummy source structures* of Park such that they *surround the staircase contacts*.

F. Claim 6

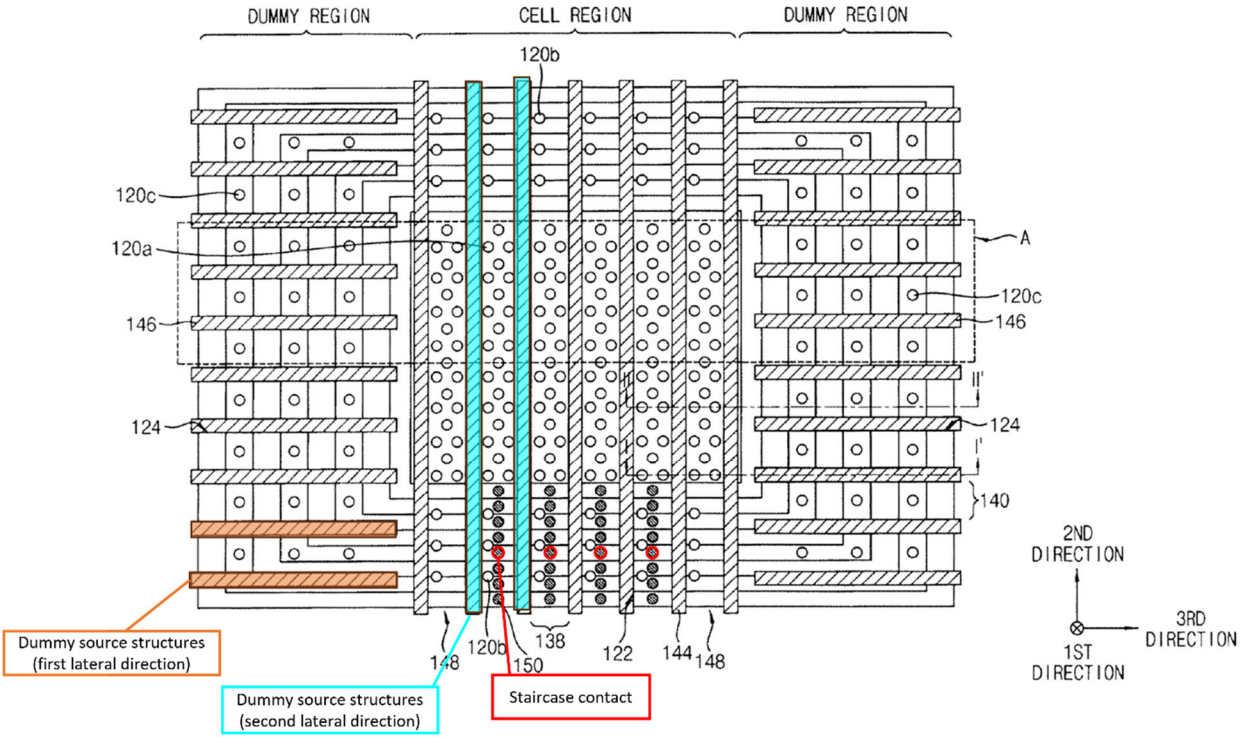
1. [6] "The 3D memory device of claim 5, wherein in the plan view, at least two other dummy source structures are arranged in a second row that extends along a second lateral direction perpendicular to the first lateral direction."

170. Park discloses this limitation.

171. As shown below, two dummy source lines in orange are arranged in a first row that extends along a first lateral direction (north to south direction or 2nd direction in Figure 1). And two common source lines in teal are in a second row that extends along a second lateral direction perpendicular to the first lateral direction (namely, from west to east or 3rd direction in Figure 1). The second row is like a series of a match sticks in the west to east direction.

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FIG. 1



Ex. 1005 (annotated), Fig. 1. Note that the *plurality of dummy source structures* includes all of the *dummy source structures* of Park such that they *surround the staircase contacts*.

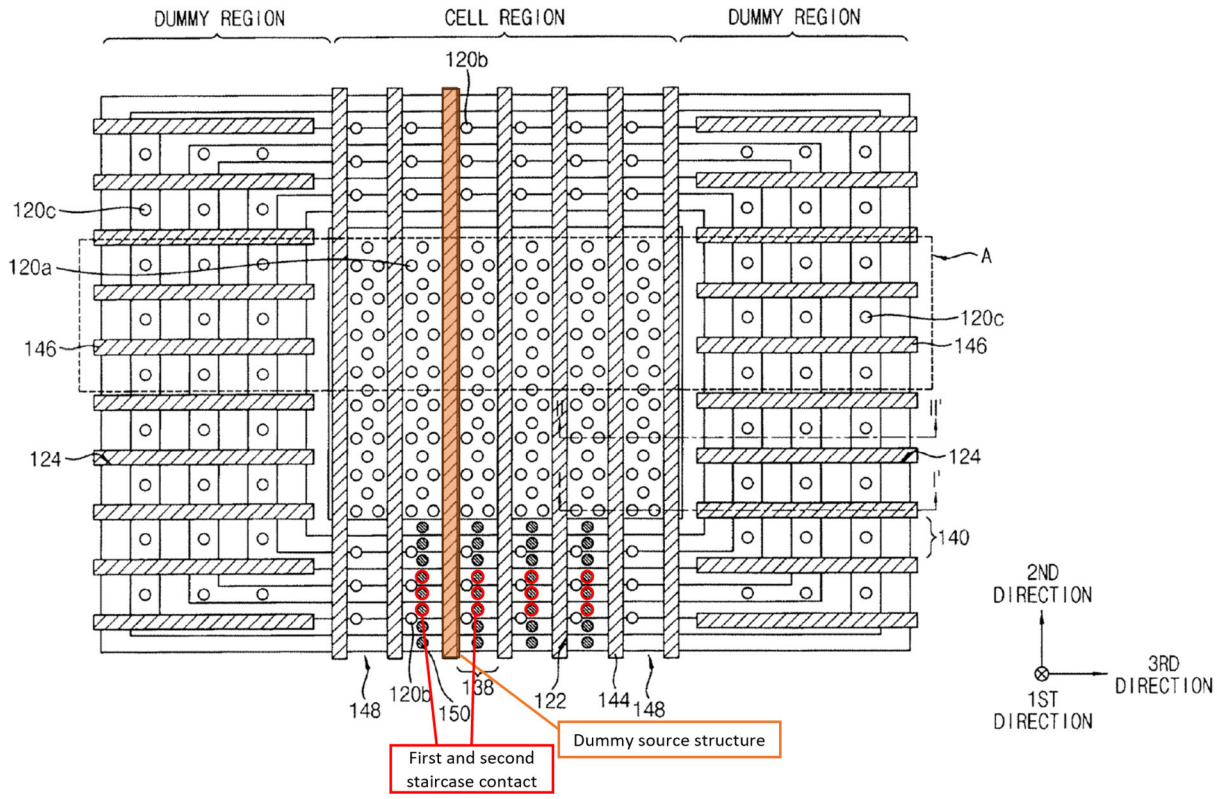
G. Claim 11

1. [11] "The 3D memory device of claim 1, comprising first and second staircase contacts, wherein at least one dummy source structure is located between the first and second staircase contacts."

172. Park discloses this limitation.

173. As shown below, the first and second contact plugs 150 ("staircase contact") in red, and at least one common source line 144 (i.e., "dummy source structure") in orange, that is located between the first and second staircase contacts.

FIG. 1



Ex. 1005 (annotated), Fig. 1.

H. Claim 13

1. [13] "The 3D memory device of claim 1, wherein the conductive contact comprises a conductor layer, and wherein the at least one dummy source structure further comprises a spacer surrounding the conductor layer along a sidewall of the conductor layer, the spacer comprising a dielectric material."

174. Park discloses, or at least renders obvious, this limitation.

175. Recall that after the first opening 122 and second opening 124 are formed, "an insulation layer may be formed conformally on sidewalls and bottoms of the first and second openings 122 and 124." Ex. 1005, 13:42-46. This insulation layer is formed on the sidewalls. It acts as a spacer between the conductive core and the memory stack. It is necessary because the gate layers are conductive. Thus, without the spacer, there would be electrical shorts between the conductive core and the gate layers. Thus, the dummy source structure comprises a *spacer surrounding the conductor layer along a sidewall of the conductor layer, the spacer comprising a dielectric material*.

176. The insulator layer would have been understood to be a dielectric material. Park consistently describes its insulators as being made with dielectric materials. Ex. 1005, 6:50-53, 7:19-22, 9:47-51, 10:16-20. And this is for good reason, in the semiconductor context, the term insulator layer, particularly an insulating liner layer, is understood as a dielectric material, such as silicon oxide.

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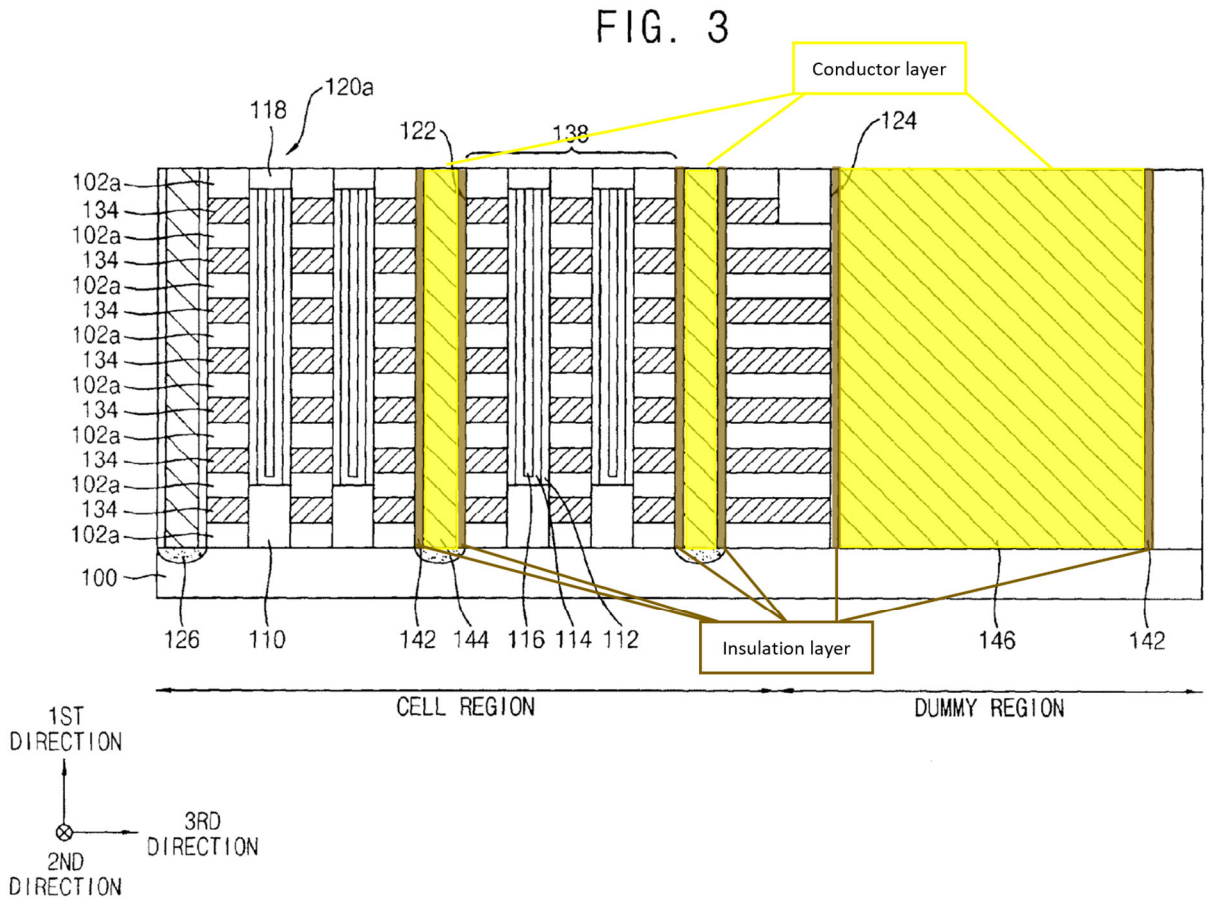
This is because silicon dioxide is one of the most common insulators in the field with high breakdown voltages and low leakage current, and which can be deposited at low temperatures by ALD, CVD or PECVD. Further the use of dielectric materials, such as silicon oxide, was advantageous because of its compatibility with semiconductor processing. For this application, the silicon dioxide will be deposited by chemical vapor deposition (CVD) or plasma enhanced CVD (PECVD), rather than being thermally grown. This is because the silicon substrate is not available for thermal oxidation at this stage of the fabrication. CVD or PECVD by the reaction of precursors such as silane (SIH_4) and oxygen requires lower temperatures than thermal oxidation, which is a bonus. CVD silicon dioxide is chemically very stable. Such use of oxide insulating liners is shown, for example, in Tessariol. Ex. 1006, [0038].

177. It would have at least been obvious to employ a dielectric material as the insulating liner for the same reasons that such use of silicon dioxide was common place in the industry, as I describe above. Again, dielectric materials, e.g., silicon dioxide, were the ideal material for insulator liners and easy to implement.

178. As I discuss under limitation [1.F], a "conductive layer" then fills the rest of the first opening 122 and second openings 124 to form a common source line 144 and dummy source line 146, respectively. Park, 13:53-54. This creates a

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vertical member with a conductive core and insulator liner. Annotated Figure 3 shows this below.



XIV. GROUND 2: CLAIMS 1-6 AND 11-13 ARE OBVIOUS OVER TESSARIOL

179. Tessariol (Ex. 1006), when considered in view of the knowledge of a POSITA, renders claims 1-6 and 11-13 obvious under PO's apparent construction of *dummy source structures*.

A. Claim 1

1. [1.PRE] "A three-dimensional (3D) memory device, comprising:"

180. I offer no opinion on whether the preamble is or is not limiting. To the extent the preamble is limiting, Tessariol discloses it.

181. Tessariol describes its embodiments in the context of "a construction 10." Ex. 1006, [0027]. Construction 10 would have been understood to be a memory device. For example, Tessariol discloses that construction 10 may include "memory cells." *Id.*, [0042]. Tessariol further discloses that "[e]mbodiments disclosed herein pertain to devices, to methods used in forming a circuit structure, and to methods used in forming an array of elevationally-extending transistors and a circuit structure adjacent thereto." *Id.*, [0001]. This refers to vertical memory strings, and thus an embodiment of construction 10 is a 3D NAND. *Id.*, [0006] ("NAND architecture may be configured in a three-dimensional arrangement comprising vertically-stacked memory cells individually comprising a reversibly programmable vertical transistor."), [0030] ("Elevationally-extending channel openings 26 have been formed into vertically-alternating tiers 16 and 18 in first stack 24."). The various figures, as I discuss below, further depict the 3D memory architecture.

182. Thus, Tessariol discloses *a three-dimensional (3D) memory device* (e.g., construction 10).

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2. [1.A] "a substrate;"

183. Tessariol discloses this limitation.

184. As shown below, Tessariol discloses that "construction 10 comprises a base substrate 11." Ex. 1006, [0027]. Base substrate refers to the substrate on the bottom of the device, as some 3D NAND devices may include another substrate, e.g., for circuit elements above the memory stack.

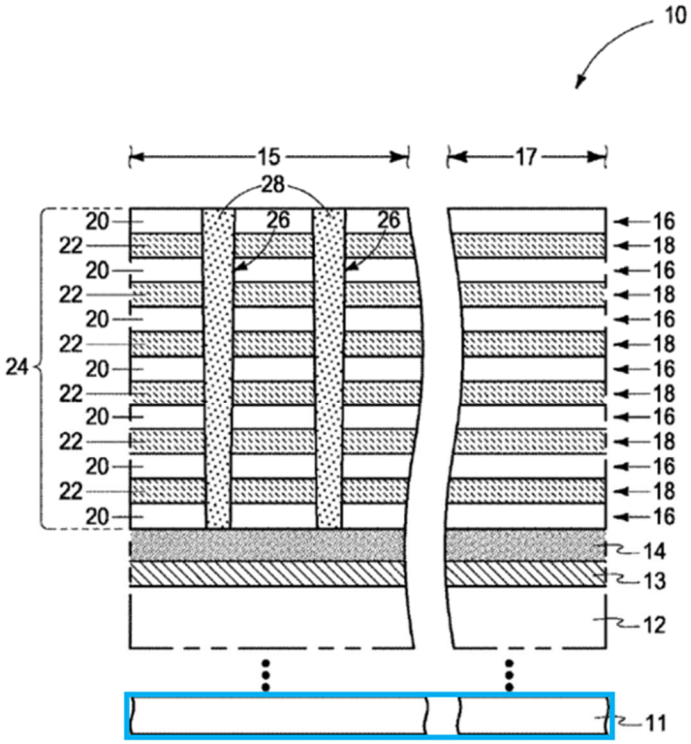


FIG. 1

Id., Fig. 1 (annotated).

185. Thus, Tessariol discloses *a substrate* (*e.g.*, base substrate 11).

3. [1.B] "a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;"

186. Tessariol discloses this limitation.

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187. The '872 Patent defines "on" as follows: "the meaning of 'on,' 'above,' and 'over' in the present disclosure should be interpreted in the broadest manner such that 'on' not only means 'directly on' something but also includes the meaning of 'on' something with an intermediate feature or a layer therebetween." Ex. 1001, 3:27-33.

188. Tessariol's memory stack consists of two stacks. Ex. 1006, [0028] ("The discussion largely proceeds with a fabrication method forming two stacks."). Tessariol's multiple-stack structure includes "vertically-alternating tiers [16 and 18] of different composition first [20] and second materials [22], with the vertically-alternating tiers comprising an array portion [15] and a portion adjacent to the array portion [17]." *Id*.

189. As shown below, Tessariol discloses first forming "a ***first stack 24*** of vertically-alternating tiers 16 and 18." Ex. 1006, [0029] (emphasis added).

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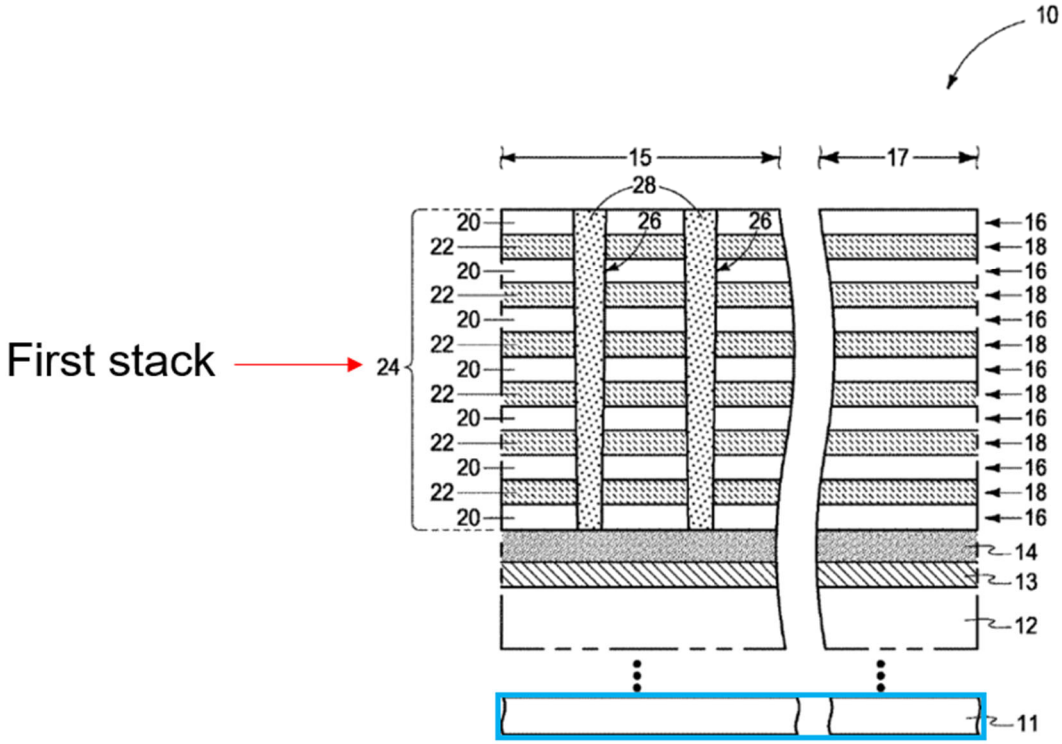


FIG. 1

Id., Fig. 1 (annotated).

190. Then, as shown below, Tessariol discloses forming "a ***second stack 30*** of vertically alternating tiers 18, 16, of different composition materials 22, 20 . . . over first stack 24." Ex. 1006, [0031] (emphasis added). Vertically alternating means that the layers, as shown above, spread over the X-Y direction and alternate in the Z direction.

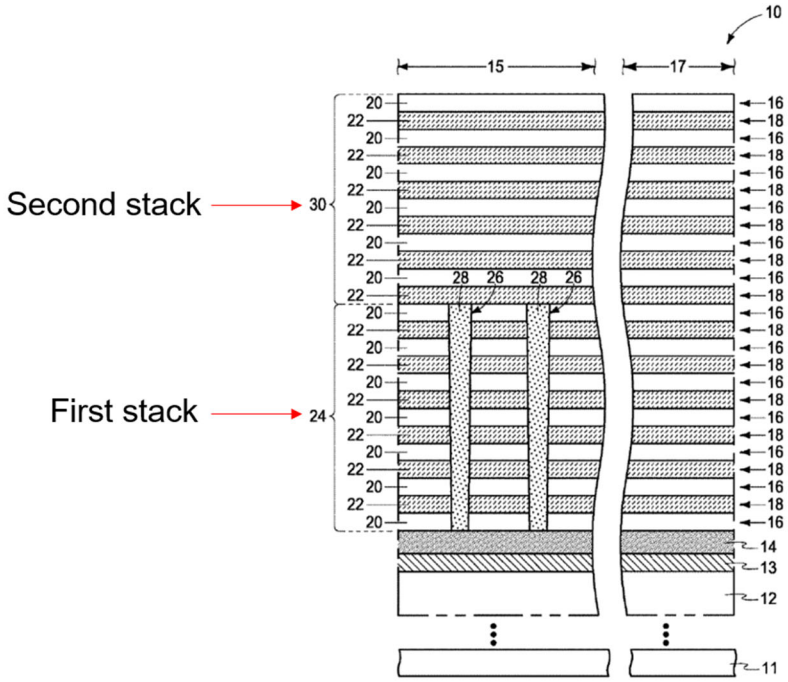


FIG. 2

Id., Fig. 2 (annotated).

191. Stacks 24 and 30 include "[v]ertically-alternating tiers 16 and 18 of different composition first and second materials 20 and 22." Ex. 1006, [0029]. "Ideally, materials 20 and 22 are of the same relative compositions with respect to one another in first stack 24 and second stack 30." *Id.*, [0031]. Tessariol further discloses that "[f]irst material 20 comprises insulative material" and "[s]econd material 22 . . . may comprise any one or more of conductive, semiconductive, and insulative materials. *Id.*, [0029]. As I discuss below, the second material 22 layers are sacrificial gate layers, so the important characteristic about this material is that it is selectively etchable relative to the dielectric layers during the gate replacement

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process. The first material layers surround the second material layers (which are gate lines):

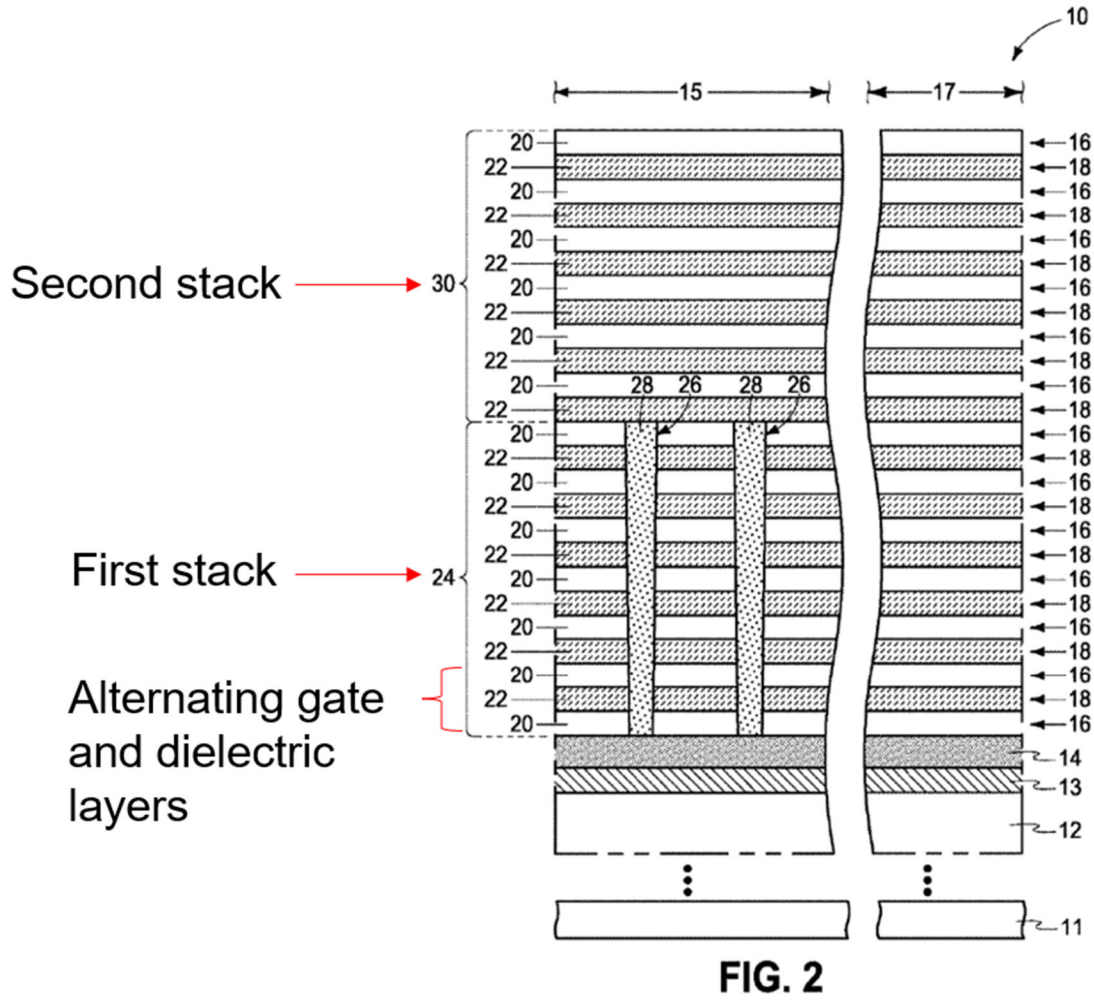


FIG. 2

Id., Fig. 2 (annotated).

192. During the gate layer replacement process (see Section VIII), the sacrificial gate layers 22 are etched away and replaced with gate layers 72. Ex. 1006, [0041] ("FIGS. 11-13 show the void space (not shown) resulting from etching away material 22 (not shown) as having been filled with conductive material 72 (e.g.,

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metal material). Steps 40-47 now comprise conductive steps due to presence of conductive material 72 and that are at least partially elevationally separated from one another by insulative material 20."). The gate layers 72 are conductive. *Id.*

193. Thus, Tessariol discloses *a memory stack comprising interleaved conductive layers and dielectric layers* (e.g., stacks 24 and 30, which comprise alternating layers 20 and 72) *on the substrate* (e.g., substrate 11).

4. [1.C] "a staircase structure on one side of the memory stack;"

194. Tessariol discloses this limitation.

195. Tessariol's memory device includes "an array portion [15] and a portion adjacent to the array portion [17]." Ex. 1006, [0028]. The adjacent portion, as the name suggests, is *on one side of the memory stack*:

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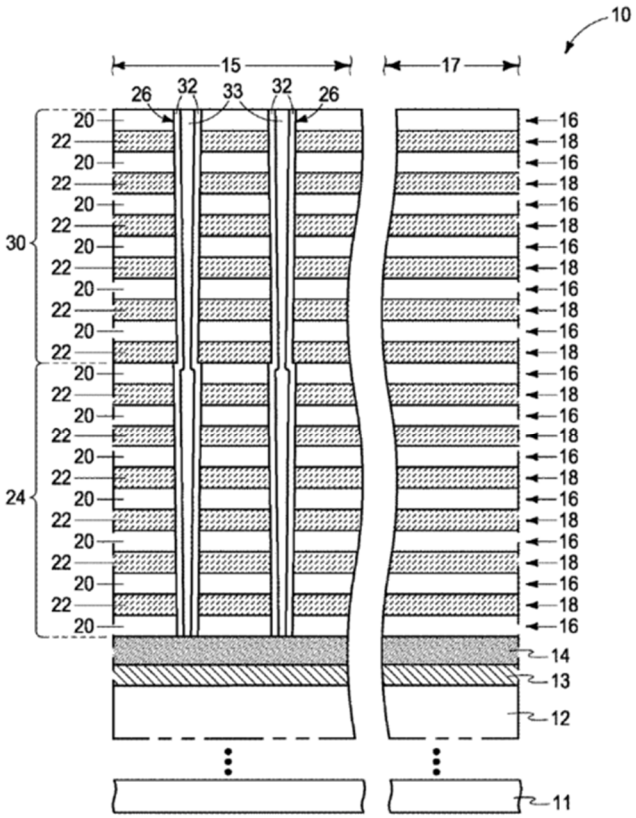


FIG. 5

Id., Fig. 5.

196. I discuss the basics of staircase structures in Section XIII. The adjacent region 17 is the *staircase structure* portion of Tessariol's multi-stack structure. Again, this portion provides the landing areas on the gate layers for contacts. Tessariol discloses exemplary staircases in Figures 6-7: "FIGS. 6 and 7 show an expanded, yet reduced-scale, version of adjacent portion 17 as comprising three stair step structures 34, 36, and 38." Ex. 1006, [0034].

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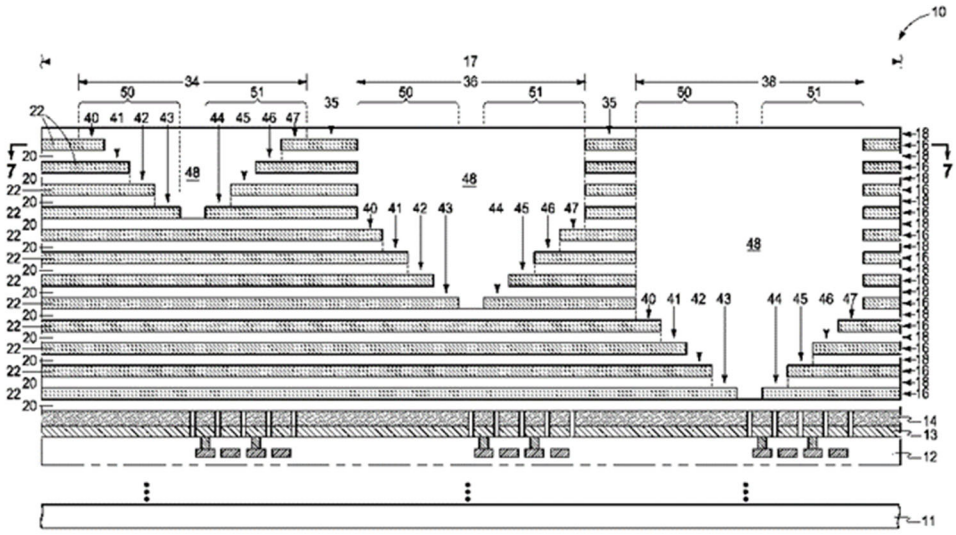


FIG. 6

Id., Fig. 6. Further, Tessariol discloses that "[a]dditionally, only one stair step structure, two stair step structures, or more than three stair step structures may be formed. Such may be formed by any suitable existing or yet-to-be-developed technique, with photolithographic patterning and etch being one example." *Id.,* [0034]. "[P]hotolithographic patterning and etch" refers to a repeating process in which a cycle consists of making portions of the stack and then etching. This process forms the stepped structure.

197. Note that in Tessariol, only the left portion of each staircase structure (48) actually functions as a staircase structure. This is because, as shown above, the right portion of the staircase structure includes gate layers that do not connect to the memory stack in region 15.

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198. Thus, Tessariol discloses *a staircase structure on one side of the memory stack* (e.g., staircase in adjacent region 17 next to array region 15).

5. [1.D] "a staircase contact in the staircase structure; and"

199. Tessariol discloses this limitation.

200. Tessariol discloses "[r]eferring to FIGS. 15-18, and in one embodiment, operating conducting vias 80 have been formed which individually extend elevationally to and directly electrically couple with conductive material 72 of one of conductive steps 40-47." Ex. 1006, [0046]; *see also id.*, [0052] ("In one embodiment, operating conducting vias (e.g., 80) individually extend elevationally to and directly electrically couple with conductive material (e.g., 72) of one of the conductive steps."). Again, the steps form landing pads for the staircase contacts. The gate layers are the word lines of the memory. And the staircase contact allows upper level components to control the word lines for memory cell access operations.

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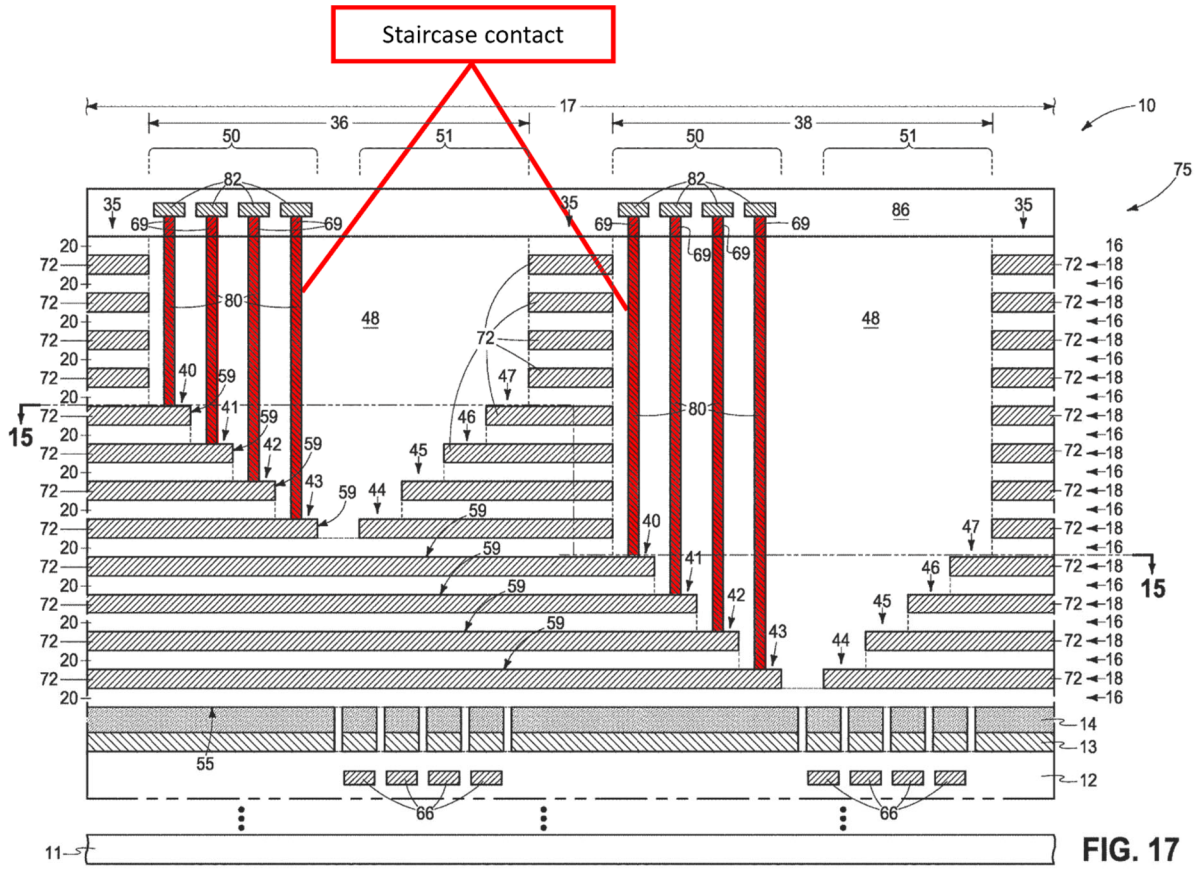


FIG. 17

Id., Fig. 17.

201. Thus, Tessariol discloses *a staircase contact* (e.g., a staircase-region contact 80) *in the staircase structure* (e.g., staircase in adjacent region 17).

6. [1.E] "a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact,"

202. Tessariol discloses this limitation under Patent Owner's apparent construction of *dummy source structures*.

203. First, Tessariol's dummy source structures are dummy structure 60 and operative conductive vias 58. Specifically, Tessariol discloses that these perform a

support function (the operative vias 58 also provide an interconnect function), and both comprise "an insulative lining 62 (e.g., silicon dioxide and/or silicon nitride) and a conductive core 64 (e.g., metal material)." Ex. 1006, [0038]; *see also id.*, [0041] (support function).

204. The dummy structures 60 and operative conductive vias 58 are formed in dummy structure openings 56 and elevationally extending via openings 54 that are formed through a memory stack comprised of insulating and conductive materials. Ex. 1006, [0037]-[0038]. The dummy structure openings 56 and via openings 54 may be formed simultaneously, and the respective dummy structures 60 and operative conductive vias 58 may also be formed simultaneously. *Id.*, [0037]-[0038]. Forming them simultaneously will save time and process steps. This will also create these structures the same. However, because the dummy structures 60 are dummy structures, it is unnecessary to connect these to upper level interconnects.

205. The structure of dummy structures 60 and conductive vias 58 match those, as for example, in the '872 Patent. The '872 Patent provides an example of a dummy source structure with a conductive core and insulating liner, and states that it may be an active interconnect. Ex. 1001, 5:37-43. Thus, under PO's interpretation, dummy structures 60 and conductive vias 58 are *dummy source structures*, even though they are not formed in voids that are used in the gate line replacement process. The dummy structures 60 are not interconnects. But recall

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that the dummy source structures may be dummy structures and not function as interconnects. *See* Section X.A.

206. Second, as shown below, these structures *extend[] vertically through the staircase structure*. As I describe above, this is because the etch forms holes through the memory stack, and then a deposition fills those holes.

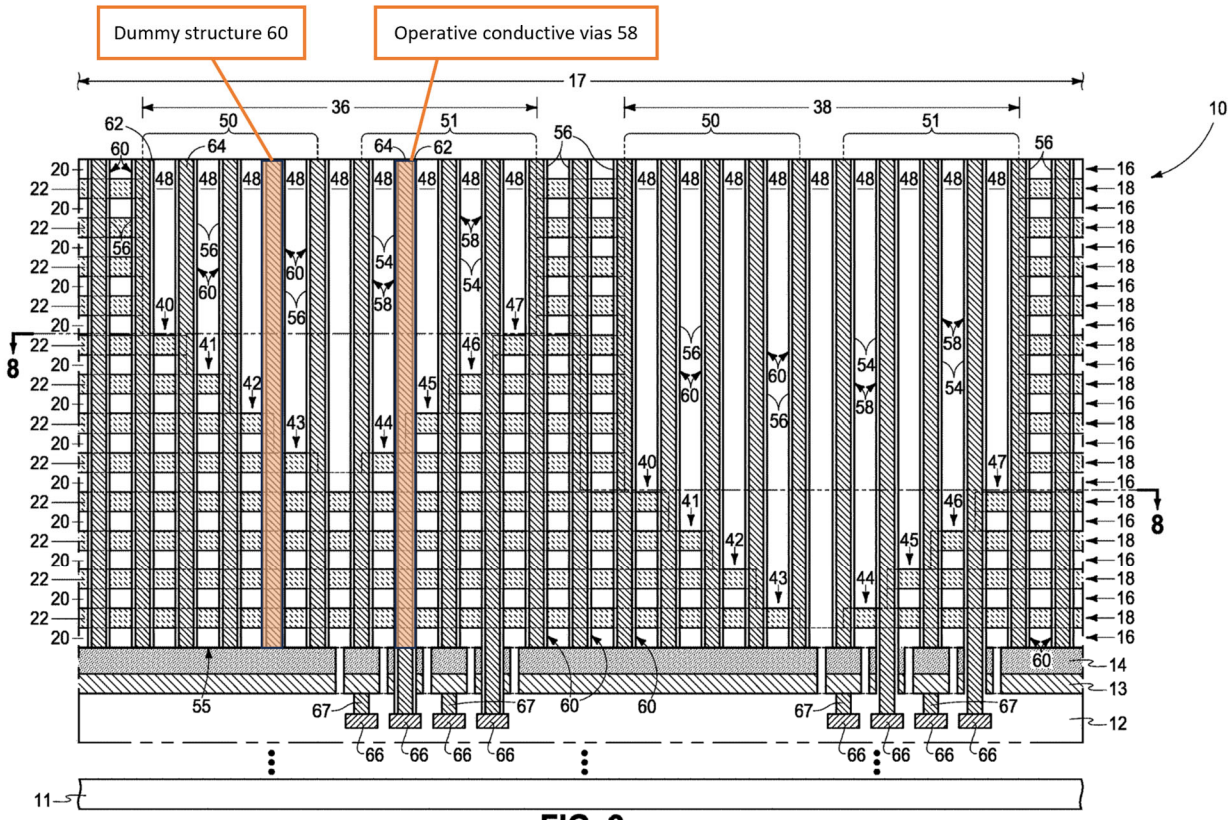


FIG. 9

Ex. 1006, Fig. 12, [0041] ("Such may thereby temporarily effectively leave void space (not shown) elevationally between first material tiers 20, with such tiers being elevationally supported and prevented from collapsing within array portion 15 by

transistor material 32 and by both dummy-support structures 60 and operative conductive vias 58 within the stair step structures in adjacent portion 17.").

207. Third, Tessariol discloses that *the plurality of dummy source structures surround[] the staircase contact*. Tessariol process forms the staircase contacts after forming the dummy structures 60 and conductive vias 58. Thus, Figure 11 of Tessariol shows only the dummy structures 60 and conductive vias 58. Note in subsequent Figures, all of the labels of these structures are not visible. Below is a top-down view (note dummy support structures 60 are in regions 50 and the conductive vias 58 are in regions 51):

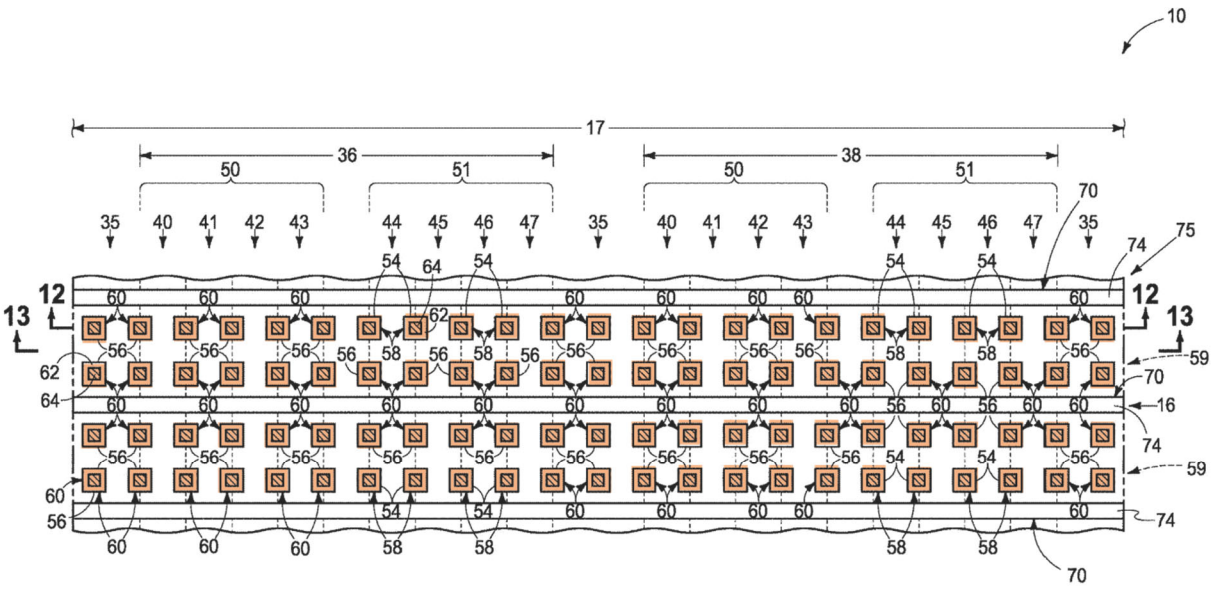


FIG. 11

Ex. 1006, Fig. 11.

208. Next, Tessariol forms the *staircase contacts* 80 (in red circles below). Recall that these extend down to respective gate layers (word lines).

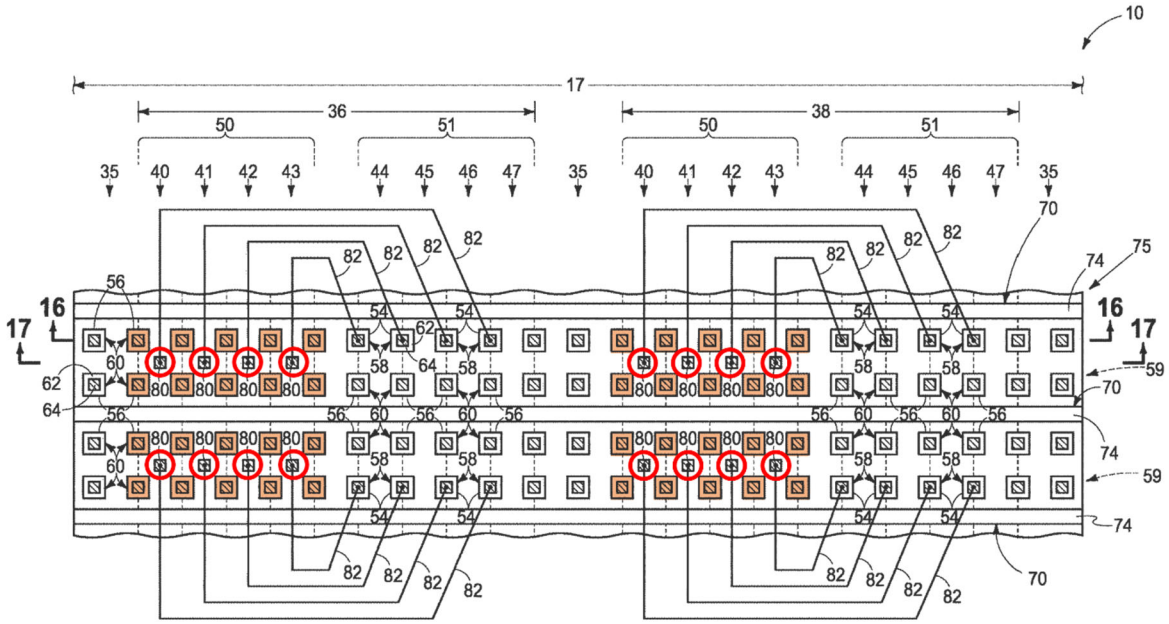


FIG. 15

Ex. 1006, Fig. 15 (annotated), [0046] ("Referring to FIGS. 15-18, and in one embodiment, operating conducting vias 80 have been formed which individually extend elevationally to and directly electrically couple with conductive material 72 of one of conductive steps 40-47.").

209. Taking the case of a *staircase contact*, *a plurality of dummy source structures surround* a given *staircase contact*, just like the exemplary embodiments of the '872 Patent in which four *dummy source structures surround the staircase contact*. *See* Section VII. Thus, whatever is/are the *staircase contact[(s)]*, *a*

plurality of dummy source structures will *surround the staircase contact[(s)]*. This is shown below with an example of a single *staircase contact*.

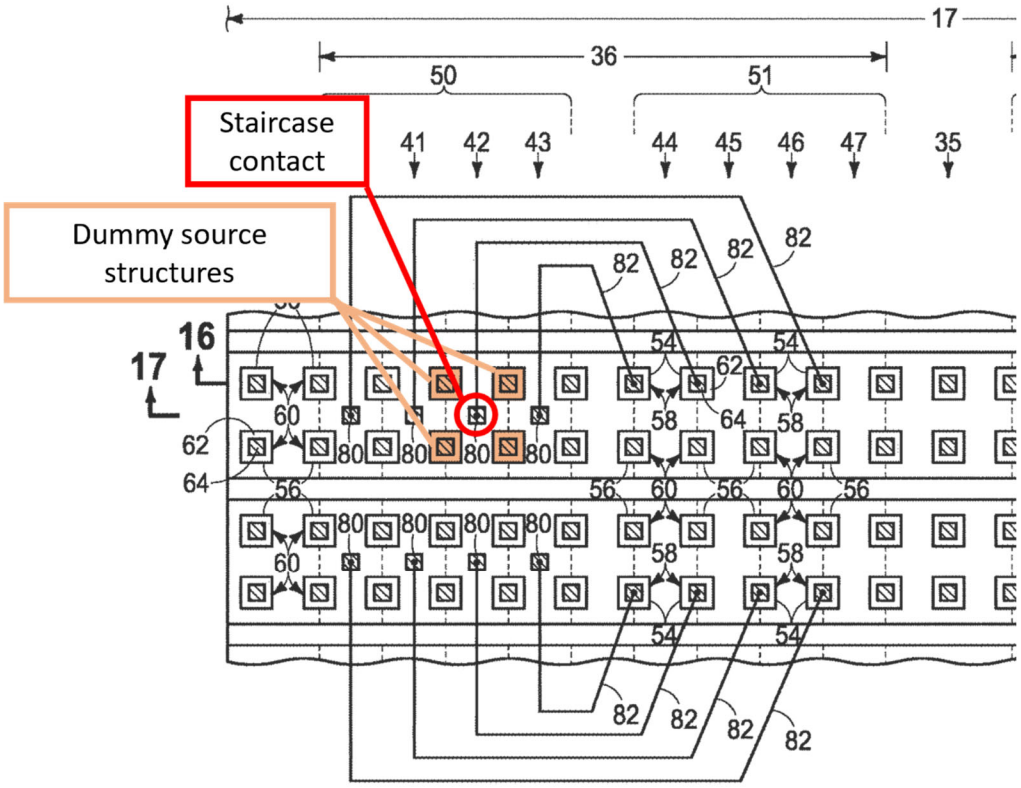


FIG. 15

Ex. 1006, Fig. 15 (partial) (annotated).

210. Thus, Tessariol discloses *a plurality of dummy source structures* (e.g., dummy structures 60) *each extending vertically through the staircase structure* (e.g., through adjacent region 17), *the plurality of dummy source structures surrounding the staircase contact* (e.g., a via 80).

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7. [1.F] "wherein each of the dummy source structures comprises a conductive contact."

211. Tessariol discloses this limitation or at least renders it obvious.

212. Tessariol discloses dummy structures 60 and operative conductive vias 58 that comprise "an insulative lining 62 (e.g., silicon dioxide and/or silicon nitride) and a conductive core 64 (e.g., metal material)." Ex. 1006, [0038]. This is like an embodiment of the '872 Patent in which the dummy structures have a conductive core and insulating liner.[5] Ex. 1001, 11:34-49.

213. The conductive vias are operable vias and thus connect to interconnect lines: "Interconnect lines 82 have been formed above stair step structures 36 and 38 and individually directly electrically couple together different individual operating conducting vias 80 to different individual operative conductive vias 58 through conductive extensions 69." Ex. 1006, [0046], Fig. 16. As I discuss in Section X, while the claim term includes the word "dummy" (which suggests an inoperable structure), the specification explains that the structure need not be inoperative. The specification states that "dummy source structures" can "contact with the substrate

[5] As I note above, unlike the '872 Patent, Tessariol's dummy structures 60 and operative conductive vias 58 do not fill the voids used for the sacrificial gate replacement process. Thus, I am applying PO's construction here.

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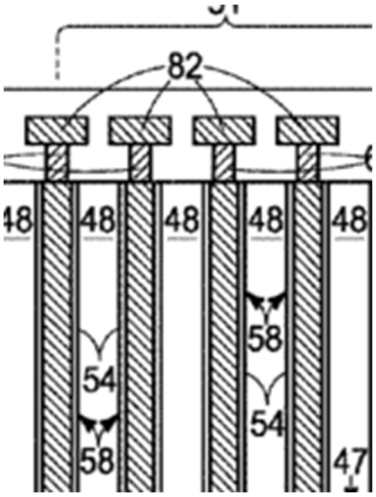
and may provide interconnect between the 3D memory device and peripheral devices." Ex. 1001, 5:40-43, 16:63-66. Again, "interconnect" refers to the fact that via is forming an electrical connection between an upper-level device and a lower-level device through the memory stack. The insulating liner of the via ensures the connection does not short circuit to a gate layer.

214. Were Patent Owner to argue that Tessariol does not disclose that the dummy structures 60 include a *contact* on the theory that they do not connect to an upper-level interconnect and thus cannot connect to an upper-level interconnect, I would disagree with the Patent Owner because as I discuss above, the '872 specification does not require the *dummy source structures* to function as interconnects. *See* Section X. Also, the claimed *contact* need not be a separate element from a conductive core. *See* Section XIV.A.7. That is, the dummy structures include a *contact*, because they include a conductive core. And the *dummy source structure* does not need to contact an upper-level interconnect, because the '872 Patent explains that a *dummy* structure does not have to make such contact and can be a dummy structure. *See* Section X. The *dummy source structures* of Tessariol include a conductive core, like the '872 Patent embodiments, and thus comprise a *contact*. Ex. 1006, [0046].

215. In any event, in my opinion, it would have been obvious that the dummy source structures 60 can connect to an upper-level interconnect.

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216. Second, at the very minimum, it would have been obvious that Tessariol's dummy structures can contact an upper-level interconnect. The dummy structure 60 includes the same structure as the conductive vias that do *contact* the upper-level interconnect. As I explain above (*see* Section XIV.A.6), Tessariol's dummy structures and conductive vias are made at exactly the same time in the same way. The conductive vias 58 do contact upper-level interconnects 82. On the other hand, these interconnects 82 are simply not made on the dummy structures, because there is no need for them to connect to upper-level devices.



Ex. 1006, Fig. 16 (partial), [0046]. It would therefore have been obvious to a POSITA that dummy source structures 60 can include a *contact* that could connect to an upper-level interconnect. It would simply involve performing the same process to create interconnects 82 on top of the dummy structures. And because the dummy structures 60 and conductive vias are made with the same process, the interconnects would provide the same function for the dummy structures 60 as the conductive vias

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58, and thus dummy structures certainly could connect to upper-level interconnects with such interconnects. This demonstrates that the dummy structures 60 are capable as functioning as a conductive via, as all that is necessary is connecting the dummy structures 60 to upper-level devices in the same way as is done for the conductive vias 58. And Tessariol's process is advantageous. As I explain above under limitation [1.E], it reduces time and process steps. It was common to build dummy structures in this way. Dummy simply refers to, for example, that the structures are not put to use as actual interconnects.

217. Thus, Tessariol discloses, or at least renders obvious, a *conductive contact* (e.g., the metal core of the dummy structures 60 and conductive vias 58).

B. Claim 2

1. [2] "The 3D memory device of claim 1, wherein the plurality of dummy source structures are located adjacent to the staircase contact."

218. Tessariol discloses this limitation. *See* Section XI.A.6. As shown below, the plurality of dummy structures 60 (i.e., *dummy source structures*) are located adjacent to and surround the operating conducting via 80 (i.e., *staircase contact*).

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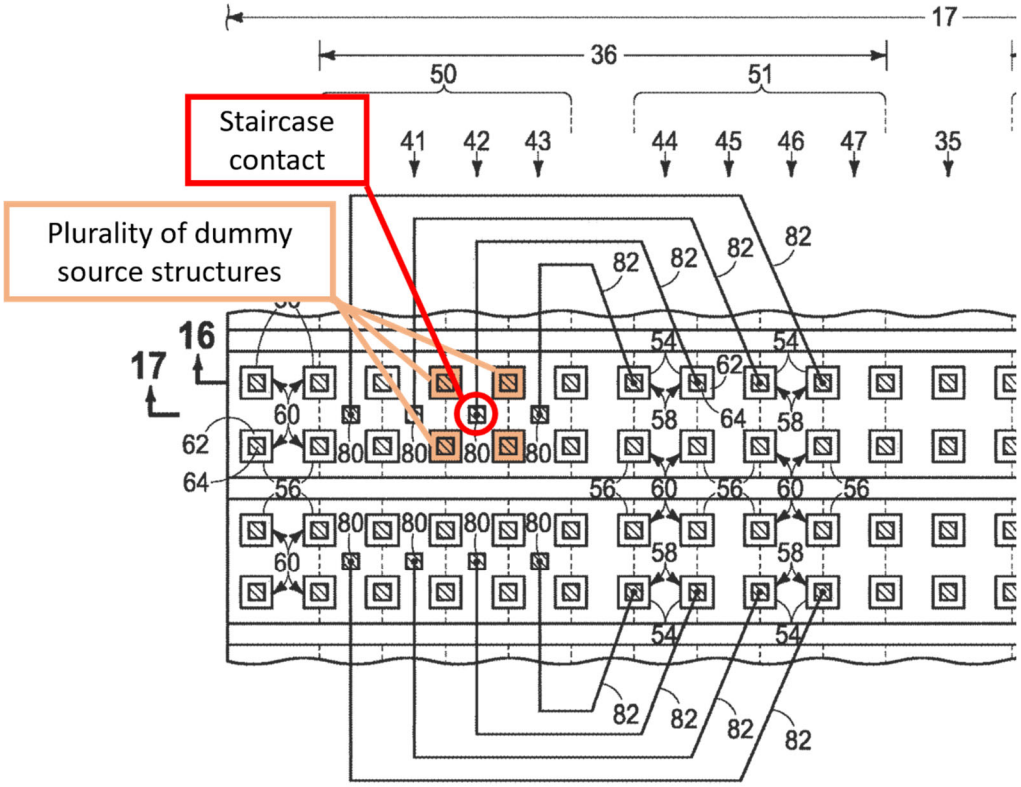


FIG. 15

Ex. 1006, Fig. 15 (partial) (annotated).

C. Claim 3

1. [3] "The 3D memory device of claim 1, wherein at least two of the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact."

219. Tessariol discloses this limitation. *See* Section XI.A.6. As shown below, at least two of the dummy structures 60 (i.e., *dummy source structures*) *are of nominally equal lateral distances* to the operating conducting via 80 (i.e.,

staircase contact). I discuss the '872 Patent use of this claim language in Section XIII.C.

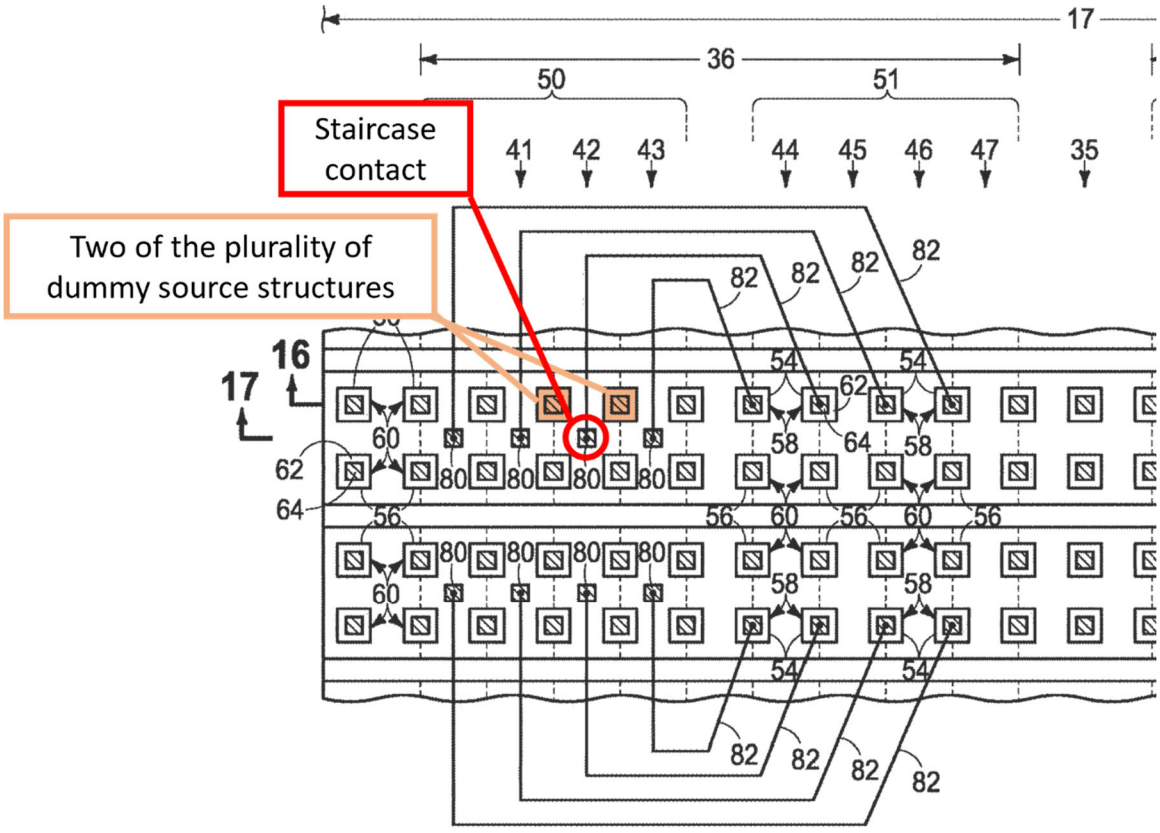


FIG. 15

Ex. 1006, Fig. 15 (partial) (annotated).

D. Claim 4

1. [4] "The 3D memory device of claim 1, wherein the plurality of dummy source structures are of nominally equal lateral distances to the staircase contact."

220. Tessariol discloses this limitation. *See* Sections XI.A.6., C.

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E. Claim 5

1. [5] "The 3D memory device of claim 1, wherein in a plan view, at least two of the plurality of dummy source structures are arranged in a first row that extends along a first lateral direction."

221. Tessariol discloses this limitation.

222. As shown below, dummy structures 60 (i.e., *dummy source structures*) in orange arranged in a first row that extends along a first lateral direction.

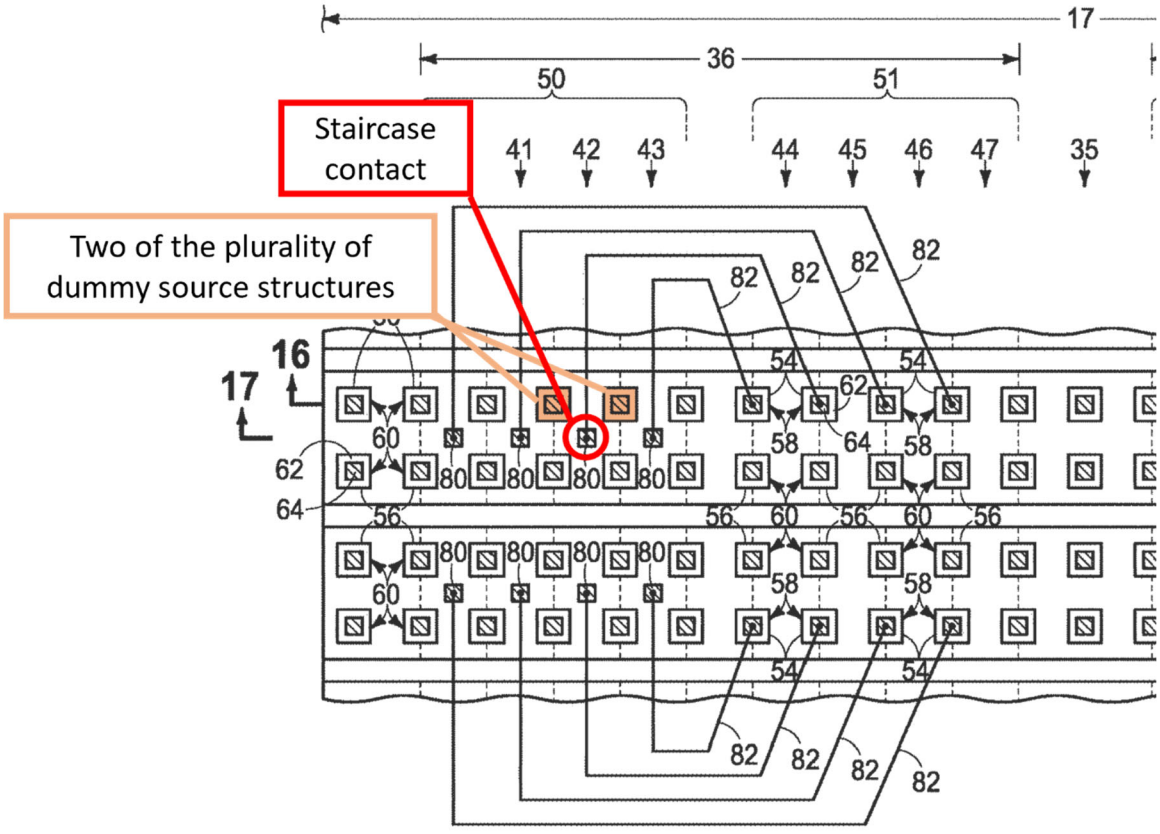


FIG. 15

Ex. 1006, Fig. 15 (annotated). The plurality of *dummy source structures* may include all of the *dummy source structures* surrounding the staircase structures (for

each *staircase contact*, four *dummy source structures* that *surround* the respective *staircase contact*).

F. Claim 6

1. [6] "The 3D memory device of claim 5, wherein in the plan view, at least two other dummy source structures are arranged in a second row that extends along a second lateral direction perpendicular to the first lateral direction."

223. Tessariol discloses this limitation.

224. Recall that the '872 Patent discloses that the first lateral direction may be a X direction, and the second lateral direction may be a Y direction. Ex. 1001, 6:54-59. Figure 1A is an embodiment of claim 6, which shows two *dummy source structures* along the first row in the X axis and two *dummy source structures* along the second row in the Y axis. *Id.*, Figure 1A. The two *dummy source structures* in the first row do not surround the same *staircase contact*, and the two *dummy source structures* in the second row similarly do not surround the same *staircase contact*. But the plurality of *dummy source structures* may include all of the *dummy source structures* to surround the staircase structures (for each *staircase contact*, four *dummy source structures* that *surround* the respective *staircase contact*).

225. Annotated Figure 15 below shows two dummy structures 60 (i.e., *dummy source structures*) in orange arranged in a first row that extends along a first lateral direction (highlighted in orange) and two dummy structures 60 in teal

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arranged in a second row that extends along a second lateral direction (highlighted in teal) perpendicular to the first lateral direction.

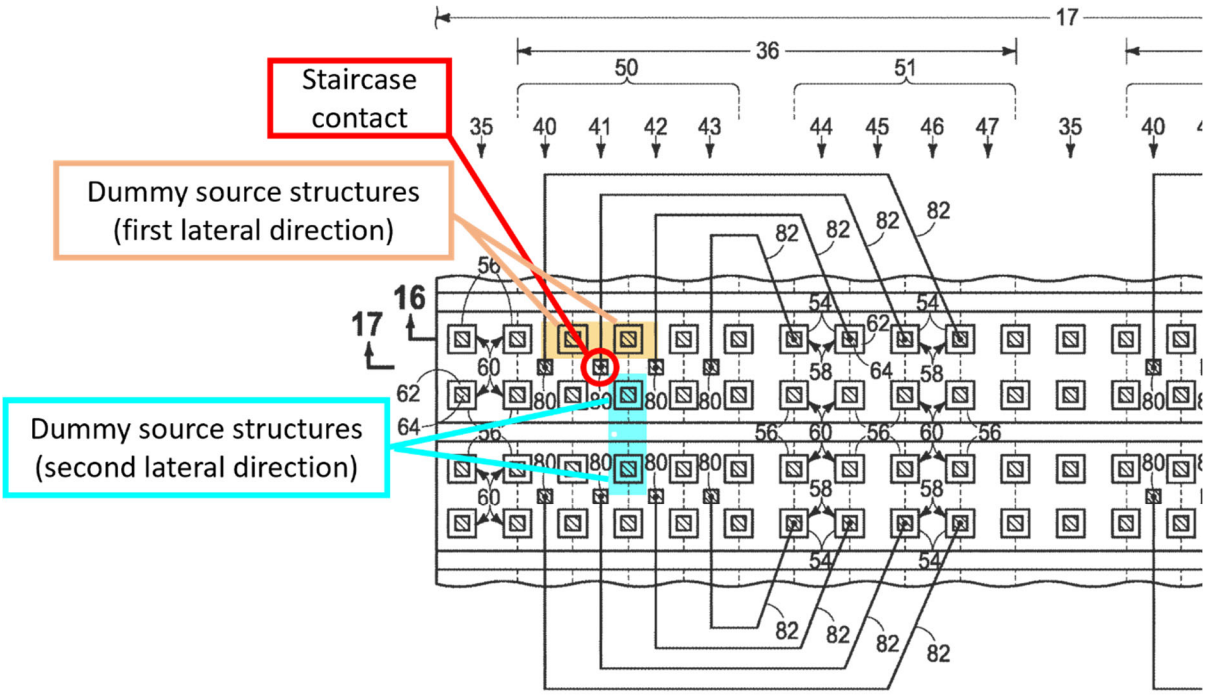


FIG. 15

Ex. 1006, Fig. 15 (partial) (annotated).

G. Claim 11

1. [11] "The 3D memory device of claim 1, comprising first and second staircase contacts, wherein at least one dummy source structure is located between the first and second staircase contacts."

226. Tessariol discloses this limitation.

227. One dummy structure 60 (i.e., *dummy source structure*) (in orange) is located between the first and second *staircase contacts* (in red).

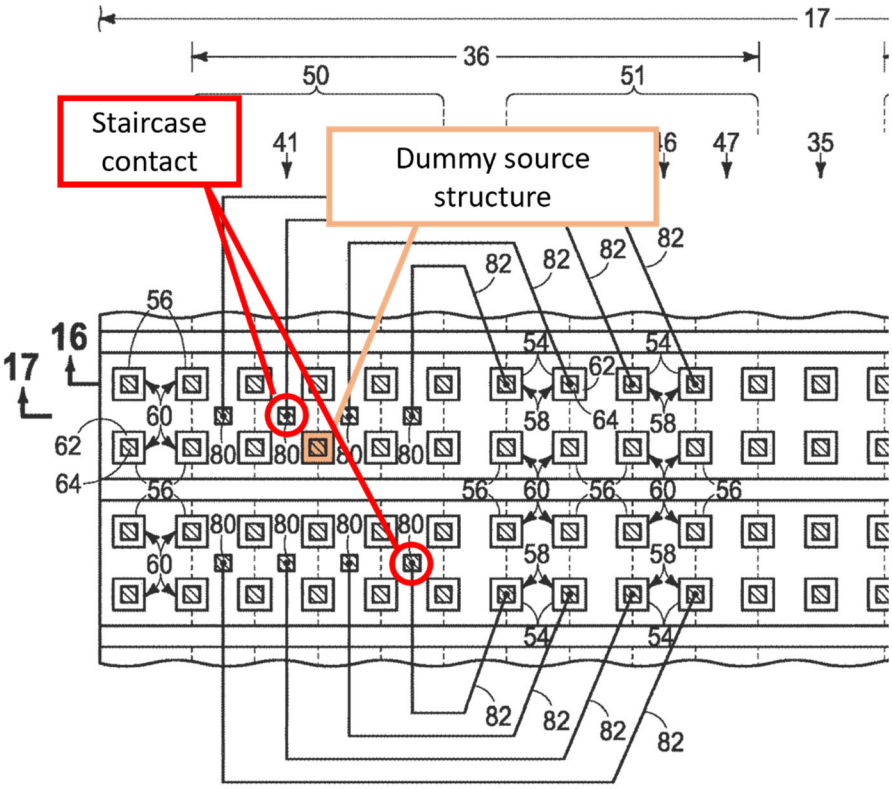


FIG. 15

Ex. 1006, Fig. 15 (annotated). In all cases, the dummy source structures (*plurality of dummy source structures*) above *surround* the *staircase contacts*, because 4 dummy source structures surround each staircase contact.

H. Claim 12

1. [12] "The 3D memory device of claim 1, wherein at least two dummy source structures are located between the first and second staircase contacts."

228. Tessariol discloses this limitation.

229. Annotated Figure 15 below shows the first and second operative vias 80 (*staircase contacts*) in red, and at least two dummy structures 60 (*dummy source structure*) in orange, that are located between the first and second staircase contacts.

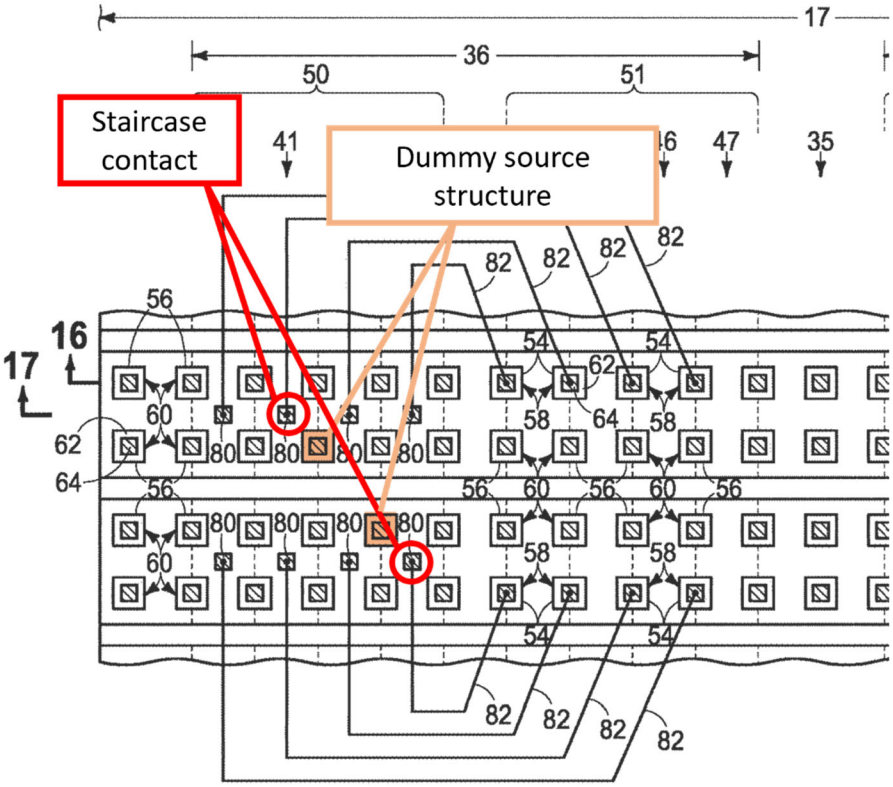


FIG. 15

Ex. 1006, Fig. 15. In all cases, the dummy source structures (*plurality of dummy source structures*) above *surround* the *staircase contacts*, because 4 dummy source structures surround each staircase contact.

I. Claim 13

1. [13] "The 3D memory device of claim 1, wherein the conductive contact comprises a conductor layer, and wherein the at least one dummy source structure further comprises a spacer surrounding the conductor layer along a sidewall of the conductor layer, the spacer comprising a dielectric material."

230. Tessariol discloses this limitation.

231. As I discuss in limitations [1.E] and [1.F] above, Tessariol discloses both dummy structures 60 and operative conductive vias 58 as *dummy source structures* with *conductive contacts*. Tessariol's dummy structures 60 and operative conductive vias 58 are formed "to comprise an insulative lining 62 (e.g., silicon dioxide and/or silicon nitride) and a conductive core 64 (e.g., metal material)." Ex. 1006, [0038].

232. Both silicon oxide and silicon nitride are *dielectrics*. Ex. 1001, 10:9-12. The insulative lining 62 acts as a *spacer* that surrounds the conductor layer along a *sidewall of the conductor layer*. Ex. 1006, Fig. 9 (annotated). The word spacer here refers to the fact that the liner creates a space between the stack and the core. This prevents the shorting of the conductive gate layers to the conductive core.

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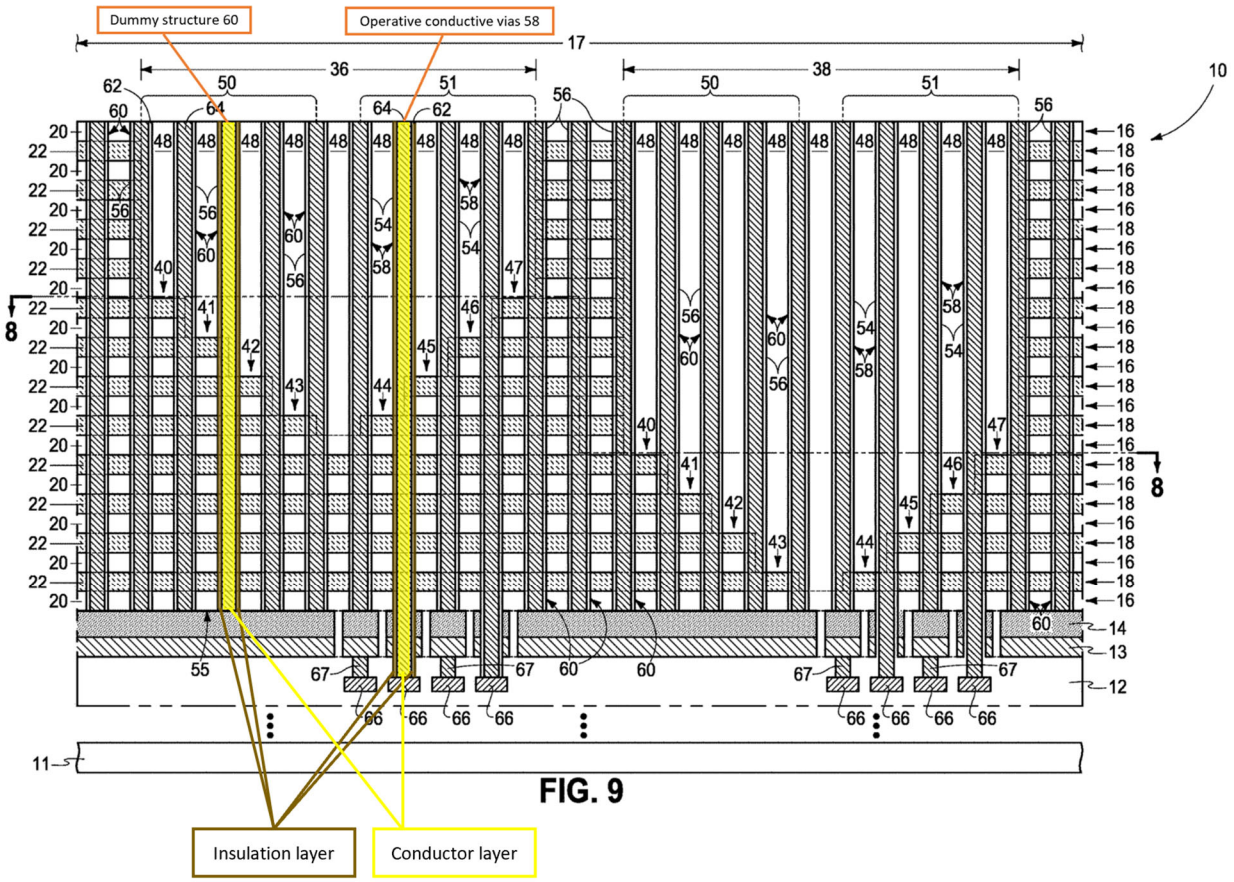


FIG. 9

XV. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS

233. During my review of the materials discussed herein, I did not become aware of any evidence suggesting the existence of any secondary indicia or considerations of non-obviousness. In the event that Patent Owner proffers any such evidence, I shall provide my opinions on such evidence in a reply declaration.

XVI. DECLARATION

234. In signing this declaration, I realize that this declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the USPTO.

235. I am aware that willfully false statements and the like made by me in connection with this declaration are punishable by fine or imprisonment, or both (18 U.S.C. § 1001) and may jeopardize the validity of the Petition. All statements herein made by me of my own knowledge are true and all statements made on information and belief are believed to be true. I declare under penalty of perjury that the foregoing is true and correct.

Executed this 17th day of April 2024 at Austin, Texas.



Sanjay Banerjee, Ph.D.

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