

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00789

Patent 10,861,872

**PATENT OWNER'S PRELIMINARY RESPONSE
UNDER 37 C.F.R. § 42.107**

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LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	Declaration of Dr. Kuhn
Ex. 2002	CV of Dr. Kuhn
Ex. 2003	Shur, “Introduction to Electronic Devices” (1996) (“Shur”)
Ex. 2004	Streetman, “Solid State Electronic Devices” (1995) (“Streetman”)
Ex. 2005	US Patent No. 8,766,336 (“Grupp”)
Ex. 2006	Declaration of Jonathan Bradford

LIST OF ABBREVIATIONS

Abbreviation	Term
'872	U.S. Pat. No. 10,861,872
'872FH	File History of U.S. Pat. No. 10,861,872
Challenged Claims	'872, Claims 1-6 and 11-13
Office	U.S. Patent and Trademark Office
Park	U.S. Pat. No. 9,859,297
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,861,872 (IPR2024-00789, Paper 1)
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner or PO	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Tessariol	U.S. Patent Pub No. 2019/0081061

Pursuant to §42.107, ¹ Patent Owner submits this Preliminary Response to the above-captioned Petition, which should be denied in its entirety based on Petitioner's failure to show a reasonable likelihood of prevailing on any asserted ground as to any Challenged Claim.

I. INTRODUCTION

U.S. Patent 10,861,872 ("the '872," Ex. 1001) is directed to a novel and improved three-dimensional memory structure scheme that mitigates problems arising from semiconductor device fabrication processes involving depositing conductive materials into voids formed in memory devices. Ex. 1001, 4:64-65, 5:22-33. The relevant prior art at the time employed gate line slit structures to fill lateral recesses in memory devices to form, for example, gate electrodes and gate lines of the device. Ex. 1001, 4:30-33. But, with advances in 3D memory device architecture, the prior art fabrication techniques presented drawbacks, including nonuniformity resulting in a bowing of the semiconductor wafer, which contributed to yield loss during manufacturing. Ex. 1011, 5:22-30.

The '872 introduced a different memory device architecture that uses dummy

¹ All emphasis and color annotations herein are added, and all statutory and regulatory citations are to either 35 U.S.C. or 37 C.F.R., as the context indicates, unless otherwise stated.

source structures to solve the problems caused by gate line structures. Ex. 1001, 1:39-42, 5:31-36, 8:20-24. The new architecture taught by the '872 and recited in the claims is characterized by arranging the dummy source structures such that they surround a staircase contact. This includes arranging the dummy source structures in a particular pattern, layout, or design based on the size of the staircase region. *Id.* 8:49-51, 6:41-46. Such an arrangement is advantageous, for example, because it allows the deposited conductive material to travel “shorter distances to fill up the lateral recesses,” thus allowing the formed gate electrodes and gate lines to be “less susceptible to voids or density nonuniformity.” Ex. 1001, 4:52-58.

Institution should be denied because the Petition fails to establish a reasonable likelihood of prevailing with respect to any of the Challenged Claims.

Petitioner does not assert that any of the cited references anticipates any of the Challenged Claims, and seemingly concedes that the art does not explicitly disclose certain features, such as limitations relating to the claimed “dummy source structures.” *See* Pet., 8. Instead, Petitioner raises obviousness arguments based on a mix of incorrect claim constructions, faulty analysis, and conclusory testimony from its expert.

First, Petitioner relies on the “Park” reference (Ex. 1005) for each limitation of the Challenged Claims, but fails to show that Park discloses or renders obvious at least two separate requirements of the claims. Park does not disclose or render

obvious that its alleged dummy source structures are “surrounding the staircase contact” as required by the Challenged Claims because Park’s contact is merely “between” two alleged dummy source structures. Indeed, the applicant admitted prior art (“AAPA”) in the ’872 presented this same structure and the claims were properly allowed over the AAPA during prosecution. In addition, Petitioner has not shown that Park discloses or renders obvious “dummy source structures” because Park’s purported dummy source structures actually function as a source for the memory cell and are therefore not “dummy source structures.” Tellingly, Petitioner relies on “common source lines” as the “dummy source structures” that allegedly surround the contacts—as opposed to the “dummy source lines,” which do not. Attempting to circumvent this problem, Petitioner a flawed claim construction for the term—reading out the requirement that this be a “dummy” source structure.

Second, Petitioner relies on the “Tessariol” reference (Ex. 1006) for each limitation of the Challenged Claims, but again, Petitioner fails to show that Tessariol discloses or renders obvious at least two separate requirements of the claims. Petitioner has not shown that Tessariol discloses or renders obvious that the alleged “dummy source structures” comprise a “conductive contact,” because there is no evidence of such a contact, and Petitioner’s argument for obviousness provides only a conclusory and illogical argument as a purported motivation to modify the

reference. Its arguments are no more than impermissible hindsight. In addition, Petitioner has failed to show that Tessariol discloses or renders obvious “dummy source structures.” Not only does Tessariol fail to meet the plain and ordinary meaning of the term, but Petitioner concedes that its own construction of “dummy source structures” is not met by Tessariol either.

Because each reference fails to disclose or render obvious limitations of the Challenged Claims, the Board should deny institution.

II. THE CLAIMED INVENTION OF THE '827 PATENT

The claimed invention of the '872 is directed to “an improved 3D [three-dimensional] memory structure scheme” that mitigates problems arising from semiconductor device fabrication processes, which contribute to production yield loss and device performance variability. Ex. 1001, 4:64-65, 5:22-33.

Specifically, the '872 is directed to improving a semiconductor fabrication technique for 3D memory structures. Ex. 1001, 1:15-18, 4:30-33. As 3D memory devices are “scaled to smaller sizes” and “feature sizes of memory cells approach a lower limit,” fabrication becomes more challenging. Ex. 1001, 1:18-22, 4:37-38. To illustrate these challenges, the '872 describes the common approach of using openings, called gate line slits (GLSs), to deposit conductive material into trenches (or “lateral recesses”) that extend laterally in the memory array of a memory device. Ex. 1001, 4:44-49, 5:17-20. Once filled with conductive material, the trenches form

the device gate lines. The GLS, as depicted in the color-annotated version of the '872's Fig. 5 below, has “a dimension along the extending direction (or the x-direction) much greater than the dimension along the expanding dimension (or the y-direction)).” Ex. 1011, 5:22-30. As a result of this shape, formation of the GLS “can contribute to unbalanced variations of wafer flatness (e.g., wafer warpage bias) in different directions,” which “can have an adverse impact on the photolithography process to form device patterns, leading to potential die yield loss.” *Id.*

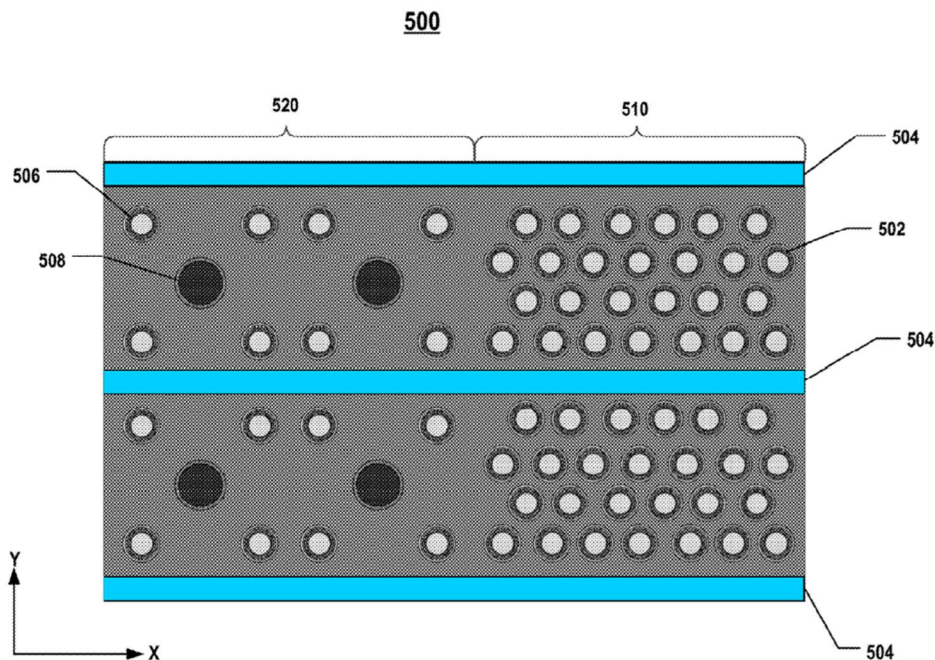


FIG. 5

The '872 solves this issue, for example, by “*replacing* the GLSs” with “a plurality of dummy source structures,” each which “extend[s] vertically” through the staircase structure on “one side of the memory stack.” Ex. 1001, 1:39-42, 5:31-

36 (emphasis added). That is, the claimed invention of the '872 allows for “**removing** GLSs from the staircase region” altogether. Ex. 1001, 8:22-23 (emphasis added). The dummy source structures can be “arranged in a pattern” such that gate electrodes or gate lines are formed with “improved uniformity and quality.” Ex. 1001, 4:43-52. The specific arrangement of the dummy source structures, as taught by the '872, is advantageous because it allows the deposited conductive material to travel “shorter distances to fill up the lateral recesses,” thus allowing the formed structures to be “less susceptible to voids or density nonuniformity.” Ex. 1001, 4:52-58.

An exemplary arrangement of **dummy source structures** is depicted in the plan view in the color-annotated version of the '872's Fig. 1A, below. The **dummy source structures** are “arranged in a pattern,” meaning in an arrangement that is “repeated at a regular interval.” Ex. 1001, 7:61-8:1. The '872 further teaches that the **dummy source structures** “surround **staircase contacts 122** of nominally same lateral distances to the respective **staircase contacts 122**” so that, as one example, the depositing “conductive material for forming the gate electrodes may travel nominally same distances to surrounding lateral recesses” to fill the lateral recesses, which “facilitat[es]” the fabrication process such that the gate electrodes are formed “with improved uniformity and quality” and “warpage bias” of the memory device is reduced. Ex. 1001, 8:25-34., 8:45-49. The '872 emphasizes that the “symmetrical

architecture” of dummy source structures is advantageous because it “can improve the performance and efficiency of etching processes,” which are additional processes in fabricating the memory device. Ex. 8:49-51. The ’872 further teaches that the **dummy source structures** are “located adjacent to **staircase contact 122**,” meaning there are “no other components” between staircase contact 122 and each of the dummy source structures. Ex. 1001, 6:41-46.

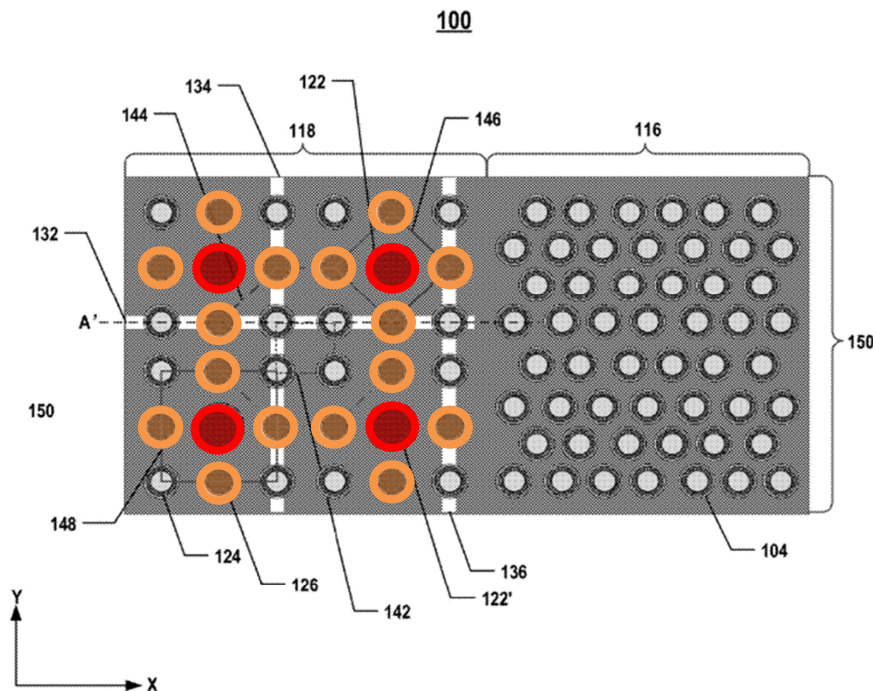


FIG. 1A

Other exemplary images of the dummy source structure arrangement entail arranging the dummy source structures symmetrically around **staircase contacts 122**, such that each structure is nominally the same lateral distance to the respective **staircase contacts 122**. Additionally, in each of the embodiments of the ’872, each of the **dummy source structures** is located adjacent to a **staircase**

contact 122, such that there are no other components located between. These arrangements are depicted in Figs. 1B-1C, below. The '872 does not include any illustrations of the dummy source structure arrangement in plan view other than those depicted in Figs. 1A-1C.

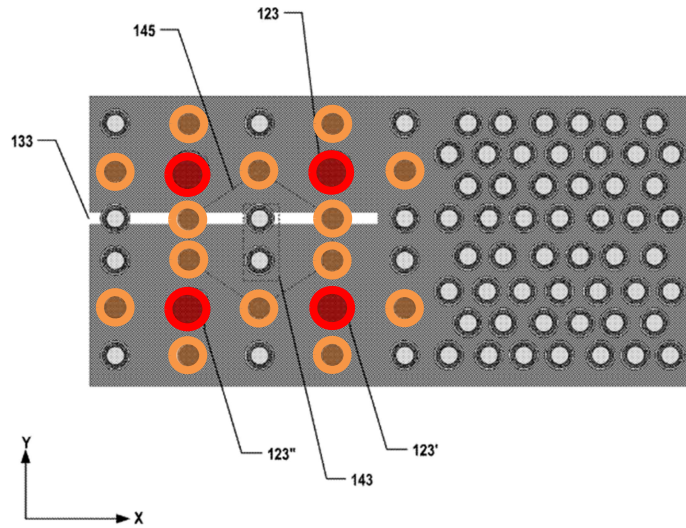


FIG. 1B

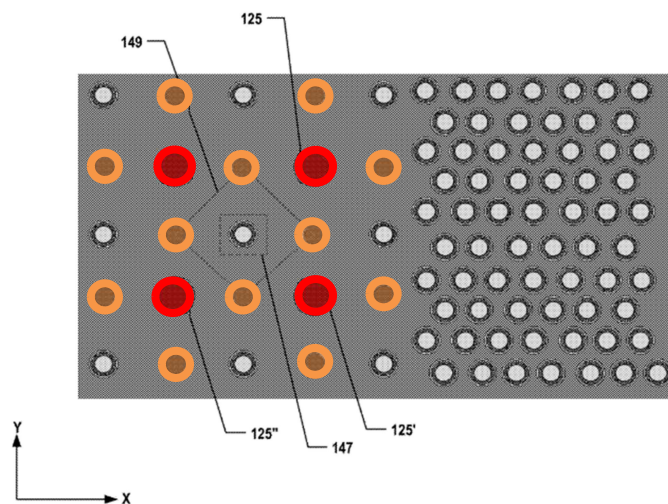


FIG. 1C

The memory device of the '872 includes: (1) **substrate** with “two lateral

surfaces extending laterally in the x-y plane” (Ex. 1001, 9:3-5); (2) “**memory stack 160**” that includes “interleaved conductive layers 106 and dielectric layers 108” and “a staircase structure 175” on “[a]t least [] one side in the lateral direction” (Ex. 1001, 9:67-10:3); (3) “dummy source structure 178” that includes “a dummy source hole filled with conductive materials as **a contact 179**”; and (4) a “spacer 177 made of any suitable dielectric materials (e.g., silicon oxide) between contact 179 and memory stack 160 to electrically separate surrounding conductive layers 106 in memory stack 160 from contact 179” (Ex. 1001, 11:39-43). A cross-section view of the memory device, depicting the dummy source structure, is below.

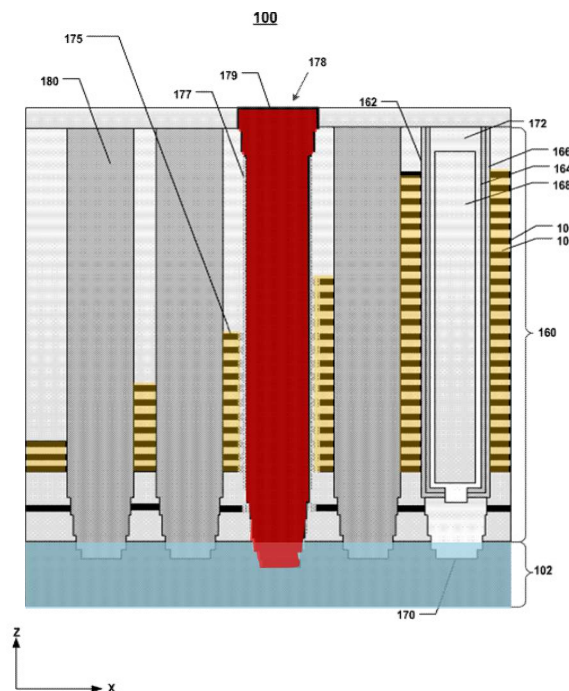


FIG. 1D

The only independent claim of the Challenged Claims, claim 1, is directed to

aspects of the above-described invention:

[1.pre] A three-dimensional (3D) memory device, comprising:

[1.a] a substrate;

[1.b] a memory stack comprising interleaved conductive layers and dielectric layers on the substrate;

[1.c] a staircase structure on one side of the memory stack;

[1.d] a staircase contact in the staircase structure; and

[1.e] a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact,

[1.f] wherein each of the dummy source structures comprises a conductive contact.

III. FILE HISTORY

The claims of the '872 remain patentable over the prior art for at least the same reasons identified during prosecution. As discussed further below in §VI, the prior art does not disclose or render obvious, *inter alia*, the claimed “dummy source structures” that comprise a “conductive contact” of the '872. Claims directed to this limitation were allowed after extensive prosecution and consideration of numerous prior art references.

The '872 was filed on May 2, 2019. During the pendency of the '872 patent

application, Applicant was required to restrict the invention to that of a “three-dimensional (3D) memory device” or “a method for forming” the same. Ex. 1002 (Part 1 of 2), 458 (5/21/2020 Requirement for Restriction/Elections). Applicant elected claims that restricted the invention of the ’872 to that of a “three-dimensional (3D) memory device.” Ex. 1002 (Part 1 of 2), 466 (5/22/2020 Applicant Arguments/Remarks Made in an Amendment).

The Examiner then rejected under 35 U.S.C. § 102(a)(1) as being allegedly anticipated by and under 35 U.S.C. § 103 as being allegedly obvious over U.S. Pub. No. 2016/0293622 (“Jeong”). Ex. 1002 (Part 1 of 2), 468-78 (6/11/2020 Office Action). In supporting this assertion, the Examiner mapped the ’872’s claimed “plurality of dummy source structures” to Jeong’s “dummy pillars” because “like the dummy source of the instant application, [they] function as a mechanical support for conductive layers” of a memory stack. Ex. 1002 (Part 1 of 2), 470, 474, 476-77 (6/11/2020 Office Action). During a telephonic Applicant-initiated interview, Applicant discussed with the Examiner the distinction between the claimed “dummy source” and the “dummy pillar” of Jeong. Ex. 1002 (Part 1 of 2), 505 (8/14/2020 Applicant-Initiated Interview Summary, Office Action Appendix). Based on these discussions, Applicant subsequently filed an amendment to the claims, further limiting the independent claims to recite, “wherein each of the dummy source structures comprises a conductive contact.” Ex. 1002 (Part 2 of 2), 510, 513

(8/18/2020 Request for Reconsideration After Non-Final Rejection). Applicant stated that the “dummy pillars in Jeong are different from the claimed ‘dummy source structure’ in amended independent claims 1 and 8 at least because the dummy pillars do not include conductive contacts,” explaining:

Nothing in Jeong’s pillar is conductive contact, as the pillar consists of insulating layers, a semiconductor pattern, and a charge storage layer. By contrast, as explained at paragraph [0057] of the present application: ‘In some embodiments, ***dummy source structure 178 includes a dummy source hole filled with conductive materials as a contact 179.*** Dummy source structure 178 can further include a spacer 177 made of any suitable dielectric materials (e.g., silicon oxide) between contact 179 and memory stack 160 to electrically separate surrounding conductive layers 106 in memory stack 160 from contact 179. As a result, dummy source structures 178 can laterally separate 3D memory device 100 into multiple memory regions, such as memory blocks.’

Id., 514-15 (emphasis added). The Applicant reiterated that the claimed “dummy source structure” includes “a contact” made of “conductive materials,” and that Jeong’s structure made solely of “insulating layers,” a layer containing a “semiconductor pattern,” and a “charge storage layer” did not meet this criterion. *Id.* In making this argument, the Applicant cited to a section of the specification that additionally states that the claimed “dummy source structure” ***can*** function to “laterally separate” the three-dimensional memory device into “multiple memory regions” ***to the extent that*** the “dummy source structure” includes “a spacer [] made of any suitable dielectric materials,” such as “silicon oxide,” situated “between contact 179 and memory stack 160.” *Id.* Neither the spacer nor the functionality of

laterally separating the memory device into regions of memory is recited in any of the independent claims of the '872. As such, these features were not necessary to overcome the prior art of record.

The Examiner subsequently allowed all pending claims and did so after reviewing four additional prior art references identified by the Applicant in a later-submitted Information Disclosure Statement.² Ex. 1002 (Part 2 of 2), 1-6 (10/26/2020 Notice of Allowance), Ex. 1002 (Part 2 of 2) 1-2 (10/30/2020 Information Disclosure Statement), Ex. 1002 (Part 2 of 2), 236-37 (11/9/2020 Notice of Allowance) (“The reasons for allowance have not changed since the previous Office Action (Notice of Allowance, mailed on 10/26/2020).”). The Examiner stated in the Reasons for Allowance that the prior art of record does not teach or render obvious the limitation “*wherein each of the dummy source structures comprises a*

² Petitioner incorrectly asserts that “Examiner did not consider any prior art references in connection with or following the August 14, 2020 claim amendments.” Pet., 22-23. An Information Disclosure Statement, which identified an additional four foreign patent documents, was submitted by Applicant on October 30, 2020, complied with the provisions of 37 C.F.R. § 1.97, and was considered by the Examiner. Ex. 1002 (Part 2 of 2) 1-2 (10/30/2020 Information Disclosure Statement), Ex. 1002 (Part 2 of 2), 237 (11/9/2020 Notice of Allowance).

conductive contact.” Ex. 1002 (Part 2 of 2), 7 (10/26/2020 Notice of Allowance) (emphasis in the original). The Examiner further stated, “the individual limitations may be found in a plurality of prior arts but there is no motivation to combine,” and “[b]ecause no reference alone teaches all the limitations, nor is there any motivation to combine the prior arts to construct all the limitations of” independent pending claims 1 and 8, the independent claims are “deemed patentable over the prior arts.” *Id.*, 7-10. The ’872 issued on December 8, 2020 with twenty claims. Ex. 1002 (Part 2 of 2), 272 (Issue Notification).

IV. CLAIM CONSTRUCTION

The Board construes claim terms “using the same claim construction standard that would be used to construe the claim in a civil action.” §42.100(b). Under this standard, claim terms are “generally given their ordinary and customary meaning” to a person of ordinary skill in the art. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). A person of ordinary skill in the art (“POSITA”) ascertains the meaning of the claims based on the claim language, specification, prosecution history, and relevant extrinsic evidence, although the claims and patent specification are the primary sources for construing claims. *Id.*, 1314-16.

The parties have not yet exchanged proposed claim constructions in the parallel district court proceeding. The Petition raises proposed constructions for two terms: “dummy source structure” and “surrounding,” which Patent Owner addresses

below. Other than the terms “dummy source structure” and “surrounding,” Patent Owner submits that constructions of the claim terms are not necessary to assess whether the prior art reads on the Challenged Claims for the purposes of institution. Patent Owner, however, reserves the right to modify its proposed constructions and to raise further claim construction issues if the Board institutes IPR, and to raise claim construction issues in the underlying district court proceedings.

A. “dummy source structure” (Claims 1-6, 11-13)

The term “dummy source structure” should be construed according to its plain and ordinary meaning as a structure that does not function as a source. Petitioner proposed construing this term as “structure[s] that occupies the void that was used for the gate replacement process,” but Petitioner’s proposal fails to differentiate between “dummy” source structures and non-dummy source structures and would impermissibly limit the language of an apparatus according to the process by which the apparatus is made.

1. Patent Owner’s Construction Is Supported by the Intrinsic Evidence

Consistent with the plain and ordinary meaning and the intrinsic record, “dummy source structure” should be construed as a structure that does not function as a source to the memory cells. The claim term at issue is “dummy source structure” rather than “source structure,” and Patent Owner’s construction properly gives meaning to the word “dummy.” Moreover, the ’872 teaches that the dummy

source structures do not function as a source to the memory cells. For example, the “dummy source structures”—as the qualifying term “dummy” suggests—“function[] as a mechanical supporting structure.” ’872, 16:38-44. And while the ’872 teaches that the dummy source structures may function as “interconnects to connect 3D memory device 100 with *other* peripheral devices,” the ’872 nowhere describes the dummy source structure functioning as a source to the memory cells. *See, e.g.*, ’872, 5:40-43, 11:46-49. As the specification explains, the dummy source hole is filled with “dielectric materials, conductive materials, or any combination thereof” so that a “dummy source structure 246 including spacer 242 and contact 244 is thereby formed in the dummy source hole.” Ex. 1001, 16:28-31, 16:56-63. “When conductive materials are used to fill dummy source hole 212 (e.g., contact 244), the dummy source structure 246 may function as an interconnect to connect 3D memory device 100 with other peripheral devices,” and “[w]hen dielectric materials are used to fill dummy source hole 212, dummy source structure 246 may function as a mechanical support structure to improve the stability of the staircase region.” Ex. 1001, 16:63-17:3. At no point does the specification suggest that a dummy source structure can function, in contradiction to its name, as a source to the memory cells. As such, “dummy source structure” should be construed as a structure that does not function as a source to the memory cells.

2. Petitioner’s Proposed Construction Fails to Give Meaning to “Dummy” Source Structure, and Improperly Limits the Term to a Process of Manufacture

Petitioner’s proposal that “dummy source structure” should be construed as a “structure that occupies the void that was used for the gate replacement process” fails to differentiate between “dummy” source structures and non-dummy source structures, and would impermissibly limit the language of an apparatus according to the process by which the apparatus is made.

First, Petitioner’s proposed construction is improper because it ignores the plain meaning of the term and fails to differentiate between dummy source structures and non-dummy source structures (*i.e.*, actual source structures that function as the source for memory cells). Indeed, structures that occupy (or are formed from) voids used for gate replacement processes can be either dummy source structures, if they do not function as a source, or source structures if they do function as a source for the memory cells. Petitioner ignores the distinction between the two types of structures and their functions. A dummy source structure was a type of dummy structure that was used for the purposes of improving integrated circuit functionality and manufacturing yield. For example, dummy structures mimic the physical properties of non-dummy structures, but do not perform the primary function of its non-dummy counterpart—functioning as the source. Instead, dummy structures can serve, for example, as load-bearing

structures during semiconductor device fabrication, which reduces mechanical stress on non-dummy structures during fabrication. '872, 5:5:21-48. For instance, while dummy source structures may be comprised of conductive material and thus may function, *e.g.*, as an “interconnect between the 3D memory device and peripheral devices” ('872, 5:37-43), they do not function as the source for memory cells. Petitioner’s proposed construction ignores this key difference and does not properly distinguish between dummy and non-dummy source structures.

Second, Petitioner’s proposed construction impermissibly attempts to limit the language of an apparatus—here, the claimed three-dimensional memory device—in such a way as to dictate the process by which the apparatus is made. As the Federal Circuit has held, “[a] novel product that meets the criteria of patentability is not limited to the process by which it was made.” *Vanguard Prods. Corp. v. Parker Hannifin Corp.*, 234 F.3d 1370, 1372-73 (Fed. Cir. 2000). And, while “process steps can be treated as part of a product claim if the patentee has made clear that the process steps are an essential part of the claimed invention,” that is not the case here. *See Cont’l Circuits LLC v. Intel Corp.*, 915 F.3d 788, 799 (Fed. Cir. 2019).

Here, the Challenged Claims are directed to an apparatus—not a product by process or method of manufacture. Indeed, as discussed in connection with §III, during prosecution Applicant expressly elected to restrict the invention to the

claimed 3D memory device to the apparatus itself, and not to any process by which the device or its features are made. Ex. 1002 (Part 1 of 2), 458 (5/21/2020 Requirement for Restriction/Elections).

Third, Petitioner also has not shown that the “gate replacement process” required by its construction is an essential part of the claimed invention such that it should be read into the claims through the construction of “dummy source structure.” Petitioner does not cite to any lexicography or disclaimer that would support such a construction. Instead, Petitioner relies on one disclosure, which, in full, reads:

“Also, the arrangement of the dummy source structures may allow the gate electrodes/word lines to be formed with improved uniformity and quality, reducing the resistivity of the gate electrodes/word lines. ***For example, the gate-replacement process can be performed to deposit a conductive material through the dummy source holes that subsequently form the dummy source structures.*** Because the conductive material travels shorter distances to fill up the lateral recesses for forming the gate electrodes, the gate electrodes are less susceptible to voids or density nonuniformity.”

Pet., 25 (citing ’872, 5:49-58) (emphasis added). This statement, on its face, is merely an “***example***” of how the claimed dummy source structures “***can***” be

formed and does not suggest that “a gate-replacement process” is an essential part of the claimed invention. Indeed, the specification repeatedly qualifies the use of the “gate-replacement process” as merely one possible manufacturing method. *See e.g.*, ’872, 4:30-33 (“[A] gate-replacement process is *often* used”), 5:52-55 (“the gate-replacement process *can* be performed to deposit a conductive material through the dummy source holes”), 16:40-49 (“*In some embodiments* ... dummy source structure 246 *may*...function[] as a mechanical supporting structure after gate-replacement process.... *In some embodiments*, ... dummy source structure 246 *may* ... still reach the lower part of the dielectric stack to carry out the gate-replacement process.”). In addition, the ’872 teaches that the dummy source structures can be formed a number of ways using “one or more thin film deposition processes including ALD [atomic layer deposition], CVD [chemical vapor deposition], PVD [physical vapor deposition], any other suitable processes, or any combination thereof.” Ex. 1001, 13:55-64; *see also* Ex. 1001, 12:34-36 (defining acronyms), 19:61-20:2 (explaining that “Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s)” and that the “breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the [] claims and their equivalents”).

Finally, Petitioner’s construction attempts to impermissibly narrow the scope of the claim by limiting it to one particular disclosed embodiment: gate replacement process. *See In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1369 (Fed. Cir. 2004) (“We have cautioned against reading limitations into a claim from the preferred embodiment described in the specification, even if it is the only embodiment described, absent clear disclaimer in the specification.”); *see also*, *Superguide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004); *Liebel-Flarsheim Co. v. Medrad Inc.*, 358 F.3d 898, 906 (Fed. Cir. 2004) (discussing recent cases wherein the court expressly rejected the contention that if a patent describes only a single embodiment, the claims of the patent must be construed as being limited to that embodiment).

For each of these reasons, the Board should reject Petitioner’s to construe “dummy source structure” as a “structure that occupies the void that was used for the gate replacement process.”

B. “surrounding” (Claims 1, 13)

The term “surrounding” should be given its plain and ordinary meaning, which, contrary to Petitioner’s arguments, requires features that are more than just on two sides with another structure “between.”

As an initial matter, the Board need not resolve the full scope of “surrounding” and need not determine whether it requires “fully encircling.”

Petitioner has alleged that the claimed “plurality of dummy source structures surrounding the staircase contact” of Claim 1 is satisfied “by structures on two sides” of the object. Pet., 61; *see generally* Pet., 50-62. Similarly, Patent Owner’s arguments directed to this limitation (§VI.A.1) turn on whether “surrounding” encompasses structures on only two sides. Thus, the Board need only resolve whether “surrounding” encompasses structures on only two sides. The Board does not need to reach Petitioner’s purported clarification that “surrounding” does not “require fully encircling” because the Board is required to construe terms “only to the extent necessary to resolve the controversy.” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019).

The term “surrounding” does not encompass features that are merely on two sides. First, the claim term at issue is “surrounding” rather than “between.” Indeed, the claims expressly distinguish the concepts of “surrounding” and “between.” The term “between” is used when reciting the concept of being located in the middle of two structures and “surrounding” is used when reciting the concept of being located in the middle of more than two structures. *Compare* ’872 Claim 17 (“wherein at least *one dummy channel structure is surrounded by at least eight dummy source structures*”) with ’872, Claim 11 (“wherein at least *one dummy source structure is located between the first and second staircase structure*”); *see also, e.g.*, Claim 12, Claim 15, Claim 16.

The '872 specification likewise repeatedly uses the terms “surrounding” and “between” to describe different concepts. As in the claims, the specification uses “between” when discussing the concept of being located in the middle of two structures and “surrounding” when discussing the concept of being located in the middle of more than two structures:

As shown in FIG. 1A, multiple dummy source structures, such as the four dummy source structures indicated by a diamond shape 146, may surround a staircase contact, such as staircase contact 122. ... [¶] ... A plurality of dummy channel structures, such as the four dummy channel structures indicated by square shape 148, may surround a staircase contact. The four dummy channel structures may be spaced with nominally equal lateral distances to the staircase contact, as shown in FIG. 1A. In other words, the dummy channel structures surrounding a staircase contact may be evenly distributed around the staircase contact. ... [¶] ... In some embodiments, at least one dummy source structure may be located between two staircase contacts. For example, FIG. 1A shows that two dummy source structures are located between staircase contacts 122 and 122'. FIG. 1B shows another embodiment in which two dummy source structures are located between staircase contacts 123 and 123', while one dummy source structure is located between staircase contacts 123' and 123". FIG. 1C shows yet another embodiment in which one dummy source structure is located between staircase contacts 125 and 125', and one dummy source structure is located between staircase contacts 125' and 125". Other numbers of dummy source structures may also be disposed between two staircase

contacts.”

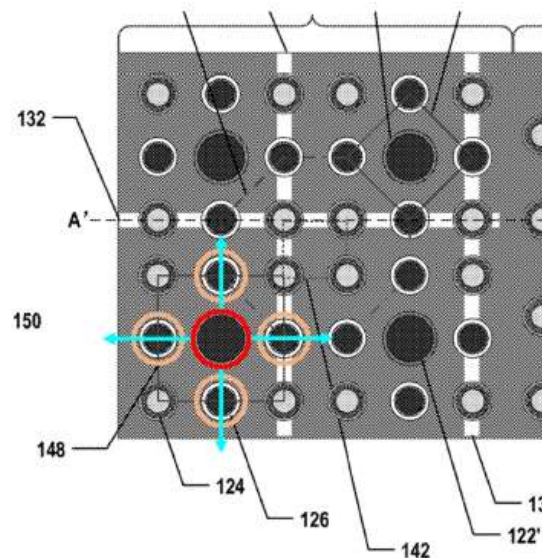
’872, 6:38-7:28 (emphasis added). This distinction is used consistently throughout the specification, including when the structures are slits. ’872, 4:56-61 (“*[D]ummy channel holes are formed between adjacent GLS*”).

Nothing in the ’872 teaches that a staircase contact can be “surrounded” by just two dummy source structures. If structures placed on only two sides of an object was within the scope of the plain meaning of “surrounding,” then there would have been no need for the ’872 to consistently use different terminology—“located between”—when there are structures on just two sides.

Petitioner’s argument that the specification contemplates “less than four dummy source structures that ‘surround’ a word line contact” (Pet., 28 (citing ’872 8:8-11)) is irrelevant. The dispute is not whether less than four (*e.g.*, three) dummy structures can “surround” a word line contact, the dispute is whether exactly two parallel dummy structures can “surround” a word line contact.

Petitioner argues that Figure 1A demonstrates that “surrounded includes being able to draw four lines outward from the staircase contact with each line being separated from the others by 90 degrees and intersecting a dummy source structure” (Pet., 30), but this argument is convoluted and a far departure from the plain meaning of “surrounding.” Even if “surrounding” was defined by some minimum angle between structures (as described by Petitioner), Figure 1A

illustrates a separation of 90 degrees from the *center* of such structures:



Pet., 31 (Petitioner’s annotations). Thus, this configuration disclosed in the specification with four dummy source structures at 90 degrees is different from—and does not provide support for—a configuration having only two dummy structures, *i.e.* where the angle is 180 degrees.

Finally, Petitioner’s extrinsic evidence should be given little weight. Petitioner fails to explain the relevance that a lay description of an “isthmus” (provided by the website “<https://www.studycountry-com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-sides>” in March of 2024) has to the meaning of “surrounding” as used by the ’872. Pet., 32 (citing Ex. 1018). Similarly, Petitioner’s reliance on U.S. Pat. No. 9,530,492 (the “’492 patent”) is misplaced. Pet., 32 (citing Ex. 1019, 2:14-16). Although the ’492 patent states that “the conventional SBPI operations are strongly affected by the stored Vts of two

surrounding NAND cells dispersed in the adjacent left and right BLs” (Ex. 1019, 2:14-16), this passage is merely referring to the effects of NAND cells in the surroundings (*i.e.*, in the vicinity). The ’492 patent does not suggest that two NAND cells can surround SBPI operations. And even if Petitioner’s interpretation of the ’492 patent were correct, it cannot overcome the consistent usage of “surrounding” in the ’872 patent, consistent with the plain meaning.

V. BACKGROUND OF THE ASSERTED PRIOR ART

A. U.S. Patent No. 9,859,297 (“Park”) (Ex. 1005)

Petitioner does not contend that Park anticipates the Challenged Claims, and instead argues only that it renders obvious certain claims, including the sole independent Challenged Claim, Claim 1. Pet., 8, 40-74.

Park discloses aspects of a memory device upon which the ’872 improves. Park describes a semiconductor device including: a substrate having a cell region and stepped dummy region; a common source line (“CSL”); gate lines; insulating interlayer patterns; dummy patterns; and dummy source lines. Ex. 1005, 6:1-9:3, Figs. 1-2. Park’s semiconductor device includes both **common source lines**, which function as a common source for the memory cell (and are therefore not dummy source structures), and **dummy source lines** in the dummy region. Ex. 1005, 13:53-58, 23:1-4, Fig. 1, Fig. 13. As illustrated in Figures 1 and 13 below, **common source lines** extend in the “2nd direction,” and are spaced apart from each

other along the “3rd direction,” of the cell region; the **dummy source lines**, on the other hand, extend in the “3rd direction,” and are spaced apart from each other along the “1st direction,” of the dummy region:

FIG. 13

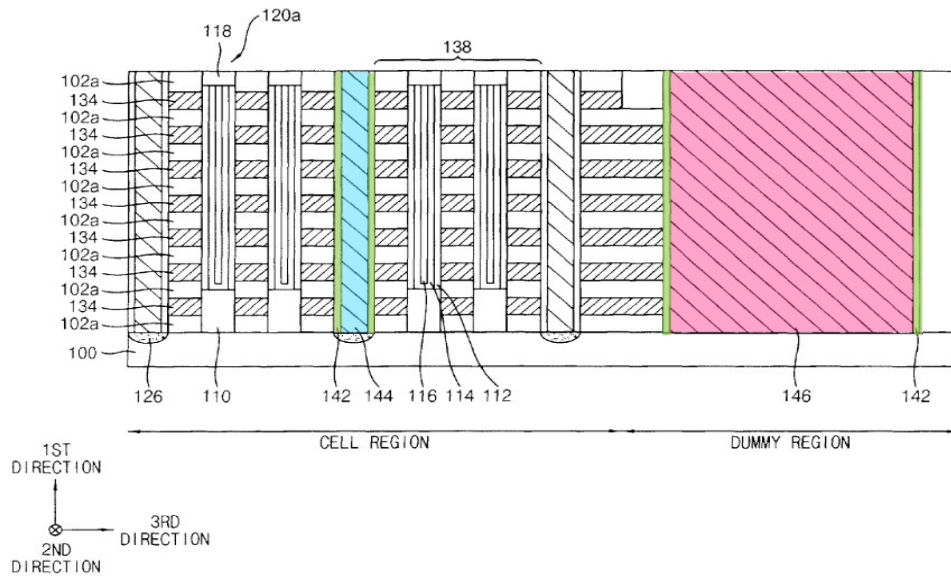
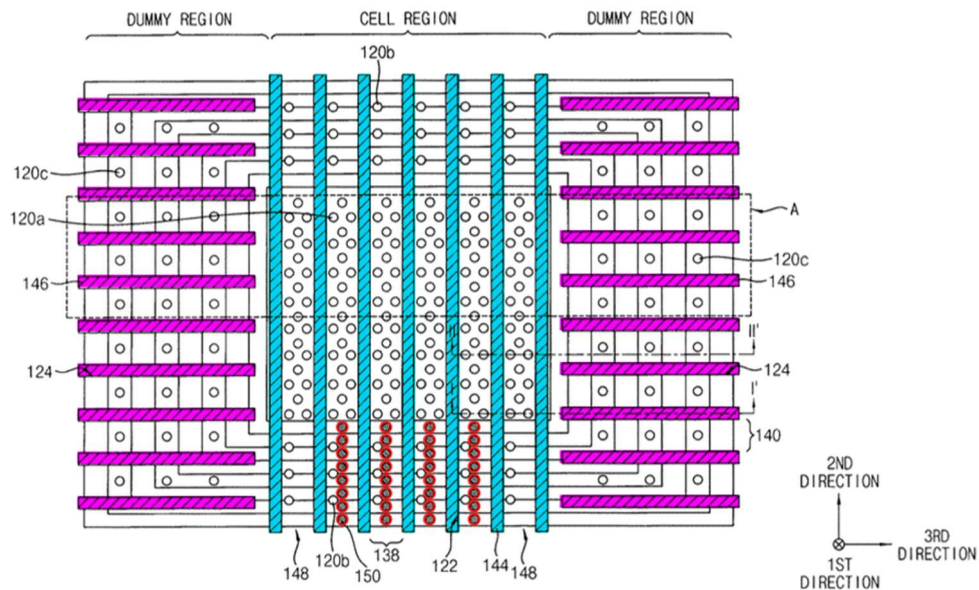


FIG. 1



Ex. 1005, Fig. 13, Fig. 1, 3:6-9.

Park further discloses that between the **common source lines** is a wiring region, where **contact plugs** (annotated in red in Figure 1 above) are formed in contact holes etched through the upper insulation layers and electrically connect to the gate lines. Ex. 1005, Fig. 1, 7:26-37, 13:60-54. Because Park's contact plugs are just between two **common source lines**, the **common source lines** do not surround the **contact plugs**. See Ex. 1005, Fig. 1. Park's **dummy source lines** also do not surround the **contact plugs** as shown above in Fig. 1.

B. U.S. Patent Pub No. 2019/0081061 ("Tessariol") (Ex. 1006)

Petitioner does not contend that Tessariol anticipates the Challenged Claims, and instead argues only that it renders obvious the Challenged Claims. Pet., 8, 74-101.

Tessariol discloses aspects of three-dimensional memory devices upon which the '872 claims improve. Ex. 1006, [0006]. Tessariol's circuit structure includes a stair step structure composed of **vertically-stacked alternating layers** (e.g., alternating layers of insulative material and conductive materials). Ex. 1006, [0029], [0031], [0034]. Dummy-structure openings and via openings are formed through the vertically-alternating layers. Ex. 1006, [0037]. Within via openings **operative conductive vias** are formed and within dummy openings **dummy structures** are formed—each extending through the **vertically-alternating layers**,

as depicted below. Ex. 1006, [0038].

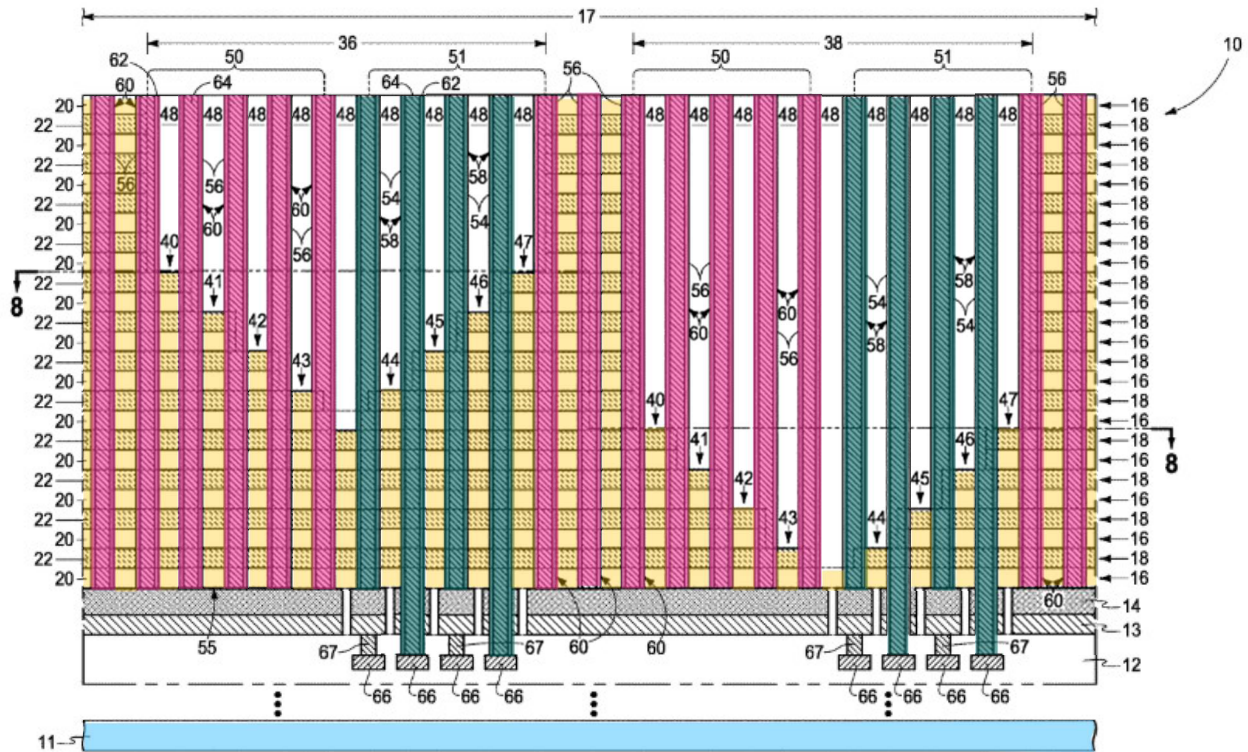


FIG. 9

Tessariol discloses that **operative conductive vias** and **dummy structures** may be composed of an **insulative lining** (e.g., silicon dioxide and/or silicon) and a **conductive core**, as depicted below. Ex. 1006, [0038]. Whereas the **operative conductive vias** may “directly electrically couple to individual conductive lines,” Tessariol does not disclose that the **dummy structures** can comprise a conductive contact. As Tessariol explains, “[i]n this document, a ‘dummy structure’ refers to a structure which is used to mimic a physical property of another structure (e.g., presence, or physical load-carrying/supporting ability of *an operative structure*) and which may comprise a circuit inoperable electrical dead end (e.g., is not part

of a current flow path of a circuit even if conductive).” Ex. 1006, [0068]

(emphasis added). In other words, while dummy structures may be conductive, they are not part of a circuit because they only mimic the physical properties (not the functional properties) of their operative counterparts. Consequently, even as electrical dead ends, dummy structures do not have a conductive contact.

Tessariol additionally discloses **operating conductive vias**, depicted in the color-annotated below:

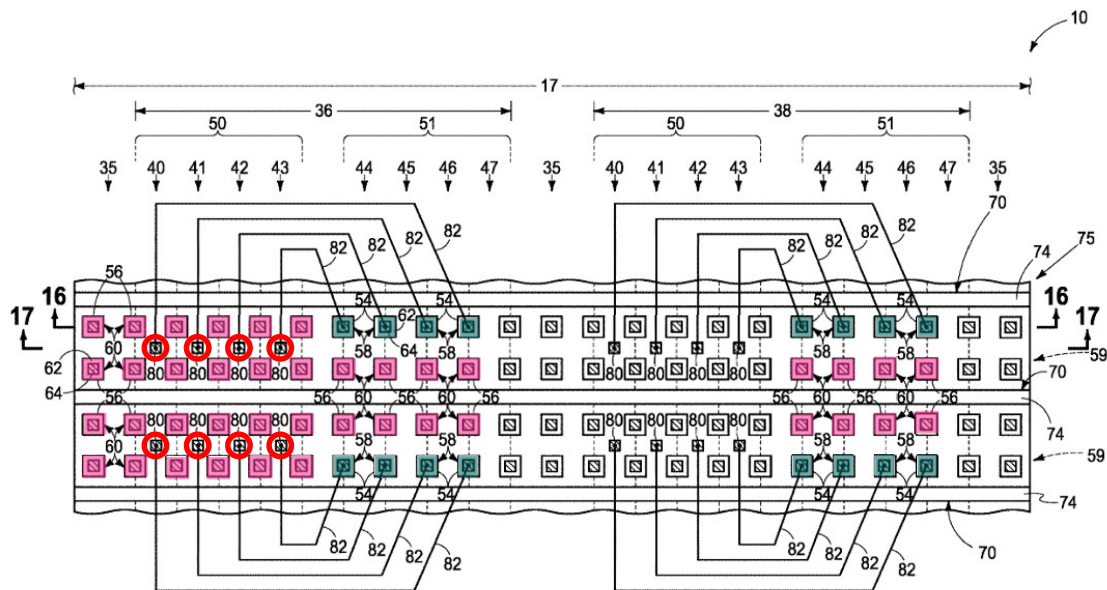


FIG. 15

These **operating conductive vias** each connect to a conductive step of the **vertically-alternating layers**, extend through the layers, and are “directly electrically coupled to one another by an interconnect line” above the alternating layers. Ex. 1006, [0046], [0052].



VI. PETITIONER FAILS TO ESTABLISH A REASONABLE LIKELIHOOD THAT IT WOULD PREVAIL WITH RESPECT TO THE CHALLENGED CLAIMS

Petitioner fails to establish a reasonable likelihood that it would prevail with respect to the Challenged Claims because Petitioner has failed to show that the prior art discloses or renders obvious the limitations of the Challenged Claims relating to the “dummy source structures.” As explained below, Petitioner cites two references—Park and Tessariol—and asserts that each one individually shows these features. Each of Petitioner’s arguments fails.

First, Park does not render obvious the Challenged Claims. Park does not disclose or render obvious that its alleged dummy source structures are

“surrounding the staircase contact” as required by the Challenged Claims because the contact is merely “between” the alleged dummy source structures, and under the proper construction of “surrounding” (§IV.B), it is insufficient to be merely “between” two dummy source structures. In addition, Petitioner has not shown that Park discloses or renders obvious “dummy source structures” because the purported dummy source structures function as a source and are therefore not “dummy source structures” as properly construed.

Second, Tessariol does not render obvious the Challenged Claims.

Petitioner has not shown that Tessariol discloses or render obvious that the alleged “dummy source structures” comprise a “conductive contact,” because there is no evidence of such a contact, and Petitioner’s argument for obviousness provides only a conclusory and illogical argument as a purported motivation to modify the reference. In addition, Petitioner has failed to show that Tessariol discloses or renders obvious “dummy source structures” under its incorrect construction and the plain and ordinary meaning of that term.

A. Ground 1: Park Does Not Disclose or Renders Obvious Multiple Independent Requirements of Limitation [1.e]

Petitioner fails to show that Park discloses or renders obvious limitation [1.e]: “a plurality of dummy source structures each extending vertically through the staircase structure, the plurality of dummy source structures surrounding the staircase contact.” Park’s common source lines and dummy source lines, alone or

collectively, are not “surrounding” the purported “staircase contact.” Instead, Park’s disclosures are nearly-identical to the very prior art that the invention of the ’872 improves upon. Moreover, Ground 1 is reliant on Petitioner’s incorrect construction for “dummy source structure” and the misunderstanding that this term is met by Park’s common source line—it is not.

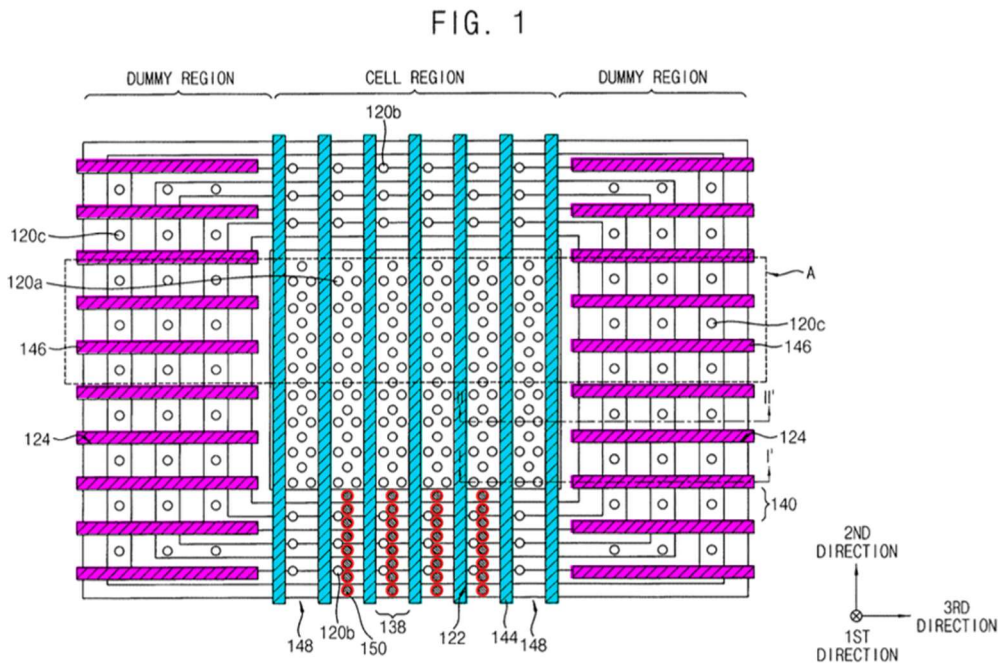
1. Park’s Common Source Lines and Dummy Source Lines, Alone or in Combination, Are Not “Surrounding” the Contact Plugs

Park’s alleged dummy source structures are not “surrounding the staircase contact” as required by the Challenged Claims because, under the proper construction of “surrounding” (§IV.B), it is insufficient for the alleged staircase contact to be merely “between” two dummy source structures.

All Challenged Claims require “the plurality of dummy source structures” to be “surrounding the staircase contact.” Petitioner maps the claimed “staircase contact” to a subset of Park’s contact plugs 150 (Pet., 48-49) and maps the claimed “dummy source structures” to Park’s common source lines 144 and dummy source lines 146, collectively. *See* Pet., 50-58. Although Petitioner argues that common source lines 144 and dummy source lines 146 collectively surround the contact plugs 150 (Pet., 58), Petitioner’s explanation focuses solely on the common source lines 144 alone. *See* Pet., 58-62. Nevertheless, the flaws in Petitioner’s arguments apply to both types of lines. Specifically, Petitioner argues that “[c]ommon source lines

144 alone surround the staircase contacts, and that is all that is necessary to satisfy claim 1.” Pet., 59-60.

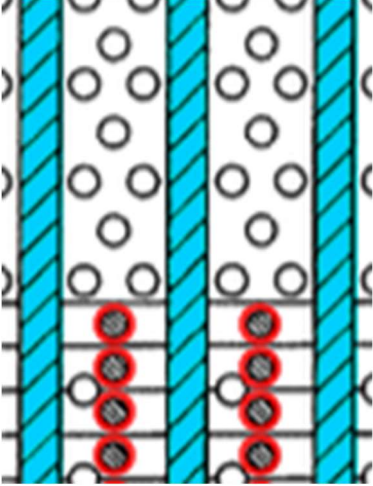
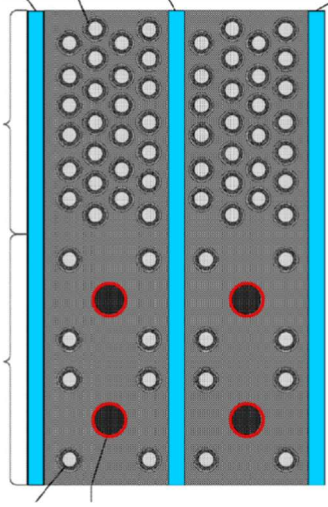
As a preliminary matter, Park’s **dummy source lines 146** do not “surround” the **contact plugs** as depicted below:



Park’s also common source lines 144 do not “surround” contact plug 150. As discussed in §IV.B, the plain meaning of the term “surrounding” is not satisfied by structures on two sides of an object that is merely between those two structures. Under the plain meaning, there is no dispute that Park’s common source lines 144 fail to disclose or render obvious this limitation.

Moreover, Petitioner overlooks that the configuration of Park’s common source line 144 and contact plug 150 is precisely the configuration that the invention

distinguished over the admitted prior art. Below is a side-by-side comparison of the relevant portions:

	
Excerpt of Petitioner's annotated Park, Fig. 1 (Pet., 59) (highlighting contact plugs 150 in red between parallel common source line 144 in orange). <i>See also</i> Ex. 1005, 2:46-47, 5:27-33, 6:15-17.	'872, Fig. 5 (rotated view of admitted prior art, illustrating staircase contacts 508 in red between parallel gate line slits 504 in green). <i>See also</i> Ex. 1001, 5:1-14.

The '872 discloses that the prior art GLSs extend through a staircase region that includes staircase contacts 508. Ex. 1001, 5:1-8. Similarly, Park's common source lines 144 cross through the wiring region that contain contact plugs 150. Ex. 1006, 13:62-64. The '872 discloses that characteristics of "the shape of GLS 504" is "a slit shape with a dimension along the extending direction (or the x-direction) much greater than the dimension along the expanding dimension (or the y-direction)." Ex. 1001, 5:23-25. Similarly, Park's common source lines 144 "extend in the

second direction” in “a plan view,” in which the “second direction [is] parallel to the top surface of the substrate,” and much greater than in the third direction. Accordingly, Park’s common source lines 144 geometry and arrangement are identical to that of the prior art GLSs that the ’872 improved upon. Notably, the ’872 patent uses the term “between”—not “surround”—to describe the “dummy channel holes [] between adjacent GLSs.” ’872, 4:56-57. Accordingly, Park discloses, at best, the same configuration of staircase contacts “between” parallel gate line slits, rather than “surround[ed]” by dummy source structures.

Thus, under the proper construction of “surrounding” as excluding features that are merely on two sides with another structure “between,” Park’s alleged dummy source structures are not “surrounding the staircase contact” as required by the Challenged Claims.

2. Park’s Common Source Lines Are Not “Dummy Source Structures”

Petitioner has not shown that Park discloses or renders obvious “dummy source structures” because the purported dummy source structures, Park’s common source lines, function as a source and are not “dummy source structures” as properly construed.

All Challenged Claims require “a plurality of dummy source structures.” As discussed in §IV.A, the claimed “dummy source structure” is a structure that does not function as a source. While Park discloses “dummy source lines,” Petitioner

instead maps the claimed “dummy source structures” to Park’s common source lines 144 (Pet.. 50-58). But Park’s common source lines 144 are not dummy source structures because they function as a source to the memory cells and are, therefore, actual—not dummy—source structures.

As an initial matter, while Petitioner alleges that Park’s common source lines 144 and dummy source lines 146 are collectively “a plurality of dummy source structures,” Petitioner maps *only* the common source lines to other limitations of the claims relating to the dummy source structure, such as the requirement that “the plurality of dummy source structures surrounding the staircase contact” as discussed above. Pet.. 50-62. For example, with respect to the “dummy source lines,” Petitioner has failed to show that they surround a contact plug as discussed above. And with respect to the “common source lines 144,” Petitioner must show that those particular alleged dummy source structures are in fact “dummy source structures.” They are not.

Park’s common source lines 144 are not “dummy source structure[s]” because they function as a source. Park expressly distinguishes between the “common source line” for the memory cell structure, which functions as the source line, and a “dummy source line.” *See, e.g.*, Park, 6:1-11, 7:59-60, 13:39-41. Similarly, the figures of Park show separate regions where the common source line and dummy source lines are located—the common source line is in the “cell region” and the

dummy source line is in the “dummy region.” Park, Fig. 1. Thus, Park’s common source lines 144 are not dummy source structures.

Petitioner incorrectly attempts to equate Park’s common source line to the ’872 patent’s teaching that “‘dummy source structures’ can [make] ‘contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices.’” Pet., 55-56 (omitting citations). Contrary to Petitioner’s suggestion, the ’872 patent’s disclosure that “dummy source structures” may “serve as an interconnect between the 3D memory devices and peripheral devices” (Ex. 1001, 5:40-43) does not suggest that Park’s common source line is also a dummy structure. Specifically, the interconnect referenced in the ’872 patent is not a source line. The ’872 explains that the “peripheral device” that the dummy source structure may connect to includes “peripheral circuits used for facilitating the operation of the 3D memory device 100, such as page buffers, decoders, and latches.” Ex. 1001, 9:37-40. As such, the ’872 “dummy source structure” does not function as a source to a memory cell. Park’s common source lines 144, on the other hand, do function as the source to memory cells, and therefore common source lines 144 are *actual* source structures and not “*dummy*” source structures.

B. Ground 2: Tessariol Does Not Disclose or Render Obvious Multiple Independent Requirements of Limitation [1.f]

Petitioner fails to show that Tessariol discloses or renders obvious multiple requirements of limitation [1.f]: “wherein each of the dummy source structures

comprises a conductive contact.” First, Tessariol does not disclose or render obvious that its alleged “dummy source structures” comprise a “conductive contact.” Petitioner relies on separate features that are not part of or even connected to the alleged “dummy source structures,” and its obviousness argument suggests adding upper-level interconnects to “dummy” structures without a rationale for doing so. Second, Petitioner has failed to show that Tessariol discloses or renders obvious “dummy source structures.” Under Petitioner’s proposed construction—“structure that occupies the void that was used for the gate replacement process”—Petitioner admits that “Tessariol’s dummy structures 60 and operative conductive vias 58 *do not fill the voids used for the sacrificial gate replacement process.*” Pet., 89 n.6 (emphasis added). In addition, under the plain meaning of “dummy source structures,” Petitioner has not addressed how the structures it maps to this limitation are “dummy” source structures as opposed to operative source structures that function as a source to the memory cells.

1. Tessariol’s Dummy Structures Do Not Comprise a “Conductive Contact”

Petitioner has not shown that Tessariol discloses or renders obvious that the alleged “dummy source structures” comprise a “conductive contact.” All Challenged Claims require that “each of the dummy source structures comprises a conductive contact.” Tessariol includes dummy structures 60, which are the only feature that Petitioner attempts to map to each requirement of the claimed “dummy

source structure.” Tessariol’s dummy structures 60, however, do not comprise a conductive contact, nor would it have been obvious to add one.

Petitioner maps Tessariol’s **dummy structures 60** (pink) *and* **conductive vias 58** (green), collectively, to the claimed “dummy source structures,” as annotated below.

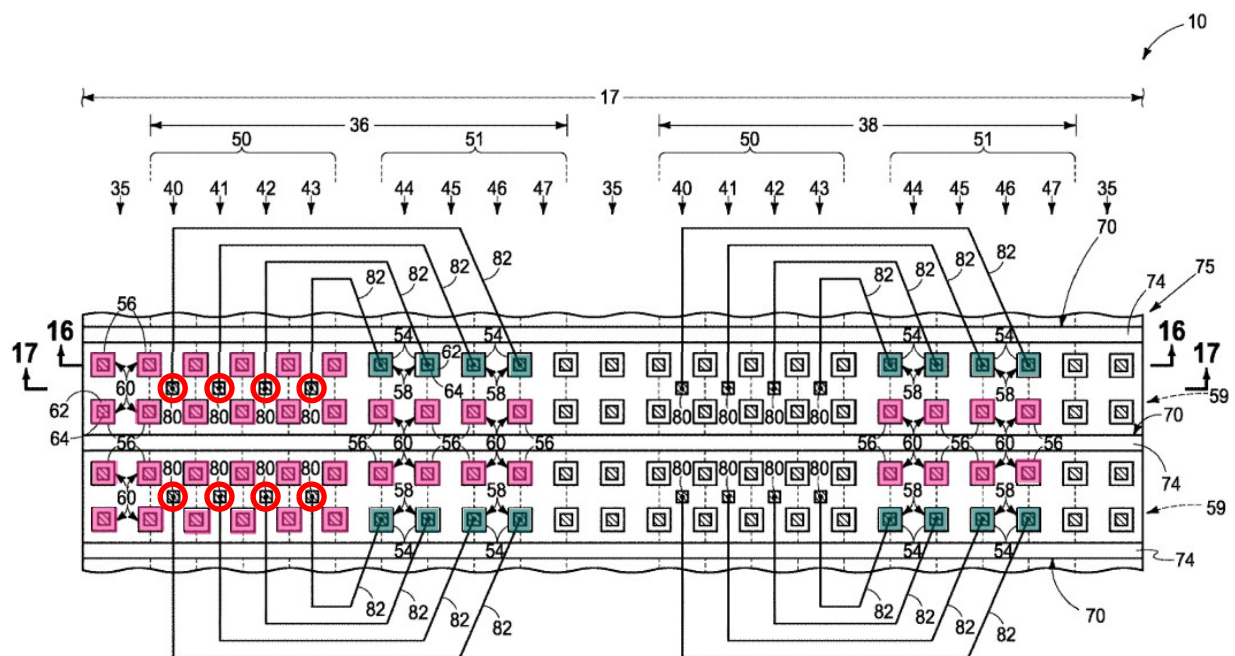


FIG. 15

See Pet., 82-86, Tessariol, Fig. 15. For the later limitation [1.e], Petitioner maps Tessariol’s **dummy structures 60** and **operative conducting vias** (red) to show “the plurality of dummy source structures surrounding the staircase contact.” See Pet., 87-88. Petitioner does not, and could not, argue that **conductive vias 58** are dummy source structures “surrounding” **operative conducting vias** (the alleged staircase contact). Thus, **dummy structures 60** are the *only* alleged “dummy source structure”

that Petitioner carries forward in its claim mapping. For this reason, it is vital to Petitioner’s argument that Tessariol teaches that **dummy structures 60**—the only alleged “dummy source structure” that Petitioner attempts to analyze for the full claim—comprises a conductive contact. It does not. It is irrelevant whether a separate component, such as **conductive vias 58**, comprises a conductive contact.

Thus, Petitioner has failed to show that **dummy structures 60** comprises a conductive contact, as required by the claims. Tessariol instead explains that while a “dummy structure” may be conductive, they are “not part of a current flow path of a circuit” because they only “mimic a physical property” (not the functional property) of “an operative structure.” Tessariol, ¶68. Consequently, dummy structures would not have a “conductive contact” as that is a functional property, not just a physical property, of the operative structure. *See* Ex. 2001, ¶¶39-46 (explaining that dummy structures with a “conductive contact” must “be appropriately conductive to be able to serve as an interconnect”).

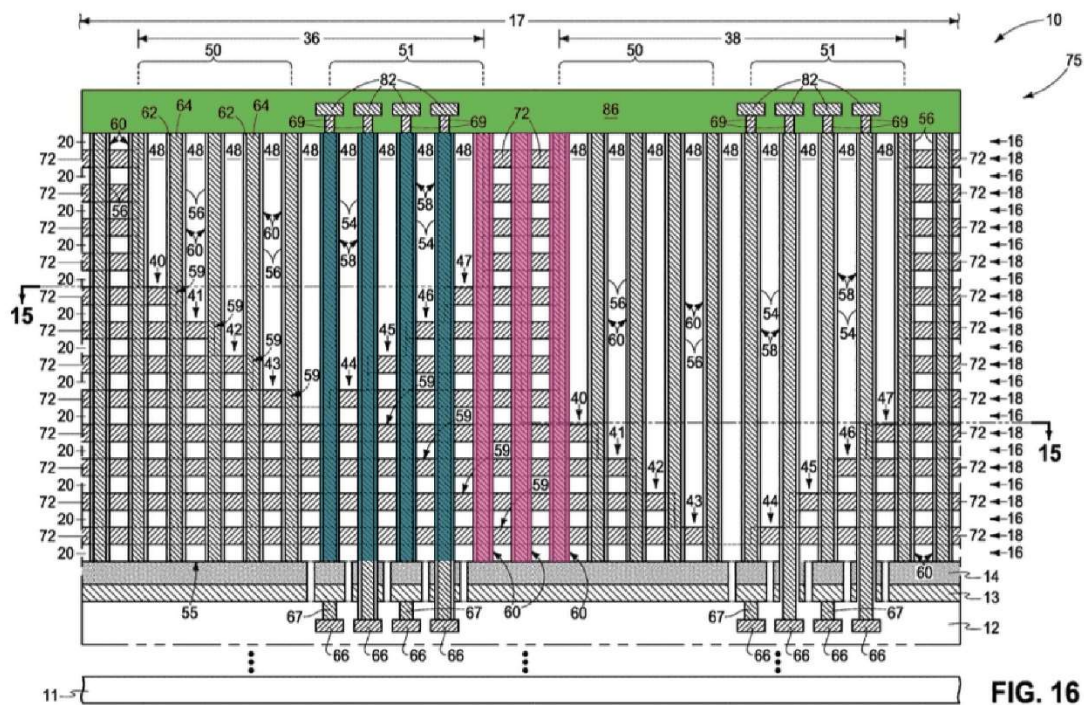
Petitioner’s assertion that the “claimed contact need not be a separate element from a conductive core” (Pet., 90) is misplaced. A conductive core alone does not teach a “conductive contact.” As shown in Figure 16 of Tessariol, even if the dummy structures are conductive, they land on a semiconductor. A POSITA would not consider the mere description of a metal contacting a semiconductor to meet the conditions for a “conductive contact” as outlined in ’872. Ex. 2001, ¶ 47; *see also*,

Ex. 2001, ¶¶48-51; Ex. 1001, 5:37-47. As Dr. Kuhn explains, a POSITA would not understand a metal-to-semiconductor contact to be a “conductive contact” “unless there is a clear description of how an ‘ohmic’ (*i.e.*, conductive) contact is formed between the metal and the semiconductor.” Ex. 2001, ¶¶ 52-54. Moreover, Petitioner does not explain why “dummy” structures would have had conductive contacts.”

Recognizing the weakness of its position, Petitioner further argues that “it would have been obvious for [*sic*] that the dummy source structures 60 **can** contact an upper-level interconnect.” Pet., 90 (emphasis added). As an initial matter, whether it is **possible** for dummy source structures 60 to contact an upper-level interconnect is not the proper test for obviousness. *See also* Ex. 1003, ¶215 (“In any event, in my opinion, it would have been obvious that the dummy source structures 60 **can** connect to an upper-level interconnect.”), ¶216 (“It would therefore have been obvious to a POSITA that dummy source structures 60 **can** include a contact that could connect to an upper-level interconnect.”). The question for obviousness is whether a POSITA would have been motivated to make this change. *In re Nuvasive, Inc.*, 842 F.3d 1376 (Fed. Cir. 2016). In any event, Petitioner has not shown a motivation to modify Tessariol to include conductive contacts. Indeed, Petitioner’s expert concedes that “interconnects 82 are simply not made on the dummy structures, because **there is no need for them** to connect to upper-level

devices.” Ex. 1003, ¶216.

Petitioner does not argue that POSITA would have been motivated to add upper-level interconnects to Tessariol's dummy structures 60 for any added functionality, but rather that by using the same process used to make conductive vias it would save time and cost (Pet., 90-91), but this argument is based on nothing more than conclusory expert testimony. Ex. 1003, ¶¶204, 216. Neither Petitioner nor its expert provides any explanation for how this modification would save process steps—because it would not. As shown below in Figure 16 of Tessariol, regardless of whether upper-level interconnects are added to **dummy structures 60** during the same process to make the interconnects 82 above the **operative conductive vias**, doing so would not eliminate any layer or patterning process:



Indeed, the same **insulating material** that covers the **dummy structures 60** without interconnects (see above) would still need to be deposited to fill the areas surrounding any added interconnects. And, contrary to Petitioner's argument, the additional design and materials for adding more upper-level interconnects would further complicate the design. So even if it were *possible* to add an interconnect to the dummy structures, Petitioner failed to identify any motivation for a POSITA to add upper-level interconnects to the top of the non-functional dummy structures 60.

Thus, Petitioner has not shown that Tessariol discloses or renders obvious that the alleged "dummy source structures" comprise a "conductive contact."

2. Petitioner Fails to Show That Tessariol Discloses or Renders Obvious "Dummy Source Structures"

Petitioner has failed to show that Tessariol discloses or renders obvious "dummy source structures" under its incorrect construction and the plain and ordinary meaning of that term.

First, Petitioner admits that Tessariol fails to meet the claims under its construction of "dummy source structures" as "structure that occupies the void that was used for the gate replacement process." Petitioner maps the claimed dummy source structures to Tessariol's dummy structures 60 and conductive vias 58, collectively. Pet., 82 (pertaining to limitation [1.e] reciting in part "a plurality of dummy source structures). By Petitioner's own admission, however, "Tessariol's dummy structures 60 and operative conductive vias 58 do not fill the voids used

for the sacrificial gate replacement process.” Pet., n. 6. As such, neither the dummy structure 60 nor operative conductive via 58 teaches a dummy source structure under Petitioner’s proposed claim construction of a “structure that occupies the void that was used for the gate replacement process.”

In addition, Petitioner has failed to identify features that would meet this limitation under the plain and ordinary meaning of “dummy source structure” as a structure that does not function as a source. *See* §IV.A. Indeed, Petitioner has not presented any analysis regarding whether the features it identifies satisfy this requirement. Petitioner maps the dummy structures 60 and conductive vias 58 together collectively as the claimed “dummy source structure,” but the conductive vias 58 are not referred to as “dummy” structures in Tessariol, and they are expressly described as “operative” conductive vias that are connected to the source. Tessariol, ¶39. Petitioner also has not addressed this requirement for Petitioner’s proposed modification to Tessariol’s dummy structures 60.

VII. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board deny institution.

Dated: July 29, 2024

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 complies with the type-volume limitation in 37 C.F.R. § 42.24(c)(1). According to the word-processing system's word count, the brief contains 8,714 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

Dated: July 29, 2024

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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Dated: July 29, 2024

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