

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

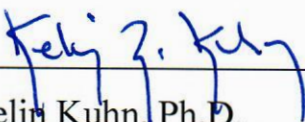
YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00789
Patent 10,861,872

**DECLARATION OF KELIN KUHN, Ph.D. IN SUPPORT OF PATENT
OWNER'S PRELIMINARY RESPONSE**

Executed this 29th day of July, 2024 in Winthrop, Washington.



Kelin Kuhn, Ph.D.

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I, Kelin Kuhn, Ph.D., hereby declare as follows:

I. INTRODUCTION

1. I have been retained by counsel for Yangtze Memory Technologies Company, LTD (“YMTC”) in the above captioned *inter partes* review of U.S. Patent No. 10,861,872 (Ex. 1001, “’872 patent”). I have been asked to consider the scope and content of the prior art, and respond to certain allegations regarding the prior art, presented by Micron Technology, Inc., (“Petitioner”) in its petition for *inter partes* review of the ’872 patent (“Petition”) and the April 17, 2024 Declaration of Dr. Sanjay Banerjee (Ex. 1003, “Liu”).

2. I am being compensated for my time at my usual consulting rate of \$600 per hour, plus reimbursement for any actual expenses. No part of my compensation depends on the content of the opinions that I herein render or on the outcome of this review proceeding. I have no expectation or promise of additional business with Patent Owner in exchange for the positions explained herein. I do not have any direct financial interest in any of the parties.

3. Unless otherwise noted, the statements made herein are based on my personal knowledge, and if called to testify about this declaration, I could and would do so competently and truthfully.

II. QUALIFICATIONS

4. My qualifications including cases in which I was an expert are stated more fully in my curriculum vitae which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

5. I received my B.S., magna cum laude, in Electrical Engineering from the University of Washington, Seattle in 1980, and received an M.S. and a Ph.D. in Electrical Engineering from Stanford University in 1985. I undertook post-doctoral work at Stanford from 1985 to 1987.

6. I am presently retired from industry. However, I still periodically engage in engineering projects for select clients and have a small business (Confluence Technology Services) to support that activity.

7. I am also currently an adjunct professor of Materials Science and Engineering at Cornell University, where my research interests are in the areas of quantum materials, post-CMOS technology, and spintronics.

8. For nearly a decade, beginning in 1987, I held faculty positions at the University of Washington, Seattle, beginning as a Research Assistant Professor in Material Science and Engineering, then as Assistant Professor in Electrical and Computer Engineering, and finally as a tenured Associate Professor of Electrical and Computer Engineering. During this period, I worked in III-V molecular beam

epitaxy and optoelectronics, and was awarded the University's highest accolade for a faculty member, the Distinguished Teaching Award, in 1995.

9. In 1997, I joined Intel Corporation ("Intel") at the Aloha Campus in Oregon as a Senior Process Engineer. I focused on front-end integration on the Intel 0.35 μ m process technology. In this role, I was responsible for the silicide section of the process flow, interaction with the reliability community, and integration on the CMOS camera chip project.

10. In 1999, I was transferred to Portland Technology Development at Ronler Acres, Oregon, as a Senior Process Engineer. I worked on front-end integration on the 130 nm CMOS generation. In this role, I was responsible for the isolation section of the process flow as well as integration of Optical Proximity Correction technologies into 130 nm.

11. In 2001, I advanced to the title of Principal Engineer. In 2002, I was promoted to the role of Process Program Manager for Intel's 90 nm communications process technology. Over a three-year period, my team developed a derivative analog/RF technology (including a SiGe bipolar junction transistor ("BJT")) on top of Intel's premium 90 nm microprocessor process.

12. In 2004, I advanced to the title of Senior Principal Engineer and was promoted to the role of Device Technology Manager of the pathfinding team at Intel that was responsible for the high-k metal-gate transistor architecture of Intel's

45 nm microprocessor processor technology. I received an Intel Achievement Award in 2006 for my work on the high-k metal gate.

13. In 2007, I achieved the title of Intel Fellow and became Director of Advanced Device Technology. Fellow is the highest level of technical achievement within Intel, with approximately 50 Fellows among approximately 100,000 total employees. My work evolved to a strategic role in overseeing the transition of advanced device technologies from research into development. In this role, I played an active part in the transfer of transistor technology for the 32 nm node, 22 nm node, and 14 nm node (the last two nodes involving Intel's FinFET device). I received a second Intel achievement award in 2008 for my work on Intel's FinFET device.

14. In 2009, my title remained the same, but my role transitioned from development (in Portland Technology Development, at Ronler Acres) to research (in the Components Research Group, still at Ronler Acres). From 2009 until my retirement from Intel in 2014, I researched advanced device architectures for Intel processes in the five-to-ten year time frame.

15. While much of my later work at Intel still remains confidential, certain aspects of my work during this period are featured in my book CMOS And Beyond: Logic Switches for Terascale Integrated Circuits (Co-Editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015), as well as in my paper "Considerations

for Ultimate CMOS Scaling” (IEEE Trans. on Elec. Dev., Vol. 59, No. 7, 2012), winner of the 2013 Paul Rappaport Award.

16. Since my retirement in 2014, my consulting work has included a variety of semiconductor related projects. While the detailed technical content is, of course, protected by client confidentiality, these projects include, FinFETs, vertical power transistors, solar cells, conventional (planar) MOS, and flash.

17. I am the author of more than 100 technical papers in electronics and photonics. I am currently the Associate Editor in Chief (AEiC) of IEEE Electron Device Letters, having served as an editor since 2015, and as AEiC since 2024.

18. A few of my other representative journal publications include: “Understanding the feasibility of scaled III–V TFET for logic by bridging atomistic simulations and experimental results,” (Symposium on VLSI Technology, 2012); “Process Technology Variation,” (IEEE Transactions on Electron Devices, Vol. 58, No. 8, 2011); “A 45 nm logic technology with high- k +metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging,” (2007 IEEE International Electron Devices Meeting); and “Comparison of Junctionless and Conventional Trigate Transistors With L_g Down to 26 nm,” (IEEE Electron Device Letters, Vol. 32, No. 9, 2011).

19. A few representative book chapters include, “The Magic of MOSFET Manufacturing,” Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8. Chapter 1, CMOS and Beyond CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS Applications”, Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616).
20. I am an inventor on approximately 80 granted U.S. patents in the field of semiconductor technology.
21. A few of my other relevant honors include being a Fellow at the Institute of Electrical and Electronics Engineers (“IEEE”), a recipient of the IEEE Frederik Philips Award (2016), a recipient of the IEEE Paul Rappaport Award (2013), the recipient of eleven Intel Divisional Awards, and election to the National Academy of Engineering (2023). Earlier in my career, I received the NSF Presidential Young Investigator Award.
22. As specifically relevant to this project, I want to highlight the 3’D gate-last vertical gate-all-around (GAA) devices and the 3’D vertical GAA arrays that are discussed at some length in “Considerations for Ultimate CMOS Scaling” (see Fig. 15 in particular). I also want to highlight on-going proprietary and confidential work, in the matter of Silicon Storage Technology, Inc. vs. Taiwan Semiconductor Manufacturing Company involving flash.

23. Attached as Exhibit 1 to this report is a current copy of my curriculum vitae, which outlines my academic, professional and experiential qualifications in the semiconductor and integrated circuit industries, as well as a list of publications I have authored and co-authored and presentations I have given.

III. MY ASSIGNMENT AND BASES OF OPINIONS

24. I have been asked to provide my opinions as to the scope and content of the '872 patent as well as the prior art presented by Petitioner and Dr. Banerjee in Ground 2 of the Petition. Specifically, I have been asked to opine on what a person of ordinary skill in the art would have understood the '872 patent to disclose and teach as it relates to the term “conductive contact,” and I have been asked to provide my opinions concerning whether Tessariol (Ex. 1006) discloses or renders obvious dummy source structures that comprise a “conductive contact.”

25. In the course of conducting my analysis and forming my opinions, I have reviewed the references and materials cited herein including those listed below:

Exhibit No.	Reference
N/A	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,861,872 (IPR2024-00789, Paper 1)
Ex. 1001	U.S. Patent No. 10,861,872 B2 to Liu et al.
Ex. 1002	File History of U.S. Patent No. 10,861,872 B2 to Liu et al.
Ex. 1003	Declaration of Dr. Sanjay Banerjee (“Banerjee”)
Ex. 1005	U.S. Patent No. 9,859,297 B2 to Park et al. (“Park”)
Ex. 1006	U.S. Patent Publ. No. 2019/0081061 A1 to Tessariol et al. (“Tessariol”)
Ex. 2003	Shur, “Introduction to Electronic Devices” (1996) (“Shur”)
Ex. 2004	Streetman, “Solid State Electronic Devices” (1995) (“Streetman”)

Ex. 2005	US Patent No. 8,766,336 (“Grupp”)
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26. My opinions in this declaration are based on my review of these documents, as well as upon my education, training, research, knowledge, and experience.

27. All emphases (such as bolding, underlying, or italics) appearing in quotations and citations cited herein have been added by me, unless otherwise stated.

IV. SUMMARY OF MY OPINIONS

28. It is my opinion, based on what a person of ordinary skill in the art would have understood the ’872 patent to disclose and teach as it relates to the term “conductive contact,” that Tessariol does not disclose or render obvious dummy source structures that comprise a “conductive contact.”

V. APPLICABLE LEGAL STANDARDS

29. I am not a legal expert and offer no opinions on the law. However, I have been informed by counsel of the various legal standards that apply, and I have applied those standards in arriving at my conclusions.

A. Ordinary Skill in the Art

30. My opinions in this declaration are based on the understandings of a person of ordinary skill in the art, which I understand is sometimes referred to as an “ordinary artisan” or by the acronyms “POSITA” (person of ordinary skill in the art) or “POSA,” as of the time of the invention.

31. I have been asked to consider the level of ordinary skill that someone in the field of technology of the '872 patent would have had at the time the claimed invention disclosed in the '872 patent was made. In determining the level of ordinary skill in the art, I considered the following: (1) the levels of education and experience of persons working in the field; (2) the types of problems encountered in the field; and (3) the sophistication of the technology.

32. In my opinion, a person of ordinary skill in the art capable of reading and understanding the claims of the '872 patent at the time of the invention would have had at least a bachelor's degree in electrical engineering, computer engineering, or a similar discipline, along with at least 2 years of professional experience with semiconductor memory devices, or an equivalent level of knowledge and experience. For example, an advanced degree may replace some of the professional experience, or extensive experience may replace some of the educational requirements.

33. In this case, Dr. Banerjee has asserted in his declaration that a person of ordinary skill in the art at the time of the invention described in the '872 patent would have a:

a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (*e.g.*, researching, designing, or teaching) monolithic 3D structures and NAND memory devices, or an equivalent level of skill, knowledge, and experience (*e.g.*, an advanced degree may replace some of the professional experience). This POSITA would have been aware of and generally knowledgeable about 3D NAND's structure, its component parts, how it operates, and how it is controlled.

Banerjee, ¶42.

34. In view of my educational background and years of experience, including my many years of experience developing and manufacturing MOS transistors, 3'D MOS transistors, monolithic 3'D gate-all-around transistors, and memory devices, I both met and exceeded the qualifications of a person of ordinary skill in the art as of the earliest possible priority date of the '872 Patent in February 2019. That is true under both my own definition of a person of ordinary skill in the art, as well as under Dr. Banerjee's definition, and my opinions as set forth herein are the same regardless of which definition of a person of ordinary skill in the art is applied.

B. Claim Construction

35. I understand that Patent Owner has proposed that the term "dummy source structure" is properly construed as a "structure that occupies the void that was used for the gate replacement process," and that the term "surrounding" (as it appears in independent claim 1 as "the plurality of dummy source structures surrounding the staircase contact") would not have been understood to require that the dummy source structures form a border that fully encloses the staircase contact. I understand that these are the only terms Patent Owner proposes for construction in its Preliminary Response.

36. I also understand that the parties have identified proposed terms to be construed in the district court case that is proceeding in parallel with this requested IPR, but that the parties have not yet exchanged proposed claim constructions. At this time, I have not been asked by Patent Owner to provide an opinion on claim construction in either the requested IPR or in the parallel district court proceedings.

37. Where applicable, I have been instructed to apply Patent Owner's proposed construction of the terms "dummy source structure" and "surrounding" when rendering my opinions. However, my opinions below do not depend on the particular construction of these terms. For all other terms, I have applied the plain and ordinary meaning of the claims consistent with the intrinsic evidence.

VI. SCOPE AND CONTENT OF THE '872 PATENT

38. I understand that Petitioner and Dr. Banerjee assert that claims 1-6 and 11-13 of the '872 patent are obvious over Tessariol (Ex. 1006). Petition at 74-101; Banerjee, ¶¶179-232. I have been asked to opine on the scope and content of the '872 patent and what a person of ordinary skill in the art would have understood the '872 patent to disclose and teach as it relates to the term "conductive contact."

A. "Conductive contact"

39. The term "conductive contact" appears in the asserted claims of the '872 patent. *See, e.g.*, '872, claims 1 (limitation [1.f] reciting "wherein each of the dummy source structures comprises a conductive contact") and 13 (reciting in

part “wherein the conductive contact comprises a conductor layer”). In the following paragraphs, I discuss what a person of ordinary skill in the art would have understood the ’872 patent to disclose and teach as it relates to the term “conductive contact,” and whether Tessariol discloses or renders obvious a “conductive contact.”

(a) The term “conductive contact” as used in the ’872 patent

40. The term “conductive contact” is used once in the of ’872 patent specification and asserted claims. The usage in the specification is important for understanding the context and is as follows: “Each dummy source structure may include an insulating spacer layer in a dummy source hole and a conductive contact within the spacer layer. In some embodiments, one or more dummy source structures are in contact with the substrate and may provide interconnect between the 3D memory device and peripheral devices.” ’872, 5:37-47.

41. There are also three usages of the term in the claims of the ’872 patent. One use in the claims provides additional clarification on the composition of the conductive contact: “wherein the conductive contact comprises a conductor layer.” ’872, Claim 13. Two uses in the claims are identical and relate the dummy source structure to the conductive contact: “wherein each of the dummy source

structures comprises a conductive contact” (’872, Claim 1), and “wherein each of the dummy source structures comprises a conductive contact” (’872, Claim 14).

42. The usage in the specification is the primary usage for understanding the context of “conductive contact” in the ’872 patent. Taking a closer look at the usage of the phrase “conductive contact” in the specification, there are three important features. **First**, the conductive contact is included in the dummy source structure as: “Each dummy source structure may include an insulating spacer layer in a dummy source hole and a conductive contact within the spacer layer.” ’872, 5:37-40. **Second**, the dummy source structure is in contact with another structure as “one or more dummy source structures are in contact with the substrate.” ’872, 5:40-41. **Third**, the dummy source structure is capable of serving as part of a circuit, as: “may provide interconnect between the 3D memory device and peripheral devices.” ’872, 5:42-43. Overall, in my opinion, a person of ordinary skill in the art would interpret the language of the ’872 patent specification (and claims) for conductive contact as requiring at least three key attributes: (1) it is a physical structure, (2) it is “in contact with” another structure (or layer), and (3) the final configuration meets the conditions necessary to appropriately “provide interconnect between the 3D memory device and peripheral devices” as described by the ’872 patent. ’872, 5:40-43.

43. A person of ordinary skill in the art would be fully aware that not all situations where a physical structure is “in contact with” another structure (or layer) would also meet the conditions necessary to be able to “provide interconnect between the 3D memory device and peripheral devices.” Examples of situations that would not meet the interconnect conditions include: **(1)** the physical structure itself is not appropriately conductive to serve as an interconnect, **(2)** the layer that the physical structure is “in contact with” is not appropriately conductive to serve as an interconnect, and **(3)** the contact region (contact interface) between the physical structure and the layer is not appropriately conductive to be able to serve as an interconnect.

44. Saying this another way, a person of ordinary skill in the art would have recognized that at least three conditions must be met simultaneously in order for a structure to meet the '872 patent's conditions of a “conductive contact.” More specifically, **(1)** the physical structure itself needs to be appropriately conductive to serve as an interconnect to peripheral circuitry, **(2)** the layer that the physical structure is “in contact with” needs to be appropriately conductive to serve as an interconnect to peripheral circuitry, and **(3)** the contact region (contact interface) between the physical structure and the layer needs to be appropriately conductive to be able to serve as an interconnect to peripheral circuitry.

45. The first two conditions (the physical structure needs to be appropriately conductive to serve as an interconnect, and the layer that the physical structure is “in contact with” needs to be appropriately conductive to serve as an interconnect) are quite similar. A person of ordinary skill in the art would have recognized that most metals would meet these two conditions, most insulators would NOT meet these two conditions, and that semiconductors (or semi-metals) may or may not meet these conditions based on certain factors discussed below.

46. The third condition (the contact region between the physical structure and the layer needs to be appropriately conductive to be able to serve as an interconnect) can be more complex, particularly if one material is a metal and the other a semiconductor, due to the complex physics that arises when two dissimilar materials are “in contact with” each other. This situation that occurs when a metal is in contact with a semiconductor is discussed in more detail in the following paragraphs.

(b) Contacts need to be “ohmic” to be useful in circuits

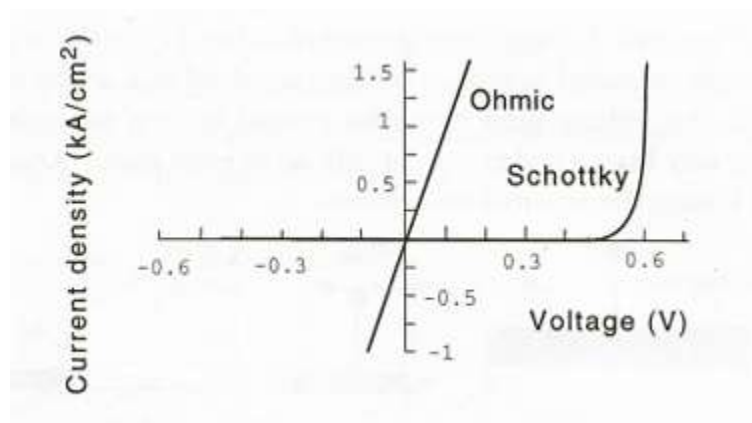
47. Typically, a contact between two dissimilar materials needs to be an “ohmic contact” in order to be capable of serving as an interconnect in a circuit. An “ohmic contact” is one where the I-V curve (current-voltage curve) is a straight line. As described in Chapter 4 (Diodes and Contacts), Section 4.9 (Ohmic

Contacts) in a textbook titled “Introduction to Electronic Devices” (Ex. 2003,
“Shur”):

All electronic devices have to be connected to the outside world in order to form an electronic circuit in combination with other circuit elements. [] These contacts need to be as unobtrusive as possible, so the current flowing through a semiconductor device, and hence, through the contacts, leads to the smallest parasitic voltage drop possible. Whatever voltage drop does occur across the contact has to be proportional to the current so that the contacts do not introduce uncontrollable and unexpected non-linear elements into the circuit. Since such contacts satisfy Ohm’s law, they are usually called ohmic contacts.

Shur (Ex. 2003), 256. Saying this another way, for a contact to be useful in a circuit, it needs to be an ohmic contact, which also means it needs to display a straight line on an I-V plot (*e.g.*, the voltage drop is proportional to the current).

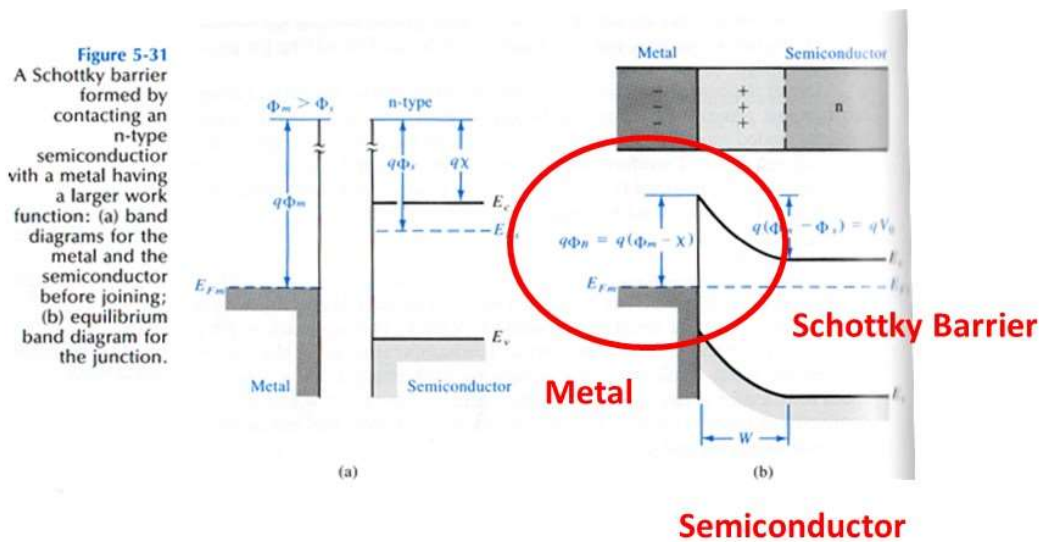
Shur illustrates this in Fig. 4.9.1 reproduced below:



Shur (Ex. 2003), 257. Fig. 4.9.1. illustrates the difference in the I-V curve between an ohmic contact and a Schottky (or rectifying) contact.

(c) **Metal-semiconductor contacts are typically not ohmic**

48. A contact between a semiconductor and a metal is typically not an ohmic contact. Rather, it is a diode (or rectifying) contact with an exponential (not linear) I-V characteristic. To understand this in more detail, I have reproduced Fig. 5-31 from a textbook titled, “Solid State Electronic Devices” (Ex. 2004, “Streetman”). Fig. 5-31 depicts the energy band diagram for the contact between a metal (left) and an n-type semiconductor (right):

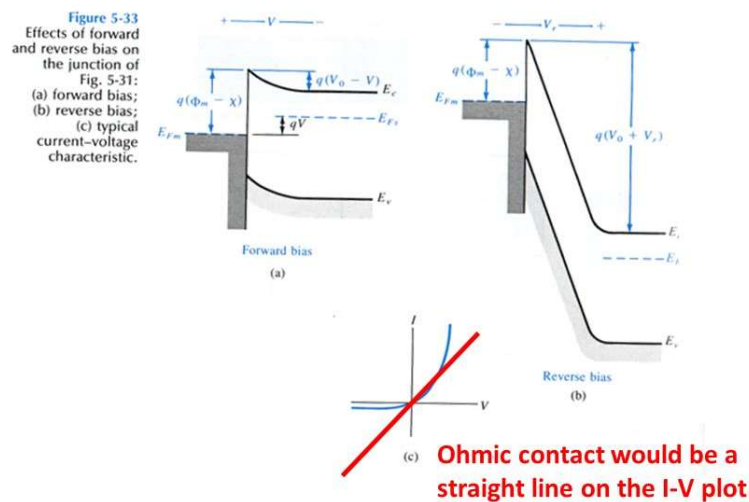


Streetman (Ex. 2004), 184. As I circle in red in the figure above, a Schottky barrier is formed between a metal and an n-type semiconductor.

49. Once the contact is made, there is an “energy barrier” (sometimes called a Schottky barrier) represented by Φ_m between the two materials. The current across this barrier is diode-like (it is much larger in one direction than the other) and can be represented by:

$$I_o \propto e^{-q\Phi_B/kT}$$

Streetman (Ex. 2004), 187. This is an exponential equation, not at all like the straight line required of an ohmic contact. The consequences of putting a voltage on this barrier are illustrated below—note, in particular, the non-linearity of the I-V graph in middle lower part of the illustration. This figure illustrates the rectifying (non-ohmic) behavior of a metal-semiconductor junction (Schottky junction).



Streetman (Ex. 2004), 186. I annotated the figure to include an ohmic I-V curve (in red) in the bottom center I-V curve for comparison.

50. In summary, a person of ordinary skill in the art would assume that an arbitrary metal-to-semiconductor contact is not ohmic, and thus not capable of serving as an interconnect in a circuit.

(d) Making ohmic contacts at metal to semiconductor junctions

51. A person of ordinary skill in the art would be aware that creating an ohmic metal-to-semiconductor contact requires special processing. A person of ordinary skill in the art would also be aware that special processing methods appropriate to the manufacturing environment fall into three categories namely: **(1)** heavily dope the semiconductor in the region immediately under the contact (if the semiconductor is n-type, the doping would then be heavily n-type or an n⁺ doping) (Streetman (Ex. 2004), 188-190); **(2)** form a silicide on the semiconductor surface (depending on the materials used, the silicide is either a metal or a semi-metal, and intentional engineering of the various materials can reduce or eliminate the Schottky barrier) (Streetman (Ex. 2004), 188-190); and **(3)** intentionally form a thin oxide layer on the surface of the semiconductor to eliminate Fermi-level pinning of the surface, but keep the barrier so thin that carriers can freely tunnel through the junction, typically called a MIS interface (US Patent No. 8,766,336 (Ex. 2005, “Grupp”), Abstract).

(e) The term “conductive contact” interpreted in light of metal-to-semiconductor junctions

52. As I described earlier, a person of ordinary skill in the art would have recognized that three conditions must be fulfilled to meet the ’872 patent description for “conductive contact.” These are: **(1)** the structure needs to be

appropriately conductive to serve as an interconnect, **(2)** the layer that the structure is “in contact with” needs to be appropriately conductive to serve as an interconnect, and **(3)** the contact region (contact interface) between the structure and the layer needs to be appropriately conductive to be able to serve as an interconnect.

53. A person of ordinary skill in the art would have recognized that an arbitrary metal-to-semiconductor contact will typically not meet the third condition (*e.g.*, the contact region between the structure and the layer needs to be appropriately conductive to serve as an interconnect) because an arbitrary metal-to-semiconductor contact is not an ohmic contact.

54. As such, a person of ordinary skill in the art would not consider the mere description of a metal contacting a semiconductor, as illustrated in Tessariol Figure 9, to meet the conditions for a “conductive contact” as outlined in ’872 patent. Even if the metal is identified (and thus known to be conductive) and the semiconductor doping is described (and thus known to be conductive), unless there is a clear description of how an “ohmic” contact (rather than a rectifying contact or Schottky contact) is formed between the metal and the semiconductor, the three required conditions are not met.

VII. CONCLUSION

55. For at least the reasons discussed above, I disagree with the arguments raised in the Petition regarding the scope and content of the '872 patent and Tessariol as understood by a person of ordinary skill in the art, and I disagree that a person of ordinary skill in the art would have understood that Tessariol discloses or renders obvious a conductive contact, as asserted by the Petitioner and Dr. Banerjee in Ground 2 of the Petition.

56. This declaration represents my opinions that I have formed to date on the specific issues for which I have been asked to opine and based on the material currently available to me. I reserve the right to supplement this declaration to address any new information offered by Petitioner or provided by the Board. Also, I reserve the right to supplement this declaration insofar as Petitioner is permitted to supplement the record with any additional opinions or arguments.

57. I hereby declare that all statements made herein of my own knowledge are true and all statements made herein on information and belief were and are believed by me to be true, and that all statements herein were and are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that any such willful false statements may jeopardize the validity of the application or any patents issued thereon.