CURRICULUM VITAE
Dr. Kelin J. Kuhn

CONTACT INFORMATION:

Kelin J. Kuhn
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EDUCATION:

Ph.D., Electrical Engineering, Stanford University, Stanford, CA. June 1985
M.S., Electrical Engineering, Stanford University, Stanford, CA. June 1985
B.S., Electrical Engineering, University of Washington, Seattle, WA. March 1980
(magna cum laude)

PRESENT ROLE:

Confluence Technology Services, Winthrop, WA (kjkuhn@confluence-tech.com); present role

Dr. Kuhn's business (Confluence Technology Services) supports a variety of engineering services in electronics and photonics, with emphasis on CMOS and beyond-CMOS technologies.

Cornell University, Ithaca, NY; Materials Science and Engineering (kjk236@cornell.edu) 2014 to date

Position: Adjunct Professor
Key Collaborator: Darrell Schlom

Prof. Kuhn's role is collaborating with a diverse group of faculty (both at Cornell and elsewhere) for establishment of long-term research programs in the area of valleytronics, inverse-design, quantum materials, post-CMOS technology, and spintronics.

CLIENTS / SIGNIFICANT INTERACTIONS POST-2014:

Keystone Strategy LLC: Initiated 2024 and on-going**.** Technical evaluation and consulting on matters related to *MicroSemi Corporation v. Commissioner of Internal Revenue*.

Ropes and Gray: Initiated 2023 and on-going**.** Technical evaluation and consulting on the matters related to *Yangtze Memory Technologies Company, LTD. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC, Case No. 5-23-cv-05792*.

YMTC Ex. 2002
Micron v. YMTC
IPR2024-00789 Page 1

Heim, Payne & Chorush: Initiated 2023 and on-going. Technical evaluation and consulting representing *Microchip Corporation* and its subsidiary *Silicon Storage Technology, Inc*. with regards to a dispute with *Taiwan Semiconductor Manufacturing Company*.

Smith Baluch LLP: Initiated 2022 and on-going**.** Technical evaluation and consultation to advise and assist Smith Baluch LLP matters relating to semiconductor processing.

Carter Arnett: Initiated 2022 and ongoing**.** Technical evaluation and consultation to advise and assist Carter Arnett PLLC in representing *Katana Silicon Technologies, LLC* in IPR2022-00763 and litigation related to Case No. 6:22-cv-00191 (W.D. Tex), adverse to *GlobalFoundries, Inc., GlobalFoundries, U.S. Inc., and GlobalFoundries U.S*. 2 LLC.

Mintz: Completed 2022-2023. Technical evaluation and consulting representing *Daedalus Prime LLC* with regards to the ITC Case: 337-TA-133, Certain Semiconductor Devices, Mobile Devices Containing Same (Taiwan Semiconductor Manufacturing Company).

Heim, Payne & Chorush: Completed 2021-2023. Technical evaluation and consulting representing *Arigna Technology Limited* with regards to IPR2021-01321 (*Volkswagen*) and IPR2021-01382 (*Infineon*).

Quinn Emanuel Urquhart & Sullivan: Believed complete 2021-2023. Technical evaluation and consulting representing *Hanwha* with regards to ITC Inv. No. 337-TA-1271.

Ropes and Gray: Completed 2021-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.*

Lawrence and Phillips: Completed 2021-2022. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.* with regards to *inter partes reviews* (IPRs) filed by Samsung.

Wolf Greenfield: Completed 2020-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.* with regards to *inter partes reviews* (IPRs) filed by Micron.

Hueston Henningan: Completed 2020-22. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.*

Skadden Arps: Initiated 2020 and on-going. Technical consulting for the *Audit Committee of the Intel Board of Directors* on matters related to Technology Development.

PARADIM: Initiated 2016 and on-going. PARADIM's mission is to create new interface materials with unprecedented properties for the next generation of electronic devices. Dr. Kuhn is a member of the External Advisory Committee. In this role, Dr. Kuhn provides technical and management support with regards to PARADIM operations.

Quinn Emanuel Urquhart & Sullivan: Completed, 2020-2021. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.*

Susman Godfrey: Completed 202-2023. Technical evaluation and consulting with regards to *Arigna Technology Limited* on matters related to CMOS transistor design.

Womble Bond Dickinson: Completed, 2020. Technical consulting for KIPB LLC (formerly KAIST IP US LLC) on an *ex parte reexamination* ("EPR") proceeding in the United States Patent and Trademark Office with regards to patent 6,885,055.

Womble Bond Dickinson: Completed, 2019-2020. Technical evaluation and consulting in the matter of *KIPB LLC v. Samsung Electronics et al*. Dr. Kuhn supported this litigation for the plantiff as an expert witness, including completion of the Infringement and Rebuttal Reports, as well as completing a deposition conducted on the contents of the Infringement and Rebuttal Reports. This case was settled out of court in September 2020.

Lathrop Gage: Completed, 2018-2020. Technical evaluation and consulting for KIPB LLC (formerly KAIST IP US LLC) on Korean Patent 10-0458288 (Korean counterpart to US 6,885,055).

Ropes & Gray: Completed, 2018. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Qualcomm Inc. et al.*

GlaserWeil: Completed, 2016-2018. Technical evaluation and consulting in the matter of *KAIST IP US LLC v. Samsung Electronics Co., Ltd., Case No. 2:16-cv-01314.* Dr. Kuhn supported this litigation for the plantiff as an expert witness. This included IPR proceedings (a total of 6 IPRs were presented to the PTO in this case). This also included completion and submission of the Claim Construction Declaration, the Infringement Report, and the Rebuttal Report, as well as depositions conducted on the contents of these Reports. This case went to trial June 11-15, where Dr. Kuhn presented both Direct testimony on infringement (6/12/18) and Rebuttal (6/14/18) testimony on validity.

yoR Labs Inc.: Completed. 2015-2017. yoR Labs is a medical instrumentation start-up, focusing on non-invasive medical imaging instrumentation. Dr. Kuhn served first as a member of the External Advisory Committee and later as a member of the Board of Directors. In this role, Dr. Kuhn provided technical and management support with regards to yoR labs operations.

Oregon State University, Department of Electrical Engineering and Computer Science: Completed. 2015 to 2018: Professor-courtesy. Prof. Kuhn's role was establishment of long-term research programs in the area advanced CMOS technology and post-CMOS technology.

FORMER ROLES (2014 and PRIOR)

Intel, Portland, OR, (advanced development / research) 2008-2014 (retired in 2014)
Grade level: 12 (Fellow)
Manager: Mike Mayberry, VP

Dr. Kuhn's role was researching advanced device architectures for Intel processes in the 5-10 year time frame. While much of her work as an Intel Fellow remains proprietary, some of the public domain aspects are captured in her book *CMOS and Beyond: Logic Switches for Terascale Integrated Circuits* (Cambridge, 2015) and her paper "Considerations for Ultimate CMOS Scaling," (IEEE Trans. on Elec. Dev., Vol: 59 , No: 7, 2012 , pp. 1813 – 1828 which won the Paul Rappaport Award). She received an Intel IAA in 2008 for her work on the TriGate transistor.

Intel, Portland, OR, (45nm Device technology manager in pathfinding) 2004-2008
Grade level: 10/11 (Principal Engineer / Sr. Principal Engineer)
Manager: Mark Bohr, Senior Intel Fellow / Kaizad Mistry, VP

Dr. Kuhn's role was as device technology manager of the pathfinding team responsible for the high-k metal-gate transistor architecture for Intel's 45nm microprocessor processor technology. She received an Intel IAA in 2006 for her work on high-k metal-gate.

Intel, Portland, OR, (90nm communication process manager) 2001-2004+
Grade level: 9/10 (Sr. Engineer / Principal engineer)
Manager: Scott Thompson (was Intel Fellow at the time, now a professor at Univ. of Florida).

Dr. Kuhn's role in this time frame was Process Program Manager of the team responsible for Intel's 90nm communications process technology. Over a 4-year period, this team developed a derivative analog/RF technology (including a SiGe BJT) on top of Intel's premium 90nm microprocessor process.

Other Intel experience:

Intel, Portland, OR, (130nm front-end integration engineer) 1998-2001
Intel, Portland, OR, (0.35um front-end integration engineer) 1997-1998
Grade level: 7-9 (Sr. engineering grades)

During the 130nm generation, Dr. Kuhn was an integration engineer responsible for the isolation section of the flow. 130nm was the last of the "classic" CMOS generations, and her work in that generation was updating the isolation process. She had the satisfaction of watching the work she did in the 130nm successfully scale through 90nm, 65nm, 45nm, and 32nm, with little change in the base process.

Dr. Kuhn joined Intel on the 0.35um generation as a sustaining integration engineer in F15. She was responsible for the silicide section of the flow. Additionally, she participated in the DIVD camera chip project (Intel's historical project to build CMOS camera chips).

Other relevant experience:

Univ. of Washington, Seattle, WA (Assoc. Prof., Ass't. Prof., Res. Ass't. Prof.), 1987-1997

Dr. Kuhn held faculty positions at the University of Washington (in Seattle) for roughly a decade in the order of Research Assistant Professor (Materials Science and Engineering), Assistant Professor (Electrical and Computer Engineering), and Associate Processor (Electrical and Computer Engineering). She left the University in 1997 as a tenured Associate Professor of Electrical and Computer Engineering. While at the Univ. of Washington, she achieved distinction in both research and teaching.

Highlights include:

- University of Washington, Distinguished Teaching Award, 1995 (UW's highest level of achievement for a faculty member)
- NSF Presidential Young Investigator award, 1991-6 (The National Science foundation is the most prestigious funding agency for faculty and the NSF PYI award is the most prestigious national level award for junior faculty).
- Single-author on a textbook, Laser Engineering, Prentice-Hall, 1998, ISBN 0-02-366921-7 (this is a mezzanine text discussing the theory and practice of building conventional and diode laser systems).

BOOKS

Laser Engineering, (sole author) Prentice-Hall, 1998, ISBN 0-02-366921-7

CMOS and Beyond: Logic Switches for Terascale Integrated Circuits (Co-editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015, ISBN 978-1107043183).

BOOK CHAPTERS

"The Magic of MOSFET Manufacturing,", Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8.

Chapter 1, CMOS and Beyond CMOS: Scaling Challenges" (Book title: "High Mobility Materials for CMOS Applications", Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616) .

AWARDS:

Elected to the National Academy of Engineering (2023)
IEEE Frederik Philips Award (2016)
IEEE Paul Rappaport Award (2013)
IEEE Fellow (2011)

Intel Achievement Awards (Intel's highest technical award): IAA 2006 (for HiK-MG) and IAA 2008 (for key contributions to Intel's 22nm TriGate technology)
Intel Divisional Awards: Turbo operation (2009), RF Vccmin (2007), TCC (2005), SCD 1213.4 SCD/ICG (2004), LAD NW/Ophir A-1 (2003), SiGe BJT (2002), Hitachi etch (2002), 2um2SRAM (2001), Gamma Test chip (2000), Certification P854.6 (1999), F15 ISO 9000 (1998)
Academic Engineer of the Year Award, Puget Sound Engineering Council, 1996
University of Washington, Distinguished Teaching Award, 1995
College of Engineering, Outstanding Faculty Achievement Award, 1994
NSF Presidential Young Investigator award, 1991-6
NSF Research Initiation Award, 1989-91
IBM Graduate Fellowship, 1983-5
Hertz Graduate Fellowship, 1982-3
National Merit Scholar, 1976-80

JOURNAL PUBLICATIONS:

49. "First principles modeling of defects in the Al2O3 /In0.53Ga0.47 As system", G. Greene-Diniz, K. Kuhn, P. Hurley, and J. Greer, J. Appl. Phys., Vol. 121, No. 7, Jan. 2017.

48. "Doping top-down e-beam fabricated germanium nanowires using molecular monolayers," B. Long, G. Alessio Verni, J. O'Connell, M. Shayesteh, A. Gangnaik, Y.M. Georgiev, P. Carolan, D. O'Connell, K.J. Kuhn, S.B. Clendenning, R. Nagle, R. Duffy, and J.D. Holmes, Materials Science in Semiconductor Processing, Vol. 62, May 2017, pp. 196-200.

47. "Device Physics Modeling of Surfaces and Interfaces from an Induced Gap State Perspective," J. Wager and K. Kuhn, Critical Reviews in Solid State and Materials Science, Oct. 4, 2016.

46. "Adhesion Limits and Design Criteria for Nanorelays", Kevin L. Lin, Graham L. W. Cross, Peter Gleeson, Johann P. de Silva, Alejandro Levander, Jorge A. Muñoz, Chytra Pawashe, Alexis Potie, Patrick Theofanis, John J. Boland, and Dr. Kuhn J. Kuhn, IEEE Trans. on Elec. Dev., Vol. 63, No. 1, Jan. 2016, 465-470.

45. Distributive Quasi-Ballistic Drift Diffusion Model Including Effects of Stress and High Driving Field, Roza Kotlyar,, Rafael Rios, Cory E. Weber, Thomas D. Linton, Mark Armstrong and Dr. Kuhn Kuhn, IEEE Trans. on Elec. Dev., Vol. 62, No. 3, March 2015. Pp. 743-750.

44. Improved MOSFET characterization technique for single channel length, scaled transistors, Ferdousi, F., Rios, R., Kuhn K.J. Solid State Electronics, Vol. 104, pp. 44-6, Feb. 2015

43. Capacitance and Conductance for an MOS System in Inversion, with Oxide Capacitance and Minority Carrier Lifetime Extractions, Monaghan, S. O'Connor, E., Rios, R., Ferdousi, F., Floyd, L., Ryan, E., Cherhaoui, K., Povey, I.M., Kuhn, K.J., Hurley, P.K. IEEE Transactions on Electron Devices, Vol. 61, No. 12, pp. 4176-85, Dec. 2014.

42. First principle-based analysis of single-walled carbon nanotube and silicon nanowire Junctionless transistors, Ansari, L., Feldman, B., Faga, G., Martinez, L.C., Haverty, M.G., Kuhn, K.J., Shankar, S., Greer, J.C., IEEE Transactions on Nanotechnology, Vol. 12, No. 6, pp. 1075-81, Nov. 2013.

41. Scaling Limits of Electrostatic Nanorelays, Pawashe, C., Lin, K., Kuhn, K.J., IEEE Transactions on Electron Devices, Vol. 60, No. 9, pp. 2936-42, Sept. 2013,

40. Bandgap engineering of group IV materials for complementary n and p tunneling field effect transistors, Kotlyar, R.; Avci, U.E.; Cea, S.; Rios, R.; Linton, T.D.; Kuhn, K.J.; Young, I.A., Applied Physics Letters, v 102, n 11, March 18, 2013.

39. Effects of alternating current voltage amplitude and oxide capacitance on mid-gap interface state defect density extractions in InGaAs capacitors, Monaghan, Scott ; O'Connor, Eamon ; Povey, Ian M. ; Sheehan, Brendan J. ; Cherkaoui, Karim ; Hutchinson, Barry J. A. ; Hurley, Paul K. ; Ferdousi, Fahmida ; Rios, Rafael ; Kuhn, Dr. Kuhn J. ; Rahman, Anisur, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, Vol: 31 , No: 1, 2013, pp: 01A119 - 01A119-8.

38. Considerations for Ultimate CMOS Scaling, Dr. Kuhn J. Kuhn, invited review paper, IEEE Trans. on Elec. Dev., Vol: 59 , No: 7, 2012 , pp. 1813 – 1828 (won the Paul Rappaport Award)

37. Does the low hole transport mass in <110> and <111> Si nanowires lead to mobility enhancements at high field and stress: a self-consistent tight-binding study, R. Kotlyar, T. D. Linton, R. Rios, M. D. Giles, S. M. Cea, K. J. Kuhn, Michael Povolotskyi, Tillmann Kubis, and Gerhard Klimeck, Vol: 111 , No: 12, 2012, pp 123718 - 123718-11

36. Comparison of Junctionless and Conventional Trigate Transistors With Lg Down to 26 nm, Rios, R.; Cappellani, A.; Armstrong, M.; Budrevich, A.; Gomez, H.; Pai, R.; Rahhal-orabi, N.; Kuhn, K., IEEE Electron Device Letters, Vol. 32, No. 9, 2011, pp. 1170 - 1172

35. Process Technology Variation, Kuhn, K.J.; Giles, M.D.; Becher, D.; Kolar, P.; Kornfeld, A.; Kotlyar, R.; Ma, S.T.; Maheshwari, A.; Mudanai, S., IEEE Transactions on Electron Devices, Aug. 2011, vol.58, no.8, pp. 2197-208.

34. Moore's crystal ball: Device physics and technology past the 15nm generation, Kuhn, K.J., Microelectronic Engineering, July 2011, vol.88, no.7, pp. 1044-9.

33. Variability in nanoscale CMOS technology, Kuhn, K.J., K. Sci. China Inf. Sci. (2011) 54: 936. doi:10.1007/s11432-011-4219-6 (May 5, 2011).

32. Compressive Uniaxial Stress Bandstructure Engineering for Transferred-Hole Devices, Kotlyar, R.; Giles, M.D.; Mudanai, S.P.; Kuhn, K.J.; Cea, S.M.; Linton, T.D.; Pillarisetty, R.; IEEE Elec. Dev. Lett. Vol. 31, No. 8, 2010, pp. 878-880.

31. Managing process variation in Intel's 45 nm CMOS technology, Kuhn, K., Kenyon, C., Kornfeld, A., et al. Intel Technology Journal Volume: 12 Issue: 2 Pages: 93-4 Published: 17 June 2008

30. Analytical Modeling of Output Conductance in Long-Channel Halo-Doped MOSFETs, Electron Devices, Mudanai, S.; Shih, W.-K.; Rios, R.; Xi, X.; Rhew, J.-H.; Kuhn, K.; Packan, P.;, IEEE Transactions on Volume 53, Issue 9, Sept. 2006 Page(s):2091 - 2097

29. A 90-nm logic technology featuring strained-silicon, Thompson, S.E.; Armstrong, M.; Auth, C.; Alavi, M.; Buehler, M.; Chau, R.; Cea, S.; Ghani, T.; Glass, G.; Hoffman, T.; Jan, C.-H.; Kenyon, C.; Klaus, J.; Kuhn, K.; Zhiyong Ma; Mcintyre, B.; Mistry, K.; Murthy, A.; Obradovic, B.; Nagisetty, R.; Phi Nguyen; Sivakumar, S.; Shaheed, R.; Shifren, L.; Tufts, B.; Tyagi, S.; Bohr, M.; El-Mansy, Y., IEEE Transactions on Electron Devices, vol.51, no.11, Nov. 2004. p. 1790-7.

28. Integration of mixed-signal elements into a high-performance digital CMOS process. Kuhn, K.J.; Ahmed, S.; Vandervoom, P.; Murthy, A. Intel Technology Journal, no.2, 2002

27. Elevated temperature performance of pseudomorphic AlGaAs/InGaAs MODFETs. Zurek, S.J.; Darling, R.B.; Kuhn, K.J.; Foisy, M.C. IEEE Transactions on Electron Devices, vol.45, no.1, Jan. 1998. p. 2-8

26. Synthetic wide bandpass X-ray polarizers. Cross, J.O.; Bennett, B.R.; Bell, M.I.; Kuhn, K.J. Applied Physics Letters, vol.70, no.17, 28 April 1997. p. 2224-6

25. Electro-optic polymer light modulator based on surface plasmon resonance. Jung, C.; Yee, S.; Kuhn, K. Applied Optics, vol.34, no.6, 20 Feb. 1995. p. 946-9

24. A "hands-on" course in consumer electronics design. Hannaford, B.; Kuhn, K. Mechatronics, vol.5, no.7, Oct. 1995. p. 753-62 Journal Paper

23. Finite element solutions to GaAs-AlAs quantum wells with connection matrices at heterojunctions. Li, T.L.; Kuhn, K.J. Journal of Computational Physics, vol.115, no.2, Dec. 1994. p. 288-95

22. Integrated optics waveguide modulator based on surface plasmon resonance. Jung, C.; Yee, S.; Kuhn, K. Journal of Lightwave Technology, vol.12, no.10, Oct. 1994. p. 1802-6

21. Effects of spin-orbit interaction on the envelope-function equations for semiconductor heterostructures. Li, T.L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.50, no.12, 15 Sept. 1994. p. 8589-601

20. Effects of mass discontinuity on the numerical solutions to quantum wells using the effective mass equation. Li, T.L.; Kuhn, K.J. Journal of Computational Physics, vol.110, no.2, Feb. 1994. p. 292-300

19. Validity of the connection-matrix approach to GaAs-Al/sub x/Ga/sub 1-x/As quantum wells. Li, T.L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.49, no.4, 15 Jan. 1994. p. 2608-14

18. Optical properties due to intersubband transitions in n-type quantum wells including the effects of the exchange interaction. Sengers, A.J.; Tsang, L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.48, no.20, 15 Nov. 1993. p. 15116-22

17. Band-offset ratio dependence on the effective-mass Hamiltonian based on a modified profile of the GaAs-Al/sub x/Ga/sub 1-x/As quantum well. Li, T.L.; Kuhn, K.J. Physical Review B (Condensed Matter), vol.47, no.19, 15 May 1993. p. 12760-70

16. Use of active loads with MSM photodetectors in digital GaAs MESFET photoreceivers. Darling, R.B.; Youn, H.J.; Kuhn, K.J. Journal of Lightwave Technology, vol.10, no.11, Nov. 1992. p. 1597-605

15. Mobility of strained and dislocated In/sub x/Ga/sub 1-x/As semiconductor material. Kuhn, K.J.; Darling, R.B. IEEE Transactions on Electron Devices, vol.39, no.6, June 1992. p. 1288-94

14. Dislocation scattering in n-type modulation doped Al/sub 0.3/Ga/sub 0.7/As/In/sub x/Ga/sub 1-x/As/Al/sub 0.3/Ga/sub 0.7/As quantum wells. Zhao, D.; Kuhn, K.J. IEEE Transactions on Electron Devices, vol.38, no.12, Dec. 1991. p. 2582-9

13. Free carrier induced changes in the absorption and refractive index for intersubband optical transitions in Al/sub x/Ga/sub 1-x/As/GaAs/Al/sub x/Ga/sub 1-x/As quantum wells. Kuhn, K.J.; Iyengar, G.U.; Yee, S. Journal of Applied Physics, vol.70, no.9, 1 Nov. 1991. p. 5010-17

12. Electric field effects in AlGaAs-GaAs symmetric and asymmetric coupled quantum wells. Juang, C.; Kuhn, K.J.; Darling, R.B. IEEE Journal of Quantum Electronics, vol.27, no.9, Sept. 1991. p. 2122-8

11. Effect of etch treatment prior to Schottky contact fabrication on In/sub 0.05/Ga/sub 0.95/As. Johnson, M.J.; Kuhn, K.J.; Darling, R.B. Applied Physics Letters, vol.58, no.17, 29 April 1991. p. 1893-5

10. An enhanced and linear Stark shift in n-i-n AlGaAs/GaAs symmetric and asymmetric coupled quantum wells. Kuhn, K.J.; Cheng Juang; Darling, R.B. Journal of Applied Physics, vol.69, no.5, 1 March 1991. p. 3135-41

9. AlGaAs-GaAs multiple-quantum-well spectrally tunable photoconductors. Youn, H.J.; Darling, R.B.; Kuhn, K.J. IEEE Photonics Technology Letters, vol.3, no.2, Feb. 1991. p. 159-61

8. Effect of AlGaAs window and buffer layers on the response characteristics of GaAs photoconductive detectors. Youn, H.J.; Darling, R.B.; Kuhn, K.J. Applied Physics Letters, vol.57, no.19, 5 Nov. 1990. p. 2001-3

7. Selective etching of GaAs and Al/sub 0.30/Ga/sub 0.70/As with citric acid/hydrogen peroxide solutions. Juang, C.; Kuhn, K.J.; Darling, R.B. Journal of Vacuum Science & Technology B (Microelectronics Processing and Phenomena), vol.8, no.5, Sept.-Oct. 1990. p. 1122-4

6. Stark shift and field-induced tunneling in Al/sub x/Ga/sub 1-x/As/GaAs quantum-well structures. Juang, C.; Kuhn, K.J.; Darling, R.B. Physical Review B (Condensed Matter), vol.41, no.17, 15 June 1990. p. 12047-53

5. An indium-free substrate holder for radiative heating of quarter-wafer molecular-beam epitaxy samples. Kuhn, K.J. Review of Scientific Instruments, vol.61, no.1, pt.1, Jan. 1990. p. 184-5

4. Variation in GaAs surface oxide desorption temperature as a function of shuttered aluminum oven temperature. Kuhn, K.J.; Pubanz, G.A. Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films), vol.7, no.6, Nov.-Dec. 1989. p. 3265-8

3. Static gas conduction cooled slab geometry Nd:glass laser. Reed, M.; Kuhn, K.; Unternahrer, J.; Byer, R.L. IEEE Journal of Quantum Electronics, vol.QE-21, no.5, May 1985. p. 412-14

2. The slab geometry laser. I. Theory. Eggleston, J.M.; Kane, T.J.; Kuhn, K.; Unternahrer, J. IEEE Journal of Quantum Electronics, vol.QE-20, no.3, March 1984. p. 289-301

1. Implementation of Distributed Microprocessor Systems in Custom Heavy Trucks, K.J. Kuhn, 1979-80 IEEE Student Papers, Vol. TT0114 IEEE, pg. 334-342.

CONFERENCE PUBLICATIONS

54. Bias temperature instability variation on SiON/Poly, HK/MG and trigate architectures, C. Prasad, M. Agostinelli, J. Hicks, S. Ramey, C. Auth, K. Mistry, S. Natarajan, P. Packan, I. Post, S. Bodapati, M. Giles, S. Gupta, S. Mudani and K. Kuhn, 2014 IEEE International Reliability Physics Symposium (IRPS), June 2014.

53. Semiconductors Stand Aside, the Age of Metals is Here! K. Kuhn, A. Sanchez, C. George, R. Rios, J. Clarke, J. Greer, Lester Eastman Conference, Cornell, May 2014.

52. The ultimate CMOS device and beyond, Kuhn, K.J. ; Avci, U. ; Cappellani, A. ; Giles, M.D. ; Haverty, M. ; Seiyon Kim ; Kotlyar, R. ; Manipatruni, S. ; Nikonov, D. ; Pawashe, C. ; Radosavljevic, M. ; Rios, R. ; Shankar, S. ; Vedula, R. ; Chau, R. ; Young, I. 2012 IEEE International Electron Devices Meeting (IEDM), pp. 171-174.

51. Understanding the feasibility of scaled III–V TFET for logic by bridging atomistic simulations and experimental results, Avci, U.E. ; Hasan, S. ; Nikonov, D.E. ; Rios, R. ; Kuhn, K. ; Young, I.A., Symposium on VLSI Technology (VLSIT), 2012, pp: 183 – 184.

50. Beyond the Planar Transistor: Progress in Next Generation Switches, K. Kuhn, Int'l Symposium on Adv. Gate. Stack Technology, Oct. 19-21, 2011 New York

49. Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation, K. Kuhn, INFOS 2011 (June 22, 2011, France)

48. Comparison of power and performance for the TFET and MOSFET and considerations for P-TFET, Avci, U.E.; Rios, R.; Kuhn, K.J.; Young, I.A., IEEE Conference on Nanotechnology (IEEE-NANO), 2011 11th, pp. 869 – 872

47. Comparison of performance, switching energy and process variations for the TFET and MOSFET in logic, Avci, U.E.; Rios, R.; Kuhn, K.; Young, I.A., 2011 Symposium on VLSI Technology (VLSIT), 2011 , pp. 124 – 125

46. CMOS scaling for the 22nm node and beyond: Device physics and technology, Kuhn, K.J., 2011 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2011 , pp. 1 – 2

45. Past, Present and Future: SiGe and CMOS Transistor Scaling. K. J. Kuhn, A. Murthy, R. Kotlyar, and M. Kuhn, ECS 2010, Oct. 10, Las Vegas, CA, USA.

44. Peering into Moore's Crystal Ball, Transistor Scaling beyond the 15nm node, K. J. Kuhn, Int'l Symposium on Adv. Gate. Stack Technology, Sept. 29th, 2010; Albany, NY, USA.

43. CMOS transistor scaling past 32nm and implications on variation, K. Kuhn, 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), ASMC'2010, 11-13 July 2010, San Francisco, CA, USA, pp. 241-246.

42. Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond, K. Kuhn, Nikkei Electronics Symposium, June 29th, 2010.

41. Technology options for 22nm and beyond, K. Kuhn, Technology, Kuhn, K.J.; Liu, M.Y.; Kennel, H.; 2010 International Workshop on Junction Technology (IWJT), IWJT'10, 10-11 May 2010, Shanghai, China, pp. 1-6.

40. CMOS technology beyond 22nm, K. Kuhn, 12th IEEE International Workshop on Cellular Nanoscale Neetworks and Applications, CNNA 2010, February 3-5 Berkeley, California

39. Transistor architecture: 45nm and beyond, K. Kuhn, Intel European Research and Innovation Conference, 8-10th September 2009, Leixlip, Co. Kildare.

38. Moore's Law Past 32nm: The Challenges in Physics and Technology Scaling, K. Kuhn, Solid State Devices and Materials Conference (SSDM), September 18, 2009, Sendai, Japan.

37. CMOS scaling beyond 32 nm: challenges and opportunities, Kuhn, K.J., 2009 46th ACM/IEEE Design Automation Conference (DAC), 26-31 July 2009, San Francisco, CA, USA, Pages: 310-13 Published: 2009

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2. Progress in slab geometry solid state lasers. Eggleston, J.M.; Kane, T.; Kuhn, K.; Byer, R.L. Proceedings of the SPIE - The International Society for Optical Engineering, vol.335, 1982. p. 104-8 Conference Paper

1. Implementation of distributed microprocessor systems in custom heavy trucks. Kuhn, K.J. In: Wescon/80 Conference Record. El Segundo, CA, USA: Electron. Conventions, 1980. p. SS2-3/1-8 Conference Paper.

PATENTS

	PAT. NO.	Title
1	11,302,777	Integration methods to fabricate internal spacers for nanowire devices
2	11,195,919	Method of fabricating a semiconductor device with strained SiGe fins and a Si cladding layer
3	11,139,400	Non-planar semiconductor device having hybrid geometry-based active region
4	11,024,714	Nanowire transistor fabrication with hardmask layers
5	10,991,799	Silicon and silicon germanium nanowire structures
6	10,825,752	Integrated thermoelectric cooling
7	10,804,357	Integration methods to fabricate internal spacers for nanowire devices
8	10,636,871	Silicon and silicon germanium nanowire structures
9	10,593,804	Non-planar semiconductor device having hybrid geometry-based active region
10	10,586,868	Non-planar semiconductor device having hybrid geometry-based active region
11	10,580,899	Nanowire structures having non-discrete source and drain regions
12	10,580,860	Integration methods to fabricate internal spacers for nanowire devices
13	10,535,770	Scaled TFET transistor formed using nanowire with surface termination
14	10,424,580	Semiconductor devices having modulated nanowire counts
15	10,283,589	Integration methods to fabricate internal spacers for nanowire devices
16	10,121,861	Nanowire transistor fabrication with hardmask layers
17	10,121,856	Integration methods to fabricate internal spacers for nanowire devices
18	10,115,822	Methods of forming low band gap source and drain structures in microelectronic devices
19	10,109,711	CMOS FinFET device having strained SiGe fins and a strained Si cladding layer on the NMOS channel
20	10,074,573	CMOS nanowire structure
21	10,074,357	Integrated acoustic phase array
22	10,026,829	Semiconductor device with isolated body portion
23	9,978,636	Isolated and bulk semiconductor devices formed on a same bulk substrate
24	9,947,805	Nanowire-based mechanical switching device
25	9,935,205	Internal spacers for nanowire transistors and method of fabrication thereof
26	9,935,107	CMOS FinFET device with dual strained cladding layers on relaxed SiGe fins, and method of fabricating the same
27	9,926,193	Magnetic nanomechanical devices for stiction compensation

28	9,911,835	Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs
29	9,893,167	Integration methods to fabricate internal spacers for nanowire devices
30	9,882,053	Molded dielectric fin-based nanostructure
31	9,859,368	Integration methods to fabricate internal spacers for nanowire devices
32	9,825,130	Leakage reduction structures for nanowire transistors
33	9,812,524	Nanowire transistor devices and forming techniques
34	9,691,843	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition
35	9,680,013	Non-planar device having uniaxially strained semiconductor body and method of making same
36	9,673,302	Conversion of strain-inducing buffer to electrical insulator
37	9,614,060	Nanowire transistor with underlayer etch stops
38	9,608,059	Semiconductor device with isolated body portion
39	9,595,581	Silicon and silicon germanium nanowire structures
40	9,583,602	Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs
41	9,583,491	CMOS nanowire structure
42	9,564,522	Nanowire structures having non-discrete source and drain regions
43	9,559,160	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition
44	9,508,796	Internal spacers for nanowire transistors and method of fabrication thereof
45	9,484,447	Integration methods to fabricate internal spacers for nanowire devices
46	9,472,613	Conversion of strain-inducing buffer to electrical insulator
47	9,425,212	Isolated and bulk semiconductor devices formed on a same bulk substrate
48	9,412,872	N-type and P-type tunneling field effect transistors (TFETs)
49	9,385,221	Nanowire transistor with underlayer etch stops
50	9,362,074	Nanowire-based mechanical switching device
51	9,355,242	Method and apparatus for managing and accessing personal data
52	9,343,559	Nanowire transistor devices and forming techniques
53	9,287,576	Self-powered internal medical device
54	9,258,114	Quantum key distribution (QSD) scheme using photonic integrated circuit (PIC)
55	9,224,810	CMOS nanowire structure
56	9,183,829	Integrated accoustic phase array

57	9,129,829	Silicon and silicon germanium nanowire structures
58	9,129,827	Conversion of strain-inducing buffer to electrical insulator
59	9,105,344	Shut-off mechanism in an integrated circuit device
60	9,087,863	Nanowire structures having non-discrete source and drain regions
61	9,064,944	Nanowire transistor with underlayer etch stops
62	9,029,221	Semiconductor devices having three-dimensional bodies with modulated heights
63	9,012,284	Nanowire transistor devices and forming techniques
64	8,890,120	Tunneling field effect transistors (TFETs) for CMOS approaches to fabricating N-type and P-type TFETs
65	8,853,741	Junctionless accumulation-mode devices on decoupled prominent architectures
66	8,766,372	Copper-filled trench contact for transistor performance improvement
67	8,753,942	Silicon and silicon germanium nanowire structures
68	8,558,279	Non-planar device having uniaxially strained semiconductor body and method of making same
69	8,507,948	Junctionless accumulation-mode devices on prominent architectures, and methods of making same
70	8,487,348	Methods and apparatus to reduce layout based strain variations in non-planar transistor structures
71	8,269,283	Methods and apparatus to reduce layout based strain variations in non-planar transistor structures
72	8,258,057	Copper-filled trench contact for transistor performance improvement
73	7,999,607	Power switches having positive-channel high dielectric constant insulated gate field effect transistors
74	7,888,710	CMOS fabrication process utilizing special transistor orientation
75	7,737,770	Power switches having positive-channel high dielectric constant insulated gate field effect transistors
76	7,312,485	CMOS fabrication process utilizing special transistor orientation
77	6,627,506	Thin tensile layers in shallow trench isolation and method of making same
78	6,368,931	Thin tensile layers in shallow trench isolation and method of making same
79	4,617,669	Method and apparatus for pumping lasant slabs
80	4,563,763	Method and apparatus for cooling a slab laser

INVITED TECHNICAL PRESENTATIONS/SEMINARS :

Invited panel, IEDM, Variation and the End of the World, December, 2013.

Keynote, The End of Scaling?, ICTC, December 2013.

Invited seminar, CMOS and Beyond, Portland State University, October, 2013.

Keynote panel, CMOS and Beyond: Future Device Technology, ENF 2013, Ireland, June 2013.

Invited seminar, CMOS and Beyond: Future Device Technology for the Mobile World, IDF, May 2013.

Invited Workshop, The Future is Already Here: Evolving Concepts in Device and Materials Technology, AMAT, March 2013.

Invited paper, "The Ultimate CMOS Device and Beyond," IEDM 2012, San Francisco.

Invited talk, Beyond Simply Small: Progress in Advanced Transistor Architectures, Cornell, November 2012.

Invited seminar, Demystifying Moore's Law How it Really Works!, IDF, Sept. 2012, San Francisco.

Invited talk, The Ultimate CMOS Device and Beyond, Ireland, April 2012.

Keynote: "MOS scaling for the 22nm node and beyond: Device physics and technology," April 24, 2011, Taiwan, VLSI-TSA

Plenary: "Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation," INFOS 2011 (June 22, 2011, France)

Keynote: "Beyond the Planar Transistor: Progress in Next Generation Switches," Int'l Symposium on Adv. Gate. Stack Technology, Oct. 19-21, 2011 New York

Invited seminar - "Polishing Moore's Crystal Ball: Advanced Transistor Architectures …and Beyond," K. Kuhn, March 30th. 2011, MIT, MTL seminar series.

Invited seminar - "Emerging Devices: Moore's Law and Advanced Transistor Architectures," K. Kuhn, Varian Technology Symposium, March 31st. 2011.

Keynote: "Scaling Electronics:Trends and Bottlenecks," K. Kuhn, April 4th. 2011, MIT Microphotonics meeting.

Invited seminar - "Gazing into Moore's Crystal Ball: Transistor Scaling after the 15nm node," K. Kuhn, Feb. 17th, 2010, Berkeley.

IEDM 2010 Short Course chair for 15nm technology, December 2010.

Plenary: Past, Present and Future: SiGe and CMOS Transistor Scaling, ECS 2010, Oct. 10, Las Vegas, CA, USA.

Keynote: Peering into Moore's Crystal Ball, Transistor Scaling beyond the 15nm node, Int'l Symposium on Adv. Gate. Stack Technology, Sept. 29th, 2010; Albany, NY, USA.

Plenary: CMOS transistor scaling past 32nm and implications on variation, 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), ASMC'2010,11-13 July 2010, San Francisco, CA, USA

Keynote: Technology options for 22nm and beyond, K. Kuhn, 2010 International Workshop on Junction Technology (IWJT), IWJT'10, 10-11 May 2010, Shanghai, China, pp. 1-6.

Invited seminar: Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond, Nikkei Electronics Symposium / June 29th, 2010.

Plenary - CMOS technology beyond 22nm, K. Kuhn, 12th IEEE International Workshop on Cellular Nanoscale Neetworks and Applications, CNNA 2010, February 3-5 Berkeley, California

Keynote - Transistor architecture: 45nm and beyond, K. Kuhn, Intel European Research and Innovation Conference, 8-10th September 2009, Leixlip, Co. Kildare.

Plenary - Moore's Law Past 32nm: The Challenges in Physics and Technology Scaling, K. Kuhn, Solid State Devices and Materials Conference (SSDM), September 18, 2009, Sendai, Japan.

Invited talk - CMOS scaling beyond 32 nm: challenges and opportunities, Kuhn, K.J., 2009 46th ACM/IEEE Design Automation Conference (DAC), 26-31 July 2009, San Francisco, CA, USA, Pages: 310-13 Published: 2009

Keynote - Variation in 45nm and Implications for 32nm and Beyond, K. Kuhn, NMI International Conference on CMOS Variability, 12th & 13th May 2009, London, UK.

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Invited – International Electron Device meeting – short course.
http://download.intel.com/pressroom/pdf/kkuhn/Kuhn_22nm_Device.pdf

Invited seminar - "45nm High-k + Metal Gate Logic Technology," K. Kuhn, May 2008, MIT, MTL laboratory.

Invited talk - Reducing variation in advanced logic technologies: approaches to process and design for manufacturability of nanoscale CMOS, Kuhn, K.J., 2007 IEEE International Electron Devices Meeting - IEDM '07, 10-12 December 2007, Washington, DC, USA, IEDM '07 Pages: 471-4

Invited seminar - "CMOS Transistor Architecture Challenges and Opportunities," K. Kuhn, September 2005, MIT, MTL laboratory.

Keynote - "Nanotechnology Challenges and Opportunities," K. Kuhn, January 2005, MIT, MTL laboratory.

Invited seminar - "Transistor Scaling and its Impact on Analog/RF Device Performance", Dr. Kuhn Kuhn, March 2005, Stanford University, invited seminar.

Invited seminar - "Advanced transistor architecture approaches and their implications for device and circuit performance," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2004.

Invited seminar - "Moore's Law meets Materials Science", Dr. Kuhn Kuhn, September 2004, University of Washington.

Invited seminar - "Centrino, convergence of computing and communications," November 2003, Dr. Kuhn Kuhn, Stanford University, invited seminar.

Invited seminar - "Challenges in the parallel development of the 90nm communications (121x) and microprocessor (1262) process technologies," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2003.

Invited seminar - "RF/analog integration with 90nm digital CMOS", Dr. Kuhn Kuhn, MIT invited seminar, March 2003

Invited seminar - "Femtosecond pulse laser technology", Dr. Kuhn Kuhn, Oregon State University, March 10, 1997.

Invited talk- "Symbolic Solvers and their impact on engineering education", Dr. Kuhn Kuhn, Fifth annual conference on the teaching of mathematics, Baltimore, Maryland, June 21, 1996.